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POWER QUALITY ENHANCEMENT AT DISTRIBUTION LEVEL UTILIZING THE UNIFIED POWER QUALITY CONDITIONER (UPQC)

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AMÉLIORATION DE QUALITÉ DE L'ONDE AU NIVEAU DE DISTRIBUTION EN UTILISANT LE CONDITIONNEUR UNIFIÉ DE QUALITÉ DE L'ONDE (UPQC)

KHADKIKAR, Vinod

RÉSUMÉ

Les équipements basés sur de l'électronique de puissance émergent rapidement telle une composante essentielle aux systèmes de distribution à haute puissance modernes. Les équipements de conversion de la puissance qui bénéficient de cette technologie offrent un éventail de possibilités et permettent entre autre une flexibilité de contrôle, une réduction des coûts, une optimisation des l'espace et des performances, etc. D'un autre côté, l'opération de ces équipements peut entraîner certains des plus sérieux problèmes de la qualité de l'onde tels une consommation de puissance réactive et la génération d'harmoniques qui polluent le réseau de distribution. De plus, les équipements modernes sont de plus en plus sensibles à la tension d'alimentation qui leur est imposée. Augmenter la capacité des postes de génération d'électricité existants est difficile et très coûteux, surtout lorsque l'on considère les contraintes environnementales. Désormais, l'amélioration de la qualité de l'onde peut non seulement rendre les réseaux de distribution plus propres et performants mais entraîne aussi une réduction importante des pertes lors du transport et par conséquent, des économies significatives.

Les filtres actifs de la puissance sont largement utilisés afin de remédier à quelques uns des plus importants problèmes de la qualité de l'onde. La tendance actuelle vise la conception d'équipements multitâche qui permettent de remédier à plusieurs problèmes de la qualité de l'onde simultanément. Le conditionneur universel de puissance, mieux connu sous l'appellation anglophone Unified Power Quality Conditioner (UPQC), est l'un des filtres actifs des plus polyvalents permettant de compenser significativement les problèmes de la qualité de l'onde tels les harmoniques de tensions, hauts et creux de tension, déséquilibre de tension et papillotements, harmoniques de courant, puissance réactive de charge, déséquilibre du courant et courant de neutre.

Le UPQC consiste en un dispositif divisé en deux onduleurs de tension connectés dos-à-dos à travers un bus de tension continue commun autosupporté. Le premier onduleur est contrôlé telle une source de tension variable de la même manière que l'on fait régulièrement avec un filtre actif série, alors que le second est contrôlé en courant d'une manière similaire à un filtre actif parallèle. La littérature existante sur le sujet suggère que le filtre actif parallèle soit assigné à la compensation de la puissance réactive consommée par la charge. D'autre part, le filtre actif série est toujours utilisé afin de mitiger les problèmes reliés à la tension. Les hauts, creux et papillotements de la tension sont des détériorations de la qualité de l'onde de courtes durées. L'approche traditionnelle de contrôle du UPQC afin d'améliorer les problèmes de la qualité de l'onde présentent le désavantage de la sous-utilisation de l'onduleur du filtre actif série. Par conséquent, le facteur d'utilisation du filtre actif série est beaucoup plus bas que celui du filtre parallèle.

Le présent travail de doctorat est basé sur la philosophie d'utilisation optimale des ressources disponibles, c'est-à-dire de la manière la plus efficace possible et avec le meilleur rendement afin d'améliorer l'efficacité du système et de réduire le coût de fabrication et d'opération. Ce travail propose un concept de contrôle innovateur appelé Power Angle Control (PAC), ce qui signifie, contrôle de l'angle de puissance. Le concept stipule que les convertisseurs série et parallèle se partagent la puissance réactive de la charge, en parfaite coordination, sans affecter le fonctionnement fondamental de la compensation du UPQC. Cette situation résulte en une meilleure utilisation de l'onduleur série, en une réduction de la capacité de l'onduleur parallèle et ultimement, en une réduction du coût de l'ensemble du UPQC. De plus, cette thèse introduit une nouvelle fonctionnalité au UPQC dans laquelle il est possible d'étendre le concept du UPQC triphasé à trois fils vers celui triphasé à quatre fils.

Le concept PAC développé dans ce travail a été validé avec succès par simulation numérique et extensivement par de multiples manipulations en laboratoire. Les résultats expérimentaux montrent que, dans les conditions présentes au laboratoire avec une charge très inductive, un redressement de l'angle de puissance δ=28° entre la tension de source et celle résultante à la charge peut réduire la capacité du convertisseur parallèle de 50%. L'évaluation de la performance du concept PAC en présence de hauts, de creux et de distorsion de la tension de source et d'une charge non-linéaire est aussi effectuée. Sous l'effet de la distorsion de la tension de source (THD de la tension de source = 6.6%) ainsi que d'une charge non-linéaire (THD du courant de charge = 23.4%), le UPQC contrôlé avec le concept PAC compense efficacement les harmoniques de la tension de source (THD de la tension de charge = 3.2%) et la distorsion du courant (THD du courant de source 2.94%) et permet le partage simultané de la puissance réactive entre le convertisseur parallèle et série.

Ce travail a été partiellement exécuté en collaboration avec Hydro-Québec, Montréal, Canada et l'Institut de recherche d'Hydro-Québec IREQ, Varennes, Canada.

Mots-clés: Qualité de l'onde, filtre actif, conditionneur unifié de la qualité de l'onde, compensation de puissance réactive, compensation des harmoniques.

POWER QUALITY ENHANCEMENT AT DISTRIBUTION LEVEL UTILIZING THE UNIFIED POWER QUALITY CONDITIONER (UPQC)

KHADKIKAR, Vinod

ABSTRACT

Power electronics based equipments are rapidly emerging as key components in the present modern power distribution system. Power processing utilizing these devices offer vast advantages such as flexible control, cost reduction, overall size optimization, etc. On the other hand, operation of these devices gives rise to some of the serious power quality problems, such as, the reactive power requirement and generation of harmonics that pollutes the power distribution system. Moreover, modern equipments are becoming highly sensitive to the voltage supplied to them. Increasing the generation capacities of existing power stations is difficult and expensive due to environmental constraints. Hence, improving the quality of power can not only make the power distribution systems healthier and more efficient, but also results in reduced power losses, and thus saving in terms of costs.

Active power filters are widely used to tackle some of the important power quality problems. Recent trends are geared towards the realization of multitasking devices which can tackle several power quality problems simultaneously. The unified power quality conditioner (UPQC) is one of the most versatile active power filters that can compensate significant power quality issues, such as, voltage harmonics, voltage sag, voltage swell, voltage unbalance, voltage flicker, current harmonics, load reactive power, current unbalance, and neutral current.

A UPQC consists of two voltage source inverters connected back to back with each other sharing a common self-supporting DC link. One inverter is controlled as a variable voltage source in same manner as in the series active power filter (APF), and the other as a variable current source which is similar in operation as that of the shunt APF. The existing literature suggests the dependency on shunt inverter to compensate the load reactive power demand. Moreover, the series inverter is always utilized to overcome all the voltage related problems. The voltage sags, swells and the flickers are short duration power quality problems. Hence, this traditional approach of utilizing the UPQC to compensate the power quality problems shows a significant drawback of under usage of the available series inverter. Therefore, the utilization factor of the series inverter is much lower than that of the shunt inverter.

The present doctoral work is based on the philosophy of optimal utilization of the available resources in a most effective and efficient way to improve the product efficiency and to reduce the overall cost. This work proposes a novel control concept, termed as power angle control (PAC), in which both the series and shunt inverters share the load reactive power in co-ordination with each other without affecting the basic UPQC compensation capabilities. This eventually results in a better utilization of the series inverter, reduction in the shunt inverter rating to some extent and ultimately in the reduction of the overall cost of UPQC.

Moreover, this thesis also introduces a new functionality for UPQC in which, it is possible to extent the UPQC based three-phase three-wire system to a three-phase four-wire system.

The developed PAC concept is successfully validated through digital simulation as well as extensive experimental investigations. The experimental results show that for the given laboratory test conditions with a highly inductive load, a boost in power angle $\delta=28^{\circ}$ between the source and the resultant load voltage can reduce the shunt inverter rating by 50%. The performance evaluation of PAC approach under voltage sag, voltage swell, distorted source voltage and non-linear load conditions is also carried out. Under distorted source voltage (source voltage THD=6.6%) and the non-linear load (load current THD=23.4%), the UPQC with proposed PAC concept, effectively compensates the harmonics in source voltage (load voltage THD=3.2%), load current (source current THD= 2.94%) and shares the load reactive power between the series and shunt inverters, simultaneously.

This work was partially conducted in collaboration with Hydro-Québec, Montréal and Institut de recherche d'Hydro-Québec (IREQ), Varennes, Canada.

Keywords: power quality, active power filter, unified power quality conditioner, reactive power compensation, harmonics compensation.

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LIST OF ABBREVIATIONS

1D	One dimensional
2D	Two dimensional
3P3W	Three-phase three-wire
3P4W	Three-phase four-wire
AC	Alternating current
ANN	Artifical neural network
APF	Active power filter
ASD	Adjustable speed drive
AVC	Automatic voltage controller
C-DAC	Centre for development of advance computing
CSI	Current source inverter
CUF	Current unbalance factor
DBR	Diode bridge rectifier
DC	Direct current
DVR	Dynamic voltage restorer
FACTS	Flexible AC transmission systems
FFT	Fast fourier transform
GRÉPCI	Grupe de recherche en électronique de puissance et commande industrielle
HP	Horse power
HPF	High pass filter
IGBT	Insulated gate bipolar transistor
IREQ	Institute de recherche d'Hydro-Québec

IUPQC	Interline unified power quality conditioner
LPF	Low pass filter
LSR	Laboratoire simulation de résaux
LVRC	Line voltage regulator/conditioner
NPC	Neutral point clamp
PAC	Power angle control
PCC	Point of common coupling
p. f.	Power factor
PFC	Power factor correction
PI	Proportional-Integral
PLL	Phase-locked loop
PWM	Pulse width modulation
QVI	Quadrature voltage injection
rms	Root mean square
RPM	Revoluation per minute
SMPS	Switch mode power supply
SSC	Static series compensator
STATCOM	Static var compensator
THD	Total harmonics distortion
TSC	Thyristor switched capacitor
TSR	Thyristor switched reactor
UAPF	Unified active power filter
UAPLC	Universal active power line conditioner

UPFC	Unified power flow controller
UPQC	Unified power quality conditioner
UPQCS	Universal power quality conditioning system
UVTG	Unit vector template generation
VSI	Voltage source inverter
w.r.t.	with respect to

LIST OF SYMBOLS

δ	Power angle between source and load voltages
δ_f	Fixed power angle technique
δ_{max}	Maximum value of power angle δ
δ_v	Variable power angle technique
β	Phase angle between source voltage and load current during PAC approach
φ_S	Phase angle of source current *w.r.t.* source voltage
φ_L	Phase angle of load current *w.r.t.* load voltage
φ_{Sr}	Phase angle of series injected voltage *w.r.t.* source voltage
φ'_{Sr}	Phase angle of series injected voltage *w.r.t.* source voltage during voltage sag
φ''_{Sr}	Phase angle of series injected voltage *w.r.t.* source voltage during voltage swell
φ_{Sh}	Phase angle of shunt injected current *w.r.t.* source voltage
$\varphi_{Sh\text{-}S}$	Phase angle of shunt injected current *w.r.t.* source voltage during PAC approach (steady-state condition)
$\varphi_{Sh\text{-}L}$	Phase angle of shunt injected current *w.r.t.* source load voltage during PAC approach (steady-state condition)
$\varphi'_{Sh\text{-}S}$	Phase angle of shunt injected current *w.r.t.* source voltage during PAC approach (voltage sag condition)
$\varphi'_{Sh\text{-}L}$	Phase angle of shunt injected current *w.r.t.* source load voltage during PAC approach (voltage sag condition)
$\varphi''_{Sh\text{-}S}$	Phase angle of shunt injected current *w.r.t.* source voltage during PAC approach (voltage swell condition)
$\varphi''_{Sh\text{-}L}$	Phase angle of shunt injected current *w.r.t.* source load voltage during PAC approach (voltage swell condition)
Cdc	DC link capacitor

C_f	Ripple filter capacitor used for series inverter
i_{Grid}	Grid current
$I_{L,N}$	Load side neutral current
i_{La}, i_{Lb}, i_{Lc}	Load current for phase-a, phase-b, phase-c
$i_{La,\alpha}$,$i_{Lb,\alpha}$,$i_{Lc,\alpha}$	α-axis load current for phase-a, phase-b, phase-c
$i_{La,\beta}$,$i_{Lb,\beta}$,$i_{Lc,\beta}$	β-axis.load current for phase-a, phase-b, phase-c
I'_S	Source current during voltage sag
I''_S	Source current during voltage swell
i_{Sa}, i_{Sb}, i_{Sc}	Source current for phase-a, phase-b, phase-c
i^*_{Sa}, i^*_{Sb}, i^*_{Sc}	Reference source current for phase-a, phase-b, phase-c
I'_{Sh}	Shunt inverter current during voltage sag
I''_{Sh}	Shunt inverter current during voltage swell
i_{Sha}, i_{Shb}, i_{Shc}	Shunt inverter current for phase-a, phase-b, phase-c
i^*_{Sha}, i^*_{Shb}, i^*_{Shc}	Reference shunt inverter current for phase-a, phase-b, phase-c
$I_{Sh,N}$	Shunt inverter injected neutral current
$I_{S,N}$	Source side neutral current
I_m	Output of PI controller
$I_{Sh,PAC}$	Generalized shunt inverter current using PAC approach
k	Desired load voltage magnitude
k_f	Voltage fluctuation factor
K_{Sr}	Factor to denote % of maximum series inverter injection limit *w.r.t.* desired load voltage
L_S	Source inductance

L_{Sr}	Series inverter coupling inductor
L_{Sh}	Shunt inverter coupling inductor
P_L	Active power demanded by load
p_{La}, p_{Lb}, p_{Lc}	Instantaneous total active power extracted using single-phase p-q theory for phase-a, phase-b, phase-c
$\bar{p}_{La}, \bar{p}_{Lb}, \bar{p}_{Lc}$	Instantaneous fundamental active power extracted using single-phase p-q theory for phase-a, phase-b, phase-c
$\tilde{p}_{La}, \tilde{p}_{Lb}, \tilde{p}_{Lc}$	Instantaneous harmonic active power extracted using single-phase p-q theory for phase-a, phase-b, phase-c
P_S	Active power delivered by source
P_{Sh}	Active power handled by shunt inverter
$P_{Sh,PAC}$	Generalized active power handled by shunt inverter using PAC approach
P_{Sr}	Active power handled by series inverter
$P_{Sr,PAC}$	Generalized active power handled by series inverter using PAC approach
Q_L	Reactive power demanded by load
q_{La}, q_{Lb}, q_{Lc}	Instantaneous total reactive power extracted using single-phase p-q theory for phase-a, phase-b, phase-c
$\bar{q}_{La}, \bar{q}_{Lb}, \bar{q}_{Lc}$	Instantaneous fundamental reactive power extracted using single-phase p-q theory for phase-a, phase-b, phase-c
$\tilde{q}_{La}, \tilde{q}_{Lb}, \tilde{q}_{Lc}$	Instantaneous harmonic reactive power extracted using single-phase p-q theory for phase-a, phase-b, phase-c
Q_S	Reactive power delivered by source
Q_{Sh}	Reactive power handled by shunt inverter
$Q_{Sh,max}$	Maximum reactive power supported by shunt inverter
$Q_{Sh,PAC}$	Generalized reactive power handled by shunt inverter using PAC approach

Q_{Sr}	Reactive power handled by series inverter
$Q_{Sr,max}$	Maximum reactive power supported by series inverter
$Q_{Sr,PAC}$	Generalized reactive power handled by series inverter using PAC approach
R_S	Source resistance
S_{Series_APF}	Series inverter rating
v_{Grid}	Grid voltage
V_{dc}	Actual DC link voltage
V^*_{dc}	Reference DC link voltage
V'_L	Resultant load voltage with PAC approach
v_{La}, v_{Lb}, v_{Lc}	Load voltage for phase-*a*, phase-*b*, phase-*c*
v^*_{La}, v^*_{Lb}, v^*_{Lc}	Reference load voltage for phase-*a*, phase-*b*, phase-*c*
$v_{La.\alpha}$,$v_{Lb.\alpha}$,$v_{Lc.\alpha}$	α-axis load voltage for phase-*a*, phase-*b*, phase-*c*
$v_{La.\beta}$,$v_{Lb.\beta}$,$v_{Lc.\beta}$	β-axis.load voltage for phase-*a*, phase-*b*, phase-*c*
V_m	Peak amplitude of source voltage
V_{Lm}	Peak amplitude of desired load voltage
$v^*_{quad.a}$	Reference series inverter voltage for phase-*a* using quadrature voltage injection (QVI) approach
$v^*_{quad.b}$	Reference series inverter voltage for phase-*b* using approach
$v^*_{quad.b}$	Reference series inverter voltage for phase-*c* using QVI approach
v_{Sa}, v_{Sb}, v_{Sc}	Source voltage for phase-*a*, phase-*b*, phase-*c*
v^*_{Sa}, v^*_{Sb}, v^*_{Sc}	Reference source voltage for phase-*a*, phase-*b*, phase-*c*
V_S	Rated source voltage during steady-state condition
V'_S	Source voltage during sag condition

V''_S	Source voltage during swell condition
$V_{Sa1}, V_{Sb1}, V_{Sc1}$	Positive sequence voltages for phase-*a*, phase-*b*, phase-*c*
$V_{Sa2}, V_{Sb2}, V_{Sc2}$	Negative sequence voltages for phase-*a*, phase-*b*, phase-*c*
$V_{Sa0}, V_{Sb0}, V_{Sc0}$	Zero sequence voltages for phase-*a*, phase-*b*, phase-*c*
$V_{Sah}, V_{Sbh}, V_{Sch}$	Harmonics voltages for phase-*a*, phase-*b*, phase-*c*
V^e_{Sd}, V^e_{Sq}	Distorted source voltages direct (d) and quadrature (q) components in synchronous rotating frame
$V^e_{Sd.f}$, $V^e_{Sq.f}$	Fundamental component of source voltage in synchronous rotating frame
$V^e_{Sd.h}$, $V^e_{Sq.h}$	Harmonics component of source voltage in synchronous rotating frame
V^S_{Sd}, V^S_{Sq}	Distorted source voltages direct (d) and quadrature (q) components in stationary frame
$V^S_{Sd.f}$, $V^S_{Sq.f}$	Fundamental component of source voltage in stationary frame
$V^S_{Sd.h}$, $V^S_{Sq.h}$	Fundamental component of source voltage in stationary frame
V_{Sr}	Series injected voltage during PAC approach
V_{Sr1}	Series injected voltage during PAC approach (steady-state condition)
V_{Sr2}	Series injected voltage for voltage sag compensation
V'_{Sr}	Resultant series injection voltage for voltage sag compensation with PAC approach
V_{Sr3}	Series injected voltage for voltage swell compensation
V''_{Sr}	Resultant series injection voltage for voltage swell compensation with PAC approach
$V_{Sr.max}$	Maximum series injection voltage limit
$V_{Sr.PAC}$	Generalized series inverter voltage using PAC approach
$v_{Sra}, v_{Srb}, v_{Src}$	Series inverter voltage for phase-*a*, phase-*b*, phase-*c*
$v^*_{Sra}, v^*_{Srb}, v^*_{Src}$	Reference series inverter voltage for phase-*a*, phase-*b*, phase-*c*

INTRODUCTION

In recent years, the term "*Power Quality*" has gained significant importance, especially in electrical engineering related fields. As per international standards, the term power quality can be defined as the physical characteristics of the electrical supply provided under normal operating conditions that do not disrupt or disturb the user's processes. However, the term power quality can have different meanings and significances according to the requirements or environmental condition under which it has been defined. For example, for the *utility* – it might be the concern of non-linear load causing harmonics on the network; for the *consumers* – it might be the distortion present in the supplied voltage, etc.

The ever-increasing interest in the subject of power quality can be explained in the context of some of the major key issues:

- Traditionally, equipments were simpler and thus more robust and insensitive to minor variations in supply voltage. Most of the loads on the early electric distribution network were dominated by non-polluting loads. The major concern in early electric power system was the reactive power support. The development of modern power electronics switching devices has completely changed the load characteristics. The switch mode power supplies (SMPS), dimmers, current regulator, frequency converters, low power consumption lamps, arc welding machines, etc, are some out of the many vast applications of power electronics based devices. The operation of these loads/ equipments generates harmonics and thus, pollutes the modern distribution system. Additionally, equipments are increasingly becoming sophisticated, at the same time highly sensitive to the quality of voltage supplied to them.
- Consumers of electricity have become much more aware of their rights and demand low-cost electricity of high reliability and quality.
- The growing interest in the utilization of renewable energy resources for electric power generation is making the electric power distribution network more susceptible to power quality problems. The integration of renewable energies (solar, wind, etc.) and their accommodation in the existing electric networks is often a complex issue.

Major Power Quality Problems

The important power quality problems at the distribution level are discussed below (Dugan *et al*., 1996, Schlabbach *et al*., 2001; Stones and Collinson, 2001; Sankaran, 2002).

- **Voltage Sag:** It is a decrease in rms value of supply voltage for a short duration. The duration of voltage sag may vary between 5 cycles to a minute. Voltage sags can be caused by the system faults, increased load demand, transitional events such as large motor starting, etc.

- **Voltage Swell:** It is an increase in rms value of supply voltage for a short duration. The duration of voltage swell may vary between 5 cycles to a minute. Voltage swells can be by to system faults, switching off of large rated loads, etc.

- **Transient:** It is an undesirable momentary deviation of the supply voltage or current, which can be impulsive or oscillating in nature. An impulsive transient is a sudden, non power frequency change in voltage or current which is unipolar in nature. These transients are mainly caused by lighting strikes.

- **Voltage Flicker:** A very rapid change in the supply voltage is called as voltage flicker. These are systematic random variations in supply voltages. The arc furnace is one of the most common causes of voltage flicker on utility transmission and distribution systems.

- **Waveform Distortion:** It is a steady state deviation in the voltage or current waveform from an ideal sine wave at a fundamental supply frequency, characterized by the spectral content of the deviation. These distortions can be classified as DC offset, harmonics, notching and noise.

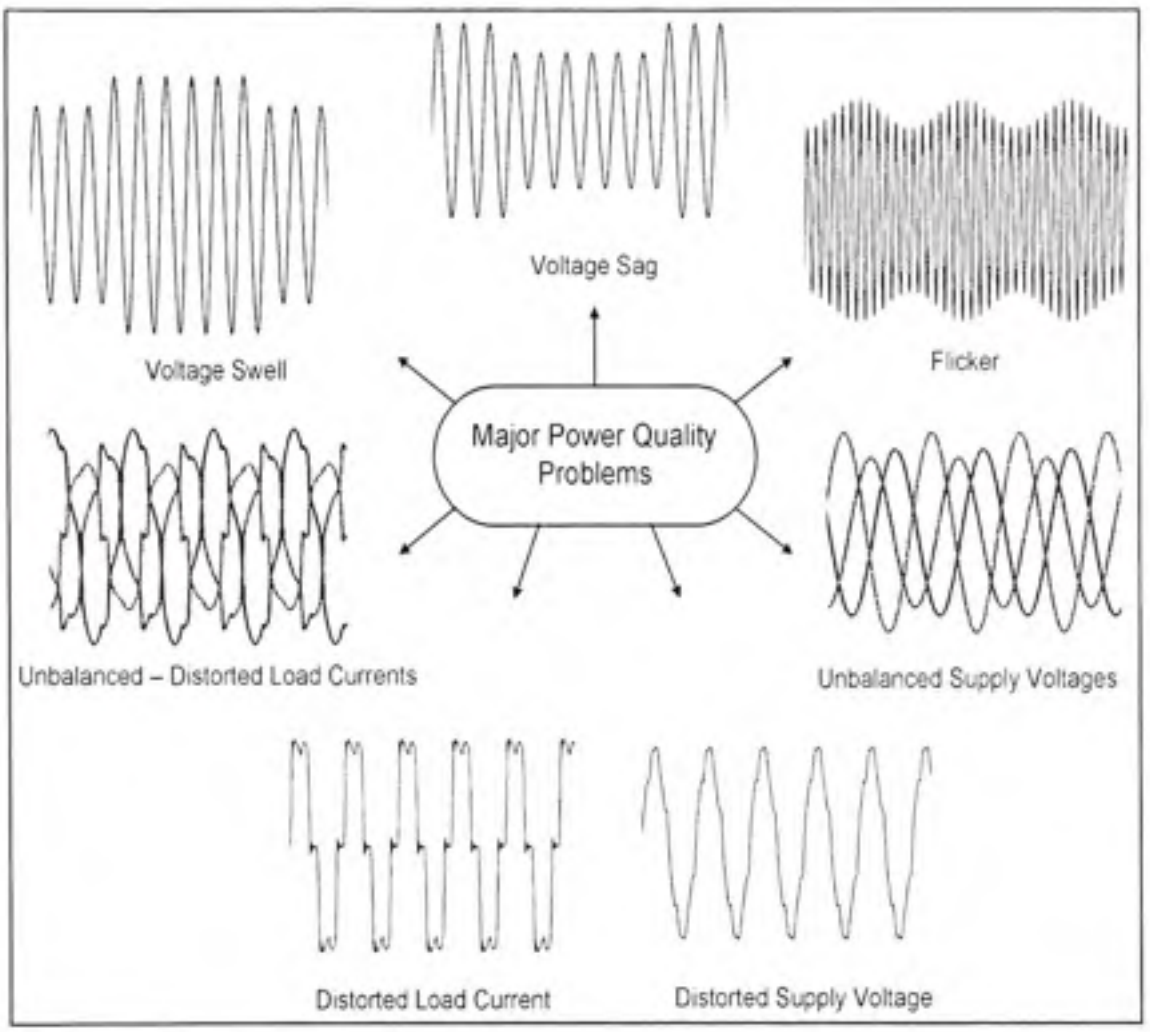
- **Harmonics:** Harmonics are sinusoidal voltages or currents having frequencies that are integral multiples of the fundamental supply voltage frequency. Harmonic distortion is caused by the nonlinear characteristics of devices and loads on the power system. The term total harmonics distortion (THD) gives the measure of harmonics content in a signal and is generally used to denote the level of harmonics present in the voltage/current. High harmonic amplitudes may not only cause malfunctions, additional losses and overheating, but also overload the power distribution network and overheat the neutral conductor and cause its burn out. The harmonics can generate additional acoustic noise from motors and other apparatus, reducing the motor efficiency and also can cause interference with neighboring telephone lines.

- **Unbalance:** The voltage/current unbalance is a condition in which the voltages/currents of the three phases of the supply are not equal in magnitude. Furthermore, they may not even be equally displaced in time. The primary cause of voltage/current unbalance is the single-phase load on three-phase circuits. Severe imbalance can result during single phasing conditions when the protection circuit opens up one phase of a three-phase supply.

- **Frequency Deviation:** These variations are usually caused by rapid changes in the load connected to the system. The supply frequency may drop during the operation of large drag lines in a comparatively low inertia system. The supply frequency should not deviate too much from the nominal frequency (50 or 60 Hz).

- **Interruption:** An interruption occurs when the supply voltage or load current decreases to less than 0.1 *p. u.* for a period of time not exceeding 1 min. It can be the result of faults in the power system, equipment failures, and control malfunctions.

Some of the important power quality problems are shown in the following Figure.



Pictorial view of major power quality problems on distribution level.

Power Quality Problem Compensation – Why is it important?

The disturbances in voltage (harmonics, sags, swells) may cause tripping of sensitive electronic equipment which can lead to disastrous consequences in industrial plants, such as, unexpected results or a termination of the whole production line. These events are common in industrial sectors and cause high economical damage. In the above scenario, it is the source that disturbs the load/ sensitive equipment. To avoid heavy economical losses, the industrial customers often install mitigation devices/ equipments to protect their own plants from such kind of disturbances.

The presence of power electronics based equipments/ loads at the commercial as well the industrial sector is quite common. A diode bridge rectifier followed by a front end capacitor is one of the most common types of topologies used in all the power electronics based power processing applications. These equipments are more often insensitive to disturbances in voltage, but draw the currents which are highly distorted in nature. Moreover, studies show that such kinds of equipments are of major concern since they produce distortion in supply voltages. Another important fact is that the harmonics and unbalanced currents ultimately result in distorted and unbalanced voltages. In this condition, even if the plant does not experience any direct impact, they are the main cause of deterioration in the quality of power supplied to the neighboring customers. There may be many similar types of loads connected on the same feeder. The pollution on the distribution network is increasing gradually at the extent that the utility providers can no longer support them. Therefore, strict standards are being imposed by the utilities on industrial and domestic consumers to limit the amount of harmonics currents, unbalance and/or flicker that a load may introduce to the network. To comply with these limits, customers often have to install mitigation equipments to reduce the level of pollution caused by their loads and thus, avoid heavy penalties forced by the utility.

The growing use of power electronics based equipments in modern plants is resulting in a load which is sensitive and harmonics producing in nature. Interestingly, these equipments generally produce distortion in currents and/or voltages. Thus, there is a new trend to install mitigating equipments that can serve the dual purpose, to both the utility as well as to the customer. The important objective under such an environment is to simultaneously protect sensitive equipments from voltage disturbances and to reduce the distortion injected by the plant to the network.

Role of Power Electronics Devices in Power Quality Enhancement

As discussed in the previous sections, the power electronics based devices/equipments have become key components in today's modern power distribution system. In spite of the vast advantages offered by utilizing the power electronics based equipment for power processing,

the operation of these devices gives rise to some serious drawbacks in terms of power quality. These devices generate harmonics polluting the power distribution system, and demand reactive power. In order to provide technical solutions to the new challenges imposed on the power systems, the concept of flexible AC transmission systems (FACTS) was introduced in the late 1980s. The FACTS devices incorporate power electronics based controllers to enhance the controllability and to increase power transfer capability of the transmission system. There are two approaches for the realization of power electronics based compensators: one employs conventional thyristor-switched capacitors (TSC) and reactors (TSR), and the other uses self-commutated switching converters. Both the schemes help to efficiently control the real and reactive power, but only the second one can be used to compensate current and voltage harmonics. Moreover, self-commutated switching converters present a better response time and more compensation flexibility.

The static VAR compensators (SVC) are used to control AC voltage by generating or absorbing the reactive power by means of passive elements. A SVC consists of an anti-parallel thyristors and passive elements such as a capacitor (TSC) or a reactor (TCR). The effective value of the capacitor or inductor reactance is changed continuously by controlling the firing angle of the thyristors. A major drawback in the use of SVC is that the reactive power handled by the SVC system is limited by the size of passive elements. One of the most versatile FACTS devices is the STATCOM. It consists of a voltage source converter (VSC)/ voltage source inverter (VSI) with pulse width modulation (PWM) and has a faster speed of response. In the transmission system, it can be used to improve the system stability and damping or to support the voltage profile. The same structure at the distribution level, known as D-STATCOM, can be used for reactive power support or for voltage regulation. The static series compensator (SSC) or dynamic voltage restorer (DVR) is a VSI connected in series with the supply line and acts as a controlled voltage source to obtain the desired load voltage. When an external DC voltage source is utilized for VSI, the SSC/ DVR can be used to compensate harmonics in the voltage, to regulate load voltage, and to compensate voltage unbalance, sag and flicker.

Another device, the active power filter (APF) is the most promising solution to mitigate some of the major power quality problems at the distribution level. They can be classified as shunt APFs, series APFs, hybrid APFs, and unified power quality conditioner (UPQC). The UPQC is one of the most versatile power quality enhancement devices which offer advantages of both the shunt and series APFs, simultaneously. A detailed operating principle and the vast capabilities of UPQC are discussed in CHAPTER 2. The use of any one of these APFs is slowly becoming a common practice in modern industrial installations.

Research Objectives

This work was conducted partially in collaboration with Hydro-Québec and IREQ. The present work had two defined goals – *i*) to carry out the feasibility analysis of UPQC under a realistic network condition and *ii*) to develop a novel control approach for UPQC to improve the system performance, and thus to contribute in the on going research work in the area of power quality enhancement.

The research objectives are summarized below:

- To carry out an in-depth analytical study on how the active and reactive power flows between the utility, UPQC and the load. The purpose of this analysis is to understand how the UPQC may behave under different operating conditions.

- To perform feasibility analysis of UPQC under a realistic network environment. The network Simulink model was built and provided by *Network Simulation Lab (LSR), IREQ*, Varennes, Québec.

- To realize a novel system configuration for the three-phase four-wire UPQC based system. This provides an additional option to future industrial customers to realize the three-phase four-wire system from three-phase three-wire network.

- To utilize the series inverter up to its true capabilities, since it is revealed that the series inverter in almost all the applications is underused.

- To reduce the rating of shunt inverter such that it will ultimately help to optimize the overall UPQC cost.

- To develop a new control philosophy for UPQC which can incorporate the last two objectives. (discussed in CHAPTER 6, termed as Phase Angle Control of UPQC).

Methodology

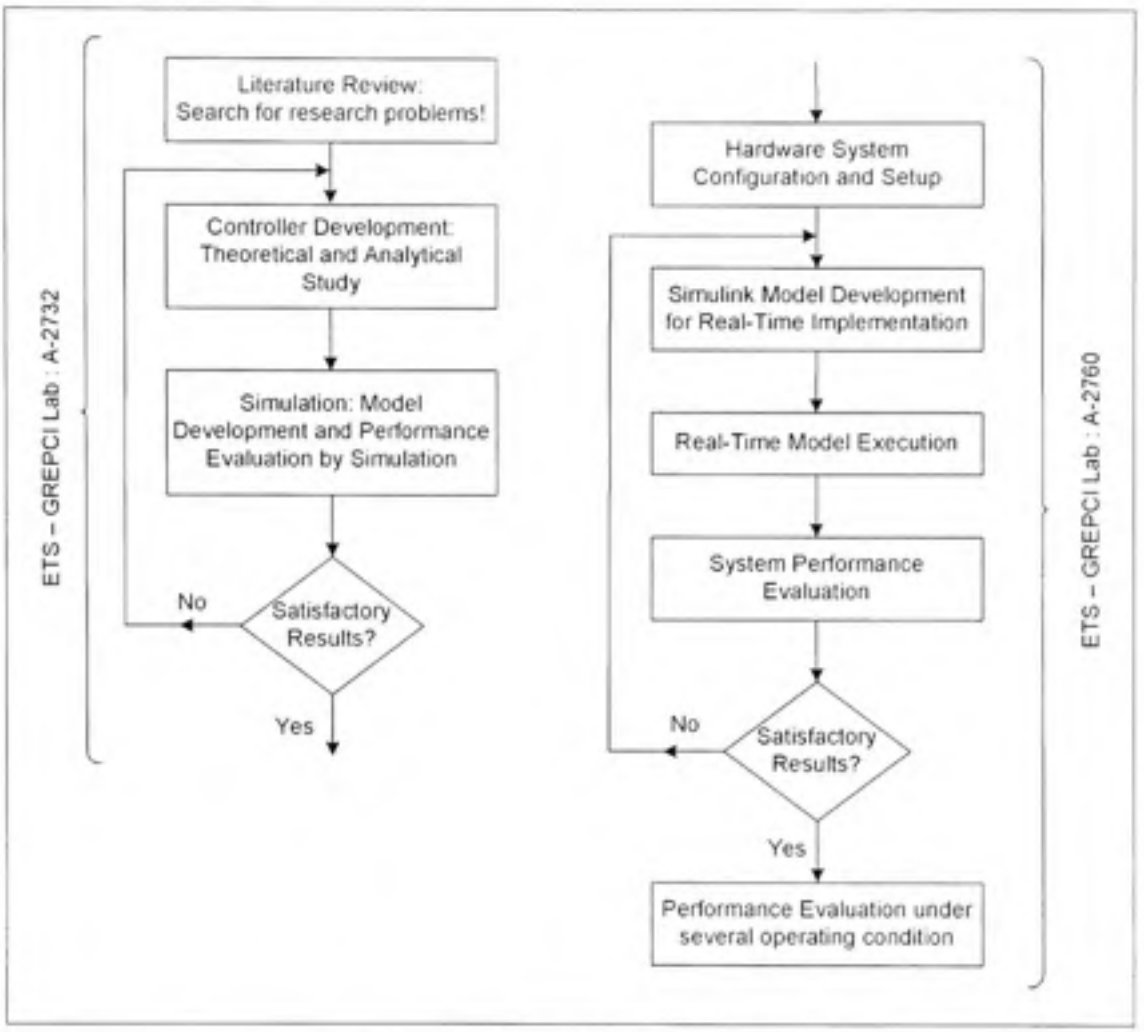
To accomplish the objectives highlighted above three important steps are followed which are outlined below:

- This thesis is made of the basic laws of trigonometry, circuit theory and electrical engineering. All the developed control approaches are first put forward through adequate mathematical formulation supported with detailed vector diagram representations.

- The developed control approaches are then modeled using a digital simulation tool, in this work, MATLAB/ Simulink. The SIMPOWERSYSTEM (SPS) block sets are predominantly used to represent the electrical system and to build the necessary simulation models. The performance of UPQC with developed control approaches is evaluated under different operating conditions.

- Finally, the reported research work is validated through laboratory experimental studies. A rapid hardware prototyping board from dSPACE, such as, DS1104 is used to interface the hardware system with MATLAB/ Simulink based control models. The developed controllers are tested under several different operating conditions.

The flow chart to achieve the proposed research work is shown below.



Research work flow chart.

Thesis Contributions

The thesis work was initiated with the project of feasibility analysis of emerging power quality enhancement devices such as unified power quality conditioner, popularly known as UPQC, for possible practical applications.

The foundation of this thesis work relies on the two significant terms, active power and reactive power. High importance is given to these two quantities while compensating several important power quality problems. At a given time, the source should supply only active power to the load, while, the reactive power should be locally supported by the active power filter system. In the course of action, several controller approaches/concepts are proposed

which are applicable to the shunt APFs, series APFs and/or UPQC. The important control approaches are highlighted as: unit vector template generation, quadrature voltage injection, generalized single-phase *p-q* theory, power angle control of UPQC.

The remarkable accomplishment of the proposed work is in the development of a novel control philosophy for UPQC, named as, power angle control (PAC) approach. CHAPTERS 2, 3 and 4 are provided for easy and better understanding of the PAC concept and serve as a benchmark for the thesis work. The fundamentals of the PAC approach are described by providing detailed phasor representations and an in-depth mathematical analysis. The concept of the PAC approach is supported through simulation studies and is successfully validated experimentally. The concept of PAC approach is standardized in such a way that it is well understood under varieties of conditions which includes the normal steady-state, voltage sag and voltage swell.

An interesting UPQC based system configuration/structure is also proposed for future three-phase four-wire (3P4W) distribution system. In the proposed system configuration, a 3P4W system is realized from three-phase three-wire (3P3W) UPQC based system. The neutral of series transformer, used in the series part UPQC, is considered as the neutral for the proposed 3P4W system. Thus, even if the power supplied by the utility is 3P3W, an easy expansion to 3P4W system, in UPQC based applications, can be achieved.

Finally, an experimental prototype is built in the *Groupe de recherche en électronique de puissance et commande industrielle*, GRÉPCI, (Power Electronics & Industrial Control Research Group) laboratory at École de technologie supérieure to implement the proposed control algorithms. The prototype is comprised of two three-phase voltage source inverter connected back to back with each other. A kind of universal active power filter which houses 14 insulated gate bipolar transistor (IBGT's), physically provides an option of realizing almost any active power filter system configuration, such as, single-phase and three-phase (three-wire or four-wire) shunt APF, series APF, UPQC or any types of hybrid APFs. A hybrid analog-digital control system is designed and built particularly for this prototype. It

consists of a digital signal processor board, DS1104, used to realize the developed control algorithms in real-time. The DS1104 is predominantly utilized to generate reference current/voltage signals. A separate analog board is designed and fabricated to perform pulse width modulation. The developed board has an option to select a triangular carrier signal based fixed frequency PWM (switching frequency can be set to 1kHz to 20kHz) or a variable frequency hysteresis controller. Several loads, both linear and non-linear are realized in the laboratory to produce a variety of load profiles. The developed system performance is verified under different source voltages and different loading conditions. The experimental results are promising and support the findings reported in the proposed work.

Thesis Outline

This thesis is organized as follows:

CHAPTER 1 presents a thorough review of the past and the most recent research work being done in the area of power quality compensation using UPQC. Reported literature on the topic is briefly discussed. The UPQC basics, including key concepts and operating principles, are explained which serves as a foundation for this thesis work. A steady-state power flow analysis is also carried out and supported with a numerical example. This chapter is partially based on two published papers (Khadkikar *et al.*, 2006a, Khadkikar and Chandra, 2006e).

CHAPTER 2 is fully dedicated to the collaboration project. Development of the simplest controller for UPQC is carried out. Extensive simulation results with UPQC installed on realistic network conditions are reported. The detailed experimental results on single-phase UPQC system under several lab tests are also discussed at the end of the chapter. The work presented in this chapter (analytical and simulation studies) is based on the paper entitled "Application of UPQC to protect a sensitive load on a polluted distribution network", (Khadkikar *et al.*, 2006b).

In CHAPTER 3, special attention is given to the voltage sag compensation using reactive power control. A new simplified approach is developed to determine the quadrature injection voltage necessary to compensate the voltage sag on the system. Interesting experimental results are discussed both for single-phase and three-phase UPQC system. This work (analytical and simulation studies) is reported in "A Novel Control Approach for Unified Power Quality Conditioner Q without Active Power Injection for Voltage Sag Compensation", (Khadkikar and Chandra, 2006e).

CHAPTER 4 is the result of an innovative topology by which the future industrial customers or utility providers will have an option to realize a three-phase four-wire system on a three-phase three-wire network. A new concept to compensate the unbalanced load on three-phase system is also reported. The validation of the proposed work is done through simulation and experimental studies. Part of the work is already published in "A Novel Structure for Three-Phase Four-Wire Distribution System Utilizing Unified Power Quality Conditioner (UPQC)". (Khadkikar and Chandra, 2006d).

CHAPTER 5 includes the major contribution of this thesis work. A new concept and philosophy to support the load reactive power utilizing both the shunt and series inverters of UPQC is proposed. This co-ordinated load reactive power sharing feature of UPQC (termed as Power Angle Control (PAC)) results in the shunt inverter rating reduction, and thus the overall cost of UPQC. A detailed mathematical analysis, simulation results and experimental investigations are given. The experimental results show that for a given laboratory load condition the shunt inverter rating can be reduced up to 50%. The reported work is published in IEEE Transactions on Power Delivery ("A New Control Philosophy for Unified Power Quality Conditioner (UPQC) to Co-ordinate Load Reactive Power Demand Between Shunt and Series Inverters", Khadkikar and Chandra, 2008b).

In CHAPTER 6, the concept of PAC of UPQC is further extended for different source voltage conditions. Generalized equations for the PAC approach are also formulated. Validation of the reported work is done through simulation and experimental studies.

The key conclusions of this thesis work and recommendations for future work are also reported. Finally, at the end of the thesis, the list of key references and appendices are provided.

CHAPTER 1

UPQC BASICS AND STEADY-STATE POWER FLOW ANALYSIS

1.1 Introduction

This chapter is aimed to develop necessary background knowledge and to briefly discuss the latest development in the field of *active power filters* (APF). The chapter begins with a detailed working principle of the UPQC. Later on in the chapter, a systematic literature review on the active power filters is given. It is shown that the *unified power quality conditioner* (UPQC) is truly a versatile device among the active power filters to compensate several different power quality problems, simultaneously. This was one of the motivations to carry out the research work on UPQC. An interesting analytical study on how the active and reactive power flows between source, UPQC, and load under different operating conditions is done. This conceptual study helps to understand the power transfer capabilities of UPQC.

1.2 UPQC Concept and Operating Principle

There are two important types of active power filters (APF) – shunt APF and series APF. The shunt APF is the most promising to tackle the current related problems, whereas, the series APF is the most suitable to handle voltage related problems. Since the modern distribution system demands a better quality of voltage being supplied and current drawn, installation of these two APFs have great scope in the near future. However, installing two separate devices to compensate voltage and current related power quality problems, independently, may not be a cost effective solution. Moran (1989), introduced a system configuration in which both series and shunt APFs were connected back to back with common DC reactor in between them. He termed the topology as line voltage regulator/conditioner (LVRC). The back-to-back inverter system configuration truly came into attention when Fujita and Akagi (1998) proved the practical application of this topology with 20kVA experimental results. Fujita and Akagi named this device as – unified power quality conditioner (UPQC), and since then the name UPQC has been popularly used by many researchers (Chen *et al.*, 2000; Elnady *et al.*,

2001; Ghosh *et al.*, 2004; Khoor *et al.*, 2005; Kazemi *et al.*, 2006a; Kolhatkar and Das, 2007).

UPQC is the integration of shunt and series APFs with a common self-supporting DC bus.

1.2.1 UPQC System Configuration

Figure 1.1 shows system configuration of a three-phase UPQC. As marked in the figure, the key components of UPQC can be highlighted as follows:

- Comp-A, voltage source inverter (VSI): it is connected across the load and controlled to function as shunt APF.
- Comp-B, VSI: it is controlled to function as series APF.
  Both the VSIs are realized by using six insulated gate bipolar transistors (IGBTs) each and are connected to the network by using coupling inductors.
- Comp-C, DC link capacitor: the two VSIs are connected back to back with each other through this capacitor. The voltage across this capacitor provides the self-supporting DC voltage for proper operation of both the inverters. With proper control, the DC link voltage acts as a source of active as well as reactive power and thus eliminates the need of external DC source (For example: DC battery).
- Comp-D, coupling inductor: it is utilized to connect the shunt inverter to the network and facilitates the flow of compensating current. It also helps in smoothing the current wave shape.
- Comp-E, LC filter: it serves as a passive low pass filter and helps to eliminate high frequency switching ripples on generated inverter output voltage.
- Comp-F, series transformer: the necessary voltage generated by the series inverter to maintain the load voltage pure sinusoidal and at desired value is injected in the line through these series transformers. A suitable turn ratio is often considered to reduce the current flowing through the series inverter.

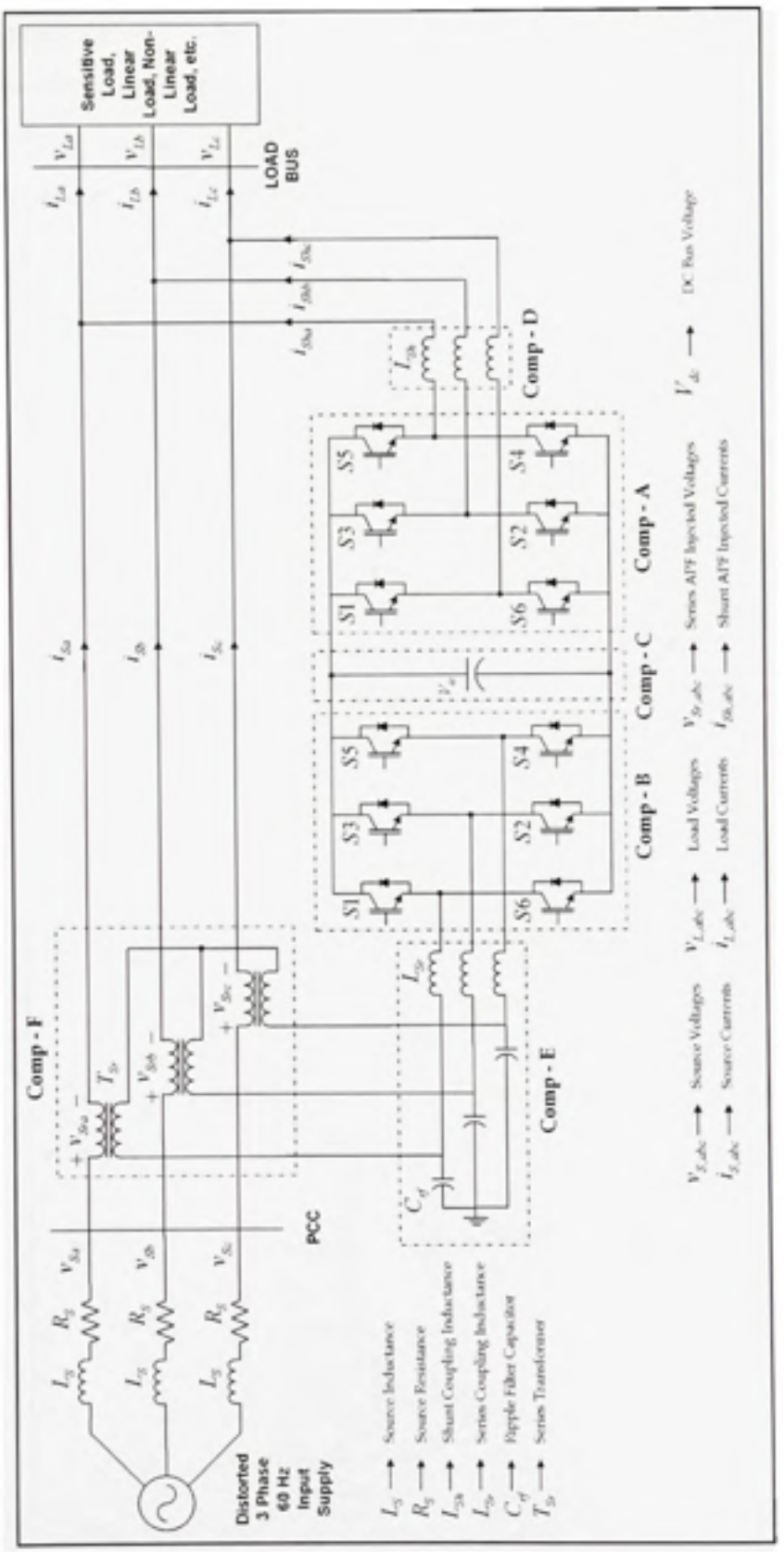


Figure 1.1 Detailed system configuration of three-phase UPQC.

As UPQC is a combination of shunt and series APFs, its working principle can be easily understood by describing the operation of shunt and series parts, separately. Enormous work has been reported in the literature on shunt and series inverters as active filters which include modeling, detailed parameter selection, practical consideration, controller development etc. In this thesis work, only brief operating principle of both the APFs is discussed and other basic details are not given.

1.2.2 Shunt Inverter Operation

The shunt inverter, when realized as shunt active filter, is shown in Figure 1.2. These kinds of active filters are widely used to compensate *i) current harmonics, ii) reactive power, iii) load current unbalance,* and *iv) neutral current* (in case of 4 wire system) (Akagi, 1996; Singh *et al.*, 1999, El-Habrouk *et al.*, 2000). The name "*shunt active filter*" (some researchers also use the name "*parallel active filter*") comes from the fact that the inverter is connected across (in shunt or in parallel) the load whose power quality problems need to be compensated.

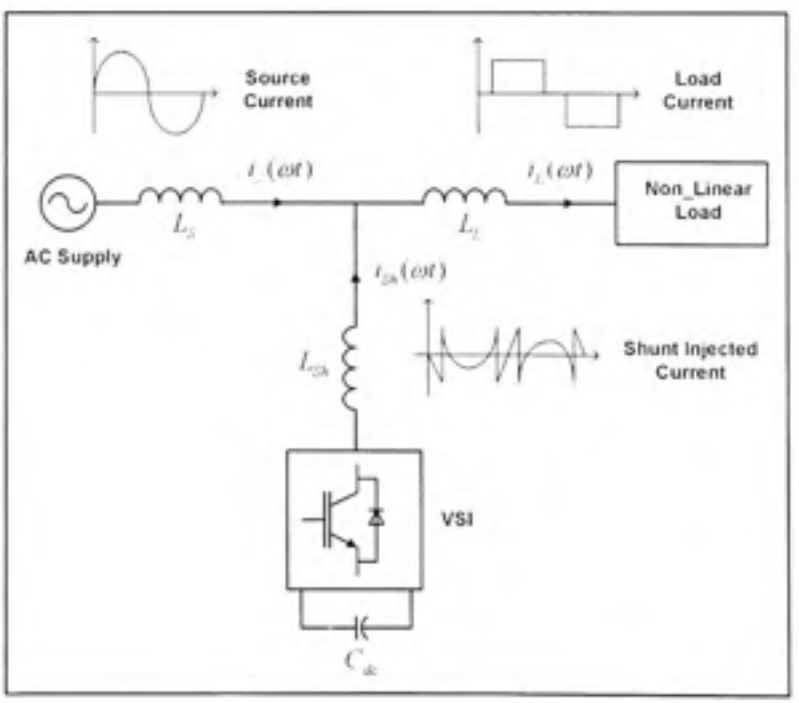


Figure 1.2 Shunt active filter operating principle.

The coupling inductance, L_{sh}, provides smoothing and isolation for high frequency components. The desired current waveforms are obtained by adequate control of the inverter switches (IGBTs). The control of wave shape is limited by the inverter switching frequency and by the available driving voltage across the coupling inductance. The driving voltage across the coupling inductance determines the maximum di/dt that can be achieved from the active filter. This is important because relatively high values of di/dt may be needed to cancel higher order harmonics components. Therefore, there is a trade-off involved in sizing the coupling inductor. A large inductor is better for isolation from the power system and protection from transient disturbances. However, large inductor limits the ability of active filter to cancel higher order harmonics.

Figure 1.2 also illustrates the fundamental operating principle of the shunt inverter to cancel current harmonics. The inverter in the shunt APF is a bilateral converter. It is operated in current control mode i.e. switching of the inverter is done in such a way that it delivers a current which is equal to the set value of the reference current as governed by the active filter control algorithm. As shown in Figure 1.2, the load on the system is non-linear which draws a square wave current from the source. In order to cancel the harmonics generated by the non-linear load and to make the source current perfect sinusoidal, the shunt inverter should inject the current as given by following equation:

$$i_{sh}(\omega t) = i^{*}_{s}(\omega t) - i_{l}(\omega t) \tag{1.1}$$

Where, $i^{*}_{s}(\omega t)$ represents the reference source current generated by the active filter controller.

Thus the basic principle of the shunt inverter, as shunt APF, can be stated as: *it generates a current equal and opposites in polarity to the harmonic current drawn by the load and injects it to the point of coupling thereby forcing the source current to be pure sinusoidal.*

1.2.3 Series Inverter Operation

The series inverter when realized as series active filter is shown in Figure 1.3 This kind of active filters can be used to compensate *i) voltage harmonics, ii) voltage sag, iii) voltage swell, iv) voltage unbalance,* and *v) voltage flicker* (Akagi, 1996; Singh *et al.*, 1999, El-Habrouk *et al.*, 2000). The name "*series active filter*" comes from the fact that the inverter is connected in series between the source and load, and acts as a voltage controlled source.

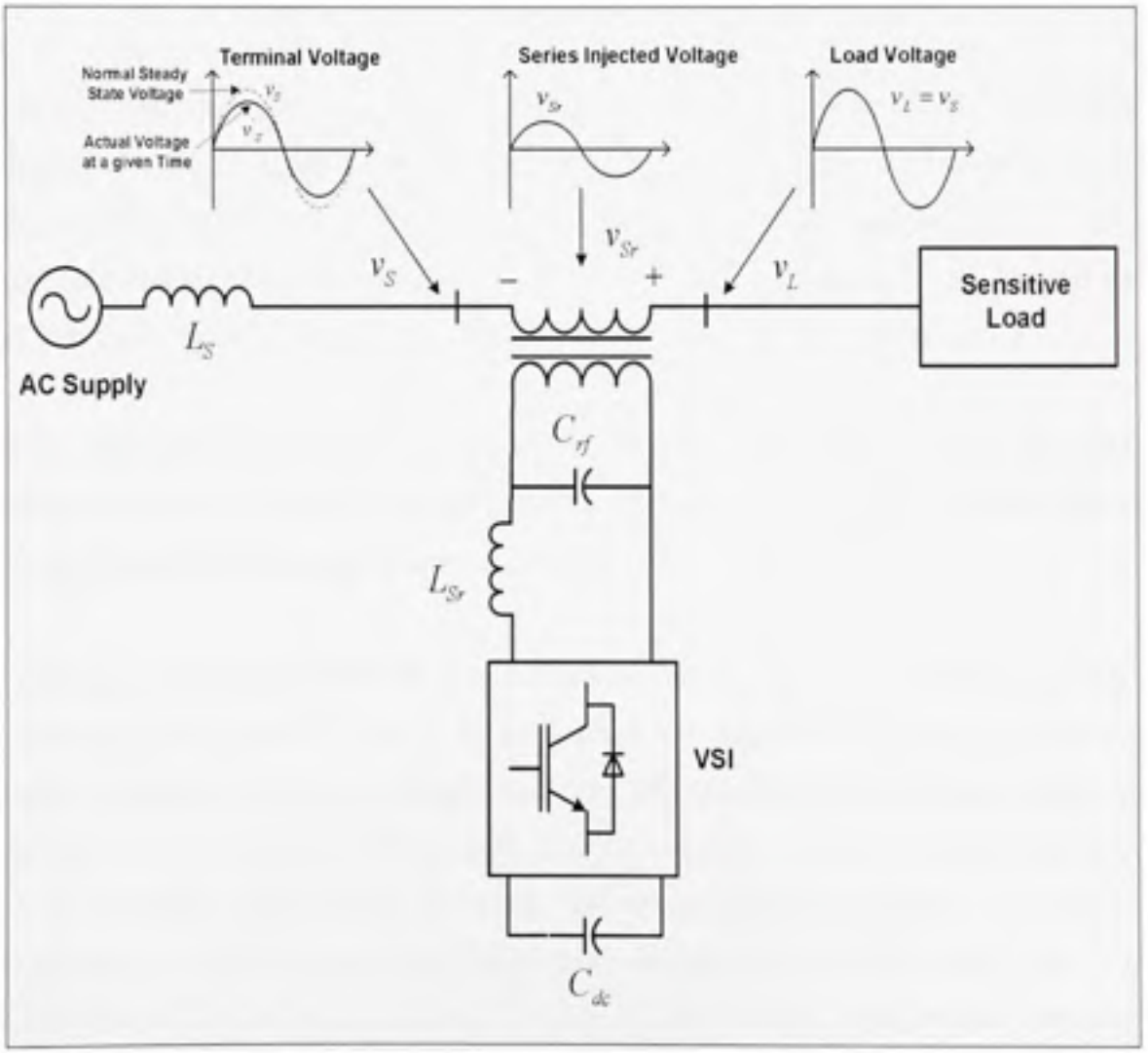


Figure 1.3 Series APF operating principle.

Figure 1.3 illustrates the fundamental operating principle of series APF to maintain the load end voltage insensitive to the variation in the source voltage. The inverter in the series APF is

operated in voltage control mode i.e. switching of the inverter is done in such a way that it delivers a voltage which is equal to the set value of the reference voltage as governed by the APF control algorithm. A sag in the source voltage is shown in the figure. The reduced voltage is marked as v'_S. In order to keep the voltage at load terminal equal to the normal steady-state voltage, the series inverter should inject a voltage as given by following equation:

$$v_{Sr}(\omega t) = v^{*}_{L}(\omega t) - v_{S}(\omega t) \tag{1.2}$$

Where v^{*}_{L} is the desired voltage at the load bus. Thus, to compensate a dip in voltage the series inverter should supply an in-phase voltage (other options are also available), such that the sum of the reduced source voltage and series injected voltage maintains the desired load voltage. If the source voltage contains the harmonics, using (2.12), the series inverter should inject harmonic part of voltage in order to maintain the load voltage sinusoidal.

Thus the basic principle of series inverter, as series active filter, can be stated as follows: *it generates a voltage and inject in series with line such that the voltage at the load side would be always sinusoidal, free from distortion, and at desired voltage magnitude.*

Sometimes, as configured in Figure 1.4, a tuned passive LC filter is connected in shunt with the load along with the series APF. In such cases, the series APF compensate the current distortion produced by the non-linear load, by imposing a high impedance path to the harmonics current, and thus forcing high frequency currents to flow through passive filter. The high impedance imposed by the series APF is created by generating a voltage of the same frequency that the current harmonic component needs to be eliminated. Thus a series APF can also act as a harmonic isolator. In such applications the rating of series inverter is a small fraction of the load kVA rating.

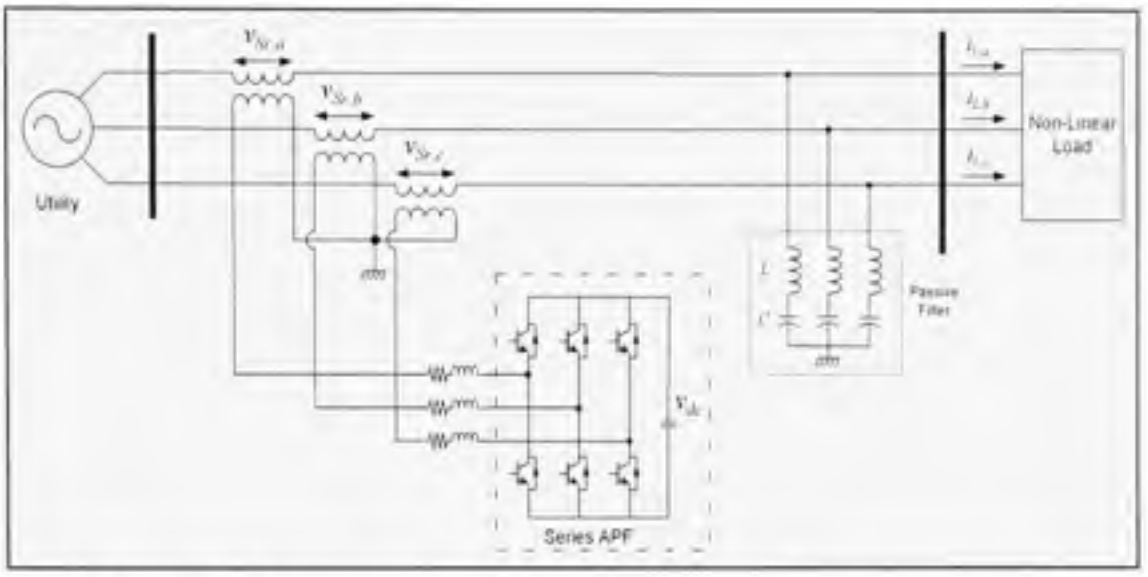


Figure 1.4 Combined series APF and shunt passive filter to compensate load current harmonics.

1.2.4 The Role of Shunt Inverter in UPQC Operation

The voltage injected in series with the load by series inverter is made to follow a control law such that the sum of this injected voltage and the utility voltage is sinusoidal. Moreover, as the series inverter injects a voltage in series with the utility voltage, a better controllability over load bus voltage is ascertained. This means that if utility voltages are non-sinusoidal or unbalanced, proper selection of magnitude and phase for the injected voltages will make the voltages at load bus to be balanced and sinusoidal. In addition to this, the load can be isolated from voltage sags, swells and flickers. Therefore, the series inverter can help to impose strict discipline at load bus and thus, the sensitive loads connected to the load bus will always see a stiff sinusoidal voltage source.

While performing the aforementioned tasks the phase of the injected voltage can vary from 0^0 to 360^0. This implies that the series inverter may have to supply or absorb real power in addition to the reactive volt-amperes. As a result, the series inverter cannot have a self-supporting DC link. In order to have real power balance, the series inverter has to be connected in conjunction with a shunt inverter sharing a common DC link. Thus, the adequate performance of UPQC is essentially determined by the proper control of shunt

inverter to regulate the DC bus voltage at a desired value. In this case the shunt inverter not only supplies or absorbs the requisite real power as demanded by the series inverter but also, at the same time, takes an active role in compensating the load current related power quality problems.

1.2.5 Control of UPQC

The active filters do not need to consume any real power to cancel current and voltage harmonics. The harmonic currents/ voltages to be cancelled can be considered as reactive power. In the control part, the control scheme/ algorithm of UPQC should assure – *i*) accurate generation of reference current signals for shunt inverter, *ii*) accurate generation of reference voltage signals for series inverter, *iii*) maintain the DC link voltage at constant set level, and *iv*) generation of proper switching pulses for both the inverter switches.

To generate accurate reference signals for UPQC, the control scheme may be based on the combination of one of the popular control strategies, such as, instantaneous reactive power theory, synchronous reference frame method, symmetrical component theory etc. The DC link voltage control can be achieved by adjusting the small amount of real power absorbed by the inverters.

Finally, the current modulator generates the switching patterns for inverter switches. Most of the modulation techniques used for APFs are based on pulse width modulation (PWM) strategies. The control modulator can be a periodical sampling control, Hysteresis band control, Triangular carrier control, space vector control, etc.

In this thesis work, many control approaches are proposed and discussed in detail.

1.3 Literature Review

The earliest systematic paper on active power filters can be dated back in 1976 written by Gyugyi L. and E. Strycula. This paper presents the PWM converters based family of APF circuits which can function either as ideal current or voltage generators. The APFs were classified as shunt APF to cancel out the harmonics generated by non-linear loads and series APF to cancel the harmonics present in the source voltage. Since then, there has been tremendous development in the field of active power filters with laboratory prototypes as well as field installations.

Although considerable research work in the area of shunt APF is taking place, as noticed from the available literature, the interest in the area of series APF is not that significant. This is due to the fact that it is difficult to compensate the load current harmonics using series APF and thus can only be used to compensate voltage harmonics. Additionally, the current harmonic issue is more dominant than the voltage harmonics. Better the profile of current drawn from the source, better would be the voltage at the distribution level. Interestingly, the improved current profile (close to sinusoidal) certainly helps to improve the PCC voltage profile, but, the reversal is not necessarily achievable. Moreover, the cost of series APF, due to the requirement of series transformer, compared to the shunt APF is noticeably high. Later on, the concept of hybrid active power filter has evolved in order to reduce the overall cost of APF system (Akagi, 1996; Singh *et al.*, 1999; El-Habrouk *et al.*, 2000).

The modern power distribution system is becoming highly vulnerable to the different power quality problems (Dugan *et al.*, 1996; Schlabbach *et al.*, 2001; Stones and Collinson, 2001; Sankaran, 2002). Therefore, some kind of compensation at all the power levels is becoming a common practice (Hingorani *et al.*, 2000; Emadi *et al.*, 2001; Ghosh *et al.*, 2002; Sood, 2004). At the distribution level, UPQC can be a significantly attractive solution to compensate several power quality problems.

UPQC (Fujita *et al.*, 1998) is a mitigating device that is similar in construction to a unified power flow controller (UPFC) (Gyugyi, 1992). Both the UPQC and UPFC employ two voltage source inverters (VSIs) that are connected to a common DC energy storage element, such as an inductor or capacitor. UPFC is employed in power transmission system where as UPQC is employed in a power distribution system, to perform the shunt and series compensation simultaneously. However, a UPFC only needs to provide balance shunt and/or series compensation, since a power transmission system generally operates under a balanced and distortion free environment. On the other hand, a power distribution system may contain DC components, distortion and unbalance. Therefore, a UPQC should operate under this environment while performing shunt and/or series compensation.

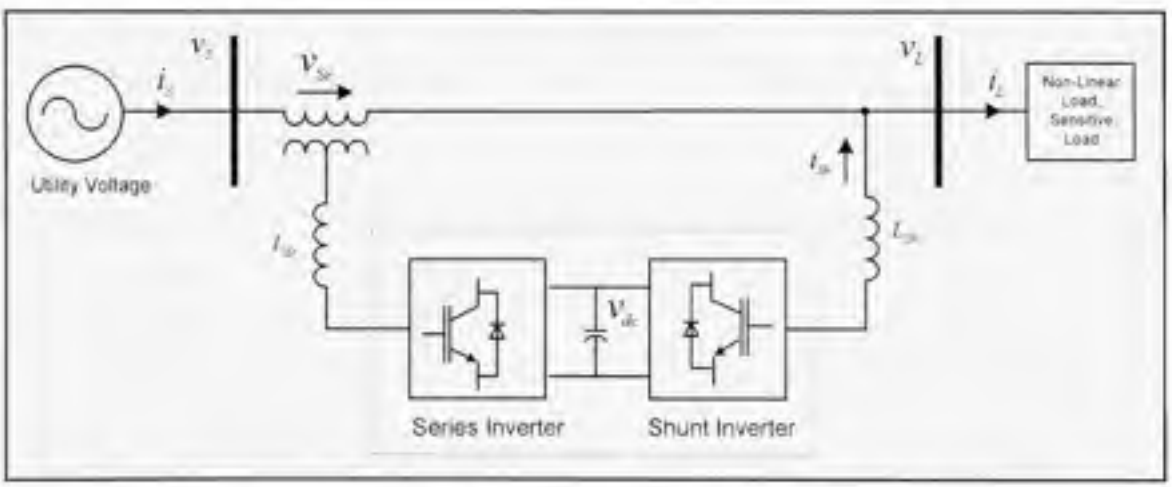


Figure 1.5 General block diagram representation of UPQC system.

The general block diagram representation of a UPQC based system is shown in Figure 1.5. The main purpose of a UPQC is to compensate for supply voltage power quality issues, such as, sags, swells, unbalance, flicker, harmonics, etc, and for load current power quality problems, such as, harmonics, unbalance, reactive current, etc. Different articles based on UPQC have been critically reviewed and a systematic study is provided in order to have a basic knowledge of various topologies and control techniques that are available in the literature depending on the system configuration, working conditions, application and load requirements. Various authors have given different name to this combined system of shunt and series APF, such as, Line Voltage Regulator/ Conditioner (LVRC) (Moran, 1989),

Unified Active Power Filter (UAPF) (Muthu and Kim, 1997), Universal Active Power Line Conditioner (UAPLC) (Aredes *et al.*, 1998), Universal Power Quality Conditioning System (UPQCS) (Graovac *et al.*, 2000).

1.3.1 Classification of UPQC

In this section, a UPQC is systematically classified considering different aspects, such as, the type of supply system, converter topology used for realization, UPQC system configuration and type of control strategies used. Figure 1.6 shows the pictorial view for the classification of UPQC.

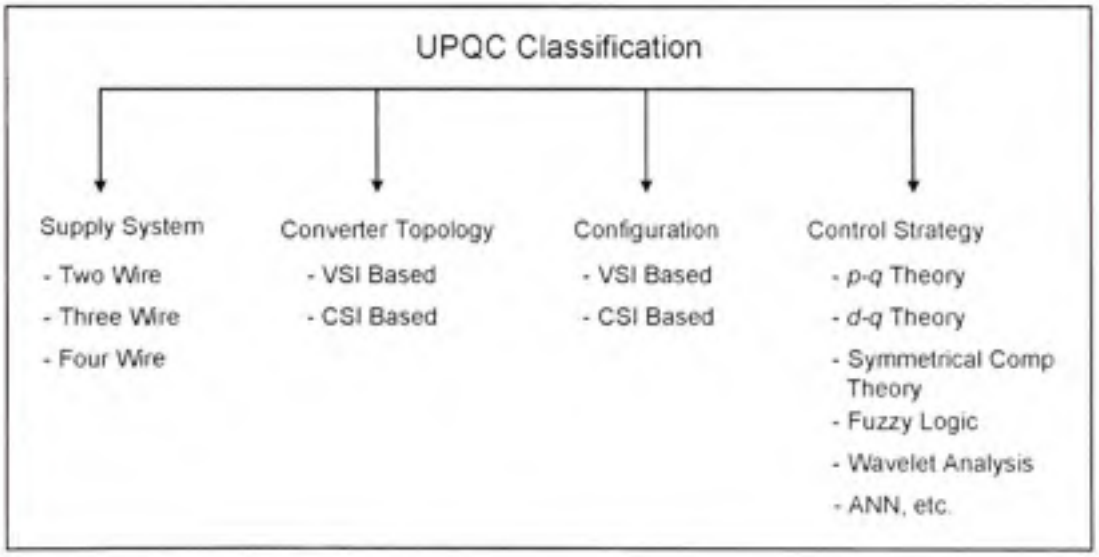


Figure 1.6 Pictorial view for the classification of UPQC.

1.3.1.1 Classification Based on Supply System

The loads or equipments can be broadly divided into single-phase or three-phase, supplied by single-phase (two wire) or three-phase (three-wire or four-wire) source of power. Therefore, to compensate the power quality problems UPQC can be classified based on the type of the supply system. Figure 1.7 shows a UPQC system configuration (Basu *et al.*, 2001; Nasiri and Emadi, 2003; Prieto *et al.*, 2005; Kazemi *et al.*, 2006b; Khoor and Machmoum, 2007) realized to compensate the power quality problems in single-phase supply system.

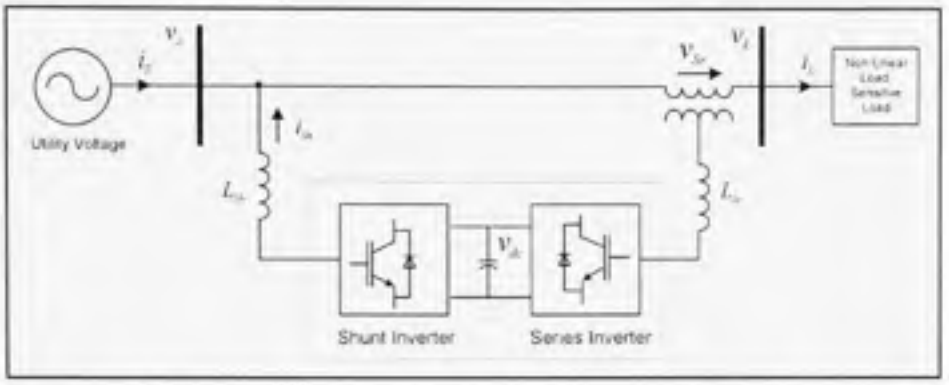


Figure 1.7 Single-phase two-wire UPQC system configuration.

There are several non-linear loads, such as, adjustable speed drives (ASD), fed from three-phase three-wire system. In such a case, a three-phase three-wire UPQC (most of the articles are based on this topology, few examples: Gu *et al.*, 2002; Monteiro *et al.*, 2003; Tlusty *et al.*, 2004; Landaeta *et al.*, 2006; Axente *et al.*, 2007) as shown in Figure 1.8 is used. On the other hand, many industrial plants often consist of combined loads, such as, a variety of single-phase loads and three-phase loads, supplied by three-phase four-wire supply. In such cases a three-phase four-wire UPQC can be utilized. There are two possible UPQC system configurations based on four-leg (Faranda *et al.*, 2002; Zhili *et al.*, 2006; Li *et al.*, 2007) or split capacitor topology (Chen *et al.*, 2004). Figure 1.9 shows a three-phase four-wire split capacitor topology based UPQC system configuration

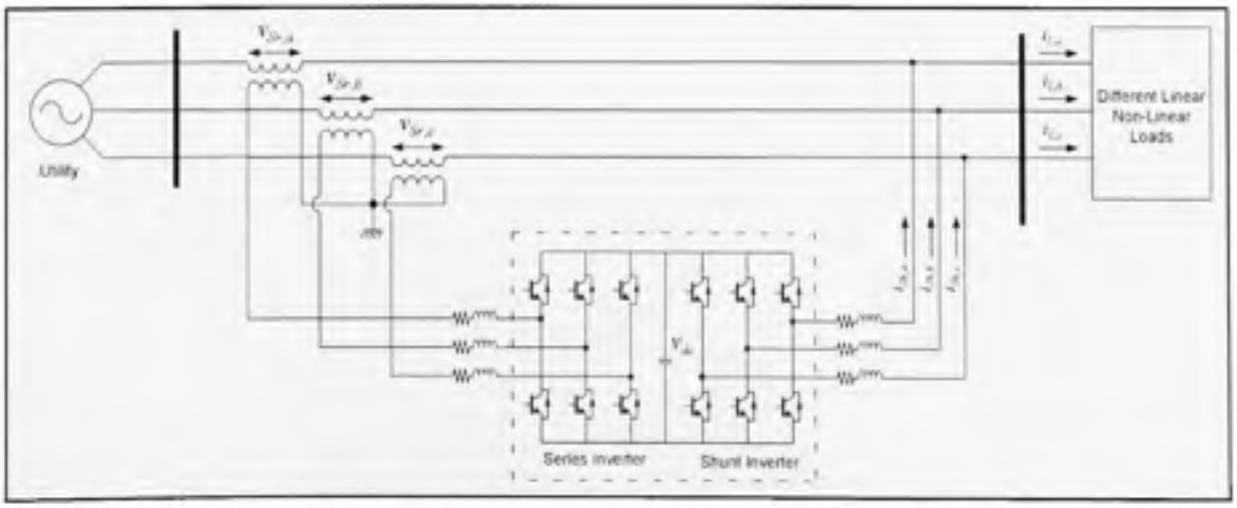


Figure 1.8 Three-phase three-wire UPQC system configuration.

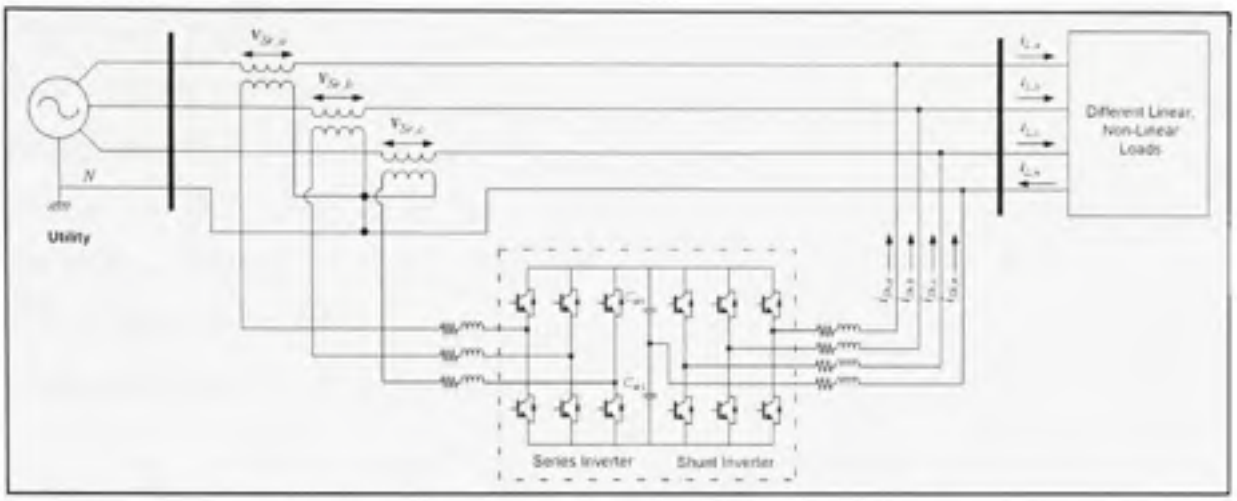


Figure 1.9 Three-phase four-wire UPQC system configuration.

1.3.1.2 Classification Based on Converter Topology

As mentioned before, in a UPQC, both the shunt and series inverters share a common DC link. The UPQC may consist of pulse width modulated (PWM) current source inverters (CSI) (Moran, 1989), which share a common energy storage inductor to form the DC link. Here, the DC current in the inductor is regulated such that the average input power is equal to the average output power plus the power losses in the UPQC. The UPQC based on CSI topology is not popular because of higher losses, expense and the fact that it can not be used in multilevel mode operation. Figure 1.10 shows the block diagram representation of a CSI based UPQC system configuration.

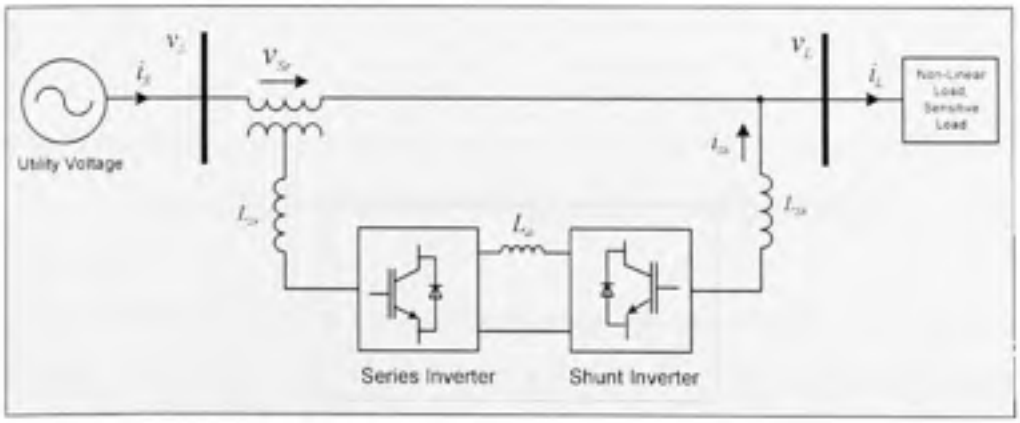


Figure 1.10 CSI based UPQC system configuration.

In the other topology, the UPQC consists of PWM voltage source inverter (VSI), which shares a common energy storage capacitor. This is the most common and popular converter topology for UPQC. All the references except work done by Moran, 1989, utilize the VSI topology for UPQC. Here the voltage across the capacitor acts as source of DC power in order to have suitable UPQC performance. The block diagram representation of a VSI based UPQC system configuration is given in Figure 1.5. The CSI or VSI based UPQC system can be realized as single-phase or three-phase system.

1.3.1.3 Classification Based on UPQC Configuration

There are two possible ways to connect the UPQC at the point of common coupling (PCC), depending on the placement of shunt inverter *w.r.t.* the series inverter. Figure 1.5 represents the right shunt UPQC system configuration and which is the dominant system configuration used by the researchers, for example: Vilathgamuwa, 1998; Hu, 2000; Monteiro, 2003; Hongchun, 2005; Chakraborty, 2007). Figure 1.11 shows the left shunt UPQC system configuration (Fujita, 1998; Elnady, 2002; Ghosh, 2003; Jayanti, 2007).

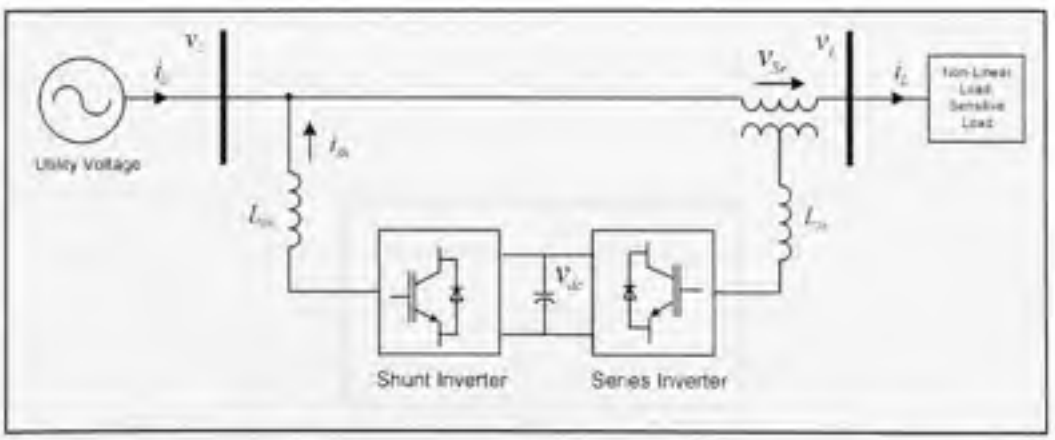


Figure 1.11 Left shunt UPQC system configuration.

The right shunt UPQC structure is the most common structure due to zero power injection/ absorption mode. Moreover, as the shunt inverter compensates the harmonics in the load, the current flowing through the series inverter (series transformer) would be sinusoidal in the right shunt UPQC configuration. Thus, the right shunt UPQC could give a better

performance under a highly distorted condition. The left shunt UPQC structure is sometimes used in special cases, for example, to avoid the interference between the shunt inverter and passive filters. The right shunt and the left shunt UPQC can be realized using CSI or VSI topology and used for single-phase and three-phase systems.

1.3.1.4 Classification Based on Control Strategy

There are many control strategies that can be used for UPQC, such as, Instantaneous Reactive Power Theory (or Three-phase *p-q* Theory), Synchronous Reference Frame Method (*d-q* Theory), Deadbeat control, Fuzzy Logic control, Artificial Neural Network (ANN) based control, Symmetrical Component Theory, etc. The UPQC controller can be based on one or a combination of the above control strategies. The popular control strategies, algorithms or approaches available in the literature are briefly discussed in the next section.

1.3.2 UPQC Control Strategies

Control strategy is the heart of any power electronics based system. It is the control strategy which decides the behavior and the desired operation of a particular device. The effectiveness of the APF system (shunt, series or UPQC) solely depends upon its control algorithm. In case of UPQC, the control strategy determines the reference signals (current and voltage) and thus decides the switching instants of inverter switches, such that the desired performance can be achieved. One of the distinguishing features of APF is that it does not consume any active power from the source. However, in actual practice there is always some power consumption to overcome the switching losses. Some of the important control strategies are discussed in the following section.

1.3.2.1 Frequency Domain Compensation Method

This method is based on the Fast Fourier Transformation (FFT). The harmonic content of voltage or current is obtained by extracting AC fundamental component using a low pass filter. Then the FFT of harmonics is carried out and coefficients for each harmonic are

computed. The disadvantage of this method is large computation time and hence, delay for the calculation of FFT. In many cases a minimum one whole period of waveform is needed to perform the FFT. Therefore, the controllers based on frequency domain methods are not popular for active filter application, because the response time plays a crucial role. The UPQC controller realized using frequency domain method can be found in articles by Tlusty *et al.*, 2004 and Kwan *et al.*, 2007.

1.3.2.2 Time domain Compensation Methods

Control methods for active filters in the time domain are based on instantaneous derivation of compensating commands in the form of either voltage or current signals. There are a large number of control methods in the time domain. Only the most popular are briefly discussed below.

- Instantaneous Reactive Power Theory

This method is also known as a three-phase *p-q* theory, proposed by Akagi *et al.*, 1984. This theory has proven that, with proper control of VSI, without energy storage device, the harmonics generated by non-linear load, and/or the load reactive power can be compensated effectively. The concept of 3-φ *p-q* theory is based on a variable transformation from *a-b-c* reference frame to α-β co-ordinates. Once the voltages and currents are transformed into the α-β co-ordinates, the instantaneous total load active as well as the reactive powers are computed. The fundamental and the harmonics quantities, from the total instantaneous active and reactive powers, are then separated using a low pass (LPF) or high pass filter (HPF). For load reactive power and current harmonic compensation, the computed instantaneous total reactive power and the instantaneous harmonic part of the load active power are considered, and transferred back to the *a-b-c* frame as reference APF signals.

The most significant advantage of *p-q* theory is that the real and reactive powers associated with fundamental components are dc quantities. These quantities can easily be extracted

using a low pass filter. Due to the DC signal extraction, filtering of signal in the α-β reference frame is insensitive to any phase shift errors introduced by low pass filter. But this method works properly with three-phase balanced system and when three-phase voltages are pure sinusoidal without harmonics, otherwise the results are poor.

This theory has been extensively used in the three-phase APF (three-wire and/or four-wire) system. UPQC controller based on three-phase *p-q* theory can be found in articles by Fujita *et al.*, 1998; Aredes *et al.*, 1998, 2005; Liu *et al.*, 2003; Zhili *et al.*, 2006; Li *et al.*, 2007 and Turunen *et al.*, 2007.

- Synchronous Reference Frame Method (*d-q* Theory)

This method is also known as *d–q* method and is based on *a–b–c* to *d–q* transformation, proposed by Bhattacharya *et al.*, 1995. This method can be used to extract the harmonics contained in the supply voltages or currents. For current harmonics compensation, the distorted currents are first transferred into two-phase stationary co-ordinates using α-β transformation (same as in *p-q* theory). After that, the stationary frame quantities are transferred into synchronous rotating frame using cos and sin functions from the PLL. The sin and cos functions help to maintain the synchronization with supply system. Similar to the *p-q* theory, using a LPF or HPF, the harmonics and fundamental components are separated easily and transferred back to the *a–b–c* frame as reference signals for the APF.

In *p-q* theory, to compute the instantaneous active and reactive powers the knowledge of both the source voltage and the load current is essential, while, the *d-q* theory deals with the current independent of the supply voltage (or vice versa). Therefore, the *d-q* theory performs better under distorted supply voltages. The UPQC controller based on *d-q* transformation can be found in Vilathgamuwa *et al.*, 1998; Graovac *et al.*, 2000; Hu *et al.*, 2000; Li *et al.*, 2000; Elnady *et al.*, 2001b; Chen *et al.*, 2004; Cheng *et al.*, 2004 and Strzelecki *et al.*, 2005.

- Symmetrical Component Theory

An unbalance in the three-phase system has been generally treated through symmetrical components. In this theory, a set of unbalance ac voltage or current phasors are converted to three-phase balance phasors. Therefore this approach is very useful for mitigating unbalance problem in supply voltage and thus can be used to extract the reference voltage signals for series APF.

Here, the three-phase voltages are resolved into positive, negative and zero sequence components by using *a-b-c* to *0-1-2* plane transformation, given by,

$$\begin{bmatrix} v_{a0} \\ v_{a1} \\ v_{a2} \end{bmatrix} = \frac{1}{\sqrt{3}} \begin{bmatrix} 1 & 1 & 1 \\ 1 & a & a^2 \\ 1 & a^2 & a \end{bmatrix} \cdot \begin{bmatrix} v_a \\ v_b \\ v_c \end{bmatrix} \tag{1.3}$$

The reference signals are obtained by making positive sequence component, v_{a1} equal to zero. Then, by taking inverse transformation the reference signals, which will be sum of unwanted negative and zero sequence components, are computed. The UPQC based on the above approach (Chen *et al.*, 2001; Haque *et al.*, 2002; Gu *et al.*, 2002; Ghosh *et al.*, 2004; Esfandiari *et al.*, 2004; Kazemi *et al.*, 2006b) can compensate the voltage sags, swells, unbalance and flicker.

1.3.3 Additional Significant Research Work

The following section gives a brief outline of the important work carried out in the area of UPQC by different researchers.

Vilathgamunla *et al.*, 1998, have modeled UPQC using the state space averaging technique to analyze its behavior under non-linearities due to load and source disturbance condition. The delay in detection and calculation of reference signals makes it difficult for either series

inverter or shunt inverter to achieve the perfect voltage and current compensation. A predictive control method, proposed by Chen *et al.* (2000) can be used to improve the compensation effects. This method is based on taking a calculated value (the component to be compensated) of pervious period as the compensating value of next period. Ghosh *et al.* (2003) have used the pole shift control technique. It's a discrete-time control technique in which the closed-loop poles are chosen by radially shifting the open loop poles towards the origin. The kVA rating issues (Chen *et al.*, 2001; Ryoo *et al.*, 2004; Jayanti *et al.*, 2006), compensator losses (Faranda *et al.*, 2002) and protection issues (Chae *et al.*, 2001), etc., also have been considered for optimized design of the UPQC. Faranda *et al.* (2002) have given a procedure to calculate the operating losses of inverters. Kwan *et al.* (2007) have proposed a model predictive control scheme for the UPQC. It is a frequency domain method which utilizes the Kalman filters to extract the source voltage fundamental and the load current harmonics components. A constant frequency integration control approach, based on one cycle control of switching converters concept, is given for the UPQC by Vadiraiacharya *et al.* (2006).

As mentioned in section 1.2.4, the control of DC link voltage plays an important role in achieving the desired UPQC performance. Several control techniques have been utilized to maintain the DC link voltage at a constant level. During the system dynamic conditions, for example, sudden load change, voltage sag etc., the DC link feedback controller should act immediately to restore the DC link voltage at set reference value with a minimum delay as well as lower overshoot. The PI controller based DC link voltage controller is simple to implement and hence widely used by the researches (Vilathgamuwa *et al.*, 1998; Hu *et al.*, 2000; Jianjun *et al.*, 2002; Correa *et al.*, 2005; Sundeepkumar *et al.*, 2006; Xun *et al.*, 2007). However, the response time of PI based UPQC systems is slower in nature and thus, to improve the response time, several other techniques have been suggested by different researchers, such as, a fuzzy logic based controller (Singh *et al.*, 1998; Chakraborty *et al.*, 2005; Laxmi *et al.*, 2006), $PI^{\lambda}D^{\mu}$ controller (Zuquan *et al.*, 2008), optimized controller (Zhang *et al.*, 2007).

Artificial neural networks (ANN) technique can handle the multi-input multi-output control system effectively. Thus, an ANN technique can be utilized to develop the controller for the UPQC to compensate different voltages and currents. A feed forward ANN scheme is reported by Banaei *et al.* (2006) and Tey *et al.* (2002b), to separate the harmonics contents in the non-linear load. Ming *et al.* (2006) have suggested a Levenberg-Marquardt optimized back propagation ANN controller for UPQC.

The time domain and frequency domain techniques have certain drawbacks and limitations. To overcome their problems, wavelet analysis technique, a new tool for fault detection, localization and classification of different power system transients is proposed by certain researchers. Elnady *et al.* (2001) and Forghani *et al.* (2007) have introduced a control algorithm based on wavelet transformation for UPQC to compensate the load current harmonics and voltage sags. By using multi resolution analysis, the wavelet transform can represent a time varying signal in terms of frequency component. It maps a one-dimensional (1D) signal of time into a two-dimensional (2D) signal of time and frequency. Thus, the wavelet analysis can be used to extract the disturbance in current or voltage to generate the reference signal to drive the shunt active and series inverters. So far, the performance of ANN and wavelet techniques, when applied to active power filters, has carried out through simulation studies. The real-time implementations of these approaches need to be done for practical applications.

Kamran *et al.* (1995) and Chen *et al.* (2001b), have proposed a technique based on deadbeat control, wherein, the UPQC converter combination is treated as a single unit. An inverse system model is used to generate deadbeat control response for both the input current and output voltage. In this case, converters can react to the change in PCC voltages or currents. The overall system has been modeled as a single multi-input, multi output system. The resultant control includes an automatic feed forward of the disturbance resulting from the dynamics of the loading converter. This results in improved control performances over the separately controlled converters and/or reduced inter-converter energy storage. The deadbeat control algorithm can easily be implemented on a single microprocessor at moderate

switching frequencies (up to 10 kHz). The system has a fast dynamic response and high steady state accuracy. The major drawback of this control strategy is that it cannot be applied for systems having unstable or marginally stable open loop poles. Also for systems with very low damping, a deadbeat control strategy can result in large oscillations in the output.

The voltage sag on the system is one of the most important power quality problems that a UPQC should compensate effectively. Many researchers have given special attention on the voltage sag compensation using different approaches. Three significant control approaches can be found to control the sag on the system: i) active power control approach in which an in-phase voltage is injected through series inverter (Vilathgamuwa *et al.*, 1998; Gong *et al.*, 2002; Khoor *et al.*, 2005; Han *et al.*, 2006; Kazemi *et al.*, 2006), ii) reactive power control approach in which a quadrature voltage is injected (Basu *et al.*, 2002), and iii) a minimum VA loading approach in which a series voltage is injected at a certain angle (Yu *et al.*, 2004; Kolhatkar *et al.*, 2007; Kisek *et al.*, 2007). Among the above stated three approaches the quadrature voltage injection requires a maximum series injection voltage, whereas, the in-phase voltage injection requires the minimum voltage injection magnitude. However the current drawn by the shunt inverter, to maintain the DC link voltage at a constant level and to maintain the overall power balance in the network, plays an important role in the overall UPQC VA loadings. Besides the sag on the system, the flicker and unbalance caused by the arc furnace are one of the most severe power quality problems. The UPQC could be the most effective power quality conditioner to solve the flicker problems caused by an arc furnace load (Fujita *et al.*, 1998; Elnady *et al.*, 2001; Ghosh *et al.*, 2003; Tlusty *et al.*, 2004; Esfandiari *et al.*, 2004).

An interesting UPQC system configuration, for medium voltage applications, is proposed by Han *et al.* (2006a). The configuration is realized by using several H-bridge modules. The H-bridge modules for shunt part of UPQC are connected in series through a multiwinding transformer, while, the H-bridges in the series part are directly connected in series and inserted in the distribution line without a series injected transformer. Similar topology has been considered by Mufioz *et al.* (2007). A double cascade H-bridge module would require

four H-bridges (16 IGBT's) for each of the phases, and therefore, total of 48 IGBT's would be required to realize the proposed structure. As the number of modules increase the voltage handled by each individual H-bride would reduce and thus, can be useful in the medium voltage application. Rubilar *et al.* (2007) have realized a multilevel UPQC based on a three-level neutral point clamped (NPC) topology. It can be a good choice for medium or high power applications due to the reduction in voltage across each of the semiconductor devices by half. A three-level topology requires double semiconductor devices (24 IGBTs) as that of the two-level UPQC system. However, the cost involved in realizing the above mentioned multilevel topologies would be considerable high. Additionally, the increased modules result into increased number of sensors, complex control circuitry, higher losses, and additional cost for multi-winding transformer for shunt part.

Obukhov *et al.* (2003) have introduced a concept of transformerless UPQC. The transformer used to connect the series inverter in the line is replaced by a capacitor. Removal of the transformer eliminates the isolation between the two voltage sources (supply voltage and voltage generated by UPQC) and thus, often is not considered by other researchers. Additionally, without a transformer the turn ration between the series inverter generated voltage and actual injected voltage in the line acts as one. This further reduces the possibilities of reducing the current ratings of series inverter switches. Generally a suitable transformer ratio is always considered in UPQC based applications to reduce the current handled by the series inverter. Jindal *et al.* (2007) have introduced a system configuration, termed as an interline UPQC (IUPQC) to improve the power quality of two independent feeders (lines) in a distribution system, simultaneously. The shunt inverter of UPQC is connected across one feeder, while, the series inverter is connected in series with the line, through series transformers, in the other feeder. The UPQC under such a configuration can be utilized to regulate the bus voltage of one of the feeders and to protect a sensitive load on the other feeder.

Recently, increased attention is being given on evaluating the UPQC control algorithm effectiveness and performance evaluation under different load and supply voltage conditions

with experimental investigations in the laboratory (Basu *et al.*, 2001; Liu *et al.*, 2003; Chen *et al.*, 2003; Ryoo *et al.*, 2004; Prieto *et al.*, 2005; Correa *et al.*, 2005; Strzelecki *et al.*, 2005; Han *et al.*, 2006; Kolhatkar *et al.*, 2007). A 250kVA UPQC system is developed and under field test at Centre for the Development of Advanced Computing (C-DAC), Trivandrum, India (Suneepkumar *et al.*, 2006). Additional significant UPQC prototypes: 20kVA (Fujita *et al.*, 1998), 10kVA (Li *et al.*, 2007), 10kVA (Kisck *et al.*, 2007), 6kVA (Zhang *et al.*, 2007) and 4.5 kVA (Aredes *et al.*, 2005).

1.4 Steady-State Power Flow Analysis of UPQC

In this section, a comprehensive analytical study is presented. The aim of this analysis is to develop the fundamental background and thus to lay down the necessary foundation to ease the concepts presented in the thesis work. It also helps to understand how the active and reactive power flows between source, UPQC and the load, under some of the important conditions.

Figure 1.12 shows the equivalent circuit of UPQC. The gird voltage and gird current are denoted by v_{Grid}, and i_{Grid}, respectively. The voltage at PCC is referred as source voltage v_S (some researchers refer it as terminal voltage). The load voltage and load current are represented by v_L, and i_L, while, the voltage and current injected by UPQC are mentioned as v_{Sr}, and i_{Sh}. R_S and L_S denote the sum of the source and line resistance and inductance.

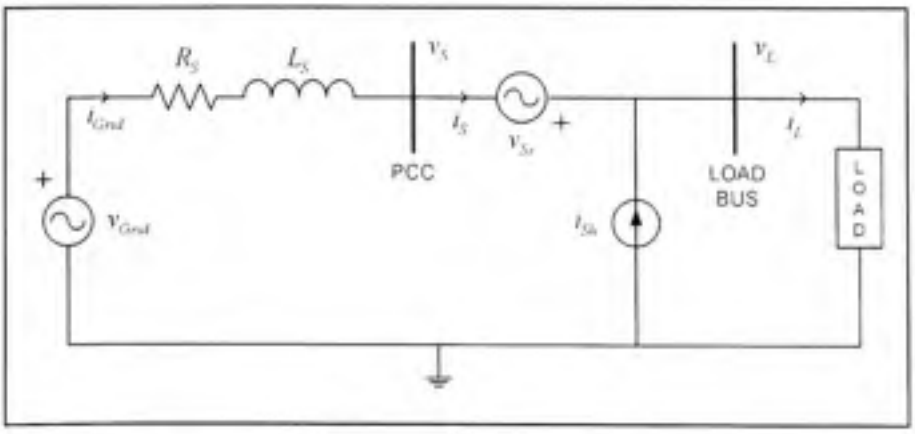


Figure 1.12 Equivalent circuit of a UPQC

Assumptions:

- The powers due to harmonics quantities are negligible as compared to the power at fundamental component, therefore, the harmonic power is neglected.
- Steady state operating analysis is done on the basis of fundamental frequency component only.
- No losses are associated with UPQC.

The UPQC is controlled in such a way that the voltage at load bus is always sinusoidal and at desired magnitude. Therefore, the voltage injected by series inverter should be equivalent to a controlled voltage source whose magnitude is equal to the difference between the supply voltage and the ideal load voltage. The function of shunt inverter is to maintain the DC link voltage at constant level. In addition to this, the shunt inverter also provides the VAR required by the load such that the input power factor will be unity. Therefore, only fundamental active power will be supplied by the source.

The voltage injected by series inverter can vary from 0^{o} to 360^{o}. Depending on the voltage injected by series inverter, there can be a phase angle difference between the load voltage and the source voltage. In the following analysis, the load voltage is assumed to be in-phase with source voltage irrespective to any variation in supply voltage. This is done by injecting the series voltage in-phase or out of phase *w.r.t.* the source voltage, during voltage sag and swell conditions, respectively. This suggests the possible real power flow through the UPQC. Depending on the relative magnitude of source voltage over the load voltage, voltage injected by series inverter could be positive or negative, absorbing or supplying the real power. Under these conditions, the series inverter does not handle any reactive power and the shunt inverter alone supplies the load reactive power.

Taking the load voltage, v_L, as a reference phasor and supposing the lagging power factor of the load $\cos\varphi_L$, we can write,

$$\overline{v}_l = V_l \angle 0^{o} \tag{1.4}$$

$$\bar{i}_L = I_L \angle -\varphi_L \tag{1.5}$$

$$\bar{v}_S = V'_L(1+k_f)\angle 0^0 \tag{1.6}$$

The small case letters for voltages, currents and powers denote the instantaneous values, while, the capital letters are used to represent the peak values. In (2.15) factor k_f is the ratio of magnitude fluctuation of source voltage which can be defined as,

$$k_f = \frac{V'_S - V'_L}{V'_L} \tag{1.7}$$

The voltage injected by series inverter should be equal to,

$$\bar{v}_{Se} = \bar{v}_L - \bar{v}_S = -k_f . V'_L \angle 0^0 \tag{1.8}$$

The UPQC is assumed to be lossless and therefore, the active power demanded from the load (P_L) is equal to the active power input at PCC (P_S). The UPQC provides a unity power factor source current, therefore, for a given load condition the input active power can be expressed by the following equations,

$$P_S = P_L \tag{1.9}$$

$$V_S . I_S = V'_L . I_L . \cos\varphi_L \tag{1.10}$$

$$V_L(1+k_f) . I_S = V'_L . I_L . \cos\varphi_L \tag{1.11}$$

$$I_S = \frac{I_L}{1+k} . \cos\varphi_L \tag{1.12}$$

The above equation suggests that the source current I_S is indirectly proportional to factor k, since, φ_L and I_L are load characteristics and are constant for a particular type of load. The active (P_{Sr}) and reactive power (Q_{Sr}) handled by the series inverter can be expressed as follow:

$$P_{Sr} = V_{Sr}.I_S.\cos\varphi_S \tag{1.13}$$

$$P_{Sr} = -k_f.V_L.I_S.\cos\varphi_S \tag{1.14}$$

$$Q_{Sr} = V_{Sr}.I_S.\sin\varphi_S \tag{1.15}$$

φ_S =0, since UPQC is maintaining unity power factor.

$$P_{Sr} = V_{Sr}.I_S = -k_f.V_L.I_S \tag{1.16}$$

$$Q_{Sr} \cong 0 \tag{1.17}$$

The current provided by the shunt inverter (i_{Sh}) is the difference between the input source current (after compensation) and the load current, which includes the load harmonics current and the reactive current.

Therefore, we can write:

$$\bar{i}_{Sh} = \bar{i}_S - \bar{i}_L \tag{1.18}$$

$$\bar{i}_{Sh} = I_S\angle 0^0 - I_L\angle -\varphi_L \tag{1.19}$$

$$\bar{i}_{Sh} = I_S - (I_L.\cos\varphi_L - jI_L.\sin\varphi_L) \tag{1.20}$$

$$\bar{I}_{Sh} = (I_S - I_L.\cos\varphi_L) + jI_L.\sin\varphi_L = I_{Sh}\angle\varphi_{Sh} \tag{1.21}$$

φ_{Sh} represents the phase angle of shunt current injected *w.r.t.* the source voltage.

The active (P_{Sh}) and reactive power (Q_{Sh}) handled by the shunt inverter can be expressed as follow:

$$P_{Sh} = V_L.I_{Sh}.\cos\varphi_{sh} = V_L.(I_S - I_L.\cos\varphi_L) \tag{1.22}$$

$$Q_{Sh} = V_L.I_{Sh}.\sin\varphi_{Sh} = V_L.I_L.\sin\varphi_L \tag{1.23}$$

Based on above analytical study the different possible modes of active and reactive power flow between source, load and UPQC are discussed in following subsections.

1.4.1 Case-I: Active-Reactive Power Flow during Normal Working Condition

Under the normal working condition (V_S=V_L), without the voltage sag or swell, the factor k_f from (1.7) will be zero. UPQC does not exchange any active power through UPQC. In this condition, if the UPQC is not connected in the circuit, the reactive power required by the load (Q_L) is completely supplied by the source (Q_S). When the UPQC is connected to the network with the shunt inverter in operation, the reactive power required by the load is now provided

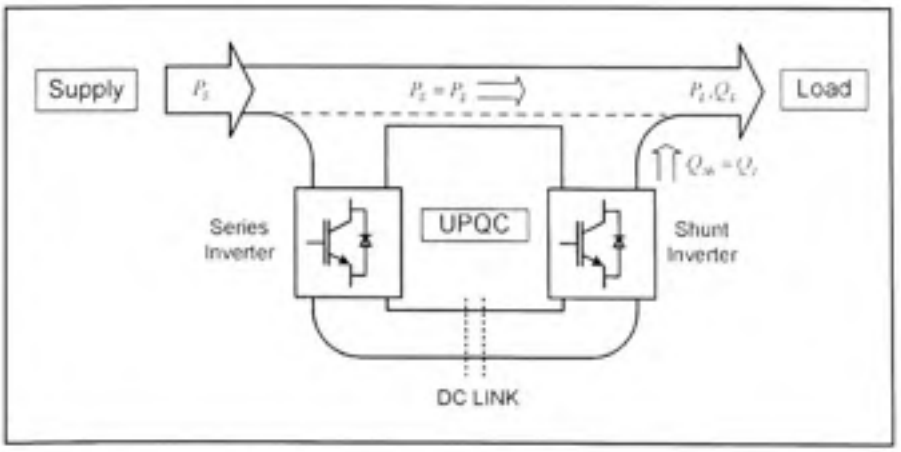


Figure 1.13 Active and reactive power flow during steady-state condition.

by the shunt inverter alone (Q_{Sh}). Thus, the reactive power burden on the source is handled by shunt inverter ($Q_S = 0$). So, as long as the shunt inverter is ON, it is responsible to supply the load reactive power irrespective to supply voltage distortion and variations. In this case, the series inverter is not taking any active part in supplying the load reactive power. The active and reactive power flow during the normal working condition is shown in Figure 1.13.

1.4.2 Case-II: Active-Reactive Power Flow during Voltage Sag Condition

If $k_f < 0$, i.e. $V_S < V_L$, then according (1.7) and (1.16), P_{Sr} will be positive. It means series inverter supplies the active power to the load. This condition is possible during the utility voltage sag. From (1.12), I_S will be more than the normal rated current. Thus, we can say that the required active power is taken from the utility itself by taking more current so as to maintain the power balance in the network and to keep the DC link voltage at desired level. This active power flows from the source to shunt inverter, from the shunt inverter to series inverter via the DC link, and finally from the series inverter to the load.

Thus, the load would get the required rated power even during voltage sag condition. Therefore, in such cases the active power absorbed by the shunt inverter from the source is equal to the active power supplied by the series inverter to the load. As mentioned in Case-I, the load reactive demand is supported by the shunt inverter in addition to the active exchange. The overall active and reactive power flow is shown in Figure 1.14.

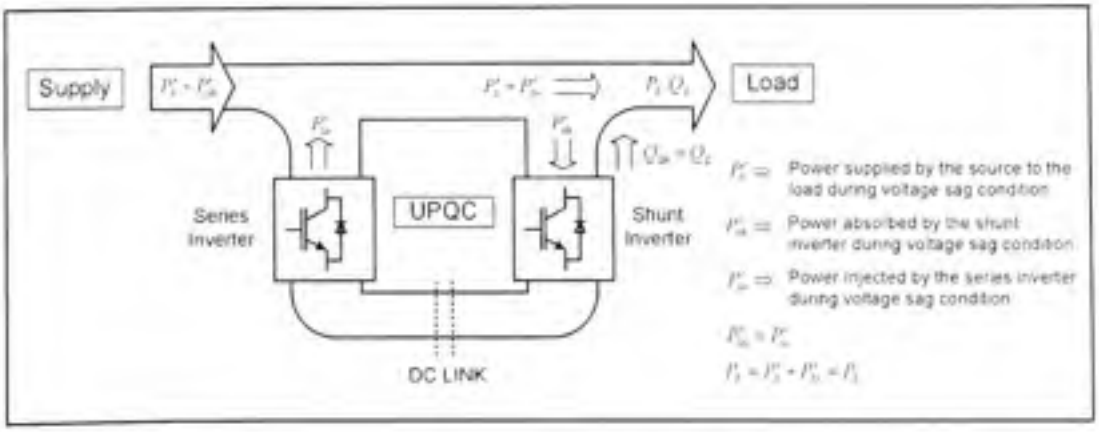


Figure 1.14 Active and reactive power flow during voltage sag condition.

1.4.3 Case-III: Active and Reactive Power Flow under Voltage Swell Condition

If $k_f > 0$, i.e. $V'_S > V'_L$, then from (1.7) and (1.16), P_{Sr} will be negative. This means that the series inverter is absorbing the extra real power from the source. This is possible during the voltage swell condition. From (1.12), I_S will be less than the normal rated current. In other words we can say that the UPQC feeds back the extra power to the supply system. The overall active and reactive power flow is shown in Figure 1.15.

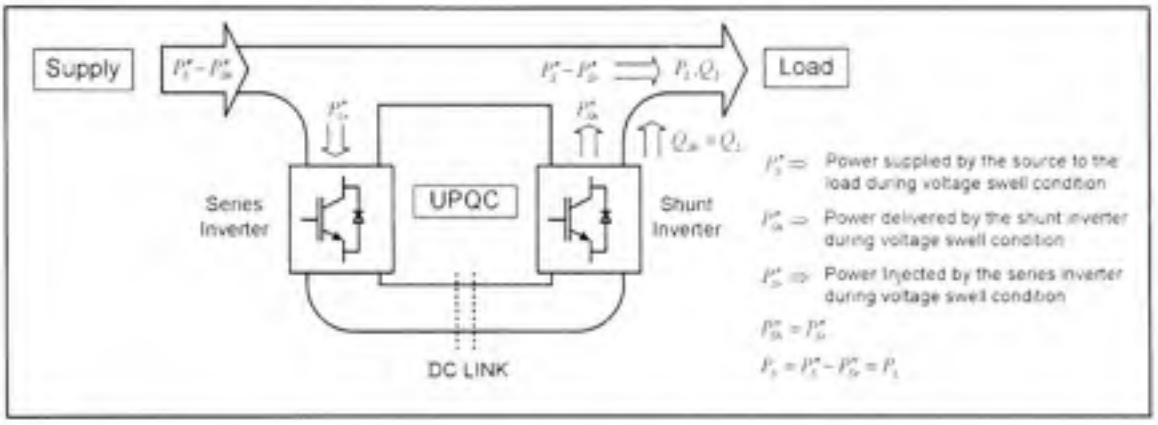


Figure 1.15 Active and reactive power flow during voltage swell condition.

1.4.4 Case-IV: Active-Reactive Power Flow under Distorted Voltages

If the voltage at PCC is distorted containing several harmonics, in such cases, the series inverter injects voltage equal to the sum of the harmonics voltage but in opposite direction. Thus, the sum of voltage injected by series inverter and distorted voltage at PCC will get cancelled out. During this voltage harmonic compensation mode of operation the series inverter does not consume any active power from the sources. This is due to the fact that the harmonics quantities contribute to the reactive power.

1.4.5 Case-V: Active-Reactive Power Flow under Distorted Load Currents

If the load is a non-linear producing harmonics, in such cases the shunt inverter injects current equals to the sum of harmonics current but in opposite direction, and thus canceling

out current harmonics generated by non linear load. During this current harmonics compensation mode of operation the shunt inverter does not consume real power from the source since it injects only harmonics current.

1.4.6 Phasor Representations of Different Operating Conditions

The phasor representations of the above discussed conditions are shown in the Figure 1.16 Figure 1.16 (a1) – (d1), and Figure 1.16 (a2) – (d2), for inductive and capacitive type of loads, respectively. Figure 1.16 (a1) represents the normal working condition, considering the source voltage V_S as a reference phasor. φ_L is lagging power factor angle of load. During this condition I_S is exactly equal to the I_L as no compensation is provided. When shunt inverter is put into the operation, it supplies the required load VARs by injecting the leading current such that the source current is in in-phase with the source voltage (Figure 1.16 (b1)). The phasor representations during voltage sag and voltage swell conditions on the system are shown in the Figure 1.16 (c1) and (d1), respectively. The deviation of shunt compensating current phasor from quadrature relationship with source voltage suggests that there is certain amount of active power involved during these conditions. This active power can be determined using (1.22).

Phasor in Figure 1.16 (a2) represents the normal working condition, considering leading power factor angle of the load. During this condition I_S will be exactly equal to the I_L. When shunt inverter is put into the operation, it cancels out the VARs generated by load by injecting a 90^0 lagging current such that the source current is in in-phase with the terminal voltage (Figure 1.16 (b2)). The phasor representations during voltage sag and voltage swell conditions on the system are shown in Figure 1.16 (c2), and Figure 1.16 (d2), respectively.

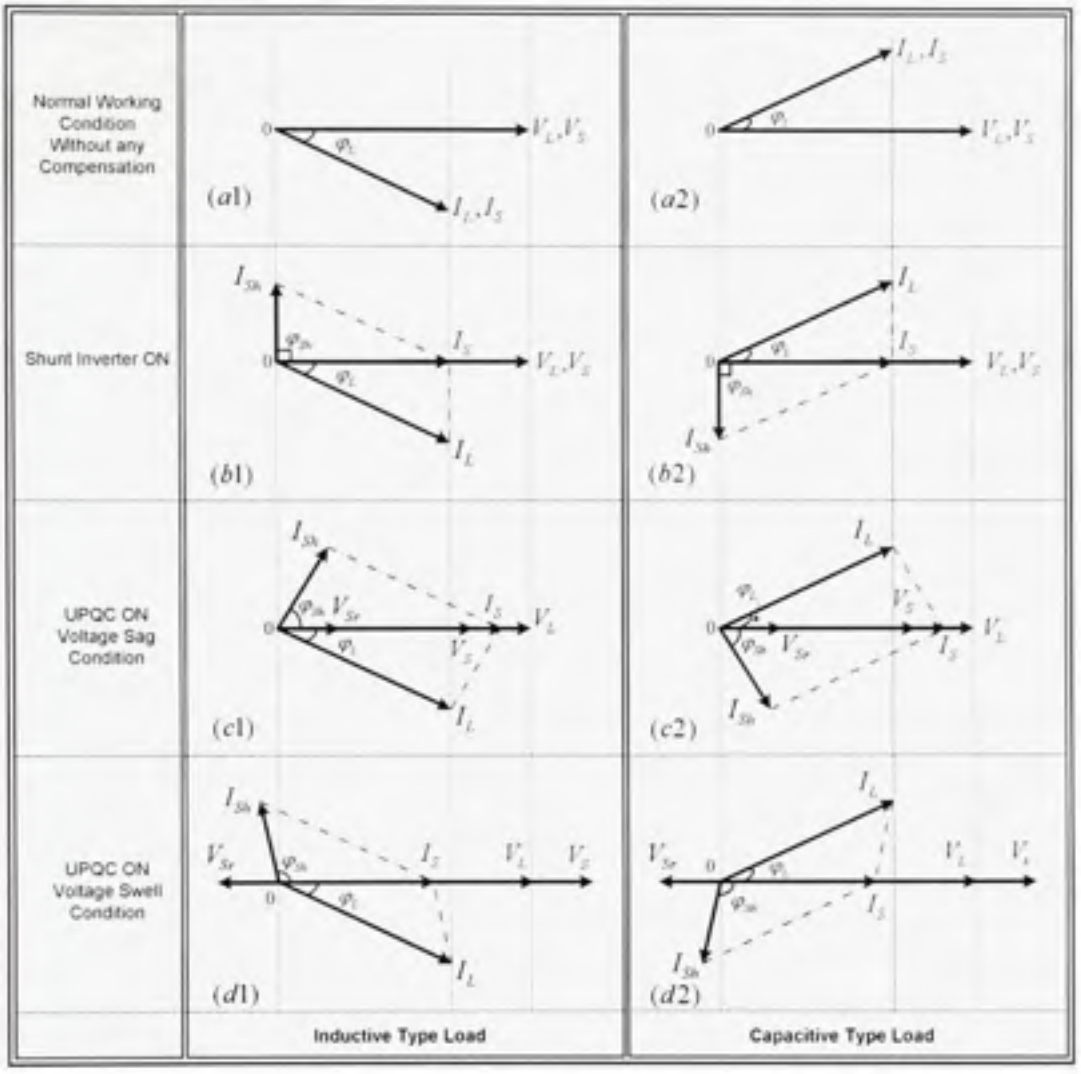


Figure 1.16 Phasor representation of all possible conditions.

1.4.7 UPQC Operation from 0^{o} to 360^{o}

As noticed from Figure 1.16, the shunt injected current can have different phase angles, φ_{Sh}, depending on the voltage deviation as well as the type of the load. The detailed variation of angle φ_{Sh} during different modes of operations of UPQC is systematically represented by zones in Figure 1.17. The figure consists of seven zones of operations. The x-axis represents the reference load voltage, whereas, the injected shunt inverter current phase angle φ_{Sh} can vary from 0^{0} to 360^{0}. Zones–I, II, and III represent the cases of pure resistive, inductive, and capacitive loads, respectively. If the load is pure resistive, shunt inverter need not to inject

any compensating current since there is no reactive power demand from the load. For this condition, the operating point is represented by origin "*O*".

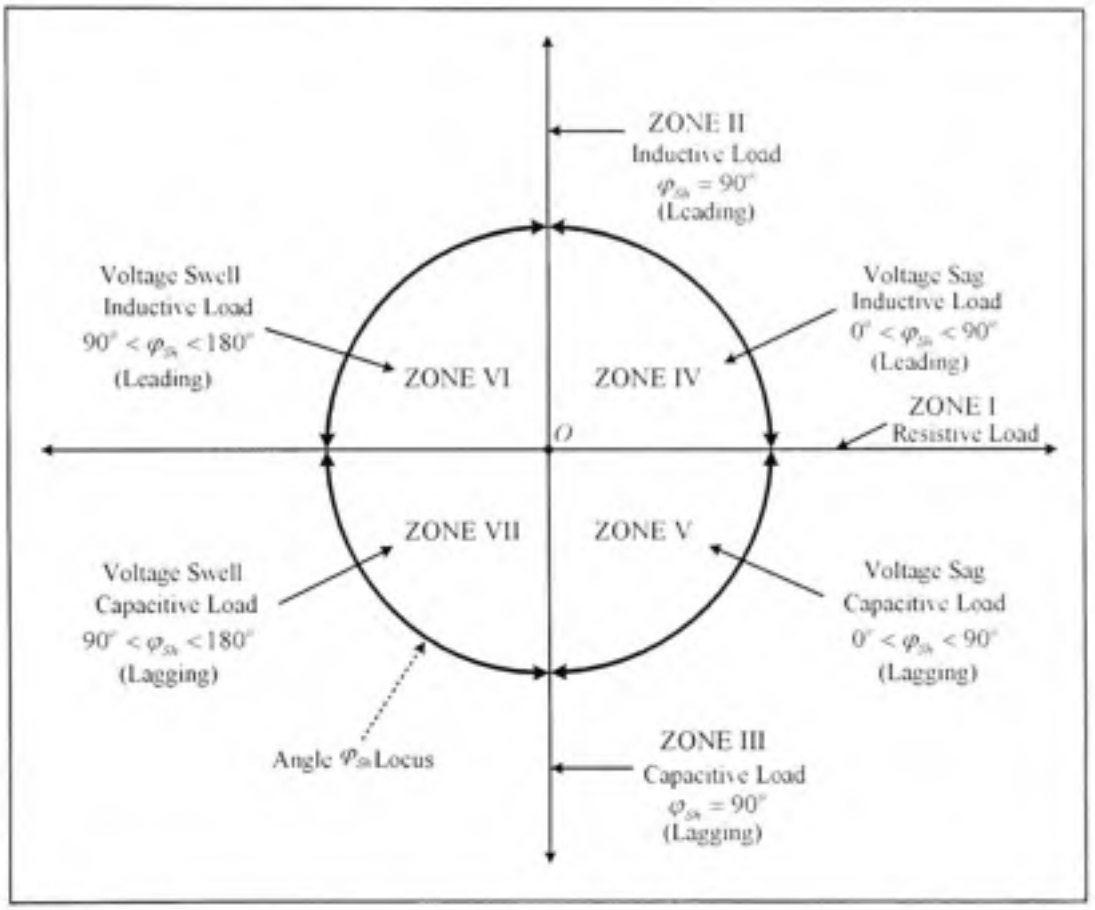


Figure 1.17 Operating zones of UPQC based on φ_{Sh} variation for Sag/Swell compensations.

Considering the case of inductive load, the load VAR requirement is supplied by shunt inverter by injecting 90^0 leading current. The magnitude of the compensating current would depend on the VARs to be compensated. This condition is represented by Zone–II. Now, if the load is capacitive one, theoretically, the load would draw leading current from the source, i.e. load generates VARs. This load generated VARs are compensated by the shunt inverter by injecting 90^0 lagging current. The magnitude of compensating current depends on the VARs to be cancelled out, represented by Zone–III. During the operation of UPQC in Zone–II and –III larger the VAR compensation more would be the compensating current magnitude.

Zone–IV and Zone–V represents the operating region of UPQC during the voltage sag on the system for inductive and capacitive type of the loads, respectively. During the voltage sag as discussed previously, the shunt inverter draws the required active power from the source by taking extra current from the source. In order to have real power exchange between source, UPQC, and load, the angle φ_{Sh} can not be 90^0. For inductive type of the load, this angle could be anything between 0^0 to 90^0 leading and for capacitive type of the load, between 0^0 to 90^0 lagging. This angle variation mainly depends on the % of sag need to be compensated and load VAR requirement. If the load is pure resistive, the φ_{Sh} would be 0^0, however the shunt inverter current will be on x-axis.

Zone–VI and Zone–VII represents the operating region of UPQC during the voltage swell on the system, for inductive and capacitive type of the loads, respectively. During the voltage swell as discussed previously, shunt inverter feeds back the extra active power from the source by taking reduced current from the source. In order to achieve this angle φ_{Sh} would be between 90^0 to 180^0 leading, and between 90^0 to 180^0 lagging for inductive, and capacitive type of load, respectively.

The analytical study carried out and the zonal representation of UPQC thus can help to understand the behavior of UPQC based system under different operating conditions.

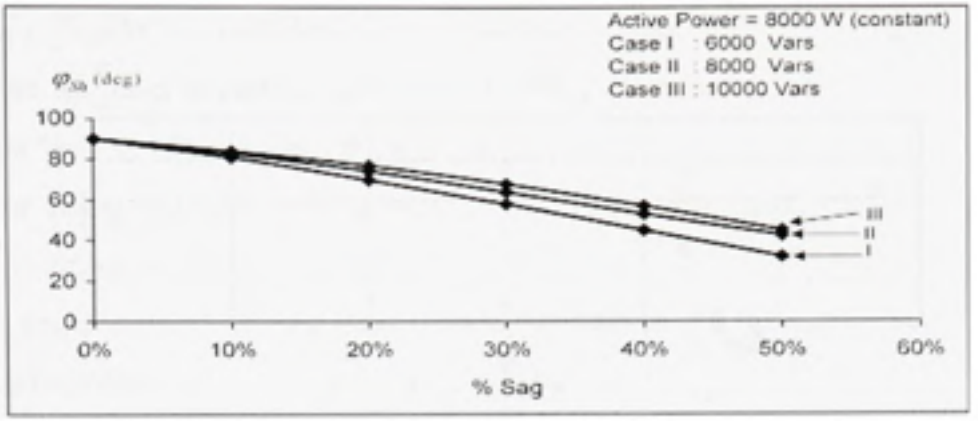
1.5 Steady State Power Flow Analysis: Numerical Study

In this section, a numerical study is presented to verify some of the important points brought into attention. The steady state power flow analysis is evaluated using digital simulation. The emphasis is given on the impact of % sag and % swell variation on the phase angle φ_{Sh}, shunt compensating current i_{Sh} , and source current i_S. Table 1.1 gives the values of φ_{Sh}, i_{Sh} and i_S for different load VAR requirements. Here, the load active power demand is kept constant, 8000 watts. With these conditions the input voltage is reduced up to 50 % of the rated value.

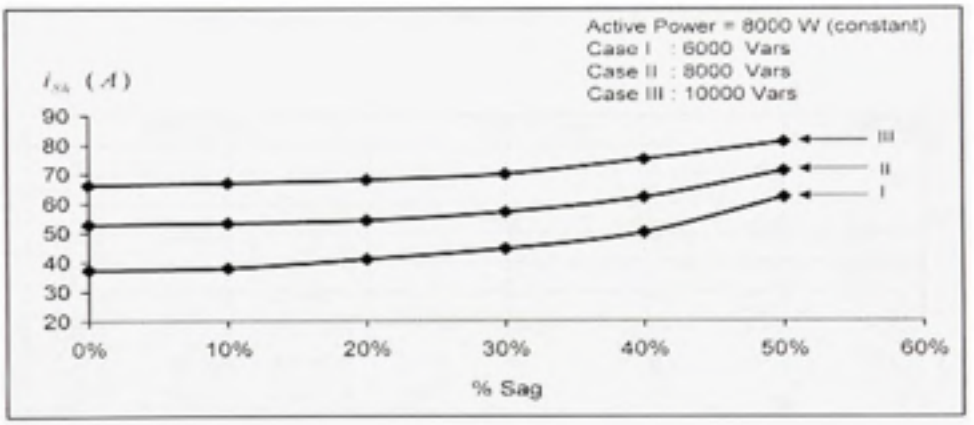
Table 1.1
Impact of % sag and load VAR variation

	6000 Vars			8000 Vars			10000 Vars		
%Sag	φ_{Sh}	i_{Sh}	i_S	φ_{Sh}	i_{Sh}	i_S	φ_{Sh}	i_{Sh}	i_S
No UPQC	--	--	65.8 A	--	--	74.0 A	--	--	74.0 A
0%	90.0^0	37.4 A	53.0 A	90.0^0	52.8 A	53.0 A	90.0^0	66.3 A	53.0 A
10%	81.0^0	38.0 A	58.7 A	83.0^0	53.2 A	59.3 A	84.0^0	67.0 A	59.8 A
20%	70.0^0	41.0 A	65.7 A	74.5^0	54.2 A	66.2 A	77.0^0	68.0 A	67.0 A
30%	58.0^0	44.5 A	74.8 A	64.5^0	57.0 A	75.5 A	68.0^0	70.0 A	76.2 A
40%	45.0^0	50.0 A	85.4 A	53.0^0	62.0 A	87.2 A	57.0^0	75.0 A	89.3 A
50%	32.0^0	62.0 A	97.8 A	42.5^0	71.0 A	100.8 A	45.0^0	81.0 A	104.0 A

Figure 1.18 (a) shows the variation in angle φ_{Sh} with % of sag variation for three different load VAR demands. As % of sag increases, the angle φ_{Sh} reduces from 90^0 and reaches towards lower value, suggests more and more active power is being transfer through UPQC. Shunt inverter is now playing an important role of handling extra load active power demand in addition to the load VAR support. The aforementioned task is achieved by taking fundamental current component from the source, as % of sag increases, shunt inverter draws more and more fundamental component, easily seen from Figure 1.18 (b). The impact of variation in both angle φ_{Sh} and compensating current i_{Sh} can be seen on the source current, which increases as % of sag increases, as shown in the Figure 1.18 (c). This is necessary to maintain the active power balance in the network and to maintain the DC link voltage at constant level.



(a)



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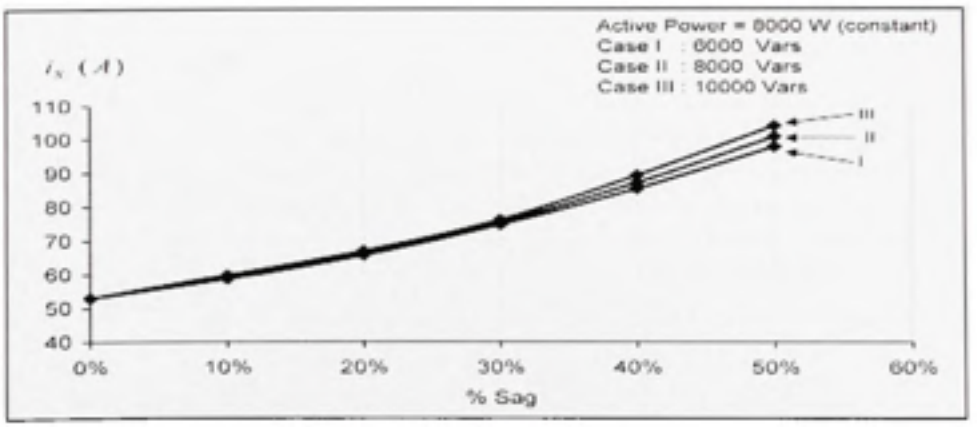


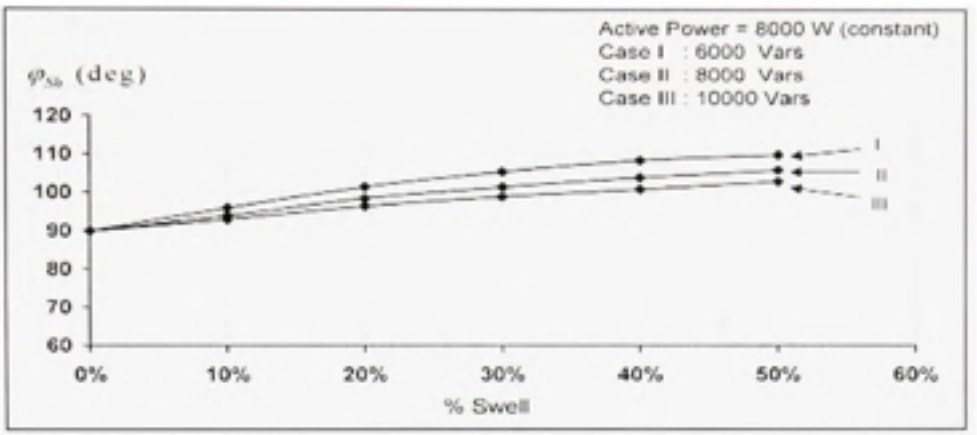
(c)

Figure 1.18 Variation in system parameters under different % of sags.

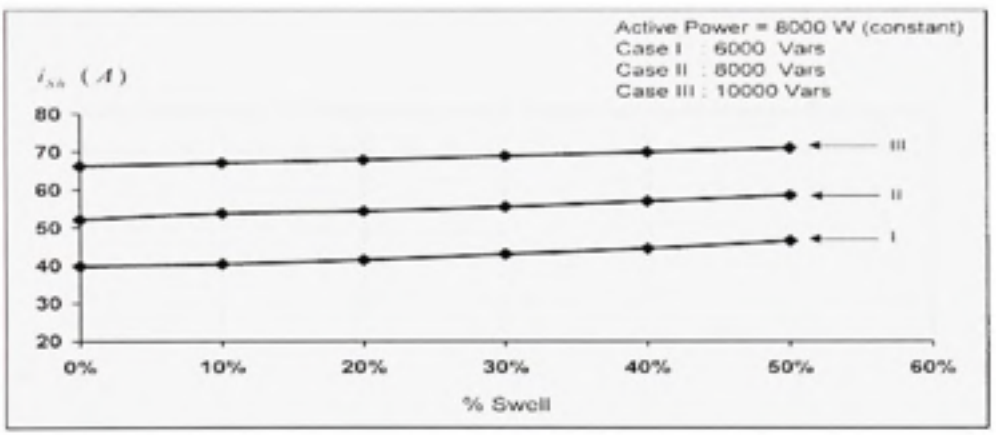
Table 1.2 gives the values of φ_{Sh}, i_{Sh} and i_S for different load VAR requirements with a swell on the system. Figure 1.1 Detailed system configuration of three-phase UPQC. Figure 1.19 (a) shows the variation in angle φ_{Sh} with % of swell variation for three different load VAR demands. As % of swell increases, the angle φ_{Sh} increases from 90^0, suggests more and more active power being fed back through the shunt inverter. The shunt compensating current magnitude increases as shown in Figure 1.19 (b), to achieve the aforementioned task. The increase in angle φ_{Sh} and compensating current results in the reduction in source current magnitude which decreases as % swell increases, as shown in Figure 1.19 (c).

Table 1.2
Impact of % swell and load VAR variation

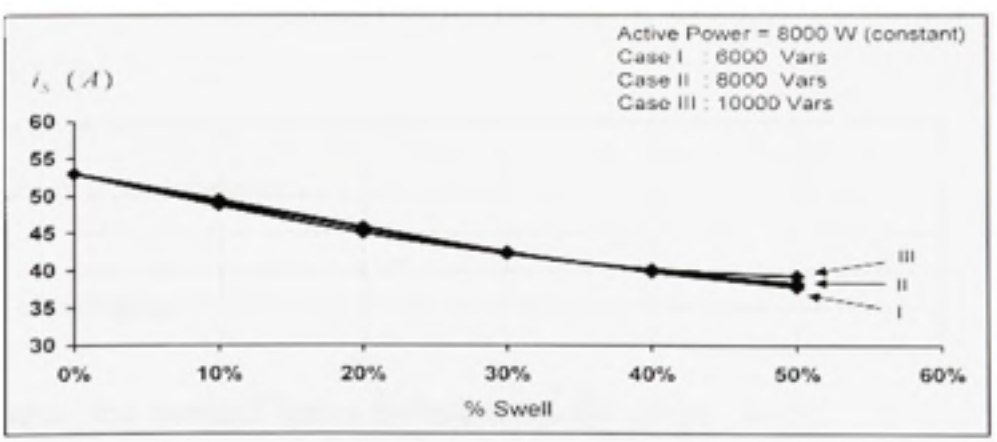
	6000 Vars			8000 Vars			10000 Vars		
%Swell	φ_{Sh}	i_{Sh}	i_S	φ_{Sh}	i_{Sh}	i_S	φ_{Sh}	i_{Sh}	i_S
No UPQC	--	--	65.8 A	--	--	74.0 A	--	--	74.0 A
0%	90.0^0	39.8 A	53.0 A	90.0^0	52.2 A	53.0 A	90.0^0	66.3 A	53.0 A
10%	96.0^0	40.4 A	48.78 A	94.0^0	53.8 A	49.16 A	93.0^0	67.2 A	49.5 A
20%	101.5^0	41.5 A	45.08 A	98.5^0	54.4 A	45.64 A	96.5^0	68.0 A	45.8 A
30%	105.5^0	43.0 A	42.27 A	101.5^0	55.5 A	42.36 A	99.5^0	69.0 A	42.5 A
40%	108.5^0	44.5 A	40.15 A	104.0^0	57.0 A	40.05 A	101.0^0	70.0 A	39.9 A
50%	110.0^0	46.5 A	39.23 A	106.0^0	58.5 A	38.29 A	103.0^0	71.0 A	37.8 A



(a)



(b)



(c)

Figure 1.19 Variation in system parameters under different % of swells.

From Table 1.1 and Table 1.2, when the UPQC is not connected in the circuit, the source supplies both active as well as reactive power demanded by the load. With UPQC in operation, source supplies only active part of load power demand. During this VAR compensation mode of operation the source current is almost constant i.e. 53A, independent of the load VAR requirements, as seen from Table 1.1 and Table 1.2, for 0 % sag and swell.

In normal operating condition, the shunt inverter provides the load VARs, whereas, the series inverter handles no active or reactive power. Therefore, in this case the rating of the series inverter would be small fraction of load rating. The shunt inverter rating mainly depends on the compensating current provided by it, which depends on the load power factor or load VAR requirement. Higher the load VAR requirement higher would be the shunt inverter rating. From (1.8), (1.12) and (1.16), the series inverter rating depends on two factors, source current i_S and factor k_f. The current i_S increases during voltage sag condition, whereas, decreases during voltage swell condition. Therefore the rating of the series inverter is considerably affected by the % of sag needed to be compensated. A compromise needs to be made while considering the series inverter ratings, which directly affects the sag compensation capability of UPQC. Depending on the load requirements, an optimization can be done on these two issues. The shunt inverter rating increases as it handles the extra active power during the voltage sag/swell conditions. Furthermore, from Figure 1.18 (b) and Figure 1.19 (b), the increase in % sag greatly affects the shunt inverter rating as compared to the increase in % swell. Thus, the analysis presented in this chapter can be very useful in the selection of kVA ratings of both the series and shunt inverters depending on the % of sag and swell needed to be compensated.

1.6 Conclusion

In this chapter, the essential basics to understand the UPQC concept, its key components, operating principle, potential applications have been highlighted. An in-depth and up-to-date literature review on UPQC based articles is also provided. For easy understanding, the operating principle of UPQC has been explained by splitting it into the shunt and series

inverter operations. Moreover, it has been pointed out that the most important task of shunt inverter is to maintain the DC link voltage at constant level without which the desired performance from UPQC can not be achieved.

Besides building the first milestone of basic understanding of term "UPQC", an interesting analytical study on "how the active and reactive power flows between source, UPQC, and load under different operating condition" has also been carried out. Additionally, a numerical study has been carried out to highlight the impact of sag and swell variations on injected shunt filter and source currents. Eventually, the study results in hand tool to select the UPQC device ratings taking different operating conditions into consideration.

CHAPTER 2

UPQC FEASIBILITY ANALYSIS FOR PRACTICAL APPLICATION

2.1 Introduction

This chapter is dedicated to validate the adaptability of UPQC in a realistic distribution network. The presented work was done in collaboration with Hydro-Québec, Montréal and *Institut de recherche d'Hydro-Québec (IREQ)*, (Hydro-Québec's Research Institute), Varennes, Canada The purpose of this collaboration project was to evaluate, through simulation study, the feasibility and the performance of UPQC when installed in a realistic distribution network. A complex network, with realistic parameters, was simulated at Power System Simulation Laboratory (*Laboratoire de simulation de réseaux*, LSR), IREQ, Varennes, which imitates the situation at one of the Hydro-Québec's consumers vicinity.

A simple control approach for UPQC is proposed and termed as *Unit Vector Template Generation* (UVTG) technique. First, the formulation of unit vector template generation controller is described. Later on, a brief description on realistic network under consideration is given. The performance of UPQC under different operating conditions, with a thorough simulation study, is discussed in detail. Some of the important laboratory experimental results are also given at the end of the chapter.

2.2 Motivation behind the Collaboration Project

Due to the extensive use of nonlinear loads on distribution networks, Hydro-Québec customers are facing power quality problems. To help some of the customers, such as, a computer factory and a sawmill, Hydro-Québec has made some attempts in the past. However, the installation of available mitigation devices did not give expected results. For mitigation of voltage sag, a dynamic voltage restorer (DVR) was suggested to the customer. Unfortunately, the electronics control circuit of the device failed to perform as expected because of the harmonics generated inside the plant. In another case, an automatic VAR

controller (AVC) was installed at the customer end for the mitigation of sags and flickers. The device could only perform well for sags but not for the flicker.

The current trends in the field of mitigation devices is towards a unified approach, in which the mitigation device tackles both the current and voltage related power quality problems, simultaneously, such as, current harmonics, load reactive power, current unbalance, excessive neutral current, voltage harmonics, voltage sag, voltage swell, voltage unbalance, voltage flicker, etc. Therefore, there was an urge to try newly upcoming power quality enhancement devices, such as the UPQC. The major goal of this project was to carry out the feasibility of UPQC to be installed in actual distribution network to support the individual sensitive customers, and also to have readily available data (as a case study) for possible future installations.

The project was divided in two parts, one in which Hydro-Québec and IREQ were involved to build realistic network Simulink model and the other in which ÉTS was involved to develop the necessary concept, control algorithm, and necessary testing by implementing the experimental setup in the laboratory.

The project goals are briefly summarized as –

- To develop the Simulink model that would represent the realistic distribution network conditions.
- Acquire the necessary background knowledge and to develop necessary control algorithm for UPQC.
- In-depth simulation study to evaluate the performance of UPQC when installed on realistic distribution network.
- Laboratory prototyping of UPQC and the experimental validation to confirm the possible practical application.

Thus, this chapter is the blend of all the important goals and discusses the findings achieved.

2.3 UPQC Controller Development

The control strategy for UPQC is basically the way to extract the reference signals for both the shunt and series inverters. The effectiveness of the UPQC compensation depends on its controller's ability to calculate the reference signals for the shunt and series inverters with a minimum error and time delay to compensate for the current and voltage distortion, voltage variation, unbalance (voltage and/or current) or any other undesirable condition. In the following sections a simple new approach is explained to extract the reference voltage and current signals for series and shunt inverters (Khadkikar *et al.* 2004, 2006b).

2.3.1 Reference Voltage Signal Generation

The major function of series part of UPQC is to strictly maintain the voltage at load bus sinusoidal and at the rated value (magnitude). Therefore, the simplest approach to generate reference signals for series inverter would be directly imposing the load bus voltage to be perfect sinusoidal. On a particular distribution system the standard magnitude of voltage being supplied is fixed. For example, high power rated industrial loads are supplied with three-phase 208/240/600 VAC @60Hz voltages and a typical household consumer is supplied by single-phase 120VAC @60Hz voltage. Therefore two important factors to maintain the precise regulation at load bus, especially for sensitive loads to be protected are – *i*) perfect sinusoidal voltage at 60Hz and *ii*) fixed load voltage magnitude. The supply voltages can be distorted, may show some dips or rise in voltage due to switching ON/OFF of high rated load connected to the same feeder, or may get unbalanced due to severe unbalanced load on the network, etc. Under such undesirable conditions, if we could force the load voltages to be perfectly sinusoidal and at fixed load voltage magnitude, the unwanted events/ problem can be solved easily.

Assuming that the terminal voltages at point of common coupling (PCC) are distorted, they can be decomposed as sum of fundamental and harmonics components, and can mathematically be represented as –

$$v_{Sa}(\omega t) = v_{Sa,1} + v_{Sa,2} + v_{Sa,0} + v_{Sa,h} \tag{2.1}$$

Where, $v_{Sa,1} \Rightarrow$ Fundamental positive sequence component of phase –*a* voltage

$v_{Sa,2} \Rightarrow$ Negative sequence component of phase –*a* voltage

$v_{Sa,0} \Rightarrow$ Zero sequence component of phase –*a* voltage

$v_{Sa,h} \Rightarrow$ Sum of the harmonics components present in phase –*a* voltage

The harmonics term further can be expressed as –

$$v_{Sa,h} = \sum_{n=2}^{\infty} v_{Sa,n} \cdot \sin(n\omega t + \theta_{na}) \tag{2.2}$$

Similarly, for other two phases –

$$v_{Sb}(\omega t) = v_{Sb,1} + v_{Sb,2} + v_{Sb,0} + v_{Sb,h} \tag{2.3}$$

$$v_{Sc}(\omega t) = v_{Sc,1} + v_{Sc,2} + v_{Sc,0} + v_{Sc,h} \tag{2.4}$$

For a three-phase system to be perfectly balanced and pure sinusoidal, only the fundamental positive sequence components should present and other remaining components should be necessarily zero.

A phase locked loop (PLL) based simple procedure is explained to define the load voltages as fundamental positive sequence components. First, the supply/terminal voltages are sensed and multiplied by a gain equals to $1/Vm$. Where, Vm represents the peak amplitude of supply voltage under consideration. Thus we can get approximate unity source voltages. These unity source voltage signals are than taken to a PLL. The PLL gives output in terms of *sin* and *cos* functions who's fundamental frequency is set by the user, in this case 60Hz. Moreover, the

sin and *cos* signals have unity magnitude. The *sin* term represents the perfect sinusoidal unity voltage signal for phase –*a*. and with proper phase angle delay of +/- 120^0, the unit templates for the other two phases can be generated easily. The unit vector templates for three-phase system can be given as –

$$Ua = \sin(\omega t) \tag{2.5}$$

$$Ub = \sin(\omega t - 120^{o}) \tag{2.6}$$

$$Uc = \sin(\omega t + 120^{o}) \tag{2.7}$$

As discussed previously, the load bus voltage magnitude, for a particular application is a known quantity. Let V_{Lm} represents the peak amplitude of normal steady-state load bus voltage. Now, if we multiply the constant term V_{Lm} with generated unit vector templates of (2.5) – (2.7), we can easily get the required profile of load bus voltages, termed as *desired load voltages* at load bus. These desired load voltages can be given as –

$$v^{*}_{La}(\omega t) = V_{Lm}.Ua = V_{Lm}.\sin(\omega t) \tag{2.8}$$

$$v^{*}_{Lb}(\omega t) = V_{Lm}.Ub = V_{Lm}.\sin(\omega t - 120^{o}) \tag{2.9}$$

$$v^{*}_{Lc}(\omega t) = V_{Lm}.Uc = V_{Lm}.\sin(\omega t + 120^{o}) \tag{2.10}$$

The block diagram representation for desired load voltages extraction is shown in Figure 2.1. If we force the series inverter to maintain the desired load voltages at the load bus then the power quality problems associate with supply voltage such ac voltage harmonics, voltage sag and swells, voltage unbalance, etc., will get compensated indirectly. In such case, the actual load voltages are compared with the desired load voltages given by (2.8) – (2.10) to carry out the PWM operation.

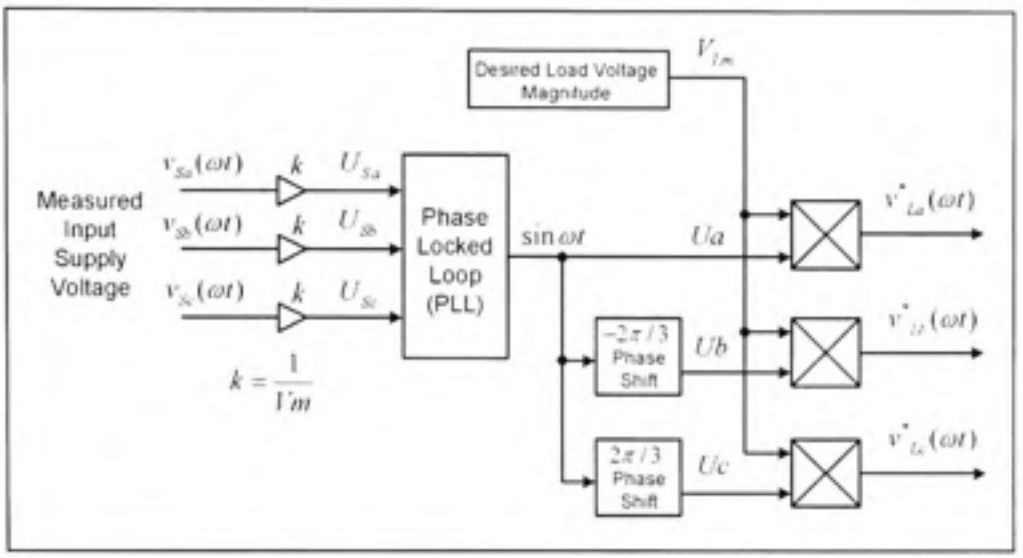


Figure 2.1 Desired load voltages signal generation.

The other option, the direct approach, in which the reference voltage signals for series inverter are generated. The reference signals for series inverter can be extracted as,

$$v^*_{Sr,a}(\omega t) = v_{Sa}(\omega t) - v^*_{La}(\omega t) \tag{2.11}$$

$$v^*_{Sr,b}(\omega t) = v_{Sb}(\omega t) - v^*_{Lb}(\omega t) \tag{2.12}$$

$$v^*_{Sr,c}(\omega t) = v_{Sc}(\omega t) - v^*_{Lc}(\omega t) \tag{2.13}$$

Here, the actual voltages injected by series inverter are sensed and compared with the reference series injected voltages of (2.11) – (2.13) to perform the PWM operation.

2.3.2 Reference Current Signal Generation

The unit vector templates generated for series part can also be used to generate reference current signals for shunt inverter. The major function of shunt inverter is to compensate current harmonics, reactive power, current unbalance, and neutral current by maintaining the DC bus voltage at constant level. The simplest way to compensate above mentioned

problems associated with the load is to force the source current to be balanced and sinusoidal. To achieve the aforementioned tasks the DC link voltage is sensed and compared with the reference DC link voltage, as shown in Figure 2.2. The error is then processed by a PI controller. The output of the PI controller can be represented as the peak amplitude of fundamental input current, I_m, which should be drawn from the supply in order to maintain DC link voltage at constant level and to supply losses associated with UPQC. Thus, by multiplying the peak amplitude, I_m, with unit vector templates of (2.5) – (2.7), gives the reference source current signals which are balanced and perfectly sinusoidal that the source should supply.

$$\text{Therefore, } i^*_{Sa} = I_m.Ua = I_m.\sin\omega t \tag{2.14}$$

$$i^*_{Sb} = I_m.Ub = I_m.\sin(\omega t - 120^\circ) \tag{2.15}$$

$$i^*_{Sc} = I_m.Uc = I_m.\sin(\omega t + 120^\circ) \tag{2.16}$$

The generated reference source current signals of (2.14) – (2.16) are than compared with actual source currents to perform PWM operation.

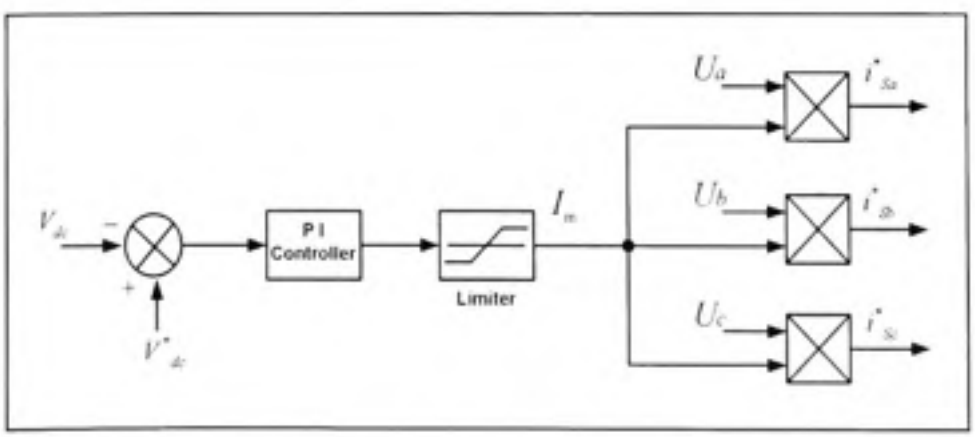


Figure 2.2 DC link control and reference source current signal generation.

As the extracted unity vector templates, using a simple PLL, are used to generate the reference signals for both the inverters, simultaneously; this method is termed as *Unit Vector Template Generation* (UVTG) approach for UPQC. The significant advantage of this approach is that it does not require complex transformations and it is very easy to implement for practical hardware applications.

2.3.3 Gating Signal Generation/ Modulator

After extracting the reference voltage and current signals for series and shunt inverters, the next step is to perform the accurate switching of both the inverters to follow the reference signals for the inverters (direct approach) or to force the load voltages and source currents (indirect approach) to accomplish the required tasks. A modulation technique is used to generate the adequate gating signal pattern to perform switching operation of the inverter switches. A hysteresis band control technique based PWM strategy is considered for the shunt inverter, while, a triangular carrier signal based fixed frequency PWM technique is used for the series inverter. The block diagram of a hysteresis controller is shown in Figure 2.3. The hysteresis controller gives the switching instant whenever the error exceeds a fixed magnitude limit as defined by the hysteresis band. To control both the inverters, the generated reference current and voltage signals, for shunt and series inverter, are compared with actual sensed source currents and the actual sensed load voltages, respectively. Finally, the error is processed to generate the gating signal pattern for shunt and series inverters. However, a hysteresis controller is required for each of the phases of source currents and the load voltages.

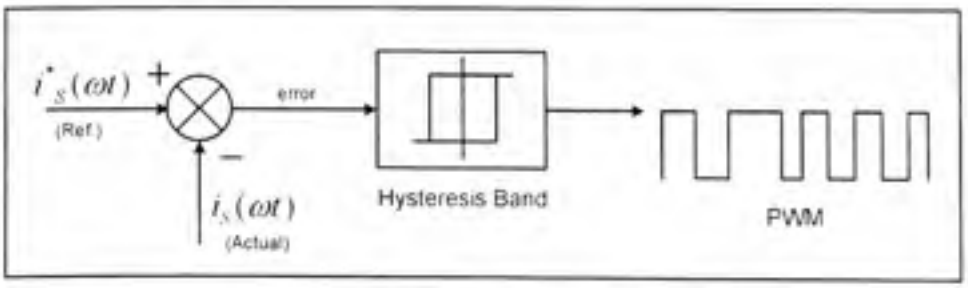


Figure 2.3 Hysteresis controller.

2.4 Realistic Network Details

Figure 2.4 shows the single-line diagram of the three-phase industrial distribution network under study. The voltage is generated at 120kV, transmitted and then stepped down at different voltage levels based on individual premises requirements. The UPQC is supposed to be installed at a plant which is located at a considerable distance from the distribution transformer and there are several loads present in between, represented by equivalent MW or MVA ratings. The voltage which is available at the input Bus Bar B3 of the plant is at 12.7kV. This voltage is further stepped down at 600V by using step down transformer T4.

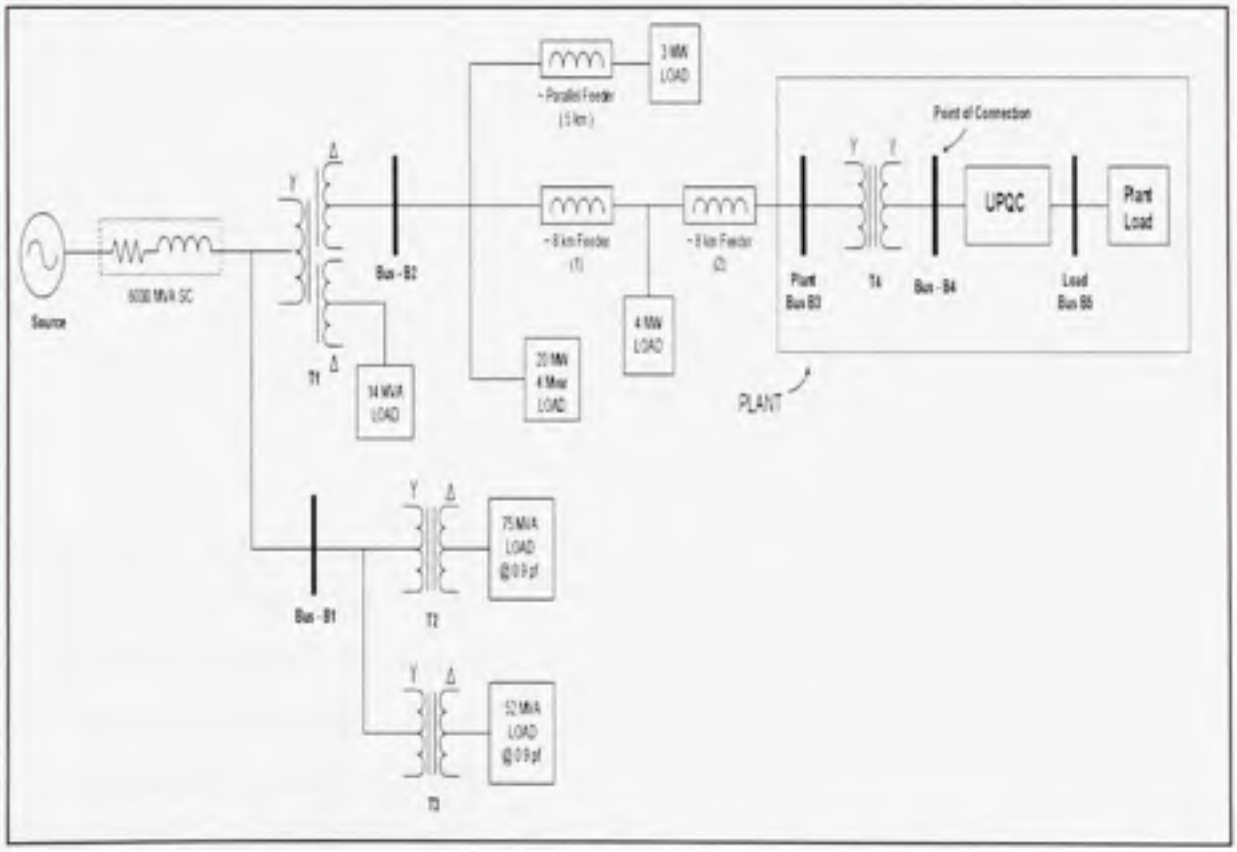


Figure 2.4 Single-line diagram: Industrial distribution network under consideration.

The point of connection is the point at which UPQC is connected to the distribution network. The UPQC is installed between bus B4 (point of connection) and load bus B5. The Simulink model for this realistic distribution network was built at LSR lab.

The plant under consideration consists of several loads among which the important ones are shown in Figure 2.5. These loads are – two AC Motors (L1 & L2), two Diode Bridge Rectifiers (DBR) (L3 & L4), and a pure Resistive load (L5). The resistive load L5 represents the sensitive load to be protected from any disturbances in the supply voltage. On the other hand, two DBR loads L3 and L4 are harmonics producing loads. The harmonics generated by them should not reach at point of connection. It is important to note here that the distribution network model represents one of the Hydro-Québec's plant site, but, the loads in the plant do not represent the actual loads. Some of the loads are deliberately added to perform the simulation study.

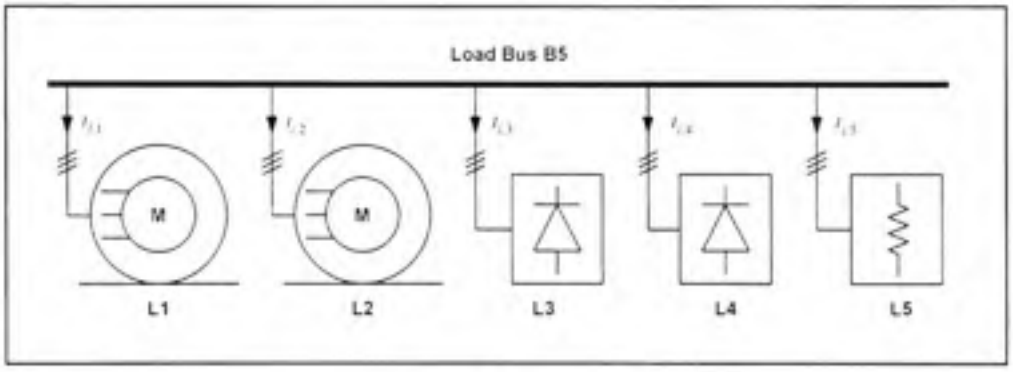


Figure 2.5 Plant load.

The ratings of all the loads are as given below:

L1: AC Motor - 50 HP, 1775 RPM, Tm = 125 N.m

L2: AC Motor - 50 HP, 1775 RPM, Tm = 75 N.m

L3: Diode Bridge Rectifier - 40 kVA

L4: Diode Bridge Rectifier - 25 kVA

L5: Resistive Load -25 kW

Figure 2.6 shows the basic block diagram of the UPQC. The voltage at bus B4 (before UPQC), the load voltage at load bus B5, voltage injected by series inverter, and the DC link voltage between two inverters are represented by v_{B4}, v_L, v_{inj} and v_{dc}, respectively, whereas, the current at bus B4, total load current drawn by all the loads, and the current injected by shunt inverter are represented by i_{B4}, i_L, and i_{sh}, respectively. Aim is to maintain the voltage

at bus B5 at desired level and free from any distortions. Also the harmonics and reactive current drawn by the loads should be compensated locally, such that, the current at bus B4, i_{B4}, would be pure sinusoidal and in-phase with utility voltage.

The voltage levels at different buses are mentioned in Table 2.1. The feeder parameters and transformer specifications are given in Table 2.2 and Table 2.3. All the voltages are mentioned on the basis of line to line values.

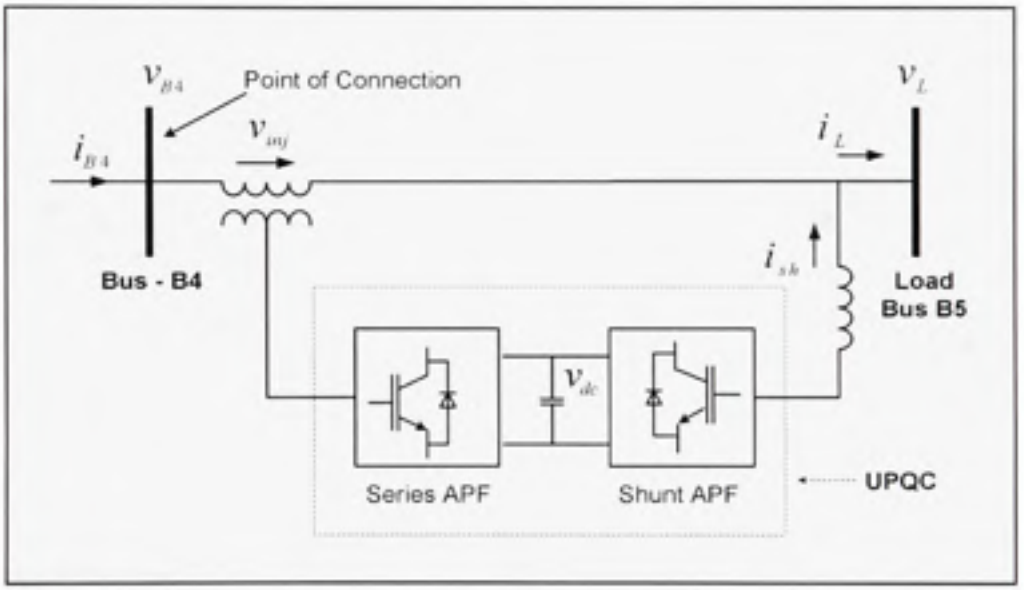


Figure 2.6 UPQC block diagram.

Table 2.1
Different load bus voltage magnitudes

Bus No.	Voltage Level
Bus-1	120kV
Bus-2	12.7kV
Bus-3	12.7kV
Bus-4	600V
Bus-5	600V

Table 2.2
Different Transformer ratings

No.	Rating	Voltages
T- 1	56 MVA	120kV / 12.7kV / 12.7kV
T- 2	100 MVA	120kV / 25kV
T- 3	104 MVA	120kV / 13kV
T- 4	1 MVA	12.7kV / 600V

Table 2.3
Transformer Specifications

Feeder No.	Feeder Length	Parameter	Value
(1) and (2)	8 km each	Positive Sequence Impedance	R1=0.1153 (ohm/km) L1=0.1048 (ohm/km)
Parallel Feeder	5 km	Zero Sequence Impedance	R0=0.3963 (ohm/km) L0=0.273 (ohm/km)

Sign Conventions used:

$+P_S$ = Active Power Supplied by the Source

$+Q_S$ = Reactive Power Supplied by the Source

$+P_L$ = Active Power Absorbed by the Load

$+Q_L$ = Reactive Power Absorbed by the Load

$+P_{Sh}$ = Active Power Absorbed by shunt inverter

$-Q_{Sh}$ = Reactive Power Generated by shunt inverter

$-P_{Sr}$ = Active Power Absorbed by series inverter

$+Q_{Sr}$ = Reactive Power Generated by series inverter

2.5 Simulation Results

To test feasibility of UPQC to be installed in actual distribution system, the performance of UPQC with developed UVTG approach is evaluated under realistic network condition using MATLAB/ Simulink. In the following subsections, an extensive simulation study is presented.

2.5.1 Steady State Plant – Network Performance

The steady state currents drawn by each of the loads under sinusoidal utility voltage condition are shown in Figure 2.7 (a) – (f). The power consumed by individual loads along with the total load power at Bus B5 is given in Table 2.1. Two 50 HP AC motors draw considerable amount of reactive power from the utility. This can be noticed from Figure 2.7 (a) and (b), compared to the fundamental current component drawn by resistive load, shown in Figure 2.7 (e). The diode bridge rectifiers followed by RL loads (DBRs) generate distortion in the currents. The total load current, i_L, which is the summation of all the load currents, is shown in Figure 2.7 (f). The THD of load L3 is 28.66% and load L4 is 28.9%, whereas, the current THD of total load current is 13.88%. Under the normal operating condition, without UPQC installed, total plant load consumes 132.7 kW active and 41.08 kVAR reactive power.

Losses across plant step down transformer T4 (Connected between Plant Bus B3 and Bus B4) – The power supplied by the utility to the plant before transformer T4 is 136.5 kW active and 45.37 kVAR reactive power. On the other hand, the total power at Bus B4 is 132.7 kW active and 41.08 kVAR reactive powers. This suggests a total power loss of 3.8 kW active power and 4.29 kVAR reactive power across plant step down transformer T4 under steady-state condition.

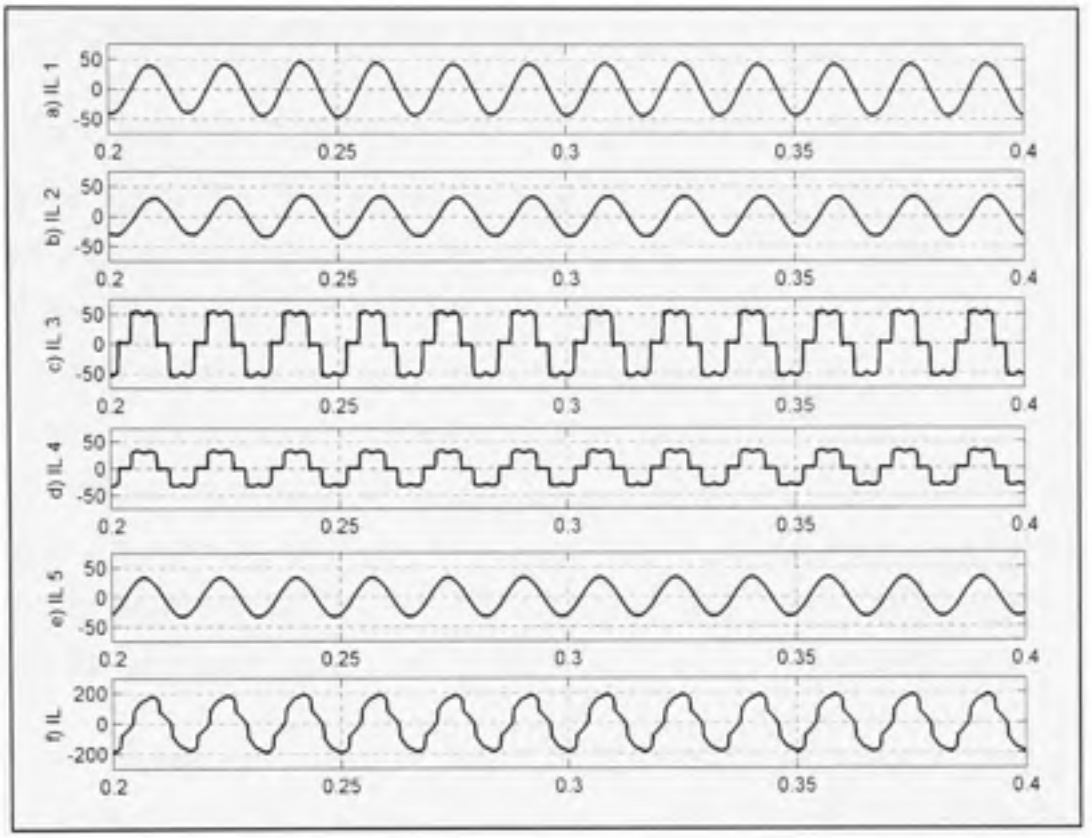


Figure 2.7 Simulation results: Steady state current drawn by each of the loads.

Table 2.4
Steady-state load power consumption under sinusoidal voltage

Sr. No.	Load Type	P (kW)	Q (kVAR)	THD_i
1.	L1: AC Motor	26.69	19.19	-
2.	L2: AC Motor	17.30	18.18	-
3.	L3: DBR	40.76	25.76	28.66%
4.	L4: DBR	24.52	11.37	28.90%
5.	L5: Resistive	23.42	00.00	-
6.	Total Plant Load	132.70	41.08	13.88%

2.5.2 Current Harmonics Compensation

Figure 2.8 shows the simulation results for UPQC working as current harmonics compensator. In this case, since, the terminal voltages are assumed pure sinusoidal, the shunt inverter is working alone and it is put into the operation at time t1=0.15 sec. As soon as the shunt inverter is turned ON, the feedback PI controller acts immediately forcing the DC link voltage to settle down at new reference value, here 1600V. This is done by taking fundamental component of source current. The DC link voltage attains this level within two cycles of the input voltage (Figure 2.8 (d)). At the same time, the shunt inverter also starts compensating the current harmonics generated by both the diode bridge rectifier loads. The shunt inverter injects a current (Figure 2.8 (g)) in such a way that the source current becomes sinusoidal. The improved source current profile can be noticed from Figure 2.8 (e).

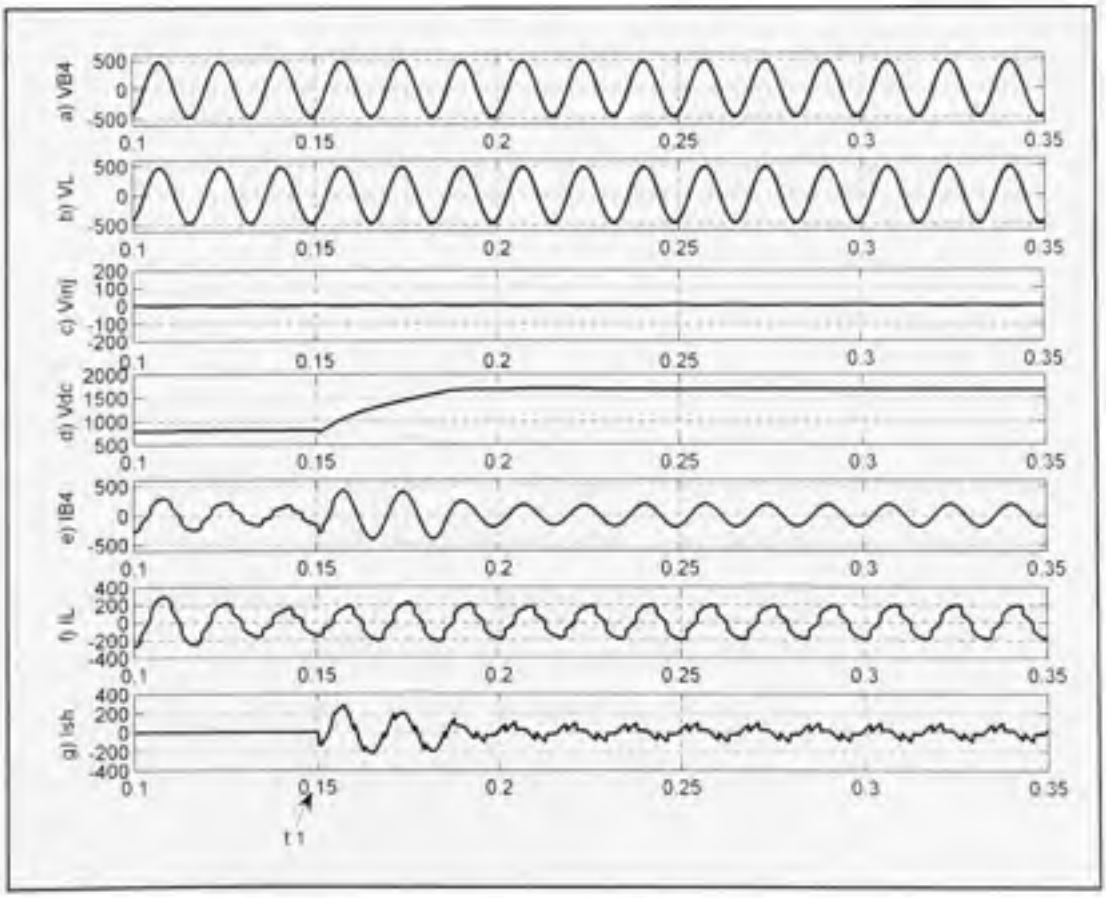


Figure 2.8 Simulation results: current harmonics compensation.

Table 2.5
PQ - Current harmonic compensation

Sr. No.	Parameters / Condition	1. Utility Side *(Before Bus B4)*			2. Load Side		
		P_S (kW)	Q_S (kVAR)	THD_{iS} (%)	P_L (kW)	Q_L (kVAR)	THD_{iL} (%)
1	Before Shunt inverter ON	132.85	41.13	13.88%	132.7	41.08	13.88%
2	After Shunt inverter ON	134.16	0.0	1.94%	132.9	41.0	13.88%
		3. Shunt inverter			4. Series inverter		
		P_{Sh} (kW)		Q_{Sh} (kVAR)	P_{Sr} (kW)		Q_{Sr} (kVAR)
3	Before Shunt inverter ON	0.15		0	-		-
4	After Shunt inverter ON	1.26		-41.07	-		-

Table 2.5 shows the THD values and overall active – reactive power flow between supply, UPQC and the load, before and after shunt inverter put into the operation. The plant total load current has THD of 13.88%. With shunt inverter in operation there is considerable reduction in THD at plant source side current, from 13.88% to 1.94%.

2.5.3 Reactive Power Compensation and Power Factor Correction (PFC)

Under steady state condition, without any compensation, utility provides 41.08 kVAR to the plant. With UPQC installed, since shunt inverter is supporting all reactive power demanded by the plant loads, utility is now supplying the load active power demand. The negative sign of Q_{Sh} (Table 2.5) implies that the shunt inverter is generating the required VARs. The lagging VARs required by the loads are supplied by shunt inverter, forcing the current drawn by the supply to in-phase with supply voltage and only fundamental active component of current is drawn from the source. Thus, the input power factor is improved to unity. Figure 2.9 shows the input voltage and current profile which suggests that the voltage and current are in-phase.

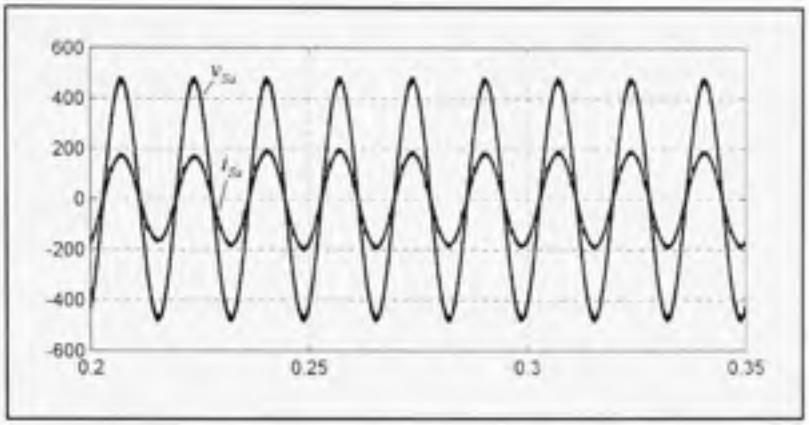


Figure 2.9 Simulation results: power factor correction.

2.5.4 Dynamic Performance under sudden load change

In order to evaluate the performance of UPQC during dynamic condition, the load on the system is changed momentarily. The simulation results during this condition are shown in the Figure 2.10. Before time t1=0.3 sec, only two motors are ON. Both shunt and series inverters are working under this condition. The shunt inverter provides the reactive power demanded by both the motors by injecting a 90^0 leading current (before time t1 in Figure 2.10 (d)). Suddenly, at time t1=0.3 sec, both DBR loads are connected to the load bus. This results in increased and distorted load current as noticed from Figure 2.10 (b). During this dynamic

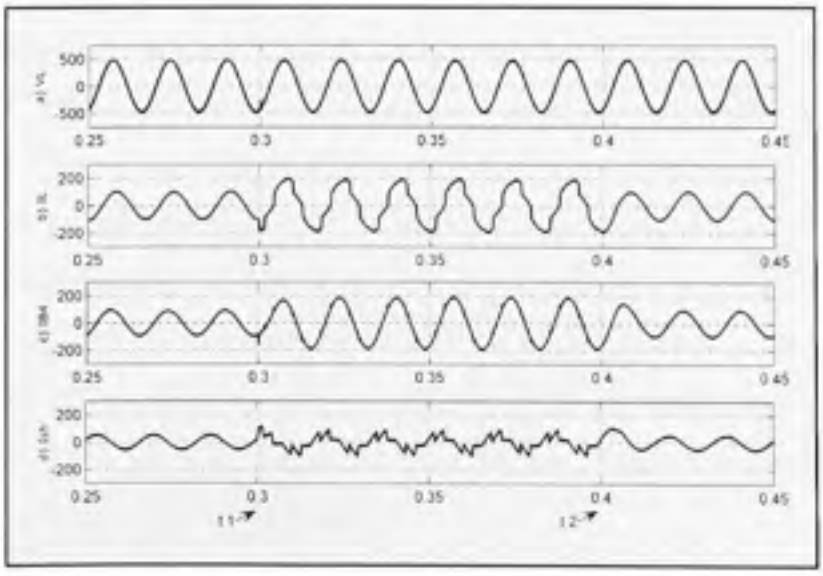


Figure 2.10 Simulation results: dynamic performance during sudden load change.

condition, the UPQC controller acts immediately, without any delay in the operation, and gains the new steady-state condition. The shunt inverter now injects a current equals to sum of harmonic and reactive currents. At time t2=0.4 sec, both the DBR loads are turned OFF and during this condition UPQC adapts new steady state condition without any problem.

2.5.5 Voltage Harmonics Compensation

To evaluate the performance of series inverter, the distortion in utility voltages are introduced deliberately by injecting a 5^{th} (10%), 7^{th} (7.5), 9^{th} (15%), 11^{th} (5%), 13^{th} (2.5%), 17^{th} (1.25%) and 19^{th} (1%) order voltage harmonics. The resultant highly distorted source voltage waveform shown in Figure 2.11 (a) has THD of 28.01%. Such a highly distorted voltage may be problematic for many sensitive loads. In addition to this the current drawn by loads with such distorted voltage could be highly distorted (Figure 2.11 (f)). Here THD of the load current i_l increases from 13.88% to 29.23% due to the distorted voltage present at Bus B4. Table 2.6 and Table 2.7 give the overall active – reactive power flow between supply, UPQC and the load, and the THD values before and after UPQC put into the operation.

Initially, the shunt inverter is put into operation at time instant t1=0.15 sec and its performance is as discussed already. After some time, at t2=0.25 sec, the series inverter is put into the operation such that both shunt and series inverters now work as UPQC. The series inverter starts compensating voltage harmonics immediately by injecting sum of the 5^{th}, 7^{th}, 9^{th}, 11^{th}, 13^{th}, 17^{th} and 19^{th} harmonics, making load voltage at load bus B5 distortion free (Figure 2.11 (b)). The voltage injected by series inverter is shown in Figure 2.11 (c). Here load voltage THD is improved from 28.01% to 3.52%. This improved voltage at bus B5 not only improves the load current THD value from 29.23% to 12.8% (steady-state value under sinusoidal case), but also improves source current (i_{B4}) THD value too. Since under distorted utility voltage, when only shunt inverter is ON, the THD of source current improves from 29.23% to 4.15%. With series inverter also in operation further reduces the source current THD to 2.35%, can be noticed from Table 2.7.

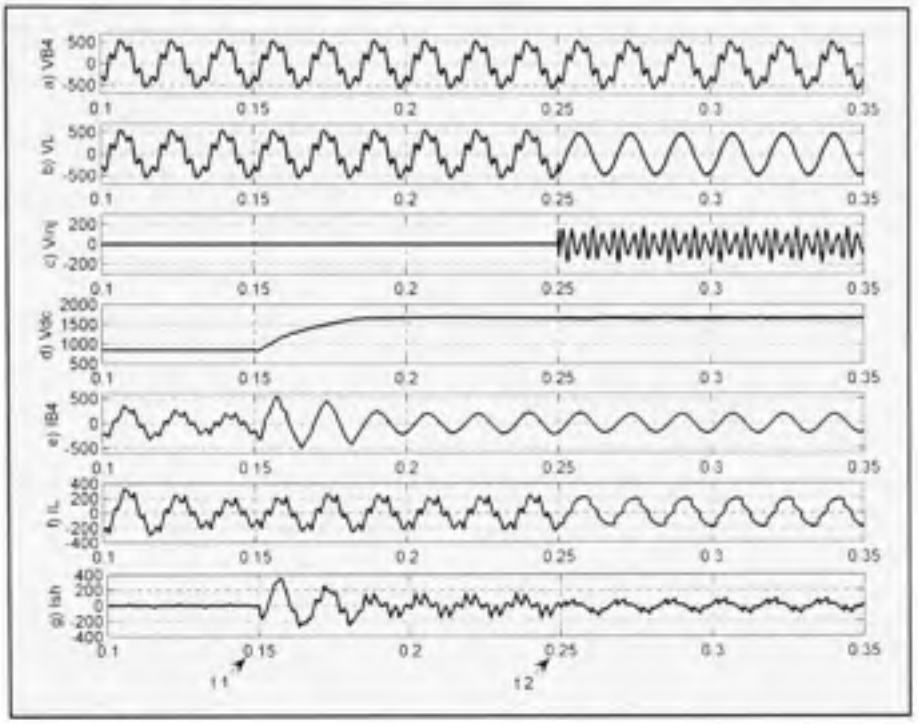


Figure 2.11 Simulation results: voltage harmonics compensation.

Table 2.6
PQ - Voltage harmonic compensation

Sr. No.	Parameters / Condition	Source Side		Load Side		Shunt inverter		Series inverter	
		P_S (kW)	Q_S (kVAR)	P_L (kW)	Q_L (kVAR)	P_{Sh} (kW)	Q_{Sh} (kVAR)	P_{Sr} (kW)	Q_{Sr} (kVAR)
1	Without Compen.	128.18	48.76	128.41	48.76	0.25	0	-	-
2	Shunt inverter ON	130.21	0.5	129.83	52.81	1.3	-52.31	-	-
3	UPQC ON	134.25	0.23	132.50	40.13	1.35	-40.15	0.40	0.22

Table 2.7
THD values: Voltage harmonic compensation

Sr. No.		Source Side		Load Side	
		THD*i*	THD*v*	THD*i*	THD*v*
1	Without Compensation	29.23%	28.01%	29.23%	28.01%
2	Shunt inverter ON	4.15%	28.14%	29.23%	28.16%
3	UPQC ON	2.35%	28.70%	12.8%	3.52%

As viewed from the Table 2.6, without any compensation, the power drawn by the loads under distorted source voltage is noticed as 128.41 kW + *j* 48.76 kVAR. When UPQC is ON, as the series inverter maintains the load voltage sinusoidal and at desired value, the load now draws its rated power from the source. A small amount of active power loss occurs across shunt and series inverters as switching loss, coupling resistive and inductive loss. The shunt inverter consumes very small amount of power as compared to the total load kVA rating to maintain the DC link voltage at constant level.

2.5.6 Voltage Sag Compensation

Figure 2.12 shows the simulation results during a sag condition on the system. There are four instants; t1, t2, t3 and t4. At t1 = 0.15 sec and at t2 = 0.25 sec, the shunt and series inverters are put into operation, respectively. At instant t3 = 0.35 sec, a sag (25%) is introduced to the system. This sag lasts till time t4 = 0.45 sec. Table 2.8 gives overall active – reactive power flow between supply, UPQC and the loads during different operating conditions.

During the voltage sag condition, the series inverter injects an in-phase voltage (25%) equals to the difference between the desired load voltage and actual source voltage, as seen from Figure 2.12 (c). Thus, helps to maintain the load voltage profile (Figure 2.12 (b)) at desired level such that the sag in source voltage does not appear at the load terminals. As discussed in steady-state power flow analysis (CHAPTER1, Section 1.4), in order to inject the in-phase voltage the UPQC requires certain amount of active power. This active power comes from the source, extracted by shunt inverter, by taking extra fundamental current component to maintain the DC link voltage at constant level. Without doing this, the DC link voltage will fall down in few cycles. The fundamental current drawn by shunt inverter can be noticed from Figure 2.12 (g) (between time t3 and t4), and therefore, the source current magnitude also increases accordingly (Figure 2.12 (e)).

In terms of powers, from Table 2.8, when there is sag on the system, and if the UPQC is not put into operation, the load could hardly draw 91.53 kVA (88.735 kW + *j* 22.45 kVAR) from the source due to the reduction in the terminal voltage (25%); instead of 138.91 kVA (132.7

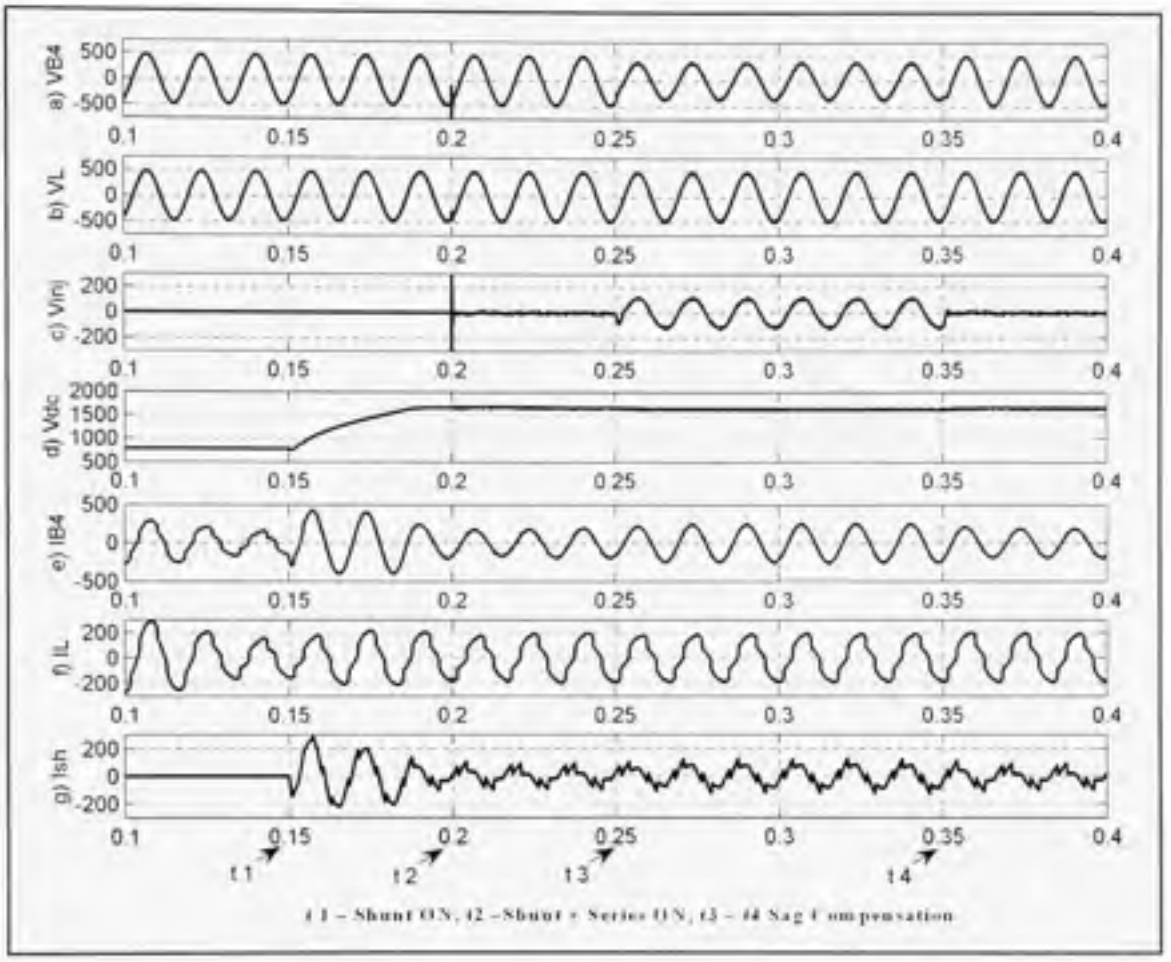


Figure 2.12 Simulation results: voltage sag compensation.

Table 2.8
PQ - Voltage sag compensation

Sr. No.		Source Side		Load Side		Shunt Inverter		Series Inverter	
	Parameters	P_{Sh}	Q_{Sh}	P_{Sr}	Q_{Sr}	P_{Sh}	Q_{Sh}	P_{Sr}	Q_{Sr}
	Condition	(kW)	(kVAR)	(kW)	(kVAR)	(kW)	(kVAR)	(kW)	(kVAR)
1	Normal Condition	133.42	41.15	132.7	41.10	0.24	0.03	-	-
2	UPQC ON (before Sag)	134.35	0.25	132.7	41.10	1.25	-41.2	0.4	0.2
3	UPQC ON (during Sag)	131.4	0.192	126.79	36.59	43.197	-37.51	39.51	0.73
3	UPQC OFF (Sag on system)	89.3	22.713	88.735	22.45	-	-	-	-

kW + *j* 41.08 kVAR), as in normal working condition. In this case, the source is supplying only 65.89 % of rated load power. When the UPQC is put into operation under the same sag condition, the series inverter is providing the required power to the load by injecting the in-

phase voltage (25%). This extra power flows from source to shunt inverter, shunt inverter to series inverter and finally, from series inverter to load, but without any delay in the operation. The active power drawn from the utility by shunt inverter is found as 43.2 kW. The major part of this active power is supplied to the load through series inverter. The series inverter provides 39.51 kW power to the load. With UPQC installed, the combination of source and UPQC could supply 94.78% (131.96 kVA, 126.79 kW + j 36.59) of rated load power. The remaining 3.69 kW power is utilized to maintain the DC link voltage at constant level (2.79% of rated load active power). Thus, the UPQC acts as a media to transfer active power to the load via shunt – series inverters.

2.5.7 Voltage Swell Compensation

Figure 2.13 shows the simulation results for a swell condition. Between time t3 =0.25 sec and t4 =0.35 sec, a swell (25%) is introduced on the system. Table 2.9 gives overall active – reactive power flow between supply, UPQC and the loads under different operating conditions.

The voltage swell phenomenon is exact opposite to the voltage sag condition. Therefore, during a swell on the system, the series inverter now injects out-of phase voltage (25%) equals to the difference between the desired load voltage and actual source voltage (Figure 2.13 (c)). Thus, the UPQC cancels the increased source voltage that may appear at the load side and maintains the load voltage profile (Figure 2.13 (b)) at desired level. The rise in source voltage means the utility now try to supply some extra power to the load. This may damage equipments and loads due to the increase in the current drawn by them. At the same time, the rise in source voltage also causes the DC link voltage to increase. Under such condition, the shunt inverter injects fundamental out-off phase current component (Figure 2.13 (g), between time t3 and t4) to maintain the DC link voltage at constant level. Therefore, the source current magnitude decreases (Figure 2.13 (e)). In other words, the extra active power coming from the utility side, due to the swell on the system, is now fed back by taking reduced source current from the source.

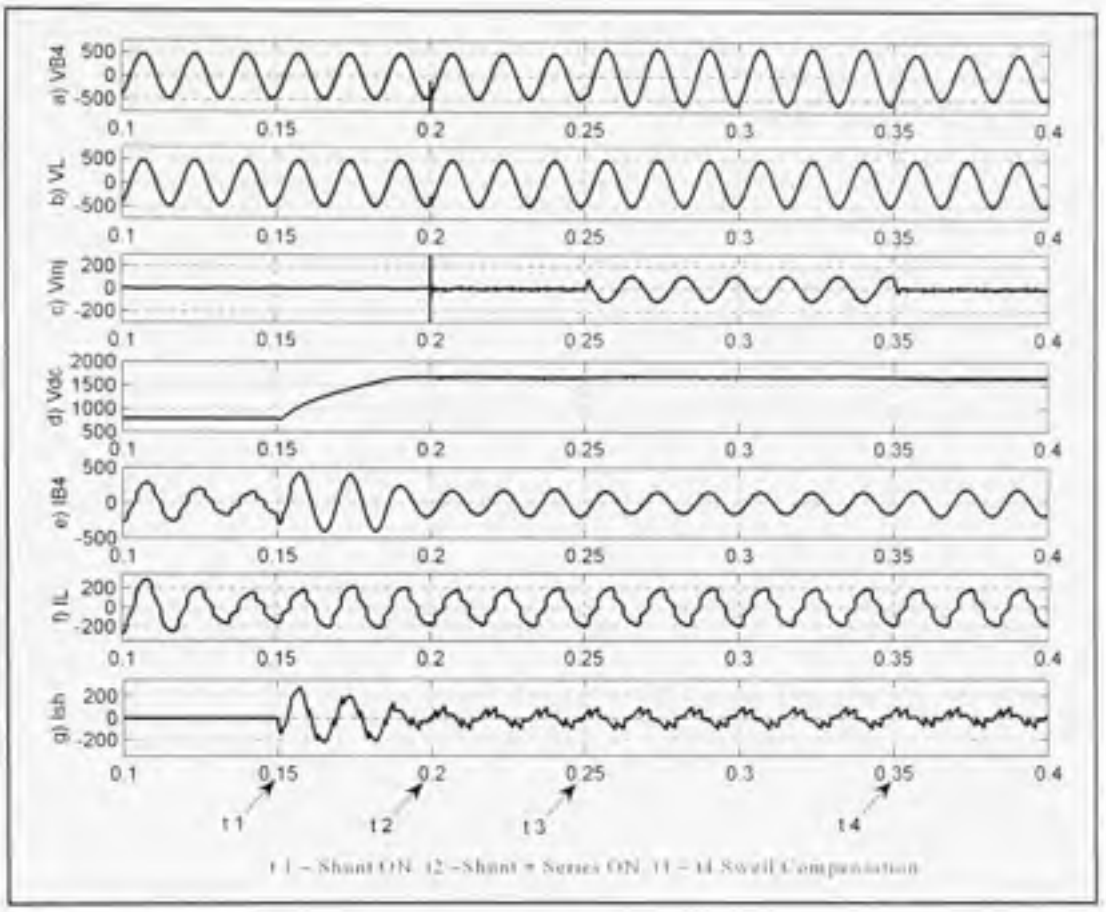


Figure 2.13 Simulation results: voltage swell compensation.

Table 2.9
PQ - Voltage swell compensation

Sr. No.		Source Side		Load Side		Shunt Inverter		Series Inverter	
	Parameters	P_{Sh}	Q_{Sh}	P_{Sr}	Q_{Sr}	P_{Sh}	Q_{Sh}	P_{Sr}	Q_{Sr}
	Condition	(kW)	(kVAR)	(kW)	(kVAR)	(kW)	(kVAR)	(kW)	(kVAR)
1	Normal Condition	133.42	41.15	132.7	41.10	0.24	0.03	-	-
2	UPQC ON (before Swell)	134.35	0.25	132.7	41.10	1.25	-41.2	0.4	0.2
3	UPQC ON (during Swell)	136.00	1.448	132.41	42.30	-22.77	-43.91	-25.4	-0.32
3	UPQC OFF (Swell on system)	186.7	66.641	184.29	65.75	0	0	0	0

From Table 2.9, during the swell on the system (UPQC in OFF mode), the load is supplied up to 195.67 (184.29 kW + *j* 65.75) kVA due to the rise in the terminal voltage (25%), which is 140.86% of its rated power. With UPQC in operation, under this swell condition, the series inverter is absorbing the extra active power by injecting the out-of phase voltage (25%). In

this case the series inverter handles 25.4 kW active power. The major portion (22.77 kW) of this active power is fed back to the source by shunt inverter. The combination of source and UPQC restricts the power being supplied to the load up to 99.84% of its rated power.

2.5.8 Voltage Fluctuation / Flicker Compensation

Voltage fluctuation or flicker is often difficult-to-solve power quality problem. It occurs, typically, due to voltage variation or phase-shifting harmonics, resulting from frequent motor starts, switching of capacitors or other load changes at the customer site or at other sites on the same line, or from momentary high impedance faults like trees brushing the line. Rapid voltage deviations could produce extremely annoying fluctuations in the output of lights, especially if the frequency of repetitive deviations is 5-15 Hz. Motors and equipments are designed to be most efficient at a set voltage and any minor fluctuations, up or down, decreases the motor's efficiency, generate heat and electrical losses. Significant voltage fluctuations can cause equipment to shut down or fail. Conventional flicker control is accomplished with static VAR compensators, which use passive devices. However, these devices may not provide adequate protection because their response time is not fast enough to regulate the voltage, and may allow additional voltage fluctuation to occur.

In the following section, the flicker compensation capability of UPQC is tested. The simulated results are shown in Figure 2.14. The effect of a 5Hz flicker envelops on the source voltage is shown in Figure 2.14 (a). The term *flicker index* is defined as follows:

$$\text{Flicker Index} = \frac{\Delta v}{V} \tag{2.17}$$

$$\text{Where, } \Delta v = V_{P1} - V_{P2} \tag{2.18}$$

V_{P1} = Maximum positive or negative peak

V_{P2} = Minimum positive or negative peak

V' = Peak amplitude of rated voltage

For the given condition, using Figure 2.14 (a):

$$V'_{p1} = 552 \ , \ V'_{p2} = 408 \text{ and } V' = 480$$

Therefore, Flicker Index = 0.3 or 30 %

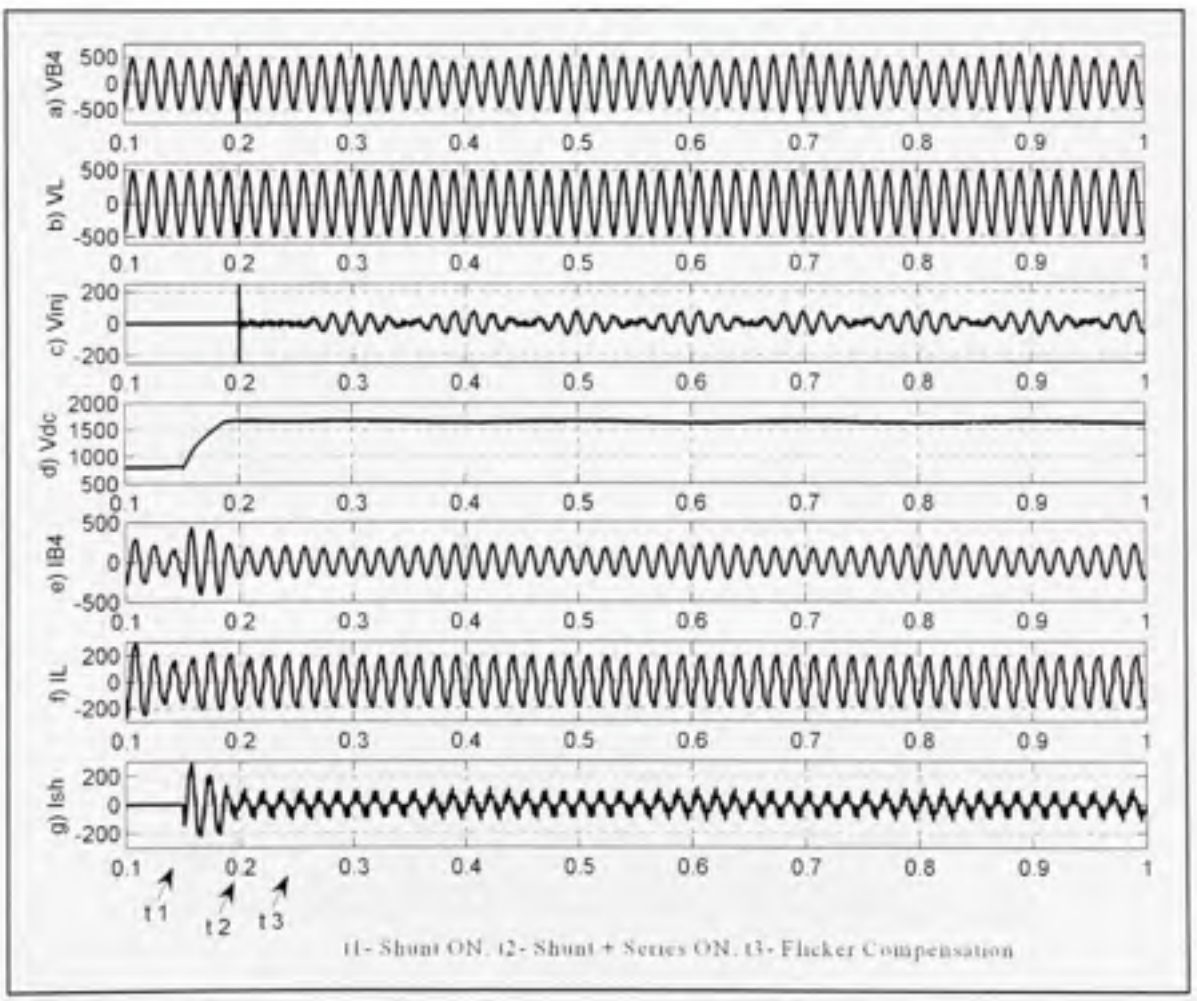


Figure 2.14 Simulation results: flicker compensation.

The UPQC effectively compensated this flicker condition on the system by injecting appropriate voltage through series inverter. The voltage injected by series inverter to

compensate the flicker effect is shown in the Figure 2.14 (c), whereas, the compensated load voltage is as shown in Figure 2.14 (b).

Thus for compensated load voltage, using Figure 2.14 (b);

$$V_{P1} = 485 \ , \ V_{P2} = 480 \text{ and } V = 480$$

Therefore, Flicker Index = 0.0104 or 1.04 %

Thus with UPQC installed, the flicker index is reduced from 30% to only 1.04% making load bus free from flicker variation. The three-phase source voltage and load voltage profiles are as shown in Figure 2.15.

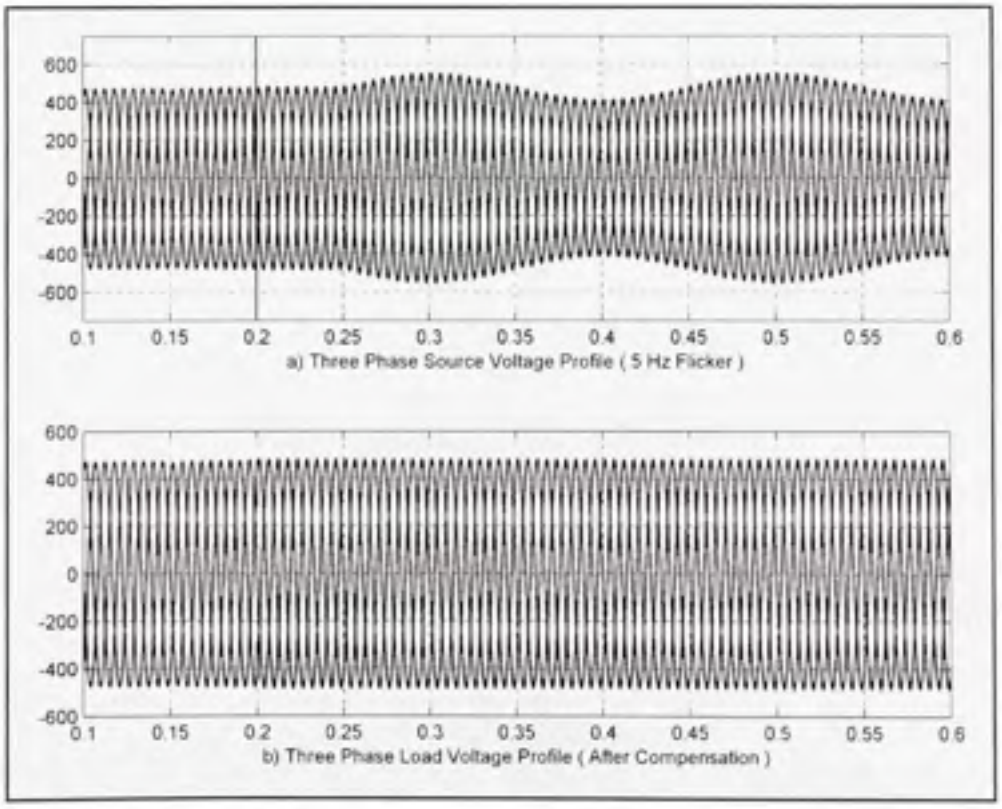


Figure 2.15 Three-phase source and load voltage profiles.

2.6 Laboratory Experimental Results

The performance of UPQC is also validated through laboratory experimental study. The experimental prototype consists of two voltage source inverter connected back to back through a capacitor which acts as a self supporting DC bus for proper operation of UPQC. A rapid prototyping board, DS1104 from dSPACE is used to implement and control the inverters, using proposed UVTG approach in real-time. The dSPACE is solely utilized to implement the controller approach. The PWM modulation is carried outside the dSPACE using analog circuitry. The detailed experimental setup and all the key components of hardware system are discussed in Appendix–I. In the following subsections, the experimental

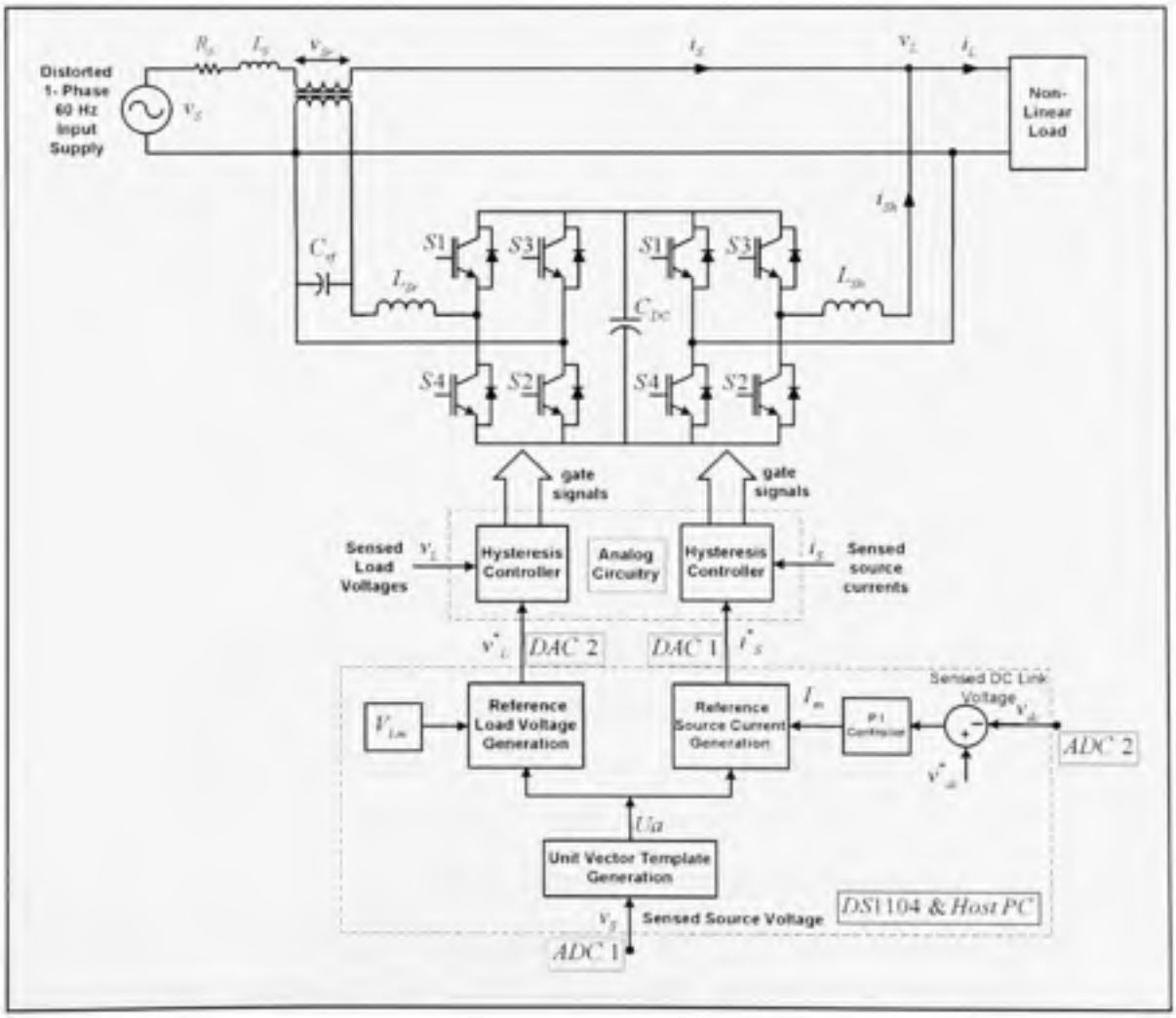


Figure 2.16 Hardware system set-up diagram for single-phase UPQC based on developed UVTG controller.

results for single-phase UPQC based on UVTG approach are discussed. The block diagram representation of UVTG based hardware system is shown in Figure 2.16.

2.6.1 Current Harmonics Compensation

The performance of UVTG approach to compensate the current harmonics generated by non-linear load is evaluated first. Figure 2.17 shows the experimental results when only shunt inverter is turned ON, whereas, the gate pulses to series inverter are not applied and the transformer secondary which is in the series of the line is short circuited. The load on the system is considered as a non-linear load, which realized using a diode bridge rectifier followed by RL load (R=13.3 Ω, L=50 *mH*). The load current profile shown in Figure 2.17 (a) [trace 3], has THD of 29.6%.

While performing the experimental investigation on the UVTG based approach, an interesting fact on PI controller based shunt inverter system is observed. The performance of UPQC, when the shunt inverter is in operation, is shown in Figure 2.17 (a). As noticed from the figure, the source current shows significant presence of harmonics even after the compensation (source current THD = 7.4%). Though, the close look at the figure suggests that the source current profile is combination of fundamental component superimposed by switching noise. The reason behind this partial compensation is explain here. As discussed in UVTG controller formation that the output of PI controller (which is error between actual and set reference DC link voltage) is multiplied with unit vector templates to generate the reference source current signals. In actual practice, when shunt inverter is in operation, the switching of its IGBT switches gives the switching transients/ ripples on the DC bus voltage, which can be noticed from Figure 2.17 (b) [trace 1]. The output of PI regulator, I_m, in real-time, is shown in trace 2. This output is highly distorted due to the presence of switching ripples on actual sensed DC bus voltage. The profile of generated reference source current is shown in trace 3, and it is clearly evident that the switching ripples on DC bus gives a distorted reference source current. The actual source current [trace 4], therefore, is highly

distorted. The above discussion suggests that a corrective action is essential on sensed DC bus voltage to achieve better performance from shunt inverter/ APF.

To overcome the problem due to the ripples on DC bus voltage, one of the simplest solutions is to filter out the ripples on DC bus voltage. Figure 2.17 (c) shows the experimental results after the use of one of such kind of filters. The actual sensed DC voltage, before processing through PI controller, is filtered out using a low pass filter (LPF). Here, in MATLAB/ Simulink model, a first order LPF with cut-off frequency of 15Hz is used. The output of PI regulator, after filtering out the ripples, is shown in Figure 2.17 (c) [trace 2], and as compared with Figure 2.17 (b) [trace 2], it gives ripple-free constant magnitude output. Therefore, the generated reference source current signal [trace 3] is perfect sinusoidal without any distortion or noise on it. The shunt inverter performance, with a LPF on sensed DC bus voltage, is given in Figure 2.17 (d). As noticed from the figure, the source current [trace 2], after the compensation, is now perfect sinusoidal with THD of 3.6%. The THD spectrum of load current and source current after compensation is given in Figure 2.18.

As it is well known that the use of LPF can create a problem, especially during a dynamic condition, since, its output response can be oscillating under sudden change in its input. The response of shunt inverter, therefore, is evaluated to make sure that the use of LPF does not result in undesirable performance from shunt inverter. Figure 2.17 (e) and (f) shows the experimental results without and with the use of a LPF on sensed DC bus voltage. As noticed from these figures, when shunt inverter is put into the operation, the DC bus regulator forces the DC bus voltage to settle down at new set reference value (here 100V). This is done by taking a fundamental component from the source. The system gets settle down at new steady state in 3-4 cycles. The output of PI controller with a LPF on DC bus voltage is shown in Figure 2.17 (f) [trace 2]. The sudden change in operation condition causes the output to oscillate before attending the new steady state condition. Thus, without a LPF there is no overshoot on the DC bus voltage, whereas, the use of LPF cause a slight overshoot. But, importantly, the inverter does not lose the control on the system and attains the new steady state in short period of time without affecting its compensation capabilities.

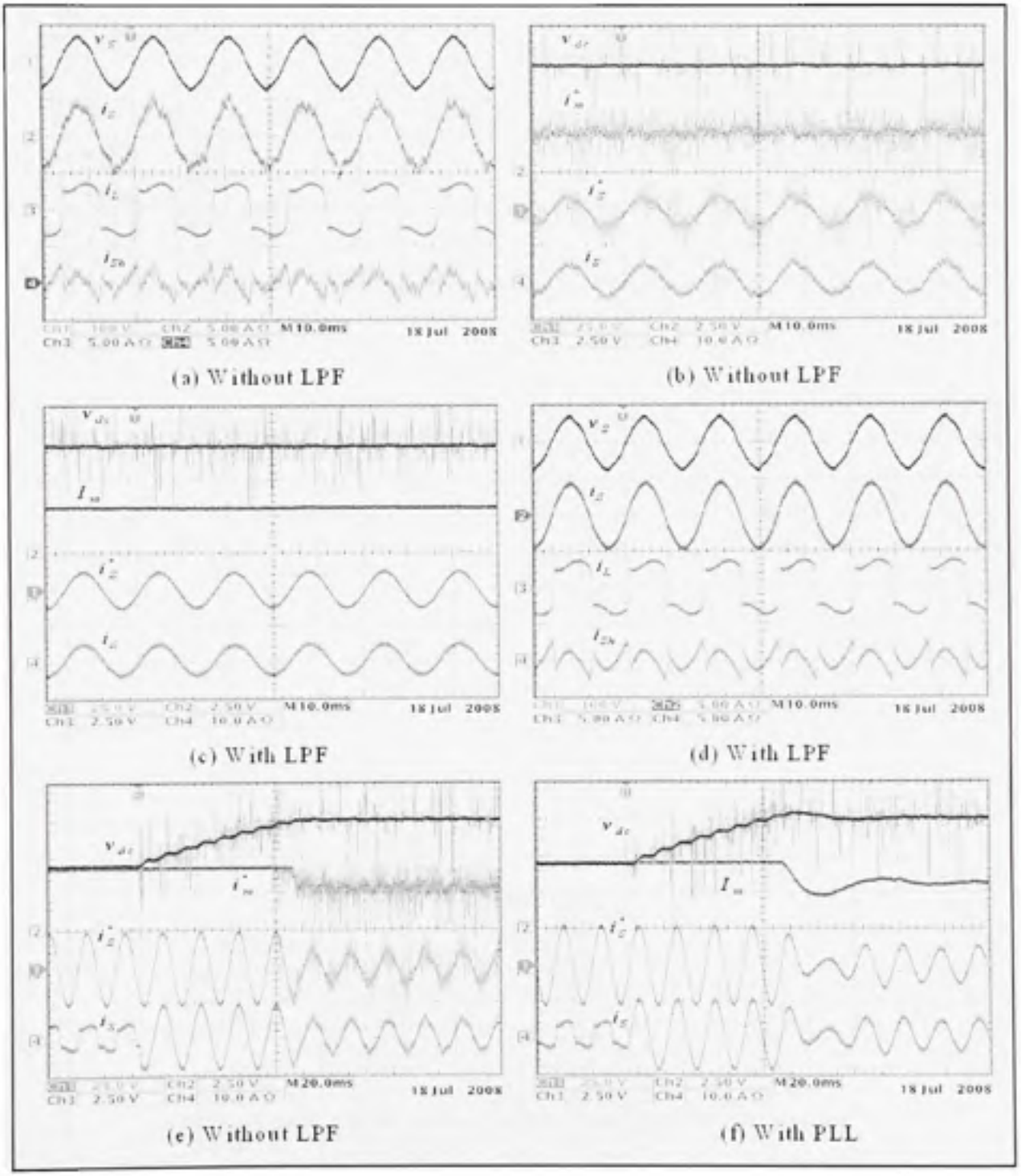
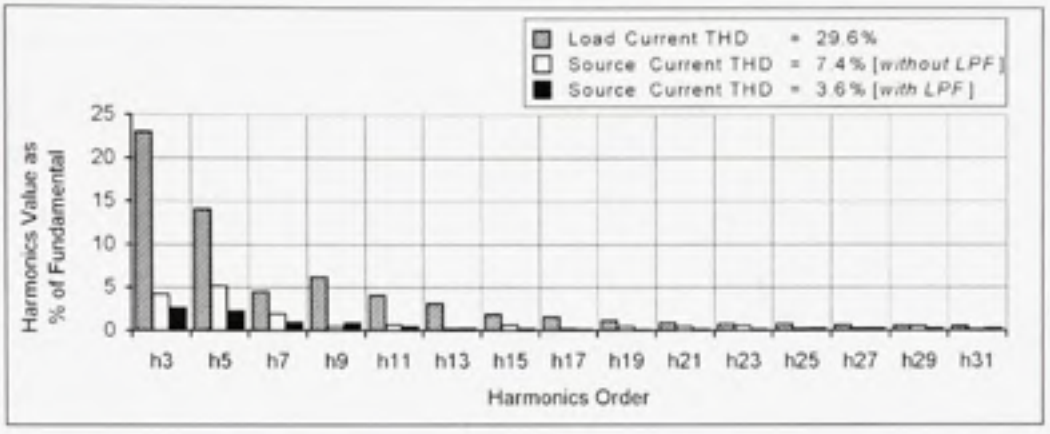


Figure 2.17 Experimental results: Current harmonics compensation and performance with and without use of low pass filter on sensed DC link voltage.



Harmonics	i_L	i_S (without LPF*)	i_S (with LPF)
	ODD HARMONICS (%)		
3	23.01	4.2	2.63
5	14.04	5.17	2.23
7	4.54	1.93	0.95
9	6.22	0.47	0.85
11	4.11	0.65	0.47
13	3.13	0.16	0.22
15	1.88	0.61	0.2
17	1.54	0.16	0.12
19	1.1	0.47	0.08
21	0.91	0.43	0.12
23	0.76	0.55	0.12
25	0.74	0.16	0.22
27	0.61	0.24	0.22
29	0.55	0.51	0.24
31	0.53	0.1	0.24
	EVEN HARMONICS (%)		
DC	0.72	0.65	0.53
2	0.15	0.83	0.2
4	0.08	1.03	0.06
8	0.08	0.26	0.08
10	0.08	0.32	0.02
% THD	**29.6%**	**7.4%**	**3.6%**

* *For controller development, with and without low pass filter (LPF) on sensed DC bus voltage*

Figure 2.18 Current harmonics compensation – harmonics spectrum and individual harmonic values as % of fundamental.

2.6.2 Reactive Power Compensation

The performance of shunt inverter, when a linear RL load (R=13.3 Ω, L=50 *m*H) is connected to the system is shown in Figure 2.19. This highly inductive load draws a load current [trace 3] which is at 0.58 lagging power factor with respective to the supply voltage. When shunt inverter is turned ON, it supplies the load reactive power demand by injecting a leading quadrature current [trace 4]. The shunt inverter compensates the load reactive power demand locally. Thus, the load seen by the source appears as a linear resistive load supplying only active power demand of the load at unity power factor. The reduction in source current magnitude [trace 2] as compared to actual load current [trace 3] magnitude also justifies the fact.

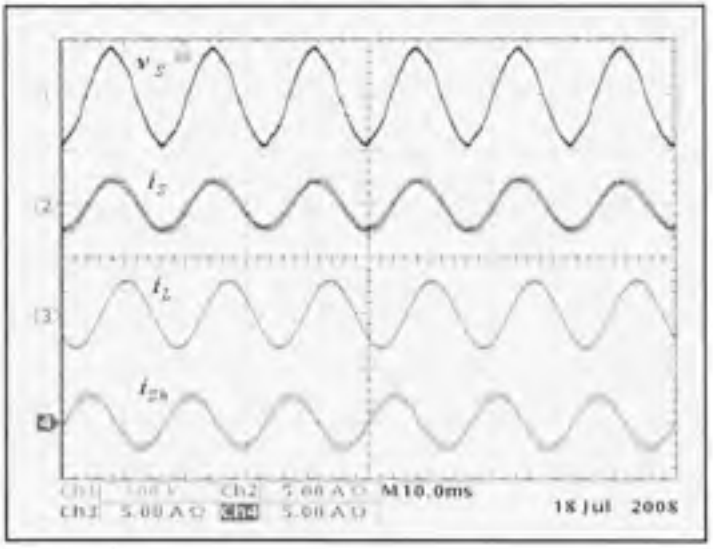


Figure 2.19 Experimental results: Reactive power compensation.

2.6.3 Dynamic Response under Sudden Load Change

The response of UPQC system during sudden load change condition is shown in Figure 2.20. Assuming the system is in steady state with a load L_1 (DBR with R=20 Ω, L=50 *m*H). At time t1, a resistive load (R=40 Ω) is suddenly connected across the load L1. The parallel combination of load L_1 and resistive load is marked as load L_2. The sudden increase in load current profile, at time instant t1, can be noticed from Figure 2.20 (a) [trace 3]. Within a

cycle, the shunt inverter controller detects the change in load current and takes the necessary action. As viewed from the source current profile [Figure 2.20 (a), trace 2], the changeover from one operating condition to the other is quite smooth, maintaining the perfect compensation. At time instant t2, the extra resistive load is suddenly removed from the system [Figure 2.20 (b)]. During this high to low load current changeover the shunt inverter maintains the perfect compensation. The sudden change in load on the system does not show any considerable effect on the DC bus voltage profile as viewed from [Figure 2.20 (c), trace 2].

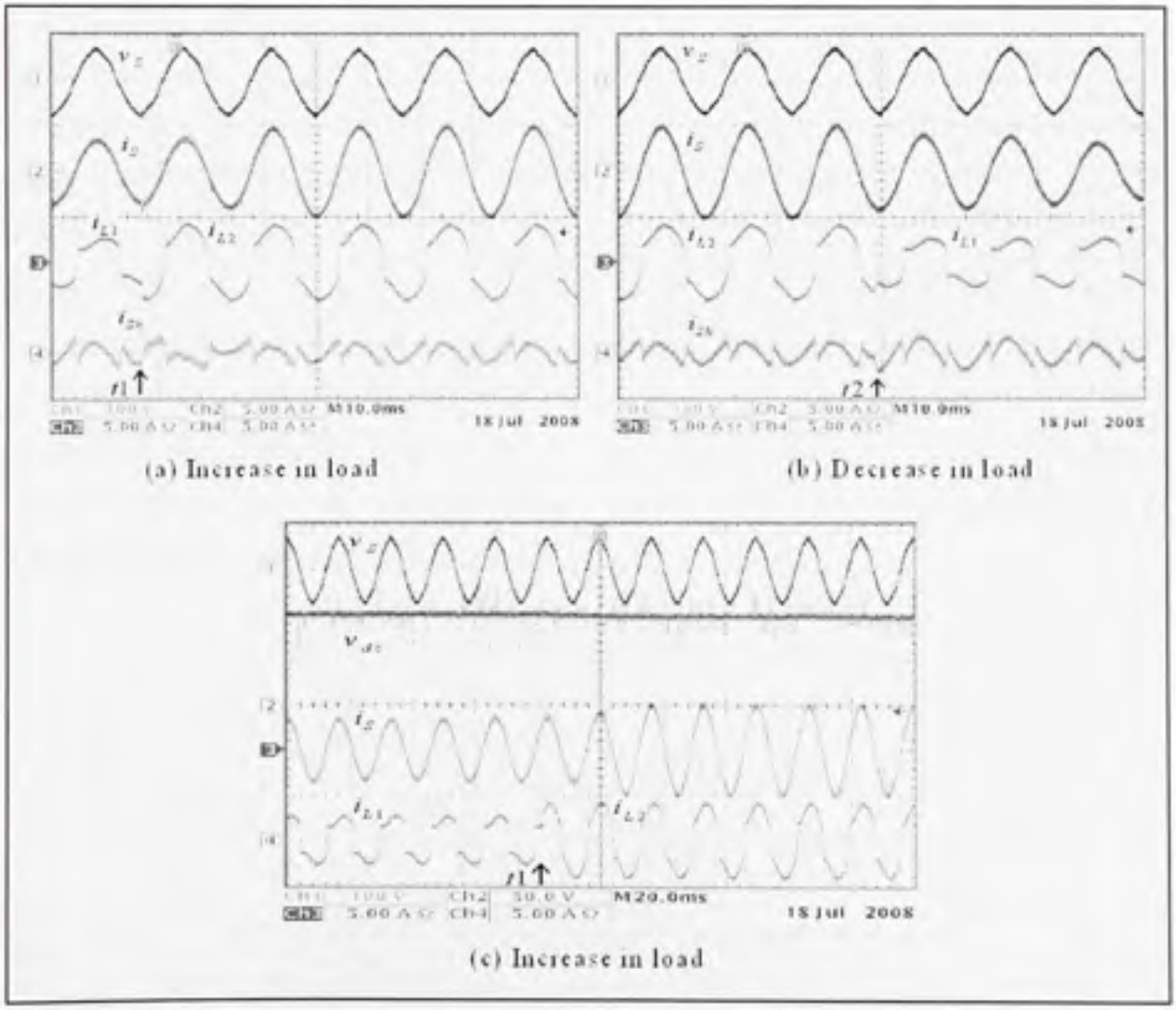


Figure 2.20 Experimental results: dynamic performance of shunt inverter.

2.6.4 Voltage Harmonics Compensation

The performance of UPQC, especially, under distorted voltage condition is discussed in the following subsections. The distortion in supply voltage is deliberately introduced. The experimental setup to introduce harmonics in supply voltage is shown in Figure 2.21. To cause a voltage drop in the line, which helps to generate distortion in supply voltage, an inductive impedance (2.5mH) is connected in the line. A capacitor is used to form a LC filter which helps to reduce the high frequency switching ripples on the voltage. The voltage available at point "X" has THD of 4%.

To further increase the distortion level in supply voltage, a diode bridge rectifier followed by a capacitor is used. It is noticed that, when a load is connected across the output of diode bridge rectifier load, the voltage gets severely distorted with THD of 40% and more. To generated moderated harmonics in supply voltage, the output of diode bridge rectifier is kept open circuited. Another interesting fact is that the distorted voltage thus generated at point "Y" is dependant on the current flowing through the line. This is due to the inserted impedance in the line to produce voltage drop across it. Therefore, when a linear RL load is connected to the system, the THD in supply voltage at point "Y" is noticed as 8.1%, whereas, with a non-linear load this THD level increases to 14%. In the following discussion, the voltage at point "Y" is considered as supply voltage.

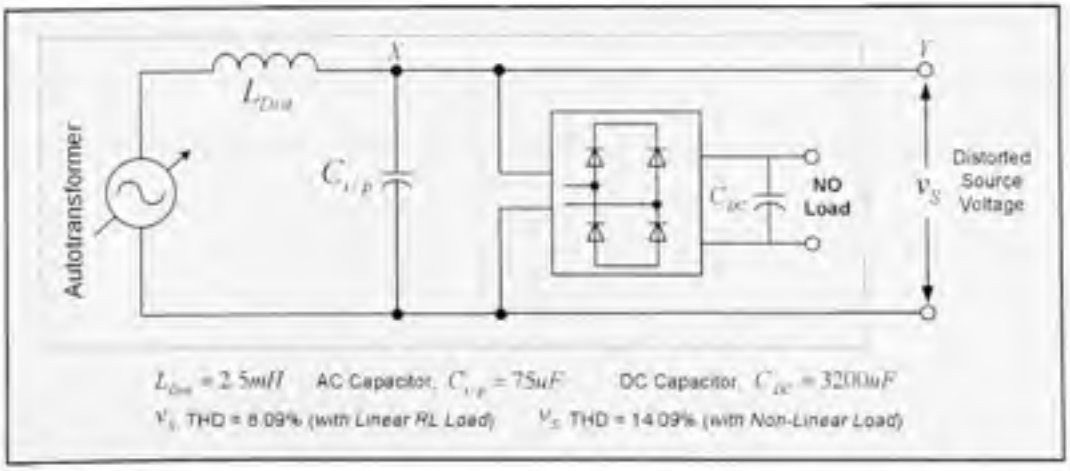


Figure 2.21 Experimental setup to generate harmonics in source voltage.

2.6.4.1 Performance under Linear RL Load

The experimental results, when a linear RL load is connected to the system, are given in Figure 2.22. The distorted source and load voltage profiles are shown in Figure 2.22, trace 1 and 2, respectively. The source voltage has THD of 8.1%. At this point the series transformer secondary is short circuited. Since the voltage at load terminal is distorted, the current drawn by the linear RL load (*0.72 lagging p. f.*) is also slightly distorted. Figure 2.22 (b) shows the experimental results when only series inverter is put into the operation. It is evident from the figure that the series inverter injects the necessary voltage [trace 3] in the line such that it cancels the harmonics present in the supply voltage. The distortion free load voltage profile can be noticed from Figure 2.22 (b) [trace 2]. The load voltage has THD of 3.2%. As the voltage profile at load bus gets improved, the current profile of RL load also becomes sinusoidal [Figure 2.22 (b), trace 4].

Figure 2.22 (c) shows the experimental results when both the inverters are in operation. The load voltage THD further reduces to 2.1% [trace 2]. This is due to the fact that the shunt inverter compensates the load reactive power demand locally, making source current sinusoidal and in phase with source voltage, and thus the profile of voltage dropped across inductive impedance also improves. The voltage distortion at point "Y" slightly reduces to 7.1% due to the reduced sinusoidal source current. The UPQC thus compensates the voltage harmonics presented in source voltage and load reactive power demand, simultaneously. The profile of self supporting DC bus voltage, current injected by shunt inverter, and voltage injected by series inverter is shown in Figure 2.22 (d), trace 1, 2 and 3, respectively. The harmonic spectrums of the source and load voltages are given in Figure 2.23.

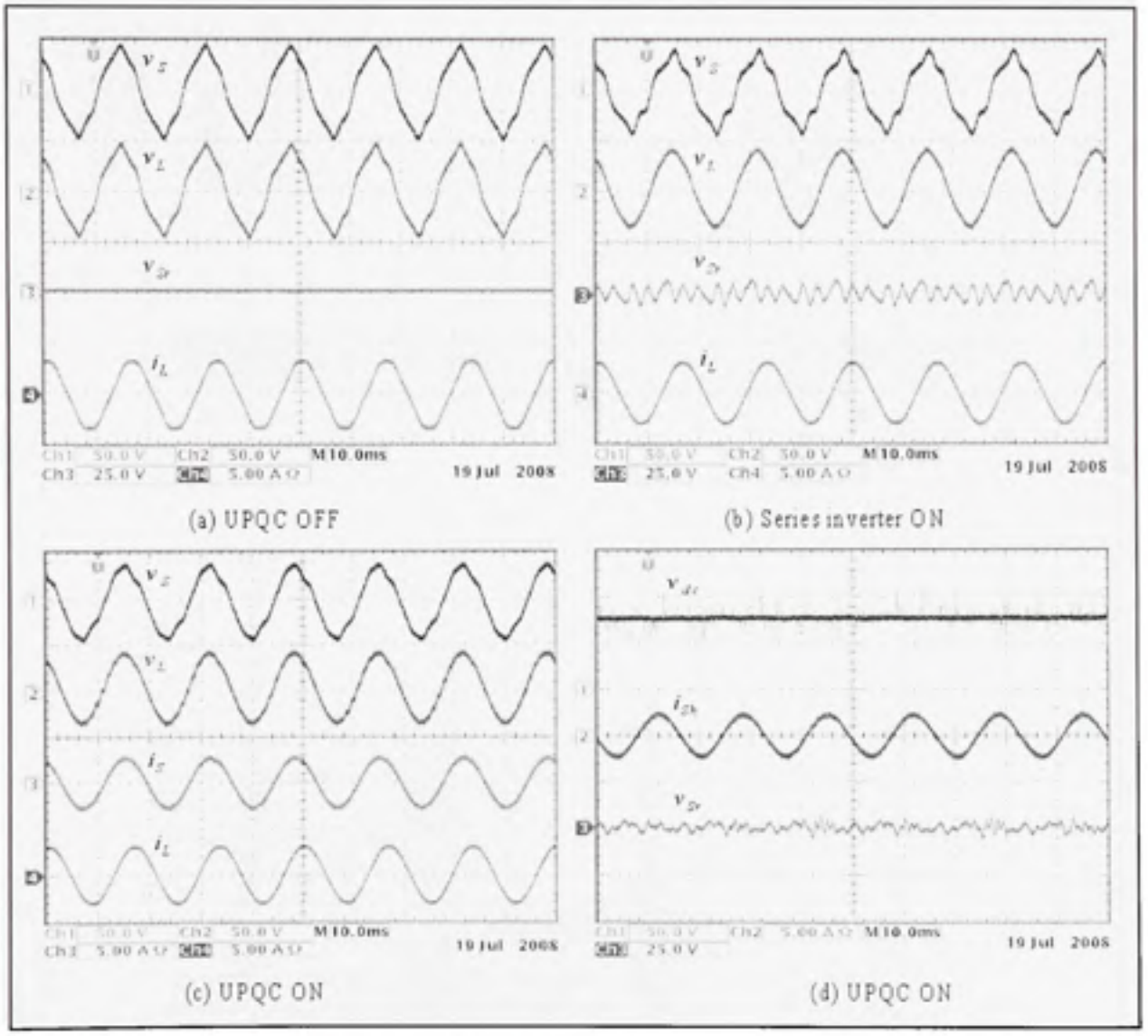
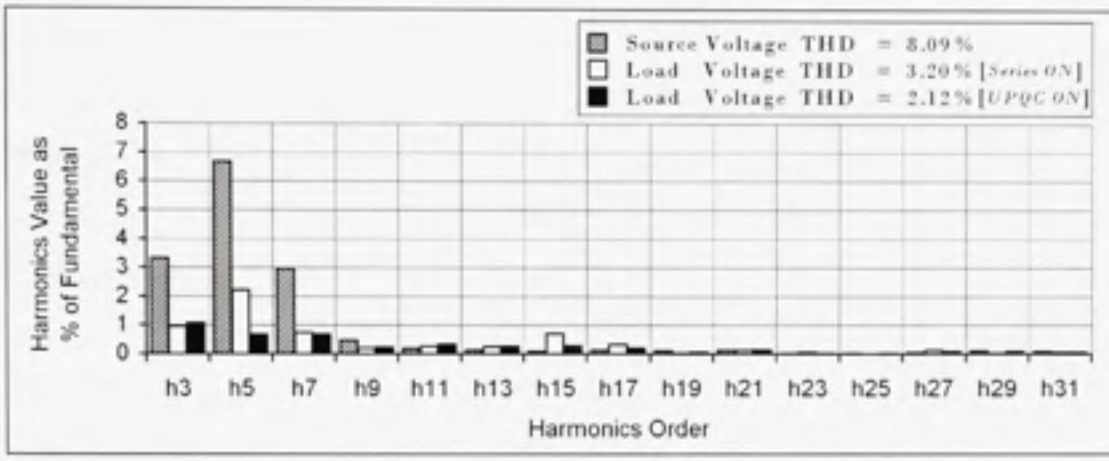


Figure 2.22 Experimental results: simultaneous voltage harmonics and reactive power compensation.



Harmonics	v_S	v_L (*Series ON*)	v_L (*UPQC ON*)
	ODD HARMONICS (%)		
3	3.32	0.94	1.07
5	6.67	2.21	0.66
7	2.96	0.74	0.69
9	0.47	0.21	0.23
11	0.18	0.27	0.32
13	0.13	0.24	0.26
15	0.08	0.71	0.29
17	0.13	0.32	0.20
19	0.10	0.03	0.06
21	0.13	0.12	0.14
23	0.03	0.06	0.03
25	0.03	0.00	0.03
27	0.05	0.12	0.09
29	0.10	0.03	0.09
31	0.08	0.06	0.06
	EVEN HARMONICS (%)		
DC	0.47	0.5	0.49
2	0.1	1.45	1.1
4	0.34	0.38	0.17
8	0.49	0.5	0.49
10	0.31	0.32	0.49
% THD	**8.09%**	**3.20%**	**2.12%**

Figure 2.23 Voltage harmonics compensation (under linear RL load) – harmonics spectrum and individual harmonic values as % of fundamental.

2.6.4.2 Performance under Non-linear Load

Simultaneous voltage and current harmonics compensation capability of UPQC is tested and discussed here. Due to the non-linear load on the system the supply voltage at point "Y" has THD of 14%. The distorted supply and load voltage profiles, when both the inverters are in OFF condition, can be noticed from Figure 2.24 (a), trace 1 and 2, respectively. The non-linear current profile shown in trace 3 has THD of 27.4%.

The improved load voltage profile, when only series inverter is in operation can be noticed from Figure 2.24 (b) [trace 2]. The load voltage has THD of 4.7%. Figure 2.24 (c) shows the interesting results when both the inverters are in operation. Here, the UPQC compensates the harmonics present in the source voltage and the current harmonics generated by non-linear load, simultaneously. This is the important application of UPQC, where, it maintains the voltage at load bus sinusoidal, free from distortion and thus can help to protect a sensitive load connected to the weak gird. At the same time, the UPQC compensates the current harmonics generated by the non-linear load, making the non-linear load to appear as linear, as seen from the source side. This indeed restricts entry of current harmonics entering from load side in the network. With UPQC is in operation, the load voltage and the source current THDs are found as 2.54% and 4.5%, respectively. The harmonic spectrums of the source and load voltages are given in Figure 2.25.

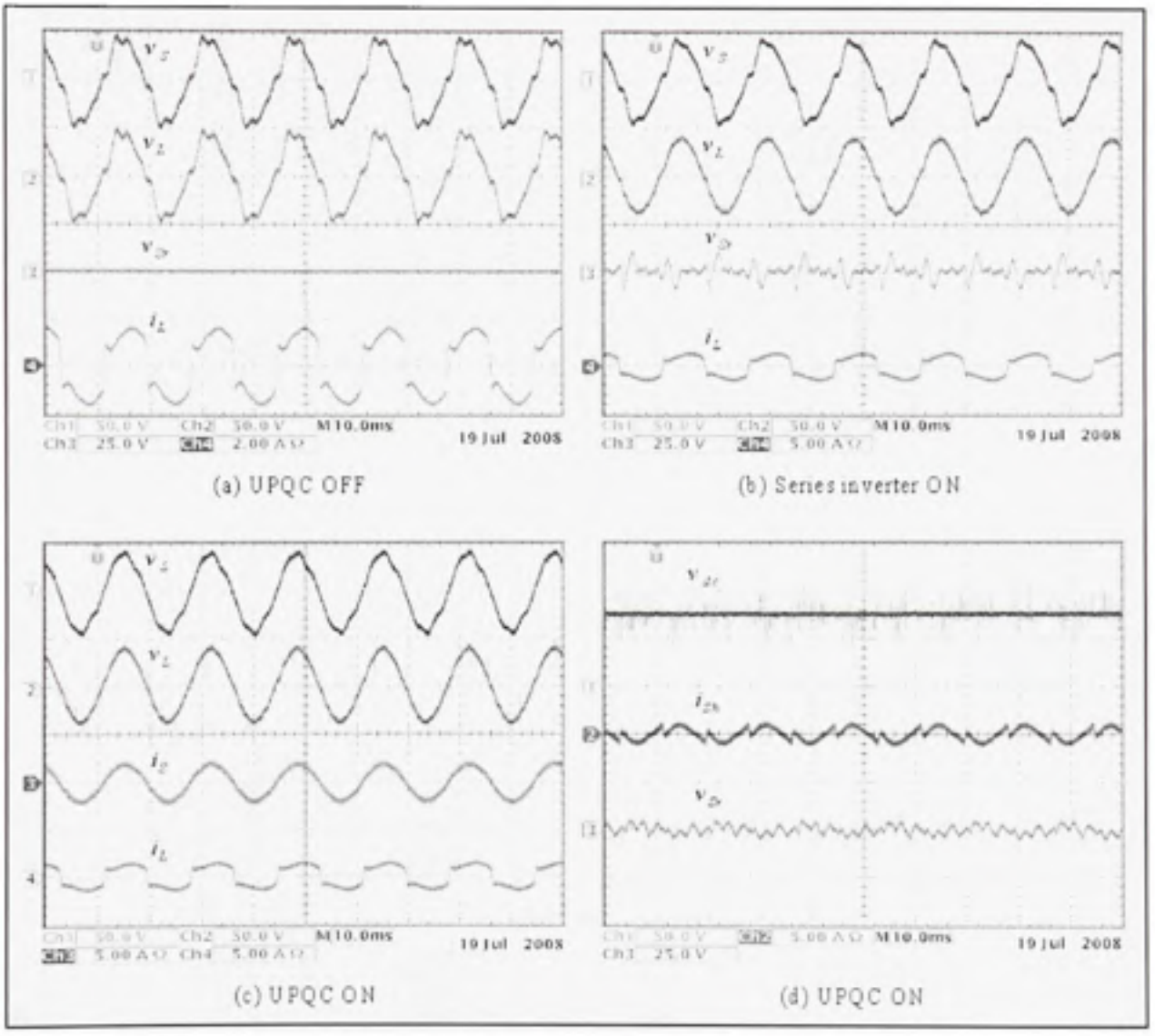
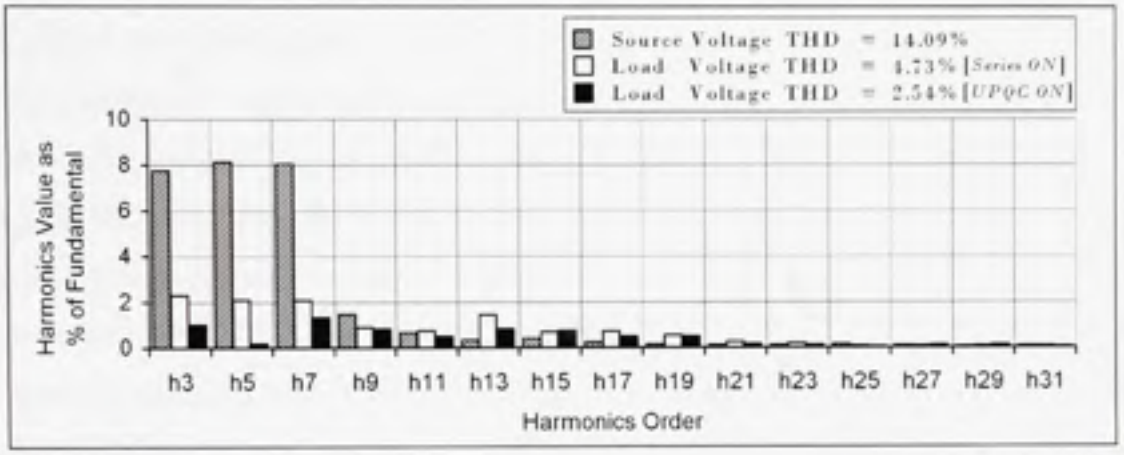


Figure 2.24 Experimental results: Voltage and current harmonics compensation under non-linear load



Harmonics	v_S	v_L (Series ON)	v_L (UPQC ON)
	ODD HARMONICS (%)		
3	7.75	2.3	1.02
5	8.12	2.1	0.17
7	8.05	2.07	1.31
9	1.47	0.88	0.8
11	0.65	0.74	0.48
13	0.32	1.45	0.82
15	0.4	0.68	0.74
17	0.22	0.71	0.48
19	0.12	0.54	0.48
21	0.1	0.26	0.14
23	0.1	0.17	0.11
25	0.12	0.06	0.03
27	0.07	0.06	0.11
29	0.02	0.06	0.09
31	0.05	0.06	0.03
	EVEN HARMONICS (%)		
DC	0.32	0.4	0.45
2	0.3	0.68	0.57
4	0.57	0.26	0.06
8	0.72	0.71	0.14
10	0.35	0.65	0.43
% THD	**14.09%**	**4.73%**	**2.54%**

Figure 2.25 Voltage harmonics compensation (under non-linear load) – harmonics spectrum and individual harmonic values as % of fundamental.

2.6.5 Voltage Sag Compensation

In this section the performance of UPQC to compensate sag on the system is discussed. Figure 2.26 shows the experimental results during sag on the system. There is sag of 30% on the system. The reduced source voltage can be noticed from Figure 2.26 (a) [trace 1]. As discussed in the simulation section and CHAPTER 1 (Section 1.4), in order to compensate sag on the system, the series inverter injects an in-phase voltage, which is the difference between desired load voltage and actual source voltage. By injecting the in-phase voltage, the series inverter is actually supporting the active power to the load. It is very important to have self supporting DC bus during this sag condition, in order to facilitate the active power transfer. Interestingly, this active power comes from the source only. The shunt inverter draws the necessary active power and maintains the DC bus voltage at constant level. This power is then fed back to the load by series inverter. Figure 2.26 (a) and (b) verifies the above mentioned fact.

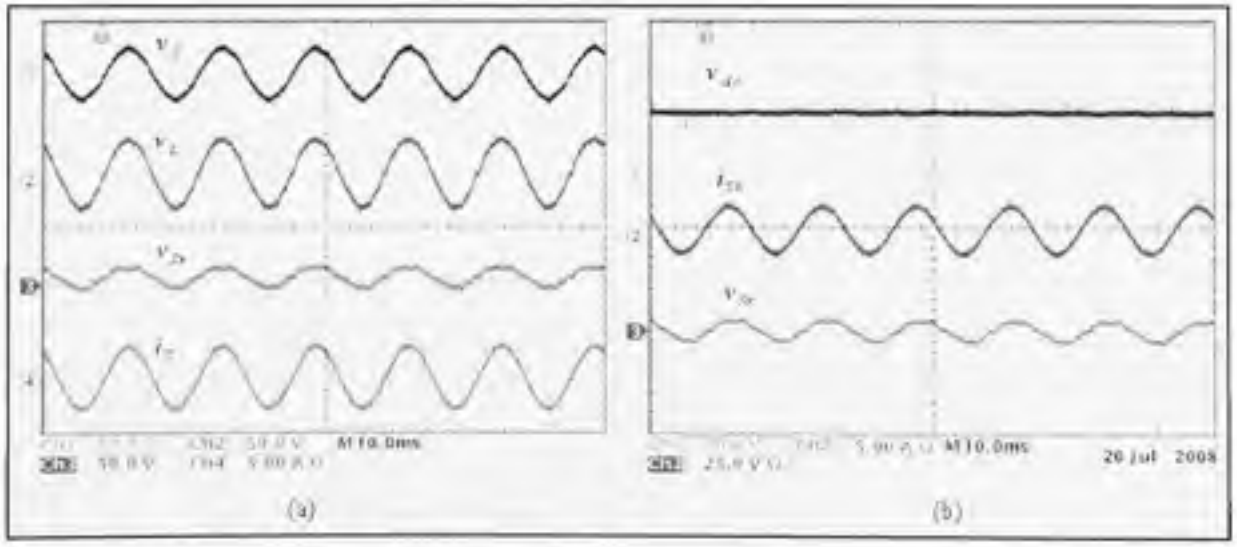


Figure 2.26 Experimental results: voltage sag compensation (steady state condition).

The injected series inverter in-phase voltage and the resultant load voltage profiles are shown in Figure 2.26 (a). As already discussed, the input source has THD of 4%. In order to maintain the voltage at load bus sinusoidal and at rated value, the series inverter injects sum of in-phase voltage and harmonics voltage. The self supporting DC bus voltage and the

necessary current drawn by shunt inverter along with series injected voltage is shown in Figure 2.26 (b), trace 1, 2 and 3, respectively. It is found that the UPQC under 30% sag condition is able to maintain the voltage at load bus up to 98% of its rated value. In addition to this, the UPQC also compensates the reactive power required by the RL load.

Figure 2.27 shows the experimental results during the sudden occurrence of sag on the system. To emulate the sag condition, the output of autotransformer is suddenly reduced. Since the output is reduced manually, the source voltage reduces slowly. As seen from Figure 2.27 (a), the reduction in source voltage [trace 1] does not appear on the load voltage [trace 2]. The series inverter injects the appropriate in-phase voltage [trace 3] in order to maintain the load voltage at desired level, whereas, the shunt inverter helps the series inverter by taking increased source current to maintain the DC link voltage at constant level. As noticed from Figure 2.27 (b), there is slight reduction in DC bus voltage during the sag condition, but it does not affect the performance of UPQC.

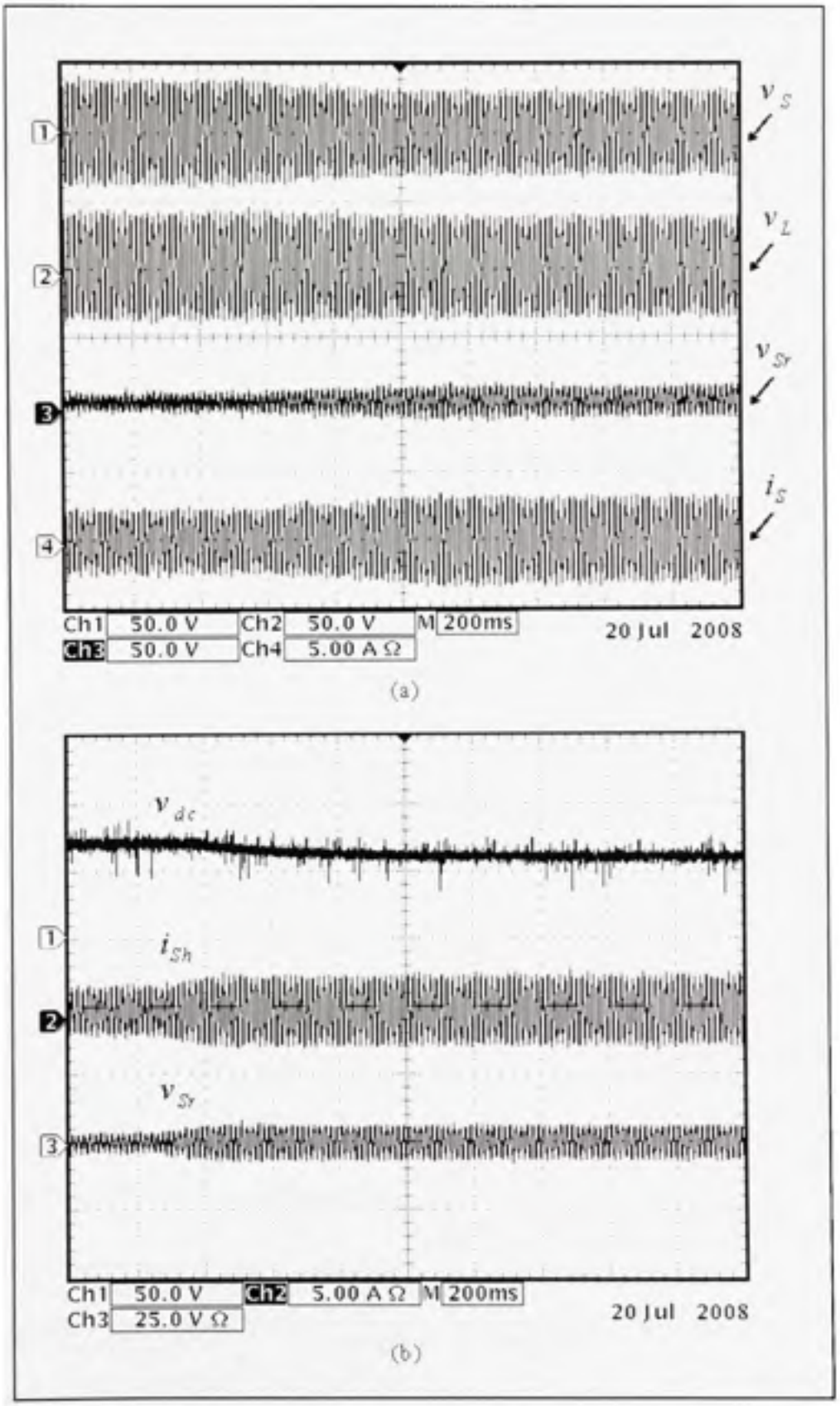


Figure 2.27 Experimental results: voltage sag compensation (dynamic condition).

2.6.6 Voltage Swell Compensation

In this section the performance of UPQC to compensate swell on the system is tested. The experimental results are shown in Figure 2.28 and Figure 2.29. A swell of 30% is imposed on the system. The operating principle of UPQC under swell condition is exactly opposite to the sag condition. During a swell on the system, in order to maintain the load bus voltage at desired constant level, the series inverter now injects a out-off phase voltage. Thus the extra voltage due to the voltage swell is cancelled out by series inverter. It is found that the ripple filter used during this experimental study, introduces some distortion in injected voltage, especially during voltage swell condition. Therefore, the load voltage is slightly distorted with THD of 5.7%, as can be noticed from Figure 2.28 (a) [trace 2]. The series injected voltage profile is shown in trace 3. Figure 2.28 (b) shows self supporting DC bus voltage profile along with shunt injected current and series injected voltage.

The experimental results during the sudden occurrence of swell on the system are shown in Figure 2.29. As noticed in previous section, the sag causes a dip in the DC bus voltage, on the other hand, the swell does not cause reduction in DC bus voltage [Figure 2.29 (b), trace 1]. Nevertheless, UPQC is able to compensate the swell on the system effectively. It is found that for a swell of 30%, the UPQC maintains the voltage at load bus at 102% of its rated value.

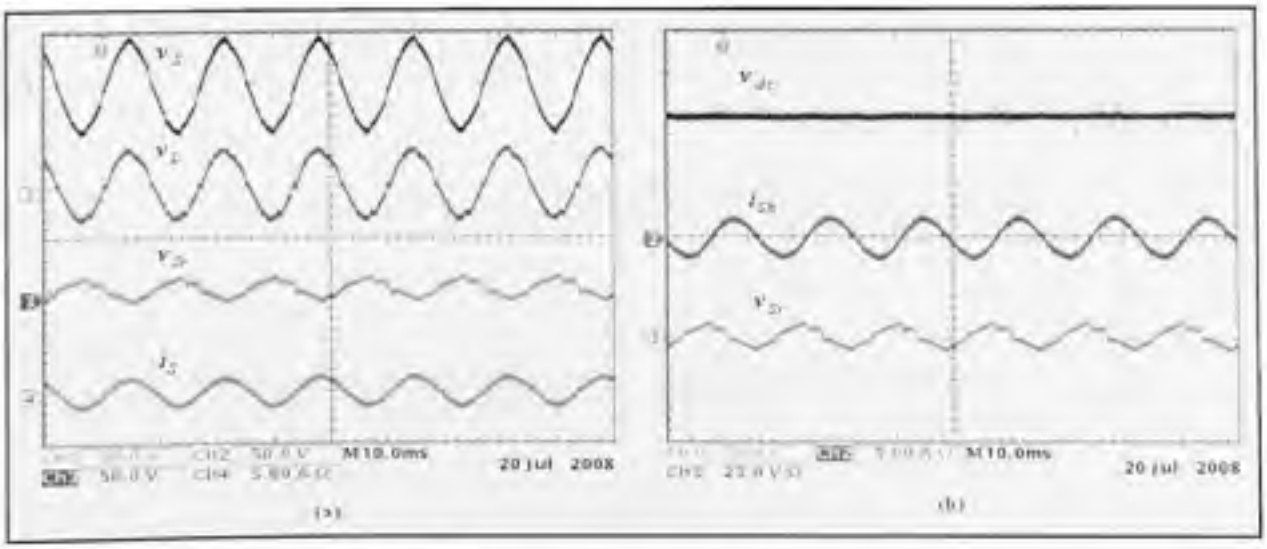


Figure 2.28 Experimental results: voltage swell compensation (steady state).

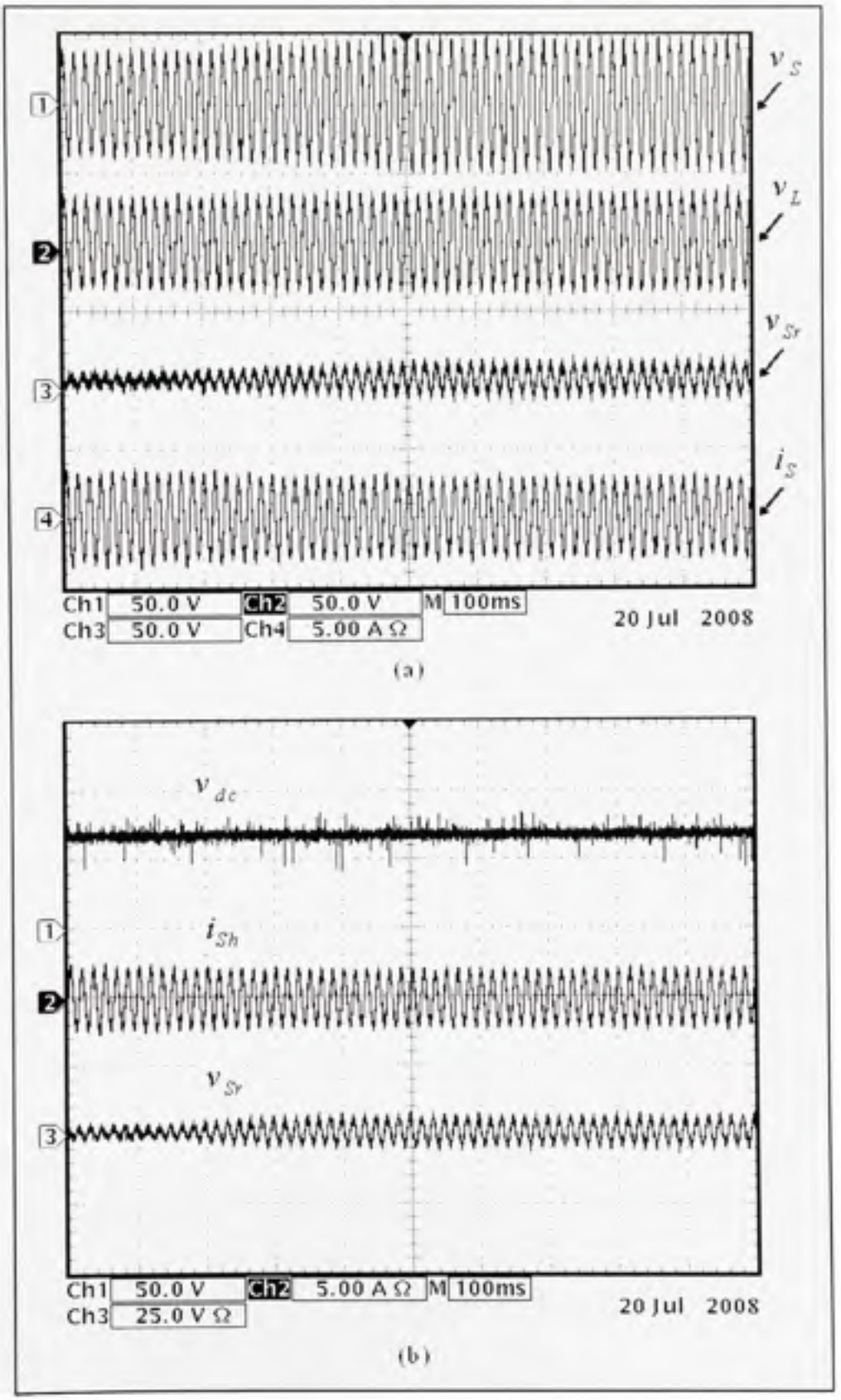


Figure 2.29 Experimental results: voltage swell compensation (dynamic).

2.6.7 Voltage Fluctuation/ Flicker Compensation

Figure 2.30 shows the experimental results under the fluctuating voltage condition. The envelops of source and load voltages are given in Figure 2.30 (a) [trace 1 and trace 2]. The UPQC injects appropriate voltage in order to maintain the load bus voltage at desired constant level. As noticed from the figure, the flicker in the supply voltage is greatly reduced at load terminal. The profiles of series injected voltage and the source current are shown in Figure 2.30 (a) [trace 3 and trace 4].

The profile of self supporting DC bus is shown in Figure 2.30 (b) [trace 2]. The shunt inverter, during this flicker condition facilitates the active power exchange between source, UPQC, and the load by taking necessary current form the source. It is important to point out that the shunt inverter is able to maintain the DC bus voltage at constant level, without any dip or rise in voltage, which indeed helps to achieve better performance from the UPQC. As already discussed in the sag condition, the increased source current profile can also be noticed from the figure, especially, when voltage is at minimum level during the flicker on the system.

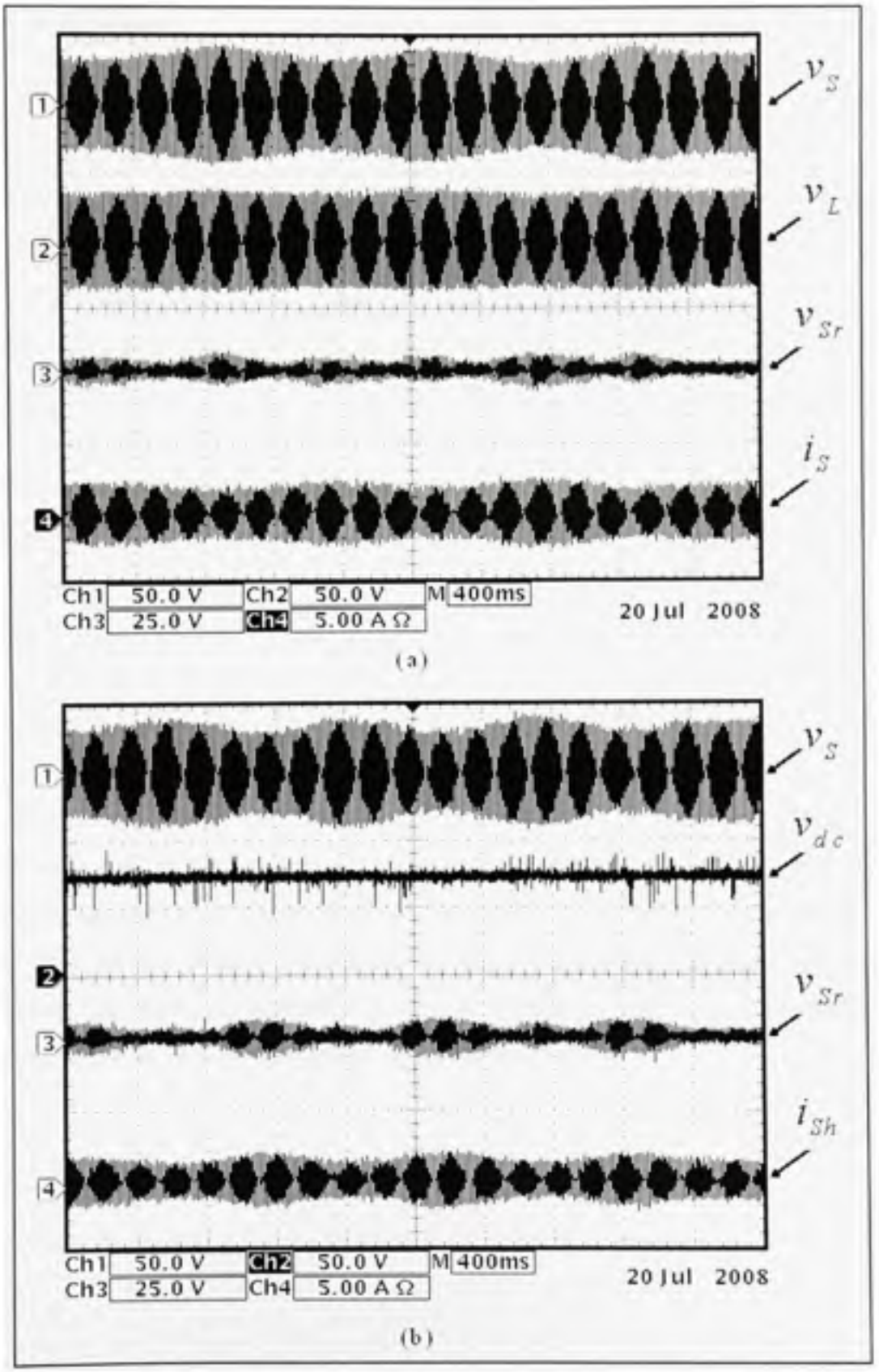


Figure 2.30 Experimental results: Voltage flicker compensation (dynamic).

2.7 Conclusions

This chapter explores the capabilities of unified power quality conditioner (UPQC). The UPQC combines functionalities of shunt and series active power filters. Thus, we have better and simultaneous control over load current as well as source voltage related power quality problems. The UPQC can be installed in order to isolate and thus to protect the loads within a plant from any disturbance in the source voltage. In addition to this, it also acts as harmonic suppressor, and thus prevents the penetration of current harmonics from the plant side towards the network.

The performance of UPQC to compensate the most significant power quality issues on distribution level, such as, current harmonics, reactive current, voltage harmonics, voltage sag, voltage swell and voltage flickers, is evaluated by simulation as well as with experimental validations. Under distorted supply voltage (THD = 14.09%) with non-linear load on the system (load current THD = 30.14%), the UPQC is able to reduce the THD in load voltage to 2.54%, whereas, the source current THD is found as 4.5%.

The work presented here may show significant impact on the feasibility of UPQC to be installed in actual distribution networks. The developed controller (UVTG), extensive simulation study under realistic network and the laboratory experimental investigation highly supports the future prospective for the UPQC being commercialized for practical applications. Therefore, in summary, it can be concluded that the joint-venture project between ETS, IREQ, and Hydro-Québec was a great success.

CHAPTER 3

VOLTAGE SAG COMPENSATION THROUGH REACTIVE POWER

3.1 Introduction

This chapter focuses on voltage sag compensation – one of the most undesirable phenomenons on power distribution level. Recently, static compensators (D-STATCOM) and dynamic voltage restorers (DVR) have been utilized to overcome the voltage sag problem (Haque, 2002; Newman *et al.*, 2003; Masdi *et al.*, 2004). The D-STATCOM can help to compensate voltage sag along with load current harmonics, but its performance can be affected in the presence of voltage harmonics. On the other hand, the DVR can effectively compensate voltage sag with reactive power control and minimum active power injection mode, under a distorted utility condition, but it can not tackle the load current harmonic problem effectively. The UPQC can also be considered as an integration of D-STATCOM and DVR.

As highlighted in the CHAPTER 2, by utilizing UPQC, the voltage sag is effectively compensated by injecting in-phase voltage through series inverter equals to the difference between the rated load voltage and reduced voltage due to the sag condition. In order to achieve the adequate voltage sag compensation the shunt inverter draws the required active power from the source side. Since active power is involved in voltage sag compensation it is termed as UPQC-P. The other possible approach to tackle the sag on the system is through reactive power control and when UPQC is controlled in such manner then it is referred as UPQC-Q (Basu *et al.*, 2002).

This chapter deals with the voltage sag compensation using reactive power control. A simplified approach is proposed to estimate the required quadrature voltage magnitude. As the voltage sag is controlled by reactive power by injecting voltage in quadrature with source current through series inverter, the UPQC-Q does not require any active power. Detailed mathematical formulation to estimate the required quadrature voltage is also given in the

chapter. The proposed simplified approach for quadrature voltage injection (QVI) is first validated through simulation studies. Later on, in-depth laboratory experimental results for single-phase as well as three-phase UPQC-Q system are given. Finally, a discussion on voltage sag compensation using active and reactive power control approaches is carried out.

3.2 UPQC-Q Concept

UPQC is one of the most effective power quality conditioning devices that can be utilized for voltage sag compensation at the distribution level. The voltage sag compensation can be done by using active power as well as reactive power control. When UPQC is used to compensate voltage sag by reactive power control, it is termed as UPQC-Q. The concept is to inject a quadrature voltage such that the sum of actual source voltage and the injected voltage will give the required rated voltage at the load bus terminal. The shunt part of UPQC necessarily maintains the unity power factor operation at the source side under all kinds of loads. Injecting the series inverter voltage in quadrature with the source thus essentially is in quadrature with the source current too. Power handled by the series inverter is governed by its injected voltage and the current flowing through the series transformer. Therefore, by injecting the series inverter voltage in quadrature with the source voltage eliminates the need of active power to compensate the sag on the system. However, the resultant voltage thus achieved gives phase angle shift with respective to the source voltage.

There are two possible ways to inject the quadrature voltage: 90^0 lagging or 90^0 leading. If the load is inductive in nature, the later has advantage of input power factor improvement due to a reduction in the effective phase angle between source voltage and load current, and hence, is considered in this research work. Thus, during voltage sag compensation using UPQC-Q, the reactive power burden on shunt inverter may get reduced. This is an additional benefit of QVI control of UPQC-Q when compared to the voltage sag compensation by the active power control method. Since, in case of active power control, the power handled by shunt inverter increases with increased percentage of sag (Khadkikar *et al.*, 2006a, 2006c), and it increases the required shunt inverter ratings.

3.2.1 UPQC-Q Phasor Representation

The phasor representation for basic understanding of operating principle of quadrature voltage injection (QVI) is shown in the Figure 3.1. For simplicity, the load is considered as linear RL and it is assumed that the load remains same during steady-state as well as during sag conditions.

Under normal steady-state operating condition, the load voltage $V_{L(0)}$ is at rated supply voltage $V_{S(0)}$ value, taking a load current $I_{L(0)}$ with a lagging power factor angle of φ_L. Now, a sag condition occurs on the system or on PCC such that the supply voltage reduces to $V_{S(1)}$. In order to maintain the load voltage at rated value (V^*_L), the series inverter should inject an appropriate compensating voltage. With reactive power control approach, the injected voltage should be $V_{Sr(1)}$, in quadrature with the source current such that the resultant load voltage will become $V_{L(1)}$. As noticed from the Figure 3.1, the injection of quadrature voltage causes the resultant load voltage to lead the source voltage. The phase angle difference thus occurs between the source and the resultant load voltage, denoted as power angle δ_1.

Interestingly, the power angle δ_1 causes a load phase angle boost with respect to the source voltage giving β_1, an effective phase angle between $V_{S(1)}$ and $I_{L(1)}$. As the load on the system is considered to be constant during this operation, the phase angle between $V_{L(0)}$ - $I_{L(0)}$ and $V_{L(1)}$ - $I_{L(1)}$ would not get affected. The phase advancement between load currents $I_{L(0)}$ and $I_{L(1)}$ is equal to δ_1. The QVI not only compensates the voltage sag but also improves the effective input power factor angle and thus, supplies a certain amount of reactive power through series inverter too. For higher % sag $V_{S(2)}$, δ_2 would get more advanced, reducing β_2 further, but at the same time increasing the series compensating voltage magnitude ($V_{Sr(2)}>V_{Sr(1)}$).

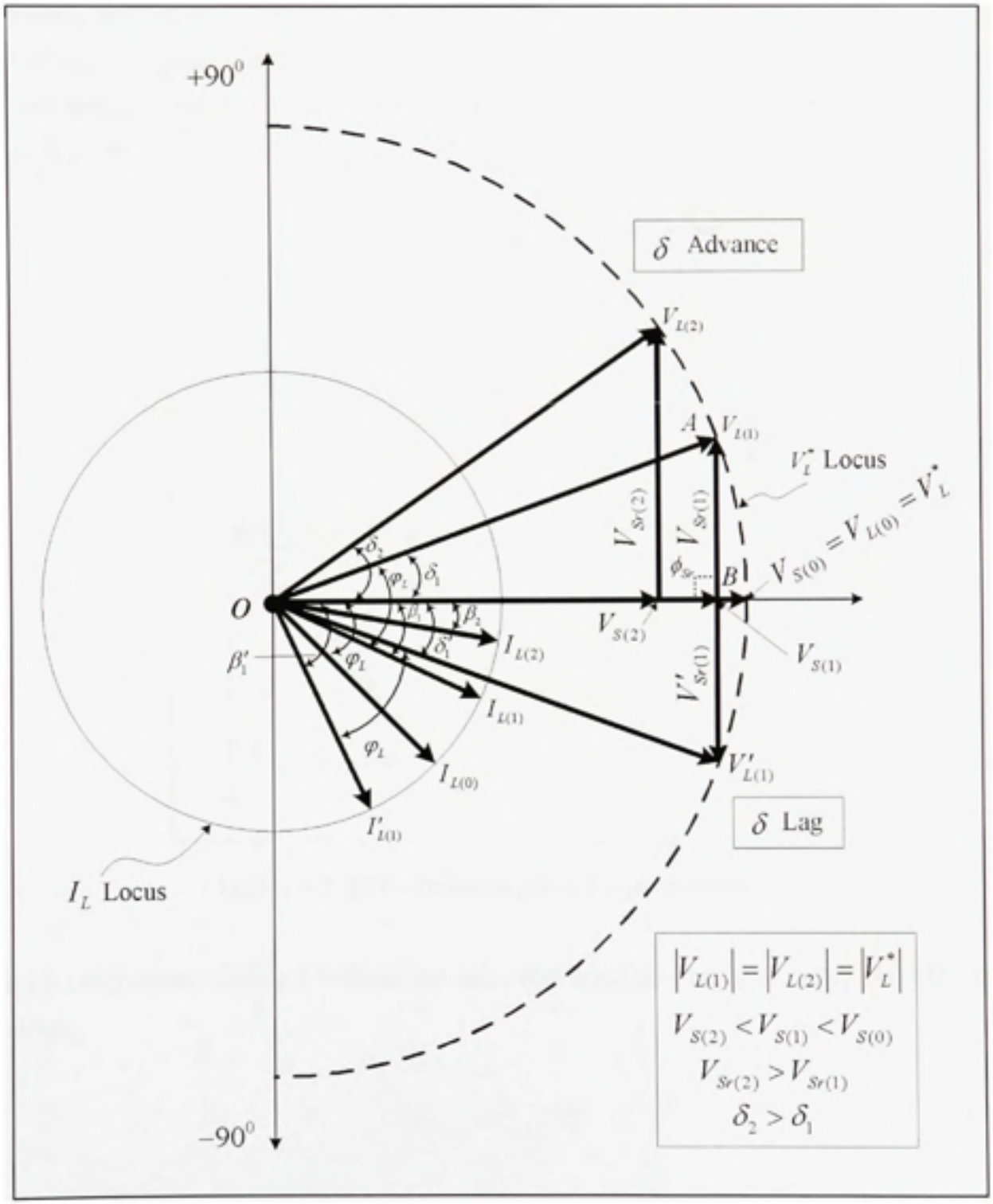


Figure 3.1 UPQC-Q concept: phasor representation.

3.2.2 Proposed Approach to Estimate Quadrature Injection Voltage

A simple approach is proposed below to estimate the required quadrature injection voltage for effective voltage sag compensation (Khadkikar *et al.*, 2006d). The detailed phasor representation to determine the required parameters of the proposed QVI approach is shown in Figure 3.2.

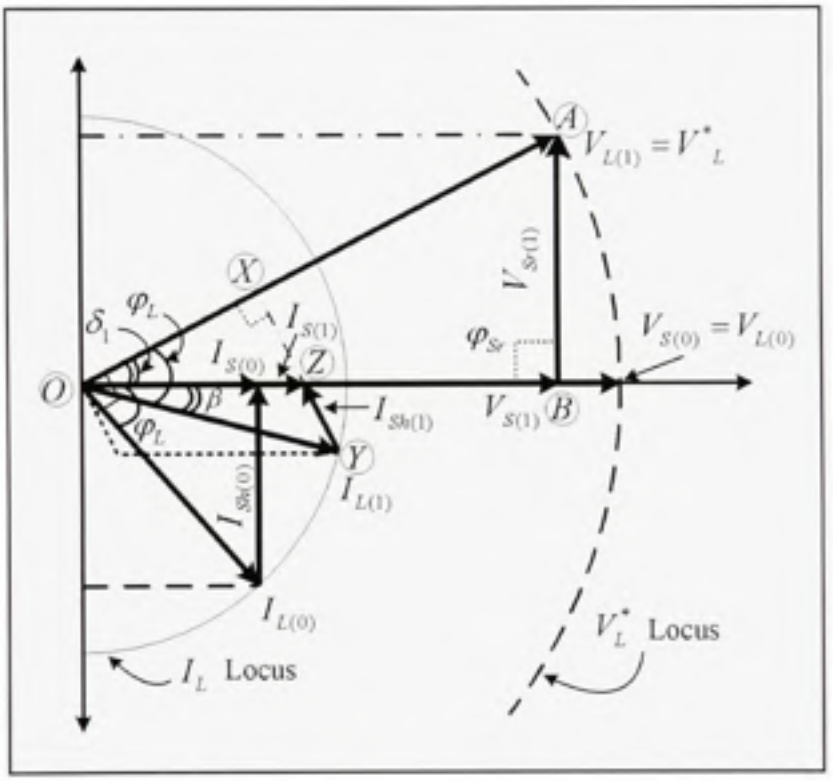


Figure 3.2 QVI – Detailed phasor representation.

Under steady-state condition, without any sag, considering the rated load voltage as reference voltage;

$$V_{S(0)} = V_{L(0)} = V^*_L \tag{3.1}$$

During the voltage sag condition,

$$V_{S(1)} < V^*_L \tag{3.2}$$

From $\Delta\ OAB$ (Figure 3.2),

$$\cos\delta_1 = \frac{l(OB)}{l(OA)} = \frac{V'_{S(1)}}{V'_{L(1)}} \tag{3.3}$$

$$\text{Since, } \left|V'_{L(1)}\right| = \left|V^*_L\right| \tag{3.4}$$

$$\text{Therefore, } \delta_1 = \cos^{-1}\left(\frac{V'_{S(1)}}{V^*_L}\right) \tag{3.5}$$

The reduced source voltage during the voltage sag condition, $V'_{S(1)}$, can be determined easily and V^*_L is a known quantity, therefore, δ_1 can be calculated as:

$$\sin\delta_1 = \frac{l(AB)}{l(OA)} = \frac{V'_{Sr(1)}}{V^*_L} \tag{3.6}$$

$$\text{Therefore, } V'_{Sr(1)} = \sin\delta_1 . V^*_L \tag{3.7}$$

$$\text{In general, } V_{Sr} = (\sin\delta).V^*_L \tag{3.8}$$

Equation (3.8) gives the required magnitude of voltage to be injected in quadrature, through the series inverter, for effective voltage sag compensation.

Under steady state condition, to support load reactive power, the shunt inverter injects a compensating current $I_{sh(0)}$ in quadrature with the load voltage such that the source current $I_{s(0)}$ becomes in-phase with the source voltage, as shown in Figure 3.2. During voltage sag condition, as discussed previously, QVI by series inverter generates a phase lead between the resultant load voltage and the actual source voltage. However, the phase angle between the resultant load voltage and the load current $I_{L(1)}$ remains same. As seen from the source side,

this action certainly causes the reduction in load power factor angle from φ_L to β. The voltage which appears across shunt inverter is the resultant load voltage. In order to compensate the new reactive power demand, as seen from the shunt inverter side, the shunt inverter should now inject the compensating current $I_{sh(1)}$ in quadrature with the resultant load voltage. This is essential, since the shunt inverter should also not handle any active power. Now looking back from the source side, there is an increase in the resultant source current $I_{s(1)}$ magnitude. This is essential to maintain the active power balance in the entire network.

The increased source current magnitude can be calculated as:

$$\text{In } \Delta\, OXY,\ \cos\varphi_L = \frac{I(OX)}{I(OY)} \tag{3.9}$$

$$I(OX) = \cos\varphi_L . I_{L(1)} \tag{3.10}$$

$$\text{In } \Delta\, OXZ,\ \cos\delta = \frac{I(OX)}{I(OZ)} \tag{3.11}$$

$$\cos\delta = \frac{\cos\varphi_L . I_{L(1)}}{I_{S(1)}} \tag{3.12}$$

$$\text{Therefore, } I_{S(1)} = I_{L(1)} \cdot \frac{\cos\varphi_L}{\cos\delta} \tag{3.13}$$

The above equation gives the magnitude of increased source current in order to maintain the power balance in the entire network.

3.2.3 Active and Reactive Power Flow during QVI

The active and reactive power flow through the series inverter during QVI can be computed as:

$$P_{Sr} = V'_{Sr(1)}.I_{S(1)}.\cos\varphi_{Sr} \tag{3.14}$$

$$P_{Sr} = 0 \ \left(\text{since}, \cos 90^0 = 0\right) \tag{3.15}$$

$$Q_{Sr} = V'_{Sr(1)}.I_{S(1)}.\sin\varphi_{Sr} \tag{3.16}$$

$$Q_{Sr} = V'_{Sr(1)}.I_{S(1)} \ \left(\text{since}, \sin 90^0 = 1\right) \tag{3.17}$$

$$Q_{Sr} = \sin\delta.V'^{*}_{L}.I_{S(1)} \tag{3.18}$$

$$Q_{Sr} = \sin\delta.I_{L(1)}.\frac{\cos\varphi_L}{\cos\delta}.V'^{*}_{L} \tag{3.19}$$

$$Q_{Sr} = \left(\tan\delta\right).\left(\cos\varphi_L\right).\left(I_{L(1)}.V'^{*}_{L}\right) \tag{3.20}$$

$$Q_{Sr} \propto \tan\delta \tag{3.21}$$

The equation (3.21) suggests that the reactive power supported by the series inverter to compensate the voltage sag is the function of power angle δ. The power angle δ is dependant on the % of sag need to be compensated.

3.2.4 Critical Operating Condition

An interesting condition can occur, termed as critical operating condition, when δ becomes equal to φ_L. The phasor representation of above situation is shown in Figure 3.3.

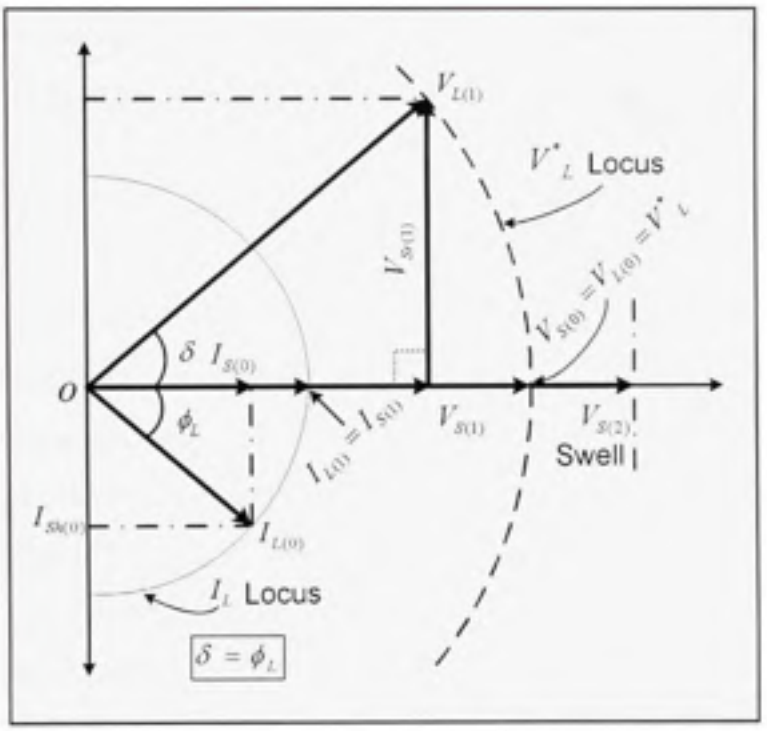


Figure 3.3 QVI – Critical operation condition.

$$\text{For critical condition, } \delta = \varphi_L \tag{3.22}$$

$$\text{Therefore, from (3.13), } I_{S(1)} = I_{L(1)} \tag{3.23}$$

Thus during a critical operating condition, the load current becomes in-phase with the source voltage such that no VAR compensation is required from the shunt inverter side. Thus the RL load now appears as a linear resistive load. However, in this mode of operation, the load active and reactive powers are supplied as active power. This causes an increase in source current magnitude from $I_{S(0)}$ to $I_{S(1)}$.

For any rise in voltage ($V_{S(2)}>V^{*}_{L}$), as shown in Figure 3.3, the quadrature injected voltage can not intersect the reference load voltage locus, suggesting that QVI with zero active power consumption does not compensate the swell on the system. However, with minimum active power involvement, the swell can be compensated easily. Further, if the load is having high power factor (close to unity), in such a scenario, the voltage sag compensation may result in leading load current operation with respect to the source voltage. In such cases the shunt inverter should inject lagging compensating current to achieve unity power factor operation.

3.3 UPQC-Q Controller Development

The source voltages can be distorted, therefore, it is essential to take necessary corrective action while developing the controller for UPQC-Q. As discussed in CHAPTER 2, to compensate the voltage sag using active power control, the load voltages were forced to be sinusoidal at a desired rated value. The advantage in forcing the load voltage is the harmonics in the source voltage (if any) gets compensated indirectly, without extracting them. In UPQC-Q the series inverter injects voltage in quadrature with the source current. Thus, we can not force the load voltage to be sinusoidal without extracting the harmonics present in the source voltage. In the following subsections, the extraction of voltage harmonics, and determination of the required quadrature injection voltage for voltage sag compensation, is explained in detail.

3.3.1 Voltage Harmonics Extraction

The *d-q* transformation based approach (Bhattacharya *et al.*, 2005) is used to extract the harmonic contained in the supply voltages. The three-phase distorted source voltages are first transferred into two-phase stationary co-ordinates using following eqution:

$$\begin{bmatrix} v'_{sd} \\ v'_{sq} \end{bmatrix} = \sqrt{\frac{2}{3}} \cdot \begin{bmatrix} 1 & -1/2 & 1/2 \\ 0 & \sqrt{3}/2 & -\sqrt{3}/2 \end{bmatrix} \cdot \begin{bmatrix} v_{sa} \\ v_{sb} \\ v_{sc} \end{bmatrix} \tag{3.24}$$

This transformation helps to represent the three-phase distorted supply voltages as direct (d) and quadrature (q) components, v^s_{sd} and v^s_{sq}, respectively. The notations "sd" and "sq" used to identify that the source voltage d and q quantities are extracted and the suffix "s" is used to denote that these quantities are in stationary reference frame.

The stationary reference frame quantities are then converted into synchronous rotating reference frame by using (3.25).

$$\begin{bmatrix} v^e_{sd} \\ v^e_{sq} \end{bmatrix} = \begin{bmatrix} \cos\theta & -\sin\theta \\ \sin\theta & \cos\theta \end{bmatrix} \cdot \begin{bmatrix} v^s_{sd} \\ v^s_{sq} \end{bmatrix} \tag{3.25}$$

Where, θ is a time variant angle that represents the angular position of the reference frame. This reference frame is rotating at a constant speed in synchronism with the three-phase ac voltages. A PLL can be used to extract $\sin\theta$ and $\cos\theta$ terms necessary for synchronous frame synchronization. The suffix "e" is used to denote the quantities which are in synchronous rotating frame. The transformation from the stationary reference frame to the rotating reference helps to separate the harmonics from the fundamental component. The term v^e_{sd} and v^e_{sq} can be represented as sum of AC and DC components:

$$\begin{bmatrix} v^e_{sd} \\ v^e_{sq} \end{bmatrix} = \begin{bmatrix} (\bar{v}_{sd})^e + (\tilde{v}_{sd})^e \\ (\bar{v}_{sq})^e + (\tilde{v}_{sq})^e \end{bmatrix} = \begin{bmatrix} v^e_{sd\_f} + v^e_{sd\_hr} \\ v^e_{sq\_f} + v^e_{sq\_hr} \end{bmatrix} \tag{3.26}$$

The DC quantities represent the fundamental frequency component, whereas, the AC quantities gives the total harmonics present in the supply voltage. The fundamental and harmonics components are denoted by the suffix "f" and "hr", respectively. The harmonics quantities can easily be extracted by using a high pass filter (HPF). These extracted harmonic components are transferred back to the stationary reference frame by (3.27) and then to the three-phase reference harmonic components of source voltage in $a-b-c$ frame by (3.28). Figure 3.4 gives the block diagram representation of voltage harmonics extraction using synchronous reference frame based method.

$$\begin{bmatrix} v^{s}_{sd\_hr} \\ v^{s}_{sq\_hr} \end{bmatrix} = \begin{bmatrix} \cos\theta & \sin\theta \\ -\sin\theta & \cos\theta \end{bmatrix} \cdot \begin{bmatrix} v^{c}_{sd\_hr} \\ v^{c}_{sq\_hr} \end{bmatrix} \tag{3.27}$$

$$\begin{bmatrix} v^{*}_{sa\_hr} \\ v^{*}_{sb\_hr} \\ v^{*}_{sc\_hr} \end{bmatrix} = \sqrt{\frac{2}{3}} \cdot \begin{bmatrix} 1 & 0 \\ -1/2 & \sqrt{3}/2 \\ 1/2 & -\sqrt{3}/2 \end{bmatrix} \cdot \begin{bmatrix} v^{s}_{sd\_hr} \\ v^{s}_{sq\_hr} \end{bmatrix} \tag{3.28}$$

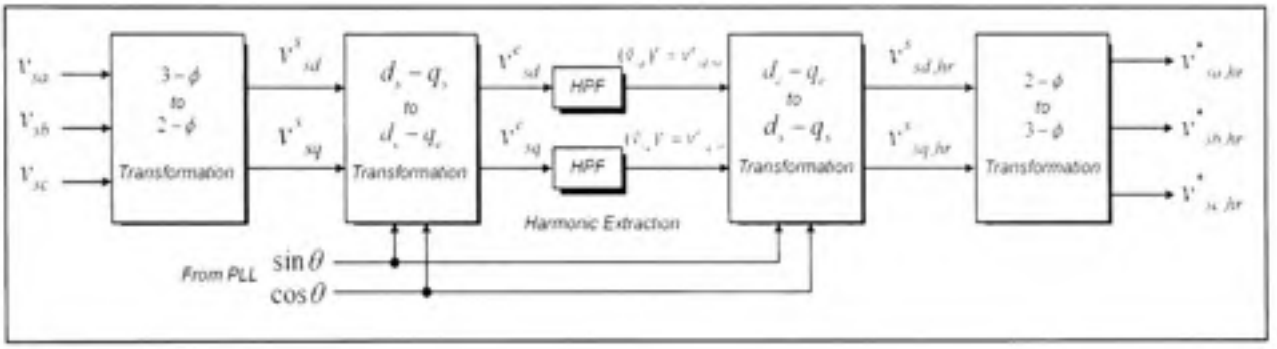


Figure 3.4 Voltage harmonic extraction based on synchronous reference frame method.

3.3.2 Determination of Quadrature Injection Voltage

In this section, real-time implementation of the proposed simplified approach for direct determination of required quadrature injection voltage is explained. For simplicity, it is assumed that the system voltages are balanced. The actual source voltage is sensed and its fundamental *rms* value is continuously computed, and divided by the constant rated load voltage magnitude. The resultant quantity represents the term cosδ and the power angle δ thus can be estimated easily. The required injection voltage magnitude V_{Sr}, for effective sag compensation, is then calculated using standard mathematical computations. If the supply voltages are unbalanced in nature, the separate *rms* values of each phase voltage and thus separate injection voltage magnitude determination would be required.

To generate three-phase reference sag signals at 90^0 phase lead, the terms $\sin\theta$ and $\cos\theta$ from PLL, used for voltage harmonics extraction, are utilized to generate three unity signals which are at 90^0 lead *w.r.t.* the actual source voltages. The shunt inverter helps to maintain the source current in phase with source voltage. The PLL on the source voltage gives accurate quadrature voltage *w.r.t.* the source current, the essential signals for voltage sag compensation using reactive power control. These signals are then multiplied with calculated series injected voltage magnitude V_{Sr}, giving the reference signals for voltage sag compensation.

Finally, the extracted reference harmonic voltage and sag signals are summed together to generate the reference compensating signals for the series inverter. The overall control block diagram for the series part of UPQC for simultaneous voltage sag and voltage harmonics compensation is shown in Figure 3.5. As discussed and highlighted in the previous chapter, the major function of shunt inverter is to maintain the DC link voltage at a constant level in addition to harmonic and reactive power compensation. The shunt inverter controller is realized using the UVTG approach.

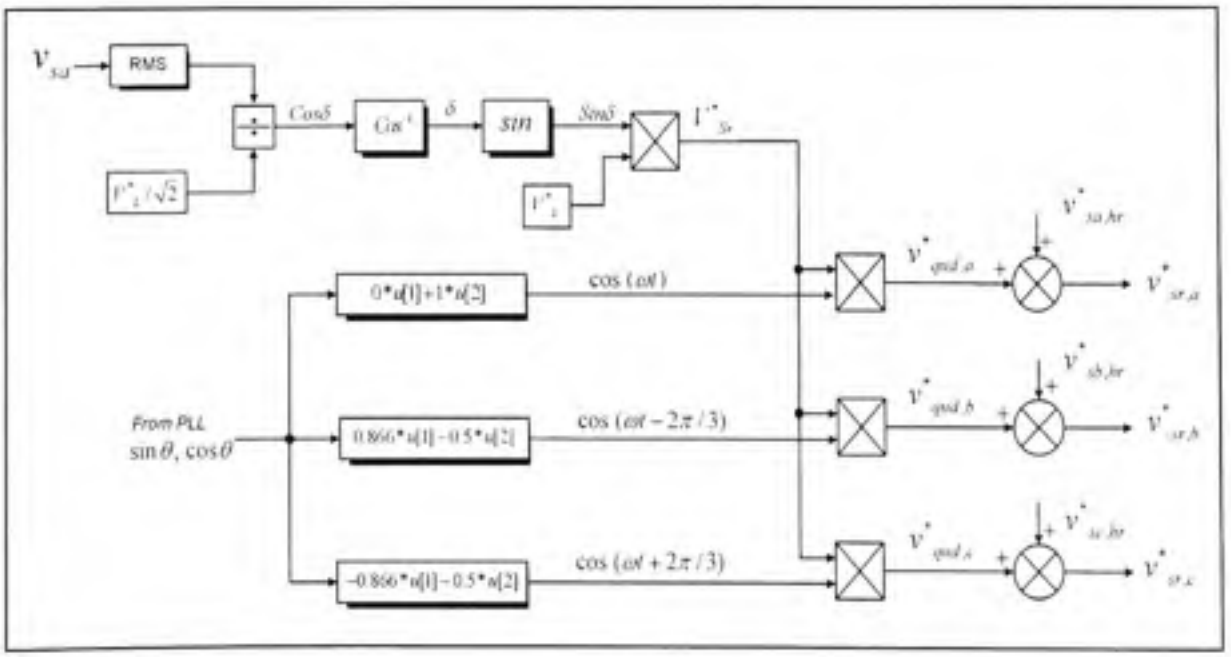


Figure 3.5 Overall control diagram for series inverter to compensate voltage sag and harmonics.

3.4 Simulation Results

This section discusses the digital simulation results based on MATLAB/ Simulink. Different conditions are simulated to verify the performance of proposed simplified QVI approach. The simulation results are given in the Figure 3.6 – Figure 3.8.

3.4.1 Voltage Sag Compensation under Sinusoidal Voltages and Linear Load

Initially, the performance of UPQC-Q based on QVI under the assumption of ideal mains voltage condition is evaluated. The load on the system is considered as linear R-L load with lagging power factor of 0.56. The simulated results are shown in Figure 3.6. At time t1, the shunt inverter is put into operation. After maintaining the DC link voltage at a set reference value (Figure 3.6 (d)), it starts compensating the reactive power demanded by the load by injecting quadrature leading current (Figure 3.6 (g)). At time t2, series inverter is put into operation such that both the shunt and series inverters now functions as UPQC. At time t3, a sag (20%) condition is imposed on the network. The series inverter starts injecting the required quadrature voltage. The slow response in injected series voltage (Figure 3.6 (c)) is due to the one cycle delay in the calculation of *rms* value of reduced input voltage. The resultant load voltage profile (Figure 3.6 (b)) shows that the UPQC-Q maintains it at a desired level with the proposed QVI approach.

As discussed in the theory (from (3.5)), the QVI results in power angle δ of 36^0 between the resultant load voltage and source voltage. This causes the effective phase angle β of 20^0 between source voltage and the load current instead of 56^0 at steady state. In other words, the reactive power demanded by the load as seen from the source side gets reduced. The certain amount of load reactive power demand is now supplied by series inverter, reducing the reactive power burden on the shunt part. This can be noticed from Figure 3.6 (g), where, the shunt inverter injected current magnitude gets reduced after time t3. Thus, the load reactive power demand is shared by both the shunt and series inverters, which depends on the % of sag on the system. The source current magnitude (from (3.13)) increases in order to maintain the power balance in the network (Figure 3.6 (f)).

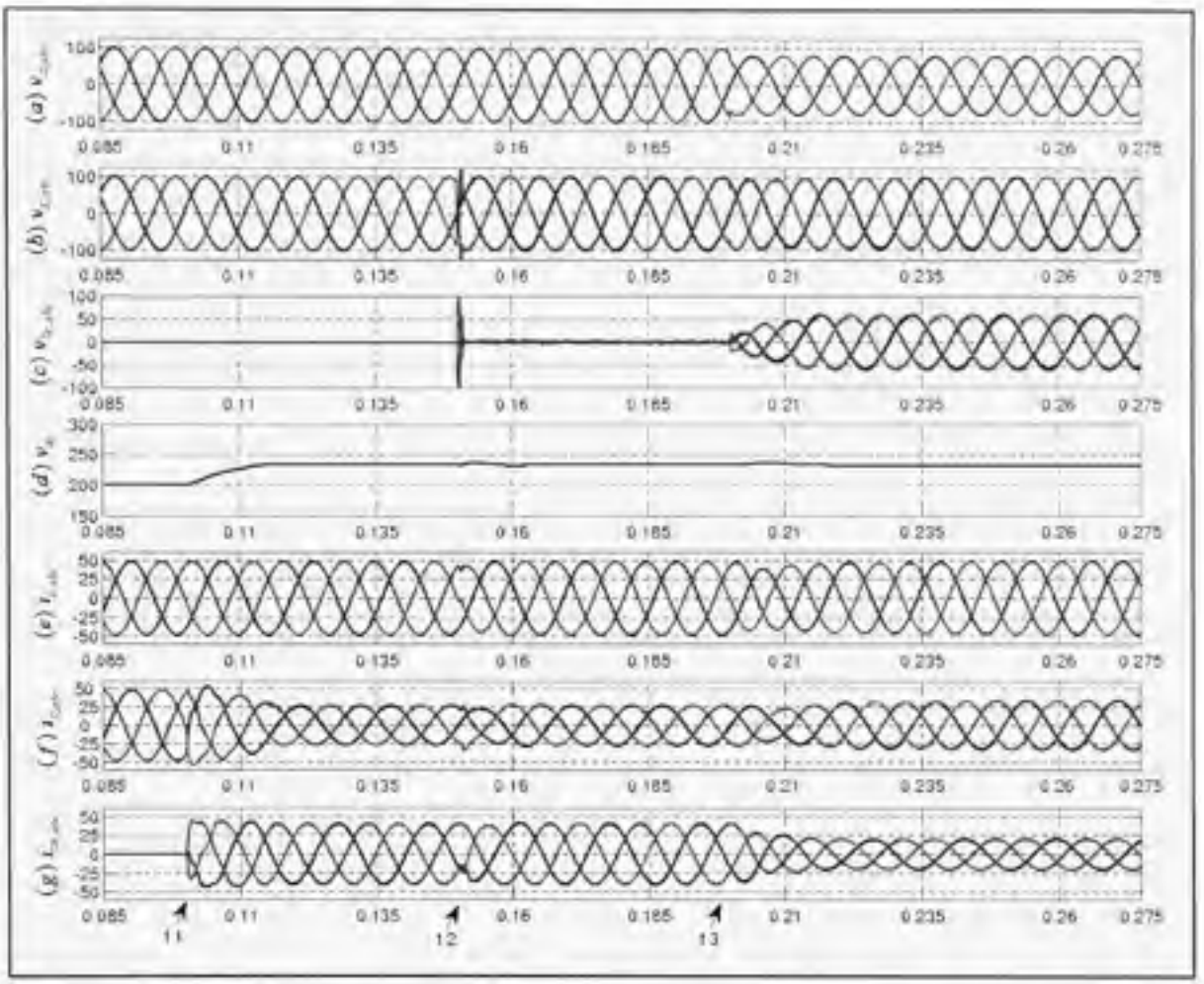


Figure 3.6 Simulation results: voltage sag compensation by QVI under sinusoidal source voltages.

3.4.2 Voltage Sag Compensation under Distorted Condition

The performance of UPQC under the condition of distorted load current and distorted source voltage with QVI approach is evaluated here. The distorted supply voltage shown in Figure 3.7 (a) has THD of 15%. The load is considered as a combination of R-L load and a diode bridge rectifier followed by R-L load. The distorted load current is shown in Figure 3.7 (e). has THD of 16%. At time t1, the shunt inverter starts compensating the load current harmonics and reactive power demand, making source current in-phase with source voltage (Figure 3.7 (f)). At time t2, the series inverter starts compensating the voltage harmonics present in the supply, by injecting the required voltages as extracted using *d-q*

transformation. Thus distortion present in the source voltages are isolated by UPQC and does not appear on the load terminals. The load voltage has THD of 2%.

During the condition of voltage harmonics and voltage sag (20%), after time t3, the series inverter injects appropriate voltage to maintain the load voltage at a desired constant level and free from distortion (Figure 3.7 (b)). The series injected voltage (Figure 3.7 (c)) is the summation of harmonic contents in source and the required quadrature voltage to compensate the 20% of sag.

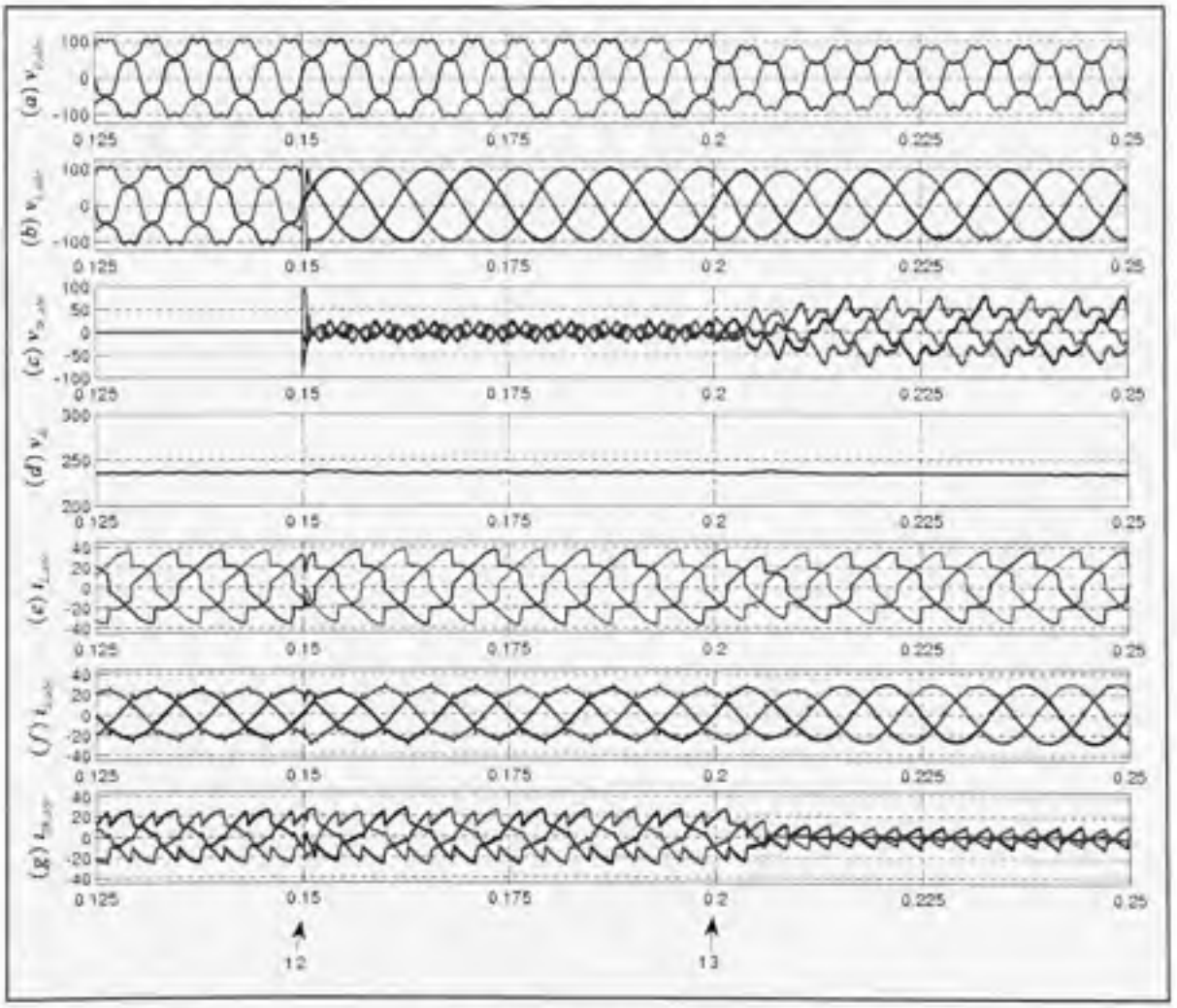


Figure 3.7 Simulation results: Voltage sag compensation by QVI under distorted condition.

3.4.3 Critical Operating Condition

When δ becomes equal to φ_L, critical operating condition occurs. The simulation results for such condition are shown in Figure 3.8. To demonstrate the operating of UPQC-Q under critical condition, the load on the system is considered in such ways that for 20% of sag, δ will become φ_L. When UPQC starts (after time t3) compensating the voltage sag (20%) by injecting quadrature voltage, the phase angle difference between resultant load voltage and source voltage becomes exactly equal to the load power factor angle. Thus the load seen from the source side appears as a pure resistive with no VAR requirement with respective to the source. Therefore, shunt inverter does not inject any compensating current (Figure 3.8 (c)). Due to this, both the source current and the load current magnitudes become the same, which can be noticed from Figure 3.8 (a) and (b), respectively.

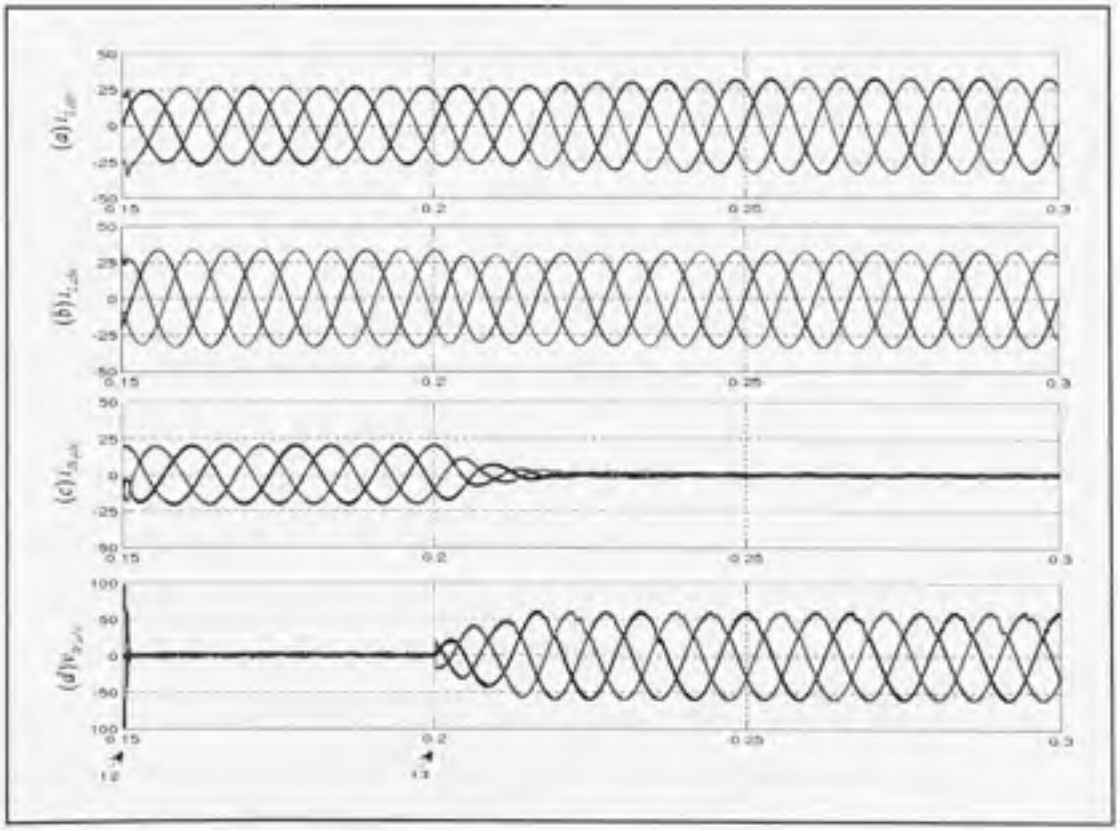


Figure 3.8 Simulation results: critical operating condition ($\delta=\varphi_L$)

3.5 Laboratory Experimental Results

The performance of UPQC-Q with proposed simplified approach to extract the necessary quadrature injection voltage is also supported through laboratory experimental study. Physically, the system configuration of UPQC-Q is exactly similar to the one already discussed in CHAPTER 2. The only difference is in the control of series inverter that gives the name UPQC-Q to basic UPQC. In the following subsections, the real-time QVI extraction, and the experimental results for single-phase as well as three-phase UPQC-Q are discussed.

3.5.1 Real-Time Quadrature Injection Voltage Extraction

In this section, the scheme used to extract the necessary quadrature voltage to compensate the sag on the system, in real-time, is explained briefly. Figure 3.9 shows the Simulink model built for experimental validation of proposed single-phase QVI approach.

The actual source voltage is sensed and its fundamental *rms* value is continuously computed using a "*discrete rms value*" block from MATLAB/ Simulink. The computed *rms* value is then divided by the desired load voltage magnitude to calculate the term "cosδ". Taking the inverse of cosδ, the power angle δ is extracted. There are two possible modes of operation – *i*) cosδ = 1, represents the system is in steady-state, and *ii*) cosδ < 1, represents the sag on the system. Thus, the inverse operation of cosδ to determine the angle δ can have two distinguished values, *i*) δ = 0, for the condition cosδ = 1, and *ii*) δ > 0, for cosδ < 1. When the system is in steady-state, δ = 0 and thus the $V_{sr} = 0$. On the other hand, when the system voltage falls below the rated value during the sag on the system the term δ gives the necessary power angle. For any increase in the source voltage due to the swell on the system, the inverse of cosδ using Simulink "*acos*" (represents *cos* inverse) block gives zero output. In this way, the simple approach automatically takes care of all the possible conditions on the network and the user does not need to pay any special attention to determine the sag on the system. Figure 3.10 shows the experimental result to demonstrate the real-time extraction of the required quadrature injection voltage.

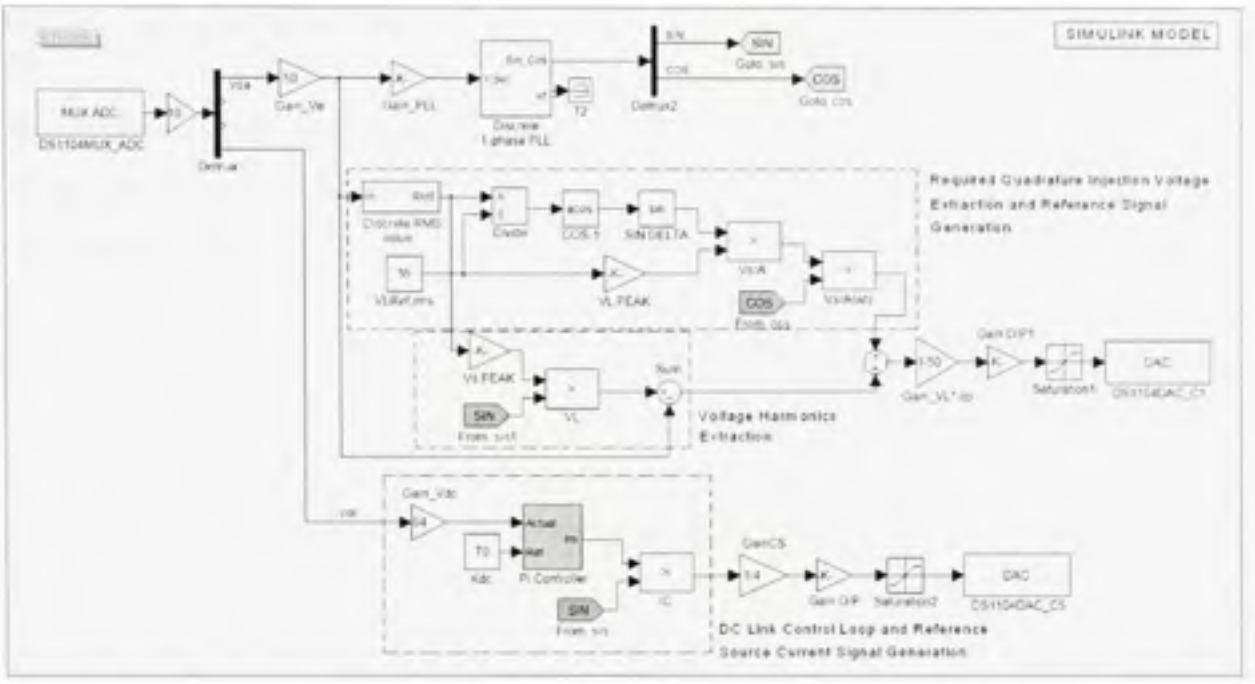


Figure 3.9 Developed Simulink model to extract the quadrature injection voltage in real-time. Figure also shows the reference signal generation for series and shunt inverters.

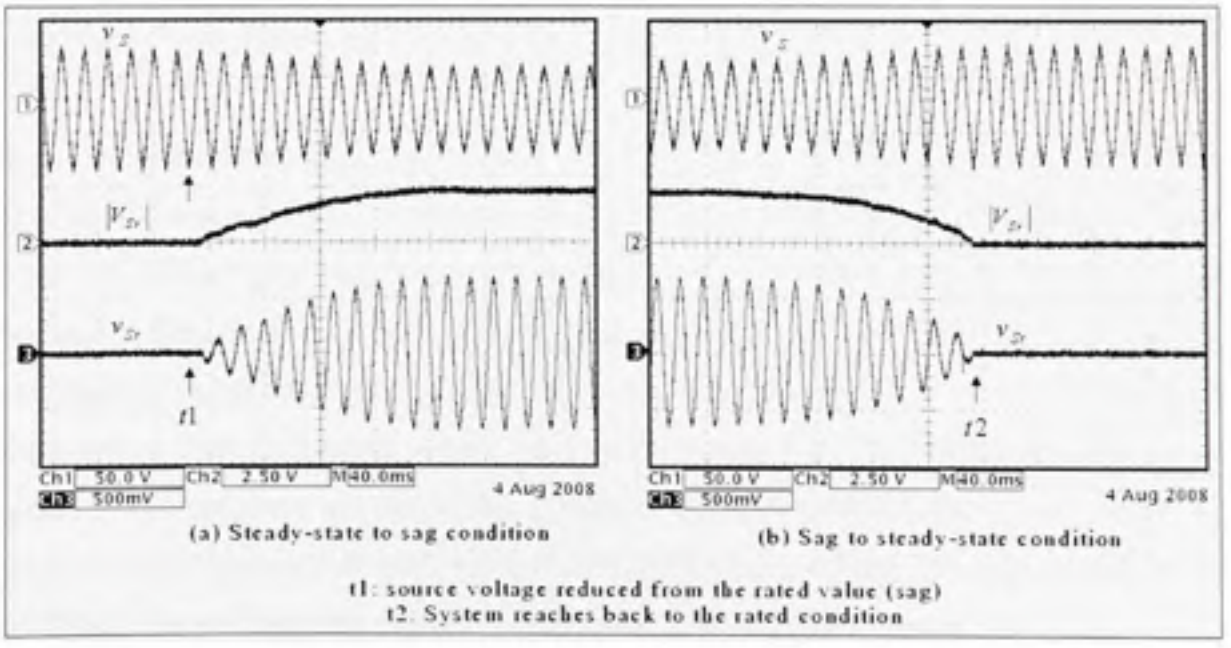


Figure 3.10 Real-time extraction of required quadrature injection voltage.

3.5.2 Single-Phase UPQC-Q System Performance

The performance of single-phase UPQC-Q system is discussed in detail, since it is easy to tackle one phase instead of three phases. The experimental results under different working conditions are given in Figure 3.11 - Figure 3.15.

3.5.2.1 Voltage Sag Compensation under Sinusoidal Condition

The source voltage is considered as sinusoidal with a linear RL load on the system. The RL load draws a lagging current with power factor of 0.59. The desired load voltage is considered as 35V *rms*. A sag of 15% (appx.) is imposed on the system. Figure 3.11 shows the experimental results during the given operating condition. The profile of reduced source voltage can be noticed from trace-1 (Figure 3.11 (a)), whereas, the resultant load voltage profile in trace-2 shows that the UPQC compensates the sag on the system effectively. The voltage injected by series inverter is shown in trace-3, whereas, the source current is shown in trace-4. A closer look at trace-1 and trace-4 suggest that the shunt inverter maintains unity power factor operation under the voltage sag condition.

The enlarged profiles of the source, load and the series injected voltages are given in Figure 3.11 (b). The source voltage, at trigger point "T" in the figure, is at zero-crossing. It is clearly evident from the figure that the injected voltage is approximately at quadrature (89° lead) to the source voltage, and therefore, in quadrature with source current (UPQC-Q maintains unity power factor operation). Thus, it proves that the voltage sag on the system get compensated through reactive power. To compensate sag of 15% (@ 35V) the series inverter injects 17V quadrature voltage which is almost 52% of the rated value. The phase angle boost between the resultant load voltage and actual source voltage can also be noticed from the figure. The performance of both the inverters is plotted in the Figure 3.11 (c).

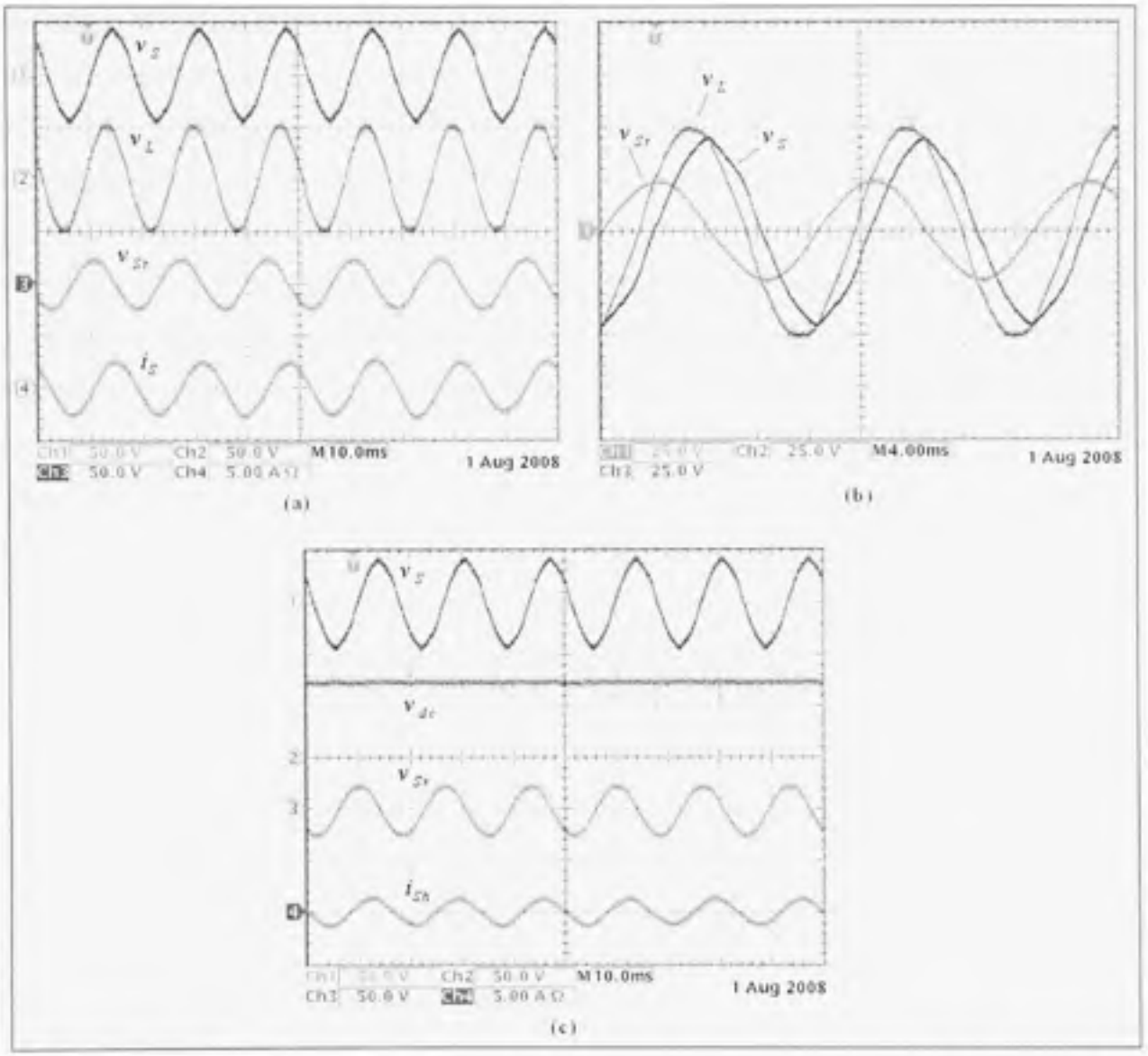


Figure 3.11 Experimental results: voltage sag compensation by QVI under sinusoidal condition (single-phase system).

During steady-state condition, the phase angle between the source and load voltage is zero. The load current is 0.59 lagging (φ_L=55°) to the load voltage under this condition. The relative phase angles between different voltages and currents during QVI of UPQC-Q are demonstrated in Figure 3.12. For better understanding, the phasor diagram is also plotted in Figure 3.12. To compensate the sag on the system the series inverter injects the quadrature voltage. In this experimental study the phase angle (φ_{Sr}) is found as 89° (very close to 90°). The series injected voltage together with the source voltage gives the desired load voltage

magnitude. The generated phase angle boost between the source voltage and the resultant load voltage can be noticed from trace-1 and trace-3 (Figure 3.12). This phase angle boost (δ) is found as 31^o. However, the QVI operation does not change the phase angle, 55^o, between the resultant load voltage and load current (since load is assumed as constant during voltage sag condition), as noticed from trace-3 and trace-4. It is essential to point out here that when the system is working at steady state condition, the phase angle (55^o) between the source voltage and the load current is also the same as between load voltage and load current. Interestingly, under QVI operation of UPQC-Q, the phase angle between the source voltage and the load current now improves from 55^o to 24^o (β), which can be seen from trace-1 and trace-4. In other words, the reactive power required by the load, as seen from the source side, reduces, and thus the QVI approach during voltage sag condition also supports a certain amount of load reactive power.

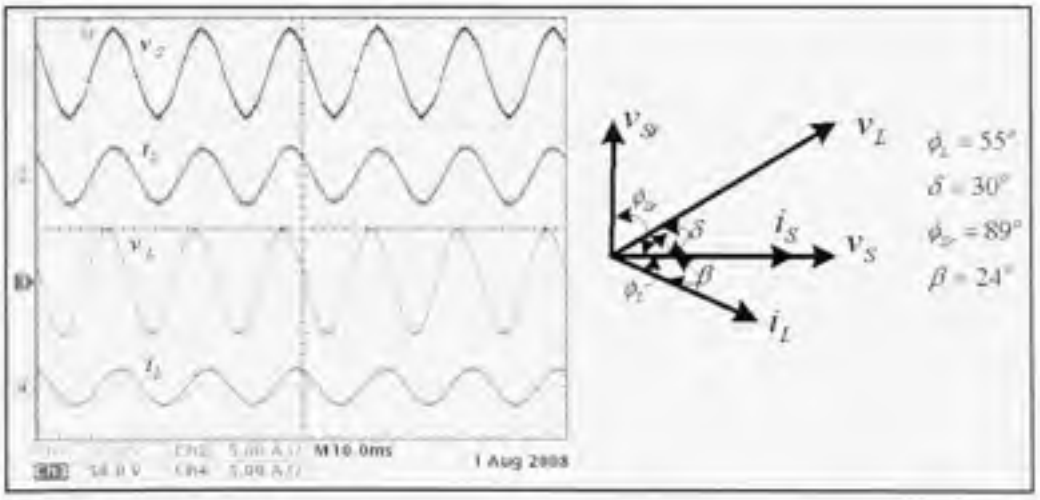


Figure 3.12 Experimental results: phase relationships between different parameters during voltage sag compensation using QVI.

3.5.2.2 Voltage Sag Compensation under Distorted Condition

In this section, the performance of UPQC-Q to compensate voltage harmonics and sag along with current harmonics, simultaneously, is tested. Figure 3.13 shows the experimental results where source voltage and load current are distorted. The source voltage has THD of 20.24% with the load current THD of 29.62%. When UPQC is turned ON, the series inverter injects

the appropriate voltage to cancel out the unwanted harmonics component present in the source voltage. The improved load voltage profile can be noticed from trace-2 (Figure 3.13 (b)). As discussed in the previous chapter, when the UPQC is in operation, the improvement in source current profile also improves the source voltage profile. The load voltage and source voltage THDs, when UPQC is ON, are found as 3.8% and 5.04%, respectively, with the source current THD of 2.72%. The profiles of series inverter injected voltage and shunt inverter compensating current along with the self supporting DC bus voltage are given in Figure 3.13 (c).

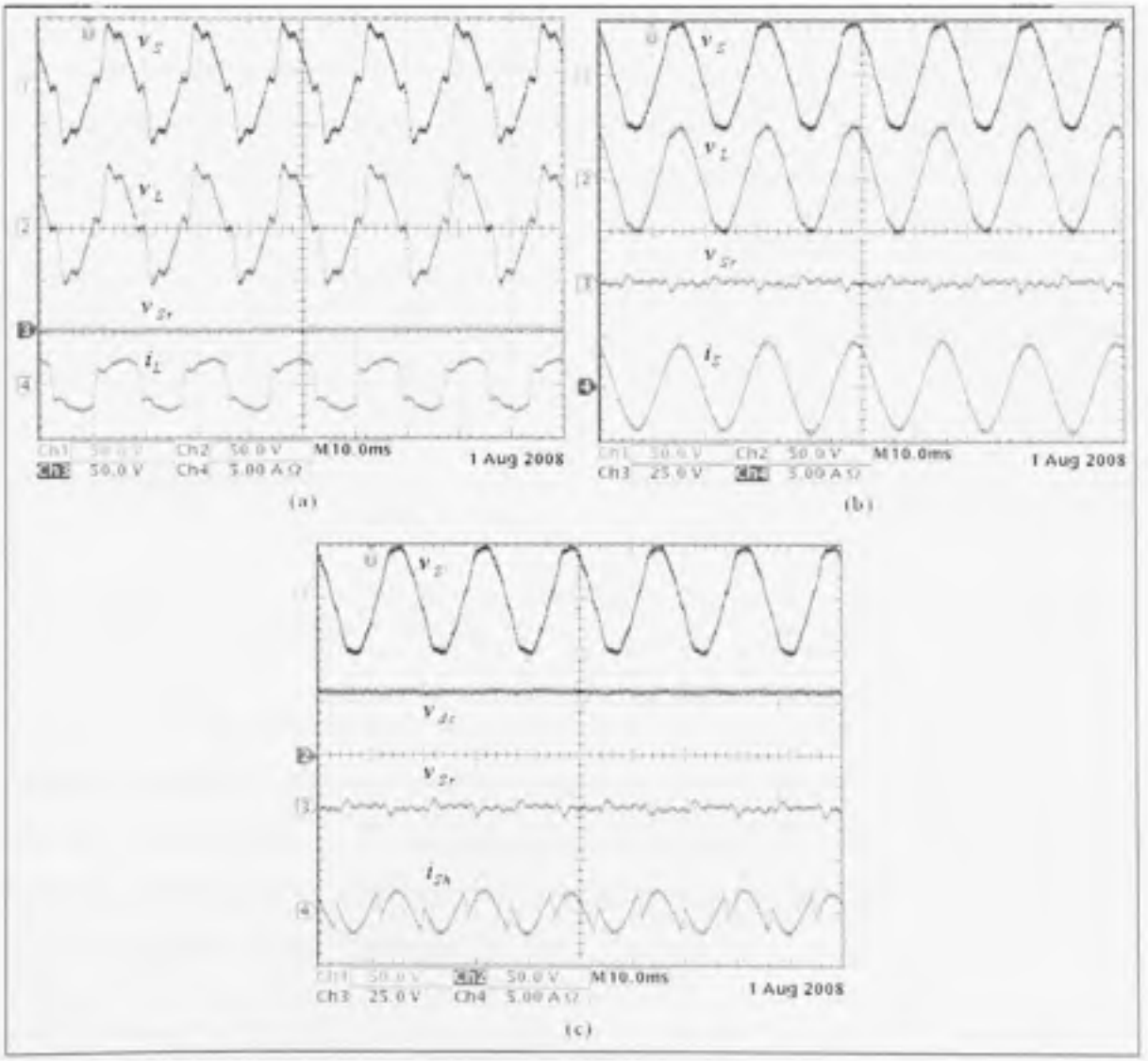


Figure 3.13 Experimental results: UPQC-Q voltage and current harmonic compensation.

The experimental results during the voltage sag under distorted source voltage condition are given in Figure 3.14. As noticed from trace- 3, the series inverter now injects a voltage which is the summation of quadrature voltage as determined by QVI approach and voltage harmonics present in the source side. Thus the UPQC-Q with the proposed QVI approach effectively compensates the voltage sag, voltage harmonics and current harmonics, all at the same time.

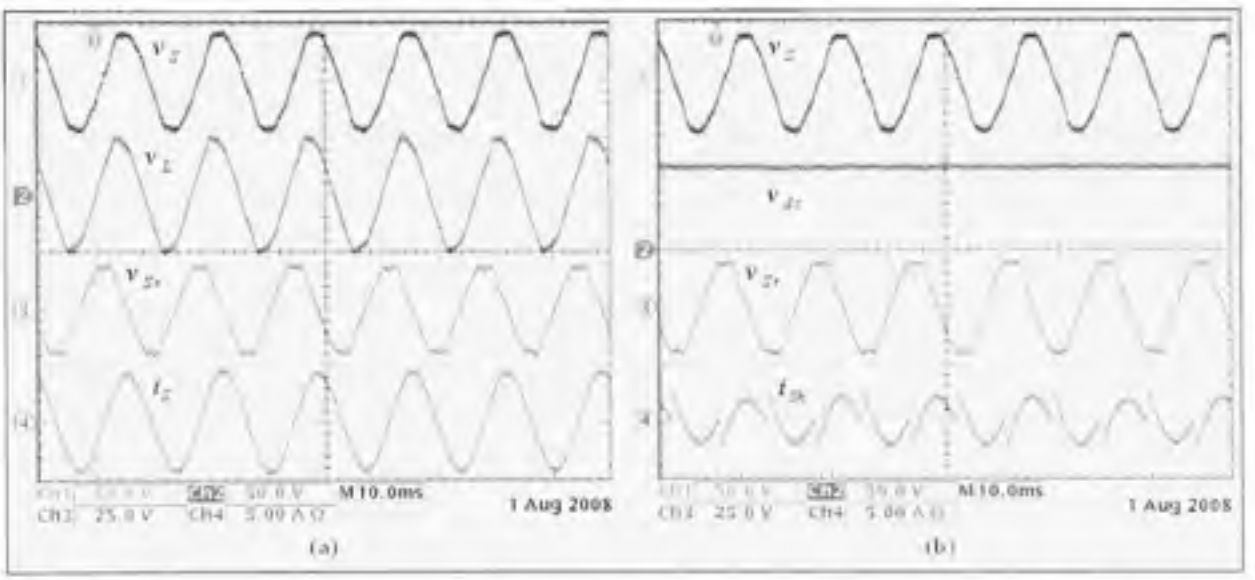


Figure 3.14 Experimental results: performance of QVI to compensate voltage sag and voltage harmonics simultaneously.

3.5.2.3 UPQC-Q Dynamic Performance

In this section the dynamic performance of UPQC-Q is demonstrated. Initially, the UPQC is ON compensating the voltage and current harmonics. All of a sudden, a voltage sag condition is imposed on the system. In the laboratory, to create such a situation, the supply voltage is reduced by reducing the output of the autotransformer, and therefore, there is a slow reduction in supply voltage magnitude.

The experimental results during such transient condition are given in Figure 3.15. As noticed from Figure 3.15 (a), the QVI approach detects the sag on the system and starts injecting the required quadrature injection voltage in addition to the voltage harmonics component. The

effect of the sudden occurrence of sag does not appear across the load side. Thus UPQC-Q effectively maintains the load voltage at the desired level. Increased in the source current magnitude can also be noticed from the figure. The injected series voltage and shunt current envelops along with a self supporting DC bus voltage, which are given in Figure 3.15 (b). An important observation during voltage sag compensation using QVI approach is that the DC bus voltage during the transient condition remains unaffected.

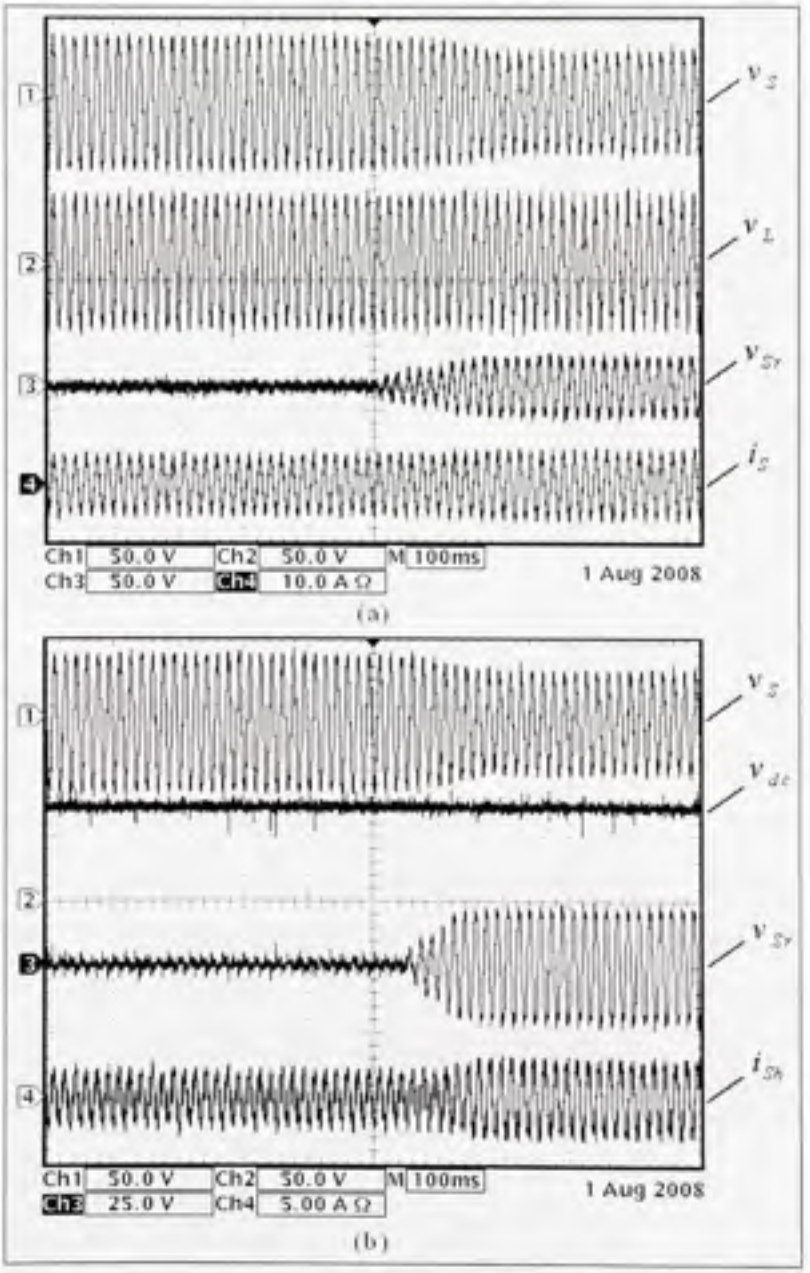


Figure 3.15 Experimental results: Dynamic performance of UPQC-Q.

3.5.3 Three-Phase UPQC-Q System Performance

In this section, the performance of three-phase UPQC-Q is discussed. The three-phase UPQC system implementation involves total 19 signals to be monitored, which is a cumbersome task. These signals include 10 voltages, such as, three source voltages, three series injected voltages, three load voltages, and the DC link voltage, and 9 currents, such as, three load currents, three source current and three shunt injected currents. Therefore, it is often difficult to monitor all the quantities at the same time. The variation in parameter values, for example, the same rating capacitors from one manufacturer shows little or sometimes significant deviation in their values when measured.

The series inverter is more susceptible to parameter variation than the shunt as a LC filter is essential at the series inverter side, in order to generate proper output voltage from the inverter. Moreover, the sensing circuits used to sense different currents and voltages also show some deviation in their output values. While doing experimental validation of controllers, especially, for three-phase UPQC system, we came across some of the above mentioned difficulties. However, the basic aim to carry out the experimental investigation is to validate the effectiveness of the developed controllers for real-time applications.

3.5.3.1 Three-Phase Voltage Sag Compensation using QVI

In this section, the experimental validation for three-phase UPQC-Q system, for voltage sag compensation, is carried out. The experimental results on the performance of proposed QVI approach for single-phase system have already been discussed in detail. Therefore, here the results are briefly discussed. Figure 3.16 (a) shows the profile of source voltages under steady state condition. As noticed, these voltages are slightly unbalanced and distorted. The load on the system is considered as non-linear and the current profiles are shown in Figure 3.16 (b).

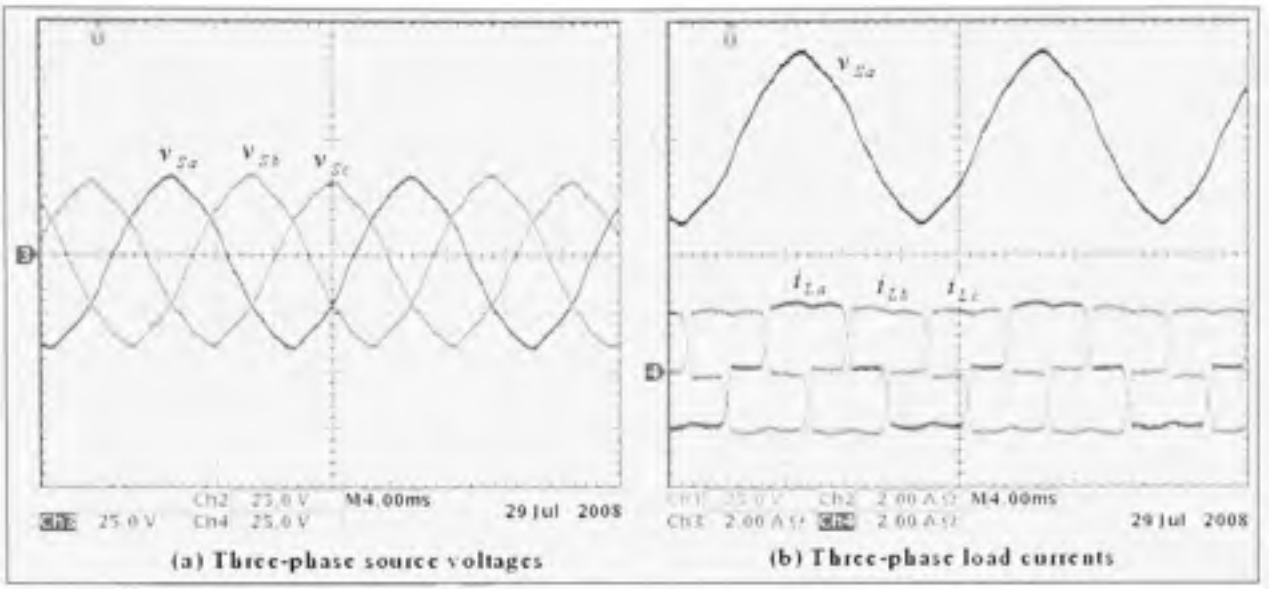


Figure 3.16 Experimental results: Three-phase steady state source voltages and load currents.

The experimental results during the voltage sag on the three-phase system are shown in Figure 3.17 – Figure 3.18. As discussed, in order to compensate the sag on the system, the UPQC-Q injects the required quadrature voltages in each of the phases. The performance of each individual phase is shown in Figure 3.17. The voltages injected by series inverters are slightly distorted partly due to the parameter mismatch of LC filter. It is also found that the performance of phase-*c* was not up to the mark. However, these experimental results validate the effectiveness of the proposed QVI approach for UPQC-Q.

Figure 3.18 shows the performance of both the inverters and the compensated source currents during voltage sag compensation mode of operation. The profile of three-phase quadrature injected voltages by series inverter is shown in Figure 3.18 (a), whereas, three-phase shunt injected current profiles are given in Figure 3.18 (b). The sinusoidal source currents maintained by shunt inverter are shown in Figure 3.18 (c).

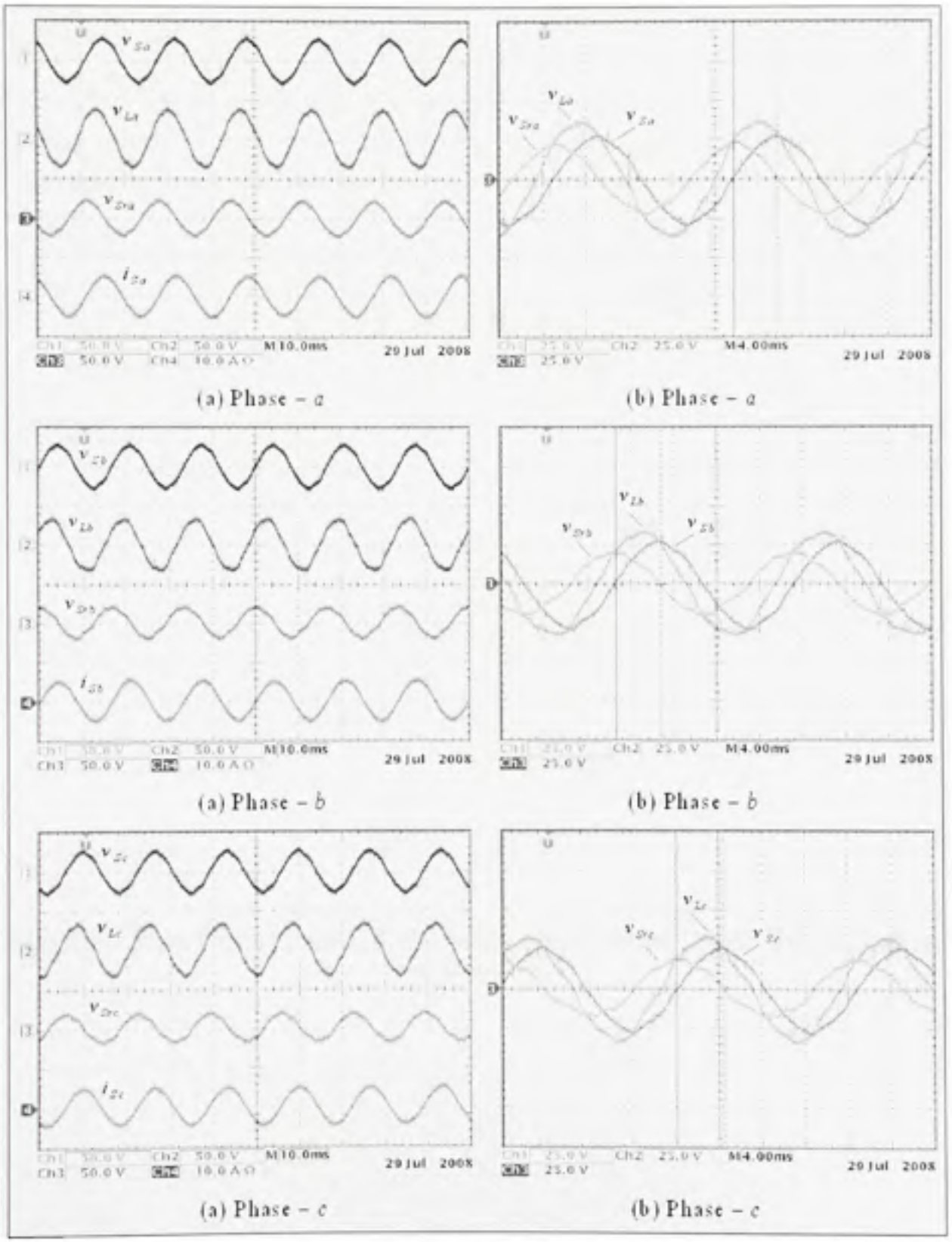


Figure 3.17 Experimental results: Individual phase performance during voltage sag compensation.

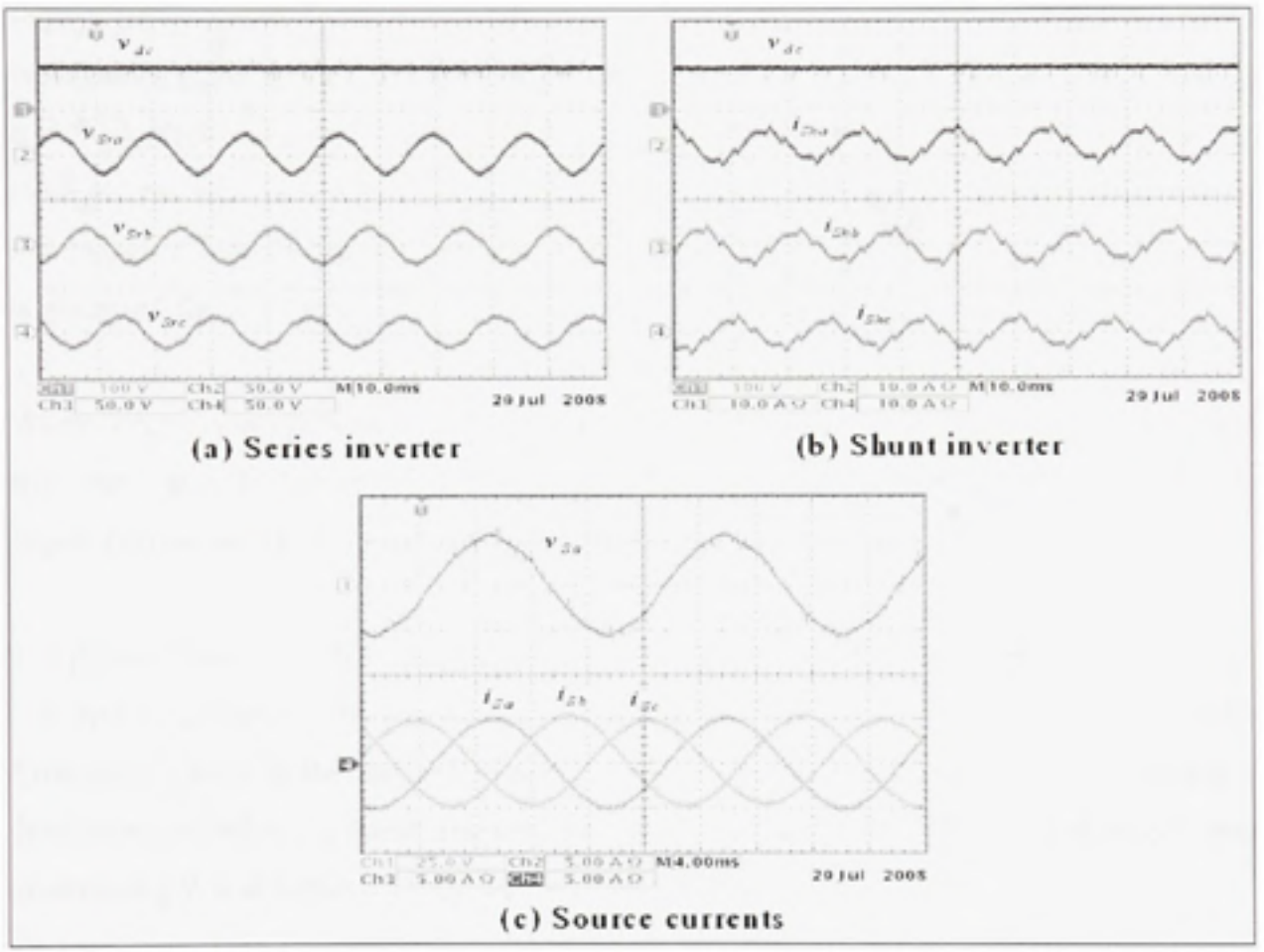


Figure 3.18 Experimental results: Performance of three-phase UPQC-Q during voltage sag condition.

3.5.3.2 Voltage Harmonics Compensation using *d-q* Transformation

The performance of UPQC to compensate the harmonics present in three-phase source voltages is discussed in this section. The voltage harmonics present in the source voltages are estimated using *d-q* transformation method. The load on the system is also considered as non-linear. The distorted supply voltage profile is shown in Figure 3.19 (a). These source voltages are also unbalanced in nature due to unequal impedance values of inserted line resistances to generate harmonics voltage drop across them. The distorted load current profile is given in Figure 3.19 (b).

When UPQC is in operation, the load voltage profile is given in Figure 3.19 (c). As noticed from the figure, the harmonics present in the source voltages are reduced at the load side. The source current profile is shown in Figure 3.19 (d).

The performance of each of the phases are given in Figure 3.20 (a), (b), and (c) for phase – *a*, – *b*, and – *c*, respectively. As noticed from the figures, in order to compensate the voltage harmonics present in the source voltages, the series inverter injects the necessary voltages as determined utilizing *d-q* transformation. The performance of UPQC series inverter and shunt inverter is given in Figure 3.20 (d) and (e), respectively.

The THD values of each of the source and load voltages and respective harmonics spectrums are plotted in Figure 3.21, whereas, Table 3.1 gives the detailed value of individual voltage harmonic as % of fundamental component. The current harmonics generated by non-linear load together with the source current harmonics spectrums after the compensation is plotted in Figure 3.22. The individual current harmonic values can be noted from Table 3.2.

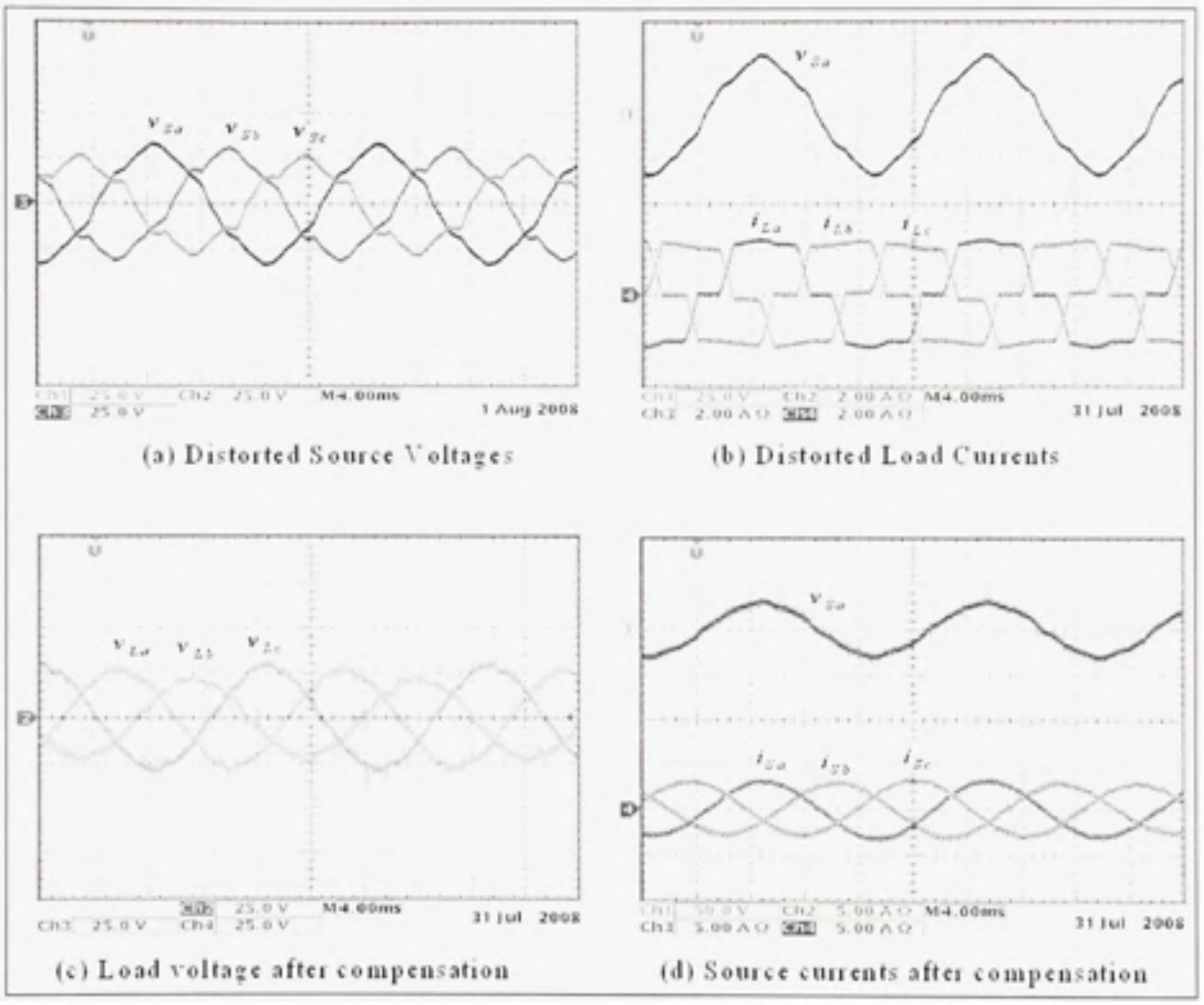


Figure 3.19 Experimental results: voltage and current harmonics compensation performance of three-phase UPQC.

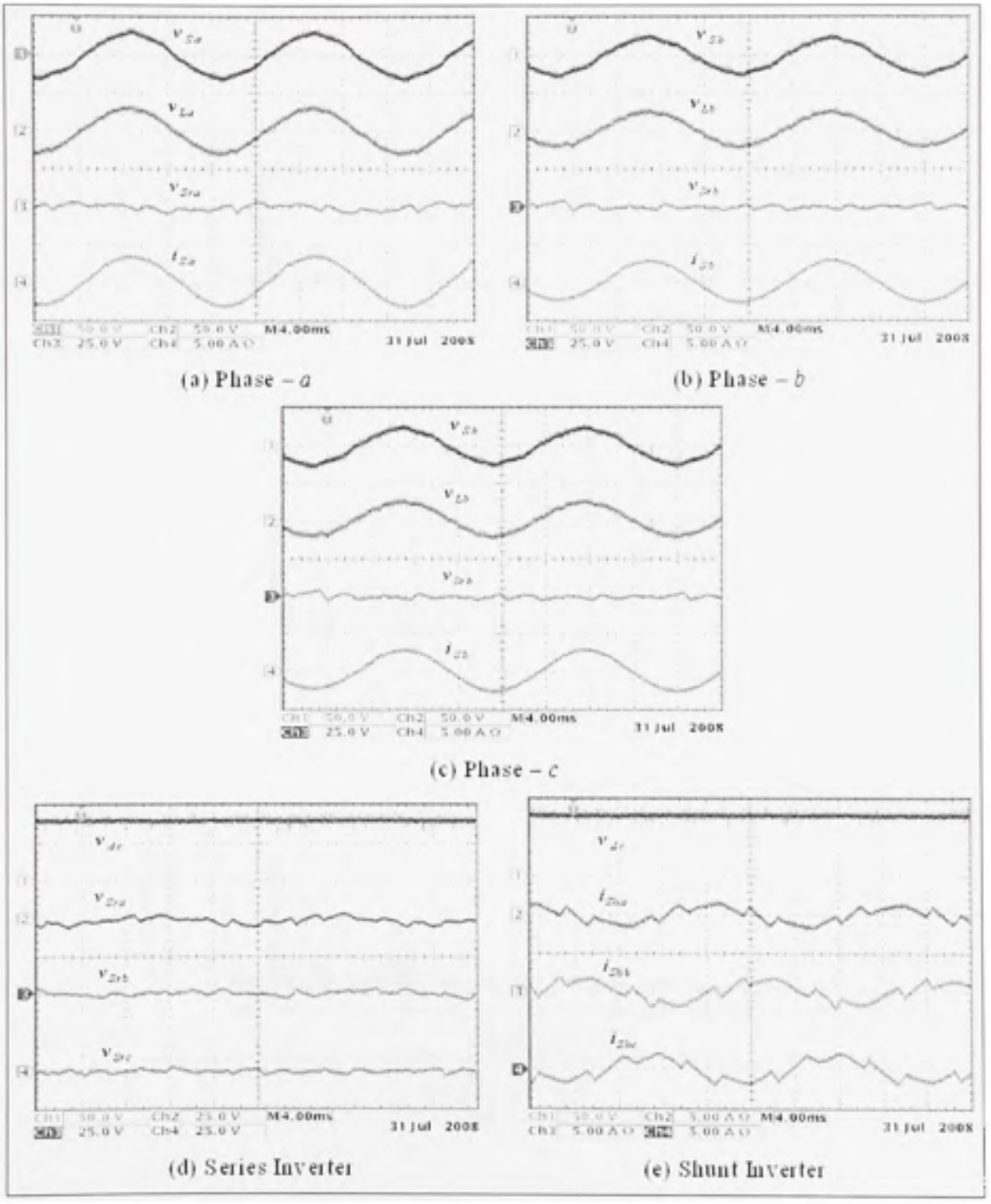


Figure 3.20 Experimental results: voltage and current harmonics compensation performance of three-phase UPQC

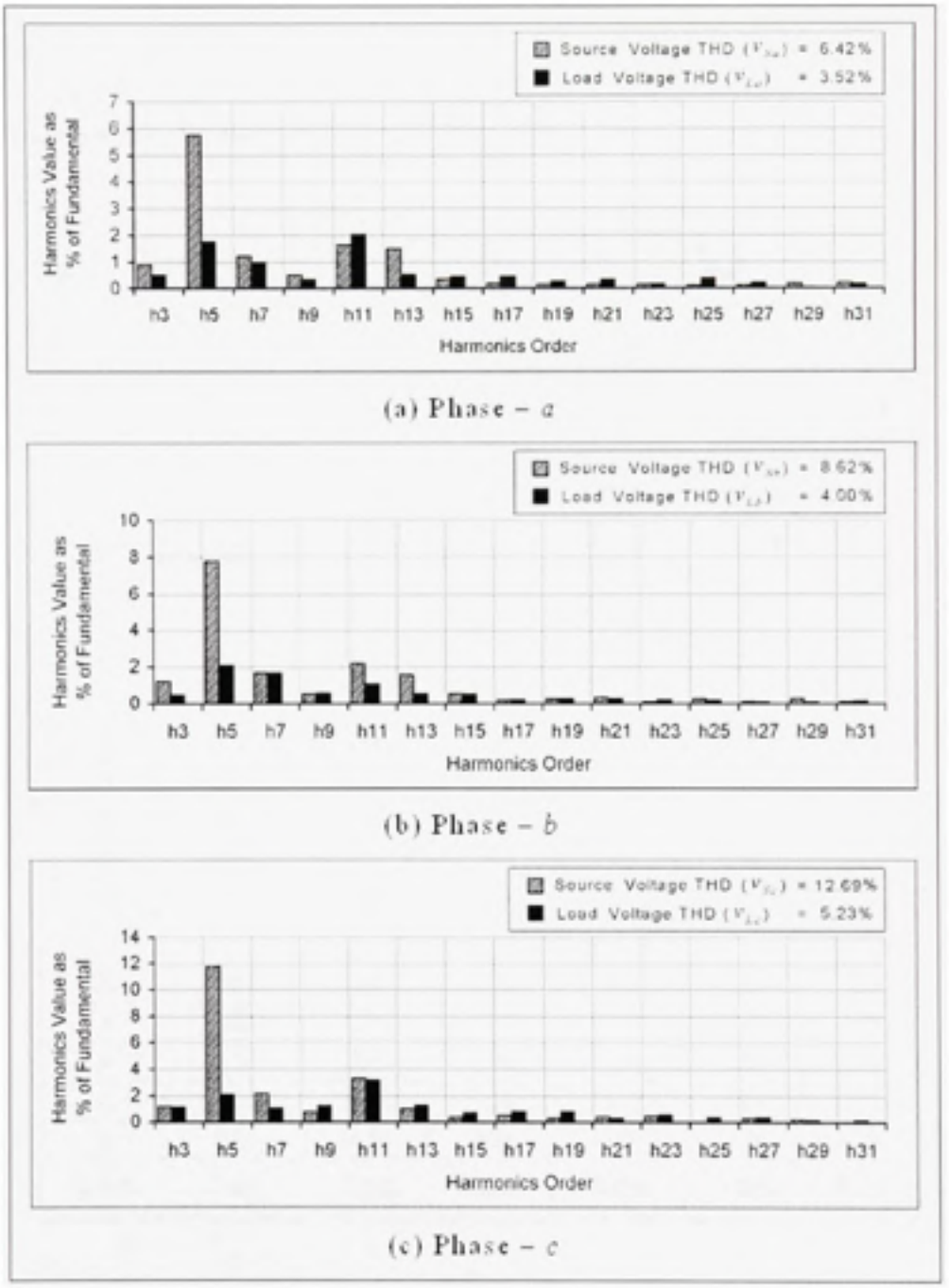


Figure 3.21 Voltage harmonics compensation - harmonics spectrum of load voltages after compensation.

Table 3.1
Voltage harmonics compensation - Individual harmonics values as % of fundamental

Harmonics	V_{Sa}	V_{Sb}	V_{Sc}	V_{La}	V_{Lb}	V_{Lc}
Odd Harmonics (%)						
3	0.89	1.22	1.16	0.50	0.45	1.11
5	5.74	7.80	11.77	1.76	2.09	2.07
7	1.20	1.68	2.15	0.95	1.68	1.06
9	0.50	0.50	0.77	0.34	0.57	1.21
11	1.63	2.18	3.31	2.02	1.06	3.13
13	1.49	1.57	0.99	0.53	0.53	1.26
15	0.35	0.53	0.34	0.46	0.49	0.71
17	0.18	0.19	0.52	0.46	0.20	0.81
19	0.14	0.23	0.30	0.27	0.25	0.81
21	0.14	0.31	0.43	0.31	0.25	0.30
23	0.14	0.08	0.47	0.15	0.20	0.56
25	0.11	0.23	0.04	0.38	0.16	0.35
27	0.11	0.11	0.30	0.19	0.04	0.35
29	0.18	0.27	0.21	0.04	0.04	0.15
31	0.21	0.11	0.04	0.15	0.12	0.15
Even Harmonics (%)						
DC	0.85	0.84	0.17	0.57	0.16	4.09
2	0.25	0.65	0.30	1.07	2.09	1.41
4	0.28	0.38	0.34	0.65	0.90	0.40
8	0.18	0.19	0.26	0.57	0.61	0.71
10	0.21	0.08	0.26	0.38	0.16	0.96
% THD	**6.42%**	**8.63%**	**12.69%**	**3.52%**	**4.00%**	**5.23%**

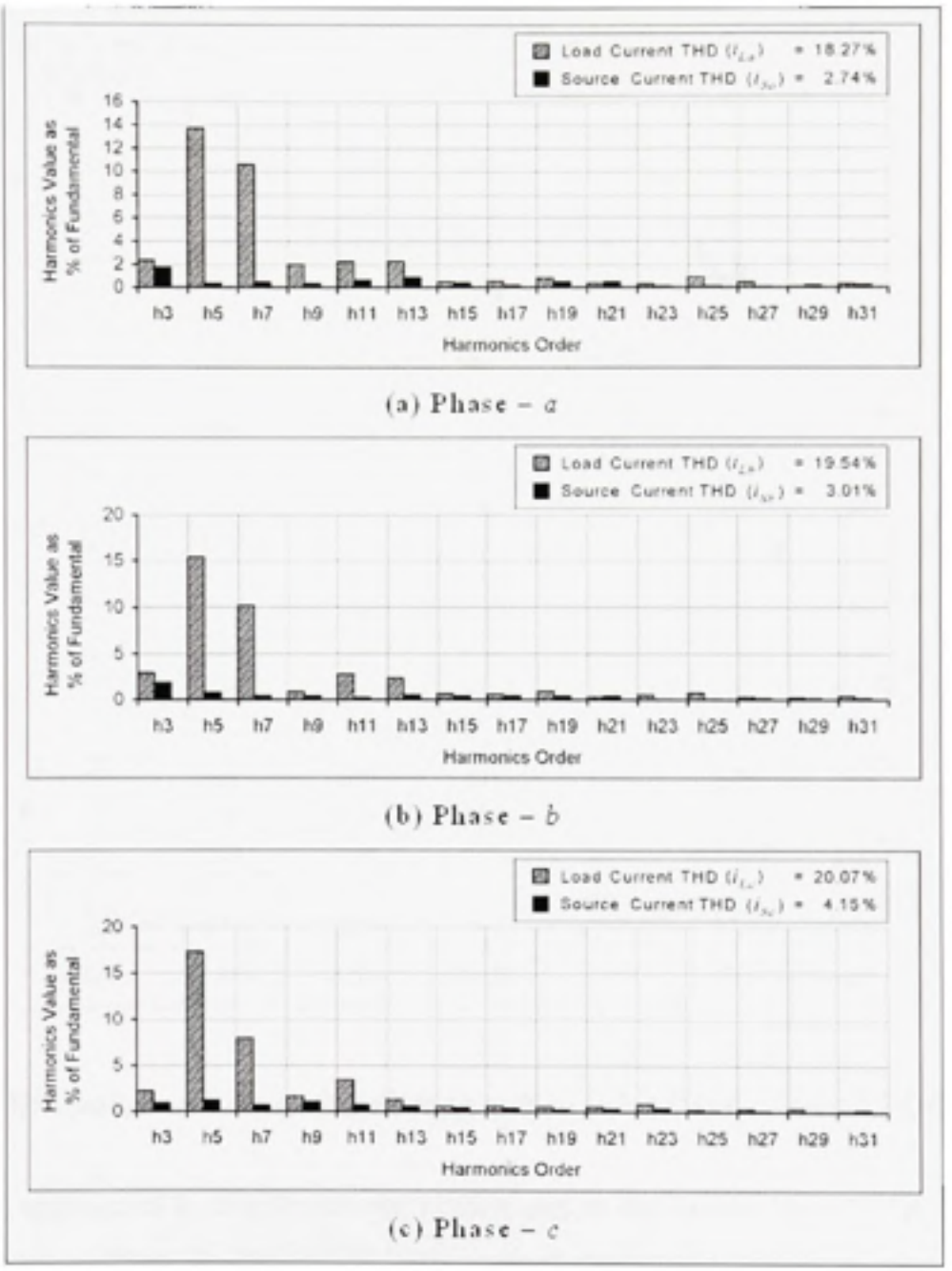


Figure 3.22 Current harmonics compensation - harmonics spectrum of source currents after compensation.

Table 3.2
Current harmonics compensation - Individual harmonics values as % of fundamental

Harmonics	i_{La}	i_{Lb}	i_{Lc}	i_{Sa}	i_{Sb}	i_{Sc}
Odd Harmonics (%)						
3	2.32	2.9	2.17	1.77	1.84	0.96
5	13.7	15.39	17.3	0.37	0.81	1.27
7	10.56	10.19	7.95	0.42	0.47	0.71
9	1.96	0.84	1.67	0.37	0.39	1.10
11	2.18	2.75	3.42	0.65	0.19	0.73
13	2.25	2.35	1.29	0.84	0.50	0.59
15	0.46	0.66	0.53	0.39	0.39	0.45
17	0.50	0.59	0.61	0.17	0.47	0.42
19	0.78	0.95	0.53	0.48	0.42	0.25
21	0.36	0.29	0.53	0.45	0.39	0.28
23	0.29	0.51	0.87	0.11	0.06	0.37
25	0.86	0.70	0.27	0.11	0.11	0.11
27	0.43	0.29	0.30	0.06	0.14	0.08
29	0.07	0.22	0.34	0.14	0.17	0.06
31	0.29	0.4	0.08	0.23	0.17	0.20
Even Harmonics (%)						
DC	1.21	0.33	1.10	1.35	1.34	0.68
2	1.36	0.51	0.34	1.01	1.62	2.79
4	0.07	0.44	0.27	0.34	0.14	1.21
8	0.14	0.70	0.61	0.31	0.28	0.90
10	0.14	0.59	0.23	0.34	0.33	0.51
% THD	**18.27%**	**19.54%**	**20.07%**	**2.74%**	**3.01%**	**4.15%**

3.6 Discussion on Voltage Sag Compensation Using UPQC-P and UPQC-Q

So far, two approaches to compensate the voltage sag on the system using UPQC have been described and validated. In CHAPTER 2, the voltage sag is tackled by supporting the active power, such that, the voltage at load bus remains constant irrespective of supply voltage variation. Under such a condition, since UPQC provides the active power, it is termed as UPQC-P. In this chapter, instead of active, the reactive power is used to overcome the sag on the system. As the sag is compensated through reactive power, the UPQC is termed as

UPQC-Q. Some of the important advantages and limitations of these approaches are highlighted.

UPQC-P: Voltage sag compensation using ***Active Power***

UPQC-Q: Voltage sag compensation using ***Reactive Power***

- Both the approaches compensate the voltage sag effectively and thus maintain the load voltage at constant level.

- In UPQC-P, during the sag on the system, an in-phase voltage equals to the difference between actual source voltage and the reference load voltage injected through the series inverter, whereas, in UPQC-Q, a quadrature voltage is injected such that vector sum of the reduced source and injected voltages equals the desired load voltage magnitude. Figure 3.23 shows the phasor representation of both the approaches. It is obvious from the phasors that to compensate the sag on the system, UPQC-P requires the minimum possible voltage, whereas, the UPQC-Q uses the maximum possible voltage. The injected voltage magnitude is a significant component to determine the series inverter ratings.

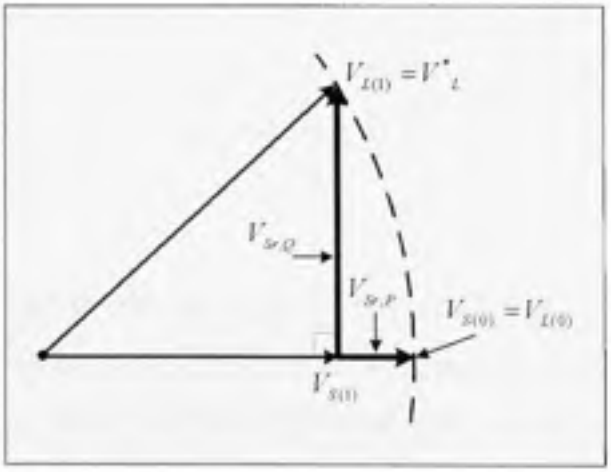


Figure 3.23 Phasor representation of UPQC-P and UPQC-Q.

The voltage necessary to be injected by both the approaches can be given as:

For UPQC-P:

$$V_{SrP} = V^*_L - V_S \tag{3.29}$$

For UPQC-Q:

$$V_{SrQ} = \sqrt{(V^*_L)^2 - (V_S)^2} \tag{3.30}$$

- Assuming, the load voltage magnitude to be maintained at 1 *p. u.* and the source voltage is reduced to 0.8 *p. u.* due to the sag on the system. Using (4.30) and (4.31), the UPQC-P should inject 0.2 *p. u.* voltage, while the UPQC-Q should inject 0.6 *p. u.* voltage. At this point anyone would prefer to opt for UPQC-P, since the required series inverter rating is lesser compared to UPQC-Q.

- However there is another side of the coin too, and in this case, it is the shunt inverter. As already discussed, in UPQC-P the shunt inverter rating increases with increase in the % of sag. Thus, even if the series inverter rating is at its minimum value, the shunt inverter rating increases accordingly. In case of UPQC-Q, as no active power is involved to compensate the sag, there is no active power exchange between the source, shunt and series inverters. Thus, the current handled by the shunt inverter in UPQC-Q is lower than UPQC-P. In other words, to compensate the same percentage of sag, the required shunt inverter rating using UPQC-Q would be lower than the UPQC-P. Therefore, the increased series inverter voltage rating is counter balanced (at certain percentage) by reduced shunt inverter current rating.

- Another interesting fact is that when UPQC-Q compensates the sag, it causes the load current power factor to boost *w.r.t.* the source voltage. Thus, UPQC-Q would be a better choice in applications where the load power factor is very low (high reactive power demand). On the other hand, under such scenarios the shunt inverter rating of UPQC-P further increases.

- Under the laboratory test conditions (for voltage sag compensation), it is observed that in UPQC-P the DC link voltage falls down slightly (Figure 2.27 (b)), whereas, in UPQC-Q

the DC link voltage remains unaffected (Figure 3.15 (b)). This suggests that stress on UPQC-P shunt inverter switches should be much higher than that on UPQC-Q.

- Unfortunately, UPQC-Q can not compensate the swell on the system. Therefore, modification or corrective action is essential while developing the controller for UPQC-Q. The sag and swell and thus the flickers are easily compensated by UPQC-P without modifying its controller.

The discussion on UPQC-P and UPQC-Q does not fully answer the question – *which approach should be used to compensate the sag on the system?* Though, it certainly gives the broad view to select one out of the two approaches based on the particular load and system requirements.

3.7 Conclusions

In this chapter it has been demonstrated through simulation as well as experimental studies that voltage sag on the system can be effectively compensated through reactive power control. A simplified approach to extract the required quadrature voltage required to be injected through series inverter, to achieve the reactive power control has also been proposed. The interest in selection of QVI approach is that it does not require any active power for its operation. In addition to this, if the load is inductive in nature demanding high reactive power, the QVI during voltage sag compensation, also helps to improve the effective load power factor angle, i.e. the series inverter also takes part in load reactive power compensation. Thus the reactive power burden on shunt inverter during voltage sag condition reduces considerably.

A brief discussion on voltage sag compensation using UPQC-P and UPQC-Q has been also reported at the end of chapter. It highlights the advantages and limitations offered by both the approaches. Indeed it helps to make an adequate choice while selecting the UPQC to protect sensitive loads from voltage sag on the network.

CHAPTER 4

A NOVEL SYSTEM CONFIGURATION FOR THREE-PHASE FOUR-WIRE DISTRIBUTION SYSTEM

4.1 Introduction

Modern distribution systems are becoming increasingly sensitive and vulnerable due to several power quality issues. Therefore, the field installation of active filters to overcome some of the major power quality problems is slowly becoming popular. UPQC is one of the leading power quality enhancement devices that has a great scope in futuristic distribution systems. A three-phase four-wire (3P4W) distribution system is generally realized by providing a neutral conductor along with the three power lines from substation or by utilizing a delta-star transformer at the distribution level. Additionally, the UPQC installed for 3P4W applications generally considers 3P4W supply (Aredes *et al*., 1998; Faranda and Valade, 2002). Considering this aspect, an interesting UPQC based system configuration/structure is proposed in this chapter for future modern three-phase four-wire (3P4W) distribution system.

The 3P4W system is realized from three-phase three-wire (3P3W) UPQC based system. The neutral of series transformer, used in the series part of UPQC, is considered as a neutral for proposed 3P4W system. Thus, even if the power supplied by utility is 3P3W, an easy expansion to 3P4W system can be achieved in UPQC based applications.

Unbalanced load currents are very common and a significant problem in a 3P4W distribution system. Therefore, this chapter also focuses on unbalanced load current problem with a new control approach. In this approach, the fundamental active power demanded by each of the phases is computed first and these active powers are then equally redistributed to each phase. Thus, the proposed control strategy can truly make the unbalanced load currents as perfectly balanced at source side. Moreover, attention is also given on neutral current compensation such that the transformer neutral point will always be at virtual zero potential. A fourth leg is added to the existing shunt inverter for effective neutral current compensation. The

simulation as well as experimental results are given to validate the possible utilization of proposed 3P4W UPQC system configuration and to evaluate the performance of proposed unbalance compensation approach.

4.2 Three-Phase Four-Wire (3P4W) Distribution System Configurations

In this section, the conventional 3P4W distribution systems and proposed UPQC based 3P4W distribution system configuration are briefly discussed.

4.2.1 Classical 3P4W Distribution System

Generally, a three-phase four-wire (3P4W) distribution system is realized by providing the neutral conductor along with the three power conductors from generation station or by utilizing a three-phase delta-star (Δ-Y) transformer at distribution level. Figure 4.1 shows a 3P4W network in which the neutral conductor is provided from the generating station itself, whereas, Figure 4.2 shows a 3P4W distribution network considering Δ-Y transformer. In both the cases the utility provides the neutral conductor to the consumers/ loads. There are two important issues related with the neutral conductor, the cost involved to install and the losses (resitive) associated with it. The size of the neutral conductor increases with increased current magnitude.

Consider a plant site where three-phase, three-wire UPQC is already installed to protect a sensitive load and to restrict any entry of distortion from load side towards utility, as shown in Figure 4.3. Now, we want to upgrade the system from 3P3W to 3P4W system as a result of the installation of some single-phase loads. In such cases, if the distribution transformer is close to the plant under consideration, the utility can provide the neutral conductor from this transformer without major cost involvement. In certain cases, the distribution transformer may be not situated in close vicinity. In those cases it will be a costly solution.

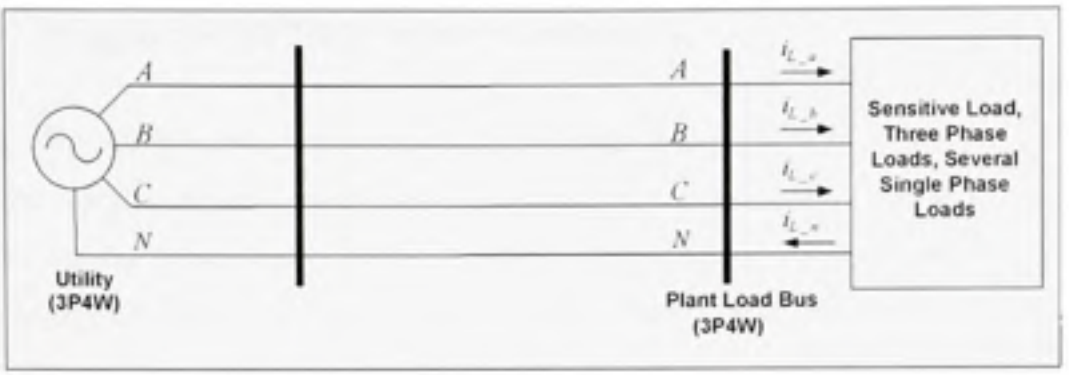


Figure 4.1 Three-phase four-wire distribution system: neutral provided from generation station.

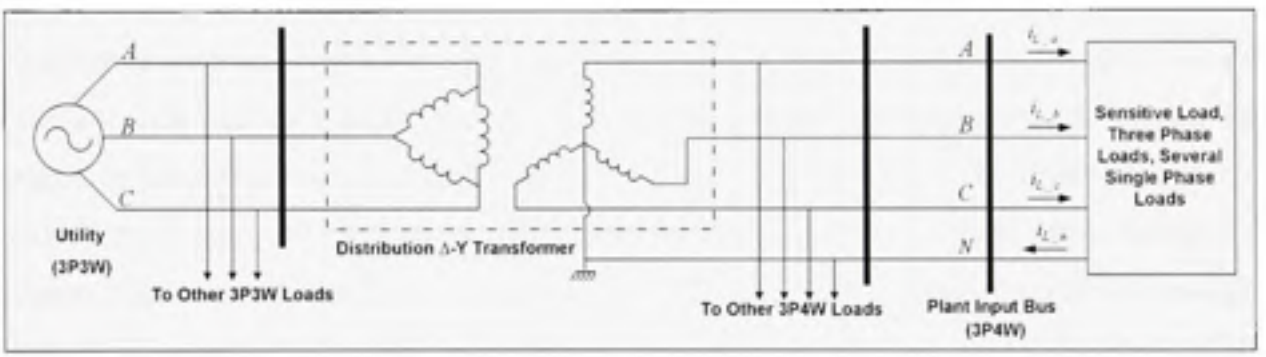


Figure 4.2 Three-phase four-wire distribution system: neutral provided from Delta-Star transformer.

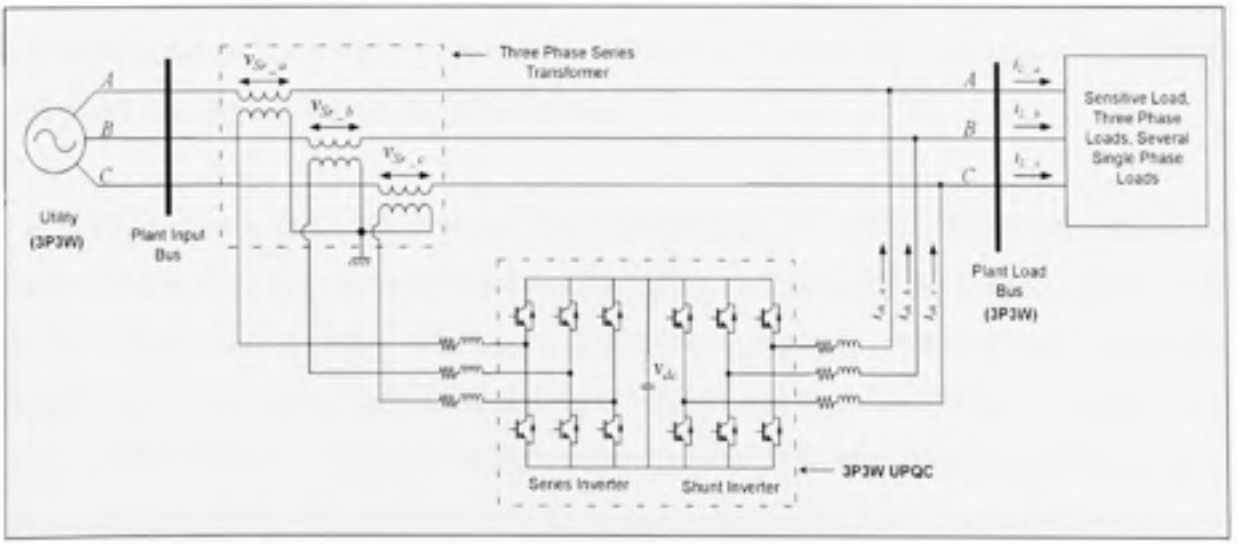


Figure 4.3 Three-phase three-wire UPQC topology.

4.2.2 Proposed 3P4W UPQC System Configuration

Recently, the utility service providers are exercising increased restrictions on the current THD limits, drawn by non-linear loads, to control the power distribution system harmonic pollution. At the same time, the use of sophisticated equipments/loads that has been increasing significantly, need clean power for their proper operation. Therefore, in the future distribution system and the plant/load centers consisting of UPQC would be a common practice.

As noticed from Figure 4.3, the UPQC should necessarily consist of three-phase series transformer (or three single units of single-phase transformers) in order to connect one of the inverters in the series with the line to function as controlled voltage source. If we use the neutral of three-phase series transformer as the neutral wire to realize the three-phase four-wire system, then, 3P4W system can easily be achieved from a three-phase three-wire system. Figure 4.4 shows the proposed novel 3P4W topology realized from 3P3W system. This proposed system has all the advantages of general UPQC in addition to easy 3P3W system to 3P4W system expansion. The proposed topology may play an important role in the future 3P4W distribution system for more advanced, UPQC based plant/load center installation, where the utility would be have an additional option to realize 3P4W system just by providing three-phase three-wire supply. Additionally, the neutral point can be grounded at the plant site, depending on the requirements.

In a 3P4W system, the load is most likely unbalanced in nature. Therefore, the current unbalance as well as the neutral current compensations are the significant power quality issue that the UPQC should tackle effectively. The neutral current, present if any, would flow through this fourth wire towards transformer neutral point. A fourth leg is added on the existing 3P3W UPQC to compensate the neutral current flowing towards transformer neutral point and it can assure zero current flow towards neutral point. Thus, the transformer neutral point will always be at virtual zero potential.

The distinguishing features of proposed topology are highlighted as:

- Easy expansion from 3P3W UPQC based system to 3P4W system.
- Can serve as an additional option for utility/ plant in futuristic UPQC based distribution system.
- Elimination of neutral conductor required from utility side (hence the cost associated with it).
- The use of forth-leg for shunt inverter helps to restrict flow of current towards transformer neutral point. Thus, the transformer neutral point will be at virtual zero potential.

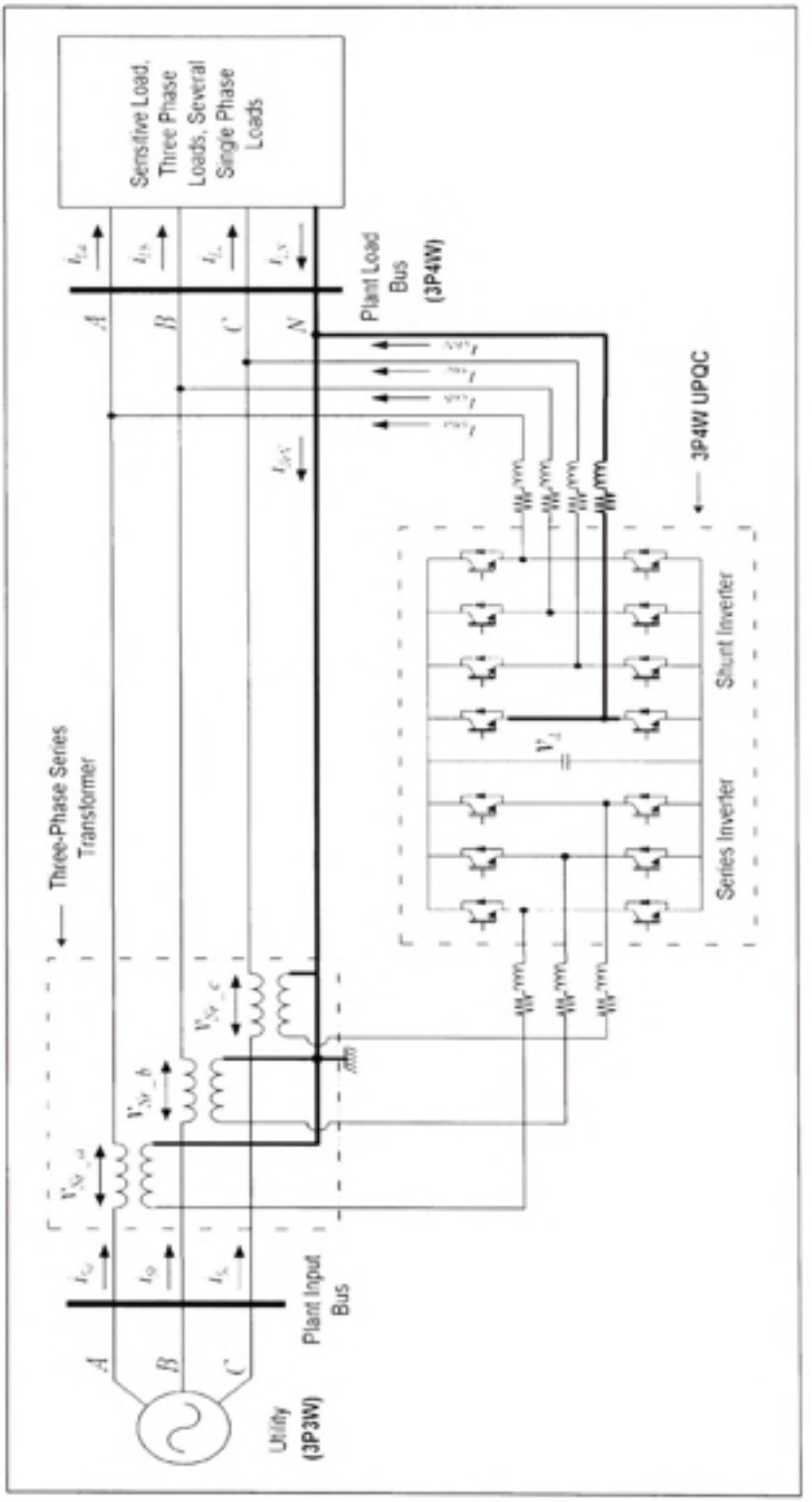


Figure 4.4 Proposed three-phase four-wire (3P4W) system realized from three-phase three-wire (3P3W) UPQC based system.

4.3 UPQC Controller Development

In this section, the topologies used to compensate current related problems in 3P4W system are briefly discussed first. Later on in the section, a new control approach to generate balance reference source currents under unbalanced load condition is proposed and discussed in detail.

4.3.1 Active Filter Topologies for Three-Phase Four-Wire System

The load on the 3P4W system can be a combination of several three-phase loads (linear/ non-linear) and single-phase loads connected between neutral and any of the phases or between any of the two phases. This suggests that in 3P4W system the currents drawn from the source would be unbalanced. Moreover, if the single-phase loads are supplied utilizing the neutral conductor, a current will be flow through it. Thus, among the single-phase, three-phase three-wire and three-phase four-wire systems, the 3P4W system is the most susceptible to different power quality problems as the utility has to deal with reactive power, current harmonics, current unbalance and neutral current.

Three shunt active filter topologies are available to tackle the power quality problems associate with the load currents in 3P4W system, *i*) split capacitor topology (Figure 4.5), *ii*) four-leg topology (Figure 4.6), and *iii*) three H-bridge topology (Figure 4.7). The split capacitor topology essentially needs two capacitors (therefore, two DC voltage sensors) and an extra control loop to maintain zero voltage error difference between both the capacitor voltages, resulting more complex control loop to maintain the DC bus voltage at constant level. The four-leg topology requires one addition leg (two switches), whereas, the three H-bridge topology requires six additional switches, as compared to the split capacitor topology. Three H-bridge topology can be of significant advantage for high power application (Khadkikar V. and Chandra A., 2008a).

The most important and essential constraint to realize the proposed UPQC based 3P4W system is that the neutral point should be at zero potential. Among the three topologies, only

the four-leg topology offers direct control over the neutral current. On the other hand, in split capacitor and 3H bridge topologies, there is no direct control over neutral current. Hence, a four-leg topology is used for shunt inverter in realization of proposed UPQC based 3P4W system.

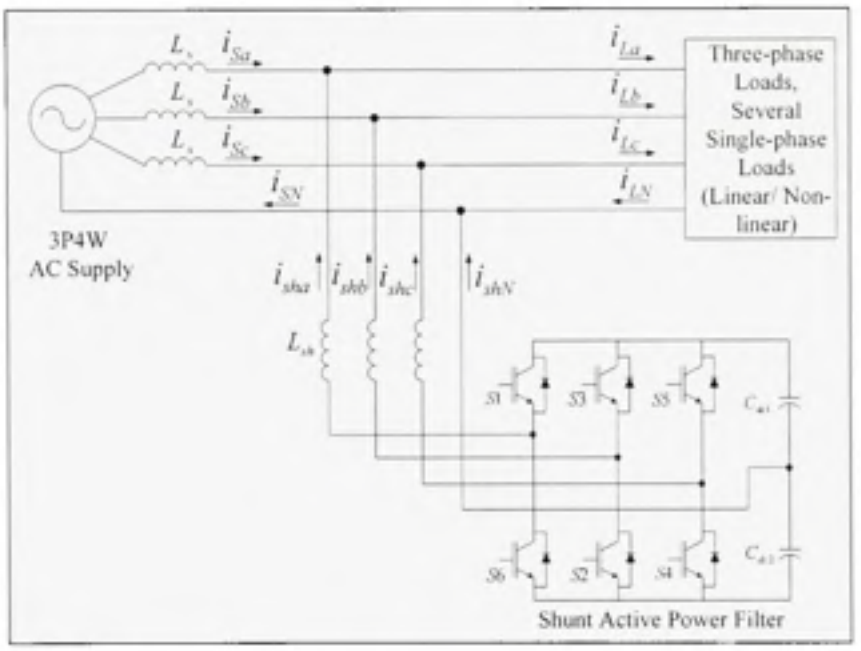


Figure 4.5 Split capacitor topology used for 3P4W shunt active filter.

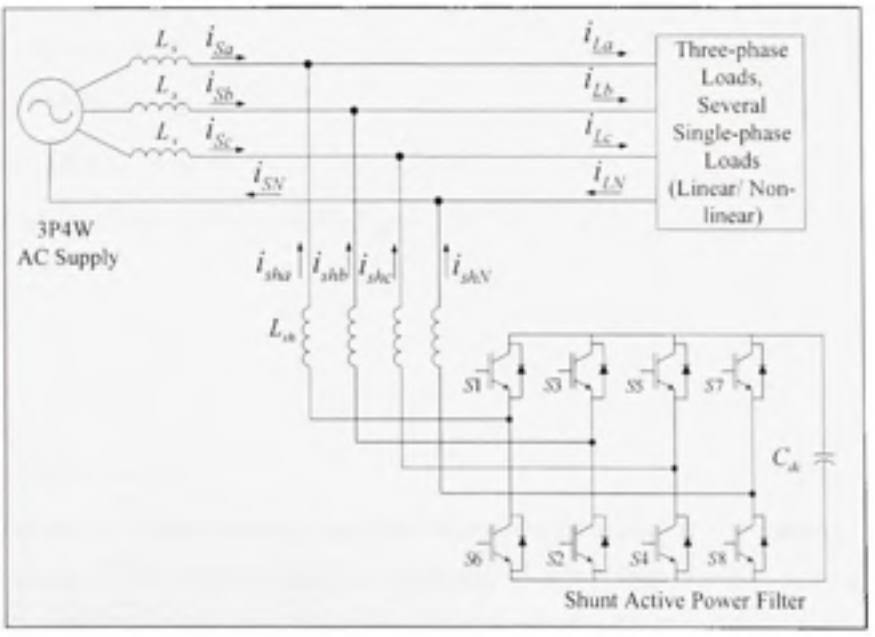


Figure 4.6 Four-leg topology used for 3P4W shunt active filter.

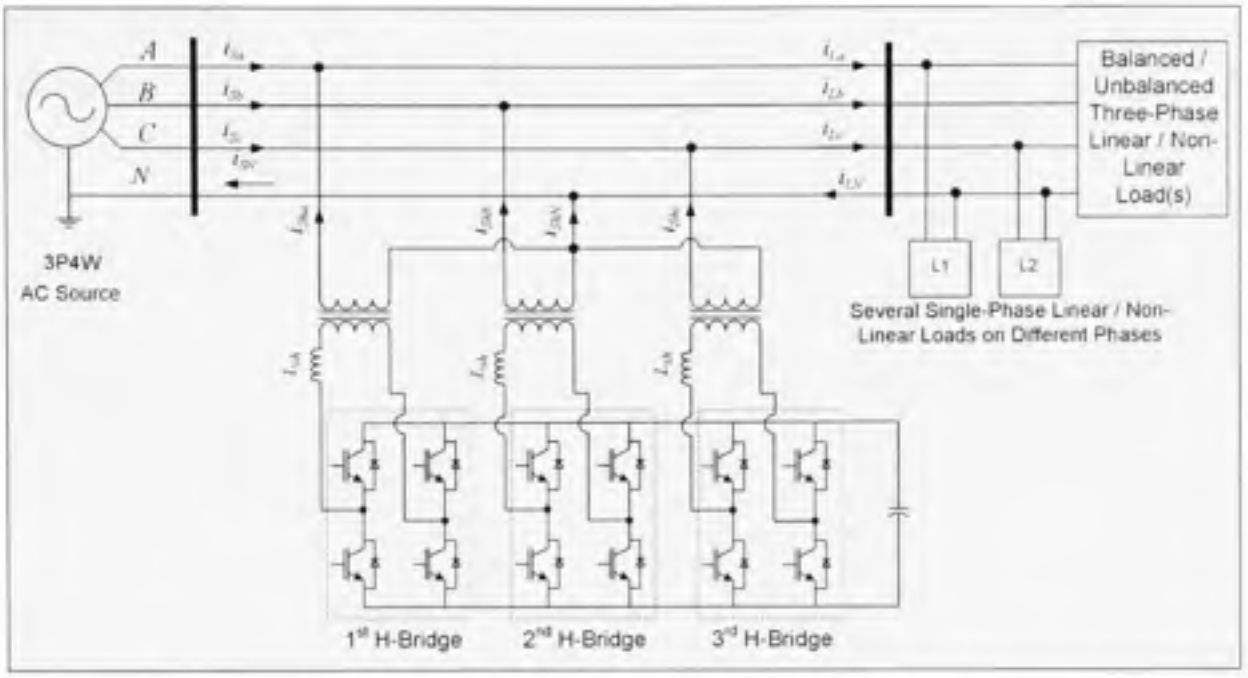


Figure 4.7 3H bridge topology used for 3P4W shunt active filter.

4.3.2 Current Unbalance Compensation

As mentioned already, the 3P4W system is highly vulnerable to different power quality problems. Severely unbalance currents in 3P4W system can introduce significant unbalance in the supply voltages. There are several control strategies that have been utilized to compensate the unbalanced load currents, but, very few give the desired results. For example, the PI regulator based control strategy which is the simplest one, requires two voltage sensors[1] (one for source voltage and other for DC link voltage) to generate reference current signals. In such an approach, the knowledge of actual load currents is not essential. But, the

[1] Additionally, three or four current sensors are also required to perform PWM operation. These sensors are used to sense the actual source currents (indirect approach) or shunt filter currents (direct approach). Three current sensors are essential for split-capacitor topology, whereas, the four-leg topology may requires three or four (forth for neutral current) current sensors based on the control strategy.

unbalanced current injected by the shunt inverter causes the DC link voltage to oscillate/fluctuate. Therefore, in most cases the perfect current unbalance compensation using PI regulator based approach is uncertain.

The three-phase *p-q* theory based approach requires the knowledge of all the phase voltages and load currents. Under sinusoidal supply voltage the *p-q* theory performs well, but its performance is greatly affected when supply voltages are unbalanced (Khadkikar and Chandra, 2008d). The *d-q* transformation based approach can give a better performance as it is independent of the source voltages.

4.3.3 Proposed Current Unbalance Compensation Approach

In this section, a new control approach to generate perfect balanced reference source current signals is addressed. The controller for shunt inverter is developed based on the proposed approach. The control algorithm for series inverter is based on unit vector template generation scheme as already discussed in CHAPTER 2.

4.3.3.1 Balanced Reference Source Current Signal Generation

Based on the load on 3P4W system the currents drawn from the utility may be unbalanced. In this chapter, a new control strategy is proposed to compensate the unbalance present in the load currents by expanding the concept of generalized single-phase *p-q* theory (Khadkikar and Chandra, 2008c). According to this theory (Liu *et al.*, 1999; Haque *et al.*, 2002), a signal-phase system can be defined as a pseudo two-phase system by giving $\pi/2$ lead or $\pi/2$ lag. The resultant two phase system is then represented in α-β coordinates. Thus, the concept of *p-q theory* applied to balanced three-phase system (Akagi *et al.*, 1984) can now also be realized in single-phase system and instantaneous load active as well as reactive powers can be determined.

To apply the single-phase *p-q* theory based approach to the three-phase system, each of the phase voltages and currents of original three-phase system are considered as three

independent two-phase systems. The actual load voltages and load currents are considered as *α–axis* quantities, whereas, the π/2 lead load voltages and π/2 lead load currents are considered as *β–axis* quantities. The major disadvantage of *p-q theory* is that it gives poor results under distorted and/or unbalanced utility voltages. In order to eliminate these limitations the reference load voltage signals extracted for series inverter are used instead of actual load voltages.

For phase–*a*, the load voltage and current in *α–β* coordinates can be represented as follows:

$$\begin{bmatrix} v_{La,\alpha} \\ v_{La,\beta} \end{bmatrix} = \begin{bmatrix} v^{*}_{La}(\omega t) \\ v^{*}_{La}(\omega t + \pi/2) \end{bmatrix} = \begin{bmatrix} V^{*}_{Lm} \sin(\omega t) \\ V^{*}_{Lm} \cos(\omega t) \end{bmatrix} \tag{4.1}$$

$$\begin{bmatrix} i_{La,\alpha} \\ i_{La,\beta} \end{bmatrix} = \begin{bmatrix} i_{La}(\omega t + \varphi_L) \\ i_{La}[(\omega t + \varphi_L) + \pi/2] \end{bmatrix} \tag{4.2}$$

Where, $v^{*}_{La}(\omega t)$ represents the reference load voltage and V^{*}_{Lm} represents the desired load voltage magnitude (as defined in CHAPTER 2).

Similarly, for phase *b* and *c*, the load voltages and currents in *α–β* coordinates can be represented as follows:

$$\begin{bmatrix} v_{Lb,\alpha} \\ v_{Lb,\beta} \end{bmatrix} = \begin{bmatrix} v^{*}_{Lb}(\omega t) \\ v^{*}_{Lb}(\omega t + \pi/2) \end{bmatrix} = \begin{bmatrix} V^{*}_{Lm} \sin(\omega t - 120^{\circ}) \\ V^{*}_{Lm} \cos(\omega t - 120^{\circ}) \end{bmatrix} \tag{4.3}$$

$$\begin{bmatrix} i_{Lb,\alpha} \\ i_{Lb,\beta} \end{bmatrix} = \begin{bmatrix} i_{Lb}(\omega t + \varphi_L - 120^{\circ}) \\ i_{Lb}[(\omega t + \varphi_L - 120^{\circ}) + \pi/2] \end{bmatrix} \tag{4.4}$$

$$\begin{bmatrix} v_{Lc,\alpha} \\ v_{Lc,\beta} \end{bmatrix} = \begin{bmatrix} v^{*}_{Lc}(\omega t) \\ v^{*}_{Lc}(\omega t + \pi/2) \end{bmatrix} = \begin{bmatrix} V^{*}_{Lm} \sin(\omega t + 120^{\circ}) \\ V^{*}_{Lm} \cos(\omega t + 120^{\circ}) \end{bmatrix} \tag{4.5}$$

$$\begin{bmatrix} i_{Lx,\alpha} \\ i_{Lx,\beta} \end{bmatrix} = \begin{bmatrix} i_{Lx}(\omega t + \varphi_L + 120^\circ) \\ i_{Lx}[(\omega t + \varphi_L + 120^\circ) + \pi/2] \end{bmatrix} \tag{4.6}$$

By using the definition of 3-phase *p-q* theory for balanced three-phase system (Akagi *et al.*, 1984), the instantaneous power components can be represented as:

Instantaneous active power,

$$p_{Lx} = v_{Lx,\alpha} \cdot i_{Lx,\alpha} + v_{Lx,\beta} \cdot i_{Lx,\beta} \tag{4.7}$$

Where, x represents a, b, or c, for phase a, b or c, respectively.

Instantaneous reactive power,

$$q_{Lx} = v_{Lx,\alpha} \cdot i_{Lx,\beta} - v_{Lx,\beta} \cdot i_{Lx,\alpha} \tag{4.8}$$

Considering phase–a, the phase–a instantaneous load active and instantaneous load reactive powers can be represented as:

$$\begin{bmatrix} p_{La} \\ q_{La} \end{bmatrix} = \begin{bmatrix} v_{La,\alpha} & v_{La,\beta} \\ -v_{La,\beta} & v_{La,\alpha} \end{bmatrix} \cdot \begin{bmatrix} i_{La,\alpha} \\ i_{La,\beta} \end{bmatrix} \tag{4.9}$$

Where,

$$p_{La} = \overline{p}_{La} + \tilde{p}_{La} \tag{4.10}$$

$$q_{La} = \overline{q}_{La} + \tilde{q}_{La} \tag{4.11}$$

In (4.10) and (4.11), $\overline{p}_{La}$ and $\overline{q}_{La}$ represent the DC components that are responsible for fundamental load active and reactive power, whereas, $\tilde{p}_{La}$ and $\tilde{q}_{La}$ represent the AC components that are responsible for harmonic powers. The phase–a fundamental

instantaneous load active and reactive power components can be extracted from p_{La} and q_{La}, respectively, by using a low pass filter (LPF).

Therefore, instantaneous fundamental load active power for phase –*a*:

$$p_{La,1} = \overline{p}_{La} \tag{4.12}$$

Similarly, the fundamental instantaneous load active powers for phase–*b* and phase–*c* can be calculated as follows:

Instantaneous fundamental load active power for phase –*b*:

$$p_{Lb,1} = \overline{p}_{Lb} \tag{4.13}$$

Instantaneous fundamental load active power for phase –*c*:

$$p_{Lc,1} = \overline{p}_{Lc} \tag{4.14}$$

Since, the load current drawn by each of the phases may be different due to different loads that may be connected to the respective phases, the instantaneous fundamental load active power demand for each phase may not be the same. In order to make this load unbalanced power demand, seen from the utility side, as a perfectly balanced fundamental three-phase active power, the unbalanced load power should be properly redistributed between utility, UPQC (shunt inverter) and load such that, the total load seen by the utility would be linear and balanced. The aforementioned task can be achieved by summing instantaneous fundamental load active power demands of all the three phases and redistributing it again on each of the utility phases. The total fundamental active power demanded by all the loads on the 3P4W system can be computed as –

$$p_{L,total} = p_{La,1} + p_{Lb,1} + p_{Lc,1} \tag{4.15}$$

For equal redistribution of total load active power demand on each of the phases,

$$p^{*}_{S/ph} = \frac{p_{L,total}}{3} \tag{4.16}$$

Equation (4.16) gives the redistributed per phase fundamental active power demand that each of the phases of utility should supply in order to achieve perfect balanced source currents. It is also evident that under all the conditions, the total fundamental active power demanded by the loads would be equal to the total power drawn from the utility but in a perfectly balanced way. Thus, the reference compensating currents representing a perfectly balanced three-phase system can be extracted by replacing the instantaneous total load active power (p_{La}) in (4.9) with redistributed per phase power ($p^{*}_{S/ph}$) and taking its inverse transformation.

$$\therefore \begin{bmatrix} i^{*}_{Sa,\alpha} \\ i^{*}_{Sa,\beta} \end{bmatrix} = \begin{bmatrix} v_{La,\alpha} & v_{La,\beta} \\ -v_{La,\beta} & v_{La,\alpha} \end{bmatrix}^{-1} \cdot \begin{bmatrix} p^{*}_{S/ph} + p_{dc/ph} \\ 0 \end{bmatrix} \tag{4.17}$$

In (4.17), $p_{dc/ph}$ is the precise amount of per phase active power that should be taken from the source in order to maintain the DC link voltage at constant level and to overcome the losses associated with UPQC. The oscillating instantaneous active power ($\tilde{p}_L$) should be exchanged between the load and shunt inverter. The reactive power term (q_L) in (4.17) is considered as zero, since the utility should not supply load reactive power demand. In the above matrix, the *α–axis* reference compensating current represents the instantaneous fundamental source current, since *α–axis* quantities belong to the original system under consideration and the *β–axis* reference compensating current represents the current that is at $\pi/2$ lead with respect to the original system.

$$\text{Therefore, } i^{*}_{Sa,\alpha} = i^{*}_{Sa}(t) = \frac{v_{La,\alpha}(t)}{v^{2}_{La,\alpha} + v^{2}_{La,\beta}} \cdot \left[p^{*}_{S/ph}(t) + p_{dc/ph}(t) \right] \tag{4.18}$$

Similarly, the reference source current for phase–*b* and phase–*c* can be estimated as follows:

$$i^{*}_{Sb}(t) = \frac{v_{Lb,\alpha}(t)}{v^{2}_{Lb,\alpha} + v^{2}_{Lb,\beta}} \cdot \left[p^{*}_{L/ph}(t) + p_{dc/ph}(t) \right] \tag{4.19}$$

$$i^{*}_{Sc}(t) = \frac{v_{Lc,\alpha}(t)}{v^{2}_{Lc,\alpha} + v^{2}_{Lc,\beta}} \cdot \left[p^{*}_{L/ph}(t) + p_{dc/ph}(t) \right] \tag{4.20}$$

4.3.3.2 Neutral Current Compensation

As observed from the previous section, to generate balanced sinusoidal source currents under unbalanced load condition, all the three load currents are sensed and utilized. Using symmetry, the actual neutral current can be extracted simply by adding all the sensed load currents, without actual sensing, as follows:

$$i_{L\_N}(t) = i_{La}(t) + i_{Lb}(t) + i_{Lc}(t) \tag{4.21}$$

The reference neutral current for forth leg thus can be given as,

$$\therefore \; i^{*}_{sh\_N}(t) = -i_{L\_N}(t) \tag{4.22}$$

A block diagram representation of the proposed balanced per phase fundamental active power estimation, DC link voltage control loop based on PI regulator, the reference source current generation as given by (4.18) – (4.22), and the reference neutral current generations are shown in Figure 4.8 (a), (b), (c), and (d), respectively.

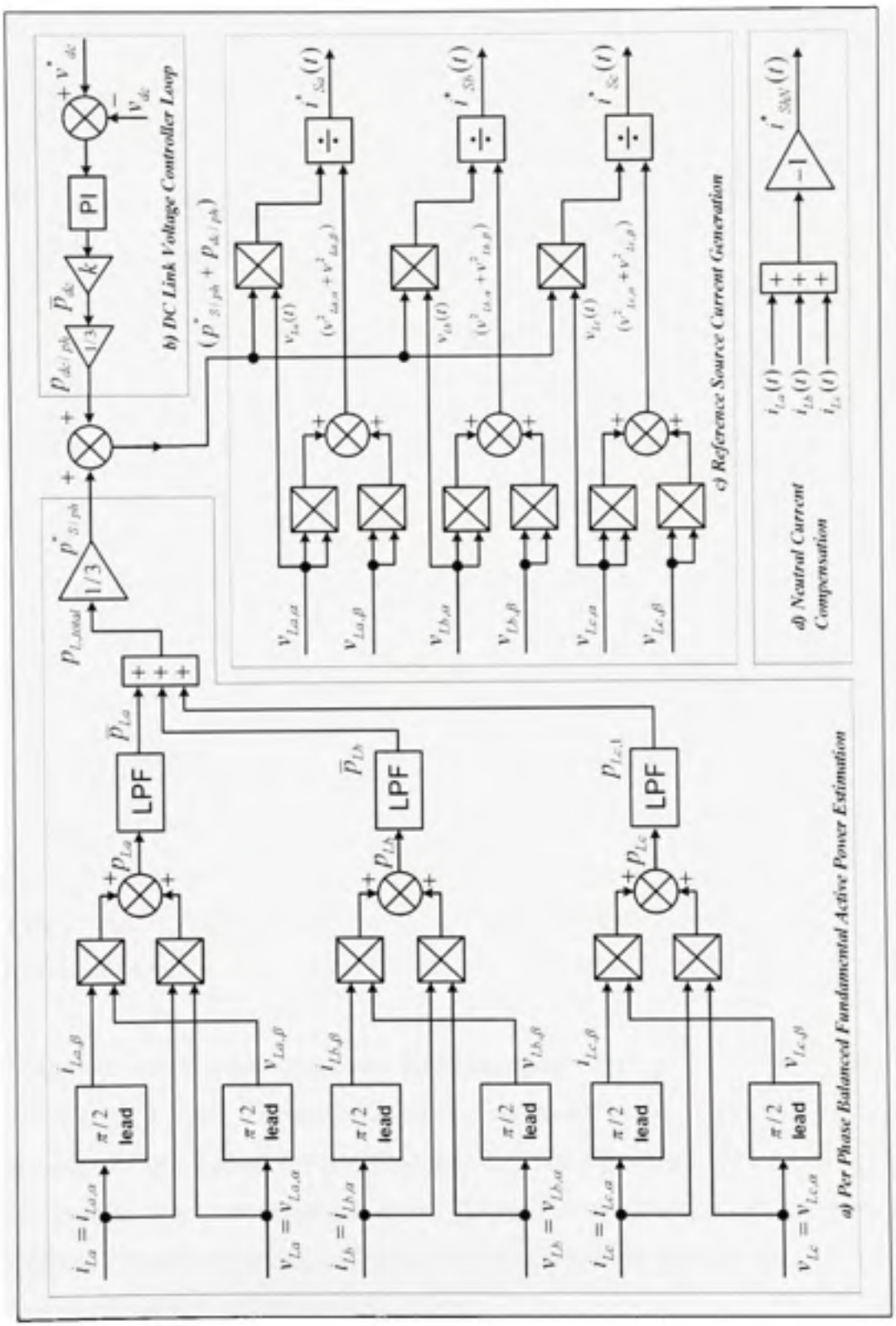


Figure 4.8 Shunt inverter control block diagram.

4.4 Simulation Results

The simulation results for proposed UPQC based 3P4W topology are shown in Figure 4.9 (a)–(j). MATLAB/Simulink is used as a simulation tool. The utility voltages are assumed to be distorted with voltage THD of 9.5%. These distorted voltages profile is shown in Figure 4.9 (a). UPQC should maintain the voltage at the load bus at a desired value and free from distortion. The plant load is considered as the combination of a balanced three-phase diode bridge rectifier followed by a R-L load, which acts as a harmonic generating load, and three different single-phase loads on each phase, with different load active and reactive power demands. The resulting load current profile shown in Figure 4.9 (g) has THD of 12.15%.

The shunt inverter is turned ON first at time t=0.1 sec such that it maintains the DC link voltage at set reference value, here 220 V (not shown in the Figure 4.9). At time t=0.2 sec, the series inverter is put into the operation. The series inverter injects the required compensating voltages through a series transformer, making the load voltage free from distortion (THD= 1.5%) and at a desired level (Figure 4.9 (b)). The series inverter injected voltage profile is shown in Figure 4.9 (c). Simultaneously, the shunt inverter injects the compensating currents to achieve the balanced source current, free from distortion, as discussed in the pervious section. The compensated source currents shown in Figure 4.9 (f) are perfectly balanced with the THD of 2.3%. The currents injected by the shunt inverter are shown in Figure 4.9 (g).

Since there are some loads connected between phase and neutral, current flows towards transformer neutral point. The load side neutral conductor current profile is shown in Figure 4.9. As noticed from Figure 4.9 (e), the shunt inverter effectively compensates the current flowing towards transformer neutral point. Thus, the series transformer neutral point is maintained at virtual zero potential. The compensating current injected through fourth leg of shunt inverter is shown in Figure 4.9 (j).

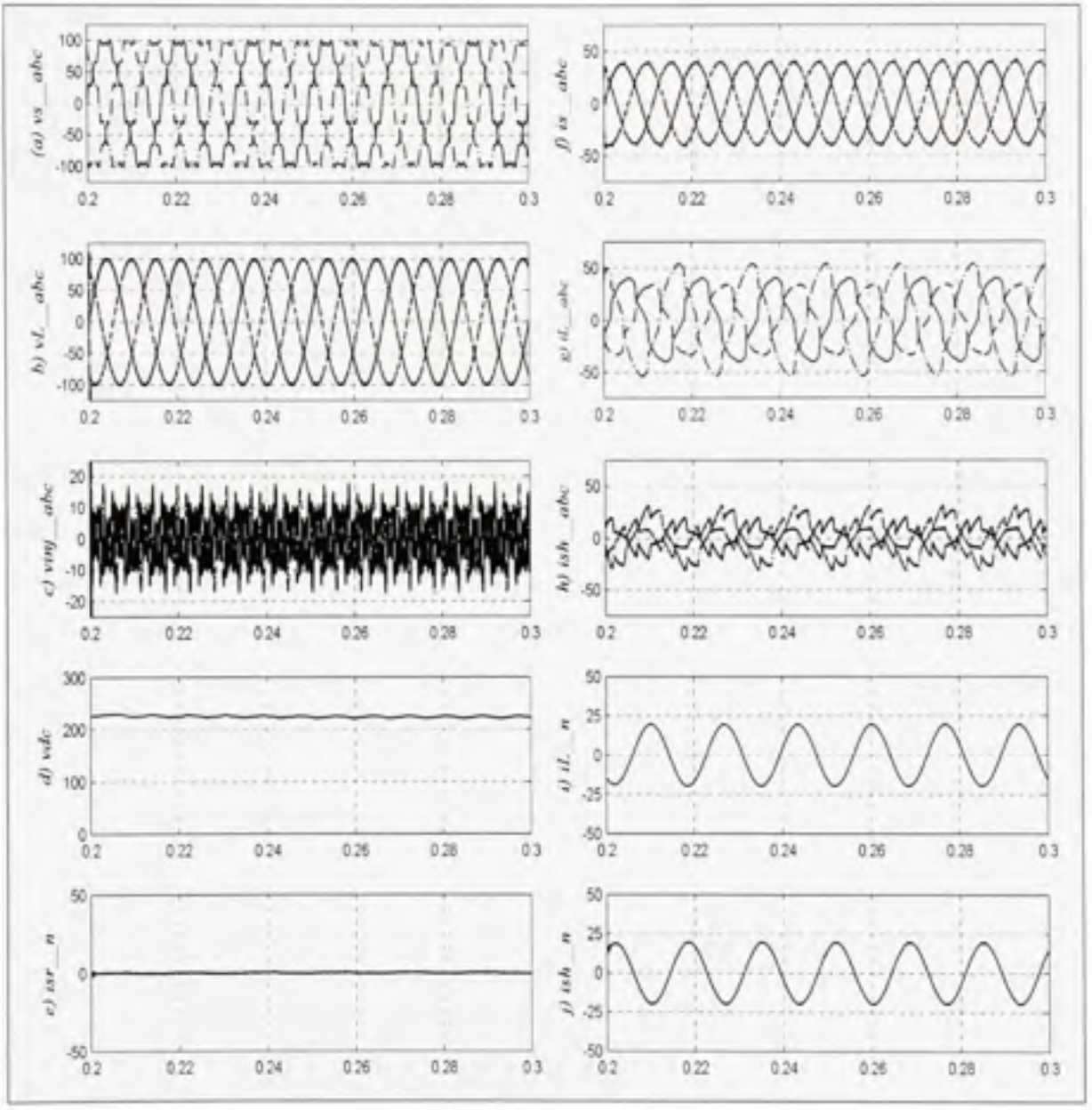


Figure 4.9 Simulation results – performance of proposed current unbalance compensation approach applied under novel UPQC topology.

4.5 Laboratory Experimental Results

The performance of proposed current unbalance compensation approach, when applied to novel 3P4W UPQC system configuration, is validated in the laboratory. Performance of the series part of UPQC is similar to that discussed in the previous chapters. In this section, attention is given to maintaining the series neutral point at virtual zero level. Interesting results are presented and discussed in the following subsections.

4.5.1 System under Consideration

The laboratory experimental setup to generate unbalanced load currents is given in Figure 4.10. The total load on the system consists of *i*) load L1, three-phase diode bridge rectifier (DBR) followed by a capacitor (very common type of load in ASD application). *ii*) load L2, a highly inductive load between phase –*a* and neutral, and *iii*) load L3, a single-phase non-linear load (single-phase DBR followed by RL load) between phase –*b* and neutral. In Figure 4.10, the magnetic actuator SW1 is used to connect/disconnect highly inductive load to/from the network, whereas, the manual switch SW2 is utilized to disconnect the phase –*a* from the circuit (three-phase to single phasing condition).

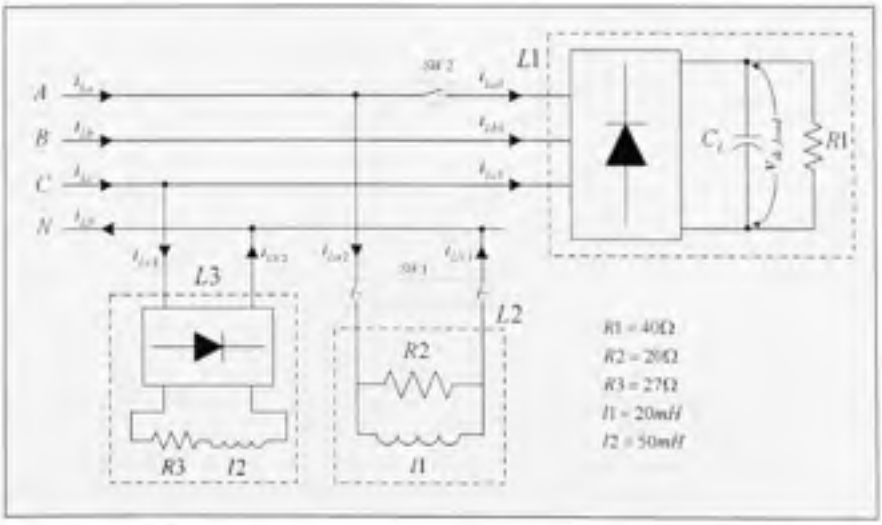


Figure 4.10 Experimental setup to generate unbalanced load currents.

The current drawn by the individual loads and the total load on each of the phases under steady state are given in Figure 4.11. As seen from the Figure 4.11 (a), the total current drawn by the phase –*a* (trace-4) is the combination of a non-linear current (trace-2) and a highly inductive load current (0.33 lagging, trace-3). Phase –*b* supplies only three-phase non-linear load and its current profile is shown in Figure 4.11 (b), trace-2/trace-3. Phase –*c* current is the combination of three-phase (trace-2) and single-phase (trace-3) non-linear currents (Figure 4.11 (c)). Since there are two separate single-phase loads connected to the neutral conductor, the current flowing through it is the combination of individual current drawn by those loads, as can be noticed in Figure 4.11 (d). In Table 4.1, the *rms* value of current, % THD, K factor (ratio of maximum value to the fundamental value), and power factor of each load current is mentioned.

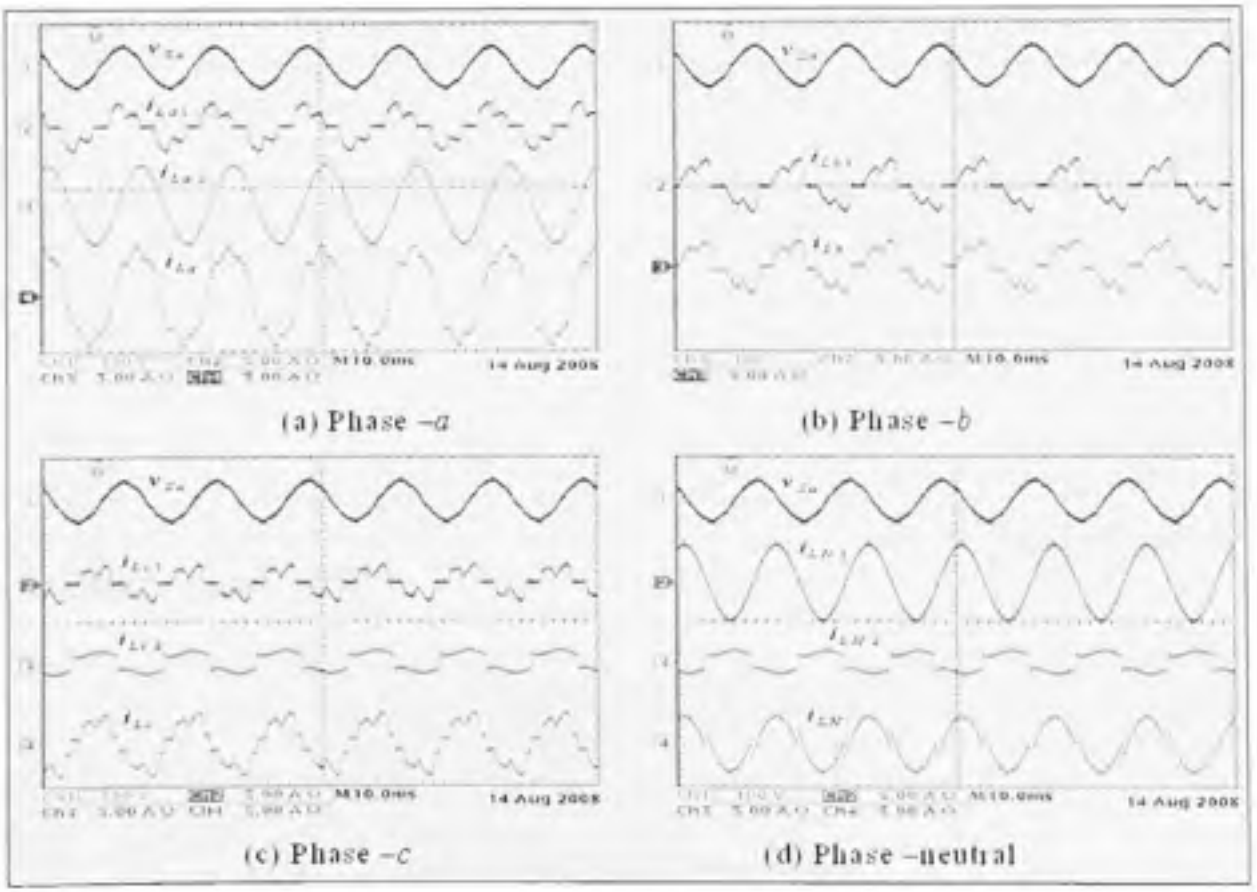


Figure 4.11 Individual current drawn by each of the loads.

Table 4.1
Individual load current details

Current	RMS	% THD	K-factor	P. F.
i_{La1}	1.68 A	34.89 %	4.12	0.94 (lag)
i_{La2}	3.33 A	1.12 %	1.01	0.33 (lag)
i_{La}	4.15 A	14.49 %	1.53	0.65 (lag)
i_{Lb}	1.91 A	32.03 %	3.72	0.94 (lag)
i_{Lc1}	1.31 A	41.72 %	6.56	0.90 (lag)
i_{Lc2}	1.16 A	31.05 %	6.91	0.95 (lag)
i_{Lc}	2.48 A	26.27 %	3.8	0.95 (lag)

The unbalance present in the load currents is expressed by computing the current unbalance factor (CUF) which is calculated as follow:

$$CUF = \frac{\max\{|I_{avg} - I_a|, |I_{avg} - I_b|, |I_{avg} - I_c|\}}{I_{avg}} \tag{4.23}$$

$$\text{Where, } I_{avg} = \frac{(I_a + I_b + I_c)}{3} \tag{4.24}$$

Using the data from Table 4.1,

$$I_{avg} = \frac{(4.15 + 1.91 + 2.48)}{3} = 2.847 \tag{4.25}$$

$$|I_{avg} - I_{La}| = |2.847 - 4.15| = 1.303 \tag{4.26}$$

$$|I_{avg} - I_{Lb}| = |2.847 - 1.91| = 0.937 \tag{4.27}$$

$$\left|I_{avg} - I_{Lc}\right| = \left|2.847 - 2.48\right| = 0.367 \tag{4.28}$$

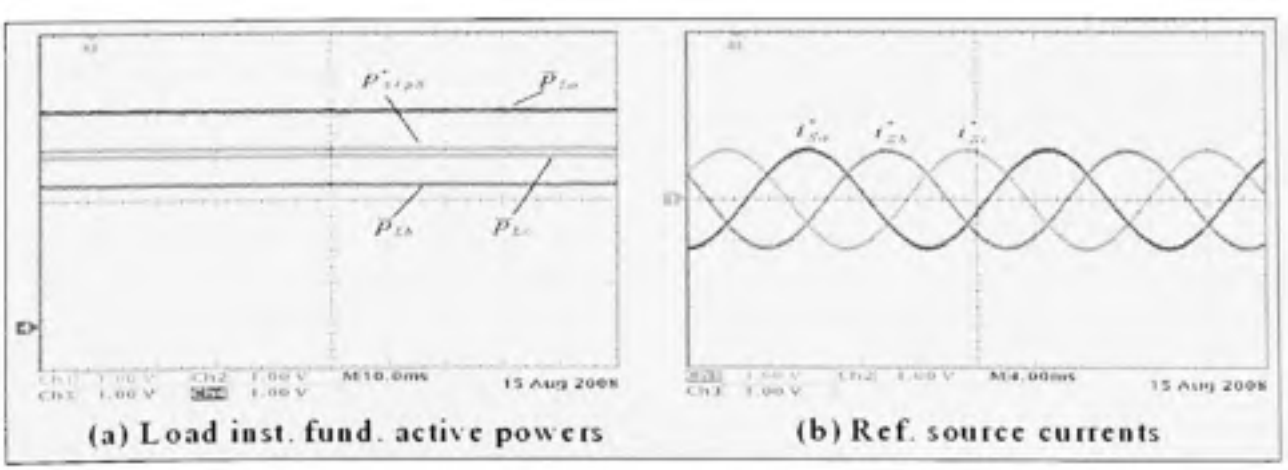
$$\text{Using (4.23), } CUF = \frac{\max\{1.303, 0.937, 0.367\}}{2.847} = \frac{1.303}{2.847} = 0.4576 \tag{4.29}$$

$$\text{Therefore, } CUF = 45.76\% \tag{4.30}$$

Thus, the unbalance present in the load current, on the basis of current *rms* values, is determined as 45.76%.

4.5.2 Real-Time Instantaneous Fundamental Load Active Power Extraction

Figure 4.12 (a) shows the experimental result to demonstrate the real-time extraction of instantaneous fundamental active power demanded by each phase and the redistributed per phase fundamental active power. Note that the computed load fundamental active powers in α-β coordinates are DC values. The generated balanced reference source current signals using proposed approach are shown in Figure 4.12 (b).



(a) Load inst. fund. active powers (b) Ref. source currents

Figure 4.12 Real-time extraction of instantaneous fundamental load active power and generated reference source current signals using proposed approach.

4.5.3 Current Unbalance Compensation – Steady State Results

The steady-state experimental results when the shunt inverter is put into operation are given in Figure 4.13. The gate pulses to the series inverter are kept off and the series transformers secondary windings (connected in the line) are short circuited. The unbalanced load current profile (CUF= 45.76%) is shown in Figure 4.13 (a). The source current profile (Figure 4.13 (b)) suggests that the unbalanced and distorted load currents now appear as almost balanced sinusoidal source currents, free from unwanted reactive and harmonics components. The *rms* currents drawn from the source, %THD vales, k-factors and power factors are given in Table 4.2. The source current unbalance factor using proposed approach is found as 1.08%[2] (practically balanced). The interesting observation (Figure 4.13 (c)), is that to make unbalanced load currents as balanced, the currents injected by shunt inverter are unbalanced in nature.

The forth leg compensates the neutral current present due to the single-phase loads effectively (Figure 4.13 (d), trace-2), restricting the current to flow towards transformer neutral point. In other words, the transformer neutral point is at virtual zero potential and thus the proposed UPQC based 3P4W configuration could be promising and considered in future distribution system.

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[2] From Table 4.2, $I_{avg} = 2.77$, $CUF = \frac{\max\{0.03, 0.02, 0.01\}}{2.77} = \frac{0.03}{2.77} = 1.08\%$

Table 4.2
Source current details before and after compensation

Current	*RMS*	*Peak*	*% THD*	*K-factor*	*P. F.*
Before Compensation					
i_{Sa}	4.15 A	5.90 A	14.49 %	1.53	0.65 (*lag*)
i_{Sb}	1.91 A	3.11 A	32.03 %	3.72	0.94 (*lag*)
i_{Sc}	2.48 A	3.70 A	26.27 %	3.80	0.95 (*lag*)
After Compensation					
i_{Sa}	2.80 A	3.95 A	1.53 %	1.03	1.0 (*unity*)
i_{Sb}	2.75 A	3.81 A	2.93 %	1.08	1.0 (*unity*)
i_{Sc}	2.76 A	3.87 A	2.94 %	1.14	1.0 (*unity*)

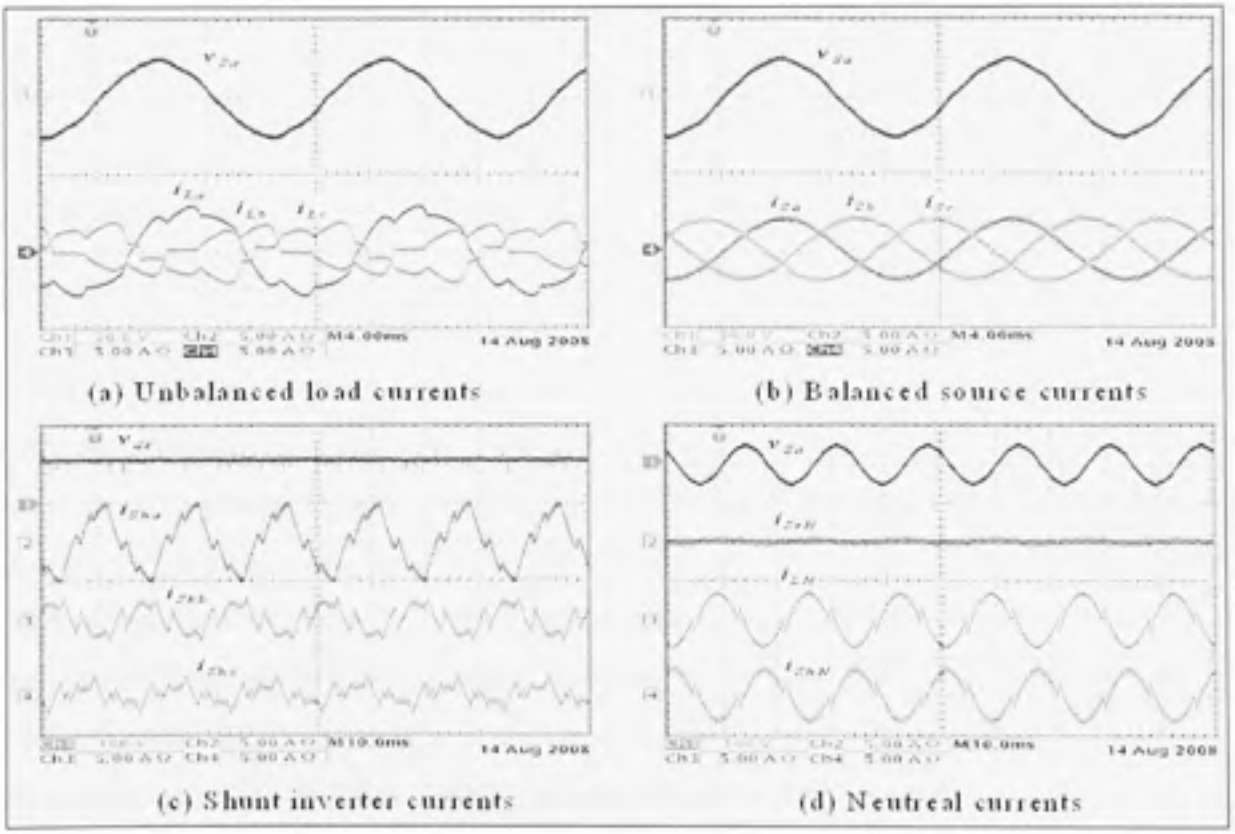

Figure 4.13 Experimental results (steady-state condition): performance of proposed current unbalance compensation approach.

4.5.4 Dynamic Performance

The performance of the proposed approach under dynamic conditions are also tested. Two different situations are considered, in one case the load on the system is increased/ decreased arbitrarily, whereas, in the other case one phase is removed from the circuit. These tests are carried out to ensure that the proposed controller adapts the new steady state quickly, maintaining balanced source currents and the neutral point remains at virtual zero potential irrespective of the change in the load conditions.

4.5.4.1 Load Change

The experimental results during momentary increase in the load on the system are given in the Figure 4.14. All of a sudden switch SW1 (Figure 4.10) is closed such that the highly inductive single-phase RL load get connected to the network. The change in load current profiles can be noticed from the Figure 4.14 (a). As the load is connected between phase *–a* and the neutral conductor, there is increase in phase *–a* load current (trace-1) and the neutral current (trace-4). The phase *–b* and phase *–c* load currents remain unaffected.

The added RL load demands high reactive power and certain amount of active power. In the proposed approach, as discussed in the previous sections, each phase fundamental active power is summed together and redistributed as balanced active power on each of the phases. This fact can be confirmed from the Figure 4.14 (b), where, there is slight increase in source current magnitude of phase *–b* and *–c* currents in order to accommodate the newly added fundamental load active power demand and thus to maintain the balanced source currents. The performance of shunt inverter is shown in Figure 4.14 (c). Phase –a shunt compensating current now supports the load reactive power demand locally in addition to the harmonics generated by non-linear load. Note the DC link voltage strictly remains at constant value. Importantly, the forth leg of shunt inverter effectively compensates the change in the neutral current and does not allow the neutral current to flow towards transformer neutral point.

After a period of time, the highly inductive load is removed from the network. The experimental results during this dynamic condition are given in Figure 4.15. The reduction in source current magnitude can be noticed from the Figure 4.15 (a). Thus, the changeover from one operating condition to the other is found to be very smooth and the proposed controller computes the necessary increased/ decreased fundamental load active power demand and maintains the balanced sinusoidal source currents successfully.

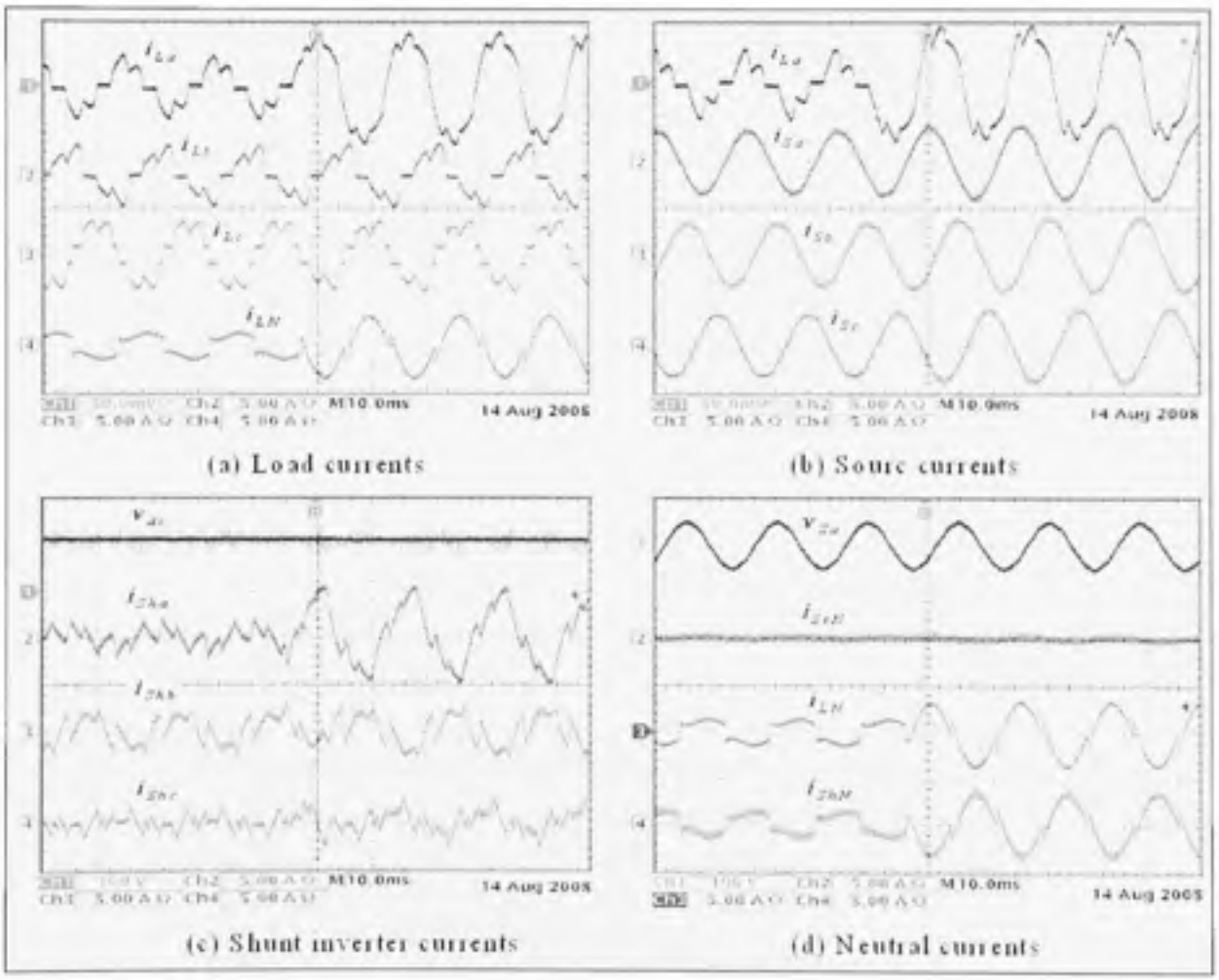

Figure 4.14 Experimental results (dynamic condition): performance of proposed current unbalance compensation approach under sudden increase in the load current.

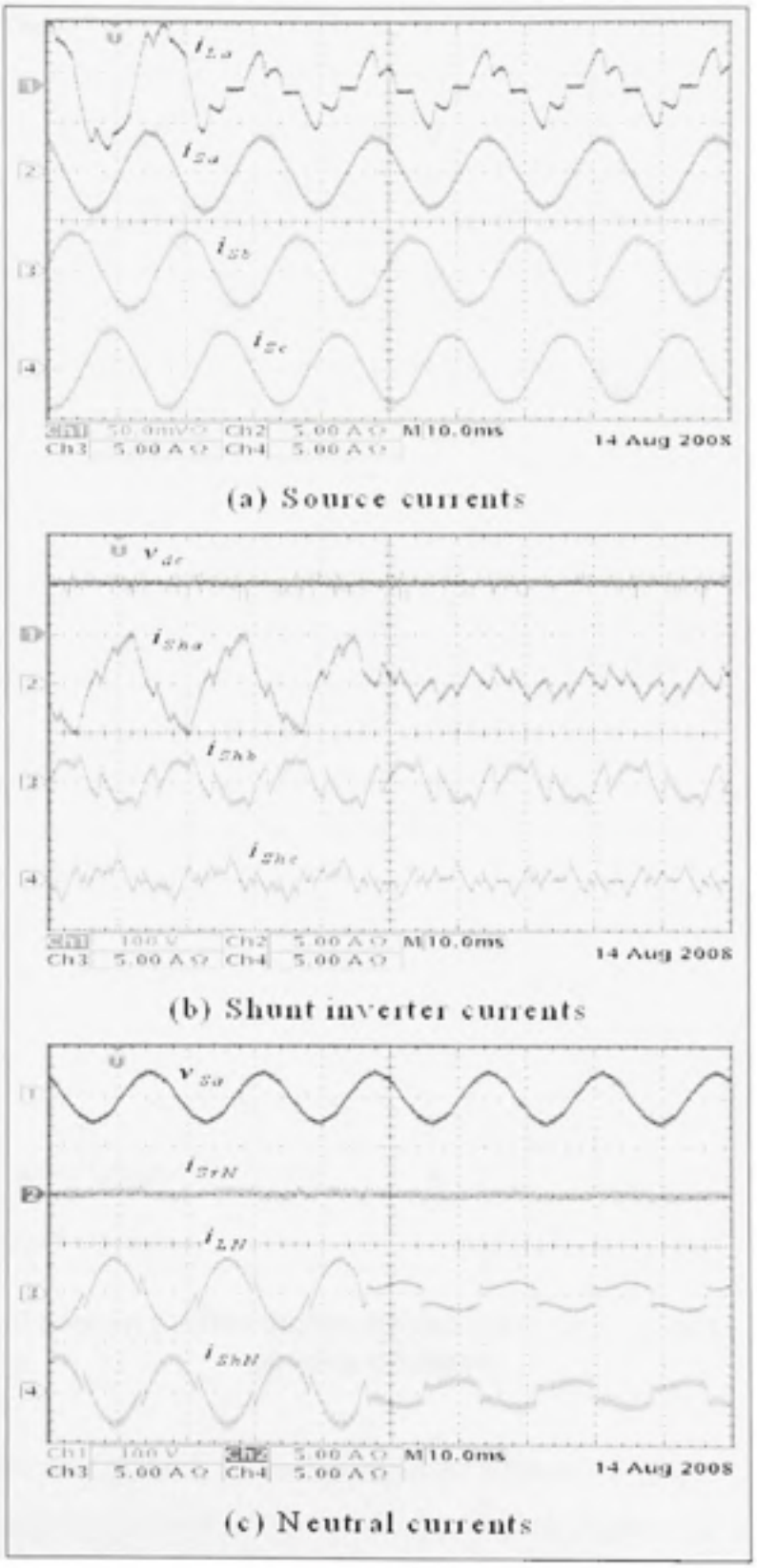

Figure 4.15 Experimental results (dynamic condition): performance of proposed current unbalance compensation approach under sudden decrease in the load current.

4.5.4.2 Three-Phase to Single-Phasing Condition

The response of UPQC system during a load single-phasing condition is discussed in this section. Figure 4.16 shows the experimental results when phase-*a* is momentarily open circuited, by opening the manual switch SW2 (Figure 4.10), and thus causing its load current to be zero. This single-phasing removes the RL load (between phase–*a* and neutral) from the network. Additionally, the three-phase diode bridge rectifier followed by a capacitor is now supplied by phase –*b* and –*c*. A close examination of phase –*b* and –*c* currents (trace-3 and trace-4) suggests that the phase-*c* acts as return path for the load current (current profiles are exactly opposite to each other). The peaky current shape of phase –*b* and –*c* currents also confirm the above observation. As one phase is out, the voltage across the capacitor (C_L) settles down to lower value (Figure 4.16 (a), trace-1), causing the load currents to increase gradually (according to the fall in DC link voltage).

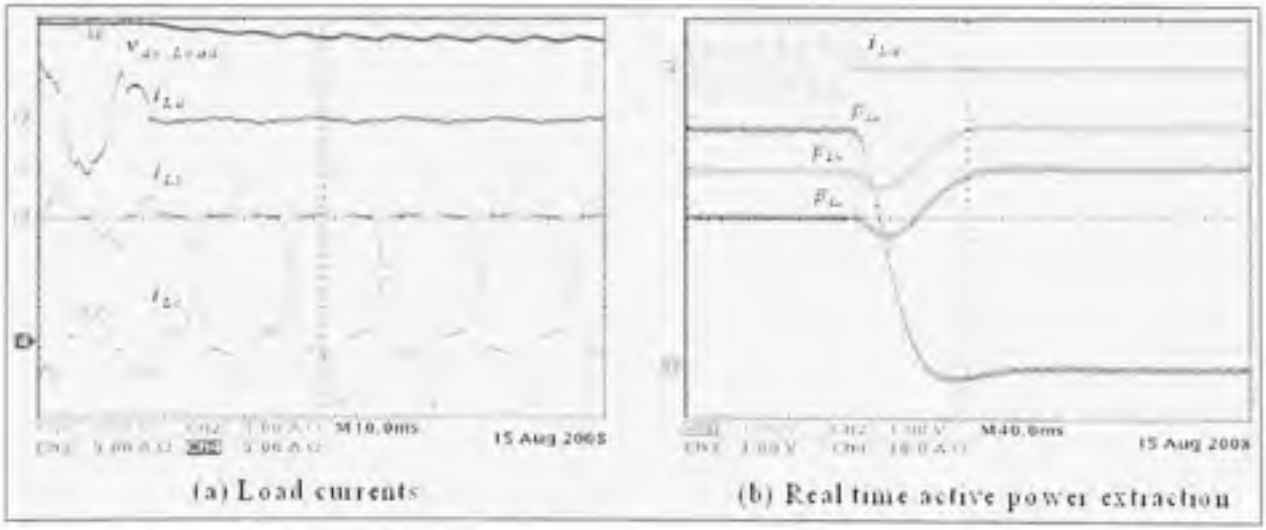

Figure 4.16 Load current profiles during sudden occurrence of three-phase to single-phasing condition.

The real-time extraction of each phase fundamental load active power demand during the single-phasing condition is shown in Figure 4.16 (b). The dip in phase –*b* and –*c* fundamental load active powers is due to the sudden reduction in respective phase current magnitudes. As the phase currents settle to new steady-state condition, the extracted load fundamental active

powers also attain the steady-state values. Phase –*b* also supplies the single-phase non-linear load, and therefore, computed phase –*b* fundamental active power has greater magnitude than phase –*c* fundamental active power.

The experimental results to evaluate the UPQC system response during the three-phase to single-phasing condition are given in Figure 4.17. It is considered that prior to single-phasing, the UPQC system (here, shunt inverter only) was in operation. As observed from the Figure 4.17 (b), the sudden removal of phase –*a* does not affect the performance of system. The changeover from one steady-state condition (three-phase) to the other (single-phasing) is very smooth, maintaining the perfect compensation. Table 4.3 gives the load and source currents data once the system settle down to new steady-state condition. In this case, the load and source current unbalance factors are found as 100%[3] and 2.27%[4], respectively.

Table 4.3
Source current details before and after compensation (single-phasing condition)

Current	*RMS*	*Peak*	*% THD*	*K-factor*	*P. F.*
Before Compensation					
i_{Sa}	0.0 A	0.0 A	-	-	-
i_{Sb}	2.62 A	5.27 A	61.62 %	2.01	0.81 (*lag*)
i_{Sc}	3.47 A	6.51 A	50.88 %	3.44	0.73 (*lag*)
After Compensation					
i_{Sa}	2.15 A	3.08 A	2.03 %	1.04	1.0 (*unity*)
i_{Sb}	2.20 A	3.12 A	2.52 %	1.41	1.0 (*unity*)
i_{Sc}	2.25 A	3.08 A	4.94 %	1.23	1.0 (*unity*)

[3] From Table 4.3, $I_{avg} = 2.03$, $CUF = \frac{\max\{2.03, 0.59, 1.44\}}{2.03} = \frac{2.03}{2.03} = 100\%$

[4] From Table 4.3, $I_{avg} = 2.2$, $CUF = \frac{\max\{0.05, 0.0, .05\}}{2.2} = \frac{0.05}{2.2} = 2.27\%$

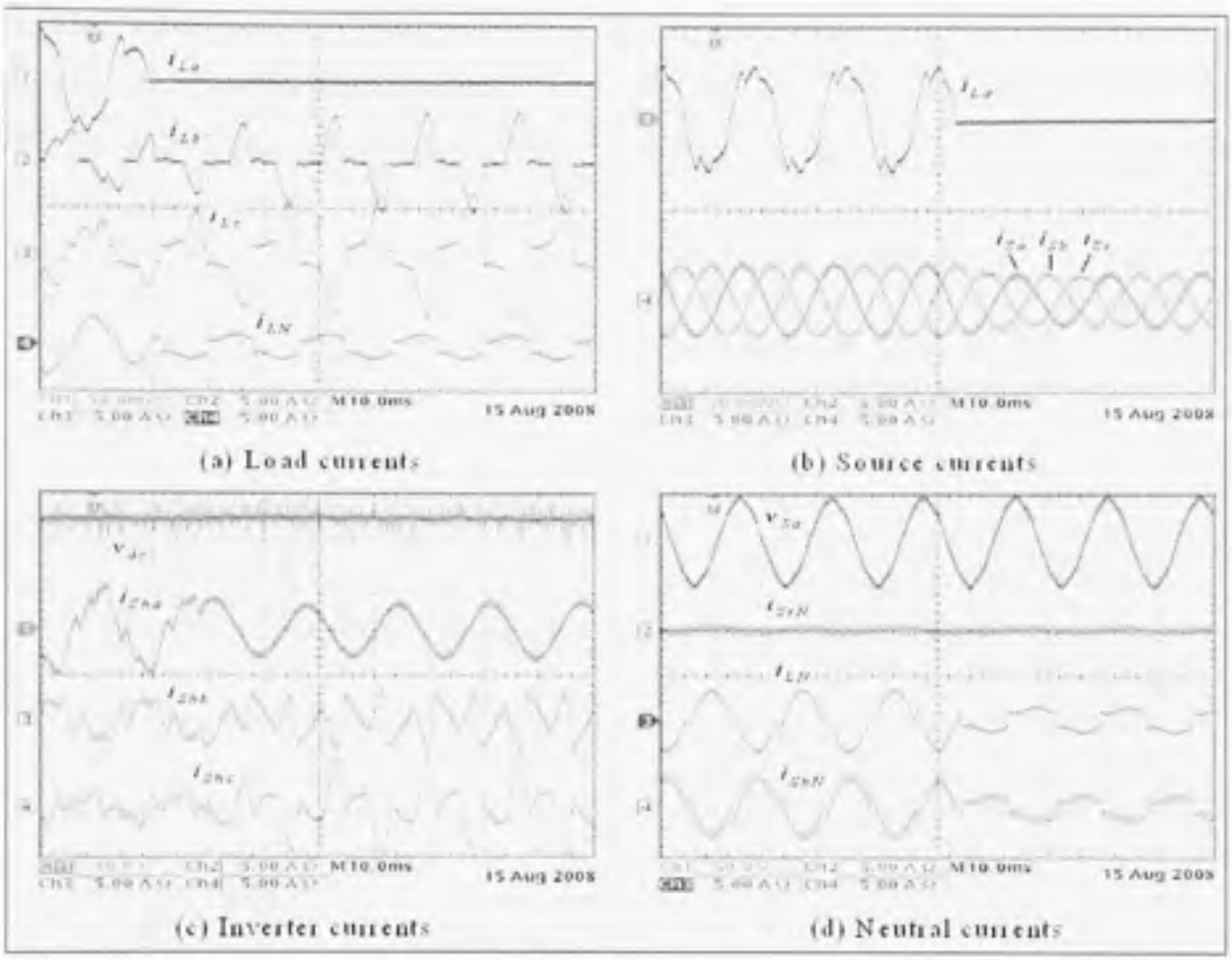

Figure 4.17 Experimental results (dynamic condition): performance of proposed current unbalance compensation approach under sudden occurrence of three-phase to single-phasing condition.

The load and the source current THD spectrums and individual harmonics as percentage of fundamental component are given in Figure 4.18 and Table 4.4, respectively. As noticed from the Figure 4.17 (c), trace-2, to maintain the source currents as perfectly balanced at source side, the shunt inverter draws the sinusoidal current (phase $-a$). In other words, the shunt inverter takes the active power from the source phase $-a$ and supplies to the load through other two phases, such that the entire active power between the source, shunt inverter and the load remains balanced. The DC link voltage remains at constant level during this changeover. The shunt inverter also maintain the transformer neutral point at virtual zero potential.

The above discussion confirms that, during the event of single-phasing, the currents drawn from the supply remain balanced and sinusoidal. Thus, even as load changes from three-phase to single-phase, the relative effect seen from the source side is always three-phase balanced load.

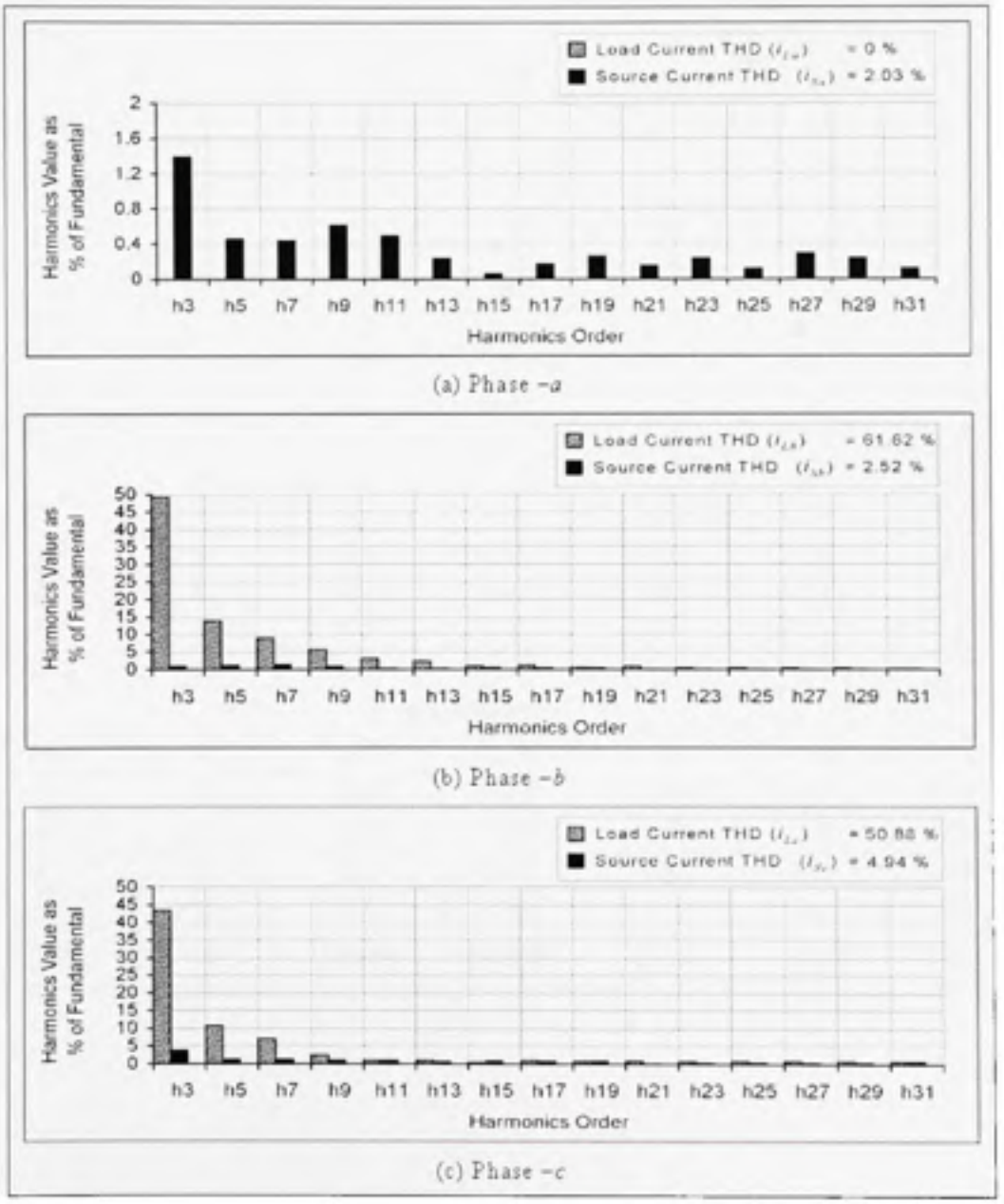

Figure 4.18 Harmonics spectrum of source currents under single-phasing condition.

Table 4.4
Individual harmonics values as % of fundamental (single-phasing condition)

Harmonics	i_{La}	i_{Lb}	i_{Lc}	i_{Sa}	i_{Sb}	i_{Sc}
Odd Harmonics (%)						
3	0	49.27	43.34	1.39	0.96	3.91
5	0	13.76	10.67	0.46	1.11	1.19
7	0	8.91	7.07	0.44	1.33	1.14
9	0	5.68	2.34	0.61	0.88	1.00
11	0	3.03	1.03	0.49	0.31	0.97
13	0	2.39	0.94	0.23	0.20	0.61
15	0	0.98	0.52	0.06	0.57	0.92
17	0	1.17	0.97	0.17	0.4	0.78
19	0	0.57	0.76	0.26	0.37	0.92
21	0	0.84	0.92	0.15	0.17	0.11
23	0	0.48	0.78	0.23	0.17	0.25
25	0	0.41	0.92	0.12	0.14	0.53
27	0	0.41	0.85	0.29	0.09	0.31
29	0	0.38	0.87	0.23	0.14	0.50
31	0	0.24	0.79	0.12	0.23	0.78
Even Harmonics (%)						
DC	0	0.17	0.72	0.96	0.99	1.08
2	0	0.60	0.25	0.58	0.37	0.19
4	0	0.72	0.20	0.09	0.20	0.22
8	0	0.69	0.14	0.20	0.17	0.03
10	0	0.33	0.05	0.17	0.28	0.28
% THD	**0%**	**61.62%**	**50.88%**	**2.03%**	**2.52%**	**4.94%**

4.6 Conclusion

This chapter proposes a novel functionality for UPQC in which it is possible to expand the existing UPQC based 3P3W system to 3P4W and introduces a new current unbalance compensation approach. The proposed 3P4W topology would be very useful to expand the existing 3P3W system to 3P4W system where UPQC is installed to compensate the different power quality problems, which may play an important role in future UPQC based distribution system.

The simulation and the experimental results confirm the utilization of given topology for practical applications. With the proposed approach the unbalance in the source currents is reduced from 45.76% to 1.08%. Moreover, under highly unbalanced (CUF=100%) and distorted (THDs = 61.62% and 50.88%) condition the UPQC strictly maintains the balanced source currents (CUF=2.2%). In all the conditions, the neutral current flowing towards transformer neutral point is maintained at zero value.

CHAPTER 5

UPQC: POWER ANGLE CONTROL – A NOVEL CONTROL PHILOSOPHY

5.1 Introduction

As a thumb rule in all areas of engineering, the proper utilization of the resources that we have, at most efficient way, has lead to great development and is the major concern for most of the engineers in their respective fields. This chapter is an attempt to make use of the existing series inverter to compensate load reactive power by introducing a power angle difference between the source and load voltages. It will eventually result in a better utilization of series inverter. This new reactive power sharing feature between both the inverters would help to reduce the burden on shunt inverter and ultimately result in the reduction of shunt inverter rating to some extend. This new control philosophy is termed as "Power Angle Control (PAC) of Unified Power Quality Conditioner".

The concept of proposed PAC theory is discussed thoroughly and supported by an in depth mathematical analysis. Informative and useful equations are developed to compute the achievable maximum power angle, percentages of load reactive power shared by each of the inverters, percentage of reduction in shunt inverter rating, etc. The most significant factor to implement the PAC approach rely on instantaneous power angle δ determination. A control scheme, based on instantaneous load fundamental active and reactive power extraction, is developed to compute the power angle δ in an instantaneous manner. Once angle δ is known, the required series injection voltage with adequate magnitude and phase angle is generated easily.

The proposed theory is validated through simulation as well as experimental investigation. To show the effect of power angle δ on the shunt inverter rating, several experiments are carried at different power angles.

5.2 Power Angle Control (PAC) of UPQC

This section introduces the fundamental concept of power angle control (PAC) of UPQC (Khadkikar and Chandra, 2008b). The conceptual difference between PAC of UPQC and QVI (CHAPTER 3) of UPQC-Q is also highlighted. This comparison is performed for a better understanding of the working principles of these approaches.

5.2.1 Background and Relevance

The reactive power compensation is one of the most common yet very important issues for power system engineers at transmission as well as at distribution levels. A typical distribution network consists of distribution transformer, motor loads, etc, which demands the reactive power. This load reactive power demand level is mainly affected by the type of loads present on the network. Capacitor banks have been used to compensate the load reactive power demand. It is the simplest and, under certain conditions, an effective way to compensate the load reactive power demand. This traditional approach has certain major disadvantages, such as, fixed compensation, possible occurrence of resonance condition with near by loads, switching transient, bulky size, aging effect, etc.

The rating of shunt inverter/ APF is significantly dependant on the load reactive power needs to be compensated (Khadkikar and Chandra, 2006c). To support the load reactive power demand the shunt inverter/ APF injects a current which is in quadrature with the voltage, in order to avoid the active power involvement in reactive power compensation. The shunt APF has proven its capabilities to compensate the load reactive power even under variable load conditions and the capacitors have successfully being replaced by shunt APFs. At this juncture it is also important to point out that the STATCOM (similar in configuration as shunt APF) are also widely being used to support the reactive power as well as to regulate the load voltage. As the quadrature component requires higher value compared to the in-phase component, the ratings of shunt APFs and STATCOMs are completely determined by its reactive power support. The series inverters/ APFs are not popular to support the load reactive power, as it also involves certain amount of active power too. Another important

issue is that, providing the reactive power through series APF/ inverter under steady-state condition may increase the magnitude of the resultant load voltage. Therefore, to this date, the efforts that have been reported to perform the load reactive power compensation using series APFs/ inverters are not significant.

The most significant advantage of UPQC is that it has two voltage source inverters, where, one is controllerd as variable voltage source (series APF) and other as variable current source (shunt inverter). These back to back connected inverters, if controlled meticulously, can circulate both active as well as reactive powers between themselves. However, on browsing the available literature it is observed that most of the researchers have not tried to project the research work in this direction. Therefore, the load reactive power compensation in most of the UQPC based power quality compensation applications is done by shunt inverter, whereas, the series inverter is generally utilized to overcome the voltage related problems. In a typical distribution system the voltage sag and/or swell, flicker, unbalance, etc., are short duration power quality problems. On the other hand, current harmonics, load reactive power demand, etc., are load dependant issues which are constant for a particular type of load. Hence, the utilization factor of the shunt inverter is much higher than that of the series inverter.

5.2.2 Power Angle Control (PAC) Concept

The voltage sag on the distribution network can be effectively compensated by both the reactive (Basu *et al.*, 2002; Khadkikar *et al.*, 2006e) as well as the active power (Khadkikar and Chandra, 2006b) approaches through UPQC. With the reactive power control approach, the load reactive power can be compensated by a certain percentage along with the voltage sag compensation. In such an approach, the series voltage is injected in such a way that it maintains the quadrature relationship with source current i.e., no active power involvement. But, this approach is effective only during voltage sag on the system. If we inject a series voltage in such a way that it is not at quadrature of source current, it causes a phase angle difference between source voltage and load voltage (termed as power angle) without changing the resultant load voltage magnitude. In that case then a certain amount of reactive

as well as active power would flow through series inverter. This chapter proves that with the proper control of power angle difference between source and load voltage, the series inverter can also help in compensating the load reactive power demand without putting extra active power burden on the source.

Thus, the concept of power angle control of UPQC can be stated as – *"to inject a voltage through series inverter, with proper magnitude and phase angle, such that both the shunt and series inverters will share and support the load reactive power demand, without increase or decrease in the steady-state load voltage magnitude"*

5.2.3 Phasor Representation of PAC

The per phase phasor representation of PAC scheme is shown in Figure 5.1. Considering the source voltage as reference phasor, during normal working condition the source voltage (at the plant input) and the load voltage will be at same magnitude and in-phase as represented by V_S and V_L, respectively. The line impedance is neglected since the UPQC is supposed to be installed at plant vicinity, very close to the loads. For simplicity assuming balanced, harmonic free source voltage without any sag and/or swell condition.

In order to have a phase angle difference between both the voltages, the series inverter should inject the voltage V_{Se} such that the resultant load voltage V'_L will be at desired load voltage magnitude giving δ power angle difference. This causes the load current phasor advancement from I_L to I'_L maintaining the same load phase angle φ_L relationship with load voltage. Therefore, the effective load phase angle with respect to source voltage boosts from φ_L to β, resulting in reduced reactive power handled by shunt inverter. In other words, with δ power angle lead between source and load voltages, the series inverter now generates a certain amount of reactive power. Thus, both the inverters of UPQC now take part in load reactive power compensation.

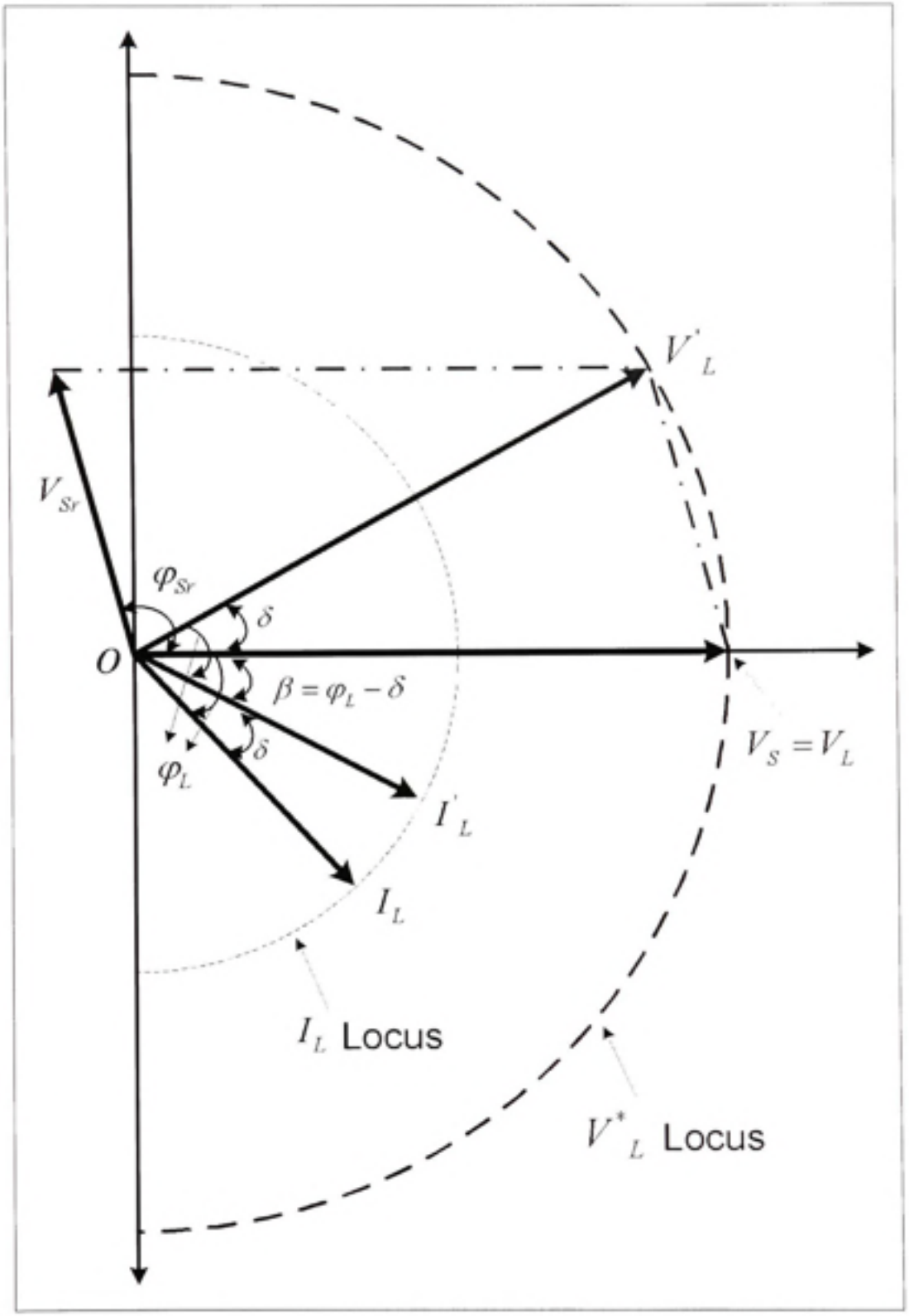

Figure 5.1 Power Angle Control (PAC) concept: phasor representation.

The reactive power shared by both the inverters depends on certain factors and are analyzed in the coming sections. The rating of series inverter is first defined based on the sensitive load requirements. Based on the series inverter rating, the maximum possible power angle lead δ_{max} that could be achieved, without affecting its rating is computed. This δ_{max} gives the maximum amount of reactive power that the series inverter can share. Thus, this analysis promises "no" additional burden on series inverter rating. This results in the better utilization of the existing series inverter at a reduced shunt inverter rating, i.e., reduction in the overall UPQC cost and the better device utilization.

5.3 Mathematical Formulation of PAC

In order to implement the PAC approach in practical application it is necessary to estimate the power angle δ between source and load voltages, based on load reactive power demand, but in instantaneous manner. In this chapter, a simple method is proposed for instantaneous δ angle determination and discussed later in section 5.5. At first, let's assume that PAC gives a power angle difference δ. The boundary condition for maximum δ_{max} lead that can be achieved with PAC, without affecting series inverter rating, is also presented later in the section 5.3.3.

5.3.1 Series Inverter Parameter Estimation

Figure 5.2 shows the detailed phasor representation for required series voltage injection estimation, where, k represents the peak value of desired load voltage, which is a known quantity.

During steady-state condition,

$$|V_S'| = |V_L| = |V_L'| = k \tag{5.1}$$

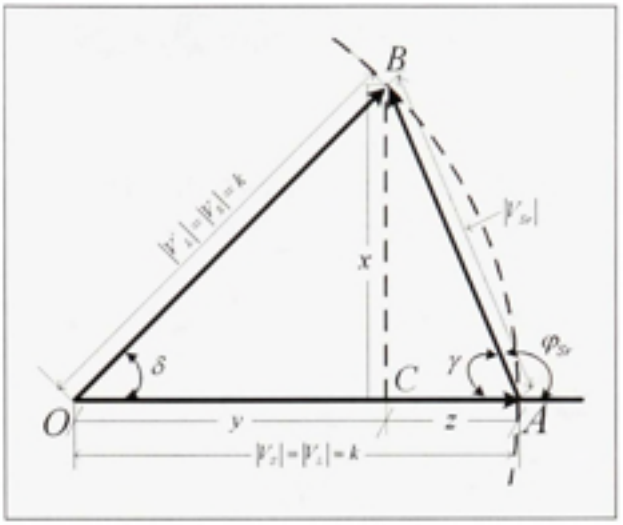

Figure 5.2 Determination of V_{Sr} and φ_{Sr}.

From ΔOCB (Figure 5.2)

$$\sin\delta = \frac{x}{k} \tag{5.2}$$

$$x = k.\sin\delta \tag{5.3}$$

$$y = k.\cos\delta \tag{5.4}$$

From Isosceles ΔOAB,

$$OA = k = y + z \tag{5.5}$$

$$z = k - k.\cos\delta \tag{5.6}$$

$$z = k.(1 - \cos\delta) \tag{5.7}$$

From ΔABC,

$$|V_{Sr}| = \sqrt{x^2 + z^2} \tag{5.8}$$

$$|V'_{Se}| = \sqrt{(k.\sin\delta)^2 + (k.(1-\cos\delta))^2} \tag{5.9}$$

$$|V'_{Se}| = k.\sqrt{(\sin\delta)^2 + (1-\cos\delta)^2} \tag{5.10}$$

$$|V'_{Se}| = k.\sqrt{\sin^2\delta + 1 - 2.\cos\delta + \cos^2\delta} \tag{5.11}$$

$$|V'_{Se}| = k.\sqrt{2 - 2.\cos\delta} \tag{5.12}$$

$$|V'_{Se}| = k.\sqrt{2}.\sqrt{1-\cos\delta} \tag{5.13}$$

$$\text{Now,} \quad \angle CAB = \gamma = \tan^{-1}\left(\frac{x}{z}\right) \tag{5.14}$$

$$\gamma = \tan^{-1}\left(\frac{k.\sin\delta}{k.(1-\cos\delta)}\right) \tag{5.15}$$

$$\gamma = \tan^{-1}\left(\frac{\sin\delta}{1-\cos\delta}\right) \tag{5.16}$$

$$\text{Therefore,} \quad \angle\varphi_{Se} = 180^0 - \angle\gamma \tag{5.17}$$

The equations (5.13) and (5.17) give the required magnitude and phase angle, respectively; at which the series voltage should be injected in order to achieve δ power angle lead such that the amplitude of V''_L will be at desired value. For a definite value of k, series injected voltage only depends on the power angle δ.

5.3.2 Shunt Inverter Parameter Estimation

Figure 5.3 represents the phasor diagram for different currents due to the δ power angle advancement. Without PAC, the load reactive power demand is fulfilled by shunt inverter alone by injecting the shunt compensating current I_{Sh}. With PAC, the load current phasor is shifted to I'_L. The effective phase angle β between source voltage and load current suggests that the reactive power demand seen from the source side gets reduced. The shunt inverter should now inject the compensating current I'_{Sh} in such a way that no extra active power should be taken from the source during this operating period, i.e. the source current I_S should be the same as that of one without PAC approach. Figure 5.4 depicts the detailed phasor representation to determine the shunt compensating current (I'_{Sh}) and its phase angle (φ'_{Sh_L}) with respect to resultant load voltage (V''_L).

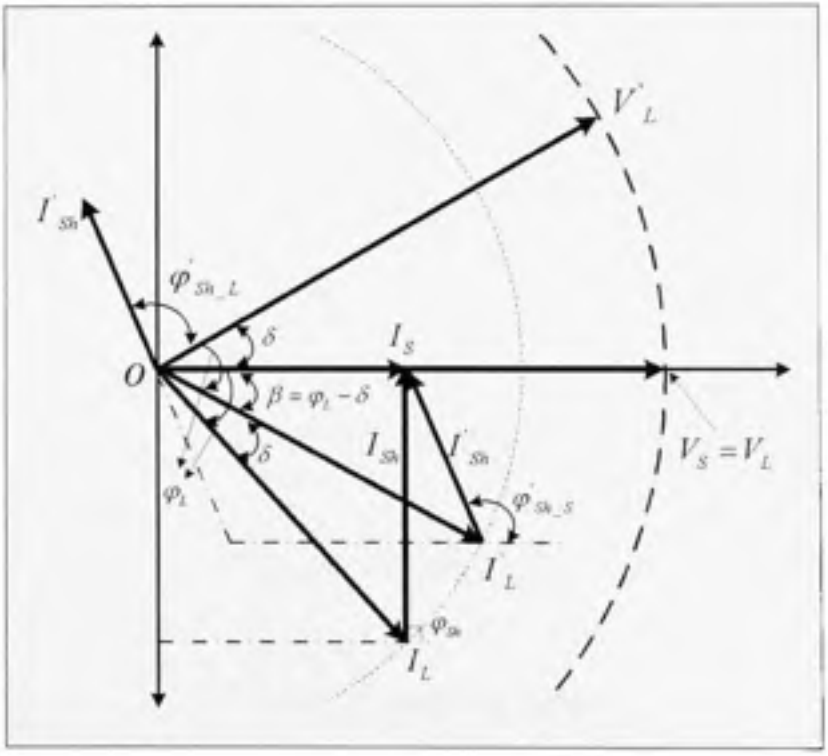

Figure 5.3 Power Angle Control: current phasor representation.

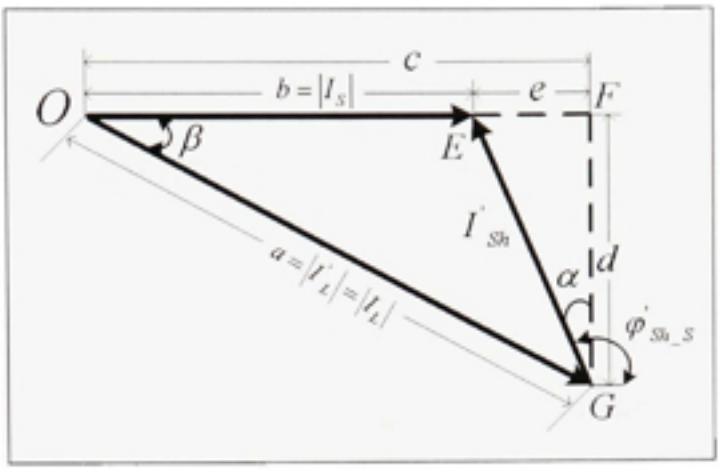

Figure 5.4 Determination of I'_{Sh} and φ'_{Sh_S}.

From Figure 5.4,

$$\beta = \phi_L - \delta \tag{5.18}$$

In ΔOGF ,

$$\cos\beta = \frac{OF}{OG} \tag{5.19}$$

$$OF = c = |I'_L|.\cos\beta \tag{5.20}$$

$$GF = d = |I'_L|.\sin\beta \tag{5.21}$$

$$EF = e = |I'_L|.\cos\beta - |I_S| \tag{5.22}$$

$$EF = e = |I'_L|.\cos\beta - |I_L|.\cos\varphi_L \tag{5.23}$$

$$EF = e = |I'_L|.[\cos\beta - \cos\varphi_L] \tag{5.24}$$

$$|I'_{Sh}| = EG = \sqrt{e^2 + d^2} \tag{5.25}$$

$$|I'_{Sh}| = \sqrt{\{|I'_L|.[\cos\beta - \cos\varphi_L]\}^2 + \{|I'_L|.\sin\beta\}^2} \tag{5.26}$$

$$|I'_{Sh}| = |I'_L|.\sqrt{1 + \cos^2\varphi_L - 2.\cos\beta.\cos\varphi_L} \tag{5.27}$$

$$\text{Now, } \tan\alpha = \frac{e}{d} \tag{5.28}$$

$$\angle\alpha = \tan^{-1}\left(\frac{|I'_L|.[\cos\beta - \cos\varphi_L]}{|I'_L|.\sin\beta}\right) \tag{5.29}$$

$$\angle\alpha = \tan^{-1}\left(\frac{\cos\beta - \cos\varphi_L}{\sin\beta}\right) \tag{5.30}$$

$$\text{Therefore, } \angle\varphi'_{Sh\_S} = \angle\alpha + 90^0 \tag{5.31}$$

$$\angle\varphi'_{Sh\_L} = \angle\alpha + 90^0 - \delta \tag{5.32}$$

The equations (5.27)and (5.32) give the required magnitude and phase angle of shunt compensating current in order to achieve desired operation.

Figure 5.3 and Figure 5.4,

$$\text{Net Reduction in } I_{Sh} \text{ Magnitude} = |I_{Sh}| - |I'_{Sh}| \tag{5.33}$$

$$\text{Therefore, net reduction in shunt inverter kVA rating} = |I'_L|.(|I_{Sh}| - |I'_{Sh}|) \times 1e-3 \tag{5.34}$$

$$= |V_L'| . |I_L| . (\sin\varphi_L - \sqrt{1 + \cos^2\varphi_L - 2.\cos\beta.\cos\varphi_L}) \times 1e-3 \quad (5.35)$$

Therefore, Net Reduction in shunt inverter kVA rating as % of full load kVA rating,

$$= (\sin\varphi_L - \sqrt{1 + \cos^2\varphi_L - 2.\cos\beta.\cos\varphi_L}) \times 1e-1\ \% \quad (5.36)$$

Equation (5.36) gives the net reduction in kVA rating of shunt inverter as percentage of the full load kVA rating with PAC scheme, without affecting the existing series inverter rating, discussed in next subsection. Equations (5.13), (5.17), (5.27), and (5.32) are performance equations of PAC approach. The effectiveness of this approach is completely governed by proper reference signal generation based on these quantities, in real time without delay in computation. For a particular load condition, the load parameters I_L and φ_L are constant; hence, these equations show that the PAC approach is independent of other network parameters. This results in a highly robust and parameter insensitive approach to compensate the load reactive power demand by utilizing both the shunt and series inverters simultaneously.

5.3.3 Boundary Condition for Maximum δ

The rating of series part of UPQC is mainly governed by percentage of sag that need to be compensated. If the maximum voltage that can be injected through series inverter is denoted by $V_{sr,max}$ and the percentage of this maximum voltage limit in terms of desired load voltage by factor K_{sr}, then we can write,

$$S_{Series\_APF} = V_{Sr,max}.I_S^* \quad (5.37)$$

$$\text{From (5.13)}, \ |V_{Sr,max}| = k.\sqrt{2}.\sqrt{1-\cos\delta_{max}} \quad (5.38)$$

$$K_{Sr}.k = k.\sqrt{2}.\sqrt{1-\cos\delta_{\max}} \quad \left(\text{since, } K_{Sr} = \frac{|V_{Sr,\max}|}{k}\right) \tag{5.39}$$

$$K_{Sr} = \sqrt{2}.\sqrt{1-\cos\delta_{\max}} \tag{5.40}$$

$$\delta_{\max} = \cos^{-1}(1-\frac{K^2_{Sr}}{2}) \tag{5.41}$$

For a particular application in which UPQC is to be installed, the series inverter rating is known. Utilizing (5.41) we can calculate the maximum power angle δ_{max} that can be achieved without affecting the existing series inverter rating. Thus, δ_{max} limit will guarantee the reactive power sharing feature without overloading the series inverter, and hence, no extra series inverter cost addition.

5.4 Active and Reactive Power (P-Q) Flow

This section gives the per phase active and reactive power flow between shunt and series inverters.

5.4.1 P-Q Flow without PAC Approach

For series inverter,

$$P_{Sr} = V_{Sr}.I_S.\cos\varphi_{Sr} \tag{5.42}$$

$$Q_{Sr} = V_{Sr}.I_S.\sin\varphi_{Sr} \tag{5.43}$$

For shunt inverter,

$$P_{Sh} = V_L.I_{Sh}.\cos\varphi_{Sh} = k.I_{Sh}.\cos\varphi_{Sh} \tag{5.44}$$

$$Q_{Sh} = V_L.I_{Sh}.\sin\varphi_{Sh} = k.I_{Sh}.\sin\varphi_{Sh} \tag{5.45}$$

The shunt inverter supplies all the load reactive power demand by injecting 90^0 leading shunt compensating current I_{Sh}.

$$\therefore \; P_{Sh} = 0 \tag{5.46}$$

$$Q_{Sh} = V_L.I_{Sh} = k.I_{Sh} \tag{5.47}$$

5.4.2 P-Q Flow with PAC Approach

With PAC of UPQC, both active as well as reactive power will flow through the series inverter and they are computed as follow,

$$P_{Sr} = \left(I_S.k.\sqrt{2}.\sqrt{1-\cos}\right).\cos\varphi_{Sr} \tag{5.48}$$

$$P_{Sr} = \left(\sqrt{2}.I_S.k.\sqrt{1-\cos\delta}\right).\cos(180^0-\gamma) \tag{5.49}$$

$$P_{Sr} = -\left(\sqrt{2}.I_S.k.\sqrt{1-\cos\delta}\right).\cos\gamma \tag{5.50}$$

$$P_{Sr} = -\left(\sqrt{2}.I_S.k.\sqrt{1-\cos\delta}\right).\frac{\sqrt{1-\cos\delta}}{\sqrt{2}} \tag{5.51}$$

$$P_{Sr} = -I_S.k.(1-\cos\delta) \tag{5.52}$$

The negative sign in (5.52) implies that during power angle control of UPQC, the series inverter consumes certain amount of active power. Due to this active power the DC link voltage can be increased. To maintain the DC link voltage at the constant level, the shunt

inverter should now inject the compensating current in such a way that the extra active power should be fed back to the supply side, i.e. should circulate between the series and shunt active inverters through the DC link. Thus, in an ideal condition without any losses, the active power consumed by series inverter should be equal to the active power fed back by the shunt inverter and hence, the source current would be at a constant level. In actual practice there can be a slight increase in the source current magnitude due to the losses associated with both the inverters, DC link, coupling inductances and series transformer.

$$Q_{Sr} = \left(\sqrt{2}.I_S.k.\sqrt{1-\cos\delta}\right).\sin(180^0 - \gamma) \tag{5.53}$$

$$Q_{Sr} = \left(\sqrt{2}.I_S.k.\sqrt{1-\cos\delta}\right).\sin\gamma \tag{5.54}$$

$$Q_{Sr} = \left(\sqrt{2}.I_S.k.\sqrt{1-\cos\delta}\right).\frac{\sin\delta}{\sqrt{2}.\sqrt{1-\cos\delta}} \tag{5.55}$$

$$Q_{Sr} = I_S.k.\sin\delta \tag{5.56}$$

From (5.56), the reactive power injected by series inverter mainly depends on the power angle δ. Higher the value of δ, higher will be the reactive power compensation through series inverter, but at the same time higher will be the magnitude of series injected voltage by (5.13).

For shunt inverter,

$$P'_{Sh} = V''_L.I'_{Sh}.\cos\varphi'_{Sh\_L} = k.I'_{Sh}.\cos\varphi'_{Sh\_L} \tag{5.57}$$

$$Q'_{Sh} = V''_L.I'_{Sh}.\sin\varphi'_{Sh\_L} = k.I'_{Sh}.\sin\varphi'_{Sh\_L} \tag{5.58}$$

$$\text{At all condition, } Q_L = Q_{Se} + Q'_{Sh} \tag{5.59}$$

5.4.3 Percentage of Reactive Power Shared by Two Inverters

The reactive power supplied by the series inverter as % of total load reactive power demand can be expressed as:

$$\%\, Q_{Series} = \frac{Q_{Se}}{Q_L} \times 100\% \tag{5.60}$$

$$= \frac{|I_S|.k.\sin\delta}{|I'_L|.k.\sin\phi_L} \times 100\% \tag{5.61}$$

$$= \frac{|I_S|.\sin\delta}{|I'_L|.\sin\phi_L} \times 100\% \tag{5.62}$$

$$= \frac{|I_L|.\cos\phi_L.\sin\delta}{|I'_L|.\sin\phi_L} \times 100\% \tag{5.63}$$

$$= \frac{\cos\phi_L}{\sin\phi_L}.\sin\delta \times 100\% \tag{5.64}$$

$$\text{Therefore, } \%\, Q_{Series} = \frac{\sin\delta}{\tan\phi_L} \times 100\% \tag{5.65}$$

Similarly, the reactive power supplied by shunt inverter as % of total load reactive power demand can be expressed as:

$$\%\, Q_{Shunt} = \frac{Q'_{Sh}}{Q_L} \times 100\% \tag{5.66}$$

$$= \frac{|I_S|.k.\sin\phi'_{Sh\_L}}{|I'_L|.k.\sin\phi_L} \times 100\% \tag{5.67}$$

$$= \frac{\left(|I'_L|\sqrt{1+\cos^2\phi_L - 2.\cos\beta.\cos\phi_L}\right).\sin\phi'_{Sh\_L}}{|I'_L|.\sin\phi_L} \times 100\% \tag{5.68}$$

$$\text{Therefore, } \%\, Q_{Shunt} = \frac{\left(\sqrt{1+\cos^2\phi_L - 2.\cos\beta.\cos\phi_L}\right).\sin\phi'_{Sh\_L}}{\sin\phi_L} \times 100\% \tag{5.69}$$

5.5 Power Angle δ Determination

This section describes the procedure and steps involved to determine the power angle δ in real-time. As mentioned in section 5.3.3 and using (5.41), the theoretical value of maximum δ that can be achieved for a given UPQC system is determined. This δ_{max} is calculated based on the series inverter rating. Using (5.56), the theoretical value of maximum reactive power that the series inverter can support without additional increase in its own ratings can be computed as:

$$Q_{Sr\_max} = I_S.k.\sin\delta_{max} \tag{5.70}$$

Let Q_{L_max} be the maximum load reactive power demand that UPQC should supply. This load reactive power demand will be shared by series and shunt inverters. Knowing the maximum reactive power shared by series inverter by (5.70), we can fix the reactive power handled by shunt inverter, as Q_{Sh_max}.

$$\therefore\ Q_{Sh\_max} = Q_{L\_max} - Q_{Sr\_max} \tag{5.71}$$

Since, we know the theoretical maximum value of reactive power that the shunt inverter should supply, the next step is to determine the instantaneous value of reactive power that the series inverter can handle. If the load reactive power demand is less than Q_{Sh_max}, the shunt

inverter should compensate this reactive power alone. In such cases the series inverter should not take part in reactive power compensation. At a given time, if the load reactive power demand increases above $Q_{Sh,max}$ limit, the series inverter should now take part in load reactive power compensation.

$$Q_{Sr} = Q_L - Q_{Sh,max} = I_S.k.\sin\delta \tag{5.72}$$

In the above equation, $Q_{Sh,max}$ is a constant value as fixed by (5.71).The instantaneous value of Q_L can be computed (discussed later in the section 5.6.1), and thus the instantaneous value of Q_{Sr} can be known.

$$\text{Therefore, from (5.72), } \sin\delta = \frac{Q_{Sr}}{I_S.k} \tag{5.73}$$

$$\sin\delta = \frac{Q_{Sr}}{S_S} \tag{5.74}$$

Since, the shunt inverter supports the load reactive power demand; the source supplies only the active part of load power demand. Thus, the apparent power in (5.74) can be replaced by the active power supplied by the source (P_S).

$$\therefore\ \delta = \sin^{-1}\left(\frac{Q_{Sr}}{P_S}\right) = \sin^{-1}\left(\frac{Q_{Sr}}{P_L}\right) \tag{5.75}$$

The source should supply only the load active power demand as the load reactive power demand will be shared by both the inverters. Interestingly, the δ determination is based on two important parameters, the actual (instantaneous) load reactive power demand and the actual (instantaneous) load/source fundamental active power. Thus, from equation (5.72) to (5.75), if we could extract the load active as well as reactive power demands instantaneously, δ can be estimated accordingly in instantaneous manner. Figure 5.5 gives the flow chart for the above discussed steps to determine the δ in actual practical systems.

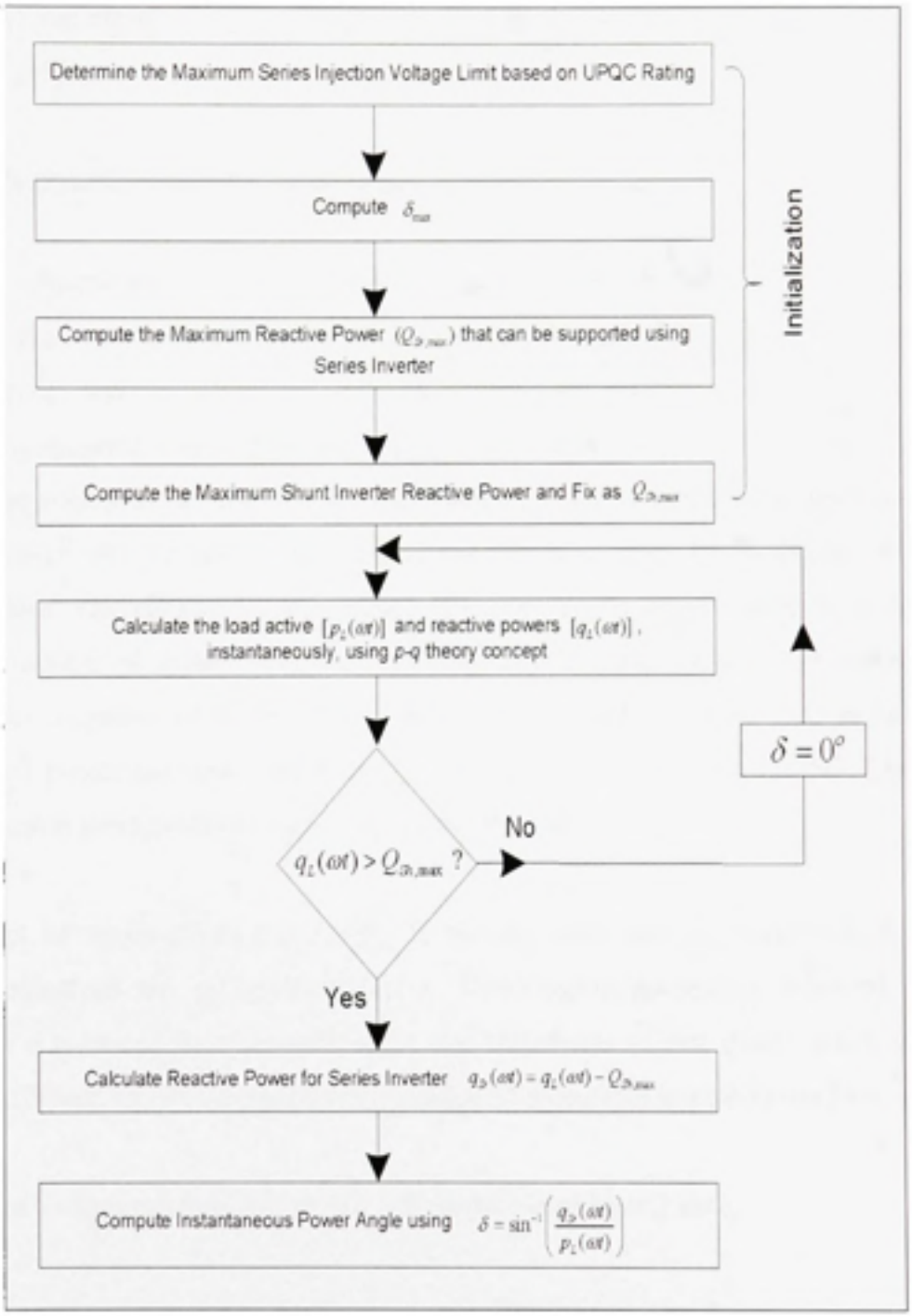

Figure 5.5 Flow chart of steps involved in determination of δ in actual practical applications.

5.6 UPQC Controller Development based on PAC

This section describes the generation of the reference signals for both series and shunt inverters of UPQC.

5.6.1 Instantaneous δ Determination

The load on a particular plant where UPQC is to be installed may not be constant all the time. The load reactive power demand, therefore, can vary based on the plant loads. As discussed in the previous section, when the load reactive power demand is well within the shunt inverter compensation limits, the series inverter should not act (i.e. $\delta=0^{o}$). Now, if the plant load changes such that the load reactive power demand exceeds the shunt inverter maximum limit, the series inverter should act immediately to take over the additional load reactive power demand. Therefore, the performance of power angle control approach solely depends on the extraction of power angle δ in real-time. In this section, the instantaneous δ determination is proposed by extracting instantaneous load active as well as instantaneous load reactive power demand. The single-phase *p-q* theory (Liu *et al.*, 1999; Haque, 2002) based concept is used to achieve the aforementioned task.

The concept of single-phase *p-q* theory is already discussed in chapter 4. Some of the important equations are re-emphasized here. This chapter assumes a balanced three-phase system. For a balanced three-phase system, the knowledge of one phase active and reactive power is sufficient for the determination of required quantities to realize the PAC approach.

Phase-*a* load voltage representation in $\alpha - \beta$ co-ordinates by $\pi/2$ lead,

$$\begin{bmatrix} v_{La,\alpha} \\ v_{La,\beta} \end{bmatrix} = \begin{bmatrix} v_{La}(\omega t) \\ v_{La}(\omega t + \pi/2) \end{bmatrix} = \begin{bmatrix} V_{Lm}\sin(\omega t) \\ V_{Lm}\cos(\omega t) \end{bmatrix} \tag{5.76}$$

Similarly, for Phase-a load current,

$$\begin{bmatrix} i_{La,\alpha} \\ i_{La,\beta} \end{bmatrix} = \begin{bmatrix} i_{La}(\omega t + \varphi L) \\ i_{La}(\omega t + \varphi L) + \pi/2 \end{bmatrix} \tag{5.77}$$

The per phase instantaneous load active and instantaneous load reactive power can be represented by,

$$\begin{bmatrix} p_L \\ q_L \end{bmatrix} = \begin{bmatrix} v_{La,\alpha} & v_{La,\beta} \\ -v_{La,\beta} & v_{La,\alpha} \end{bmatrix} \cdot \begin{bmatrix} i_{La,\alpha} \\ i_{La,\beta} \end{bmatrix} \tag{5.78}$$

The p_L and q_L can be expressed as,

$$p_{La} = \overline{p}_{La} + \tilde{p}_{La} \tag{5.79}$$

$$q_{La} = \overline{q}_{La} + \tilde{q}_{La} \tag{5.80}$$

Where, $\overline{p}_{La}$ and $\overline{q}_{La}$ represent the DC components that are responsible for fundamental load active and reactive power, whereas, $\tilde{p}_{La}$ and $\tilde{q}_{La}$ represent the AC components that are responsible for harmonic powers. The per phase fundamental instantaneous load active and fundamental instantaneous load reactive power can be extracted from p_L and q_L, respectively, by using a low pass filter (LPF). Once these quantities are known, the instantaneous power angle δ can be determined easily by using (5.75). The instantaneous δ determination block diagram is shown in Figure 5.6. Here, the care is taken to compute the power angle δ only when $\overline{q}_{La} > Q_{Sh,\max}$ (not shown in the figure).

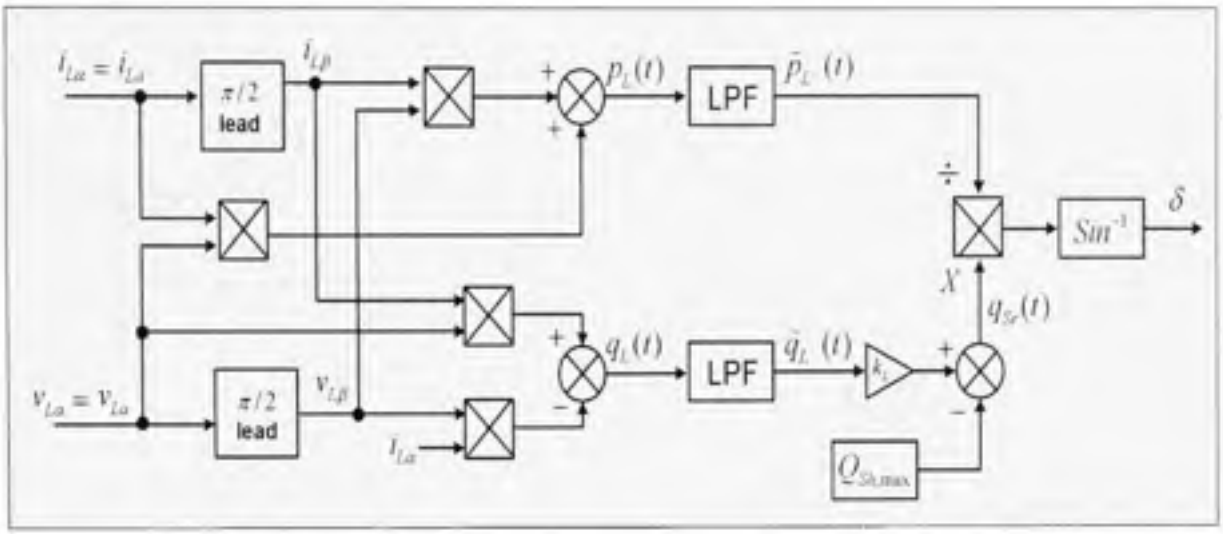

Figure 5.6 Instantaneous power angle δ determination.

5.6.2 Reference Voltage Signal Generation for Series Inverter

Figure 5.7 shows the series injected voltage reference signals generation utilizing determined instantaneous δ angle. With standard mathematical computation the required series injected voltage magnitude and its phase angle are calculated as given by (5.13) and (5.17), respectively. These computations are based on peak values.

To generate a time varying, 60 Hz sinusoidal signal with estimated phase angle φ_{Sr}, the Matlab *s-function* blocks are utilized. The *sin* and *cos* signals, at unity magnitude, from the PLL are used to maintain synchronization between the generated reference signal and the supply voltage. This signal multiplied with computed series voltage magnitude V_{Sr} gives the required series injected voltage signal with desired phase angle shift. Similarly, with ± 120° phase angle difference the reference signals for other two phases are generated. These three reference series injected voltages are compared with sensed three phase series injected voltages and the errors are then processed by PWM controller to generate the required switching signals for series inverter switches.

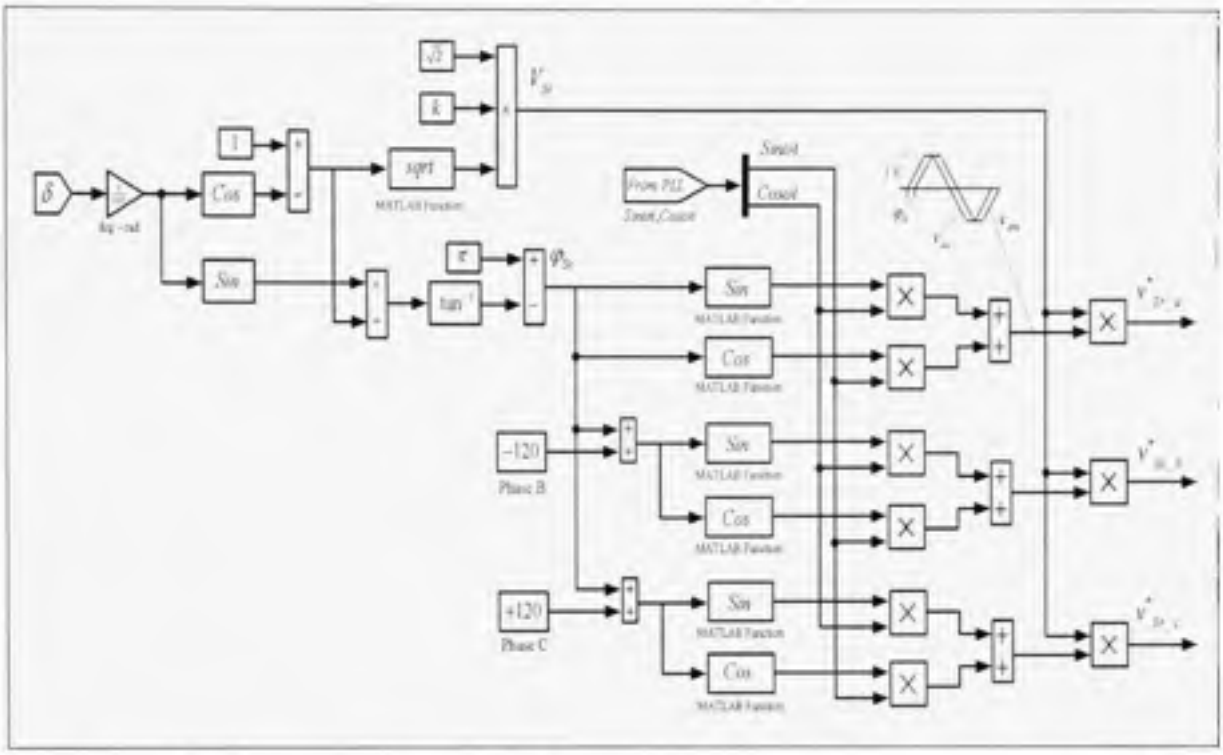

Figure 5.7 Reference voltage signal generation for series inverter based on PAC approach.

5.6.3 Reference Current Signal Generation for Shunt Inverter

The shunt inverter is used to compensate the current harmonics, current unbalance, reactive current and to maintain the DC link voltage at the constant level. Instead of calculating the shunt injected current magnitude and its phase angle, an alternative approach is used for shunt part. In this approach reference source currents are generated directly. This indirect control of shunt compensating currents also helps to compensate the harmonics generated by the loads, if any. Therefore, there is no necessity for the load current harmonics to be extracted. The other reason behind this consideration is to utilize the already calculated parameters for instantaneous δ determination such as $v_{L\alpha}$, $v_{L\beta}$ & $\bar{p}_L(t)$, and hence to reduce the overall controller complexity and computation time. Thus, the reference source current signals can be generated by utilizing the instantaneous load active power as discussed below.

Using (5.78) and (5.79),

$$\begin{bmatrix} i^{*}_{L\alpha,\alpha} \\ i^{*}_{L\alpha,\beta} \end{bmatrix} = \begin{bmatrix} v_{L\alpha,\alpha} & v_{L\alpha,\beta} \\ -v_{L\alpha,\beta} & v_{L\alpha,\alpha} \end{bmatrix}^{-1} \cdot \begin{bmatrix} \overline{p}_{L} \\ 0 \end{bmatrix} \tag{5.81}$$

$$i^{*}_{L\alpha}(\omega t) = \frac{1}{Ax} \cdot v_{L\alpha}(\omega t) \cdot [\overline{p}_{L}(\omega t)] \tag{5.82}$$

$$\text{Where, } Ax = v^{2}_{L\alpha,\alpha} + v^{2}_{L\alpha,\beta} \tag{5.83}$$

Equation (5.82) gives the load current corresponding to the fundamental load active power. As discussed, PAC approach gives a power angle δ boost between resultant load voltage and source voltage, maintaining the same voltage magnitudes. The load phase angle between $v_{L,abc}$ & $i_{L,abc}$ and $v'_{L,abc}$ & $i'_{L,abc}$ is constant, but, the phase angle between the resultant load current $i'_{L,abc}$ *w.r.t.* source voltage is now boosted to β (Figure 5.1). Therefore, in order to supply only required fundamental load active power, the active power demand seen from the source side should be equal to the power given in (5.82) plus losses associated with UPQC ($\overline{p}_{dc}$).

The term Ax, in steady-state condition, gives a constant DC value. Now, if we replace the load voltage signals in (5.82) with actual source voltage signals, since, both the voltages have the same magnitude, the reference signals for source currents can be determined easily. This is done to maintain the synchronism between the reference source current and the actual voltage to achieve unity power factor operation.

$$\text{Therefore, } \quad i^{*}_{Sa}(\omega t) = \frac{v_{Sa}(\omega t)}{Ax} \cdot [\overline{p}_{L}(\omega t) + \overline{p}_{dc}(\omega t)] \tag{5.84}$$

$$i^{*}_{Sb}(\omega t) = \frac{v_{Sb}(\omega t)}{Ax} \cdot [\overline{p}_{L}(\omega t) + \overline{p}_{dc}(\omega t)] \tag{5.85}$$

$$i^{*}_{Sk}(\omega t) = \frac{v_{Sk}(\omega t)}{\Delta x}.[\bar{p}_{L}(\omega t) + \bar{p}_{dc}(\omega t)] \tag{5.86}$$

The above equations give the reference source current signals that would supply only fundamental load active power demand and losses associated with UPQC. The block diagram for reference source current signals generation is shown in Figure 5.8. For unbalanced load, each phase should be tackled separately and the current unbalance compensation approach proposed in CHAPTER 4 can be utilized. The overall block diagram of power angle contol of UPQC is shown in Figure 5.9.

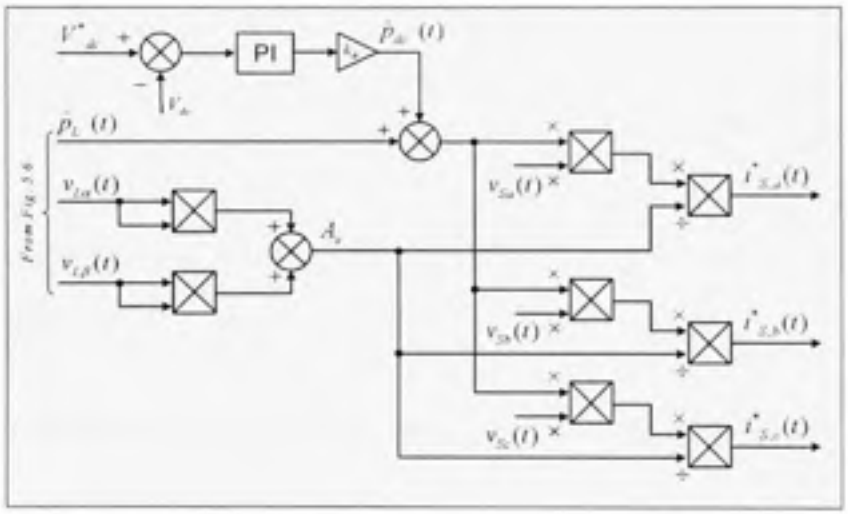

Figure 5.8 Reference current signal generation based on PAC approach.

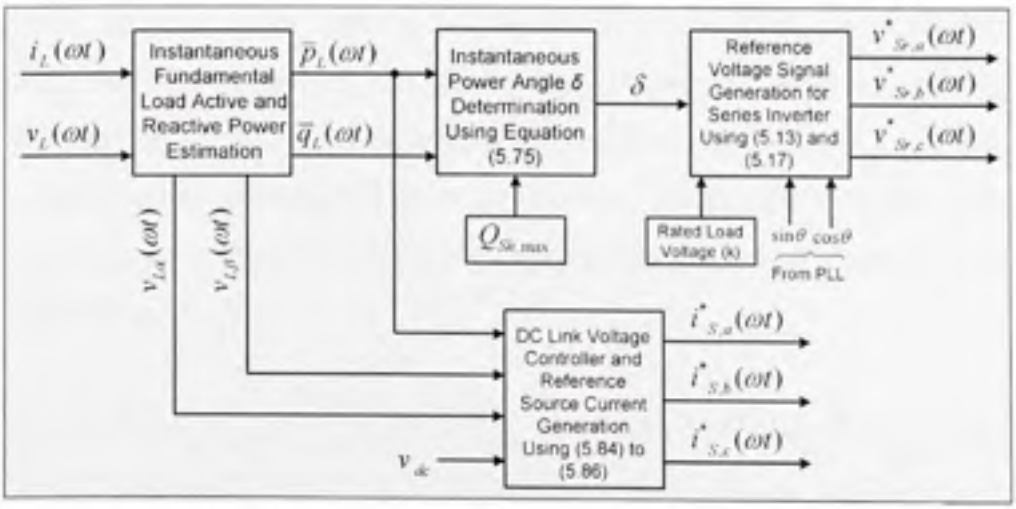

Figure 5.9 Overall control block diagram of proposed PAC approach.

5.7 Simulation Results

The reactive power sharing feature of both the inverters of UPQC has been evaluated by digital simulation. The load is assumed to be highly inductive to have a better visualization of the results. The supply voltage which is available at the UPQC terminal is considered as three phase, 60 Hz, 600 V (line to line) with the maximum load power demand of 15 kW + j 15 kVAR (load power factor angle of 0.707 lagging). The maximum voltage that can be injected by the series inverter is assumed to be 40 % of the rated input voltage (k_{Sr}=0.4). This gives the δ_{max}= 23.07^0 by (5.41). With the given maximum load active power demand (15 kW, I_s = 20.5A rms) and by (5.70), the maximum reactive power that the series inverter can inject, without affecting it's rating is approximately 1.96 kVARs per phase or 5.8 kVARs of total load kVARs. Here, the maximum kVAR that the series inverter should compensate is considered as 5.7 kVAR, thus, using (5.71), the maximum kVAR compensation limit for shunt inverter is fixed as 9.3 kVARs of total load kVAR demand. In the following sections the simulation results for load reactive power compensation using basic UPQC operation and proposed PAC approach are discussed.

5.7.1 Load Reactive Power Compensation without PAC Approach

Figure 5.10 (a) – (h) shows the simulation results during normal working condition without PAC approach. At the onset, only a pure resistive load (15 kW) is considered on the system. At time t1=0.1 sec, the shunt inverter is put into the operation. The DC link feedback controller acts immediately forcing DC link voltage to settle down at set reference voltage, here 725 V by taking the fundamental current from the source. Within a cycle the DC link voltage is maintained at the constant level, as shown in the Figure 5.10 (d). At time t2=0.2 sec, the series inverter is put into operation such that both series and shunt inverters are now operating together as UPQC.

During this time interval since there is no reactive load on the network, the shunt inverter does not inject any compensating current. At time t3=0.3 sec, the maximum plant load i.e. 15 kW + j15 kVAR is switched ON. The shunt inverter now injects a 90^0 leading compensating

current and supplies the load VARs, making the input power factor to unity. The source current waveform and the shunt compensating current waveform are shown in Figure 5.10 (e) and (g), respectively.

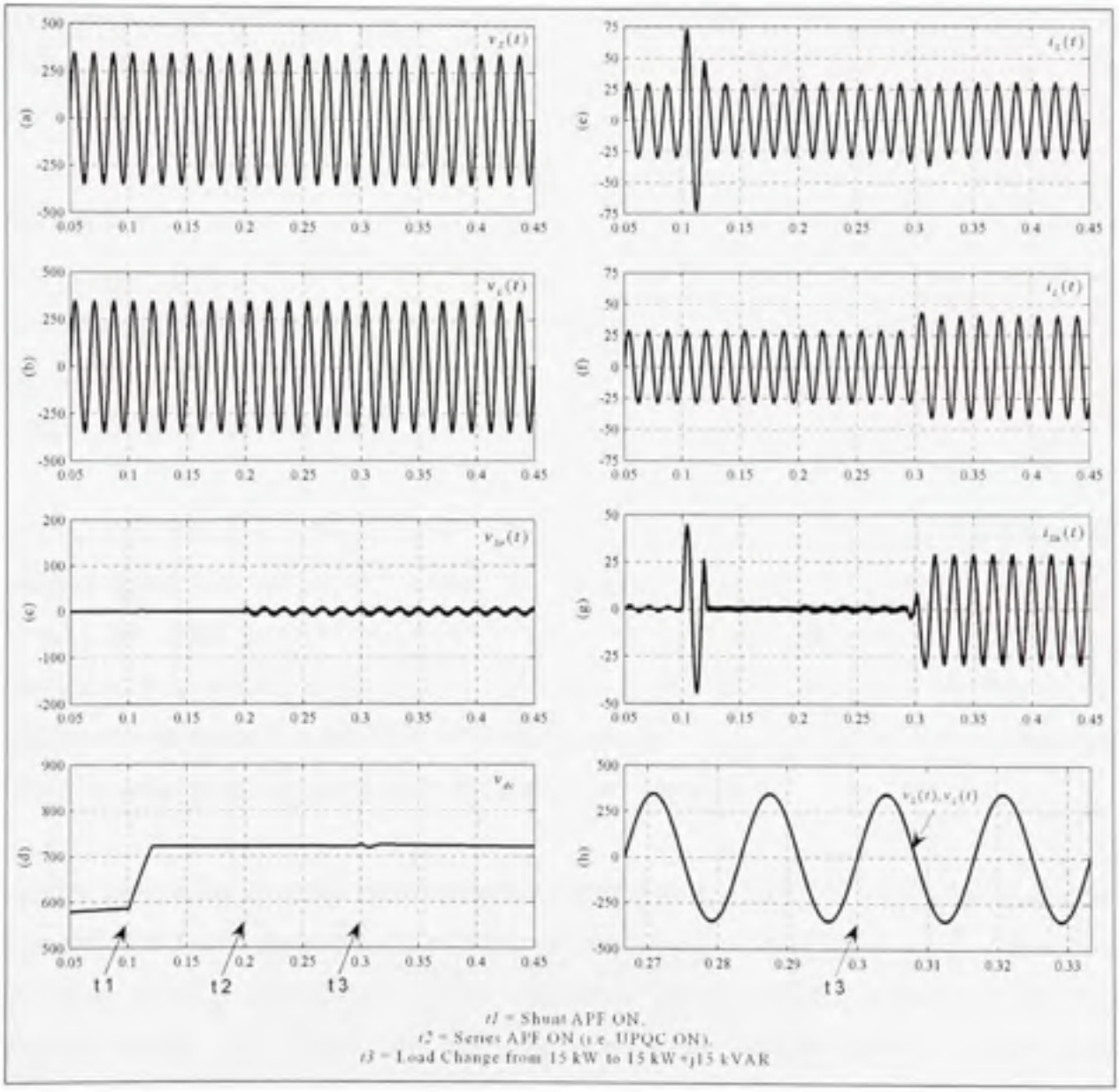

Figure 5.10 Simulation results: load reactive power compensation without PAC of UPQC.

5.7.2 Load Reactive Power Compensation with PAC Approach

The simulation results during proposed PAC of UPQC are shown in Figure 5.11. There are four different operating conditions to visualize the effectiveness of the proposed approach. Further, for better understanding, the load active power demand is kept constant during all operating conditions at 15 kW and only reactive power demand is changed. Thus, the source current should remain at the constant level irrespective of change in the load reactive power demand.

At time t1=0.1 sec and t2=0.2 sec both shunt and series inverters are put ON, respectively, with a pure resistive load (15 kW) on the system. During time t2 to t3, the UPQC is not performing any compensation due to the presence of resistive load. This can be noticed from the Figure 5.11 (c) and (g), where both shunt and series inverters do not inject any compensating current and voltage, respectively.

At time t3=0.3 sec, the load on the system is changed to 15 kW + j 7 kVAR. Since the load reactive power demand is well within the shunt inverter VAR compensation limits (9.3 kVAR), the shunt inverter should now act immediately to compensate the load reactive power alone. As viewed form Figure 5.11 (g), the shunt inverter starts compensating the load reactive power demand by injecting 90^{o} leading current. The series inverter does not take part in load reactive power compensation as noticed from Figure 5.11.

At time t4=0.4 sec, the load on the system is increased to 15 kW + j 12 kVAR. The series inverter should now share the part of the load reactive power demand, since, it is more than the shunt inverter compensation limit. The series inverter starts compensating the load reactive power (2.7 kVAR) by injecting appropriate voltage (61V) through series transformers at the proper phase angle as calculated by the controller, shown in Figure 5.11 (c). This causes 9.7^{o} power angle advancement in load voltage *w.r.t.* the source voltage without changing the resultant load voltage magnitude as seen from Figure 5.11 (b) and (h). The 9.7^{o} power angle difference between these two voltages can be noticed from scaled

Figure 5.11 (h). During this condition the shunt inverter compensates the load reactive power up to its maximum limit. Thus, both the shunt (9.3 kVAR) and series (2.7 kVAR) inverters share the load reactive power demand effectively.

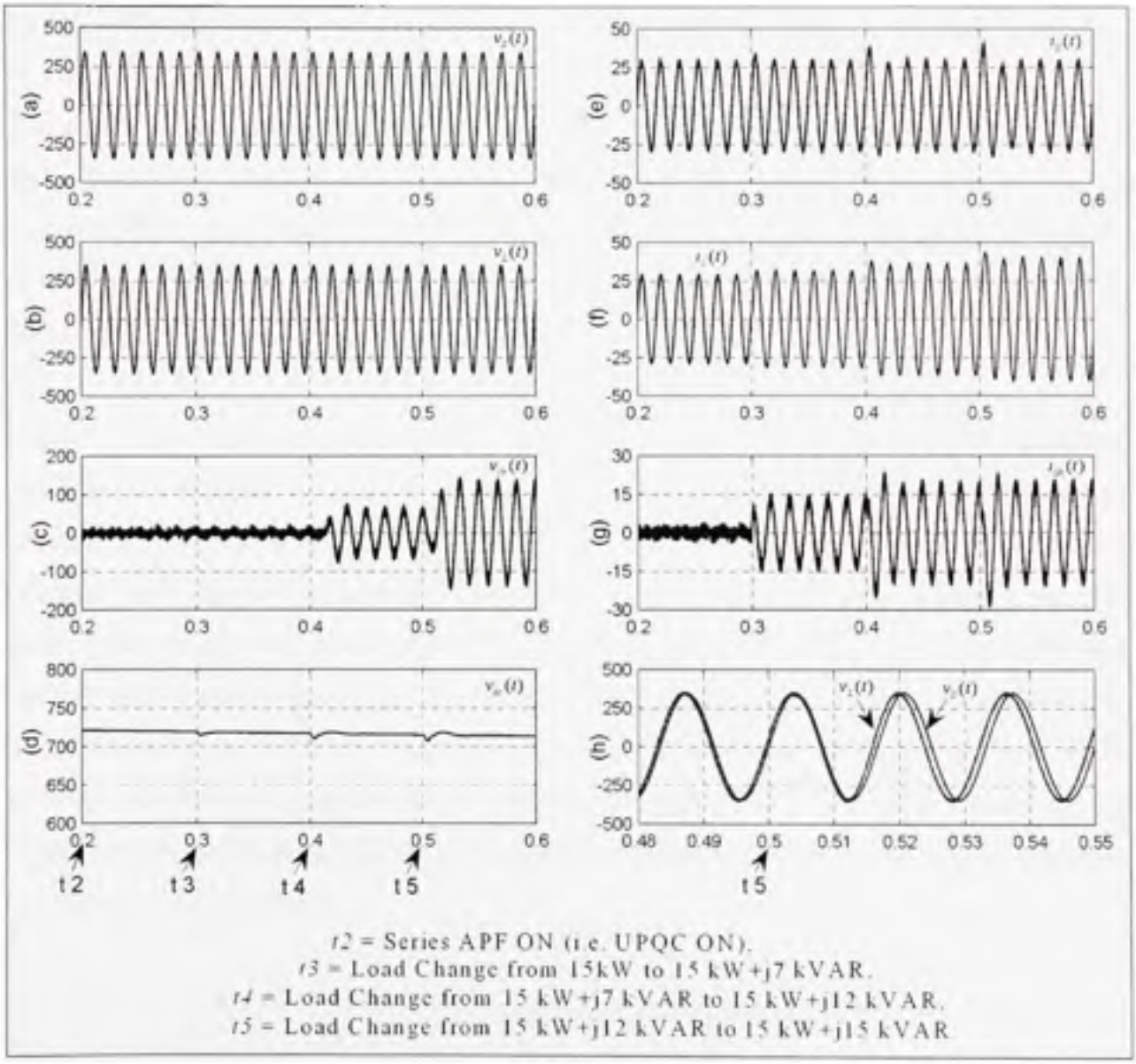

Figure 5.11 Simulation Results: load reactive power compensation with PAC of UPQC.

At time t5=0.5 sec, the system is loaded up to its maximum rated condition i.e. 15 kW + j 15 kVAR. During this condition, the series inverter injects required voltage (140V) to compensate the increased load reactive power demand. This causes further increase in power angle δ from 9.7° to 21.5 ° between both the source and load voltages, as discussed in the theory which can be noticed from the Figure 5.11 (h). Here, the shunt APF compensates 9.3 kVAR, while series inverter compensates 5.7 kVAR of the total load reactive power demand.

The source current, as shown in Figure 5.11 (e), is strictly at the constant value during all the above conditions. The load current profile under different load conditions is shown in Figure 5.11 (f). Thus, from Figure 5.11 (e) and (f), the source delivers only the load active power demand, i.e. in other words, the PAC approach does not put any extra active power burden on the source. The DC link voltage profile is shown in Figure 5.11 (d).

Figure 5.12 (a) – (d) shows computed different active and reactive powers under the above mentioned load conditions. All these values are based on per phase calculation. The power handled by series inverter, till time t4 is almost zero. This is due to the fact that the load reactive power demand is supported by the shunt inverter alone. At time t4 and t5, the load reactive power demands are changed such that the series inverter also takes part in the load reactive power compensation. As noticed from the Figure 5.12 (b), the source supplies only active power to the load, whereas, the reactive power is shared by both shunt and series inverters. Moreover, the active power handled by series inverter is complemented by the shunt inverter, such that no additional active power burden is put on the source for realization of proposed PAC approach.

The different parameters during above mentioned conditions are shown in Table 5.1 and Table 5.2. All the current and the voltage values are mentioned on the per phase basis and are represented as peak amplitude. As noticed from Table 5.1 and Figure 5.10, with the full load on the network, without considering PAC control approach, the required shunt inverter compensating current in order to compensate the load reactive power demand is 29A.

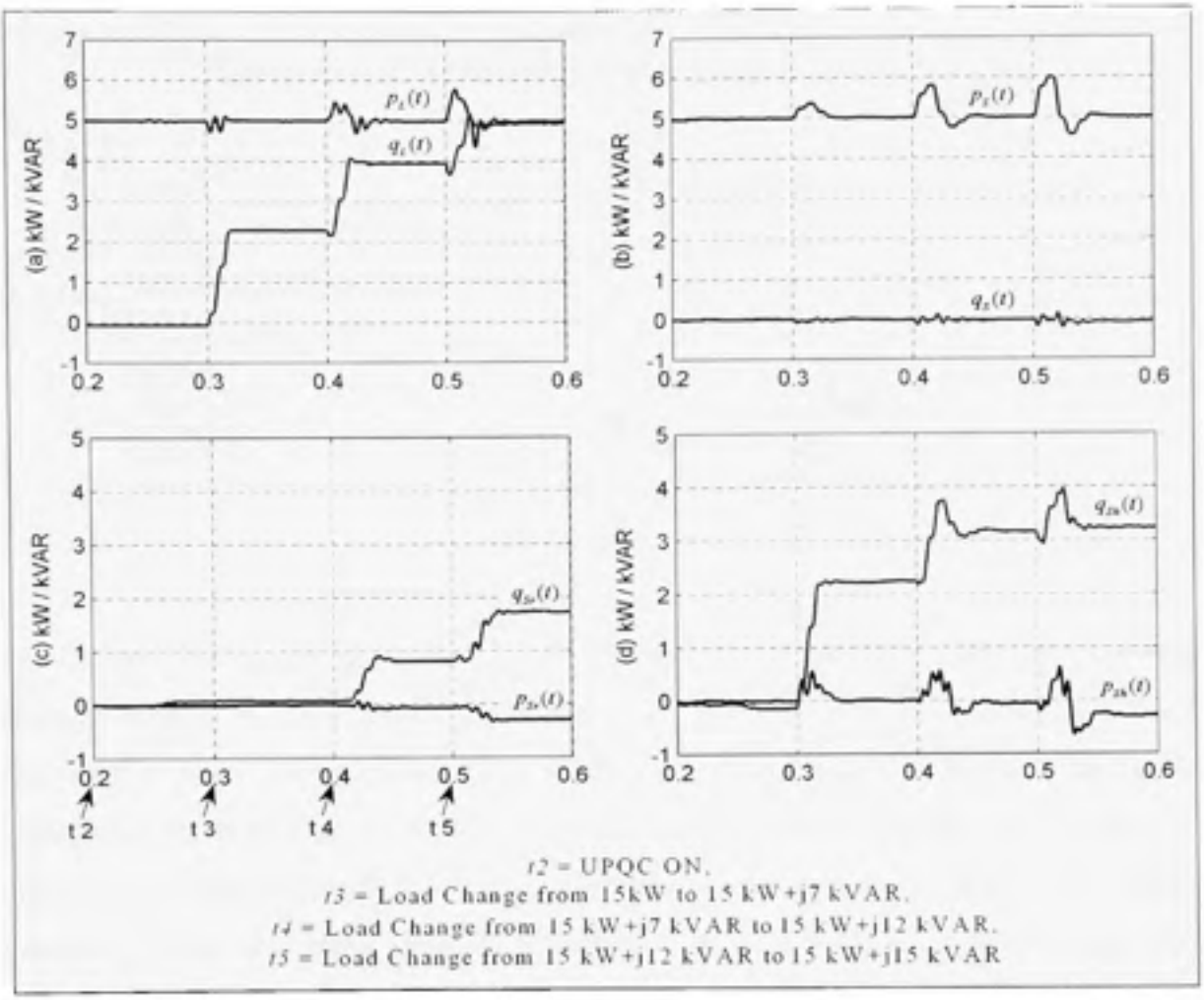

Figure 5.12 Simulation Results – active and reactive power flow during PAC of UPQC.

Table 5.1
Different voltage and current magnitude (peak values)

	Load Condition	V_S (V)	V_L (V)	V_{Sr} (V)	I_S (A)	I_L (A)	I_{Sh} (A)
a	15kW (*t0* to *t3*)	347	347	0	29.0	29.0	0.0
b	15kW+*j*7kVAR (*t3* to *t4*)	347	347	0	30.0	31.7	13.4
c	15kW+*j*12kVAR (*t4* to *t5*)	347	347	61	30.0	36.7	18.5
d	15kW+*j*15kVAR (*t5* onwards)	347	347	132	30.0	40.5	18.5
e	15kW+*j*15kVAR (without PAC)	347	347	0	29.0	40.5	29.0

Table 5.2
Phase angle relationship between voltages and currents

	Load Condition	φ_L (deg.)	φ_S (deg.)	δ (deg.)	β (deg.)	φ_{Sh} (deg.)	φ_{Sh_S} (deg.)	φ_{Sh_L} (deg.)
a	15kW (*t0* to *t3*)	0^0	0^0	0^0	0^0	0^0	-	-
b	15kW+*j*7kVAR (*t3* to *t4*)	-24.6^0	0^0	0^0	-24.6^0	0^0	+90.4	+90.4
c	15kW+*j*12kVAR (*t4* to *t5*)	-38.3^0	0^0	9.7^0	28.6^0	$+95^0$	+100.8	+91.1
d	15kW+*j*15kVAR (*t5* onwards)	-44.7^0	0^0	21.5^0	23.2^0	$+101^0$	+117.5	+96
e	15kW+*j*15kVAR (without PAC)	-45.0^0	0^0	0^0	0^0	0^0	+90.4	+90.4

From Table 5.1 (d) and Figure 5.11 (g), the proposed PAC approach results in considerable reduction in shunt inverter current magnitude from 29A to 18.5A. Thus, with the proposed approach the shunt inverter current can be reduced by 10.5A. In other words, with the PAC approach the shunt inverter kVA rating get reduced to 25.6% of total load kVA rating. The source current magnitude is almost constant and at unity power factor during all the operating conditions, since, the active power demand on the load is kept constant under those conditions. This confirms that the PAC of UPQC does not demand additional active power from the source for its operation, and thus, is proven to be advantageous in almost all the UPQC based applications.

5.8 Experimental Validation of Proposed Phase Angle Control Approach

The performance of proposed PAC theory is also validated through extensive experimental investigation. The proposed PAC approach is equally applicable for single-phase system. For simplicity, the experimental investigation is carried out for single-phase system. The hardware setup is the same as discussed in Appendix-1. Additionally, a highly inductive load is considered for better visualization of results.

5.8.1 Real-Time Instantaneous Active and Reactive Power Computation

Figure 5.13 shows the computed real-time instantaneous load active (trace-3) and reactive (trace-4) powers. These quantities are essential to execute the proposed PAC in real-time. Initially, the load on the system is simple resistive load. As noticed from the figure, even if the load is resistive in nature, the real-time computation shows certain amount of reactive power demand on the system. This is due to the fact that the voltage available at the input of UPQC is slightly distorted. After a certain period of time, a highly inductive load is switched on, and connected in parallel with resistive load. The developed control algorithm takes less than 2 cycles to compute changes in the load active and reactive powers. Thus, using these two powers the power angle δ is computed easily in real-time.

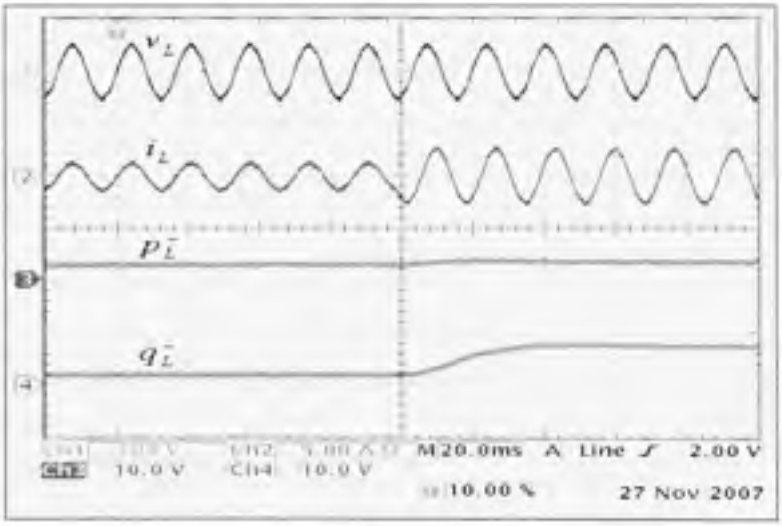

Figure 5.13 Experimental Results: Real-Time Instantaneous $\bar{p}_L$ & $\bar{q}_L$ Computation.

5.8.2 Performance of UPQC without Phase Angle Control Approach

In this section, the basic function of UPQC to compensate the load reactive power is highlighted. As in the traditional case, only the shunt inverter is utilized to compensate the load reactive power demand. The experimental results under such test condition are shown in Figure 5.14. The profiles of load and source voltage-current are shown in Figure 5.14 (a), which are identical, since, the UPQC is in OFF mode. The load current lags the load voltage

by an angle of 53^0 (0.6 lagging power factor). Figure 5.14 (b) shows the experimental results when the shunt inverter is ON. Here, the series inverter is in OFF condition as the load voltage is at the desired value (neglecting the slightly distorted voltage). The shunt inverter compensates the load reactive power by injecting the required quadrature current and thus, makes the source current in-phase with the source voltage. The reduction in source current magnitude also confirms this fact, as the source now supplies only active part of the total load power demand.

The above example demonstrates that if the voltage supplied from the utility is well within the required constraints (close to pure sinusoidal and at rated magnitude), the series inverter stays in idle condition. It plays an important role only during sudden variation in utility voltages (sag, swell, flicker, etc.) and if the voltages show the presence of harmonics.

On the other hand, the shunt inverter is solely utilized to compensate the load reactive power demand (harmonics, unbalance, etc. depending on the load on the system). Thus, it can be pointed out that in traditional UPQC applications the series inverter is under utilized.

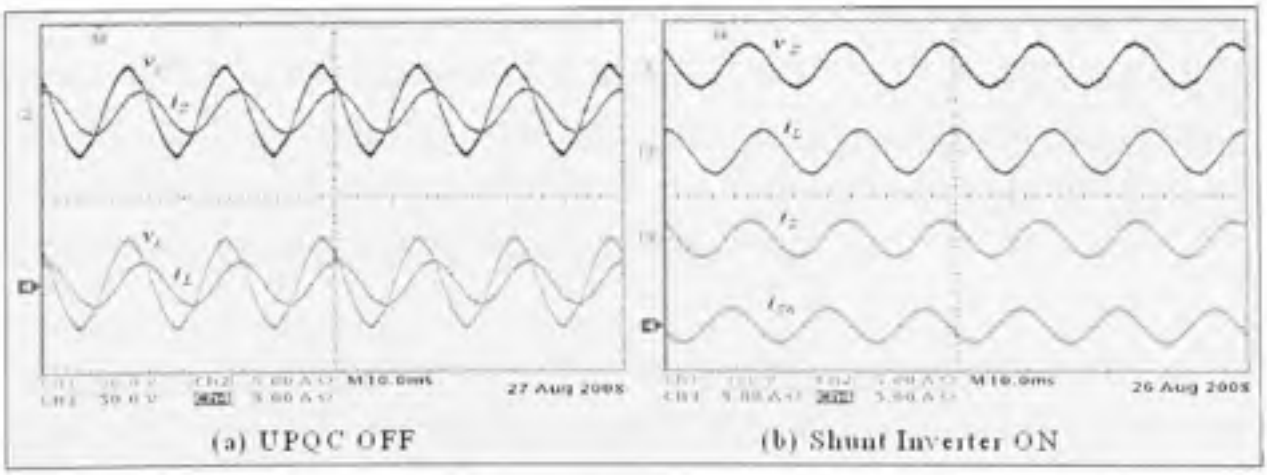

Figure 5.14 Experimental Results – performance of UPQC without PAC Approach.

5.8.3 Performance of UPQC with Phase Angle Control Approach

The performance of proposed PAC of UPQC, under the same system conditions (as that of without PAC approach, section 5.8.2), is shown in Figure 5.15. To demonstrate the effectiveness of PAC approach, the series inverter is turned ON first. The experimental result during this condition is shown in Figure 5.15 (a). As noticed from the figure, when the series inverter is put into operation, it gives a phase lead to load voltage *w.r.t.* source voltage. The phase shift between the source and resultant load voltage, i.e. power angle δ, is found as 18°. Moreover, a close view of the figure also suggest that 18° power angle shift between load and source voltages boost the power factor angle between source voltage and source current from 53° lagging to 35° lagging. In other words, the source side power factor improves from 0.6 lagging to 0.82 lagging. Figure 5.15 (b) shows the experimental results when the shunt inverter is also put in operation i.e. UPQC ON. The shunt inverter now supplies the remaining load reactive power demand, thus, making the source current in exact phase with the source voltage.

The occurrence of power angle δ between the sources and load voltages can be clearly noticed from Figure 5.15 (c). At this point it is essential to mention that, at first glance the source and load voltage magnitude does not appear to be equal. The source voltage is slightly distorted and shows the sharp peaks at its maximum values (Figure 5.15 (b), upper trace) reflect that the source voltage magnitude is higher than the load voltage. But, the *rms* values of both the voltages are identical. The improved sinusoidal load voltage profile (Figure 5.15 (b) lower trace) also helps to realize the above stated fact.

The performance of both the inverters along with the self supporting DC bus, under the PAC approach, is plotted in Figure 5.15 (d). The series injected voltage profile is distorted as it compensates the harmonics in source voltage in addition to load reactive power. The shunt inverter performance is given in Figure 5.15 (e). As noticed from Figure 5.14 (b) and Figure 5.15 (e), the shunt current (i_{sh}) profiles suggest the reduction in compensating current

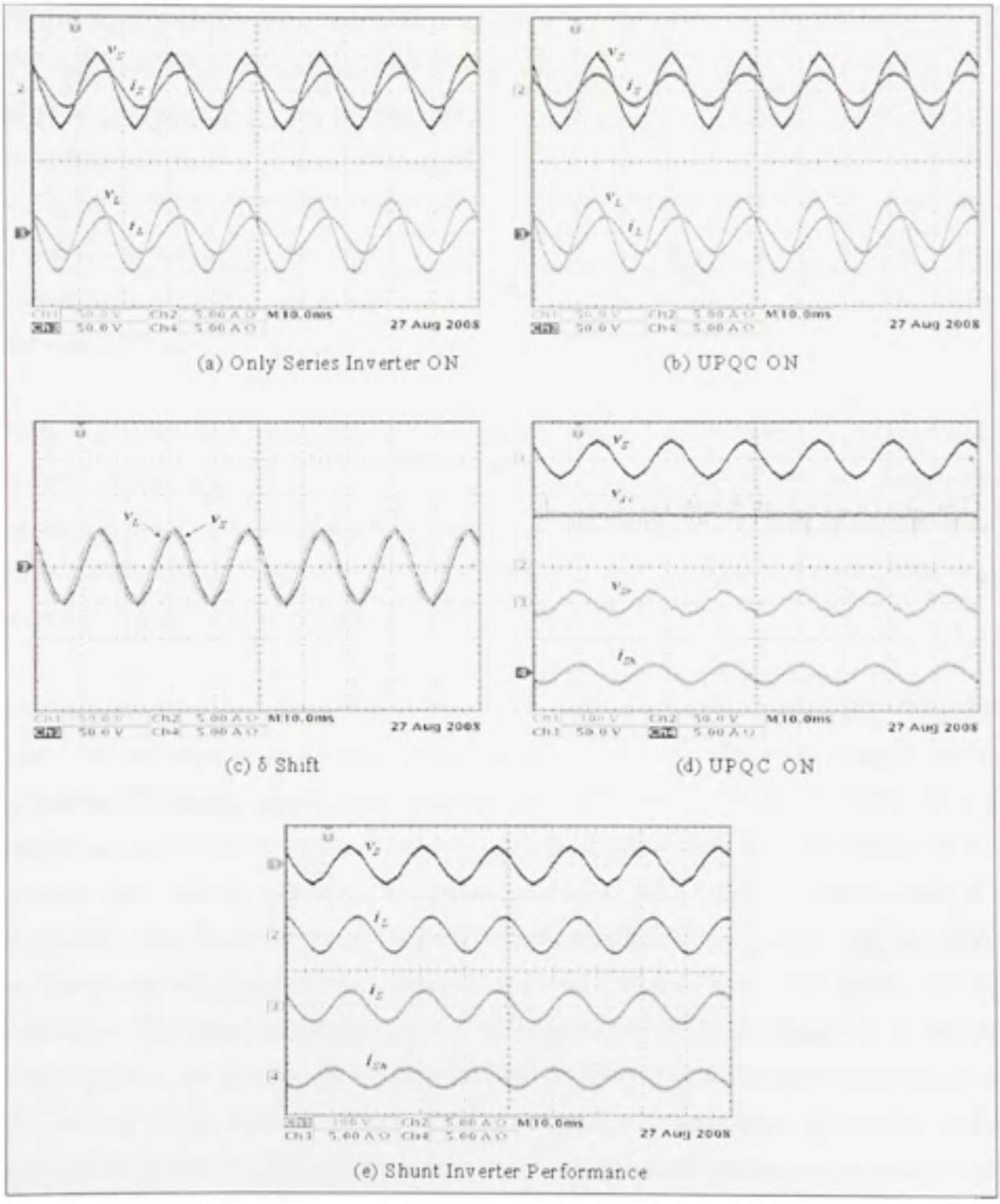

Figure 5.15 Experimental Results – Performance of proposed PAC approach.

magnitude. The required shunt compensating current magnitude to support the total load reactive power, without PAC approach, is found as 1.92A (peak value). With the proposed PAC approach, the shunt compensating current magnitude reduces to 1.34A (peak value). In terms of percentages, the net reduction in shunt current magnitude with reference to the actual shunt current magnitude (without PAC approach) is estimated around 30%. In other words, the PAC of UPQC helps to reduce the reactive power burden on shunt inverter and eventually its rating. This experimental investigation thus proves that the reactive power sharing feature of UPQC can be achieved effectively by appropriate control of both the series and shunt inverters.

Table 5.3 gives the magnitudes and percentage THD values of different voltages and currents, while, Table 5.4 gives the different phase angle relationships between voltages and currents. Fluke 41B Power Harmonics Analyzer is used to record the given data. In Figure 5.16, the determined information is represented as a phasor diagram, drawn considering source voltage as reference phasor.

The fundamental values (*rms*) of both source and load voltages are almost equal. From the Table 5.4, the phase angle of shunt compensating current *w.r.t.* the source voltage can be noticed as 86^{o} leading. Ideally, this value should be 90^{o}, but, as the shunt inverter takes a certain amount of active power from the source to maintain the DC link voltage at the constant level and to overcome the losses associated with UPQC, it defers from the quadrature value. Nevertheless, it is still close to the required 90^{o} phase shift. This also helps to reveal that the proposed PAC approach does not consume extra active power for its realization. The voltage that appears across shunt inverter is the load voltage and as noticed from Table 5.4, the phase angle between the load voltage and shunt compensating current is 68^{o}. In other words, a certain amount of active power transfer takes place between the shunt and series inverters. But this active power is counterbalanced between both the inverters such that it maintains the overall active and reactive power balance in entire system.

Table 5.3
Measured voltage and current magnitude using Fluke 41B

	1	2	3	4	5	6
Measured Parameter	V_S	V_L	V_{Sr}	I_S	I_L	I_{Sh}
RMS Value	35.22 V	35.18 V	11.02 V	1.51 A	1.75 A	0.94 A
Peak Value	52.8 V	50.05 V	16.81 V	2.09 A	2.46 A	1.34 A
% THD	3.78%	2.66%	-	3.04%	2.19%	-

Table 5.4
Different phase angle determination

	1	2	3	4	5	6	7	8
Measured angle between	$v_S - i_S$	$v_S - i_L$	$v_S - i_{Sh}$	$v_L - i_S$	$v_L - i_L$	$v_L - i_{Sh}$	$v_{Sr} - i_S$	$v_{Sr} - i_L$
Parameter extracted	φ_S	β	φ_{Sh_S}	δ	φ_L	φ_{Sh_L}	φ_{Sr}	--
Angle (deg.)	0° (unity)	35° (lag)	86° (lead)	18° (lead)	53° (lag)	68° (lead)	100° (lag)	135° (lag)

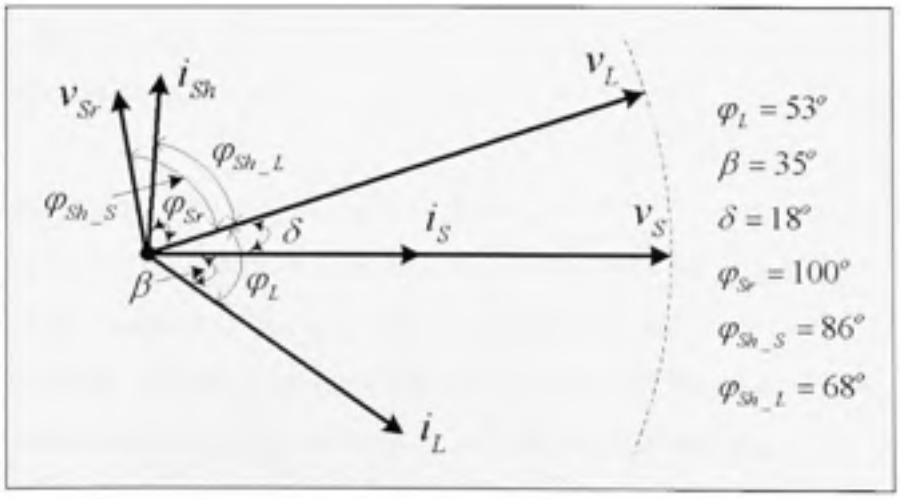

Figure 5.16 Phasor representation showing relative phase angles between different voltages and current with power angle δ=18°.

5.8.4 Performance of UPQC under Different Power Angles

In this section, the summary of an extensive experimental investigation, under several different power angles δ, is presented. To show the effect of power angle δ on the shunt inverter rating, the experiments are carried at δ = 10°, 15°, 18°, 23°, and 28°. Some of the important experimental results are given in Figure 5.17 to Figure 5.20. Table 5.5 gives the detailed values of each of the voltages and currents. Based on the above mentioned experimental data, a comparative evaluation on UPQC parameters (voltage/current) is carried out in Figure 5.21.

Figure 5.17 gives the experimental results when only the series inverter is put into operation. In traditional UPQC applications (δ=0°), as the series inverter does not take part in load reactive power compensation, the load and source voltages are in-phase. As power angle δ increases gradually the effective phase angle between the source voltage and the source current (β) reduces accordingly. This suggests the increased load power factor seen from the source side. The experimental results when both the inverters are ON can be seen in Figure 5.18. The shunt inverter now compensates the remaining load reactive power demand, thus, making the source current in-phase with the source voltage. Under all the power angles δ the UPQC maintains the unity power factor operation. The important point to be noted here is that the source current magnitude is almost constant irrespective of the boost in power angle δ (can also be verified from the Table 5.5).

The experimental results showing the power angle δ between source and load voltages are shown in Figure 5.19. The presence of power angle δ can also be observed from Figure 5.18 and Figure 5.19 by comparing the load voltage profiles at the zero crossings of respective source voltages. Note that the fundamental values (*rms*) of both the voltages are strictly equal, which is one of the significant features of proposed power angle control theory. The difference in these voltage magnitudes may result in additional active power exchange between the source and UPQC.

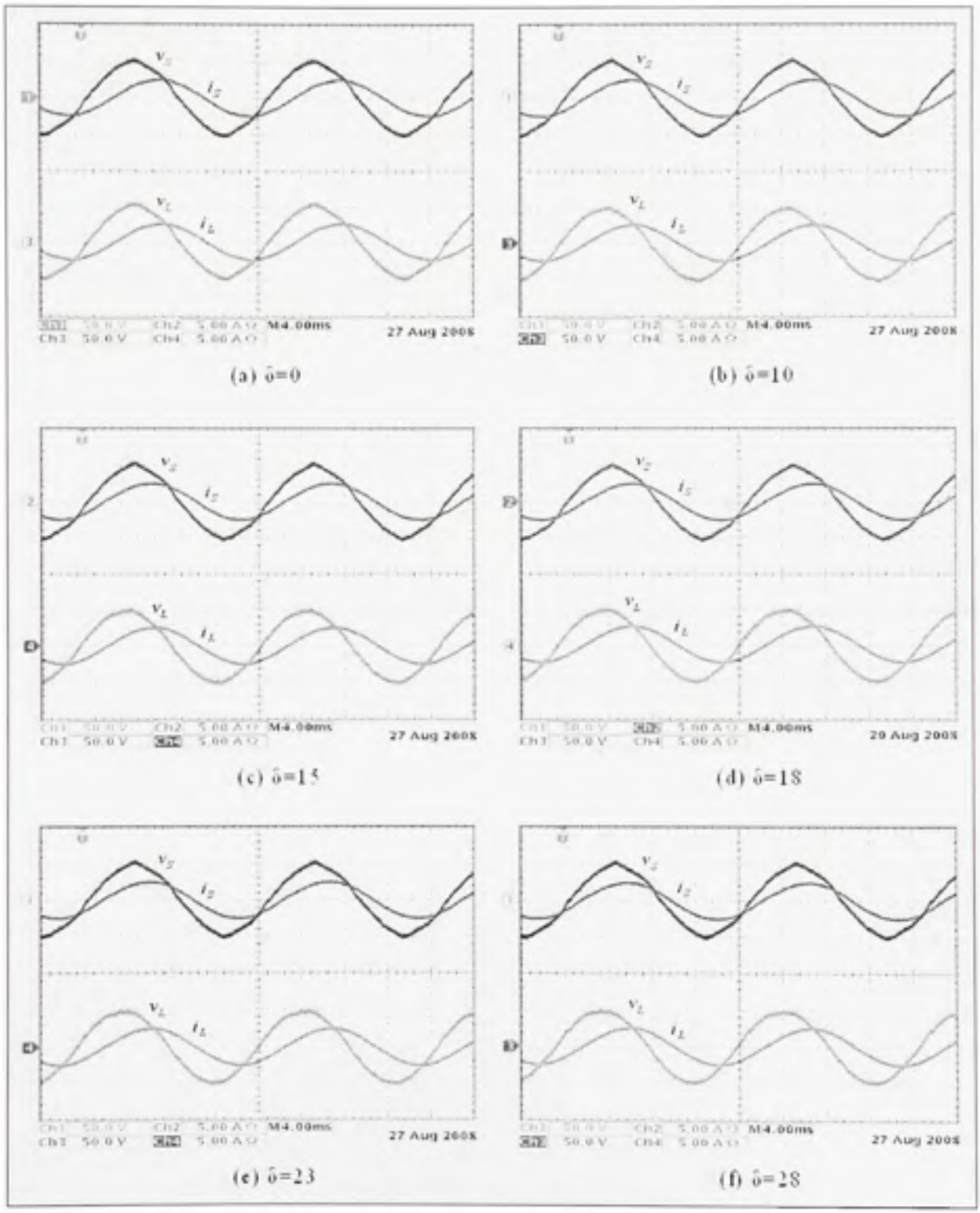

Figure 5.17 Experimental Results – PAC approach performance under different power angles, only series inverter is ON.

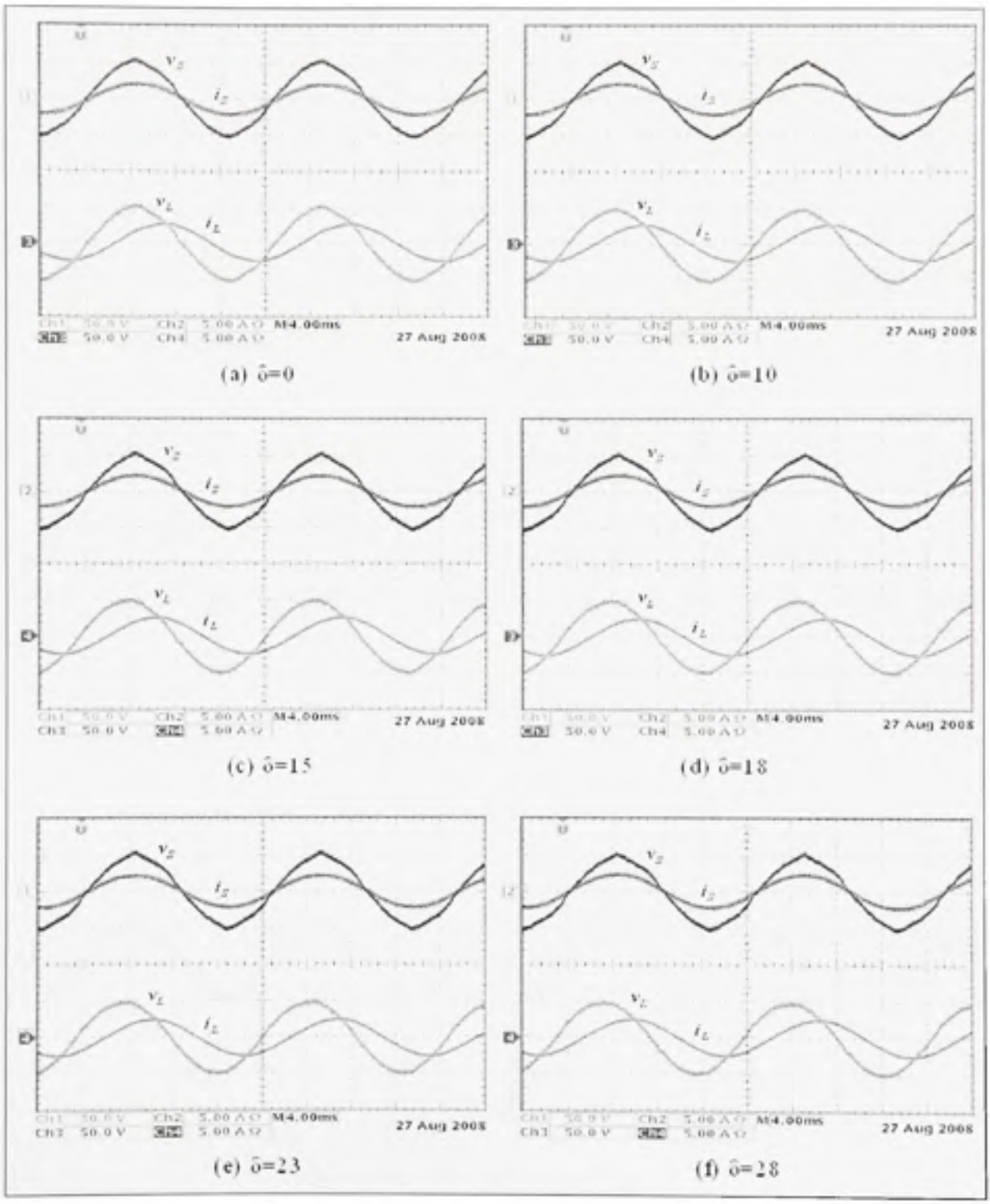

Figure 5.18 Experimental Results – PAC approach performance under different power angles, UPQC ON.

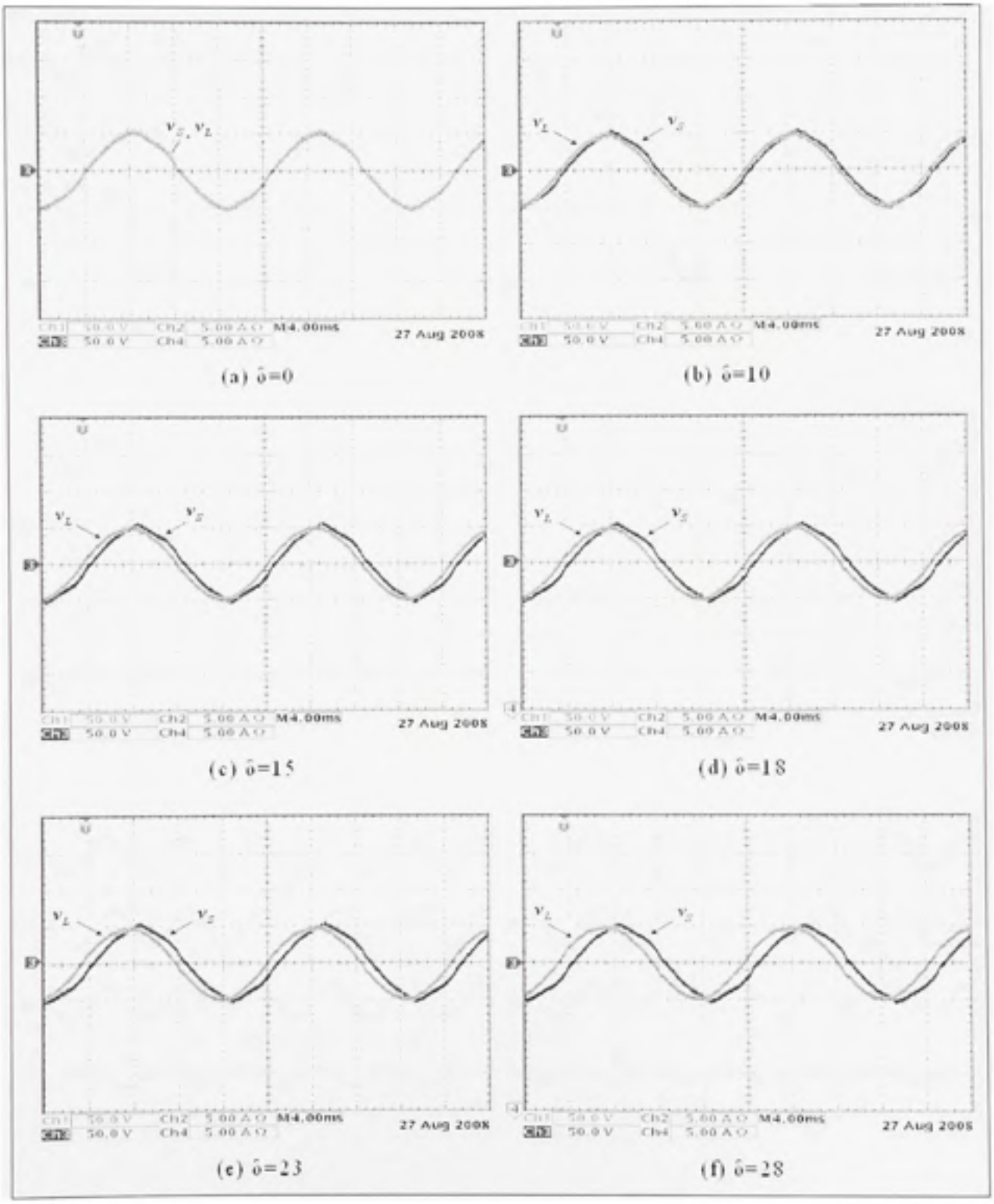

Figure 5.19 Experimental Results – source and load voltage phase shifts under different power angles.

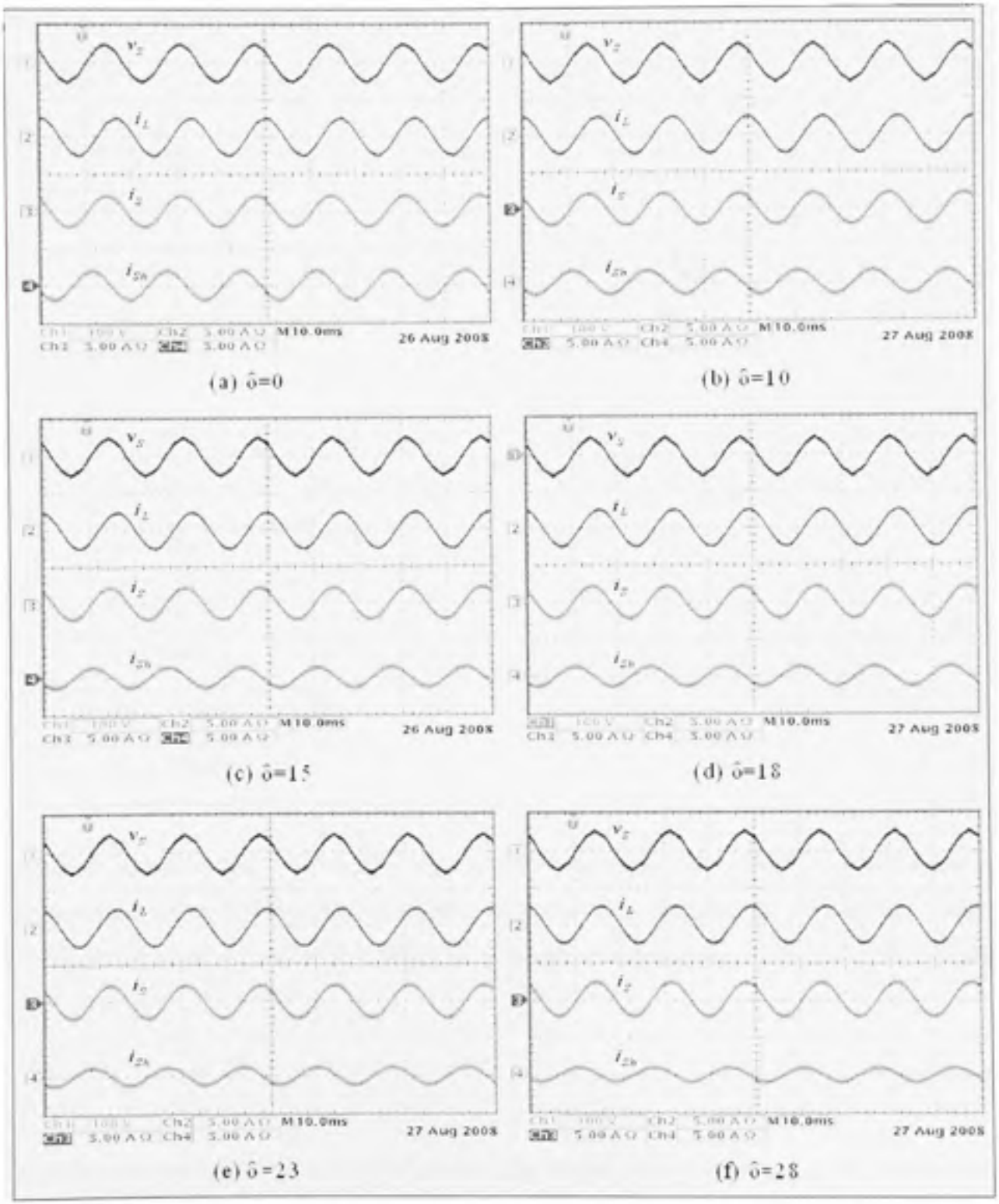

Figure 5.20 Experimental Results – shunt inverter compensating current reduction under different power angles.

Table 5.5
Performance of PAC approach under different power angles δ

		$\delta = 0^{\circ}$	$\delta = 10^{\circ}$	$\delta = 15^{\circ}$	$\delta = 18^{\circ}$	$\delta = 23^{\circ}$	$\delta = 28^{\circ}$
1	$V_S(rms) \rightarrow$	35.24 V	35.10 V	35.10 V	35.20 V	35.20 V	35.04 V
2	$V_L(rms) \rightarrow$	35.24 V	35.00 V	35.00 V	35.18 V	35.15 V	35.05 V
3	$V_{Sr}(rms) \rightarrow$	-	06.53 V	09.82 V	11.02 V	13.39 V	16.82 V
4	$I_L(rms) \rightarrow$	1.74 A	1.75 A	1.75 A	1.75 A	1.75 A	1.75 A
5	$I_S(rms) \rightarrow$	1.47 A	1.50 A	1.50 A	1.51 A	1.52 A	1.54 A
6	$I_{Sh}(rms) \rightarrow$	1.36 A	1.12 A	0.98 A	0.94 A	0.84 A	0.68 A
7	$\varphi_L(lag) \rightarrow$	[5]53°	53°	53°	53°	53°	53°
8	φ_S(unity) $\rightarrow$	0°	0°	0°	0°	0°	0°
9	$\beta(lag) \rightarrow$	-	43°	38°	35°	30°	25°
10	φ_{Sr}(lead) $\rightarrow$	-	96°	98°	100°	102°	103°
11	$\varphi_{Sh\_S}(lead) \rightarrow$	87°	86°	86°	86°	87°	87°
12	$\varphi_{Sh\_L}(lead) \rightarrow$	-	75°	70°	68°	64°	59°

Figure 5.20 shows the most interesting results of the proposed work. The shunt inverter performance under different power angles δ is given and compared with traditional UPQC ($\delta=0^{\circ}$) performance. It is clearly visible that as the power angle δ increases, the shunt inverter

[5] All the phase angles are computed by taking the reading between the respective voltages and currents using Fluke 41B. There might be an error of ±1 degree due to the measurement error as well as due to the unavailability of exact phase knowledge as the used instrument rounds off the measured phase angle. However, the care is taken to use exact same methodology to carry out the experiments and to compute different parameters.

compensating current magnitude reduces accordingly. Note that the load and source current magnitudes are almost unaffected with change in angle δ (also see the Table 5.5). Thus, this experimental investigation confirms and validates the proposed phase angle control theory developed for UPQC applications.

The data given in Table 5.5 is plotted in Figure 5.21. Some of the important observations are highlighted below:

- As the power angle δ increases, in order to maintain the same voltage (source and load) magnitudes, the voltage injected by series inverter also increases accordingly.
- The increase in δ causes the reduction in shunt compensating current but keeping the source current magnitude almost constant. The slight increase in source current can be noticed for higher value of power angle δ. This is mainly due to the losses associated with UPQC which are increased slightly. A well designed hardware system would certainly maintain the source current at a constant value.
- The change in series injected voltage phase angle *w.r.t.* source voltage is quite small.
- The shunt compensating current phase angle remains in close quadrature relation *w.r.t.* to the source voltage, suggests no additional active power drawn from the source side. On the other hand, its phase angle *w.r.t.* the load voltage reduces in proportion to increase in the power angle δ. This suggests that increasingly reactive and active power is being exchanged between shunt and series inverters.
- The shunt inverter maintains the unity power factor irrespective of change in power angle δ.
- The increased δ tends to improve the power factor angle between the resultant load current and the source voltage ($\cos\beta$).

- With the increased δ the net reduction in shunt inverter rating[6] is significant. Even a small shift in the power angle δ (< 10°) can lead to a considerable reduction in shunt inverter rating (here, up to 17.5%).

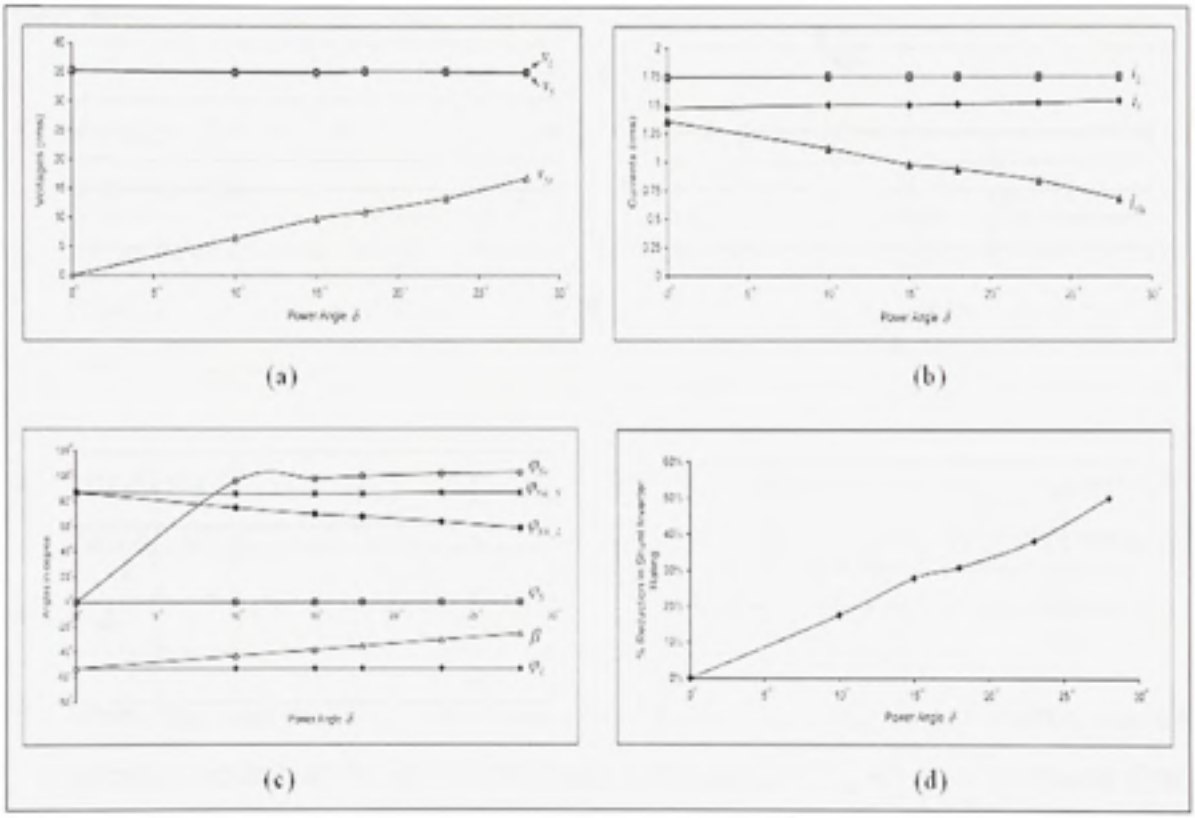

Figure 5.21 Comparative evaluation under different power angles.

[6] The net reduction in shunt inverter rating is computed by comparing it with δ=0 (without PAC approach) and is calculated as: Net reduction in shunt inverter rating $= \frac{I_{Sh}|_{(\delta=0)} - I_{Sh}|_{(\delta)}}{I_{Sh}|_{(\delta=0)}} \times 100\%$

5.9 Conclusions

This chapter proposes a new control philosophy for UPQC in which both the shunt and series inverters share the load reactive power demand, termed as power angle control (PAC) of UPQC. The complete mathematical analysis is presented. The proposed approach is validated through extensive simulation and experimental studies. The major key points of PAC theory for load reactive power compensation are highlighted below:

- Based on the given system, load and UPQC constraints, the maximum series inverter VAR compensation can be estimated. This helps to fix the maximum shunt inverter compensation limit which result in the reduction of the shunt inverter rating. However, it does not affect the existing series inverter rating. Thus, the overall cost of UPQC is reduced.

- The shunt inverter always has the priority to compensate the load reactive power demand up to its maximum limit. This assures the full utilization of shunt inverter for load reactive power compensation.

- When the load reactive power increases above the shunt inverter limits, the series inverter comes into the role to compensate the remaining load reactive power demand with in a short period of time. The half cycle delay in the series inverter compensation is due to the delay in computation time to extract the change in load reactive power demand.

- The shunt and series inverters operate in coordination to achieve the common task – the load reactive power compensation. Thus, a better utilization of existing series inverter can be done during a normal operating condition.

- A power angle difference occurs between source and load voltage, but the resultant load voltage magnitude is maintained constant at the desired value.

- The proposed approach does not put any extra active power burden on the supply system for its operation.

- The simulation results for full load of 15 kW + *j* 15 kVAR show that the shunt inverter kVA rating can be reduced up to 25.6%, by utilizing proposed PAC approach. Additionally, the experimental results show that for high inductive load (load power factor 0.6 lagging) the shunt inverter rating can be reduced up to 50% with power angle $\delta = 28^{o}$.

CHAPTER 6

PERFORMANCE OF PAC APPROACH UNDER DIFFERENT OPERATING CONDITIONS

6.1 Introduction

In the previous chapter, the concept of proposed power angle control (PAC) is successfully designed, developed, and validated with a consideration of ideal system (i.e. pure sinusoidal without voltage sag, swell, etc.) under linear RL load. In this chapter, the theory of PAC approach is further extended for the voltage sag and swell conditions. A complete mathematical analysis is provided to compute the different UPQC parameters.

The performance equations for the proposed PAC approach are standardized to arrange them in a generalized manner. These comprehensive equations can be used to estimate the required series injection voltage and the shunt compensating current profiles (magnitude and phase angle), and the total amount of active and reactive power that flows through the UPQC under steady-state, voltage sag and swell conditions.

This chapter also introduces two control techniques for power angle δ, especially under the voltage sag and swell condition, to control the amount of reactive power shared by each of the inverters. Moreover, the emphasis is also given to overcome the distortions present in the source voltage and the load current.

The findings in this chapter are supported with the adequate simulation and the laboratory experimental results. It is shown that the PAC approach can be implemented successfully to compensate the voltage sag, voltage swell, voltage harmonics, and the current harmonics while both the inverters share the load reactive power demand.

6.2 PAC approach under Voltage Sag Condition

The analysis presented in the previous chapter was based on the steady-state condition, i.e. the source voltage was considered at rated value. The concept of PAC approach is further extended during the sag on the system. In the following subsections a detailed mathematical analysis and the necessary equations to estimate the shunt and series inverter parameters are briefly discussed.

6.2.1 Phasor Representation under Voltage Sag Condition

From the previous chapter, it is well understood that the sag on the system can be compensated through active (refer CHAPTERS 2 and 3) as well as reactive power (refer CHAPTER 4). Figure 6.1 shows the phasor representation of PAC approach with active power sag control method (Figure 6.1 (a)) and with reactive power sag control method (Figure 6.1 (b)). It is evident that the combined operation of PAC concept and the sag controlled through reactive power does not give the desired performance. Therefore, the active power control for voltage sag and swell is considered.

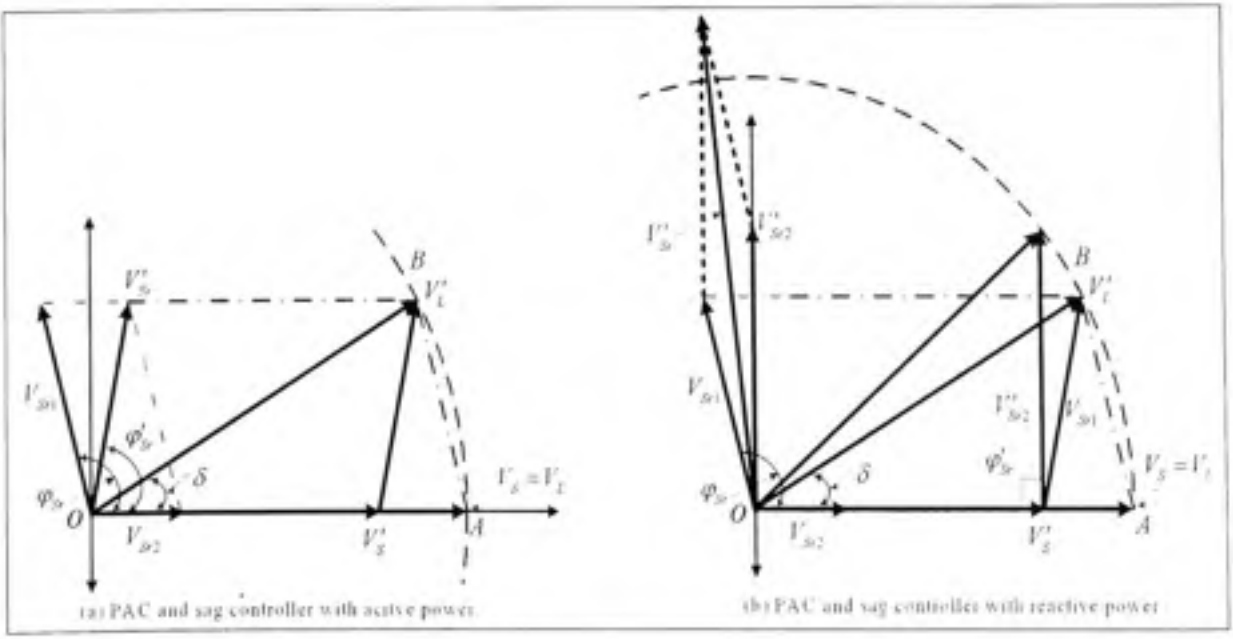

Figure 6.1 Phasor representation of PAC approach under voltage sag condition.

Consider that the UPQC system is already working under PAC approach, i.e. both the inverters are compensating the load reactive power and the injected series voltage causes a power angle δ between resultant load and the actual source voltages. Now, if a sag condition occurs on the system, both the inverters should keep supplying the load reactive powers, as they were before the sag. In other words, irrespective of the variation in the supply voltage the series inverter should maintain same[7] power angle δ between both the voltages. Additionally, the series inverter should also compensate the voltage sag by injecting the appropriate voltage component.

Let's represent a vector V_{Sr1} responsible to compensate the load reactive power utilizing PAC concept and vector V_{Sr2} responsible to compensate the sag on the system using active power control approach. Thus for simultaneous compensation, the series inverter should now supply a component (V_{Sr1}) to support the load reactive power and another component to compensate the sag on the system (V_{Sr2}). The new series injected voltage magnitude as well as the phase angle would be the vector sum of V_{Sr1} and V_{Sr2}. This resultant series injected voltage (V_{Sr}) will maintain the load voltage magnitude at a desired level such that the dip in source voltage will not appear across the load terminal. Moreover, the series inverter will keep sharing the load reactive power demand.

In order to support the active power required during sag condition, as discussed in CHAPTER 3, the source delivers the extra source current. At this juncture it is essential to point out that while determining the maximum power angle δ_{max} the additional increase current component was taken into account, therefore, the sag condition will not cause any additional burden on both the shunt and series inverter ratings.

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[7] This is possible only if the load on the system does not change during the voltage sag condition. If the load changes under the voltage sag condition, the PAC approach will give a different δ angle. The increase or decrease in new δ angle would depends on the increase or decrease in load reactive power, respectively.

For load reactive power compensation using PAC of concept,

$$\vec{V}_{Sr1} = \vec{V}^{*}_{L} - \vec{V}_{S} \tag{6.1}$$

$$V_{Sr1}\angle\varphi_{Sr} = V'_{L}\angle\delta - V_{S}\angle 0 \tag{6.2}$$

For voltage sag compensation using active power control approach,

$$\vec{V}_{Sr2} = \vec{V}^{*}_{L} - \vec{V}'_{S} \tag{6.3}$$

$$V_{Sr2}\angle 0 = V'^{*}_{L}\angle 0 - V'_{S}\angle 0 \tag{6.4}$$

For simultaneous load reactive power and sag compensation,

$$\vec{V}'_{Sr} = \vec{V}_{Sr1} + \vec{V}_{Sr2} \tag{6.5}$$

$$V'_{Sr}\angle\varphi'_{Sr} = V_{Sr1}\angle\varphi_{Sr} + V_{Sr2}\angle 0 \tag{6.6}$$

6.2.2 Series Inverter Parameter Estimation under Voltage Sag Condition

In this section, the required series inverter parameters to achieve simultaneous load reactive power and voltage sag compensations are computed. Figure 6.2 shows the detailed phasor diagram to determine the magnitude and phase of series injection voltage.

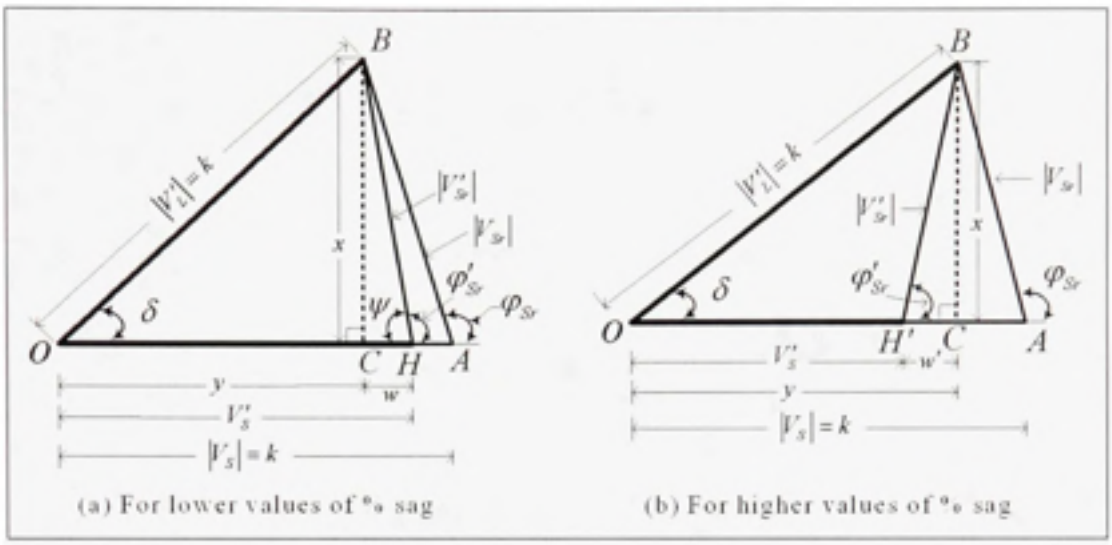


Figure 6.2 Detailed phasor representation for series inverter parameter estimation under voltage sag condition.

From ΔOCB,

$$x = k.\sin\delta \tag{6.7}$$

$$y = k.\cos\delta \tag{6.8}$$

$$w = V''_S - y \tag{6.9}$$

Rewriting the equation (1.7) from CHAPTER2,

$$k_f = \frac{V'_S - V'_L}{V'_L} \tag{6.10}$$

Representing (6.10) for sag condition under PAC,

$$k_f = \frac{V''_S - V''_L}{V''_L} = \frac{V''_S - k}{k} \tag{6.11}$$

$$I''_S = \left(1 + k_f\right).k \tag{6.12}$$

$$\text{Let's define, } 1 + k_f = n_{ff} \tag{6.13}$$

$$\text{Thus, } I''_S = n_{ff}.k \tag{6.14}$$

$$\text{Therefore, } w = n_{ff}k - y \tag{6.15}$$

$$\text{In } \Delta BCH\text{ , } \left|I''_{Sr}\right| = \sqrt{x^2 + w^2} \tag{6.16}$$

$$\left|I''_{Sr}\right| = \sqrt{(k.\sin\delta)^2 + (n_{ff}.k - k\cos\delta)^2} \tag{6.17}$$

$$\left|I''_{Sr}\right| = k.\sqrt{1 + n_{ff}^{\ 2} - 2.n_{ff}.\cos\delta} \tag{6.18}$$

$$\text{Now, } \angle CHB = \psi = \tan^{-1}\left(\frac{x}{w}\right) \tag{6.19}$$

$$\psi = \tan^{-1}\left(\frac{\sin\delta}{n_{ff} - \cos\delta}\right) \tag{6.20}$$

$$\text{Therefore, } \angle\varphi'_{Sr} = 180^0 - \angle\psi \tag{6.21}$$

Equations (6.18) and (6.21) give the required magnitude of series voltage and its phase angle that should be injected to achieve the voltage sag compensation while supporting the load reactive power under PAC approach. Figure 6.2 (b) represents the condition for the larger value of voltage sag on the system. Similar equations can be written from the phasor diagram.

Check:

If we replace V'_S by normal steady state source voltage magnitude (V_S), then, (6.18) should resolve to (5.13).

At normal steady-state, $V_S = k$, and if we replace $V'_S = V_S$, then from (6.18),

$$|V''_{Sr}| = \sqrt{k^2 + k^2 - 2.k^2.\cos\delta} = k.\sqrt{2}.\sqrt{1-\cos\delta} = \text{Equation (5.13)}$$

Also, from (6.11) and (6.20) $k_f = 0$, $\therefore n_a = 1$. $\therefore \psi = \tan^{-1}\left(\frac{\sin\delta}{1-\cos\delta}\right) = \alpha$. Hence, $\varphi_{Sr} = \varphi'_{Sr}$

Therefore, the PAC approach based controller can be designed in an adaptive manner to tackle the change in the supply voltage without affecting the proposed reactive power compensation feature.

6.2.3 Shunt Inverter Parameter Estimation under Voltage Sag Condition

In this section, the required current injected by the shunt inverter in order to achieve the load reactive power under the voltage sag compensation mode is computed. The phasor diagram based on different currents is represented in Figure 6.3.

As the UPQC is assumed to be compensating for load reactive power using PAC approach, the shunt inverter injects the current I'_{sh} prior to the sag on the system. In order to achieve the voltage sag compensation through active power control approach the source should supply increased current I'_S (refer CHAPTERS 1 and 2 for more details). Thus, to support the series inverter to inject the required voltage for load reactive power and sag compensations, the shunt inverter should now deliver the current I''_{Sh}. This resultant shunt compensating current will maintain the DC link voltage at the constant level. Thus it facilitates the required active power transfer between the source and shunt inverter, shunt inverter and series inverters

(through DC link) and finally, from series inverter to the load. Figure 6.4 represents the phasor diagrams to compute the shunt inverter injected current magnitude and its phase angle.

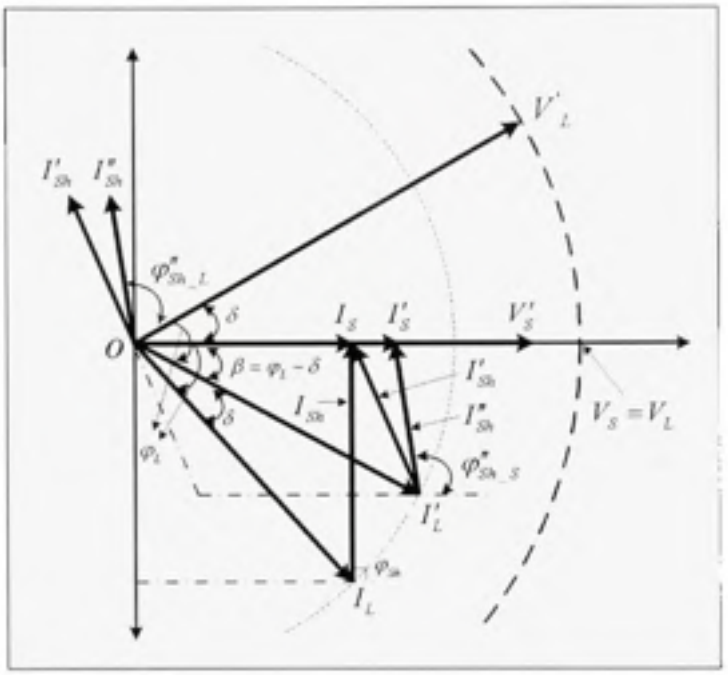


Figure 6.3 Current based phasor representation of PAC approach under voltage sag condition.

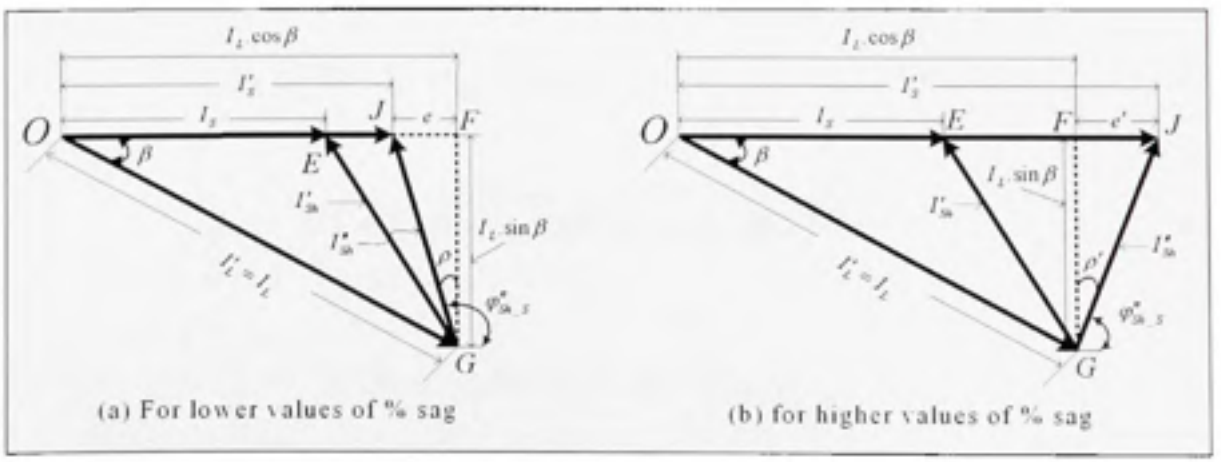


Figure 6.4 Detailed phasor diagram to compute the shunt inverter parameters under voltage sag condition.

From ΔOFG (Figure 6.4 (a)).

$$FG = I'_L.\sin\beta \tag{6.22}$$

$$OF = I'_L.\cos\beta \tag{6.23}$$

Rewriting the equation (1.12). CHAPTER1.

$$I'_S = \frac{I_L}{1+k_f}.\cos\varphi_L \tag{6.24}$$

$$\text{Let, } \frac{1}{1+k_f} = k_O \tag{6.25}$$

$$\text{Therefore, } I'_S = k_O.I_L.\cos\varphi_L \tag{6.26}$$

$$e = I'_L.\cos\beta - I'_S \tag{6.27}$$

$$e = I'_L.\left(\cos\beta - k_O.\cos\varphi_L\right) \tag{6.28}$$

$$\text{In } \Delta GFJ\text{ , } I''_{Sh} = \sqrt{(I'_L.\sin\beta)^2 + [I'_L.\left(\cos\beta - k_O.\cos\varphi_L\right)]^2} \tag{6.29}$$

$$I''_{Sh} = I'_L.\sqrt{1+k^2{}_O.\cos^2\varphi_L - 2.k_O.\cos\beta.\cos\varphi_L} \tag{6.30}$$

$$\text{Now, } \angle JGF = \rho = \tan^{-1}\left(\frac{e}{I'_L.\sin\beta}\right) \tag{6.31}$$

$$\rho = \tan^{-1}\left(\frac{I'_L.(\cos\beta - k_O.\cos\varphi_L)}{I'_L.\sin\beta}\right) \tag{6.32}$$

$$\rho = \tan^{-1}\left(\frac{\cos\beta - k_O.\cos\varphi_L}{\sin\beta}\right) \tag{6.33}$$

$$\text{Therefore, } \angle\varphi''_{Sh\_S} = \angle\rho + 90^0 \tag{6.34}$$

$$\text{and } \angle\varphi''_{Sh\_L} = \left(\angle\rho + 90^0\right) - \delta \tag{6.35}$$

Equations (6.30) and (6.35) give the required magnitude and phase angle of shunt inverter compensating current to achieve the desired operation from the UPQC. Figure 6.4 (b) represents the condition for the larger value of the source current under a high percentage of voltage sag on the system. Similar equations can be written from the phasor diagram.

Under normal steady-state condition, the factor K_O will be 1 and thus, (6.30) and (6.35)will resolve to (5.27) and(5.32), respectively.

6.3 PAC Approach under Voltage Swell Condition

This section discusses the utilization of PAC concept during a voltage swell on the system. The brief mathematical analysis and the important equations for the series and shunt inverters are computed.

6.3.1 Phasor Representation under Voltage Swell Condition

As in the previous section, the goal here is also to support the load reactive power using both the inverters in addition to the voltage swell compensation. The phasor representation during a voltage swell on the system is shown in Figure 6.5. Let's represent a vector I'_{Sr3} responsible to compensate the swell on the system using active power control approach. Thus for

simultaneous compensation, the series inverter should supply the $\vec{V}_{Sr1}$ component to support the load reactive power and $\vec{V}_{Sr3}$ to compensate the swell on the system. The resultant series injected voltage ($\vec{V}_{Sr}$) would maintain the load voltage magnitude at a desired level, while supporting the load reactive power, such that the rise in source voltage will not appear across the load terminal.

For voltage swell compensation using active power control approach,

$$\vec{V}_{Sr3} = \vec{V}'_L - \vec{V}''_S \tag{6.36}$$

$$V_{Sr3}\angle 0 = V'_L\angle 0 - V''_S\angle 180 \tag{6.37}$$

For simultaneous load reactive power and voltage swell compensations,

$$\vec{V}''_{Sr} = \vec{V}_{Sr1} + \vec{V}_{Sr3} \tag{6.38}$$

$$V''_S\angle\varphi''_{Sr} = V_{Sr1}\angle\varphi_{Sr} + V_{Sr3}\angle 180 \tag{6.39}$$

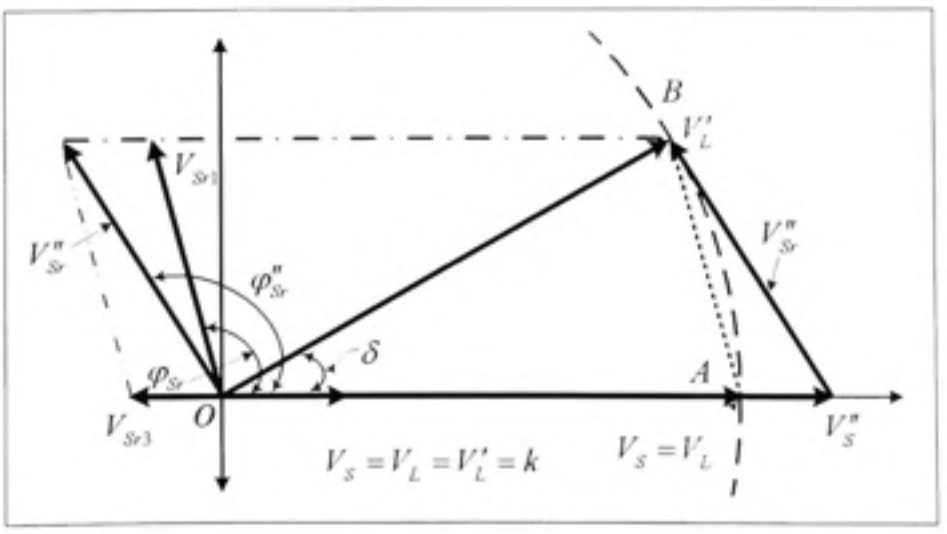


Figure 6.5 Phasor representation of PAC approach under voltage swell condition.

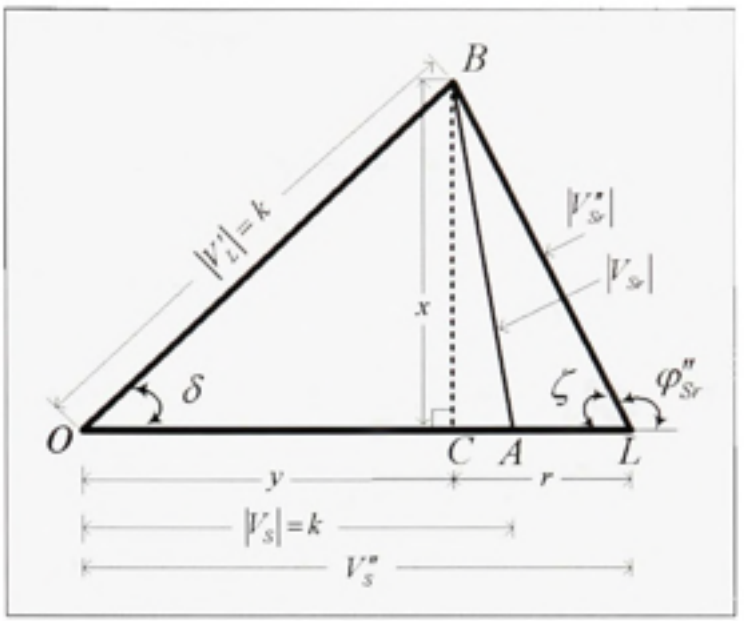


Figure 6.6 Detailed phasor representation for series inverter parameter estimation under voltage swell condition.

From Figure 6.6,

$$r = V_S'' - k.\cos\delta \tag{6.40}$$

$$\text{In } \Delta BCL,\ |V_{Sr}''| = \sqrt{x^2 + r^2} \tag{6.41}$$

$$|V_{Sr}''| = \sqrt{(k.\sin\delta)^2 + (n_v.k - k\cos\delta)^2} \quad (\because\ V_S'' = n_v.k) \tag{6.42}$$

$$|V_{Sr}''| = k.\sqrt{1 + n_v^2 - 2.n_v.\cos\delta} \tag{6.43}$$

$$\text{Now, } \angle CLB = \zeta = \tan^{-1}\left(\frac{x}{r}\right) \tag{6.44}$$

$$\zeta = \tan^{-1}\left(\frac{\sin\delta}{n_v - \cos\delta}\right) \tag{6.45}$$

$$\text{Therefore, } \angle\varphi''_{Sr} = 180^0 - \angle\zeta \tag{6.46}$$

Equations (6.43) and (6.46) give the required magnitude of series voltage and its phase angle that should be injected to achieve the voltage swell compensation while supporting the load reactive power under PAC approach.

6.3.2 Shunt Inverter Parameter Estimation under Voltage Swell Condition

In this section, the required current injected by shunt inverter in order to achieve load reactive power under voltage swell compensation mode is computed. The phasor diagram based on different currents is represented in Figure 6.7, whereas, the detailed phasor to compute the shunt inverter parameters is shown in Figure 6.8.

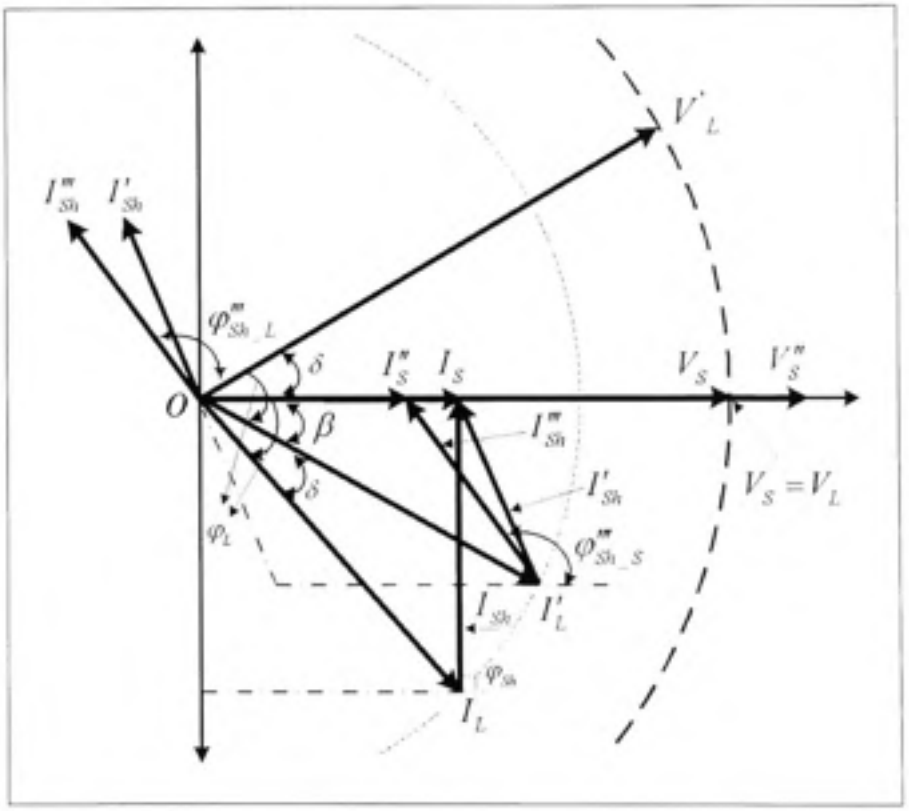


Figure 6.7 Current based phasor representation of PAC approach under voltage swell condition.

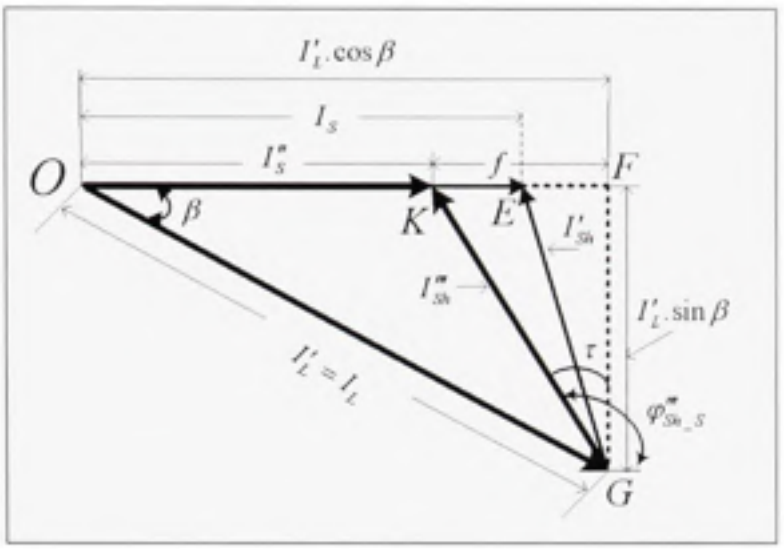


Figure 6.8 Detailed phasor diagram to compute the shunt inverter parameters under voltage swell condition.

As discussed in CHAPTER 1, the source current magnitude, while compensating the swell on the system using active power control concept, get reduced from its normal steady-state value (see Figure 1.18). This reduced current is represented as I''_S. The procedure to determine the shunt inverter parameters during swell is the same as that used for the sag condition. Therefore, only important equations are highlighted.

$$I''_S = k_{vi}.I_L.\cos\varphi_L \tag{6.47}$$

$$f = I'_L.\cos\beta - I''_S \tag{6.48}$$

$$f = I'_L.(\cos\beta - k_{vi}.\cos\varphi_L) \tag{6.49}$$

$$\text{In } \Delta GFK,\ I''_{Sh} = I'_L.\sqrt{1 + k^2_{vi}.\cos^2\varphi_L - 2.k_{vi}.\cos\beta.\cos\varphi_L} \tag{6.50}$$

$$\angle KGF = \tau = \tan^{-1}\left(\frac{f}{I'_L.\sin\beta}\right) \tag{6.51}$$

$$\tau = \tan^{-1}\left(\frac{\cos\beta - k_{cf}.\cos\varphi_L}{\sin\beta}\right) \tag{6.52}$$

$$\text{Therefore, } \angle\varphi^{m}_{Sh\_S} = \angle\tau + 90^{0} \tag{6.53}$$

$$\text{and } \angle\varphi^{m}_{Sh\_L} = \left(\angle\tau + 90^{0}\right) - \delta \tag{6.54}$$

Equations (6.50) and (6.54) give the required magnitude and phase angle of shunt inverter compensating current to achieve the desired operation from the UPQC.

6.4 Summary of PAC approach under different operating condition

To this point, the analysis on phase angle control theory applied under steady-state, voltage sag and voltage swell conditions have been thoroughly presented. Here, the brief summary of main equations governing shunt and series parameters is highlighted in Table 6.1.

Table 6.1
Summary of PAC Approach Performance Equations

	Condition	Type	Performance Equations
1	Steady-State	Series Inverter Parameters	$\lvert I'_{Sr}\rvert = k.\sqrt{2}.\sqrt{1-\cos\delta}$ (5.13) $\angle\varphi_{Sr} = 180^0 - \tan^{-1}\left(\frac{\sin\delta}{1-\cos\delta}\right)$ (5.17)
		Shunt Inverter Parameters	$\lvert I'_{Sh}\rvert = \lvert I'_L\rvert.\sqrt{1+\cos^2\varphi_L - 2.\cos\beta.\cos\varphi_L}$ (5.27) $\angle\varphi'_{Sh\_S} = 90^0 + \tan^{-1}\left(\frac{\cos\beta-\cos\varphi_L}{\sin\beta}\right)$ (5.31)
2	Voltage Sag	Series Inverter Parameters	$\lvert I''_{Sr}\rvert = k.\sqrt{1+n_{(1)}^2 - 2.n_{(1)}.\cos\delta}$ (6.18) $\angle\varphi'_{Sr} = 180^0 - \tan^{-1}\left(\frac{\sin\delta}{n_{(1)}-\cos\delta}\right)$ (6.20)
		Shunt Inverter Parameters	$I''_{Sh} = I'_L.\sqrt{1+k^2_{(1)}.\cos^2\varphi_L - 2.k_{(1)}.\cos\beta.\cos\varphi_L}$ (6.30) $\angle\varphi''_{Sh\_S} = 90^0 + \tan^{-1}\left(\frac{\cos\beta-k_{(1)}.\cos\varphi_L}{\sin\beta}\right)$ (6.34)
3	Voltage Swell	Series Inverter Parameters	$\lvert I''_{Sr}\rvert = k.\sqrt{1+n_{(1)}^2 - 2.n_{(1)}.\cos\delta}$ (6.43) $\angle\varphi''_{Sr} = 180^0 - \tan^{-1}\left(\frac{\sin\delta}{n_{(1)}-\cos\delta}\right)$ (6.46)
		Shunt Inverter Parameters	$I'''_{Sh} = I'_L.\sqrt{1+k^2_{(1)}.\cos^2\varphi_L - 2.k_{(1)}.\cos\beta.\cos\varphi_L}$ (6.50) $\angle\varphi'''_{Sh\_S} = 90^0 + \tan^{-1}\left(\frac{\cos\beta-k_{(1)}.\cos\varphi_L}{\sin\beta}\right)$ (6.53)

$$I'_{Sr\_PAC} = k.\sqrt{1+n_O^2 - 2.n_O.\cos\delta} \tag{6.55}$$

$$\angle\varphi_{Sr\_PAC} = 180^0 - \tan^{-1}\left(\frac{\sin\delta}{n_O - \cos\delta}\right) \tag{6.56}$$

$$I_{Sb\_PAC} = I_L.\sqrt{1+k^2{}_O.\cos^2\varphi_L - 2.k_O.\cos\beta.\cos\varphi_L} \tag{6.57}$$

$$\angle\varphi_{Sb\_S\_PAC} = 90^0 + \tan^{-1}\left(\frac{\cos\beta - k_O.\cos\varphi_L}{\sin\beta}\right) \tag{6.58}$$

As observed from the Table 6.1, the performance equations of PAC approach under voltage sag and swell condition for both the inverters are identical. The generalized performance equations for power angle control concept can be written as:

The terms k_f, n_O and k_O are re-written as:

$$k_f = \frac{I'x - k}{k},\ n_O = 1 + k_f,\ \text{and}\ k_O = \frac{1}{1+k_f}$$

$$\text{Where, } I'x = \begin{cases} I'_S, \text{Steady State} \\ I''_S, \text{Voltage Sag} \\ I'''_S, \text{Voltage Swell} \end{cases} \tag{6.59}$$

The possible values of k_f, n_O and k_O are given in Table 6.2.

Table 6.2
Possible values of factor k_f, n_O and k_O

	Condition	Vx	$k_f = \frac{Vx - k}{k}$	$n_{(.)} = 1 + k_f$	$k_{(.)} = \frac{1}{1 + k_f}$
1	Steady State	K	0	1	1
2	Voltage Sag	$Vx < k$	$-1 > k_f < 0$, (-ve)	$0 < n_{(.)} < 1$, (+ve)	$+\infty < k_{(.)} > 1$, (+ve)
3	Voltage Swell	$Vx > k$	$0 < k_f < +1$, (+ve)	$+1 > n_{(.)} > +2$, (+ve)	$+1 < k_{(.)} < 0.5$ (+ve)

6.5 Generalized Equations for Active–Reactive Power Flow utilizing PAC Approach

In this section, the generalized equations for active and reactive power flow through UPQC are given. Consider the voltage sag condition on the network, the active-reactive power flow through series inverter can be determined as:

During voltage sag

$$P'_{Sr} = V''_{Sr}.I'_{S}.\cos\varphi''_{Sr} \tag{6.60}$$

$$P'_{Sr} = V''_{Sr}.I'_{S}.\cos(180^{\circ} - \psi) \tag{6.61}$$

$$P'_{Sr} = V''_{Sr}.I'_{S}.(-\cos\psi) \tag{6.62}$$

From Figure 6.2 (a)

$$P'_{Sr} = -V''_{Sr}.I'_{S}.\left(\frac{w}{V''_{Sr}}\right) \tag{6.63}$$

$$P'_{Sr} = -I'_S.k.(n_{\prime\prime} - \cos\delta) \tag{6.64}$$

The increase (I'_S) or decrease (I''_S) in the source current magnitude during the voltage sag or swell condition, respectively, is represented as,

$$I'_S = I''_S = k_{\prime\prime}.I_L.\cos\varphi_L \tag{6.65}$$

$$\text{Therefore, } P'_{Sr} = -(k_{\prime\prime}.I_L.\cos\varphi_L).k.(n_{\prime\prime} - \cos\delta) \tag{6.66}$$

For a losses system, since the reactive power is handled by UPQC, the source current can be represented as,

$$I_S = I_L.\cos\varphi_L \tag{6.67}$$

$$\text{Therefore, } P_{Sr,PAC} = P'_{Sr} = -k_{\prime\prime}.(k.I_S).(n_{\prime\prime} - \cos\delta) \tag{6.68}$$

For reactive power,

$$Q'_{Sr} = I''_{Sr}.I'_S.\sin\varphi''_{Sr} \tag{6.69}$$

$$Q'_{Sr} = I''_{Sr}.I'_S.\sin(180^\circ - \psi) \tag{6.70}$$

$$Q'_{Sr} = I''_{Sr}.I'_S.\sin\psi \tag{6.71}$$

From Figure 6.2 (a)

$$Q'_{Sr} = I''_{Sr}.I'_S.\left(\frac{X}{I''_{Sr}}\right) \tag{6.72}$$

$$Q'_{Sr} = k.k_O.I_S.(\sin\delta) \quad (\because x = k\sin\delta) \tag{6.73}$$

$$\therefore\ Q_{Sr,PAC} = k_O.(k.I_S).(\sin\delta) \tag{6.74}$$

Equations (6.68) and (6.74) represent the generalized equations for active and reactive power flow through series inverter.

In steady-state condition, without sag and swell on the system, the generalized equations for the series inverter should resolve to normal steady-state equations. On the other hand, without consideration of PAC approach, under steady-state, the active as well as reactive powers handled by series inverter should be zero.

Check1:

For steady-state PAC control, without sag/swell: k_O=1, and n_O=1

Equation (6.68) will be $P_{Sr,PAC} = -k.I_S.(1-\cos\delta)$ = Equation (5.52)

and (6.74) will be $Q_{Sr,PAC} = k.I_S.(\sin\delta)$ = Equation (5.56)

Check2:

For steady-state condition, without PAC approach: k_O=1, n_O=1, and δ=0

$P_{Sr,PAC} = -k.I_S.(1-\cos 0) = 0$ and $Q_{Sr,PAC} = k.I_S.(\sin 0) = 0$

The active and reactive power handled by the shunt inverter as seen from the source side is computed. These powers, under voltage sag condition, can be determined as:

$$P'_{Sh} = V''_S.I''_{Sh}.\cos\varphi''_{Sh\_S} \tag{6.75}$$

$$P'_{Sh} = n_O.k.I''_{Sh}.\cos(90^\circ + \rho) \quad (\because V''_S = n_O.k) \tag{6.76}$$

$$P'_{Sh} = n_O.k.I''_{Sh}.(-\sin\rho) \tag{6.77}$$

From Figure 6.4,

$$P'_{Sh} = -n_O.k.I''_{Sh}.\left(\frac{e}{I''_{Sh}}\right) \tag{6.78}$$

$$P'_{Sh} = -n_O.k.I''_{Sh}.\left(\frac{e}{I''_{Sh}}\right) \tag{6.79}$$

$$P'_{Sh} = -n_O.k.I_L.(\cos\beta - k_O.\cos\varphi_L) \tag{6.80}$$

$$P_{Sh,PAC} = -\frac{(k.I_L).(\cos\beta - k_O.\cos\varphi_L)}{k_O} \tag{6.81}$$

For reactive power,

$$Q''_{Sh} = V''_S.I''_{Sh}.\sin\varphi'_{Sh\_S} \tag{6.82}$$

$$Q''_{Sh} = n_O.k.I''_{Sh}.\sin(90^\circ + \rho) \tag{6.83}$$

$$Q''_{Sh} = n_O.k.I''_{Sh}.\cos(\rho) \tag{6.84}$$

$$Q''_{Sh} = n_O.k.I''_{Sh}.\frac{I_L.\sin\beta}{I''_{Sh}} \tag{6.85}$$

$$Q_{Sh,PAC} = \frac{(k.I_L).(\sin\beta)}{k_O} \tag{6.86}$$

Equations (6.81) and (6.86) represent the generalized equations for active and reactive power flow through shunt inverter.

In steady-state condition, without consideration of PAC approach, the active power handled by the shunt inverter should be zero, whereas, the reactive power should be equal to the load reactive power demand.

Check:

For steady-state condition, without PAC approach: k_O=1, n_O=1, δ=0, and β= φ_L

$$\therefore\ P_{Sh,PAC} = -\frac{(k.I_L).(0)}{1} = 0 \text{ and } Q_{Sh,PAC} = \frac{(k.I_L).(\sin\varphi_L)}{1} = \text{Load reactive power demand}$$

Thus, the generalized equations representing the active and reactive power flow through UPQC under any condition, utilizing PAC concept, are summarized as:

$$P_{Sr,PAC} = -k_O.(k.I_S).(n_O - \cos\delta) = -k_O.(n_O - \cos\delta).(P_S) \tag{6.87}$$

$$Q_{Sr,PAC} = k_O.(k.I_S).(\sin\delta) = k_O.(\sin\delta).(P_S) \tag{6.88}$$

$$P_{Sh,PAC} = -\frac{(k.I_L).(\cos\beta - k_O.\cos\varphi_L)}{k_O} = -\frac{(\cos\beta - k_O.\cos\varphi_L)}{k_O}.(P_L) \tag{6.89}$$

$$Q_{Sh,PAC} = \frac{(k.I_L).(\sin\beta)}{k_O} = \frac{(\sin\beta)}{k_O}.(P_L) \tag{6.90}$$

6.6 Different Modes of Operations

As noticed from the previous sections, for effective voltage sag/swell compensation while sharing the load reactive power, the source current may increase or decrease. As the source current flows through series inverter, the reactive power supplied by it is directly influenced by this current. Therefore, the reactive power supplied by series inverter may vary during

voltage sag and swell conditions. However, with proper control, the series inverter can be forced to supply the fixed reactive power (same as steady-state value) irrespective of change in source current magnitude due to the voltage sag/swell on the system. Thus, two possible control techniques to control the amount of reactive power supported by series and shunt inverter are developed. Note that these control techniques are applicable only under voltage sag or swell condition.

In one of the methods, the power angle δ is kept constant under all the operating conditions (steady-state, voltage sag and swell). Let's define this control approach as *fixed power angle* δ technique. The analysis presented so far in this chapter is based on the above consideration. As can be noticed from the (6.87) and (5.13), for the voltage sag on the system, with fixed δ control technique, the reactive power supplied by the series inverter increases by a factor of k_O. Moreover, the value of factor k_O is always greater than 1 during the voltage sag (see Table 6.2). Similarly, under voltage swell the reactive power supplied by series inverter reduces due to decrease in source current magnitude.

The other possible approach is to maintain the reactive power supplied by both the inverters same under all the conditions. As the source current increases or decreases during the voltage sag or swell condition, to achieve the above mentioned constraint, the power angle δ by (6.88) should change accordingly. Let's define this control approach as *variable power angle* control technique.

Using (6.88) the necessary decrease or increase in δ angle can be computed as:

$$\sin\delta_v = \frac{Q_{Sr}}{k_O.(k.I_S)} = \frac{Q_{Sr}}{k_O.p_S} = \frac{Q_{Sr}}{k_O.p_L} \tag{6.91}$$

Where, δ_v defines the variable power angle control under voltage sag/swell condition.

6.7 UPQC Controller Development

The controller development to achieve fixed and variable power angle control techniques is given in this section. The steps essential to determine the necessary power angle and reference series injected voltage signal, to maintain the load voltage at desired voltage profile while performing the load reactive power sharing is also given.

6.7.1 Fixed Power Angle (δ_f) Control Approach

The controller to achieve the fixed power angle δ_f between the source and load voltages, during the steady-state, voltage sag and swell, is exactly the same as already discussed in CHAPTER 5. Figure 6.9 is a re-representation of Figure 5.6. It is essential to point out that as the series inverter maintains the load voltage at desired level, the reactive power demanded by the load remains constant irrespective of changes in the source voltage magnitude. Moreover, the reactive power shared by shunt inverter is fixed to a predefined value, $Q_{sh,max}$, the power angle δ remains unchanged. Note that this fixed shunt inverter reactive power limit is used just to compute the instantaneous power angle δ. The actual reactive power handled by the shunt inverter may vary based on the load requirements. As the power angle δ remains constant under different operating conditions, the reactive power shared by the series inverter and hence by the shunt inverter changes as given by (6.88) and (6.90).

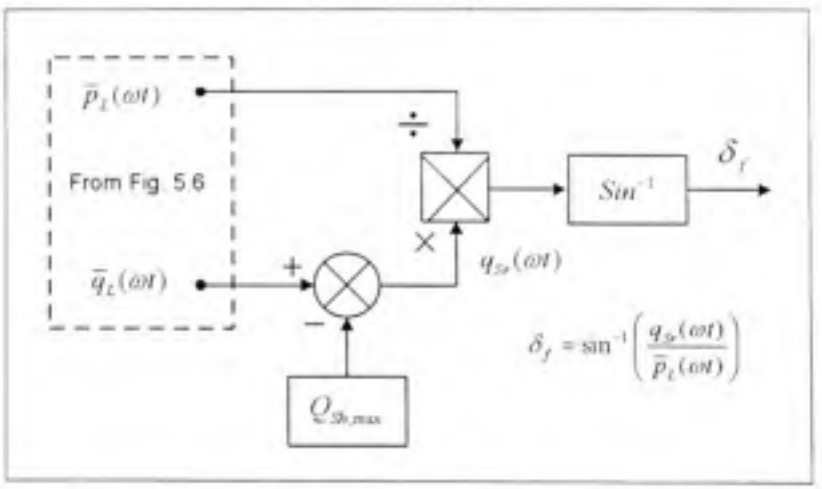


Figure 6.9 Control diagram for fixed power angle control approach.

6.7.2 Variable Power Angle (δ_v) Control Approach

In case of variable power angle (δ_v), the reactive power shared by series inverter is maintained at same level as that of steady-state value. As discussed in the previous section, to maintain the reactive power shared by series inverter at normal steady-state value, the power angle δ needs to change.

Figure 6.10 shows a block diagram representation to achieve the variable power angle δ_v based controller, realized using (6.91). During normal working condition, the factor k_O will be 1, therefore, δ_v will be the same as that computed utilizing fixed power angle control approach. The increase or decrease in source voltage magnitude will tend to change the value of factor k_O from 1, and thus, the power angle will change accordingly.

Note that the computed instantaneous reactive power shared by the series inverter $q_{Sr}(\omega t)$ has identical values (Figure 6.9 and Figure 6.10). However, the factor k_O in variable power angle control technique adjusts the instantaneous angle δ to maintain the fix value of series inverter reactive power.

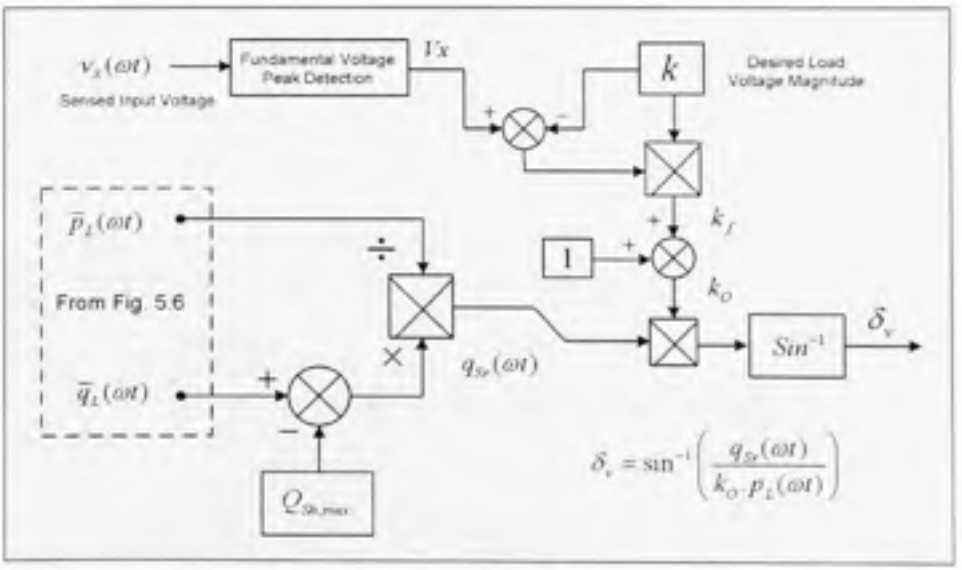


Figure 6.10 Control diagram for variable angle control approach.

6.7.3 Generalized Controller for Series Inverter

Under variable source conditions, the source voltage may reduce (sag), increase (swell) or may get distorted (harmonics). Therefore, the controller for series inverter should generate a reference voltage signal which would be a combination of, *i*) a voltage component for load reactive power compensation using PAC concept (fixed or variable power angle based approach), *ii*) a voltage component for voltage sag or swell compensation, using active power control approach, and finally *iii*) a harmonics component to compensate for any distortion present in the source voltage. Figure 6.11 shows the single-line control block diagram for series inverter to tackle all the aforementioned tasks. The control diagram for shunt inverter is similar to one given in Figure 5.8. As noticed from the Figure 6.11, the desired load voltage profile is generated using unit vector template approach and then compared with actual source voltage profile. The output voltage signal $v^*_{Sr,dist}$ gives the required injection voltage profile that could be the voltage sag/swell component or harmonics component or a combination of both components. The signal $v^*_{Sr,dist}$ is then added to the reference voltage signal essential to implement PAC. The reference signal thus generated ($v^*_{Sr,invt}$) gives the necessary series injection voltage magnitude that will share the load reactive power and compensate for voltage sag/swell and harmonics, simultaneously.

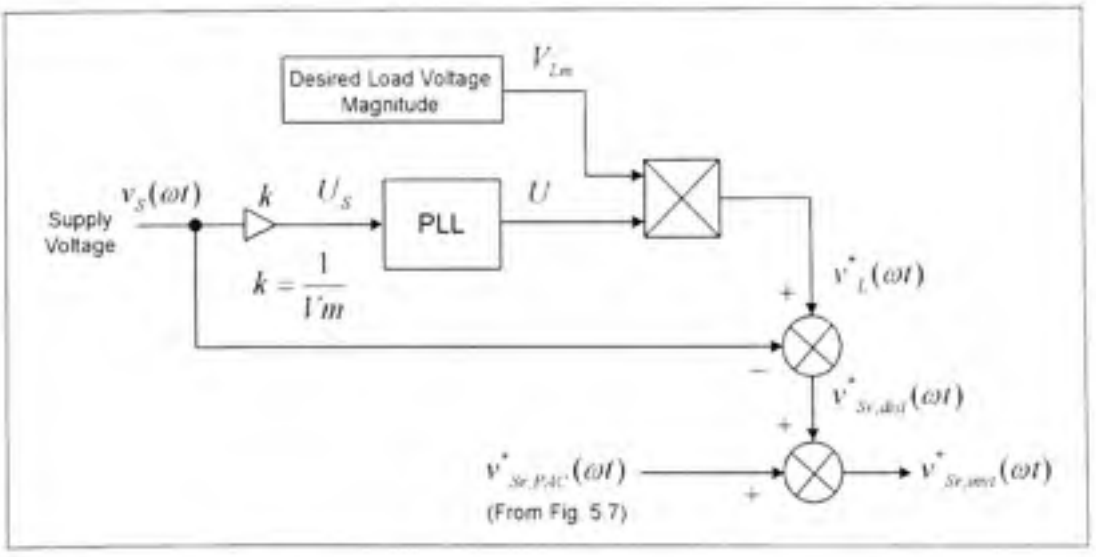


Figure 6.11 Generalized reference voltage signal generation for series inverter based on PAC approach.

6.8 Simulation Results

This section discusses the simulation results to evaluate the performance of PAC concept under voltage sag and swell conditions. Both the fixed and variable power angle technique based controller performances are discussed. Additionally, simulation results under distorted condition are also presented. The system parameters and the load are kept same as used in CHAPTER 5 (RL Load: 15 kW + *j* 15 kVAR).

6.8.1 Fixed Power Angle Based PAC Performance under Voltage Sag and Swell Conditions

The simulation results for PAC approach implemented using fixed power angle based concept are given in Figure 6.12. Before time t6, the UPQC system is working under steady-state condition (S. S.) to compensate the load reactive power using both the inverters. At time t6=0.6 sec, a sag of 20% is introduced on the system (sag last till time t=0.7 sec). Between the time period t=0.7 and t=0.8 sec, the system is again in the steady-state. A swell of 20% is imposed on the system for a time period of t7=0.8 sec to 0.9 sec. The active and reactive power flow through the source, load and UPQC are given in Figure 6.13. The peak values of the source and the shunt inverter currents, the series injected voltage and important phase angles are also shown in Figure 6.13.

The significant features of fixed power angle based PAC approach are outlined as:

- The load voltage profile is maintained at a desired level irrespective of decrease or increase in the source voltage magnitudes (Figure 6.12 (a) and (b)).
- During the sag/swell compensation, utilizing active power control (UPQC-P), to maintain the appropriate active power balance in the network, the source current increases during the voltage sag and reduces during swell (Figure 6.12 (f)).
- Note that the power angle between the source and load voltages during the steady-state (Figure 6.12 (e)), voltage sag (Figure 6.12 (i)), and voltage swell (Figure 6.12 (j)), remains unchanged to 21^{o} (also see Figure 6.12 (f)). As power angle δ remains

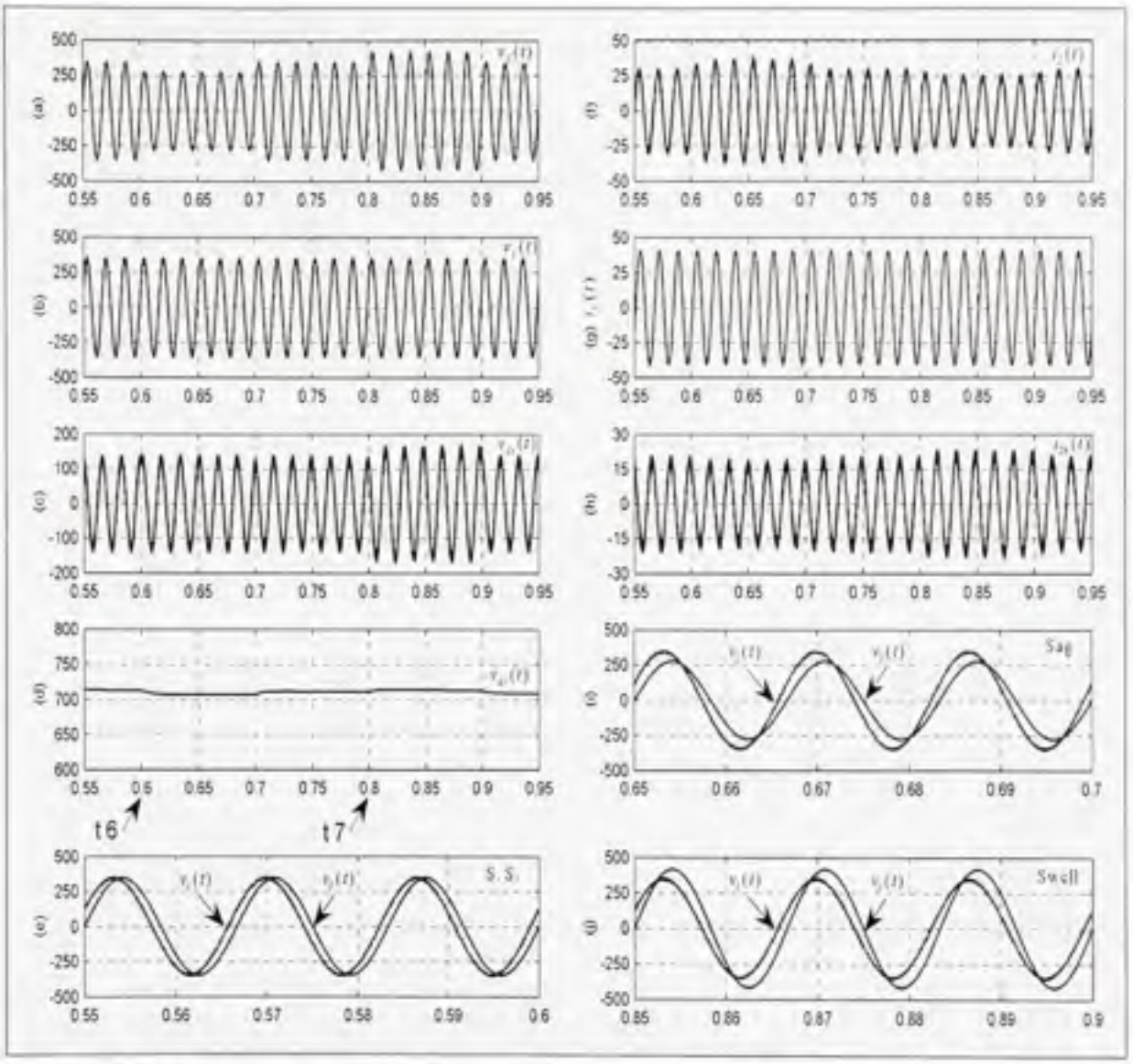


Figure 6.12 Simulation results: Fixed power angle based PAC performance during voltage sag and swell conditions.

the same during steady-state, voltage sag and swell conditions, this technique is termed as "fixed" power angle control technique.

- To compensate equal percentage of sag and swell, the PAC approach requires smaller series injection voltage magnitude for voltage sag as compared to the voltage swell.
- The power supplied by source and the power consumed by the load remains identical.
- The reactive power supplied by the series inverter, during the voltage sag condition increases due to the increased source current. As load reactive power demand is

constant, the reactive power supplied by the shunt inverter reduces accordingly. On the other hand, during the voltage swell condition, the reactive power shared by the series inverter reduces and shunt inverter increases (see Figure 6.13 (c) and (d)). The reduction and increment in shunt compensating current magnitude (Figure 6.13 (e)) also confirms the abovementioned fact.

- Although the reactive power shared by the series and shunt inverters is varied, the sum of their reactive powers always equals the reactive power demanded by the load.

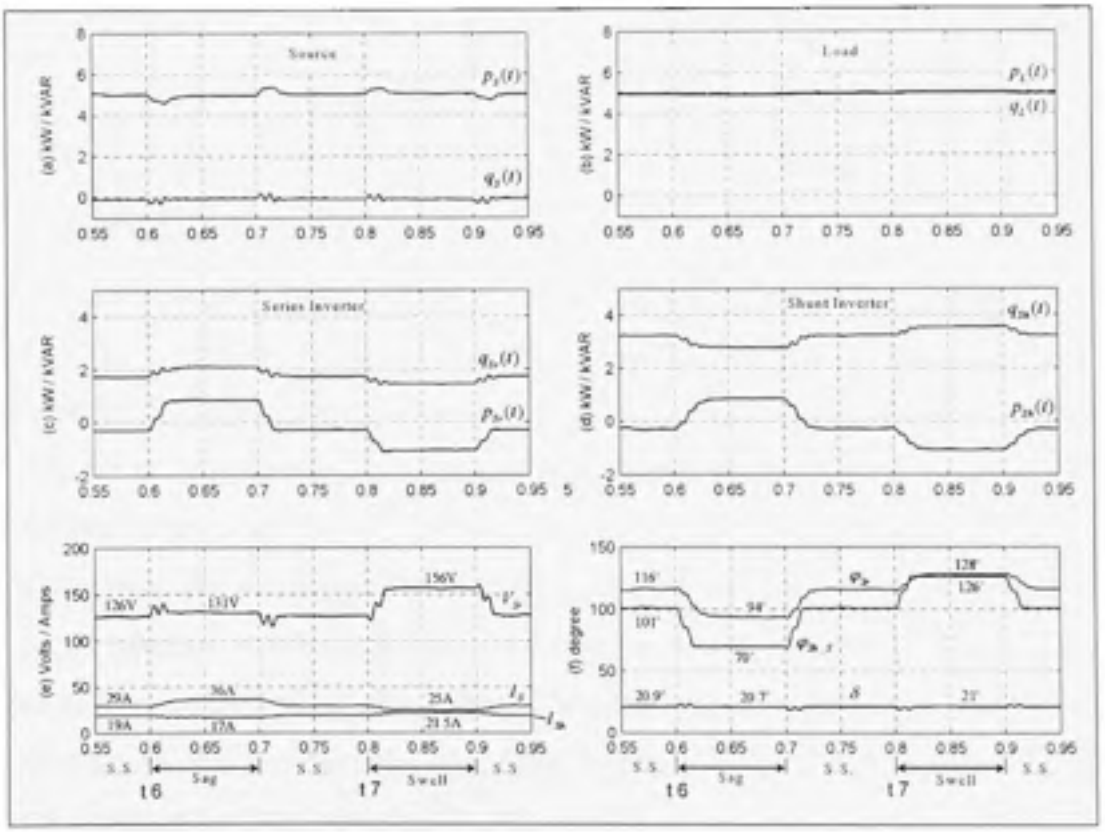


Figure 6.13 Simulation results: active – reactive power flow under fixed power angle based PAC approach.

6.8.2 Variable Power Angle Based PAC Performance under Voltage Sag and Swell Conditions

The simulation results based on variable power angle control technique are given in Figure 6.14 and Figure 6.15. All the conditions and parameters are kept identical to the one used for fixed power angle control technique.

The distinctive features of variable power angle based PAC approach are described and compared with fixed power angle control technique:

- The load voltage profile is effectively maintained at a desired level during voltage sag and swell condition (Figure 6.14 (a) and (b)).
- As noticed from the Figure 6.15 (e) and Figure 6.13 (e), irrespective of fixed or variable power angle control, the source delivers almost same amount of currents to compensate for voltage sag and swell on the system.
- The power angle between the source and load voltages during the voltage sag (Figure 6.14 (i)) is reduced to 16.5^{o} as compared to steady state value of 20.9^{o} (Figure 6.14 (e)). On the other hand, during the voltage swell, the power angle δ is increased to 26^{o}. Since, power angle δ changes during supply voltage sag and swell conditions, this technique is termed as "variable" power angle control approach.
- To compensate equal percentage of sag, the variable δ control requires slightly lesser series injection voltage magnitude compared to the fixed δ control. For equal amount of voltage swell, the variable δ control requires higher magnitude of injection voltage than the fixed δ control technique. This is due to the increased power angle between the resultant load and source voltages.
- The power handled by the source and the load remains identical to the steady-state values.
- Note: The reactive power supplied by the series and shunt inverter, during the voltage sag and swell, maintained at the constant level equals to the steady-state value, irrespective of the increase or decrease in the source current magnitude (Figure 6.15 (c) and (d)). Also, note that the shunt compensating current magnitude remains almost constant during all the conditions.

- The major factor to achieve the fixed reactive power sharing (as in variable power angle control) and the variable reactive power sharing (as in fixed power angle control) features is obtained by controlling the magnitude and the phase angles of the injected voltage and current of the UPQC. The difference in these quantities can be noticed from the Figure 6.13 (f) and Figure 6.15 (f).

In summary, the proposed PAC concept effectively compensates the voltage sag and swell on the system. Two different control techniques, namely, variable δ and fixed δ control are introduced to give high degree of freedom for optimal utilization of UPQC under variable voltage condition.

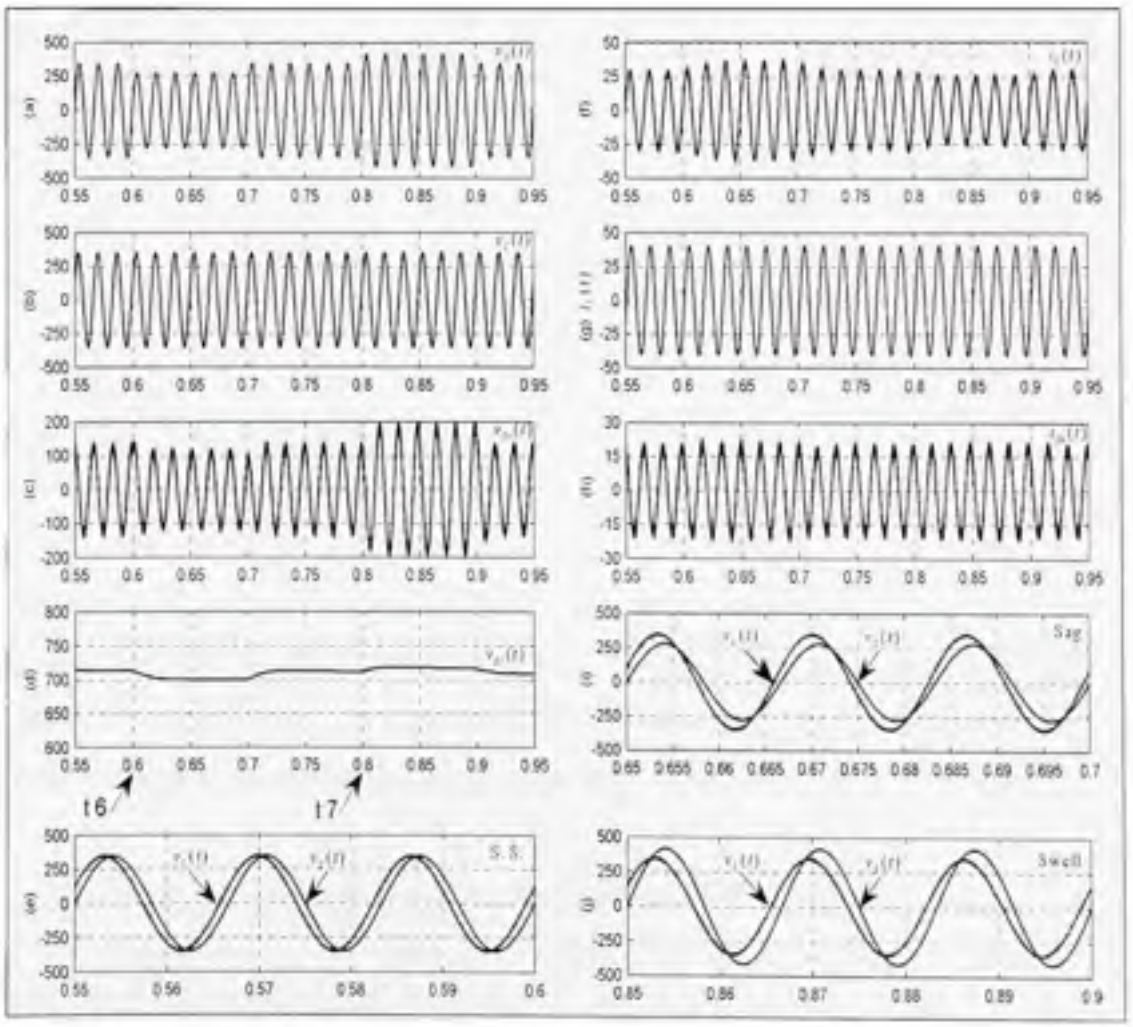


Figure 6.14 Simulation results: variable power angle based PAC performance during voltage sag and swell conditions.

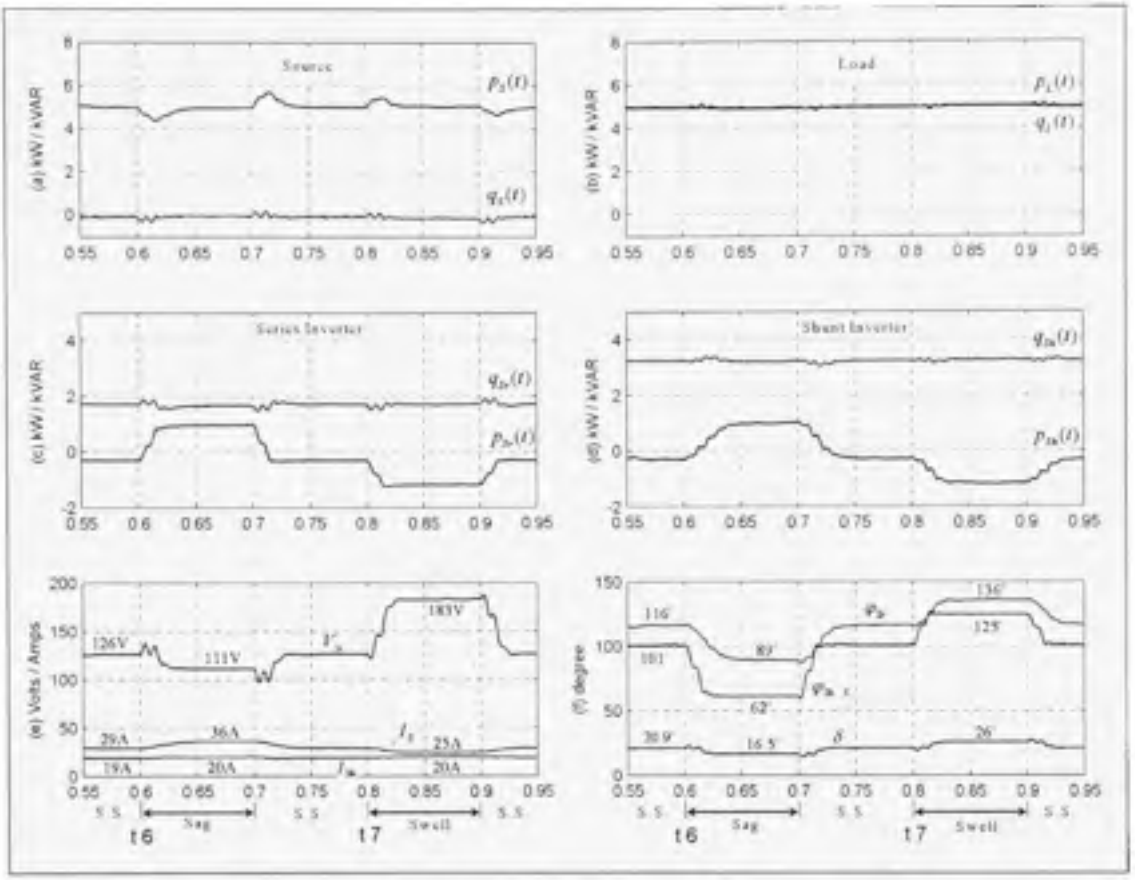


Figure 6.15 Simulation results: active – reactive power flow under variable power angle based PAC approach.

6.8.3 PAC Performance under Distorted Conditions

The performance of UPQC under distorted supply voltage and under non-linear load is discussed here. At time t8=1 sec, distortion in supply voltage is introduced. The supply voltage has THD of 12.5% with dominant 5^{th} and 7^{th} harmonics of 10% and 7.5%, respectively. As noticed from the Figure 6.16 (b), after time t8, the load voltage (2% THD) is maintained at desired value by injecting appropriate voltage through series inverter.

At time t9=1.1 sec, the load on the network is changed from highly inductive to a non-linear load. The distorted load current profile is shown in Figure 6.16 (e), has a THD of 26.3% with dominant 5^{th}, 7^{th}, and 11^{th} harmonics of 22%, 9.96%, and 7.4%, respectively. As viewed from Figure 6.16 (d), after time t9, the shunt inverter effectively compensates the harmonic

generated by non-linear load by injecting appropriate compensating current. Note that under the above mentioned distorted condition, the UPQC shares the load reactive power demands between the shunt and series inverters in addition to the voltage and current harmonics compensation.

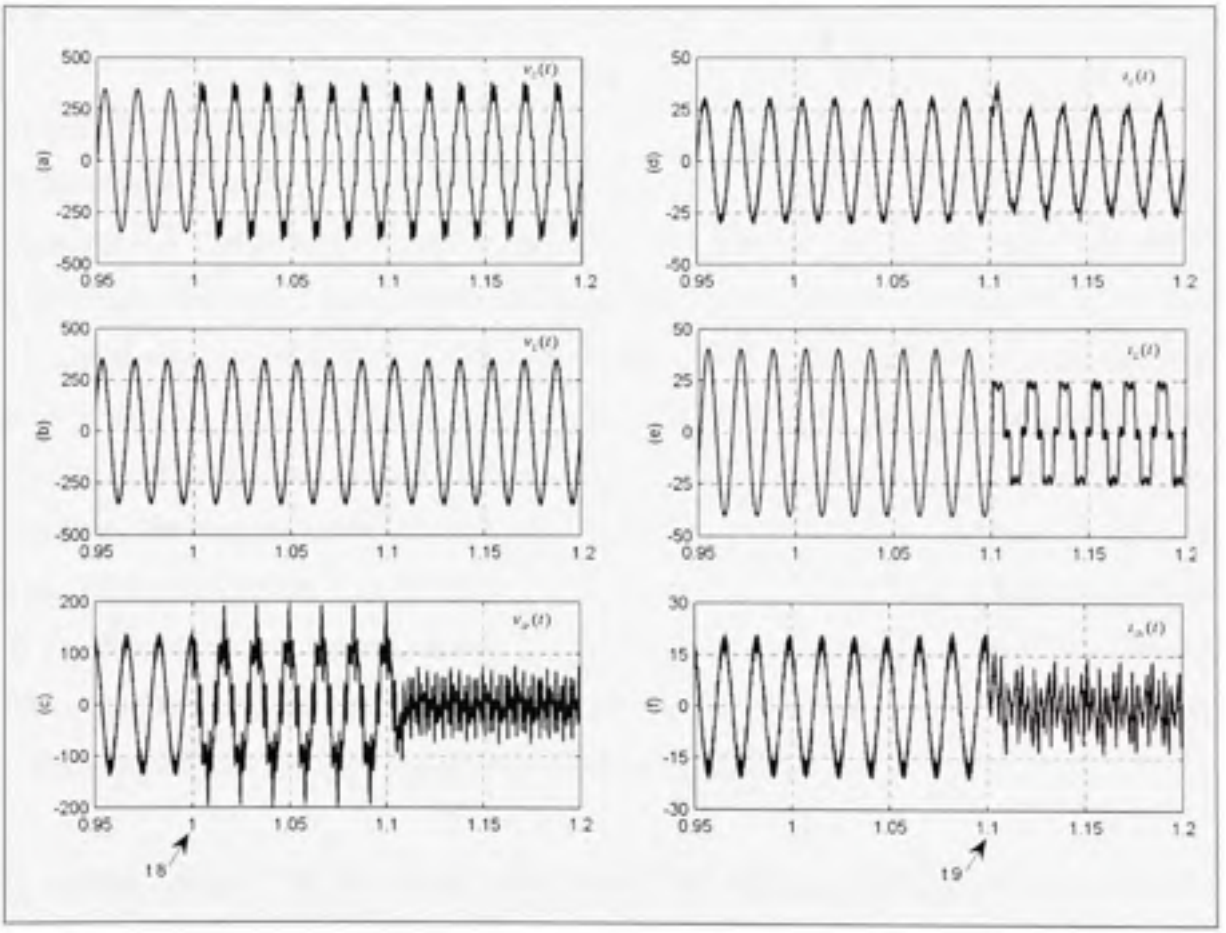


Figure 6.16 Simulation results: performance of PAC approach under distorted supply voltage and non-linear load (using δ_f).

6.9 Experimental Results

In this section, the performance of PAC approach, with fixed power angle δ_f, under voltage sag, swell and distorted supply voltage is validated through experimental study. All the parameters and the load conditions are identical as that discussed and used in CHAPTER5.

6.9.1 Performance of PAC under Voltage Sag Condition

The experimental results during the voltage sag on the system are shown in Figure 6.17. It is considered that the UPQC is already working under PAC (with fixed power angle δ_f control technique) and shares the load reactive power (load power factor 0.6 lagging) utilizing both the inverters. The power angle δ between the load and source voltages is found as 10^0. Under such condition, a sag of 17% is introduced on the system. The reduced source voltage profile can be noticed from the Figure 6.17 (a) [upper trace]. The UPQC with the proposed PAC theory maintains the load voltage at a desired level while supporting the load reactive power using both the inverters. As discussed previously, there is a slight increase in the source current magnitude (from 1.5A to 1.65A) in order to achieve an effective sag compensation. The resultant load and source voltage profiles are compared in Figure 6.17 (b). Note the effect of reduced supply voltage does not appear across the load terminal. The power angle 10^0 between the two voltages is also noticeable in the figure.

The voltage injected by the series inverter and the shunt current during the voltage sag compensation mode of operation are given in Figure 6.17 (c). The presence of in-phase voltage component (v_{sr2}) in addition to the load reactive power component (v_{sr1}) can be observed from the series injected voltage profile (trace-3). The performance of the shunt inverter is plotted in Figure 6.17 (d). Comparing Figure 5.20 (b) and Figure 6.17 (d), the slightly increased source and shunt current magnitudes can be noticed during the voltage sag compensation. Figure 6.18 gives the experimental results showing the source, load and series injected voltages under 17% and 28% of sags with power angles $\delta=10^0$ and $\delta=15^0$.

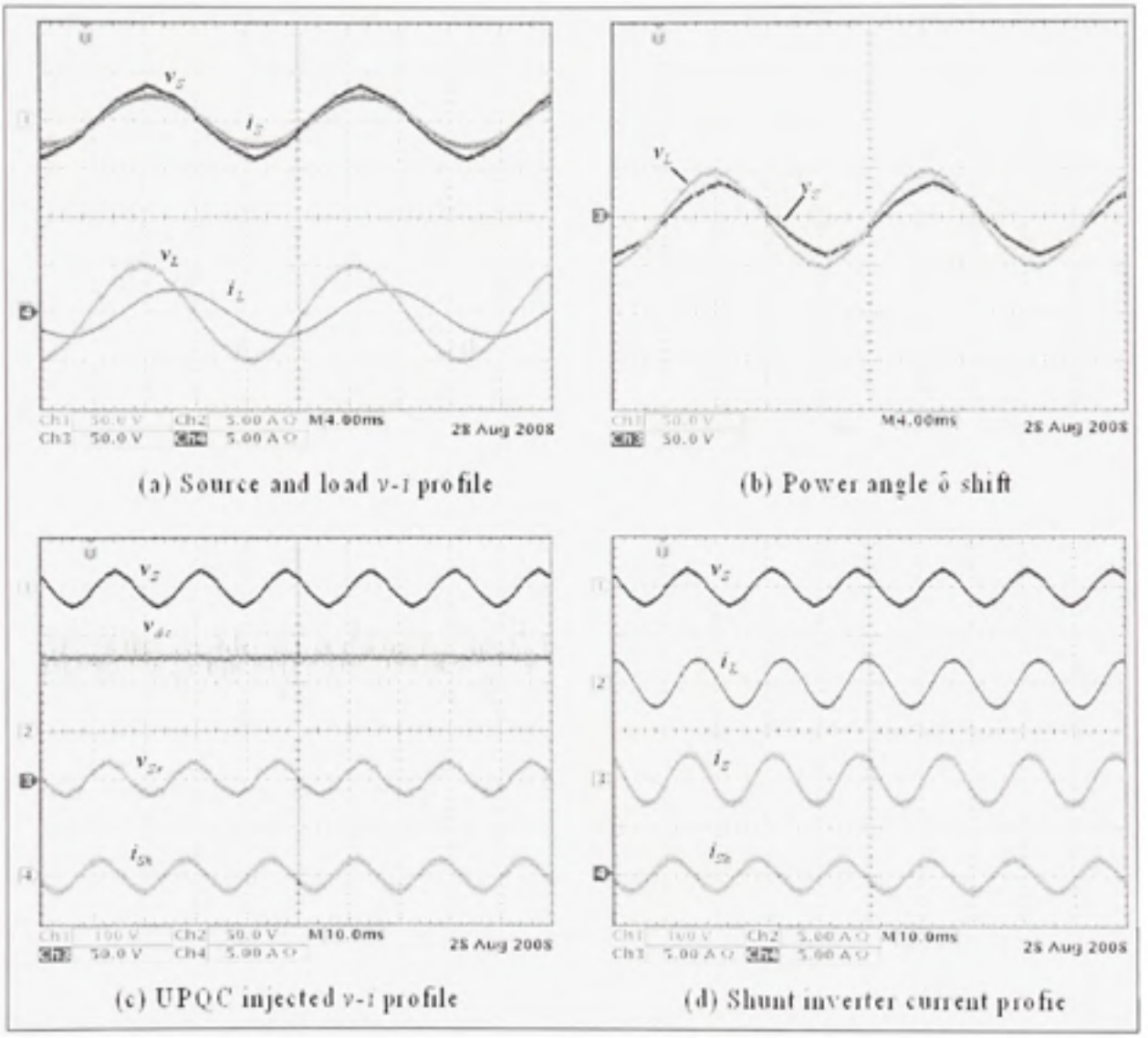


Figure 6.17 Experimental results: performance of PAC (δ_f) approach under voltage sag condition (Sag =17%, δ=10°).

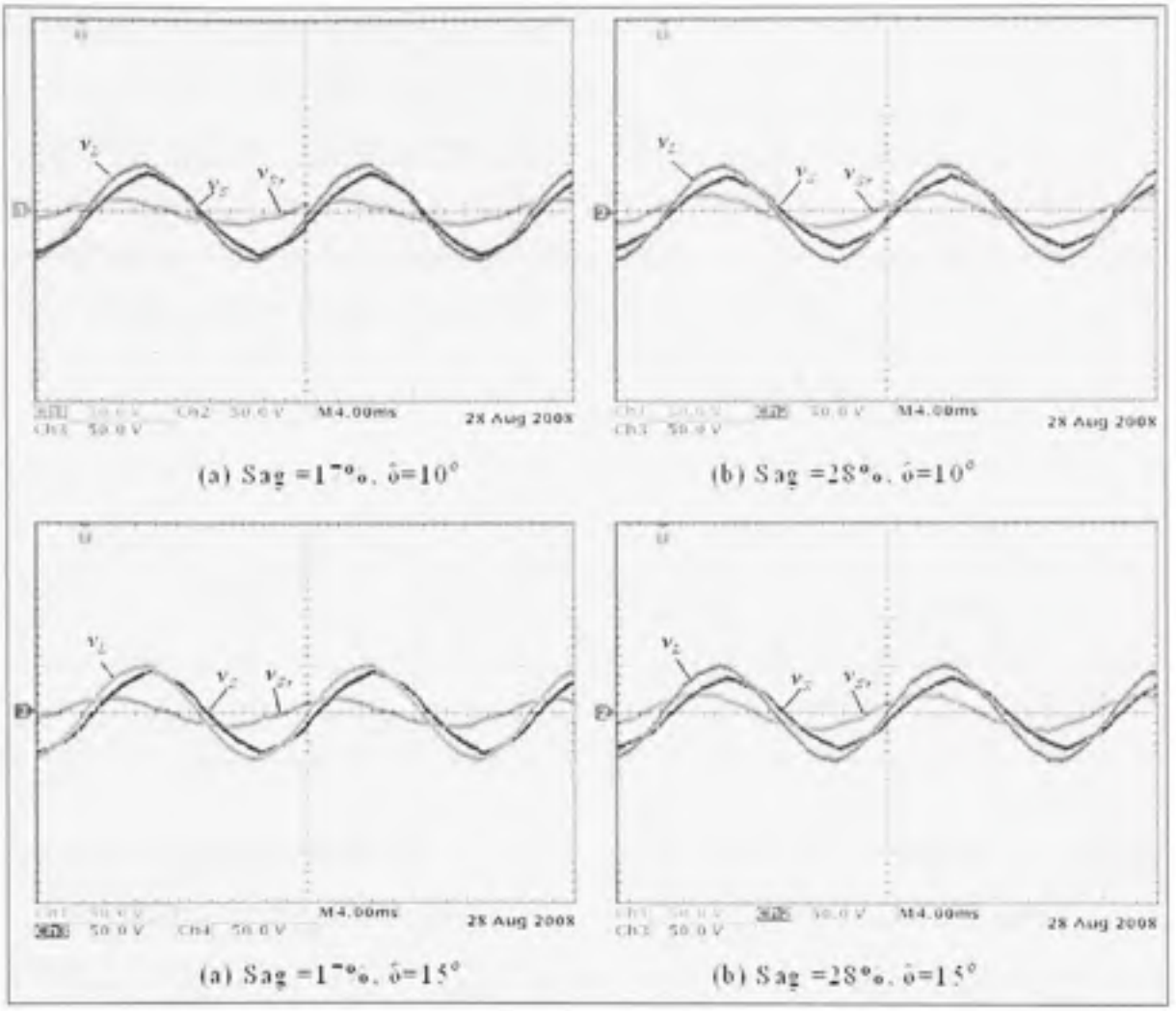


Figure 6.18 Experimental results: performance of PAC (δ_f) approach under different voltage sags and power angles.

6.9.2 Performance of PAC under Voltage Swell Condition

The experimental results during a voltage swell (22%) on the system are shown in Figure 6.19. The increased source voltage profile can be noticed from the Figure 6.19 (a) [upper trace]. The UPQC with proposed PAC theory maintains the load voltage at the desired level while supporting the load reactive power using both the inverter [Figure 6.19 (a), lower trace]. The slightly reduced source current can also be noticed. Figure 6.19 (b) shows the profiles of both the load and source voltages. Note that the effect of increased supply voltage does not appear across the load terminal. The voltage injected by the series inverter and the

shunt current during the voltage swell compensation mode of operation are given in Figure 6.19 (c). The series injected voltage which is the sum of an out-phase voltage component (v_{sr3}) and the load reactive power component (v_{sr1}) can be viewed from Figure 6.19 (trace-3). The performance of shunt inverter is plotted in Figure 6.19 (d). The experimental results showing the source, load and series injected voltage under two different percentages of sags with two different power angles are given in Figure 6.20.

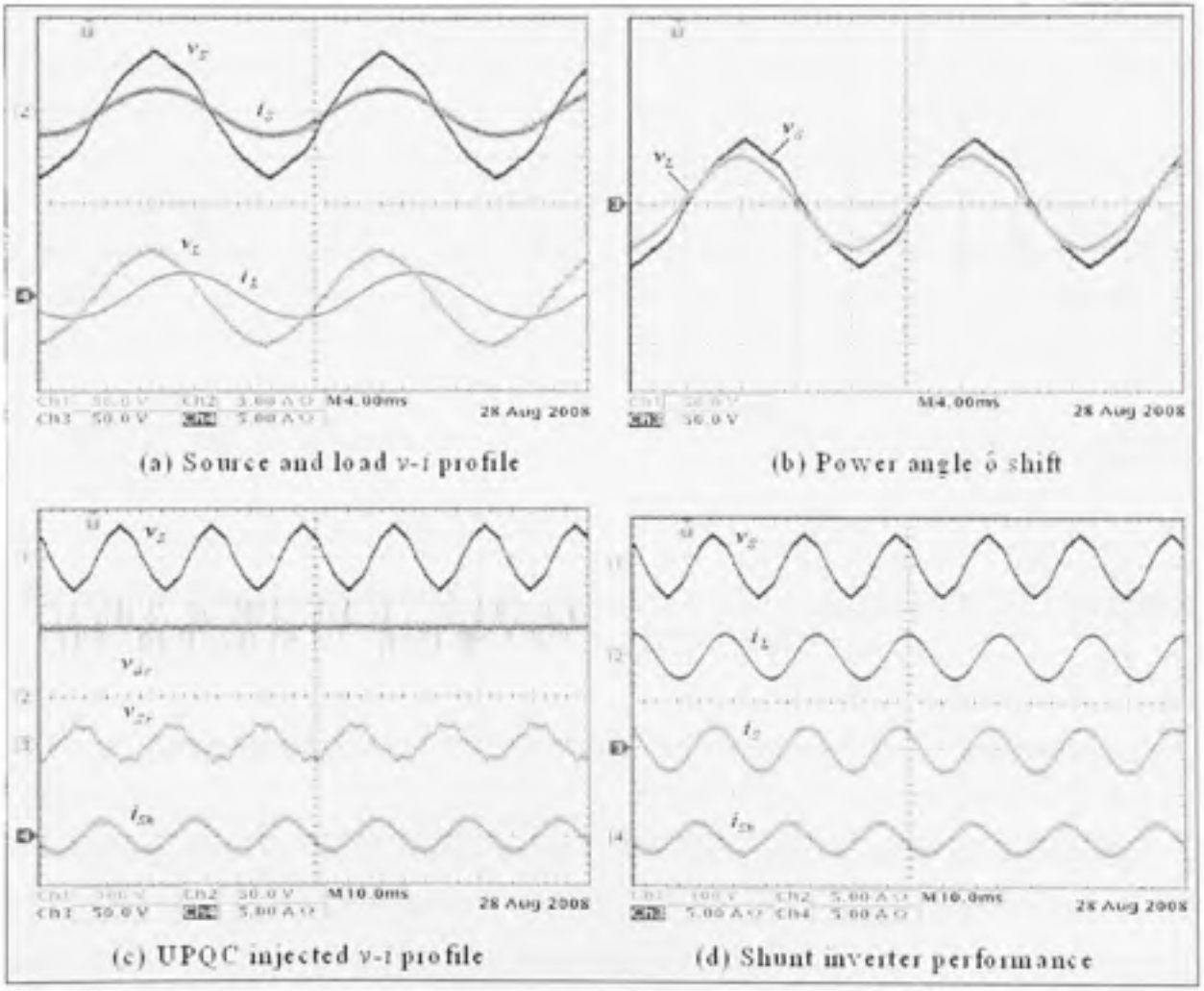


Figure 6.19 Experimental results: performance of PAC approach (δ_f) under voltage swell condition (Swell =22%, δ=10°).

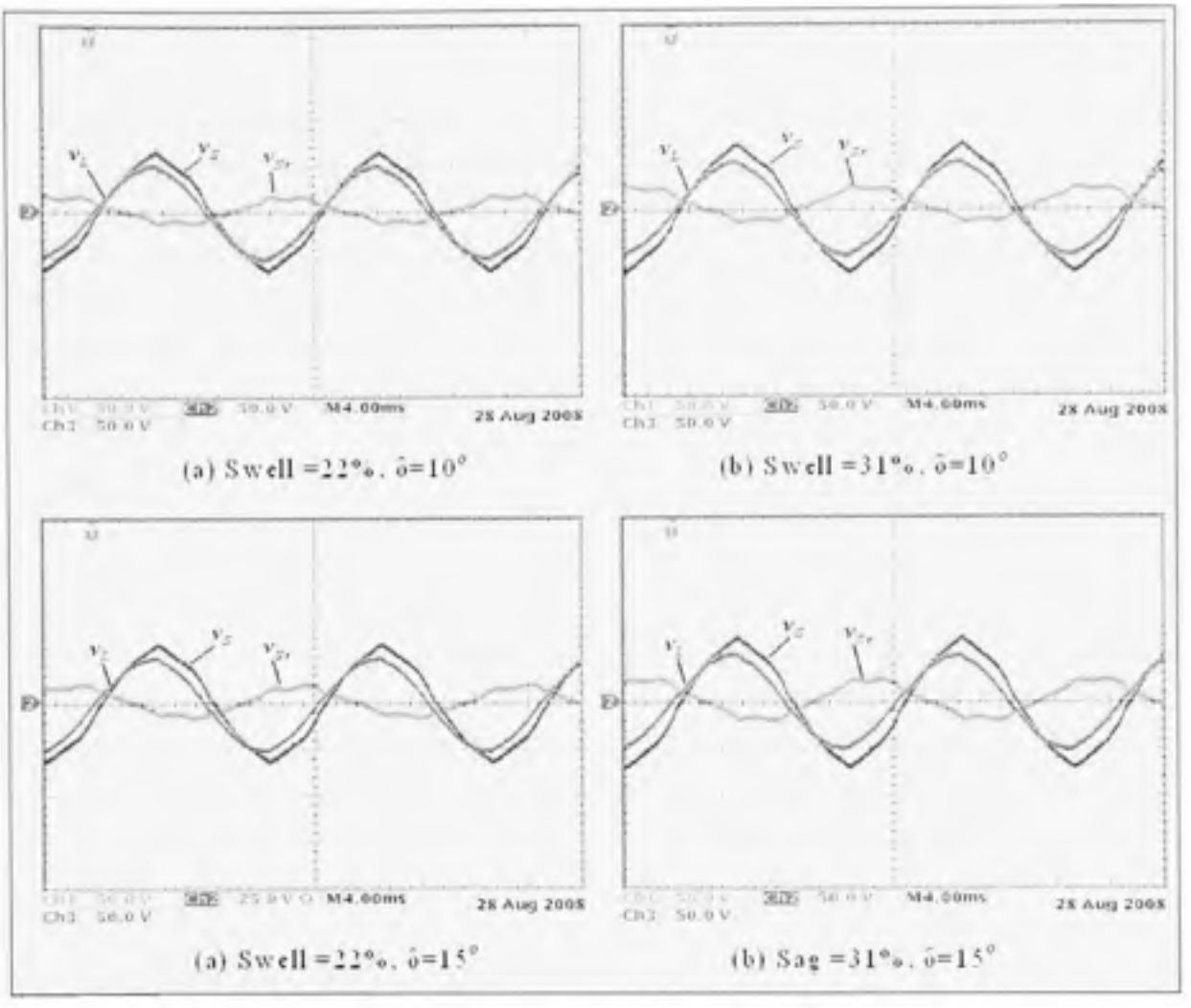


Figure 6.20 Experimental results: performance of PAC (δ_f) approach under different voltage swells and power angles.

6.9.3 Dynamic Performance of PAC during Voltage Sag\Swell Conditions

The dynamic performance of UPQC with proposed PAC under momentary occurrence of the voltage sag and the voltage swell is given in Figure 6.21 and Figure 6.22, respectively. The scaled profiles of the source, load and series injected voltages are also given in the respective figures. Note that the UPQC maintains the load voltage at constant level irrespective of changes (decrease or increase) in the source voltage. The power angle δ between the resultant load voltage and the actual source voltage can also be noticed from the scaled figures. In both the cases, the UPQC shares the load reactive power utilizing the shunt and series inverters.

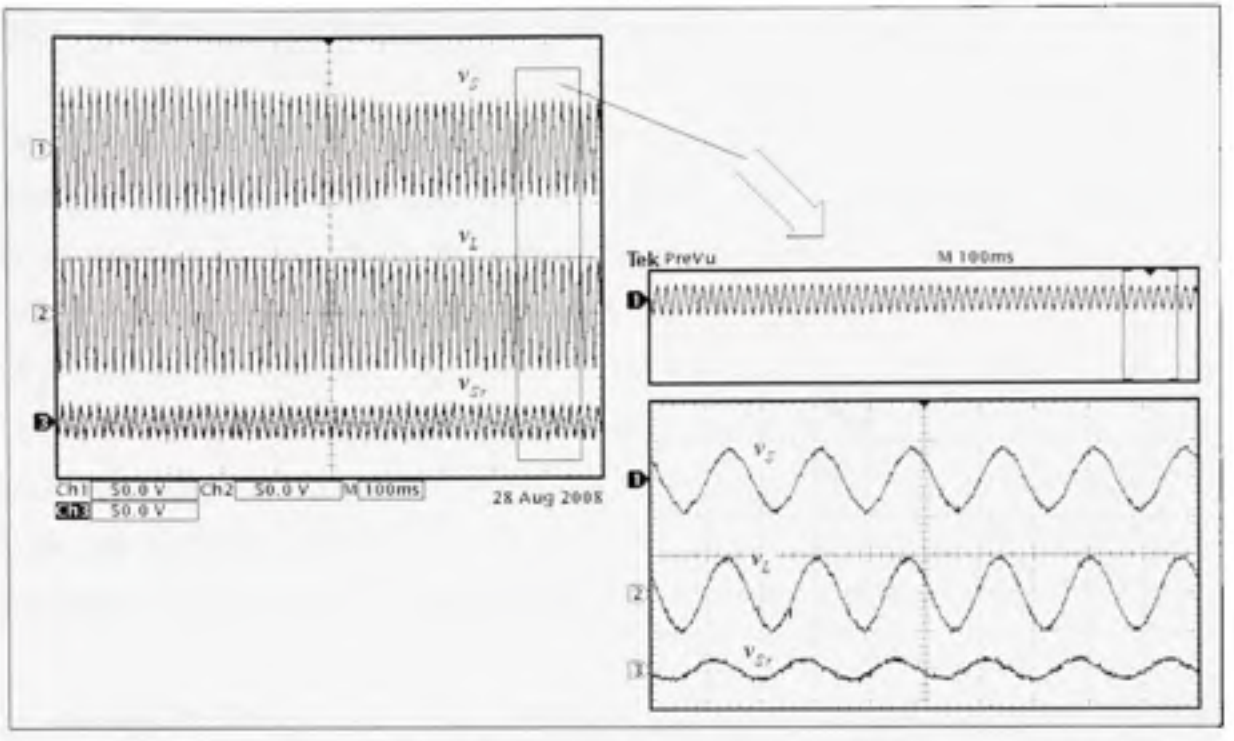


Figure 6.21 Experimental results: dynamic performance of PAC approach during momentary voltage sag condition.

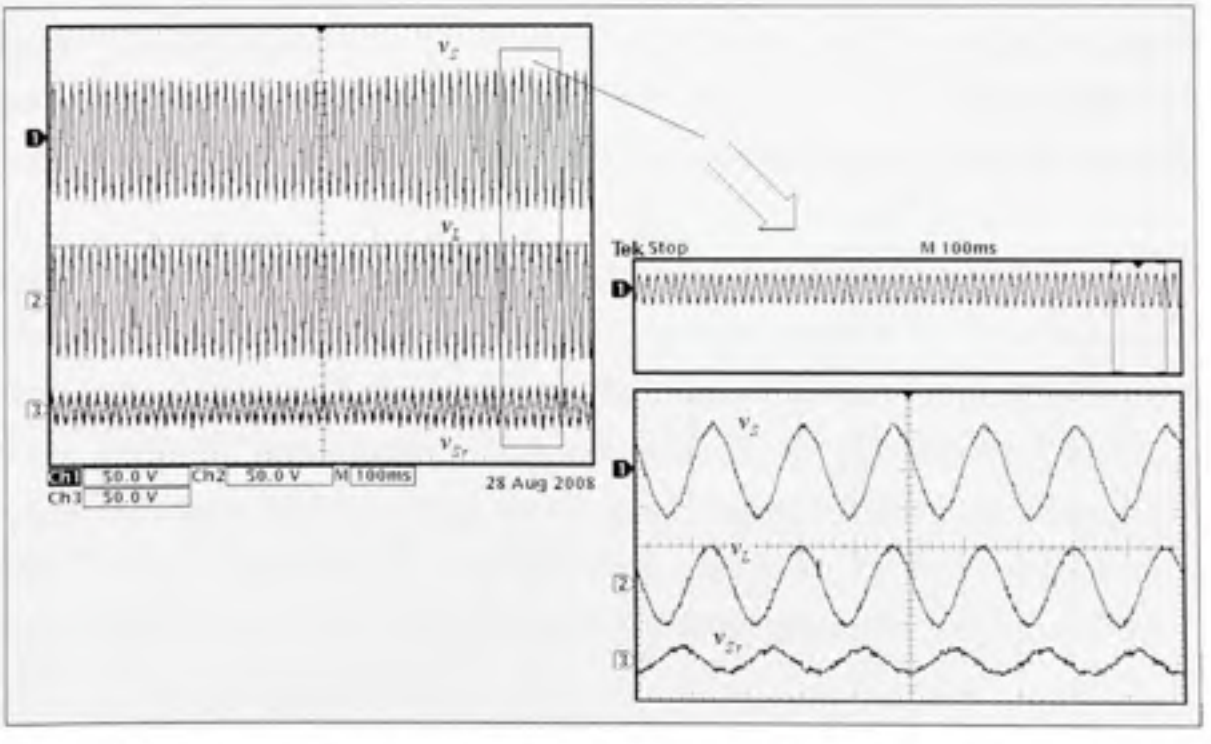


Figure 6.22 Experimental results: dynamic performance of PAC approach during momentary voltage swell condition.

6.9.4 Performance of PAC under Distorted Source Voltage

Finally, the performance of proposed PAC approach under distorted source voltage and non-linear load conditions is highlighted in this section. Some of the significant experimental results are given in Figure 6.23. The distorted source voltage profile can be noticed from the Figure 6.23 (a). The source voltage has THD of 6.6%, with dominant 3rd (5.98%) and 5th (2.02%) harmonics. The load on the system is a combination of a highly inductive load (same as used for steady-state, sag-swell conditions) and a non-linear load realized using a single-phase diode bridge rectifier followed a capacitor and RL load. The distorted load current profile can also be noticed from the Figure 6.23 (a). The load current has THD of 23.4% with dominant 3rd (17.1%) and 5th (9.7%) harmonics.

The experimental results, when, only the series inverter is put into operation are shown in Figure 6.23 (b). The series inverter compensates the harmonics present in the source voltage such that the load voltage profile is maintained perfectly sinusoidal. Moreover, the series inverter also compensates the part of the load reactive power as defined by the proposed PAC approach. The power angle boost (δ=24°) between the resultant load voltage and the distorted source voltage can be observed from Figure 6.23 (b). Also note the improvement in the effective load power factor angle between the resultant source current and the source voltage.

Figure 6.23 (c) shows the experimental results when the shunt inverter is also put into operation. The remaining load reactive power is now supplied by the shunt inverter. Moreover, the shunt inverter also cancels out the harmonics generated by the non-linear load, and thus makes the source current perfect sinusoidal and in-phase with the source current. The improvement in the load voltage and the source current THDs are noticed as 3.2% (3rd 2.3%, 5th 0.78%) and 2.94% (3rd 1.5%, 5th 1.9%), respectively. For better visualization, the distorted source and compensated load voltages are plotted separately in Figure 6.23 (d).

The voltage and current injected by series and shunt inverters together with self-supporting DC bus voltage are given in Figure 6.23 (e). Note that, to eliminate the distortion present in

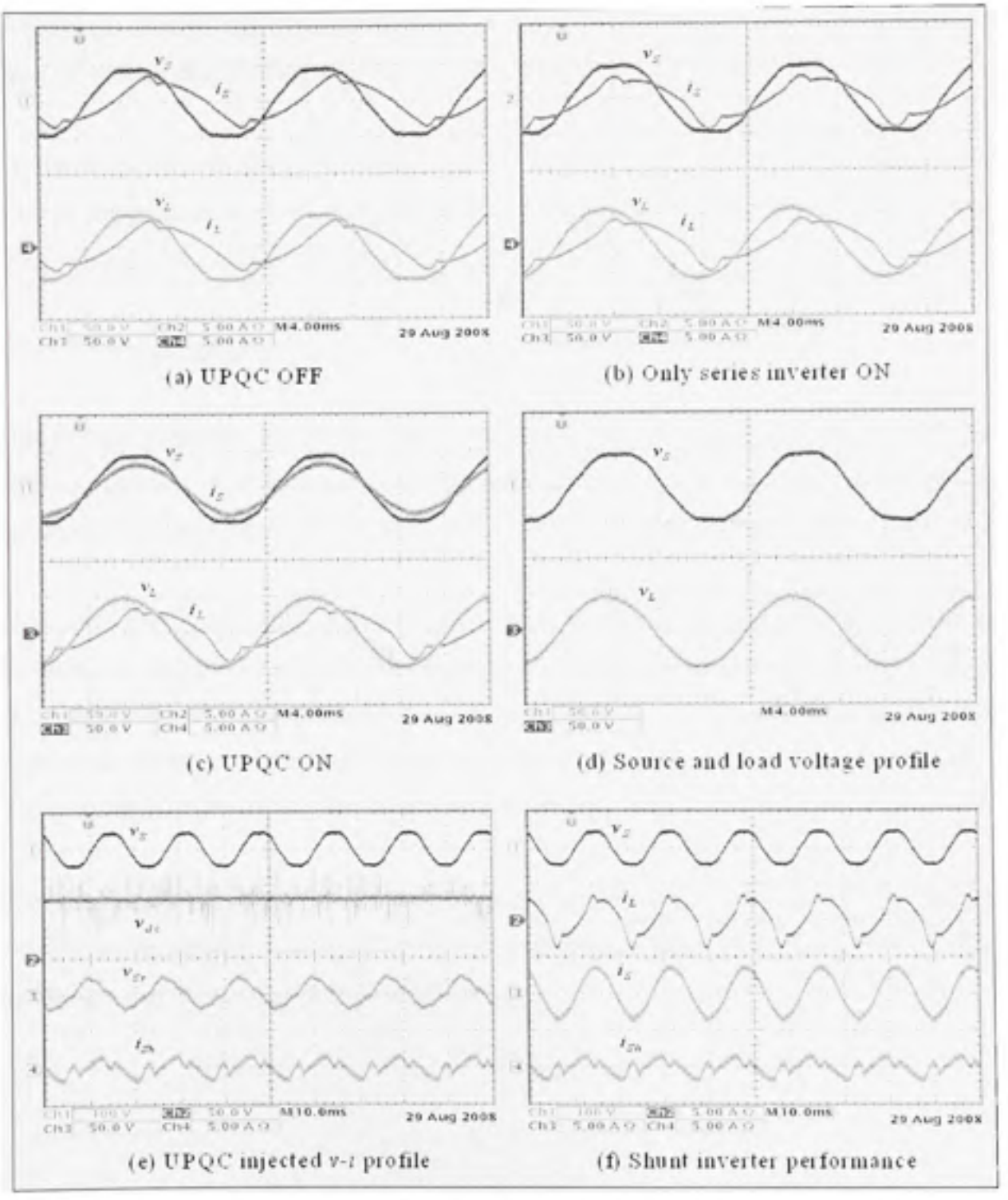


Figure 6.23 Experimental results: performance of PAC (δ_f) approach under distorted condition (δ=24°).

the source voltage and the load current, the UPQC injects the required harmonics components through the series and shunt inverters, respectively. The performance of the shunt inverter is shown in Figure 6.23 (f).

As observed from the above experimental investigation, the UPQC with the proposed PAC concept compensates the voltage harmonics, current harmonics and handles the load reactive power through the series and shunt inverters, simultaneously.

6.10 Conclusions

This chapter elaborates the proposed theory of power angle control of UPQC under different utility conditions, which includes the steady-state, voltage sag, voltage swell and the voltage distortion, and demonstrates its capabilities to overcome different power quality issues.

The developed generalized performance equations are important to predetermine the performance of UPQC under various operating conditions. The newly introduced fixed and variable power angle δ control techniques are useful to estimate the reactive power shared by each of the inverters, particularly, under the voltage sag and swell conditions. Moreover, it also gives high degree of freedom to optimize the ratings of both the inverters.

Both the simulation and the experimental results confirm the accomplishment of proposed reactive power sharing feature of the UPQC under the voltage sag, voltage swell, voltage harmonics, and the non-linear load conditions.

CONCLUSIONS

This thesis presents a comprehensive research work in the area of power quality enhancement utilizing the unified power quality conditioner (UPQC). It addresses the control and real-time implementation aspects of UPQC for possible practical applications. Several new concepts are introduced, supported by thorough analytical studies, confirmed using digital simulation results and finally, validated through experimental investigations. Moreover, the scope of presented work covers single-phase, three-phase three-wire and three-phase four-wire UPQC based systems.

The significant conclusions of this thesis work are summarized as follows:

- A conceptual analysis to understand the active and reactive power flow between source, UPQC and the load under different operating conditions is carried out. Based on the given analytical study, a numerical example shows the impact of sag and swell on the current and voltage injected by UPQC. The purpose of this analysis is to predetermine the amount of power (current) that would flow during different operating conditions. This first step helps to compute the ratings of UPQC inverters based on the system and application requirements.

- The feasibility of UPQC for practical distribution level installation has been validated successfully under realistic network model. The reported collaboration project work between ÉTS, Hydro-Québec and IREQ supports the future prospective for the UPQC being commercialized.

- A relatively simple control approach termed as Unit Vector Template Generation (UVTG) has been proposed for UPQC to tackle the most important power quality issues. UVTG scheme utilizes a phase locked loop (PLL) and a proportional - integral (PI) regulator to generate the reference signals for shunt and series inverters. Thus, the need of complex mathematical computation to realize the controller was

been eliminated. The performance of UVTG approach has been validated through simulation as well as experimental results.

- A special attention has been given to the voltage sag compensation, in which, the sag is tackled using reactive power control approach. The advantage of using reactive power to overcome the voltage sag is that it does not require any active power and hence helps to reduce the burden on the shunt inverter. A new approach to extract the required quadrature injection voltage has also been developed and successfully validated through simulation and experimental investigation.

- A comparative evaluation on the voltage sag compensation using active power (UPQC-P) and reactive power (UPQC-Q) approaches has also been carried out. The summarized advantages and limitations of both the concepts can help to select the most suitable approach depending on the particular application requirements.

- An innovative topology for UPQC based application has been presented, in which, a three-phase four-wire (3P4W) system is realized from a three-phase three-wire (3P3W) system. The neutral of series transformers, used in UPQC, is utilized to provide the neutral conductor (forth wire) to the load. The newly introduced topology can play an important role in future UPQC based distribution system.

- The load on the 3P4W system is most likely to be unbalanced in nature. In order to compensate the unbalance present in the load currents such that the source currents would appear perfectly balanced, a new control approach has been proposed. Due to the unbalanced nature of the load, the load active power demanded by each of the phases may not be the same. Therefore, the idea is to compute the instantaneous fundamental active power drawn by individual phases separately using the developed concept of generalized single-phase p-q theory. The total instantaneous fundamental load active power demand thus can be determined by adding individual phase active powers. This total load active power is then redistributed between utility and UPQC

(shunt inverter) as three-phase balanced power. The experimental results show that the unbalance of 45.76% present in the load current has been reduced to 1.08% at source side using the developed approach.

- The most important and significant contribution of this thesis work is in the development of a new control philosophy, termed as power angle control (PAC) of UPQC. The concept is to use the existing series inverter at its full capacity. The load reactive power demand is meticulously supported utilizing both the shunt and series inverters by introducing a phase angle boost between the source and the load voltages. To achieve the aforementioned task, a voltage through series inverter is injected in such a way that it does not cause a rise or decrease in the resultant load voltage, i.e. it strictly maintains the equal magnitudes of source and load voltages. This co-ordinated load reactive power sharing feature of UPQC results in the shunt inverter rating reduction. The simulation as well as the experimental results validate the effectiveness of the proposed approach. A systematic experimental study to show the effect of power angle on different UPQC parameters has also been carried out. Moreover, the experimental results show that for given laboratory load condition (high inductive load with power factor 0.6 lagging), with proposed PAC approach ($\delta = 28^{\circ}$) the shunt inverter rating can be reduced up to 50%. In other words, without putting extra burden on the existing system and without compromising the basic functionalities of UPQC, the rating of shunt inverter and hence the overall cost of UPQC can be reduced.

- The developed theory of PAC of UPQC has also been extended to incorporate the voltage sag and swell on the system. The performance equations of PAC approach are arranged in generalized manner to accommodate several operating conditions. On the course of controller development of UPQC under the voltage sag and swell conditions, two different control techniques, namely, fixed and variable power angle δ controls are introduced. Both the simulation and experimental results illustrate the capability of PAC approach to achieve the voltage sag/swell compensation while

sharing the load reactive power between the two inverters. The performance of PAC is also demonstrated under distorted source voltage and non-linear load conditions, where the UPQC compensates the voltage harmonics, load current harmonics and handles the load reactive power through the series and shunt inverters, simultaneously.

In summary, this thesis work puts forward a new control philosophy which not only improves the UPQC utilization factor but also reduces the overall system cost. Moreover, it also proves that with proper and meticulous control of available resources (in this case the series inverter) significant advantages can be achieved. The work reported in this thesis with extensive experimental validation would certainly be considered as a remarkable development in the field of power quality enhancement utilizing the unified power quality conditioner.

RECOMMENDATIONS

This thesis work provides the comprehensive aspects of the unified power quality conditioner to enhance the quality of power at the distribution level. This section presents some guidelines to extend the research work as it stands now. A brief discussion on the directions for possible future work is also outlined.

Recommendations For Thesis Work Extension

- As discussed in CHAPTER 1, a UPQC can be realized as a right shunt or left shunt. The work presented in this thesis utilizes the right shunt UPQC topology. All the developed concepts (UPQC-P, UPQC-Q, PAC, etc.) may be equally applicable to both the UPQC topologies. However, applying these concepts successfully to the left shunt UPQC system require modifications. This is mainly due to the current that flows through the series transformer (inverter). In the right hand UPQC, as the shunt inverter compensates the load current harmonics and reactive power, the current that flows through the series transformer (here source current) is assumed as sinusoidal. On the other hand, the current that flows through the series transformer, in case of the left shunt UPQC is a load current. In actual practice, as the series transformer possesses leakage impedance, the non-linear load may produce additional harmonics in the load voltage or source voltage (due to non-linear voltage drop across transformer winding). Thus, the shunt inverter in the left shunt UPQC system may need to provide the current harmonics caused by the series inverter. Additionally, a comparative evaluation, for different approaches, with the right and left shunt UPQC systems can be carried out.

- As mentioned already, the voltage sag on the distribution system is one of the most important power quality problems that UPQC needs to compensate effectively. Based on this thesis work, three different approaches, such as, active power control (CHAPTER 2), reactive power control (CHAPTER 3) and active-reactive power control using PAC concept (CHAPTER 6) can be used to tackle the voltage sag problem. A systematic

comparative study can be done on the voltage sag compensation using the three above mentioned approaches. This study can be focused on the advantages and limitations of each of the approaches. Such a kind of study could be of significant importance and can act as a comprehensive guide to select the best suitable approach based on the system requirements (rating, cost, applications, etc.).

Possible Direction For The Future Work

Solar and wind energies are emerging as alternate sources of electricity. AC to DC or DC to DC voltage source converters play an important role in these technologies to transfer the extracted renewable energy to the loads or gird. The UPQC can be combined with one or several distributed generation (DG) systems. Under such conditions, the power generated by the wind, solar or any other form of renewable energy can be fed directly to the DC bus of the UPQC. This DG power can be regulated and managed through UPQC to supply to the loads connected to the PCC in addition to the voltage and current power quality problem compensation. During normal operating condition, the UPQC–DG system can provide active power to the loads connected to the PCC and can compensate the load current harmonics, load reactive power, current unbalance, voltage harmonics, voltage sags and swell.

Additionally, a battery can be connected to the DC bus, such that the excess renewable energy can be stored and used as backup. In the event of voltage interruption, the UPQC – DG system gives additional benefit by providing the power to the load (Uninterruptible power supply). The DG power can be transferred in an interconnected mode (power to the gird and loads) or islanding mode (power to the specific loads). Now, research is slowly being directed towards this UPQC based application (Han *et al.*, 2006b). Power supplied by the UPQC-DG system under a normal working condition, low energy generation from renewable system, voltage interruption mode, etc., depends on several factors and these issues need to be addressed adequately. However, the integration of UPQC and renewable energy may play a significant role in modern distribution system to simultaneously regulate the load power demand as well as enhance the quality of power (voltage and current).

ANNEXE I

LABORATORY EXPERIMENTAL SETUP DETAILS

The prototype for active power filter system is designed, developed, and implemented in the laboratory. In this section the essential hardware prototype components are briefly discussed. Some of the important problems and limitations that arose during the experimental implementation and the steps taken to overcome those issues are also highlighted.

The major components of the prototype consist of:

i) Voltage Source Inverters: Two voltage source inverters are realized using Insulated Gate Bipolar Transistor (IGBT) switches. One of the inverters is considered as shunt APF and consists of 8-IGBT switches, while the other inverter is built using 6-IGBT switches and connected in series with the line through three single-phase transformers. Thus, the APF structure consists of 14-IGBT switches which can be configured into several different topologies, such as – (1) single-phase shunt APF system (4-IGBT), (2) single-phase series APF/ Dynamic Voltage Restorer (DVR) system (4-IGBT), (3) single-phase UPQC system (8-IGBT), (4) three-phase three-wire shunt APF system (6-IGBT), (5) three-phase four-wire shunt APF system (8-IGBT), (6) three-phase four-wire shunt APF based on 3H-bridge (12-IGBT), (7) three-phase three-wire/ four-wire series APF/ DVR (6-IGBT), (8) three-phase three-wire UPQC system (12-IGBT), and (9) three-phase four-wire UPQC system (14-IGBT). 14 gate driver circuitries are used to drive all the 14-IGBTs simultaneously. The entire hardware is arranged in such a way that in no time, the hardware configuration from one system to other, out of above mentioned 9 configurations, is possible.

ii) Sensors: To implement different algorithms and control techniques, the necessary voltages and currents are sensed. For example, to realize a single-phase shunt APF system one may need a maximum of 3 current and 2 voltage sensors, whereas, for a three-phase UPQC system the knowledge of 6 current and 6 voltage sensors is sufficient. Therefore, a total of 6-

current sensors were built using Hall-effect current sensors LEM LA-55P. The block diagram of the current sensing circuitry is shown in Figure A1.1. To sense different voltages, such as supply voltages (3-sensors), load or series injected voltages (3-sensors), and DC bus voltage (1-sensor), a total of 7 voltage sensors are used and built using analog circuitry. The block diagram of the voltage sensing circuitry is shown in Figure A1.2. All the sensed signals before sending to DSP are isolated using isolation amplifier, AD202.

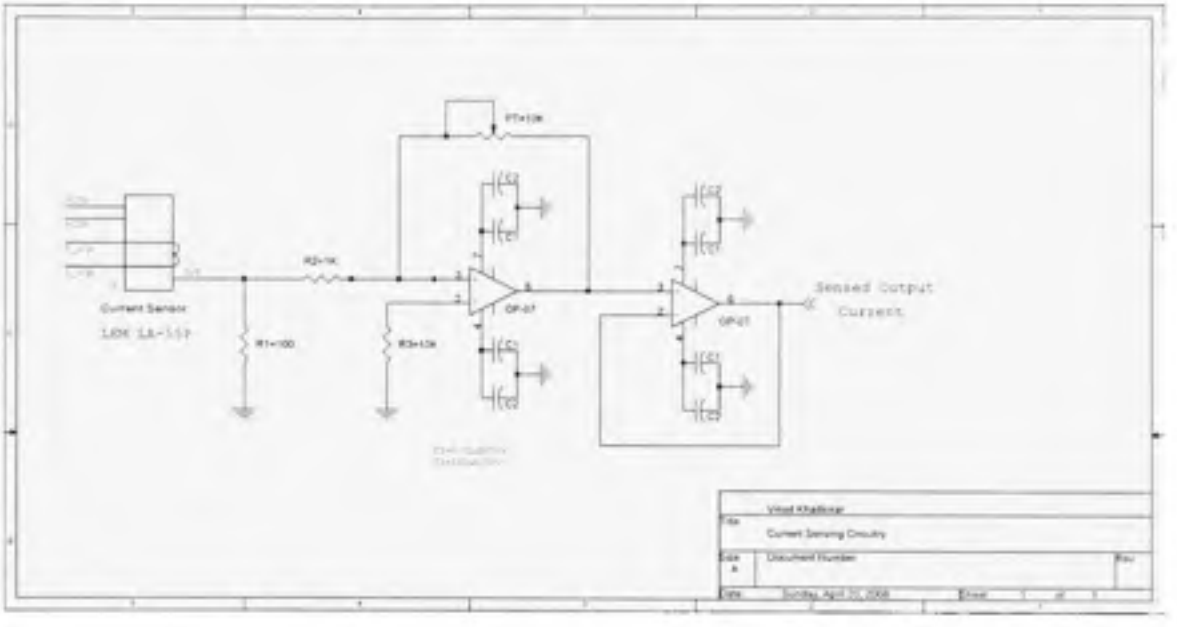


Figure A1.1 Current sensing circuit.

iii) Power Supplies: Most of the general purpose ICs require +5V (or ±5V) DC supply for their operation, whereas, most of the special purpose ICs require ± 12V DC or ±15V DC supply voltages. Thus, the developed prototype requires +5V DC, ±12VDC, and ±15VDC supplies. Some of the power supplies are built in the laboratory, and some readily available DC power sources are used.

iv) dSPACE: For real-time control of both the inverters a digital signal processor (DSP) is used. A rapid prototyping controller board from dSPACE – DS1104 is utilized for hardware implementation. The DS1104 is selected mainly because the simulation studies are carried

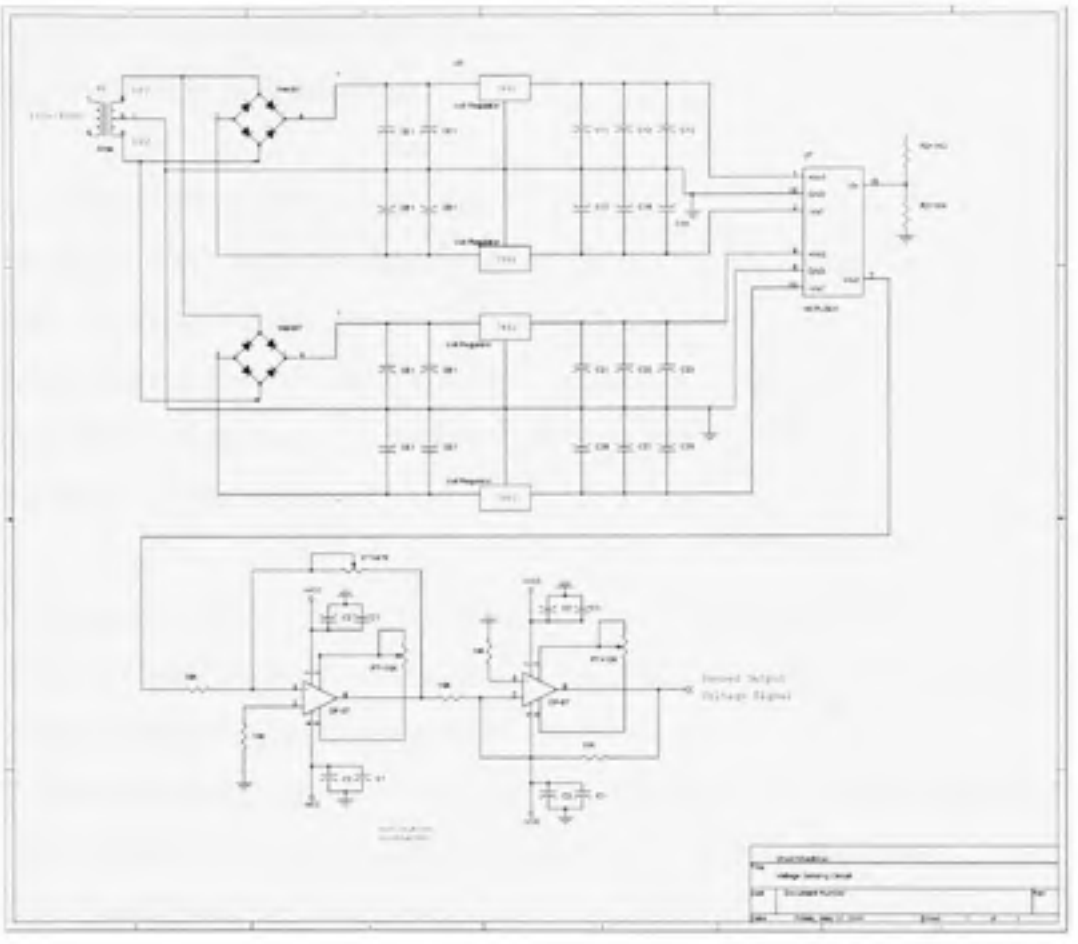


Figure A1.2 Voltage sensing circuit.

out using MATLAB/ Simulink, particularly using SIMPOWERSYSTEM block sets. Since the MATLAB/ Simulink supports the dSPACE it is easy to implement the developed control algorithms in real-time. The other option is the use of a core DSP process such as TMS320F2812 DSP from Texas Instruments. The TMS320F2812 requires coding the algorithm using *C* or *C+* language, which is a time consuming task. The changes, if any, need to be carried out in the control algorithm, during later stages of controller development, which a time consuming and tedious task. On the other hand, with MATLAB/ Simulink and dSPACE combination, the changes or even an entirely new control algorithm does not take much time to implement in real-time. Moreover, it is also possible to generate C-codes for developed MATLAB/ Simulink Model and then can be used in a core DSP. However, the

code generated in such a manner is not easy to understand and requires optimization for a better utilization of the DSP processor.

The DS1104 dSPACE board is built with – 1) a *master* microcontroller unit which has a *Motorola Power PPC 603e* processor (64 Bit Floating Point Processor with CPU Clock Frequency – 250 MHz), and 2) a slave DSP from Texas Instruments – TMS320F240 (16 Bit Fixed Point Processor). The DS1104 board consists of 8 channels for analog to digital conversion (ADC), 8 channels for digital to analog conversion (DAC), timers, interrupters, and 20 bit input – output (I/O) ports.

The actual integration between hardware and software is highlighted here :

- The *MATLAB/ Simulink* is first used as an offline simulation tool for the modeling, analysis, and design of the controller.
- The *Real-Time Interface* enhances the Simulink block library with additional blocks, which provide the link between Simulink and the real-time hardware.
- The Simulink model is transferred into real-time code using *real-time workspace* (RTW) which then generates automatic *C-codes* for developed Simulink model.
- The generated *C*-codes are then automatically loaded in then dSPACE master or slave unit, and are ready to use to achieve the desired tasks.

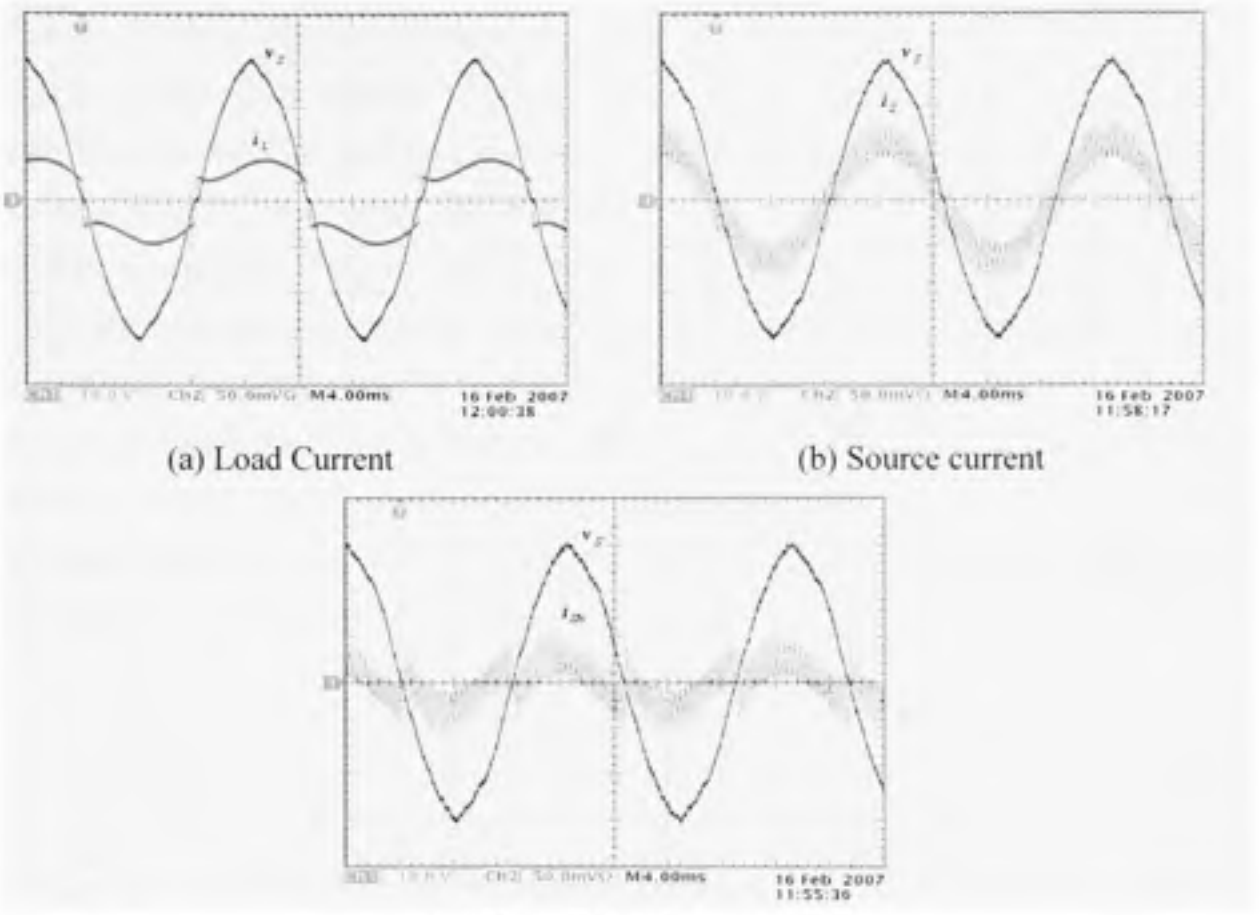
v) Analog PWM and Hysteresis Controller: The major limitations of dSPACE based hardware system while performing the experimental studies is discussed below:

- To realize a three-phase UPQC controller in real-time, a total of 13 signals (3 actual load currents, 3 source voltages and a DC bus voltage for controller development, and 3 actual source or 3 actual shunt filter currents and 3 load or series filter voltages to perform PWM operation) need to be sent to the dSPACE unit through ADC channels. The DS1104 has only 8 ADC channels for A/D Conversion and thus, the obvious question was how to implement the UPQC controller in real-time with insufficient ADC channels.

- The other important observation we made is that the dSPACE based hardware system performance is solely governed by its sampling time. It is very difficult to run the unit at the smaller sampling time, for example, sampling time of 10 *μsec*.

The sampling time in dSPACE based hardware system is determined by the MATLAB/ Simulink *real-time built procedure* depending on the complexity of the developed controller. More complex the system or higher the mathematical computations involved, longer will be the sampling time. Thus, there is always a certain minimum sampling time below which MATLAB/ Simulink build procedure gives an error – *"[#4] ds1104 – RTI: Task Overrun: Program cannot be executed in real-tim (12)"*. The user always needs to find the minimum sample time for a particular controller using standard the *"trial and error"* procedure.

The experimental results for one of the earlier studies are shown in Figure A1.3. In this experimental study, the controller for a single-phase shunt APF system was developed (the most simple out of 9 configurations). The controller to generate the reference signal and the Hysteresis current controller were developed inside the MATLAB/ Simulink. The necessary switching pulses for IGBT gate drivers were sent using I/O ports (through proper isolation i.e. through opto-couplers). The algorithm required 40 *μsec* as sampling time to execute the generated *C*-codes in real-time. It was found that due to the sampling time of 40 *μsec* the dSPACE system was just able to generate a maximum switching frequency of 2 kHz. For active power filtering, 2 kHz is not a sufficient switching frequency to achieve a better performance from the system. This fact can be noticed from Figure A1.3 (b), when APF system is in operation the low frequency switching ripples (noise) can be noticed on compensated source current profile. The source current THD under this condition was reduced from 28% to 10% .



(a) Load Current

(b) Source current

(c) Shunt injected current

Figure A1.3 Experimental results: performance of shunt APF at lower switching frequency.

At this point the concerns were: *how to overcome the problem with limited ADC channels to implement UPQC controller in real-time, and how to increase the switching frequency for better performance?"* The options we had at that time were – (*i*) to use the I/O port to send the remaining 5 signals (out of 13) to the host PC, but the problem of sampling time was still around. So, the next option was – (*ii*) to use a core DSP and write *C*-codes for the developed algorithm. The second option was a better choice and the chances to achieve a better performance were high. However, to the modification of the entire dSPACE system and writing C-codes was a time consuming task.

To improve the performance of the hardware system we decided to use the *dSPACE to generate the reference signals for both the inverters.* The MATLAB/ Simulink is then just

used to develop the controller in real-time and the reference signals are then taken out from dSPACE through DAC channel. These signals are then compared with the actual sense signals to perform PWM operation. An analog PWM and Hysteresis controller is built out side the dSPACE. The printed circuit boards (PCBs) for analog PWM and Hysteresis controller are designed using the Orcad Layout. It is interesting to note that both the PWM and Hysteresis controllers are built on a single board and a toggle switch is used to change from PWM to Hysteresis mode or vice-versa mode of operation, instantaneously. Care was also taken to realize the PWM or Hysteresis mode of operation for single-phase, three-phase three-wire, or three-phase four-wire system configuration with ease. The block diagram for PWM and Hysteresis controllers is shown in Figure A1.4, and the isolation provided using opto-coupler IC6N137 is shown in Figure A1.5.

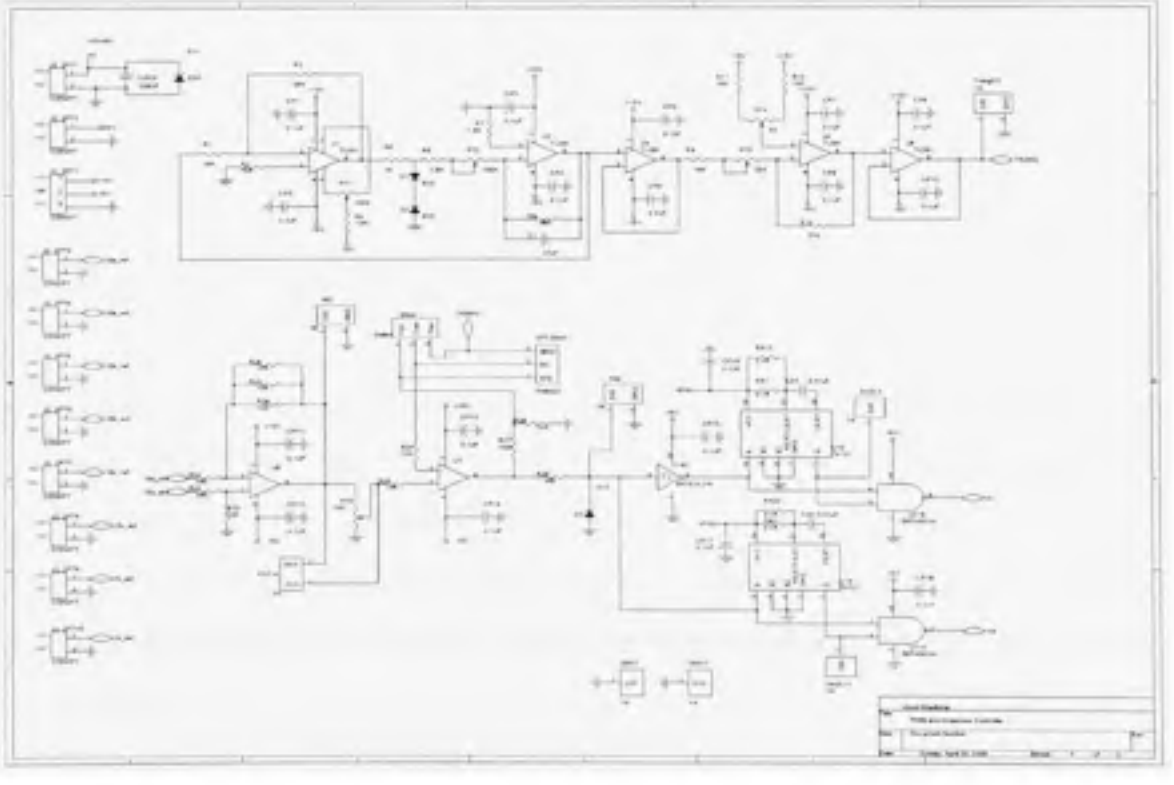


Figure A1.4 Analog PWM & Hysteresis Controller Circuitry

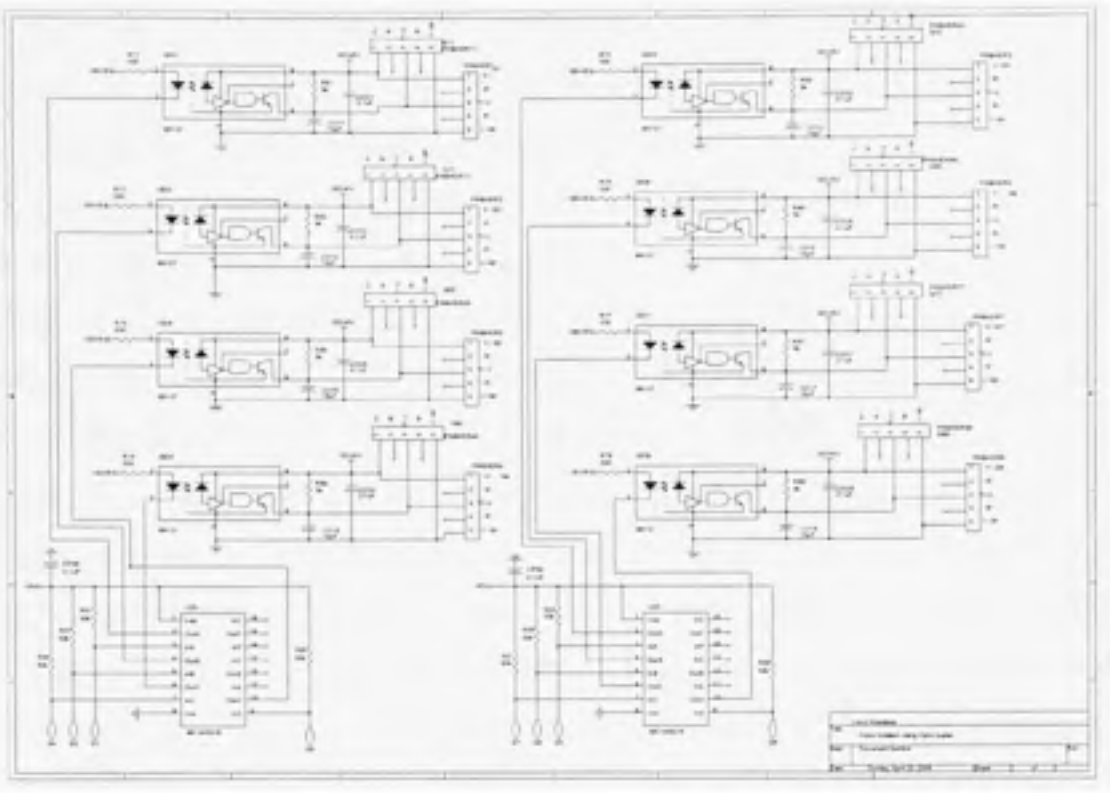
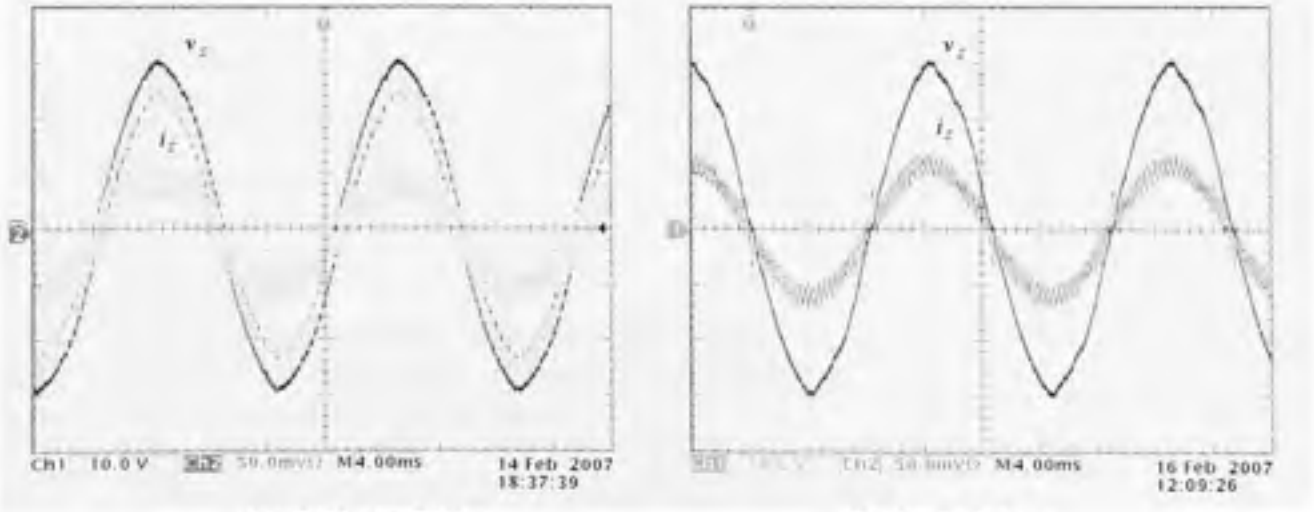


Figure A1.5 Gate pulse isolation circuitry.

The advantages offered by constructing an analog PWM / Hysteresis board are:

- Reduction in the number of signals needed to send to dSPACE through ADC channel from 13 to 7. thus the controller can now be implemented easily, i.e. the limitation imposed by 8 ADC channels is overcome.
- Since the PWM or Hysteresis controller for inverter switching is not carried out inside the MATLAB/ Simulink model, the sampling time for a particular controller is reduced.
- The system is works independent of sampling time. It is observed that for same control algorithm, a sampling time from 30 μsec to 120 μsec (with step of 10 μsec), does not show anyeffect on the performance of the APF system.
- It is now possible to switch the inverters up to 20 kHz without any problems.

vi) Autotransformer – It is essential to mention here that in the laboratory a three-phase autotransformer is used to carry out all the experiments. The autotransformer has high winding impedance which is inductive in nature. When the shunt inverter is turned ON, its high frequency operation causes a highly switching frequency voltage drop across the internal inductance of autotransformer, thus results in distorted voltage. The experimental result under such a condition is shown in Figure A1.6 (a). It is obvious from the figure that the internal inductance of the autotransformer causes the problem. To eliminate the effect of the autotransformer impedance, three AC capacitors are connected in delta with the three phase lines. The improved voltage profile, when APF is ON, is shown in Figure A1.6 (b). The voltage after the capacitor banks are then considered as the input voltages for the APF system. For simplicity, in this work, these voltages are mentioned as supply voltages or source voltages. The autotransformer winding inductive impedance together with the capacitor impedance forms a low pass filter and results in slightly distorted voltages. The used autotransformer output voltages are also slightly unbalanced. The pictorial view of the laboratory experimental setup is shown in Figure A1.7 to Figure A1.10.



(a) Without Filter (b) With Filter

Figure A1.6 Analog PWM & Hysteresis controller circuitry.

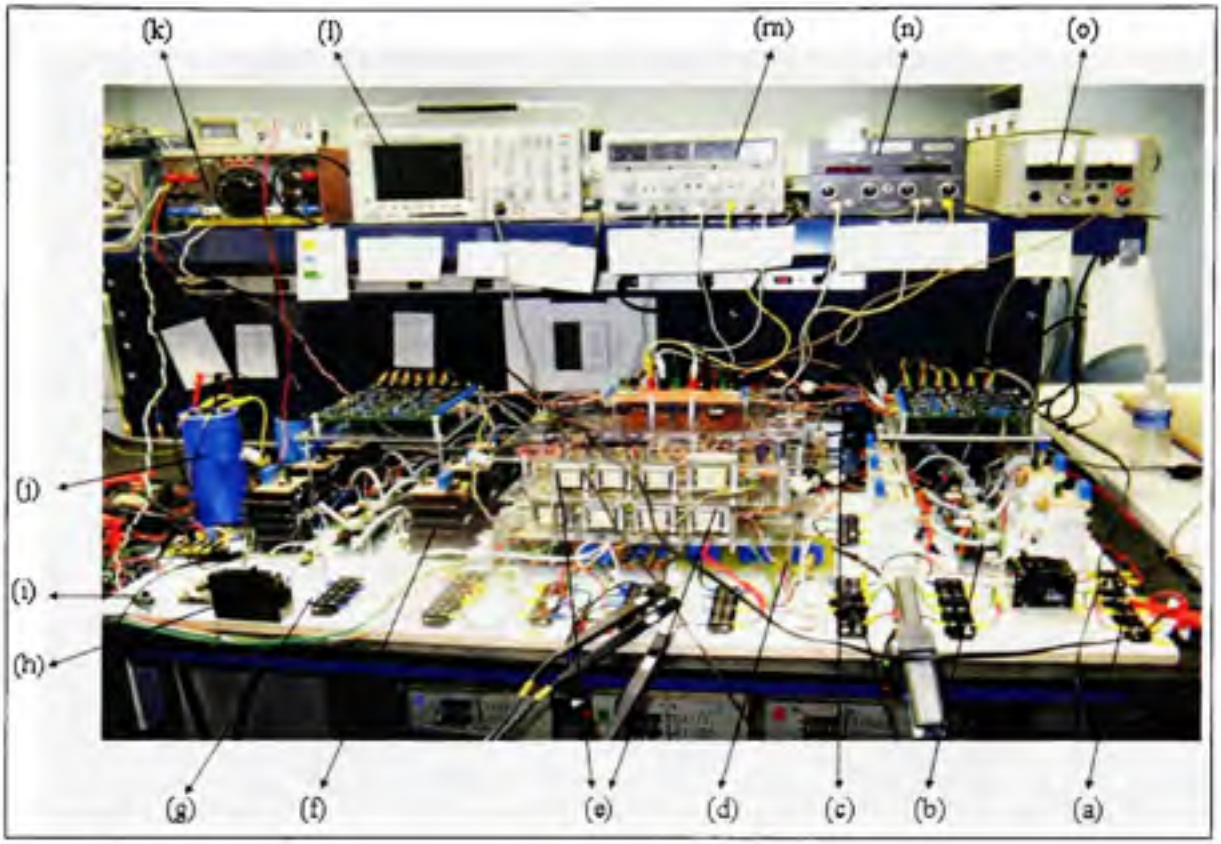


Figure A1.7 Experimental setup pictorial view: Overall UPQC system configuration

(a) Source side
(b) Series inverter
(c) DS1104 dSPACE
(d) Current sensors
(e) Voltage sensors
(f) Shunt inverter
(g) Load side
(h) Manual switch to create single-phasing condition
(i) Switch to control magnetic actuator for load changing
(j) Self supporting DC bus capacitor
(k) Single phase 110V/60 Hz supply used for different interfacing circuits
(l) Oscilloscope to record experimental results (TDS3032B)
(m) ± 12V DC supply used for analog PWM board
(n) ± 10V DC supply used for dSPACE protection circuit
(o) +5V DC supply used for shunt and series inverter driver circuits

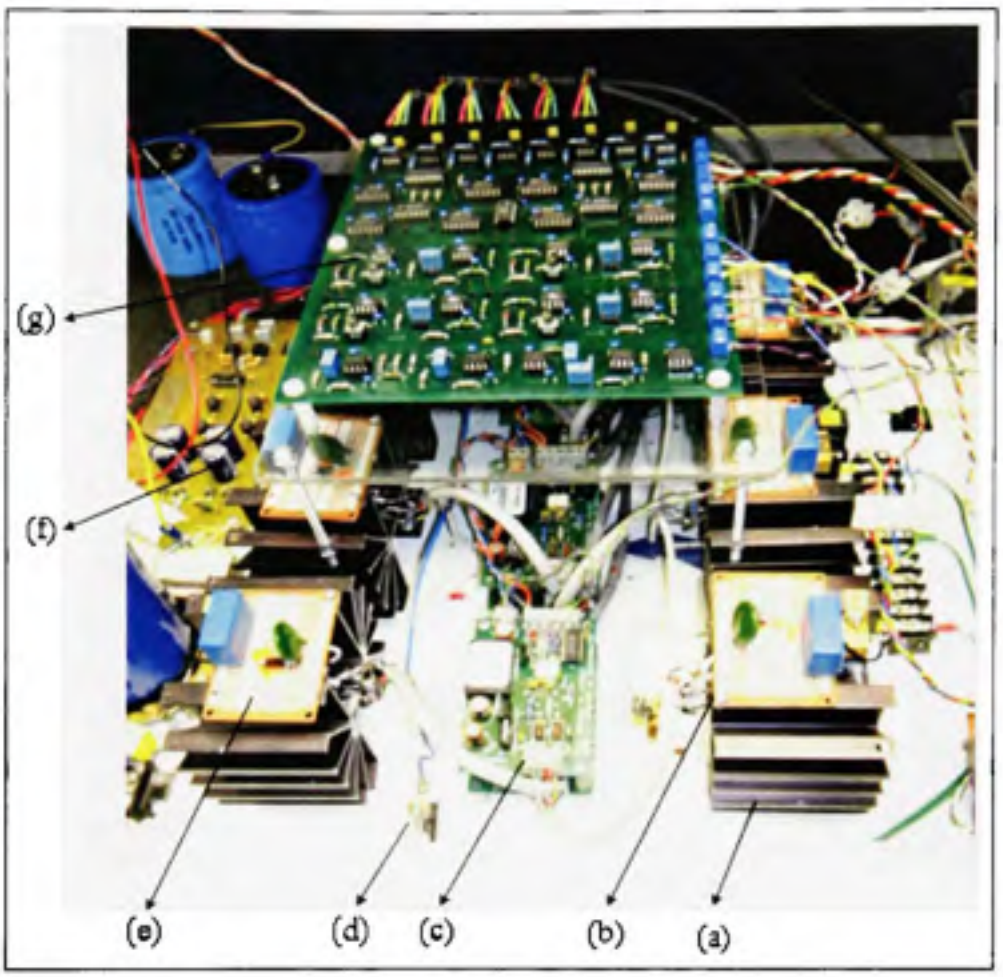


Figure A1.8 Experimental setup pictorial view: Shunt inverter with external PWM circuitry

(a) Heat sink
(b) IGBT (IXGH24N60CD1)
(c) IGBT gate driver
(d) Protection fuse
(e) Snubber circuit
(f) DC link voltage sensor
(g) Analog PWM/ Hysteresis Controller

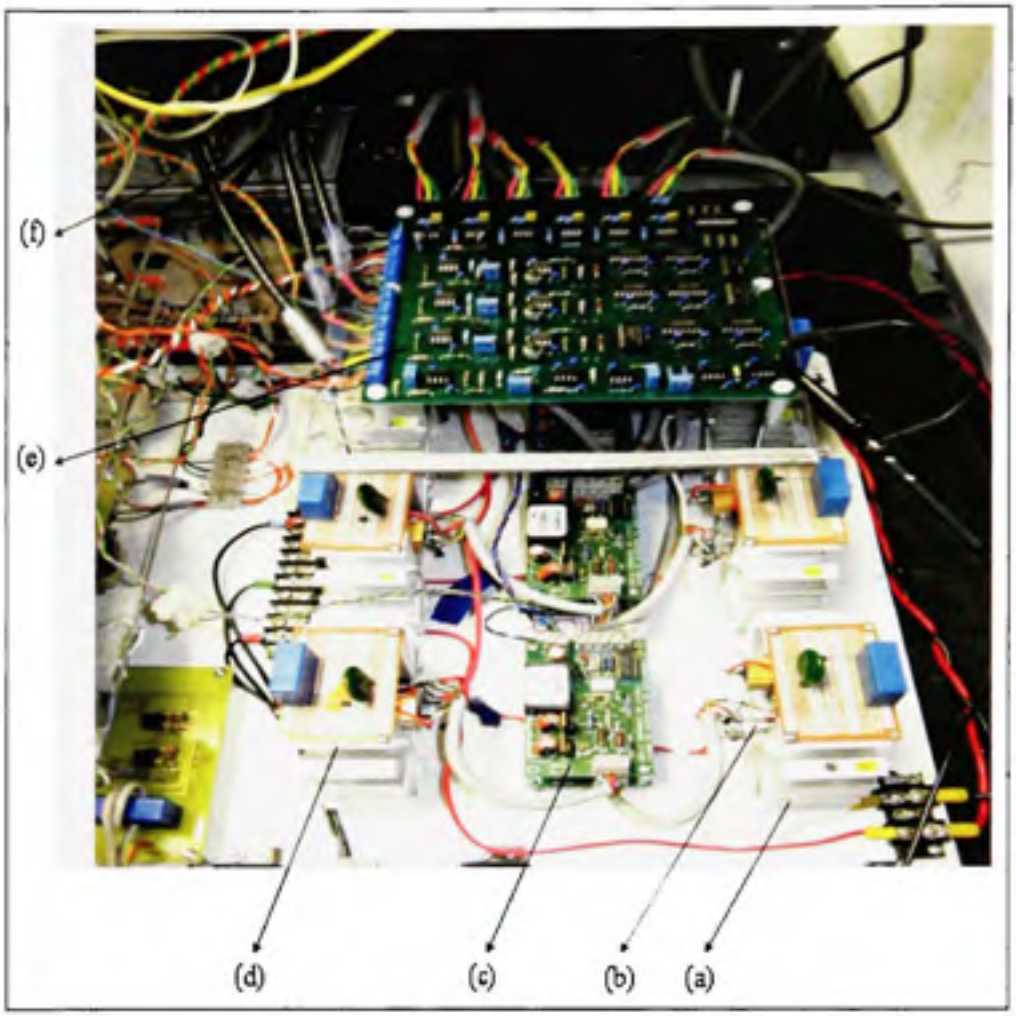


Figure A1.9 Experimental setup pictorial view: Series inverter with external PWM circuitry

(a) Heat sink
(b) IGBT (IXGH24N60CD1)
(c) IGBT gate driver
(d) Snubber circuit
(e) Analog PWM/ Hysteresis Controller
(f) DS1104 dSPACE

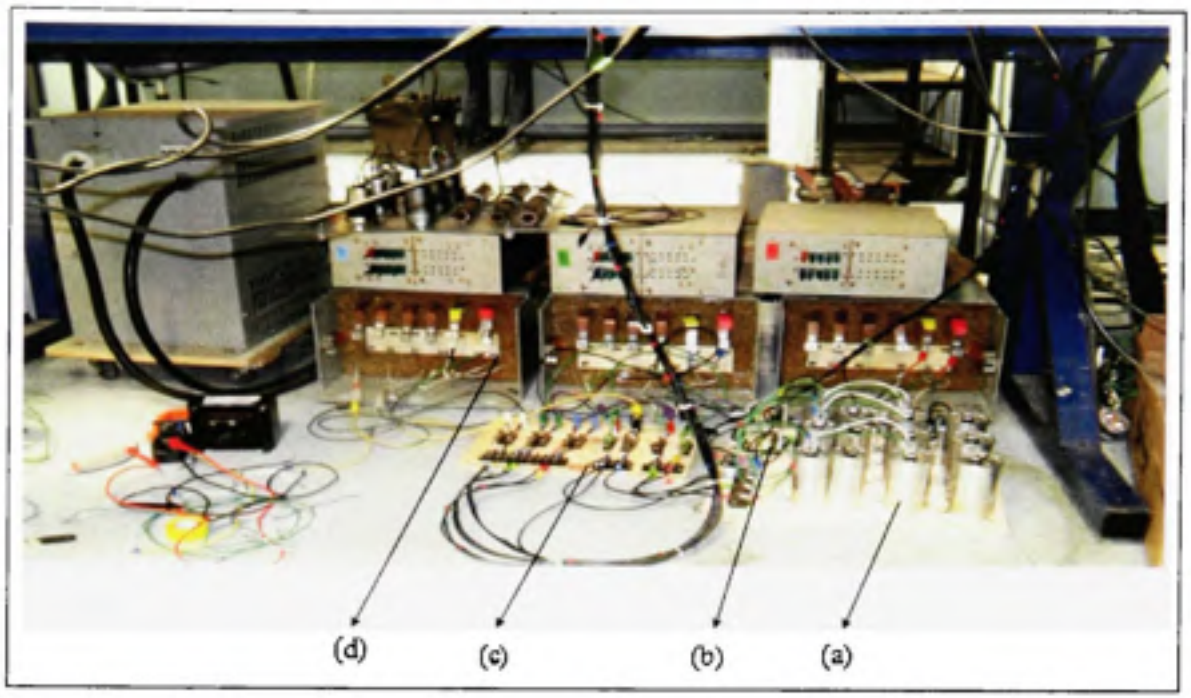


Figure A1.10 Experimental setup pictorial view: Series injection transformers

(a) Ripple filter capacitor
(b) Ripple filter inductor
(c) Protection fueses
(d) Series transformer

ANNEXE II

PRINCIPAL EXPERIMENTAL PARAMETERS

The principal experimental parameters are listed below:

CHAPTER 2

- AC supply voltage

  60V (*rms*) single-phase, f=60 Hz
- Load

  i) RL Load: R = 13.23 Ω + L = 50 *m*H

  ii) Non-Linear: DBR followed by R = 13.23 Ω + L = 50 *m*H

  iii) Dynamic: Load changed from DBR followed by R = 20 Ω + L = 50 *m*H to (R = 20 Ω + L = 50 *m*H) in parallel with R= 40 Ω
- Shunt Inverter

  Switching frequency (f_{Sh}) = 5-7 kHz (Hysteresis controller), L_{Sh} = 5 *m*H
- Series Inverter

  Switching frequency (f_{Sr}) = 5 kHz (Triangular carrier based PWM controller),

  L_{Sr} = 2 *m*H, C_f = 40 μF
- Transformer turn ratio = 1:2
- Reference DC link voltage = 115V
- dSPACE sampling time = 50 μsec

CHAPTER 3

Single-phase System

- AC supply voltage

  Source voltage (single-phase) = 30V (*rms*), Rated load voltage = 35V (*rms*), f=60 Hz

- UPQC

  f_{Sh} = 5-7 kHz, L_{Sh} = 5 *m*H, f_{Sr} = 5 kHz, L_{Sr} = 2 *m*H, C_f = 40 µF,

  Reference DC link Voltage = 70V
- Transformer turn ratio = 1:3
- dSPACE sampling time = 45 µsec

Three-phase System

- AC supply voltage

  Source voltage (three-phase) = 19V (*rms*), Rated load voltage = 25V (*rms*), f=60 Hz
- Load

  Non-linear load: DBR followed by R = 26.67 Ω + L = 10 *m*H
- UPQC

  f_{Sh} = 5-7 kHz, L_{Sh} = 5 *m*H, f_{Sr} = 5 kHz, L_{Sr} = 1 *m*H, C_f = 50 µF,

  Reference DC link Voltage = 100V
- Transformer turn ratio = 1:3
- dSPACE sampling time = 75 µsec

CHAPTER 4

- AC supply voltage

  Source voltage (three-phase) = 35V (*rms*), f=60 Hz
- UPQC

  f_{Sh} = 5-7 kHz, L_{Sh} = 5 *m*H, f_{Sr} = 5 kHz, L_{Sr} = 2 *m*H, C_f = 50 µF,

  Reference DC link Voltage = 120V
- Transformer turn ratio = 1:3
- dSPACE sampling time = 65 µsec

CHAPTER 5 and CHAPTER 6

- AC supply voltage

  Source voltage (single-phase) = 35V (*rms*), f=60 Hz
- Load

  Highly inductive load: R = 40 Ω in parallel with L = 50 *m*H
- UPQC

  f_{Sh} = 5-7 kHz, L_{Sh} = 5 *m*H, f_{Sr} = 5 kHz, L_{Sr} = 2 *m*H, C_f = 40 μF,

  Reference DC link Voltage = 70V
- Transformer turn ratio = 1:3
- dSPACE sampling time = 50 μsec

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