Development, Modulation, and Voltage Balancing of Multi-Level Converters and Modular multilevel Converters (MMCs)

by

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Développement, modulation et équilibrage de la tension des convertisseurs multiniveaux et des convertisseurs modulaires multiniveaux (CMM)

Saeed ARAZM

RÉSUMÉ

Les topologies de convertisseurs multiniveaux (CMN) permettant de réduire le nombre de composants tout en améliorant la qualité de puissance restent une préoccupation majeure pour les applications industrielles. Bien qu'au cours des dernières années, de nombreux CMN aient été proposés dans le domaine de la recherche pour augmenter les niveaux de tension, les sources de courant continu (CC) isolées et le nombre de dispositifs de commutation sont les facteurs limitatifs de leurs applications dans les industries. Les sources de CC isolées augmentent non seulement le poids, le volume et le coût des onduleurs en raison du transformateur déphaseur, mais aussi les pertes de puissance en raison des redresseurs. Les convertisseurs multiniveaux modulaires (CMM) sont la solution pour remplacer la source CC isolée par une seule source CC; cependant, des multitudes de dispositifs à semi-conducteurs doivent être utilisés dans les demi-pont convertisseurs multiniveaux modulaires (DM-CMM) classiques et populaires pour générer un niveau de tension donné. La gestion du courant de défaut CC, l'équilibrage de la tension dans les condensateurs volants et les courants de circulation sont des questions controversées pour les applications des CMM. Dans la première partie de cette thèse, une topologie à nombre réduit de composants du convertisseur multiniveau est proposée avec une seule source de CC pour les systèmes monophasés et triphasés. Cette topologie unipolaire appelée Z-Packed U-Cell (ZPUC) est utilisée comme sous-module de CMM (ZPUC-CMM) pour augmenter les niveaux de tension par rapport à ses homologues. L'équilibrage de tension intégré à la modulation de largeur d'impulsion de déphasage (MLI-DP) est mis en œuvre sur ce convertisseur pour réguler les tensions des condensateurs. La génération de niveaux de tension plus élevés avec une distorsion harmonique totale (DHT) plus faible fait de ce convertisseur une alternative appropriée pour les applications de haute et moyenne tension telles que les entraînements de moteur. Dans la deuxième partie de cette thèse, un équilibrage de tension basé sur l'apprentissage profond et intégré à la modulation par largeur d'impulsion à décalage de niveau (MLI-DN) et à la MLI-DP hybrides avec une tension de référence unique est mis en œuvre sur le ZPUC-CMM pour augmenter les niveaux de tension. Les résultats de simulation en état d'équilibre sont utilisés pour former l'équilibreur de tension d'apprentissage profond et il est mis en œuvre sur ZPUC-CMM dans le laboratoire sur les états stables et transitoires. Dans la dernière partie de cette thèse, la topologie PUC est développée comme un convertisseur Y-PUC triphasé à source unique en CC. Le convertisseur PUC nécessite trois sources CC isolées pour un système triphasé, ce qui limite son application. La topologie Y-PUC qui est un convertisseur modulaire multiniveau (PUC-CMM) avec sous-module PUC est proposé pour résoudre ce problème. Le Y-PUC modulaire peut être utilisé dans l'application HVDC en raison du fait que PUC est un convertisseur bipolaire, et il est capable de bloquer le courant de défaut CC. L'équilibrage de tension intégré avec la technique de modulation est mis en œuvre dans Y-PUC pour illustrer les performances du convertisseur proposé dans des états stables et transitoires.

Mots-clés: équilibrage de tension, convertisseur multiniveau, convertisseur multiniveau modulaire, ZPUC-CMM, Y-PUC, modulation, apprentissage profond, MLI-DP, MLI-DN

Development, modulation, and voltage balancing of multilevel converters and modular multilevel converters (MMC)

Saeed ARAZM

ABSTRACT

Multilevel converter (MLC) topologies with lower components counts along with higher power quality are still a major concern for industrial applications. Although in recent years, many MLCs have been proposed in the research area to increase the voltage levels, isolated DC sources and number of switching devices are the limiting factors for their applications in industries. Isolated DC sources not only, increase the weight, volume, and cost of the inverters due to the phase-shift transformer, but also, increase the power losses because of the rectifiers. Modular multilevel converters (MMCs) are the solution to replace the isolated DC source with a single DC source; however, multitudes of semiconductor devices must be utilized in the conventional and popular HB-MMCs to generate a given voltage level. DC fault current handling, voltage balancing in flying capacitors, and circulating currents are controversial issues for MMCs applications. In the first part of this thesis, a single DC source reduced components counts topology of the multilevel converter is proposed for single-phase and three-phase systems. This unipolar topology called Z-Packed U-Cell (ZPUC) is used as a submodule of MMC (ZPUC-MMC) to increase the voltage levels over its counterparts. Voltage balancing integrated with phase-shift pulse width modulation (PS-PWM) is implemented on this converter to regulate the voltages of the capacitors. Higher voltage levels waveform generation with a lower total harmonic distortion (THD) makes this converter an appropriate alternative for high power and medium voltage applications such as motor drives. In the second part of this thesis, a deep-learning-based voltage balancing integrated with hybrid level-shift pulse width modulation (LS-PWM) and PS-PWM with a single reference voltage is implemented on ZPUC-MMC to increase the voltage levels. Simulation results in steady states are employed to train the deep-learning voltage balancer and it is implemented on ZPUC-MMC in the lab on both steady and transient states. In the final part of this thesis, PUC topology is developed as a single DC source three-phase Y-PUC converter. PUC converter requires three isolated DC sources for a three-phase system which limits its application. Y-PUC topology that is a modular multilevel converter (PUC-MMC) with PUC submodule is proposed to address this problem. Modular Y-PUC can be used in HVDC applications due that PUC is a bipolar converter, and it is capable to block DC fault current. Voltage balancing integrated with modulation technique is implemented in Y-PUC to illustrates the performance of the proposed converter in steady and transient states.

Keywords: voltage balancing, multilevel converter, modular multilevel converter, ZPUC-MMC, Y-PUC, modulation, deep-learning, PS-PWM, LS-PWM

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LIST OF ABBREVIATION

TWh	Tera watt-hour
GDP	Gross Domestic Product
GW	Giga watt
AC	Alternative Current
DC	Direct Current
PCC	Point of Common Coupling
MOSFET	Metal–Oxide–Semiconductor Field-Effect Transistor
IGBT	Insulated-Gate Bipolar Transistor
IGCT	Integrated Gate Controlled Thyristor
GaN	Gallium Nitride
HV	High Voltage
MV	medium Voltage
THD	Total Harmonic Distortion
MLC	Multilevel Converter
MMC	Modular Multilevel Converter
CHB	Cascaded H-Bridge
NPC	Neutral Point Clamped
FC	Flying Capacitor
PUC5	5 Level Packed U-cell
ZPUC	Z-Packed U-cell
ZPUC5	5 Level Z-Packed U-cell
ZPUC-MMC	Z-Packed U-cell- Modular Multilevel Converter

Y-PUC	Double Star Packed U-Cell
PS-PWM	Phase Shift Pulse Width Modulation
LS-PWM	Level Shift Pulse Width Modulation
SVM	Space vector Modulation
HVDC	High Voltage Direct Current
STATCOM	Static VAR Compensator
AI	Artificial Intelligence
NN	Neural Network

INTRODUCTION

Nowadays, by augmenting the number of renewable energy sources, utilizing the power electronic converters is considerably increasing (Carrasco et al., 2006). Based on British Petroleum's statistical review of world energy 2021, the COVID-19 pandemic causes reduce energy consumption at the fastest rate since 1945. Nevertheless, renewable energy sources, especially solar power plants and wind farms, are growing faster than ever. In fact, the power demands declined to 4.4%, 405 TWh in 2020, while the renewable energy generation demonstrate its largest-ever including 173 TWh for wind and 148 TWh for solar energy. This augmentation in renewable energy is the largest ever which has been recorded (British-Petroleum, 2021).

Figure 0.1 demonstrates the share of coal and renewable in global power generation from 2010 to 2020. To illustrate, increased rate of wind and solar energy are depicted separately in figures 0.2 and 0.3.

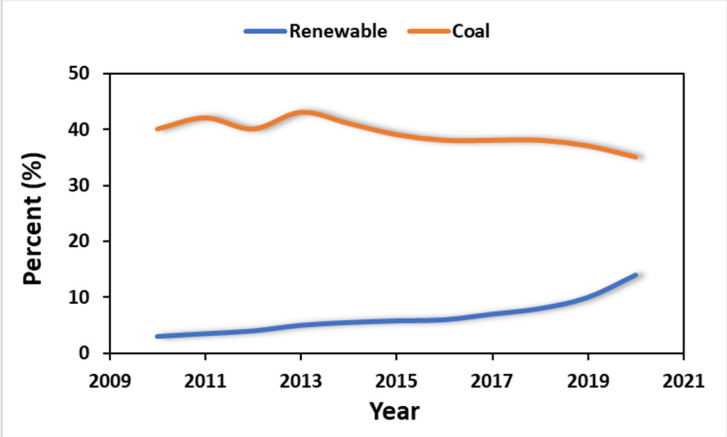

Figure 0.1 Share of renewables and coal in global power generation
Adapted from British-Petroleum (2021, p. 5)

Augmentation of renewable energy generation was 238 GW in 2020 despite the collapse in GDP due to the pandemic that is 50% more than ever before. Between 2015 to 2020, the

capacity of solar and wind have doubled, and the increased capacity was around 800 GW. Thus, through such growth on the renewable energy and distributed generations, providing the

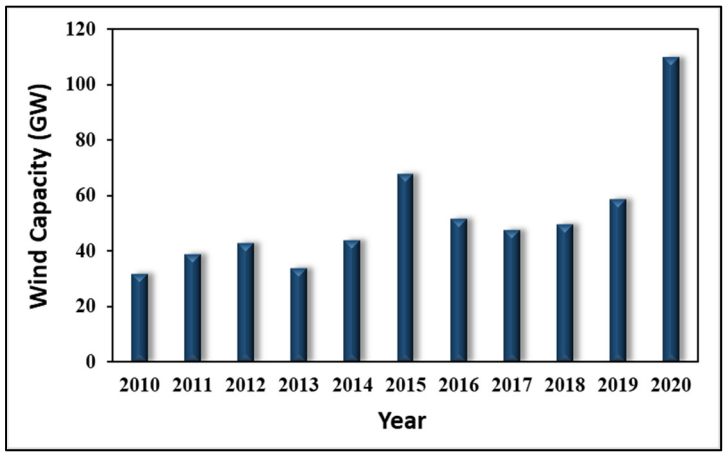

Figure 0.2 Annual change of wind capacity
Adapted from British-Petroleum (2021, p. 5)

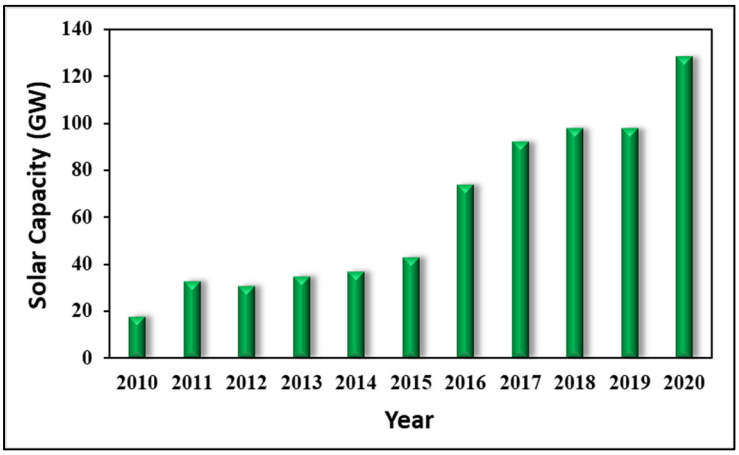

Figure 0.3 Annual change of solar capacity
Adapted from British-Petroleum (2021, p. 5)

suitable technology to integrate them into the electrical grid is inevitable. Power electronic converters are the interface apparatus toward green energy and the world without carbon emission. In past years, switching devices have developed at the fastest rate by progressing in the semiconductor industries. The application of nanotechnology in this industry leads to

produce the new generation of switches in which the frequency, voltage rating and power rating have considerably augmented. Consequently, one of the biggest obstacles to apply the power electronic on high voltage and power was removed. Moreover, emerging of the robust digital controller paved the way of power electronic converters applications to integrate renewable sources into the grid.

In solar plants, two types of converters are utilized including chopper (DC/DC) and inverter (DC/AC) to connect to the principal electrical grid. In wind power plants rectifier (AC/DC) and inverter (DC/AC) are used to regulate the frequency, phase, and voltage amplitude for grid connection at the point of common coupling (PCC). Furthermore, in the high voltage transmission system, power electronic converters are responsible to exchange the frequency between two systems with different power frequencies, or transferring the DC voltage instead of AC to reduce the power losses. High power application of power converters is to drive the motors of compressors, pumps, fans, grinding and rolling mills, conveyors, crushers, and so forth (Kouro et al., 2010).

Today, the new generation of semiconductor switches that are almost used to construct the power electronic converters are insulated-gate bipolar transistor (IGBT), metal–oxide–semiconductor field-effect transistor (MOSFET), and Gallium Nitride (GaN). The main drawbacks of thyristor and gate turn-off thyristor (GTO) are the lower switching frequency and efficiency which limits their application on high power applications (K. J. Chen et al., 2017). In contrast, GaNs are the newest switches with the highest proficiency and switching frequency rather than their counterparts. Figure 0.4 illustrates the diagram of voltage in terms of frequency for three types of switches. For high switching frequency, the MOSFETs are not suitable due to their lower efficiency. In other words, when the frequency is increased the rise and fall time of the switches play the roles which are lower in GaN compared to MOSFET and IGBT. On the other hand, voltage blocking in the GaNs is lower than IGBT and MOSFET (Lidow & Reusch, 2015). Thus, appropriate selection of the switches and proper designing of the power converters are the vital process that must be considered.

Figure 0.5 shows the two-level power converter in which the total voltage of the system must be tolerated by each switch (Fang Zheng, Jih-Sheng, McKeever, & VanCoevering, 1996; Flourentzou, Agelidis, & Demetriades, 2009). However, as mentioned above, there are some limitations to choose suitable switching devices. To illustrate, figure 0.4 shows that the maximum voltage blocking for accessible IGBT in the market is around 1200V. Series switches, among which the total voltage could be divided, can be a solution to address this problem; however, the higher dv/dt and THD in the waveform is still trouble that causes to enlarge the printed circuit board (PCB) due to large size of the filters.

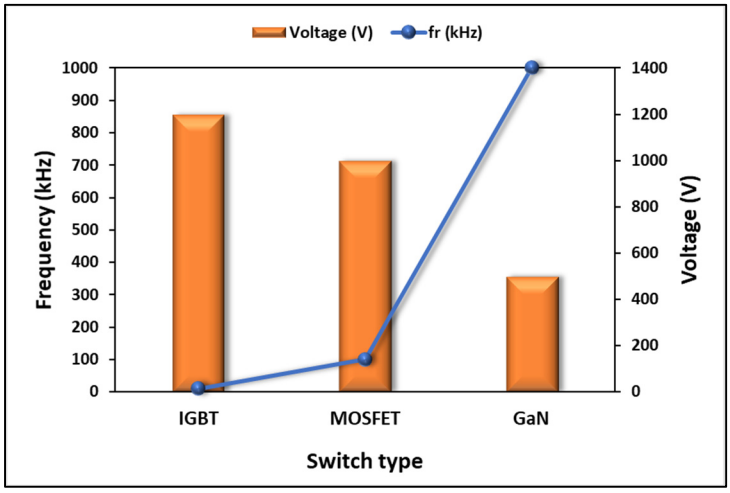

Figure 0.4 Semiconductor technologies in terms of frequency and voltage blocking

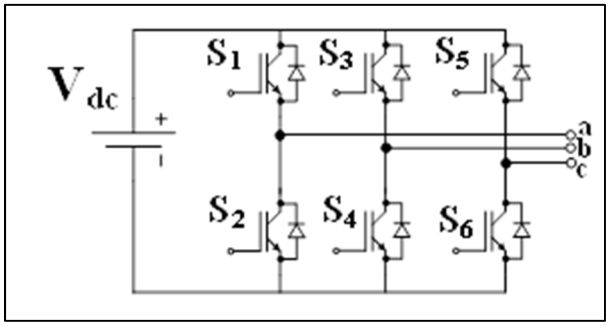

Figure 0.5 Two-Level Conventional converter

Description of the problem

Application of power converters in medium voltage and high voltage is challenging due to the maximum allowable rating power and blocking voltage of the switching devices. Multilevel converters are the best solution to address this complication. This concept not only divides the voltage among several switches, but also reduces the THD and dV/dt that is not addressed on series switches in conventional two-level converters (Jose Rodriguez, Lai, & Peng, 2002).

The main drawbacks of Multilevel converters (MLCs) are the higher number of DC sources, switches, flying capacitors (FCs) and complications in modulation and control systems compared to the conventional ones. DC sources can be replaced by the FCs in some types of MLCs in which capacitors must be balanced properly with a minimum ripple. Due to that, the FCs occupy a large portion of the PCBs compared to the semiconductor parts, obtaining the lower size of FCs through appropriate and simple voltage balancing methods to achieve the minimum ripple is one of the controversial issues on MLCs.

A large number of isolated DC sources problem on MLCs was resolved by introducing the modular multilevel converters (MMC) which was invented firstly by Prof. R. Marquardt (Lesnicar & Marquardt, 2003). It includes submodules that can be conventional two-level converters (HB-MMC) or Multilevel converters such as 3-L flying capacitors (FC-MMC). HB-MMCs are the most common type of MMCs which require N cells per arm to generate N+1 voltage levels at the output. Besides, to achieve the higher quality of output waveform, the number of submodules in standard type must be increased that causes a higher power loss, lower reliability, higher complexity in voltage balancing, and higher number of components. To devise an optimized topology of MMCs, their application, as well as the standard requirements, must be considered to trade-off between the complexity and power losses (Debnath, Qin, Bahrani, Saeedifard, & Barbosa, 2015).

It should be noted that the unipolar topologies on MMCs cannot disconnect the DC short circuit fault current through the switches and they require the external DC circuit breaker (Callavik, Blomberg, Häfner, & Jacobson, 2012).

On the other hand, modulation strategy on MLCs is another challenging issue due to a large number of switches and different types of switching patterns and redundancy. Phase shift pulse width modulation (PS-PWM), level shift pulse width modulation (LS-PWM), and space vector modulation (SVM) are three well-known modulation strategies that are often used to generate the signals for switching of semiconductors (Saeed Arazm, Hani Vahedi, & Kamal Al-Haddad, 2018). The main advantage of PS-PWM in comparison with LS-PWM and SVM is shifting the harmonic contents to farther than the fundamental frequency. Accordingly, the size and cost of output filters could be reduced while the power quality is improved. PS-PWM is also interesting to apply on MMCs for improving the voltage balancing due to their high switching frequency with the same carrier frequency compared to LS-PWM and SVM (Y. Li, Wang, & Li, 2015). However, the normal type of PS-PWM through the logic gate can not be applied to all types of MLCs. (Bin Wu & Narimani, 2017a)

Research Objective

As mentioned in the problem description, PS-PWM is an advantageous modulation strategy on MLCs. Thus, in this thesis, a generalized algorithm is proposed for designing the PS-PWM based on its analytical model in order to be implemented on all multilevel converters regardless of structure and number of levels.

Moreover, to overcome the problem of isolated DC sources on MLCs, one topology is invented to achieve the higher voltage levels, lower THD and consequently lower filter size through a single DC source for single-phase and three-phase. This topology is the proper alternative for MMC to reach the higher quality waveform with the lower devices. In addition, a deep learning-based voltage balancer integrated with hybrid phase shift and level shift modulation is proposed in this research work to increase the voltage levels in multilevel converters.

Furthermore, A bipolar configuration MMC is proposed in this thesis to be capable to disconnect the DC fault current through the semiconductor switches instead of the DC circuit breaker.

The summary of research objective is as follows:

- Proposing a Multilevel topology for single-phase, three-phase and MMCs applications.
- Developing the voltage balancing technique integrated with the modulation technique to control the FCs on MMCs without requiring the external controller.
- Developing a deep learning voltage balancer integrated with the hybrid modulation technique to increase the voltage levels on MMCs.
- Developing a (Packed U-Cells) PUC converter as a single DC source three-phase multilevel converter and for MMC applications to remove the DC fault circuit breaker.

Methodology

This research methodology is based on three following steps:

1- Theoretical and mathematical analysis.
2- Simulation in Sim power system toolbox in Matlab.
3- Implementation in an experimental setup in GREPCI LAB.

First, a literature review has been carried out to scrutinize the several types of MLCs and MMCs. Modulation and control techniques are investigated to find their pros and cons. Secondly, mathematical, and theoretical analysis to resolve the problems is carried out. For this research work, the theoretical analysis is performed in three sections including modulation, voltage balancing, and suitable topology for MLCs. Thirdly, simulation and modeling of the novel ideas of topology and modulation are performed by the MATLAB Simulink. Finally, the single-phase pilot experimental set-up of MMCs with the newly proposed topology is constructed in the GREPCI Lab. The control algorithm of voltage balancing integrated with

modulation technique has been implemented on dSpace 1103 as a real-time controller and switching pulses are sent to the switches through the dSpace 1103 interface board.

Thesis Contributions

The main novelties and contributions of this thesis are as follows:

1. **Proposing a single DC source topology for single-phase, three-phase and MMC application**

In this section that is the main part of this research work, ZPUC topology is proposed as a multilevel electric power converter which has been filed in US patent (Saeed Arazm & Al-Haddad, 2019). This topology is originated from the Flying Capacitor similar to the PUC topology. However, in contrast with the PUC, it requires a single DC source in a three-phase system. Moreover, in MMC application, this is a powerful topology that can be a serious alternative to HB-MMC. HB-MMC is the most popular submodule of MMC which is produced by famous manufacturers such as Siemens, ABB, Alstom, and so forth. However, it requires a large number of semiconductor switches and FCs to generate the same voltage levels compared to ZPUC. Comparison between ZPUC and the other well-known topologies demonstrates its superiority for high power and medium voltage applications. In fact, more voltage level generation with the lower components counts makes ZPUC a converter with more power quality and lower cost.

2. **Voltage balancing control method integrated with a modulation technique**

In fact, to eliminate the external control system for voltage balancing of the FCs which reduces the system reliability and increases the total cost of the converter, the voltage balancing integrated with PS and LS-PWM is proposed in this research. Although some topologies like the PUC5 could be operated in sensor-less mode, these converters are not economically feasible due that it causes to the increase in the size of the FCs. Thus, voltage balancing

integrated with the modulation technique is one solution to reduce the size of the FCs without using external control systems.

3. development of voltage balancing on ZPUC-MMC by Deep learning integrated with hybrid modulation to increase the voltage levels

HB-MMCs with N submodules per arm which are largely used in the industries, generate N+1 voltage levels across the load in their output terminals. Although the voltage levels on high voltage applications such as HVDC is as much as high so that its THD is sufficiently low, in medium voltage application, where N is low, generating more voltage levels is advantageous to have a lower THD and consequently to reduce the filter size. In fact, in the usual method of modulation and voltage balancing for HB-MMC, FC-MMC, and ZPUC-MMC, the output voltage is N+1, 2N+1, and 4N+1. To increase the voltage levels on ZPUC-MMC, one method based on the artificial network is presented in this research. A deep learning-based voltage balancer integrated with hybrid LS and PS-PWM is proposed to generate 8N+1 voltage levels with the counts of the same component.

4. Development of PUC as a single DC source modular three-phase PUC

PUC is a Multilevel converter topology that is well-known for its lower components counts. The 5-level waveform is generated by only 6 switches and one FC supplied by a single DC source. However, for the three-phase system, three isolated DC source is required which is not feasible. Thus, to cope with this challenge, one configuration of PUC is proposed in this research work which not only requires a single DC source for three-phase PUC but also, it is a modular multilevel converter which is called Y-PUC (Saeed Arazm & Kamal Al-Haddad, 2020). This configuration can also be called PUC-MMC. Since PUC is a bipolar converter, the output voltage levels of this configuration are less than ZPUC-MMC. Nevertheless, the semiconductor in this configuration can be used to disconnect the DC fault current without using the external DC circuit breaker. The bipolar full-bridge MMC can be replaced by this topology due to the lower size and cost, and power losses. It is also shown in this section that the components count of PUC-MMC is lower than HB-MMC.

Thesis Outline

The structure of this thesis is organized as follows:

Chapter 1 reviews the state of the arts of the multilevel converters and MMCs as well as the modulation methods. The topologies and waveforms of the famous and new converters are reviewed, and their challenges are explained. In Chapter 2, ZPUC multilevel converter topology is proposed and generalized ZPUC topology is developed. Moreover, modeling, control, and voltage balancing, switching states, circulating current, reliability, and power losses are completely explained on ZPUC-MMC. Increased voltage levels ZPUC-MMC through deep learning-based voltage balancing integrated with hybrid PS-PWM and LS-PWM modulation is described in chapter 3. Chapter 4 introduces a complete approach to a single DC source modular three-phase PUC converter. Moreover, challenges of PUC-MMCs including circulating current are discussed in this chapter. Finally, the conclusion of this thesis is discussed and some related ideas according to the author's opinion for future studies are listed.

CHAPTER 1

LITERATURE RIVIEW ON MULTILEVEL AND MODULAR MULTILEVEL CONVERTERS

1.1 Introduction

Multilevel converter (MLC) is firstly introduced in 1975 by Baker in which multilevel waveform is generated at the output of the converter instead of the two-level waveform (R. H. Baker & Bannister, 1975). This topology that is called cascaded H-bridge (CHB), requires a large number of isolated DC sources to generate more voltage levels. The same authors introduce a topology to generate 3-Level and 5-Level with a single DC sources due to the fact that isolated DC sources are very bulky, heavy, and costly (R. Baker, 1980). This topology which is called Neutral point diode clamped was later developed by Nabae (Nabae, Takahashi, & Akagi, 1981). Then in 1992, the multilevel technology based on flying capacitor was invented which is the basic concept of a large number of novel MLCs topologies which are recently designed (Lavieville, Carrere, & Meynard, 1997),(T. Meynard & H. Foch, 1992),(Bin Wu & Narimani, 2017a).

MLCs have become more popular due to the following reasons: lower stress on power switches because of lower dv/dt, lower total harmonic distortion which leads to the lower filter size and better electromagnetic interference, the lower common-mode voltage which is better for motor drive application, switching redundancy that facilitates the voltage balancing and fault tolerance, output current with smaller THD compared to the two-level converter, lower switching frequency and lower switching losses, and combination of MLCs with the renewable energies such as wind and solar plants.(Gupta, Ranjan, Bhatnagar, Sahu, & Jain, 2016)

Since the MLCs require a great number of semiconductor devices, designing the reduced device counts MLC is always unavoidable. Hybrid topologies which are often comprised of two or more classical multilevel converters are one of the common ways to reduce the

components counts (Abarzadeh & Al-Haddad, 2019). In fact, the most important criteria to evaluate the MLCs are as following: 1. The number of semiconductor devices, 2. The total blocking voltage of the converter, 3. Controllability and simplicity of the converter to balance the voltages or sensor-less balancing. However, the application of the converters is the most important factor to define the competency of the MLC topology.

Modular multilevel converter (MMC) was firstly proposed by Prof. Marquardt that was implemented on half-bridge (HB-MMC) converter aiming to employ the multilevel converters in high voltage DC (HVDC) system. Voltage levels, modularity and scalability, simplicity in repair and maintenance, high efficiency, low switching frequency, small switching losses, THD reduction, and small size of the filters are the main advantages of this type of multilevel converters (Abarzadeh & Al-Haddad, 2019; Amarir & Al-Haddad, 2008; Javadi & Al-Haddad, 2015; Lesnicar & Marquardt, 2003). PI controllers have been used in HB-MMC to balance the FC voltages and to suppress the circulating current (Hagiwara & Akagi, 2009).

Although a large number of MLCs have been introduced in research work, a few of them can be employed as a submodule on MMCs. A three-level flying capacitor multilevel converter (FC-MLC) is a multilevel topology that is placed as a submodule of MMC with the purpose of increasing the voltage levels and improving the performance of MMCs (A. Dekka, Wu, Zargari, & Fuentes, 2016). In (Solas et al., 2013a, 2013b) authors replaced two-level half-bridge (HB), 3-level NPC, and FC as the submodules in MMC configuration. This research shows that the NPC is not a proper topology for MMC submodules due to unbalance in flying capacitors voltages. Moreover, although the capacitors are acceptably balanced in three-level FC-MMC, it does not have a considerable advantage rather than the HB-MMC due that the number of switching devices and capacitors are identical to generate the given voltage levels. However, the rated voltage blocking and the size of half of the flying capacitors and switches of 3L FC-MMC are twice those for HB and the rests have the same size. 3L FC-MMCs and their all issues have been discussed in (Du, Wu, & Zargari, 2017; Du, Wu, Zargari, & Cheng, 2017). Despite the mentioned disadvantages of 3L FC-MMC compared to HB-MMC, the authors (Du, Wu, & Zargari, 2018) verifies that this configuration of MMC is advantageous

for motor drives application due to deal with the issues of low-speed operation evaluated against the HB-MMC.

The Cross-connected submodule is introduced by authors in (Nami, Wang, Dijkhuizen, & Shukla, 2013) that uses two cells of half-bridge which have been connected in crossway for dc fault breaking current. This topology can be used as a submodule of MMCs individually or in a hybrid with half-bridge cells. Thus, proposing a suitable topology of MLCs to be replaced by the submodules of MMCs in order to reduce the components counts, power losses, and increasing the reliability for given voltage levels would be a great contribution. In the next sections, several well-known topologies as well as the recently introduced topologies, are discussed to draw out the highlights and challenges.

1.2 Conventional 2-Level converters

The basic topology of conventional converters is shown in Figure 1.1. This configuration is called a full bridge or H-bridge, because of the apparent arrangement. Switches of each arm operate in a complementary manner. Thus, the voltage across the load varies between $-V_{dc}$ and $+V_{dc}$. Two voltage levels generate the high content of THD at the output of the inverter so that the large size of the filters must be utilized to reduce the filter size. In addition, voltage and power permissible rates of switches are another issue for high voltage and high-power applications. This is a reason why the series switches are utilized in this figure to divide the voltage among the switches. However, higher THD, the number of elements and, power losses are the problems that lead the researcher and manufacturer to use the multilevel converters.

1.3 Multilevel converters topologies

1.3.1 Cascaded H-Bridge

Cascaded H-Bridge (CHB) is obtained by cascading the conventional 2-L voltage source

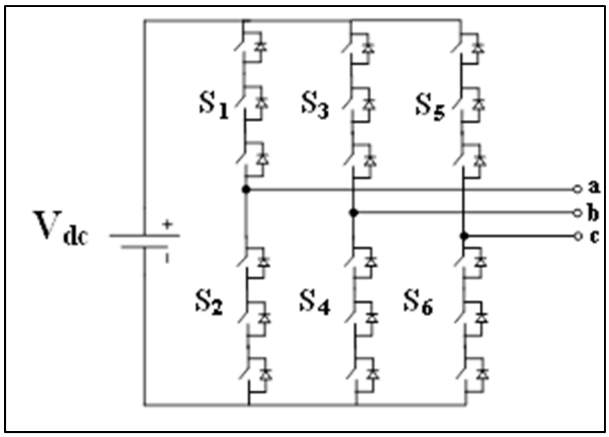

Figure 1.1 Conventional 2-L converter with series switches

converters. Consequently, a multilevel waveform can be achieved to alleviate the voltage stress on devices. A three-phase CHB with three cascaded H-bridge is depicted in Figure 1.2 in which a 7-L single-phase waveform is generated at the output. The output voltage is equal to the sum of the voltages of each cell. For example, in this figure, $V_{aN}=V_{H1}+V_{H2}+V_{H3}$. Figure 1.3 shows the 7-level waveforms of the inverter to clarify the pulse technique in CHB. It should be noted that the DC source voltage at CHB could be either equal or unequal. The number of single-phase voltage levels for equal type is given by:

$$L_{Phase} = 2N + 1 \tag{1.1}$$

Where, L implies the number of voltage levels for N cells of H-Bridge for a single-phase system. Generally, the voltage level in line voltage is obtained by the following equation:

$$L_{Line} = 2L_{Phase} - 1 \tag{1.2}$$

Where, L_{Phase} and L_{Line} are the level number of phase and line voltage waveform, respectively. Moreover, the switching states and their corresponding redundancy are listed in Table 1.1 for CHB with two cells. It can be seen from this table that 16 switching states generate five voltage levels for single-phase including +2E, +E, 0, -E, -2E when the DC source voltage is equal to E. Although the equal DC source is worthwhile due that all the devices require the same rated

voltage, the plenty of the redundant states cause to use more devices for given voltage levels. In unequal DC source CHB, if $V_{DC1}=2V_{DC2}$, then 7-L and when $V_{DC1}=3V_{DC2}$, then 9-L is generated across the load. It is evident that, the redundancy in 9-L may not be sufficient for some purposes such as fault tolerant and voltage balancing modes.

Table 1.1 Switching States of 5L CHB With Equal DC Source

State	S11	S31	S12	S32	Output Voltage
1	1	0	1	0	2E
2	1	0	1	1	E
3	1	0	0	0	E
4	1	1	1	0	E
5	0	0	1	0	E
6	0	0	1	1	0
7	0	0	0	0	0
8	1	1	1	1	0
9	1	1	0	0	0
10	1	0	0	1	0
11	0	1	1	0	0
12	0	1	0	0	-E
13	0	1	1	1	-E
14	0	0	0	1	-E
15	1	1	0	1	-E
16	0	1	1	1	-2E

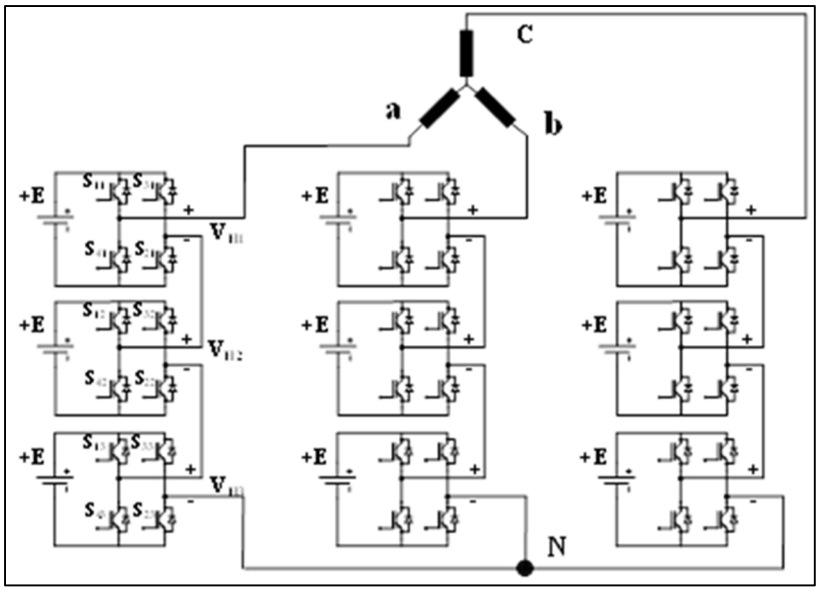

Figure 1.2 Three-phase cascaded H-Bridge with 7-L phase-voltage

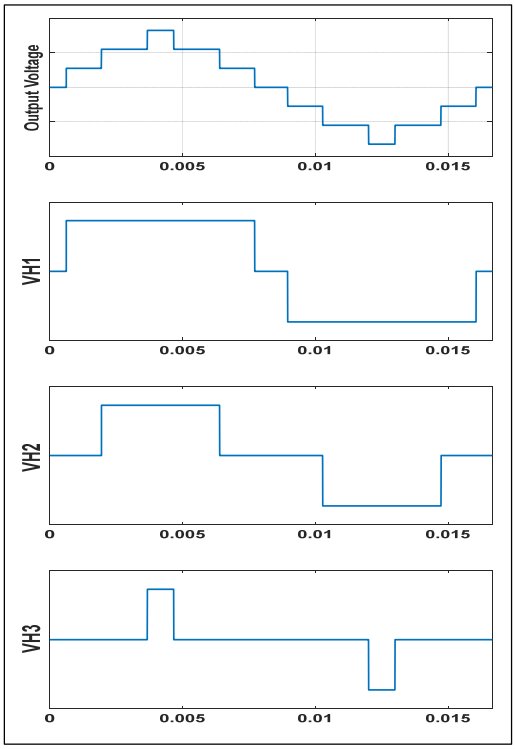

Figure 1.3 7L waveforms in CHB with three cells

1.3.2 Neutral Point Clamped (NPC) and its family topologies

NPC topology is a multilevel converter that produces even and odd voltage levels in contrast to the CHB that is only capable to produce the odd levels. Four and five-level NPCs are not usually used by the industry due to the high number of components and voltage balancing issues. In other words, NPCs are most popular as a three-level multilevel inverter.

Figure 1.4 shows a three-phase, three-level NPC inverter that could be used instead of conventional two-level VSI. Figure 1.5 illustrates a 3-level single-phase voltage waveform as well as the current wave at the output of NPC.

Figure 1.6 depicts a 5-Level NPC with 8 switches and 6 unequal rated voltage diodes or 12 equal rated voltage diodes which it is not interested in the industry. 5-L NPC output 5-Level voltage waveform as well as the output current is depicted in Figure 1.7.

In addition, 5L HNPC multi-level inverter has been also proposed based on equation 1.2 to generate more voltage levels with lower components counts compared to 5L NPC. Figure 1.8 shows a three-phase 5L HNPC in which the letter H is chosen due to its similarity by the full-bridge converters (Cheng & Wu, 2007).

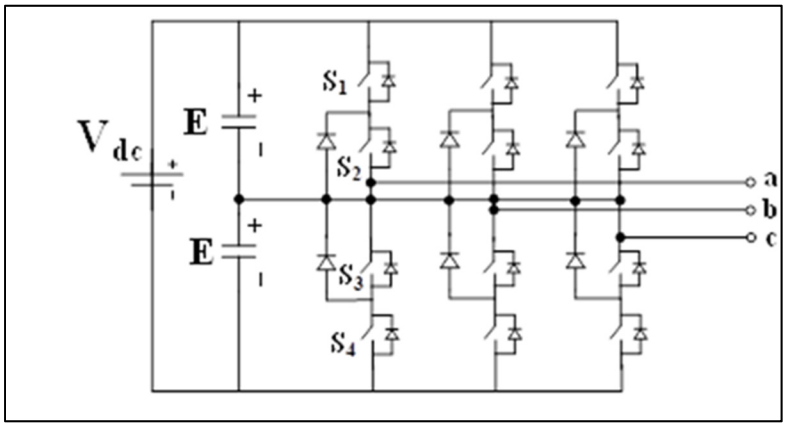

Figure 1.4 Three-phase three-level NPC

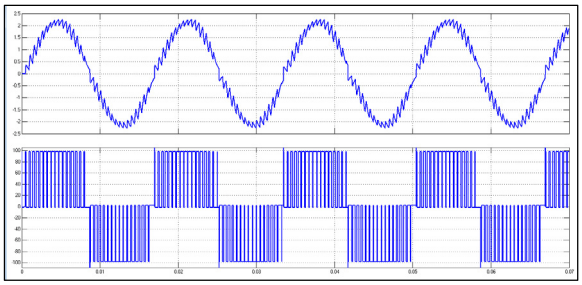

Figure 1.5 Load current and phase voltage across the output terminals in 3L NPC

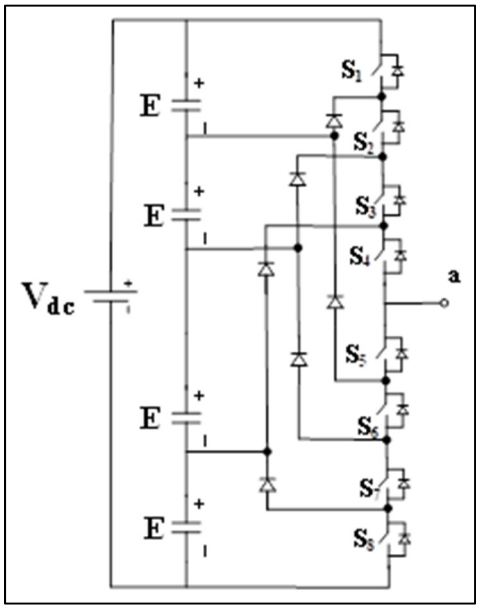

Figure 1.6 Single-phase 5L NPC

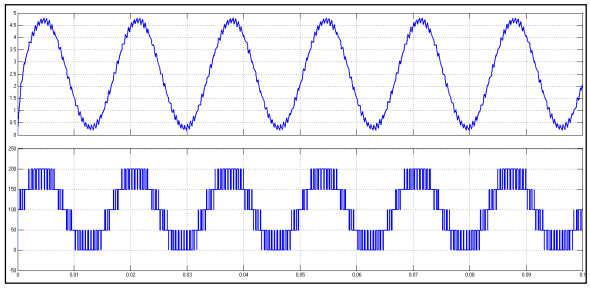

Figure 1.7 Load current and voltage at the output of 5L NPC

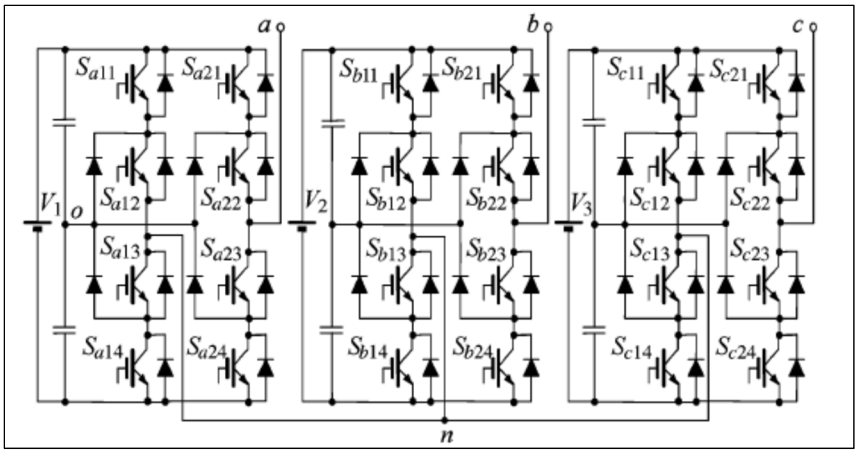

Figure 1.8 Three-phase HNPC to generate 5-level waveform
Taken from Cheng & Wu (2007)

Another configuration which is extracted from HNPC is called Active NPC or ANPC which is a patent of ABB Company. Since the voltage stresses of switches are not equal in NPC, the power losses are distributed unevenly which causes the design of the special consideration for a cooling system. ANPC is invented to address this problem so that the IGBTs are substituted by diodes at NPC. Accordingly, it leads to the distribution of uniform losses among switches. This topology is shown in figure 1.9 (Bruckner, Bernet, & Guldner, 2005).

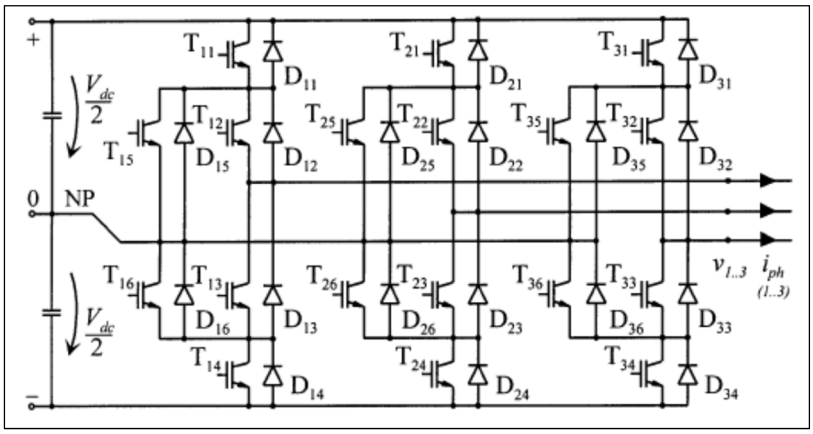

Figure 1.9 Three level ANPC topology
Taken from Bruckner, Bernet, & Guldner (2005)

In flying capacitor multilevel topology, the clamped diode in NPC is replaced by the flying capacitors. It is derived from a two-level inverter that every two switches are supplied by a capacitor. Since a large number of flying capacitors are used in FC, it accordingly requires plenty of isolators for DC capacitors and a complex voltage balancing control which complicates its industrial applications. Figure 1.10.a. shows a three-phase three-level FC topology in which a bipolar waveform including the voltages +Vdc, 0, and -Vdc are produced in V_{aN1}. However, through replacing the null point N1 with point N2, unipolar waveforms with the levels 0, Vdc, 2Vdc are generated at V_{aN2}. In addition, a 5L single-phase FC topology is depicted in Figure 1.10.b in which the flying capacitors must tolerate the voltages 3Vdc/2, Vdc/2, and Vdc/4 and consequently, all the switches have to suffer Vdc/4. The capacitors with different rated voltages can also be replaced by the series capacitors with identical nominal voltages. Apart from these well-known topologies, considerable amounts of MLCs are introduced in recent years so as to achieve higher performance and quality with lower cost.

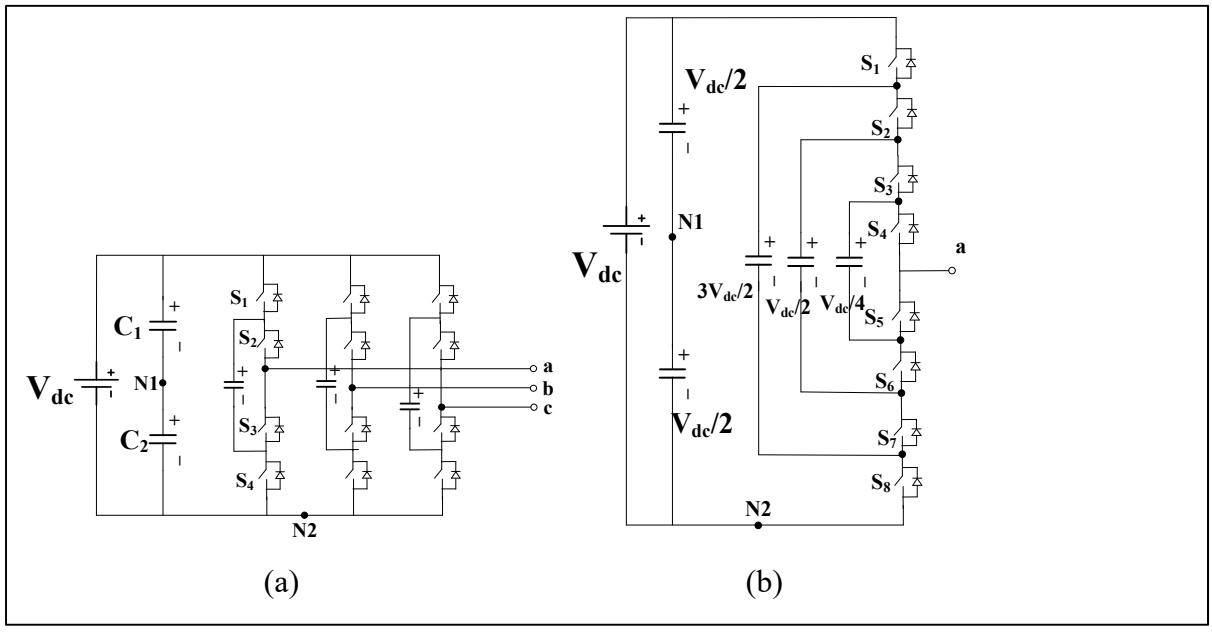

Figure 1.10 Flying capacitor multilevel topology a) three-level three-phase FC b) 5L single-phase FC

In (Gupta et al., 2016) the authors review the MLCs with reduced component counts. Authors in (Poorfakhraei, Narimani, & Emadi, 2021) review the topologies which are used in electrical

vehicles. In (Salem, Khang, Robbersmyr, Norambuena, & Rodriguez, 2021), the authors investigate some topologies of hybrid MLCs to reduce the counts of the component. Some of the interesting topologies which lead to reducing the counts of the devices are investigated in the following subsections.

1.3.3 Hybrid T-type NPC and FC H-bridge:

In this topology, one T-type NPC is connected to FCHB in which a 9L waveform is generated through the connection of two low-frequency switches to the DC source. In this topology, the FC voltages are balanced naturally through the PWM strategy.

Figure 1.11 shows this topology and its application in PV connection to the grid (Sandeep & Yaragatti, 2017).

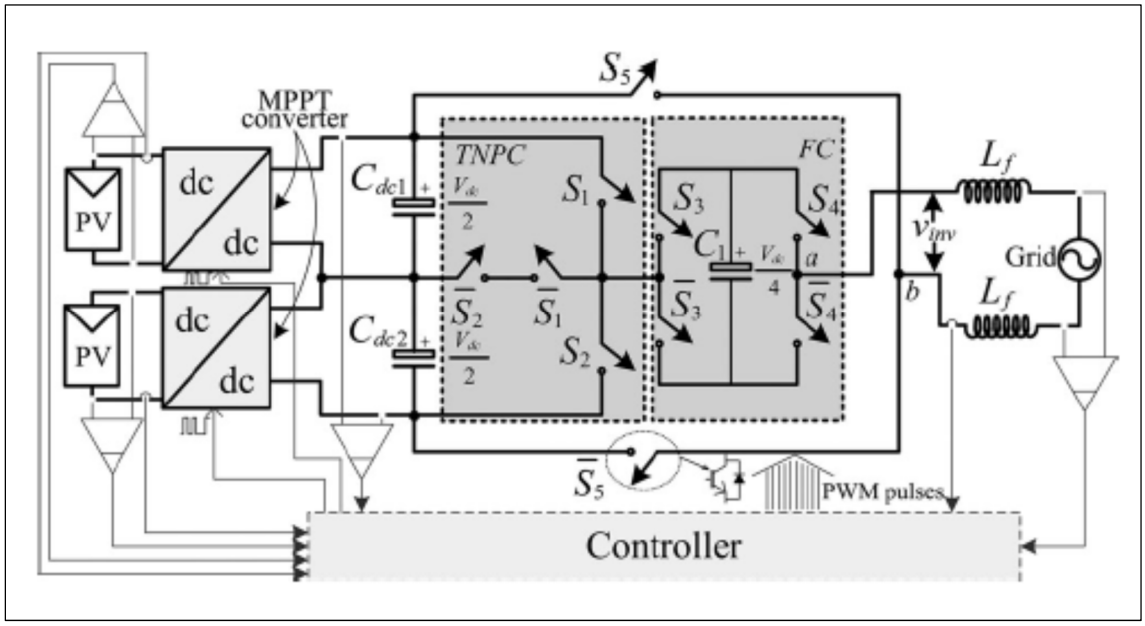

Figure 1.11 Hybrid multilevel converter to generate 9L waveform
Taken from Sandeep & Yaragatti (2017)

1.3.4 Topologies T-Type based structure:

The T-type structure is depicted in Figure 1.12.a in which two switching devices are replaced by two diodes in NPC topology; however, there is a slight difference in their structures. It is firstly invented by authors (Guennegues, Gollentz, Meibody-Tabar, Rael, & Leclere, 2009) which represent a valuable 3L converter compared to NPC due that the blocking voltage of the semiconductor devices is half of the NPC. Moreover, in Figure 1.12.b an H-bridge T-type is illustrated in which not only the voltage levels are increased to 5L, but also the power losses are reduced due that the middle switches operate in system frequency. In (Bahrami & Narimani, 2019) authors present one 5L T-Type Nested Neutral Point Clamped (T-NNPC) Converter. T-NNPC is illustrated in figure 1.12.c in which V_{C1} and V_{C2} must be one-quarter of the DC source to generate five voltage levels.

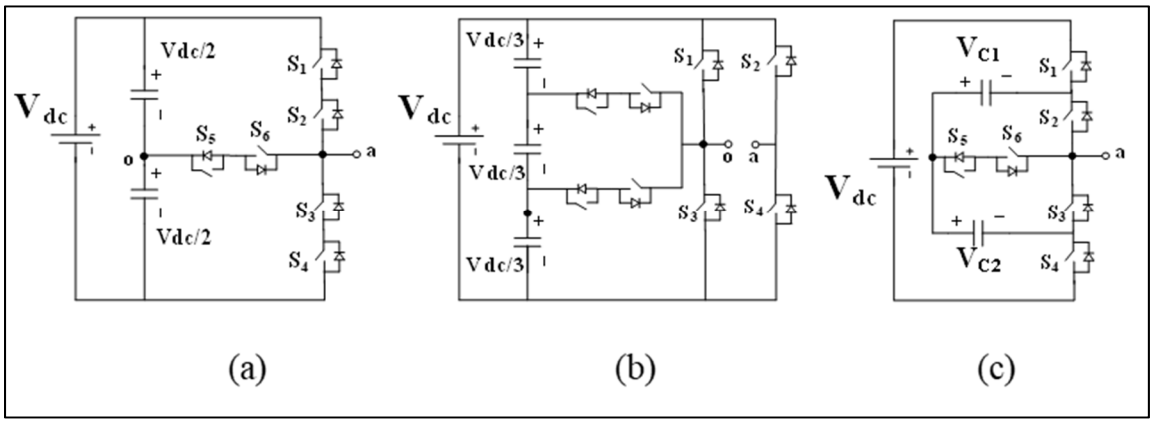

Figure 1.12 T-type based multilevel converter topologies a) T-type 3L Converter b) H-Bridge T-type 5L c) T-NNPC 5L Converter

1.3.5 Packed U-Cell (PUC) topology and switching states

PUC inverter was firstly introduced as a 7-level topology. Afterward, it was developed as a 5-level converter to simplify its complicated voltage balancing. The main benefits of PUC5 are single-DC-source, sensor-less voltage balancing of the auxiliary capacitor, reliable performance and reduced counts of components (K. Al-Haddad, Ounejjar, & Gregoire, 2011;

Metri, Vahedi, Kanaan, & Al-Haddad, 2016; Trabelsi, Bayhan, Ghazi, Abu-Rub, & Ben-Brahim, 2016; Trabelsi, Bayhan, Metry, et al., 2016; Vahedi & Al-Haddad, 2015; Vahedi & Al-Haddad, 2016a; Vahedi, Al-Haddad, & Kanaan, 2014). To achieve this purpose, FC voltage must be regulated at half of the DC source voltage which makes a 5-L waveform at the output of the converter. PUC topology is depicted in Figure 1.13 in which one FC, as well as 6 switches, are used to generate a 5L waveform. One component counts comparison between PUC5 and the other topologies is listed in table 1.2. It demonstrates that this topology is more cost-effective than the other mentioned inverters. Table 1.3 illustrates the switching states and conditions to produce 5 and 7 level waveforms. This table shows that there are no redundant switching states for PUC7 that cause a complicated control system to balance the FC voltages.

Table 1.2 Component Counts of Single-Phase MLCs to Generate 5L Waveform

Inverter Type	DC Source	Flying Capacitor	Clamped Diode	Active Switch	Total equipment
CHB	2	0	0	8	10
NPC	1	4	6	8	19
ANPC	1	3	0	8	12
FC	1	3	0	8	12
PUC	1	1	0	6	8

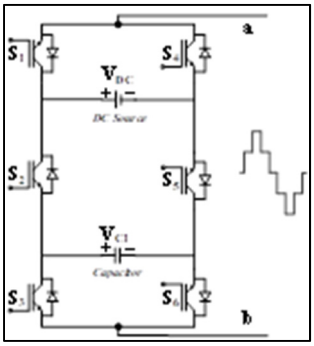

Figure 1.13 PUC topology

Table 1.3 Switching States of PUC Converter to Generate 5 and 7 Level Waveform

State	S1	S2	S3	Vout	Vout(PUC-5)	Vout(PUC-7)
1	1	0	0	V1	2E	3E
2	1	0	1	V1-V2	E	2E
3	1	1	0	V2	E	E
4	1	1	1	0	0	0
5	0	0	0	0	0	0
6	0	0	1	-V2	-E	-E
7	0	1	0	V2-V1	-E	-2E
8	0	1	1	-V1	-2E	-3E

PUC9 is an extended topology of PUC5 which is obtained by adding one more switch in each arm. Since nine voltage levels are generated at the output of PUC9, THD and consequently the size of the filters are considerably reduced.

Moreover, due to the redundant switching states, FCs voltage is balanced integrated with modulation strategy. However, 15 levels at the output of this inverter can be generated with a complex control system due to the fact that there is not sufficient redundancy in switching states. Equation 1.3 illustrates the relationship between voltages and switching states.

$$V_{ab} = V_{dc}(S_1 - S_2) + V_{c1}(S_2 - S_3) + V_{c2}(S_3 - S_4) \tag{1.3}$$

Figure 1.14 shows the topology of PUC9. Switching states and voltage balancing on PUC9 are discussed in detail in (S. Arazm, Vahedi, & Al-Haddad, 2019). In addition, in (S. Arazm, Kamwa, & Al-Haddad, 2019), 15-Level waveform is produced by the same topology through model predictive control method.

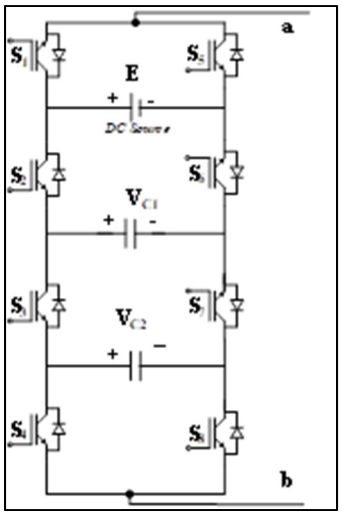

Figure 1.14 PUC9
converter topology

1.3.6 Topologies with PUC structures

The PUC converter and its families that have already been introduced for single-phase systems are the topologies with the counts of the reduced component. They are almost more suitable than their counterparts for a given voltage level generation.

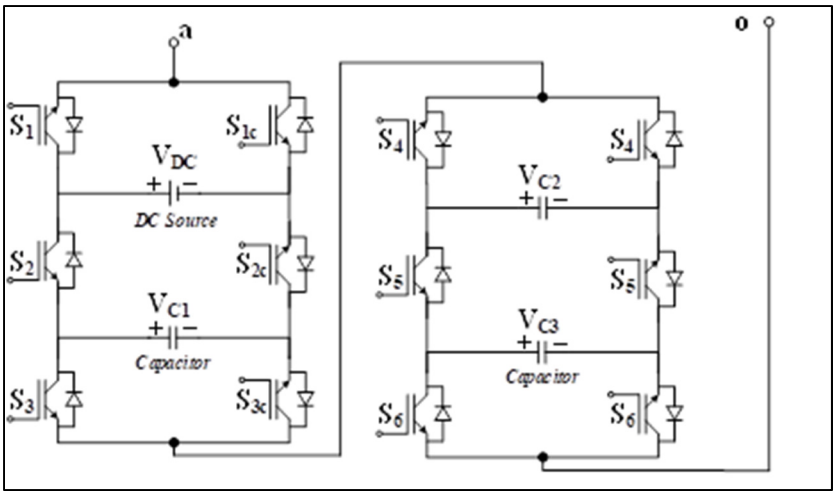

Figure 1.15 H-PUC 23Level multilevel converter

1.3.6.1 H-PUC

Authors in (Sorto-Ventura, Abarzadeh, Al-Haddad, & Dessaint, 2020) propose two cascaded single DC source PUC converters to generate 23 levels. Finite control set model predictive control is used to balance the voltages in FCs. Figure 1.15 illustrates a single DC source H-PUC converter.

1.3.6.2 Qn-Hybrid-NPC

Qn-Hybrid-NPC is depicted in Figure 1.16 in which one HNPC topology is connected to one PUC converter with the aim of obtaining more voltage levels. Hybrid of one 5L HNPC with PUC5 converter leads to generate 21Level in this topology with modulation technique and without using the complicated control system (Abarzadeh & Al-Haddad, 2019).This topology is capable to generate more voltage levels through additional modules of PUC5. Basic topology requires two isolated DC sources, and each additional PUC requires its DC source.

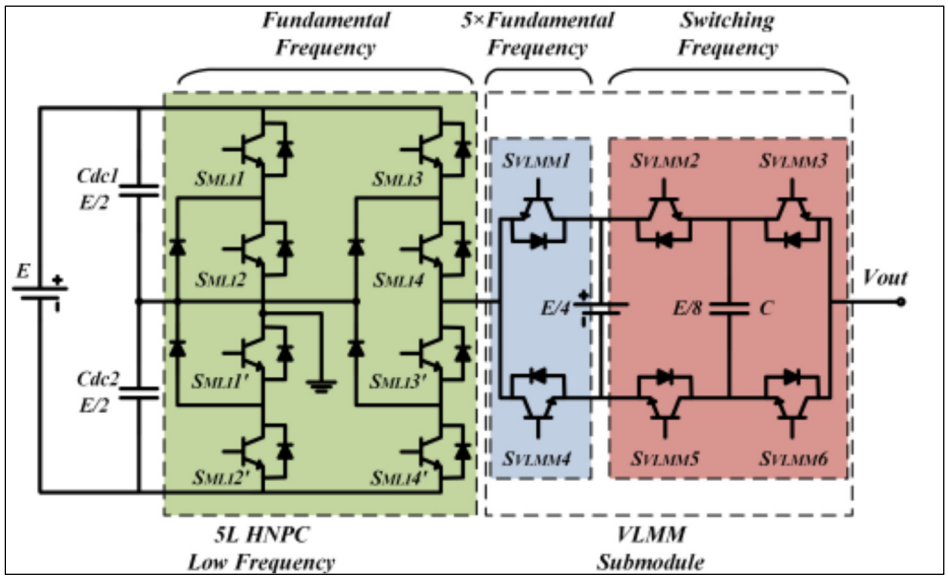

Figure 1.16 21 Level Qn-Hybrid HNPC
Taken from Abarzadeh & Al-Haddad (2019)

1.3.6.3 Packed E cell (PEC) converter topology

This topology includes 8 switches and one DC source as well as 2 flying capacitors which generate 9L at the output. This topology is depicted in Figure 1.17 which is a single-phase and single DC source with two FCs (Sharifzadeh & Al-Haddad, 2019). This topology is highly similar to the PUC9 topology regarding their reduced component counts.

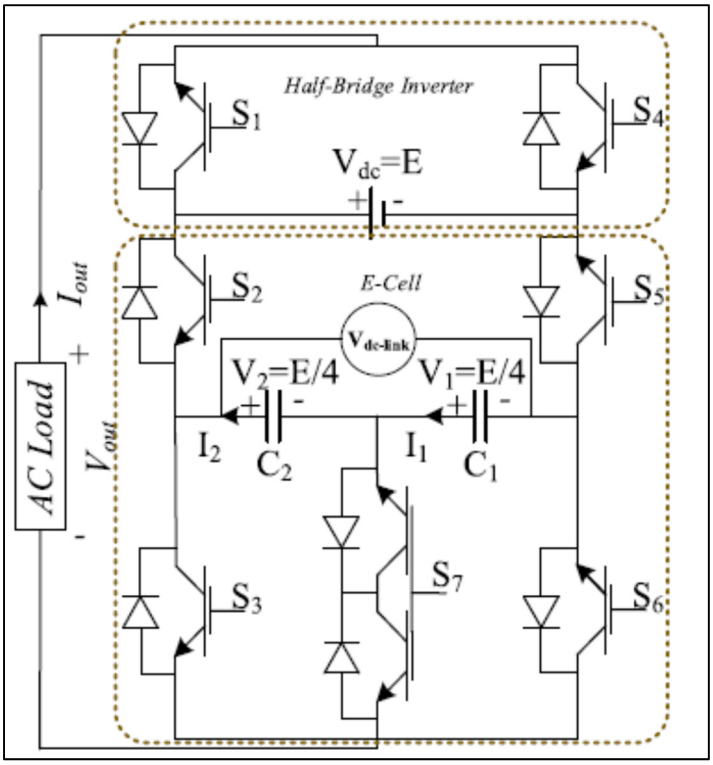

Figure 1.17 Packed E-cell (PEC) multilevel converter topology
Taken from Sharifzadeh & Al-Haddad (2019)

1.4 Modular multilevel converters (MMCs)

This type of converter includes some scalable modules of multilevel converters (MMC), which could be used for high voltage and high-power applications. Their principal merits are as follows:

- Modularity, which is vital for repair and maintenance due to the simple exchange of the affected modules by the new ones.
- voltage scalability.
- lower total harmonic distortion (THD) (which higher one cause the thermal problem and aging on batteries)
- higher quality of output voltage and current waveforms.
- fault tolerance and redundancy.
- Reducing the power losses in semiconductor switches due to lower switching frequency.
- Filter size reduction.

Three classifications are proposed for MMCs including: 1. single star configuration, 2. delt configuration, and 3. double star configuration, that double star is most well-known among them (Hagiwara & Akagi, 2009). In fact, the delta and single star types are not applicable for most of the topologies, and this is a reason why double star configuration is a general configuration and all surveys in research and industry use this configuration.

Generally, there are two types of submodules including unipolar and bipolar which are employed as submodules of MMCs. Bipolar topologies in contrast to unipolar topologies are capable to disconnect the DC fault current; however, they require more devices than unipolar ones.

MMC configuration along with 6 famous submodules are illustrated in figure 1.18.

Figure 1.18.a and b depict the most popular modules of MMCs including unipolar half-bridge and bipolar full-bridge converters which are called HB-MMCs and FB-MMCs. Switching devices for FB submodule is two times of HB submodules which means higher losses, cost; however, they do not need the external DC circuit breaker to disconnect the DC fault. In (Adam, 2015) FB-MMC is developed and the control strategy is introduced to balance the

voltages and disconnect the faults. Although FB generates a 3-Level voltage waveform, two positive levels among them are only used to synthesize the output waveform of MMC.

FC-MMC is a 3L unipolar MMC which is shown in figure 1.18.c. They comprise 4 switches and two flying capacitors for generating three voltage levels. Since the two modules of HB can also generate 3-Level waveform with the lower size of the flying capacitor, its industrial application is not so far advertised; however, it is almost popular in the research area.

Moreover, NPC is a 3L multilevel converter that can be replaced by submodules of MMCs (Glinka & Marquardt, 2005; Solas et al., 2013a, 2013b). However, the results which are shown in (Solas et al., 2013b) demonstrate that NPC-MMC is not as appropriate as HB, FB, and FC-MMC in normal conditions when the power factor is close to 1. In contrast, it is applicable and competitive for special applications such as STATCOM where the $\cos\varphi=0$. This submodule topology is shown in figure 1.18.d.

Cross-connected topology is shown in figure 1.18. e is a 5-L MLC that is proposed by Nami (Nami et al., 2013) as a bipolar converter. Since FB-MMC requires a large number of switching devices, this topology is a promising alternative for given voltage levels. This submodule comprises 6 semiconductor switches as well as two flying capacitors. Moreover, in this article authors proposed an MMC with a hybrid cross-connected submodule and HB submodule to reduce the size, cost, and power loss. In the fault occurrence, switches S5 and S6 will be opened and the fault current flows from the antiparallel diodes through the negative polarity of the C1 and C2.

The Clamp-Double submodule which is illustrated in figure 1.18.f is a bipolar topology with two half-bridge cells as well as two diodes and one more switch. This topology is more beneficial than the FB submodule for given voltage levels due to reduced counts of devices which lead to a lower power loss.

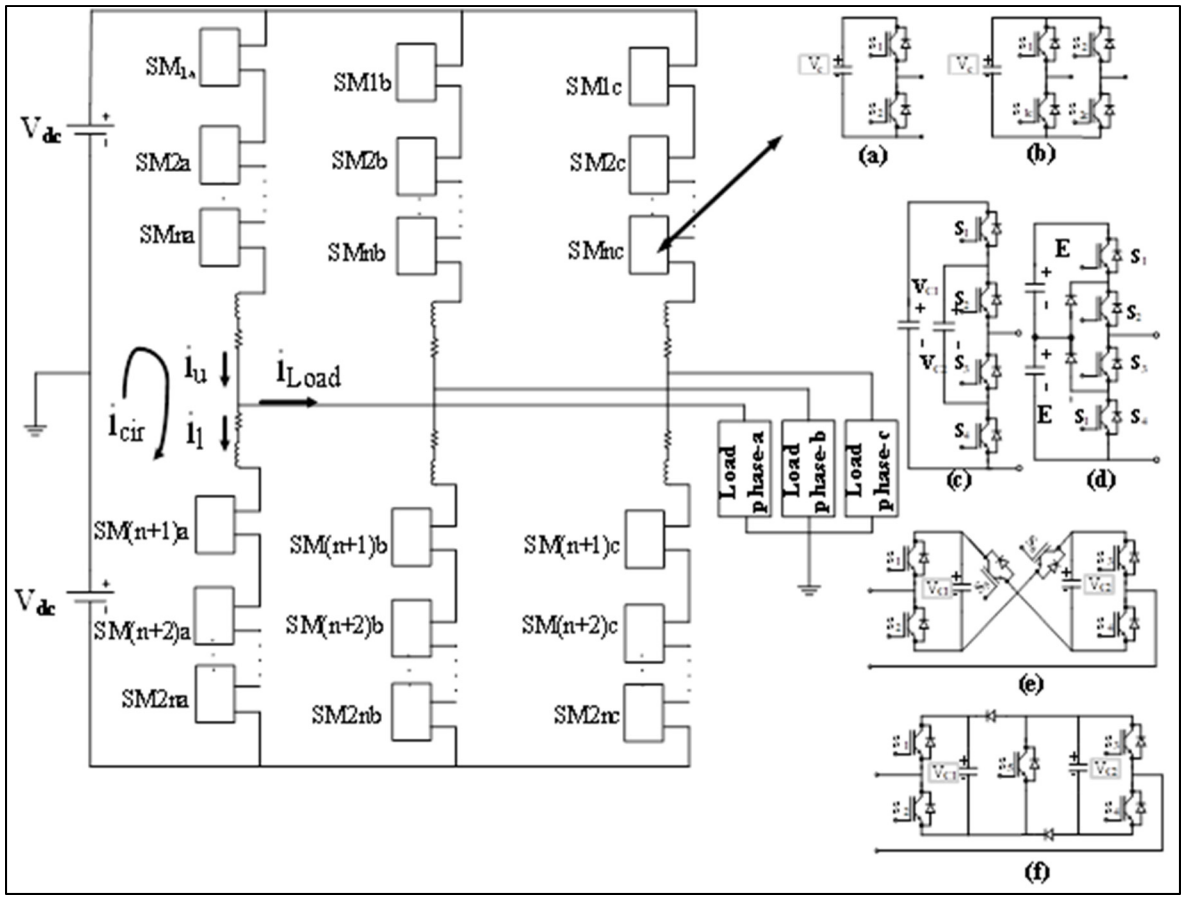

Figure 1.18 Double star MMC configuration a) HB-MMC b) FB-MMC c) FC-MMC d) NPC-MMC e) cross connected-MMC f) Double clamped-MMC

Furthermore, (Adam et al., 2017) authors present one topology which is very similar to ANPC as a submodule of MMC. This topology is more reliable than HB and reduces the power losses in the HVDC system. Three voltage levels including 2Vc, Vc, and 0 is generated which are exactly like the 3L FC. This submodule is shown in figure 1.19.a.

Simplified FB double submodule topology (S-FBDSM) is introduced by the authors in (Meng et al., 2021) which is bipolar topology to address the fault DC breaking current. figure 1.19.b shows that this topology constitutes two half-bridge as well as two diodes and two more switches to block the converter during the DC fault.

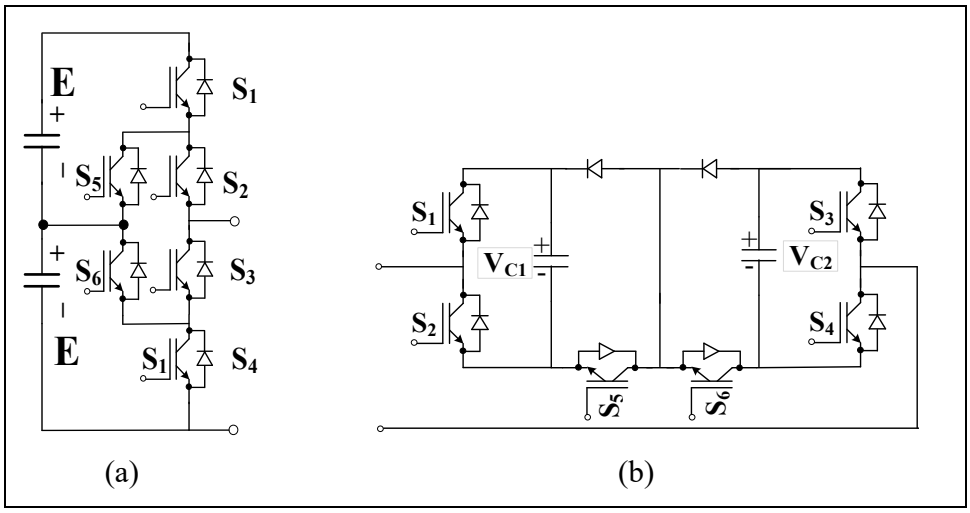

Figure 1.19 MMC submodules a) Modified ANPC submodule for MMC
b) S-FBDSM

The principal challenges of MMCs are the voltage balancing on the flying capacitors. In fact, all MLCs could not be employed as a submodule of MMCs due that their capacitors are not balanced appropriately for all types of loads, modulation index, and switching frequency. This is the main reason why the number of appropriate submodules for MMCs is not as much as MLCs. Fault tolerance, reliability and contingency, modulation, and control, circulating current control, DC and AC faults, are the other controversial issues in MMCs. The applications of MMCs are as following: 1. HVDC transmission system 2. Medium Voltage DC (MVDC) system such as shipboard, on-board converters, energy storage system, and active filter applications which require high-reliability converters, 3. motor drive application which requires a lower ripple FCs voltage, lower common-mode voltage, and circulating currents to extend the life duration aiming to reduce the aging. 4. STATCOM, a special reduced count of devices configuration of ZPUC topology is introduced in (S. Arazm & Al-Haddad, 2021) which is appropriate for this application 5. Solid-state transformer 6. High voltage pulse generator (M. A. Perez, Ceballos, Konstantinou, Pou, & Aguilera, 2021)

It should be noted that the MMCs are almost operated transformerless and without external filters or with a small size of the filters. However, for a given application, the proper design must be carried out and compromise must be performed among the alternatives of MLCs or

MMCs converters. Figure 1.20 illustrates the figure of STATCOM built by HITACHI ABB group (Hitachi-ABB, 2009).

Figure 1.20 STATCOM with the MMC structure
Taken from Hitachi-ABB (2020)

1.5 Modulation strategies

There are some strategies to modulate the waveforms of the multilevel converters. Carrier-based techniques include: 1. phase-shift pulse width modulation (PS-PWM), 2. level-shift pulse width modulation (LS-PWM) and vector-based technique include space vector modulation (SVM) (S. Arazm, H. Vahedi, & K. Al-Haddad, 2018a, 2018c). Moreover, Multiband hysteresis modulation for the multilevel converter and adaptive current control are the other strategies for modulation at current control mode inverters (Shukla, Ghosh, & Joshi, 2011). Furthermore, selective harmonic elimination pulsed width modulation (SHE-PWM) and selective harmonic mitigation pulse width modulation (SHM-PWM) are the other methods for modulation that eliminate and mitigate the amplitudes of desired harmonic orders, respectively and would be profitable at low switching frequency (Pérez-Basante et al., 2018). The nearest level is a modulation technique which operates in power frequency and due to its simplicity is interesting in industrial applications; however, its THD is more than the multicarrier PWM.

PS-PWM is an approach with better harmonic performance than the LS-PWM. The carriers frequency and the number of carriers for a multilevel converter at PS-PWM and LS-PWM are similar; however, the amplitude of all carriers in LS-PWM is divided by their number; whereas, their magnitude in PS-PWM are independent of their levels and all of them are 1pu (K. Wang, Zheng, Wei, Fan, & Li, 2017). Some profound advantages of PS-PWM rather than LS-PWM are as follows: (Huang, Zou, & Ma, 2016; Shi, Wang, Tolbert, & Wang, 2013; Townsend, Summers, & Betz, 2015):

- Equal distribution of losses among all semiconductor switches in the CHB family of multilevel converters.

- Exact switching frequency in comparison with the other modulation strategy such as LS-PWM and SVM.

- Shifting the harmonics to the higher orders reduces the size of output filters significantly.

- Reduced total harmonic distortion (THD) of output voltage/current waveforms due to shifted harmonics to the higher orders

- Faster voltage balancing of the auxiliary capacitor (Thielemans, Ruderman, Reznikov, & Melkebeek, 2012)

Conventional PS-PWM has been introduced for cascade H-bridge in (Rabinovici, Baimel, Tomasik, & Zuckerberger, 2013). Because of the above-mentioned advantages, the design and modification of PS-PWM have been carried out and implemented on a variety of converter topologies. For instance, in (X. Liu et al., 2017), a PS-PWM was applied on a diode clamped converter. In (Kartick, Sujit, & Suparna, 2016), a dual reference PS-PWM was implemented on a 5-level hybrid single-phase inverter module. In (Ghias, Pou, Capella, Acuna, & Agelidis, 2016), an improved method of PS-PWM was applied on flying capacitor converters. In (C. Li, Wang, Guan, & Xu, 2017), a hybrid modulation concept using space vector modulation (SVM)

and PS-PWM was implemented on a 5L-ANPC converter. In (Sepahvand, Liao, Ferdowsi, & Corzine, 2013), a five-level cascaded H-bridge converter with one DC voltage source and one capacitor has been modeled. It used the PS-PWM as a modulation technique and a closed-loop to regulate the capacitor voltage at a certain level. All those published works proved the capability of the PS-PWM to run the multilevel power converters with better harmonic performance. On the other hand, there are some limitations to apply the phase shift strategy for some topologies. As an example, in (M Liserre, Monopoli, Dell'Aquila, Pigazo, & Moreno, 2006; M. Liserre, Pigazo, Monopoli, Dell'Aquila, & Moreno, 2005; Monopoli, Ko, Buticchi, & Liserre, 2017; Bin Wu & Narimani, 2017a), authors stated that PS-PWM strategy could not be applied on CHB when their voltage DC sources are unequal and for NPC. However, in this thesis, one general method of PS-PWM is proposed and is implemented in proposed MLCs which in general is capable to implement on all types of MLCs, and MMCs.

1.5.1 Level-shift Modulation (LS-PWM)

Carrier's arrangements determine the type of modulation. In LS-PWM, the carriers are located vertically between -1 to1 in order to be modulated by the modulating signal. Thus, their peak-to-peak amplitude should be divided by the number of carriers.

It should be noted that in all multilevel converters the number of carriers is equal to the number of voltage levels at the output of inverters minus one which is given by:

$$N_{cr} = n - 1 \tag{1.4}$$

$$A_{Cr(Peak-Peak)} = \frac{2}{N_{cr}}$$

Where Ncr is the number of carriers, n is the number of voltage levels, and $A_{cr(Peak\text{-}Peak)}$.is peak to peak amplitude of each carrier. To illustrate, Figure 1.21 shows four carriers with $A_{cr(Peak\text{-}Peak)}$. equal to 0.5 to generate five-level waveforms.

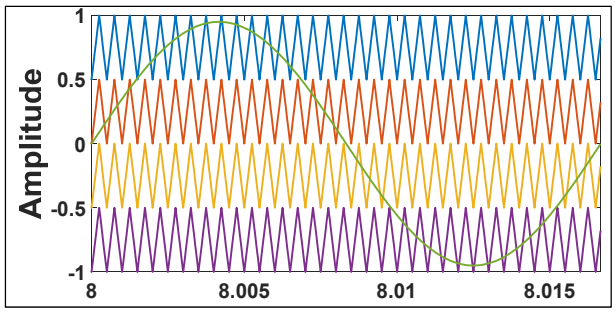

Figure 1.21 Carriers and modulating signals in LS-PWM

1.5.2 Phase shift modulation (PS-PWM)

PS-PWM for multilevel inverters with *m* voltage levels requires *m-1* carriers. It is due to the fact that modulation of each carrier makes one voltage level in the multilevel inverter structure. These *m* carriers should be placed by phase displacement (Δ∅) between any two adjacent carriers that can be computed and given in equation (1.5) (B. Wu, 2006).

$$\Delta\varphi = \frac{2\pi}{m-1} \tag{1.5}$$

Figure 1.21 shows four triangular carriers cover the reference signal to modulate and produce required pulses for the 5L inverter. Therefore, they would have π/2 phase shift. Modulation index in PS-PWM technique is given by equation (1.6) [31].

$$m_a = \frac{|V_{ref}|}{|Cr_i|} \tag{1.6}$$

Where Cri (i=1, 2, 3, 4) are the amplitude of carrier waveforms and V_{ref} is the magnitude of the modulation signal. The phase shift modulation technique is a profitable method to shift the harmonic orders to further frequency. It leads to reduce the size of the external filters or even removing them depend on the switching frequency. The total switching frequency of the converter which is modulated by PS-PWM is given by:

$$f_{sw-inverter} = (m-1) f_{cr} \tag{1.7}$$

Where $f_{sw\text{-}inverter}$ is the total converter switching frequency, m is the voltage level and fcr is the carrier frequency.

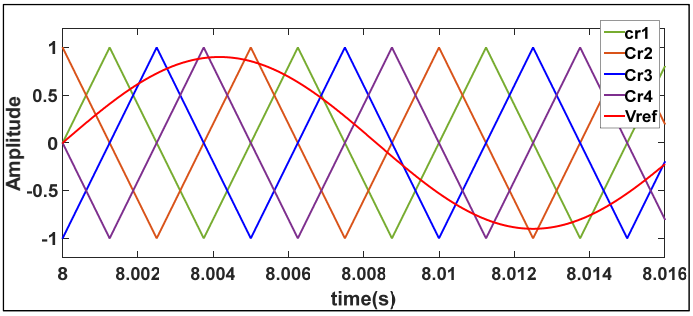

Figure 1.22 Phase shift PWM carrier wave forms

The main reason to shift the harmonic components in PS-PWM is that the switching frequency of the inverter is multiple of the carrier frequency. However, at level shift modulation, the inverter frequency is equal to the carrier frequency. The experimental results on the PUC5 inverter with 300 Hz carrier frequency are shown in figure 1.23 in which the 20th harmonic order sidebands are the first dominant harmonics group. This result demonstrates that the first dominant harmonics are the sideband of 1200 Hz that is 4 times the carrier frequency. Furthermore, it is extracted from figure 1.23.c, that the number of switching pulses in switches S1, S2, and S3 are 1, 10, and 10 respectively which shows the 1200Hz total inverter switching frequency.

Figure 1.24 illustrates the simulation results of LS-PWM with 1200Hz and PS-PWM with 300Hz carrier frequency on the PUC5 inverter. In fact, for a given switching frequency of the converter, the carrier frequency in PS-PWM can be selected in 1/m of LS-PWM.

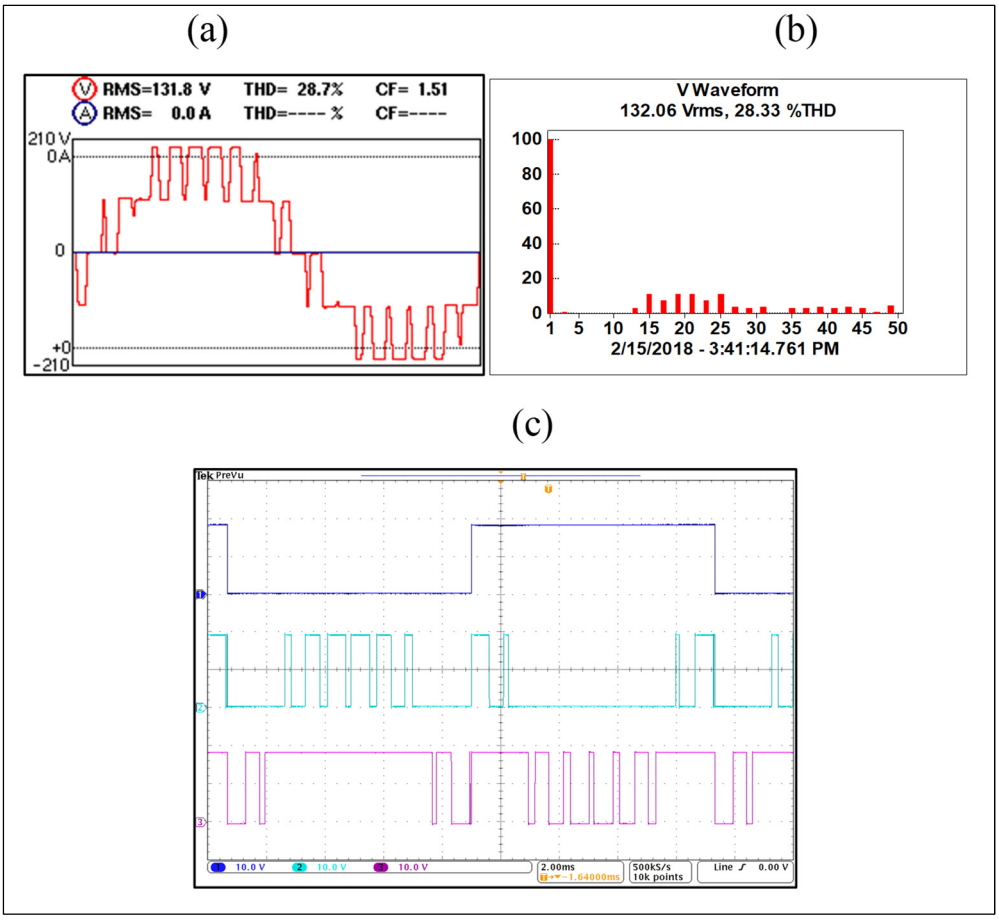

Figure 1.23 Implementation of proposed PS-PWM on PUC5 inverter
a) Output voltage b) Voltage THD c) Switching patterns

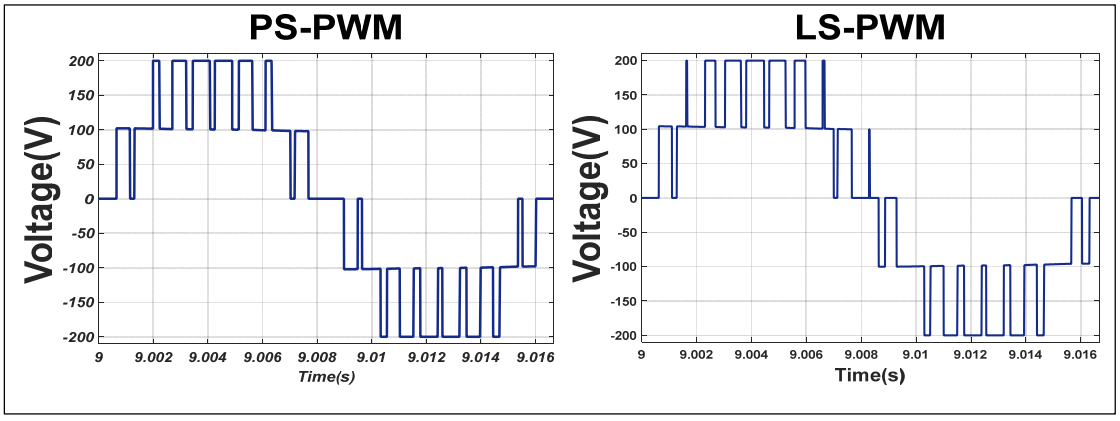

Figure 1.24 Waveforms of PS-PWM with 300Hz and LS-PWM with 1200Hz carrier frequency

1.5.2.1 Proposed general phase-shift for all types of MLCs

The conventional PS-PWM is not applicable on the NPC multilevel converter and some MLCs with similar structures (McGrath & Holmes, 2000; Solas et al., 2013a; Bin Wu & Narimani, 2017a). Thus, one method has been proposed in (S. Arazm et al., 2018a; S. Arazm, H. Vahedi, & K. Al-Haddad, 2018b) to address this problem which can be used for all MLCs and MMCs which is illustrated in figure 1.25. This flowchart implies that for generating a 2n+1 voltage level, parameter i is started from 1 to n (i= 1, 2, …, n) and the required carriers include: Cr1, Cr2, Cr3, ……, Crn, Crn+1, Crn+2, Crn+3, ……,Cr2n so that the carriers Cri and Crn+i are in the opposite phase (S. Arazm et al., 2018a).

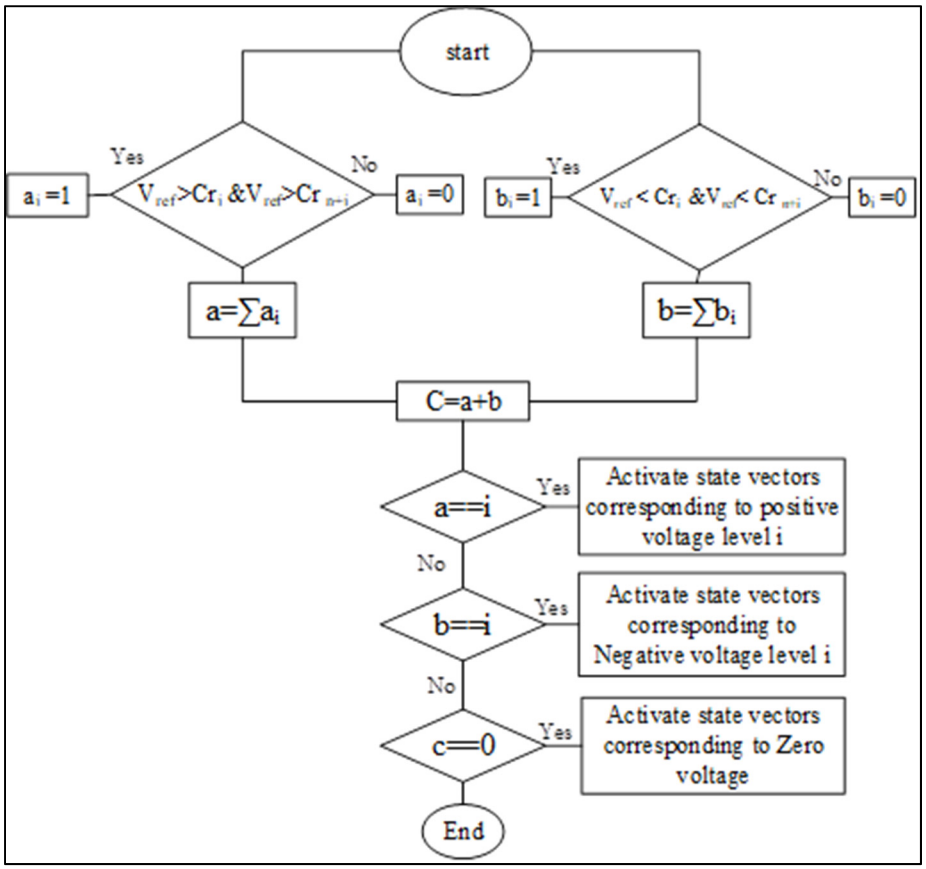

Figure 1.25 Generalized PS-PWM flowchart
Taken from S. Arazm et al. (2018)

1.5.3 Space Vector Modulation Method (SVM)

1.5.3.1 Three-phase space vector

SVM is a modulation technique that uses the vector concept to generate pulses for switches. In this technique, the voltage vectors are calculated in each set of switching states. Then, the magnitude and phase of the reference voltage vector will be determined instantaneously. By considering the reference voltage vector location, a combination of nearest voltage vectors will be chosen and the corresponding switches to generate these voltage vectors will be fired for specified intervals. These time intervals are calculated based on reference voltage vector information. Figure 1.26 shows the basic concept of the space vectors for the three-phase two-level inverter. Modulation index in SVM is obtained by the following equation:

$$m_a = \frac{\sqrt{3}V_{ref}}{V_d} \tag{1.8}$$

Where Vd id the DC voltage and Vref is the reference voltage.

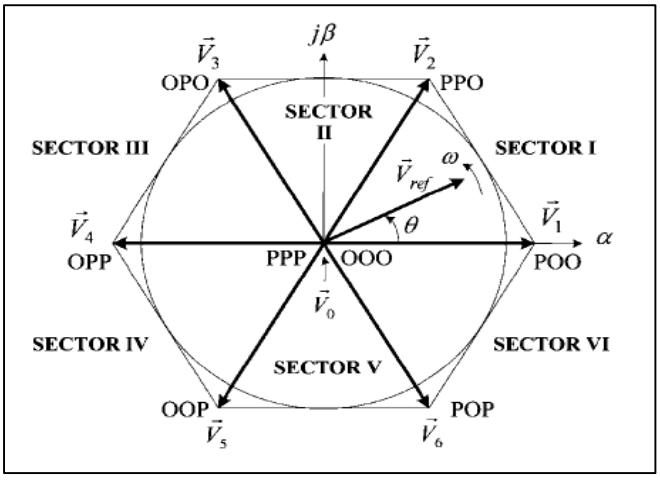

Figure 1.26 Vectors to produce switching states
Taken from Bin Wu & Narimani (2017)

1.5.3.2 Single-phase SVM for MLCs

Although the proposed SVM technique is designed in one dimension for single-phase, It can be applied for three-phase system through three reference voltages (S. Arazm, 2018).

Voltage levels on single-phase multi-level converters and their accompanying state vectors should be sectionalized by the number of areas defined by the following equation (S. Arazm et al., 2018c):

$$N_R = m - 1 \tag{1.9}$$

Where N_R is the number of regions and m is the output voltage level. Reference voltage in terms of dwell time and state vector is given by:(S. Arazm et al., 2018c).

$$\begin{aligned} V_{ref} T_S &= V_1 T_1 + V_2 T_2 + ... + V_n T_n \\ T_S &= T_1 + T_2 + ... + T_n \end{aligned} \tag{1.10}$$

Where V_{ref} is a reference voltage, V_n is the state vectors, which determine the region voltage levels, T_s is the period at the switching frequency and T_n is the state vectors corresponding to dwell time. Moreover, the modulation index that is given by (S. Arazm et al., 2018c):

$$m_a = \frac{V_{ref}}{V_{DC}} \tag{1.11}$$

Where V_{DC}, is the inverter DC source voltage. Generally, minimum modulation index in MLCs through the proposed SVM method with N_R region is obtained by (S. Arazm et al., 2018c):

$$m_{a-\min} = \frac{m-3}{N_R} \tag{1.12}$$

If m_a is less than $m_{a\text{-}min}$, the inverter's output voltage may be one or more levels below the target voltage level. For example, if a nine-level voltage is created at the inverter's output, eight regions must be examined in order to allocate nine state vectors and the minimum modulation

index for nine voltage levels is 0.75. The following equation can be used to demonstrate the relationship between generated voltage levels and modulation index. (S. Arazm et al., 2018c).

$$m_{ak} = \frac{m - 3 - 2k}{N_R} \tag{1.13}$$

In fact (m-2k) waveform level is produced where k is varied from 0 to (m-5)/2 and m_{ak} is the minimum. For example, four regions are chosen for the examination of state vectors of the PUC5 inverter according to equation (1.9). Figure 1.27 depicts the state vectors and four areas for the PUC5 inverter, which represent five voltage levels.

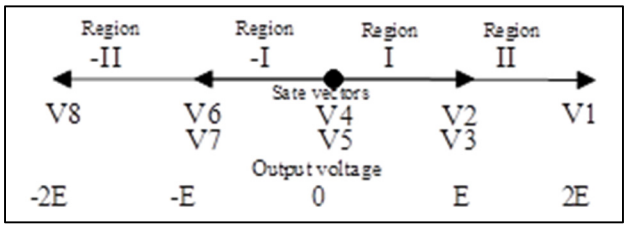

Figure 1.27 State vector diagram for five voltage levels at the output of PUC5
Taken from S. Arazm et al. (2018)

Complete analysis of SVM on single-phase PUC5 is discussed in (S. Arazm et al., 2018c).

1.6 Industrial application

Although a large number of multilevel converters have been introduced and proposed in recent years in the research area, only a few of them including CHB and NPC are employed in the industry. Moreover, among the proposed MMCs submodules, HB-MMCs, are the most popular for industrial application. However, the route is gradually paved for entering the new generation of MLCs in industries. Their application is a motor drive, battery charger, power converters for wind farms and solar plants, etc. Figure 1.28 shows the schematic diagram and section of one motor drive in which the input configuration is 24 pulse diode rectifier, and the output configuration is 3L NPC. This driver that is manufactured by ABB has the following

specification: output voltage: 4.16 kV, Output frequency: 0 to 82.5 Hz, and output power:5 MW (Hitachi-ABB, 2009).

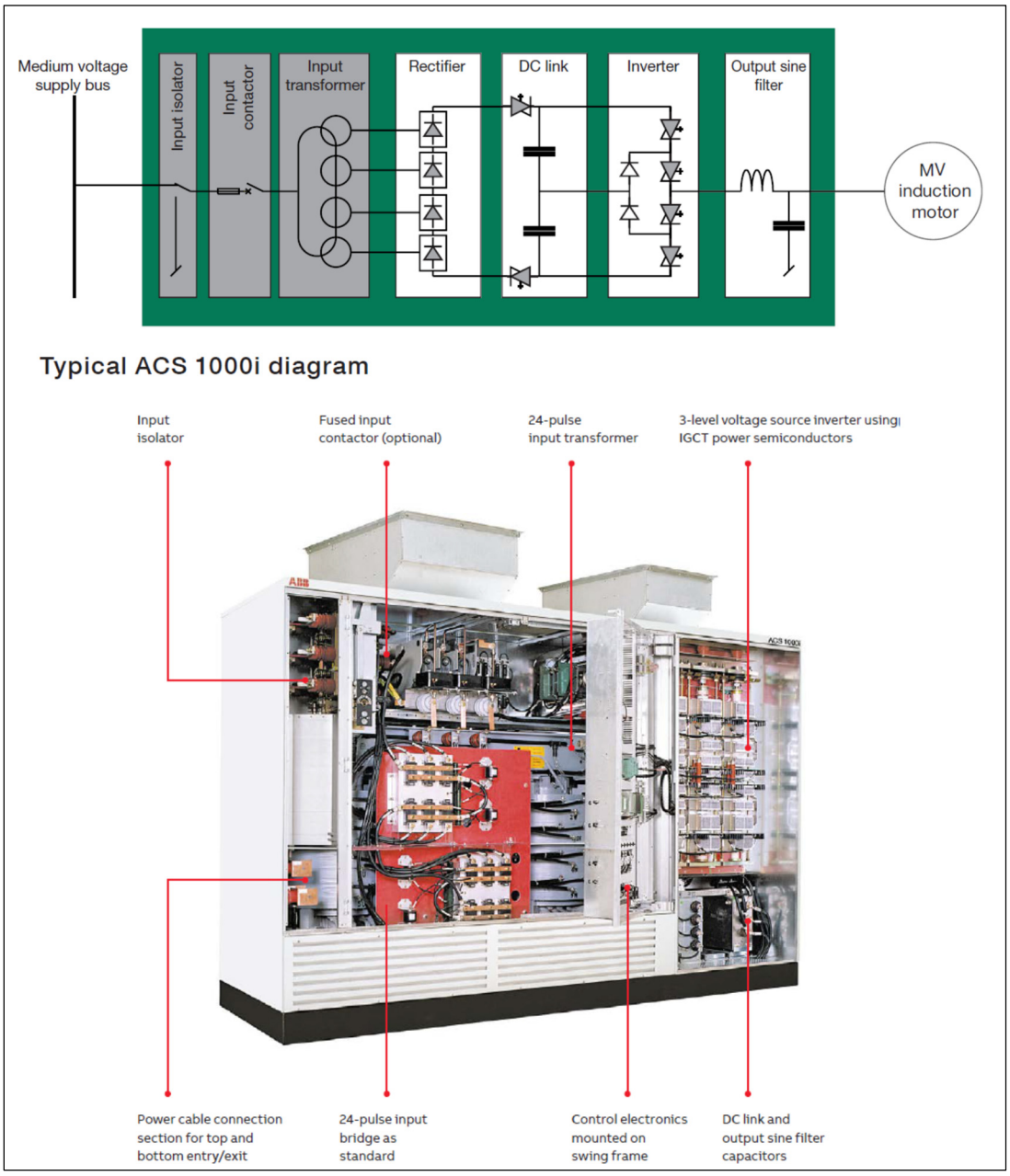

Figure 1.28 3L NPC employed in motor drive 4.16 kV, 5MW
Taken from Hitachi-ABB (2009)

Siemens is the pioneer of MMC technology. Two types of HB-MMCs and FB-MMCs are manufactured, designed, and constructed by this company all around the world. FB-MMC with the capability of clearing the DC fault current in immediate time is usually proposed for overhead lines with long distances. On the other hand, HB-MMCs are mostly used for an offshore wind park, link between two grids, and, etc. Figure 1.29 shows two schematic diagrams of HVDC application and Figure 1.30 depicts an accomplished 2×1000 MW project for linking the grid between Spain and France through HB-MMC (Siemens, 2016).

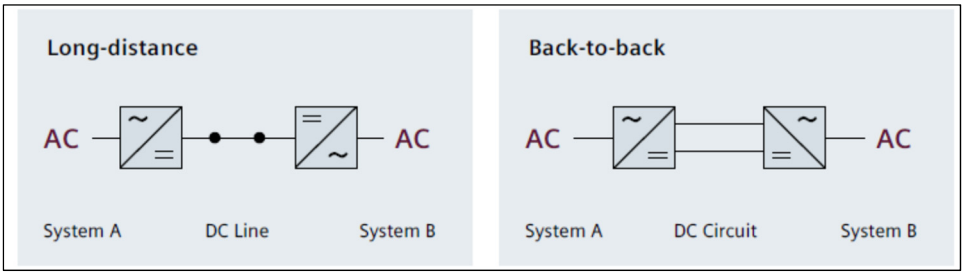

Figure 1.29 Diagram of HVDC applications
Taken from Siemens (2016)

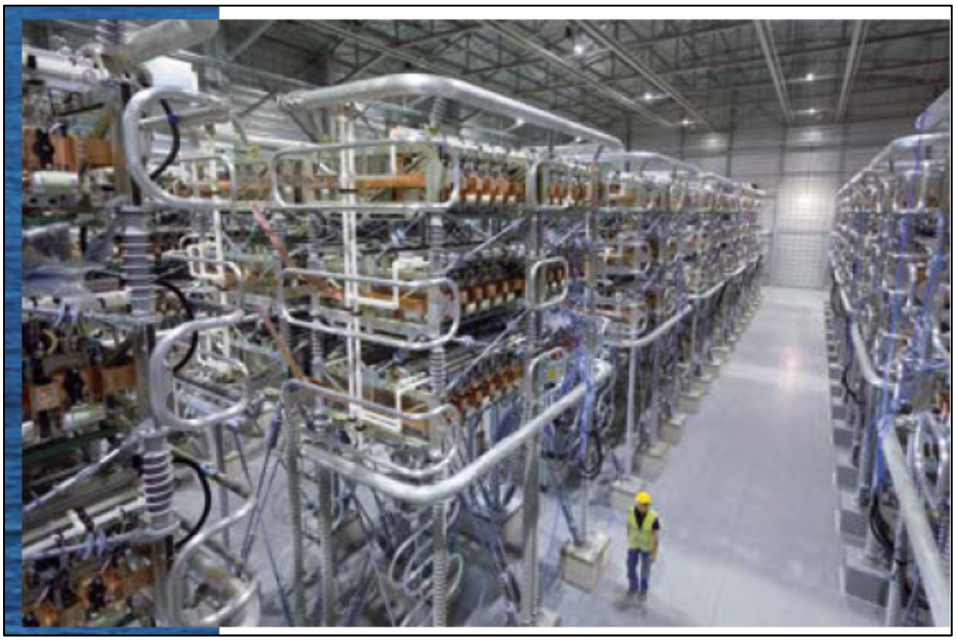

Figure 1.30 Half-Bridge MMC project for linking between two grids
Taken from Siemens (2016)

In addition, Figure 1.31 illustrates one submodule of half-bridge based on the cutting edge IGBT technology with 2 kA DC current and 6.5 kV rated voltage. This high-power density HB technology leads to the use of a smaller number of submodules (Siemens, 2016).

Figure 1.31 One HB cutting edge submodule with 2 kA current and 6.5 kV rated voltage Taken from Siemens (2016)

Furthermore, Hitachi-ABB manufactures a wide range of multilevel converters which is called PCS6000, including NPC, CHB, and MMCs for STATCOM, static var compensator (SVC), medium voltage and high-power wind turbine full power converter up to 9 MW, frequency converters, and so forth (Hitachi-ABB, 2020).

PUC converter belongs to the new generation of MLCs which has already been commercialized by Ossiaco as a 7-kW electrical vehicle charger and 15 kW solar inverter. Since two switches in the PUC converter operate in power system frequency, their efficiency is 97.8% and due to generate 5 level waveforms, their THD is less than 3%. Figure 1.32 depicts a 7 kW module of PUC5 (Ossiaco, 2020).

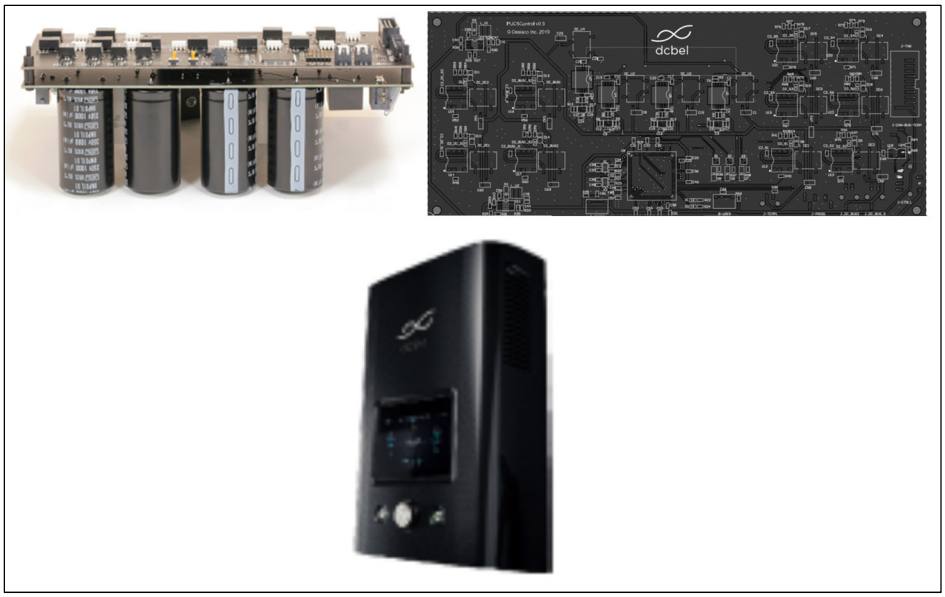

Figure 1.32 Layout and section of PUC5
Taken from Ossiaco (2020)

1.7 Conclusion

This chapter has reviewed the state of the art of multilevel converters and modular multilevel converters along with the modulation strategies to trigger the switching devices. The maturity level from the two-level conventional converter to hybrid and modular multilevel converters has been briefly discussed in this chapter. Although the conventional converters are simple to manufacture due to their lower devices and straightforward control system, they require large passive filters which increase the size and cost of the converter. Multilevel converters are invented to reduce the size of the filters and to address the voltage stress on switching devices. Increased voltage levels waveform with reduced components counts are still a matter of controversy in multilevel converters. Single DC source converters are another vital issue in multilevel converters due that isolated DC sources increases the size and cost of the converter because of phase-shift transformer and rectifier. Simplification in switching algorithm through an appropriate modulation strategy as well as the uncomplicated voltage balancing techniques are also the key factors to select among the multilevel converters for industrial applications. Modular multilevel converters are the modular fault tolerant single DC source types of

multilevel converters which use the flying capacitors instead of isolated DC sources. However, a large number of switching devices and the size of the flying capacitors are challenging issues. The development of multilevel converters is progressing due to the evolution of the standards and novel technologies; however, attracting the industries to accept the topologies and control methods is still highly competitive.

CHAPTER 2

ZPUC: A NEW CONFIGURATION OF SINGLE DC SOURCE FOR MODULAR MULTILEVEL CONVERTER (MMC) APPLICATIONS

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2.1 Abstract

Z packed U-cell (ZPUC) converter topology is presented in this chapter as a new type of multilevel converter topology that can be operated in a single phase as well as in three-phase configurations while using a single DC source. Since each U-cell includes two switches and one capacitor, in this topology, three U-cells are needed to generate 5 or 7 voltage levels. Moreover, the configuration proposed for the ZPUC is more appropriate for high-power application modular multilevel converters (MMCs) to increase the voltage levels compared to other topologies. Accurate voltage balancing on small-sized auxiliary capacitors is due to integrated modulation strategy without using additional controllers; additionally, the reduction of total harmonic distortion (THD) in AC currents for higher voltage levels is an advantage of this configuration. A full topology sequence of operation and performance analysis of ZPUC based on the 5-L inverter is investigated in Matlab-Simulink and experimentally validated on a 3 kVA prototype. The obtained results illustrate the good dynamic performance of the proposed topology and the implemented integrated switching pattern voltage balancing.

Keywords

ZPUC topology, modular multilevel converter (MMC), ZPUC-MMC active voltage balancing, power quality, reliability.

2.2 Introduction

Multilevel converter topologies have become more popular and are progressively replacing two-level converters due to their high impacted advantages on reducing the size of harmonic filters, increased nominal power capability and component voltage stress reduction (Kouro et al., 2010). Cascaded full bridge, flying Capacitor (FC), neutral point clamped (NPC) and active neutral point clamped (ANPC) are the popular and classic topologies of multilevel converters that have been commercialized in recent years, replacing conventional converters in several industrial applications (Cortés, Wilson, Kouro, Rodriguez, & Abu-Rub, 2010; Ebrahimi & Karshenas, 2017; J. Li, Huang, Liang, & Bhattacharya, 2012; J. Rodriguez, Bernet, Steimer, & Lizama, 2010).

Multilevel converters have recently been used in medium-voltage and high-voltage applications, such as medium-voltage drives, the connection of solar and wind turbine plants to the main grid, and high-voltage direct current (HVDC) and flexible AC transmission systems (FACTS) (Jiangchao Qin & Saeedifard, 2013; Sleiman, Al-Haddad, Blanchette, & Kanaan, 2018).

Multilevel converters present many challenges related to isolated DC sources (Hinago & Koizumi, 2010), topology complexity (Lezana & Aceiton, 2011), modulation techniques (J. Rodriguez et al., 2009), modeling and control (J. Qin & Saeedifard, 2012), as well as the voltage balancing challenge (S. Song et al., 2020) of flying capacitors that have persuaded researchers and industries to improve and enhance their performance.

Modular multilevel converters (MMCs) have become attractive to industries in recent years for their modularity, which is vital for repair and maintenance due to simple exchange of the affected modules by new ones. Other advantages that have contributed to MMCs' growing popularity include voltage scalability, lower total harmonic distortion (THD), higher quality of output voltage and current waveforms, fault tolerance, and redundancy (Ahmadijokani et al., 2020; Marcelo A Perez, Bernet, Rodriguez, Kouro, & Lizana, 2015). Reducing the power

losses in semiconductor switches and the sizes of filters are the other useful features of MMCs (Dong, Yang, Li, & He, 2019; Makhamreh, Sleiman, Kükrer, & Al-Haddad, 2019).

With regard to the impacts of the increased number of devices, assembling complexity, heat dissipation of losses, and total cost of the multilevel converters and MMCs, the tendency nowadays is to develop multilevel converter topologies with reduced numbers of power devices while generating more voltage levels.

Multilevel submodules such as 3-L NPC, 5-L FC, 3-L full bridge, 5-L cross-connected cells and 3-L FC are the blocks that can be replaced by 2-L usual half bridge on MMCs to counteract its negative effects (Apparao Dekka, Wu, Fuentes, Perez, & Zargari, 2017; Nami, Liang, Dijkhuizen, & Demetriades, 2015). However, to have an optimized topology of MMCs, considering their application as well as the standard requirements, would be necessary in order to trade off between the complexity of cells and power losses. In addition, higher output voltage levels accompanied by proper modulation techniques make the harmonic filters smaller due to the reduced THD of the output wave (Abarzadeh, Vahedi, & Al-Haddad, 2019; S. Arazm et al., 2018a).

Recently several new topologies of multilevel converters were proposed based on hybrid FC, NPC and CHB topologies with the aim of increasing the voltage levels and reducing the component counts. A reduced component count five level converter was presented in (Karthik & Loganathan, 2020). However, it uses the common FC topology for three-phase which has an impact on system reliability when used in three-phase configuration and in case of one phase failure. The authors proposed 5-L topologies in (Majumder et al., 2020) for open end induction motor (OEIM) applications with the aim of increasing the reliability and fault tolerance. Although this topology, solve the reliability problem, its application is limited for OEIM. In (J. Chen & Wang, 2020) a single-phase Seven-Level Inverter for reduced components count was proposed; however, the latter requires three isolated DC sources for three-phase system. In (G. Chen, Bahrami, & Narimani, 2020) authors present a new seven level topology in which single DC source has been replaced by an isolated DC source. A new approach to voltage level

multiplication has been introduced that permits the multiplication of the number of output voltages while operating at different frequencies to enhance converter efficiency (Abarzadeh & Al-Haddad, 2019).

Packed U-cell (PUC) topology is one of the recently introduced topologies of multilevel converters that highly reduces the component count (Kamal Al-Haddad, Ounejjar, & Gregoire, 2016). This converter generates seven voltage levels through six switches three of which operate complementarily. Thus, there is no redundancy, which requires the complicated control system to balance the auxiliary capacitor (Ounejjar, Al-Haddad, & Gregoire, 2011). The authors in (Vahedi, Labbé, & Al-Haddad, 2016) utilized the redundancy in PUC and achieved five voltage levels at the output wave while the FC was controlled without sensors and only by a modulation technique. In (S. Arazm et al., 2018b, 2018c) modulation techniques were presented to control PUC5 without any sensors as well. Moreover, authors in (S. Arazm, Vahedi, et al., 2019) present nine levels waveform through an additional U-cell that is called PUC9 and voltage balancing method to balance two FCs. More recently, several papers have been published for modification of PUC converter. In (Niu et al., 2020), a nine level T-type PUC is presented which generate nine levels at the output of inverter; however, it uses two DC source for single-phase converter. Authors present an improved PUC topology as a boost converter which makes the output AC voltage peak of inverter up to one and half times of input voltage (Sathik, Bhatnagar, Sandeep, & Blaabjerg, 2020). However, this topology uses three additional switching devices compared to traditional PUC converter.

It is worth noting that all the literatures which has already been published regarding PUC converters, require isolated DC sources in a three-phase system which is their main drawback. To cope with this challenge of isolated bidirectional power flow DC sources, a new topology is presented in this chapter called Z packed U-cell (ZPUC).

The number of switches in this topology is the same as in PUC; however, one more capacitor has to be added in order to replace the bidirectional DC source in standard PUC.

ZPUC topology can be extended through additional U-cells, and the output voltage levels would be increased to two times minus one for redundant states and two-times plus one for non-redundant states in terms of adding one U-cell. The simplest module of ZPUC includes three U-cells which generates five levels with redundant switching states that are easily controlled and seven levels with an added complex control system. ZPUC can generate 9-L for redundant switching states and 15-L for non-redundant switching states, just by adding one more U-cell. The number of devices in ZPUC topology is very low in comparison with the other topologies such as FC and NPC. It should be noted that one of the major advantages of this new topology is that it requires only a single DC source for all systems configuration such as single-phase, three-phase, and multiphase connections as well. The voltage levels generated by proposed topology are unipolar that are instrumental to operate as a single DC source to generate higher voltage levels compared to a bipolar one such as PUC converter.

In this chapter the new topology of ZPUC and the switching states for single-phase and three-phase system is discussed in section 2.3. As well, voltage balancing algorithm integrated with modulation technique and reliability is discussed in this section for one sub-module of ZPUC. The application of ZPUC5 on MMCs are discussed in section 2.4. Finally, Simulations and experimental results are shown in section 2.5 and 2.6 for stand-alone and grid-connected aimed to validate the performance of ZPUC single phase and three phases which implement voltage balancing technique.

2.3 ZPUC topology and switching states

The simplest model of ZPUC topology that has been shown in figure 2.1.a has six switches same as PUC5 in which three devices works complimentarily. Thus, there are eight states for this topology that generate 5-L waveform with regard to necessary redundancy to balance the voltage in the flying capacitors or 7-L with complex control system. Additional flying capacitor can be added to make this topology appropriate for generating more voltage levels especially in a three-phase system with a single DC source. In fact, an additional capacitor in ZPUC5 compared to PUC5 makes the output waveform unipolar at E step from 0 to 4E instead

of -2E to +2E in PUC converter. Generation of unipolar waveform at the output of ZPUC topology makes this topology suitable to generate more voltage levels in MMC configuration in comparison with the PUC topology. Figure 2.1.b shows that one U-cell and one FC has been added to simplest ZPUC which output voltage levels are increased by two-times minus one for redundant states (9-Level) and two-times plus one (15-L) for non-redundant states. Figure.1.c shows the general topology of ZPUC. The relation between the U-cells and voltage levels is given by equations 2.1 and 2.2.

$$M = 2^{n-1} + 1 \tag{2.1}$$

$$M = 2^{n} - 1 \tag{2.2}$$

Where *n* is the number of U-cells, and M is the voltage levels. Equation 2.1 and 2.2 are relevant for redundant switching states and nonredundant switching states, respectively.

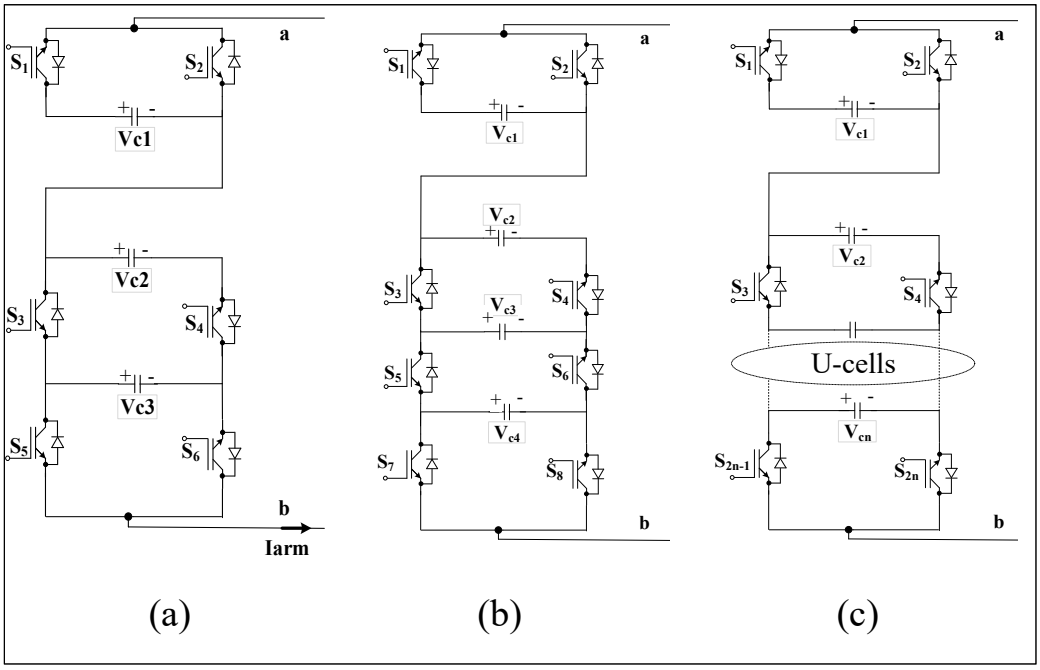

Figure 2.1 ZPUC topology (a) Simplest ZPUC converter topology with three capacitors and 6 switches that can generate 5-L or 7-L waveform (b) ZPUC9 or ZPUC15 topology (c) General model of ZPUC

2.3.1 Switching States of ZPUC5

There are six active switches in simplest ZPUC inverter which switches S_1, S_3 and S_5 operate in complimentary way with S_2, S_4 and S_6 respectively. Eight switching states in this topology generate 5 voltage levels at the output with sufficient redundancy to balance the voltage in flying capacitors. This topology uses the redundant states to balance the voltages without complicated control system and only through modulation strategy. Equation 2.3 and 2.4 show the relation between the states and the output voltage levels. Equation 2.3 is related to the simplest ZPUC that could generate 5-L or 7-L depend on the relation of V_{C1}, V_{C2}, and V_{C3}. Furthermore, equation 2.4 is applied for general type of ZPUC proposed topology.

$$V_{ab} = S_1 V_{c1} + (1 - S_3)V_{c2} + (S_3 - S_5)V_{c3} \tag{2.3}$$

$$V_{ab} = S_1 V_{c1} + (1 - S_3)V_{c2} + (S_3 - S_5)V_{c3} + \ldots\ldots\ldots (S_{2n-3} - S_{2n-1})\, V_{cn} \tag{2.4}$$

Where V_{ab} is the output voltage across nodes ab in figure 2.1, V_{c1}, V_{c2}, V_{c3}, and V_{cn} are the flying capacitor voltages in C_1, C_2, C_3 and C_n respectively and S_1, S_3, S_5 and S_{2n-1} are the switching devices that would be 1 when the switches are turned on and would be 0 when they are turned off. Simplest ZPUC switching states is listed in the table 2.1 according to equation 2.3 and their corresponding topologies are depicted in figure 2.2.

In order to generate 5-L voltage across ab node (V_{ab}), voltages in capacitors 1 and 2 (V_{c1} and V_{c2}) should be regulated in 2E and voltage in capacitor 3 (V_{c3}) must be regulated in E which is illustrated in equation 2.5. Accordingly, to generate 7-L waveform across the ab node the voltages should be set as the equation 2.6.

$$V_{C1} = V_{C2} = 2E, V_{C3} = E \tag{2.5}$$

$$V_{C1} = V_{C2} = 3E, V_{C3} = E \tag{2.6}$$

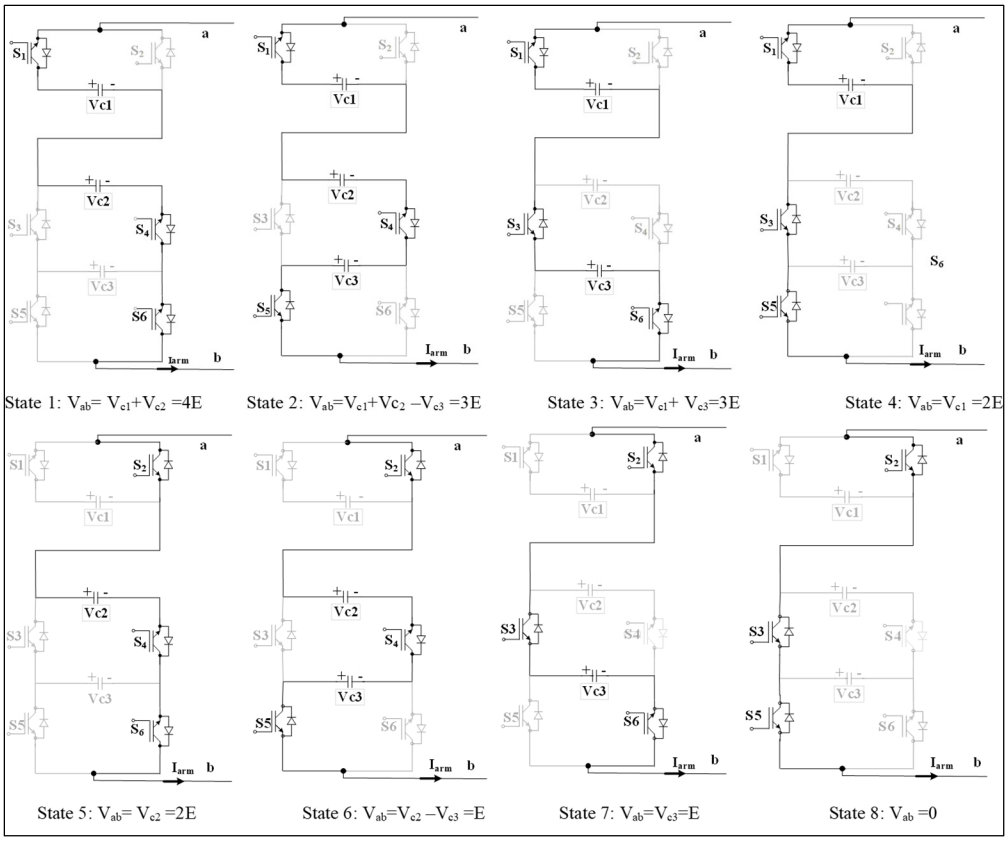

Figure 2.2 Switching states of ZPUC inverter in standalone mode

Table 2.1 Switching States of ZPUC Converter to Generate Five and Seven Level Waveforms

State	S1	S3	S5	Vab	Vab-5L	Vab-7L
1	1	0	0	Vc1+Vc2	4E	6E
2	1	0	1	Vc1+Vc2 –Vc3	3E	5E
3	1	1	0	Vc1+ Vc3	3E	4E
4	1	1	1	Vc1	2E	3E
5	0	0	0	Vc2	2E	3E
6	0	0	1	Vc2 –Vc3	E	2E
7	0	1	0	Vc3	E	E
8	0	1	1	0	0	0

In figure 2.3 the inverter model of ZPUC topology is depicted which could be operated as a single DC source single-phase or three-phase multilevel inverter. As well, additional modules could be easily added in series connection which is suitable for MMC applications. In next section the performance of ZPUC for MMC is discussed.

This configuration is suitable for industrial applications such as motor drives, renewable energy connection to the grid, HVDC etc. Voltage waveform across the load in figure 2.3 includes 9-L for phase voltage and 17-L for line voltage.

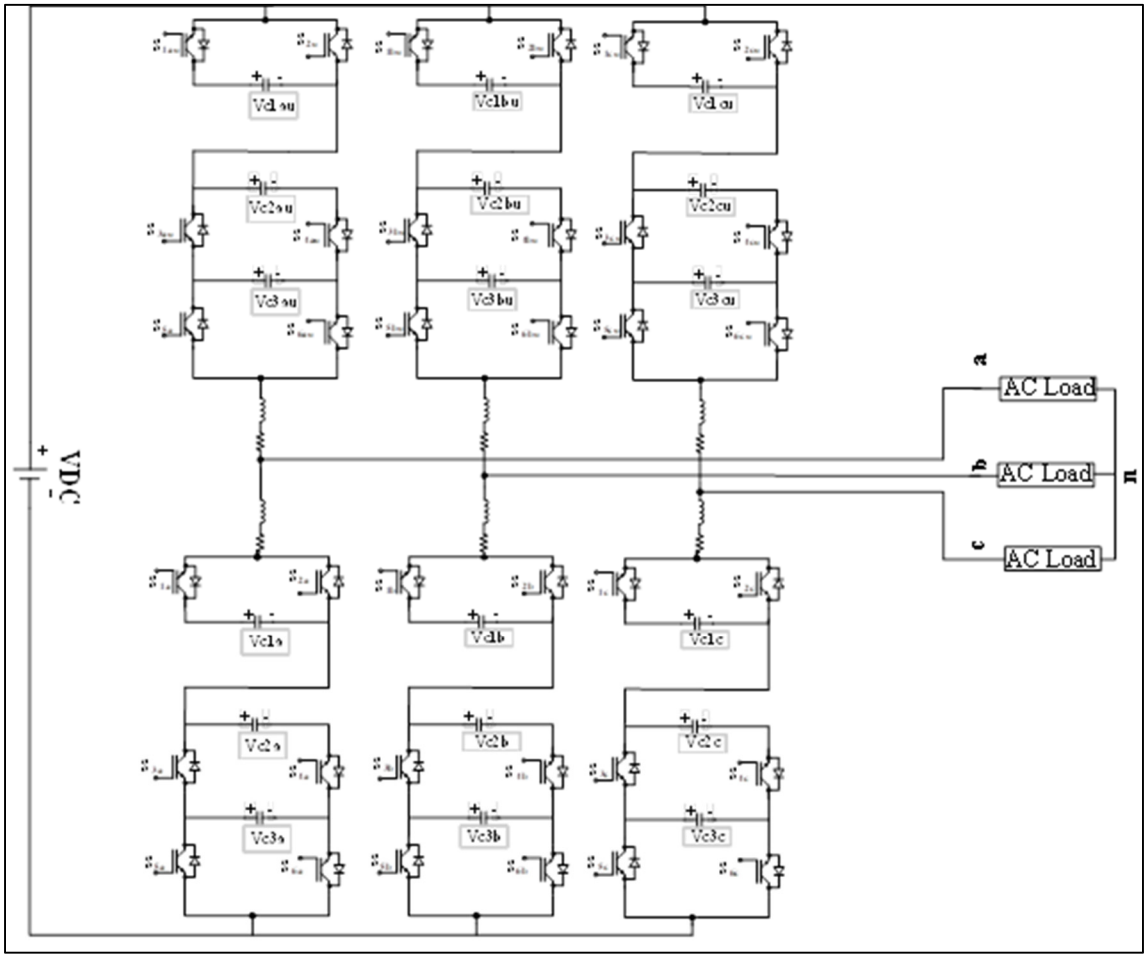

Figure 2.3 Three phase ZPUC converter topology which generates 9-L single phase waveform and 17-L line-voltage waveform

ZPUC converter topology has been devised so that it could be placed in all applications of converters such as active rectifier and multilevel inverter and is much suitable for application on modular multilevel rectifier and inverters as well as the excellent candidate to replace the half bridge or full bridge used till now as a unique cell for MMC application.

As well, capability of this converter to balance the flying capacitor voltages integrated with modulation technique and without using the external control system in desired values with minimum ripples and offset would be interesting for industries. This topology requires the single DC source for three-phase system in contrast with the other competitive topology such as the PUC. The value of this topology is the reduced counts of power devices than the other equivalent topologies such as NPC, FC, and CHB to generate equal voltage levels at the output (S. Arazm et al., 2018a; Bin & Mehdi, 2017; J. Rodriguez, Jih-Sheng, & Fang Zheng, 2002).

Table 2.2 shows the comparison among the number of devices in several popular type of inverters in three-phase systems to generate 9-L phase-waveform and 17-L line waveform. This table illustrates that the number of switching devices in ZPUC is less than the other types of converters and is equal to the PUC5. However, the number of isolated DC sources in ZPUC5 is $1/6^{th}$ of PUC5 that could be a suitable alternative for PUC5 in three-phase systems due to the considerable cost and bulkiness reduction of DC supply system and complexity. It is noteworthy that, ZPUC topology is not only suitable converter for three-phase system due to single-DC source requirements, but also for single-phase application compared to other PUC family of converters. For instance, single-phase traditional PUC5 converter requires two isolated DC sources and 12 switches and two FCs to generate 9-L waveform in contrast to the single DC source, 12 switches, and 6 FCs for ZPUC converter. Although ZPUC5 requires 4 more FCs, the cost of isolated DC sources is still an issue. PUC9 is the converter that uses three DC sources with lower number of switching devices; however, this topology is not as modular as ZPUC and it could not be suitable for higher levels waveforms in three phase applications.

In addition, a general ZPUC topology that can be replaced in all Poles as to increase the voltage levels known as the general topology as depicted in figure 1.c.

Table 2.2 Components Counts of Three-Phase Inverters to Generate 9-L Phase Voltage Wave

Inverter Type	DC Source	Capacitor	Clamped Diode	Active Switch	Total components
CHB	12	0	0	48	60
NPC	1	8	42	48	99
FC	1	21	0	48	60
PUC5	6	6	0	36	48
PUC9	3	6	0	24	33
ZPUC5	1	18	0	36	55

The number of U-cells determine the required total amount of output voltage levels depend on the application. However, to generate more voltage levels; more complex and challenging control and modulation technique and hardware implementation can be expected. To overcome this problem, the authors suggest using the simplest ZPUC5 in modular way which not only, divide the voltages among capacitors and reduce the rating size of elements, but also, would have the other advantages of MMCs.

For designing power converters, dividing the currents between modules is an advantageous way to choose lower current rating switching devices and consequently lower conduction power losses. This benefit is achieved by the configuration of the figure 2.3, while the voltage levels have been duplicated compared to the other competitive topologies.

2.3.2 Voltage Balancing Method on Single Module of ZPUC5

The theory of voltage balancing in this chapter is based on energy storage in each capacitor. With the assumption that the capacitance of FCs is similar, measured FCs voltages should be compared with one another in the voltage balancing algorithm as a first step. Modulation strategy must be implemented on the converter to generate the appropriate gate signals.

Redundant switching states which have been shown in figure 2.2, facilitate to balance the voltage between the involved FCs in each voltage level. If the current flows from the positive polarity of capacitors, it means that the capacitor is being charged and vice versa. Hence, charge and discharge of the FCs depend on the arm current direction and this situation is altered through current direction variation reciprocally. Generally, the FCs with the greater voltage values are selected to be discharged between the redundant states in each voltage level. Situations of charge and discharge of the FCs in terms of current direction (I_{arm}) are listed in table 2.3. It should be explained that - sign in the table 2.3 demonstrates that the corresponding capacitors are neither charged nor discharged. In other words, they have no effect in the circuit. In addition, abbreviations of CH and DC imply charge and discharge of FCs.

Table 2.3 Situations of Charging and Discharging of Flying Capacitors at Corresponding States

State	**$I_{arm}>0$**			**$I_{arm}<0$**		
	C1	**C2**	**C3**	**C1**	**C2**	**C3**
1	CH	CH	-	DC	DC	-
2	CH	CH	DC	DC	DC	CH
3	CH	-	CH	DC		DC
4	CH	-	-	DC		-
5	-	CH	-	-	DC	-
6	-	CH	DC	-	DC	CH
7	-	-	CH	-	-	DC
8	-	-	-	-	-	-

For instance, states 6 and 7 are redundant states which generate voltage level of E at the output of ZPUC module in which capacitors C_2 and C3 are charged and discharged respectively in state 6, and C_3 is discharged in state 7 when the arm current is positive as shown in figure.2.2. Thus, state 6 must be selected in voltage balancing algorithm to generate E voltage level in positive arm current when measured voltage value of C_3 is greater than C_2. Inversely, state 7 should be selected between states 6 and 7 when the voltage of C_3 is lower than C_2 at the same

arm current direction. Charge and discharge of FCs are reversed when the arm current direction (I_{arm}) is inversed. The voltage balancing algorithm for one module of ZPUC converter is listed in table 2.4 according to above-mentioned explanation.

Phase shift modulation technique introduced in (S. Arazm et al., 2018a) is utilized in this chapter. Four carriers and one reference voltage for one module of ZPUC is shown in figure 2.4 and the voltage balancing control method integrated with PS-PWM technique is illustrated in flowchart of figure 2.5. Corresponding states of voltage levels are selected based on comparison between carrier waves and reference voltage. Only the modulation conditions based on the flowchart of figure 2.5 should be investigated to generate voltages of 0 and 4E. Whereas, to generate the other voltage levels including 3E, 2E and E the conditions of modulation of figure 2.5 and conditions of voltage balancing of the table 2.4 should be examined simultaneously.

2.3.3 Reliability of One Module of ZPUC Topology

In this section, the reliability of single-phase ZPUC topology is briefly discussed based on the

Table 2.4 Voltage balancing Algorithm for ZPUC of figure 2.2

Condition	**$I_{arm}>0$**	**$I_{arm}<0$**	**Voltage level from modulation strategy**
No condition	State1	State1	4E
Vc3>0.5Vc2	State2	State3	3E
Vc3<0.5Vc2	State3	State2	3E
Vc1>vc2	State5	State4	2E
Vc1<Vc2	State4	State5	2E
Vc3>0.5Vc2	State6	State7	E
Vc3<0.5Vc2	State7	State6	E
No condition	State8	State8	0

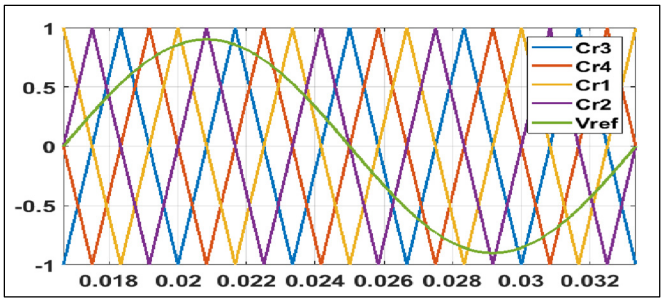

Figure 2.4 Carriers and voltage reference
for modulation of one module of ZPUC

method presented in (Richardeau & Pham, 2013; Y. Song & Wang, 2013). As defined, reliability is the performance of the system during a defined time. Based on the IEEE std 493-2007, reliability is the capability of a system to accomplish associated functions over a time ("IEEE Recommended Practice for the Design of Reliable Industrial and Commercial Power Systems," 2007). In other words, reliability is the probability that the system functions in its normal operation in defined duration. Its simplified equation is given by ("IEEE Recommended Practice for the Design of Reliable Industrial and Commercial Power Systems," 2007; Y. Song & Wang, 2013):

$$R(t) = e^{-\lambda t} \tag{2.7}$$

$$\lambda = \frac{1}{MTTF} \tag{2.8}$$

Where *R(t)* is the reliability of the system and λ is the failure rating that is an inverse of MTTF (mean time to failure). *MTTF* shows the time duration in which the equipment or system operates in normal function. Each device or systems in power converters have their own failure rating which are normally mentioned in the manufacturer data sheets. Redundancy would enhance the reliability of the system through reduction in λ index. Two popular series and parallel reliability models has been introduced in (Richardeau & Pham, 2013; Y. Song & Wang, 2013). While there is redundancy in parallel model and operation of *k* devices out of *n* devices are adequate for normal operation of system. Total failure rating and reliability in series model is obtained by:

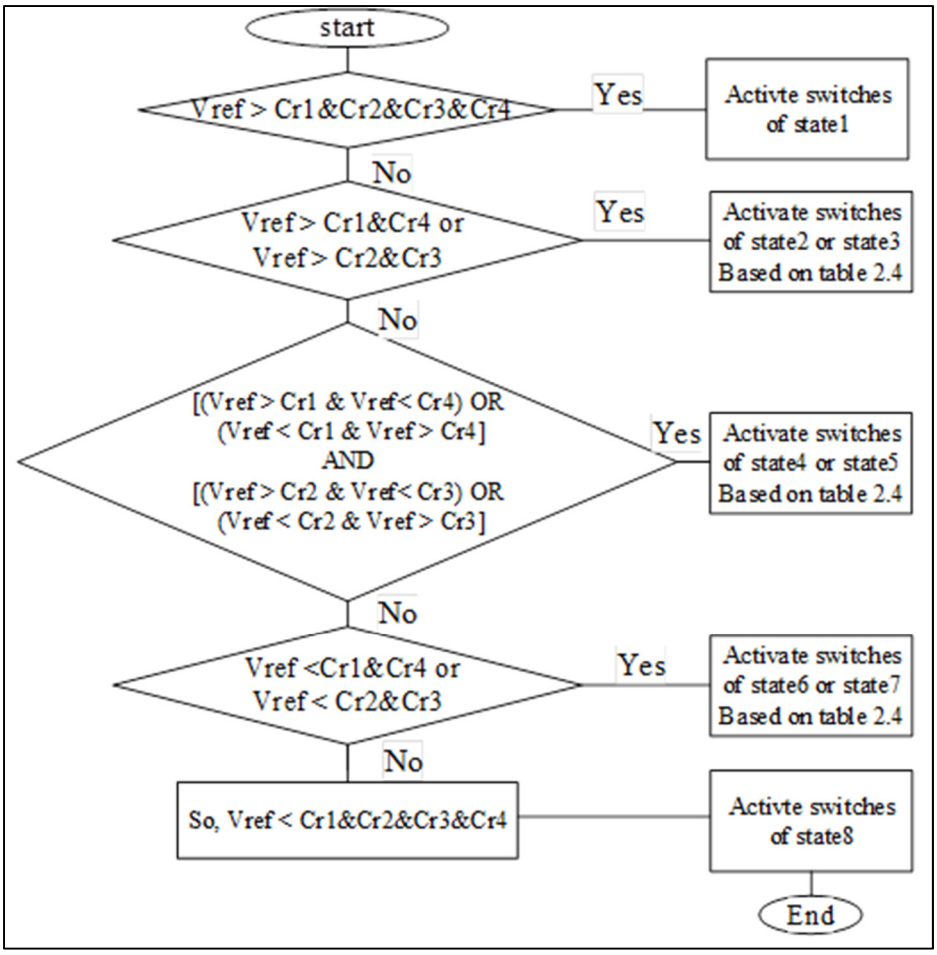

Figure 2.5 Flowchart of voltage balancing integrated with phase-shift modulation strategy

$$\lambda = \sum_{i=1}^{n} \lambda_i \tag{2.9}$$

$$R(t) = \prod_{i=1}^{n} R_i(t) \tag{2.10}$$

Where, i denotes the number of devices or subsystems and λ_i is the failure rating of i^{th} subsystem. In non-redundant systems, the reliability is reduced when the devices are added. To illustrate, the topology and reliability block diagram of one module of ZPUC5 topology in series model in which generating 5L waveform is necessary to meet the power quality standard is depicted in figure.2.6. a and b. Total reliability of the system for this series model is obtained as equation 2.9 and 2.10. In this diagram, $\lambda_{S1, S2}$, $\lambda_{S3, S4}$ and $\lambda_{S5, S6}$ are called failure rating of cell

1, cell 2 and cell 3 respectively. On the other hand, overall reliability of the parallel model for operation of *k* subsystem out of *n* subsystem or devices is given by equation.2.11.

$$R(t) = \sum_{i=k}^{n} C(n,i) R_i(t)^i \left(1 - R_i(t)\right)^{n-i} \tag{2.11}$$

Where *C(n,i)* is combination of *i* elements from a set of *n* devices or subsystems which is obtained by equation 2.12.

$$C(n,i) = \frac{n!}{i!(n-i)!} \tag{2.12}$$

Reliability block diagram for one module of ZPUC topology by taking into account the redundancy is illustrated in figure 2.6.c.

One module of ZPUC5 topology generates 5L waveform in normal condition and it generates 4L and 3L when one cell out of three cells is faulty and it is bypassed. It also can operate to generate two level waveforms when two cells out of three cells are failed and bypassed. Thus, depend on the desired voltage waveform at the output of the converter, the reliability of ZPUC module varies due to variation in required redundancy. For instance, combinations of (3,2) from equation 2.12 must be replaced in equation 2.11 to obtain the reliability of the ZPUC converter regarding several combinations such as 5L, 4L and 3L output waveform. Following redundancy could be considered for ZPUC module due to failure of cells:

a. normal condition (5L)
b. Cell 1 fails (3L)
c. Cell 2 fails (3L)
d. Cell3 fails (4L)
e. Cells 1, 2 fail (2L)
f. Cells 2, 3 fail (2L)
g. Cells 1, 3 fail (2L)

Reliability for four states from (a) to (d) to have at least 3L waveform in terms of ZPUC module is obtained by summation of reliabilities in these four states by substituting of suitable

combination of *n* from *k* in equation 2.11. Ergo, the reliability of ZPUC could be increased through redundant states which is another advantage of this topology due to its proper redundancy to generate variety of voltage levels by failing one or two cells out of 3 cells. It should also be noted that to calculate the reliability of converter, the failure rating of controller, gate drives and DC sources must be added to the switching devices and capacitors.

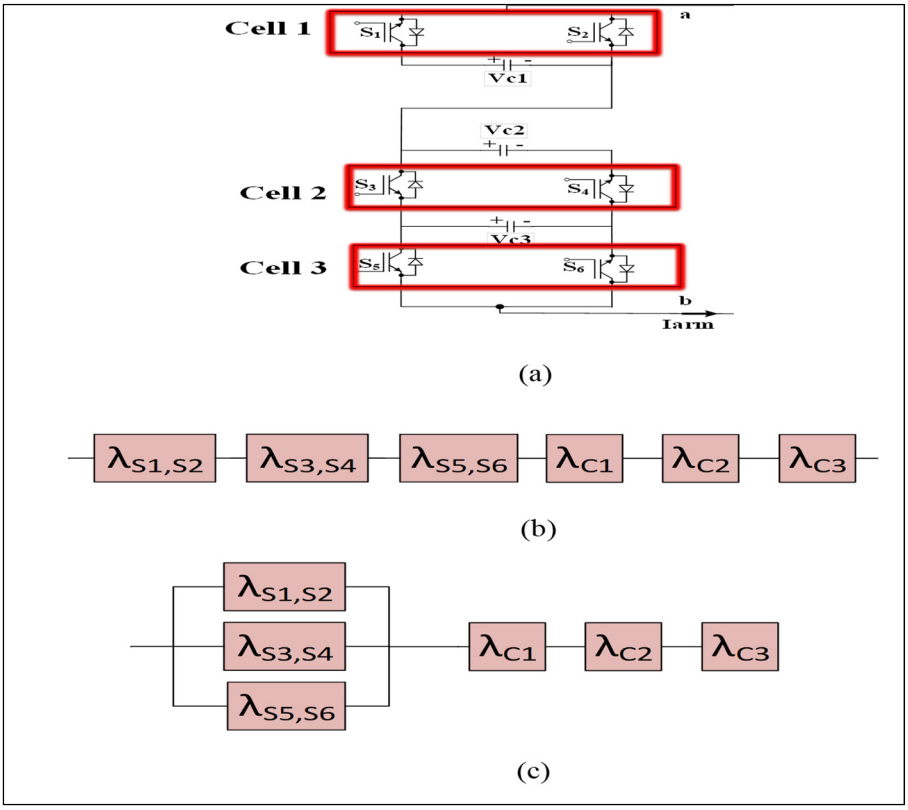

Figure 2.6 Reliability analysis a) Structure of one module of ZPUC topology based on separated Cells, b) reliability block diagram of one module of ZPUC without redundancy c) with redundancy

2.3.4 Voltage Balancing Method On Three-Phase ZPUC Multilevel Converter

ZPUC converter which is shown in figure 2.3 generates 9L waveform across the load in stand-alone mode. Hence, 8 carrier is required to modulate the reference wave. Figure 2.4 shows the carriers Cr1 to Cr4 which are placed in 0°, 90°, 180°, 270° and they are modulated with reference voltage Msin*(ωt)*. These carriers and reference voltage are utilized to build 5-L waveform and

voltage balancing in three flying capacitors of the upper arm. As well, carriers Cr5 to Cr8 with -Msin(ωt) which is shown in figure 2.7, are used to balance the voltage and making 5-L voltage in the lower arm. Phase shift among carriers Cr5, Cr6, Cr7 and Cr8 are in 45°, 135°, 225° and 315°. It should be noted that flowchart of figure 2.5 and table 2.4 is used for upper and lower arm separately except that the carriers Cr1 to Cr4 must be replaced by Cr5 to Cr8 for lower arm. Control diagram of ZPUC converter which has been shown in of figure 2.3 is depicted in figure 2.8.

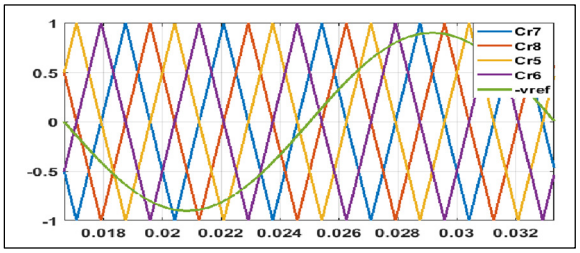

Figure 2.7 Carriers and voltage reference for modulation ZPUC module of the lower arm shown in figure 2.3

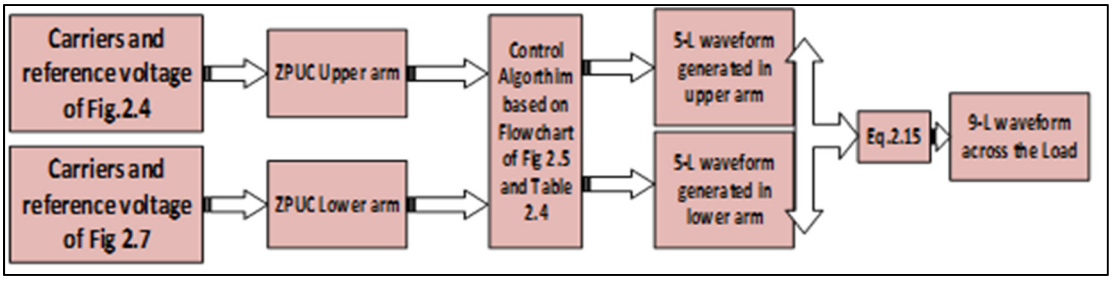

Figure 2.8 Control diagram of two ZPUC module in 9-L multilevel converter

To illustrate the algorithm of voltage balancing in ZPUC converter and generation of 9-L waveform, one single line diagram of two ZPUC modules is depicted in figure 2.9.

The equations for output voltage of figure 2.9 are given by:

$$V_{xu} = V_{DC} - V_L \tag{2.13}$$

$$V_{xl} = V_{DC} + V_L \tag{2.14}$$

$$V_L = \frac{V_{xl} - V_{xu}}{2} \tag{2.15}$$

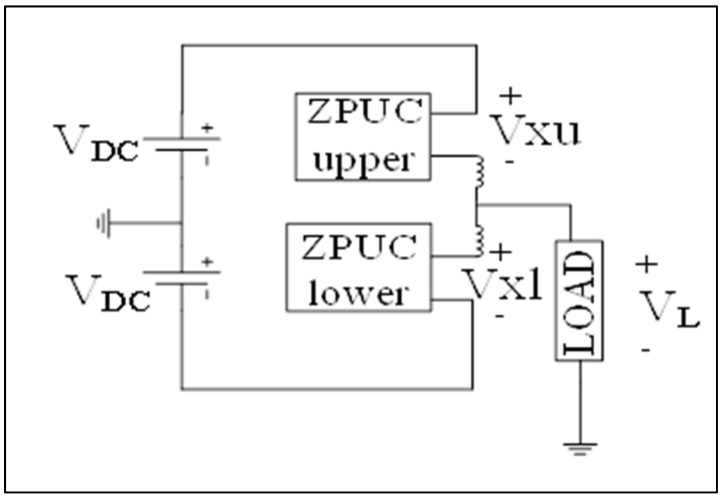

Figure 2.9 Single line diagram of 9-L ZPUC converter

V_{xu} and V_{xl} in figure 2.9 are voltages in upper and lower arms, V_L is the load voltage and x index shows the phases a, b, c. Equation 2.15 shows that load voltage levels would be twice of voltage of each arm so that they sorted in both negative and positive side through mentioned modulation. In other words, 5-L unipolar waveform is produced in upper and lower arms and 9-L bipolar waveform is generated across the load. The control diagram to generate 9-L waveform through voltage balancing integrated with the modulation technique is shown in figure 2.8. Figure 2.10 shows the 9L voltage across the load from ZPUC converter in which 400 V DC voltage is divided in 9 steps having 15.67% voltage THD and 0.9% current THD. It should be noted that the total harmonic distortion (THD) on ZPUC multilevel converter is reduced due to increased voltage levels in comparison with the competitive topologies of multilevel converters.

2.4 Application of ZPUC5 on Modular Multilevel Converters (MMCs)

Figure 2.11 illustrates the configuration of MMC with sub-module of ZPUC in which MMC configuration consists of cascaded ZPUC in two arms per phase. Generally, 4N+1 levels

waveform is generated in upper and lower arm in terms of N submodules in each arm. They are arranged from 0 to 4NE in E steps. It should be noted that 4NE is equal to total DC link voltage or $2V_{DC}$. Load voltage level is equal to 8N+1 that is

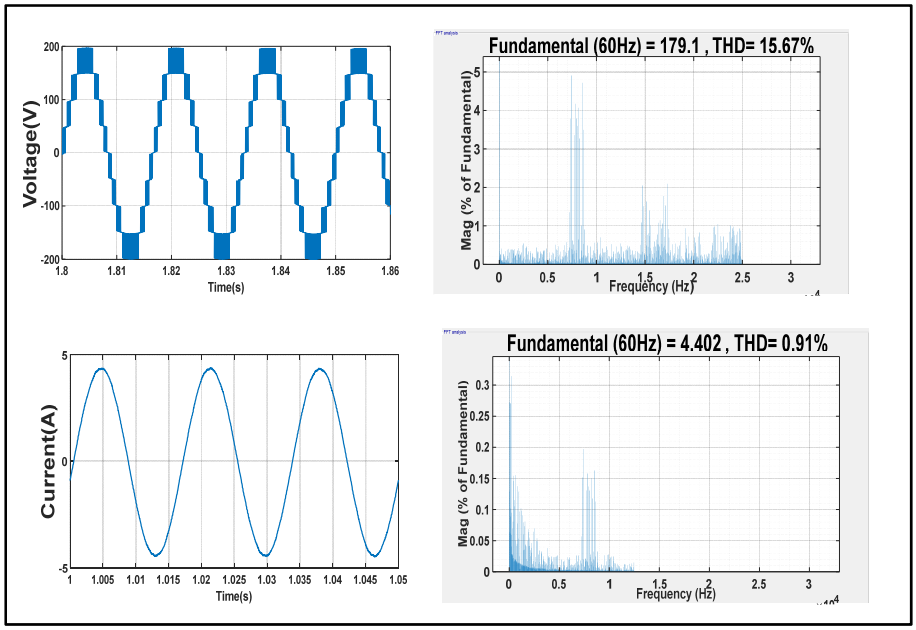

Figure 2.10 Voltage and Current waveform, voltage and current THD of single-phase ZPUC of figure 2.3

located from -2NE to +2NE in steps ½E. Figure 2.12 shows that how voltages are generated in upper and lower arms and accordingly across the load in ZPUC-MMC. Number of voltage levels in ZPUC-MMC is as follows:

$$M_{phase} = 8N+1 \tag{2.16}$$

Where M_{phase} is the voltage levels across the load in general ZPUC-MMC. General relation between the line waveform and phase waveform is given by:

$$L_{line-W} = 2L_{phase-W} - 1 \tag{2.17}$$

Ergo, in ZPUC-MMC the line waveform level across the three-phase loads is obtained by equation 2.18.

$$M_{line} = 16N + 1 \tag{2.18}$$

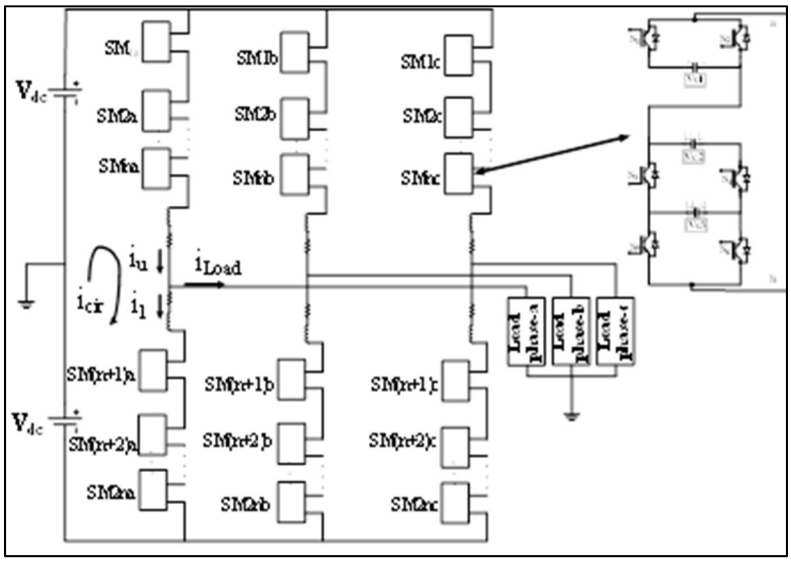

Figure 2.11 MMC configuration with ZPUC submodule

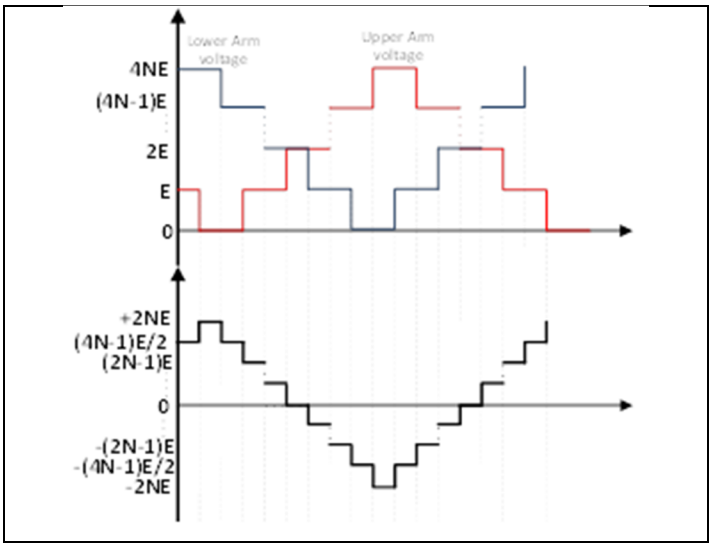

Figure 2.12 General voltage waveforms of upper and lower arms and across the load on ZPUC-MMC

Following steps shows the algorithm of voltage balancing in MMC based on algorithms listed in table IV and flowchart of figure 2.5.

a. Sorting of the total stored energy of each module based on normalized measured voltages of flying capacitors in descending way. The simplified equation with the assumption that all capacitors are similar is as follows:

$$E_{ci} = \sum_{j=1}^{3} V_{cij}^{2} \qquad (2.19)$$
$$I = sort(E_{ci})$$

Where Eci is the total storage energy in ith module of ZPUC in each arm. I is the sorting matrix in which ZPUC modules of each arm are arranged with a maximum energy values to minimum. Vcij is the measured voltage of FCs in ith module and j defines the number of capacitors in each module.

b. implementation of modulation strategy to generate voltage levels.

c. defining the direction of corresponding arm current

d. To generate maximum voltage level of 4NE, all submodules per arm should be operated in state 1 based on table IV. To generate voltage level of (4N-1)E, the module corresponding to the first array I (1) in equation 2.19 should be selected to operate in states 2 or 3. I(1) defines the submodule with the maximum energy which must be selected in order to discharge its FC with the aim of energy reduction. The algorithm described in table 2.4 should be used for selection between mentioned states. Actually, the other submodules operate at state 1. As well, to generate state (4N-2)E, the submodules corresponding to the arrays of I (1), I (2) have to be selected to operate in states 2 or 3 depends on normalized voltages as in table 2.4. This method is performed for the other voltage levels.

Equation 2.15 is rewritten by following equation for output voltage of ZPUC-MMC.

$$V_L = \frac{\sum_{i=1}^{N} u_{li} - \sum_{i=1}^{N} u_{ui}}{2} \qquad (2.20)$$

Where, $\sum u_{ui}$ and $\sum u_{li}$ are the total voltage of ZPUC submodules in upper and lower arms. N is the number of ZPUC submodules in each arm and i index implies voltage at the i^{th} ZPUC. Output voltage of ZPUC-MMC with the assumption that 2Vdc=4NE, is listed in Table 2.5 based on Figure 2.12. The rows of this table show the total voltages on lower arms, upper arms, and output of ZPUC-MMC for corresponding switching states for 8N+1 switching states.

2.4.1 Circulating Current in ZPUC-MMC

Circulating current is an issue which appear in modular multilevel converters and increases the power losses due to negative sequence components. Although, it is limited through current limiting inductor that is called buffer inductor, control method also plays the effective role to mitigate and suppress it. Load current and circulating current in terms of upper and lower currents which has been shown in figure 2.11 are obtained by equations. 21 to 23.

$$i_u - i_l = i_{Load} \tag{2.21}$$

$$i_{cir} = i_u - \frac{i_{Load}}{2} = i_l + \frac{i_{Load}}{2} \tag{2.22}$$

$$\frac{i_u + i_l}{2} = i_{cir} \tag{2.23}$$

Where i_u, i_l and i_{cir} are upper arm current, lower arm current and circulating current respectively. Figure 2.11 demonstrates that the circulating current is created through the difference between AC and DC voltages. Following equation is obtained by KVL loop which cause the circulating current in figure 2.11.

$$\sum_{i=1}^{N}(u_{ui} + u_{li}) + \mathrm{L}_{arm}\frac{d}{dt}\left(i_u + i_l\right) + \mathrm{R}_{arm}\left(i_u + i_l\right) = 2\,\mathrm{V}_{dc} \tag{2.24}$$

Where u_{ui}, u_{li} are the output voltage of each submodule in upper arm and lower arm respectively, L_{arm} and R_{arm} are the inductance and resistance of current limiting reactor or buffer inductor, and N is number of ZPUC submodules per arm. Regarding to the lower

resistance compared to inductance in buffer inductor, the resistance term is neglected from equation 2.24. Moreover, by substituting equation 2.23 into equation 2.24, and separating current terms from voltage terms following equations are obtained:

$$2\,\mathrm{V}_{dc} - \sum_{i=1}^{N} (u_{ui} + u_{li}) = 2\,\mathrm{L}_{arm} \frac{di_{cir}}{dt} \tag{2.25}$$

$$V_{diff} = 2\,\mathrm{V}_{dc} - \sum_{i=1}^{N} (u_{ui} + u_{li}) \tag{2.26}$$

Left hand term of equation 2.25 implies the reason why the circulating current is created in MMCs which is shown separately by equation 2.26. In fact, the control method should reduce the difference between the DC voltage and AC voltage to mitigate the circulating current. Although, the buffer inductance, L_{arm}, plays an evident role based on equation 2.25 to mitigate the circulating current, it could not be selected so large due to its bulkiness and much cost of the converter. Circulating current is automatically controlled by proposed voltage balancing control method integrated with modulation strategy through selection of appropriate switching states in upper and lower arm submodules. To illustrate, the difference voltage which cause the circulating current are listed in table 2.5 together with ZPUC-MMC arms voltages and output voltage for all *8N+1* states. For instance, to generate voltage *2NE* at the output of MMC, corresponding switching states should be designated in upper and lower arms to generate voltage levels 0 and *4NE* respectively in which difference voltage would be zero according to equation 2.26 and this assumption that $2V_{dc}=4NE$. Table 2.5 shows that the absolute value of voltage difference in all states are zero or *E* which makes this converter controllable against the circulating current. With regard that DC link voltage, $2V_{dc}$, is assumed to be *4NE*, V_{diff} is reduced by increasing the number of ZPUC submodules. In other words, the value of *E* is reduced through expansion of the submodules due to the following equation:

Table 2.5 V_{diff} in Corresponding Lower and Upper Arms Voltages

Total Voltage at lower arm ($\sum U_{li}$)	**Total Voltage at upper arm ($\sum U_{ui}$)**	**MMC Output voltage**	**Difference voltage (V_{diff})**
4NE	0	2NE	0
4NE	E	(4N-1)E/2	-E
(4N-1)E	0	(4N-1)E/2	+E
(4N-1)E	E	(2N-1)E	0
(4N-1)E	2E	(4N-3)E/2	-E
(4N-2)E	E	(4N-3)E/2	+E
(4N-2)E	2E	2(N-1)E	0
(4N-2)E	3E	(4N-5)E/2	-E
(4N-3)E	2E	(4N-5)E/2	+E
(4N-3)E	3E	(2N-3)E	0
(4N-3)E	4E	(4N-7)E/2	-E
: :	: :	: :	: :
4E	(4N-3)E	-(4N-7)E/2	-E
3E	(4N-3)E	-(2N-3)E	0
2E	(4N-3)E	-(4N-5)E/2	+E
3E	(4N-2)E	-(4N-5)E/2	-E
2E	(4N-2)E	-2(N-1)E	0
E	(4N-2)E	-(4N-3)E/2	+E
2E	(4N-1)E	-(4N-3)E/2	-E
E	(4N-1)E	-(2N-1)E	0
0	(4N-1)E	-(4N-1)E/2	+E
E	4NE	-(4N-1)E/2	-E
0	4NE	-2NE	0

*note: $4NE=2V_{dc}$

$$E=\frac{V_{dc}}{2N} \tag{2.27}$$

Where V_{dc} is half of the DC link voltage as shown in figure 2.11, E is the step voltage value in the output waveform, and N is the number of ZPUC submodules in each arm. In fact, E parameter in ZPUC-MMC is reduced by increasing the N which demonstrates that V_{diff} is reduced as shown in table 2.5. Accordingly, the circulating current of ZPUC-MMC is reduced, similarly of DC link voltage by expansion of submodules. The special control methods to suppress the circulating current could also be implemented on ZPUC-MMC as the other well-known MMCs such as HB-MMC.

2.4.2 Power losses in ZPUC-MMC

Conduction and switching losses are the main parts of power losses in power converters devices. Conduction loss is created due to the on resistance and on state voltage of switching devices and antiparallel diodes. Switching losses are the loss of energy which are created for nonideality in switches commutation caused by turn on and turn of times. In this subsection, ZPUC converter is compared to the HB-MMC which is the most popular type of MMC in research area and industry, to evaluate from power loss aspect. The power losses have been calculated through presented methods on papers (Gao & Lu, 2018; Kangarlu & Babaei, 2013). The calculations have been carried out for the same type of IGBT from Fuji electric (FGW35N60HD). Following equation can be obtained according to the typical output characteristic figure in manufacturer datasheet for maximum junction operation temperature.

$$\begin{aligned} i_c &= 0.028V_{CE} + 0.933 \\ i_D &= 0.03V_D + 0.9 \end{aligned} \tag{2.28}$$

Where, V_{CE} is the collector-emitter voltage of IGBT, V_D is the antiparallel diode voltage, i_c is the collector current, and i_D is the antiparallel diode current. Resistance and on state voltage of IGBT and diode are utilized to obtain the conduction losses.

Table 2.6 shows the parameters of load and DC source that is selected to compare the power losses between two MMCs in the similar primary conditions and the same switching devices.

It should be noted that the similar condition is considered to calculate the power losses for two types of MMCs. It can be observed that the total power losses in ZPUC-MMC is lower than. well-known HB-MMC to generate the same voltage levels.

Table 2.6 Power Losses Comparison Between HB-MMC and ZPUC-MMC with 9-L Output Waveform

Parameters	**HB-MMC**	**ZPUC-MMC**
Cells per arm	8	1
Vdc (V)	400	400
L_{arm} (mH)	1	1
R_{arm} (Ω)	0.1	0.1
L_{load} (mH)	25	25
R_{load} (Ω)	20	20
Cosφ	0.9	0.9
carrier frequency	2000 Hz	2000 Hz
Modulation Index	0.95	0.95
P	730	730
Q	345	345
Total Power losses	78.2watt	46.87 watt
efficiency	89.43%	93.76%

2.4.3 Flying Capacitor design

Design of flying capacitors in ZPUC converter which consists of three FCs in each module plays a crucial role to mitigate the voltage ripple and consequently to improve the voltage and current waveform. Since, the converters during the grid connected must meet the related standards requirements, FC must be designed carefully in terms of voltage ripple. Following general equation which implies the capacitor current with respect to the capacitance and capacitor voltage is utilized to design the FCs.

$$i_p = C\frac{dv}{dt} = C\frac{\Delta v}{\Delta t} \tag{2.29}$$

Where, i_p is the peak of the load current, C is the capacitance of FCs in ZPUC converter, Δv is the peak-to-peak voltage ripple which can be selected based on permissible value in associated applications. As FCs of ZPUC modules operate at switching frequency in the proposed voltage balancing control method, capacitance value of FCs is obtained by equation 2.30.

$$C = \frac{i_p}{f_{sw}\Delta v} \tag{2.30}$$

Where f_{sw} is the switching frequency. For instance, C on the ZPUC converter set up of figure 2.3 with DC source of 100V is 2000μF which based on the switching frequency of 1000 Hz and load current peak of 2A, voltage ripple on the lower FCs is 1 V. With regard that voltage on the lower capacitor should be regulated on 25 V, voltage ripple is 4%. Capacitance value can be selected lower with increasing the permissible voltage ripple or increase on the DC source voltage. On the other hand, it should be selected in higher value when load current increases

2.4.4 Grid Connected Mode of ZPUC-MMC

ZPUC converter could also be operated as an inverter to inject the current into the grid. Voltage balancing control in this mode is exactly as explained in stand-alone mode. However, current control must be carried out in grid connected mode to protect the converter against the overcurrent which cause the failure of devices. Furthermore, the power factor is controlled while the power is injected to the grid. Figure 2.13 shows the single-line diagram of control for ZPUC converter in grid connected mode.

Typical PI controller is used to show the performance of ZPUC converter in grid connected mode. $I_{ref}Sin(\omega t+\varphi)$ is the reference current that is the desired injected current into the grid in which phase angle, ωt, is obtained by PLL circuit. I_{ref} is the current amplitude which is adjusted

based on the power rating of converter to restrain the overcurrent and to preserve the converter in case of fault events.

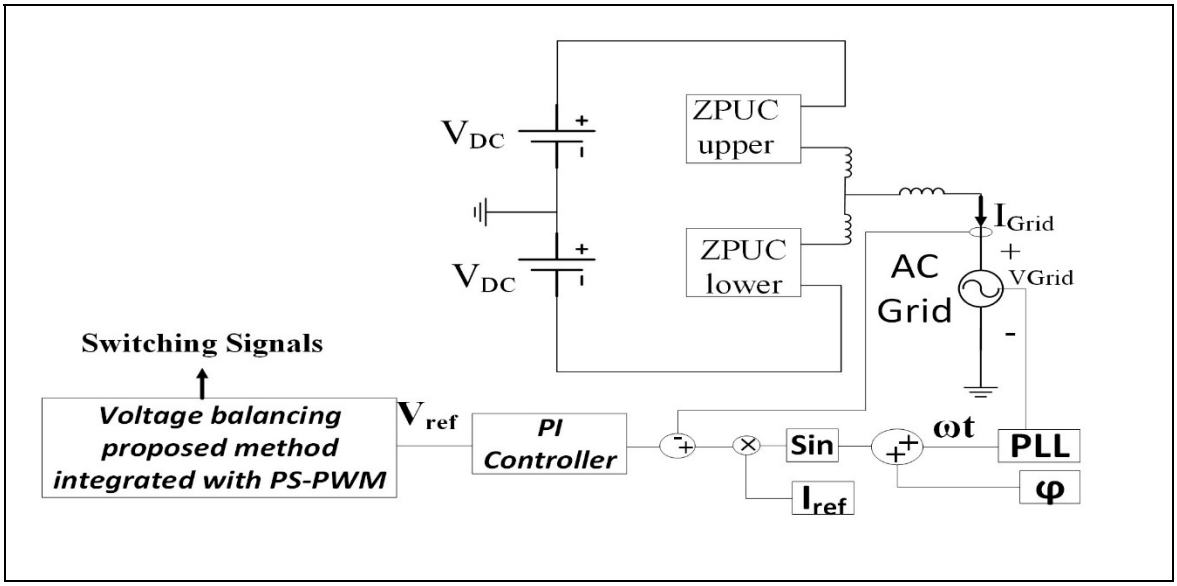

Figure 2.13 Single-line diagram of controller for ZPUC converter in grid connected mode

Injected current from ZPUC inverter into the grid is measured and then it is subtracted by reference signal to generate the error signal. Output of PI controller makes the voltage reference signal from the error current signal that is sent to the modulation strategy integrated with the voltage balancing program to balance the flying capacitor voltages and to control the grid current simultaneously. Through appropriate selection of phase shift, φ, the desired value of power factor is achieved which could be a profitable option for connection of photovoltaic power plant to the grid. Moreover, this converter could play the role of active and reactive power compensator through regulating of phase shift when it works in grid-connected mode. The associated results are discussed in results section to show the performance of the converter on grid connected mode.

2.5 Simulation Results

The proposed converter has been studied by simulation using MATLAB/Simulink on standalone feeding RL loads and grid connected system in order to verify the proposed topology operation as well as the proposed control method on ZPUC-MMC. The system parameters which has been used in simulation and experimental stand-alone tests are listed in table 2.7. Voltage balancing algorithm integrated with phase shift PWM method (S. Arazm et al., 2018a) is used to show the voltage balancing in flying capacitors in this case study.

Table 2.7 Simulation and Experimental Parameters of Stand-alone Mode

DC source voltage	**100 V**
Switching frequency	1000 Hz
System frequency	60Hz
Load	40 Ω, 20 mH
Buffer inductance	2 mH
Capacitor C1, C2, C3	2000 μF
Sampling time	46 μs

2.5.1 Standalone mode

Nine level phase voltage and seventeen level line voltage across the three-phase star load of single DC source three-phase ZPUC converter of figure 2.3 is shown in figure 2.14.

Moreover, figure 2.15 shows the three-phase current and related THD in steady state which demonstrate the performance of this converter and proposed voltage balancing integrated with modulation technique.

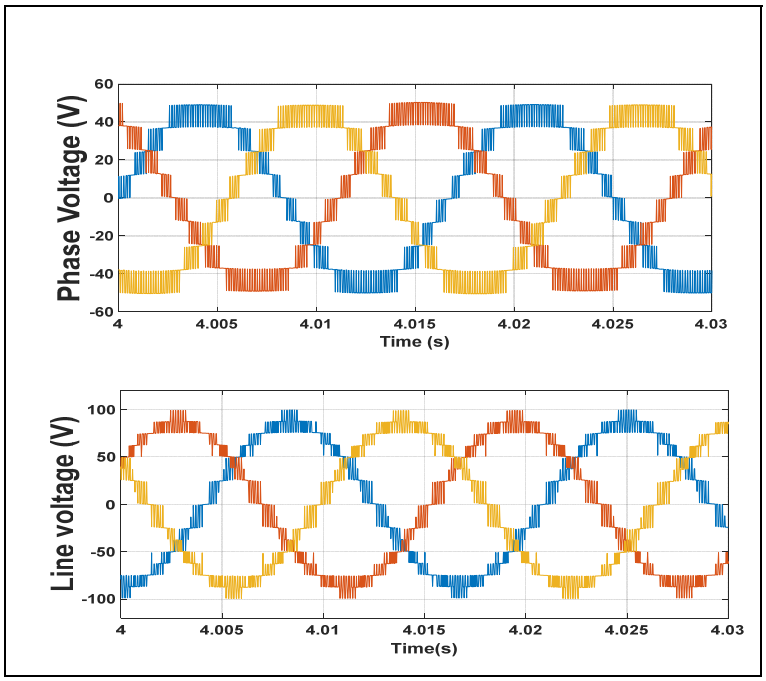

Figure 2.14 9L phase voltages and 17L line voltages in three-phase single DC source ZPUC inverter

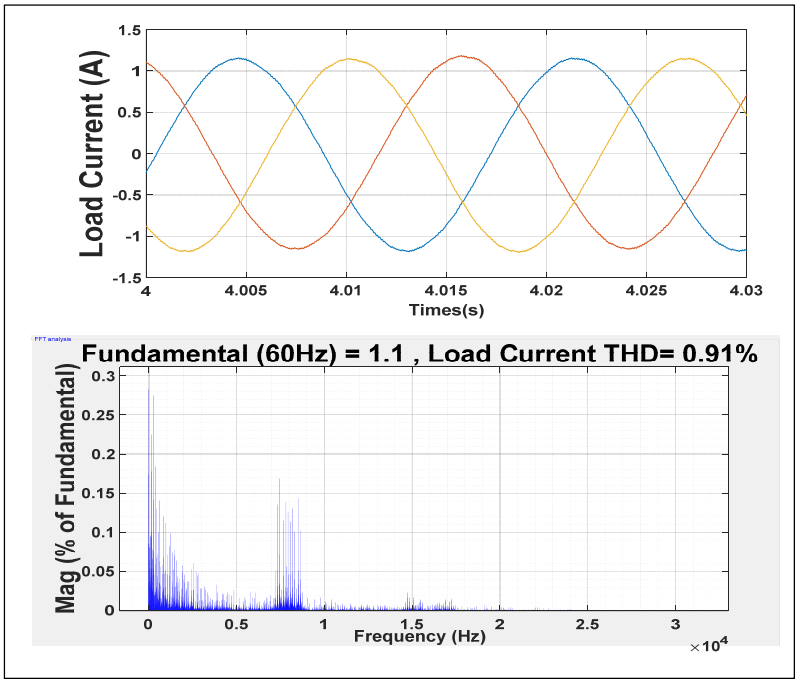

Figure 2.15 Three-phase current and current THD of ZPUC converter

The dynamic performance of ZPUC-MMC with two modules of ZPUC per arm during the DC source variation is illustrated in figure 2.16. Voltages in all twelve FCs has been shown in figure 2.16. The voltages in FCs are balanced properly in steady state and in transient state with a sever DC voltage variation. As well, small value of voltage THD for 17-L phase voltage demonstrates that the output filter size can be very much reduced which reduces the cost of converter considerably.

To study the dynamic response of ZPUC-MMC converter a step of DC voltage changes representing the worst-case scenario on the DC link capacitor has been considered and the simulation results are depicted in figure 2.17. This figure shows the dynamic response of the converter when the DC source is varied by 100% from 100 V to 200 V and then back to 100 V. FCs voltages are completely stabilized within 200ms, and the magnitude of voltage surge is less than 68 V. However, in practical application up to 20% of voltage variations can be tolerated in which the surge magnitude is consequently very limited.

Moreover, load current is another parameter which may be changed in stand-alone mode. Thus, in figure 2.18, performance of ZPUC-MMC with two modules per arm under the load variation is examined. The load is varied from 40Ω to 20Ω and again it comes back to its first value 40Ω. The inductance was not changed in this test. FC voltages are balanced in their desired value which has been carried out by proposed voltage balancing method. However, the voltage ripple in FCs is increased due to the load current increase which is verifiable from the equation 2.30. As well, it is shown that the load voltage is constant during the load variation which verifies the performance of the converter. Moreover, circulating current and load current are shown in this figure which confirms the acceptable circulating current control through voltage balancing method integrated with the modulation technique. However, additional control system can be used for complete elimination of circulating current which reduces the reliability and requires the more cost.

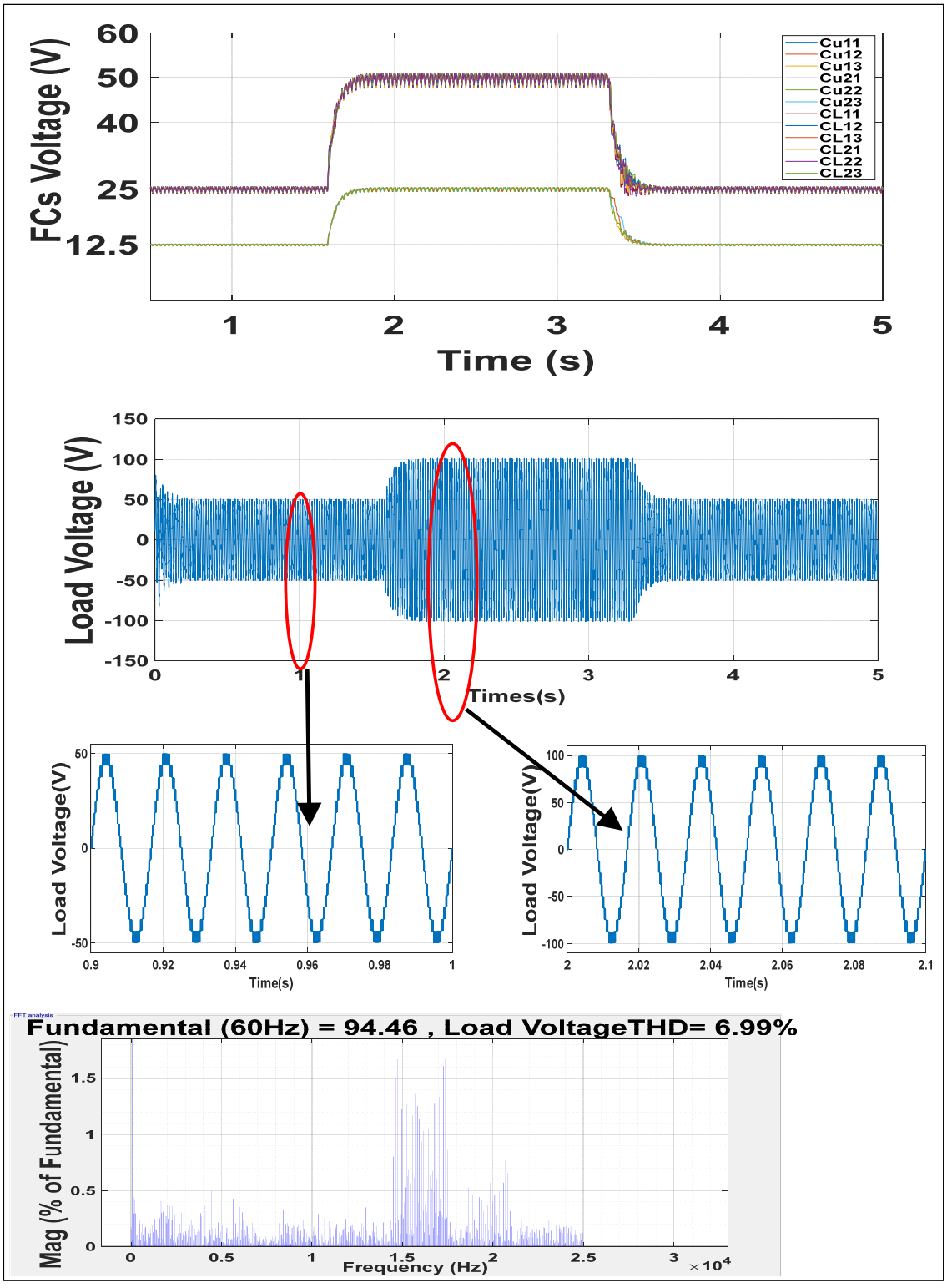

Figure 2.16 FCs voltage waveforms and load voltage during the DC link Variation from 100V to 200V and back to 100V, Load voltage THD when the DC link has been increased

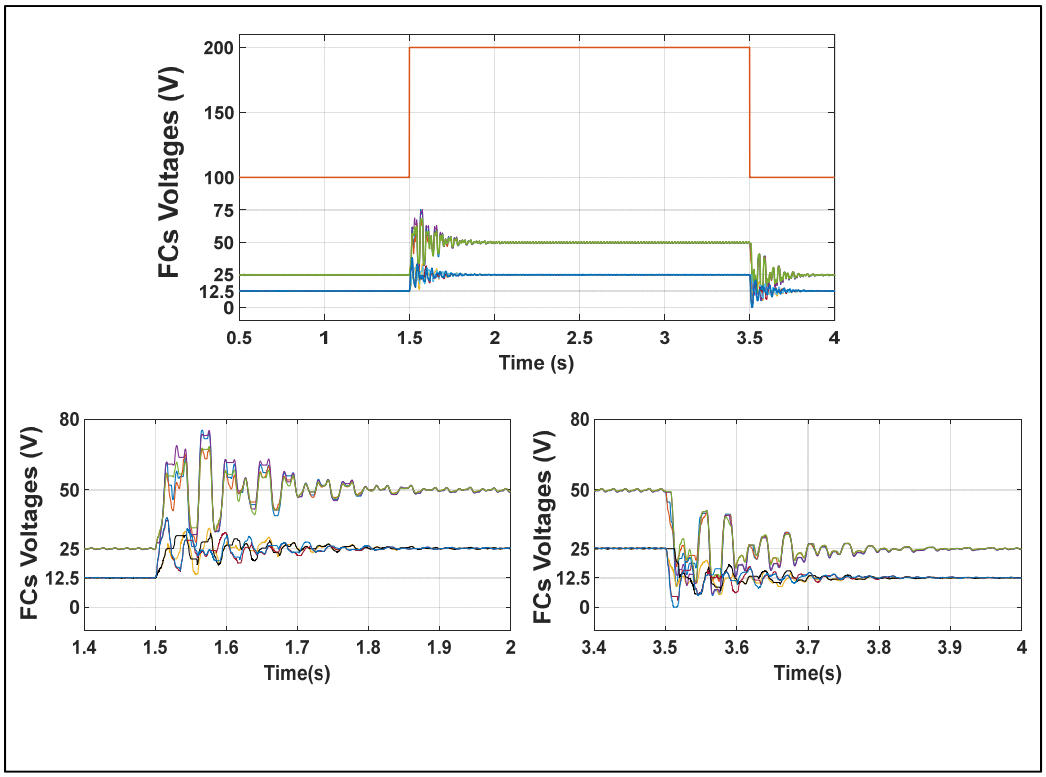

Figure 2.17 Dynamic response of ZPUC-MMC converter for a 100% step of dc voltage changing from 100 V to 200 V and then back to 100 V

2.5.2 Grid-connected mode

ZPUC-MMC with two modules per arm is considered for grid-connected operation so as to verify the performance of the proposed converter and the control.

As discussed in section 2.4.4. the PI control integrated with voltage balancing algorithm is used to current and power factor control. Dynamic response of ZPUC-MMC has been investigated in two transient mode including reference current variation and power factor variation. Simulation parameters are listed in table 2.8 in which DC link voltage and FCs size has been altered due to current injection to the grid and voltage ripple control based on equation 2.30.

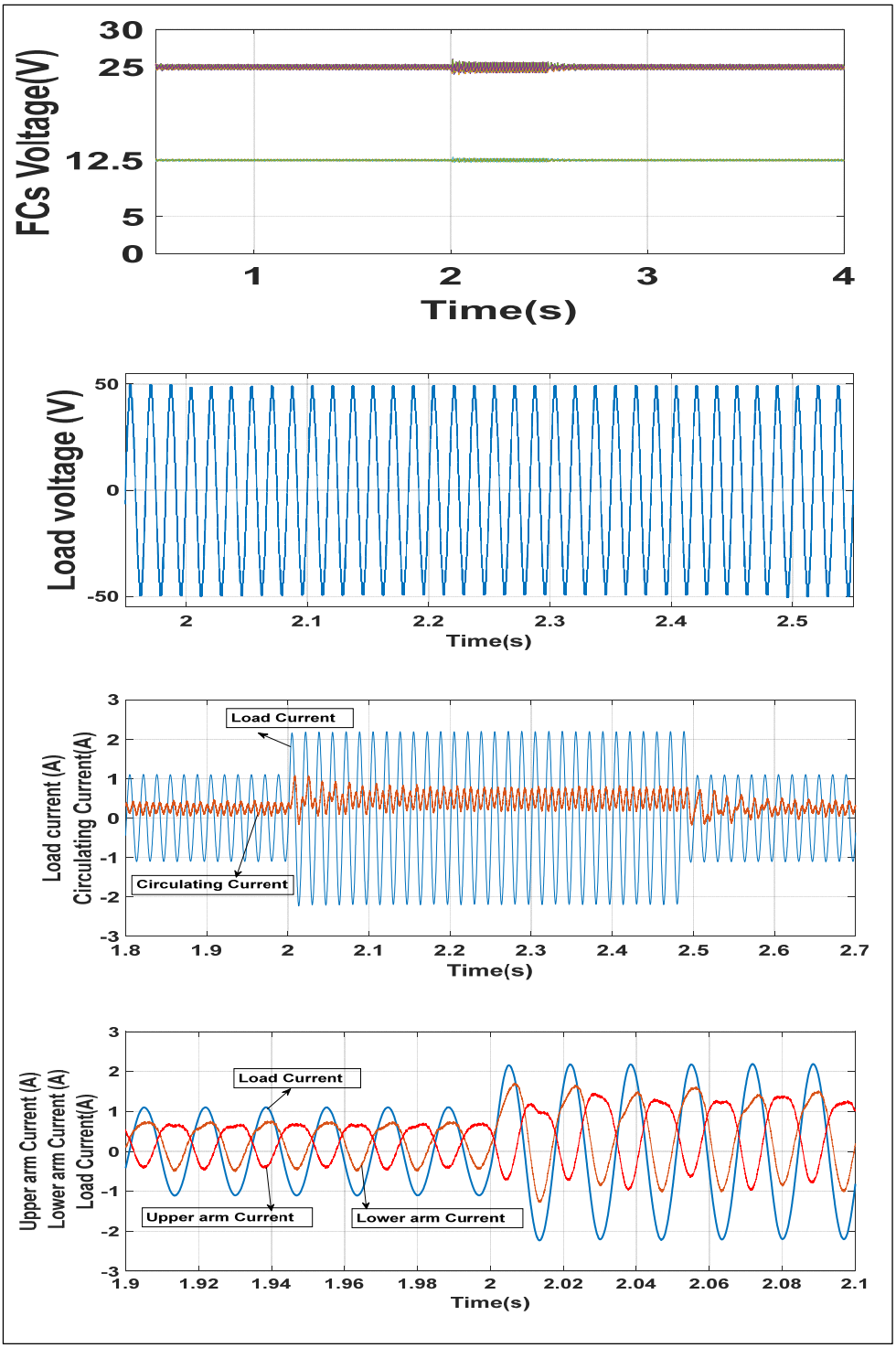

Figure 2.18 Wave forms of FCs voltage, load voltage, load current, upper arm current, upper arm current and circulating current during the load variation from 40Ω-20Ω-40Ω

Table 2.8 Simulation Parameters of Grid-Connected Mode

DC link voltage	400 VDC
Grid voltage	120 Vrms
Grid link inductor	2 mH
Capacitor C1, C2, C3	**5**000 µF
Reference current	20A
Refence power factor	1

Power factor and injected current are the parameters which must be controlled when the converter is connected to the grid. Thus, in transient state, these two parameters are severely varied to verify the performance of the converter. Figures 2.19 illustrates the grid voltage and grid current at the same figure to show the power factor control and injected current control simultaneously. It can be seen that the grid current is changed from 20A to 40A based on reference current change and the phase shift between the grid current and grid voltage wave is zero which implies the performance of controller to make the reference PF=0 exactly.
Figure 2.20.a depicts the FC voltages which shows the performance of voltage balancing algorithm and control system during the transient state due the load variation. Figure 2.20.b shows, upper and lower arm voltages which are placed in opposite phase shift based on the proposed voltage balancing control method. Nine level waveform is generated in each arm that make 17L waveform at the output of inverter due to using two ZPUC modules per arm.

Figure 2.21 shows the circulating current and arms current that verifies the performance of voltage balancing integrated with modulation technique to mitigate it. THD of current which is injected into the grid through ZPUC converter shows extremely small value that are due to 17L voltage at the output of the inverter. This small value is useful to drastically reduce the filter size from the ZPUC inverter. Figure 2.22 illustrates grid current and voltage as well as the voltage balancing in FCs during the power factor variation in which the PF was changed

from 1 to 0 at t=3s and back to 1 at t=3.2s. This fast-dynamic response also verifies the performance of ZPUC converter at transient state in grid connected mode.

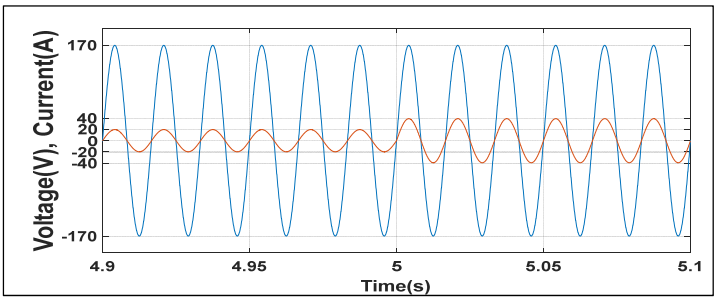

Figure 2.19 Grid current and grid voltage during the variation in reference current from 20A to 40A and reference PF=0

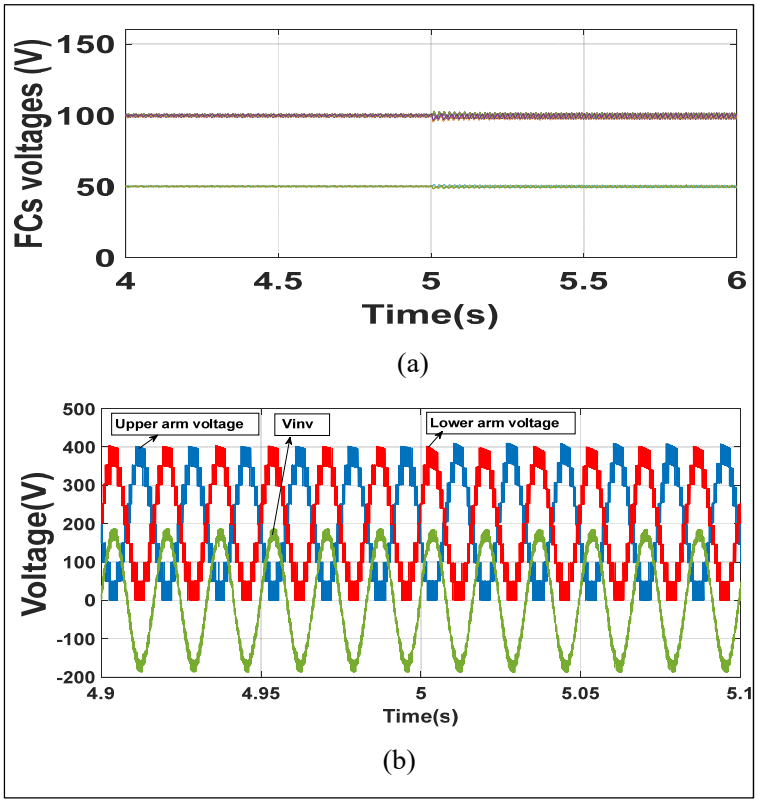

Figure 2.20 a) FCs voltages b) upper arm voltage, lower arm voltage and inverter voltage during reference current changes from 20A to 40A and reference PF=0

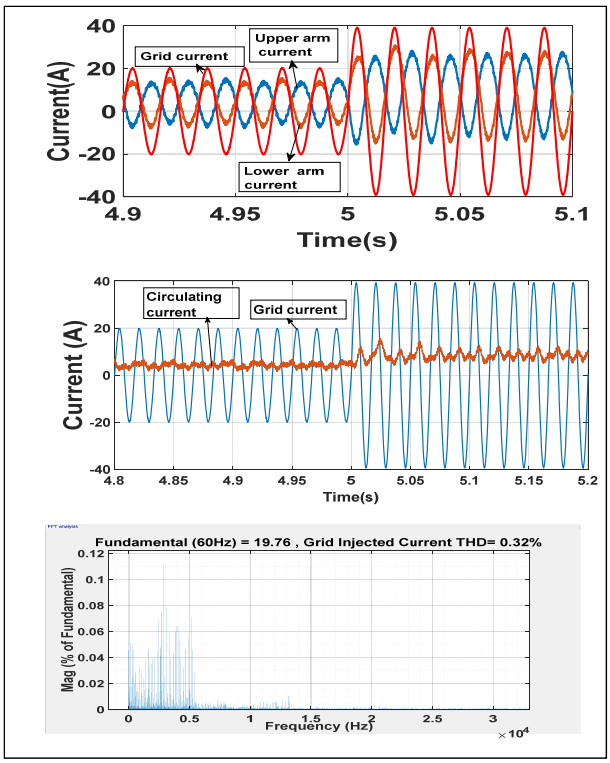

Figure 2.21 Current waveforms in upper arm, lower arm, load current, circulating current, and current THD during reference current variation from 20A to 40A and reference PF=0

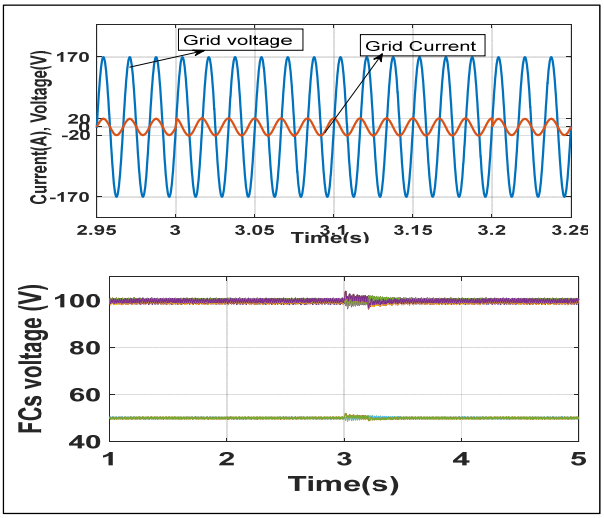

Figure 2.22 Grid connected waveforms, grid voltage and current during PF variations from 1 to 0 and again back to 1; and FCs voltage

2.6 Experimental Results

Two 3 kVA module prototypes of ZPUC5 inverter have been built. They are assembled based on the configuration of figure 2.3 to validate the performance of topology and voltage balancing control method. The control algorithm of voltage balancing integrated with modulation technique has been implemented on dSpace 1103 as real-time controller and switching pulses are sent to the ZPUC5 switches in lower and upper arms through the dSpace 1103 interface board. ZPUC setup for experimental test in the lab is shown in figure 2.23. The parameters are the same as table 2.7. Experimental results are categorized based on steady state and transient mode to prove the performance of topology and controller. Figure 2.24 shows the 9-L load voltage and current and capacitor voltages in the upper arm. DC source is 100 V and two upper capacitors and one lower capacitor in each module of ZPUC are balanced in 50 V and 25 V respectively and the load voltage is established in steps of 25 V as illustrated in figure 2.24.

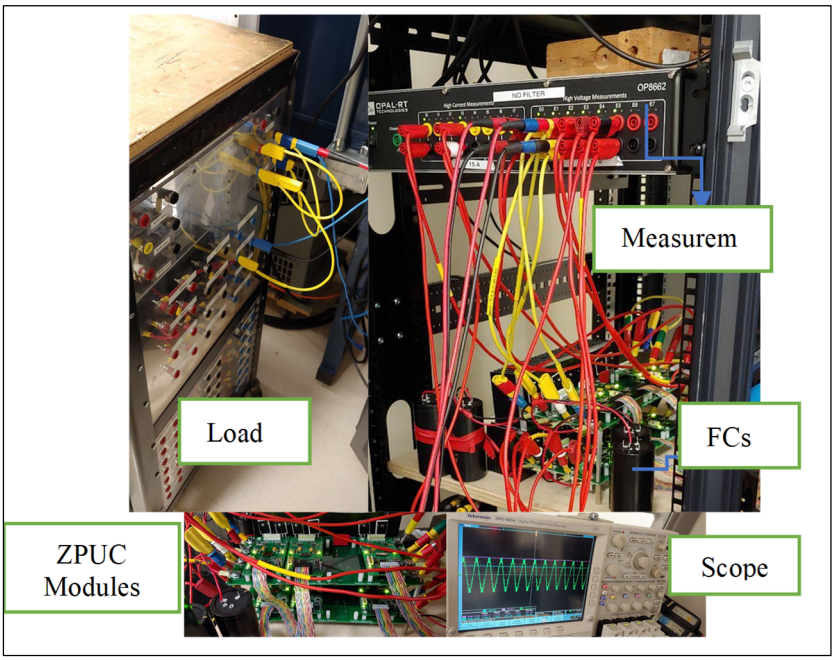

Figure 2.23 Experimental setup of the ZPUC multilevel converter

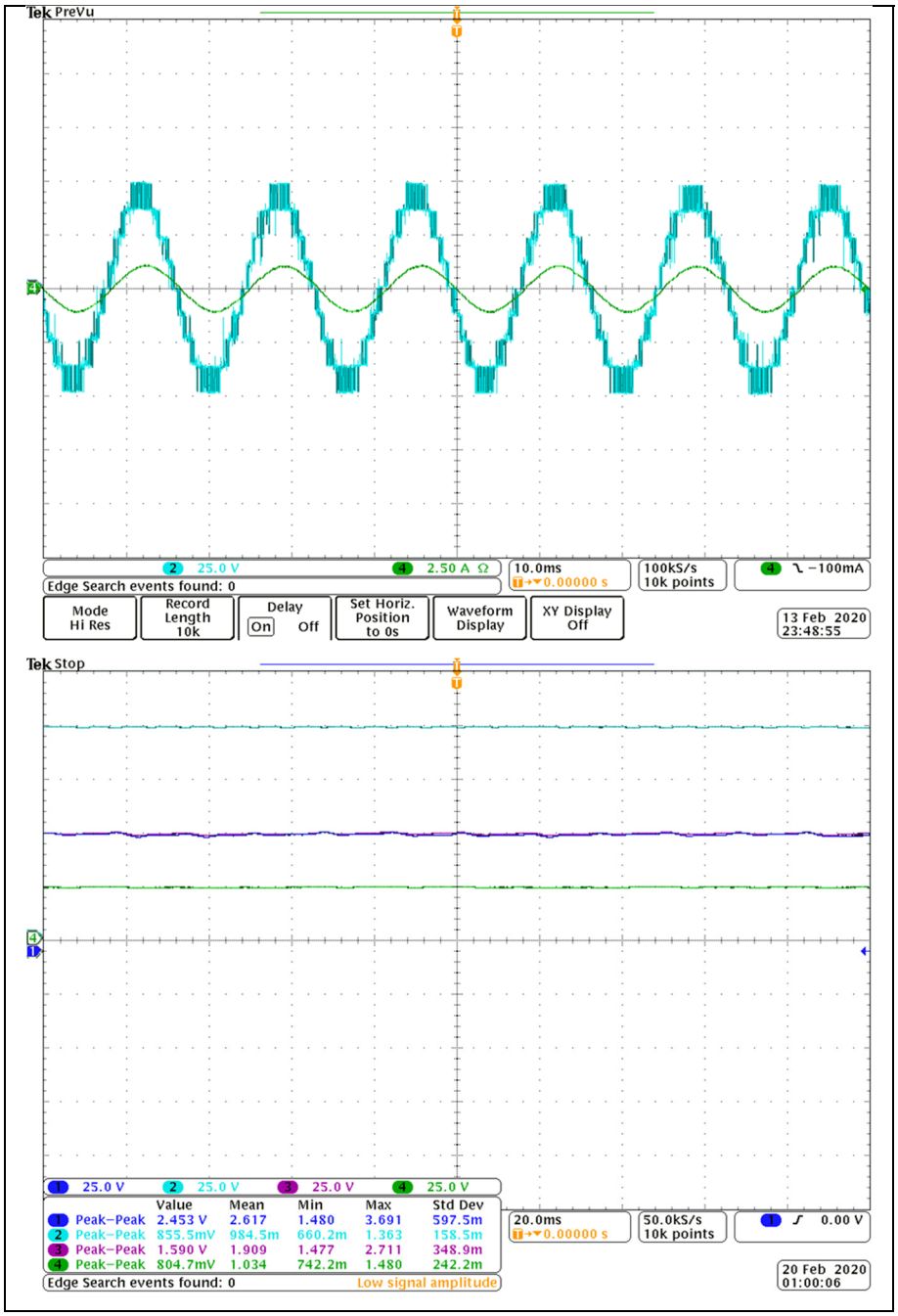

Figure 2.24 Load voltage, load current and capacitor voltage balancing

The capacitor voltage ripple for two upper capacitors in each state is less than 2.5% and for lower capacitor is about 1% that shows the performance of the topology and the control method.

Figure 2.25 shows the total harmonic distortion of ZPUC converter that is obtained through AEMC power analyzer which validates the lower THD due to its increased voltage levels. As a transient study, load is varied from 40 ohm to 20 ohm and then it comes back to 40 ohm to examine the performance of the topology during the load variation in the inverter.

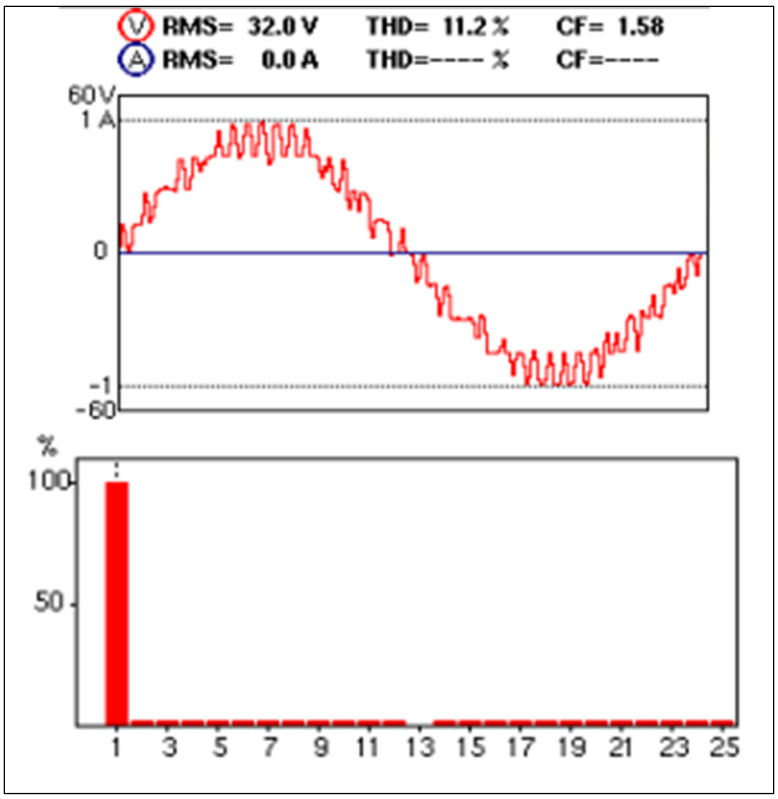

Figure 2.25 Total harmonic distortion of load voltage of ZPUC converter

Figure 2.26 shows that the load voltage is not varied due to the load variation which supports the performance of ZPUC converter in transient state. In addition, FCs voltages is depicted in this figure in which the DC value is constant that confirms the voltage balancing control method. Increase in the voltage ripple verifies the effect of the current load in voltage ripple based on equation 2.30.

Figure 2.27 shows the variation in DC link voltage source which is increased from 100 V to 150 V and then back to 100 V. It can be seen from figure 2.27 that the flying capacitor voltages

are balanced despite 50% changes in DC source which confirm the dynamic performance of the proposed voltage balancing control method.

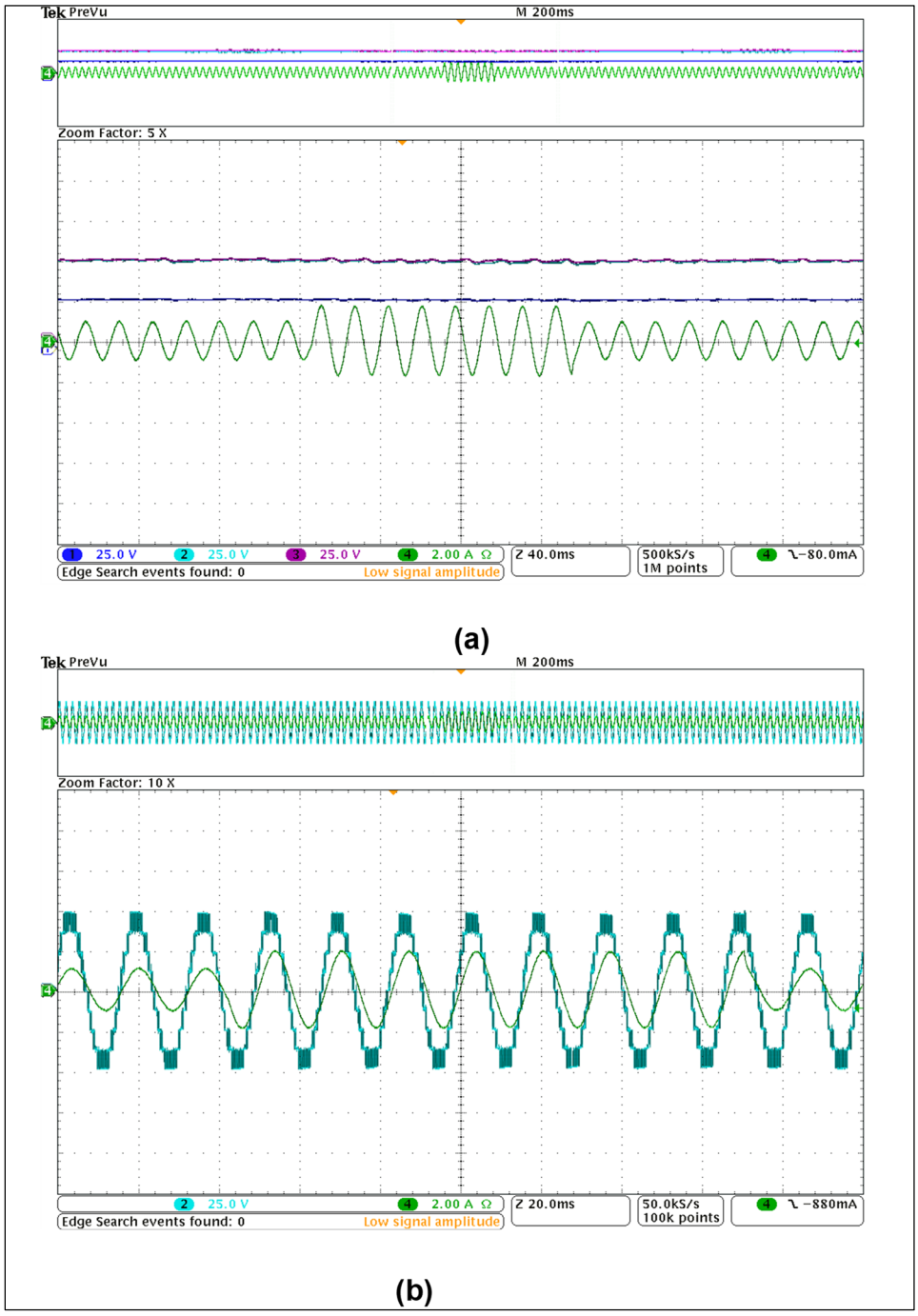

Figure 2.26 a) FCs voltages and load current b) Load voltage and load current during the load variation from 40 Ω-20Ω-40Ω

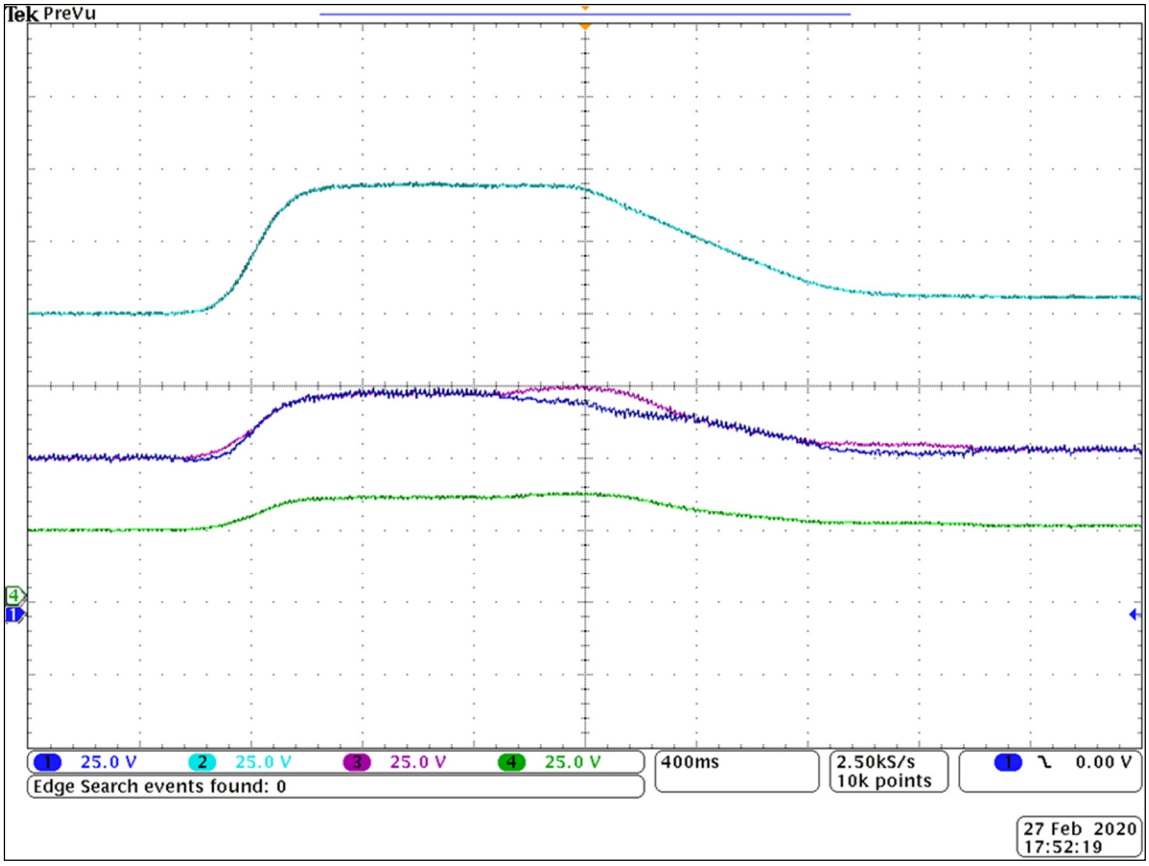

Figure 2.27 FCs voltage variation during the DC link voltage change Channel 2 (light blue wave is the DC link voltage), Channels 1 and 3 are the voltage of C1 and C2 in upper arm module, Channel 4 is the voltage of C3 at upper arm module

Furthermore, figure 2.28 shows the load voltage and current waveforms through mentioned DC source variation. This figure shows the achievement of ZPUC converter and proposed control method to generate the voltage and current waveforms with a remarkable quality during the transient state as well as the steady state. Finally, load voltage and current as well as capacitor voltages at C1 and C2 in upper arm in terms of changing the modulation index from 0.6 to 0.9 is shown in figure 2.29. ZPUC Converter generates 7-L waveform while modulation index is regulated in 0.6 and then it generates 9-L wave when modulation index is increased to 0.9. During these variations the voltage in the capacitors are still balanced and they are not changed that shows the performance and ability of converter to balance the voltages in FCs and consequently generating the high-quality output waveform.

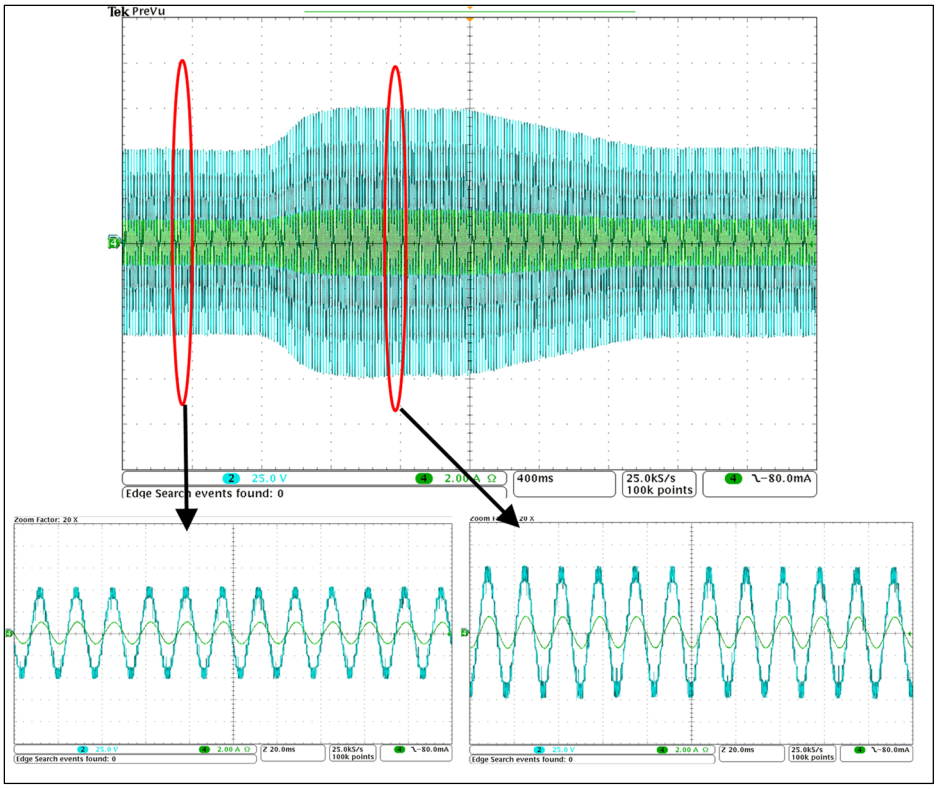

Figure 2.28 Load voltage and current during the DC source variation

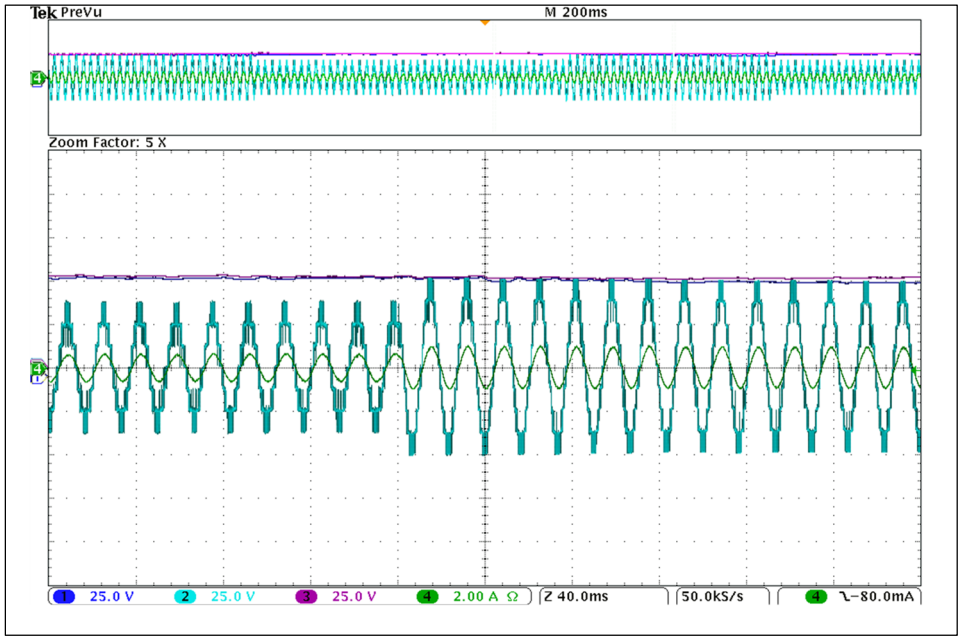

Figure 2.29 Load voltage, load current, voltage in capacitors C1 and C2 during the modulation index variation from 0.6 to 0.9

2.7 Conclusion

ZPUC topology is a new multilevel converter that has been proposed in this chapter. This topology can be utilized on rectifier or inverter modes as well as modular multilevel converters. Its application is motor drive, renewable energy integration to the grid, battery chargers, HVDC, STATCOM etc. As well, this topology could be a suitable alternative for multilevel converters in single-phase and three-phase system due to generating the high number of voltage levels, scalability and makes use of one DC source. This topology has some advantages compared to the other multilevel converters for single-phase and three-phase systems such as less component and switching devices, less power losses and more reliability. Voltage balancing in the capacitors are performed integrated with modulation strategy without any additional control loops. Appropriate voltage balancing algorithm for this topology has been presented in this chapter. Simulation and experimental results demonstrate that voltage regulation of three flying capacitors is tuned to their desired values and voltage across the load has been set to nine levels in steady states and transient modes.

CHAPTER 3

DEEP LEARNING-BASED VOLTAGE BALANCING INTEGRATED WITH HYBRID SPWM TO INCREASE VOLTAGE LEVELS IN ZPUC-MMC

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3.1 Abstract

In this chapter, a voltage balancing method based on deep learning integrated with the hybrid phase shift pulse width modulation (PS-PWM) and level shift pulse width modulation (LS-PWM) is employed to increase the voltage levels in ZPUC- modular multilevel converter (ZPUC-MMC) through one reference voltage. Voltage balancing on the flying capacitors (FCs) are carried out through three categories of deep learning method including 3-Layer Neural-Network, Fully Connected Neural Network, and Convolutional Neural Network which are trained based on the results of the simulation on ZPUC-MMC in steady state and it has been shown that the Convolutional Neural Network method with 100% accuracy is the more suitable to employ on voltage balancing on MMCs. The network is trained in terms of one reference voltage for upper and lower arms and signal carriers which select the appropriate switching states to balance the voltage in FCs. Moreover, through the proposed control method on ZPUC-MMC, the DC source voltage is divided among the submodules of the leg; while in all other types of MMCs such as half-bridge MMCs (HB-MMCs) and flying capacitor MMCs (FC-MMCs), it is divided among the submodules of the arms. A trained deep learning network based on the proposed hybrid strategy is implemented on the prototype of ZPUC-MMC on stand-alone mode to validate the performance of deep learning voltage balancing.

Keywords

ZPUC-MMC, modular multilevel converter, deep learning, PS-PWM, LS-PWM, voltage balancing.

3.2 Introduction

Multilevel converters have been recently commercialized by industries due to their advantages on the dv/dt reduction, lower size of the harmonic filters, lower common mode voltage, and efficiency improvement (Kouro et al., 2010).

Modular types of multilevel converters, MMCs, first are invented to use for high voltage DC current (HVDC) applications ("IEEE Recommended Practice for the Design of Reliable Industrial and Commercial Power Systems," 2007; Saeedifard & Iravani, 2010). Though, some advantages such as modularity, scalability, lower size of harmonic filters, and convenient maintenance make them an appropriate alternative for motor drive and power quality improvement applications (Akagi, 2011). However, voltage balancing, circulating current, and current control are the issues of MMCs which must be addressed for industrial applications (M. A. Perez et al., 2021).

Half-bridge (HB), full-bridge (FB), neutral point clamped (NPC), and flying capacitor (FC) are the well-known multilevel topologies that are used as submodules of MMCs (Solas et al., 2013a; Zheng et al., 2020). HB-MMC is the most well-known type which is used in industries. A novel topology which is called ZPUC-MMC has been proposed in (S. Arazm & K. Al-Haddad, 2020) to reduce the size of the HB-MMC for generating the same power and voltage level at the output waveform. Output voltage waveform level in HB-MMCs with N cells per arms through regular modulation and control techniques of voltage balancing is N+1. However, 2N+1 voltage level has been discussed in some literature through the implementation of the modulation techniques for upper and lower arms separately. This technique uses 2 reference voltages for upper and lower arms and N carrier signals for each arm.

In (Pérez-Basante et al., 2018), the authors implement the selective harmonic elimination (SHE) modulation control method on HB-MMC to generate 2N+1 voltage level. Although SHE modulation can reduce the power losses due to the lower switching frequency, it increases the voltage ripples of the FCs and it is complex to calculate the trigger angles. Ergo, this modulation is not general and would be applicable only for a low number of submodules and especially for medium voltage applications. Modified nearest level method (NLM) with two reference voltages that generate 2N+1 level in HB-MMC is also another type of lower switching frequency modulation which is simple and convenient in contrast to the SHE. However, due to the poor quality of the waveform, it would be suitable for high voltage applications where many numbers of submodules are required. Space vector PWM is also a digital modulation method that has already been used to generate 2N+1 voltage levels; however, it is not proper for the MMCs in high voltage applications due to the complexity of vector and related times calculations. In (Ronanki & Williamson, 2020) authors proposed 2N+1 output voltage levels through a single carrier which reduces the number of carrier signals which is appropriate to the digital control similar to the SVM. However, it requires two reference voltages for upper and lower arms.

PS-PWM is the most popular type of modulation which is utilized to generate the appropriate signals to generate either N+1 or 2N+1 output voltage levels in HB-MMCs. Moreover, this technique has been utilized in FC-MMCs with N cells per arm to generate 2N+1 output voltage levels as unified PWM. Authors in (A. Dekka et al., 2016) proposed 4N+1 output voltage level through PS-PWM and two reference voltages. In (Ronanki, Azeez, Patnaik, & Williamson, 2018) the hybrid modulation technique has been proposed to address the uneven switching frequency of the LS-PWM in HB-MMC to generate N+1 voltage levels. LS-PWM is also employed in many research articles to improve the quality of output voltage waveforms and voltage balancing. However, the unified LS-PWM can not be used for generating 2N+1 waveform and the carriers which have been used for upper and lower arms must be interleaved through an appropriate phase angle (McGrath, Teixeira, & Holmes, 2017; Mei, Xiao, Shen, Tolbert, & Zheng, 2013). In addition, authors in (S. Arazm & K. Al-Haddad, 2020) proposed

the PS-PWM to generate increased 8N+1 voltage levels. It is worth mentioning that all the literature that interleaves the upper and lower carriers through PD-PWM and PS-PWM used two reference modulating signals.

FCs of MMCs which play the role of DC capacitors in multicell cascaded converters must be controlled at the desired voltage levels with a minimum of voltage ripple. Voltage balancing is implemented on FCs through external controllers such as PI controllers or predictive control methods. However, using external controllers reduces the reliability of the converters. To cope with this problem, voltage balancing is carried out integrated with modulation techniques by sorting the values of the FCs voltages and selecting the lowest and highest cells to flow the current depends on the current direction. However, the complexity of these methods will be increased in high voltage applications where utilizing a high number of cells are inevitable (Y. Liu & Peng, 2020).

In this chapter, a hybrid LS-PWM and PS-PWM through one reference voltage for both upper and lower arm are used to generate 8N+1 voltage level at the output of ZPUC-MMC. Moreover, a deep learning-based voltage balancing integrated with modulation technique is proposed to resolve the complexity problem of the conventional method. The network including FCs voltages of lower and upper arms cells are trained using the different artificial neural networks (ANNs) in steady state conditions and then the deep learning-based balancer is used in transient and dynamic states and the simulation and experimental results verify the performance of the method.

This chapter is organized as follows: in section 3.3, 8N+1 increased voltage level through one reference voltage is discussed. Section 3.4 explains the approach of deep learning and establishing the networks through three methods of 3-Layer NN, FCNN, and CNN. In section 3.5, a comparison among the mentioned methods is carried out on ZPUC-MMC and the best method is introduced to take the experimental results. Finally, in section 3.6, the experimental results which are obtained based on the proposed methods are discussed.

3.3 Hybrid Carrier-Based PWM

Figure 3.1 illustrates ZPUC-MMC with the simplest ZPUC submodule which is capable to generate 5L across the terminal (S. Arazm & K. Al-Haddad, 2020). Hybrid PS-PWM and LS-PWM through a single modulating signal have been chosen to increase the voltage levels to 8N+1 across the load terminal of ZPUC-MMC. In other words, N submodules of ZPUC5 per arm in MMC configuration generate 4N+1 voltage level across the arm terminal that leads to generating 8N+1 across the load terminal; while, in HB-MMC and FC-MMC, N+1 and 2N+1voltage levels are generated across the load, respectively. However, they can generate 2N+1 and 4N+1 voltage levels at increased levels modes through 2 reference signals (A. Dekka et al., 2016).

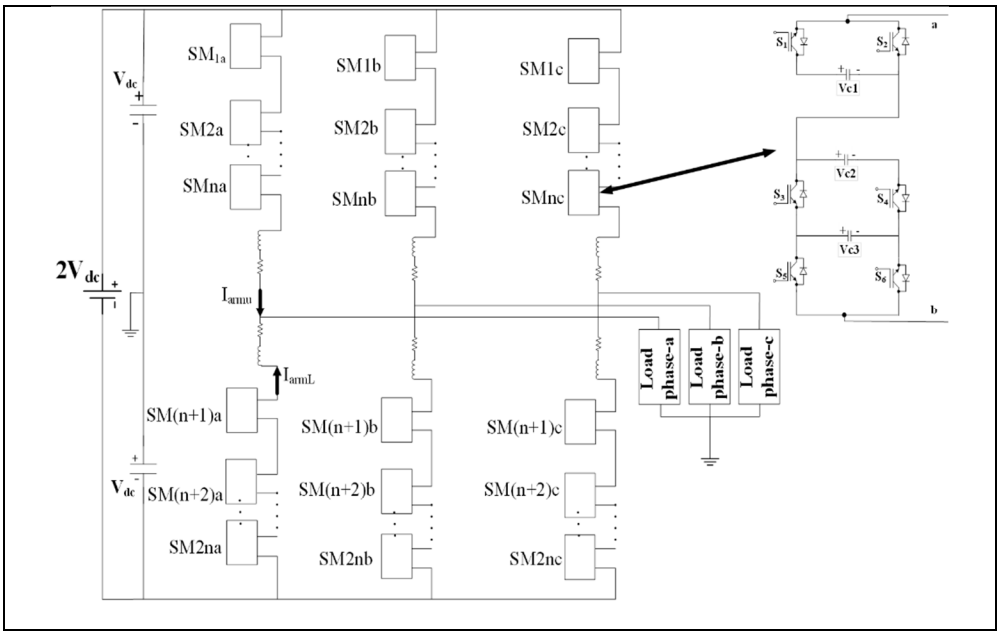

Figure 3.1 Three-phase ZPUC-MMC configuration

3.3.1 8N+1 Increased Voltage Level Algorithm

Figure 3.2.a and 3.2.b illustrates an LS-PWM technique with one reference voltage as well as carriers Cr_{ui} and Cr_{Li} that are related to the upper and lower arms, respectively. Figure 3.2.c

depicts the hybrid LS and PS modulation technique in which one modulating signal is modulated by the carriers Cr_{ui} and Cr_{Li}. It should be noted that the upper and lower carriers' waves are disposed of at 180 degrees. In this algorithm, 8N carriers are required for upper and lower arms so that carriers Cr_{u1}, Cr_{u2}, …, Cr_{u4n} modulate the reference voltage to trigger the switches of the upper arm and the same reference voltage are modulated by Cr_{L1}, Cr_{L2}, …, Cr_{L4n} to initiate the switching devices of the lower arm. Figure 3.3 depicts the control block diagram to implement on the ZPUC-MMC to generate 8N+1 across the load.

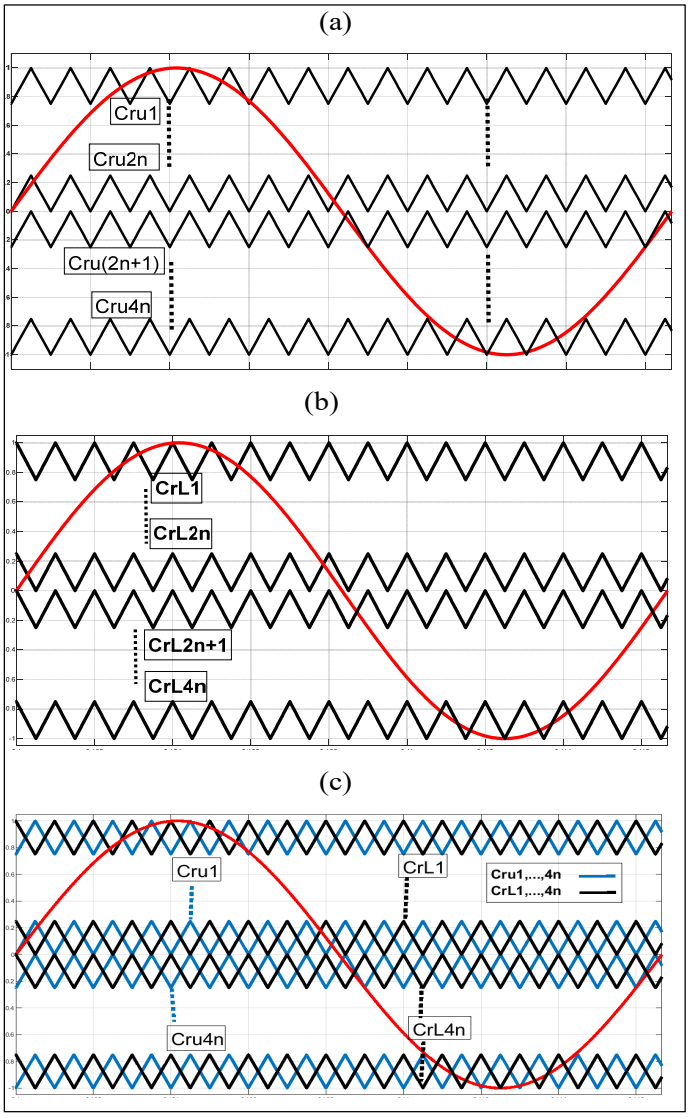

Figure 3.2 Carriers and reference signals attributed for upper and lower arms

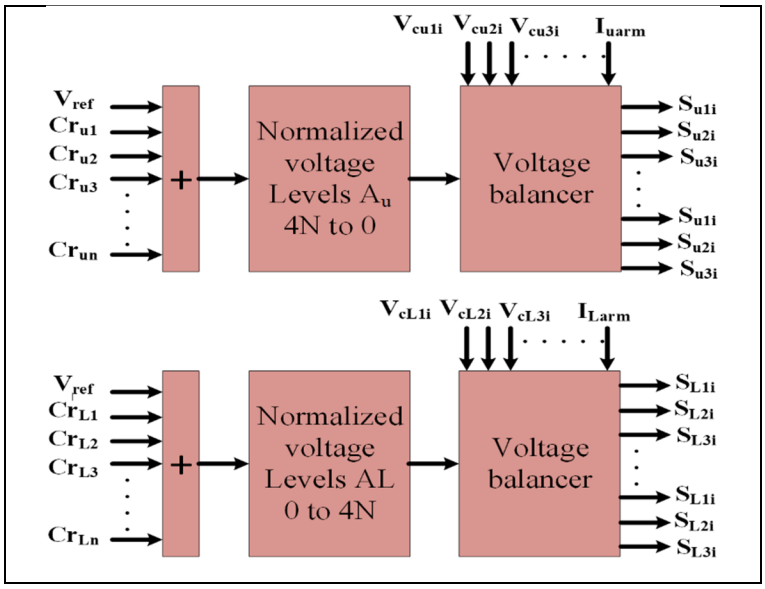

Figure 3.3 General control block diagram for upper and lower arms of ZPUC-MMC

The normalized level number in ZPUC-MMC in terms of N submodules per arm for each arm is given by:

$$A = 4(N - x) - y \tag{3.1}$$
$$A \geq 0$$
$$x = 0,1,\ldots,N$$
$$y = 0,1,2,3$$

Where x implies that the redundant switching states must be applied on which of the submodules and y shows how the redundant switching states 2 and 3, 4 and 5, and finally 6 and 7 are chosen for the selective submodule. The switching states for the submodule of ZPUC are listed in table 3.1.

Based on equation.3.1 the maximum normalized level is 4N when x and y are zero and it is reduced by increasing the x until it reaches zero. To have one reference voltage, as illustrated in figure.3.3, the function A, for upper and lower arms must be opposite. In other words, the switching states which are selected for the upper arm would be in the reverse manner rather than the lower one.

Table 3.1 Switching States of ZPUC Submodule

State	S1	S3	S5	Vab	Vab-5L
1	1	0	0	Vc1+Vc2	4E
2	1	0	1	Vc1+Vc2 –Vc3	3E
3	1	1	0	Vc1+ Vc3	3E
4	1	1	1	Vc1	2E
5	0	0	0	Vc2	2E
6	0	0	1	Vc2 –Vc3	E
7	0	1	0	Vc3	E
8	0	1	1	0	0

To illustrate, the switching states 1 and 8 for all submodules of the upper arm must be chosen to generate the maximum level 4N and 0 respectively. However, the switching states 8 and 1 must be selected for the lower arm. Energy in every submodule is calculated based on the energy storage in its three flying capacitors (FCs) that is given by:

$$E_{ui} = \frac{1}{2}C_{u1i}V_{cu1i}^2 + \frac{1}{2}C_{u2i}V_{cu2i}^2 + \frac{1}{2}C_{u3i}V_{cu3i}^2 \quad (3.2)$$
$$E_{Li} = \frac{1}{2}C_{L1i}V_{cL1i}^2 + \frac{1}{2}C_{L2i}V_{cL2i}^2 + \frac{1}{2}C_{L3i}V_{cL3i}^2$$

$$I_u(i) = sort(E_{ui}) \quad (3.3)$$
$$I_L(i) = sort(E_{Li})$$

Where E_{ui} and E_{Li} are the storage energy in every submodule of upper and lower arms. C_{u1i}, C_{u2i}, and C_{u3i} are the capacitances of three FCs in the submodule i^{th} at the upper arm, and C_{L1i}, C_{L2i}, and C_{L3i} are the capacitances of three FCs in the submodule i^{th} at the lower arm. V_{Cui} and V_{CLi} are their corresponding measured voltage. $I_u(i)$ and $I_L(i)$ demonstrate the arrays corresponding to the submodules Which are arranged in order from lowest to highest. The detailed voltage balancing integrated with modulation technique control based has already

been discussed in (S. Arazm & K. Al-Haddad, 2020) which two references voltages and PS-PWM have been employed. However, to train the voltage balancer function in this chapter hybrid PWM as well as single reference voltage has been used. The flowchart of voltage balancing is illustrated in figure 3.4 with the aim of deep learning training of voltage balancer. For instance, it is supposed that N and x are 4 and 2 respectively, it is corresponded to generate normalized level 7^{th} based on equation 3.1. As well, N shows that ZPUC-MMC generates 33 L across the single-phase load. To illustrate the flowchart, it is assumed that energy storage ascending sorting in 4 submodules of upper arms is [E_2, E_4, E_1, E_3]. If the upper arm current is positive, the switching state S_1 is selected for the submodule $(N-x-1)^{th}$ which in this example is E_2 (submodule 2) due to that N=4, x=2.

Switching states S2 to S7 as defined in the flowchart, are chosen for (N-x) that is the second index of sorting vector, E_4 (submodule 4), to be investigated based on their capacitor. voltage measurement. Finally, switching state S8 are selected for x submodules with the highest energy which is E_1 and E_3 (submodules 1, 3).

3.4 Deep Learning-Based Voltage Balancer

ANN has already been implemented on power electronic devices for several purposes such as model predictive control machine learning-based and optimization of design parameters (Dragičević, Wheeler, & Blaabjerg, 2019; Gardezi & Hasan, 2018). In (S. Wang, Dragicevic, Gao, Chaudhary, & Teodorescu, 2021) a deep learning ANN-based circulating current injection has been utilized to reduce the voltage ripples in FCs on MMCs due to the phase to phase ground fault current. In this chapter, a voltage balancing ANN-based is introduced to control the MMC without using the external control system. The voltage balancer machine learning which is trained based on the data in steady state are applicable for all transient, dynamic, and steady states. Indeed, in this section three deep learning methods are introduced as a potential of ANN voltage balancer to be trained by the steady states results. There is a voltage balancer at the heart of the MMC control system that receives normalized voltage level

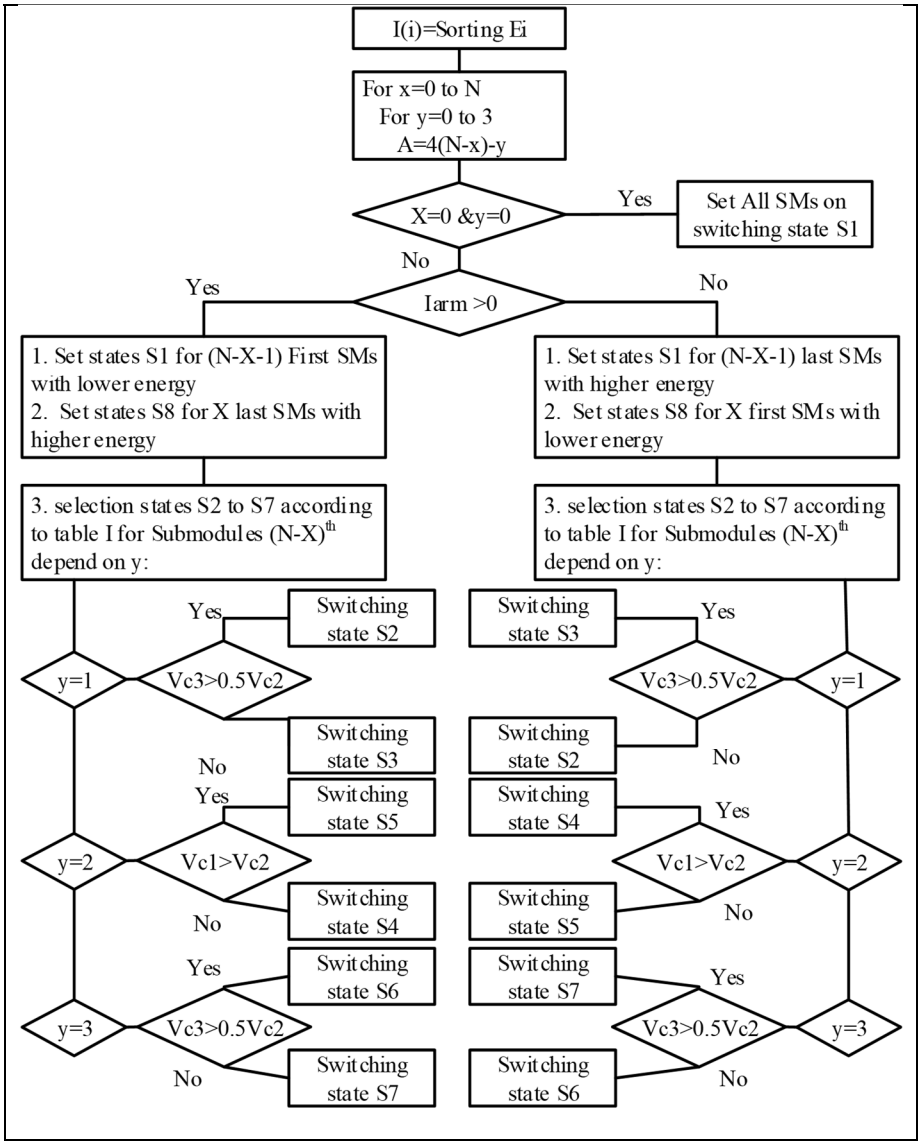

Figure 3.4 Voltage balancing algorithm for one arm of ZPUC-MMC

A_u and A_L, FCs voltages, and upper and lower arms current to estimate the correct value of states. Formally, the balancer could be defined as a function shown in equations 3.4 and 3.5.

$$[S_{L1}, S_{L2}, S_{L3}] = LowerArmVoltageBalancer(A_L, I_L, V_{CL1}, V_{CL2}, V_{CL3}) \quad (3.4)$$

$$[S_{L1}, S_{L2}, S_{L3}] = LowerArmVoltageBalancer(A_L, I_L, V_{CL1}, V_{CL2}, V_{CL3}) \quad (3.5)$$

Where S_{L1}, S_{L2}, and S_{L3} are lower switching devices states, A_L is the normalized voltage level at the lower arm, I_L is the lower arm current, and V_{CL1}, V_{CL2}, V_{CL3} are FCs voltages of the lower arm. The variables of the upper arm are indicated by U with the same definition as the lower arm. In this chapter, Deep Learning-Based is replaced by the traditional voltage balancer to trigger the switching states automatically. Thus, three deep learning methods including 3-Layer NN, FCNN, and CNN are employed to achieve this purpose. First, we describe how to collect data for training, and then three methods and their network architectures will be fully explained.

3.4.1 Data Preparation and Normalization

The first step in building a deep network is preparing good data for machine training. ZPUC-MMC is run in a steady state and all the mentioned variables, and their corresponding states are recorded. The run time simulation was about 3sec, and data includes 150,000 records. Unfortunately, the training result was unsuccessful, although the accuracy was over 98%. The key problem was the distribution of the variables. When the data were inspected, it was found that most of the values are around balanced voltages. Since the data was collected from a balanced state of the machine, the machine did not learn what decision should it make when it goes out of equilibrium. As a result, we needed to consider out-of-range values in the training phase and train the network with new values.

For this purpose, uniform distribution was not an excellent choice because out-of-range values rarely occurred and having an enormous amount of unused data would cost and slow down the training process. On the other hand, we needed large amounts of data around balance voltages with a small delta. Given these two points, a normal distribution would be the best choice. The capacitor voltages are firstly normalized to the range of [0, 1] by dividing them to Reference Voltage (Vref). Then the 100,000 samples of VCL1, VCL3 values were generated randomly with a normal distribution with a mean of 0.5 and a standard deviation of 0.1, and VCL2 values were generated randomly with a normal distribution with a mean of 0.25 and a standard

deviation of 0.05. The same process was repeated for VCU1, VCU2, and VCU3. The generated data was given to the running ZPUC-MMC, and the corresponding device states were recorded. The final training data are described as follows:

Lower Arm Balancer

Predictor Variables

$$\begin{aligned} &AL: 0 \le AL \le 4 \\ &IL: -1 \le IL \le +1 \\ &VCL1: \quad N(0.5, 0.1) \\ &VCL2: \quad N(0.25, 0.05) \\ &VCL3: \quad N(0.5, 0.1) \end{aligned} \tag{3.6}$$

Target Variables

$$\begin{aligned} &SL1: SL1 \in \{0,1\} \\ &SL2: SL2 \in \{0,1\} \\ &SL3: SL3 \in \{0,1\} \end{aligned} \tag{3.7}$$

Upper Arm Balancer

Predictor Variables

$$\begin{aligned} &AU: 0 \le AU \le 4 \\ &IU: -1 \le IU \le +1 \\ &VCU1: \quad N(0.5, 0.1) \\ &VCU2: \quad N(0.25, 0.05) \\ &VCU3: \quad N(0.5, 0.1) \end{aligned} \tag{3.8}$$

Target Variables

$$\begin{aligned} &SU1: SU1 \in \{0,1\} \\ &SU2: SU2 \in \{0,1\} \\ &SU3: SU3 \in \{0,1\} \end{aligned} \tag{3.9}$$

Next, several data preprocessing techniques were performed on the predictor variables. A common preprocessing technique in deep learning is zero-centering. With non-zero-center variables, parameter updates are only restricted to specific directions which in turn will make it difficult to converge. This phenomenon is known as the zigzag effect. So, we subtracted the value of AL and AU by 2. Also, because only the IL and IU sign was important in the system decision, all negative values of IL and IU were replaced by -1, and all positive values of IL and IU were replaced with +1. Finally, the difference between VC1 and VC2, VC2 and VC3 are computed, because the observations show that these differences are important for state determination, not the exact values of voltages. All preprocessing operations are summarized below.

Preprocessing Operators

$$AL = AL - 2 \_ s.t \_ AL \in \{-2, -1, 0, 1, 2\} \tag{3.10}$$

$$AU = AU - 2 \_ s.t \_ AU \in \{-2, -1, 0, 1, 2\} \tag{3.11}$$

$$IL = \begin{cases} +1 \_ IL \geq 0 \\ -1 \_ IL \leq 0 \end{cases} \tag{3.12}$$

$$IU = \begin{cases} +1 \_ IU \geq 0 \\ -1 \_ IU \leq 0 \end{cases} \tag{3.13}$$

$$DVCL13 = \begin{cases} +1 \_ VCL1 - VCL3 \geq 0 \\ -1 \_ VCL1 - VCL3 \leq 0 \end{cases} \tag{3.14}$$

$$DVCL23 = \begin{cases} +1 \_ VCL2 - VCL3 \geq 0 \\ -1 \_ VCL2 - VCL3 \leq 0 \end{cases} \tag{3.15}$$

$$DVCU23 = \begin{cases} +1 \_ VCU2 - VCU3 \geq 0 \\ -1 \_ VCU2 - VCU3 \leq 0 \end{cases} \tag{3.16}$$

$$DVCU23 = \begin{cases} +1\_VCU2 - VCU3 \geq 0 \\ -1\_VCU2 - VCU3 \leq 0 \end{cases} \quad (3.17)$$

The preprocessing graph operation is sown in figure 3.5.

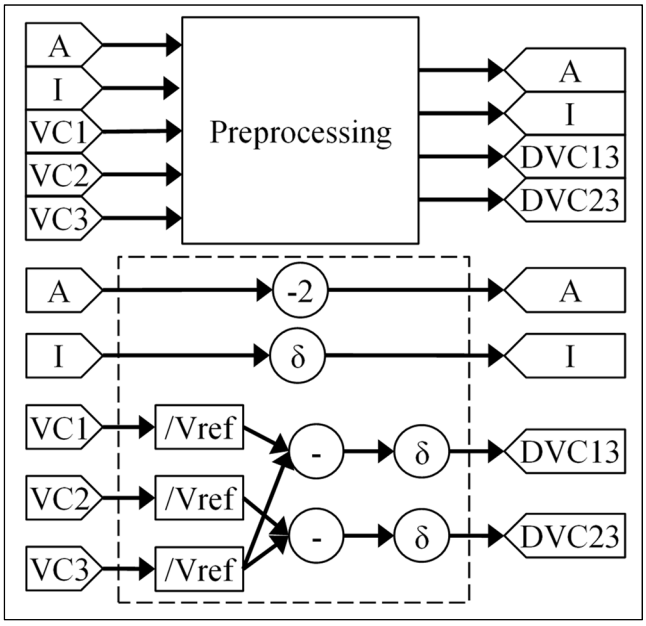

Figure 3.5 Preprocessing Module - $\delta(x > 0) = +1$ and $\delta(x < 0) = -1$

The six prepared training data used for the deep networks described in the next sections are summarized in table 3.2.

Table 3.2 Training Data Fields

#	**Predictor Variables**				**Target Variables**
1	AL	IL	DVCL13	DVCL23	SL1
2	AL	IL	DVCL13	DVCL23	SL2
3	AL	IL	DVCL13	DVCL23	SL3
4	AU	IU	DVCU13	DVCU23	SU1
5	AU	IU	DVCU13	DVCU23	SU2
6	AU	IU	DVCU13	DVCU23	SU3

3.4.2 3-Layer Neural Network

As a first approach, we used our pre-knowledge of the balancer to design a neural network. The neural network can estimate the value of a nonlinear function by learning from training data. A 3-Layer partially connected neural network is used to learn the Balancer function outcomes. All connections between layers and their initial weights came from our pre-knowledge about our system balancer. Although this network works well for the tested ZPUC-MMC, the big problem with this design is that it is not general and cannot be extensible to any other system. The weakness of this network is that it is designed based on our previous knowledge of a particular system. But its result demonstrates that the neural network can estimate the Balancer function very well and we can replace the balancer with a neural network. The architecture of the designed 3-Layer NN is shown in figure 3.6.

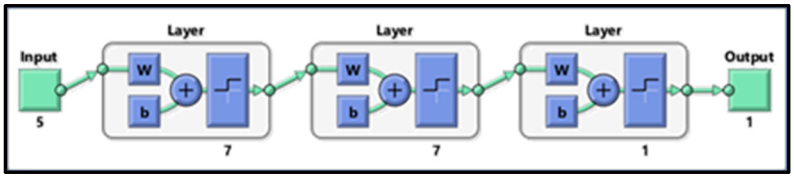

Figure 3.6 The architecture of the designed 3-Layer NN

For each layer the “Hard-Limit” activator function is selected because we need a binary output 0, 1 to set the devices’ states. The neural network has 5 inputs including A, I, VC1, VC2, VC3, and 3 hidden layers with 7, 7, 1 neuron, respectively. Six separate models for each switching states SL1, SL2, SL3, SU1, SU2, and SU3 are built as network output.

3.4.3 Fully Connected Neural Network

Since we wanted to build a general balancer that could be used on all MMC, the network designed for our ZPUC-MMC was not very efficient. A Fully Connected Network is a popular deep learning solution that can estimate almost any non-linear function. The major advantage of fully connected networks is that no special assumptions or knowledge need to be made about

the system. A fully connected layer offers learns from all the combinations of the features of the previous layer. So, we try to train a fully connected network with our predictor variable and predict the device states. The architecture of fully connected network is shown in figure 3.7. The input layer has 4 neurons after preprocessing on 5 input predictor variables. The network consists of 3 hidden layers with 10, 7, and 10 neurons, respectively. The output layer comprises 2 neurons of the binary device states value. The same architectures are applied for predicting six device states, SL[1-3] and SU[1-3].

To detect the nonlinear relationship between inputs and outputs, the RELU activation function is applied in each hidden layer. To overcome the internal covariate shift and vanishing problems, the Batch-Normalization [7] is used in each layer. A Dropout layer [8] has also been added to the network to prevent overfitting. The classification output layer uses the sigmoid activation function because we need a binary value for state output.

3.4.4 Convolutional Neural Network

Another common deep learning technique is Convolutional Neural Network. Fully connected networks do not scale up, because they use far too many parameters. CNNs are a much less flexible model compared to a fully connected network. CNNs can extract relevant information

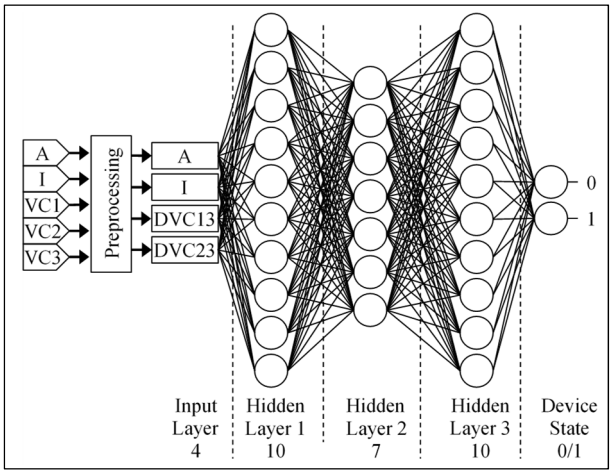

Figure 3.7 Fully Connected Network Balancer

at a low computational cost. We simulate our balancer with CNN as a third approach. The architecture of the implemented CNN is shown in figure 3.8.

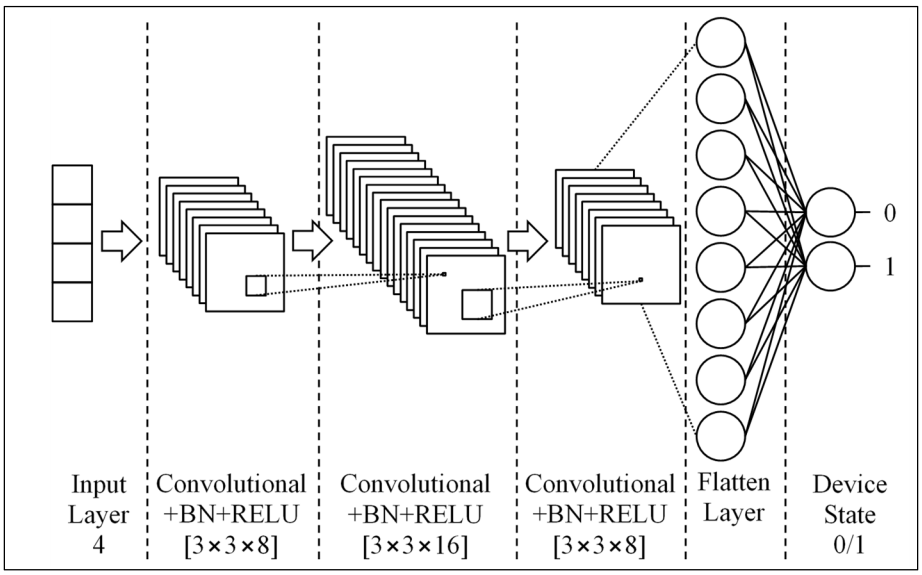

Figure 3.8 Convolutional Neural Network Balancer

The input layer is a 1 D vector of 4 elements after preprocessing on 5 predictor variables. The CNN consists of 3 convolutional layers with 8,16, and 8 filters of size 3×3, respectively. The stride parameter is 1, and the same padding is used for all layers. The output layer comprises 2 neurons of the binary device states value. The same architectures are applied for predicting six device states, SL [1-3] and SU [1-3]. Again, for the same reason mentioned in Fully Connected Network, the RELU activation function and Batch-Normalization layers are used on CNN. The classification output layer uses the sigmoid activation function because we need a binary value for state output.

3.5 Results

First, the voltage balancing shown in the control block diagram of figure 3.3 based on the flowchart of figure 3.4 is simulated to prepare the appropriate data to train the ANN. Thereafter, the voltage balancer block is replaced by ANN to implement on ZPUC-MMC. The

results demonstrate that deep learning methods learn the nonlinear behavior of the system simply and their results are highly close to the principal system.

3.5.1 Comparison of Deep Learning Methods

MATLAB R2020 and Simulink are used to train and test the networks. The system parameters for simulation and experimental tests are as follows: Vdc=100 V, C1,2,3=2 mF, fs=60Hz, Inductance=2mH, load=40 Ω, 20mH, sampling time= 50 μs. All networks have been trained with random data generated according to the mentioned distributions. 70% of the samples are used for training and the remain 30% of samples are used for validation. The real ZPUC-MMC data is used in test steps and our predicted states have been compared with the balancer output in the actual state-run. The results are averaged after 10 runs for each network with different 100,000 random inputs.

In table 3.3, the confusion matrices of 3-NN are shown. The confusion matrix is a table that shows the prediction error of each class. The obtained results are not very mind-boggling because the implemented 3-NN is trained base on our previous knowledge of a particular balancer, so it must be consistent with the data. The number of errors is very small, and the overall performance of the system shows 100% accuracy. In cases where the value of 99.99% is observed, it is due to the error of rounding numbers with an accuracy of two decimal places. As mentioned before, the main weakness of this approach is that it is made for a special case and cannot be generalized.

In contrast with 3-NN, the Fully Connected Network can be used to train any MMC with any configuration. Table 3.4 shows the confusion matrices of our implemented FCNN. Since FCNN is trained without any prior knowledge and because it is all-purpose, a higher error rate can be expected.

The overall performance of the FCNN shows more than 99.98% accuracy, which is very acceptable. The result of Simulink also confirms it as shown in figure 3.9.

Table 3.3 Confusion Matrix of 3-NN

SL1	0	1	Sum
0	49880	5	99.99%
	49.88%	0.01%	0.01%
1	1	50114	100.00%
	0.00%	50.11%	0.00%
Sum	100.00%	99.99%	99.99%
	0.00%	0.01%	0.01%

SL2	0	1	Sum
0	49880	5	99.99%
	49.88%	0.01%	0.01%
1	1	50114	100.00%
	0.00%	50.11%	0.00%
Sum	100.00%	99.99%	99.99%
	0.00%	0.01%	0.01%

SL3	0	1	Sum
0	49815	2	100.00%
	49.82%	0.00%	0.00%
1	4	50179	99.99%
	0.00%	50.18%	0.01%
Sum	99.99%	100.00%	99.99%
	0.01%	0.00%	0.01%

SU1	0	1	Sum
0	49885	5	99.99%
	49.89%	0.01%	0.01%
1	4	50106	99.99%
	0.00%	50.11%	0.01%
Sum	99.99%	99.99%	99.99%
	0.01%	0.01%	0.01%

SU2	0	1	Sum
0	49844	4	99.99%
	49.84%	0.00%	0.01%
1	4	50148	99.99%
	0.00%	50.15%	0.01%
Sum	99.99%	99.99%	99.99%
	0.01%	0.01%	0.01%

SU3	0	1	Sum
0	49883	1	100.00%
	49.88%	0.00%	0.00%
1	2	50114	100.00%
	0.00%	50.11%	0.00%
Sum	100.00%	100.00%	100.00%
	0.00%	0.00%	0.00%

As the last approach, we test the implemented Convolutional Network. Table 3.5 shows the confusion matrices of our implemented CNN. CNN results show 99.99% accuracy, which is more than FCNN. The error rate is so small that it will not affect balancer performance. Because the CNN structure makes our model easier to train, so the prediction accuracy is higher. The Simulink CNN result is shown in figure 3.10. In addition to the victory of the CNN over FCNN in the accuracy factor, the convergence time of the CNN is less than FCNN.

Table 3.4 Confusion Matrix of FCNN

SL1	0	1	Sum
0	49881	9	99.98%
	49.88%	0.01%	0.02%
1	6	50104	99.99%
	0.01%	50.10%	0.01%
Sum	99.99%	99.98%	99.99%
	0.01%	0.02%	0.02%

SL2	0	1	Sum
0	49888	10	99.98%
	49.89%	0.01%	0.02%
1	7	50095	99.99%
	0.01%	50.10%	0.01%
Sum	99.99%	99.98%	99.98%
	0.01%	0.02%	0.02%

SL3	0	1	Sum
0	49825	7	99.99%
	49.83%	0.01%	0.01%
1	10	50158	99.98%
	0.01%	50.16%	0.02%
Sum	99.98%	99.99%	99.98%
	0.02%	0.01%	0.02%

SU1	0	1	Sum
0	49852	8	99.98%
	49.85%	0.01%	0.02%
1	8	50132	99.98%
	0.01%	50.13%	0.02%
Sum	99.98%	99.98%	99.98%
	0.02%	0.02%	0.02%

SU2	0	1	Sum
0	49870	8	99.98%
	49.87%	0.01%	0.02%
1	10	50112	99.98%
	0.01%	50.11%	0.02%
Sum	99.98%	99.98%	99.98%
	0.02%	0.02%	0.02%

SU3	0	1	Sum
0	49809	11	99.98%
	49.81%	0.01%	0.02%
1	6	50174	99.99%
	0.01%	50.17%	0.01%
Sum	99.99%	99.98%	99.98%
	0.01%	0.02%	0.02%

According to figure 3.11, it can be seen that CNN has reached 100% training and validation accuracy much earlier. Also, note that the final amount of the loss function is less. This value is 0.0149 for CNN and 0.410 for FCNN, almost 28 times smaller. According to the results, Convolutional Neural Network has the best performance in accuracy and loss function among all designed approaches.

Table 3.5 Confusion matrix of CNN

SL1	0	1	Sum
0	49893	6	99.99%
	49.89%	0.01%	0.01%
1	6	50095	99.99%
	0.01%	50.10%	0.01%
Sum	99.99%	99.99%	99.99%
	0.01%	0.01%	0.01%

SL2	0	1	Sum
0	49824	5	99.99%
	49.82%	0.01%	0.01%
1	8	50163	99.98%
	0.01%	50.16%	0.02%
Sum	99.98%	99.99%	99.99%
	0.02%	0.01%	0.01%

SL3	0	1	Sum
0	49826	5	99.99%
	49.83%	0.01%	0.01%
1	7	50162	99.99%
	0.01%	50.16%	0.01%
Sum	99.99%	99.99%	99.99%
	0.01%	0.01%	0.01%

SU1	0	1	Sum
0	49841	5	99.99%
	49.84%	0.01%	0.01%
1	6	50148	99.99%
	0.01%	50.15%	0.01%
Sum	99.99%	99.99%	99.99%
	0.01%	0.01%	0.01%

SU2	0	1	Sum
0	49847	4	99.99%
	49.85%	0.00%	0.01%
1	8	50141	99.98%
	0.01%	50.14%	0.02%
Sum	99.98%	99.99%	99.99%
	0.02%	0.01%	0.01%

SU3	0	1	Sum
0	49815	5	99.99%
	49.82%	0.01%	0.01%
1	5	50175	99.99%
	0.01%	50.18%	0.01%
Sum	99.99%	99.99%	99.99%
	0.01%	0.01%	0.01%

3.5.2 Experimental results

The proposed voltage balancer controller with increased voltage levels integrated with hybrid modulation technique is implemented on 6 KVA single-phase ZPUC-MMC inverter to validate the performance of the proposed method. The controller is implemented on dSpace 1103 as a

real-time controller and the lower and upper arms switches are triggered by the dSpace interface.

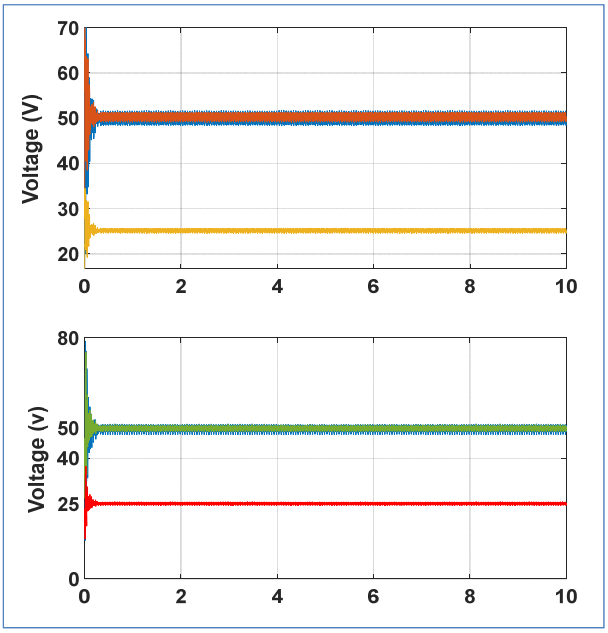

Figure 3.9 Simulink results for FCNN

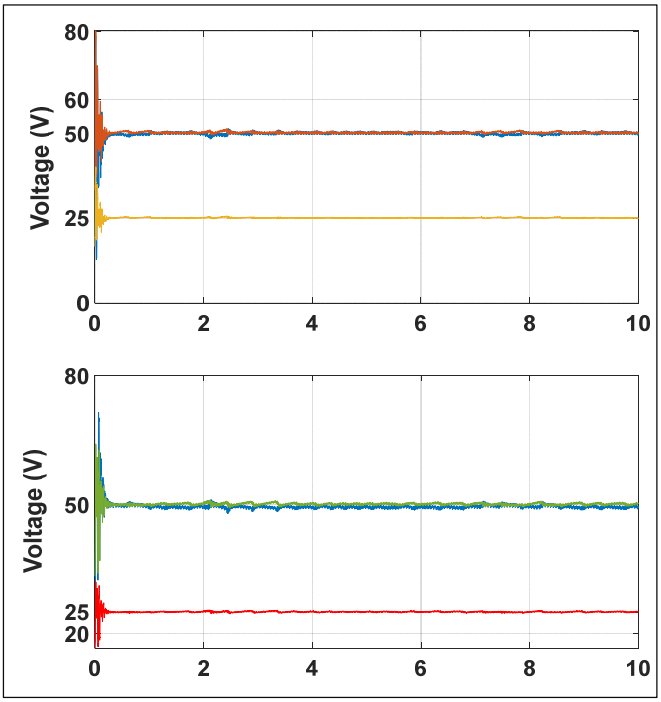

Figure 3.10 Simulink results for CNN

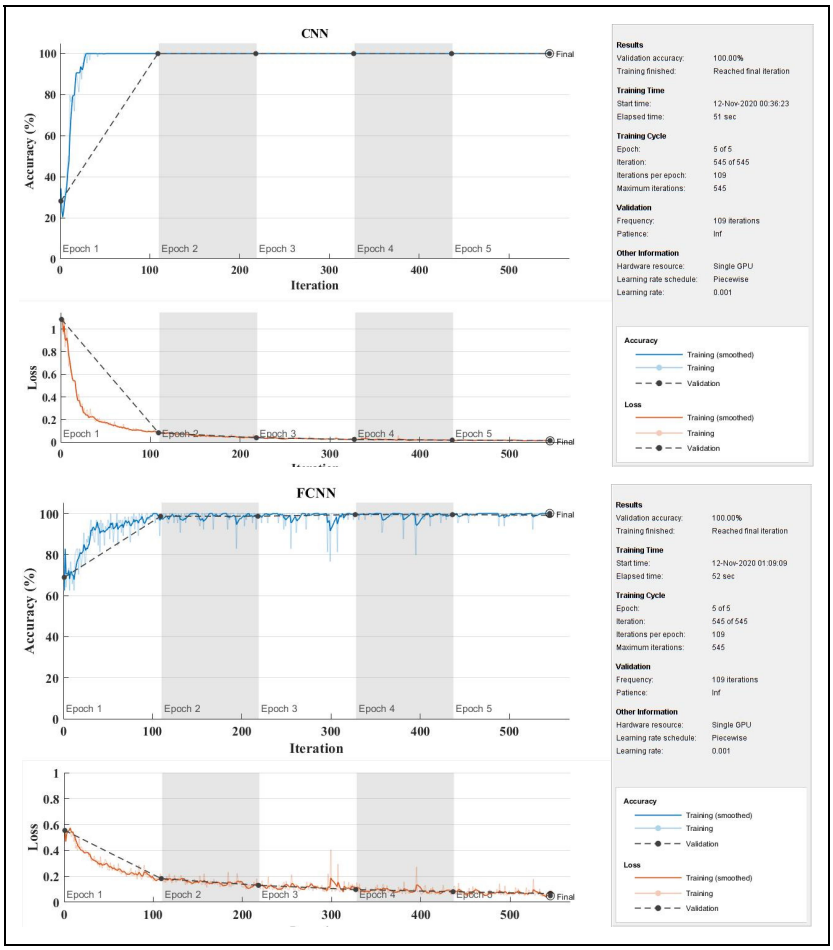

Figure 3.11 Training process CNN vs FCNN according to accuracy and loss function

Table 3.6 Simulation and Experimental Parameters of Stand-alone Mode

DC source voltage	100 V
Switching frequency	1000 Hz
System frequency	60Hz
Load	40 Ω, 20 mH
Buffer inductance	2 mH
Capacitor C1, C2, C3	2000 µF
Sampling time	46 µs

Figure 3.12 illustrates the nine-level voltage waveform which has been generated through one ZPUC submodule in each arm. Parameters which are used in experimental and simulation results is listed in table 3.6.

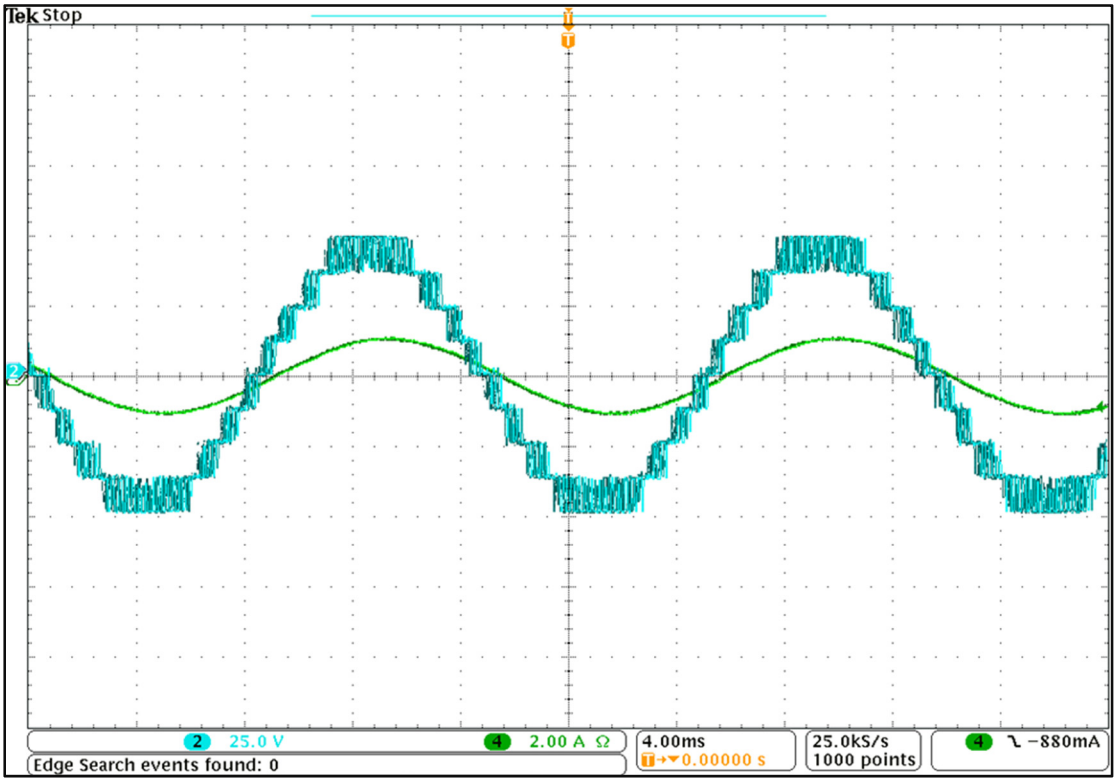

Figure 3.12 9L (8N+1) voltage level waveform (V) and load current (A)

Furthermore, figure 3.13 depicts the voltage balancing among the FCs. It can be seen that DC source voltage is divided between the submodules of one leg. The light blue shows the DC source voltage which is 100V, $V_{c1u,L}$=$V_{c2u,L}$= 50V, and finally $V3_{cu,L}$=25V. However, in FC-MMC and HB-MMC the DC source voltage is divided between submodules of one arm. As well, it must be said that the DC source voltage is divided among the submodules of the arms in MMCs which are presented in the literature until now.

To show the performance of the method on dynamic state, figure 3.14 shows that the voltages on flying capacitors are still balanced without variation when the load is changed in the range 40 Ω-20 Ω-40 Ω.

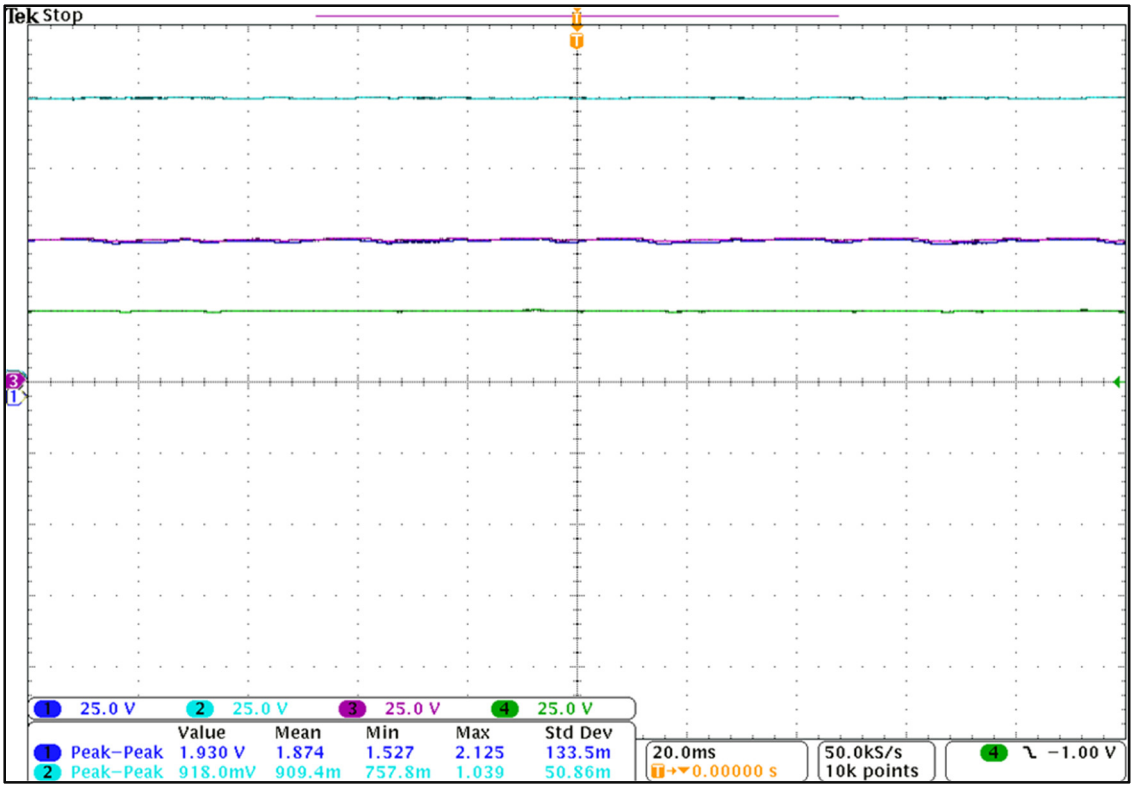

Figure 3.13 Flying capacitor voltage balancing on upper and lower arms

Figure 3.15 investigates the dynamic impacts of DC source variation on voltage balancing. DC source is changed from 100V to 150V and then it comes back to the 100V. Voltages of upper and lower FCs follow exactly the source voltage variations.

Figure 3.16 shows that the 9L (8N+1) voltage is generated before, during (transient), and after the variation so that the voltage in each step (level) corresponds to the voltage in the flying capacitor VC3.

Figure 3.17 demonstrates that the FCs voltages are constant all during the modulation index which verifies the performance of the control method.

Finally, table 3.7 shows one comparison among two well-known commercialized MMCs and ZPUC-MMC when an increased level is considered for all of them.

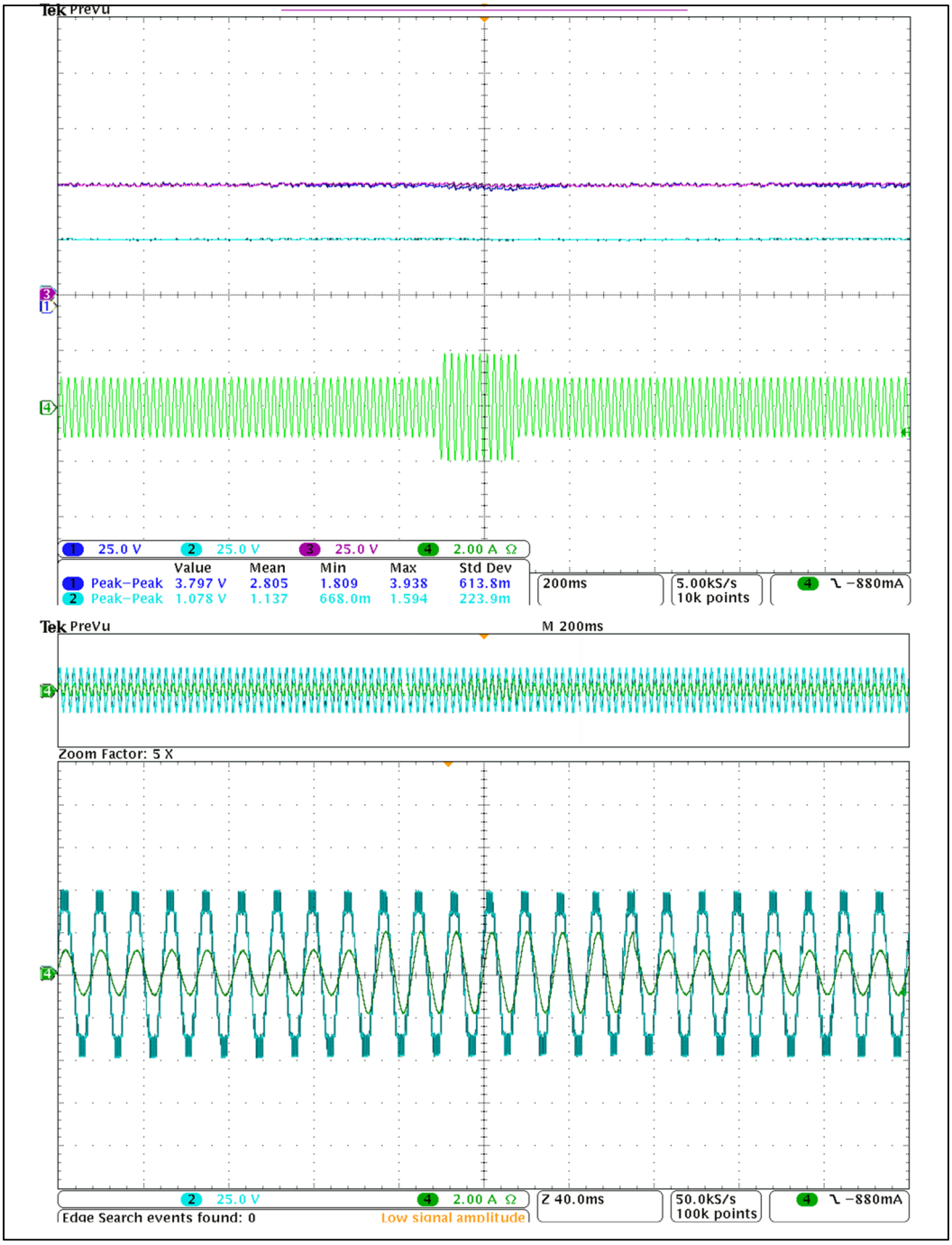

Figure 3.14 Load Voltage, load current, and voltage balancing during load variation in the range 40 Ω-20 Ω-40 Ω

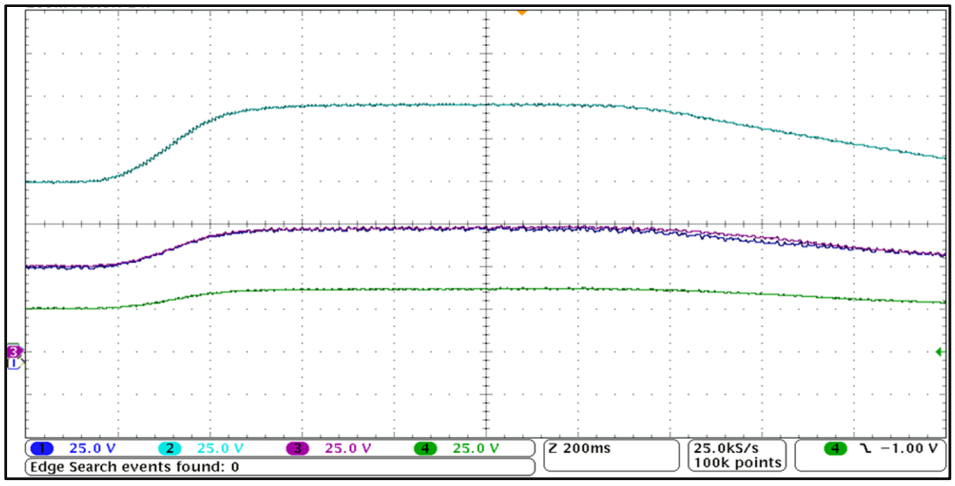

Figure 3.15 FCs voltages on upper and lower arms during the DC variation in range 100V-150V-100V

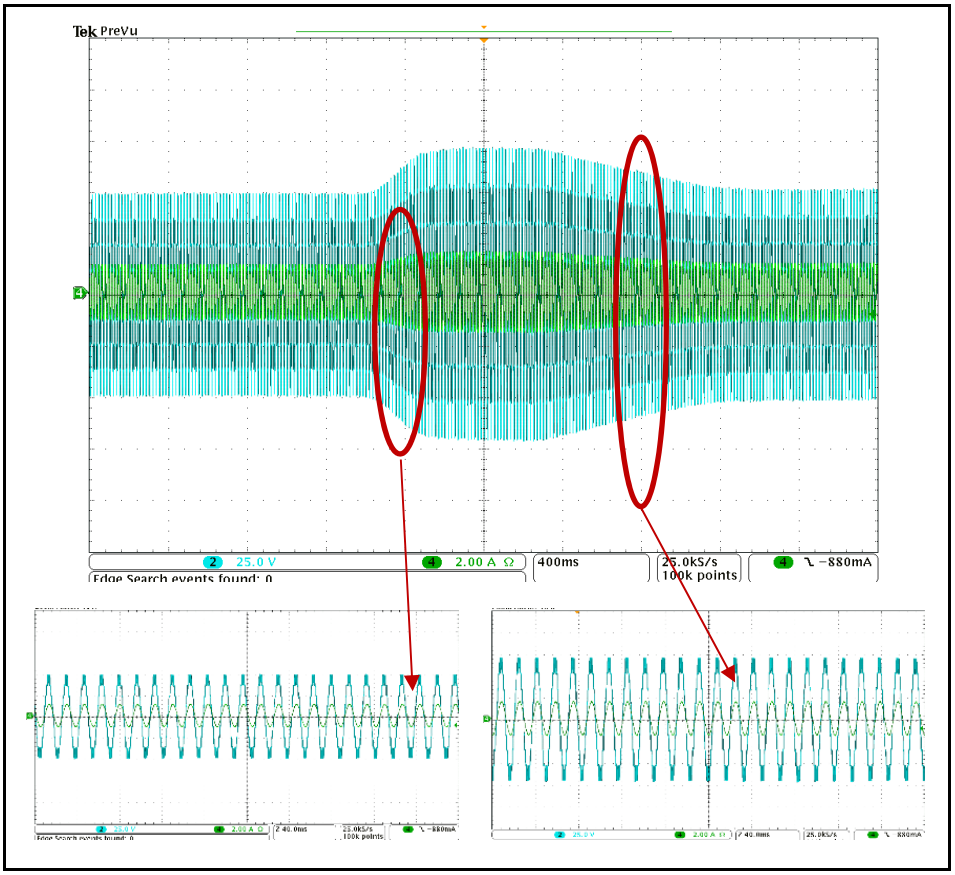

Figure 3.16 Output voltage and load current during the DC variation

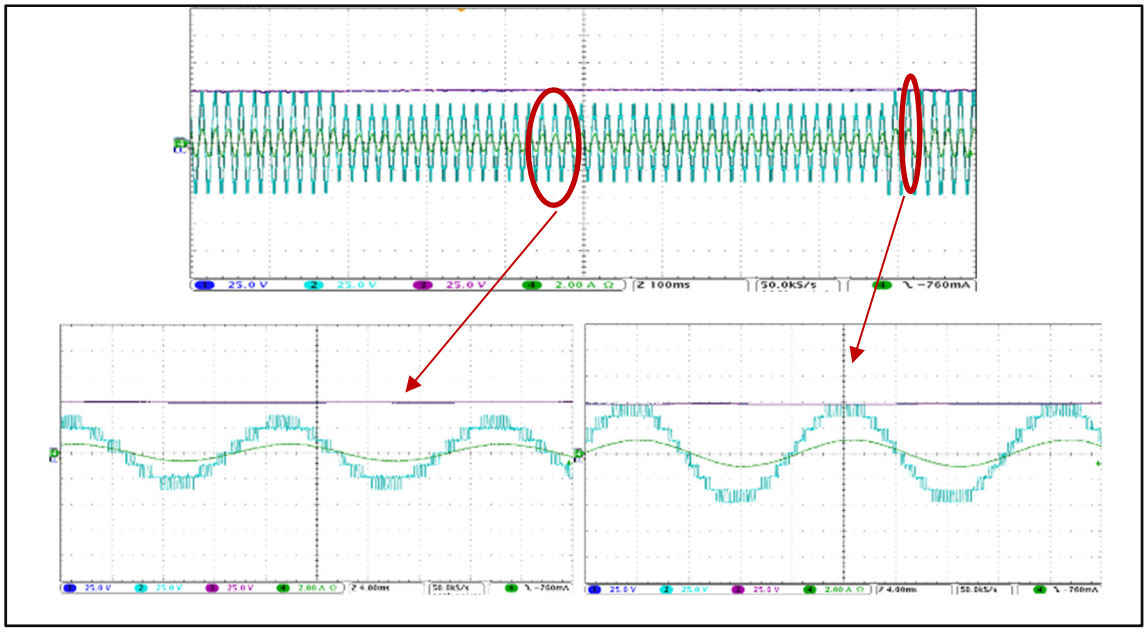

Figure 3.17 Voltages of FCs, output voltage and load current during modulation index change (0.95-0.6-0.95)

Table 3.7 Comparison Among the MMCs for Single-Phase 9L Waveform Generation with N Submodules per Arms (Vdc=100V)

	N	**Switching devices**	**Flying capacitors**	**Voltage dividing**
FC-MMC (4N+1)	2	16	8	VC1=50V, VC2=25V
HB-MMC (2N+1)	4	16	8	VC=25V
ZPUC-MMC (8N+1)	1	12	6	VC1=50V, VC2=25V

3.5.3 Conclusion

This chapter presents a hybrid modulation technique integrated with the deep learning voltage balancing without using the external control system to achieve the increased voltage levels. Obtaining more voltage level waveform through the same devices makes the lower THD and higher power quality which is advantageous. In contrast to the literature in which two reference signals is used to increase the voltage levels, in this study hybrid modulation technique through one reference voltage is employed to train three categories of deep learning method including 3-Layer Neural-Network, Fully Connected Neural Network, and Convolutional Neural Network. It is shown from the simulation results that the Convolutional Neural Network method is the most suitable to implement on ZPUC-MMC. Although the deep learning voltage balancer is trained in a steady state which reduces the volumes of data and run-time, it has a high performance in dynamic states as well. Finally, this chapter shows that in contrast to the other popular MMCs the DC sources are divided among one leg in ZPUC-MMC which leads to the use of lower components counts with the same rating values compared to its counterparts.

CHAPTER 4

A NOVEL SINGLE DC SOURCE THREE-PHASE WYE PACKED U-CELL (Y-PUC) CONVERTER

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4.1 Abstract

A new configuration of three-phase Wye Packed U-cells (Y-PUC) with a single DC source is proposed in this chapter. In fact, this configuration represents a single DC source modular three-phase PUC converter. The DC source on PUC topology is replaced by a flying capacitor to obtain a suitable submodule. Moreover, the modularity of the Y-PUC configuration makes it an appropriate alternative for MMC applications. Furthermore, the proposed structure is an advantageous configuration for high voltage applications such as high voltage direct current (HVDC) transmission lines with the capability of DC fault handling. All PUC topologies such as PUC5, PUC7, PUC9, PUC15 can be replaced in the modules of this proposed single-phase and three-phase configuration to multiply the load voltage levels for improving the output waveform. Active voltage balancing technique through carrier-based modulation is applied. System modeling and operating sequences are developed. Simulation and experimental results are presented and discussed to validate the performance of the proposed structure.

Keywords

Multilevel converter, Y-PUC converter, PUC-MMC, three-phase PUC converter, Single DC source, Ungrounded Double star, voltage balancing, circulating current, SPWM.

4.2 Introduction

Nowadays, Multilevel type of converters are used in several industrial applications such as transportations including electrified railway, motor drives, electrical vehicles charging stations (Abu-Rub, Holtz, Rodriguez, & Baoming, 2010; Akagi, 2017), as well as in renewable energy integration to the grid such as wind farms and photovoltaic plants (Bin Wu & Narimani, 2017b). Moreover, these converters have found application in power systems at both transmission and distribution levels namely power quality devices, STATCOM, static Var compensator (SVC), UPQC and active filters (H. M & Bina, 2011; Kouro et al., 2010). Higher-voltage levels and consequently lower THD, lower dv/dt as well as lower switching frequency are the main characteristics and advantages of multilevel converters topologies (J. Rodriguez et al., 2002).

Cascaded H-bridge (CHB), Flying Capacitor (FC), neutral point clamped (NPC), active neutral point clamped (ANPC) are the best-known multilevel converters (MLCs) that has been commercialized (T. A. Meynard & H. Foch, 1992; Nabae et al., 1981; Bin Wu & Narimani, 2017b). Hybrid MLCs (HMLCs) are presented in order to produce more voltage levels for applications such as motor drives. Reducing the total harmonic distortion (THD) and wave propagation over long cable is one of the technical specifications of motor drives which must be met by the drive's manufacturer. Although increased voltage levels are produced through the cascading of the popular topologies of MLCs, more DC sources are inevitably used to make the structure operational (Abarzadeh & Al-Haddad, 2019; Gao & Lu, 2018). This drawback would be managed by modular multilevel converters (MMCs) which made up of series topologies to divide the voltage among the devices when one DC source is required (Lesnicar & Marquardt, 2003). Half Bridge (HB), Full Bridge (FB), FC and NPC are the topologies used mainly as a sub-module on MMC structures.

HBs that are the simplest single-phase converter including two switching devices and one auxiliary capacitor have often been employed as a submodule in MMCs (C. Liu et al., 2020; Saeedifard & Iravani, 2010). However, due that they are the unipolar converters, the switching

devices cannot block the DC fault current, and they require the external DC circuit breaker. Against the AC circuit breakers which are common technology, some issues in DC circuit breakers manufacturing, such as losses, fault clearing time, arcing time are still the matter of controversy. (Bucher, Walter, Pfeiffer, & Franck, 2012). To address this problem and to handle the DC fault current, full-bridge (FB) converter which is a bipolar multilevel converter is utilized as a submodules of MMCs (FB-MMCs) (Zheng et al., 2020). In other words, FB-MMCs are capable to clear the DC short circuit fault through their switching device blocking, without using the external DC breakers (Adam & Davidson, 2015). However, the number of switching devices would be twice compared to HB which increase the power loss, the cost and bulkiness of the system. FB-MMCs are the most common alternatives for HVDC transmission lines system due to the high probability of pole to pole or pole to ground faults (Siemens, 2016). FCs have been introduced as submodules in MMCs for medium voltage motor drive application (Du, Wu, & Zargari, 2017; Du, Wu, Zargari, et al., 2017). It should be pointed out that, the number of switching devices in FC-MMCs are identical to HB-MMCs for generating the similar voltage level at the output, while the former is not as convenient as latter. NPCs are not suitable for application of MMCs due to the unbalance voltage balancing in auxiliary capacitors (Solas et al., 2013a, 2013b). However, NPC-MMC and FC-MMC cannot handle the DC fault current. ZPUC-submodule has been proposed in (S. Arazm & K. Al-Haddad, 2020) to reduce the size of the MMCs through reduction of the number of active switches and auxiliary capacitors to generate more voltage levels. This topology reduces the size of the converter more than half of the HB-MMC. However, it can not block the DC fault breaking current. Authors in (Adam et al., 2017) introduce the new submodule that can be replaced by the FB to reduce the total losses through switching devices reduction. Moreover, cross connected (CC-MMC) is another bipolar converter with the capability of DC fault clearing. In this topology, two half-bridge cells are connected through two isolated gate bipolar transistors (IGBTs) (Nami et al., 2013). Three-level converter for MMC submodule (TL-MMC) is a topology with a full DC fault blocking capability in which two HB cells are connected with clamped circuit with two switches and two clamp diode (R. Li, Fletcher, Xu, Holliday, & Williams, 2015). Clamp-Double-Submodule (C-DSM) has been proposed by Marquardt to address the DC fault clearing problem. This clamp-double (CD-MMC) requires two diode

clamp, 5 IGBT, and two flying capacitors with the aim to lower losses compared to FB-MMC (Marquardt, 2010). It should be noted that all the references in (Adam et al., 2017; R. Li et al., 2015; Marquardt, 2010; Nami et al., 2013) propose the topologies with the capability of DC fault handling with lower devices compared to FB-MMCs. Hybrid of these bipolar topologies with the unipolar topologies are also the solution to reduce the power losses and cost of the MMCs in overhead line HVDC applications (Cui & Sul, 2016; Nguyen, Hosani, Moursi, & Blaabjerg, 2019; Oliveira & Yazdani, 2017; Zeng, Xu, Yao, & Williams, 2015).

Bipolar PUC converter topology is a MLC with the minimum counts of power semiconductor components as well as the capacitors to generate a given voltage levels in comparison with its counterparts (Kamal Al-Haddad et al., 2016). This topology generates 5 or 7 voltage levels depends on the voltage balancing method (Vahedi & Al-Haddad, 2016b; Vahedi et al., 2016). Regarding the complexity of voltage balancing control in PUC7 (Ounejjar et al., 2011), the authors investigate different modulation methods to balance the capacitors voltage as to generate 5L without the use of sensors and feedback control loops (S. Arazm et al., 2018b).

One of the main drawbacks of PUC topology is that it is not easy implementable for multiphase system and as a modular way since it requires additional isolated DC sources. To prevail over this problem, a double star configuration of bipolar PUC5 topology with the capability of DC fault handling is proposed in this study so that it could be operated as a modular single or three-phase system with one main DC bus voltage. Proposed topology and configurations are suitable to implement on high-power and high voltage application through its capability to operate in series and parallel modules of PUC such as HVDC system. In other words, this configuration can be applied as MMC (PUC-MMC) through its ability to add more modules in each leg. PUC-MMC is a reduced components counts MMC with DC fault blocking capability. An algorithm for Voltage balancing integrated with SPWM is proposed in this project to regulate the voltage on flying capacitors without using the control system. DC fault current handling of PUC-MMC is elaborated in this chapter. Single DC source, modularity, and DC fault current handling are the principal features of proposed configuration.

The outline of this chapter is organized as follows: In section 4.3, single DC source single-phase and three-phase proposed Y-PUC configuration is explained and the control method on modified module of PUC is discussed. Switching states and voltage balancing integrated with PS-PWM is also explained in this section. Finally, the simulation and experimental results are illustrated and discussed in section 4.4 aimed to validate the proposed configuration and control method.

4.3 Topology Description and Analysis

A modular Y-PUC converter topology is illustrated in figure 4.1 in which a PUC converter is located as a submodule (SM). This configuration, not only address the problem of isolated DC source requirements in three-phase PUC for medium voltage applications, but also, is an instrumental MMC with the capability of DC fault handling in high voltage applications such as HVDC.

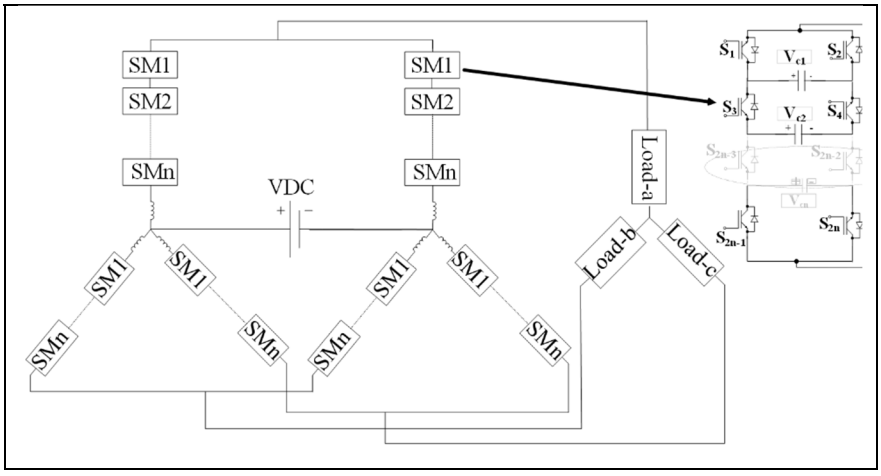

Figure 4.1 Single DC source three-phase Modular Wye Packed U-Cell (Y-PUC) Converter

In proposed configuration the single DC source double star, Y-PUC can be connected to the three-phase load or to the grid. Figure 4.2 shows a single-phase representation in which the neutral point is constructed by midpoint of two DC link capacitors. DC link could be either grounded directly or connected to the load as four wire connections. However, in three-phase

system this point is made naturally, and DC link capacitor is not required unless for direct grounding system.

4.3.1 Switching States and Voltage Balancing in Single Module of PUC5

Generalized PUC converter as shown in figures 4.1 and 4.2 can be located in each submodule (SM). Figure 4.3 shows a simplest type of PUC converter which is called by PUC5 or PUC7

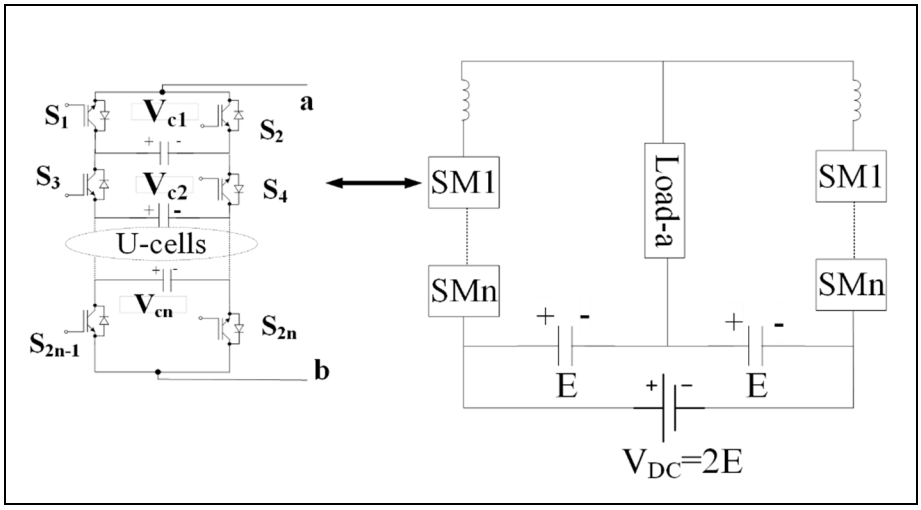

Figure 4.2 Single Phase of Proposed Configuration of PUC Converter

depend on the generated voltage level. PUC5 topology with redundant switching states that generates a 5L waveform is used as a SM of Y-PUC in this study. In this section, the topology and switching states as well as the charge and discharge conditions of the flying capacitors (FCs) are explained. Switching states of simple module of PUC converter with two flying capacitors are listed in table 4.1 in which output waveform could be 5-L when VC1=2VC2. The voltage equation Vab across one module of PUC as a function of the switching states S1, S2, S3 and flying capacitors voltages VC1 and VC2 is given by:

$$V_{ab} = V_{c1}(S_1 - S_3) + V_{c2}(S_3 - S_5) \tag{4.1}$$

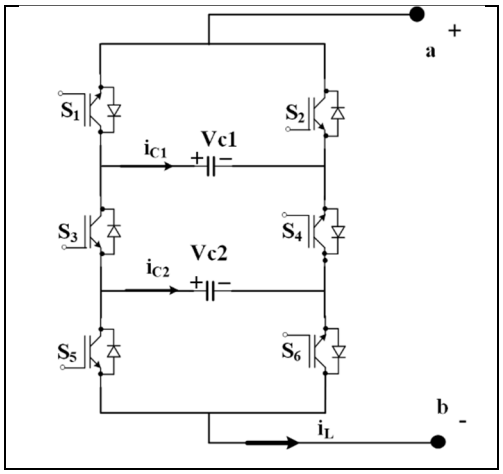

Figure 4.3 PUC topology with two flying capacitors as a SM in Y-PUC

Table 4.1 Switching States of PUC5 Converter

State	S1	S3	S5	Output Voltage	i_{C1}	i_{C2}	$i_L>0$ C1 C2	V_{ab} PUC5
1	1	0	0	$+V_{C1}$	i_L	0	↑ -	2E
2	1	0	1	$+V_{C1}-V_{C2}$	i_L	$-i_L$	↑ ↓	E
3	1	1	0	$+V_{C2}$	0	i_L	- ↑	E
4	1	1	1	0	0	0	- -	0
5	0	0	0	0	0	0	- -	0
6	0	0	1	$-V_{C2}$	0	$-i_L$	- ↓	-E
7	0	1	0	$-V_{C1}+V_{C2}$	$-i_L$	i_L	↓ ↑	-E
8	0	1	1	$-V_{C1}$	$-i_L$	0	↓ -	-2E

Currents i_L, i_{C1}, i_{C2} and the polarities of the flying capacitors are shown in figure 4.3 that are used for the following analysis. Capacitors currents in terms of load current and switching states are given by:

$$i_{c1} = (S_1 - S_3)\, i_L \qquad (4.2)$$
$$i_{c2} = (S_3 - S_5)\, i_L$$

According to equation 4.2 capacitors currents could be positive, negative or zero depends on the switching states as defined in table 4.1. Equation 4.3 demonstrates the charging and discharging status of the flying capacitors in terms of load current that is obtained from equation 4.2.

$$C_1 \frac{dV_{C1}}{dt} = (S_1 - S_3)\, i_L \qquad (4.3)$$
$$C_2 \frac{dV_{C2}}{dt} = (S_3 - S_5)\, i_L$$

This equation shows that charging and discharging of the FCs are fully dependent on the load current direction and switching states of the power devices. dVc/dt is the charging and discharging criteria for the capacitors, so that the capacitors are charged or discharged when the other side of equation 4.3 is positive or negative respectively. Table 4.1 also shows the charge and discharge of the capacitors in terms of the load current. It is evident from table 4.1 that the voltage in C_2 must be regulated to half of the voltage in C1 for 5 L waveform and it is assumed to be E for simplification. Hence, between redundant switching states to generate corresponding voltage level, one state is selected based on comparison between the voltages of two FCs and load current. Table 4.2 is extracted according to the table 4.1 in which suitable states in redundant switching states are selected in terms of current direction and conditions of charging and discharging of the flying capacitors.

Table 4.2 Selection of States on PUC5

Condition	**I_L>0**	**I_L<0**
$V_{C1} > 2V_{C2}$	State3	State2
$V_{C1} < 2V_{C2}$	State2	State3
$V_{C1} > 2V_{C2}$	State7	State6
$V_{C1} < 2V_{C2}$	State6	State7

4.3.2 Switching States and Circulating Currents of Y-PUC

Procedure of voltage balancing on the proposed configuration is the same as for those mentioned for modified single module of PUC. Nevertheless, some modification needs to be carried out to overcome the problem of circulating current in the new configuration. Circulating current in this configuration is due to voltage unbalances in two branches and the DC source. Some of the switching states create more unbalance than the others. To control and mitigation of circulating current, the switching states which generate positive polarity should be selected. To simplify the control and voltage balancing discussion, a single-line diagram of Y-PUC configuration is depicted in figure 4.4 aimed to explain the reason why the positive states are selected. M_{1x} and M_{2x} imply the collection of PUC submodules which are connected in series as shown in figures 4.1 and 4.2, in left and right arms respectively. In addition, the role of circulating current to cause the problem in control of PUC bipolar converters is investigated. Furthermore, the switching states in Y-PUC and circulating current control is discussed through the mathematical formulas in this section. It should be noted that all the control and voltage balancing in this study is integrated with the modulation technique and without any external control system.

Load current (i_X), left module current (i_{LX}), right module current (i_{RX}) and circulating current (i_{cir}) are given by equation 4.4 to equation 4.6.

$$i_X = i_{LX} - i_{RX} \tag{4.4}$$

$$\begin{aligned} i_{LX} &= \frac{i_X}{2} + i_{cir} \\ i_{RX} &= -\frac{i_X}{2} + i_{cir} \end{aligned} \tag{4.5}$$

$$\frac{i_{LX} + i_{RX}}{2} = i_{cir} \tag{4.6}$$

Index ‘x’ demonstrates the phase index which could be phase-a, phase-b, or phase-c. Through applying the KVL Voltage loop in left and right arms of figure 4.4, following equations are obtained:

$$L_0 \frac{di_{LX}}{dt} + R_0 i_{LX} = E - V_{LX} - V_X \tag{4.7}$$

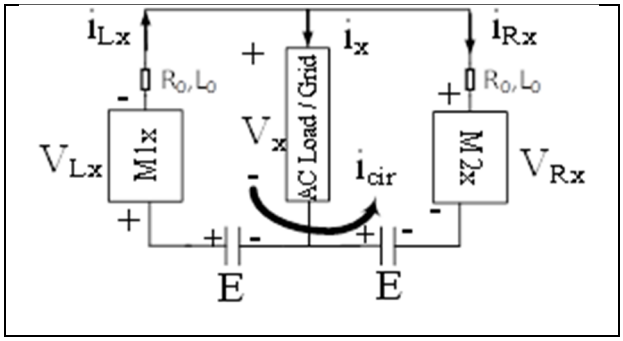

Figure 4.4 Single line diagram of proposed PUC converter

$$L_0 \frac{di_{RX}}{dt} + R_0 i_{RX} = E - V_{RX} + V_X \tag{4.8}$$

Where, R_0 and L_0 are the buffer resistance and inductance, V_{LX} and V_{RX} are the voltage across modules M1X and M2X and E is the dc source voltage where dc link is equal to 2E.

By subtracting the equation 4.7 from equation 4.8, the following equation is extracted:

$$L_0 \left(\frac{di_{RX}}{dt} - \frac{di_{LX}}{dt}\right) + R_0 (i_{RX} - i_{LX}) + V_{RX} - V_{LX} = 2V_X \tag{4.9}$$

For defining the relationship between the load voltage and voltage across each module in right and left side, equation 4.10 is obtained from equation 4.9.

$$-\frac{L_0}{2}\frac{di_X}{dt} - \frac{R_0}{2} i_X + \frac{V_{RX} - V_{LX}}{2} = V_X \tag{4.10}$$

With regard to lower amounts of buffer impedance voltage, equation 4.11 could be written through simplification on equation. 4.10 by neglecting the buffer voltage.

$$\frac{V_{RX} - V_{LX}}{2} = V_X \tag{4.11}$$

This equation is used for writing the switching states of Y-PUC based on switching states of one module of PUC5. Switching states for right and left module switches of PUC5 to generate a single phase 5-L waveform at the output of Y-PUC5 is listed in table 4.3. S_{RX} and S_{LX} are the switches S_1, S_3 and S_5 in M1X and M2X respectively. The other switches operate in complimentary way.

Figure 4.5 depicts the three-level waveform of M1X and M2X for PUC5. Based on table 4.1, modules of PUC5 can generate 5L at the output; however, only the positive levels are used in this purpose. This reason would be discussed by introducing the circulating current in next equations. It should be noted that these waveforms are assumed to be operated in switching frequency equal to system frequency for simplification on explaining the control method; however, the switching frequency is more than system frequency practically.

In this control method, the phase shift between waveforms in M1X and M2X is necessary to generate 5-L at the output based on equation 4.11and figure 4.5. Otherwise, three-level waveform is generated at the output of Y-PUC5.

The switching states listed in table 4.3 has been obtained according to the figure 4.5. For instance, when voltage of Vx is equal to +E/2, switching state of right-side module of PUC5 is 101 or 110 while the left side module of PUC5 is in zero state (000) or right-side module is 100 and left side one is 101 or 110. Similarly, the other states are obtained in such a way that is listed in table 4.3.

Table 4.3 Switching States of Y-PUC to Generate 5-Level Waveform

State	S_{R1}	S_{R3}	S_{R5}	S_{L1}	S_{L3}	S_{L5}	V_{RX}	V_{LX}	V_{diff}	V_X
1	1	0	0	0	0	0	+2E	0	0	+E
2	1	0	0	1	1	0	+2E	+E	-E/2	+E/2
3	1	0	0	1	0	1	+2E	+E	-E/2	+E/2
4	1	0	1	0	0	0	+E	0	+E/2	+E/2
5	1	1	0	0	0	0	+E	0	+E/2	+E/2
6	1	0	1	1	0	1	+E	+E	0	0
7	1	0	1	1	1	0	+E	+E	0	0
8	1	1	0	1	0	1	+E	+E	0	0
9	1	1	0	1	1	0	+E	+E	0	0
10	1	0	1	1	0	0	+E	+2E	-E/2	-E/2
11	1	1	0	1	0	0	+E	+2E	-E/2	-E/2
12	0	0	0	1	0	1	0	+E	+E/2	-E/2
13	0	0	0	1	1	0	0	+E	+E/2	-E/2
14	0	0	0	1	0	0	0	+2E	0	-E

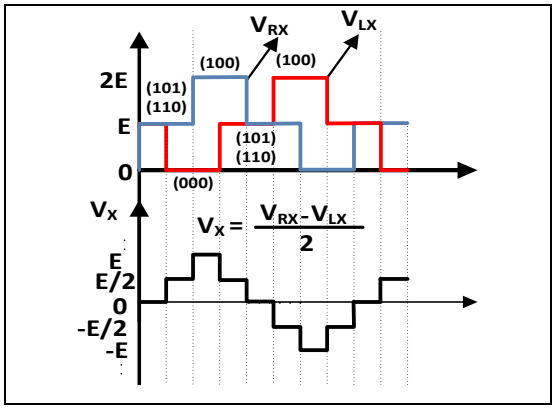

Figure 4.5 Voltage waveform across M1X, M2X and load on phase-x in Y-PUC converter that has been defined by VLX, VRX and VX respectively

In addition, equation.4.12 is achieved through summation of equation 4.7 and equation 4.8.

$$\mathrm{L}_0(\frac{di_{LX}}{dt}+\frac{di_{RX}}{dt})+\mathrm{R}_0(i_{LX}+i_{RX})=2E-(V_{LX}+V_{RX}) \tag{4.12}$$

By substituting equation 4.6 into equation 4.12, the following equation is drawn out to obtain the circulating current from the voltages of modules:

$$\mathrm{L}_0(\frac{di_{cir}}{dt})+\mathrm{R}_0(i_{cir})=E-\frac{(V_{LX}+V_{RX})}{2} \tag{4.13}$$

In fact, the right hand of equation 4.13 introduces the voltage source which produces the circulating current. In other words, voltage unbalance or difference voltage between AC and DC causes the circulating current which can be denoted by following equation:

$$V_{diff}=E-\frac{(V_{LX}+V_{RX})}{2} \tag{4.14}$$

equation 4.14 includes AC and DC part that the AC part shows the electro-motive force (emf_{cir}) of circulating current. Which is defined as following equation:

$$e_X=\frac{(V_{LX}+V_{RX})}{2} \tag{4.15}$$

Figure 4.6 depicts the equivalent circuit of circulating current in which two AC and DC sources cause the flowing of unwanted circulating current.

Through substituting the equation 4.14 to equation 4.13, equation 4.16 is obtained as follows:

$$\mathrm{L}_0\frac{d}{dt}i_{cir}+\mathrm{R}_0\,i_{cir}=\mathrm{V}_{diff} \tag{4.16}$$

Solving this first order equation, circulating current is calculated by the following equation:

$$i_{cir}=\frac{V_{diff}}{R_0}+(\mathrm{I}_0-\frac{V_{diff}}{R_0})\mathrm{e}^{\frac{-t}{\tau}} \qquad \text{Where} \qquad \tau=\frac{L_0}{R_0} \tag{4.17}$$

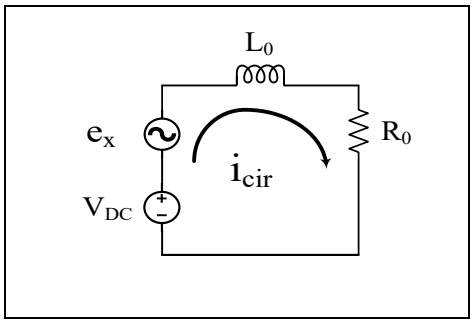

Figure 4.6 Equivalent circuit of circulating current

Equation 4.17 shows that the main part of circulating current is the V_{diff} that should be mitigated to reduce the circulating current. In each switching state, half of the summation of voltages in M1X and M2X should be equal or close to the half of the DC link voltage; otherwise, depending on the magnitude of V_{diff} higher circulating current can be generated. I_0 shows initial value of current, τ is the time constant. V_{diff} is also shown in table 4.3 in corresponding switching states for single-phase of Y-PUC. It is clear from the table 4.3 that the V_{diff} is equal to zero in states which VX is +E, -E and 0 and its absolute value is E/2 for other states. Thus, through selection of these redundant switching states, capacitor voltage of the converter is balanced and circulating current is almost controlled without using the external control; however, to remove the circulating current thoroughly, it needs an additional control system that could be discussed in future research works.

4.3.3 Voltage balancing integrated with phase-shift modulation on Y-PUC

To generate 5-L voltage waveforms based on switching states in table 4.3, three reference voltage and 4 carrier signals are required for the modulation of three-phase Y-PUC converter with one module of PUC in each arm. It is evident from table 4.3 that, each module (V_{RX} and V_{LX}) generates 3-L waveform (0, E, 2E) in order to produce 5-L across the load (V_X). It should be noted that the negative states are utilized for DC fault current handling. The concept of PS-PWM that has been presented in (S. Arazm et al., 2018b), is used in this study to modulate the reference voltage in Y-PUC converter. Figure 4.7 illustrates four desired carriers for left and

right arms as well as three reference voltage for three-phase system. Carriers CrR1 and CrR2 have 180° phase shift that modulate the reference voltages Vref-a , Vref-b, and Vref-c to create 3L voltages 0, +E, and +2E for right arm. Similarly, the phase displacement between CrL1 and CrL2 is π and the same reference voltages are used to generate 3L voltages in the left arm. The phase shift between the right carriers CrR1, CrR2 and left carriers CrL1,CrL2 to generate 5L waveform is π/2. Equation 4.18 shows the phase displacement between the carriers in each arm.

$$\Delta\phi = \frac{2\pi}{2n} \tag{4.18}$$

Where, n is the number of PUC5 submodules per arm. Phase displacement between the corresponding right and left arms carriers is given by:

$$\Delta\phi = \frac{2\pi}{n} \tag{4.19}$$

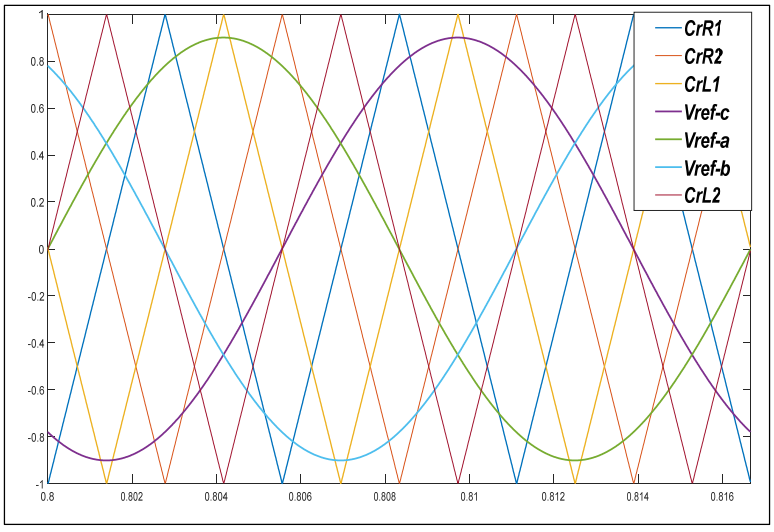

Figure 4.7 Carrier signals and reference voltage for modulation of proposed configuration with PUC5

The situations of the charge and discharge of the flying capacitors in left- and right-side modules for all 14 states in Y-PUC is determined in table 4.4. For instance, in state 6, if $I_{RX}>0$

the upper capacitor of right arm (CR1) is charged and the lower capacitor of right arm (CR2) is discharged and if $I_{LX}>0$, the upper capacitor of left arm (CL1) is charged and the lower capacitor of left arm (CL2) is discharged. In fact, there are 14 redundant states to generate 5-L voltages in which states 1 and 14 that generate +E and -E are not redundant; however, there

Table 4.4 Charge and Discharge Situation on Flying Capacitors of One Phase of Double Star Y-PUC5 Inverter

State	**$I_{RX}>0$**		**$I_{RX}<0$**		**$I_{LX}>0$**		**$I_{LX}<0$**		**V_X**
	CR1	**CR2**	**CR1**	**CR2**	**CL1**	**CL2**	**CL1**	**CL2**	
1	↑	-	↓	-	-	-	-	-	+E
2	↑	-	↓	-	-	↑	-	↓	+E/2
3	↑	-	↓	-	↑	↓	↓	↑	+E/2
4	↑	↓	↓	↑	-	-	-	-	+E/2
5	-	↑	-	↓	-	-	-	-	+E/2
6	↑	↓	↓	↑	↑	↓	↓	↑	0
7	-	↑	-	↓	↑	↓	↓	↑	0
8	↑	↓	↓	↑	-	↑	-	↓	0
9	-	↑	-	↓	-	↑	-	↓	0
10	↑	↓	↓	↑	↑	-	↓	-	-E/2
11	-	↑	-	↓	↑	-	↓	-	-E/2
12	-	-	-	-	↑	↓	↓	↑	-E/2
13	-	-	-	-	-	↑	-	↓	-E/2
14	-	-	-	-	↑	-	↓	-	-E

are 12 states with sufficient redundancy to balance the flying capacitor voltages in M1X and M2X in Y-PUC converter. Moreover, states 2, 3, 4, 5 generate voltage levels +E/2 that states 2 and 3 are used to balance the capacitors voltage in M1X and states 4 and 5 are utilized for voltage balancing in M2X. Due that in steady states the voltage of the upper capacitor of right

arm (V_{CR1}) and the voltage of the upper capacitor of left arm (V_{CL1}) should be two times of voltages in lower capacitors of right arm (V_{CR2}) and left arm (V_{CL2}), this condition is investigated in sampling time and is applied in carrier frequency to select the appropriate states. Thus, when +E/2 is generated based on the modulation strategy, if, $I_{LX}>0$ and $V_{CL1}>2V_{CL2}$, state 2 should be selected and if $I_{RX}>0$ and$V_{CR1}>2V_{CR2}$ states 5 should be chosen. As well, at the same current direction if $V_{CL1}<2V_{CL2}$, state 3 and if $V_{CR1}<2V_{CR2}$ state 4 should be selected for M1X and M2X respectively. State selections for generating 5L waveform across the load in Y-PUC converter is listed in table 4.5. To simplify the voltage balancing method, especially for modular Y-PUC, the right and left carriers (CrRi, CrLi) with one reference voltage per phase is implemented on each arm separately. The flowcharts of figures 4.8 and 4.9 illustrate the voltage balancing integrated with phase shift modulation on Y-PUC with one module per arm.

Table 4.5 Selection of Suitable States on Y-PUC

Condition	**$I_{L,RX}>0$**	**$I_{L,RX}<0$**	**Voltage level**
-	State1	State1	+E
$V_{CL1}> 2V_{CL2}$	State2	State3	+E/2
$V_{CL1}<2V_{CL2}$	State3	State2	+E/2
$V_{CR1}> 2V_{CR2}$	State5	State4	+E/2
$V_{CR1}<2V_{CR2}$	State4	State5	+E/2
$V_{CL1}> 2V_{CL2}$	State8	State7	0
$V_{CL1}<2V_{CL2}$	State7	State8	0
$V_{CR1}> 2V_{CR2}$	State7	State6	0
$V_{CR1}<2V_{CR2}$	State6	State7	0
$V_{CL1}> 2V_{CL2}$	State13	State12	-E/2
$V_{CL1}<2V_{CL2}$	State12	State13	-E/2
$V_{CR1}> 2V_{CR2}$	State11	State10	-E/2
$V_{CR1}<2V_{CR2}$	State10	State11	-E/2
-	State14	State14	-E

It is illustrated from the flowchart that the switching states for left and right arms must be conversely selected to avoid using two reference voltages. The switching states corresponding to negative voltage levels are not chosen in normal operation and they are used to block the DC fault current.

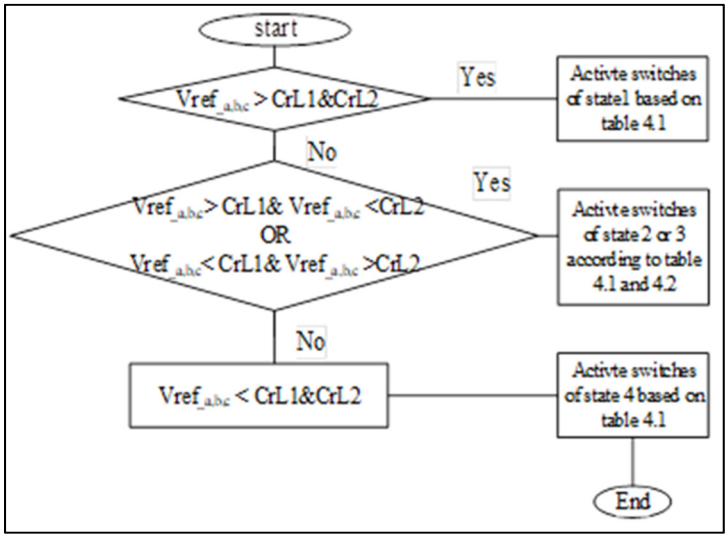

Figure 4.8 Voltage balancing integrated with PS-PWM flowchart for left arm of Y-PUC

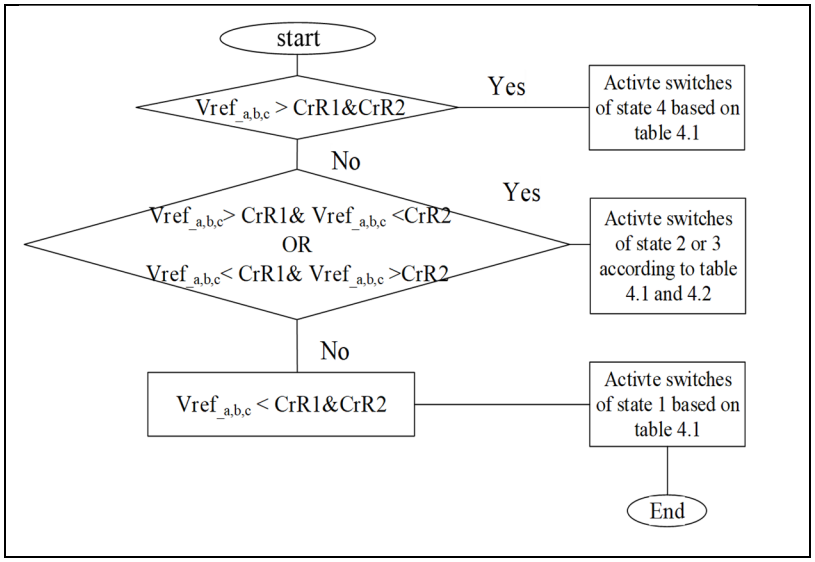

Figure 4.9 Voltage balancing integrated with PS-PWM flowchart for right arm of Y-PUC

Thus, voltage levels 2E, E, and 0 are generated through the PS-PWM conditions defined in flowcharts of figures 4.8 and 4.9. Voltage balancing in the FCs of PUC is carried out through suitable selection between the redundant switching states. For example, to generate voltage level, E, if iL>0, and Vc1>2Vc2, state 3 should be chosen, elseif Vc1<2Vc2, then state 2 should be selected. The other condition is listed in table 4.2. Voltage balancing control block diagram for Y-PUC converter is shown in figure 4.10 in which FCs voltages and arm current as well as the modulation parameters are the system input, and the switching patterns are the system output.

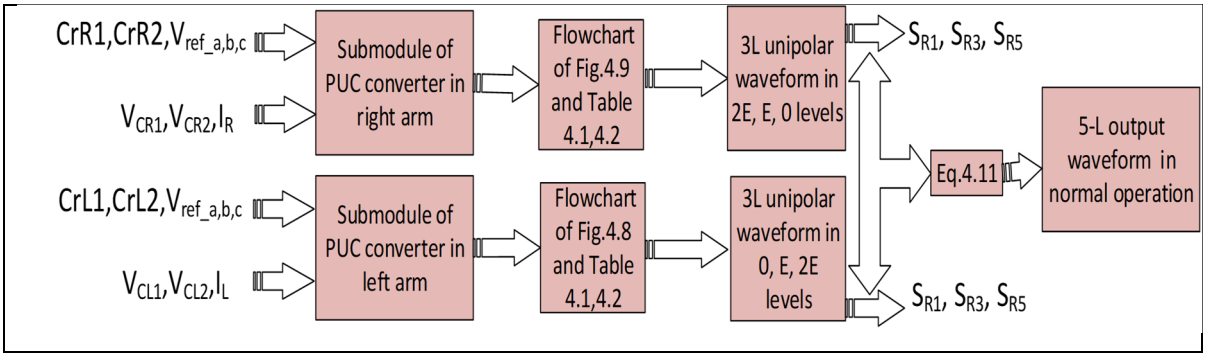

Figure 4.10 Voltage balancing block diagram control of Y-PUC converter

4.3.4 DC fault blocking on modular Y-PUC converter

In transmission line of HVDC, DC short circuit fault clearing through the switching devices of the converter is a vital issue. To achieve this capability, the submodules which used in MMCs, must be bipolar so that their flying capacitors could be inserted in their revers-biased voltage in the route of fault current. When the fault current is flows, first, all the IGBTs must be blocked and thereafter, fault current flows from free-wheeling diode as shown in figure 4.11. On the other hand, DC fault current is blocked, when sum of the upper capacitor voltages (V_{C1} In figure 4.11) in each leg of Y-PUC along the fault current path is higher than the maximum line to line voltage. Following equation illustrates this condition.

$$2N_{PUC}V_{C\_Upper} \geq V_{peak(Line\_Line)} \tag{4.20}$$

Thus, power switching devices and FCs rating must be chosen in such a way to meet this objective. Figure 4.12. shows the Y-PUC in HVDC application and its DC fault current path.

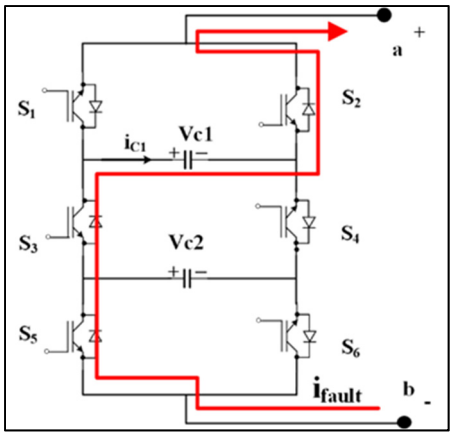

Figure 4.11 DC fault current path during the short circuit event

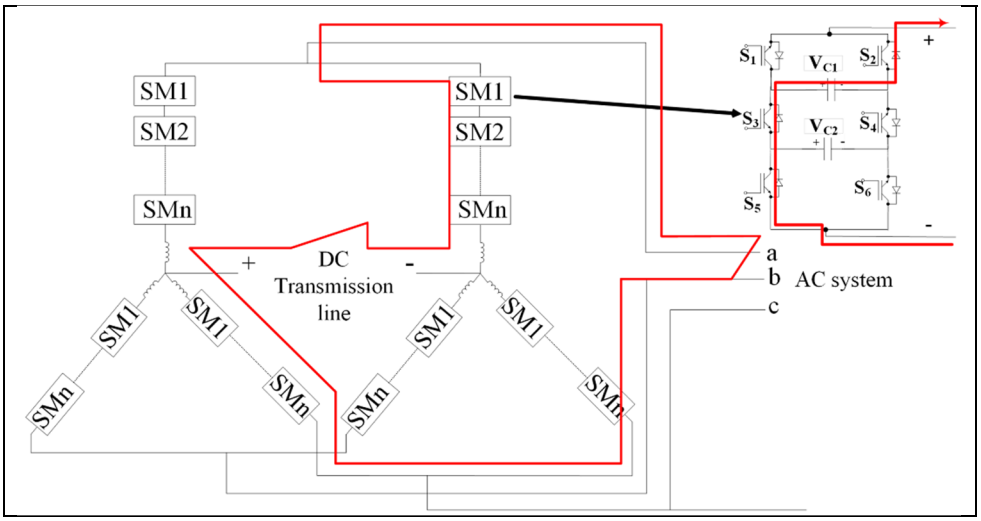

Figure 4.12 Pole to pole DC short circuit and fault current path during in HVDC system with Y-PUC configuration

Utilising the PUC5 submodule in Y-PUC HVDC application save the more switching devices and capacitors compared to FB-MMC. In fact, PUC5 submodule like cross connected, and double clamped reduces the size and cost of the MMC. However, the voltage stresses in PUC5

switches are lower than the cross connected which is a feature of this topology in HVDC application. It should be noted that the hybrid MMC is another solution to obtain the reduced components counts with lower power losses while are capable to handle the DC fault (Adam & Williams, 2014; Nguyen et al., 2019; J. Qin, Saeedifard, Rockhill, & Zhou, 2015). In hybrid MMC, one of the bipolar submodules such as full-bridge, cross-connected, PUC are connected in series with the half-bridge submodule. Table 4.6 illustrates one comparison between the various submodules of MMCs to demonstrate the advantage of Y-PUC converter. All of the introduced submodules in this table except HB-MMC and FC-MMC are capable to handle the DC fault current (J. Qin et al., 2015).

Table 4.6 Comparison of Modular Multilevel Converters and Y-PUC to Generate Single-phase 21 Voltage Levels at the Output when DC Link Voltage is 2E

Converters	**Number of switching devices per arm**	**Number of FCs per arm**	**Number of diodes per arm**	**Total components per arm**	**Switch Voltage stress**
HB-MMC	40	20	0	60	E/10
FC-MMC	40	20	0	60	E/10
FB-MMC	80	20	0	100	E/10
CD-MMC	50	20	20	90	E/10
CC-MMC	60	20	0	80	E/5, E/10
TL-MMC	60	20	20	100	E/10
Y-PUC5	30	10	0	40	2E/5, E/5

It is drawn out from table 4.6 that the number of components in Y-PUC converter is less than half of the FB-MMC and the other counterparts. Moreover, its total components count is also less than HB-MMC and FC-MMC which are not capable to block the DC fault current. Although the voltage stress in switching devices in Y-PUC is more than the topologies listed in table 4.6, regarding a highly reduced component count of Y-PUC, it is still acceptable

Table 4.7 Comparison the Technical Specifications Among Three Types of MMCs

MMC type	**HB-MMC**	**Y-PUC**
Vdc (V)	400	400
N: Number of cells in each arm	16	4
M: voltage levels	17	17
Fs: carrier frequency	2000Hz	2000Hz
THD_I	0.6%	0.54%
THD_V	7.15%	7.14%
Modulation Index	0.95	0.95
P	1650	1650
Q	820	820
I_{rms}	13.95	13.95
V_{rms}	131.5	131.5
C: cells capacitor	20 mF	C1= 5mF
		C2=2.5mF
I_{dc}	4.2 A	4.2 A
Vc: voltage at each capacitor or voltage divided among cells	25V	Vc1=100V Vc2=50V
Switching device rating	25V/15A	2upper switches: 100V/15A 4 lowers witches: 50V/15A
Number of switching devices	64	48
Number of flying capacitors	32	16
Components counts	69	64
Ripple voltage at each capacitor	<5%	C1,3 <4% C2 <4%
efficiency	89.43%	89.6%

alternative not only for popular FB-MMC, but also for HB-MMC. To illustrate, a detail comparison between Y-PUC and HB-MMC is shown in the following subsection.

4.3.5 Full comparison between Y-PUC and HB-MMC

In this subsection a comparison between the most conventional HB-MMC and PUC-MMC (Y-PUC) has been carried out to evaluate the power losses and waveform quality as well as the counts and the rating values of the equipment. To conclude the exhaustive comparison, the technical parameters are selected according to one commercialized HB-MMC simulator OPAL-1210 (OP-1210). The results are calculated based on Matlab simulation for two types of MMCs to generate 17-L voltage waveform. A full comparison is listed in table 4.7 in which two MMCs have been designed to feed one single-phase 2KVA RL load with one 400 V DC source. The output results show that their wave quality and power losses are almost similar.

4.4 Simulation Results

Validation of the proposed single DC source configuration of Y-PUC converter is carried out by Matlab/Simulink. Simulation results for three-phase system based on the parameters listed in table 4.8 is performed and related figures are depicted in figures 4.13 to 4.18.

Table 4.8 System Parameters for Proposed Y-PUC5 Configuration

DC link voltage (2E)	200 V
RL load	40Ω, 20mH
Switching frequency	1000 Hz
Modulation Index	0.95
Sampling time	50 μs
Capacitor	1 mF

Voltage waveform with 5-L phase voltage and 9-L line voltage in steady state are illustrated in figure 4.13 which demonstrates the validity of the proposed configuration of single-DC source three-phase Y-PUC.

Voltage balancing capability of flying capacitors in steady states are illustrated in figure 4.14.a in which six upper and lower capacitors are balanced as 2E and E. Figure 4.14.b depicts the voltage ripples in 6 capacitors $V_{CL1\text{-}a,\,b,\,c}$ and $V_{CR1,\,a,\,b,\,c}$ that are the upper capacitor voltages in left and right modules of three-phase Y-PUC. As well, voltage ripples of six lower capacitors $V_{CL2\text{-}a,\,b,\,c}$ and $V_{CR2,\,a,\,b,\,c}$ are illustrated in figure 4.14.c. voltage ripples with 1mF flying capacitor is less than 5% that shows the performance of voltage balancing method in Y-PUC configuration.

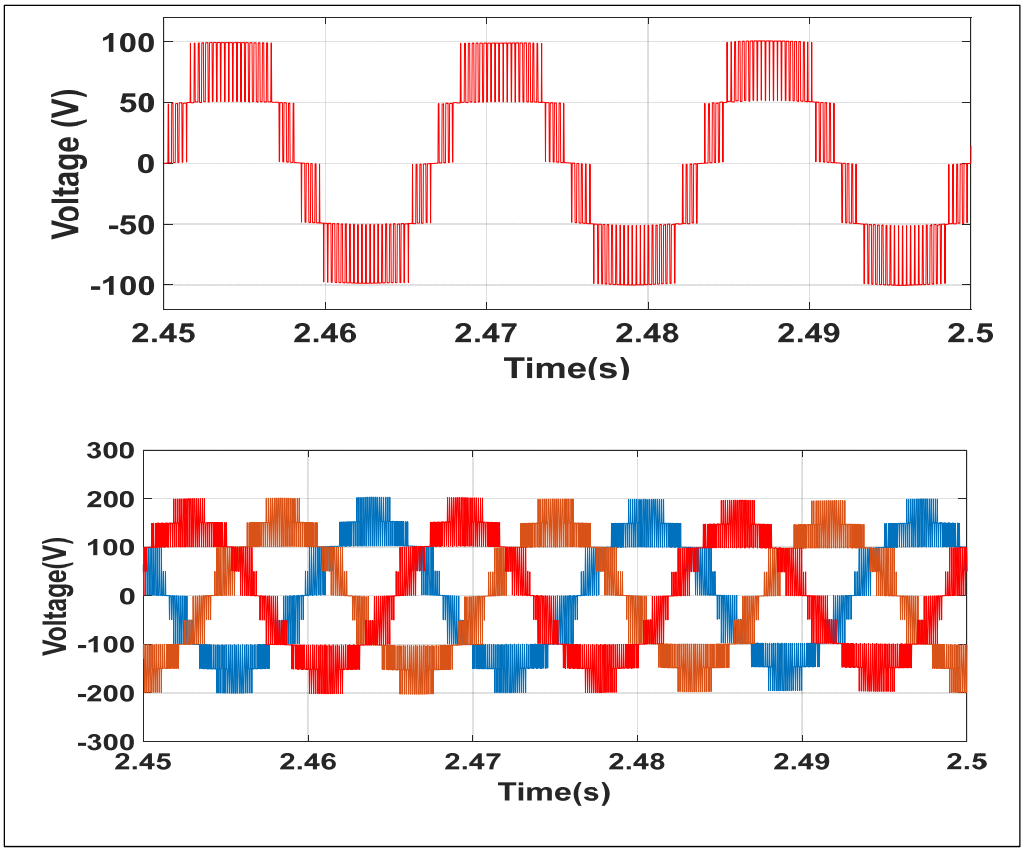

Figure 4.13 5-L single phase voltage and 9-L Line voltage waveform of three-phase single DC source Y-PUC converter

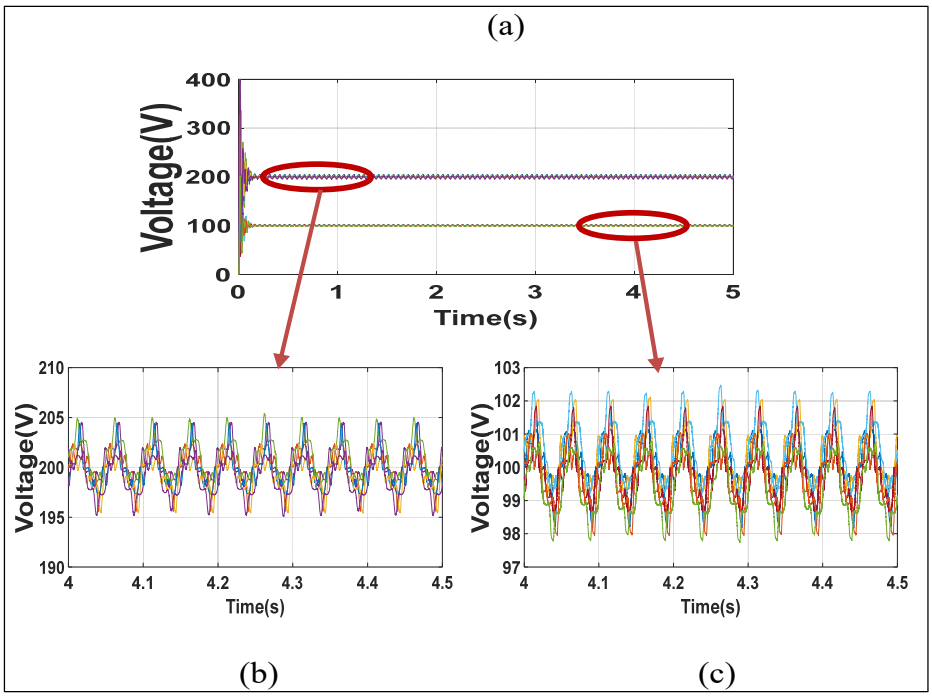

Figure 4.14 a) Voltage balancing on flying capacitors b) Voltage balancing across the FCs of upper arm c) Voltage balancing across the FCs of lower arm

To examine the dynamic response of the three-phase Y-PUC converter, DC voltage is varied from 200 V to 400V and is returned to 200 V which voltage variations as well as line voltages are shown in figure. 4.15.

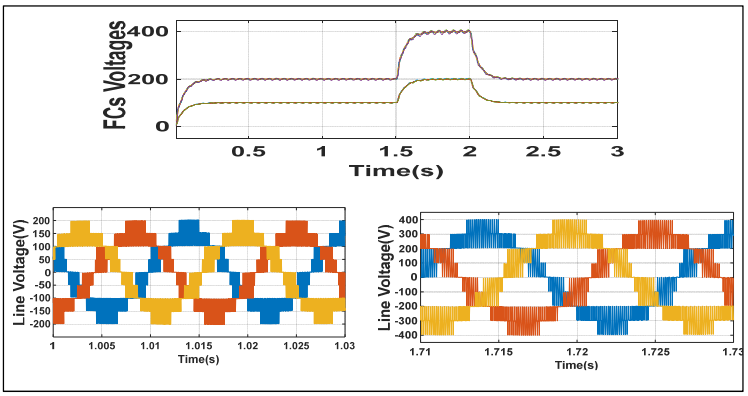

Figure 4.15 Flying capacitors voltages during the DC link variation from 200 V to 400 V and returning to 200 V

Moreover, variation of load parameters from R=40 Ω, L=20mH to R=80 Ω and L=40mH has been studied and the results are shown in figure 4.16 which shows the capability of the converter to adjust with the severe alteration in load.

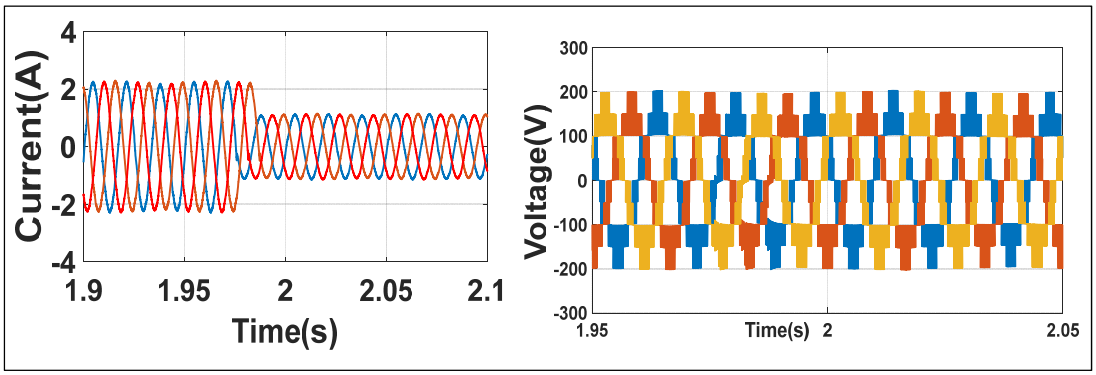

Figure 4.16 Current and Voltage waveform at the output of single DC source three-phase PUC due to load variation

To validate the modularity performance of Y-PUC, four modules have been placed in each arm and the Simulink is run with the similar parameters of table 4.8. the results of figure 4.17 show the circulating current, load current and output voltage of converter during the Load current variation.

Figure 4.18 shows the voltage balancing in FCs in modular Y-PUC when the DC voltage is varied to two times.

4.5 Experimental Results

The algorithm of combined voltage balancing integrated with PS-PWM is implemented on single-phase double star configuration of Y-PUC to validate the performance of the configuration. The algorithm is implemented on dSpace 1103 as real-time controller and switching pulses are sent to the left and right-side modules of PUC switches through the interface board. The setup of experimental devices is shown in figure 4.19. experimental

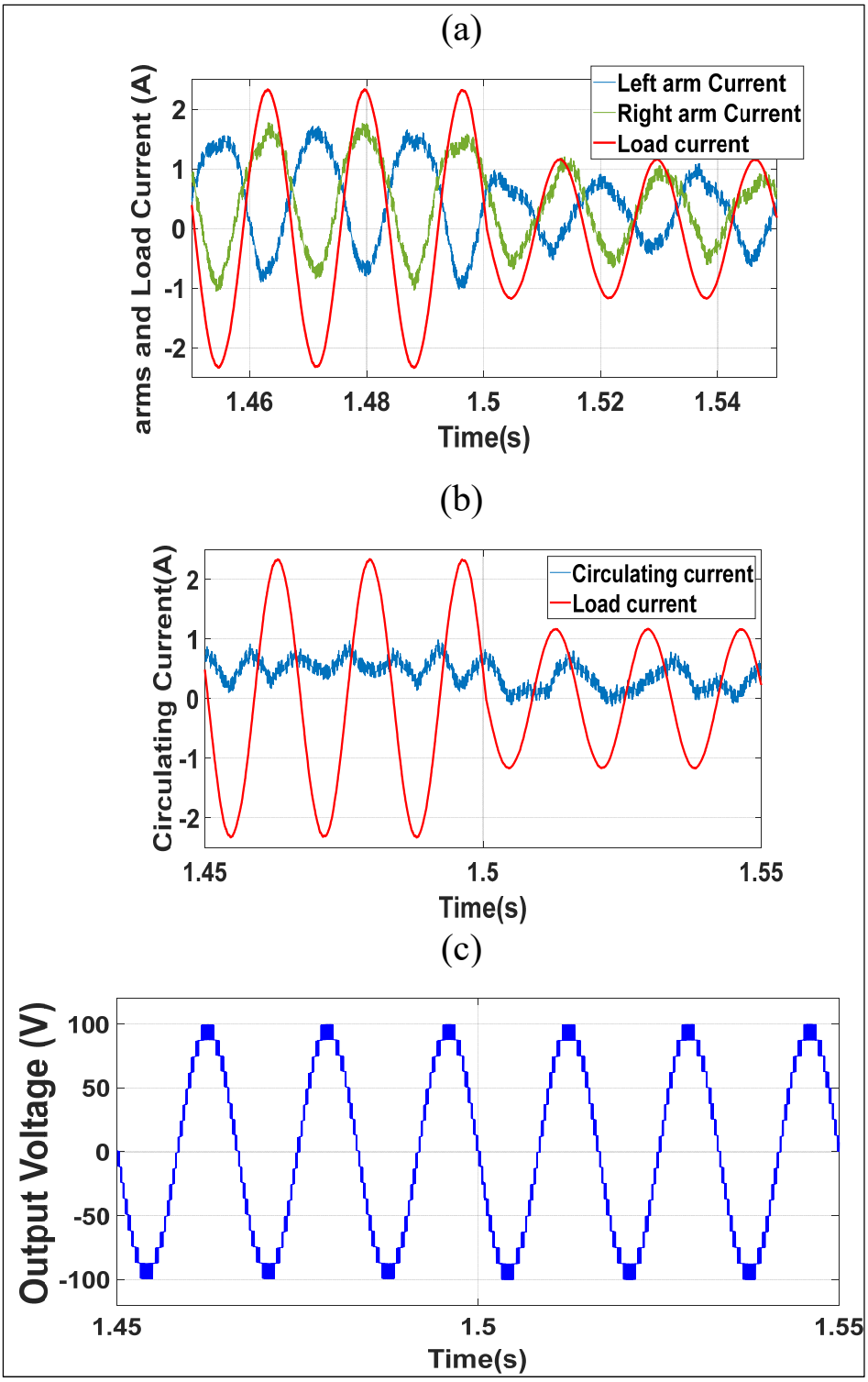

Figure 4.17 Dynamic response of Modular Y-PUC converter with 4 modules per arm during the load variation from 40 ohm to 80 ohm a)Arms current and load current b) circulating current c) load voltage

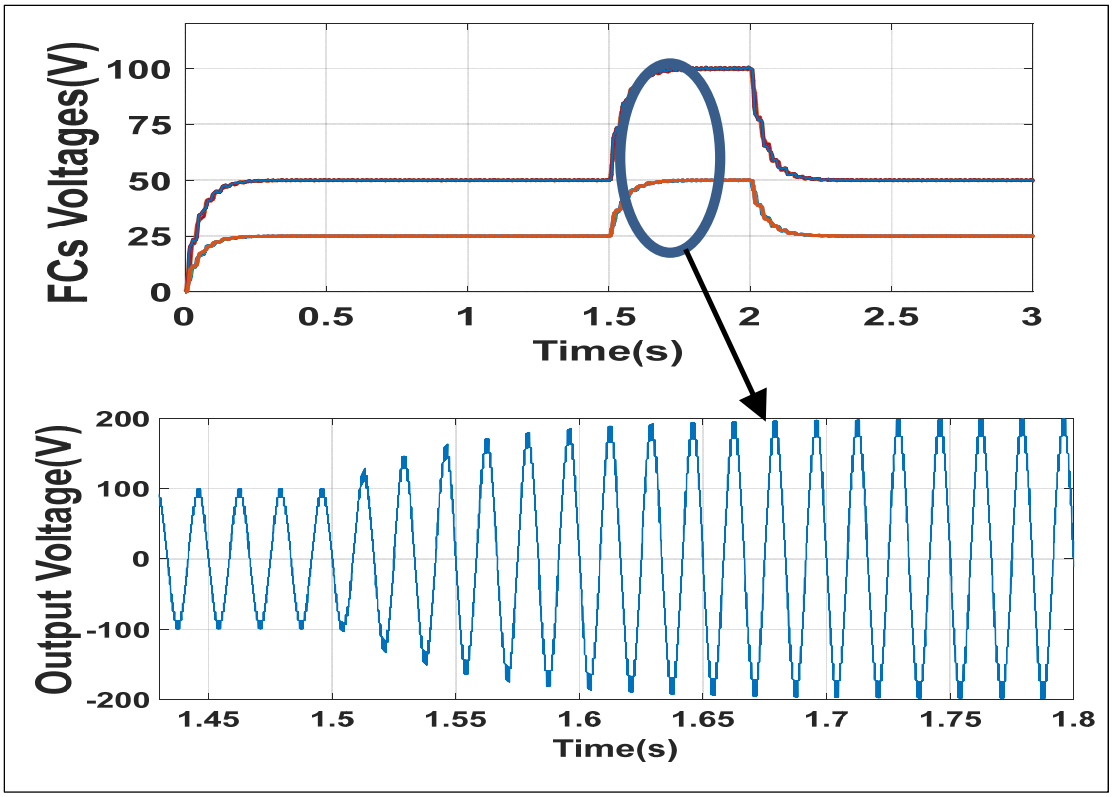

Figure 4.18 Dynamic response of Modular Y-PUC converter with 4 modules per arm during the DC voltage variation from 200 V to 400 V and returning to 200 V

parameters are listed in table 4.8. The real time controller sampling time of dSpace is set to 50μs and all the flying capacitors are 1mF. The Y-PUC set up has been prepared to implement the voltage balancing control method on proposed Y-PUC converter to study the performance of the converter in steady states and transient. Figure 4.20 shows the 5-L load voltage and sinusoidal current in the load which are defined in channels 2 and 4. As well, voltage across the upper and lower capacitors are shown in channels 1 and 3. One can notice the well-regulated voltages across all circuit capacitors. As well, voltage across the upper and lower capacitors are shown in channels 1 and 3. One can notice the well-regulated voltages across all circuit capacitors.

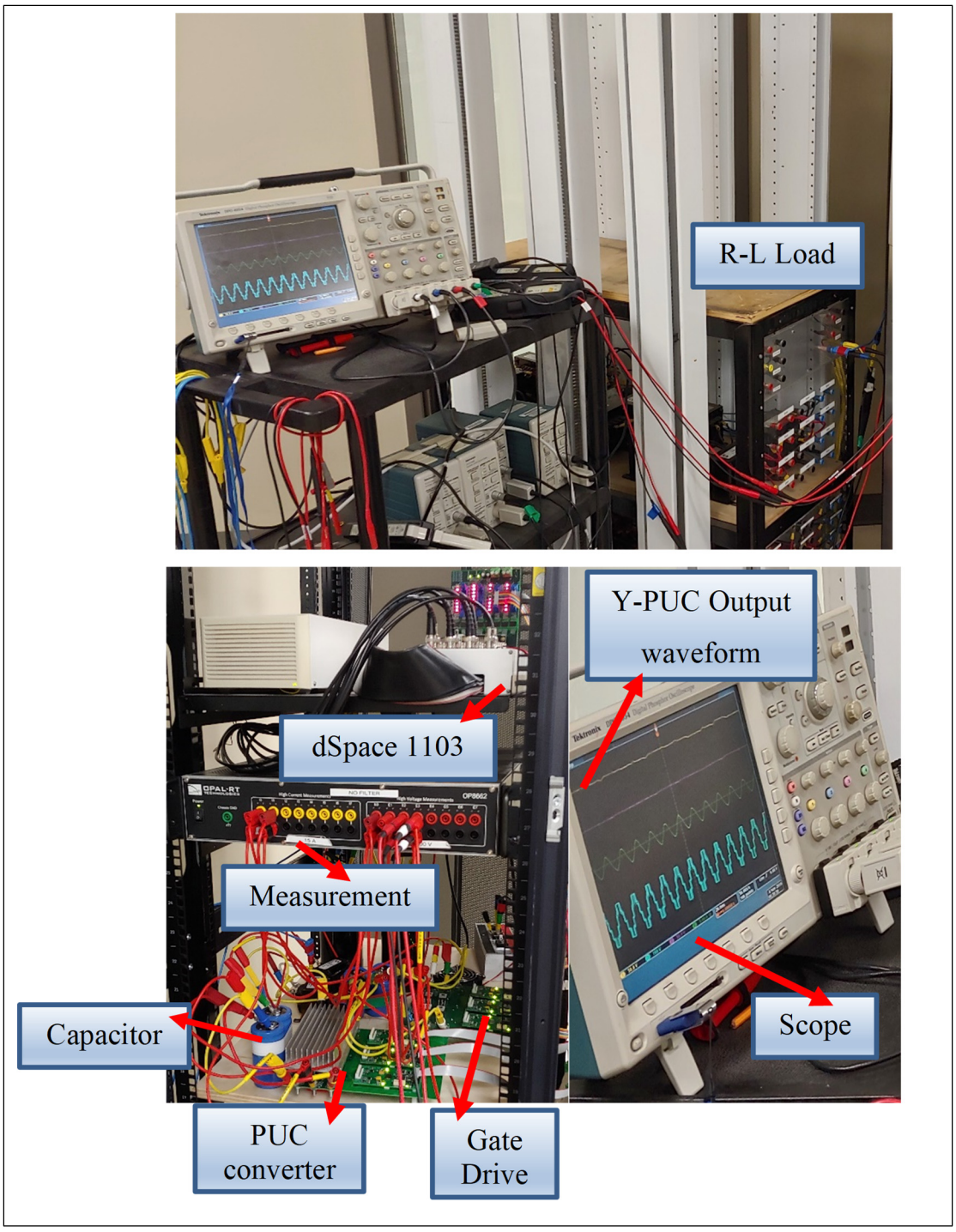

Figure 4.19 Laboratory setup of proposed configuration of Y-PUC

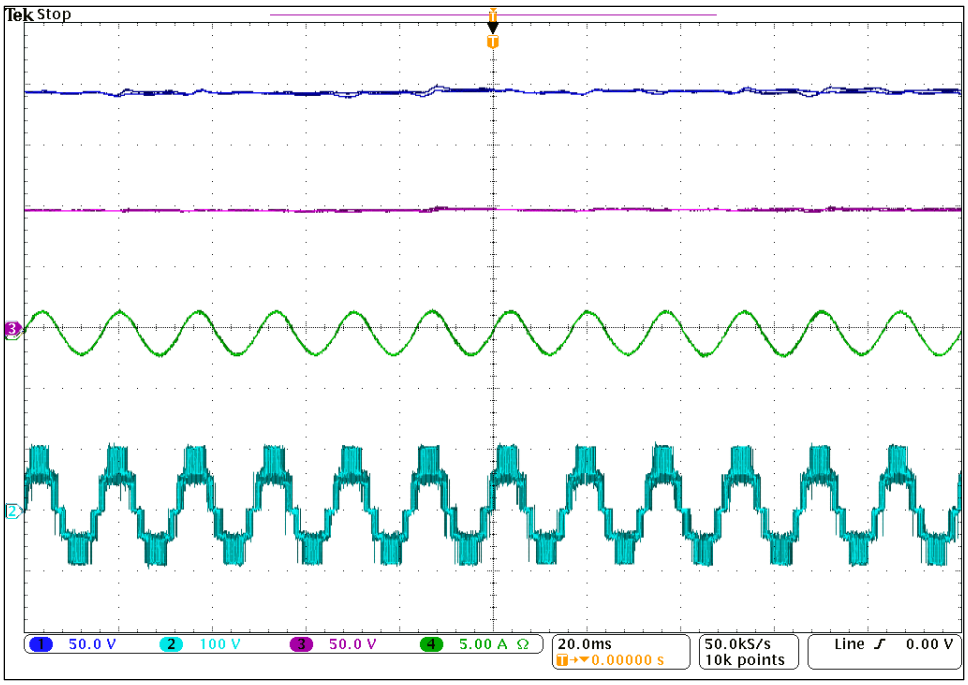

Figure 4.20 5-L voltage (light blue wave, Channel.2), current (Channel.4, green wave), capacitor voltage V_{CL1} and V_{CR1} (dark blue, Channel.1) and capacitor voltage V_{CL2} and V_{CR2} (violet DC wave, Channel.3)

Figure. 4.21 shows the voltage balancing on four 1000 µF capacitors for right and left modules of Y-PUC converter. Note that voltage ripple is about 5% that is the same as the simulation results and that would be an acceptable ripple for design of the converters; however, the ripples would be reduced through increase in size of the capacitors. Voltage balancing in V_{CL1}, V_{CL2}, V_{CR1} and V_{CR2} is depicted in figure. 4.21.

Dynamic performance of Y-PUC is validated through several variations on the DC source voltage, the load size and modulation index. Voltage source in DC link voltage is suddenly changed from 100V to 180V and voltage of the upper capacitors (V_{CL1}, V_{CR1}) and lower capacitors (V_{CL2}, V_{CR2}) and output voltage (V_X) are adjusted very fast that has been illustrated in figure 4.22. Channel 3 shows the DC source, and channels 1 and 4 depict the upper and lower FCs voltages. Moreover, channel 2 shows the output voltage which is adjusted properly with DC voltage variation.

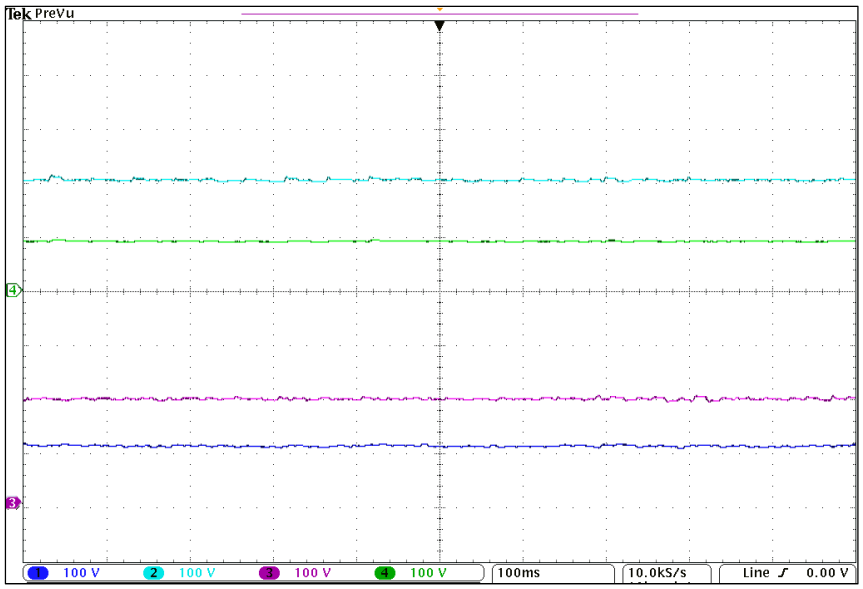

Figure 4.21 Voltage balancing on four 1000µF flying capacitors. Channel 1, dark blue wave,100 V/div is VCL2, Channel 3, violet wave 100V/div is VCL1, Channel 4, dark green wave, 100 V/div is VCR2, Channel 3, blue wave 100V/div is VCR1

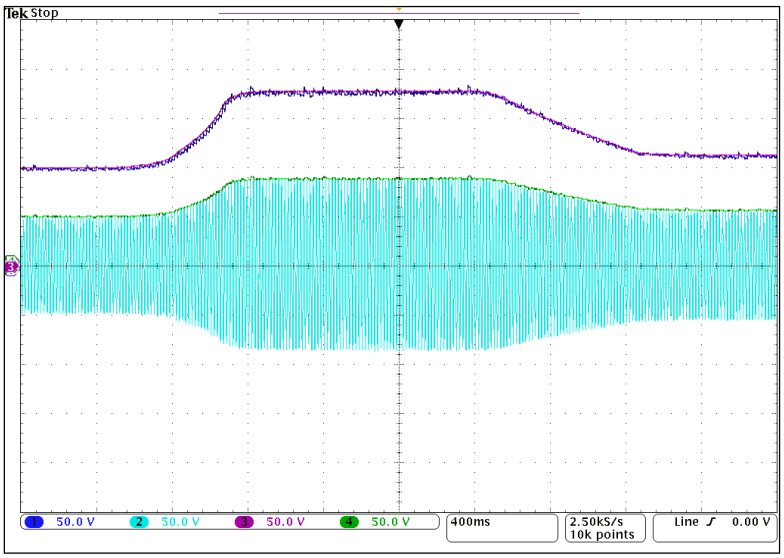

Figure 4.22 Voltage balancing on FCs and load voltage adjustment during the DC source variation. Channel 1, dark blue wave,50 V/div is the V_{CL1} voltage in upper capacitor, Channel. 2, blue wave, 50 V/div is the V_X , voltage across the load in Y-PUC converter, Channel. 3, violet wave, 50 V/div is the DC source voltage, Channel 4, green wave, 50 V/div is the V_{CL2} voltage in the upper capacitor

To verify the performance of the converter with load current variation, resistance has been changed from 80 Ω- 40 Ω and again 80Ω. Figure 4.23 shows the voltage and current of the load as well as the voltages in two FCs during the load variation. It can be seen from the figure that voltage on FCs and consequently across the load is appropriately balanced during the load variations and load voltage is independent from load current which shows the performance of the control method.

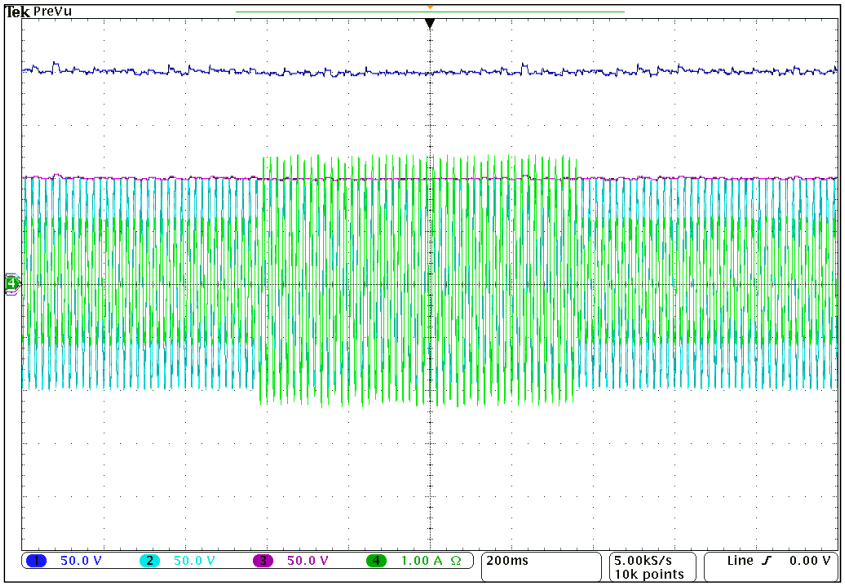

Figure 4.23 Voltage (light blue wave) and current (green wave) across the load and FCs voltages during the load variation (dark blue wave is the V_{CR1}, violet wave is the V_{CR2})

Figure 4.24 shows capacitor voltages, load voltage and load current in terms of modulation index variation. For this study, the modulation index is varied from 0.95 to 0.6 and again it is returned to 0.95. This figure validates the performance of the Y-PUC converter and the voltage balancing algorithm in FCs in a wide range of modulation index variation.

4.6 Conclusion

In this chapter a new double star, single-phase and three-phase configuration for Y-PUC converter with a single DC source is proposed. This configuration not only resolve the problem

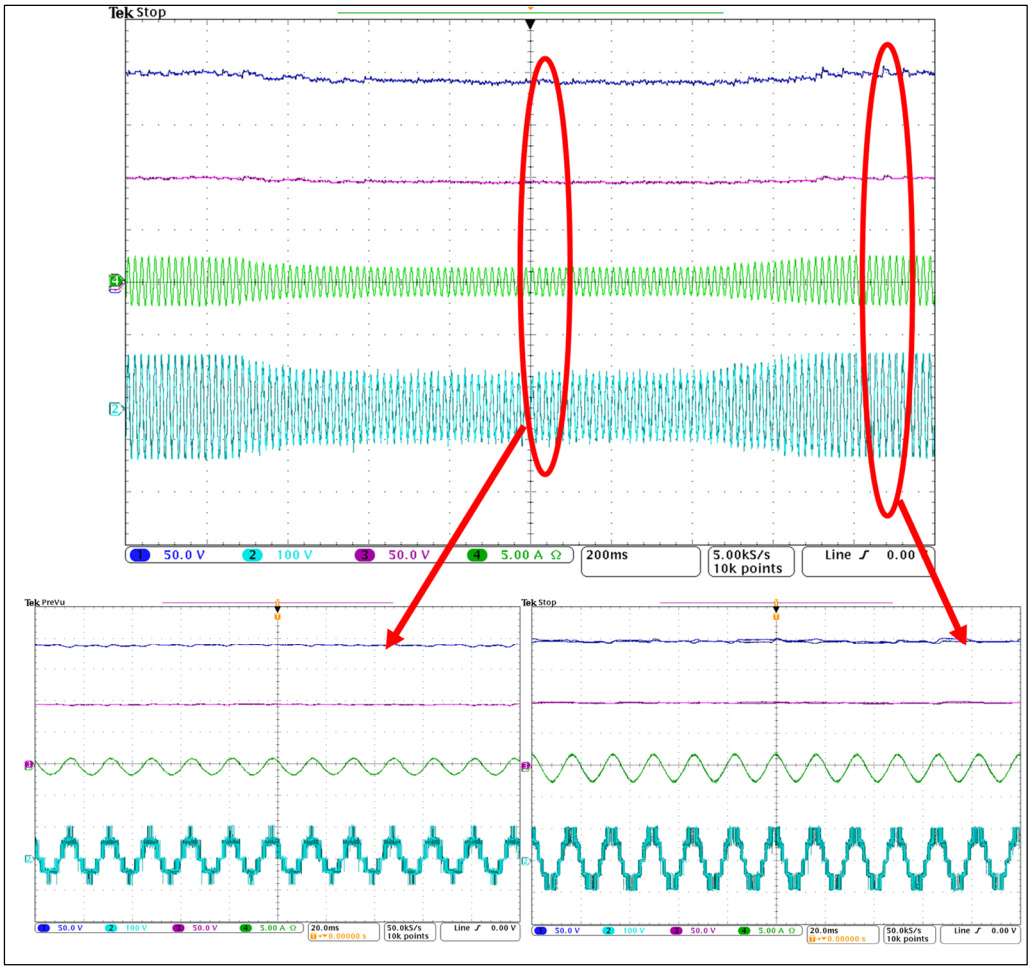

Figure 4.24 Load voltage, current and capacitor voltages during the modulation index variation from 0.6 to 0.95

of isolated DC source in three-phase PUC converters but can also be applied in single-phase and three-phase systems for high power and high-voltage applications due to its modularity and DC fault handling capability. A generalized PUC converter can be located as a submodule in the proposed configuration. Analysis of PUC5 as a simple packed U-cell converter with the redundant switching states are completely explained by the algorithm of control to balance the voltage. Voltage balancing integrated with PS-PWM strategy is implemented on the proposed double star (Y-PUC) configuration to validate the control algorithm and the configuration. Simulation and experimental results validate the performance of the proposed configuration and its control approach for voltage balancing in static and dynamic states.

CONCLUSION

Conventional two-level converters are recently being replaced by multilevel converters (MLCs) and modular multilevel converters (MMCs) due to voltage stress reduction, lower harmonic filters, higher quality waveforms. However, size, cost, simplicity of topology, and patterns of switching are still significant concerns that must be addressed for each application. NPC is one of the popular types of MLCs which has already been commercialized as a three-Level converter and it is not appropriate for more than 3-Level waveforms because of the large number of semiconductor devices counts. CHB is another commercialized and famous MLC topology for its simple structure and switching patterns; however, it requires an isolated DC source for generating more than 3-Levels waveform. Isolated DC sources are not interesting for the industries due to their bulkiness and cost. DC link capacitors and flying capacitors (FCs) are the solutions to remove the isolated DC sources. Although FCs have a lower size and cost compared to the isolated DC sources, they are still passive devices that must be designed in lower size to be justifiable for industrial applications. Appropriate voltage balancing integrated with the modulation technique not only is a strategy for FCs size reduction but also, simplifies the control system by removing the external controller. On the other hand, modulation strategy plays a crucial role to facilitate the complication of switching algorithms in MLCs. PS-PWM is a high-frequency modulation strategy that can be useful to reduce the size of the harmonic filters and that is a practical technique for FCs voltage balancing in MMC application.

Briefly, in this thesis, after literature review and investigation of merits and demerits of MLCs, ZPUC topology which is a single DC source single and three-phase MLC is proposed to increase the voltage levels with reduced components counts. ZPUC can be applied in both MLCs and MMCs. A voltage balancing integrated with the PS-PWM modulation technique is implemented on ZPUC-MMC to reduce the size of the FCs compared to its most popular counterpart HB-MMC. A deep-learning voltage balancer is also introduced to increase the voltage levels in ZPUC-MMC. Since PUC converter is not applicable for the three-phase system due that it requires the isolated DC source, Y-PUC configuration is introduced to address this complication. In fact, Y-PUC is a single DC source modular multilevel converter

that can also be called (PUC-MMC). This configuration is capable to handle the DC fault current due to the PUC topology is a bipolar converter.

An exhaustive conclusion for each chapter is organized as follows:

First, the popular types of MLCs including CHB, NPC, and FC have been reviewed in chapter 1. Their structure, switching states and operation have been studied and due to their simple structure and control to generate a 3-L waveform, they have a large number of applications for wind turbines, solar panels, STATCOM, motor drives, electric vehicles and so forth. Thereafter, FCs topologies and their families have been examined to show that how the isolated DC sources in CHB can be addressed. The hybrid topologies which are often the hybrid of HB, NPC, and FC, have been surveyed and it can be seen that they generate more voltage levels. However, they often require isolated DC sources or a large number of flying capacitors which cause a complex control method for voltage balancing. MMCs have also been investigated in this chapter to figure out that which submodules are more applicable for high voltage and medium voltage applications. HB-MMC and FB-MMC are the commercialized types of MMCs that are used in HVDC, STATCOM, by Siemens, Alstom, ABB, etc. Nevertheless, needing a high amount of switching devices and FCs in the mentioned MMCs is a challenging issue. Modulation strategies including PS-PWM, LS-PWM, and SVM have been explained which play a crucial role in voltage balancing in MMCs and MLCs.

In chapter 2, ZPUC unipolar topology which has been filed as a US provisional patent in 2019, is introduced to achieve the higher voltage level with reduced components counts. ZPUC is a general topology in which the output waveform level increases exponentially through adding one cell similar to PUC topology. However, the simplest type of ZPUC which generates 5-Level is selected as a submodule of MMCs. ZPUC-MMC is an appropriate alternative for HB-MMC due that it requires lower components counts, lower power losses, lower gate drives and simplest controller, and more reliability. For the medium voltage and high-power applications, ZPUC-MMC is a better alternative rather than HB-MMC due that it generates more voltage levels and consequently it needs a lower harmonic filter size. ZPUC application is for motor

drives, STATCOM, electrical vehicles, wind farms, and solar plants. Voltage balancing integrated with PS-PWM is proposed in this chapter to trigger the switches and regulate the FCs without additional controllers. It has been illustrated that the circulating current is controlled through a voltage balancing algorithm and without an extra controller. However, to remove it completely, an external controller must be designed. Two ZPUC submodules have been designed and constructed in the GREPCI lab and the control method has been implemented on two 3 KVA ZPUC-MMC through dSpace. The experimental results validate the performance of the converter to balance the voltage on FCs and generating high-quality waveform in transient and steady states.

An increased voltage level waveform has been proposed in chapter 3 based on the deep-learning voltage balancing control method. In fact, deep-learning-based voltage balancing integrated with hybrid LS-PWM and PS-PWM with one modulating signal has been carried out for FCs voltage balancing and consequently to generate the high-quality voltage waveform. Three categories of deep learning methods including 3-Layer Neural-Network, Fully Connected Neural Network, and Convolutional Neural Network are employed to train the data. Simulation results show that the Convolutional Neural Network method is the most appropriate to implement on ZPUC-MMC. Deep-learning voltage balancer is trained in steady states and the experimental results which have been obtained by implementing the proposed method on ZPUC-MMC through dSpace in the Lab show its performance in transient states as well as steady-state. In addition, it should be noted that the DC link voltage is divided among the arm submodules in HB-MMC, FC-MMC, FB-MMC, and the other MMCs. While it is divided among the leg submodules in ZPUC-MMC that alleviate the voltage stress in ZPUC-MMCs.

Although PUC is a cost-effective and simple topology for a single-phase system, it requires an isolated DC source for a three-phase system. Thus, in chapter 4, the Y-PUC configuration has been introduced as a single DC source three-phase PUC. In addition, Y-PUC is a modular multilevel converter that is constituted by PUC submodules. Due that PUC is a bipolar converter, Y-PUC is capable to block the DC fault current and it does not need the external DC circuit breaker. The comparison among the various types of MMCs and Y-PUC has

demonstrated that it is a cost-effective topology with lower semiconductor devices, lower FCs, and lower power losses compared to its counterparts. HVDC transmission line system is one of the principal applications of modular Y-PUC where FB-MMC has currently dominated as a unique topology. Simulation and experimental results show the performance of Y-PUC converter in steady and transient state in DC source, modulation index, and load variations.

RECOMMENDATIONS

In this thesis, two general topologies of the multilevel converter including ZPUC, and Y-PUC to reduce the counts of the component and increase the voltage levels have been proposed. These topologies are the novel categories of MMCs which a large number of research projects can be focused on them to develop and to address their complications. A number of suggestions have been organized for future works as follows:

Single module of ZPUC converter for all applications

In recent research work, ZPUC has been introduced as a submodule of MMC and it requires two submodules of ZPUC in a simple type. In (S. Arazm & Al-Haddad, 2021) authors introduce a single DC source three-phase converter with a single module of ZPUC; however, its application is limited to the inductance loads such as STATCOM. Developing this topology or designing a control method to address this complication will have a valuable contribution.

ZPUC-MMC as a battery charger

ZPUC-MMC has already been developed as an inverter; however, battery-charger is currently being extended all around the world due to the future prospect of electric vehicles and the replacing of gasoline vehicles with electric vehicles. Thus, the operation of ZPUC-MMC or a single module of ZPUC as a battery charger will be greatly interesting.

Various types of application on ZPUC converter:

Investigation, development, and operation of ZPUC in each following application will be a new project that will be valuable to continue due that this is a reduced components counts converter with a high-quality waveform: HVDC, motor drive, STATCOM, active filters and so forth.

Circulating current control of ZPUC-MMC and Y-PUC

Although the circulating current control has been addressed in this research work with the voltage balancing integrated to the modulation technique, it can be also controlled separately with an external controller to be eliminated completely. Thus, an investigation among the circulating current controllers which have already been implemented on popular MMCs like HB-MMC and developing new ideas according to the modeling of ZPUC-MMC and Y-PUC will be a novel project.

All issues related to the MMCs

Reliability, DC fault handling, various types of control methods such as predictive control and robust and resilient AI-based controls can be employed on ZPUC-MMC and Y-PUC for the motor drive or HVDC applications.

Hybrid Y-PUC to reduce the power losses and components counts

One of the essential research projects to continue in future works is proposing the hybrid Y-PUC with half-bridge or ZPUC so as to handle DC fault current as well as reduced component counts. The hybrid FB-MMC and HB-MMC have already been discussed which could be employed to utilize for Y-PUC.

Resilient AI controllers for balance the capacitor voltages on Y-PUC and ZPUC

The robustness of the deep learning controller against the variation in input data such as input voltage and current has been investigated in this research work. However, proposing a resilient AI controller in order to remove the voltage and current sensors, are highly interesting and stability of the controller due to the aging and designing the AI-based controller independent from the probable change of the system would be a very hot topic subject for future work.

APPENDIX I

GENERALIZED PS-PWM WITH CASE STUDY ON PUC5

A generalized phase shift modulation which has been introduced in this research work (S. Arazm et al., 2018a, 2018b), has been implemented on the PUC5 inverter based on the algorithm of figure-A I-1. The states will be selected according to table 4.1.

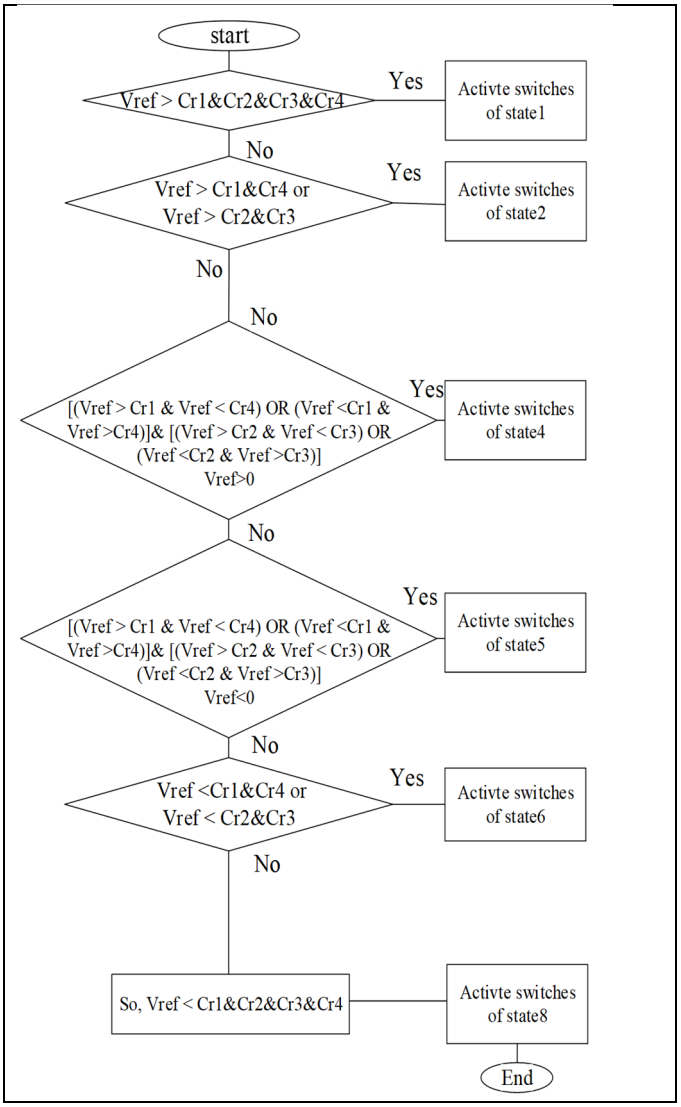

Figure-A I-1 PS-PWM design algorithm on PUC5 inverter

It should be noted that application of this algorithm on single-phase PUC5 inverter which has been shown in figure-A I-2, balance the voltage on flying capacitor without needing the voltage sensor.

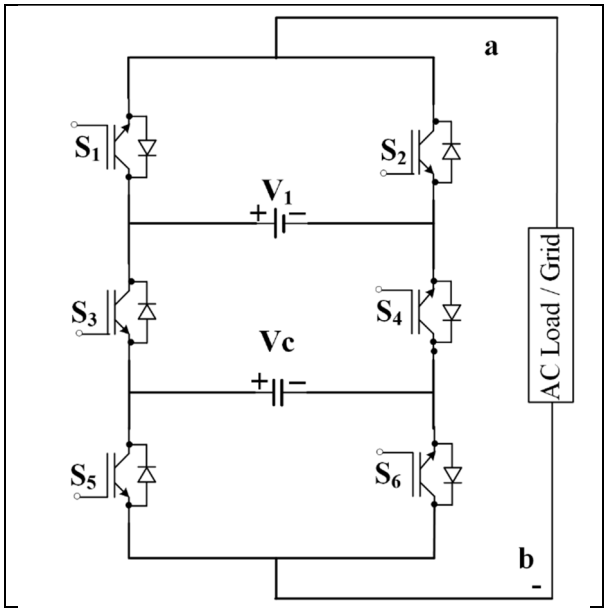

Figure-A I-2 PUC5 converter topology

Mathematical analysis of PS-PWM on PUC5 Inverter

In this section, the mathematical analysis of the designed PS-PWM on the PUC5 inverter is described and the main advantage of this strategy is demonstrated which is shifting the harmonics to the higher orders. Generally, each periodic function could be extended by the Fourier series to analyze the harmonic components. In the modulation strategy, there are two periodic waves (carrier and reference signal) and the output pulses are produced through their comparison. If f(x) and f(y) are functions of high-frequency carrier and fundamental frequency reference wave, respectively, and also $x=\omega ct+\theta c$, $y=\omega 0t+\theta 0$, then the Fourier series by double variable to analyze harmonic components for f(x,y) is given by:

$$
\begin{aligned}
&f(x,y) = f(t) = \frac{A_{00}}{2} \\
&+\sum_{n=1}^{\infty} A_{0n}\cos[n(\omega_0 t+\theta_0)] + B_{0n}\sin[m(\omega_0 t+\theta_0)] \\
&+\sum_{m=1}^{\infty} A_{m0}\cos[n(\omega_c t+\theta_c)] + B_{m0}\sin[m(\omega_c t+\theta_c)] \\
&+\sum_{n=1}^{\infty}\sum_{m=-\infty}^{\infty} [A_{mn}\cos[n(\omega_0 t+\theta_0)+m(\omega_c t+\theta_c)] \\
&+B_{mn}\sin[n(\omega_0 t+\theta_0)+m(\omega_c t+\theta_c)]]
\end{aligned}
\qquad \text{(A I-1)}
$$

Where ω_c, ω_0, are angular frequency of carrier and reference wave respectively. θ_c , θ_0 are phase angle of carrier and reference wave respectively. ,A_{mn} and B_{mn} are the coefficient of Fourier series which are defined by:

$$
\begin{aligned}
A_{mn} &= \frac{1}{2\pi^2}\int_{m=-\pi}^{\pi}\int_{n=-\pi}^{\pi} f(x,y)\cos(mx+ny)dxdy \\
B_{mn} &= \frac{1}{2\pi^2}\int_{m=-\pi}^{\pi}\int_{n=-\pi}^{\pi} f(x,y)\sin(mx+ny)d_x d_y
\end{aligned}
\qquad \text{(A I-2)}
$$

If $\omega_c t$ varies between $-\pi$ to $+\pi$, and reference voltage is M $\cos(\omega_0 t+\theta_0)$, thus f(x,y) changes from E to zero when the domain *n* changes from $-\pi/2(1+M\cos y)$ to $\pi/2(1+M\cos y)$. M is modulation index. Therefore, equation (A I-2) could be rewritten by following equation:

$$
A_{mn} + JB_{mn} = \frac{1}{2\pi^2}\int_{y=-\pi}^{y=\pi}\int_{x=-\frac{\pi}{2}(1+M\cos y)}^{x=\frac{\pi}{2}(1+M\cos y)} Ee^{J(mx+ny)}dxdy \qquad \text{(A I-3)}
$$

By substituting of the equation (A I-3) in equation (A I-1), Fourier series for node voltage (Holmes & Lipo, 2003) is given by:

$$
\begin{aligned}
V_i(\mathrm{t}) &= \frac{E}{2} + \frac{E}{2} M \cos(\omega_0 \mathrm{t} + \theta_0) \\
&+ \frac{2E}{\pi} \sum_{m=1}^{\infty} \frac{1}{m} \mathrm{J}_0(\mathrm{m} \frac{\pi}{2} \mathrm{M}) \times \cos[\mathrm{m}(\omega_c \mathrm{t} + \theta_c)] \\
&+ \frac{2E}{\pi} \sum_{m=1}^{\infty} \sum_{n=-\infty}^{\infty} \frac{1}{m} \mathrm{J}_n(\mathrm{m} \frac{\pi}{2} \mathrm{M}) \times \sin([\mathrm{m}+\mathrm{n}] \frac{\pi}{2}) \\
&\times \cos[\mathrm{m}(\omega_c \mathrm{t} + \theta_c) + \mathrm{n}(\omega_0 \mathrm{t} + \theta_0)]
\end{aligned}
\qquad \text{(A I-3)}
$$

Where 2E is the voltage at the DC source and E is the voltage balanced on the auxiliary capacitor. M is the modulation index, ω_0 is the reference signal frequency, m is the carrier index variable, n is the baseband index variable and J is the Bessel function. The details of the Bessel function have been explained in (Holmes & Lipo, 2003). In fact, Vi(t) is the obtained voltage each through comparison between one carrier and one reference voltage. Application of PS-PWM on PUC5 inverter requires four carriers which are placed in 0°, 90°, 180°, and 270°. Through subtracting of two voltages which are achieved by comparing between the reference voltage and two carriers with 180° phase shift, the following equation is obtained:

$$
\begin{aligned}
&V_{diff\,(0,180^\circ)}(\mathrm{t}) = V_{diff\,(09,270^\circ)}(\mathrm{t}) = \\
&\frac{4E}{\pi} \sum_{m=1}^{\infty} \sum_{n=-\infty}^{\infty} \frac{1}{2m} J_{2n-1}(\mathrm{m}\,\pi\,\mathrm{M}) \cos([m+n-1]\pi) \\
&\times \cos(2\,\mathrm{m}[\omega_c t + \theta_c]) + (2\,\mathrm{n}-1)\omega_0 t)
\end{aligned}
\qquad \text{(A I-4)}
$$

In last step, two obtained voltages $V_{diff\,(0,180)}$ and $V_{diff\,(90,270)}$ are added together to achieve V_{ab} as the output voltage waveform of the PCU5 inverter. Indeed, this voltage includes five voltage levels from -2E to 2E which its harmonic components can be analysed by following equation:

$$
\begin{aligned}
V_{ab}(\mathrm{t}) &= \frac{4E}{\pi} \sum_{m=1}^{\infty} \sum_{n=-\infty}^{\infty} \frac{1}{2m} J_{2n-1}(\mathrm{m}\,\pi\,\mathrm{M}) \cos([m+n-1]\pi) \\
&\times [\cos(2\,\mathrm{m}\,\omega_c t + (2\,\mathrm{n}-1)\omega_0 t) + \cos(2\,\mathrm{m}\left[\omega_c t + \frac{\pi}{2}\right]) + (2\,\mathrm{n}-1)\omega_0 t)]
\end{aligned}
\qquad \text{(A I-5)}
$$

Two last terms of equation (A I-5) are added and solved as the following:

$$\sum_{i=1}^{2}\cos(2\,\mathrm{m}\left[\omega_c t+(\mathrm{i}-1)\frac{\pi}{2}\right])+(2\,\mathrm{n}-1)\omega_0 t)] \\ =2\cos\frac{m\pi}{2}\times\cos(2\,\mathrm{m}\,\omega_c t+(2\,\mathrm{n}-1)\omega_0 t)+\frac{m\pi}{2}) \tag{A I-6}$$

Equation (A I-6) gives the fact that if m index is odd then equation (A I-5) will be zero due to the term of cos (mπ/2). Thus, m index should be even and could be defined by 2k. Since m index at equation (A I-5) includes natural number, multiple of m at last term of this equation is multiplied by 2. Thus, a simplified equation is derived by the following:

$$V_{ab}(\mathrm{t})= \\ \frac{4E}{\pi}\sum_{m=1}^{\infty}\sum_{n=-\infty}^{\infty}\frac{1}{2m}J_{2n-1}(\mathrm{m}\,\pi\,\mathrm{M})\cos([2m+n-1]\pi) \\ \times\cos(4\,\mathrm{m}\,\omega_c\,\mathrm{t}+[2\,\mathrm{n}-1]\omega_0\,\mathrm{t}) \tag{A I-7}$$

Equation (A I-7) demonstrates the fact that sidebands harmonics by (2n-1) multiples of reference frequency are located around the fourth multiples of the carrier frequency. The parameter n is started from -∞ to +∞ shows that sideband harmonics are equally spread above and below the central carrier harmonic. A prominent advantage of using phase-shift modulation technique on multilevel converters like PUC5 is its role to shift the harmonic component to the higher orders. Equation (A I-7) demonstrates how phase shift strategy could shift the harmonic component to higher orders. Obviously, the first prominent harmonic order of a 5-level waveform would appear at four times the carrier frequency because of the term $4\omega_c$ in this equation.

Experimental Results

A 5 kW prototype of PUC5 inverter has been built to validate the designed PS-PWM technique with sensor-less voltage-balancing. The algorithm shown in figure Figure-A I-1 has been implemented on dSpace 1103 as real-time controller and switching pulses are sent to the PUC5

switches through the dSpace 1103 interface board. Parameters used in experimental test have been listed in table-A I-1. Modulation index in these simulations has been set to 0.9.

Table-A I-1 System Parameters

DC source voltage	200V
RL load	40Ω, 20mH
Switching frequency	300 Hz
Capacitor	2200µF

Figure-A I-3 shows the 5-level voltage at the output of PUC 5 as well as output current and flying capacitor voltage in steady state. Voltage at the flying capacitor is balanced without any sensor on half of the DC source with ripple less than 4%.

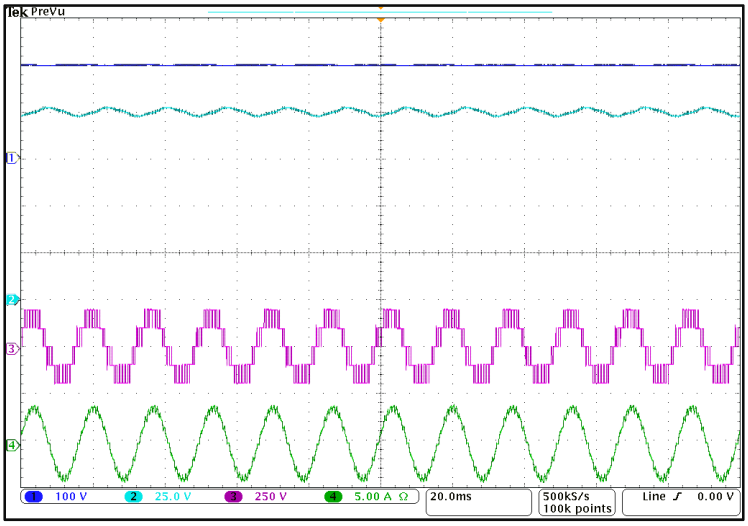

Figure-A I-3 Output voltage and current, and FC voltage

Figure-A I-4, and A I-5 shows transient response of PUC to load and DC source variations.

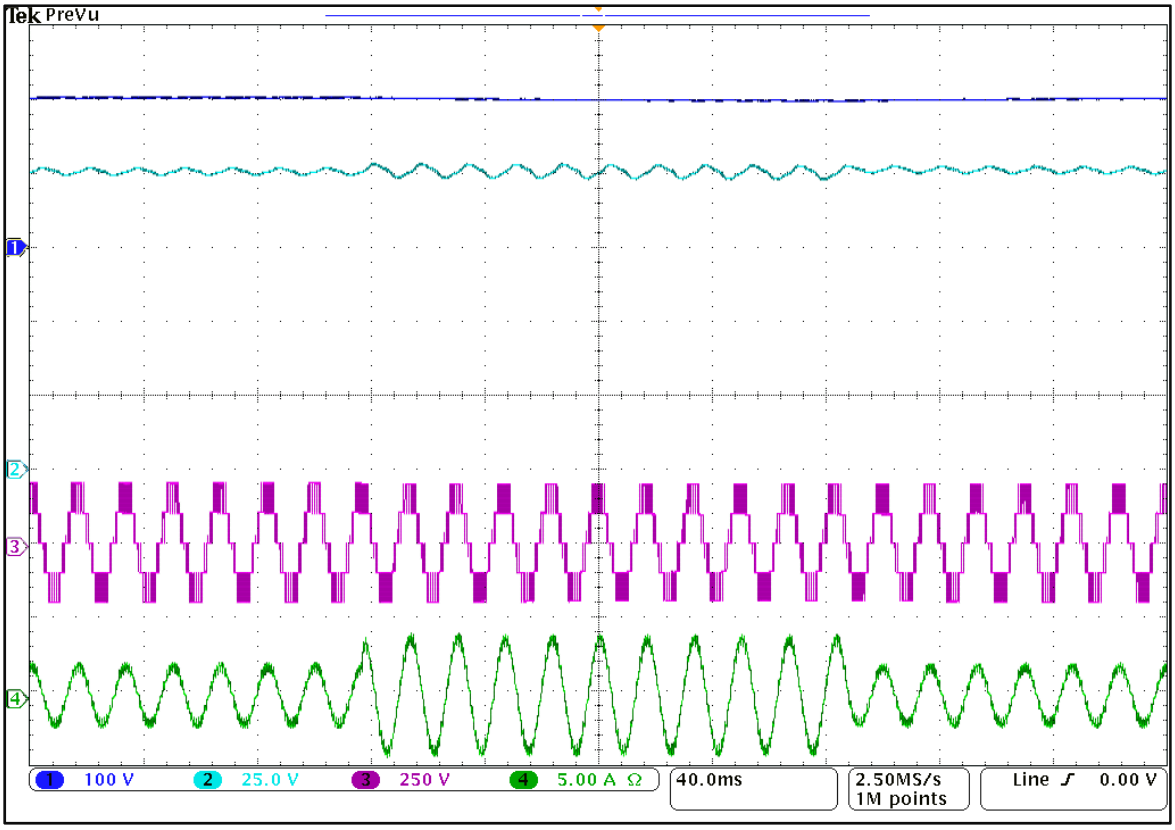

Figure-A I-4 load variation from 80 ohms, 20mH to 40ohms ,20mH

Finally, the inverter output voltage waveform has been analyzed by AEMC power analyzer and results are captured as depicted in Figure-A I-6. The 20th order sidebands harmonics are clear in that figure as the first dominant harmonics group. This result demonstrates that the first dominant harmonics are the 17^{th} and 21^{st} which are the sideband of the 1200 Hz. This latter is 4 times the carrier frequency which was regulated to 300 Hz. The 5-level voltage waveform has a low THD of almost 28% when operating at 300 Hz switching frequency without using an additional external filter.

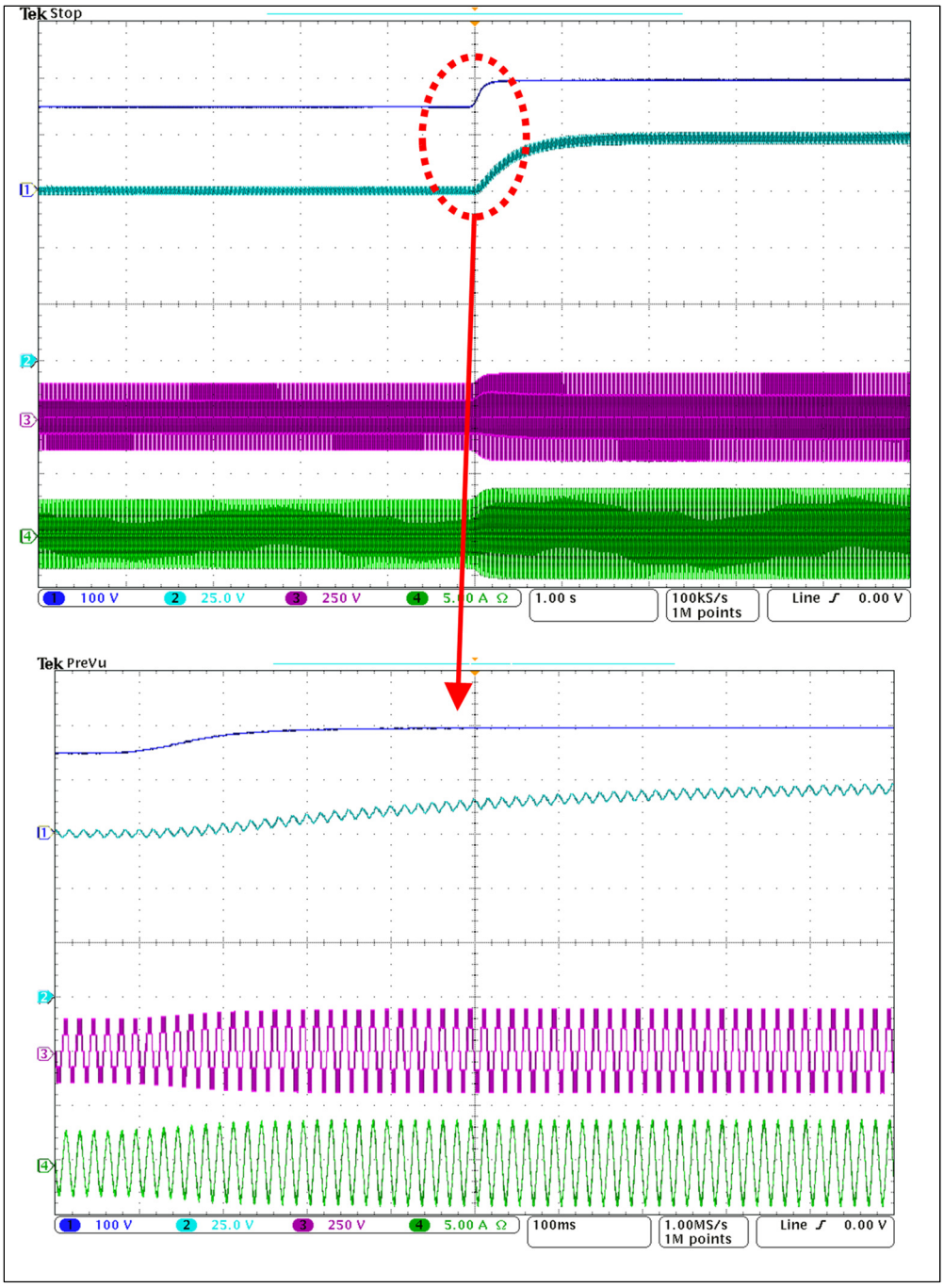

Figure-A I-5 Changing on DC source voltage from 150V to 200V

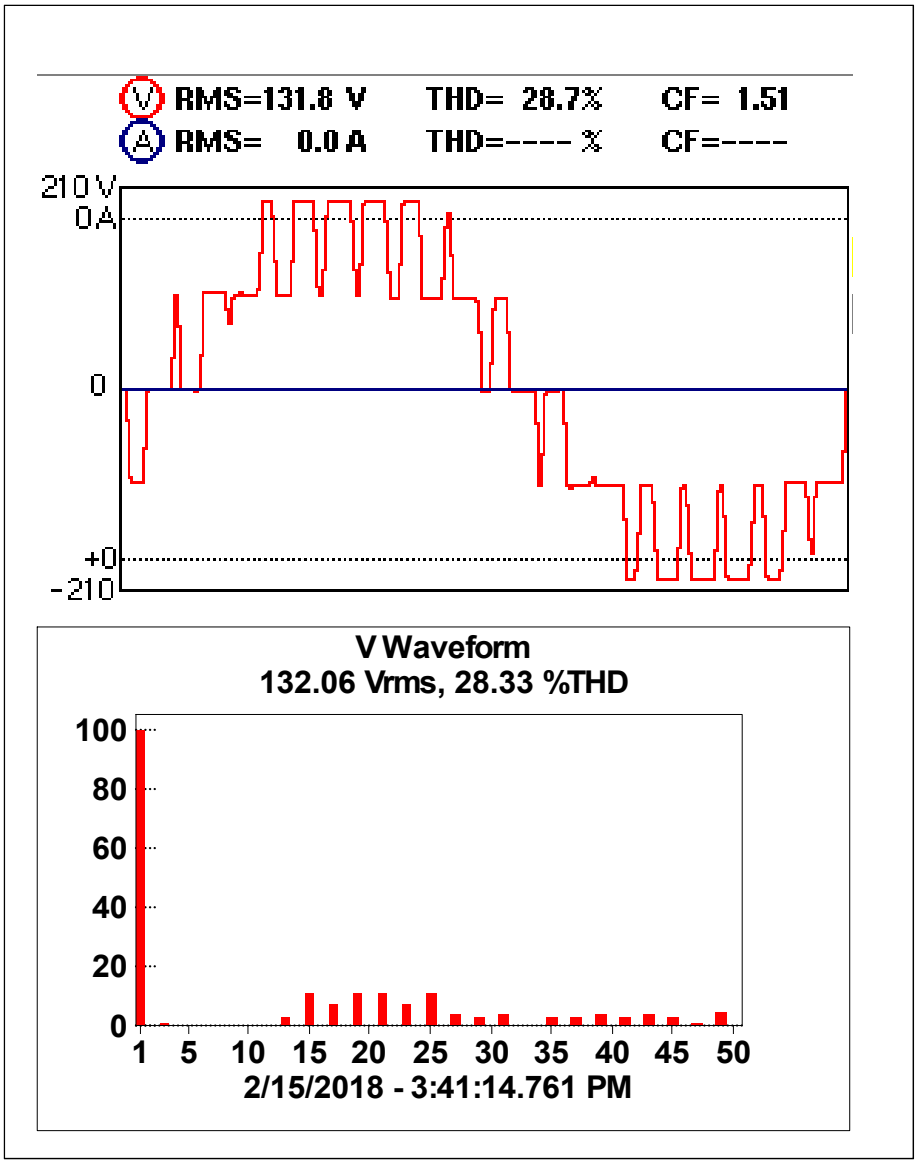

Figure-A I-6 Voltage THD at carrier frequency 300HZ on power analyser

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