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MULTI-STANDARD RF FRONT-END FOR AVIONIC SYSTEMS

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FOREWORD

The Consortium for Research and Innovation in Aerospace in Québec (CRIAQ) is a nonprofit consortium founded in 2002. It was established with the financial support of industry and university toward carrying out collaborative industry research projects at university. CRIAQ's objectives are to improve knowledge of aerospace industry through education by training students in university. It improves competitiveness by enhancing knowledge on aerospace technology. ÉTS is involved in a number of CRIAQ projects and that project was carried as part of the CRIAQ AVIO404 project. The title of the AVIO404 project is 'Multi-Standard Antenna design and in-situ implementation of multi-standard RF front-end'. Bombardier Aerospace is the lead company involved in the project. Another partner in the project is MDA Corporation. In addition, in this project, students and professors from the École Polytechnique, Concordia, and the École de technologie supérieure are involved. The main objectives of the project are the development and validation of techniques and methodologies for verifying, testing and designing multi-standard antennas and RF frontends to reduce aerodynamic issues such as drag, weight and aero acoustic noise.

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There are no proper words to convey my deep gratitude and respect for my thesis and research advisor, Professor Ammar Kouki. He taught me the skills to successfully formulate and approach a research problem. I would also like to thank him for being an open person to ideas, and for encouraging and helping me to shape my interest and ideas.

I would like to thank my family, especially my wife for always believing in me, for their continuous love and their supports in my decisions. Without them, I could not have made it here.

MULTI-STANDARD RF FRONT-END POUR SYSTÈMES AVIONIQUES

Seyyed Hassan MOUSAVI

RÉSUMÉ

Les problèmes aérodynamiques tels que la trainée, le poids ou le bruit aéro-acoustique sont des facteurs importants lors de l'évaluation de l'impact d'une antenne donnée sur la performance globale. Ils sont directement liés à la consommation en carburant, la vitesse et la portée de l'avion considéré.

Le centre d'intérêt de ce projet porte sur l'architecture électronique de la tête de réception RF. L'objectif principal étant de ramener l'équipement radio de l'avion aussi proche que possible à l'antenne afin de minimiser le poids des câbles de transmission et la complexité du circuit. Ceci demande une réduction drastique de l'équipement radio. Pour cela, les prérequis du récepteur au niveau système doivent être investigués selon la largeur de bande, débit binaire, etc. afin d'identifier les applications pour les quelles ces réductions vont être réalisables et bénéfiques.

De ce fait, l'emphase a été portée sur une analyse sur les différentes topologies qui peuvent satisfaire les spécifications. Pour chaque architecture, la tête de réception a été étudiée par rapport aux pré-requis circuit/composant. Pour chaque cas de figure, la performance, le cout, et les analyses techniques du risque sont discutés. Ensuite, la conception et le prototypage des composants clés de la tête de réception choisie sont investigués. La technologie multicouche LTCC est ensuite envisagée pour un plus grand risque mais plus avantageuse d'un point de vue réduction de volume. Au final, nous avons intégré et testé la tête de réception, d'abord en caractérisant chaque composant à part puis en considérant le sous-système global.

Mots clés: Systèmes avioniques, Récepteur multistandard, Technologie LTCC, Filtre bibande, coupleur-filtre bi-bande.

MULTI-STANDARD RF FRONT-END FOR AVIONIC SYSTEMS

Seyyed Hassan MOUSAVI

ABSTRACT

Aerodynamic issues such as drag, weight and aeroacoustic noise are important factors in evaluating the impact of a given antenna on an aircraft's overall performance. These factors are directly related to aircraft fuel consumption, speed and range. This project's focus is on RF front-end electronics.

The main goal here is to bring aircraft radio equipment as close as possible to the antennas in order to minimize wiring weight and complexity. This calls for a drastic volume reduction of the radio equipment. To this end, the system level requirements for the RF front-ends in terms of frequency bandwidths, data rates, etc, are first investigated in order to identify applications where the proposed volume reductions are the most beneficial and feasible.

Following this, the focus was on an architectural investigation of alternative topologies that can meet the specification. For each topology considered the front-end-level specification need to be translated to circuit/component level requirements. For each case, performance, cost and technical risk analyses are carried out. Then, the design and prototyping of key RF front-end circuits for the selected architecture are undertaken. The multilayered Low Temperature Co-fired Ceramic (LTCC) technology had to be considered as a high risk but more advantageous option in terms of volume/weight reduction. Finally, we aimed at integrating and testing the proposed RF front-end chain, first by characterizing each component individually, and then as a whole front-end subsystem.

Keywords: Avionic Systems, Multi-Standard Receiver, LTCC Technology, Dual-Band Filter, Dual-Band Coupler-Filter.

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LIST OF ABREVIATIONS

DRFS	Direct RF Sampling
LTCC	Low Temperature Co-fired Ceramic
DBPF	Dual Band-Pass Filter
DBC	Dual Band Coupler
DBCF	Dual-Band Coupler-Filter
SRF	Self-Resonance Frequency
SVC	Single Via Connection
MVC	Multiple Via Connection
IC	Integrated Circuit
VHF	Very High Frequency
UHF	Ultra High Frequency
ADC	Analog to Digital Converter

INTRODUCTION

The trend in modern wireless systems is continuously moving towards higher integration of multiple services that operate at various frequencies. For example, today's smart phones integrate such systems as Long-Term Evolution (LTE), Bluetooth, Wireless Local Area Network (WLAN), and Global Positioning System (GPS) which operate between 1.5 and 2.6 GHz. The new handsets will have to also accommodate new frequencies at the recently freed 700 MHz band (LaMore 2008).

In avionic systems, a similar situation exists in terms of the multitude of navigation and communication services that must be provided over various frequencies, particularly at Very High Frequency (VHF)/Ultra High Frequency (UHF) bands. However, unlike smart phones and other modern wireless devices, avionics systems have lower levels of integration and considerably more redundancy. Still, in both cases, as well as in other radio systems that use multiple frequencies, increasing integration and reducing part count are highly desirable for cost, size, weight and power reasons. One important way of achieving these goals is by increasing the functionally of RF circuits and circuit blocks but in the smallest form factor possible. Increasing functionality can be accomplished by using circuits that offer dual-band or multi-band coverage for a given functionality or, in certain cases, dual-band coverage but with dual-functionality. Increasing integration and reducing the form factor, on the other hand, require the use of advanced circuit fabrication techniques and technologies.

In radio transceiver design, the frequency of operation dictates the method of passive components implementation, whose quality factors are critical to product success. At higher frequencies distributed elements dominate. However, as we move lower in frequency, the wavelength becomes correspondingly longer and distributed elements become too large to be practical. Therefore lumped element implementation has to be chosen to make the circuits compact. However, RF lumped elements typically have poor quality factor, limiting circuit efficiency (Lopez-Villegas, Samitier et al. 2000).

Dual-band structures abound in the literature; see for example (Cheng and Fai-Leung 2004, Cheng and Fai-Leung 2005, Yong-Xin, Ong et al. 2005, Joshi and Chappell 2006, Hyunchul, Byungje et al. 2010) where various dual-band structures for filters and couplers are proposed. In these works, the periodic properties of transmission lines, coupled with some second harmonic adjustment techniques such as adding open or short parallel stubs at the output ports, are used to obtain a dual-band behavior. Such structures are suitable only for high frequencies since the size of the stubs would be impractical at VHF/UHF frequencies.

As for dual-function structures, no literature could be found showing dual-function passive circuits like coupler, and filter, in one structure. This may be due to the fact that classical RF front-end architectures are built on specific functional blocks and only dual frequency behavior is considered at best. In this chapter, the motivation for this work along with the related objectives and challenges are described. The contributions of this work to the field of Electrical Engineering are listed. Finally, the organization of thesis is presented.

Motivation and Challenges

Focusing on avionic systems, it is clear that future generation aircraft will be designed with an increased emphasis on energy efficiency, which calls for reductions in weight, air drag, vibration and noise (Bombardier 2004). As stated in (Mousavi and Kouki 2014) to meet this goal, the antenna count must be reduced by replacing several antennas with single multi-band units. This in turn will require the development of new multi-standard radio equipment, therefore new RF front-ends. Currently, RF and radio equipment is made up of bulky and heavy boxes usually placed under the cockpit and connected to the antennas by several long cables, adding weight and cost. Designing multi-standard transceivers that can be placed close to the multi-band antennas, i.e., in-situ, is one option that can help meet the objective of reducing drag, size, weight and cost (Bombardier 2004). While on the digital side new SDR (Software Defined Radio) techniques make the implementation of multi-standard transceivers relatively easy, developing new compact and multi-band RF front-ends poses an important challenge both at the level of the front-ends' architecture and the circuit fabrication technology (Yuce and Lu 2004, G. Lamontagne 2012). Each component of the receiver described in this thesis will be unique and include improvements to the state-of-the-art that will classify this work as novel. The main goal of this thesis is to design an RF front-end to cover all VHF/UHF bands of avionic systems.

The main challenges associated with achieving the goals are listed below:

Using Direct RF Sampling method in VHF/UHF application.

Direct RF Sampling (DRFS) method is the final goal for all the receivers. Since the sampling frequency of Analog to Digital Converters (ADC) are limited, down-conversion from RF to IF is usually used in receivers. According to the state of the art of ADC in Instruments (2010), this method is feasible in VHF/UHF applications because the sampling frequency is more than maximum operation frequency.

Overcoming the size performance trade-off

This is common reality in the field of microwave engineering. Desired method and optimization techniques are required to minimize the penalties of miniaturizing of passive components.

The design of high Q and Self-Resonance Frequency (SRF) passive components

Filters and couplers are passive components that rely on low-loss capacitors and inductors for good performance. High Q/high SRF inductors are typically the most difficult to design. As there are no such things, careful techniques are needed to increase SRF.

Package and interconnect design

To link all system components, low-loss interconnections are required. These connections should also be isolated from external radiation sources and create a minimum of spurious radiation.

Research Objective

This work is undertaken at LACIME lab, a leading provider of Low Temperature Co-fired Ceramic (LTCC) technology for component implementation. The objective of this work is to advance the state of the art of VHF/UHF avionic receiver modules through a LTCC implementation of a Direct RF Sampling (DRFS) receiver front-end whose dimensions are significantly smaller than current designs. Central to accomplishing this objective is a task of combining different circuits into one multi-band/multi-function circuit to optimize performance, reduce size, and maximize the potential for commercialization. LTCC multilayer technology is utilized to this end. The specific research objectives of this work are as follows:

- 1- investigate and compare DRFS receivers versus conventional receivers such as, heterodyne, and zero-IF as applied VHF/UHF avionic systems;
- 2- propose a suitable DRFS receiver to cover all the VHF/UHF bands of avionic systems;
- 3- design novel embedded dual-band and dual-band/dual-function passive components (filters, couplers) for the proposed DRFS receiver;
- 4- implement and extremely miniaturize a complete DRFS receiver front-end with active components on the surface of a LTCC substrate.

Thesis Contributions

The major contributions of this thesis are listed below:

New receiver architecture for VHF/UHF avionic systems

A new architecture for Multi-Standard Direct RF Sampling Receiver based in VHF and UHF bands of avionic system is proposed. The system comprises mainly the RF Front-End receiver chain for RF amplification and gain control, and the RF signal sampling through Analog to Digital Conversion. This new approach allows weight reduction and consequently improves fuel consumption, speed and range (S. Hassan Mousavi 2011).

Novel embedded L-C resonator

A novel way for combining inductors with capacitors, to form new L-C resonator topologies, is proposed. A toroidal structure is used for inductors and multiple parallel plates are used for capacitors in LTCC (Mousavi, Elzayat et al. 2012).

Novel techniques for Q and SRF improvement for passive components

Novel techniques to increase the Self-Resonant Frequency (SRF) of parallel plate capacitors and toroid inductors are presented. A new capacitor interconnection technique is proposed and shows 23% increase in SRF. Judiciously placed air cavities are proposed for toroid inductors and lead to a 22% increase in SRF. All inductors and capacitors are designed and fabricated in LTCC technology with very small form factor (Mousavi and Kouki 2014).

New compact and dual-band LTCC passive components

A new architecture for a compact dual-band coupler suitable for avionic systems operating in the VHF and UHF bands is proposed. The structure is implemented using lumped inductor and capacitor elements (Mousavi and Kouki 2014). Two new dual-band filters are also designed and implementaed using lumped elements (S. Hassan Mousavi 2015). The smallest reported for VHF/UHF dual-band filter, dual-band 90-degree hybrid coupler are demonstrated. Extreme miniaturization is achieved through novel packaging using DuPont 951 LTCC substrate material.

New compact and dual-band/dual-function LTCC passive components

A new architecture for compact and dual-band coupler-filter suitable for avionic systems operating in the VHF, 108-137 MHz, and UHF 329-335 MHz, bands is proposed. A systematic design methodology for this structure is presented whereby, starting with a distributed branch-line coupler, equivalent lumped element models are generated and augmented to obtain the desired functionality. The resulting topology of interconnected

inductors and capacitors are designed in LTCC technology with very small form factor (Mousavi and Kouki 2015).

Receiver front-end integration

The smallest implementation of a VHF/UHF receiver front-end is reported. In this structure all the passive components are designed in LTCC and the active components are mounted on the surface.

Thesis Organization

This thesis is organized in a way that follows the design flow for the Direct RF Sampling (DRFS) receiver. In Chapter 1 a literature review of conventional transcivers and also the state-of-the-art transcivers are provided and a DRFS receiver is proposed. The lumped element dual-band filters design for proposed receiver are presented in Chapter 2 along with a detailed literature review of dual band-pass filters. Chapter 3 discusses the methods to increase the Self-Resonant Frequency (SRF) and Quality Factor (Q) of inductors and capacitors. In Chapter 4, two new dual-band coupler and dual-band coupler-filter are designed and charactrized along with a design methodology for dual-band coupler-filter. Chapter 5 focuses on the implementation of complete RF front-end module. Finally, a conclusion of the thesis is provided.

CHAPITRE 1

LITERATURE REVIEW

In this chapter, avionic systems and their specifications are explained. Then, the conventional artichectures of transmitters are reviewed and the performances are compared. Finally the proposed architecture for VHF/UHF avionic systems and its system-level simulations are presented.

1.1 Existing Avionic Systems

An aircraft during the flight needs to be controlled to avoid disasters such as colisions, crash, etc. Figure 1.1 shows how the aircraft communicates with ground stations while figure 1.2 shows the existing antennas on most aircrafts (Bombardier 2004). Each one of these antennas is assigned to specific task, such as VOR/LOC for navigation, TCAS for monitoring and etc.



Figure 1.1 Airplane communication with ground stations Adapted from Bombardier (2004)



Figure 1.2 Various antenna in aircraft Adapted from Bombardier (2004)

By replacing multiple antennas with only one multi-standard antenna requires new RF frontends that fit the new antenna. Therefore development of new custom circuits, such as filters and multiplexers, that can meet the multiband/wideband operation requirements are necessary (Bombardier 2004).

The choice of transceiver architecture is one major decision that directly affects the overall cost, power, number of external components, receiver sensitivity, and selectivity. The main design issues and trade-offs in a transceiver are mainly in the analog front end, where it is desired to process a certain channel in the presence of a strong interferer. The main signal processing operations required before demodulation are: 1) frequency translation from the RF frequency to the baseband; 2) signal amplification and filtering to amplify the weak received signal while rejecting the surrounding interferers; and 3) digitization for further demodulation of the signal in the DSP. All the previous operations or any combination of them can be done in the digital or the analog section. This will depend on the location of the

ADC in the receiver chain. Therefore we need to have good knowledge about the transceiver architectures before choosing the architecture for our target.

In traditional implementation of multi-standard transceivers, multi-standard operation is achieved with independent RF front-ends supporting each standard. This approach needs to be revised since cost, size and weight increase as the number of target standards increases. A multi-standard transceiver should be comparable with a single standard transceiver in size, cost, and power consumption.

Before starting to study the transceiver architectures, it is useful to be familiar with the spectrum of avionic frequency bands that is shown in figure 1.3.



Figure 1.3 spectrum of avionic frequency bands Adapted from Bombardier (2004)

The frequency operation of most aircraft antennas is from AM band to X-Band, and this is a very wideband frequency range. However, most the aircraft antennas operate at relatively low frequencies, *i.e.*, VHF and UHF bands and given the close frequency operation of these bands, we have focused on VHF & UHF bands. As we can see in the figure 1.3, there are
various services in the VHF and UHF bands in modern avionic systems. The Emergency Locator Transmitter (ELT) antenna is for navigation system and it was used in both VHF & UHF bands, but in new generation of avionic systems it operates only in UHF band.

Antenna Type	MB	LOC	VOR	VHF/COM	GS	ELT
Frequency Range (MHz)	75	108- 112	108-118	116-137	329.15-335	406.025
Operation	Receive Only	Receive Only	Receive Only	Receive & Transmit	Receive Only	Transmit Only
Modulation Type	%95 AM	30% AM	30% AM	30% AM	30% AM	
RxMin Signal (dBm)	-61	-86	-93	-87	-76	NA
RxMax Signal (dBm)	-13	-33	-27	-7	-33	NA
Tx Signal Level (W)	NA	NA	NA	16 (class 3 & 5) 4 (class 4 & 6)	NA	
Rxmin SNR (dB)	15	20	6	6 (for input - 87dBm) 25 (for input -61 to -27 dBm)		NA
Maximum allowable BW for RF filter for Noise Floor (MHz)		2	11	43		

Table 1.1 Transceiver specification for VHF and UHF bands

Therefore there are four antennas in the VHF band. MB, VOR/LOC and GS antennas only operate as receiver and VHF/COM operates as both receiver and transmitter.

In the VHF & UHF bands size, and weight requirements will pose significant challenges if one is to achieve the desired level of integration. Multilayer LTCC technology enables RF modules to be reduced significantly by taking advantage of the three dimensional flexibility. Compared to a conventional two dimensional PCB, LTCC allows higher density, reduced size, and lower cost. Therefore we will be using LTCC technology for our future filter design.

Before starting to find the best solution for multi-standard transceiver, we need to know the specification of each system separately and the unique architecture must meet the specification of all systems. For this reason a spreadsheet has been made for the VHF, UHF and L-Band and has been filled out based on some RTCA Documents (Documents) as maximum as possible. This datasheet has been shown in table 1.1.

In the next section, we will overview of receiver and transmitter architectures to be familiar with the potentiality of them for multi-standard purpose.

1.2 Receiver Architecture

Before choosing architecture for multi-standard RF front-end, we need to have good knowledge about various architectures and see which structure is the best one for our task. Therefore first we need to review all existing architectures and compare the benefits and drawbacks of them.

Linearity, noise figure and power consumption are three main parameters that must be considered carefully. As it is shown in figure 1.4 selecting one criterion will not fit to others.



Figure 1.4, Trade-off among transceiver parameters

Herein we will explain briefly different architecture for transceivers.

1.2.1 Heterodyne Receiver:

The heterodyne receiver architecture is the most widely used in the past decade. In this architecture, the signal band is translated to intermediate frequency (IF), so as to relax the Q required of the channel-select filter. This translation is carried out by a down-conversion mixer.

One of the seriously difficulties in heterodyne architecture is image problem. The image power can be much higher than of the desired signal, requiring proper image rejection. As shown in figure 1.5 the common approach to suppressing the image is using an image rejection filter, placed before the mixer. This filter should have a small loss in the desired band and a large attenuation in the image band, two requirements that can be simultaneously met is $2\omega_{IF}$ is sufficiently large (B.Razavi 1998).



Figure 1.5 Image rejection by means of a filter Adapted from Razavi (1998)

As mentioned before, the principle idea of heterodyne architecture is that the desired signal is down-converted to the low frequency to relax the channel-selection filter, requiring a sufficiently low ω_{IF} . The choice of IF therefore depends on trade-offs among three parameters: the amount of image interfieres, the spacing between the desired band and the image, and the loss of the image-reject filter. To minimize the image, we can either increase the IF frequency or tolerate greater loss in a filter while increasing its Q.

From the above discussion, we can see that there is a trade-off between image rejection and channel selection. Since the image degrades the sensitivity of the receiver, we say the choice of the IF entails a trade-off between sensitivity and selectivity.

An important drawback of the heterodyne architecture is that the image-reject filter is usually realized as a passive, external component. This furthermore requires that the preceding stage -the LNA- drive the 50 Ω input impedance of the filter, inevitably leading to more severe trade-offs between the gain, noise figure, stability, and power dissipation in the LNA.

As shown in figure 1.6 to resolve the trade-off between sensitivity and selectivity, the concept of heterodyning can be extended to two down-conversions, called Double-IF topology (Mak, U et al. 2007).



Figure 1.6 Double-IF RX Adapted from Mak (2007)

The RF signal captured at the antenna is first filtered against the out-of-band interference, and then the in-band signals are amplified and down-converted to a lower center frequency IF (a few ten of MHz). A high-Q off-chip image-rejection filter prevents the image channel from being superimposed into the desired channel in the RF-to-IF down-conversion.

A high-Q off-chip Surface-Acoustic-Wave (SAW) filter as an IF filter after the first downconversion is used to partially select the wanted channel while rejecting the unwanted channels. The signal level of the selected channel is properly adjusted by a programmablegain amplifier (PGA) prior to the IF-to-baseband (BB) quadrature down-conversion. This down-conversion requires a Phase-Locked Loop (PLL) and a quadrature VCO (QVCO) for generating the in-phase (I) and the quadrature phase (Q) components. The BB low-pass filters require low-Q but high orders for ultimate channel selection. The BB PGAs adjust the signal swing for an optimum-scale Analog-to-Digital (ADC) conversion.

The advantages of heterodyne architecture are the avoidance of DC-offset and 1/f noise problem. These are realized from the superior I/Q matching because of low operation frequency.

The disadvantages of this architecture are the low integration level and high power consumption because of the off-chip filters. From the multi-standard point of view, due to the restricted IF choice for commercial filters and from that the image-reject filters and IF SAW filters are not possibly to be shared among the different standards, heterodyne architecture is not a good choice for multi-standard receiver design.

1.2.2 Image-Reject receivers Receiver: Hartley and Weaver

The trade-offs governing the use of image-reject filters in heterodyne architectures have motivated RF designer to seek other techniques of suppressing the image. To eliminate such filters, Hartley suggested the architecture shown in figure 1.7 (Mak, U et al. 2007).



Figure 1.7 Hartley RX Adapted from Mak (2007)

Hartley's circuit uses two matched mixers and mixes the RF signal with the quadrature phases of the LO frequency, $Sin(\omega_{LO}t)$ and $Cos(\omega_{LO}t)$, and then are filtered by the LPFs, finally one of them shifted by 90 degrees and added them together. It can be shown (B.Razavi 1998) that the image will have opposite polarity at the summation, and the signal has a same polarity. Thus the image will be canceled out after summation.

The principle drawback of this architecture is its sensitivity to gain and phase mismatches between two paths. If the LO phases are not in exact quadrature or the gain and phase shifts of the upper and lower paths are not identical, then the cancellation is incomplete and the image corrupts the down-converted signal (B.Razavi 1998). In practice the 90 degrees phase shift is replaced with a +45 degrees shift in one path and a -45 degrees shift in the other. Figure 1.8 shows the Hartley architecture whit an RC-CR network that often utilized for this purpose.



Figure 1.8 Hartley receiver with split phase shift stage Adapted from Razavi (1998)

The Weaver architecture as shown in figure 1.9, is identical to Hartley's one except that the 90 degrees phase shifter is replaced by a quadrature down-converter (Mak, U et al. 2007).



Figure 1.9 Weaver RX

Adapted from Mak (2007)

The Hartley and Weaver architectures share one problem: incomplete image rejection due to gain and phase mismatch. The Weaver circuit is free from the gain imbalance (B.Razavi 1998), but it suffers from the secondary image if the second down-conversion translates the spectrum to a nonzero frequency. Also, harmonics of the second LO frequency may down-convert unfiltered interferes from the first IF to the second.

1.2.3 Zero-IF Receiver:

Similar to an image-rejection RX, a zero-IF obviates the need to use any off-chip component. Shown in figure 1.10 is a zero-IF receiver, where the desired channel is translated directly to the baseband through the I and Q paths. In this architecture the image signal is not a serious problem, because the image band is itself the desired band, on the other hand, IF=0. Therefore here the mismatch of two paths is not very important and the demanded I/Q matching is particularly achievable for most applications (Mak, U et al. 2007).



Figure 1.10 Zero-IF RX Adapted from Mak (2007)

The main limitation of the zero-IF RX is its high sensitivity to low frequency interference, i.e, DC-offset. The LO leakage to the input of mixer and vice versa will cause self-mixing in the down-converter and producing an unwanted DC-signal in the output of mixer. The value of this DC-signal may be high and desensitize all of following circuits. Moreover, due to the

poor isolation from substrate coupling, ground bounce, bond wire radiation and so on, the LO leakage may reach LNA input and produce an even stronger result. This effect presents an obstacle against the integration of LO, mixer and LNA on a single silicon substrate. Figure 1.11 is shown a schematic of LO leakage to the input of mixer and LNA.



Figure 1.11 LO leakage Adapted from Razavi (1998)

Another severe problem in zero-IF architecture is the 1/f flicker noise problem. Since the frequency of LO signal is the same with RF signal, the corner frequency of 1/f noise is high compared to the second-conversion stage of heterodyne architecture and thus will corrupt the useful signal specially for narrow-channel signal (e.g. channel bandwidth of GSM signal is only 200KHz).

A capacitive-coupling and a servo loop are common choices to alleviate this problem, but at the expense of long setteling time and large chip area for realizing the very low cut-off frequency high-pass pole.

1.2.4 Low-IF Receiver:

Low-IF conversion receiver down-convert the RF signal to a very low intermediate frequency (typically one or two channels) instead of DC. Therefore the low-IF RX features a

similar integratability as the zero-IF one, but is less susceptible to the low frequency interference. By down-converting the RF signal to low IF, problems in the zero-IF architecture like a high level of the 1/f noise and DC offsets are avoided as these low frequency noises can be removed by a DC notch filter or a high-pass filter without severely deteriorating the modulated channel. Meanwhile, due to the low Q requirement, the IF SAW filter in the heterodyne receiver can be replaced by an active filter (Crols and Steyaert 1998).

Unlike the zero-IF, the image is not the desired channel itself. The required image rejection is normally higher as the power of the image can be significantly larger than that of the desired channel. This architecture does not use any image rejection SAW filter and the image rejection is done after the down-conversion by the IF polyphase filter or double quadrature mixers (Crols and Steyaert 1995, Crols and Steyaert 1998). Depending on the position of the building blocks, a low-IF RX can have more than one possible architecture, as shown in figure 1.12(a) to 1.12(d).



Figure 1.12 Low-IF Receivers Adapted from Mak (2007)

In all of these architectures the RF signal is divided into quadrature branches during the down-conversion. In case (b) and (c) an IF polyphase filter is used to suppress the image interfere after the down-conversion. The channel selection is then performed with a band-

pass filter (Crols and Steyaert 1998). Generally speaking, a low-pass filter is sufficient if IF is very close to DC, but a band-pass filter removes also DC offsets and is also preferable.

In case (a) and (d) a low-pass filter is used to select the desired channel but does not suppress the image interfere, and image rejecting will do by double quadrature mixers. In all of these architectures a double quadrature mixer is used for image rejecting and down-converting the IF to BB signal, and after that for eliminating the secondary image problem uses a DC notch or a high-pass filter.

By changing the position of this double quadrature mixer the specification of the PGAs and ADCs will vary, and we can choose one of these structures with respect to the available PGA and ADC.

1.2.5 Comparison of Different RX Architectures:

Table 1.2 gives a summary of the presented RX architectures. Their characteristics determine their appropriateness for modern wireless communication systems.

Rx Architecture	Advantages	Disadvantages
Superheterodyne	+Reliable performance +Flexible frequency plan +No DC-offset and 1/f noise	 Expensive and bulky, high power Difficult to share the SAW filter for multistandard Low multi-standard ability
Zero-IF	+Low cost +Simple frequency plan for multistandard +High integrability +No image problem +High multi-standard ability	-Quadrature RF-to-BB downconversion -DC-offset and 1/f noise problems -Suitable only for wide channel bandwidth
Low-IF	+Low cost +High integrability +Small DC-offset and 1/f	-Image is a problem -Quadrature RF-to-IF and double-quadrature IF-to-downconversion

Table 1.2 Summary of different RX architecturesAdapted from Mak (2007)

noise	-Suitable only for narrow channel bandwidth		
+High multi-standard ability			

1.2.6 Digital Receivers:

A multi-standard receiver should have enough flexibility and programmability to be applied to different standards. The concept of software-defined radio (SDR) is an emerging technology enabling the development of flexible multi-standard/multi-user systems, reconfigurable and adaptable by software. This flexibility is achieved by performing all of signal processing in software. As shown in figure 1.13 the original idea in SDR is to place the ADC right after the antenna, and then all of the filtering will be done digitally on-chip (Yuce and Lu 2004).



Figure 1.13 An ideal SDR configuration Adapted from Yuce (2004)

The digitizing of the received signal will be achieved with a high performance and wide band ADC. The state-of-the-art for ADC, in 2010, is 12 bit, 1-GSPS (Giga Sample Per Second), and 2.1 GHz input bandwidth ADC. The features of this ADC are listed in figure 1.14 (Instruments 2010).

TEXAS INSTRUMENTS	ADS5400-SP			
www.ti.com	SLAS669A-SEPTEMBER 2010-REVISED NOVEMBER 2010			
12-Bit, 1-GSPS Analog-to-Digital Converter Check for Samples: ADS5400-SP				
 FEATURES 1-GSPS Sample Rate 12-Bit Resolution 2.1 GHz Input Bandwidth SFDR = 65 dBc at 1.2 GHz SNR = 57 dBFS at 1.2 GHZ 7 Clock Cycle Latency Interleave Friendly: Internal Adjustments for Gain, Phase and Offset 	 100-Pin Ceramic Nonconductive Tie-Bar Package Military Temperature Range (-55°C to 125°C T_{case}) Processed Per Internal QML Class V Assembly/Test Flow QML Class V Qualification Pending for SMD Device 			
 1.5 - 2 V_{PP} Differential Input Voltage, Programmable LVDS-Compatible Outputs, 1 or 2 Bus Options Total Power Dissipation: 2.2 W On Chin Analog Putfer 	 Test and Measurement Instrumentation Ultra-Wide Band Software-Defined Radio Data Acquisition Power Amplifier Linearization Simple Intelligence and Jamming 			
On-Onip Analog Burler	Signal intelligence and Jamming Radar			

Figure 0.14 The features of state-of-the-art for ADC Adapted from Instruments (2010)

The Nyquist theorem states that in order to replicate an analog signal in the digital domain, it must be sampled at no less than twice the frequency of its highest frequency component. Therefore we can conclude that this mentioned ADC can use only for the frequency range bellow about 400-500 MHz.

In (G. Lamontagne 2012) a Direct RF Sampling (DRFS) receiver was proposed for GNSS application. As shown in figure 1.15 no down-conversion (mixer) and channel selection filters are used in receiver path. All the incoming signals will go through RF filters and amplifiers to reach a reasonable magnitude for conversion to the digital by ADS. This architecture is an example of DRFS, but it can only cover one system and it is not designed for multi-standard purposes.



Figure 1.15 Direct RF sampling receiver Adapted from Lamontagne (2012)

Another approach for digital receivers is shown in figure 1.16, where the first IF signal is digitized, mixed with the quadrature phases of a digital sinusoid, and low-pass filtered to yield the quadrature baseband signals. This approach is sometimes called a "digital-IF architecture". Note that digital processing avoids the problem of I and Q mismatch.



Figure 1.16 Digital-IF receiver Adapted from Razavi (1998)

In this architecture the partial performance limitation of ADC's can be alleviated because working in a lower frequency, but now still linearity, noise floor, and dynamic range requirement may necessitate a greater resolution than of the state-of-the-art ADC.

Another approach that can alleviate performance limitation of ADC's is subsampling technique. The idea is that a bandpass signal with bandwidth Δf can be translated to a lower band if sampled at a rate equal to or greater than $2\Delta f$. The images resulted from subsampling are located at the frequencies $f_{Im}=(kf_s\pm f_{in})$, where f_{in} is the input signal frequency, f_{Im} is the image frequency, f_s is the sampling frequency, and k is an integer number. Figure 1.17 is showing a time and frequency domain of signal before and after subsampling.



Figure 1.17 Subsampling: (a) time domain representation, (b) the RF or IF input spectrum after bandpass filtering, (c) signal images after subsampling Adapted from Yuce (2004)

Subsampling suffers from an important drawback: aliasing of noise. The problem arises in practice due to the fact that the front-end BPF cannot completely remove all of out-of-band white noise. Therefore, during transferring the replicas of the signals the out-of-band noise

will fall on top of each other. Subsampling by factor of M (i.e. $M = f_{in}/f_s$) will approximately multiply the out-of-band noise power by a factor 2M (one spectrum from negative and one from positive side). The overlapped noise is desired to be less than the white Gaussian noise. Another issue associated with subsampling front-end is its sensitivity to the jitter due to sampling clock that can cause degradation on the system performance. The aperture jitter on the sampling clock results in phase noise and its spectral density is amplified by M^2 . The maximum allowed input frequency of the ADC will also be limited by aperture jitter. The ADC's SNR imposed by sampling jitter can be specified by (Yuce and Lu 2004):

$$SNR_{i} = -20\log(2\pi f_{in}t_{a}) \tag{1.1}$$

where t_a is the aperture jitter for the sampling clock. As can been seen, even the system is operating at a frequency lower than the input frequency f_{in} in subsampling front-end, the jitter is still a function of f_{in} . The theoretical SNR degrades as the input frequency increases.

The defined two problems (the overlapped noise and clock jitter) associated with subsampling systems are only significant when the subsampling coefficient M is very large. However, if the input signal frequency to the ADC, f_{in} , is low enough (by using one down conversion stage to decrease the carrier frequency), then those two effects can be ignored.

1.3 Transmitter Architecture

An RF transmitter performs modulation, up-conversion, and power amplification. In contrast to the variety of approaches invented for RF reception, transmitter architectures are found in only a few forms. This is because issues such as noise, interference rejection, and band selectivity are more relaxed in transmitters than in receivers. For instance, in transmission, only one channel will be up-converted in the TX. Its power level is well-determined throughout the TX path. There are differences in the signal reception, the power of the incoming signals is variable and the desired channel is surrounded with numerous unknown-power in band and out-of-band interferences. Thus, PGAs is essential for the RX to relax the

dynamic range of the ADC, but can be omitted in the TX if the power control could be fully implemented by the power amplifier (PA).

Similarity, since the channel in the TX is progressively amplified toward the antenna and finally radiated by a PA, the linearity of the whole TX is dominated by the PA whereas it is the noise contribution of the LNA that dominates the whole RX noise figure.

1.3.1 Superheterodyne Transmitter:

Architecturally, the superheterodyne TX is a reverse of operation from its RX counterpart with the A/D conversion replaced by a digital-to-analog (D/A) conversion. However, they are very different in the design specification.

This architecture is used image rejection filter and therefore is not suitable for multi-standard transmitter. Block diagram of this architecture is shown in figure 1.18 (Mak, U et al. 2007).



Figure 1.18 Superheterodyne TX Adapted from Mak (2007)

1.3.2 Direct-Conversion Transmitter:

The direct-conversion TX features an equal integratability as the zero-IF RX. As shown in figure 1.19 the modulator is followed by a power amplifier and a matching network, whose

role is to provide maximum power transfer to the antenna and filter out-of-band components that result from the nonlinearities in the amplifier (B.Razavi 1998).



Figure 1.19 Direct-conversion Transmitter Adapted from Razavi (1998)

As shown in figure 1.20 the main drawback of this architecture is "injection pulling" because of the output carrier frequency is equal with local oscillator (LO) frequency and this lead to the PA output be a modulated waveform with high power and a spectrum centered around the LO frequency.



Figure 1.20 Leakage of PA output to oscillator Adapted from Razavi (1998)

The phenomenon of the LO pulling is alleviated if the PA output spectrum is sufficiently higher or lower than the oscillator frequency. One of the proposed architecture for solving this problem is shown in figure 1.21, where the output signals of VCO₁ and VCO₂ are mixed and the result is filtered such that the carrier frequency is equal $\omega_1 + \omega_2$, far from either ω_1 or ω_2 .



Figure 1.21 Direct-conversion transmitter wit offset LO Adapted from Razavi (1998)

1.3.3 Two-Step-Up Transmitter:

As shown in figure 1.22, similar to the low-IF RX, two-step-up TXs can be structured into four possible schemes (B.Razavi 1998).



Figure 1.22 Two-step-up TXs Adapted from Mak (2007)

In these structures the input signal up-converted to the very low-IF frequency and after amplifying and filtering the second up-converter will transfer the IF signal to the RF output. In these architectures the PA output spectrum is far from VCO frequency, so there is no injection pulling problem. Another advantage is better I and Q matching because first up-conversion is done in a low frequency, and this lead to less cross-talk between the 2 bit streams.

1.3.4 Comparison of Different TX Architectures:

Table 1.3 summarizes the presented TX architectures. Similar to the RXs, their characteristics determine their appropriateness for modern wireless communication systems.

Tx Architecture	Advantage	Disadvantages
Superheterodyne	+Reliable performance +Flexible frequency plan +No LO leakage +Simple DC-offset cancellation at BB	-Expensive and bulky, high power -Difficult to share the SAW filters for multistandard
Direct-Up	+Low cost +Simple frequency plan for multi-standard +High integratability +No image problem	 -Quadrature BB-to-RF upconversion -LO leakage -DC-offset cancellation is difficult at BB (area and settling time impacts)
Two-Step-Up	+Low cost +High integratability +Simple DC-offset cancellation at BB	-Image is a problem -Quadrature IF-to-RF and double- quadratute BB-to-IF upconversions -LO leakage (depends on the IF)

Table 1.3 Summary of different	t TX architectures
Adapted from Mak	(2007)

1.4 Proposed Receiver Architecture for VHF and UHF bands

The commonly used approach for avionic system receiver RF front-end is to employ architecture for each service separately. This traditional approach suffers from mass and power consumption. By reducing the number of antennas, these receivers should be replaced by one multi-standard receiver with good compact form. An elegant solution to this problem in the VHF and UHF bands is to use of Direct RF Sampling, because the sampling frequency of the state of the art of ADC is enough to cover whole of these bands.

In the avionic system in the VHF and UHF bands the minimum received signal is -93 dBm (for the VOR/LOC system) and the maximum received signal is -7 dBm (for the VHF/COM system). It means that we have very high dynamic range of input signal power and it is not possible to cover this high dynamic range by cascading multiple amplifiers and after that an Automatic Gain Control (AGC), because the dynamic range of AGC is not enough high.

The Full Scale voltage of ADC that is supposed to be used is $1.5 V_{pp}$. This voltage for 50 Ω reference resistor is equivalent to +7.5 dBm. The 3 dB margin is needed to be considered for % 30 Amplitude Modulation (AM). So, the target power level for ADC is +4.5 dBm. By considering 3 dB losses for the input filter, the gain required depend on the input signal power should be around 14 dB to 101 dB. For performing that We have proposed two approaches.



Figure 1.23 First DRFS Prototype Architecture

In the first approach the DRFS prototype is designed with the objective of capturing all avionic signals in VHF and UHF bands. In fact, all the components have been selected to achieve this long term objective. The complete architecture of the DRFS prototype is shown on figure 1.23 with the parts identified.

The 30% AM modulated signals (-93 dBm to -7 dBm) are first captured by a multi-standard antenna before being filtered by a hypothetical filter. Then the signals (-96 dBm to -10 dBm) are amplified by a 20 dB wideband Low Noise Amplifier (LNA) from RF Micro Device, having a 1.5 dB noise figure. After that the signals (-76 dBm to +10 dBm) will split in two paths by the coupler from RF Micro Device. The nominal coupling factor is 10 dB; it means we have 10 dB losses in parallel path signals (-86 dBm to 0 dBm); and there is 1 dB loss for the direct path of coupler, so in the main path signals power range is -77 dBm to 9 dBm.

In the main path the Variable Gain Amplifier (AD8369, Analog Device) with a gain that can be set digitally from -5 dB to +40 dB, will amplify the input signals by 40 dB default gain, but when the input signal reach -35 dBm the gain should be changed to -5 dB and for input signal more than -35 dBm the gain should be constant. In this way, we used just two gain points of this VGA.

For changing the gain of VGA we need to detect the power level of signals by a Peak Detector (PD, LT5570 Digi-Key) and control the gain of VGA. The minimum power that this detector can detect is -52 dBm. In this case we need to change the gain of VGA when the signal power reaches -35 dBm. By paying attention to the coupling and directivity coefficient of coupler, this power is equivalent to around -44 dBm for the input of Power Detector (PD) that can be easily detected.

The minimum and maximum signal powers at the output of the first VGA are around -37 dBm and +5 dBm respectively. As mentioned before, the target power level for ADC is +4.5 dBm, so an AGC will adjust the 42 dB dynamic range to a certain level that is suitable for

digitalizing by ADC (+4.5 dBm). The AGC that we want to use is shown in figure 1.24. This AGC comprises two main block: one Variable Gain Amplifier (AD8367, Analog Device) with a gain that can be set through analog loop control from -2.5 dB to +42.5 dB, and one Log Amplitude Detector (AD8318, Analog Device) (Device 2007) that will calculate the average signal level and fed it back to VGA to adjust the gain to an appropriate level for a range of input signal levels. This structure for AGC has made by Analog Device Company. The AGC loop is required to set the power level at the input of the ADC so that it is not overrun while keeping a good bit resolution on the signal.



Figure 1.24 AGC block diagram Adapted from Analog Device (2007)

In the second approach, we have used logarithmic amplifier in which low power signals will be amplified by high gain and high power signals by low gain. The detailed performance of this amplifier is represented later in this thesis. The complete architecture of this DRFS prototype is shown on figure 1.25 with the parts identified.



Figure 1.25 Second DRFS Prototype Architecture

In this approach also, the 30% AM modulated signals are first captured by a multi-standard antenna before being amplified by a 20 dB wideband Low Noise Amplifier (LNA) from RF Micro Device, having a 1.5 dB noise figure. Then, the signal passes through a logarithmic amplifier from Analog Device, converting 95 dB dynamic range (-75 dBm to +17 dBm) to 20 dB dynamic range (+1 dBm to +21 dBm) of input signal. Now an AGC will adjust the 20 dB dynamic range to a certain level that is suitable for digitalizing by ADC. The AGC that is used here has been shown in figure 1.26. This AGC is like the AGC that is used for first approach, the only difference is the VGA (ADL5330, Analog Device) (Device 2005) that the gain of this AGC is from -34 dB to +22 dB.



Figure 1.26 AGC block diagram Adapted from Analog Device (2005)

The digitizing of the received signal will be achieved with a high performance and wide band ADC. The specification of the available ADC (the ADS5400-SP from Texas Instrument) is 12 bit, 1-GSPS, and 2.1 GHz input bandwidth ADC. This ADC has been selected to be used in this project because its sampling frequency is more than twice of the maximum operation frequency. This ADC will sample the signal at a rate of 700 MHz, because the maximum frequency in these bands is 335 MHz and in terms of Nyquist theorem the sampling frequency should be at least two times of 335 MHz.

There are some aspects that we need to be care about. One of them is the overall Noise Figure (NF) of system. In this architecture there is no channel selection filter in the receiver chain, and we have only band selection filter, it implies that the noise floor (KTB) that is directly proportional to the filter bandwidth, will rise, so the signals are more sensitive to the noise generated by the receivers, and so the overall NF must be kept as low as possible.

For a cascaded system, Friis (Friis 1944) has proved the cascaded NF can be expressed as:

$$\mathbf{F} = F_1 + \frac{F_2 - 1}{G_1} + \dots \frac{F_n - 1}{G_1 G_2 \dots G_n}$$
(1.2)

Where F_i and G_i are the NF and available power gain of the stage i respectively. The NF of LNA in both approaches are 1.5 dB, in the first approach NF of first and second VGA are 7 dB and 6.5 dB respectively. Using this formula the total NF should be around 1.52 dB (at maximum gain). For second approach the NF of logarithmic amplifier is 10.8 dB at maximum gain, using this formula the total NF of this proposed architecture is 1.83 dB (at maximum gain).

These two proposed architecture have advantages and disadvantages. From the linearity and NF stand points, the first one is suitable but this architecture is a little more complicate and

has more components. In second proposed architecture, there are fewer components and the NF is worsened and the main problem of this architecture is non-linearity. In this structure logarithmic amplifier has been used and its function is like LOG(x), and only for small variation in envelop $LOG(x) \approx x$, so for large variation in envelope it will make some distortions, so this architecture is more suitable for constant envelope signals. In the avionic VHF and UHF bands the %30 AM modulation type is used and the envelope is not constant, for this reason in this project the first approach is prepared.

1.4.1 Simulation Results in ADS

For designing this proposed architecture, we have chosen Advance Design System software because there are suitable components for replacing the real components.

Figure 1.27 shows the simulation schematic of the first proposed architecture in ADS. In this design Amplifier2 is used as a LNA, Amplifier VC as VGAs, AM_Demod Tuned as peak detector and OpAmp as a comparator.



Figure 1.27 Schematic of DRFS RF front-end in ADS

Figure 1.28 shows the input power sweep versus the output power of the first VGA. There are two gain for this VGA and the gain will switch to lower one for input power more than - 54 dBm (equal to -35 dBm for input of VGA). As it is shown the range of output power is between around -39 dBm to 5 dBm.

Figure 1.29 shows the result of power sweep simulation for last part of circuit (AGC), as it is shown the input power is changed from -40 dBm to 5 dBm, but the output power is around 4.3 dBm and the maximum time for being stable is around 1 usec.



Figure 1.28 Input power versus the output power of first VGA



Figure 1.29 Input and output power sweep of AGC

Figure 1.30 shows the simulation schematic of the first proposed architecture in ADS. In this design Amplifier2 is used as a LNA, Log True as logarithmic amplifier, AmplifierVC as VGA and Amp2 as op-amp for AGC loop.

As it is shown in figure 1.30, ENVELOPE simulation has been used. In this way we can increase the input power by passing time, and seeing what will happen on the output power. We expect to have constant output power while the input power sweeping from -93 dBm to - 7 dBm.



Figure 1.30 Schematic of DRFS RF front-end in ADS

Figure 1.31 shows the result of power sweep simulation, as it is shown the input power is changed from -96 dBm to -10 dBm, but the output power is around 4.5 dBm.



Figure 1.31 DRFS RF Front-End Input and Output Power Sweep

In accordance to the datasheet in Table 1.1, the minimum SNR in the LOC/VOR system, which operates between 108 and 118 MHz, is 20 dB with a minimum received signal of -86 dBm. The VHF/COM's (118 to 156 MHz) minimum SNR is 6 dB with a minimum signal of -93 dBm. The minimum SNR of GS (329.5 to 335 MHz) system is 20 dB with a minimum received signal of -76 dB. Consequently, noise figure calculations lead to a maximum bandwidth for meeting these specifications of 2 MHz for LOC/VOR while it is more than 43 MHz for VHF/COM and GS. In the circuit of figure 1.23, only one filter with more than 2 MHz bandwidth is proposed, which will not meet the above requirements. Therefore a two-path architecture is proposed as shown in figure 1.32, where the upper path is a direct RF sampling path, for VHF/COM and GS systems which are selected by a dual-band pass filter, and the lower path is a conventional down-converting receiver for LOC/VOR system which incorporates a channel select filter to relax linearity and NF specifications.



Figure 1.32 Proposed RF front-end architecture for VHF/UHF band avionic systems

The use of a multilayer integrated circuit technology, such as the low-temperature co-fired ceramics (LTCC), will be favored for such applications because high value and high quality factor (Q) passive components can easily be designed and buried into LTCC substrates.

Active components can then be accommodated on the LTCC board which contains the entire required passive component inside the substrate. For testing this receiver chain the various amplification and gain control building blocks should be soldered on individual substrates along with matching and power supply circuits.

1.5 Conclusion

Minimizing the number of external components and highly integrated solutions in LTCC technology to cover all avionic frequency bands are the final goal of this project for RF frontend transceiver. In this chapter, an architecture for VHF and UHF bands is proposed and next steps of this project is to design suitable filters and couplers for proposed receiver architecture. The feasibility of a highly integrated RF front end for avionics services in the VHF-UHF has been discussed, the study lays the ground for developing a comprehensive compact architecture for next generation avionics systems.

CHAPITRE 2

BAND-PASS FILTER DESIGN AND METHODOLOGY

This chapter presents a novel dual-band pass filter design and the implementation in a low-temperature co-fired ceramic (LTCC) package. Here, the purpose of the dual-band pass filter is to attenuate out-of-band interfere signals. Its position in the receiver chain is presented in figure 2.1.



Figure 2.1. Proposed RF front-end architecture for VHF/UHF band avionic systems

Given the three-dimensional packaging capability of LTCC, multilayer resonators are integrated into the module eliminating the need for their discrete versions. The resonators are comprised of high Q and high SRF toroidal inductors that are combined with multilayer parallel plate capacitors, forming a novel L-C resonator topology. This topology of placing the capacitor in the center of toroidal inductor allows for simultaneous area and performance optimization. The final LTCC dual-band pass filter module measures only 32 mm × 13.8 mm × 2.2 mm. The complete methodology, from initial schematic design, through individual element design, to complete device optimization is discussed.

2.1 Dual band-pass filter background

A band-pass filter is an essential building block of any wireless communication systems. Furthermore, filters with high stop-band attenuation effectively reduce interference from strong jamming signals and as a result improve the signal-to-noise-ratio in the receiver. Dualband filters can be used in multi-standard front-ends instead of two separate single band pass filters to reduce the size.

In (Miyake, Kitazawa et al. 1997) the configuration shown in figure 2.2 was employed to realize a dual-band pass filter. A dual-band band-pass filter cannot be produced by simply connecting two band-pass filters based on the identical design because the filters short at the pass-band of the other (Miyake, Kitazawa et al. 1997). External phase shifting is typically required so that impedance to the pass-band of the other filter is high and an open state is maintained.



Figure 2.2 The prior arts of dual-band bandpass filters using external phase shifting Adapted from Miyake (1997)

In (Yong-Xin, Ong et al. 2005), a new configuration of a dual-band filter, shown in figure 2.3, is presented. The dual-band pass filter consists of two connected single-band band-pass filters without the need of using external phase shifting. The two single-band band-pass filters are re-designed so that one band-pass filter has low-pass characteristic and the other has high-pass characteristic, thus one filter is open in the pass-band band of the other. The schematic of the ideal lumped element filter and its response is shown in figure 2.3 and figure 2.4 respectively.



Figure 2.3 Schematic of two single-band bandpass filters Adapted from Yong-Xin (2005)



Figure 2.4 Simulated results of the dual-band band-pass filter at 2.4 and 5.2 GHz using the circuit simulator Adapted from Yong-Xin (2005)

This filter was implemented using lumped element in LTCC substrate. The filter layout, simulation, and fabricated results are shown in figure 2.5 and figure 2.6 respectively.



Figure 2.5 Layout (3D view) of the LTCC bandpass filter
Adapted from Yong-Xin (2005)



Figure 2.6 Measured and simulated results of the dual-band filter Adapted from Yong-Xin (2005)

In (Joshi and Chappell 2006), a unique coupling mechanisms internal to the LTCC substrate to create a dual-band lumped-element filter (DBLEF) is proposed. In this paper, a compact design approach is taken, in that only a single set of lumped elements is used. The schematic of this dual-band filter, its simplified circuit in lower and upper bands, and its frequency response are shown in figure 2.7.





Figure 2.7 (a) Schematic of the DBLEF

Figure 2.7 Simplificated Circiut at (b) lower band and (c) upper band schematic. (d) Example full-wave electromagnetic (EM) response of the DBLEF Adapted from Joshi (2006)

In this paper, the authors mathematically, using the odd and even mode analysis, proved that the circuit in figure 2.7 operates as dual-band pass filter at 2.4 GHz and 5.6 GHz center frequencies. As it is shown in figure 2.8, this filter is implemented using lumped element in LTCC. The simulation and mesurment comparisons are brought in figure 2.9.



Figure 2.8 Layout of the dual-band filter. Not to scale (expanded z-axis) for clarity Adapted from Joshi (2006)



Figure 2.9 Measured and full-wave EM results for the DBLEF Adapted from Joshi (2006)

In (Brzezina, Roy et al. 2009, Brzezina and Roy 2014), a novel methodology for the design of integrated multilayer embedded components that are mutually coupled is proposed. The methodology relies on the ability to replace, in simulations, some embedded components with ideal versions whose values are fixed and immune to mutual coupling. Finally, they designed a single band-pass filter shown in figure 2.10, using their new methodology.



Figure 2.10 Fully embedded 3-D bandpass filter structure Adapted from Brzezina (2009)

They have also implemented their filter using lumped element in LTCC. The simulation and mesurement results are presented in figure 2.11.



Figure 2.11 Measured and simulated response for fully embedded filter Adapted from Brzezina (2009)

2.2 Dual band-pass filter design consideration

To design a dual band-pass filter, one cannot simply connect two single band-pass filters together unless external phase shifting is carefully added. In (Yong-Xin, Ong et al. 2005) a dual band-pass filter is proposed by connecting two single band-pass filters using two different coupling mechanisms to ensure proper phase shifting. However, the proposed structure is not sufficiently compact. In (Joshi and Chappell 2006) a different, and more compact design, is proposed in which only a single set of lumped elements is used. In (Brzezina, Roy et al. 2009), new methodology is proposed for lumped element filter designs and a simple band pass filter is designed. However, the designed filter is a conventional single band pass filter. In this chapter we propose a new connection for two single band-pass filters and additionally we propose a new implementation of the topology proposed in (Joshi and Chappell 2006) by replacing inductance coupling by capacitance coupling to make the filter design even more compact. This proposed filter uses two resonators only, each one

repeated four times, unlike (Yong-Xin, Ong et al. 2005) where three different transmission line resonators were used.

Based on the above analysis, the filters specification should be: a center frequency of 122.5 MHz with a 3-dB bandwidth of 24%, for Band I and a center frequency of 332 MHz and a 3-dB bandwidth of 1.9%, for Band II. It should be noted that a 1.9% bandwidth requires ultrahigh Q lumped components which makes the design very challenging. Based on system level calculation, we found that an 8.5% bandwidth meets system specifications while requiring moderately high Q elements.

Two capacitance coupled single band-pass filters are designed as shown in figure 2.12 Capacitance coupling is used for further miniaturization of band-pass filters. Using the conventional formulas in (Matthaei 2000), the values of lumped component of a 4th order filter at Band I and a 2nd order filter at Band II, as shown in figure 2.12, are computed for a Chebychev filter with 0.5 dB ripple and listed in table 2.1. Note that in figure 2.12 only one set of resonator, L_r-C_r for Band I and L_p-C_p for Band II, is required. Simulation results of these single band-pass filters are shown in figure 2.13.

Lumped Elements		Value	
4 th order filter at Band I	Lr	29 nH	
	Cr	29.5 pF	
	C ₁	30.75 pF	
	C ₂	15 pF	
	C ₃	12.5 pF	
	Lp	9.5 nH	
2 nd order filter	Cp	20.5 pF	
at Band II	Cu	2.8 pF	
	Cs	0.88 pF	

Table 2.1 Designed circuit values for proposed dual band-pass filter



Figure 2.12 Schematic of the (a) 4th order and (b) 2nd order single band-pass filters



Figure 2.13 (a) Simulation results of the 4th order single band-pass filters



Figure 2.13 (b) Simulation results of the 2nd order single band-pass filters

Both band-pass filters are used capacitance coupling, so both filters have low-pass characteristic, thus the upper band-pass filter is open in the pass-band band of the other, but lower band-pass filter is not open in the pass-band of the other. Therefore an external phase shifting is required. A new connection technique is proposed by adding one resonator between two filters. Since this resonator is set to resonate at upper center frequency, thus the lower band-pass filter will be opened in the pass-band of the other. Figure 2.14 shows dual band-pass filter by connecting two single band-pass filters via one resonator. This new dual band-pass filter is optimized using Microwave Office (AWR) and the result is shown in figure 2.15.



Figure 2.14 Schematic of the dual band-pass filter using resonator connection



Figure 2.15 Simulation results of the dual band-pass filter using resonator connection

Additionally, we propose a new implementation of the topology proposed in (Joshi and Chappell 2006) by replacing inductance coupling by capacitance coupling to make the filter design even more compact. This proposed filter uses two resonators only, each one repeated

four times, unlike (Yong-Xin, Ong et al. 2005) where three different transmission line resonators were used. The proposed filter design with capacitance coupling is shown in figure 2.16.



Figure 2.16 Schematic of the 4th order dual band-pass filter using for this project

Using the conventional formulas in (Matthaei 2000), the values of lumped component of a 2^{nd} order filter at Band I are computed for a Chebychev filter with 0.5 dB ripple. Then by applying the design procedure in (Joshi and Chappell 2006), the values of other lumped components in figure 2.16 are calculated and listed in table 2.2. Simulation results of this dual band filter are shown in figure 2.17 where two second-order filters were cascaded to improve overall filter rejection.

It should be noted that the use of L_a , which is independent of the lower band frequency, allows to compensate for the frequency variation of all other L and C components.

Lumped Elements		Value	
	Lr	32 nH	
2 nd order filter	Cr	29 pF	
at Band I	Ci	29.5 pF	
	Ct	15 pF	
	L _c	52 nH	
2 nd order filter	La	14.2 nH	
at upper band	C _c	15.6 pF	
	C _b	11.4 pF	

Table 2.2 Designed circuit values for dual band-pass filter



Figure 2.17 Simulation results of the dual band filter

2.3 Passive component and filter design

2.3.1 Inductors, capacitoes, and resonators design

As seen in section 2.2, the design of dual band-pass filters amounts to the design of some resonators whose L and C values have already been determined, the coupling capacitances and some single inductors. Consequently, designing individual L and C components will be the first step followed by their integration to form the required resonators. To maintain minimum size, we opt for a lumped element implementation, which is particularly suitable at our VHF/UHF frequencies. Based on the computed inductance values, a self-shielding toroid inductor is chosen for the larger values while a solenoid inductor is chosen for smaller values. Because the magnetic field in a toroid inductor is confined inside its turns, a toroid inductor can be embedded within a substrate without parasitic coupling. Using a LTCC process, various toroid inductors were designed by electromagnetic field simulations. The inner radius of the toroid was reduced to the minimum allowable by the LTCC process, dictated by the smallest via-to-via spacing. The helix shape metal is used for the lower metal to reduce the parasitic capacitors existing between to metals, thereby increasing self-resonant frequency (SRF). Table 2.3 summarizes the designed inductors.

Inductor	#of turns	Inner radius Outer radius		Inductance	
		(mm)	(mm)		
La	3.5	N/A	N/A	14.27	
Lr	10	0.7	1.7	32.44	
L _c	13	0.85	2.1	51.8	
L _p	6	0.38	0.95	9.1	

Table 2.3 List of designed inductors and their characteristics



Figure 2.18 3D view of 52nH toroid (a) and 14.2 nH solenoid (b) inductors in HFSS

To make capacitors, we use a multi-layer parallel-plate approach, which is well suited for LTCC. To achieve higher capacitance values, while controlling the overall size, we take advantage of a very thin (1.63 mils-thick after firing) LTCC tape as well as multi-layer stacking. Using this approach several capacitors were designed using parallel circular disks as summarized in table 2.4. Figure 2.19 shows an example of multi-layer capacitor in LTCC.

Table 2.4 List of designed capacitors and their characteristics

Capacitor	#of plates	Plate radius	Capacitance (pF)	
		(mm)		
Cr	8	0.78	28.8	
Ct	8	0.61	15.1	
Ci	8	0.8	29.4	
Cc	8	0.65	15.65	
C _b	8	0.49	11.55	
C_1	8	0.81	30.2	
C ₂	8	0.61	15.1	
C ₃	8	0.5	11.9	
Cp	8	0.7	20.8	
Cu	2	0.69	2.9	
Cs	2	0.48	0.9	



Figure 2.19 3D view of the 11.55 pF capacitor in HFSS

With the design of individual inductors and capacitors completed, we proceed to their integration to make parallel L/C resonators. To this end, we place the capacitors at the center of the inductors as shown in figure 2.20 to keep the size of the resonator equal to the inductor which is a minimum possible size.



Figure 2.20 3D view of the 175 MHz resonator in HFSS

2.3.2 Filter design

After completing components design, next stage is designing of whole filter by finding a way to connect components together to occupy minimum space. Figure 2.21 shows the EM model of single band-pass filters and their integration to make a dual bandpass filters. The connectors are placed in the free space between to single band-pass filters to keep the size of the dual band-pass filter to the minimum possible size.



Figure 2.21 Top view of (a) lower single bandpass, (b) upper single bandpass and (c) the complete dual band-pass filter EM model in HFSS

Figure 2.22 shows the EM model of figure 2.16 in which the shunt inductor (L_a) and parallel capacitor (C_t) are placed in the free space between resonators for further reduction of filter size.



Figure 2.22 Top view of the complete (a) 2nd and (b) 4th order dual band-pass filter EM

2.4 Fabrication and testing

All individual inductors, capacitors, resonators and whole filters were fabricated using the LTCC process with DuPont's 951AT substrate (e_r =7.8, Tan D=0.006). Several iterations (60 components) are fabricated in one quarter of substrate which is shown in figure 2.23.

Figure 2.23 Photograph of the fabricated LTCC inductors, capacitors, and resonators

Figure 2.24 shows the 52nH toroid inductor in HFSS and its photograph in LTCC substrate. The simulation and mesurement results are also shown in figure 2.25.



Figure 2.24 (a) 3D view of the 52nH inductor in HFSS and (b) photograph of the fabricated LTCC inductor



Figure 2.25 (a) Simulated and measured magnitude of the 52nH inductor



Figure 2.25 (b) Zoomed version of simulated and measured magnitude of the 29 pF capacitor

13% difference between simulated and measured result may be attributed to slight fabrication imperfections and a possible variation in the LTCC's shrinkage factor. Note that the silver metal used in this fabrication.

Figure 2.26 shows the 29.5pF parallel plate capacitor in HFSS and its photograph in LTCC substrate. Capacitor plates are buried in LTCC substrate. The simulation and fabrication results are also shown in figure 2.27. 300 MHz shift difference for SRF may be attributed to calibration.



Figure 2.26 (a) 3D view of the 29.5pF capacitor in HFSS and (b) photograph of the fabricated LTCC capacitor



Figure 2.27 (a) Simulated and measured magnitude of the 29.5pF capacitor and (b) its zoomed in version

The 3D model of 175 MHz resonator and a photograph of the fabricated resonator are also shown in figure 2.28. The capacitor is buried inside the substrate.



Figure 2.28 (a) 3D view of the 52nH inductor in HFSS and (b) photograph of the fabricated LTCC inductor

The input impedance of the fabricated resonators was measured using the Agilent 8722ES Network and a probing station. Comparison between simulation and measured (fabricated) results are shown in figure 2.29. The resonant frequency is shifted to 184 MHz after fabrication. This 5% shift may be attributed to slight fabrication imperfections and a possible variation in the LTCC's shrinkage factor.



Figure 2.29 Simulated and measured magnitude (a) and imaginary part (b) of the resonator's input impedance



Figure 2.30 Photograph of the fabricated LTCC (a) lower single bandpass filter, (b) upper single bandpass filter and (c) dual bandpass filter

A photograph of single band-pass filters at Band I, II and their integration are shown in figure 2.30. The capacitors used in figure 2.30b are two-layer capacitors while for the figure 2.30a they are 8-layer capacitors. The s-parameters of the fabricated filter were measured

using the same mentioned network and probing station. Comparison between simulation and measured results are shown in figure 2.31. The insertion losses for HFSS simulation for the lower and upper band-passes are 1.1 dB and 2.6 dB respectively. Fabrication results show 0.2 dB more insertion loss for lower and upper band-passes.



Figure 2.31 Simulated and measured results for (a) upper single bandpass filter, (b) lower single bandpass filter



Figure 2.31 Simulated and measured results for (c) dual bandpass filter

A photograph of dual bandpass filter for option 2 is also shown in figure 2.32. All of the capacitors are buried inside the substrate. The s-parameters of the fabricated filter were measured using the same mentioned network and probing station. Comparison between simulation and measured (fabricated) results for both 2^{nd} and 4^{th} order filters are shown in figure 2.33.



Figure 2.32 Photograph of the fabricated (a) 2nd and (b) 4th order LTCC DBPF

The insertion loss for HFSS simulation for the lower and upper band-passes are 0.7 dB and 1.4 dB respectively in 2nd order filter and 1.6 dB and 2.9 dB respectively for 4th order filter. As it was expected the insertion loss for 4th order filter is twice of the 2nd order filter. Fabrication results show 0.1 dB more insertion loss for lower and upper band-passes in both filters.



Figure 2.33 Simulated and measured results for (a) 2nd order and (b) 4th order bandpass filter

2.5 Conclusion

Dual band-pass filters are designed to select the VHF/COM and GS systems. Inductors, capacitors, resonators comprising a toroid inductor and a multilayer capacitor, and finally two fully embedded dual band-pass filters are designed and fabricated in LTCC substrate. Simulation and fabrication results are in good agreement.

CHAPITRE 3

SRF IMPROVEMENT FOR PASSIVE COMPONENTS

Passive circuits such as filters and couplers for low frequency applications, especially in the VHF/UHF bands, should be implemented using lumped elements to achieve maximum circuit-size and weight reduction. Because of the low frequencies of operation, these lumped components must have much higher values than those that would be needed at high frequencies for comparable reactance. However, increasing lumped component values usually leads to a decrease in their Self-Resonant Frequency (SRF) due to parasitics. Consequently, high value capacitors and inductors usually suffer from low SRF, which may lead to more loss and thus lower quality factor.

For lumped capacitors, one may use an interdigital topology (Marquez-Segura, Casares-Miranda et al. 2006), a parallel plate approach (Brzezina, Roy et al. 2009) or surface mount components (Hoppenjans and Chappell 2009). While they can be compact, interdigital capacitors are usually limited in value, less than 2pF in (Marquez-Segura, Casares-Miranda et al. 2006), and thus suitable for high frequencies only. Parallel plate capacitors offer the potential of high capacitance values and may be used at low frequencies if their SRF can be maintained sufficiently high. In (Brzezina, Roy et al. 2009), parallel plates were used to realize 2-3pF capacitors at 1.5 GHz for GPS applications. Simulation of these structures showed that their SRF is on the order of 4GHz. In (Hoppenjans and Chappell 2009), highvalue surface mounted capacitors were used in a tunable filters with LTCC-integrated inductors at VHF frequencies though they were not fully integrated within the LTCC.

For lumped inductors, one may use a spiral topology (Ukaegbu, Kwang-Seong et al. 2011), a solenoid inductor (Aliouane, Kouki et al. 2011) or toroid inductor (Hoppenjans and Chappell 2007, Hoppenjans and Chappell 2009). Spiral inductors are suitable for high frequency applications and small inductance values since higher values require bigger size (Ukaegbu, Kwang-Seong et al. 2011), leading to lower SRF and Q. In (Aliouane, Kouki et al. 2011), a

solenoid inductor was used to realize 2-7nH inductors at 2 GHz. The simulated SRF values for these inductors were in the range of 4-7 GHz. In (Hoppenjans and Chappell 2007) a toroid inductor was designed but had poor Q and low SRF. In (Hoppenjans and Chappell 2009) high value toroid inductors, up to 190nH, were reported and used in a tunable filter design for which measured results were presented. Only simulated values were given for inductance, Q and SRF, e.g., L=75nH, Q=60, SRF=710MHz.

Based on the above discussion, parallel plate capacitors and toroid inductors offer the best option for achieving high capacitance, C, and inductance, L, values. Furthermore, such components can be realized in a highly compact form factor by using a suitable circuit fabrication technology with size reduction and high integration density (3D) such as LTCC. In this chapter, we realize high value L/C components using LTCC and we address their SRF limitations through the judicious use of interconnects and air cavities in the LTCC stack.

3.1 Capacitor and inductor design

3.1.1 Capacitor design

Parallel plate capacitors have well known dependence on geometry and material dielectric. For a given permittivity, achieving high capacitance values requires large plate areas and/or small spacing between them. LTCC is well suited to this end since it offers both small spacing, i.e., with layers as thin as 1.63 mil post firing, and large areas, through multi-layer stacking. Using a LTCC stack of 8 thin layers, various capacitors were designed using HFSS. These capacitors are typically connected though single vias (see figure 3.1a) as was done in [2], which are highly inductive. Therefore, to improve the SRF, special care has to be given to the interconnection of the various capacitor layers. Here we introduce multiple parallel vias as interconnects (see figure 3.1b) to reduce inductance. The parallel connection of these vias reduces inductance as well as resistance, thus increasing SRF and Q. We used 7 vias for each connection, which is the maximum we could achieve while respecting the design rules. Table 3.1 summarizes the characteristics of the designed capacitors.



Figure 3.1 Three-dimensional view of (a) single via-connected (SVC) 22pF capacitor and (b) multiple via-connected (MVC) 28pF capacitor

Capacitors		Plate radius (mm)	Simulated Capacitance (pF)	Simulated SRF (MHz)	
C1	SVC	1.1	41	330	
	MVC	1.1	48	410	
C2	SVC	0.9	22	560	
	MVC	0.9	28	690	
C3	SVC	0.75	10	1250	
	MVC	0.75	14	1600	

Table 3.1 Designed capaciors and their charactristics

As shown in Table 3.1, the same size plates were used for both MVC and SVC. However, given the higher area overlap in MVC due to multiple vias, a higher capacitance is obtained. Figure 3.2 shows the simulation results comparing the capacitance value of SVC and an MVC versus frequency for 0.9mm plate radius. Clearly the MVC offers both higher capacitance (28 pF vs. 22 pF, a 27% increase) and higher SRF (690 MHz vs. 560 MHz, a 23% improvement).



Figure 3.2 Simulated single and multiple via connected capacitors

3.1.2 Inductor design

Toroid inductors, see figure 3.3, are self-shielding and can achieve high inductance value due to their ability to concentrate the magnetic field as shown in figure 3.3b. This property is useful for minimizing inductor coupling; hence they can be placed close to each other enabling a high level of integration particularly in LTCC technology. Using 3D field simulation, i.e., HFSS, we designed and optimized several toroid inductors. Table 3.2 lists the parameters of some of the designed inductors.



Figure 3.3 Fields inside a 45nH toroid inductor: (a) Side view showing the electric field (b) top view showing the magnetic fields

Inductor		#of turns	Inner radius (mm)	Outer radius (mm)	Inducta-nce (nH)	SRF (MHz)
L1	Regular	13	0.72	3.6	80	375
	Cavity under	13	0.72	3.6	80	460
L2	Regular	11	0.72	3	45	580
	Cavity under	11	0.72	3	45	710
L3	Regular	9	0.72	2.6	25	990
	Cavity under	9	0.72	2.6	25	1200

Table 3.2 List of designed inductors and their charactristics

The larger dimensions of high value inductors lead to greater parasitic capacitances that reduce the SRF. By examining figure 3.3a, one can identify two main sources of parasitic capacitance: (i) electric energy stored between the top and bottom toroid metals, and (ii) electric energy stored between the bottom metallization and the ground plane. Thus, to reduce these capacitances, we introduced air cavities in the middle and under of toroid inductor and assessed their impact on the SRF by simulation. Figure 3.4 shows the three simulated configurations while figure 3.5 presents the simulation results. As can be seen from figure 3.5, placing an air cavity in the middle of the inductor improves the SRF marginally while placing the air cavity underneath it leads to a significant increase in the SRF (710 MHz vs. 580 MHz, a 22% improvement). This clearly indicates that the electric field is denser underneath the toroid than between its turns as illustrated by the electric field distribution of figure 3.3a. Furthermore the inductors with an air cavity underneath are much easier to fabricate in LTCC than those with air inside. Referring to figure 3.3a, the air cavity to be added should cover the area of highest electric field intensity. It should therefore extend beyond the outer diameter of the toroid. We used a cavity that is 10% larger than the outer diameter of the toroid.



Figure 3.4 3D view of a 45nH toroid inductor (a) without air cavity, (b) with air cavity in the middle and (c) with air cavity underneath



Figure 3.5 Simulated results for the inductor configurations of figure 3.4

3.2 Fabrication and testing

To validate the proposed techniques for increasing the SRF of capacitors and inductors, midrange L and C values were selected, i.e., C2 and L2 from tables 3.1 and table 3.2, respectively. All were fabricated using DuPont's 951AT substrate ($\epsilon r=7.8$, Tan $\delta=0.006$). Figure 3.6 show photographs of the fabricated single and multiple via-connected capacitors while figure 3.7 shows those of the fabricated toroid inductors.



Figure 3.6 Photographs of the fabricated LTCC (a) single via-connected capacitor, (b) multiple via-connected capacitor



Figure 3.7 Photographs of the fabricated LTCC (a) regular toroid inductor, (b) bottom view of toroid inductor with air cavity

The S-parameters of the fabricated components were measured using the Agilent 8722ES VNA and a probing station. The inductance and capacitance values were then extracted from the S-parameter data following the procedure detailed in (Aliouane, Kouki et al. 2011). The obtained results are shown in figure 3.8 and figure 3.9 for C2 (22/28 pF) and L2 (45nH), respectively. Figure 3.8 shows that the measured capacitance for both the SVC and MVC and their SRFs are slightly below the original simulated values. After investigation, we found that the 7.8 dielectric constant (er) value specified by DuPont is at 3GHz and this value is lower in the VHF/UHF range and that the actual radius of the fabricated vias (R) was smaller than the one used in original simulation. We incorporated these two changes in the simulation model and re-simulated the structure and found excellent agreement with measurements as shown in figure 3.8. These confirm that using multiple vias for the capacitors led to a 23% increase in the SRF (from 540 to 665 MHz).



Figure 3.8 (a) Simulated and measured single capacitor


Figure 3.8 (b) Simulated and measured multiple via connected capacitor

For the inductors, figure 3.9 also shows that using the air cavity underneath the toroid inductor makes significant shift for SRF to higher frequency, i.e., a 22% increase in the SRF from 615 MHz to 750. In fact, these measured values are higher than the simulated ones due to the observed reduction in measured capacitance as discussed above. Table 3.3 shows a comparative summary of the obtained results to those in previous works.



Figure 3.9 Measured parameters of the 45nH inductance with and without cavity

Table 3.3 Comparison of various toroid inductors

	L	Q	SRF	
	(nH)	(Max)	(MHz)	
Hoppenjans (2009)	75	60	710	Simulated
Hoppenjans (2007)	25	20	800	Measured
This work	45	100	750	Measured

3.3 Dual band-pass filter using new high SRF components

After investigating the SRF and Q problems of individual components and improving them, they can be used in dual-band pass filters which have already presented in chapter 2 to reduce the insertion loss and consequently improve the filter performance.

A photograph of top and bottom view of the second order dual band-pass filter with air cavities under inductors is shown in figure 3.10. All of the capacitors are buried inside the substrate. The s-parameters of the fabricated filter were measured using the same mentioned network and probing station. Comparison between simulation and measured (fabricated) results are shown in figure 3.11. The insertion loss is 0.65 dB for the lower band and 1.25 dB for the upper band. Compared to the DBPF without air cavities, there are 0.15 dB and 0.25 dB improvements for the lower and upper band respectively.





Figure 3.10 Photograph of (a) top and (b) bottom view of the fabricated 2nd order LTCC DBPF with air cavities



Figure 3.11 Simulated and measured results for the 2nd dual band-pass filter with air cavities

A photograph of top and bottom view of the fourth order dual band-pass filter with air cavities under inductors is shown in figure 3.12. The forth order filter is designed by connecting two second order filter using one coupling capacitor. All of the capacitors are buried inside the substrate. The s-parameters of the fabricated filter were measured using the same mentioned network and probing station. Comparison between simulation and measured (fabricated) results are shown in figure 3.13. The insertion loss is 1.3 dB for the lower band and 2.5 dB for the upper band. Compared to the DBPF without air cavities, there are 0.3 dB and 0. 5 dB improvements for the lower and upper band respectively.





Figure 3.12 Photograph of (a) top and (b) bottom view of the fabricated 4th order LTCC DBPF with air cavities



Figure 3.13 Simulated and measured results for the 4th order dual band-pass filter with air cavities

3.4 Conclusion

New techniques for achieving high SRF for lumped element components for VHF/UHF applications have been proposed. Using these techniques, toroid inductors, with air cavities underneath, and a multiple via connected multi-layer capacitors have been designed, fabricated and tested in LTCC with very small form factors. Measurement results show an increase of 23% and 22% in SRF for capacitors and inductors, respectively, compared to conventional structures. Because the proposed techniques reduce losses in both cases, the resulting lumped elements have higher quality factors in addition to higher SRF. These techniques can be extended and adapted to higher frequencies.

CHAPITRE 4

DUAL-BAND/DUAL-FUNCTION LTCC CIRCUITS

Dual-band structures abound in the literature; see for example (Cheng and Fai-Leung 2004, Yong-Xin, Ong et al. 2005, Joshi and Chappell 2006, Hyunchul, Byungje et al. 2010) where various dual-band structures for filters and couplers are proposed. In (Yong-Xin, Ong et al. 2005) a dual band-pass filter is proposed by connecting two single band-pass filters using proper external phase shifting. While this approach provides dual-band coverage, it is not sufficiently compact. In (Joshi and Chappell 2006) a dual band-pass filter with a different structure using only a single set of lumped elements is proposed. However, this structure is suitable in terms of performance and size, but is targeted for high frequency operation. In (Cheng and Fai-Leung 2004) different structures for dual-band branch-line couplers are proposed while in (Cheng and Fai-Leung 2005) a dual-band rate-race coupler is presented. In these three works, the periodic properties of transmission lines, coupled with some second harmonic adjustment techniques such as adding open or short parallel stubs at the output ports, are used to obtain a dual-band behavior. Such structures are suitable only for high frequencies.

As for dual-function structures, no literature could be found showing dual-function passive circuits like coupling and filtering in one structure. This may be due to the fact that classical RF front-end architectures are built on specific functional blocks and only dual frequency behavior is considered at best.

In this chapter we focus on the VHF/UHF and their use in avionic systems to demonstrate how dual-band/dual-functional circuits can be used to meet the goals of high integration density with reduced size and weight. In particular, we propose new lumped-element compact circuits in LTCC technology that offer dual-band and dual-band/dual-function coverage for VHF/UHF avionic systems in a manner that optimizes the overall system architecture. First a highly compact dual-band coupler is proposed followed by a dual-

band/dual-function circuit which behaves as coupler at the lower band and as filter at upper band. We call this new structure as "dual-band coupler-filter".

The remainder of this chapter is organized as follows: In section II, an overview of the proposed Direct RF Sampling (DRFS) receiver for avionic systems is presented (Mousavi, Elzayat et al. 2012) and the need for a dual-band coupler and a dual-band coupler-filter is demonstrated. In section III, a new structure for a dual-band coupler for avionic systems is proposed and is mathematically demonstrated to offer the desired performance using ideal lumped components. In section IV, a new dual-band/dual-function coupler-filter for avionic systems is proposed and simulation results are presented for ideal lumped components. Section V is dedicated to the design and fabrication of both proposed circuits in sections III and IV by realizing the proper lumped circuit elements in LTCC technology.

4.1 Proposed reciever architecture and RF front-end for multi-standard VHF/UHF avionic systems

On the architectural level, figure 4.1 shows a suitable receiver architecture which was proposed in (Mousavi, Elzavat et al. 2012) to cover all VHF/UHF avionic systems. This architecture uses two paths to handle the various services operating at different frequencies. Based on systems specifications (Aliouane, Kouki et al. 2011), we chose a Direct RF Sampling (DRFS) architecture in VHF the upper path to detect the Navigation/Communication (VHF/COM, operating in the118-137 MHz band) and Glide Slope (GS, operating in the 329.5-335 MHz band) signals. In the lower path a conventional heterodyne architecture is necessary to meet the minimum SNR (20 dB) requirement for the VHF Omni-directional Radio Range Localizer (VOR/LOC, operating in the 108-118 MHz band) signals. Hence the two frequency bands of interest are (i) Band I: 108-137 MHz, i.e., 108-118 and 118-137 MHz, and (ii) Band II: 329.5-335 MHz. Our focus in this paper will be on the front-end section of this architecture, and more specifically on signal splitting between the two paths of figure 4.1. Figure 4.2 illustrates more clearly this section of the front-end

and identifies the frequency bands of interest in each of the two paths. We will consider two options for implementing the signal splitting at the input of the RF front-end.



Figure 4.1 RF front-end architecture for VHF/UHF avionic systems



Figure 4.2 Signal splitting and filtering structure of the RF front-end architecture for VHF/UHF avionic systems

4.1.1 Signal splitting via a power divider

A first option for implementing signal splitting is to use a conventional equal power divider such as a 3 dB hybrid coupler or a Wilkinson divider. To cover the frequency bands of interest, two alternatives are then available: (i) a wideband design covering the entire band from 108 to 335 MHz, which would yield more than an octave bandwidth, or (ii) a dual band design covering the lower band, with a 24% fractional bandwidth, and the upper band, with a 1.9% fractional bandwidth. In the latter case, the out of band rejection of the divider will help filter out unwanted signals and improve SNR. Therefore, we opt for a dual band design using a hybrid coupler as a first signal splitting option. It should be noted that a 1.9% bandwidth requires ultra-high Q lumped components which makes the design very challenging. Based on system level calculation, we found that an 8.5% bandwidth meets system specifications while requiring moderately high Q elements. We will therefore target a dual band design with 24% and 8.5% fractional bandwidths in LTCC technology (LACIME 2010) of this first option. This is detailed in section III.

4.1.2 Signal splitting via a dual-function circuit

Given that the frequency range of interest in the lower receive path is only 108-118 MHz, which is part of Band I, any portion of the Band II signal going to the lower path constitutes an undesirable loss that degrades the noise figure and reduces system performance. Therefore, the ideal signal splitting circuit should allow for equal division of Band I signals between the upper and lower paths while directing all Band II signals exclusively to the upper path. This behavior can be accomplished by a dual-band dual-function circuits which operates as a divider for Band I and as a filter for Band II. Therefore, we will seek, as a second signal splitting option, the design in LTCC of a dual-band coupler-filter to function as a 3dB hybrid coupler (power splitter) in Band I, with 24% bandwidth, and as a pass-band filter in Band II, with 8.5% bandwidth. The use of this second option will result in an improvement of up to 3dB in the noise figure of the receiver in Band II. Table 4.1 summarizes the impact on noise figure of the two signal splitting options based on ideal circuits.

	BAND I		BAND II	
Signal Splitting Structure	Lower Path	Upper Path	Lower Path	Upper Path
Dual-Band Coupler (option 1)	3 dB	3 dB	3 dB	3 dB

Table 4.1 Impact on receiver noise figure

Dual-Band Coupler-Filter 3 dB 3 (option 2)	dB N/A (Isolated)	0 dB
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4.2 Dual-band coupler design

Most dual-band couplers in previous works have been implemented using distributed elements (Cheng and Fai-Leung 2004, Cheng and Fai-Leung 2005, Feng and Qing-Xin 2009, Hyunchul, Byungje et al. 2010). To obtain dual band behavior, the periodic properties of transmission lines, coupled with some second harmonic adjustment techniques such as adding open or short parallel stubs at the output ports (Cheng and Fai-Leung 2004, Feng and Qing-Xin 2009), and adding series stubs at all ports (Hyunchul, Byungje et al. 2010), were used leading to even larger circuits. Clearly, such distributed techniques are not suitable for low frequency applications such as the ones being considered here where size is critical. In (Tze-Min, Chin-Ren et al. 2010), simulations of a lumped element rat-race coupler operating at 1 and 2 GHz were presented but results show poor amplitude balance with limited bandwidth. In (Hoppenjans and Chappell 2009) a LTCC lumped element implementation was used for a tunable low frequency filter application, with no dual-band operation and using surface mounted capacitors. Here we seek a fully integrated lumped element implementation that provides dual-band coverage and meets our bandwidth requirements. To this end, we adopt the work of (Hyunchul, Byungje et al. 2010), which was developed for distributed transmission line circuits, and extend it to a lumped element implementation as follows:

We start with a simple branch-line coupler structure whose center frequency is f as shown in figure 4.3. Next, for each transmission line segment of electric size Θ at f and characteristic impedance Z_0 , i.e., $Z_0=Z_1$, $Z_0=Z_2$, or $Z_0=Z_3$, we introduce an equivalent lumped element π -model representation as shown in figure 4.4. The values of the lumped elements, L and C, for

each line segment are computed using the following two equations (Brzezina, Roy et al. 2009):

$$L = \frac{\sqrt{2}Z_0 \sin\theta}{2\pi f} \tag{4.1}$$

$$C = \frac{1}{\sqrt{2}Z_0 2\pi f} \sqrt{\frac{1 - \cos\theta}{1 + \cos\theta}}$$
(4.2)



Figure 4.3 Geometry of a distributed branch-line coupler



Figure 4.4 Lumped element π -model of a transmission line

For the dual band design Z_3 is different from reference impedance, i.e., 50 Ω , and constitutes a port extension line segment as proposed in (Hyunchul, Byungje et al. 2010). Z_1 , Z_2 and Θ are different from the conventional single band values, i.e., 35 Ω , 50 Ω and 90°, respectively.

The values of these parameters are computed following (Hyunchul, Byungje et al. 2010) where using the dual band center frequencies $f_1=122.5$ MHz $f_2=332$ MHz and setting $\theta = \frac{\pi}{1+\frac{f_2}{f_1}}$ (Hyunchul, Byungje et al. 2010), we find $\theta = 49^{\circ}$, $Z_1 = 21.6 \Omega$, $Z_2 = 30.3 \Omega$, and

 $Z_3 = 7.5 \Omega$. Applying the equivalence procedure of figure 4.4 three times, once for Θ - Z_1 , equivalent to L_1 - C_1 , once for Θ - Z_2 , equivalent to L_2 - C_2 , and once for Θ - Z_3 , equivalent to L_3 - C_3 , we obtain the circuit of figure 4.5a, which can be simplified to yield the dual band lumped element coupler model of figure 4.5b.





Figure 4.5 Lumped element model of a branch-line coupler: (a) original circuit, (b) simplified model by using $C_T=C_1+C_2+C_3$

Next, using (4.1) and (4.2) and the computed values for Θ , Z_1 , Z_2 and Z_3 , the values of L_1 , C_1 , L_2 , C_2 , L_3 and C_3 are calculated with $f = f_1$. The value of the lumped elements are calculated and listed in table 4.2.

C ₃ (pF)	C _T (pF)	$L_2(nH)$	L ₃ (nH)	$L_1(nH)$
46	50.6	42	10.5	30

Table 4.2 Optimization results for the coupler's parameters

The results of the simulated dual-band coupler frequency response using the topology of figure 4.5b with ideal L and C elements whose values are ginven in table 4.2 are shown in figure 4.6. These results meet the objective of providing dual band coverage with equal power division and good amplitude balance (-3 dB \pm 0.2 dB over 108-137 MHz and 329.5-335 MHz). In terms of fractional bandwidth, we obtained 26% and 8.5% at Band I and Band

II, respectively. It should be noted that the magnitude of S12 and S13 in Band II have been found to be particularly sensitive to L_2 , the coupling inductor.



Figure 4.6 Simulation results of proposed dual-band pass coupler

4.3 Dual-band coupler-filter design

As mentioned in section 4.2.1, another possible topology for the signal splitting structure is a dual-band/dual-function circuit. In this case we seek a circuit which behaves as coupler in Band I and as filter in Band II, i.e., a 'dual-band coupler-filter'. To design a dual-band coupler-filter we will use a new methodology that we will first illustrate with our current design for the selected frequencies. This methodology will later be summarized and presented in a flowchart format and will be further validated through a second dual-band coupler filter design at higher frequencies.

We start again with the branch line coupler structure of figure 4.3 but we seek a single band 50 Ω hybrid coupler, i.e., the reference impedance is Z0=50 Ω In this case, Z3 = Z0 and the electric length of the associated transmission line segment is not constrained to a specific value and figure 4.3 is simplified as shown in figure 4.7. Here the conventional values are used, i.e., $\Theta = 90^{\circ}$, $Z_1 = Z_0/\sqrt{2} = 35 \Omega$ and $Z_2 = Z0= 50 \Omega$. Next following the outlined equivalence procedure of figure 4.4 combined with equations (4.1) and (4.2), we construct the equivalent lumped element coupler model as shown in figure 4.8a. The resulting values are L1=46.2nH, C1=36.7pF, L2=67.7nH, and C2=24.9pF. We can simplify the circuit of figure 4.8a by combining C1 and C2, i.e., by defining C0 = C1+C2 as shown in figure 4.8b. Simulation results of this ideal lumped-element coupler model are shown in figure 4.9. They give 3dB power division in Band I and better than 25 dB rejection in Band II.



Figure 4.7 Geometry of a distributed branch-line coupler



Figure 4.8 (a) Lumped element model of a branch-line coupler



Figure 4.8 (b) simplified model by using $C_0=C_1+C_2$



Figure 4.9 Simulation results of a lumped element branch line equivalent coupler at 122.5MHz

Given that the topology of figure 4.8 does insure equal power division in Band I, our objective at this stage is to modify it such that it operates as a filter in Band II, with little or no impact on its performance at Band I. To achieve this, we first note that the filter is a two-port device and, therefore, two of the coupler ports (3 and 4 in our case) must be isolated, i.e., resonated out by using a properly dimensioned LC resonator in the shunt paths. For this, a parallel capacitor, CP = 3.5 pF, is added to L2, as shown in figure 4.10, such that the L2-Cp resonator presents and open circuit at Band II (332MHz). It should be noted that C_P has no major impact on the circuit in Band I since its reactance (373 Ω) is much larger than that of L2 (51.8 Ω) at the center frequency of 122.5MHz.



Figure 4.10 Branch-line coupler model with a shunt CP

With addition of C_P , ports 3 and 4 of the coupler are isolated at Band II frequencies and the equivalent circuit at these frequencies gives the two port network shown in figure 4.11a. Next we focus on transforming the circuit of figure 4.11a into a filter. To this end we first create

two resonators as shown in figure 4.11b by adding a parallel inductor (L_P) to each C0 capacitor. However, the addition of this inductor will degrade the coupler function in Band I. To eliminate the effect of L_P in Band I, an LC resonator (L₃ and C₃) is inserted in series with L_P as shown in figure 4.11c. The choice of L₃ and C₃ must meet the following three constraints: (i) they must present a short-circuit resonance at Band II, thus they must satisfy $f_2 = \frac{1}{2\pi\sqrt{L_3C_3}}$, (ii) the combined series inductors (L_P and L₃) must have negligible impact on the circuit at Band I, i.e., their combined reactance should be much smaller than that of C₃ at Band I, and (iii) the resonators formed by L_P and C₀-C₃ in the equivalent circuit at f_2 , shown in figure 4.11d, will resonate at a frequency $f_p = \frac{1}{2\pi\sqrt{L_p(C_0-C_3)}}$, which should be

close to f_2 . Clearly, there is not a unique solution for L3 and C3 that will satisfy all three constraints. Consequently, some design tradeoffs have to be made in their choice. For this, we introduce two parameters to guide this choice and help evaluate these tradeoffs. The first parameter is the ratio of reactances, r, which will serve to quantify the second constraint and which is given by:

$$r = \frac{1/(wC_3)}{w(L_P + L_3)} \tag{4.3}$$

The second parameter, q, quantifies the third constraint and is given by the ratio f_P/f_2 . Using these two parameters, the combined three constraints above lead to the following equation for the selection of C₃ in relation to C₀:

$$C_3 = C_0 \left(1 - \frac{r}{q^2} \left(\frac{f_1}{f_2}\right)^2\right)$$
(4.4)

Once the value of C₃ is chosen through values of r and q, the values of L₃ and L_P are fixed through f_2 and f_P , respectively.



Figure 4.11 (a) Circuit model at resonance of the L₂-C_P resonator of figure 4.10.
(b) Addition of L_P to make resonators. (c) Addition of the L₃-C₃ resonator to eliminate the effect of L_P in Band I



Figure 4.11 (d) Simplified circuit in Band II. (e) Adding L_S to obtain the complete filter structure

The circuit shown in figure 4.11d is not yet a filter and two additional series inductances, LS, need to be added to ports 1 and 2, as shown in figure 4.11e, to obtain a filter at Band II. The initial value of LS is computed using the conventional filter synthesis formulas for second order inductance coupled filters given in (Matthaei 2000) for the desired center frequency (329 MHz) and bandwidth (8.5%). In this case, L1 is fixed to value already found, i.e., 46.2nH, the values of LP and C0-C3 are ignored and the value of LS is kept and found to be LS=26nH.



Figure 4.12 Parametric variation of coupler and filter bandwidths



Figure 4.12 Parametric variation of coupler and filter bandwidths

The variation of r and q affects the bandwidths of the coupler and the filter in opposite ways as shown in figure 4.12. For a given coupler bandwidth, the values of r and q can be picked from figure 4.12a. The resulting bandwidth of filter will then be defined in figure 4.12b. Note that the filter bandwidth obtained in this step is not the final one since slight tuning can be obtained by adjusting the value of LS as shown in figure 4.12c.

Applying the above procedure to the current design, we require a coupler bandwidth of 24%, which from figure 4.12a can be achieved with r=3.6 and q=0.85. With these values and C0=56 pF, we find C3=20 pF, L3=11.5 nH, and LP=7.3 nH. Figure 4.12b indicates that our filter will have a bandwidth around 8% for the chosen r and q values and LS=26nH. Although this resulting design is feasible, one can still tune the value of LS to obtain a filter bandwidth of 8.5%. Using figure 4.12c, the value of LS is found to be slightly lower at

23.1nH. Finally, with all these lumped elements values (figure 4.11e), the filter's band-pass response was computed and the results are shown in figure 4.13.



Figure 4.13 Simulation results of the band pass filter of figure 4.11d

The addition of lumped elements in figure 4.11 that provided the required filter behavior can now be combined with the original circuit of figure 4.8 to yield the complete structure of the dual-band coupler-filter shown in figure 4.14a. This circuit can be further simplified by combining some elements together, namely by introducing C4=C0-C3 and L4=L3+LP. The resulting final circuit topology is shown in figure 4.14b and the lumped element values are given in table 4.3 as initial values.

The last step in finalizing the coupler-filter design is to carry out a tuning, in a circuit simulator, of the element values for maximum performance. The tuned values of all lumped elements are listed in table 4.3 under tuned values. Figure 4.15 shows the simulation results for the ideal lumped component dual-band coupler-filter both with original values and the

Lumped element	Initial value	Tuned value
L ₁	48.6 nH	53.4 nH
L ₂	67.5 nH	67.5 nH
L ₄	18.8 nH	18.8 nH
Ls	22.5 nH	24.7 nH
C ₃	20 pF	20 pF
C4	41 pF	41 pF
C ₀	56 pF	56 pF
C _P	3.2 pF	3.2 pF

Table 4.3 Designed circuit values for proposed dual-band coupler-filter

tuned ones. As can be seen, the tuning step brings little improvement and can be considered



as optional.





Figure 4.14 (b) final coupler-filter circuit in which C4=C0-C3, and L4=L3+LP



Figure 4.15 (a) Simulation results of proposed dual-band coupler-filter with initial values



Figure 4.15 (b) Simulation results of proposed dual-band coupler-filter tuned values

4.3.1 Design methodology summery

The above methodology can be summarized by a design flowchart, given in table 4.4, that can be applied to any given dual band configuration.

As a second validation of the proposed methodology, we designed another dual-band coupler-filter for two non-harmonically related WLAN frequencies (f_1 =2.4 GHz and f_2 =5.2 GHz). Starting with the topology of figure 4.8a and following the design flowchart of table 4.5 with r=2.5 and q=0.85, the values of all lumped elements of the final topology of figure 4.14b were computed and are listed in table 4.5 as initial values. While these values give good initial results as shown in figure 4.16, tuning them slightly as show under the tuned values column allowed us to obtain the improved results of figure 4.17. It should be noted that these lumped element values are easily realizable in LTCC as demonstrated by (Joshi and Chappell 2006).

Step	Description
0	Pick the center frequencies of the dual-bands and denote them by f_1 , for Band I and f_2 , for Band II.
0	Use the lumped element π -model shown in figure 4.4 and the equations (4.1) and (4.2) to compute the lumped element values. The resulting circuit is represented by figure 4.8a.
€	Simplify the circuit of figure 4.8a by combining parallel capacitors. The resulting circuit is represented by figure 4.8b with (C0=C1+C2).
4	Add a capacitor (CP) in parallel with L2 (found in step ⁽²⁾) as shown in figure 4.10. Set $C_p = \frac{1}{L_2(2\pi f_2)^2}$ to resonate the paths between ports 1 and 4, and 2 and 3 at f_2 . The resulting four port circuit is equivalent to the two-port circuit of figure 4.11a.

Table 4.4 Design procedure for dual-band coupler-filters

6	Start converting the circuit of figure 4.11a to a filter structure by adding a parallel inductor LP as shown in figure 4.11b.
6	Add a series resonator L3, C3 in series with LP and adjust C0 to C0-C3 as shown in figure 4.11c. The equivalent circuit at Band II is shown in figure 4.11d.
0	Complete the filter conversion by adding two series inductor (LS) at each port of figure 4.11d to obtain the circuit of Fig. 11e. Use filter synthesis formulas (Matthaei 2000) to compute initial value of LS.

Table 4.5 Design procedure for dual-band coupler-filters

Step	Description
	Chose r and q based on the desired bandwidths (use figure 4.12a,
	figure 4.12b).
	Compute C3 from equation (4.4).
8	Compute $L_3 = \frac{1}{(2\pi f_2)^2 C_3}$.
	Compute $L_P = \frac{1}{(2\pi f_P)^2 (C_0 - C_3)}$.
	Tune LS for the desired filter bandwidth (figure 4.12c).
	Combine figure 4.8a and figure 4.10e to obtain the complete dual- band coupler-filter of figure 4.14a.
Θ	Introduce C4=C0-C3 and L4=L3+LP and simplify the final circuit topology as shown in figure 4.14b.

Lumped elements	Initial values	Tuned values
L1	3.4 nH	3.5 nH
L2	4.5 nH	4.2 nH
L4	2.2 nH	2.28 nH
LS	1.55 nH	1.6 nH
C3	0.61 pF	0.62 pF
C4	1.9 pF	1.9 pF
C0	2.4 pF	2.55 pF
СР	0.2 pF	0.2 pF

Table 4.6 Designed circuit values for proposed dual-band coupler-filter



Figure 4.16 Simulation results of proposed dual-band coupler-filter with initial values



Figure 4.17 Simulation results of proposed dual-band coupler-filter with tuned values

4.3.2 Amplitude/phase balancing

To study the amplitude/phase imbalance of the coupler in Band I, we simplify the circuit of figure 4.14 for Band I as shown in figure 4.18. As can be seen from this figure, the circuit is not fully symmetric due to the presence of inductors (LS) in ports 1 and 2 but not ports 3 and 4. While the impedance of LS is negligible in Band I, it still affects the phase response and to a much lesser extent the amplitude balance. To remedy these issues and balance the coupler's response, one simply needs to add the LS inductor to ports 3 and 4 as shown in figure 4.19. The resulting circuit is fully symmetric and gives a perfectly balanced amplitude and phase responses at 122.5 MHz as shown in figure 4.20 and figure 4.21, respectively.



Figure 4.18 Simplified circuit in Band I



Figure 4.19 Modified circuit for dual-band coupler-filter with a balanced amplitude/phase responses



Figure 4.20 Simulation amplitude results of proposed dual-band coupler-filter


Figure 4.21 Simulation phase difference between port 2 and 3 of proposed dual-band coupler-filter

4.4 Passive component design

Whether designing dual-band couplers or dual-band/dual-function circuits, it is clear that the realization of these components depends on the successful design of their lumped elements with the proper values.

4.4.1 Dual-band coupler design

For our application, the design of the dual-band coupler requires the design of three inductors and two capacitors as per table 4.2. Consequently, focus will first be placed on designing these individual L and C components.

The toroid inductor topology is chosen for the larger inductances (L=42nH and L2=30nH) while the solenoid inductor topology is chosen for the smallest one (L1=10.5 nH). The magnetic field in a toroidal inductor circles inside the toroid's winding thereby ensuring good self-shielding properties. We can take advantage of this property to bury many toroidal inductors within the LTCC substrate and place them close to each other without parasitic coupling for a more compact design. For the solenoid inductor, the width and spacing

between the winding must be optimized. Using 3D field simulation, i.e., HFSS, we designed and optimized the three inductors. The obtained results are summarized in table 4.6. Figure 4.22a shows an example of a toroidal inductor design for an inductance value of 41.8 nH.

Inductor	#of turns	Inner radius	Outer radius	Inductance
		(mm)	(mm)	(nH)
L1	4	N/A	N/A	10.7
L2	10	0.64	2.2	30.44
L	11	0.72	3	41.8

Table 4.7 List of designed inductors and their charactristics

Unlike (Hoppenjans and Chappell 2009), in which the surface mounted capacitors were used, multi-layer parallel-plate capacitors buried within LTCC substrate were also designed using HFSS. Since large values of capacitance are required in the coupler circuit, the thinnest layer (1.63 mils-thick after firing) of LTCC has been used, and to save the occupied area, multi-layer stacking using 8 parallel circular disks was used. Table 4.7 summarizes characteristics of the two capacitors needed while figure 4.22b shows an example of a multilayer parallel plate capacitor (46pF).

Table 4.8 List of designed capacitors and their charactristics

Capacitor	#of plates	Plate radius (mm)	Capacitance (pF)
С	8	0.9	46
C ₁	8	0.95	50.6



Figure 4.22 3D views of (a) toroid inductor and (b) multi-layerparallelplatecapacitor

Integration of these lumped elements to build the whole dual band coupler is the next step. Figure 4.23 shows the EM model of dual band coupler where the capacitors and inductors were buried inside the substrate in different layers to reduce size.



Figure 4.23 (a) Top and (b) 3D views of the lumped element dual band coupler

4.4.2 Dual-band coupler-filter design

The design methodology for the dual-band coupler-filter is exactly like that of the dual-band coupler. First, all the required lumped elements are designed and then integrated to form the dual-band coupler-filter. The toroid inductor is chosen for all inductors in this design. Using 3D field simulation, i.e., HFSS, we designed and optimized the four inductors. The obtained results are summarized in table 4.8.

Inductor	#of	Inner radius	Outer radius	Inductance
	turns	(mm)	(mm)	(nH)
L ₁	12	0.76	2.5	47.6
L ₂	12	0.76	3.4	67.9
L ₄	6	0.32	2	19.1
Ls	7	0.46	2.5	22.7

Table 4.9. List of designed inductors and their charactristics

Multi-layer parallel-plate capacitors buried within the LTCC substrate were also designed using HFSS. Since large values of capacitance are required in the coupler circuit, the thinnest layer (1.63 mils-thick after firing) of LTCC has been used, and to save the occupied area, multi-layer stacking using 8 parallel circular disks was used. The multiple via connection capacitors shown in figure 4.24 are used to get higher Self-Resonant Frequency (SRF) (Mousavi and Kouki 2014). Table 4.9 summarizes characteristics of the four capacitors needed.

Table 4.10 List of designed capacitors and their charactristics

Capacitor	#of plates	Plate radius (mm)	Capacitance (pF)
C ₃	8	0.48	20.5
C_4	8	0.7	41.8
C_0	8	0.81	55.6





Figure 4.24 3D view of the multiple via-connected capacitor

Integration of these lumped elements to build the whole dual-band coupler-filter is the next step. Figure 4.25 shows the EM model of dual-band coupler-filter where the capacitors and inductors were buried inside the substrate in different layers to reduce size.





Figure 4.25 (a) Top view of the lumped element dual-band coupler-filter

Figure 4.25 (b) 3D view of the lumped element dual-band coupler-filter

4.5 Fabrication and testing

The dual band coupler and the dual-band coupler-filter for VHF/UHF avionic systems were fabricated using the LTCC process (LACIME 2010) with DuPont's 951AT substrate ($\epsilon r=7.8$, Tan δ =0.006). The overall size of the dual band coupler is 19mm×14mm×2.2mm while that of the dual-band coupler-filter are 22mm×28mm×2.2mm. Photographs of the fabricated circuits are shown in figure 4.26. The S-parameters of these circuits were measured using the Agilent 8722ES VNA and a probing station.



Figure 4.26 Photograph of the fabricated LTCC (a) dual-band coupler

and (b) dual-band coupler-filter

4.5.1 Result for the dual-band coupler

The EM-simulated and measured results for the dual-band coupler are presented in figure 4.27. The dual band behavior is clearly confirmed by measurements. The measured S12 is in excellent agreement with EM simulations, 3.5 dB in Band I and 4.8 dB in Band II. The measured S13, on the hand, shows very good agreement with simulation in Band I but a difference of about 2 dB in Band II. To understand the reason behind this difference, we carried out a sensitivity analysis on the dual-band coupler circuit of figure 4.5. The results of this analysis have reveals that S12 and S13 are most sensitive to L2, the coupling inductor, compared to all other elements. Figure 4.28 illustrates the variation of the magnitude of S12 and S13 at Bands I and II as the value of L2 is varied. Clearly, S13 in Band II exhibits the highest sensitivity to L2. Since the fabricated L2 value will inevitably be slightly different from the simulated one, due to inherent fabrication tolerances, the difference between simulated and measured S13 in Band II are attributable in large part to this variation. However, for our application, the magnitude of S13 in Band II is not important since Port 3 is connected to lower receiver path of figure 4.1, which operates in Band I.





Figure 4.27 (a) Simulated and measured result for division of proposed dual band coupler



Figure 4.27 (b) Simulated and measured result for isolation of proposed dual band coupler



Figure 4.28 Sensitivity of S-parameters to L₂ at Band I and Band II

4.5.2 Result for the dual-band coupler-filter

The EM-simulated and measured results for the dual-band coupler-filter are shown in figure 4.29. The measured insertion loss for the filter part, i.e., in Band II, is only 2.9 dB. Compared to the dual band coupler, the insertion loss is significantly reduced resulting in important system gains of 1.9 dB. Figure 4.30 compares the measured S12 of the dual-band coupler-filter to that of the dual-band coupler over the entire frequency range. This Figure demonstrates the performance improvement for Bands I and II, and the out of band rejection between the two bands. In addition to the insertion loss reduction in Band II, a 0.65 dB insertion loss improvement is also achieved in Band I. As shown in figure 4.29b, the simulated and measured return loss and isolation are in a good agreement.



Figure 4.29 (a) Simulated and measured result of the proposed dual-band coupler-filter for power division and filtering



Figure 4.29 (b) Simulated and measured result of the proposed dual-band coupler-filter for matching and isolation



Figure 4.30 Comparison between measured S12 of the proposed dual-band coupler-filter and dual-band coupler

Finally, looking at the phase balance of the coupler in Band I, figure 4.31 shows that the simulated and measured results are in excellent agreement with a substantial phase imbalance

of $\pm 8^{\circ}$. As stated earlier, the coupler is being used as a power divider so no effort was made to balance the phase in order to reduce the circuit size by eliminating one inductor, L_S, from ports 3 and 4. Had L_S been added to these ports, we expect that we would have achieved excellent phase balance in measurement as demonstrated by figure 4.21.



Figure 4.31 Simulated and measured result for phase differences between port 2 and 3 in Band I

4.6 Conclusion

New structures for a dual-band coupler and a dual-band coupler-filter suitable for VHF and UHF bands of avionic systems have been proposed. The use of these components in a multistandard avionic system's RF front-end has been presented and their relative merits have been discussed in the context of the front-end's architectural choices. The circuit design process for each of these structures has been detailed and a step by step design methodology has been provided. A lumped element approach has been chosen for each of their implementations and the subsequent design of each of the required lumped elements in LTCC technology has been presented. Both structures have been fabricated and tested and the measured results were found to be in close agreement with simulations. The dual-band filter-coupler, which represents a new dual-band dual-function circuit, was found to give a gain of 0.65 dB and 1.9 dB based on measurements for Bands I and II, respectively with increased out-of band rejection between the two. Both circuits come in a very small form factor, which reduces size and weight, both important in avionics. The application of the proposed dual-band coupler-filter design methodology to higher frequencies has been presented and validated through electromagnetic simulation.

CHAPITRE 5

INTEGRATION OF VHF/UHF RF FRONT-ENDS FOR AVIONIC SYSTEMS

The work contained in this chapter represents the completion of the final thesis objective. Namely, the RF front-end part of Direct RF Sampling (DRFS) receiver of the VHF/UHF avionics systems. Figure 5.1 presents these devices and their locations in the receiver chain.



Figure 5.1 RF front-end part of proposed receiver architecture

Three different versions of the structure shown in Figure 5.1 are fabricated on LTCC substrate and listed in table 5.1.

Integration	Divider	LNA	Filter
1	Dual-band coupler (DBC) (Band I IL=3.8 dB, Band II IL=4.8 dB)	CXE-2089 (Gain=20 dB, NF=1.5 dB)	2 nd order dual band- pass filter (2 nd DBPF) (Band I IL=0.85 dB, Band II IL=1.5 dB)
2	Dual-band coupler (DBC) (Band I IL=3.8 dB, Band II IL=4.8 dB)	CXE-2089 (Gain=20 dB, NF=1.5 dB)	4 th order dual band- pass filter (4 th DBPF) (Band I IL=1.7 dB, Band II IL=3 dB)
3	Dual-band coupler- Filter (DBCF) (Band I IL=3.65 dB, Band II IL=2.9 dB)	CXE-2089 (Gain=20 dB, NF=1.5 dB)	4 th order dual band- pass filter (4 th DBPF) (Band I IL=1.7 dB, Band II IL=3 dB)

Note that the same LNA is used for all the above integrations. The LNA has 20 dB gain and 1.5 dB NF.

5.1 Integration 1_DBC-LNA-2nd DBPF

In this integration the proposed dual-band coupler in chapter 4, and the proposed 2nd order filter in chapter 3 are used as a divider and filter respectively. Figure 5.2 shows a photograph of fabricated circuit.



Figure 5.2 Photograph of integration 1

Figure 5.3 shows the fabrication results of integration 1. The insertion losses are 5 dB and 9 dB for Band I and II respectively and the maximum out of band rejection is around 45 dB. Note that the total gain is 20 dB subtracting from loss, i.e 15 dB and 11 dB for Band I and II respectively.



Figure 5.3 Measured results of integration 1 (a) S11 and S12



Figure 5.3 Measured results of integration 1 (b) S13 and S14

5.2 Integration 2_ DBC-LNA-4th DBPF

In this integration the proposed dual-band coupler in chapter 4, and the proposed 4th order filter in chapter 3 are used as a divider and filter respectively. Figure 5.4 shows a photograph of fabricated circuit.



Figure 5.4 Photograph of integration 2

Figure 5.5 shows the fabrication results of integration 1. The insertion losses are 5.5 dB and 11 dB for Band I and II respectively and the out of band rejection is around -60 dB.



Figure 5.5 Measured results of integration 2 (a) S11 and S12



Figure 5.5 Measured results of integration 2 (b) S13 and S14

5.3 Integration 3_DBCF-LNA-4th DBPF

In this integration the proposed dual-band coupler in chapter 4, and the proposed 4th order filter in chapter 3 are used as a divider and filter respectively. Figure 5.6 shows a photograph of fabricated circuit.



Figure 5.6 Photograph of integration 3

Figure 5.7 shows the fabrication results of integration 1. The insertion losses are 5.5 dB and 9 dB for Band I and II respectively and the out of band rejection is more than -60 dB.



Figure 5.7 Measured results of integration 3 (a) S11 and S12



Figure 5.7 Measured results of integration 3 (b) S13 and S14

5.4 Summary

All the integration circuits were fabricated using the LTCC process (LACIME 2010) with DuPont's 951AT substrate ($\epsilon r=7.8$, Tan $\delta=0.006$). The S-parameters of these circuits were measured using the 4-Port Agilent 8722ES VNA and a probing station. A photograph of measurement setup is shown in figure 5.8.



Figure 5.8. Photograph of the measurement setup

The performances of all these integrations are summarized and compared in table 5.2.

Integration	Insertion loss (S12)		Insertion loss (S13)		Out of band	Size
	Band I	Band II	Band I	Band II	rejection	
Integration 1	4.4 dB	9.5 dB	3.6 dB	6.5 dB	-25 dB	45mm×20mm×2.2mm
Integration 2	5.1 dB	11.3 dB	3.6 dB	6.5 dB	-60 dB	45mm×38mm×2.2mm
Integration 3	5.8 dB	9 dB	3.7	26 dB	-62 dB	59mm×38mm×2.2mm

Table 5.2 Comparison of performances of all integrations

A photograph of commercial single-band coupler and fabricated LTCC dual-band couplerfilter is shown in figure 5.9 and their performances are compared in table 5.3.



Figure 5.9. Photograph of measurement setup

Commercial Coupler for LOC	Coupler-Filter for LOC and GS
Insersion loss: 5.2 dB	Insersion Loss: 3.65 dB for coupler and 2.9
	dB for filter
Dimension : 335.6mm×30.46mm×35.56mm	Dimension : 59mm×38mm×2.2mm
Coverage: Single-band coupler (LOC)	Coverage: Dual-band coupler (LOC)-filter
	(GS)

Table 5.3 Comparison between designed coupler-filter and commercial coupler

5.5 Conclusion

All the previously described receiver passive components were combined to form a fully functional RF front-end that completes the fulfilment of the final thesis objective. Integration 1 is the first demonstration of a fully embedded VHF/UHF bands RF front-end. Integration 2 has more out of band rejection, but suffer from more insertion loss compared to Integration 1. Integration 3 is the final one that has less insertion loss and more out of band rejection with the others.

CONCLUSION

This thesis has investigated methods and techniques for the integration of a VHF/UHF receiver front-end. Through the combination of custom desiged passive components and commercial active components, a novel miniature receiver RF front-end module has been successfully demonstrated for avionic systems.

The main architectures for system-level integration are presented in Chapter 1. A critical comparison of those architectures was performed and the Direct RF Sampling (DRFS) receiver was seen as the most appropriate for this work. VHF/UHF bands were selected for highest impact (Service/Band) that have potential for 5 to 1 reduction in the number of antennas. Low Temperature Co-fired Ceramic (LTCC) is chosen for implementation of RF front end because of its low loss, good reliability and ability to stack multiple layers. Therefore, passive components can be buried inside of substrate and active components can be mounted on the substrate to achive a compact receiver. Finally, some high level background information were provided resulting the chosen receiver building blocks such as the dual band-pass filters and dividers.

In Chapter 2, the design of band-pass filter building block was undertaken. In this process, novel techniques were proposed using passive lumped elements. Two dual band-pass filters were presented in a fully embedded 4th order for Band I and 2nd order for Band II LTCC that displayed an insersion loss of 1.6 dB and 2.9 dB for Band I and II respectively and a good out of band rejection. A good agreement between measurements and simulations was obtained.

In Chapter 3, new methods were proposed to increase the Self-Resonant Frequency (SRF) and Quality Factor (Q) of both toroid inductors and parallel plate capacitors. Toroid inductors with air cavity under and multiple-via connected capacitors were designed for inductors and capacitors respectively. Measurement results showed an increase of 23% and 22% in SRF for

capacitors and inductors, respectively, compared to conventional structures. Because the proposed techniques reduce losses in both cases, the resulting lumped elements have higher quality factors in addition to higher SRF.

In Chapter 4, new dual-band coupler and dual-band/dual-function coupler-filter topologies are proposed. The step by step methodology for dual-band coupler-filter is provided and to validate the proposed circuit two dual-band coupler-filter for different frequencies are designed. The lumped element implementation approach was used to design one dual-band coupler and one dual-band coupler-filter for VHF/UHF frequencies. Both structures have been fabricated and tested and the measured results were found to be in close agreement with simulations. The dual-band filter-coupler, which represents a new dual-band dual-function circuit, was found to give a gain of 0.65 dB and 1.9 dB based on measurements for Bands I and II, respectively with increased out-of band rejection between the two. Both circuits come in a very small form factor, which reduces size and weight, both important in avionics. The application of the proposed dual-band coupler-filter design methodology to higher frequencies has been presented and validated through simulation.

The building blocks of the previous chapters and a Low Noise Amplifier (LNA) were combined in Chapter 5 to present complete RF front-ends for VHF/UHF avionic systems. Three different combinations were fabricated and their performances are summerized. The size of all these modules are too small compare with a commercial coupler for the same frequency operation.

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