Modeling, Development and Control of Multilevel Converters for Power System Application

by

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MODELING, DEVELOPMENT AND CONTROL OF MULTILEVEL CONVERTERS FOR POWER SYSTEM APPLICATIONS

Hani VAHEDI

ABSTRACT

The main goal of this project is to develop a multilevel converter topology to be useful in power system applications. Although many topologies are introduced rapidly using a bunch of switches and isolated dc sources, having a single-dc-source multilevel inverter is still a matter of controversy. In fact, each isolated dc source means a bulky transformer and a rectifier that have their own losses and costs forcing the industries to avoid entering in this topic conveniently. On the other hand, multilevel inverters topologies with single-dc-source require associated controllers to regulate the dc capacitors voltages in order to have multilevel voltage waveform at the output. Thus, a complex controller would not interest investors properly. Consequently, developing a single-dc-source multilevel inverter topology along with a light and reliable voltage control is still a challenging topic to replace the 2-level inverters in the market effectively.

The first effort in this project was devoted to the PUC7 inverter to design a simple and yet efficient controller. A new modelling is performed on the PUC7 inverter and it has been simplified to first order system. Afterwards, a nonlinear cascaded controller is designed and applied to regulate the capacitor voltage at 1/3 of the DC source amplitude and to generate 7 identical voltage levels at the output supplying different type of loads such as RL or rectifier harmonic ones.

In next work, the PUC5 topology is proposed as a remedy to the PUC7 that requires a complicated controller to operate properly. The capacitor voltage is regulated at half of dc source amplitude to generate 5 voltage levels at the output. Although the 7-level voltage waveform is replaced by a 5-level one in PUC5 topology, it is shown that the PUC5 needs a very simple and reliable voltage balancing technique due to having some redundant switching states. Moreover, a sensor-less voltage balancing technique is designed and implemented on the PUC5 inverter successfully to work in both stand-alone and grid-connected mode of operation.

Eventually, a modified configuration of the PUC5 topology is presented to work as a buck PFC rectifier. The internal performance of the rectifier is like a buck converter to generate stepped down DC voltages at the two output terminals while the grid sees a boost converter externally. As well, a decoupled voltage/current controller is designed and applied to balance the output voltages identically and synchronize the input current with grid voltage to have a PFC operation acceptably. A power balance analysis is done to show the load variation range limit.

All the theoretical and simulation studies are validated by experimental results completely.

Keywords: Cascaded Nonlinear Control, Multilevel Converter, Packed U-Cell, PUC5, Power Quality, Renewable Energy Conversion.

MODÉLISATION, DÉVELOPPEMENT ET CONTRÔLE DES CONVERTISSEURS MULTINIVEAU POUR LES SYSTÈMES DE PUISSANCE

Hani VAHEDI

RÉSUMÉ

Le but principal de ce projet est le développement d'une topologie d'onduleur multiniveau utile aux applications en puissance. Bien que plusieurs topologies différentes soient introduites, elles utilisent en général une multitude d'interrupteurs et de sources CC isolées. Avoir un convertisseur multiniveau avec une seule source CC est encore une technologie en développement. En fait, chaque source CC isolée représente un transformateur et un redresseur qui possèdent leurs propres pertes et prix et rendent la plupart du temps ses systèmes inintéressants pour l'industrie. D'un autre côté, les convertisseurs multiniveaux à source unique requièrent un contrôleur plus évolué pour réguler la tension des condensateurs flottants; un requis pour avoir la forme d'onde multiniveau en sortie. Or, un contrôleur est beaucoup moins intéressant pour un investisseur. Conséquemment, développer un onduleur multiniveau avec une seule source CC et un contrôle léger et robuste de la tension est encore un défi. Le remplacement des onduleurs à deux niveaux n'est pas pour tout de suite.

Le premier effort de ce projet est dévoué à l'onduleur PUC7 dans le design de son contrôleur afin qu'il soit simple et efficace. Le développement d'un nouveau modèle mathématique du PUC7 a été simplifié à un système du premier ordre. Par la suite, un contrôleur non linéaire en cascade est développé et appliqué pour réguler la tension des condensateurs au tiers de la tension d'alimentation. Cela permet de générer 7 niveaux de tension identiques à la sortie et peut alimenter des charges linéaires et non linéaires.

La topologie à cinq niveaux, le PUC5, est proposée pour remédier à la complexité du contrôleur du PUC7. La tension du condensateur flottant est régulée à la moitié de la tension d'alimentation afin de générer les niveaux de tension à la sortie. Malgré le nombre moindre de niveaux de tension, il est démontré que le PUC5 nécessite une technique de balancement très simple due à la redondance des niveaux de tension. De plus, une technique de balancement des condensateurs sans mesure de tension a été développée et implémentée en pratique sur le PUC5 en mode onduleur autonome et connecté avec le réseau électrique.

Une configuration modifiée de la topologie PUC5 est en cours de développement afin de fonctionner comme un redresseur abaisseur avec PFC. Les performances de cette topologie en tant que redresseur est très semblable à un montage abaisseur. Cependant, le réseau voit le convertisseur comme un montage élévateur. Le contrôleur est conçu afin de balancer la tension de sortie et pour synchroniser le courant d'entrée avec le réseau. Un bilan de puissance est réalisé afin de démontrer les variations limites de la charge.

Toutes les simulations et résultats théoriques sont validés expérimentalement.

Mots-clés: Cascade de Contrôle Non-Linéaire, Converter Multiniveau, Packed U-Cell, PUC5, Qualité de l'Énergie, Conversion de l'Énergie Renouvelable

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LIST OF ABREVIATIONS

AC	Alternative Current
APOD	Alternative Phase Opposite Disposition
CHB	Cascaded H-Bridge
CSC	Crossover Switches Cell
DC	Direct Current
FB	Full Bridge
FC	Flying Capacitor
FFT	Fast Fourier Transform
HB	Half Bridge
IPD	In-Phase Disposition
KVL	Kirchhoff's Voltage Law
NPC	Neutral Point Clamped
PF	Power Factor
PFC	Power Factor Correction
PI	Proportional Integral
POD	Phase Opposite Disposition
PUC5	5-Level Packed U-Cell
PUC7	7-Level Packed U-Cell
PWM	Pulse Width Modulation
SHE	Selective Harmonic Elimination
SHM	Selective Harmonic Mitigation
SPS	SimPowerSystem
STATCOM	Static VAR Compensator

INTRODUCTION

The volume of the energy generation and distribution systems have increased significantly in recent years (Leopoldo G. Franquelo, 2012). Based on energy statistics shown in Figure 0.1, the world electricity energy consumption is increasing continuously that requests more power generation especially from renewable energy resources (wind and solar) (Enerdata, 2015). As a statistical outlook (British-Petroleum, January, 2013), total electricity consumption will be 61% higher in 2030 than in 2011. Besides, renewable energy reaches a 6% share of global energy production by 2030, up from 2% in 2011. Renewable energy resources play an important role in generating power due to green energy and low environmental impacts. However, their output is not useable by consumers and needs to be boosted and converted into a smooth AC waveform to deliver desired power to the grid with low harmonics which needs high power inverters with higher efficiency. Moreover, the industries demand higher power equipment which are more than megawatt level such as high power AC drives which are usually connected to the medium voltage networks (2.3, 3.3, 4.16 and 6.9 kV) (Rodriguez, Lai et Peng, 2002).

The output of a conventional 2-level inverter is just $+V_{dc}$ or $-V_{dc}$ from a DC capacitor with the voltage magnitude of V_{dc} that has a lot of harmonics which is vital to be filtered. Regarding these values, the switches have to suffer high amount of voltage and current if such type of inverter is used in high power applications such as mining applications, high power motor drives, PV or Wind farm energy conversion systems and etc. On the other hand, high frequency operation is also limited for high power applications due to increased power losses. Moreover, it is required to use high voltage switches which are limited by the existing technologies as shown in Figure 0.2 (Wikipedia, 2012). One solution to overcome that limitation is using more switches and capacitors in series that can divide the voltage among the switches which is shown in Figure 0.3, but that increases the number of components significantly which need more DC isolators and physical space for the converter consequently (Rodríguez et al., 2007).

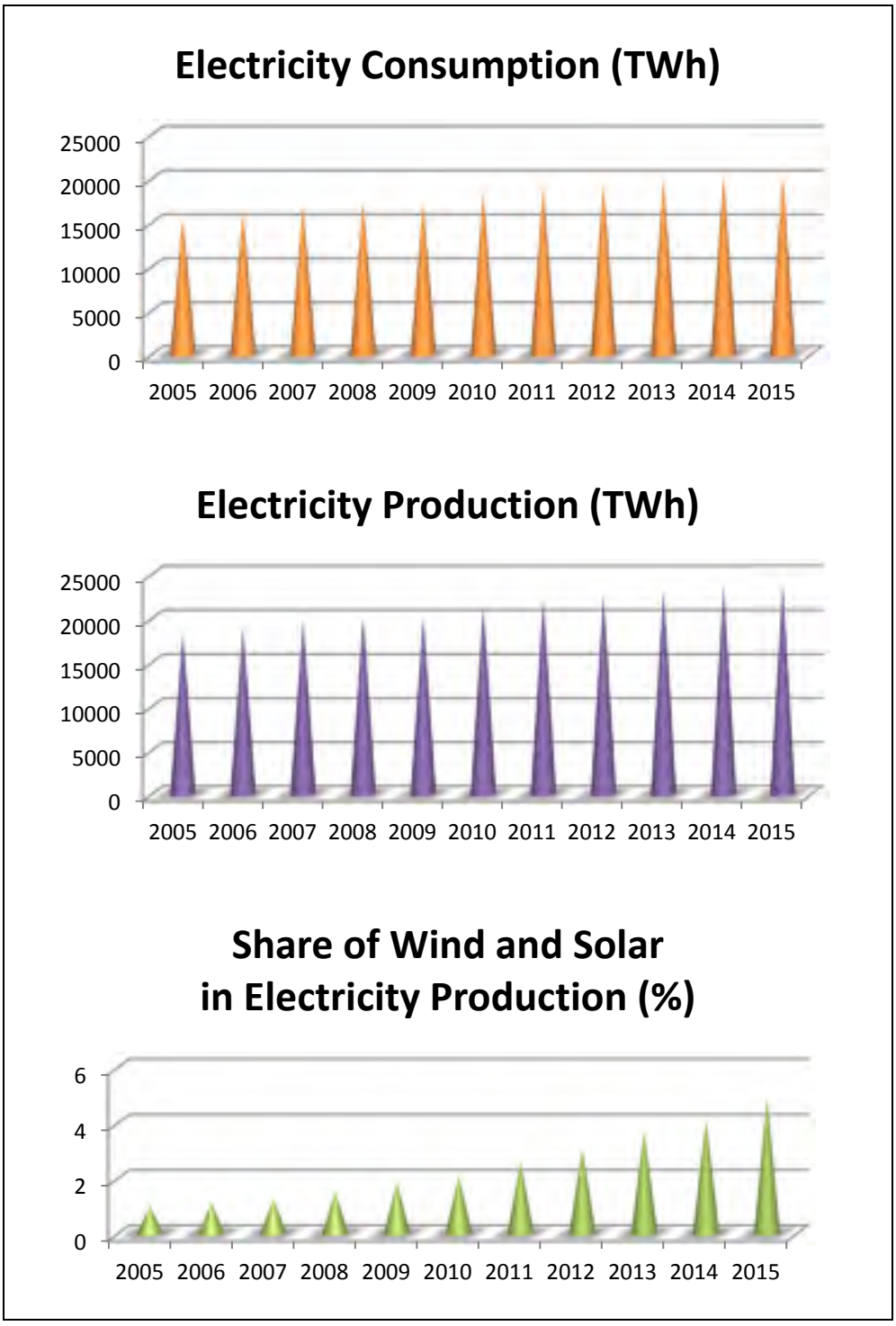

Figure 0.1 Electricity energy statistics in the world since 2005

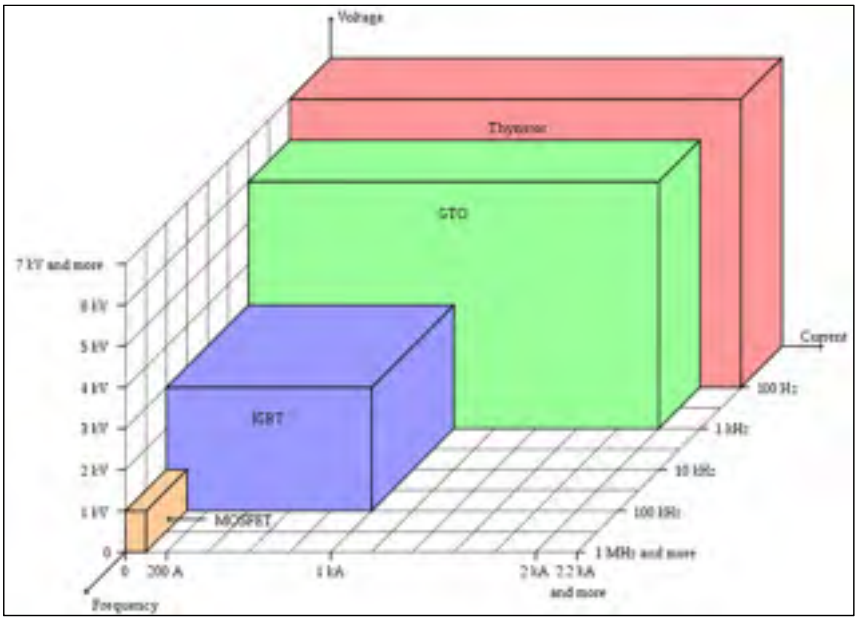

Figure 0.2 Existing technologies of semiconductor devices in power electronics applications (Wikipedia, 2012)

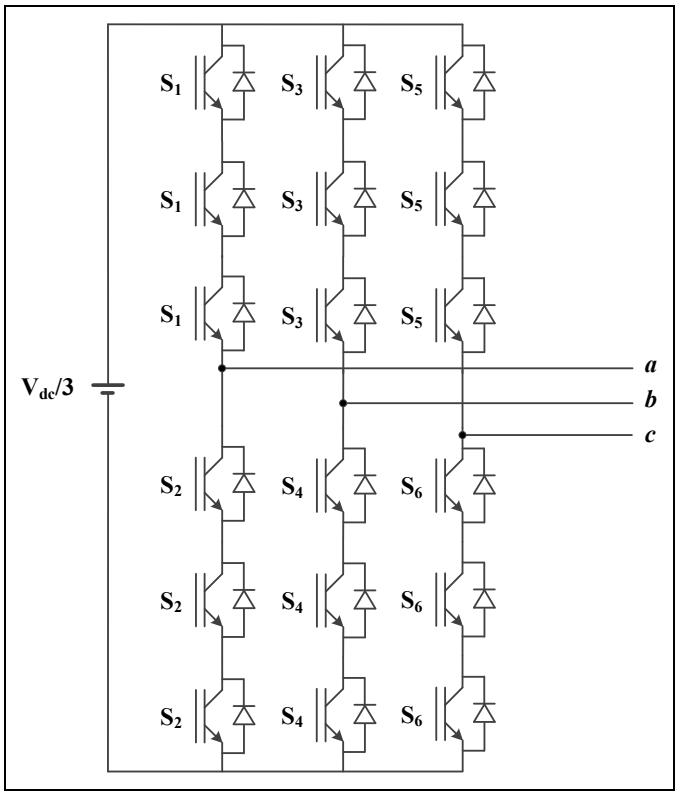

Figure 0.3 High Power VSI with series elements (switches with same names are fired coincide)

Motivation and Challenges

To resolve the above-mentioned problems, the new technology of inverters called Multilevel Inverters has been introduced employing combination of switches and DC sources to produce various voltage levels, which is being used in medium-voltage high-power applications (Rodríguez et al., 2007). Those switches are turned on and off with a pattern to produce desired combination of DC voltages at the output, while the switches are not suffering the whole DC voltage and they are just blocking a part of the DC bus. As well, producing smoother waveform leads to lower harmonic which reduces the filter size and power losses remarkably. So having less number of switches and isolated DC sources since generating high number of voltage levels at the output is always a matter of controversy where single-DC-source topologies are being considered the most suitable ones for most of the power system applications such as renewable energy conversion systems.

As large number of active switches, DC sources and capacitors are used in multilevel converters, more complicated control strategy should be designed to stabilize the voltage and keep the dynamic performance acceptable in both stand-alone and grid-connected mode of operation during healthy and faulty conditions.

Moreover, due to employing more semiconductor devices by multilevel inverters, the necessity of the modulation techniques with lower switching frequency and better performance has increased. There would be another challenge to develop the switching methods or propose new techniques in order to deal with the complex structure of multilevel inverters while balancing the auxiliary DC capacitors voltages used to increase the number of voltage levels at the output. Such voltage balancing techniques integrated into switching approaches remove the need of applying complicated external linear/nonlinear controllers to regulate the dependent DC links voltages.

Eventually, the rectifier (AC to DC conversion) mode of operation is so important for multilevel converters where low harmonic contents, low switching frequency and lower voltage rating of switches help producing a high DC voltage link with high power delivery to the batteries as one of the most challenging issues in EV charging applications.

Research Objective

Multilevel converter structure permits to generate smoother output waveform by producing different voltage levels while operating at lower switching frequency which leads to lower power losses in the power inverter and reduce the output filter size. Nowadays, the usage of such inverters has been reported up to 13.8 kV and 100 MW. In such power ratings various applications for such topologies can be mentioned, e.g.: mining applications, adjustable speed drives, renewable energy conversion, utility interface devices, reactive power compensators and etc. Moreover, multilevel rectifiers could be also used in high power applications such as newly emerged high power and super-fast chargers for EVs. The major weakness of conventional converters is limited power rating, high harmonic pollution and high switching frequency which prevents their usage when it comes to high power applications. Besides, in high power applications, the lower switching frequency is more desired to decrease the switching losses. Lower harmonic contents of voltage and current waveforms are also mandatory to reduce the size of output filters.

This project will present an improved multilevel inverter topology that can be used in high power medium voltage applications and remit the problem of using power electronics switches in high power ratings. Moreover, the low dynamic of such devices can be improved using advanced modelling and control techniques as will be proposed.

The research objectives can be summarized as the following:

- Designing and implementation of advance controllers for multilevel inverters;
- Developing voltage balancing techniques to integrate into switching pattern in order to regulate the DC capacitor voltage in multilevel inverters;
- Developing a multilevel inverter topology to work in stand-alone and grid-connected mode of operation reliably;
- Developing a multilevel rectifier topology to work in buck and boost mode of operation.

Methodology

This research has been performed in three following steps: mathematical modeling, simulation and hardware implementation.

At first literature review has been done to better understand the problems associated with multilevel converters. A thorough study has been performed about different multilevel converter topologies taking into account the number of active and passive devices, applied control strategies and switching techniques associated with the capacitor voltage balancing issue. In this step, existing models, controller, switching techniques and topologies have been simulated in Matlab/Simulink SPS toolbox to facilitate analyzing the advantages and disadvantages of those reported technologies.

The mathematical modeling of the existing and proposed topologies has been done to study the switching performance and design the advanced controllers. The developed topologies have been simulated in SPS with applied controllers to verify the good dynamic performance in stand-alone and grid-connected mode of operation. All possible transient modes such as load changing and AC or DC voltage variation have been investigated through the simulation to prevent any failure in hardware implementation.

Finally, proposed converters have been designed and made in the lab to test practically. Controllers and switching techniques have been implemented on dSpace1103 for rapid control prototyping. The OPAL-RT voltage/current measurement box has been used to sense the electrical variables and to send required information to the controller.

Thesis Contribution

The major contributions of this thesis are as the following:

Development of an improved model for the PUC7 inverter

In previous works the PUC7 inverter had been modeled based on separate switching actions. That means the concept of single input system for single-phase inverter had not been considered in modeling and controller design. Therefore, each switch was fired separately

without noticing the action on other switches. In this work a new model has been obtained for PUC7 inverter taking into account all switching states as a group of switching pulses. Therefore, no switch works individually and a set of switches are turned on/off together to generate the desired voltage level at the output. The new model complies with the mentioned concept of single input for single-phase converters. Thus, the controller could be designed using a single input to the inverter which would be modulated by PWM block to send the corresponding pulses.

Design of a low switching frequency controller for PUC7 inverter

PUC7 inverter was proposed in 2009 on which a feedback linearization control had been applied using that modeling with separate switching actions. Such process has the risk of missing some commutations at the right time results in producing a wrong voltage level. Afterwards, a hysteresis controller had been also implemented on the PUC7 inverter which has its own drawbacks such as high and variable switching frequency. In this project, new nonlinear controller has been designed and implemented on the PUC7 inverter based on the improved modeling. The applied controller does not need a new feedback from the system so it uses the existing data sent from adjusted sensors to compensate the nonlinearities of the converter model. Such robust controller allowed the PUC7 inverter to operate at low switching frequency while showing acceptable results. Moreover, the new nonlinear cascaded controller could be applied on all converters with voltage and current control loops like rectifiers or grid-connected inverters. Compared to a cascaded PI Controller, the designed nonlinear one shows better operation on all single-phase converters with fast error tracking while does not increase the complexity of calculations and implementation.

Design of a new multilevel inverter topology (PUC5)

After full investigation of PUC7 and analyzing its drawbacks, the PUC5 topology has been proposed in this thesis with most reliable performance and easy to use in various applications. The modified topology needs less number of switches considering the equal voltage rating and generates 5 voltage levels at the output with voltage THD of about 10% which is at least 10 times less than a 2-level waveform harmonics. The main feature of the

PUC5 topology is the fact that there are some redundant switching states which can be used for easy voltage balancing of the DC link capacitor. Due to new voltage rating of the switches, the PUC5 inverter could be implemented by 4 half-bridge modules.

Development of a sensor-less voltage balancing technique integrated into PWM switching block for PUC5 inverter

The most promising feature of PUC5 topology is the ability of balancing its DC link capacitor without using any voltage sensor as feedback to the controller. In fact, the auxiliary capacitor voltage is balanced using redundancy switching states but no voltage sensor or observer. It has been proved mathematically and experimentally that the capacitor voltage maintains the desired level during switching actions by the proper time of charge and discharge of energy. The applied technique makes the PUC5 inverter a strong potential to replace existing full-bridge converter in the market.

Design of a new multilevel buck PFC rectifier topology

The 5-level buck PFC rectifier topology has been proposed after a thorough analysis of rectifier mode of operation in multilevel converters. It generates two output DC voltages that help getting a boost operation from grid point of view. The sum of two DC voltages should be more than the AC main voltage thus the rectifier could work in boost mode while producing two output terminals in buck mode with reduced voltages. A decoupled voltage/current controller has been designed to operate the rectifier in all conditions such as AC source fluctuation or load changes. Moreover, a voltage balancing analysis has been performed mathematically and then based on simulation studies to validate the good dynamic performance of the proposed rectifier.

Thesis Outline

This thesis includes 5 chapters starting from literature review on multilevel converter topologies and switching technique and continuing on proposed topologies and controllers.

CHAPTER 1 includes a comprehensive review on the previously reported the multilevel converter topologies and switching techniques. CHAPTER 2 shows an improved modeling of

the PUC7 along with designing and implementing procedure of a nonlinear cascaded control. Experimental results are illustrated to validate the good dynamic performance of the applied controller operating at low switching frequency. The PUC5 topology with sensor-less voltage control is introduced in CHAPTER 3 with experimental results of stand-alone and grid-connected mode of operation. The theoretical studies are done to prove the ability of PUC5 configuration in self-voltage-balancing of the DC link capacitor. The 5-level buck PFC rectifier is elaborated in CHAPTER 4 with all details on designing the decoupled voltage/current controller and switching technique. Moreover, the power sharing issue between output terminals of the rectifier is analyzed and described exhaustively in this part. Simulation and experimental results validate the promising functionalities of the proposed 5-level buck PFC rectifier. CHAPTER 5 concludes the thesis and gives some ideas for future studies.

CHAPTER 1

LITERATURE REVIEW OF MULTILEVEL INVERTERS

1.1 Introduction

The multilevel converter technology has been started by the concept of multilevel step wave in cascade H-Bridge converters in the late 1960s. This was an attempt to present a new control method that was useful to produce and employ the stepped wave at the output of such inverters (McMurray, 1971). The circuit of that type of cascade H-bridge converter was presented in (Bedford et Hoft, 1964). In 1970, the Diode Clamped Converter was introduced (Baker, 1980) but all these efforts was done in low power applications.

In medium-voltage application the Neutral Point Clamped (NPC) and then the Cascade H-Bridge (CHB) have been introduced in 1980s (Baker, 1981; Nabae, Takahashi et Akagi, 1981). In addition to these two types, the Flying Capacitor (FC) inverter which was introduced in 1960 as a low voltage one, has been evolved to be employed in medium-voltage and high power industries in 1990 (Meynard et Foch, 1991).

As an application example of such devices is medium-voltage motor drive that was begun in the middle of 1980s when the 4500 V gate turn off (GTO) thyristors were commercialized (Wu, 2006). Afterwards, development of high power switches results in manufacturing insulated gate bipolar transistor (IGBT) and gate commutated thyristor (GCT) in the late 1990s (Steimer et al., 1997). These switches have been employed in medium-voltage and high power inverters rapidly because of their appeal characteristics, low power losses, simple gate control and snubberless operation (Wu, 2006).

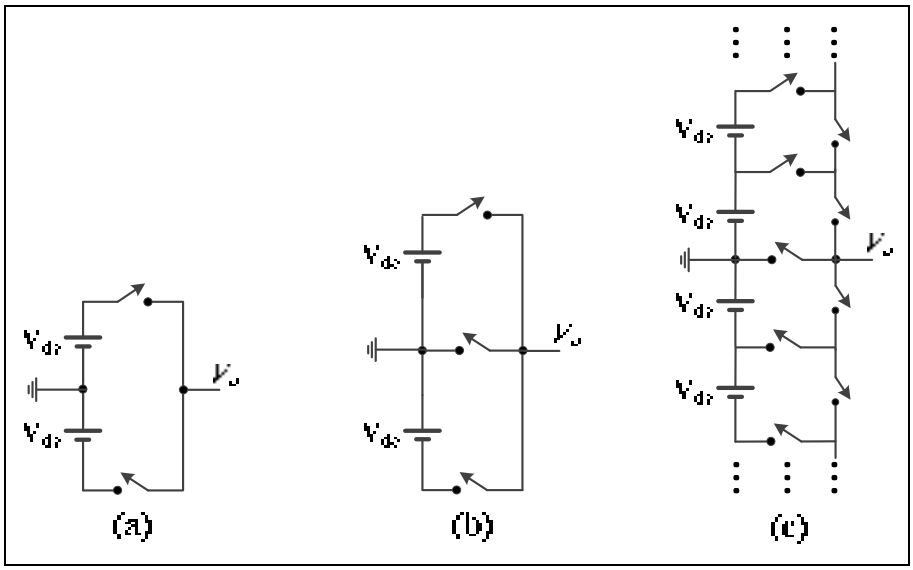

Figure 1.1 One leg of a) 2-level, b) 3-level and c) n-levels inverter

Multilevel inverter contains several semiconductor switches and DC supplies. The combination of switches actions produces various voltage levels at the output. Figure 1.1 shows the basic concept of a multilevel inverter operation. It shows the DC link and one leg of inverter in two-level, three-level and n-level configuration. The performance of semiconductor switches is shown by ideal switches. Figure 1.1-a shows a conventional inverter which can produce $+V_{dc}$ or $-V_{dc}$ at the output point of 'a' with respect to the grounded neutral point, while the three-level inverter in Figure 1.1-b produces $+V_{dc}$, 0 and $-V_{dc}$ at the output and finally the n-level inverter in Figure 1.1-c generates multilevel voltages of 0, $\pm V_{dc}$, $\pm 2V_{dc}$, … . As it is obvious from the figure, the semiconductor switches suffer only V_{dc} or less, however the output maybe more than V_{dc}. This feature of multilevel inverter helps the industries and renewably resources to reach high power demands and applications using medium-voltage equipment.

Recently, multilevel inverters are gathering the researchers and industries attention due to their attractive features. Some of the major advantages of multilevel inverters are as follows (Kouro et al., 2010; Leopoldo G. Franquelo, 2012):

- Lower distortion in the output voltage due to multiple levels of output waveform;
- Lower dv/dt (voltage stress) that leads to endure the reduced voltage by switches;

- Lower common mode voltage which is helpful in motor drives;
- Lower switching frequency results in lower switching losses.

Different types of multilevel inverters have been proposed and built which are mostly for medium-voltage and high power applications (Franquelo et al., 2008) because of the fact that a single power switch cannot be connected to a medium-voltage grid directly.

1.2 Multilevel Inverter Topologies

Different topologies have been proposed for multilevel inverters (Franquelo et al., 2008; Kouro et al., 2010; Rodriguez, Lai et Peng, 2002) which are mentioned as follows.

1.2.1 Cascade H-Bridge

The cascade H-Bridge (CHB) multilevel inverter is mostly used in medium-voltage high power drives (Wu, 2006). CHB is composed of multiple units of single-phase H-Bridge (HB) inverter which are connected in series in each phase. Figure 1.2 shows the one phase of a 7-level CHB (7L-CHB) that includes three single-phase HB cell in each phase (Malinowski et al., 2010).

In a CHB multilevel inverter the output voltage of each phase is:

$$V_{an}=V_1+V_2+V_3 \tag{1.1}$$

There are two types of CHB: One with equal DC sources and another with unequal DC sources which are described below.

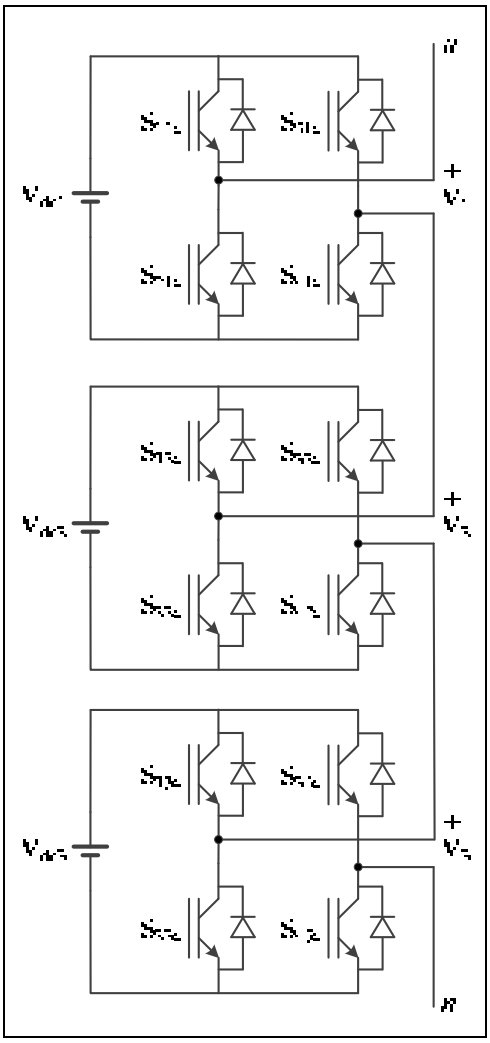

Figure 1.2 7-Level CHB

1.2.1.1 CHB with equal DC sources

Assume that $V_{dc1}=V_{dc2}=V_{dc3}=E$. To determine the number of levels in this mode the following equation can be used:

$$L=2N+1 \tag{1.2}$$

Where, L is the number of inverter levels or the output phase voltage levels. N is the number of HBs in each leg. For the Figure 1.2, there are three HBs in each leg so the CHB is a seven level inverter. The levels of inverters show the output voltage levels., so in this case, it means that the 7L-CHB in Figure 1.2 with equal DC sources would have the voltage values of 0, ±E, ±2E and ±3E which is shown in Figure 1.3 (Liu, 2009).

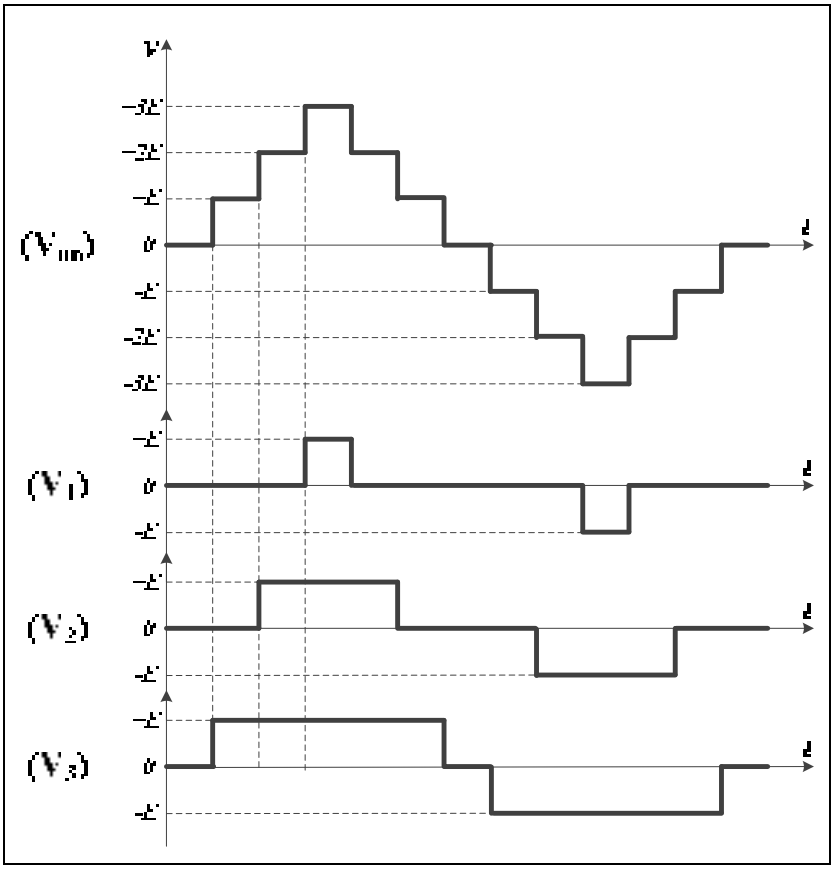

Figure 1.3 The output voltage waveform of phase a in a 7L-CHB with equal DC sources

1.2.1.2 CHB with unequal DC sources

Another type of CHB is with unequal DC sources. For instance, in Figure 1.2, consider that $V_{dc1} = E$, $V_{dc2} = 2E$ and $V_{dc3} = 4E$, so the combination of voltages results in 15 voltage levels for V_{an} which is shown in Figure 1.4. The maximum of 7E is produced while the output waveform is more similar to the sine wave with fewer harmonics.

As it is obvious from the figure 3-4, using unequal DC sources leads to more voltage levels and higher output voltages with higher power in comparison with a CHB that has the same number of cells. But CHB with unequal DC sources needs more difficult switching pattern design because of the reduction in the redundant switching states which limits the application of this type of multilevel inverter in industries (Wu, 2006). The highest levels achieves when the DC sources values are triple (Lai et Shyu, 2002; Liu et Luo, 2005). For example, if V_{dc1} =

E, V_{dc2} = 3E and V_{dc3} = 9E, then the output voltage levels will be up to 27 that can boost the output voltage to 13E and eliminates many harmonics.

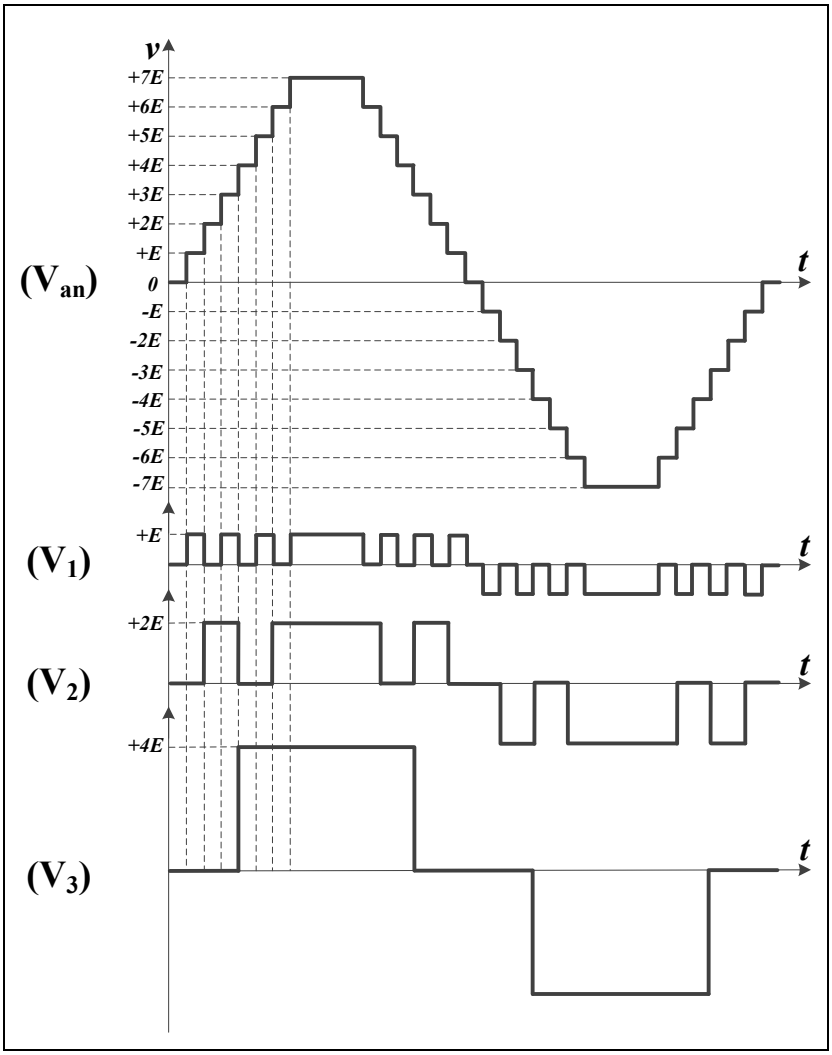

Figure 1.4 The output voltage waveform of phase a in a 15L-CHB with unequal DC sources

1.2.2 Neutral Point Clamped

Figure 1.5 shows one leg of a Neutral Point Clamped (NPC) multilevel inverter which was first introduced by Nabae (Nabae, Takahashi et Akagi, 1981) and then, the three-level NPC has found many developments and usage in industries (Rodriguez et al., 2010).

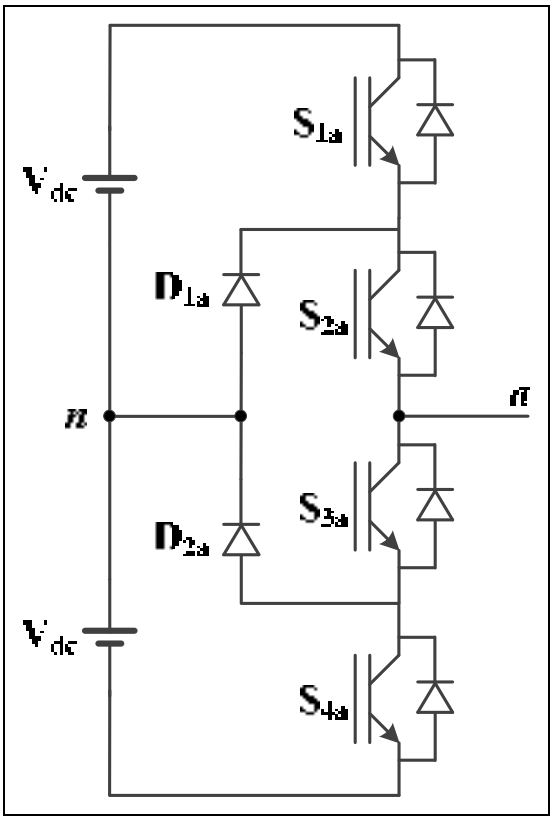

Figure 1.5 Phase 'a' of a Three Level NPC

The clamped diodes (D_{1a}, D_{2a}) are connected to the neutral point of DC capacitors that results in adding a zero level to the output voltage. Thus, in a 3L-NPC the output voltage is composed of $-V_{dc}$, 0 and $+V_{dc}$. when S_{1a} and S_{2a} are ON, the output is $+ V_{dc}$. when S_{3a} and S_{4a} are ON, the negative voltage will be appear at the output which is $-V_{dc}$. finally, if S_{2a} and S_{3a} are ON, the voltage at 'a' will be 0. S_{3a} is working in complementary of S_{1a} and the same for S_{2a} and S_{4a}. For instance, when S_{1a} is ON, S_{3a} is OFF.

One of the advantages of this topology is its flexibility for being controlled by space vector modulation (SVM) (Lewicki, Krzeminski et Abu-Rub, 2011; Rojas, Ohnishi et Suzuki, 1995) in addition to PWM. This feature makes the NPC as a desired topology for multilevel inverter for researchers to work on its control strategy and propose and test many control methods (Das et Narayanan, 2012; Lin et Wei, 2004). However the NPC is widely used in high power applications, balancing the capacitors voltages and unequal loss distribution among switches are considered as a drawback of this topology (Rodriguez et al., 2010).

1.2.3 Flying Capacitor

Another topology for multilevel inverters is Flying Capacitor (FC) which is observable in Figure 1.6 (Escalante, Vannier et Arzandé, 2002).

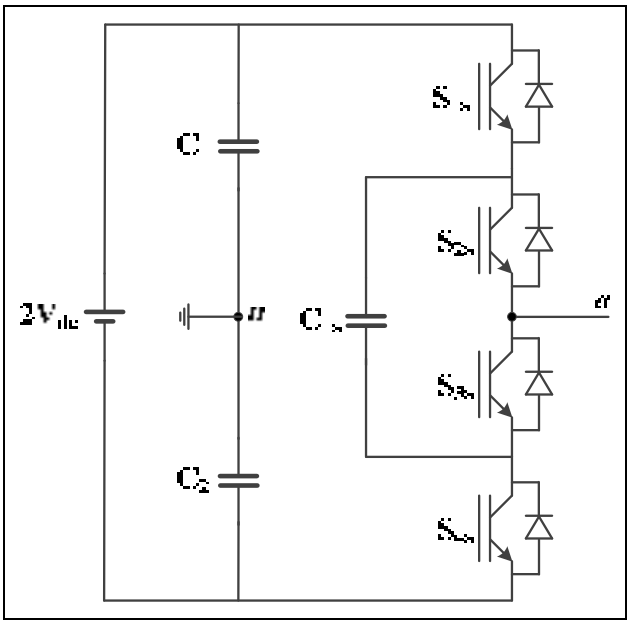

Figure 1.6 One Phase of a Three-Level FC Multilevel Inverter

The clamped diode in NPC has been replaced by a capacitor in FC model. It is derived from a two level inverter that each two switches are supplied by a capacitor. This topology produces three levels of voltages at the output which are $+V_{dc}$, 0, $-V_{dc}$. Due to employing many capacitors in FC, it needs a large number of isolators for DC capacitors and a complex voltage balancing control which limits its practical use (Wu, 2006).

In addition to these topologies, some new topologies are currently have found practical applications and these are mentioned in continue (Kouro et al., 2010).

1.2.4 Generalized Multilevel Inverter

The generalized structure was introduced by Peng in 2001 (Peng, 2001). This topology has ability to balance the capacitor voltage itself. As it is illustrated in Figure 1.7, this configuration can be expanded easily and generate more levels while self-balancing the voltage.

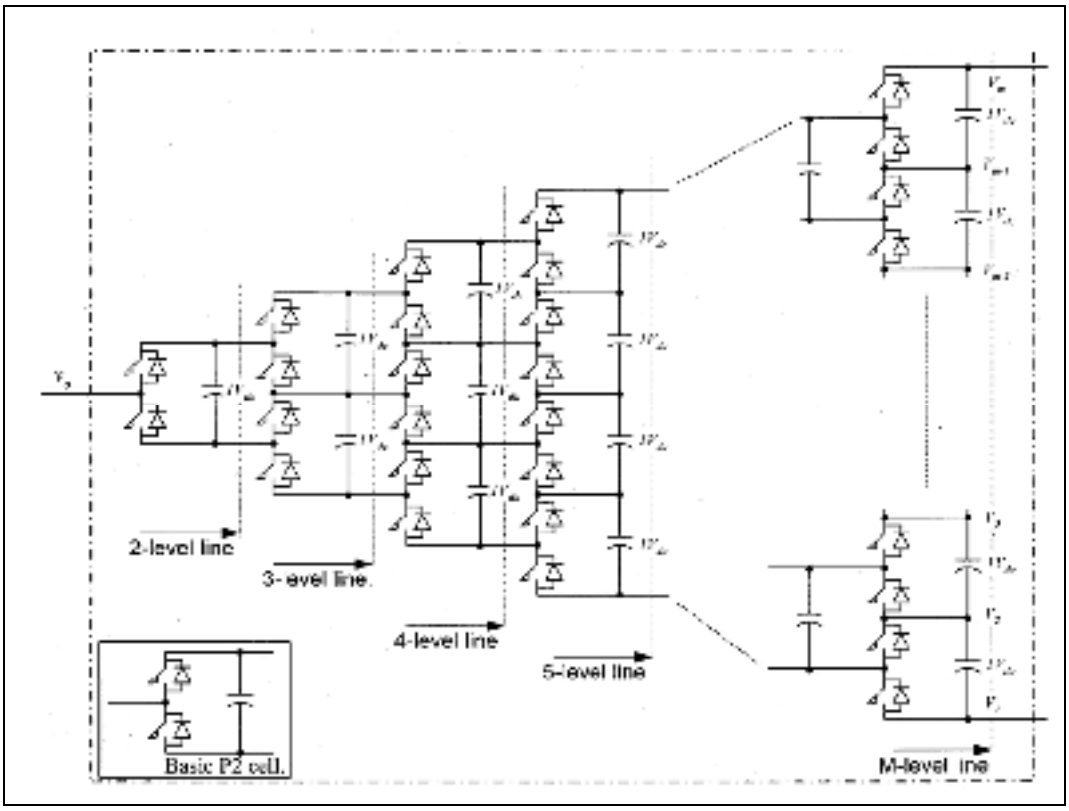

Figure 1.7 Generalized multilevel inverter topology

Being symmetrical allows deriving many other configurations from this complete configuration e.g. NPC and FC. On the other hand, using too many switches and capacitors is a limitation of this topology. However, it is a good reference of switch combinations to study and analyze the multilevel inverter structures that can result in proposing new topologies with less components and self-voltage-balancing feature.

1.2.5 Five Level H-Bridge Neutral Point Clamped

The Five Level H-Bridge Neutral Point Clamped (5L-HNPC) contains two 3L-NPC leg connected in H-Bridge format in each phase, which was first introduced in 1990 (Wu, Lau et Chung, 1999) and have been developed later (Cheng et Wu, 2007). This type of combinations is called hybrid multilevel inverters. As shown in Figure 1.8, there are lots of semiconductors that make the switching method more complicated while the output voltage is a five-level waveform and produce more power up to 120 MVA (Kouro et al., 2010).

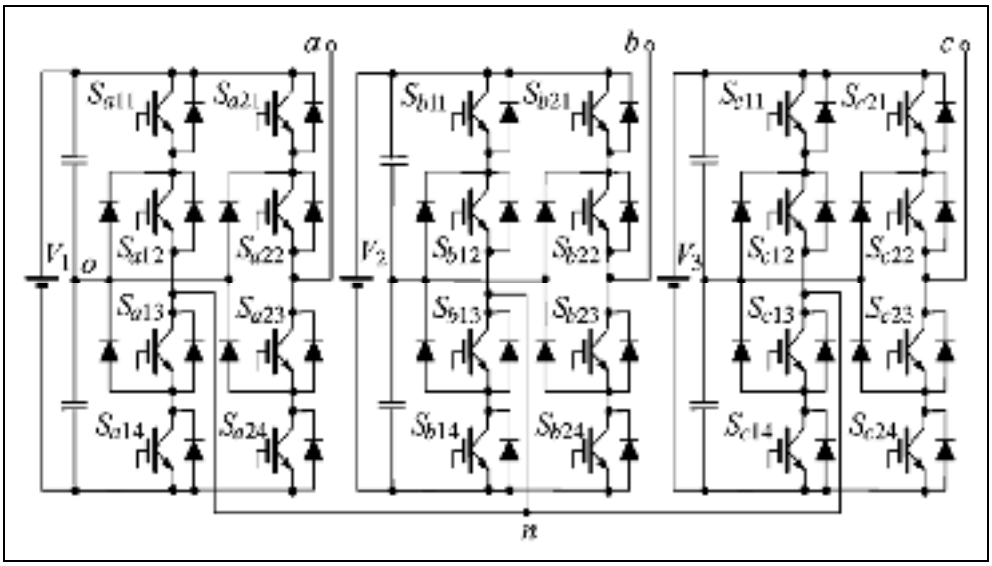

Figure 1.8 5L-HNPC multilevel inverter

Assume that $V_1 = V_2 = V_3 = 2E$ and each capacitor has a voltage of E. so the output of NPC would be +E, 0, -E and the output of the 5L-HNPC is 0, ±E, ±2E.

1.2.6 Three Level Active Neutral Point Clamped

One of practical issues with NPC is the unequal semiconductor distribution losses due to non-identical voltage stress on switches leads to asymmetrical heat sink for these switches. Moreover, there would be some junctions with different temperature in NPC structure. This issue can be solved by replacing the clamping diodes in NPC with clamping semiconductor switches. These active clamping switches make controllable path for current through the neutral point and other switches, hence the losses distribution can be controlled significantly (Bruckner, Bernet et Guldner, 2005). Figure 1.9 shows the 3L-ANPC.

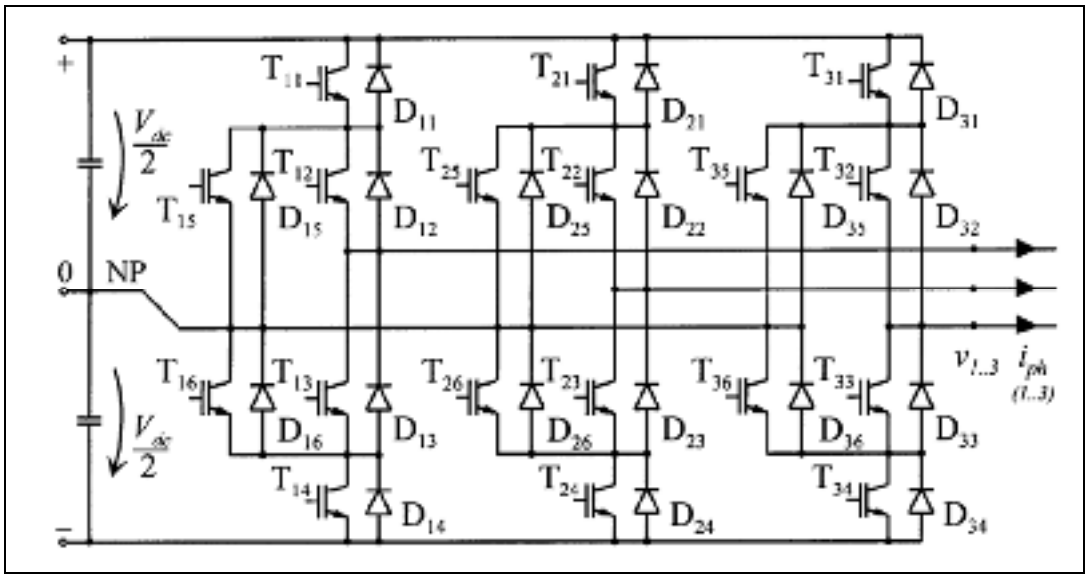

Figure 1.9 3L-ANPC with Active Clamped Switches

1.2.7 Modular Multilevel Converter

Modular Multilevel Converter (MMC) is composed of multiple cells of single-phase half-bridge or full-bridge inverters in modular structure. This topology is mostly used for transmission systems, particularly in HVDC (Gemmell et al., 2008). Figure 1.10 shows a MMC that contains a lot of cells. As it is shown in the phase ‘a’ of the figure, each cell consists of two semiconductor switches which are controlled by complementary pulses. These cells produce their DC voltage at the output so there would be an array of these DC voltages that makes multilevel voltage at the main output of phases (Kouro et al., 2010). Modularity of the MMC allows adding levels to reach medium and high voltage levels.

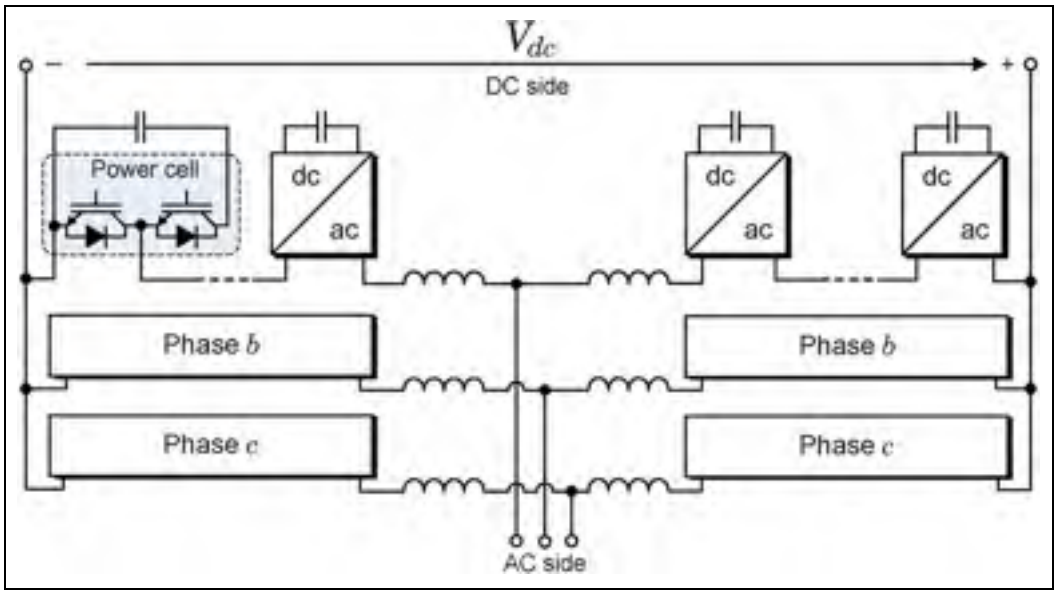

Figure 1.10 Modular Multilevel Converter (MMC)

1.2.8 Three-Level T-Type Inverter

A Three-Level T-Type inverter has been proposed in (Guennegues et al., 2009) which is similar to ANPC and shown in Figure 1.11.

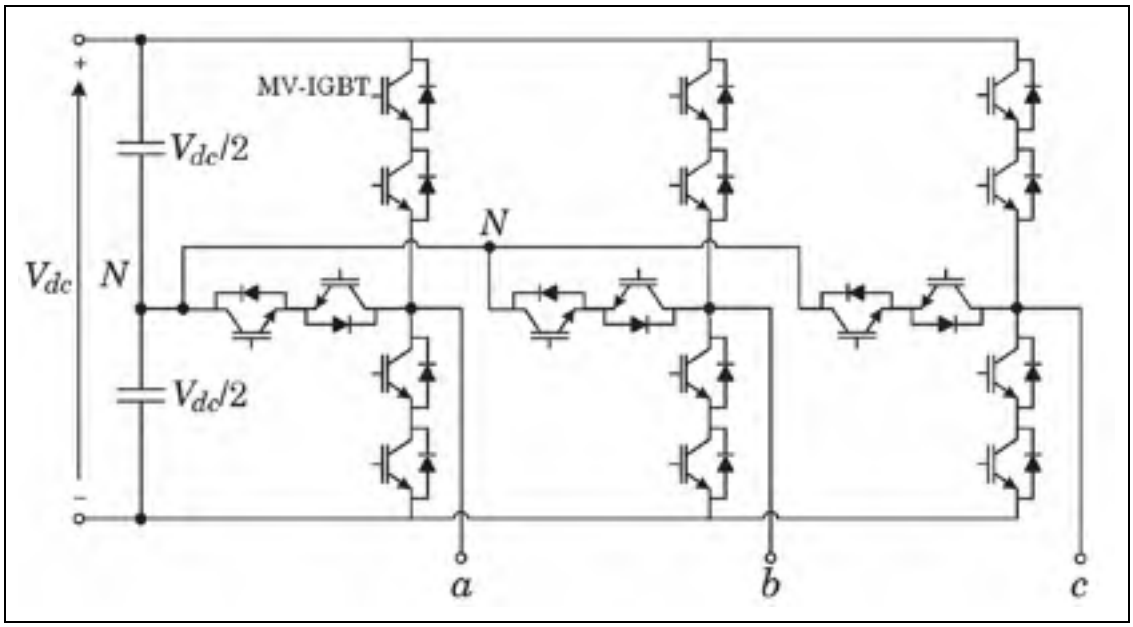

Figure 1.11 3L-NPP

In that topology, each leg is connected to the neutral point through a bidirectional switch based on two anti-series connected IGBTs. Due to controllable path to the neutral point, the

switching losses can be distributed equally. The zero level is achieved when these two IGBTs are ON. This topology can work in higher frequency due to distributed switching losses and would be suitable for variable high speed applications such as train traction drives (Kouro et al., 2010).

1.2.9 Packed U Cell

A single-phase seven level Packed U Cells (PUC) multilevel converter has been illustrated in Figure 1.12 (Al-Haddad, Ounejjar et Gregoire, 2010; Ounejjar, Al-Haddad et Grégoire, 2011). This topology is a combination of FC and CHB with reduced number of capacitors and semiconductors.

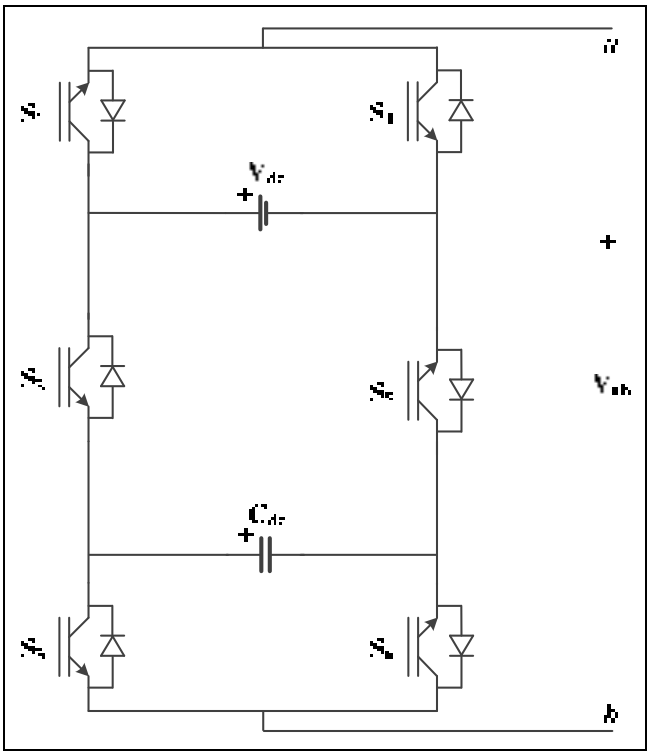

Figure 1.12 Single-Phase 7L-PUC

As it is obvious in Figure 1.12, there are just six switches and two DC buses to produce seven levels of voltages at the output. The higher voltage is produced by the switch with lower switching frequency results in suppressing the switching stress significantly. Using the value of $V_{dc}/3$ for the capacitor voltage (C_{dc}) leads to generate the output voltage levels of 0, $\pm V_{dc}/3$, $\pm 2V_{dc}/3$, $\pm V_{dc}$.

1.2.10 Pinned Mid-Points (PMP)

The PMP multilevel inverter topology has been shown in Figure 1.13 (Vahedi, Rahmani et Al-Haddad, 2013). It is a modification on T3 inverter in which for the higher levels there is no need to add bidirectional switches and only one single switch would be enough.

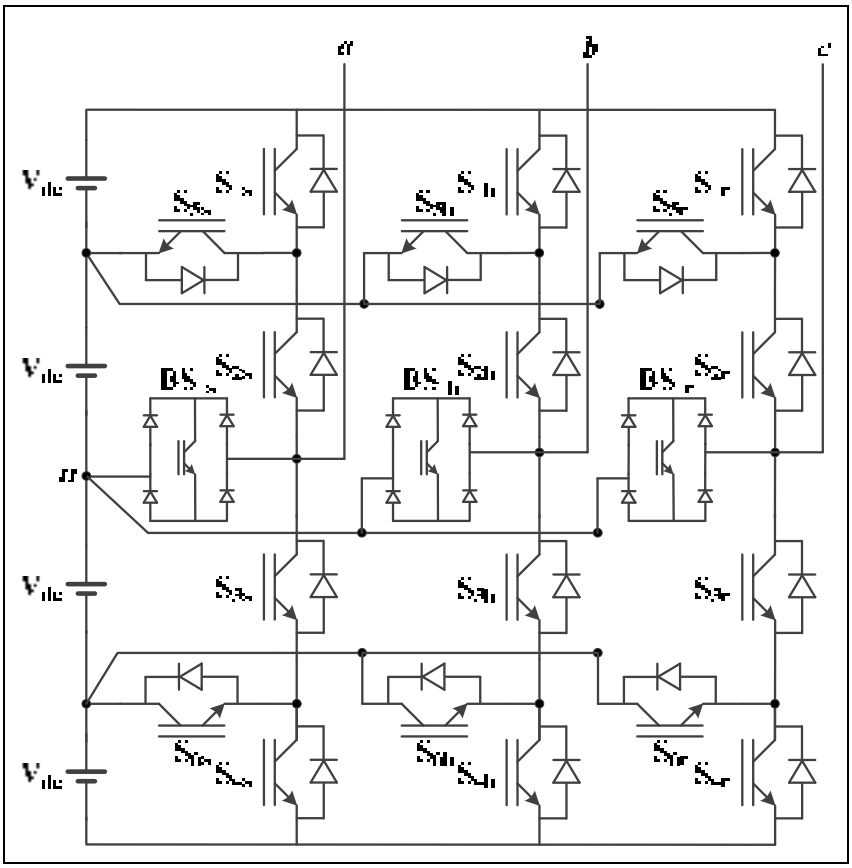

Figure 1.13 Three-phase 5-level PMP inverter

It has the advantages of NPC and T-type topologies such as common DC bus for all phases but the main issue is the voltage balancing when a single-dc-source is used and 4 capacitors voltages should be regulated effectively.

1.2.11 Crossover Switches Cell (CSC)

The CSC inverter illustrated in Figure 1.14 has been developed (Vahedi et al., 2013)as a combination between CHB and PUC in which a single-dc-source is used and the auxiliary capacitor is controlled to have a maximum voltage at the output. Some similar efforts have been done on CHB to use a single-dc-source (Vahedi et Al-Haddad, 2015b; Vahedi et al.,

2015b). The output peak voltage is the sum of DC source and DC capacitors levels but there are some limitations on the modulation index.

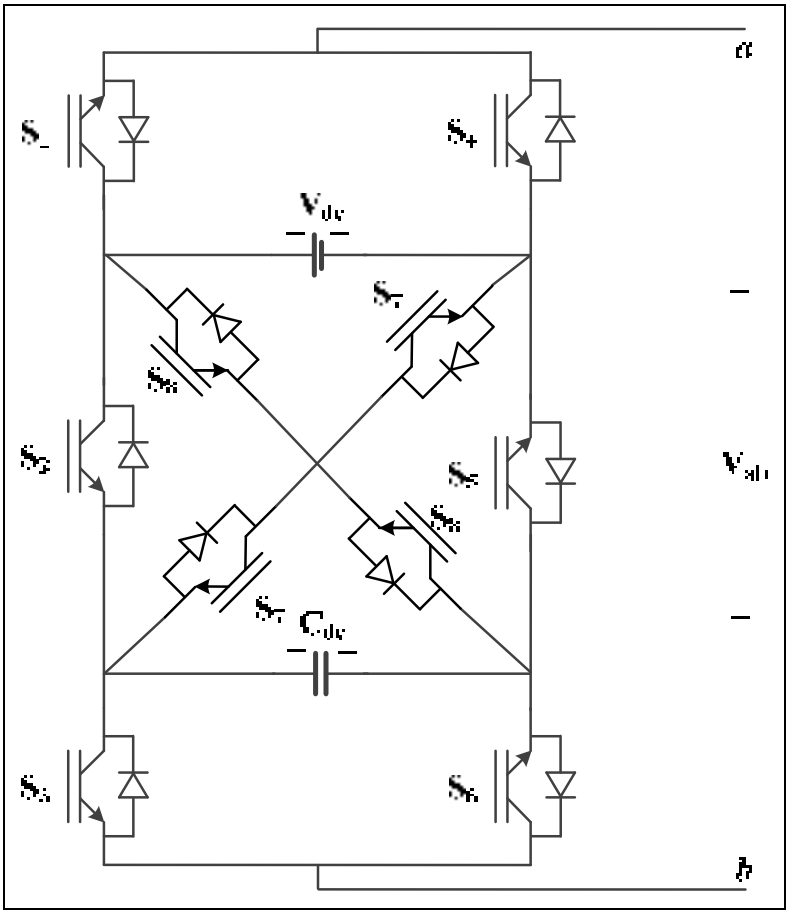

Figure 1.14 9-Level CSC inverter topology

It generates the highest number of levels among other reported multilevel inverter topologies while using only a single-dc-source and 10 switches.

1.2.12 Other Multilevel Inverter Topologies

In addition to the above-mentioned topologies, so many other ones are proposed and reported in the literature which exceeds size of this report. Some of new introduced topologies are illustrated as the following.

Figure 1.15 shows a five-level inverter (Abd Rahim, Mohamad Elias et Hew; Ceglia et al., 2006). In this topology a HB with two dc capacitors are used that the capacitors' middle point

is connected to the load by an auxiliary switch and four clamping diodes. The auxiliary circuit makes the other two levels in beside to the three-level output of a single HB. So, the output of proposed inverter will be a five-level wave (±Vs, ±Vs/2, 0).

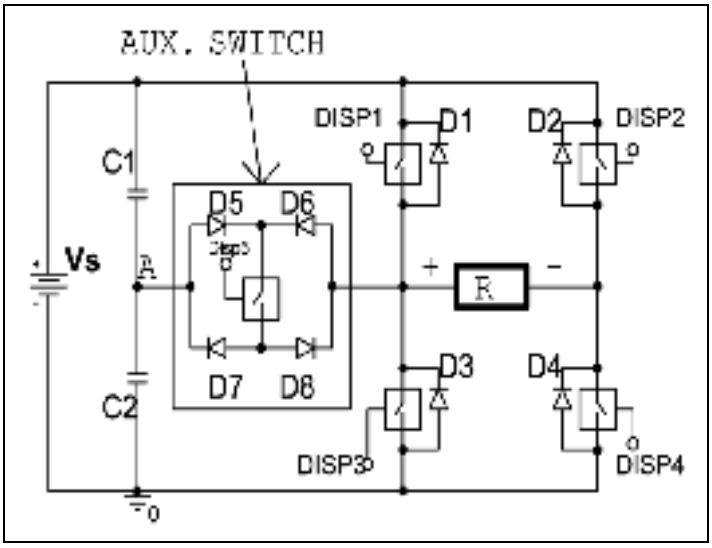

Figure 1.15 Simplified five-level inverter

The above topology generates the higher value of Vs which is equal to its DC supply as well as the switching frequency of the implemented model was high, so it cannot be used in high-power applications.

Another five-level inverter topology has been introduced in (Li et al., 2012) using coupled inductance and a HB. Figure 1.16 shows the circuit of this inverter. A single HB can generate three voltage levels, while the coupled inductances make it possible to generate more voltage levels. These inductances can divide the output voltage into half of the main DC source. So the output includes 5-levels (±2E, ±E, 0). But it has the same problem as the previous topology in generating higher voltages than the DC source.

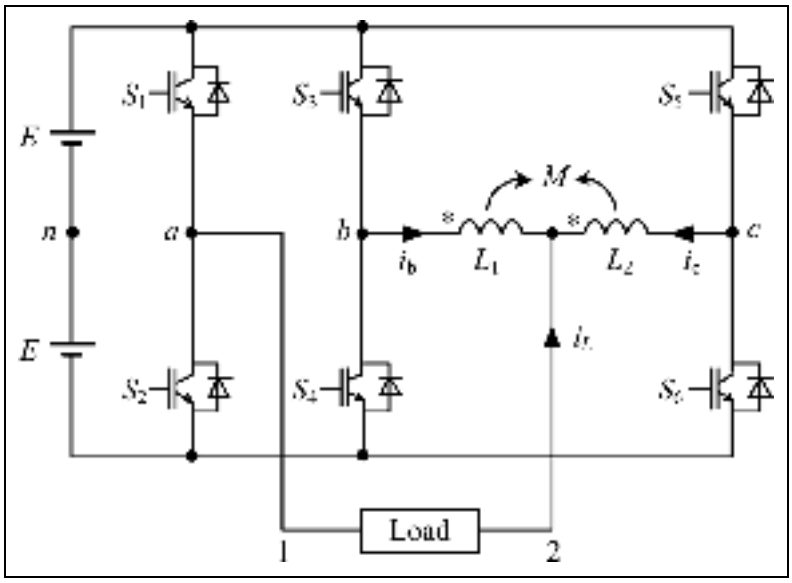

Figure 1.16 Five-level coupled inductance inverter

A five-level inverter is shown in Figure 1.17 (Waltrich et Barbi, 2010). Each phase is composed of four cells and each cell is a half-bridge inverter. The connection structure of the cells is clear in the figure. Since each phase generates a five-level waveform, the line to line voltage will have nine levels.

One of drawback of this topology is its too many number of DC sources that needs a large number of isolated transformers and rectifiers. However, the authors mentioned it as an alternative for CHB with similar characteristics like output voltage, current and harmonics.

Another multilevel inverter topology using half-bridge cells has been proposed in (Batschauer, Mussa et Heldwein, 2012) and illustrated in Figure 1.18. This configuration can produce 4, 5 and 6 levels of voltage based on using equal or unequal DC sources (V_x & V_y). In this topology the half-bridges in each phase are connected to a common three-phase VSI that reduces the number of DC sources. Although the number of DC sources increases in such topology, the output power is more than the same CHB or NPC with lower switches ratings.

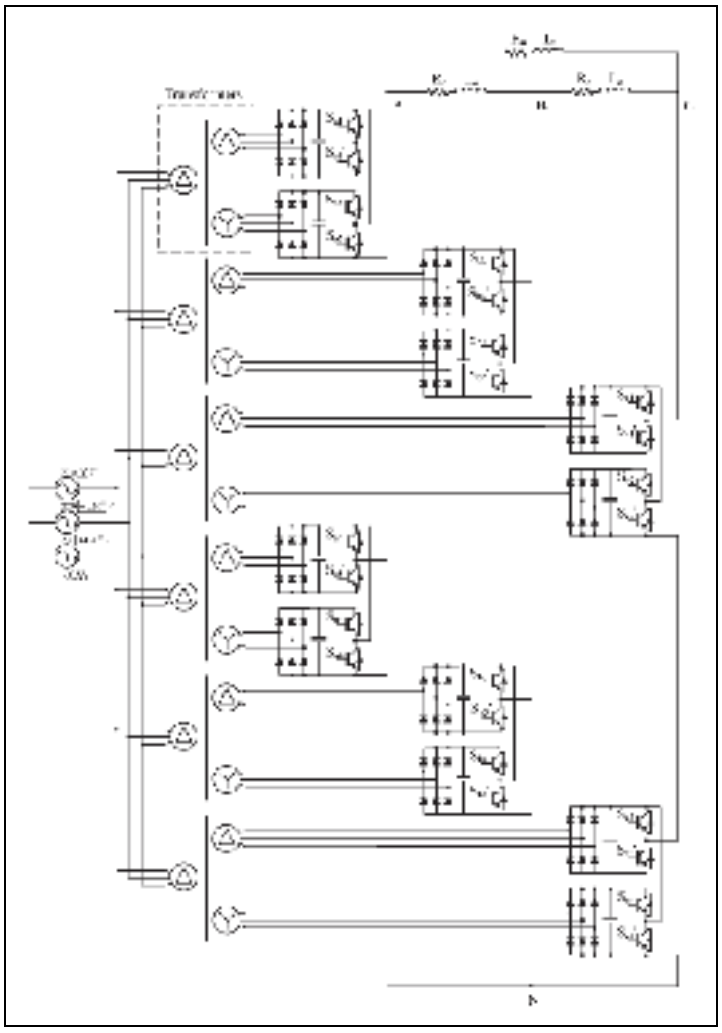

Figure 1.17 Five-level inverter using half-bridge cells

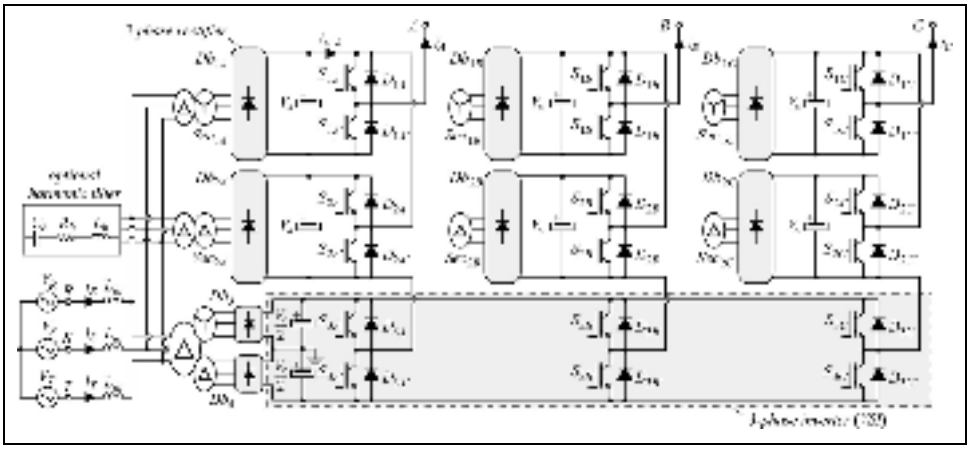

Figure 1.18 Multilevel inverter using half-bridge and three-phase VSI

Some other types of multilevel inverters are based on using combination of switches and DC sources to produce positive voltage levels. Afterwards, to produce both negative and positive parts of output cycle, a HB is employed. The HB can produce positive and negative half-cycle of a waveform from a positive DC voltage source. Therefore, all levels required to generate a full-cycle at the output are made (Banaei et al., 2012; Hinago et Koizumi, 2010; Kangarlu et Babaei, 2013; Najafi et Yatim, 2012; Ruiz-Caballero et al., 2010). Figure 1.19 shows one of these hybrid types of topologies (Najafi et Yatim, 2012).

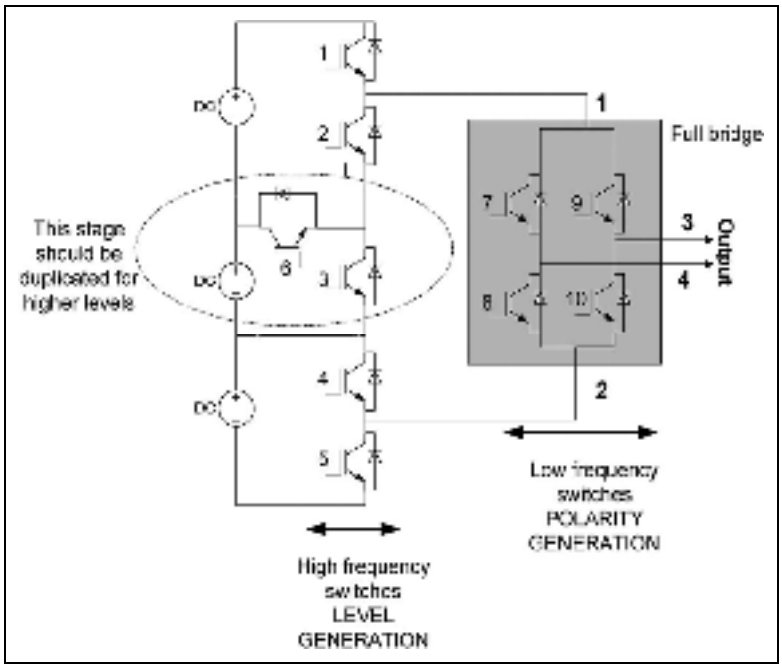

Figure 1.19 Seven-level hybrid multilevel inverter using HB cell to change the polarity

The left-side circuit is responsible for generating positive levels. This part should be high frequency to produce required levels for the HB. The right-side circuit (HB) has to change the polarity in half-cycle and generates the positive and negative levels which is not that high frequency. This part is called polarity generation. As it is obvious, these hybrid topologies require more switches due to presence of at least one impartible HB.

Finally, it should be mentioned that there are lots of research and papers about multilevel inverter topologies like: using current source inverters (Kwak et Toliyat, 2006; Noguchi, 2011), cascading three-phase VSIs or other types of multilevel inverter topologies to feed a

three-phase open-end winding machine (Barry et Veeramraju, 2013; Casadei et al., 2008; Mathew et al., 2013; Teodorescu et al., 2002), other hybrid multilevel inverters (Nami et al., 2011; Roshankumar et al., 2012) and etc., but as these types of inverters are not used and popular than described topologies, they were not illustrated in this report.

1.3 Switching Techniques of Multilevel Inverters

Multilevel inverters have much more switching components which can produce more power losses and makes the design of modulation methods more complex. Since the multilevel inverters are used in high power applications, it is preferred to implement modulation methods with low switching frequency due to reduce the switching losses. According the mentioned issue, in spite of many modulation methods introduced for multilevel inverters, there are just a few techniques which have found their way to the industries. PWM, SVM, SHE and SHM have been considered suitable to generate pulses for multilevel semiconductor components. Among these methods, the PWM is mainly used in industries (*Development of a New Multilevel Converter-Based Intelligent Universal Transformer: Design Analysis*, 2004) and SVM is being developed for industrial usage. SVM is now implemented on a 3L-NPC by ABB (Franquelo et al., 2008; Kouro et al., 2010). In following sections, the PWM and SVM are explained (Gupta et Khambadkone, 2006; Lewicki, Krzeminski et Abu-Rub, 2011; McGrath et Holmes, 2002; Wu, 2006; Yao, Hu et Lu, 2008).

1.3.1 Pulse Width Modulation

The sinusoidal PWM concept for a two level conventional inverter is shown in Figure 1.20. v_{mA}, v_{mB} and v_{mC} are sinusoidal modulation waves for three phases of the inverter and v_{cr} is the triangular carrier wave which is used for modulation action (Wu, 2006).

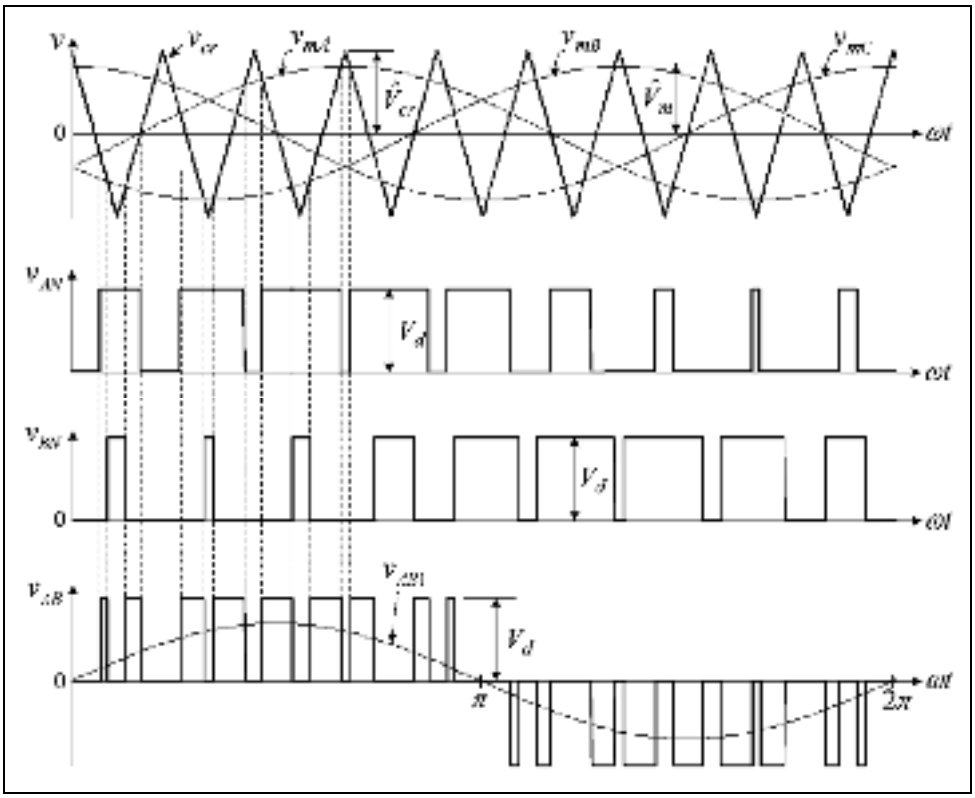

Figure 1.20 Sinusoidal PWM

In Figure 1-20 the phase voltages of 'a' and 'b' as well as the line voltage of 'ab' have been drawn that are for a typical VSI shown in Figure 1.3. The three sinusoidal modulation waveforms are compared with a carrier wave and produce three pulses that turn on and off the upper semiconductor switches (S_1, S_3 and S_5). The lower switches in each leg work unlike the upper one.

The output AC waveform frequency can be controlled by amplitude modulation index which is defined by below equation:

$$m_a = \frac{\hat{V}_m}{\hat{V}_{cr}} \qquad (1.3)$$

Where, $\hat{V}_m$ is the maximum value of the sinusoidal modulation wave and $\hat{V}_{cr}$ is the peak value of carrier wave. This index is usually adjusted by varying $\hat{V}_m$. m_a should be between 0 and 1. The switching frequency is the frequency of carrier wave.

The PWM technique for multilevel inverters uses the same concept as above but it is a bit different from the one for conventional VSI which has been described (McGrath et Holmes, 2002). The n-level multilevel inverter needs n-1 firing pulses in each phase. For example a 3L-NPC requires two separate pulses for S_{1a} and S_{2a} and the complementary pulses fire the switches S_{3a} and S_{4a} of Figure 1.5. For the illustrated 7L-CHB in Figure 1.2, six pulses are needed because each HB in each phase is fired with two pulses. To generate separate pulses from one sinusoidal wave the PWM technique has been modified and developed. These developed PWM methods are known as Level-Shifted PWM and Phase-Shifted PWM which are described as the following:

1.3.1.1 Level-Shifted PWM

As explained above, for n-level multilevel inverter, n-1 carrier wave would be compared by sinusoidal wave. In two-level PWM assume the triangular wave amplitude range is –v to v, and then in Level-Shifted PWM, the carrier waves would have same frequency and amplitude. Note that the amplitudes of n-1 carriers are $\frac{1}{n-1}th$ times of the carrier in two-level PWM. These carrier waves are vertically disposed such that the bands they occupy are adjacent. There are various methods in moving the carriers vertically:

- In-Phase Disposition (IPD): all carriers are in phase;
- Alternative Phase Opposite Disposition (APOD): all carriers are alternatively in opposite disposition;
- Phase Opposite Disposition (POD): all carriers above the zero reference are in phase but in opposition with those below the zero reference.

Figure 1.21 gives an example of these three types of carrier disposition in Level-Shifted PWM.

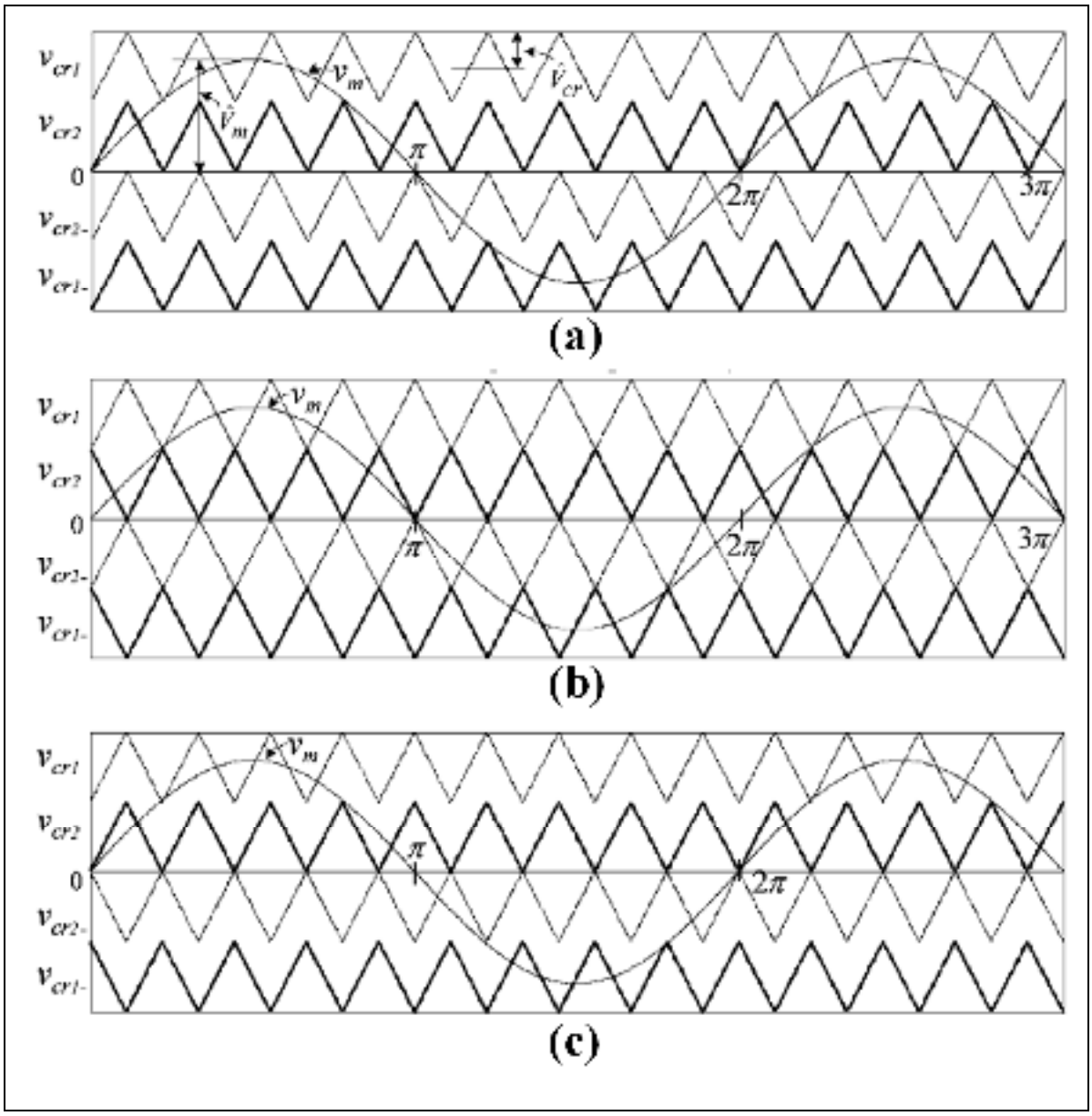

Figure 1.21 Level Shifted PWM Carriers for 5L Inverter: a) IPD , b) APOD , c)POD

As it is obvious from this figure, these carriers are for a 5L inverter that needs four pulses in each leg. For instance, consider a 5L-CHB that have two HBs in each leg and each HB needs two pulses. v_{cr1} and v_{cr1-} are for first HB, and similarly, v_{cr2} and v_{cr-2} are for the second HB. Figure 1.21-a, b and c respectively show the positions of carriers in IPD, APOD and POD that have been defined before. The switching pulses will be generated by comparing the carriers with the modulation wave like the main PWM method.

1.3.1.2 Phase-Shifted PWM

In Phase-Shifted PWM technique, n-1 triangular waves would have the same frequency and amplitude as the carrier in conventional PWM but there is a phase shift between adjacent carrier waves which is:

$$\phi_{cr} = \frac{360^{\circ}}{n-1} \tag{1.1}$$

The carrier waves for a 7L-CHB is drawn in Figure 1.22. A seven-level multilevel inverter requires six carrier waves. So these carriers should have 60º phase shift, consecutively. These carriers are shown in the figure by v_{cr1}, v_{cr2}, v_{cr3}, v_{cr-1}, v_{cr-2} and v_{cr-3}. As the phase difference is 60º, so the fourth carrier would have 180º with the first one and similarly for the fifth and sixth carrier waveforms that would be the inverse of the second and third carrier waveforms.

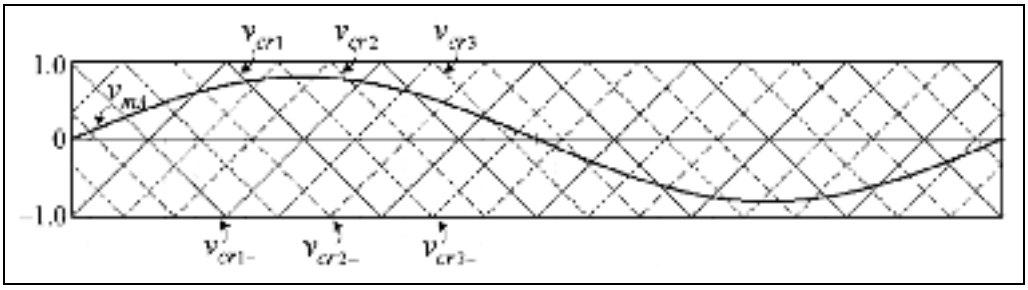

Figure 1.22 Phase Shifted PWM Carriers for 7L-CHB

Except the procedure of carrier waves, the other steps of generating pulses are like the Level-Shifted PWM. It should be mentioned, that this technique does not have good results for NPC multilevel inverters and is just suitable for CHBs.

1.3.2 Space Vector Modulation

SVM is a technique that uses vector concept to generate pulses for switches. In this technique the voltage vectors produced by each set of switching states is calculated. Then, the magnitude and phase of the reference voltage vector will be determined instantaneously. By considering the reference voltage vector location, a combination of nearest voltage vectors will be chosen and the corresponding switches to generate these voltage vectors will be fired

for specified intervals. This time intervals are calculated based on reference voltage vector information (Gupta et Khambadkone, 2006; Yao, Hu et Lu, 2008).

A detailed study of SVM for 3L-NPC has been done and presented in (Wu, 2006). This procedure is briefly described here.

In each leg of a 3L-NPC, three switching state occurs as shown in Table 1-1.

Table 1.1 Switching States of one phase of a 3L-NPC

Switching States	**S_1**	**S_2**	**S_1'**	**S_2'**	**Output Voltage (v_{an})**
P	ON	ON	OFF	OFF	E
O	OFF	ON	ON	OFF	0
N	OFF	OFF	ON	ON	-E

Taking into account all three phases of the inverter, there will be 27 possible combinations of switching states. Based on the voltage vectors magnitude, they can be divided into four categories:

- Zero Vectors: contains three switching states that can be shown for three phases as {PPP}, {NNN} and {000} which produce zero voltage at the output;
- Small Vectors: some states that produce E/3 at the output;
- Medium Vectors: whose magnitude is $\sqrt{3}$ E/3;
- Large Vectors: the magnitudes are 2E/3.

Figure 1.23 shows the sectors and regions which are determined by the voltage vectors.

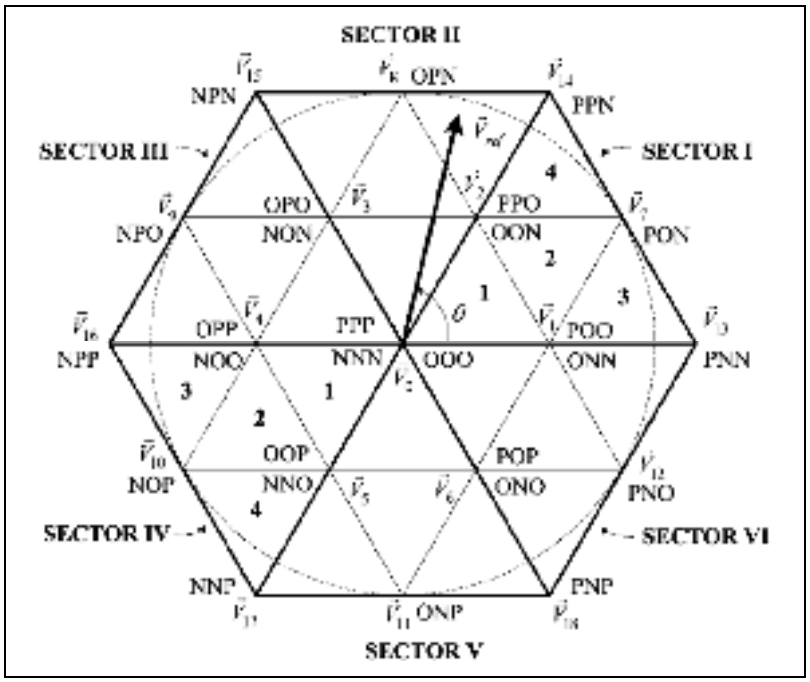

Figure 1.23 Sectors and Regions in SVM for 3L-NPC

As it can be seen in this figure, the reference voltage vector is shown by V_{ref} which is located in a region in each moment. Each sector and region is surrounded by switching vectors. So by calculating the time intervals of each state, the reference voltage can be produced by a combination of switching states.

In this method, the modulation index m_a is defined as follows (Wu, 2006):

$$m_a = \sqrt{3}\frac{V_{ref}}{V_d} \tag{1.5}$$

Where V_d is the output phase voltage (E), and V_{ref} is the reference voltage magnitude. Since in a 3L-NPC the maximum V_{ref} is the radius of the circle shown in Figure 1.23 which is $\sqrt{3}$ $V_d/3$, so the $m_{a\text{-}max}$ equals to 1.

Many developments have been performed on this method (Franquelo et al., 2008) which is flexible to be combined with evolutionary algorithms for optimized switching sequence (Cecati, Ciancetta et Siano, 2010).

1.3.3 DC Voltage Balancing

Using a DC capacitor in multilevel inverter makes the voltage balancing inevitable. Such inverters include NPC, FC and PUC. Using a PI controller is a simple method to control the capacitor voltage while there are many proposed methods to balance the voltage (Barros, Silva et Jesus, 2013; Hornik et Zhong, 2013; Marchesoni et Tenca, 2002; Ounejjar, Al-Haddad et Dessaint, 2012; Sano et Fujita, 2008; Shukla, Ghosh et Joshi, 2008; Xia et al., 2011). For instance, if the levels of a NPC increase, the number of DC capacitor used in DC link raises. Therefore, the voltages of each capacitor and the middle points should be balanced to reach a smooth waveform for output voltage. Most of voltage balancing techniques are based on control methods such as PI, predictive model, fuzzy and etc. as well, using auxiliary circuit to make additional path for capacitors currents has been reported that facilitate the energy exchanging of the capacitors to keep their voltages balanced (Shu et al., 2013).

One interesting feature of multilevel inverters is the fact that they usually have some redundant switching states which generate same voltage level using different current paths. Therefore, they would be the most helpful items in balancing capacitors voltages without requiring external controllers. Such voltage balancing techniques could decouple the voltage/current control in various applications.

All in all, the voltage balancing of the DC capacitors of a multilevel inverter is matter of importance especially in rectifiers or power system interface applications like active filters or STATCOM where a grid connected converter is needed.

1.4 Modeling and Control of Multilevel Inverter

Modeling of a multilevel inverter is the main step to design a proper controller to regulate the voltage or current. The first try on modeling a converter was done on an imbricated multilevel inverter in 1997 (Meynard, Fadel et Aouda, 1997). This model was derived based on the study of the harmonic equivalent circuit.

Some other works have been performed to model the multilevel inverters but there are a few papers totally, therefore it would be a challenging field for modeling various topologies with different methods such as average model, state space or small signal. For example, a CHB used as a STATCOM has been modeled based on small signal method to design a proper control strategy in balancing the DC voltages (Liu et al., 2009). The average model of the PUC inverter has been also derived in (Ounejjar, Al-Haddad et Grégoire, 2011) that helped to implement an appropriate controller of the DC capacitor voltage. A mathematical modelling of multilevel inverter is also introduced in (Ben Smida et Ben Ammar, 2010).

Multilevel inverters use many DC sources to produce higher voltage levels; therefore, their control becomes more complex. Since most of the multilevel inverters have isolated DC sources, they just need switching methods to produce desired voltage levels at the output. However, some topologies have capacitors as DC link which need voltage balancing control methods like PI controller to fix the DC voltage. Moreover, an associated controller is required for each application of the multilevel converters such as drive, charger, UPS, active filter and PV inverter.

1.5 State of The Art (Impact on Industry) and Originality of the research

In addition to the above-mentioned topologies there are some types of multilevel inverters that have been reported but they were not considered and developed in the market. Among the mentioned topologies, the CHB and NPC are still the most popular and accepted ones in industries, however there are some drawbacks associated with them. The other ones have some issues like high switching frequency, complex switching methods, difficult cooling system, large number of semiconductors, or using too many capacitors that needs a lot of isolators and makes the voltage balancing difficult. Note that the medium-voltage and high-power range in industries are 2.3-6.6 kV and 1-50 MW, respectively. And the desired switching frequency in industry is 500-700 Hz. In continue, some advantages and disadvantages of two most widely used types of multilevel inverters (NPC and CHB) are listed as the following (Kouro et al., 2010):

- NPC uses medium and high voltage components (IGCT, IGBT), whereas CHB employs solely low-voltage ones (LV-IGBT). Although CHB uses LV switches, it reaches higher voltage and power levels than NPC;
- NPC is definitely more proper for back-to-back applications than CHB which needs too many switches for this aim;
- NPC has simpler structure system and has flexibility for implementing various switching methods (PWM, SVM and etc.) on it;
- CHB needs a phase-shifting transformer usually to conform a 36-pulse rectifier system which is more expensive but improves input power quality.

Regarding all mentioned advantages and disadvantages of proposed topologies for multilevel inverters, there is still a lot of challenging on improving drawbacks in many aspects like topologies with less switching devices, less DC supplies, easier and faster voltage control, reducing the switching frequency and power losses, diminishing output harmonics, designing suitable output filters. The power electronics converters are widely used in industries and power networks which are so attractive for researchers to improve the performance, and with multilevel topologies the new era of such converters arrived. The growing applications of multilevel inverters show its increasing popularity and acceptable usage in market (industries and power systems).

Besides the provided information, some of the applications of multilevel converters with commercialized topologies are as the following that shows the state of the art of this technology (Leopoldo G. Franquelo, 2012; Wu, 2006):

Figure 1.24 illustrates a 4.16 kV and 1.2 MW drive which is manufactured by ABB and composed of 3L-NPC (right cabinet), cooling system and rectifier (middle cabinet) and controller (left cabinet).

Figure 1.24 GCT-based 3L-NPC drive by ABB (ACS1000)

Figure 1.25 shows a 4.16 kV and 7.5 MW drive designed and built by ASI Robicon by 11L-CHB. The phase shifting transformer (installed in left cabinet) supplies a 30-pulse rectifier.

Figure 1.25 IGBT 11L-CHB drive by ASI Robicon

ABB and Converteam have commercialized 3L-NPC back-to-back for wind power applications as shown in figures 1-26 and 1-27, respectively.

Figure 1.26 3L-NPC for wind power conversion by ABB (PCS-6000-wind)

Figure 1.27 3L-NPC for wind power conversion by Converteam (MV7000)

Figure 1.28 is a MMC for HVDC transmission system commercialized by SIEMENS. The power rating of this inverter is 1000 MW and the output frequency is 50-60 Hz.

Figure 1.28 MMC for HVDC with its Control System and Cooling System

1.6 Conclusion

multilevel converters are widely used for mining applications as regenerative conveyor, medical purposes like MRI gradient coil driver, hydro pump storage, STATCOM and Active Filters, FACTS, distributed generation, ship propulsion, train traction, aerospace and renewable energy (wind and photovoltaic) conversion (Alepuz et al., 2006; Biagini et al., 2011; Daher, Schmid et Antunes, 2008; Dixon et al., 2010; Kouro et al., 2010; Leopoldo G. Franquelo, 2012; Liu et Luo, 2005; Liu et al., 2009; Samuel, Gupta et Chandra, 2011; Xia et al., 2011). Most of the constructed multilevel inverters in industries have been devoted to the high power applications due to their good performance in very low switching frequency and using medium voltage switches. However, the google little box challenge, held in 2014, revealed the promising fact that such class of converters could be used in all range of power electronics converters due to reduced price of semiconductor switches. Since they can produce very low harmonic waveforms inherently, the size of the package would be small because of reduced size of the output passive filters. Having a single-dc-source option and less number of switches would be the most challenging part of this field.

CHAPTER 2

REAL-TIME IMPLEMENTATION OF A SEVEN-LEVEL PACKED U-CELL INVERTER WITH LOW SWITCHING FREQUENCY VOLTAGE REGULATOR

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Abstract

In this chapter a new cascaded nonlinear controller has been designed and implemented on the packed U-Cell (PUC) seven-level inverter. Proposed controller has been designed based on a simplified model of PUC inverter and consists of a voltage controller as outer loop and a current controller as inner loop. The outer loop regulates the PUC inverter capacitor voltage as the second DC bus. The inner loop is in charge of controlling the flowing current which is also used to charge and discharge that capacitor. The main goal of the whole system is to keep the DC capacitor voltage at a certain level results in generating a smooth and quasi-sine-wave 7-level voltage waveform at the output of the inverter with low switching frequency. The proposed controller performance is verified through experimental tests. Practical results prove the good dynamic performance of the controller in fixing the PUC capacitor voltage for various and variable load conditions and yet generating low harmonic 7-level voltage waveform to deliver power to the loads. Operation as an uninterruptible power supply (UPS) or AC loads interface for photovoltaic energy conversion applications is targeted.

2.1 Introduction

Nowadays, power electronics converters are becoming exclusive in supplying high quality electric energy to various electric loads, and lately they are used to deliver renewable energies to the consumers (Abu-Rub, Malinowski et Al-Haddad, 2014; Carrasco et al., 2006; Mobarrez et al., 2015). Yet, power quality and harmonic issues pushed the power industries to design multifunctional, more energy efficient, and high density power electronics

converters with less electromagnetic interferences (Kedjar, Kanaan et Al-Haddad, 2014; Singh, Al-Haddad et Chandra, 1999; Singh, Chandra et Al-Haddad, 2014). Consequently, multilevel inverters have become inevitable topologies that could properly and efficiently answer the above mentioned issues. Conventional topologies known as 2-level inverters are being slowly replaced by such high efficiency devices that produce lower harmonic voltage/current due to multilevel quasi-sinusoidal waveform (Kouro et al., 2010; Sharifzadeh et al., 2015).

Many topologies have been introduced for multilevel inverters that utilized combination of active switches and multiple isolated or dependent DC sources to generate different voltage levels at the output (Biagini et al., 2013; Kangarlu et Babaei, 2013; Lupon, Busquets-Monge et Nicolas-Apruzzese, 2014; Nami et al., 2011; Solomon et al., 2015; Vahedi et al., 2014; Vahedi, Rahmani et Al-Haddad, 2013; Youssef et al., 2015; Zhang et al., 2013).

The main challenging part of multilevel inverters is using less components count especially DC sources and power electronics devices to decrease manufacturing cost as well as reducing the package size (Du et al., 2006; Gupta et Jain, 2012; Gupta et Jain, 2013; Narimani, Wu et Zargari, 2015; Roshankumar et al., 2012; Sebaaly et al., 2014; Sepahvand et al., 2013; Vahedi et al., 2013; Vazquez et al., 2009). Moreover, for the fast growing market of photovoltaic energy conversion applications, using less number of isolated DC sources means not requiring too many MPPT (maximum power point tracking) controllers to control output power and voltage of each separated solar arrays that results in simpler structure of the energy generation system (Li et al., 2012; Mortazavi et al., 2015; Roshankumar et al., 2012; Seyedmahmoudian et al., 2013). Among various reported topologies, PUC inverter has the less number of switches and DC sources by number of output voltage levels, while generating 7 voltage levels (Al-Haddad, Ounejjar et Gregoire, Nov 2011; Chebbah, Vahedi et Al-Haddad, 2015; Ounejjar, Al-Haddad et Grégoire, 2011; Vahedi, Labbé et Al-Haddad, 2015). However, PUC topology requires complex controller to balance the dependent energy storage device voltage leads to reduce the number of isolated DC sources. As well, hysteresis current control has been applied on the PUC inverter to control the capacitor voltage at desired level that has its own related issues such as high and variable switching frequency

which is undesirable for industries (Ounejjar, Al-Haddad et Dessaint, 2012; Vahedi, Al-Haddad et Kanaan, 2014).

In this work a simple model of the PUC inverter is used which aims at defining a set of pulses for associated switches used in that topology. Based on formulated model, a cascaded nonlinear controller has been designed to fix the capacitor voltage (as dependent DC source) at one third of the reference voltage amplitude and consequently, to generate 7-level voltage waveform at the output with low harmonic contents and low switching frequency. This project also deals with real-time implementation and experimental validation of the proposed controller in various conditions including change in load and also in DC source amplitude in stand-alone mode of operation. Generating 7-level voltage waveform using only six active switches, one isolated DC source and one capacitor combined with the proposed low switching frequency voltage controller makes this topology appealing for industries as a good candidate to replace conventional single-phase full-bridge inverter in various applications such as renewable energy conversion system, UPS, switch mode power supplies and etc.

Section 2.2 includes system configuration, modelling and proposed controller design procedure in details. Experimental tests of the designed controller implemented on the 7-level PUC inverter are performed using dSpace real-time controller. Tests results are illustrated and discussed in section 2.3 to verify the good dynamic performance of the proposed controller in tracking the reference signal to response quickly and precisely according to changes happening in the system like adding nonlinear load or DC source voltage variation.

2.2 PUC Inverter Modelling and Controller Design

PUC inverter topology has been first introduced by Al-Haddad et al (Al-Haddad, Ounejjar et Gregoire, Nov 2011). It consists of 6 active switches, one isolated DC supply and one DC capacitor as second DC source (or dependent DC source) which is shown in Figure 2.1.

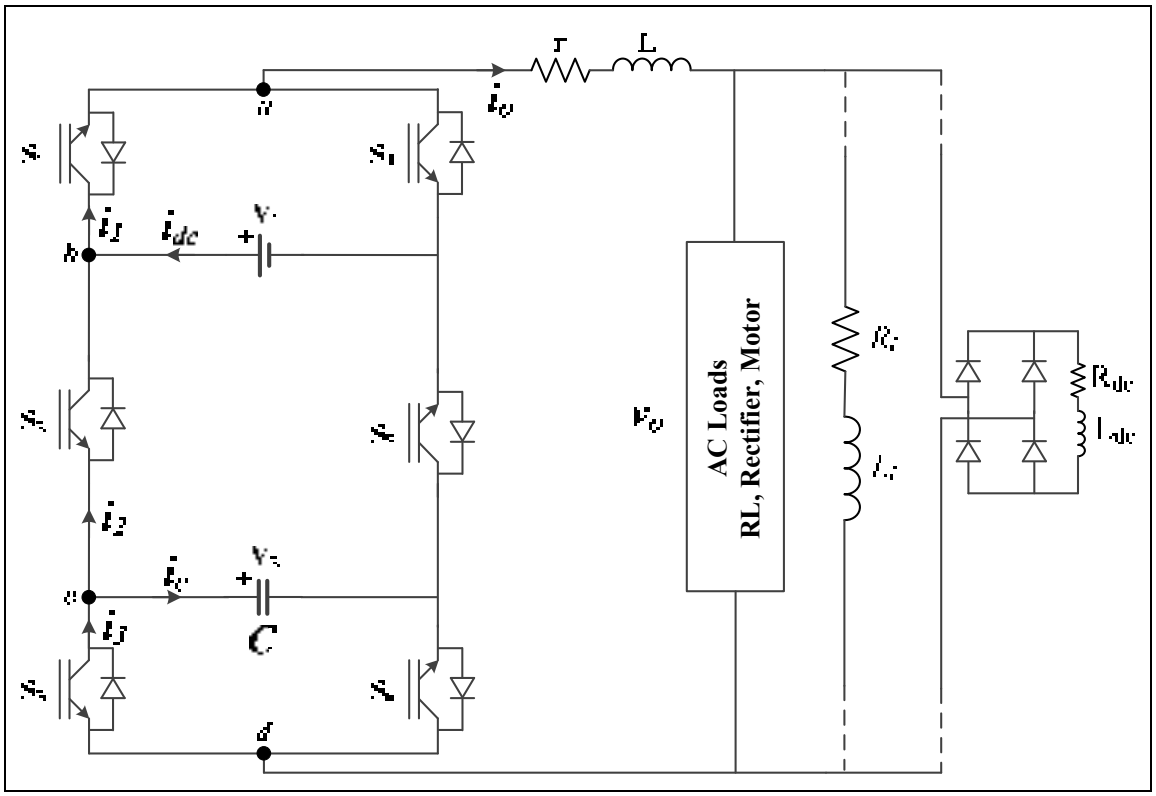

Figure 2.1 Single-phase PUC Inverter

The interesting advantage of PUC is the reduced number of components comparable to other topologies such as Cascaded H-Bridge (CHB) (Malinowski et al., 2010), Neutral Point Clamped (NPC) (Nabae, Takahashi et Akagi, 1981) and Flying Capacitors (FC) (Meynard et Foch, 1992). The less switches, the lower power losses, the less gate drives, the lower system cost. The output voltage levels of the single phase inverter topology of Figure 2.1 are listed in Table 2.1. It should be mentioned that switches S_4, S_5 and S_6 are working in complementary of S_1, S_2 and S_3. So each pair of (S_1, S_4), (S_2, S_5) and (S_3, S_6) cannot conduct simultaneously.

To have all seven levels at the output voltage waveform, the capacitor voltage (V_2) should be 1/3 of the DC bus voltage V_1 ($V_1=3V_2$), so the output voltage levels would be 0, $\pm V_2$, $\pm 2V_2$, $\pm 3V_2$. As it is clear, the PUC inverter cannot produce voltage level more than the DC bus voltage amplitude which is its prominent limitation. The maximum load voltage is equal to the DC bus voltage. In other words, it could be explained that the PUC advantage is to divide the DC bus voltage in multi levels to decrease the load voltage harmonics. This procedure reduces the required filters size at the output of the inverter.

The detailed dynamic model of the PUC inverter has been derived as follows (Kanaan et al., 2009; Ounejjar, Al-Haddad et Grégoire, 2011; Vahedi, Al-Haddad et Kanaan, 2014):

The switching functions of the PUC inverter shown in Figure 2.1 are defined as:

$$S_i = \begin{cases} 0 & if\ S_i\ is\ Off \\ 1 & if\ S_i\ is\ On \end{cases} \quad i = 1,\ 2,\ 3 \tag{2.1}$$

The inverter output voltage can be formulated as:

$$v_{ad} = v_{ab} + v_{bc} + v_{cd} \tag{2.2}$$

Table 2.1 Switching States and Voltage Levels of the PUC Inverter

Switching States	**S1**	**S2**	**S3**	**V_{ad}**
1	1	0	0	V_1
2	1	0	1	V_1-V_2
3	1	1	0	V_2
4	1	1	1	0
5	0	0	0	0
6	0	0	1	-V_2
7	0	1	0	V_2-V_1
8	0	1	1	-V_1

Where the points a, b, c and d are demonstrated in the above figure and each voltage can be computed based on the switching function:

$$\begin{cases} v_{ab} = (S_1 - 1)V_1 \\ v_{bc} = (1 - S_2)(V_1 - V_2) \\ v_{cd} = (1 - S_3)V_2 \end{cases} \tag{2.3}$$

By substituting (2.3) into (2.2),

$$\begin{aligned} v_{ad} &= (S_1 - 1)V_1 + (1 - S_2)(V_1 - V_2) + (1 - S_3)V_2 \\ &= (S_1 - S_2)V_1 + (S_2 - S_3)V_2 \end{aligned} \tag{2.4}$$

Similar to voltages relations, since one of switches in each pair of S_1&S_4, S_2&S_5 and S_3&S_6 are turned ON, the switches currents can be shown as a function of load current and switching function

$$\begin{cases} i_1 = S_1 i_o \\ i_2 = S_2 i_o \\ i_3 = S_3 i_o \end{cases} \tag{2.5}$$

Where,

$$i_3 = i_c + i_2 \tag{2.6}$$

$$i_c = (S_3 - S_2) i_o \tag{2.7}$$

$$\frac{dv_2}{dt} = \frac{(S_3 - S_2) i_o}{C} \tag{2.8}$$

As well, for the voltage and load current the KVL law is written as below:

$$v_o = v_{ad} - r i_o - L \frac{di_o}{dt} \tag{2.9}$$

Substituting Eq. (2.4) into (2.9), the following relation for the output current would be derived:

$$\begin{aligned} \frac{di_o}{dt} &= \frac{\left((S_1 - S_2) V_1 + (S_2 - S_3) V_2 \right) - r i_o}{L} \\ &= (S_1 - S_2) \frac{V_1}{L} + (S_2 - S_3) \frac{V_2}{L} - \frac{r}{L} i_o \end{aligned} \tag{2.10}$$

In (Ounejjar, Al-Haddad et Grégoire, 2011), three different duty cycles have been defined as (u_1, u_2, u_3) for each switches and a nonlinear controller has been designed accordingly; however, using 3 inputs for a single-phase inverter is not consistent with the concept of multilevel inverters in which a group of switches are closed to make a path for the current flowing through the load. Actually, those switches are not working separately to have individual duty cycles. In fact, they are turned on in a group of 3 at each level. Thus, the system input should be only one signal which is modulated by a multicarrier level-shifted

PWM technique to produce required group of pulses that apply the associated voltage level at the output. For instance, one unclear issue raised from the previous work is the question that how does the controller or modulator selects the switching states (including a group of switches to generate a specific voltage level at the output) in a correct order to have respective voltage levels without any interference? To make it clearer, it can be said that when switches work independently, how the controller or modulator ensures that the voltage level (V_1-V_2) is generated exactly between levels V_1 and V_2 and there would not exist any problem like having level V_1 before V_2 that deforms the output multilevel waveform.

To present a solution for the above-mentioned issue, following two facts should be considered (Gomez Jorge, Solsona et Busada, 2014; Hafezi, Akpinar et Balikci, 2014; Mendalek et al., 2003):

- A single-phase converter has only one output voltage or current waveform unlike the 3-phase one that has three output waveforms;

- Every controller designed for power converters can be categorized as voltage-control or current control depends on their output which is a voltage-type or current type signal.

Although single-phase multilevel inverter has more switches than a 2-level topology, it still generates one voltage and or one current waveform at its output. It uses higher number of switches in each conducting path, while they are not working independently. Actually, they work as a group and the group number is determined by the switching state as listed in Table 2.1. The controlling signal is modulated and the modulator output data is the switching state number. Each state consists of a group of switches that should be turned on to produce corresponding voltage level at the output. Such structure ensures correct orders of voltage levels. To conclude, in a multilevel converter, switches act dependently as a group to generate desired voltage levels at the output in a correct order leads to have a smooth quasi-sine multilevel voltage waveform with low harmonic contents.

To comply with those facts, in this chapter a new controller is designed based on a simplified model of the PUC inverter. It does have only one output signal which is modulated by a 6-

carrier level-shifted PWM to generate associated switching pulses for all 6 switches dependently based on the switching states listed in Table 2.1. Therefore, in this work, designed controller would send only one signal to the modulator (PWM) which is consistent with the concept of multilevel inverters switching as well as complies with the fact that single-phase converters controllers should produce one signal as their output which is sent to the modulator for pulse generation process. The 6-carrier level-shifted PWM scheme is shown in Figure 2.2 where the reference wave is modulated by different carriers to produce the associated switching pulses for the 7-level PUC inverter.

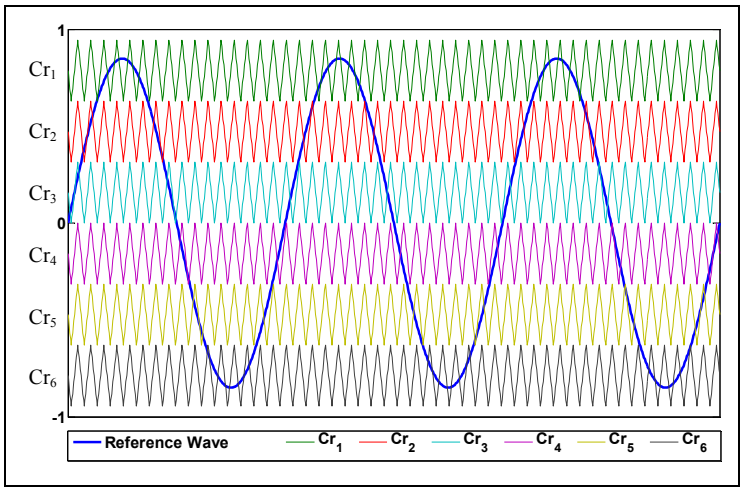

Figure 2.2 Multicarrier PWM for 7-level PUC inverter

As mentioned earlier, to solve the problem regarding three individual inputs for a single-phase inverter, a simple model of the PUC inverter has been used to design a new controller in which only equations (2.8) and (2.9) are considered as voltage and current control sections respectively.

Based on Eq. (2.8) capacitor voltage is related to the load current therefore an equivalent signal u_v can be defined as:

$$u_v = C \frac{dv_2}{dt} = d_v i_o \qquad (2.11)$$

Where, d_v depends on the switching functions of S_2 and S_3. To regulate the DC capacitor voltage (V_2), error signal of $\tilde{v}_2 = v_2^* - v_2$ should be minimized through the PI controller. Therefore:

$$u_v = k_{pv}\tilde{v}_2 + k_{iv}\int \tilde{v}_2 dt \tag{2.12}$$

Transfer function of the PI voltage controller is:

$$G_v(s) = \frac{U_v(s)}{\tilde{V}_2(s)} = k_{pv} + \frac{k_{iv}}{s} \tag{2.13}$$

Regarding Eq. (2.11), output of the voltage controller is u_v which is current-type signal. The capacitor voltage should be regulated by proper charging and discharging process which is done through the flowing current. As a cascaded controller concept, voltage controller can be used as outer loop and its output should go into the inner loop as a reference signal i_o^*. Controlled current goes through the capacitor and regulates its DC voltage at reference value. The inner loop is a current controller that is designed based on Eq. (2.9) and its dynamic should be fast enough to ensure good dynamic performance of the cascaded controller. Assuming that the outer loop regulates the capacitor voltage at the desired level and ensures $V_2 = 1/3\ V_1$, then:

$$\begin{aligned} v_{ad} &= (S_1 - S_2)V_1 + (S_2 - S_3)V_2 \\ &= (S_1 - S_2)V_1 + (S_2 - S_3)\ \frac{V_1}{3} \\ &= (S_1 - \frac{2}{3}\ S_2 - \frac{1}{3}\ S_3)V_1 \end{aligned} \tag{2.14}$$

Eq. (2.14) can be turned into Eq. (2.15) considering d_i as a signal depending on switching functions of S_1, S_2 and S_3.

$$v_{ad} = d_i v_1 \tag{2.15}$$

Substituting (2.15) into (2.9),

$$L\ \frac{di_o}{dt} + ri_o\ =\ d_i v_1\ -\ v_o \tag{2.16}$$

Same as voltage controller design procedure shown above, an equivalent signal u_i can be defined as:

$$u_i\ =\ L\ \frac{di_o}{dt} + ri_o\ =\ d_i v_1\ -\ v_o \tag{2.17}$$

The current can be regulated through a PI compensator in which the input is the error signal $\tilde{i}_o\ =\ i_o^*\ -\ i_o$ and the output is u_i:

$$u_i\ =\ k_{pc}\tilde{i}_o\ +\ k_{ic}\int\ \tilde{i}_o dt \tag{2.18}$$

Where the transfer function of the PI current controller is:

$$G_i(s)\ =\ \frac{U_i(s)}{\tilde{I}_o(s)}\ =\ k_{pi}\ +\ \frac{k_{ii}}{s} \tag{2.19}$$

Eventually, to derive the single input signal which should be modulated by level-shifted PWM, right side of the Eq. (2.17) is used as the following:

$$d_i\ =\ \frac{u_i\ +\ v_o}{v_1} \tag{2.20}$$

It should be noted for the inner loop (current control) that the PI controller would have performance where the input signal frequency is low (e.g. outer loop as DC voltage regulator); while it shows some steady-state error when the input is a time-varying signal, like a sinusoidal current, leads to tracking error in the line current. To ensure the possible minimum error on the output current, the integral gain of the $G_i(s)$ should be small enough which makes the inner loop faster than outer loop and results would be acceptable consequently. To ensure the good dynamic performance of the designed controller, inner loop dynamic should be at least five times faster than the outer loop controller. Therefore, the proportional gain of the inner loop PI should be higher than the outer loop one. Due to same reason, the inner loop PI integral gain should be smaller than the outer loop one. Gains are

listed in Table 2.2 which comply with the above-mentioned points. The controller diagram is shown in Figure 2.3 as well.

Table 2.2 Gains Values Used in Designed Controller

k_{pv}	3
k_{iv}	10
k_{pi}	30
k_{ii}	0.1

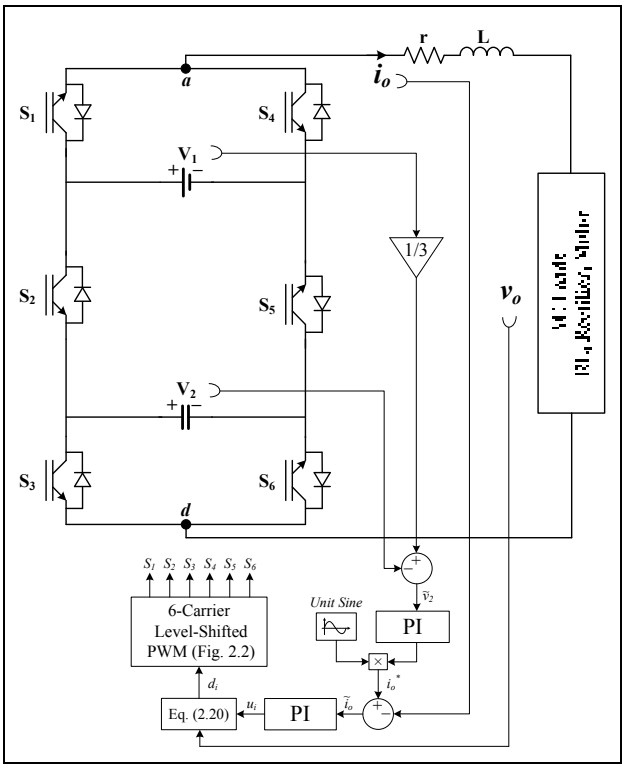

Figure 2.3 Block diagram of proposed controller applied on 7-level PUC inverter

As depicted in Figure 2.3, output of Eq. (2.13) which is the PI voltage controller is a DC signal so it should be multiplied by a unit sine-wave to generate a sinusoidal current waveform as a reference signal for inner loop. As explained earlier, the current is regulated through the PI with transfer function of (2.19). Afterwards, Eq. (2.2) is used to generate the final input signal to the system from the u_i. It is obvious that the output of the controller (that can be called system input) is a single signal d_i which is the duty cycle modulated by the 6-carrier levels shifter PWM to produce the required pulses.

The 7-level PWM shown in Figure 3.2 includes six carriers to modulate the input signal. Six carriers are shifted vertically to cover d_i. Unlike the switching pattern described in the literature in which switching signals were produced for each switch separately; in this work a group of switches would be fired by produced pulses from modulated signal. For instance, each carrier is responsible to generate pulses for group of three switches in three cells. For example if the reference wave is greater than Cr_1, then the higher voltage level which is V_1 would be generated at the output. Looking at Table 2.1, it is clear that switches S_1, S_5 and S_6 should be turned ON. In the same manner, if reference wave is between Cr_1 and Cr_2 then the second voltage level (V_1-V_2) would be produced at the output terminal of the PUC inverter which requires switches S_1, S_5 and S_3 to be closed. All other switching states would be used to generate suitable switching pulses, similarly. Using multicarrier PWM technique ensures the low and fixed switching frequency of the inverter switches against the hysteresis switching technique used in the previous works (Ounejjar, Al-Haddad et Grégoire, 2011). Moreover, it would prevent the undesirable jumping between switching sequences which was occurred in other reported techniques. This phenomenon results in injecting unwanted harmonics into the voltage and current waveform as well as producing more power losses due to higher dv/dt and higher switching frequency.

2.3 Experimental Results

A laboratory prototype for PUC inverter has been built using six 1.2KV 40A SiC MOSFETs type SCT2080KE active switches. dSpace 1103 is used for real time implementation of the designed controller which produces and sends associated pulses to the PUC inverter switches. Due to light calculations of the controller, low sampling time of 20us in implementation on the real-time controller is achieved which increases the controller accuracy significantly. System parameters used in practical tests are listed in Table 2.3.

In this part, the PUC inverter has been tested as stand-alone supplier which is connected to static RL load. This mode is suitable for PV system application in microgrids with small size filters, low THD voltage waveform and low power losses due to low and fixed switching frequency. Figure 2.4 shows the test results in which capacitor voltage V_2 (50 V) is exactly regulated at one third of the V_1 (150 V) by the proposed controller. Moreover, the capacitor

voltage ripple is measured around 1.9V which is acceptably less than 5% of its main voltage. 7-Level voltage waveform is formed at the output of the PUC inverter due to proper voltage regulation of the designed controller. It should be noted that voltage waveform before the L has been depicted in all figures which is demonstrated by V_{ad} in Figure 2.1. THD of the 7-level V_{ad} is measured at 12% without using any voltage filter. With such THD% value, it could be ensured that although PUC topology has two more switches than conventional full-bridge inverter, it requires smaller filters that reduce manufacturing costs and increases the life time of the product significantly.

Table 2.3 System Parameters Used in Practical Tests

Load Voltage Frequency	60 Hz
Inductive Filter (L_f)	2.5 mH
DC Source Voltage (V_1)	150 V
Regulated Capacitor Voltage (V_2)	50 V
Switching Frequency	2 kHz
RL Load (R_l and L_l)	40 Ω, 20 mH
Rectifier as Nonlinear Load (DC Side R_{dc} and L_{dc})	40 Ω, 100 mH
DC Capacitor	2500 µF

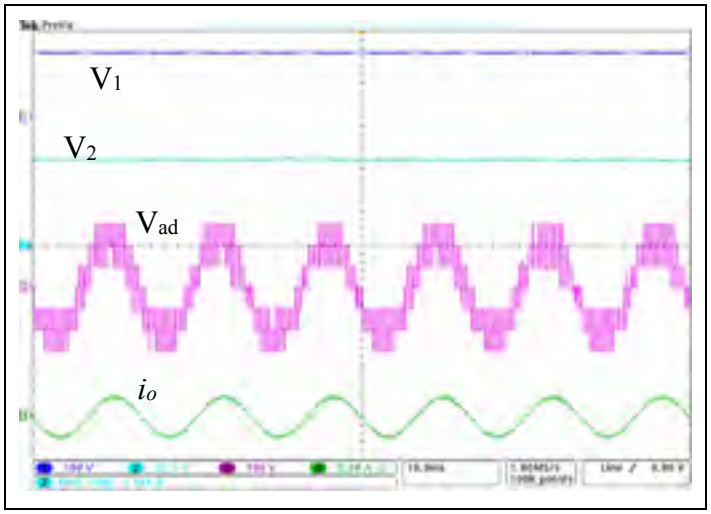

Figure 2.4 PUC inverter voltage and current waveforms in steady state condition

Moreover, the number of commutations is clearly low in this figure that validates the low switching frequency operation of the inverter running by the proposed controller. The lower switching frequency, the lower power losses and the higher efficiency.

In second test, the DC source voltage amplitude has been changed with slow rate as practical situation to validate fast response of the implemented controller in tracking the reference signal accurately. Figure 2.5 shows the test result in which V_2 is tracking the reference value which is $V_1/3$ during change in V_1. V1 has been increased for 66% from 120V to 200V and V_2 smoothly follows the one third value from 40V to 66V highlighting good dynamic performance of the proposed controller. Seven-level voltage waveform of the inverter (V_{ad}) is increasing without losing symmetry on the voltage levels during the DC source voltage variation. Such situation can happen in startup of a motor with V/f control.

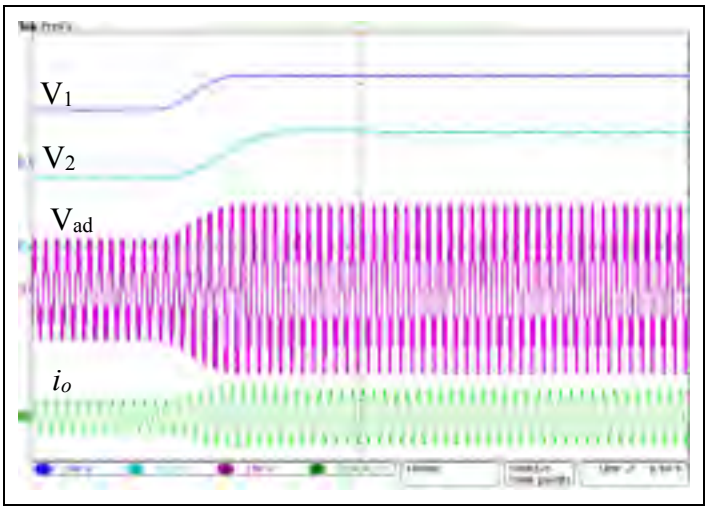

Figure 2.5 Voltage regulation during a fast 66% increase in DC source amplitude

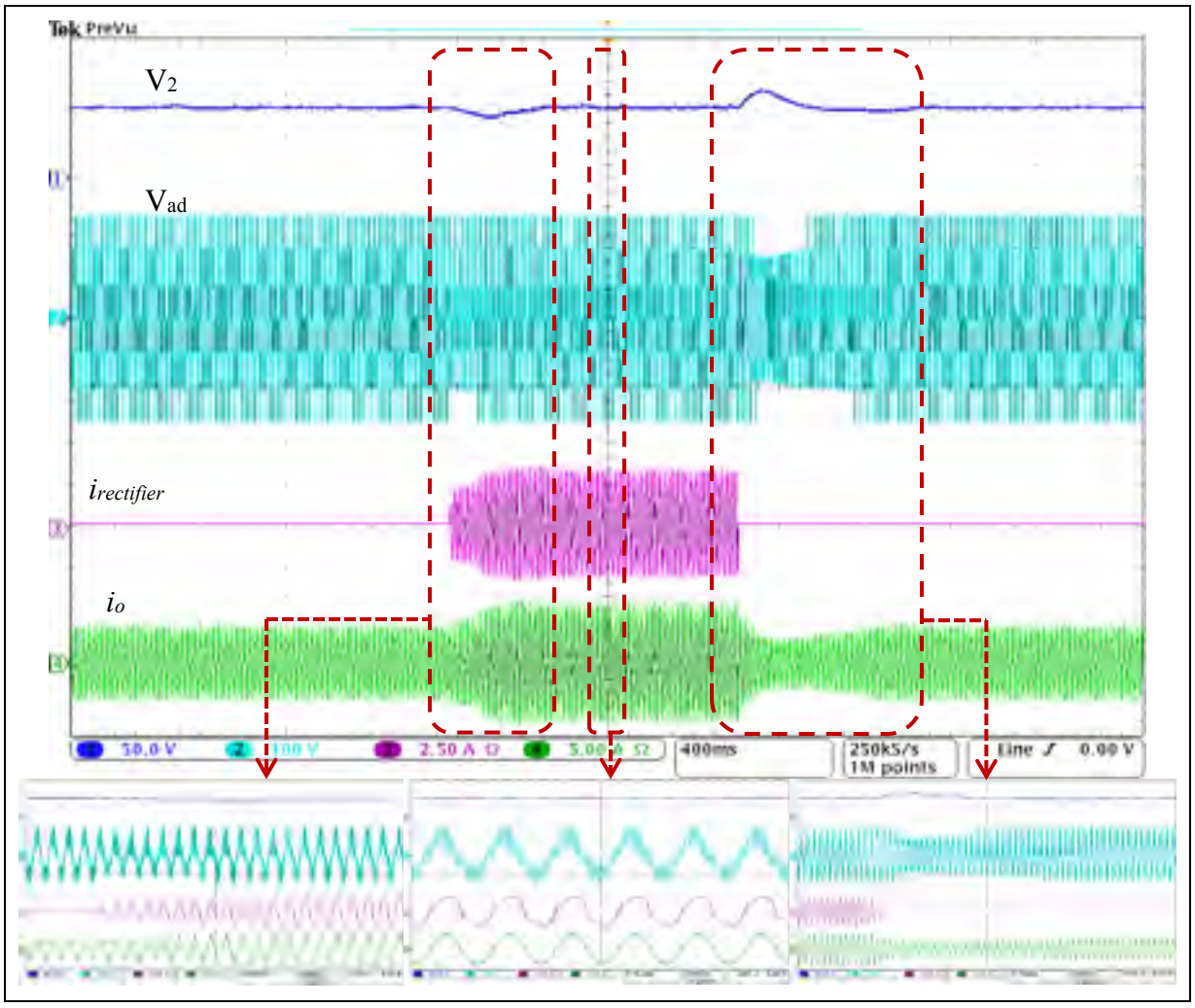

Figure 2.6 Adding a nonlinear load (rectifier) to the PUC inverter while supplying an RL load

To show the good dynamic performance of the designed controller in load change conditions as well as appropriate action in harmonic environment, a nonlinear load consists of a single-phase rectifier with R_{dc} and L_{dc} on the DC side is connected to the PUC inverter while it was supplying an RL load as shown in Figure 2.1. Results have been illustrated in Figure 2.6 in which a current probe measures the rectifier AC side current demonstrating its harmonic contents clearly.

Considering zoomed figures, it is obvious that when a load is added or removed from the output of the PUC inverter, the amount of delivered power is changed and makes unbalances in the capacitor voltage. Consequently, the applied controller adjusts the V_2 at the desired

level and prevents any unbalancing in the capacitor and output voltages. Proposed controller fixes the capacitor voltage and produces seven-level voltage waveform at the output within an acceptable time limit.

Results validate acceptable performance of the proposed controller not only in fixing the PUC inverter capacitor voltage at desired level, but also in generating equal voltage levels in 7-level voltage waveform. Low switching frequency, fast response and good dynamic performance of the experimentally tested PUC inverter proves the excellence of proposed controller against other reported techniques. Moreover, it should be repeatedly mentioned that the system input is only one signal di which is regulated by the PWM technique and ensures the correct order of switching states to be produced and sent to associated switches. Using PWM technique in generating switching pulses leads to a fix switching frequency and also results proved that the PUC inverter can work in low switching frequency as mentioned in the system parameters.

2.4 Conclusion

In this chapter a new cascaded nonlinear controller has been designed for 7-level PUC inverter based on the simple model derived by multilevel inverter topology concept. Experimental results showed appropriate dynamic performance of the proposed controller in stand-alone mode as UPS, renewable energy conversion system or motor drive applications. Different changes in the load and DC bus voltage have been made intentionally during the tests to challenge the controller reaction in tracking the voltage and current references. Proposed controller demonstrated satisfying performance in fixing the capacitor voltage of the PUC inverter, generating seven-level voltage with low harmonic content at the output of the PUC inverter and ensures low switching frequency operation of those switches. By applying the designed controller on the 7-level PUC inverter it can be promised to have a multilevel converter with maximum voltage levels while using less active switches and DC sources aims at manufacturing a low-cost converter with high efficiency, low switching frequency, low power losses and also low harmonic contents without using any additional bulky filters.

CHAPTER 3

SENSOR-LESS FIVE-LEVEL PACKED U-CELL (PUC5) INVERTER OPERATING IN STAND-ALONE AND GRID-CONNECTED MODES

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Abstract

In this chapter a new mode of operation has been introduced for Packed U-Cell (PUC) inverter. A sensor-less voltage control based on redundant switching states is designed for the PUC5 inverter which is integrated into switching process. The sensor-less voltage control is in charge of fixing the DC capacitor voltage at half of the DC source value results in generating symmetric five-level voltage waveform at the output with low harmonic distortion. The sensor-less voltage regulator reduces the complexity of the control system which makes the proposed converter appealing for industrial applications. An external current controller has been applied for grid-connected application of the introduced sensor-less PUC5 to inject active and reactive power from inverter to the grid with arbitrary power factor while the PUC auxiliary DC bus is regulated only by sensor-less controller combined with new switching pattern. Experimental results obtained in stand-alone and grid-connected operating modes of proposed PUC5 inverter prove the fast response and good dynamic performance of the designed sensor-less voltage control in balancing the DC capacitor voltage at desired level.

3.1 Introduction

High harmonic content of output voltage waveform in conventional two-level inverters is a matter of controversy. Nowadays, using more switches and DC sources in power electronics converters is a competitive field of research leads to generate more voltage levels at the output and consequently lower harmonic content, smaller size of the output filters, and lower

manufacturing cost as well (Abu-Rub, Malinowski et Al-Haddad, 2014; Franquelo et al., 2008). Multilevel inverters are designed based on configuration of more switches and DC supplies to achieve the goal of generating various voltage levels at the output. Such inverters generate low harmonic waveforms; therefore they are most suitable for energy conversion applications to deliver efficient power to the loads from renewable energy sources like photovoltaic systems (Biagini et al., 2013; Cecati, Ciancetta et Siano, 2010; Mortazavi et al., 2015; Seyedmahmoudian et al., 2013).

The main problem of multilevel converters is having more independent DC supplies than the conventional two-level ones that make the use of bulky transformers and diode rectifiers inevitable. Besides, complicated voltage control strategies must be applied in case of using DC capacitors instead of DC sources (Gupta et Jain, 2012; Kangarlu et Babaei, 2013; Mobarrez et al., 2014).

Researchers have been introducing lots of multilevel inverter topologies also for low and medium power applications like connecting photovoltaic panels to the local grid as household consumption or street lightings to convert the DC voltage of the renewable energy resource to the proper AC waveform useable at load and grid sides. In such applications a single-phase transformer-less inverter with minimum number of DC sources is preferable (Daher, Schmid et Antunes, 2008; Hinago et Koizumi, 2010; Li et al., 2012; Roshankumar et al., 2012; Sharifzadeh et al., 2015; Vahedi, Al-Haddad et Kanaan, 2014; Vahedi et al., 2014; Vahedi et al., 2013; Vahedi, Rahmani et Al-Haddad, 2013; Zhang et al., 2013). Packed U-Cell (PUC) inverter has been first introduced by Al-Haddad et al to generate 7-level voltage while using only 6 active switches, one isolated DC sources and one capacitor as second source which its voltage should be controlled to fix at 1/3 of first DC source (Al-Haddad, Ounejjar et Gregoire, Nov 2011). Although the mentioned topology has less number of components among other 7-level inverters, it has some major drawbacks including high switching frequency, asymmetric output voltage cycles and levels, requiring fast response and complicated controller with lot of feedback sensors, using large capacitor to regulate the voltage in variable situations and etc (Ounejjar, Al-Haddad et Grégoire, 2011; Vahedi, Al-Haddad et Kanaan, 2014; Vahedi et Al-Haddad, 2015a).

In this work, the PUC topology is investigated to have simple controller and better performance, which led to proposing a new self-voltage-balancing sensor-less 5-level PUC inverter called sensor-less PUC5. The PUC5 inverter capacitor voltage would be fixed at half of the DC source amplitude using a self-voltage-balancing process which is integrated into the multicarrier pulse width modulation (PWM). Therefore there would be no necessity of using voltage or current sensors due to not using complicated controllers. Since the capacitor voltage is kept constant at desired level, the output voltage waveform would have symmetrical five levels with less harmonic distortion. The PUC5 topology and proposed technique is the subject of a US provisional patent application No.: 62/073387 which is explained and fully investigated in section 3.2. In section 3.3, grid-connected controller is described. Section 3.4 includes some comparative study between multilevel inverters based on number of components. The experimental results including stand-alone and grid-connected modes are shown and discussed in section 3.5 to demonstrate the fast and good dynamic performance of proposed sensor-less self-voltage-balancing technique applied on PUC5 inverter in regulating the capacitor voltage at desired level and producing five-level output voltage in face of varying conditions.

3.2 Proposed PUC5 Inverter Topology and Self-Voltage-Balancing Switching Technique

Although the 7-level output waveform of the PUC is interesting due to generating maximum voltage levels while using minimum number of components, requiring complex controller and many sensors to provide state feedbacks for controller calculation as well as asymmetric voltage levels produced make it difficult to get wide spread acceptance by the industries and market.

3.2.1 PUC5 Inverter Configuration and Sensor-Less Voltage Balancing Investigation

The single-phase PUC inverter topology has been shown in Figure 3.1. The complete associate switching states are listed in Table 3.1 (Al-Haddad, Ounejjar et Gregoire, Nov 2011).

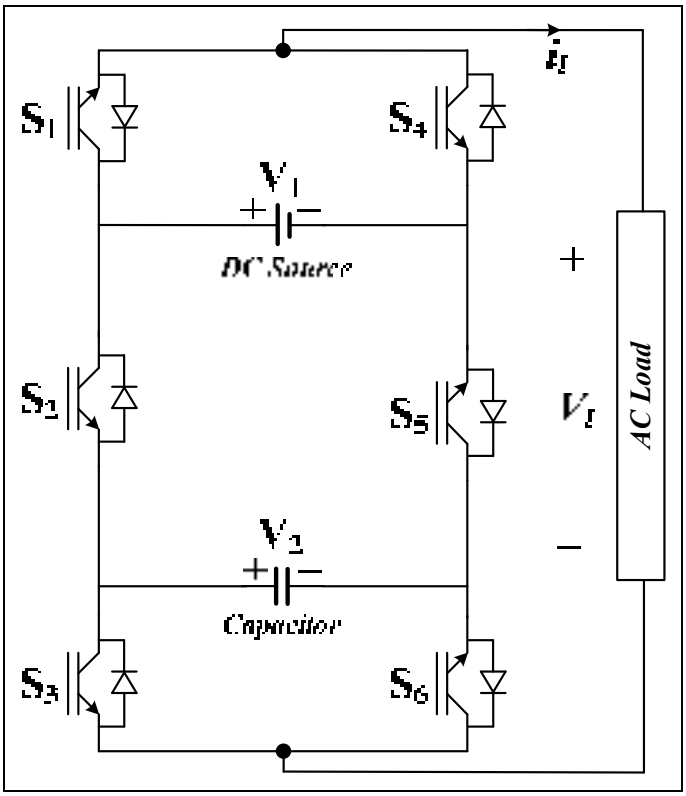

Figure 3.1 PUC5 Inverter Topology

Table 3.1 All possible switching states of PUC Inverter

States	S_1	S_2	S_3	Output Voltage	V_l
1	1	0	0	V_1	+2E
2	1	0	1	V_1-V_2	+E
3	1	1	0	V_2	+E
4	1	1	1	0	0
5	0	0	0	0	0
6	0	0	1	-V_2	-E
7	0	1	0	V_2-V_1	-E
8	0	1	1	-V_1	-2E

It is clear that 8 existing switching states can provide different paths for current to flow through the system including DC sources and load. Taking into account that the output voltage levels numbers depend on DC sources amplitudes, using unequal DC sources result in having different level numbers in output voltage waveform. First, to have maximum number of levels at the output, V_2 amplitude must be 1/3 of V_1. Assuming $V_1=3V_2=3E$, seven levels would be generated as 0, ±E, ±2E, ±3E. 7-level PUC disadvantages were mentioned

above which is mostly due to complex voltage balancing procedure, but considering Table 3.1 more precisely, it is observed that the PUC inverter has the ability to operate as 5-level inverter by assuming $V_1=2V_2=2E$, therefore the output 5-level voltage waveform includes the levels 0, ±E, ±2E. In this case, the capacitor voltage (V_2) is kept constant at half of the DC source (V_1) amplitude. Noticing Table 3.1, six switching states are available to produce three levels including –E, 0 and +E that means there are some redundant switching states which may help to find different paths for flowing current through the load. The redundant switching states can deal with charging and discharging the capacitor in order to balance the voltage at the half of the DC source voltage.

To use the redundant switching states in proper design of the required PWM technique for PUC5 inverter, all switching states have been studied noticing the effects on capacitor voltage. Figure 3.2 shows the paths made by switching states listed in Table 3.1.

Based on Figure 3.2, it is clear that in states where the DC source and capacitor are connected in series with the load, the capacitor is charged (states 2 & 7). On the other hand, on some paths that the capacitor feeds the load alone, it is discharging (states 3 & 6). Eventually, for rest of the states, the capacitor voltage is remained unchanged because it is neither connected to DC source nor to the load. Table 3.2 indicates the charging and discharging states of the capacitor.

One of the main issues with 7-level PUC inverter in balancing the capacitor voltage is high switching frequency, complexity of the controller and using too many sensors as states variables feedbacks (Ounejjar, Al-Haddad et Grégoire, 2011; Ounejjar, Al-Haddad et Dessaint, 2012). Since the investigated PUC5 inverter has redundant switching states, the capacitor voltage balancing feature can be integrated into the modulation technique.

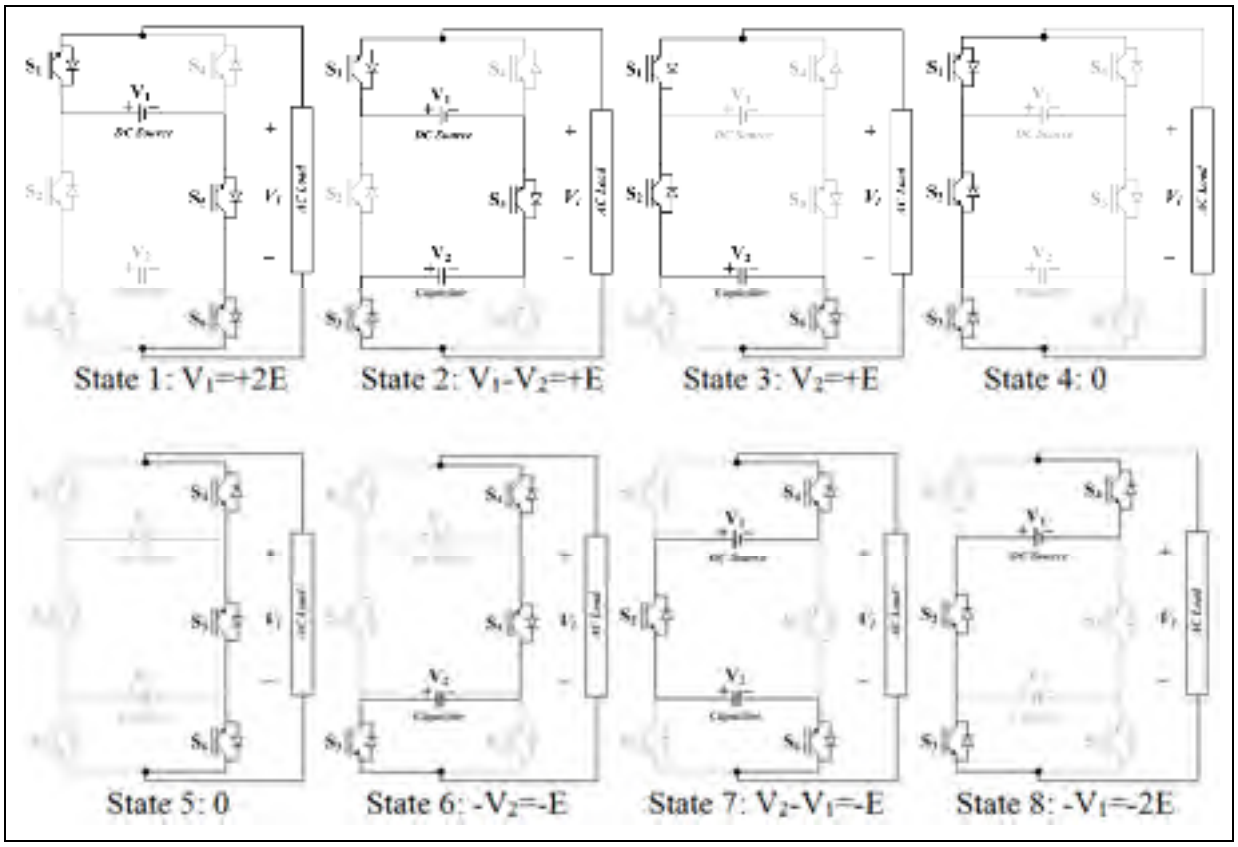

Figure 3.2 Switching states and conducting paths of PUC5 inverter

Table 3.2 PUC5 Capacitor voltage states

State	Capacitor Voltage
1	No Effect
2	Charging
3	Discharging
4	No Effect
5	No Effect
6	Discharging
7	Charging
8	No Effect

Therefore the control strategy contains only the PWM switching technique without the necessity of using additional controller (linear or nonlinear or …) which necessitates complex function and more computation effort of the real time controller therefore makes it not simple to implement. It is expected that the voltage controller integrated into switching

technique would have good dynamic performance and fast response due to simplicity and not using any feedback sensors.

The key point in Table 3.2 is the fact that capacitor can be charged or discharged in each positive or negative half cycle. Therefore, in order to keep the capacitor voltage fixed, in designing of proposed switching technique, it has been decided to charge the capacitor in the positive half-cycle and then to discharge it in negative half cycle. Due to the output voltage waveform frequency which is 60 Hz and the selected switching frequency, the capacitor can be only charged to half of the DC source amplitude.

Regarding the charging states (2 and 7), it is clear that the capacitor is charged when it is connected in series with DC source and load, as well as the load voltage should be ±E. Thus the following equations can be written:

$$V_1 = V_2 + V_l \Rightarrow \begin{cases} 2E = V_2 + E \\ -2E = V_2 - E \end{cases} \Rightarrow |V_2| = E \qquad (3.1)$$

While the source voltage is fixed at 2E, the capacitor must be charged up to E to produce the proper output load voltage. Such condition as well as the charging (discharging) time forces the capacitor to charge up to half of source voltage value.

In order to have equivalent times of charging and discharging in one period, switching state 2 is chosen to connect the DC source to the capacitor and charge it up, while on the other hand, the capacitor will be discharged in negative half cycle in order to prevent the overcharged through the switching state 6 which connects the capacitor directly to the load. The mentioned procedure is independent of the switching frequency and output voltage frequency. The capacitor charging and discharging time only depends on load value. It has direct effect on capacitor size which should be considered in calculating the system parameters for specific application design. Larger loads need smaller capacitor in DC link and vice versa.

This self-voltage-balancing procedure can be mathematically proved based on capacitor energy relations. Figure 3.3 shows one cycle of the typical output voltage and current

waveforms of PUC5 inverter. V_E is a part of output voltage generated by the capacitor (+E or –E) whether connected to the load alone as discharging path or in series with DC source as charging process.

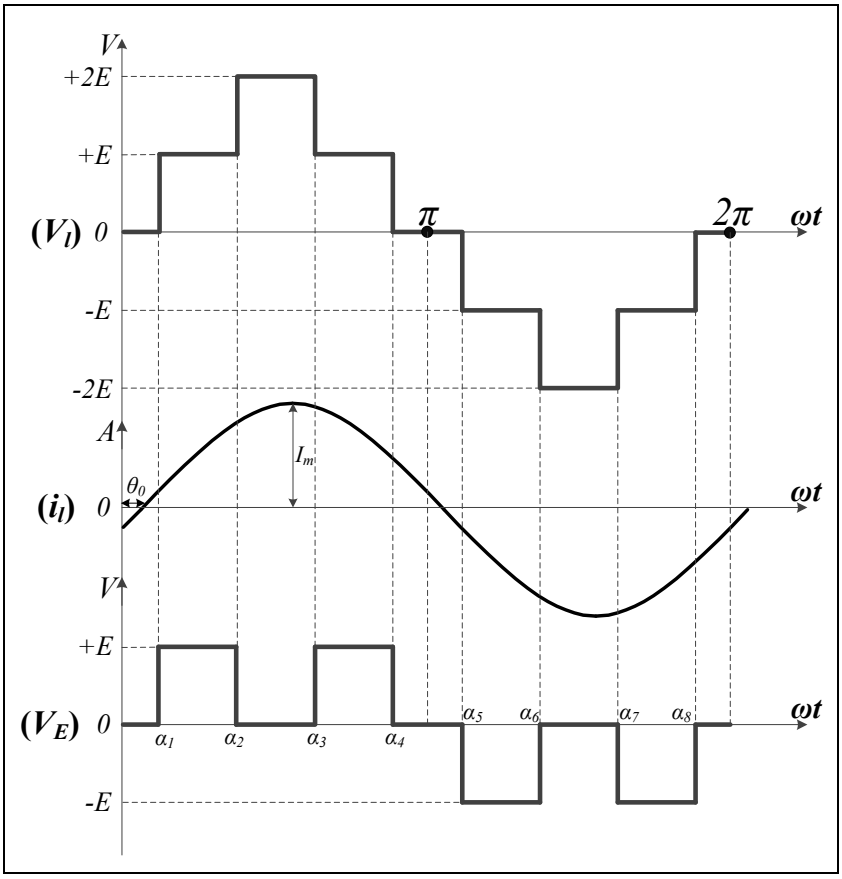

Figure 3.3 Typical output voltage and current waveform of a five-level inverter

The output voltage and current can be assumed as a following sine functions:

$$v_l(t) = V_m \, Sin(\omega t) \tag{3.1}$$

$$i_l(t) = I_m \, Sin(\omega t - \theta_0) \tag{3.2}$$

Where, V_m and I_m are the maximum value of output voltage and current waveforms, respectively. As well, θ_0 is the phase difference between output voltage and current. Based on energy absorbing or delivering to the load by dc capacitor, the following equations can be written:

$$
\begin{aligned}
& I = \frac{dq}{dt} \\
& \rightarrow dU = V\, dq = V\, I\, dt \\
& \rightarrow U = \int V\, I\, dt
\end{aligned}
\tag{3.4}
$$

Where, I, q, and U are current, electric charge, voltage and energy of the capacitor, respectively. Considering Figure 3.3 and substituting equation (3.3) into (3.4), the capacitor energy delivered or absorbed in PUC5 inverter can be derived in periods of positive and negative half-cycle of the output voltage. It should be also mentioned that the capacitor voltage is a fixed value at E.

$$
\begin{aligned}
U^{+} &= \int_{0}^{\pi} V_E I_m Sin(\omega t - \theta_0)\, d(\omega t) \\
&= I_m \int_{0}^{\pi} V_E Sin(\omega t - \theta_0)\, d(\omega t) \\
&= I_m \left[\begin{array}{l}
\int_{0}^{\alpha_1} 0 \times Sin(\omega t - \theta_0)\, d(\omega t) \\
+\int_{\alpha_1}^{\alpha_2} E \times Sin(\omega t - \theta_0)\, d(\omega t) \\
+\int_{\alpha_2}^{\alpha_3} 0 \times Sin(\omega t - \theta_0)\, d(\omega t) \\
+\int_{\alpha_3}^{\alpha_4} E \times Sin(\omega t - \theta_0)\, d(\omega t) \\
+\int_{\alpha_4}^{\pi} 0 \times Sin(\omega t - \theta_0)\, d(\omega t)
\end{array} \right] \\
&= -EI_m Cos(\omega t - \theta_0) \Big|_{\alpha_1}^{\alpha_2} - EI_m Cos(\omega t - \theta_0) \Big|_{\alpha_3}^{\alpha_4} \\
&= EI_m \left[Cos(\alpha_1 - \theta_0) - Cos(\alpha_2 - \theta_0) + Cos(\alpha_3 - \theta_0) - Cos(\alpha_4 - \theta_0) \right]
\end{aligned}
\tag{3.5}
$$

The same effort is done for calculating capacitor energy in negative half-cycle and the following equation would be obtained for U^{-}:

$$
\begin{aligned}
U^{-} &= \int_{\pi}^{2\pi} V_E I_m Sin(\omega t - \theta_0)\, d(\omega t) \\
&= I_m \int_{\pi}^{2\pi} V_E Sin(\omega t - \theta_0)\, d(\omega t) \\
&= EI_m Cos(\omega t - \theta_0) \Big|_{\alpha_5}^{\alpha_6} + EI_m Cos(\omega t - \theta_0) \Big|_{\alpha_7}^{\alpha_8} \\
&= EI_m \left[Cos(\alpha_6 - \theta_0) - Cos(\alpha_5 - \theta_0) + Cos(\alpha_8 - \theta_0) - Cos(\alpha_8 - \theta_0) \right]
\end{aligned}
\tag{3.6}
$$

Noticing the fact that two half cycles of the output voltage are symmetric, thus it can be assumed that:

$$
\begin{cases}
\alpha_5 = \pi + \alpha_1 \\
\alpha_6 = \pi + \alpha_2 \\
\alpha_7 = \pi + \alpha_3 \\
\alpha_8 = \pi + \alpha_4
\end{cases}
\tag{3.7}
$$

Then the energy amount in half cycles would be equal in value but opposite in sign:

$$
U^{-} = -U^{+} \tag{3.8}
$$

This means that the capacitor energy in full cycle would be balanced and maintained constant which leads to keep the capacitor voltage at the desired level in all conditions since the reference waveform is periodical.

Higher switching frequency implies more switching pulses make the capacitor charging/discharging time smaller; consequently better voltage balancing performance. Since the sensor-less voltage balancing concept is based on the symmetry of the charging and discharging times it is therefore independent of the grid voltage distortion or unbalanced voltage conditions where the full cycle is reformed (e.g. the 3rd or 5th harmonic are present). In such conditions, both positive and negative half cycles are still identical and symmetrical results in self-voltage-balancing of the capacitor eventually.

3.2.2 Sensor-Less Voltage Controller Integrated Into Switching Technique

Five-level PWM scheme including four carriers' waves and the sinusoidal reference waveform is depicted in Figure 3.4. The four carriers' waveforms (Cr_1, Cr_2, Cr_3, and Cr_4) are

shifted vertically to modulate the reference waveform (V_{ref}) completely (Lupon, Busquets-Monge et Nicolas-Apruzzese, 2014; Vahedi et al., 2014). The firing pulses associated with switching states 1, 2, 4, 5, 6 and 8 (listed in Table 3.1) are generated based on comparing V_{ref} with those carrier waves. Moreover, redundant switching states of 4 and 5 are used to reduce the switching frequency. If V_{ref} is positive, then state 4 will be used to produce the zero level at the output. On the other hand, if V_{ref} is negative, the output zero level voltage will be generated by state 5. The described algorithm is shown in Figure 3.5 which can produce the five-level voltage waveform at the output with minimum switching frequency while fixing the capacitor voltage at the desired level without any feedback sensor.

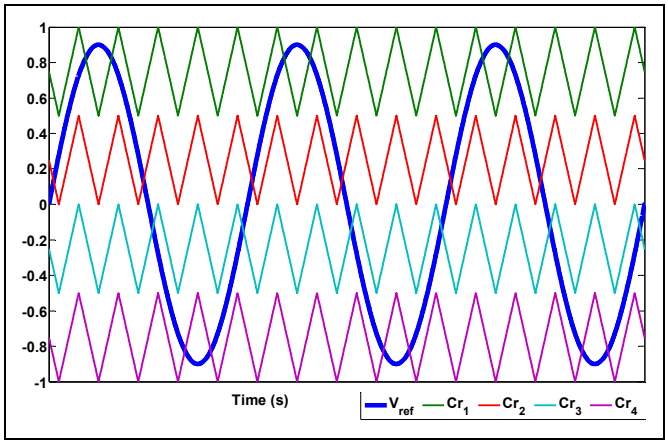

Figure 3.4 Five-level PWM scheme using four vertically shifted carrier waveforms

As mentioned before, applying the proposed algorithm on PUC5 inverter generates 5-level voltage waveform at the output without using any voltage sensors and complex calculations in controller. The capacitor voltage would be constant even at start-up and also in load change conditions. The light algorithm makes the system much faster than previously implemented controller on PUC inverter as published in the literature. The proposed technique does not depend on system model (e.g. average modelling), feedback sensors, modulation index, switching frequency and grid frequency. It can operate the system starting from zero voltage up to arbitrary amplitude and also in DC source voltage variation situations.

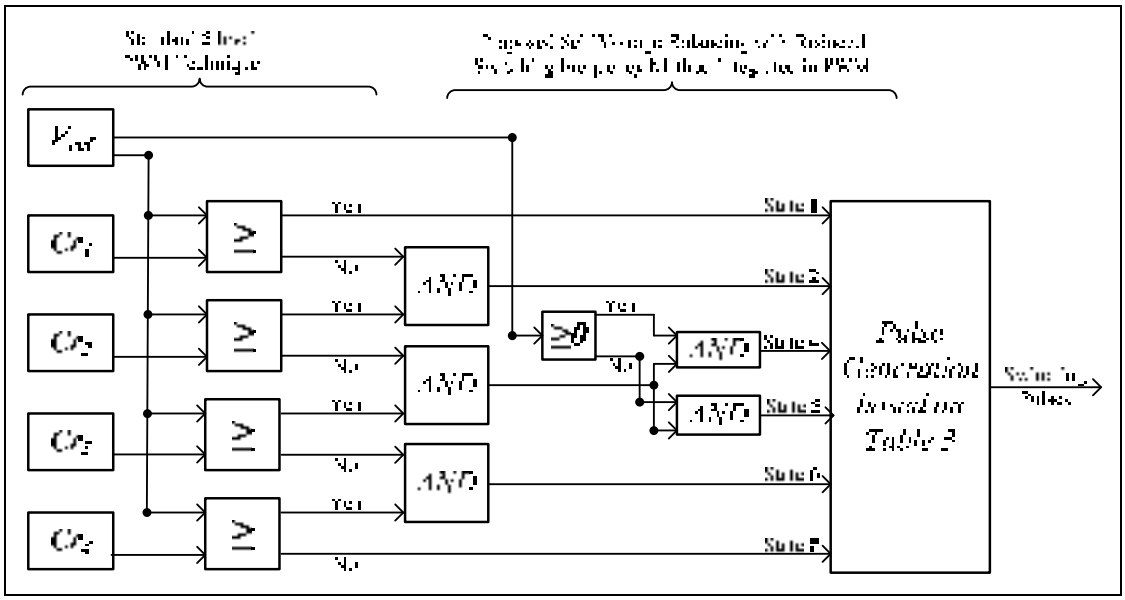

Figure 3.5 Proposed open-loop switching algorithm for self-voltage-balancing of PUC5 Inverter

3.3 Grid-Connected Mode Configuration and Controller

The grid-connected PUC5 inverter with associated controller is shown in Figure 3.6 in which i_s is the injected current from inverter to the grid. The typical controller has been designed to control the amplitude and phase-shift of i_s results in delivering active power and exchanging reactive power desirably with the grid by PUC5 inverter. Even in this controller the DC capacitor voltage is not involved since proposed technique in previous section is in charge of balancing this voltage (Hafezi, Akpinar et Balikci, 2014; Teodorescu et al., 2006; Vahedi, Chandra et Al-Haddad, 2015).

In illustrated controller, AC source voltage (v_s) is measured and sent to the PLL to extract its phase angle. The grid voltage angle is then added to the desired phase shift denoted as θ^*. to exchange reactive power with the grid while injecting active power, power factor (PF) should be between 0 and 1 which can be determined by θ^*. If the unity power factor mode of operation is targeted, therefor $\theta^* = 0$ to ensure an injected grid current synchronized with v_s. For reactive power exchange the power factor should be less than 1. For instance, to have a PF = 0.5 then $\theta^* = 60°$ should be added to the measured voltage angle. The reference angle is sent to the Sin block to produce a unit sine wave containing desired phase shift. This unit sine wave is multiplied by desired value as maximum reference current (I_m^*) which can control

the amount of power injected to the grid. The resulted function is assumed as reference current (i_s^*) that should be generated by the inverter. The actual current (i_s) is compared with reference current and the error signal is sent to a proportional-integral linear controller to minimize the steady state error. The PI controller output signal will be modulated by the proposed switching technique shown in Figure 3.5 which is also responsible in balancing the PUC5 capacitor voltage at half of the DC source amplitude.

PUC5 inverter is expected to generate lower harmonic current waveform injecting to the grid compared to conventional single-phase full-bridge grid-connected inverters due to generating more voltage levels at the output.

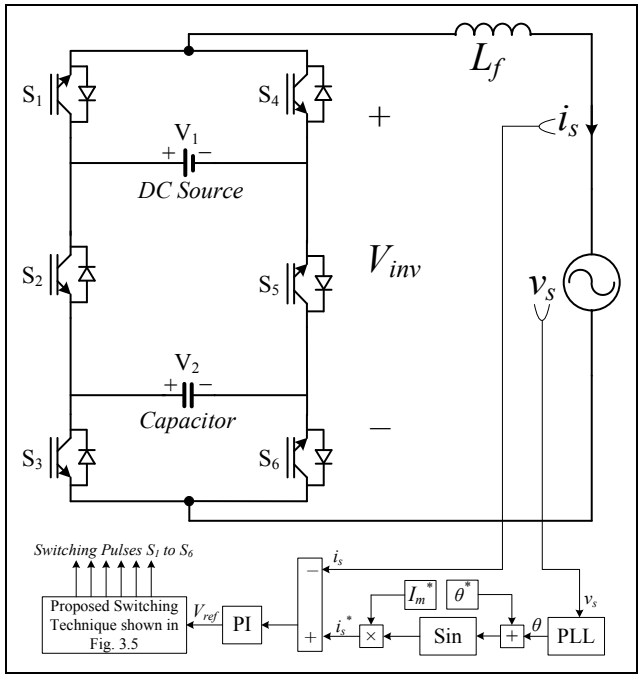

Figure 3.6 Grid-connected PUC5 inverter with designed controller

3.4 Comparative Study of Multilevel Inverter Based on Number of Components

Table 3.3 shows the components count in popular multilevel inverters as well as the proposed PUC5 inverter in case of producing single-phase 5-level output voltage waveform. It is prominent that the proposed converter with the sensor-less voltage balancing technique has the less components as well as its control complexity is very low.

Extending to the n-level, Table 3.4 will be achieved. Component counts are calculated in term of voltage level (n). It should be mentioned that in more than 3-level inverters, no reliable control techniques have been reported for NPC since all of them have some limitations on load power factor and modulation index (Saeedifard, Iravani et Pou, 2009). Although it has been compared in Table 3.3, it is not listed in the Table 3.4 for higher voltage levels. Moreover, the proposed PUC5 inverter is able to produce voltage levels using binary DC links so it would have the levels like 5, 10, 17, 26, ... (Escalante, Vannier et Arzandé, 2002; Malinowski et al., 2010; Rodriguez et al., 2010).

The following chart in Figure 3.7 demonstrates the low number of components used in PUC5 inverter rising by the voltage levels. It is observed that the number of components employed in PUC5 is slowly raised as a function of the produced voltage levels.

Table 3.3 Components count for single-phase five-level inverters

Inverter Type	DC Source	Capacitor	Clamped Diode	Active Switch	Total Parts Count	Control Complexity
CHB	2	0	0	8	10	Low
NPC with voltage control	1	4	6	8	19	Very High
NPC without voltage control	4	0	6	8	18	Low
FC	1	3	0	8	12	High
Proposed PUC5	1	1	0	6	8	Very Low

Table 3.4 Components count for single-phase multilevel inverters

Inverter Type	DC Source	Capacitor	Clamped Diode	Active Switch	Total Parts Count
CHB	$\frac{n-1}{2}$	*0*	*0*	*2(n-1)*	$\frac{5(n-1)}{2}$
NPC without voltage control	*n-2*	*0*	*2(n-2)*	*2(n-1)*	*5n-7*
FC	*1*	*n-2*	*0*	*2(n-1)*	*3(n-1)*
Proposed PUC5	*1*	$\sqrt{n-1}-1$	*0*	$2\sqrt{n-1}+2$	$3\sqrt{n-1}+2$

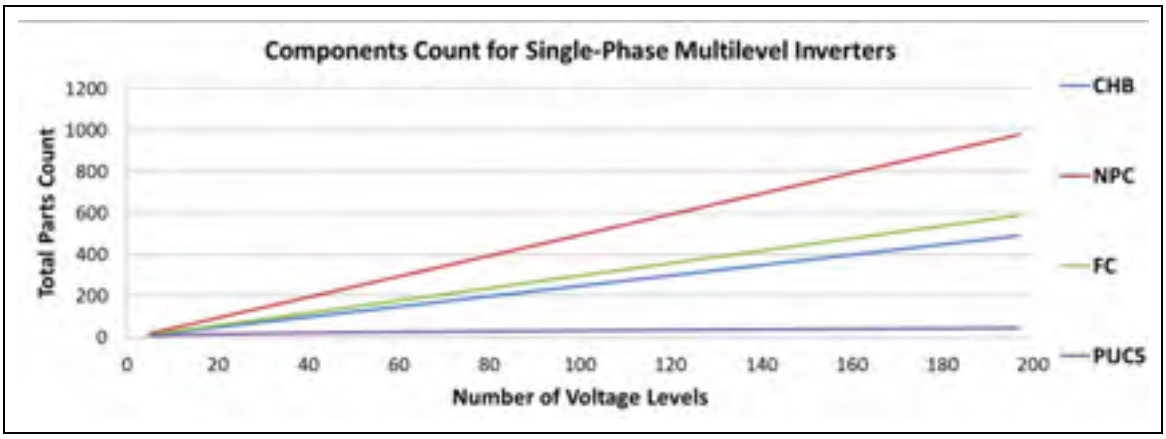

Figure 3.7 Components count chart in multilevel inverters

As a comparison only between 7-level PUC inverter and the proposed PUC5, it should be noted that the 7-level PUC needs a very complicated controller to produce desired voltage levels at the output which requires adjusting a lot of controller gains in practical works. Moreover, the controller design needs a lot of effort in modelling the system accurately and using many state variable feedbacks that increase the number of state variables and consequently voltage and current sensors. Moreover, it is highly dependent on the system parameters including load, connection line impedance, switching frequency, sampling time, DC source voltage amplitude, DC capacitor value, modulation index and output voltage frequency. It can show improper results containing a lot of spikes on the generated voltage waveform, which makes use of additional protection device inevitable. All in all, the 7-level PUC inverter needs more investigation and improvement to be useful in all conditions. On the other hand, the proposed 5-level functionality of the PUC inverter illustrates proper results in all stand-alone and grid-connected conditions without using additional feedback sensors to balance internal DC bus voltage. However, it should be mentioned that the sensor-less voltage balancing is only about the internal capacitor voltage control of the converter and it does not imply on any other external sensors such as shown in Figure 3.6 to control the line current. Less complex controller combined with lower switching frequency are some advantages of the proposed PUC5 inverter with requiring less components count as well.

3.5 Experimental Results

A prototype of PUC inverter has been built to validate the proposed PUC5 with self-voltage-balancing in both stand-alone and grid-connected modes. Six 1.2KV 40A SiC MOSFETs type SCT2080KE have been used as active switches. The proposed self-voltage balancing procedure integrated into switching technique and the designed grid-connected controller has been applied by dSpace 1103 as real-time controller and switching pulses are sent to the PUC5 switches. The tested system parameters are listed in Table 3.5.

Table 3.5 Experimental system parameters

Grid Voltage (v_s)	110 V rms
Grid Frequency	60 Hz
Grid Link Inductor (L_f)	4 mH
DC Source Voltage (V_1)	200 V
Switching Frequency	2 kHz
Stand-Alone mode RL Load	40 Ω, 20 mH
Stand-Alone mode Rectifier Load (DC Side R_{dc} and L_{dc})	40 Ω, 50 mH
DC Capacitor	2500 μF

3.5.1 Test 1: Stand-Alone Mode

The PUC5 inverter has been tested under various load conditions such as stand-alone mode as UPS application including change in load and in DC source. In this mode, the PUC5 inverter supplies an RL type of load.

At first, the start-up mode of the PUC5 inverter is shown in Figure 3.8. The capacitor is charged up to half of DC source by proposed sensor-less voltage balancing approach and five-level output voltage is generated symmetrically. Results show that no pre-charged capacitor is needed in this topology with the implemented voltage control. Moreover, the zoomed figure shows that the capacitor voltage ripple is less than 5%. The FFT analysis of the 5-level inverter voltage waveform has been performed and its harmonic spectrum is shown in Figure 3.8.

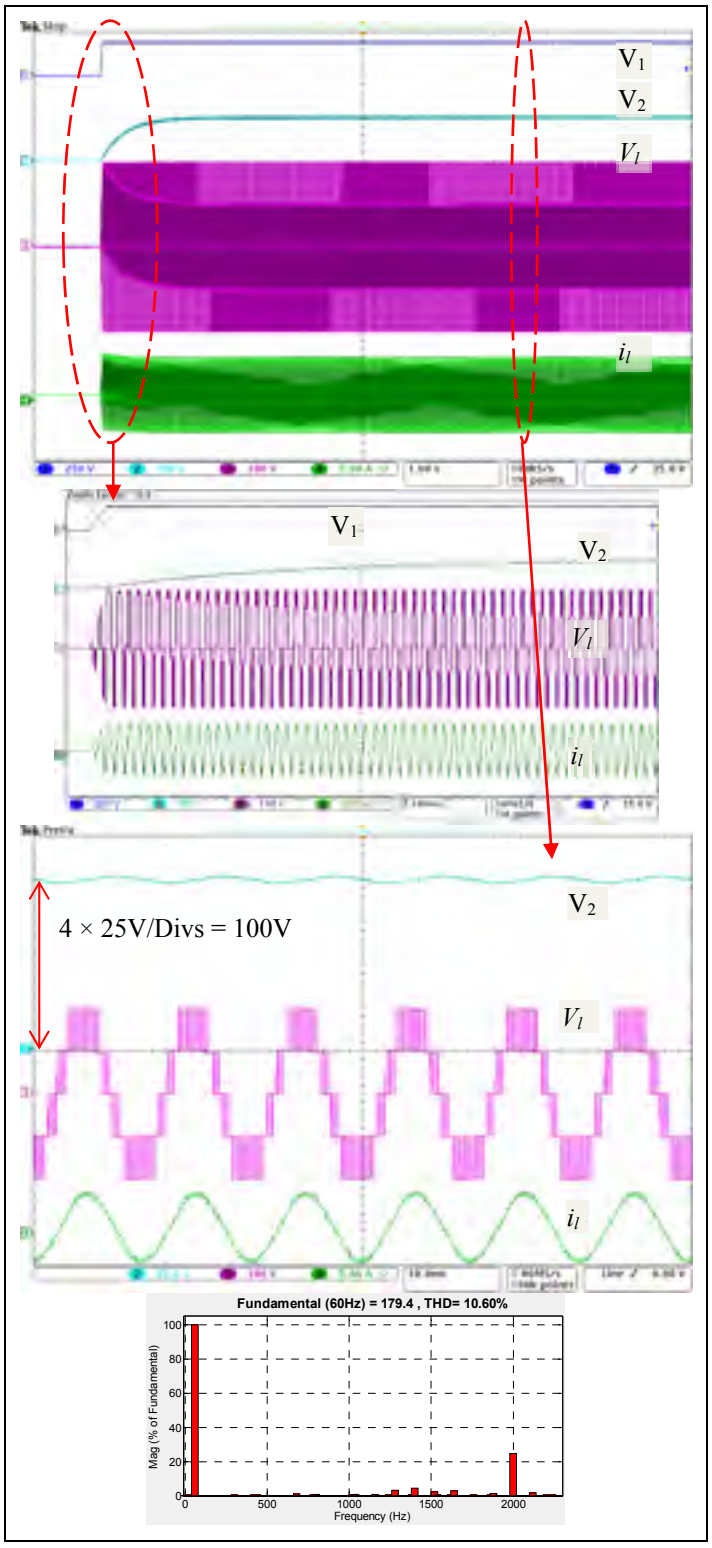

Figure 3.8 Start-up capacitor charging, 5-level voltage generating and FFT analysis

It should be mentioned that the output voltage THD is about 10% without adding additional bulky harmonic filters. 2 kHz frequency of the PWM carriers is clear in this figure as the highest amplitude of the harmonic orders except the fundamental one.

In another test, a nonlinear load consisting of a single-phase rectifier connected to R_{dc} and L_{dc} on its DC side is connected in parallel to the existing RL load and they are feed by PUC5 inverter. Results are illustrated in Figure 3.9 demonstrating the good dynamic performance of proposed technique in variable load conditions.

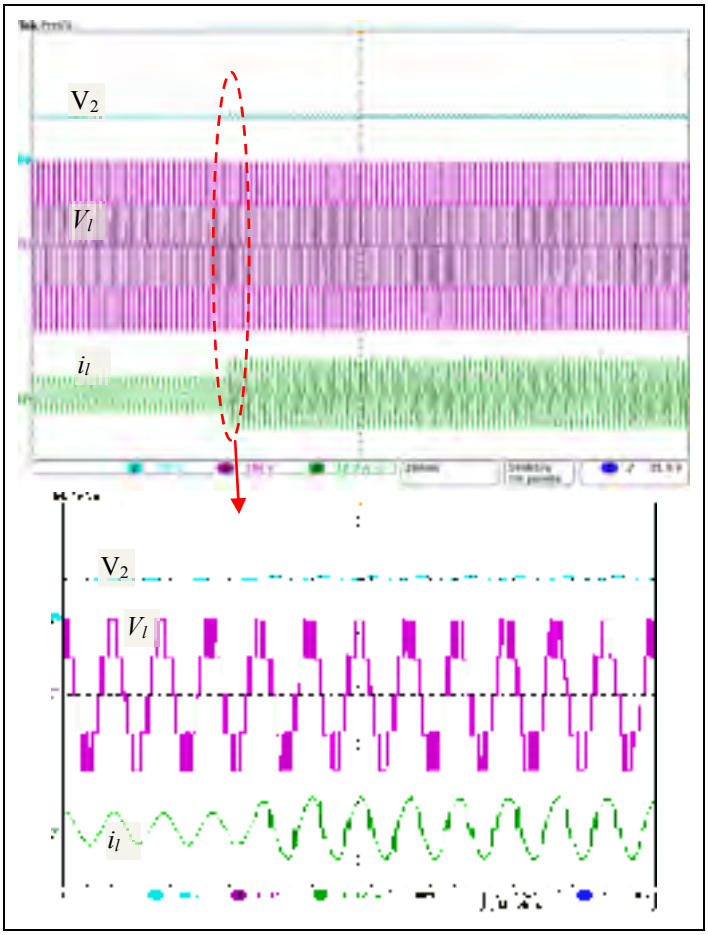

Figure 3.9 Adding single-phase rectifier as nonlinear load to the output of PUC5

Figure 3.10 contains results when the DC source voltage is changing and capacitor voltage is tracking the reference value ($V_1/2$) properly by applying proposed sensor-less voltage regulator technique integrated into switching pattern.

Finally, in stand-alone mode, switches gate pulses as well as one cycle of output voltage are depicted in Figure 3.11. It is clear that two upper switches are operating at grid frequency while their voltage rating as equal to DC source voltage (V_1). Although, four lower switches are fired with higher frequency than upper switches, the switching frequency is not that large compared to 2-level conventional inverters (Vázquez et al., 2008; Wu et al., 2013). Moreover, their voltage ratings are half of two upper switches that they have to withstand capacitor voltage which is $V_1/2$.

3.5.2 Test 2: Grid-Connected Mode

In this case, the PUC5 inverter is connected to a single-phase AC source as grid and the designed controller in section III is forcing the inverter to inject power to the grid with different power factor. At first, to show the fast response and proper dynamic performance of designed grid-connected controller as well as proposed sensor-less voltage balancing technique, $\theta^* = 0$ is selected and the current reference is changed during the test as illustrated in Figure 3.12.

As it is obvious, the grid-connected PUC5 is operating in unity power factor and injecting active power to the grid. The grid-connected controller is working acceptably in making the current waveform in phase with ac voltage waveform. Moreover, the proposed sensor-less self-voltage-balancing method operates significantly perfect in regulating the capacitor voltage at desired level while encountering any types of changes in the system and produces five-level voltage at the output of the inverter. Due to generating 5-level voltage waveform at the output of grid-connected PUC5 inverter, the injecting current through grid would have lower harmonic components without using any extra filters that enlarge the inverter package. Figure 3.13 illustrates the current THD which is too much lower than the acceptable amount in standards.

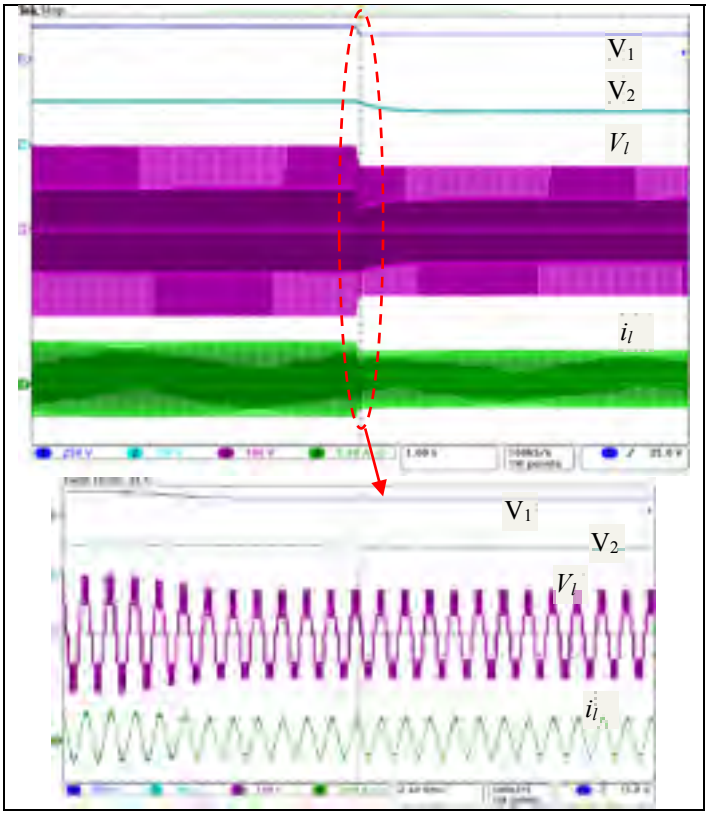

Figure 3.10 DC source voltage changes and capacitor voltage is tracking the reference value

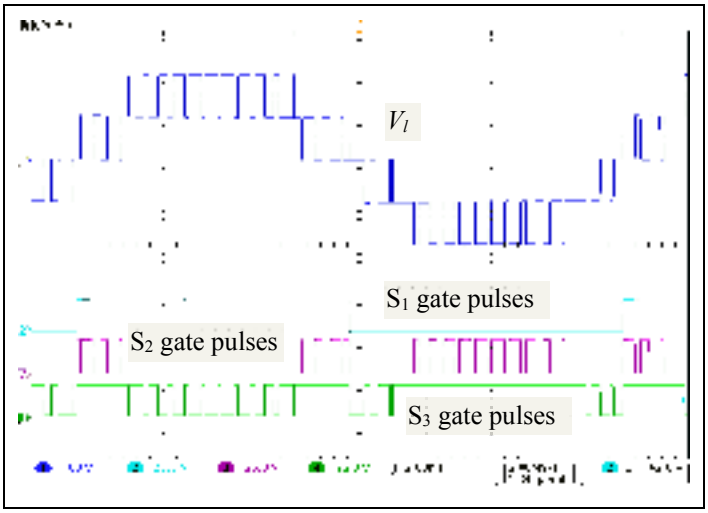

Figure 3.11 Switches gate pulses

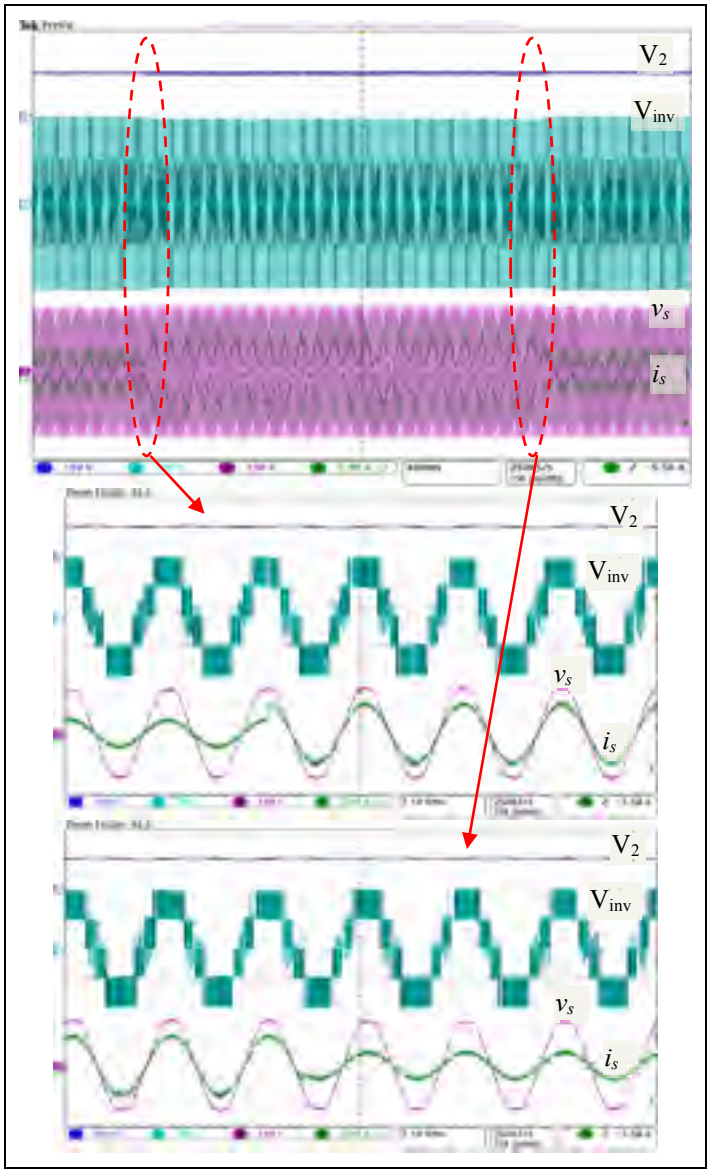

Figure 3.12 Grid-connected PUC5 with change in current reference amplitude

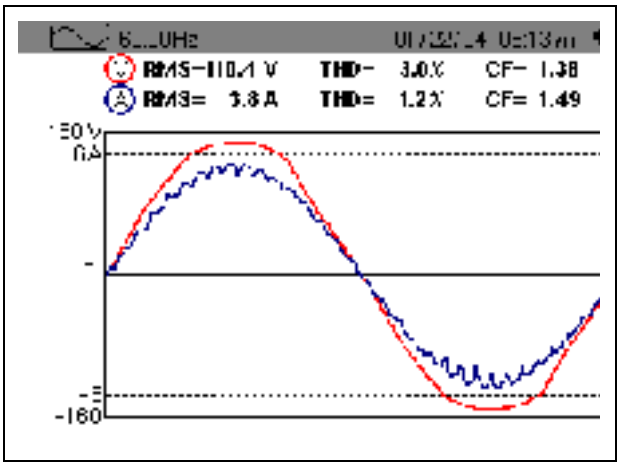

Figure 3.13 THD, and Crest factor computation of injected grid current

Final tests have been performed to exchange reactive power with the grid while injecting reduced amount of active power. Therefore, two different PFs of 0.86 and 0.5 have been selected and associated displacement angles are 30° and 60°, respectively as depicted in Fig 14 which shows the phase shift between grid voltage and current. In both cases (30° & 60° phase shift) the capacitor voltage is regulated at desired level, whereas inverter output waveform contains five identical voltage levels.

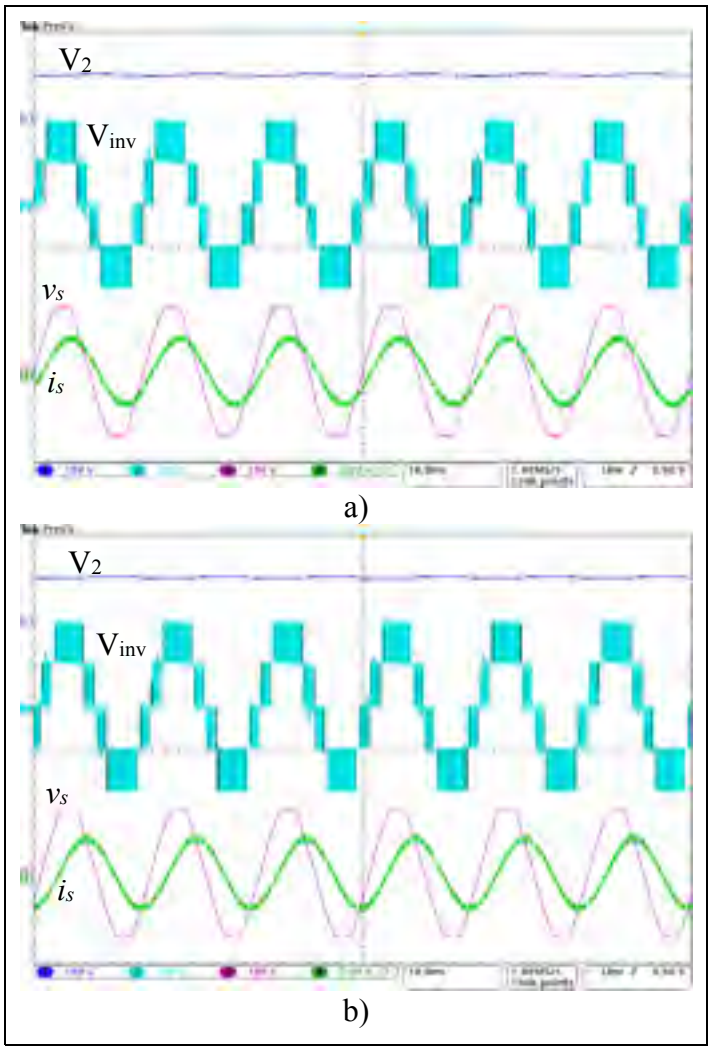

Figure 3.14 PUC5 operation at different power factors a) PF = 0.86, θ = 30° b) PF = 0.86, θ = 60°

3.5.3 Test3: 3-Phase PUC5 inverter

Finally, the 3-phase configuration of the PUC5 inverter has been tested as stand-alone mode of operation. Since the capacitors voltages are regulated automatically through redundant switching states, there would be only 3 isolated DC sources which is half of a CHB with same number of levels. Thus, it could have the same applications of a 3-phase CHB such as high power motor drives, mining applications and industrial UPS but with half number of isolated DC sources that effectively reduce the manufacturing cost and inverter size (Vahedi et Al-Haddad, 2016c).

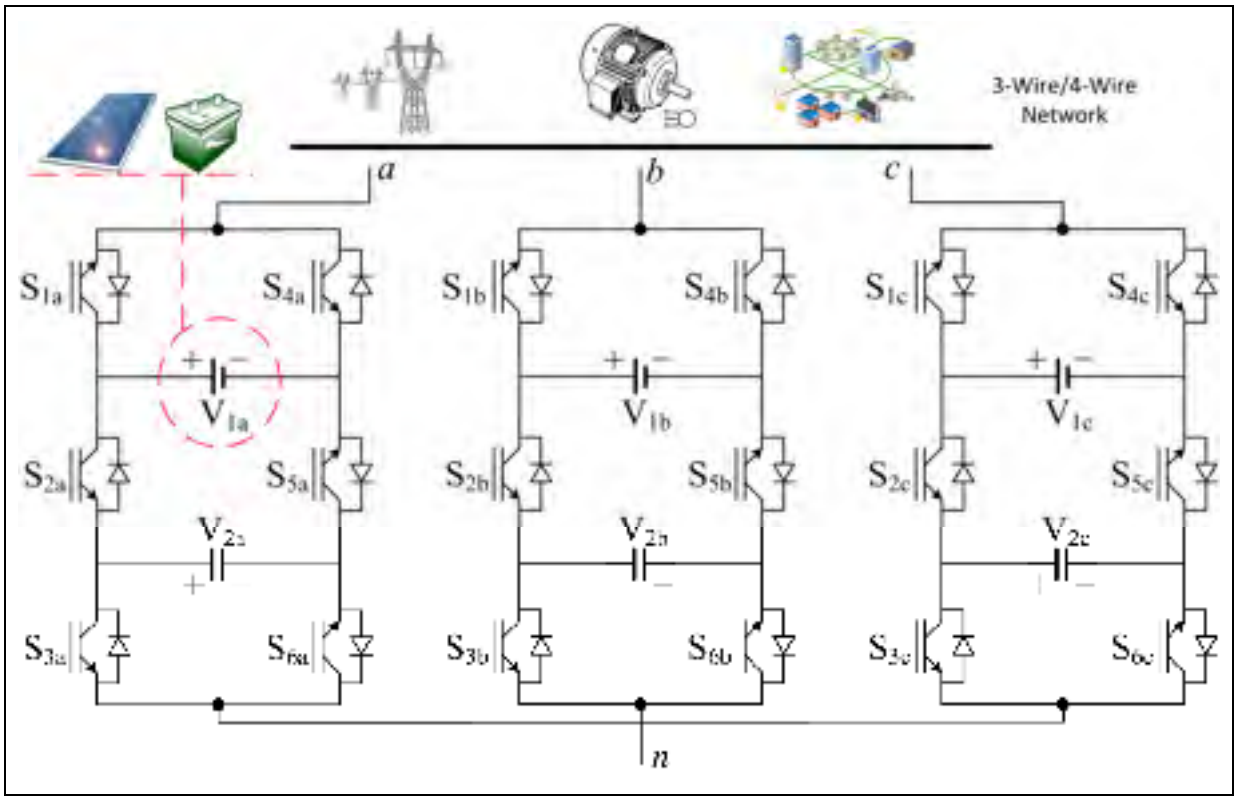

Figure 3.15 3-Phase PUC5 inverter

The 3-phase PUC5 inverter prototype has been tested experimentally. 3-phase RL load has been connected to the PUC5 inverter as 4-wire system. In first test, each DC source has been set at 50V so the capacitors voltages are regulated at 25V. As shown in Figure 3.16, the output phase voltage, line voltage and load voltage are 5-level, 9-level and 17-level, respectively. Therefore, it is clear that the load voltage would be almost sine wave with least harmonic distortion. Such voltage waveform could be used at the output to supply the loads without any addition harmonic filters.

In another test, the DC sources voltages have been raised to 150V where capacitors voltages would be fixed at 50V to have symmetrical voltages waveforms at the output. 3-phase line voltages have been captured and illustrated in Figure 3.17.

The balanced capacitors voltages resulted in straight middle voltage levels of the output waveforms which is clear in all test results.

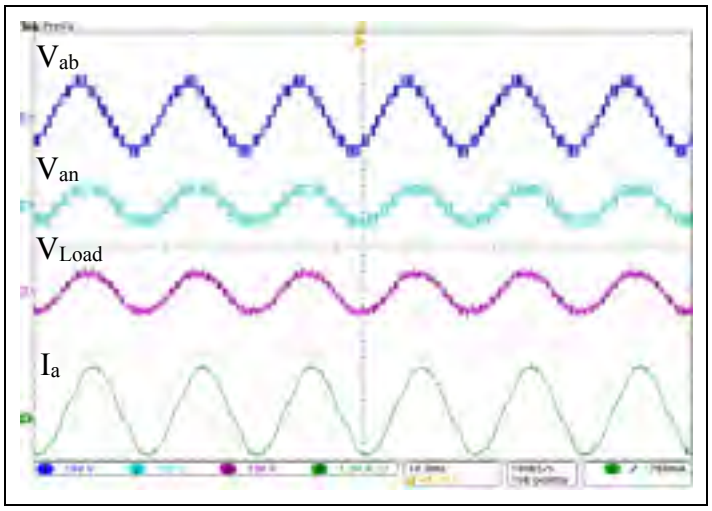

Figure 3.16 Phase, Line and Load voltage waveforms of 3-phase PUC5 inverter

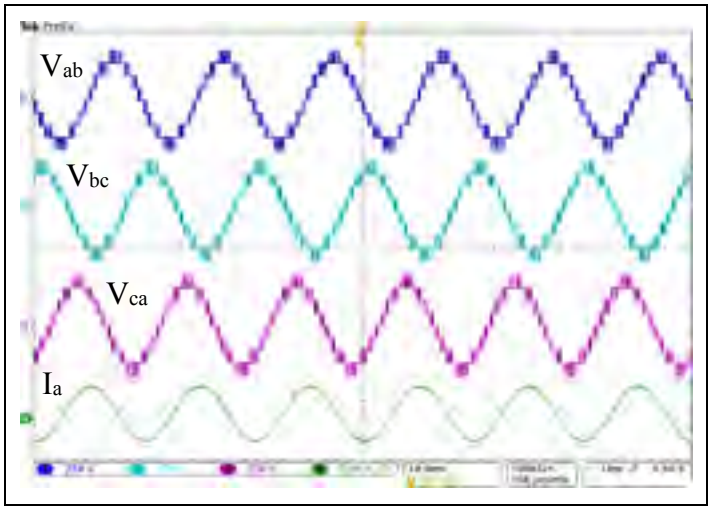

Figure 3.17 3-Phase line voltages of PUC5 inverter

7-level waveform has been replaced by 5-level operation containing equal harmonic contents while a significant simplicity has been obtained on the controller with PWM switching technique useful for various industrial applications. In the PUC5 converter, due to accurate voltage balancing process, the output voltage waveform shows a good symmetry in positive and negative half cycles that makes its THD smaller.

3.6 Conclusion

The PUC5 inverter has been proposed in this project while the capacitor voltage is balanced without involving any external controller and voltage feedback sensors. The proposed sensor-

less voltage controller has been integrated into switching technique to work as open-loop system with reliable results. Moreover, another controller has been designed for the PUC5 inverter to work as unity power factor grid-connected inverter. Low harmonics components in both voltage and current waveforms generated by PUC5, no need to bulky output filters, reliable and good dynamic performance in variable conditions (including change in DC source, load, power amount injected to the grid), requiring no voltage/current sensor in stand-alone mode, low manufacturing costs and miniaturized package due to using less components and etc are interesting advantages of the introduced PUC5 topology which have been proved by experimental results in both stand-alone and grid-connected modes. Moreover, the 3-phase three/four wire configuration of the PUC5 inverter has been illustrated and tested experimentally to show its advantages such as lower number of isolated DC sources over the other multilevel topologies in the market. The presented PUC5 inverter can be a challenging candidate for conventional photovoltaic application inverters.

CHAPTER 4

A NOVEL MULTILEVEL MULTI-OUTPUT BIDIRECTIONAL ACTIVE BUCK PFC RECTIFIER

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Abstract

This chapter presents a new family of buck type PFC (power factor corrector) rectifiers that operates in CCM (continuous conduction mode) and generates multilevel voltage waveform at the input. Due to CCM operation, commonly used AC side capacitive filter and DC side inductive filter are removed from the proposed modified packed U-cell rectifier structure. Dual DC output terminals are provided to have a 5-level voltage waveform at the input points of the rectifier where it is supplied by a grid via a line inductor. Producing different voltage levels reduces the voltage harmonics which affects the grid current harmonic contents directly. Low switching frequency of the proposed rectifier is a distinguished characteristic among other buck type rectifiers that reduces switching losses and any high switching frequency related issues, significantly. The proposed transformer-less, reduced filter and multilevel rectifier topology has been investigated experimentally to validate the good dynamic performance in generating and regulating dual 125V DC outputs terminals as telecommunication boards feeders or industrial battery chargers under various situation including change in the loads and change in the in main grid voltage amplitude.

4.1 Introduction

Nowadays DC power supply is a big demand of industries to charge up batteries especially for uninterruptible power supplies (UPS), electric vehicles (EV), feeding communication boards and to use in various power applications (Mobarrez et al., 2015). Regulated constant voltage at the output in addition to low harmonic and unity power factor current at the input

should be ensured in such equipment to comply with harmonic standards defined by different association like IEEE and IEC (IEC, 1995; IEEE, 2014). PFC rectifiers have been proposed many years ago to overcome the input AC voltage and current power factor issue. Such converters can be divided into two main categories based on their output DC voltage amplitude. If the output DC voltage level is less than the input AC peak voltage value, it is called a PFC buck rectifier and conversely, a PFC boost rectifier generates a DC voltage greater than the AC peak voltage (Singh et al., 2003).

PFC buck rectifiers are mainly known with their discontinuous conduction mode (DCM) which complicates formulating the output voltage. On the other hand, DCM operation makes the output DC voltage control depending on the load impedance and also makes it inevitable to use large inductive filters at DC side (Choi, 2013; Wu et al., 2012). Moreover, high switching frequency e.g. 65 kHz and more is a normal operating point in reported topologies that increases switching losses significantly (Jang et Jovanovic, 2011; Xie et al., 2013). Large-size LC filters at the output as well as non-removable AC side filters are inherent disadvantages of PFC buck rectifiers. Detailed problems associated with such rectifiers are investigated in the literature (Chaudhary et Sensarma, 2013; Dai et al., 2007). Another configuration to generate a reduced DC voltage is combination of diode-bridge and dc-dc buck converter in which the AC voltage is rectified by that diode-bridge and then DC voltage is stepped down at a desired level by the chopper. Such two-stage structures present more power losses, low efficiency and high manufacturing costs in medium and high power applications due to using many semiconductors and reactive components (Huber, Gang et Jovanovic, 2010).

Regarding above-mentioned facts, PFC buck rectifiers are not so much welcome in industrial applications compared to boost type of those PFC rectifiers. Such boost types do not require bulky filters at AC or DC sides since ensuring harmonic suppression of input current, unity power factor operation of the system and constant DC voltage at the output terminal. To have a reduced DC voltage at the output, bridgeless PFC boost rectifiers are usually connected to the main grid after a step-down transformer (Tanaka et al., 2013). Therefore, to have a 125 V DC at the output terminal of a PFC boost rectifier from a 120V RMS grid, a transformer

should be used to reduce the grid peak voltage to less than 125 V that has its own disadvantages.

In this section, a new family of bidirectional bridgeless buck PFC rectifiers is introduced which is an efficient cure to all above-mentioned issues. The proposed 5-level rectifier operates in boost mode while splitting the output voltage terminals to have multiple-output with reduced voltage levels as buck mode. Supplying multiple-output terminals result in producing a multilevel voltage waveform at the rectifier input that reduces the harmonic content of the rectifier voltage and consequently the grid current harmonic without using large inductive filters at the AC side (Kouro et al., 2010). Boost mode operation of the overall system helps removing bulky filters from both sides specially the DC side inductor. Moreover, CCM operation is guaranteed in a whole period. The topology and operation of the 5-level rectifier is explained in section 4.2. Integrated voltage control into switching technique as well as implemented controller is presented in section 4.3 and 4.4, respectively. Power balance analysis of the proposed rectifier is studied in section 4.5. Eventually low harmonic content of the input 5-level voltage waveform, unity power factor and low harmonic AC current waveform of the proposed rectifier is validated through experimental tests. Results are illustrated and discussed in section 4.6 to prove the good dynamic performance of the proposed rectifier in various situations including change in the loads or input AC voltage amplitude.

4.2 Proposed PFC Buck Rectifier Topology and Operation Principle

The proposed rectifier topology has been shown in Figure 4.1. It has 6 active switches and two output DC terminals. The output terminals are providing voltages V_1 and V_2 to loads that should be identical as E to have a five-level voltage waveform at the rectifier input. Rectifier input voltage is measured at points ‘a’ and ‘d’ as V_{ad}. The switching states associated to the introduced rectifier have been listed in Table 4.1.

The proposed 5-level rectifier is a modification to the well-known PUC converter (Al-Haddad, Ounejjar et Gregoire, Nov 2011; Vahedi, Labbe et Al-Haddad, 2016) in which the lower U-cell components are connected in reverse direction. The PUC converter was

proposed as an inverter to generate 7-level voltage waveform while using a single isolated DC source and a controlled capacitor (Vahedi et Al-Haddad, 2016a). Moreover, it has been tested as a 7-level rectifier supplying a DC load in boost mode of operation (Ounejjar, Al-Haddad et Dessaint, 2012). Another similar structure with cascaded cells was proposed in (Kangarlu, Babaei et Sabahi, 2013) but as an inverter application with no control that only requires too many isolated DC sources. It has been also proposed as a cell to be used in modular multilevel converters (MMC) (Nami et al., 2013).The main idea of this work is to introduce a rectifier by utilizing the similar structure of PUC with slight modification working in buck mode to supply DC loads with lower voltages than the grid where no transformer and additional filter would be required (Vahedi et al., 2015a; Vahedi et Al-Haddad, 2016b).

It is clear from Table 4.1 that each pair of switches S_1-S_4, S_2-S_5 and S_3-S_6 is working in complementary manner. All switching states and associated conducting paths are shown in Figure 4.2 which will be used in voltage regulator design section.

By controlling output DC voltages, V_{ad} would have five levels including ±2E, ±E, 0 that the maximum value is +2E. The principal concept of proposing this topology as a buck rectifier relies on this maximum value of V_{ad} which should be more than the AC source peak value ($v_{s\,max}$). The following relations can be written, accordingly.

$$V_{ad} \geq v_s \rightarrow 2E \geq v_{s\ \max} \rightarrow E \geq \frac{v_{s\ \max}}{2} \tag{4.1}$$

For instance, if RMS voltage of the AC source is 120V, then the maximum value would be 170V and the following relations would be obtained. To maintain the stable operation of the converter in buck mode, the maximum generating DC voltage is set at $v_{s\,max}$ which would be 170 V here.

$$\frac{v_{s\ \max}}{2} \leq E \leq v_{s\ \max} \rightarrow 85V \leq E \leq 170V \tag{4.2}$$

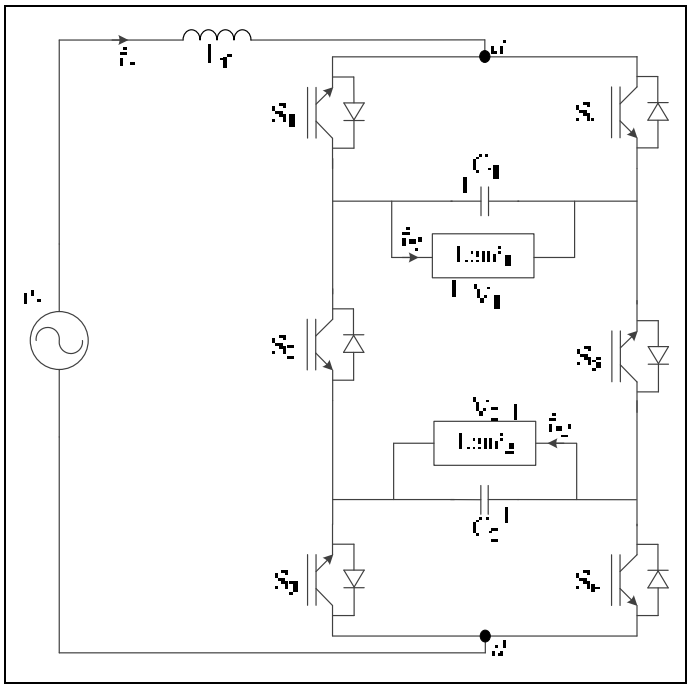

Figure 4.1 Proposed five-level buck PFC rectifier

Table 4.1 Switching States of the proposed Five-Level Buck PFC Rectifier

Switching State	**S_1**	**S_2**	**S_3**	**S_4**	**S_5**	**S_6**	**V_{ad}**	**V_{ad} voltage levels**
1	1	0	1	0	1	0	V_1+V_2	+2E
2	1	0	0	0	1	1	V_1	+E
3	0	0	1	1	1	0	V_2	+E
4	1	1	1	0	0	0	0	0
5	0	0	0	1	1	1	0	0
6	1	1	0	0	0	1	$-V_2$	–E
7	0	1	1	1	0	0	$-V_1$	–E
8	0	1	0	1	0	1	$-V_1-V_2$	–2E

As mentioned above, this rectifier is a boost converter in grid point of view due to generating peak voltage of V_1+V_2 at the input (V_{ad}) which is always equal or greater than the $v_{s\ max}$. On the other hand, by splitting the produced DC voltage between two output terminals, each one would have half voltage amplitude so their amplitude are always less than or equal to the v_{smax} that guarantees the buck mode operation of proposed rectifier from loads points of view. It could be concluded that by using two output terminals, the grid is relieved by the converter.

Therefore, the stepped down DC voltages are achieved however the overall rectifier is in step-up mode. As results, the bulky inductor at DC side as well as the capacitor filter at AC side of conventional PFC buck rectifiers would be removed. Moreover, low harmonic V_{ad} and also low THD line current (i_s) are attained even when the proposed rectifier is running at low switching frequency which leads to low power losses and high efficiency (Vahedi et al., 2015a).

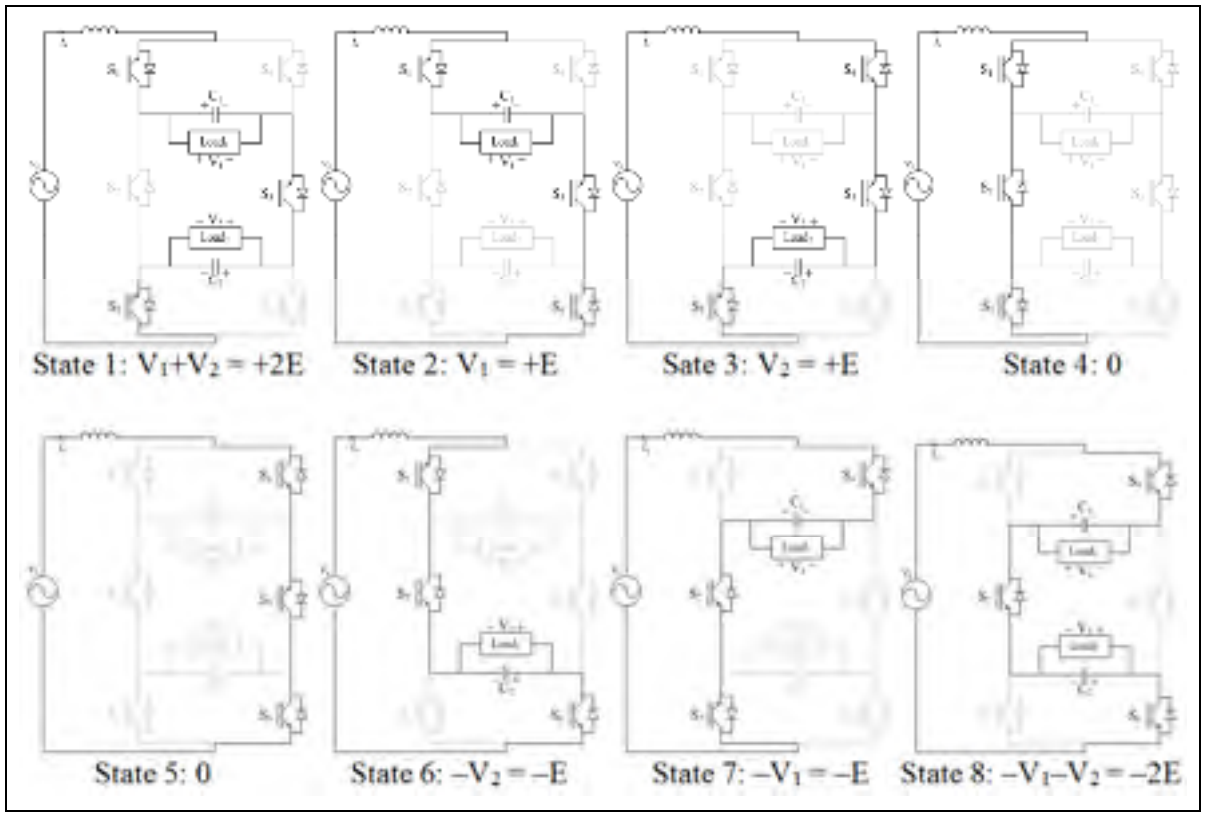

Figure 4.2 Operating sequences and conducting paths of proposed 5-level buck rectifier

4.3 Switching Technique and Integrated Voltage Regulator

Due to utilizing more than one DC capacitor in multilevel converter topologies, regulating and balancing their voltages is the most challenging part of the controller (Aquila et al., 2005; Kumar et al., 2015; Vahedi, Labbe et Al-Haddad, 2016). Redundant switching states can play an important role in facilitating the controller duty of regulating the output DC terminals voltages. In this regard, the switching states should be analyzed precisely to find the charging

and discharging path for capacitors. Table 4.2 lists such investigation results on the proposed rectifier switching states.

Noticing Table 4.2, it is clear that redundant switching states of 2, 3, 6 and 7 can help regulating capacitors voltages beneficially. Hence, the switching pattern of the PWM block would be modified in order to decide between switching states 2 or 3 when the line current is positive and the +E voltage level should be generated at the output. It means that if V_1 is less than V_2 then switching state 2 would be applied to switches and if V_1 is more than V_2 then the output pulses would be generated by switching state 3. The same process is defined to choose between switching states 6 or 7 when line current is negative and output voltage should be –E.

All these actions are taken inside the PWM block shown in Figure 4.3. Moreover, the reference signal is first modulated by 4 vertically shifted carriers in order to determine the associated voltage level and then the required pulses are sent to the switches considering capacitors voltages and redundant switching states (Leon et al., 2016; Vahedi et al., 2014).

Table 4.2 Effect of Switching States On Output DC Capacitors

Switching State	**Line Current Sign**	**V_{ad}**	**V_{ad} voltage levels**	**Effect on C_1**	**Effect on C_2**
1	$i_s > 0$	V1+V2	+2E	Charging	Charging
2	$i_s > 0$	V1	+E	Charging	Discharging
3	$i_s > 0$	V2	+E	Discharging	Charging
4	$i_s \geq 0$	0	0	Discharging	Discharging
5	$i_s \leq 0$	0	0	Discharging	Discharging
6	$i_s < 0$	-V2	–E	Discharging	Charging
7	$i_s < 0$	-V1	–E	Charging	Discharging
8	$i_s < 0$	-V1-V2	–2E	Charging	Charging

All these procedures are to simplify regulating DC voltage terminals. Therefore, the voltage control loop would generate less error due to balancing the DC voltages by the redundant switching states. Figure 4.3 depicts the PWM block input/output signals in detail.

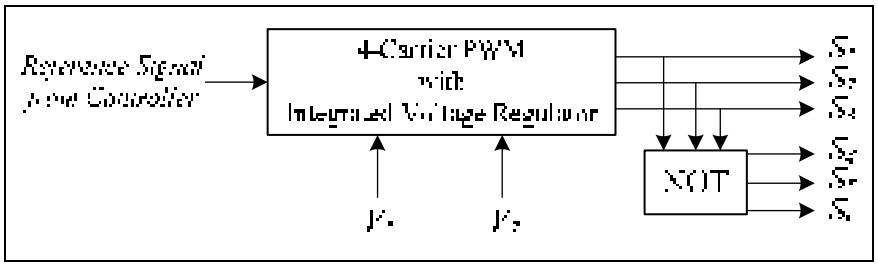

Figure 4.3 Input/output signals of PWM block with integrated voltage regulator

4.4 Implemented Controller

A cascaded PI controller has been applied to regulate the three state space variables including capacitors voltages (V_1 & V_2) as well as grid current (i_s) and to provide a unity power factor operation of the five-level rectifier (Hafezi, Akpinar et Balikci, 2014). Figure 4.4 shows the block diagram of the implemented controller. A phase locked loop (PLL) block is used to extract the voltage angle and generate the synchronized current reference i_s^* which should be drawn by the rectifier in order to ensure the power factor correction. The outer loop of the cascaded controller includes the voltage regulator which its output goes to the current controller (inner loop) as the reference signal amplitude. Therefore, to have balanced voltages at the output DC terminals, sum of the DC voltages are regulated using a PI controller. Each DC voltage reference is assumed as V_{ref}, thus the total DC voltage reference would be $2V_{ref}$. PI regulator minimizes the total DC voltages at $2V_{ref}$ as shown in Figure 4.4. Afterwards, the voltage balancing technique integrated into the switching method (as described in section 4.3) is applied to ensure equal voltage amplitude ($V_1 = V_2 = V_{ref}$) at DC buses. Concluding that the controller is regulating total DC voltage as $2V_{ref}$ using the flowing current through the converter while the switching technique and redundant states would charge and discharge the capacitors equally to have identical voltage levels (V_{ref}) at the DC output terminals. That decoupled voltage control helps balancing capacitors voltages even in faulty conditions where the switching actions could not balance two DC voltages while the sum of DC voltages is regulated at $2V_{ref}$. This mode helps preventing any uncontrolled charging up of the capacitors to an unlimited level.

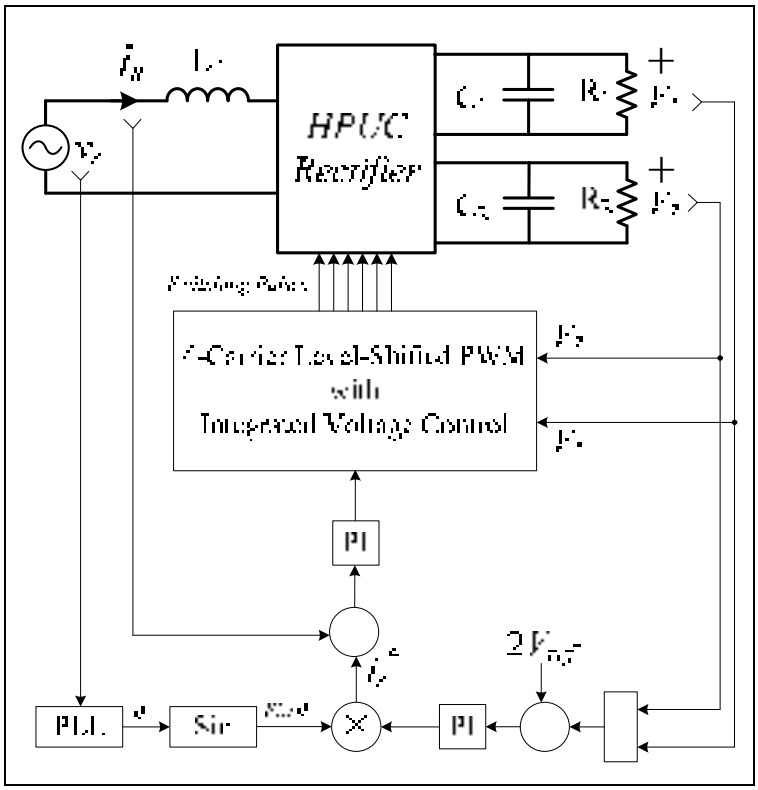

Figure 4.4 Block diagram of the proposed rectifier and Implemented controller

It should be noted for the inner loop (current control) PI controller have good performance where the input signal frequency is low (e.g. outer loop as DC voltage regulator); while it shows some steady-state error when the input is a time-varying signal, like a sinusoidal current, leads to tracking error in the line current (Wang et al., 2014). To ensure the possible minimum error on the output current, the integral gain of the current control PI block should be small enough which makes the inner loop faster than outer loop as well as not that small which is required to eliminate steady state error and consequently results would be acceptable (Bacha, Munteanu et Bratcu, 2014).

4.5 Power Balance Analysis

Noticing to the 5-level rectifier configuration in the Figure 4.1, it is clear that S_2 and S_5 have voltage rating of two times more than the other four switches (S_1, S_3, S_4, and S_6).

Therefore, S_2 and S_5 can be split into two series switches in order to suffer equal voltage rating as shown in Figure 4.5. The point (*m*) is chosen to split two cells which are kind of

full-bridge modules. Similarly to the work performed on cascaded H-bridge (CHB) multilevel converter (Vazquez et al., 2010; Vazquez et al., 2009), the following analysis is done to show the power balance ratio between two independent loads connected to the proposed rectifier.

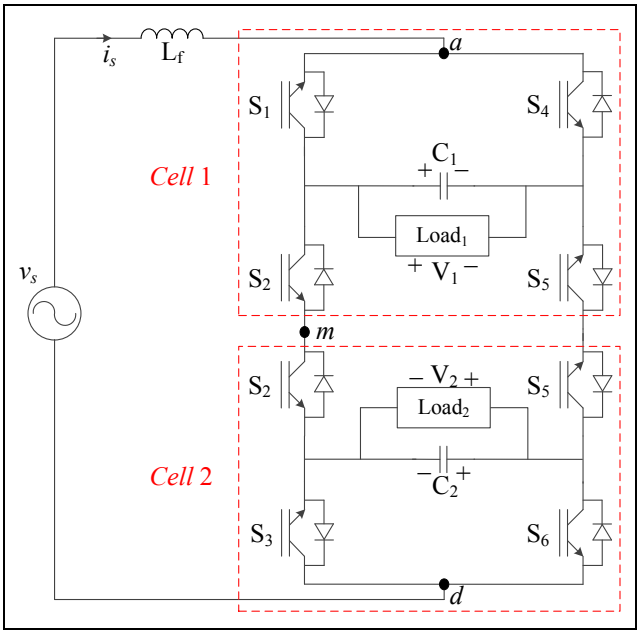

Figure 4.5 Split configuration of the proposed rectifier into two cells for power balance analysis

The following equation is visible on the rectifier structure:

$$V_{ad} = V_{am} + V_{md} \tag{1.3}$$

Therefore an extended representation of the studied rectifier topology shows that the latter is formed by two series cells (Cell 1 and Cell 2). Each cell generates a DC voltage to supply the load; however the common switches and current paths do not allow each cell to operate separately. To continue with the analysis, following definitions are provided:

v_f = RMS (V_{ad}) : rectifier RMS voltage

v_s = Grid RMS voltage

v_L = RMS (V_L) : Line Inductor RMS voltage

Moreover, since each cell voltage (V_{am} & V_{md}) are 3-level waveforms including 0 and ±E volts, their RMS values are defined as:

v_1 = RMS (Vam) = $0.7797 \times m_1 \times V_1$

v_2 = RMS (Vmd) = $0.7797 \times m_2 \times V_2$

Where, m_1 and m_2 are the modulation indexes of each cell that are between 0 and 1. So their maximum value would be defined as:

$v_{max1} = 0.7797 V_1$

$v_{max2} = 0.7797 V_2$

It should be noticed that these maximum values of RMS voltages are obtained in case of two separately working cells. The one line diagram of the presented rectifier can be drawn as shown in Figure 4.6-a. By neglecting circuit power losses and capacitor energy consumption, it can be said that the power consumed in Cell 1 is P_1 and similarly for Cell 2 power is P_2. The total power is drawn from the grid as P. They can be formulated as below:

$$P_1 = \frac{V_1^2}{R_1} \;,\; P_2 = \frac{V_2^2}{R_2} \qquad (4.4)$$
$$P = v_s i_s = P_1 + P_2$$

From Eq. (4.4) and since DC voltages are controlled, this yield to Eq. (4.5):

$$\frac{P_1}{P_2} = \frac{R_2}{R_1} \qquad (4.5)$$

In this rectifier, the buck mode of operation is proposed where $V_1 + V_2 = \text{Max}(V_{ad})$. Therefore considering RMS values, the following relation is achieved:

$$v_1 \le v_f \;,\; v_2 \le v_f \;,\; v_1 + v_2 = v_f \qquad (4.6)$$

Based on voltage relations, the phasor diagram of the rectifier can be drawn as in Figure 4.6-b.

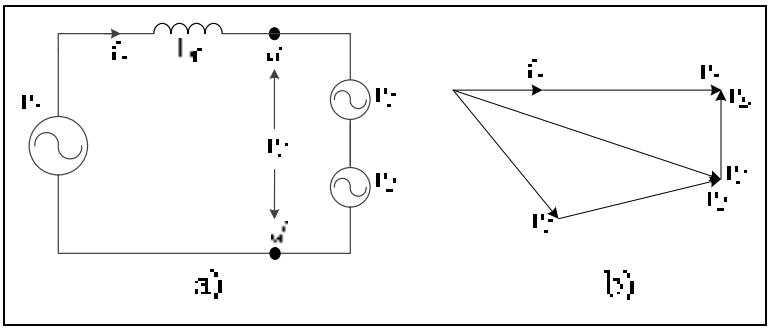

Figure 4.6 a) one line diagram of the 5-level rectifier b) Phasor diagram of the system voltages

Moreover, for the maximum voltage of each cell the following relation can be written (Vazquez et al., 2010):

$$v_{max1} \leq v_f \quad , \quad v_{max2} \leq v_f \quad , \quad v_{max1} + v_{max2} \leq v_f \tag{4.7}$$

The maximum voltages that can be generated by each cell would produce the maximum power that can be delivered to the loads (P_1 & P_2) in a stable operation. Thus, the diagram shown in Figure 4.7-a is obtained and the shaded area shows the area where maximum power can be delivered to loads while the rectifier works in stable mode. It means that the DC voltages are equally balanced and the input grid current is locked to the grid to deliver only active power.

Based on Figure 4.7-a, v_1 and v_2 can be placed in the shaded area so the boundary would be the maximum and minimum limits for those voltages that gives the maximum and minimum power generated by each cell. Since the rectifier should always draw active power from the grid, therefore the minimum and maximum limits are projected on the x-axis to ensure the unity power factor operation as 0° phase shift with current which is illustrated in Figure 4.7-b.

Paying attention to the x_1-axis, the minimum power drawn by the Cell 1 is the left vertical dashed line which is due to the lowest RMS voltage (v_1). Therefore by assuming an equal current through the converter, the remained power ($v_s i_s$–P_1) is consumed in Cell 2. Since P_1 is at the minimum level, P_2 would be the maximum. Similarly, the maximum power limit of Cell 1 is the right vertical dashed line so the voltage vectors on x_2-axis are obtained.

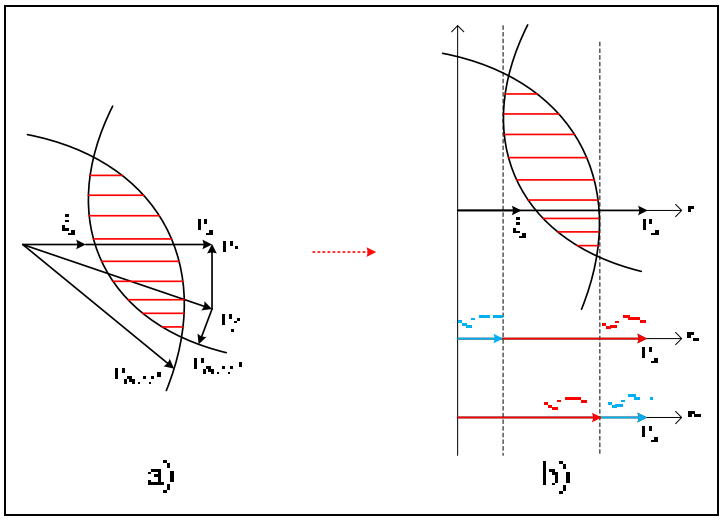

Figure 4.7 a) stable operation area of the rectifier
b) Minimum and maximum power generated by each cell and associated voltages

Based on above explanation and Figure 4.7, power relations are extracted for each cell power as Eq. (4.8).

$$
\begin{aligned}
P_{1\ \max} &= \frac{v_1^{P_{1\ \max}}}{v_s}\ P \\
P_{1\ \min} &= \frac{v_s - v_2^{P_{2\ \max}}}{v_s}\ P \\
P_{2\ \max} &= \frac{v_2^{P_{2\ \max}}}{v_s}\ P \\
P_{2\ \min} &= \frac{v_s - v_1^{P_{1\ \max}}}{v_s}\ P
\end{aligned}
\qquad (4.8)
$$

Where, $v_1^{P_1 max}$ is the cell voltage with maximum possible power delivering to the load. Other variables have the same definitions. Since two DC voltages are identical, minimum/maximum powers of two cells would be equal. Assuming $V_1 = V_2 = 125V$, the following values would be obtained:

$$
\begin{aligned}
P_{1\ \max} &= P_{2\ \max} = \frac{125 \times 0.7797}{120}\ P = 0.8121P \\
P_{1\ \min} &= P_{2\ \min} = \frac{120 - 125 \times 0.7797}{120}\ P = 0.1878P
\end{aligned}
\qquad (4.9)
$$

Based on the above values, it can be concluded that each cell can have a specific maximum and minimum power as a portion of the input total power. Therefore, the highest difference between two cells power would be in a situation where the Cell 1 takes P_{1min} (or P_{1max}) and the Cell 2 consumes P_{2max} (or P_{2min}). Thus, the maximum power ratio between two cells and consequently the power ratio between two DC loads can be obtained as:

$$\frac{R_2}{R_1} = \frac{P_{2\ max}}{P_{1\ min}} = 4.32 \qquad (4.10)$$

Due to symmetrical configuration of the 5-level rectifier, this ratio can be used for R_1/R_2 similarly.

To validate the performed analysis on the power balance of this rectifier, some simulations have been done in Matlab/SPS and three different values have been used for R_1 while R_2 was fixed at 43Ω to show the stable and unstable operation of the proposed rectifier. It should be noted that all simulation parameters except loads were same as experimental ones listed in Table 4.3. As shown in Figure 4.8, three steps have been applied.

At first step, $R_1 = R_2 = 43\Omega$ so $R_2/R_1 = 1$ and rectifier works in stable mode drawing almost 750W from the grid as shown in Figure 4.8-a (1^{st}s to 2^{nd}s). Grid voltage and current are in-phase and the rectifier voltage has 5 identical levels with low voltage ripple on DC capacitors as illustrated in Figure 4.8-b.

At second step, R_1 is reduced to 15Ω to validate the capability of the rectifier to supply different loads yet in stable area and near the limit. As illustrated in Figure 4.8-a (2^{nd}s to 3^{rd}s), 1400W power is delivered to various independent loads with equally balanced voltages but different ripples due to supplying smaller load on upper terminal (V_1). Grid voltage/current as well as the rectifier 5-level voltage waveform with identical levels have been provided in Figure 4.8-c.

Eventually, at third step (3^{rd}s to 4^{th}s), R_1 is reduced to 8Ω forcing the rectifier to fall into the unstable area where $R_2/R_1 = 5.3$. As can be seen from Figure 4.8-a at that time, the reduced load needs more power (about 1950W) but the converter cannot provide the requested

amount of current and consequently the voltage drops down undesirably. Simultaneously, the other load voltage is increased unwantedly (because of the fact that PI regulator tries to keep the sum of DC voltages at 250V) so it draws more current leads to increase in the input power to 1650W. It is illustrated that two voltages are not balanced anymore. On the other hand, the line current is still controlled to be synchronized with grid voltage. Those Unbalanced voltage levels are observable in 5-level waveform of Figure 4.8-d. Such unbalanced levels impose undesirable harmonics into the current waveform which requires larger filter to eliminate.

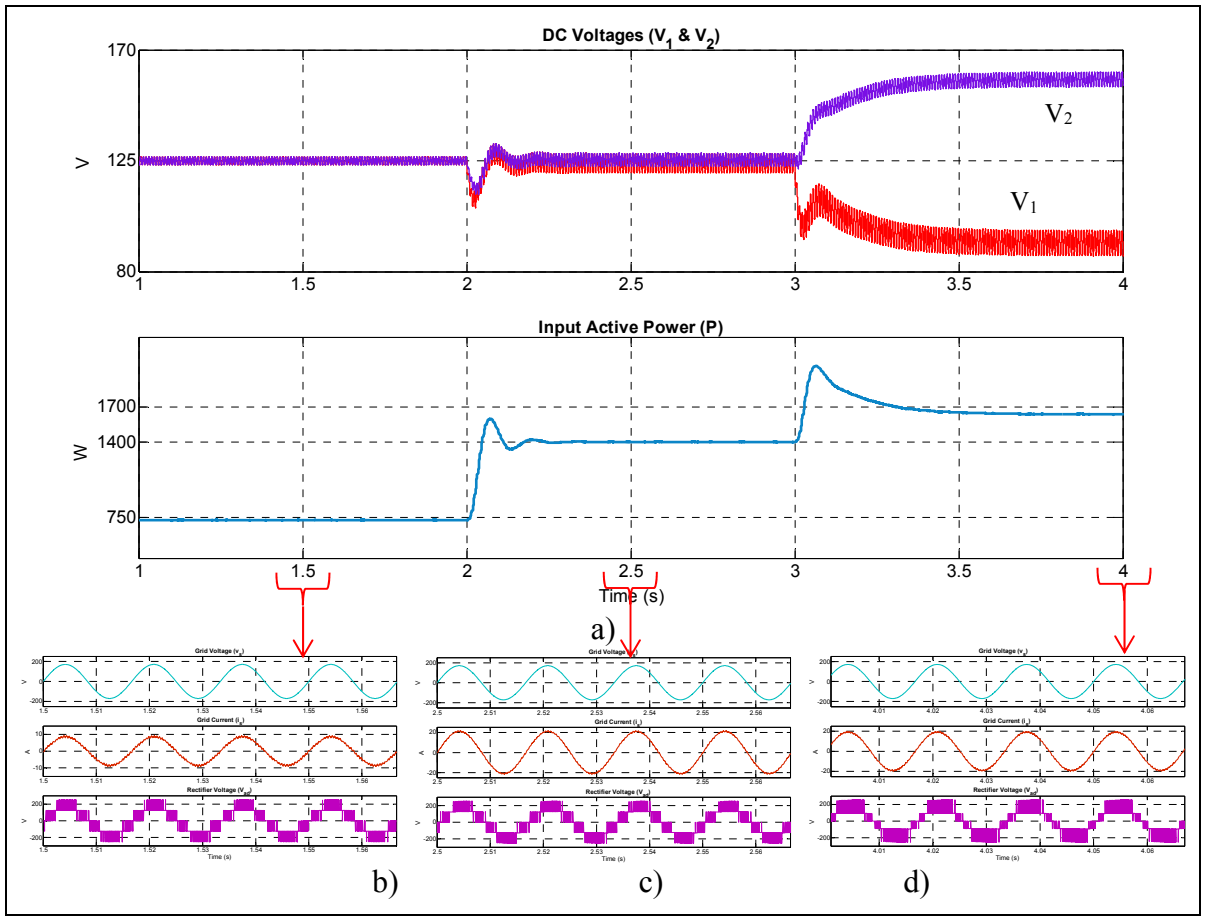

Figure 4.8 Stable and unstable operation of the proposed rectifier
a) DC voltages and input active power during changes in the loads
b) grid voltage/current and rectifier 5-level voltage when $R_1 = R_2 = 43\Omega$|
c) grid voltage/current and rectifier 5-level voltage when $R_1 = 15\Omega$ and $R_2 = 43\Omega$
d) grid voltage/current and rectifier 5-level voltage when $R_1 = 8\Omega$ and $R_2 = 43\Omega$

4.6 Experimental Results

A laboratory setup of proposed five-level buck converter has been built using 6 MOSFETS. The controller and switching technique has been implemented on dSpace1103 real-time controller with 20μs fixed sampling time to generate and send the firing pulses to turn on and off the switches. The rectifier has been connected to 120V RMS grid as real condition.

Output DC voltages have been set on 125V as buck mode operation; useable in industries to charge up batteries or in feeding telecommunication boards. Some changes are made in the operating condition such as load variation and AC source voltage fluctuation to validate the good dynamic performance of the proposed rectifier and implemented voltage regulator integrated into switching technique. All system parameters have been listed in Table 4.3.

Table 4.3 Experimental System Parameters

AC Grid Voltage	120 V RMS
AC Grid Frequency	60 Hz
Interface Inductor	2.5 mH
DC voltages (V_1&V_2)	125 V
DC Capacitors (C_1&C_2)	2500 uF
DC Load 1	53Ω
DC Load 2	80Ω
Switching Frequency	2 kHz
Current Controller Gains	$k_p = 0.8$, $k_i = 0.1$
Voltage Controller Gains	$k_p = 0.01$, $k_i = 5$

At first the steady state results are captured when the rectifier is converting 170V peak AC to 125V DC at two output terminals (in buck mode) and is supplying two loads with values mentioned in Table 4.3. All results including loads voltages/currents, grid voltage/current and rectifier input voltage in steady state is illustrated in Figure 4.9. Figure 4.9-a shows the DC loads voltages regulated at 125V with acceptable voltage ripples (measured by scope at the bottom of the photo) as buck mode of operation. Loads currents are depicted in Figure 4.9-b proportional to the DC voltages and loads impedances.

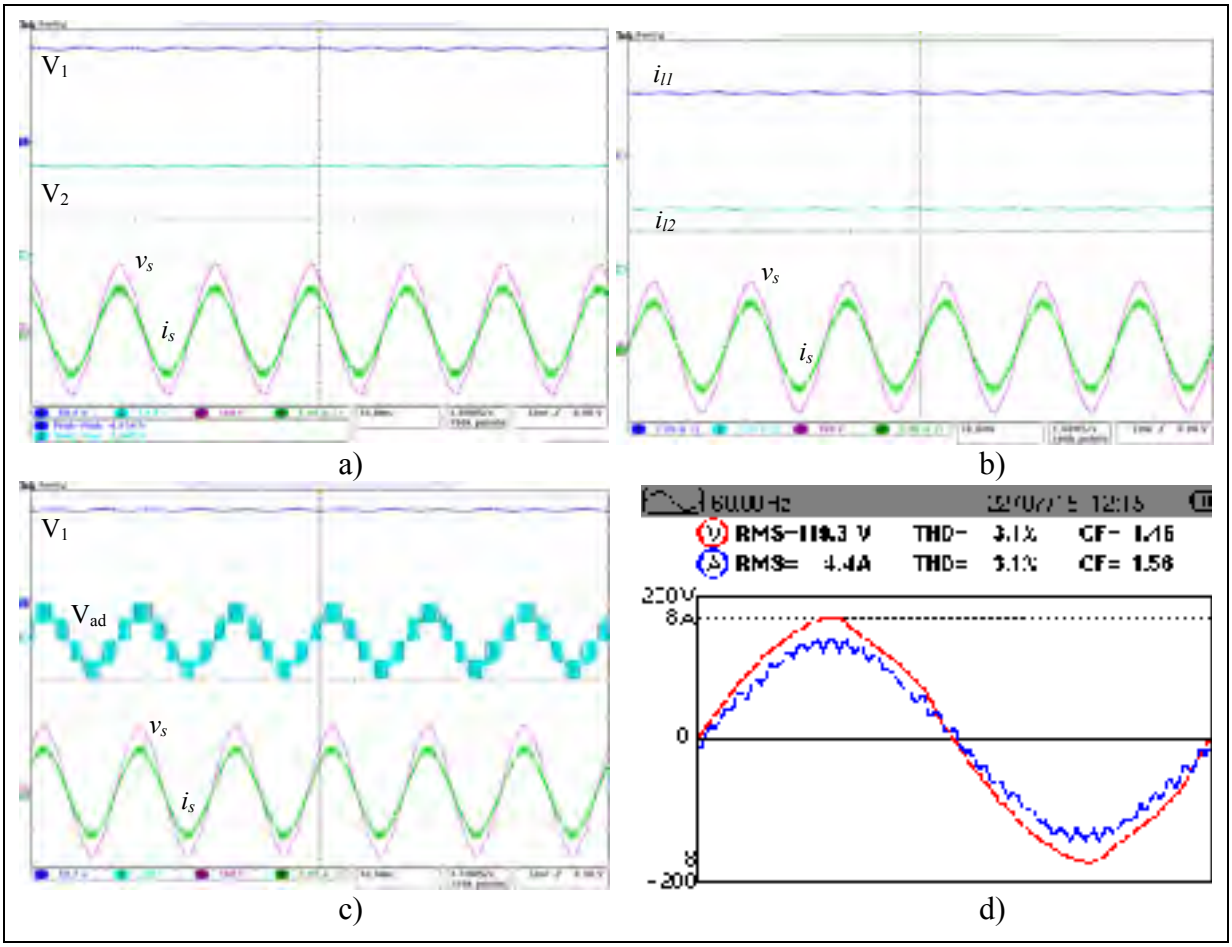

Figure 4.9 Experimental results of the proposed rectifier connected to 120V RMS AC grid and supplying two DC loads at 125V DC.
a) Output DC voltages regulated at 125V with grid side synchronized voltage and current
b) DC loads currents with grid side synchronized voltage and current
c) 5-Level voltage waveform at the input of the rectifier
d) RMS and THD values of the AC side synchronized voltage and current waveforms

Respectively, the 5-level waveform at V_{ad} is illustrated in Figure 4.9-c which is made by regulated output voltages at desired level including 0, ±125V and ±250V. Since the maximum voltage is 250V, the whole system works as boost mode while it is split into two terminals with half voltage (125V) as buck mode of operation. Low switching frequency operation (2 kHz) is clear in that figure results in low power losses and high efficiency. The main objective of this work is to demonstrate the 5-level topology performance as a multilevel buck PFC rectifier that are observed in Figures 4.9-a and 4.9-c. Finally, Figure 4.9-d has been captured by AEMC power analyzer demonstrating RMS and THD values of

the AC side voltage and current. The THD value of the current waveform is lower than standard limits while using a small inductive filter in AC line. The higher harmonic amplitude devotes to the 33rd order which is at the switching frequency (2 kHz) with 2.9% of the fundamental component. The active power delivered to the load equals to 525W and the power factor of the input AC voltage and current waveforms is almost 1 that ensures the unity power factor operation of the proposed multilevel buck rectifier with implemented voltage/current controller.

In continue, to validate the good dynamic performance of the voltage regulator integrated into switching sequences and adopted controller in driving the proposed buck PFC rectifier to supply DC loads at unity power factor, DC loads and input AC voltage are changed separately.

At first, the change has been intentionally made in Load$_1$. As it is clear from Figure 4.10, two output DC voltages and load$_2$ current (i_{l2}) do not vary during change in load$_1$. DC voltages are regulated successfully as well as DC current reduction in Figure 4.10 proves the change in load$_1$ while the second load voltage/current is not affected remarkably.

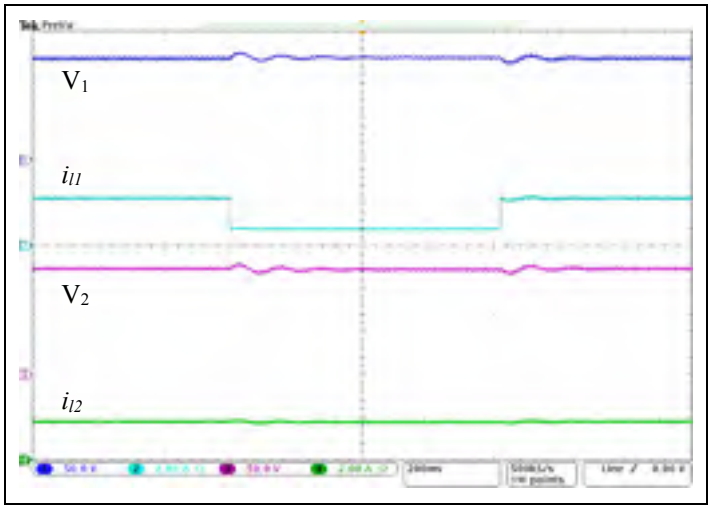

Figure 4.10 Test results during 200% increase in Load$_1$ from 53Ω to 160Ω

Similarly, a change has been made on second load to investigate the effects on the rectifier performance and the upper output DC terminal. In this case, load$_2$ is changed from 80Ω to

40Ω (50% decreases) and results are saved from both output terminals. Figure 4.11 includes captured waveforms of the load$_2$ that demonstrate changes in current during load reduction while the terminal voltage is fixed at 125V. Similar to the previous test, no effect is recorded on load$_1$ voltage/current during change in load$_2$.

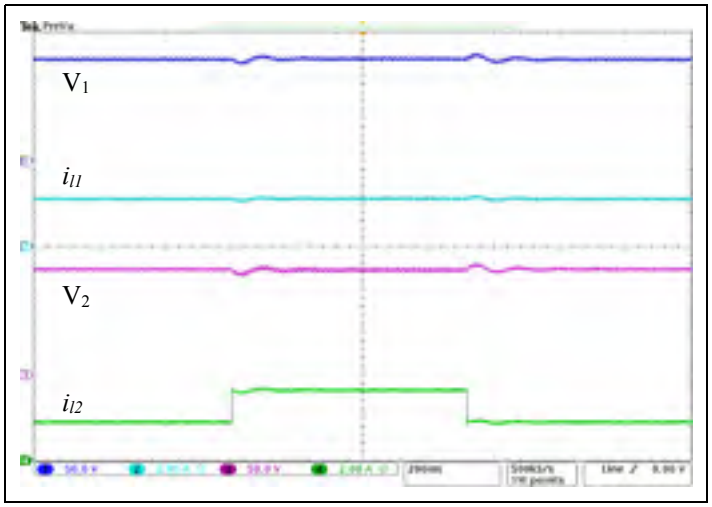

Figure 4.11 Test results during 50% decrease in Load$_2$ from 80Ω to 40Ω

Eventually, a test has been performed to validate the good dynamic performance of the proposed rectifier in unbalanced grid condition. Thus, since the rectifier is supplying loads, the input AC peak voltage is 25% increased from 162V to 200V (115V RMS to 142V RMS) and results confirm no influence on output DC voltages that are regulated at 125V DC.

Clearly seen in Figure 4.12, during change in the input AC voltage, output DC voltages are successfully kept constant at reference level (125V) forming a 5-level quasi-sine wave at the rectifier input. Moreover, the input current is slightly decreased to balance the delivered power and prevent the load over-voltage and over-current issues.

Provided results in changing conditions prove the good dynamic performance of the proposed 5-level buck PFC rectifier in generating DC voltage from AC grid. It can be concluded that the presented topology can operate as a universal PFC rectifier in buck mode of operation at low switching frequency results in low power losses and high efficiency interesting for industrial applications.

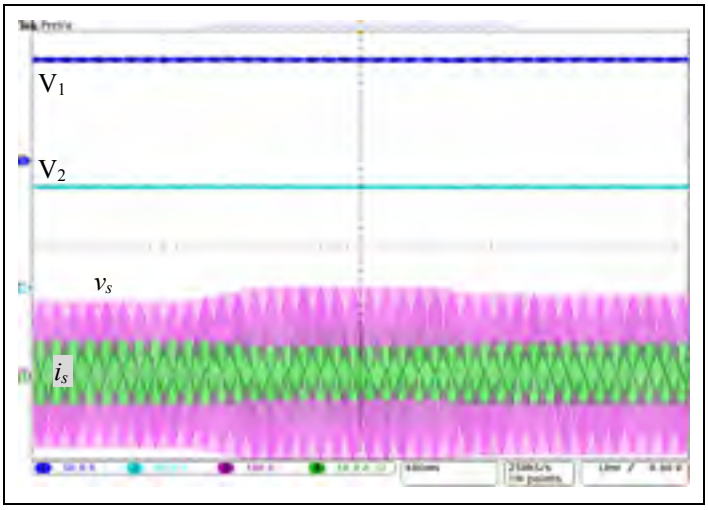

Figure 4.12 Supply voltage variation while the output DC voltages are regulated at 125V as buck mode of operation.

4.7 Conclusion

In this chapter a 5-level rectifier operating in buck mode has been proposed which is a slight modification to PUC multilevel converter. It has been demonstrated that the proposed rectifier can deceive the grid by generating maximum voltage level of 250V at AC side as boost mode while splitting this voltage value at its two output terminals to provide buck mode of operation with 125V DC useable for battery chargers or telecommunication boards' feeder. Although it has more active switches than other buck rectifier topologies and some limitations on power balance between loads, overall system works in boost mode and CCM which results in removing bulky AC and DC filters that usually used in conventional buck PFC rectifiers. Moreover, generating multilevel waveform leads to reduced harmonic component of the voltage waveform and consequently the line current. It also aims at operating with low switching frequency and small line inductor that all in all characterizes low power losses and high efficiency of the investigated rectifier. Comprehensive theoretical studies and simulations have been performed on power balancing issue of the presented rectifier. Full experimental results in steady state and during load and supply variation have been illustrated to prove the fact that presented topology can be a good candidate in a new family of buck bridgeless PFC rectifiers with acceptable performance. Future works can be devoted to developing robust and nonlinear controllers on the proposed rectifier topology.

CONCLUSION

Recently, due to significant developments in multilevel converters topologies and control methods, they have come to the industries in a vast range of applications. Those types of inverters can work in medium and high power application due to reduced price of semiconductor power switches which is growing in order to the increasing power demand in worldwide power systems. Various topologies of multilevel inverters have been studied and described. The advantages and drawbacks have been mentioned. It has been shown that among many topologies, the NPC and CHB are the popular ones which are widely used in industries. Due to exclusive structures of multilevel inverters, more switching pulses are required which makes the design of switching methods more complex and difficult to become proper for generating appropriate pulses to turn on and off the switches in a desired order. PWM and SVM have been elaborated as two mostly used switching methods. Since the most topologies use isolated DC supplies, it would be challenging to use more DC capacitor with suitable voltage controllers and less DC supplies to reduce the cost of manufacturing. Moreover, such investigation helps developing multilevel rectifier topologies based on the studied inverter ones where DC capacitors should be used to deliver active power to the DC loads.

As a brief conclusion of this thesis, it could be said that a new modeling and controller have been designed for a PUC7 inverter. Afterwards, a new operation mode of PUC inverter has been investigated resulted in emerging the new PUC5 topology. The sensor-less voltage balancing technique has been applied on the PUC5 inverter as a result of major superiority of this topology over PUC7 due to the redundancy switching states. Eventually, a modified configuration of PUC inverter has been proposed for rectifier operations. Hence, a decoupled voltage/current controller has been applied on that rectifier to generate two DC output terminals working in buck mode while the grid sees a boost rectifier that features continuous conduction mode consequently.

The comprehensive conclusion of each chapter has been collected as the following:

In chapter 1 a full literature review has been performed on multilevel inverter topologies as well as their modeling, control and switching techniques. Such study revealed the fact that single-dc-source configuration is much appreciated in the market for stand-alone or grid-connected mode of operations including numerous applications such as renewable energy conversion systems. UPS, motor drives, etc where a single DC bus is available to deliver all the energy to the other side through an inverter. Moreover, the main drawback of using too many isolated DC sources in multilevel inverter topologies (e.g. CHB) increases the cost and size undesirably. It has been also understood that multilevel inverters could be changed into rectifiers by replacing the DC sources with DC capacitors as output terminals and applying voltage and current control loops. Finally, it has been found that multilevel converters are not only used for high power applications, but also they are currently the most potential products in the market for all range of medium power applications such as residential PV inverters, small motors drives, backup UPSs, etc.

Chapter 2 contains the full modelling and controller design for a PUC7 inverter. Since the single-dc-source multilevel inverter is a matter of interest for ongoing research in this field, the previously patented PUC7 topology has been studied in detail. A new modelling has been done according to the concept of multilevel inverters switching sets and simplified to first order system. Then a nonlinear cascaded controller has been designed based on the simplified model of the PUC7 inverter to regulate the capacitor voltage at 1/3 of the DC source and generates 7 voltage levels at the output. The adopted controller requires only the existing feedback sensors of the practical system which means no additional cost of hardware implementation as a necessity of industrialization process. Moreover, the applied controller compensates the nonlinearities of the plant using some light equations without burdening the microprocessor speed significantly. The robust controller allows the PUC7 inverter to work at low and fixed switching frequency due to using PWM block which has proven advantages against reported literature using hysteresis current controller with high and variable switching frequency. Experimental results validated the good dynamic performance of the designed controller in all variable conditions like load changes or DC bus fluctuation.

The PUC5 inverter has been proposed in chapter 3 as a remedy to the PUC7 topology. It has some redundant switching states that help balancing the DC capacitor at desired level easily while the PUC7 needs complicated controller for capacitor voltage regulation. Moreover, a sensor-less voltage balancing technique has been designed and applied on PUC5 inverter to work in both stand-alone and grid-connected modes of operation by which the capacitor voltage is regulated at half of the DC source to generate 5 voltage levels at the output. Using such simple regulator ensures good performance of the proposed topology whenever the modulated reference signal is symmetric as discussed in Appendix I. The comparative study distinguished the PUC5 topology among other popular ones. It could be a real competitor full bridge converter in the market as a 5-level single-dc-source topology. Exhaustive experimental tests have been performed on the 1-phase and 3-phase configuration of PUC5 inverter and results proved the excellent performance in supplying various harmonic loads, injecting active power into the grid and exchanging reactive power with the grid. It should be mentioned that the 3-phase PUC5 inverter is able to work in both 3 and 4 wire system properly.

Chapter 4 illustrated the 5-level buck PFC rectifier as a modification to the PUC configuration to work in AC-DC mode. It features continuous conduction mode of operation due to generating boost voltage at the AC side while splitting the output terminals to generate buck mode voltage for the DC loads. It should be considered that the sum of DC voltages have to be greater than the AC supply peak amplitude. Such procedure on the AC source helps feeding DC loads with lower voltage than the grid AC peak value as buck converter while using a boost converter with inherent advantages of input harmonic suppression, requiring small passive filters, operating at low switching frequency with low power losses, etc compared to a buck converter. Since the proposed rectifier switching states include some redundancies, a decoupled voltage/current controller has been designed to balance the output DC voltages equally and to ensure unity power factor operation of the converter. A power balancing analysis has been done on the 5-level rectifier to show the limitation in supplying different loads at DC terminals. Experimental results have been demonstrated and discussed to validate the acceptable operation of the proposed rectifier and applied controller.

Future Works

This project has focused on PUC inverter topology to promote its promising advantages over reported ones. It is an initial step which could be continued for years of research. Some ideas have been summarized for future works as the following:

Extending the proposed cascaded controller on other converters

Since the proposed nonlinear cascaded controller in chapter 2 could be applied on any plants with two states of voltage and current, it could be tested on other grid-connected inverters or rectifiers especially for super-fast charger of EVs which is growing in the market significantly.

Designing other nonlinear controllers for PUC7 converter

Recently a finite set model predictive control (FS-MPC) has been designed and applied on the grid-connected PUC7 inverter successfully however featuring high and varying switching frequency. Moreover, the same controller could be implemented on rectifier mode of the PUC7.other types of controllers could be implemented on the PUC7 inverter or rectifier including sliding mode, fixed switching frequency MPC, back stepping, fuzzy, etc.

Developing new applications of PUC5 and with new design

The PUC5 topology has been only tested in inverter application. Due to its interesting features of being single-dc-source and sensor-less voltage balancing, it would be a hot topic to use it in other applications such as rectifier for battery chargers, active filter, motor drive, etc. Moreover, installing a voltage sensor and using redundant switching states helps reducing the auxiliary capacitor size significantly to couple of microfarads in a typical 3kW system studied in Appendix II. Therefore, the new design could be done considering the size of converter box using super-fast GaN devices as well.

Applying SHE or SHM techniques on 3-phase PUC5 inverter

As shown in chapter 3, the 3-phase PUC5 inverter uses only 3 isolated DC sources to generate high number of voltage levels at the output since the auxiliary capacitor is regulated easily and reliably. Thus it could be a potential replacement for conventional CHB in high power application. The SHE or SHM techniques could be applied on 3-phase PUC5 inverter to work in MW range for industrial UPS or motor drive applications with very low harmonic distortion at the output.

New applications for 5-level buck PFC rectifier

The test results of proposed rectifier showed that it could properly work with identical loads at two DC terminals. Thus, it obviously operates at no load condition which is promising for active filter and STATCOM applications.

APENDIX I

PROOF OF SELF-VOLTAGE-BALANCING IN PUC5 INVERTER

As mentioned in chapter 3, states 2 and 6 are used in PUC5 inverter in order to balance the capacitor voltage at the desired level. Those two configurations are shown in Figure-A I-1. A line inductor is used to derive the relationship between V_1 and V_2 in steady-state operation as shown by Eq. (A I-1) to (A I-10).

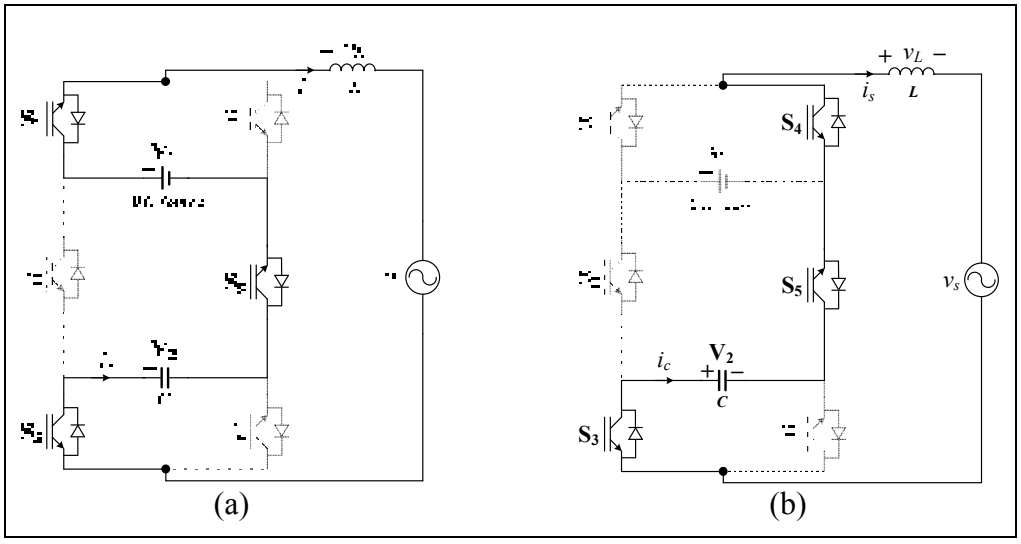

Figure-A I-1 PUC5 configuration during a) charging, and b) discharging

The capacitor current should be used to analyze its voltage balancing principle. As seen from the above figure, the current i_c equals to i_s during the switching states in which the capacitor is involved. Therefore the following equations could be written for that current:

$$i_c = i_s \tag{A I-1}$$

$$v_L = L \frac{di_s}{dt} \tag{A I-2}$$

The capacitor charge balance can be written as:

$$\int_{char.} i_s \, dt + \int_{dischar.} i_s \, dt = 0 \tag{A I-3}$$

The capacitor voltage V_2 is assumed ripple free.

For instance let us consider a charging interval of duration t_p and a discharging interval of duration t_n typically as shown in Figure-A I-2.

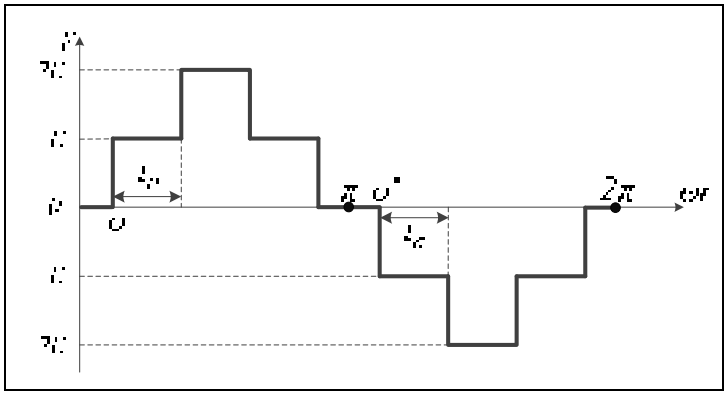

Figure-A I-2 Output 5-level voltage waveform and typical charging/discharging intervals

During the charging interval, Figure-A I-1a and Eq. (A I-2) give

$$\begin{aligned} i_s &= \frac{1}{L}\int_o^t (V_1 - V_2 - v_s)\,dt + i_{so} \\ &= \frac{V_1 - V_2}{L}\int_o^t dt - \frac{1}{L}\int_o^t v_s\,dt + i_{so} \end{aligned} \qquad \text{(A I-4)}$$

Leading to

$$i_s = \left(\frac{V_1 - V_2}{L}\right) t + i_{so} - \int_o^t v_s\,dt \qquad \text{(A I-5)}$$

During the discharging interval, and assuming the time origin is now at the beginning of this interval, Figure-A I-1b and (A I-2) give

$$\begin{aligned} i_{s'} &= \frac{1}{L}\int_{o'}^{t'} (-V_2 - v_s)\,dt' + i_{so'} \\ &= \left(-\frac{V_2}{L}\right) t' + i_{so'} - \frac{1}{L}\int_{o'}^{t'} v_s\,dt' \end{aligned} \qquad \text{(A I-6)}$$

Where, i_{so} and $i_{so'}$ are the initial currents of charging and discharging intervals, respectively. Applying the charge balance as in (A I-3), yields

$$\int_o^{t_p} i_s \, dt + \int_o^{t_n} i_{s'} \, dt' = 0 \tag{A I-7}$$

$$\frac{V_1 - V_2}{2L} t_p^2 - \frac{V_2}{2L} t_n^2 + i_{so} t_p + i_{so'} t_n - \frac{1}{L} \left[\int_o^{t_p} \left(\int_o^t v_s \, dx \right) dt + \int_o^{t_n} \left(\int_{o'}^{t'} v_s \, dx \right) dt' \right] = 0 \tag{A I-8}$$

The sinusoidal shapes of current i_S and voltage v_S, as well as symmetry in the control processed error (as shown below), imply that

$$i_{so} = -i_{so'} \quad and \quad \int_o^{t_p} \left(\int_o^t v_s \, dx \right) dt + \int_o^{t_n} \left(\int_{o'}^{t'} v_s \, dx \right) dt' = 0 \tag{A I-9}$$

Thus, the charge balance expression simplifies to

$$\frac{V_1 - V_2}{2L} t_p^2 - \frac{V_2}{2L} t_n^2 + i_{so}(t_p - t_n) = 0 \tag{A I-10}$$

Furthermore, it will be shown that, owing to the half-wave symmetry in the control signal, to every charging duration t_p corresponds an equal discharging time duration t_n.

Since the reference waveform (V_{ref}) which is sent to the modulator is a symmetric one, the charging and discharging time would be equal (due to modulating by fixed frequency and symmetric carriers). However, the following relations prove the symmetrical shape of the V_{ref}.

According to Figure 3.5, V_{ref} is a sine wave in stand-alone mode of operation imposed as open-loop system input. Therefore it has naturally a symmetric shape without requiring any proof and the output pulses of the modulator would have half wave symmetry shape with equal timing on the switching states of each half cycle.

For the closed-loop system, as grid-connected mode of operation illustrated in Figure 3.6, it should be demonstrated that the output of PI block is symmetric which is assumed as V_{ref}. As seen from that figure, the input of the PI controller is the error signal defined as Eq. (A I-11). The processing expression of a PI controller in time domain is written as Eq. (A I-12).

$$\begin{aligned} e &= i^{*} - i \\ &= a\ Sin(\omega t) - b\ Sin(\omega t) \\ &= (a - b) Sin(\omega t) \\ &= c\ Sin(\omega t) \end{aligned} \tag{A I-11}$$

$$G(PI) = k_p\ e + k_i \int e\ dt \tag{A I-12}$$

By calculating the PI output with the given input of e, the following relation is attained:

$$\begin{aligned} output\ of\ PI &= k_p c\ Sin(\omega t) + k_i \int c\ Sin(\omega t)\ dt \\ &= k_p c\ Sin(\omega t) - \frac{k_i c}{\omega}\ Cos(\omega t) \\ &= K\ Sin(\omega t - \varphi) \end{aligned} \tag{A I-13}$$

The calculated output is still a sine wave that ensures the half wave symmetry of the V_{ref}.

Considering the above effort in proving the fact the V_{ref} has half wave symmetry as sine wave, it is then obvious that the switching states 2 and 6 would have equal intervals. Going back to Eq. (A I-10), the following relation is achieved:

$$V_1 = 2V_2 \tag{A I-14}$$

So it can be concluded that the capacitor voltage tracks the half of DC source amplitude acceptably through the charging and discharging switching states (2 and 6) by applying the proposed switching technique illustrated in Figure 3.5.

APENDIX II

DESIGN CONSIDERATION OF THE PUC5 INVERTER

The PUC5 inverter is illustrated in the following figure for grid-connected applications.

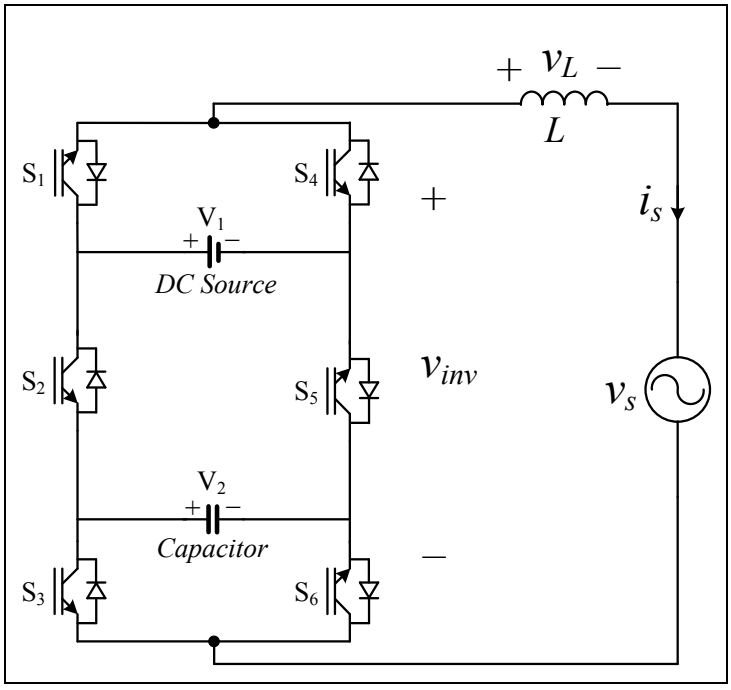

Figure-A II-1 Grid-connected PUC5 inverter

A 240V RMS 3kW system is considered as the industrial applications and the following design considerations are achieved based on. The required specifications are listed in Table-A II-1.

Table-A II-1 General Spec of the converter

AC Grid RMS Voltage	240 V RMS
AC Grid Frequency	60 Hz
Converter Rating	3 kW
DC Bus	400 V

At first step, the power switches should be chosen based on required voltage/current rating. The converter current flowing into all switches is calculated as

$$i_{s,\max} = \frac{P_{conv}}{v_{rms}} \times \sqrt{2} = \frac{3000 \times \sqrt{2}}{240} = 17.67A \quad \text{(A II-1)}$$

As it is clear from Figure-A II-1, the voltage rating of each pair of switches could be written as the following:

Table-A II-2 Voltage rating of PUC5 switches

S_1 & S_4	400V
S_2 & S_5	200V
S_3 & S_6	200V

It should be also mentioned that each pair are working in complementary so three half-bridge gate driver module could be used as interface between micro-controller and the switches to boost the gate signals properly. Moreover, the two upper switches work with line frequency while the other four ones have switching frequency as same as the PWM carrier frequency. Therefore, S_1 and S_2 could be low frequency and high voltage type of switch while the four other have higher switching frequency and lower voltage rating.

Afterwards, to design the proper inductor as grid connection filter, the following relation can be used based on a 5% current ripple (*Voltage Source Inverter Design Guide*, 2015):

$$L = \frac{V_1}{4 f_{sw} \Delta i_s} = \frac{400}{4 \times f_{sw} \times 0.05 \times 17.67} = \frac{113}{f_{sw}} \quad \text{(A II-2)}$$

One of the main advantages in using multilevel inverters is the low harmonic content of the output voltage waveform that affects the current ripple directly. This aim is also achieved at a lower switching frequency compared to a typical 2-level converter. Therefore, a 20kHz switching frequency can be set to have a 5mH inductor at the AC side.

The auxiliary capacitor can be selected according to the 5% acceptable voltage ripple.

$$i_c = C \frac{dV_2}{dt} \rightarrow C = \frac{i_c}{f \Delta V_2} \quad \text{(A II-3)}$$

The capacitor current i_c equals to line inductor current i_s in switching states where the output voltage is 200V, so Eq. (A II-2) can be recalculated to achieve the peak current at that voltage.

$$\Delta i_s = 0.05 \times i_{s,\max} = \frac{V_2}{4 f_{sw} L} = \frac{200}{4 \times 20000 \times 0.005} = 0.5A \quad \text{(A II-4)}$$
$$\rightarrow i_{s,\max} = 10A$$

Eventually, due to 120Hz voltage ripple of the capacitor, its value is obtained as

$$C = \frac{i_s}{f \Delta V_2} = \frac{10}{120 \times 400 \times 0.05} \approx 4mF \quad \text{(A II-5)}$$

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