Design and simulation of a single-phase inverter with grid support functions

by

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Conception et simulation d'un onduleur monophasé avec fonctions de support du réseau

Jean-Philippe BÉRARD

RÉSUMÉ

En réponse aux objectifs ambitieux de décarbonisation fixés à l'échelle mondiale, des efforts substantiels sont déployés afin d'électrifier de nombreux secteurs, y compris les transports, ce qui entraîne une forte augmentation de la demande en électricité. De plus, l'utilisation de combustibles fossiles comme source de production d'électricité doit également diminuer afin d'atteindre ces objectifs. Par conséquent, un nombre considérable de sources d'énergie renouvelables à zéro-émission nette de carbone sont intégrées chaque année au système électrique, dont beaucoup sont connectées via des convertisseurs à électronique de puissance. Les ressources basées sur les onduleurs comme le photovoltaïque, l'éolien et le stockage par batteries présentent de nombreux défis pour la conduite et la stabilité du réseau électrique, à tous les niveaux de tension. Pour être en mesure de palier aux impacts de la pénétration croissante de ces ressources sur le réseau, plusieurs normes d'interconnexion et des procédures de test ont été développés dans les dernières années.

Dans ce contexte, la recherche présentée dans ce mémoire porte sur un onduleur monophasé connecté au réseau basse tension pour l'interconnexion de ressources photovoltaïques à l'échelle résidentielle. Plus précisément, l'objectif est d'étudier et de concevoir un onduleur qui fournira une réponse dynamique rapide et robuste en plus d'une bonne qualité de l'onde pour une large gamme de conditions de fonctionnement. De plus, l'onduleur devra également contribuer à la stabilité du réseau grâce à l'implémentation de fonctions avancées. La théorie sous-jacente aux composants du système sera présentée et les modèles mathématiques de ces derniers seront utilisés afin de développer des procédures de conception pour le filtre de sortie et le contrôleur de courant. Le mécanisme de synchronisation au réseau et les fonctions de support avancées seront également présentés en détails. En plus de l'analyse théorique, chaque composant et le système complet seront modélisés et simulés dans l'environnement Matlab/Simulink afin de valider leurs performances. Les résultats de simulation démontreront que l'onduleur conçu respecte avec succès les critères susmentionnés.

Mots-clés: onduleur monophasé, filtre harmonique, contrôle de courant, synchronisation au réseau, fonctions avancées

Design and simulation of a single-phase inverter with grid support functions

Jean-Philippe BÉRARD

ABSTRACT

As a result of the ambitious decarbonization goals set globally, substantial efforts are put towards the electrification of many sectors, including transportation, leading to an increased demand in electricity. Meanwhile, the use of fossil fuels to generate electricity must also decrease to meet these goals. Consequently, there is a considerable number of zero-carbon renewable energy sources that are integrated to the power system every year, many of which are connected via power-electronics converters. Inverter-based resources like photovoltaic, wind power and battery storage present many challenges for the operation and stability of the electrical grid, at all voltage levels. Utilities and system operators, among others, have worked towards the development of interconnection standards and test procedures for these types of resources in order to mitigate the impact of their increasing penetration on the power system.

With regards to these challenges, this master's thesis focuses on a low-voltage grid-connected single-phase inverter for the interconnection of photovoltaic resources at the residential level. More specifically, the objective is to study and design an inverter system that will provide a fast and robust dynamic response with good power quality over a wide-range of operating conditions and also contribute to grid stability through the implementation of grid support functions. The theory behind the relevant inverter system components will be discussed and their respective mathematical models will be presented in order to develop design procedures for the output filter and current controller. Furthermore, the implementation of a grid synchronization mechanism and grid support functions will be presented. In addition to theoretical analysis, every component and the resulting system will be modeled and simulated in the Matlab/Simulink environment to validate their performance. Simulation results will demonstrate that the designed inverter successfully complies with the aforementioned criteria.

Keywords: single-phase inverter, output filter, current controller, grid synchronization, grid support functions

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LIST OF ABBREVIATIONS

AC	Alternating current
CPF	Constant power factor
DC	Direct current
FFT	Fast Fourier transform
FW	Frequency-Watt
GHG	Greenhouse gasses
GM	Gain margin
IDM	Islanding detection method
IEEE	Institute of electrical and electronics engineers
MPP	Maximum power point
MPPT	Maximum power point tracking
NPC	Neutral point clamped
P&O	Perturb and observe
PF	Power factor
PI	Proportional-integral
PLL	Phase-locked loop
PM	Phase margin
PoC	Point of connection
PR	Proportional-resonant

p.u.	Per unit
PV	Photovoltaic
PWM	Pulse-width modulation
ROCOF	Rate-of-change-of-frequency
RMS	Root mean square
SCR	Short-circuit ratio
SFS	Sandian frequency shift
SPWM	Sinusoidal pulse-width modulation
THD	Total harmonic distortion
VCO	Voltage-controller oscillator
VRT	Voltage ride-through
VVAR	Volt-VAR

LIST OF SYMBOLS AND UNITS OF MEASUREMENTS

A	Ampere
C	LCL filter capacitor
C_{base}	LCL filter base capacitance
c_f	SFS chopping factor
c_{f_0}	SFS chopping factor at fundamental frequency
D	Duty cycle
dB	Decibel
db_{of} and db_{uf}	Over and under-frequency deadband
f_c	Inverter system loop gain crossover frequency
f_o	Nominal grid frequency
f_{res}	Filter resonant frequency
f_{sw}	Inverter switching frequency
G_i	Current controller transfer function
G_{PR}	PR controller transfer function
H_{i1}	Capacitor current feedback gain
H	Henry
H_{PLL}	PLL closed-loop transfer function
Hz	Hertz
$I-V$	PV Current-voltage characteristic

I_0	PV cell diode saturation current
I_1	Inverter output fundamental RMS current
i_2	Inverter/Filter output current
i_{2D}	Inverter output current disturbance transfer function
i_{2D}	Inverter output current tracking transfer function
i_C	Filter capacitor branch current
I_d	PV cell diode current
I_L	PV cell light-generated current source
I_p	Active power current component
I_q	Reactive power current component
I_{ref}	Current reference amplitude
J	Joule
k	Boltzman constant
K	SFS acceleration factor
K_ip	Active power controller integral gain
K_iq	Reactive power controller integral gain
$K_{i_{PLL}}$	PLL loop filter integral gain
K_n	Notch filter gain at the notch frequency
k_{of} and k_{uf}	Over and under-frequency droop coefficients
K_P	PR controller proportional gain

K_pp	Active power controller proportional gain
K_pq	Reactive power controller proportional gain
$K_{p_{PLL}}$	PLL loop filter proportional gain
K_{PWM}	Transfer function between the modulating signal and the inverter output voltage
K_r	PR controller resonant gain
λ_C	Ratio of reactive power induced by the filter capacitance
λ_h	Current harmonic ratio
λ_n	Notch filter damping ratio
λ_{rip}	Current ripple ratio
L_1	LCL filter inverter-side inductor
L_2	LCL filter grid-side inductor
L_g	Equivalent grid inductor
m^2	Square meter
n	Diode ideality factor
$P-V$	PV power-voltage characteristic
P_{avail}	Available active power
P_{inv}	Inverter output active power
P_{min}	Minimum allowed active power
P_{nom}	Inverter nominal active power
P_{pre}	Pre-disturbance active power

P_R	Load active power
P_{ref}	Active power reference
q	Charge of an electron
Q_C	Load capacitive reactive power
Q_f	Load quality factor
Q_{inv}	Inverter output reactive power
Q_L	Load inductive reactive power
Q_{ref}	Reactive power reference
rad	Radian
R_s	PV cell series resistor
R_{sh}	PV cell parallel resistor
s	Second
S_{nom}	Inverter nominal apparent power
S_{PoC}	Short-circuit power at the PoC
T	Inverter system loop gain
T_{f_o}	Inverter system loop gain at fundamental frequency
T_{LCL}	LCL filter transfer function
T_o	Period of the grid voltage at nominal frequency
T_{SFS}	Period of the SFS modified current reference
T_{sw}	Switching period

t_z	SFS dead-time
V	Volt
v_c	Voltage across LCL filter capacitor
V_d	Voltage across the PV cell diode
V_{DC}	DC-link voltage
V_g	Nominal voltage at the inverter PoC
V_h	Dominant harmonic voltage
V_{inv}	Inverter output voltage
V_{ref}	Voltage reference
V_s	Grid voltage
V_T	PV cell thermal voltage
V_{tri}	PWM carrier amplitude
ω_g	Grid angular frequency
ω_h	Dominant harmonic angular frequency
ω_i	PR controller resonance angular frequency bandwidth
ω_n	Notch filter notch angular frequency
ω_o	Nominal grid angular frequency
ω_{PLL}	PLL estimated angular frequency
ω_r	PR controller resonance angular frequency
W	Watt

Z_{base}	Filter base impedance
Z_C	Filter capacitor impedance
Z_g	Equivalent grid impedance
Z_{L1}	Filter inverter-side inductor impedance
Z_{L2}	Filter grid-side inductor impedance
Z_{LCL}	Total filter impedance

INTRODUCTION

With the constant growth in global population, the economical development in emerging countries and the electrification of many industries comes an ever-increasing energy demand. A large proportion of the global energy consumed stems from fossil fuels which contributes to the emission of greenhouse gasses (GHG), proved to be a catalyst to climate changes. Facing the impacts of these changes, governmental entities throughout the world have committed to reduce their GHG emissions. In particular, the government of Canada has expressed its intention to reach net-zero emissions by 2050 and more aggressively a net-zero electrical grid by 2035. Obviously, the adoption of renewable energy resources is at the center of the solution to reach this goal. In fact, Canada Energy Regulator expects the photovoltaic (PV) capacity in the country to increase by 600% by 2050 (Canada Energy Regulator, 2020), driven primarily by these environmental policies.

In recent years, a globally growing adoption of PV generation technology was observed on various scales, even at the residential level. With many manufacturers working on improved efficiency as well as smaller footprints, these systems become a good solution particularly to meet peak demand and hence reduce energy consumption from the grid. In Quebec specifically, a mere total of 6.25 MW of photovoltaic power capacity was installed at the end of 2019 (Baldus-Jeursen, Poissant, Gall & Mckay, 2020). It is estimated that a total photovoltaic power output average of 1300 MWh is available in the south of the province (Solargis, 2022) and Hydro-Québec has already expressed its desire to expand its PV power capacity. However, this decentralized energy production inevitably impacts the distribution system to which it is connected, especially if it is allowed to inject current to the grid, i.e. reverse the power flow.

In order to mitigate the impacts of inverter-based distributed energy ressources on the grid, interconnection standards were created to define requirements that these systems must comply with. Originally, the standards required that inverters disconnect from the grid when any

disturbance was observed. However, when a larger portion of the power in an area is generated from inverter-based resources, this behaviour is less than desirable and can even exacerbate the disturbances and lead to power outages. This is demonstrated notably in the analysis of the well-known Blue Cut Fire event in Southern California, during which 1200 MW of PV power was lost as a consequence of disconnection in response to indirect voltage and frequency disturbances (NERC, 2017). Nowadays, the interconnection standards define guidelines for the inverters to be able to ride-through voltage and frequency disturbances and, furthermore, to implement grid support functions such as voltage and frequency support through active and reactive power.

Within this context, the objective of this thesis is to demonstrate the effectiveness of these grid support functions through the design and simulation of a residential scale single-phase grid-connected inverter that is compliant with these standards. More specifically, the designed inverter must comply with the following requirements:

1. Have good dynamic performance.
2. Provide appropriate power quality, i.e. low output current distortion.
3. Remain stable over a wide range of equivalent output impedance at the point of connection.
4. Ride-through under- and over-voltage events.
5. Support grid voltage and frequency through advanced active and reactive power control.

The thesis is structured in five chapters. Chapter 1 provides an overview of the inverter system under study and introduces each of its components through a literature review. Chapter 2 details the theory behind the inverter output filter and proposes a design procedure for it. The grid-connected inverter mathematical model is presented in Chapter 3 and it is used to develop a design procedure for the current controller. Chapter 4 describes the phase-locked loop used to synchronize the inverter to the grid. Finally, Chapter 5 presents the implemented grid support

functions. For every designed component presented in these chapters, simulation models are developed and used to test and validate their performance.

CHAPTER 1

SYSTEM OVERVIEW

The objective of this first chapter is to provide an overview of the inverter system under study and a brief description of its main components, their functions and underlying concepts with references to relevant publications that were consulted during the literature review. Extensive research has been conducted on the subject in the last few decades in order to improve the cost, efficiency and performance of these systems, leading to a wide variety of inverter topologies and control algorithms. However, for clarity purpose, the focus will be put on the selected topology that represent commonly available residential scale systems.

1.1 Inverter topology

The high-level inverter system topology as described in the next sections is presented in the diagram of Figure 1.1 for reference.

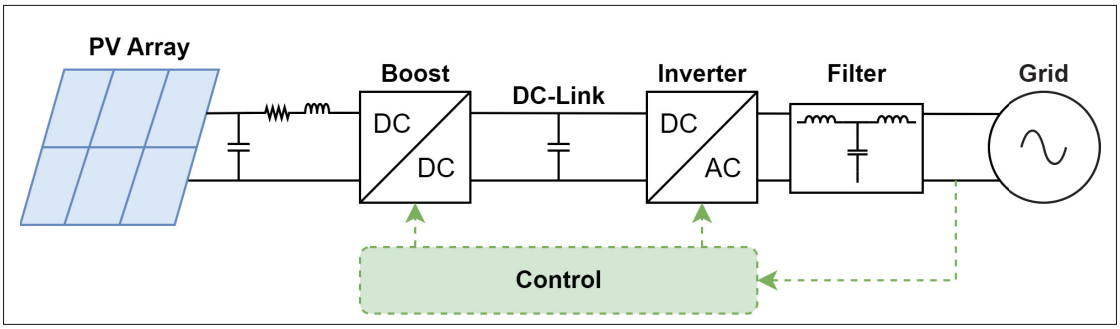

Figure 1.1 Single-phase grid-connected inverter and PV converter system structure

1.2 Photovoltaic module

The first component of the system is the electrical source, namely a solar panel or PV module. It is composed of a multitude of PV cells which convert the solar light energy into electrical current. These cells are composed of multiple layers of various materials, including positively

(p-type) and negatively (n-type) charged semiconductor layers that, when assembled, create a p-n junction. Naturally, electrons from the n-type layer will move across the junction to the p-type layer and inversely, holes from the p-type layer to the n-type layer, creating an electric field in a fine region at the junction called the space charge region. It opposes the movement of electrons and holes from occurring in this direction and only allows electrons to move from the p-type to the n-type layer. When light reaches the semiconductor layers, part of the radiant energy from the photons is transferred to electrons which become excited. These electrons eventually detach from the material valence band and reach the conduction band where they can move freely to the other layer. This movement of electrons is what constitutes an electrical current, which is captured by placing conductive surfaces on each side of the layers to create a circuit.

The electrical behaviour of a PV cell can be modeled with the equivalent circuit known as the single diode model (Bose, Szczesny & Steigerwald, 1985), (Hsiao & Chen, 2002), shown in Figure 1.2. It comprises the light-generated current source I_L, a diode, a parallel resistor R_{sh} and series resistor R_s. The current-voltage (I-V) characteristic of a diode is expressed by the Shockley equation (1.1) as:

$$I_d = I_0 \left[\exp\left(\frac{V_d}{V_T}\right) - 1 \right] \tag{1.1}$$

Where I_d is the diode current, I_0 is the diode saturation current, V_d is the voltage across the diode and V_T is the thermal voltage which is expressed by equation (1.2):

$$V_T = \frac{kT}{q} n \tag{1.2}$$

Where k is the Boltzman constant ($1.381 \cdot 10^{-23}$J/K), q is the charge of an electron ($1.6 \cdot 10^{-19}$C), T is the cell temperature in degrees Kelvin and n is the diode ideality factor.

Referring to Figure 1.2 and equations (1.1) and (1.2), the PV cell I-V characteristic can be expressed with equation (1.3):

$$I = I_L - I_0 \left[\exp\left(\frac{V + IR_s}{nV_T} \right) - 1 \right] - \left(\frac{V + IR_s}{R_s h} \right) \tag{1.3}$$

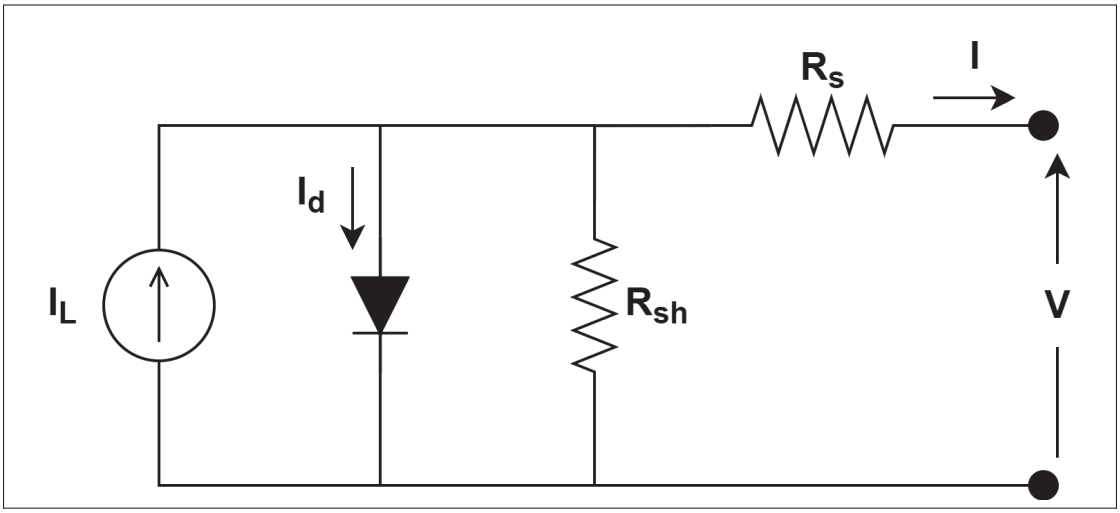

Figure 1.2 Single diode model of a PV cell

It can be seen, from the non-linear equation (1.3), that a PV module I-V characteristic is not only influenced by its internal characteristics expressed by the equivalent resistors but also by external factors like the temperature, impacting V_T, and the solar irradiance, measured in W/m^2 and impacting the amount of light-generated current I_L. A PV array is built by assembling and connecting multiple PV modules in series, resulting in a higher output voltage, and/or in parallel, resulting in a higher output current level. The current-voltage and power-voltage (P-V) characteristics of a PV array composed of 12 parallel strings of 4 series modules are shown in Figure 1.3 as an example for 3 different solar irradiance levels.

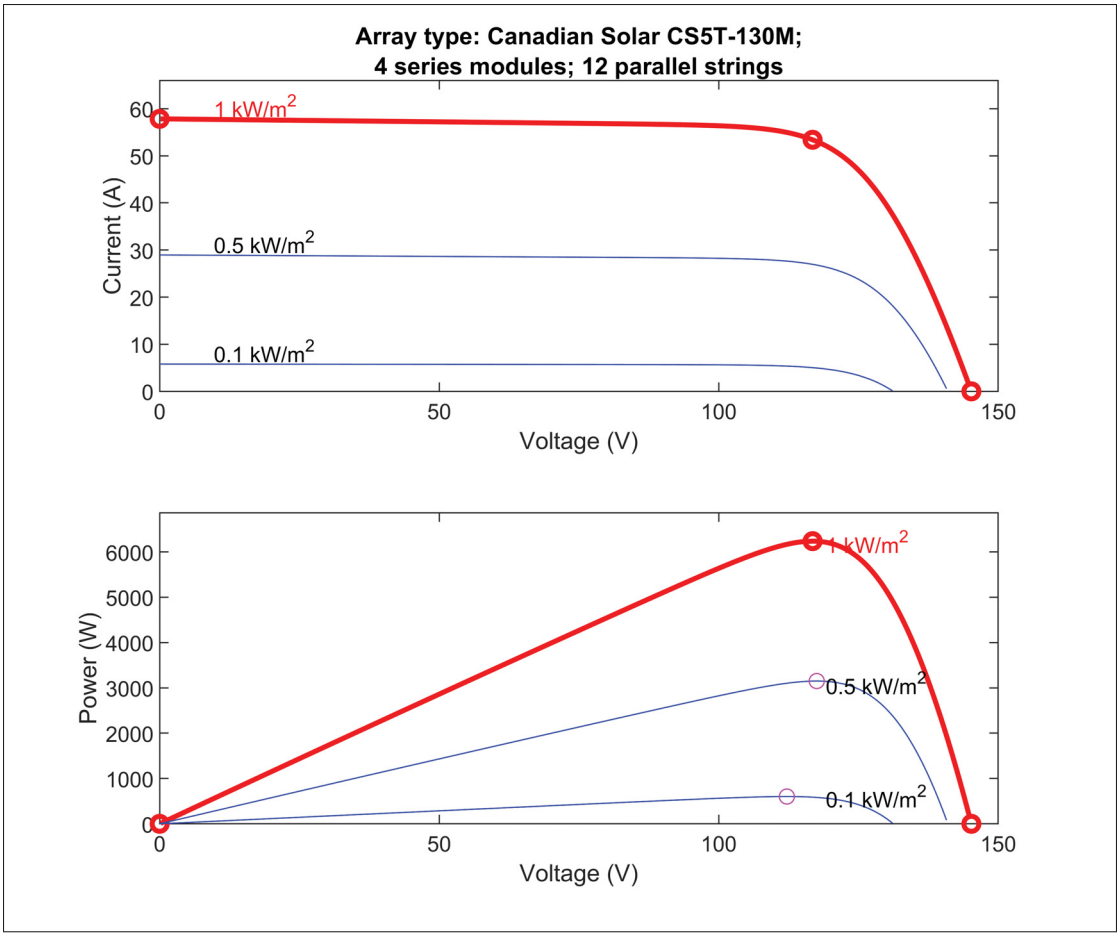

Figure 1.3 PV array I-V and P-V characteristics

From Figure 1.3, it can be observed that for every irradiance level, a PV array has an optimal operating point where the maximum current and hence power is available. This operating point is called the Maximum Power Point (MPP). A control algorithm, commonly called the Maximum Power Point Tracking (MPPT), is used by the converter connected to the PV array output presented in section 1.3 to seek the MPP and set the output voltage to the required value to extract the maximum available power. Multiple MPPT algorithms were developped to obtain the highest efficiency possible (Kamarzaman & Tan, 2014) under various conditions like rapid solar irradiance variations or partial shading. For the work presented herein, the well-known perturb and observe (P&O) MPPT (Wasynezuk, 1983) is used. It tracks the MPP continuously

by slightly increasing or decreasing the operating voltage and comparing the resulting output power with the previous operating point.

1.3 Two-stage converter

The main purpose of the power electronics based inverter is to convert the direct current (DC) power from the PV array to alternating current (AC) power synchronized with the grid. This process can be achieved with a single or multiple power conversion stages, leading to various converter topologies as shown in (Ali Khan, Liu, Yang & Yuan, 2020). With single-stage inverters (Mohammad Noor, Omar, Mahzan & Ibrahim, 2013), the conversion from DC to AC as well as the MPPT are all integrated in a single power conversion stage. However, this topology usually provides lower power quality and reduced power capacity. For this thesis, a two-stage converter is used as shown in Figure 1.1. The first stage consists of a DC/DC buck-boost converter which boosts the PV array output voltage and contains the MPPT algorithm to track the MPP and extract the maximum available power. It is connected to the second stage, namely the DC/AC inverter, through the DC-link which uses a parallel high-capacitance for power decoupling and voltage fluctuations filtering purposes.

It should be noted that a small LC filter is used between the PV array and the converter to filter out small voltage fluctuations and produce a more stable DC voltage. The buck-boost used herein is simulated as an average model, i.e. a switching-function model directly controlled by the duty cycle signal which is the output of the MPPT and follows relationship (1.4):

$$D = \frac{V_{out}}{V_{out} - V_{in}} \tag{1.4}$$

Where D is the buck-boost duty cycle, V_{out} is the output voltage and V_{in} is the input voltage.

The second stage, namely the DC/AC inverter, can also be implemented with multiple different topologies as demonstrated in (Teodorescu, Liserre & Rodriguez, 2011) where two main categories are derived, namely the neutral point clamped (NPC) and H-bridge or Full-bridge

inverters. The latter one is the topology used in this thesis. It converts the DC power to a sinusoidal waveform by controlling the switching of 4 semiconductor switches as detailed in Chapter 2.

1.4 Pulse-width modulation

A modulation process is required in order to control the states of the inverter semiconductor switches and convert the input DC voltage, V_{DC}, into a pulse width modulated square wave that will result in the desired sine wave after filtering. Numerous pulse-width modulation (PWM) techniques were developed to control different topologies of power electronics converters and to improve their power quality (Holmes & Lipo, 2003). Sinusoidal Pulse-width modulation (SPWM) techniques are used to generate the pulses applied to the gates of the inverter power electronic switching devices by comparing a reference sinusoidal modulation signal to a triangular carrier. Two main types of SPWM techniques are typically used to control single-phase full-bridge inverter topologies like the one presented herein, namely the bipolar and unipolar SPWM. A detailed explanation of these techniques will be given in Chapter 2.

1.5 Output filter

A low-pass filter consisting of passive elements is used at the output of the inverter in order to mitigate the harmonics induced by the switching of the power electronics converter and hence, provide a high-quality current waveform. The filter is required to provide a strong attenuation in the frequency range of the switching to limit the harmonics magnitudes and the total harmonics distortion (THD) within the constraints established in IEEE Std 519-2014 (IEEE, 2014) and IEEE Std 1547-2018 (IEEE, 2018). The most common topologies are L, LC and LCL filters. However, it has been demonstrated that, although its design is more complex, the LCL filter provides higher attenuation with smaller passive elements (Cha & Vu, 2010) compared to other topologies. It allows to use a lower switching frequency, reduces the size and cost of the filter passive components and provides better decoupling from the grid impedance (Behera, Behera,

Majhi & Akram, 2018). Based on these advantages, it is the topology selected for the present work. Chapter 2 presents the theory and design procedure of the inverter output filter.

1.6 Inverter synchronization

In order to connect and interface with the grid, the inverter system must be able to synchronize its output with the grid voltage. This synchronization is not only required for the stable operation of the inverter but also to properly control the active and reactive power exchange. The grid voltage frequency and phase angle information is used in every inverter control layer, from the inner current control loop as described in Chapter 3 to the outer power control loops and the implementation of grid support functions detailed in Chapter 5. To extract this information from the measured grid voltage, a phase-locked loop (PLL) is used (Best, 2003). The PLL is a control system that can track a sinusoidal signal at its input by controlling and minimizing the error in the phase of its output signal, hence providing the necessary frequency and phase angle measurements. The detailed design and implementation of the phase-locked loop to synchronize the inverter to the grid is presented in Chapter 4.

1.7 Current controller

As previously stated, the grid-connected inverter should inject high-quality current to the grid and remain stable over a wide range of equivalent grid impedance. Furthermore, it should have a good immunity to grid disturbances such as voltage and frequency deviations and provide a fast response to setpoint variations and grid conditions. A well designed current controller is of utmost importance in order to ensure that these criteria are met.

A wide variety of current control schemes exist, ranging from traditional linear proportional-integral (PI) controllers to more advanced and complex model predictive based controllers (Hu, Zhu & Dorrell, 2013). For the work presented hereby, it is desirable to select a method that can be well analyzed, yet provides a good performance and compliance to aforementioned criteria.

Although it is straightforward to implement, a PI controller has well documented disadvantages, including a limited disturbance rejection capability. Existing methods to alleviate this problem include the use of a grid voltage feed-forward path in the current control loop. However, this solution can lead to even more problems when the inverter is connected to a weaker grid. Indeed, the presence of harmonics in the grid voltage would be reflected and possibly amplified in the output current, leading to deteriorated power quality (Xu, Xie & Tang, 2013) and hence non-compliance of the inverter to the aforementioned interconnection standards. Another limitation of the PI controller, when used in the natural reference frame, is in its capability to properly track a sinusoidal reference, leading to steady-state errors in the output current amplitude and phase, which prevents precise control of the power factor.

Alternatively, Proportional-resonant (PR) controllers have been extensively studied for single-phase voltage-source converters applications (Zmood & Holmes, 2003) (Teodorescu, Blaabjerg, Liserre & Loh, 2006) and were proven to overcome the challenges previously mentioned with PI controllers. The main characteristic of the PR controller is that its resonant pole allows to achieve a large gain at the resonant frequency. By setting this resonance at the grid nominal frequency, it provides accurate reference tracking in the natural reference frame without steady-state error. It is the controller selected for the work presented herein. Its characteristics and a detailed design procedure are presented in Chapter 3.

1.8 Grid support functions

With the increasing adoption and penetration of inverter-based distributed energy resources in electric grids, it is desirable that the inverters implement advanced functions to mitigate their impact and even contribute to the grid stability. Interconnection standards such as the IEEE Std 1547-2018 (IEEE, 2018) provide the interconnection, functional, and interoperability requirements for inverter-based distributed energy resources. As opposed to past versions of the standards where it was required that inverters cease to energize and trip when disturbances occurred on the grid, it is now required that they not only ride-through voltage and frequency excursions but also support the grid voltage and frequency through the control of their active

and reactive power output. These requirements will be cited throughout this thesis and used as the basis to evaluate the designed inverter performance. Grid support functions and their implementation will be described in Chapter 5.

1.9 Designed system parameters

Table 1.1 summarizes the inverter system parameters considered for the work presented herein. The selected values are representative of typical residential single-phase inverters that would be connected to a low-voltage distribution grid in North-America.

Table 1.1 Inverter system parameters

Parameter	**Symbol**	**Value**
Grid voltage	V_s	240V RMS
Grid frequency	f_o	60Hz
Nominal active power	P_{nom}	5kW
DC link voltage	V_{DC}	440V
PWM carrier amplitude	V_{tri}	6.5V
Switching frequency	f_{sw}	20kHz

1.10 Conclusion

To summarize, this chapter provided an overview of the inverter system under study. The high-level topology of the single-phase grid-connected inverter used herein was presented and each of its fundamental components and their respective functions were described. The work presented in this thesis will focus mainly on the design and simulation of the output filter, current controller, phase-locked loop and grid support functions, which are the subjects of the following chapters.

CHAPTER 2

OUTPUT FILTER

As mentioned in Chapter 1, a filter is required at the inverter output in order to mitigate the harmonics caused by the switching of semiconductor switches and hence provide a high-quality current waveform. This chapter presents the theory behind the LCL filter used herein and the developed design procedure, which is adapted from the one proposed in (Ruan, Wang, Pan, Yang, li & Bao, 2017).

2.1 SPWM techniques

First and foremost, to understand the need and role of the inverter output filter, it is important to present the most common SPWM techniques used for single-phase grid-connected inverters using a full-bridge converter topology, as shown in Figure 2.1, along with their respective waveforms.

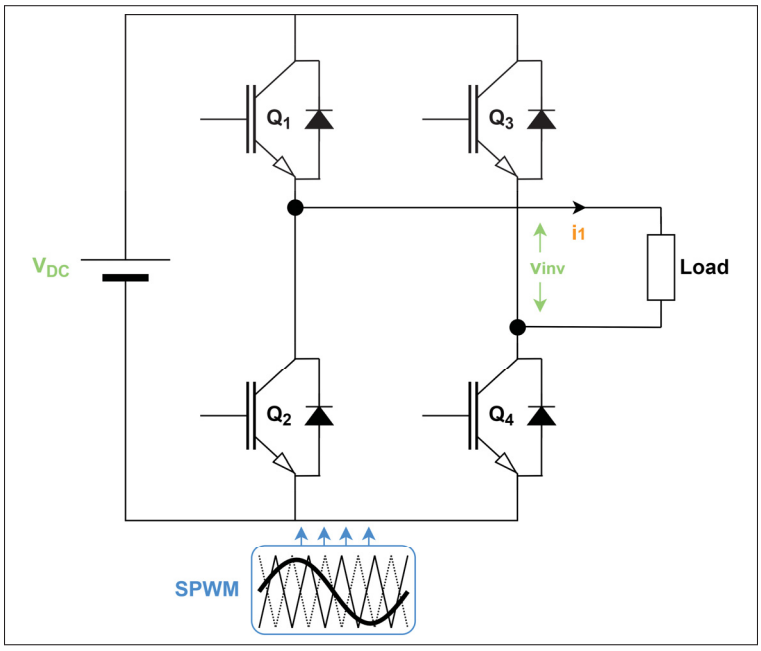

Figure 2.1 Full-bridge converter diagram

2.1.1 Unipolar SPWM

The unipolar SPWM allows three different voltage levels at the inverter output: $-V_{dc}$, $+V_{dc}$ and 0. To do so, the modulation signal v_m is compared to two triangular carriers, $+V_{tri}$ and $-V_{tri}$, with a phase shift of 180° as shown in Figure 2.2. The pulses are generated following relationship (2.1).

$$
\begin{aligned}
v_m > +v_{tri} \Rightarrow \begin{cases} Q_1 = ON \\ Q_2 = OFF \end{cases} \qquad & v_m < +v_{tri} \Rightarrow \begin{cases} Q_1 = OFF \\ Q_2 = ON \end{cases} \\
v_m > -v_{tri} \Rightarrow \begin{cases} Q_3 = OFF \\ Q_4 = ON \end{cases} \qquad & v_m < -v_{tri} \Rightarrow \begin{cases} Q_3 = ON \\ Q_4 = OFF \end{cases}
\end{aligned}
\tag{2.1}
$$

The unipolar PWM technique induces harmonics in the output voltage at around twice the carrier frequency. This particularity is advantageous for the design of the output filter since it allows the use of smaller passive components to mitigate the PWM-induced harmonics. It is the technique employed in the design of the inverter presented herein.

2.1.2 Bipolar SPWM

As opposed to the unipolar SPWM, the bipolar SPWM allows only two different voltage levels at the inverter output: $-V_{dc}$ and $+V_{dc}$. In this case, and as illustrated in Figure 2.3, the modulation signal is compared to a single triangular carrier and the pulses are generated following relationship (2.2).

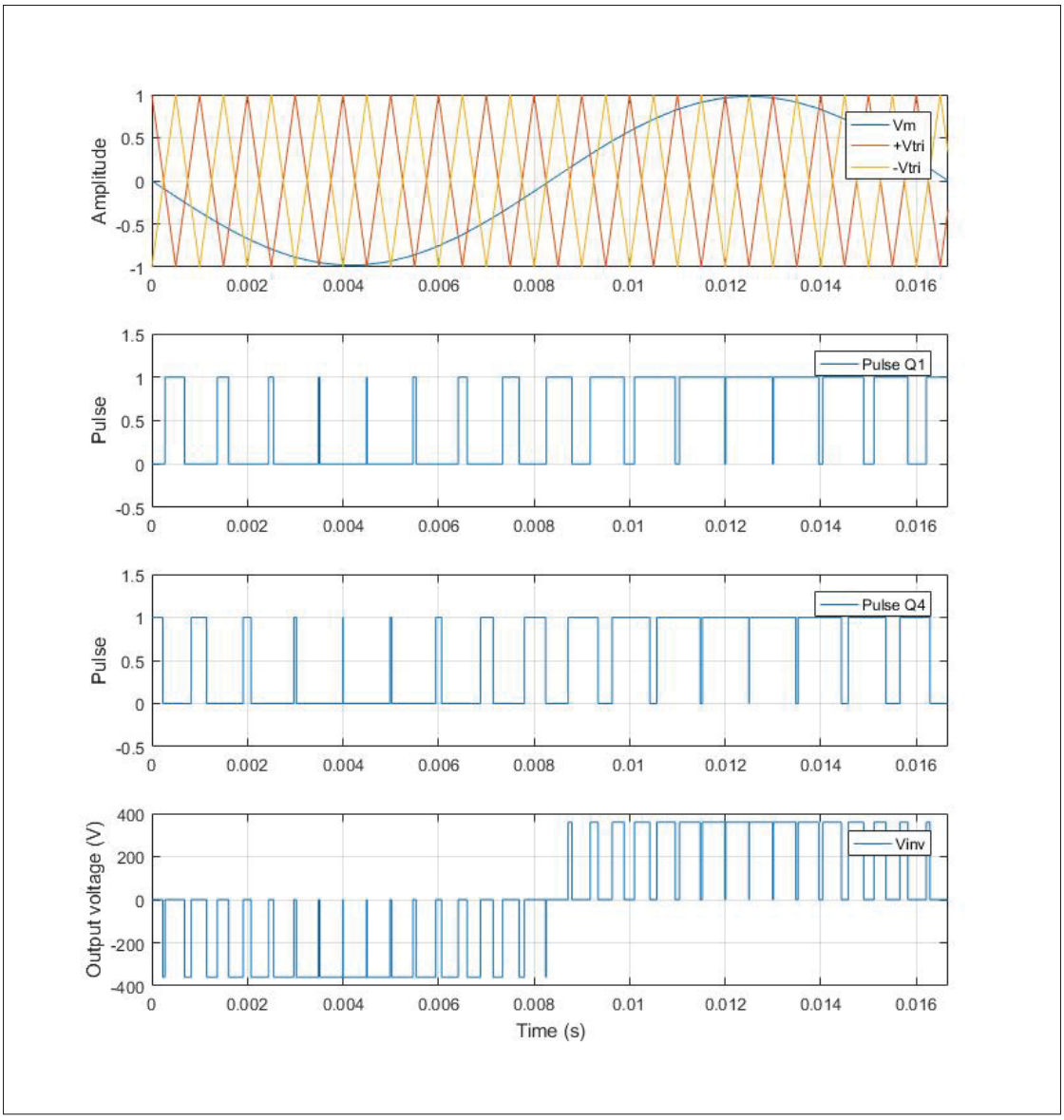

Figure 2.2 Unipolar SPWM waveforms

$$v_m > v_{tri} \Rightarrow \begin{cases} Q_1 = Q4 = ON \\ Q_2 = Q3 = OFF \end{cases} \qquad v_m < v_{tri} \Rightarrow \begin{cases} Q_1 = Q4 = OFF \\ Q_2 = Q3 = ON \end{cases}$$

(2.2)

The bipolar SPWM technique induces dominant harmonics in the output voltage at and around the carrier frequency.

As illustrated in Figure 2.2 and 2.3, the resulting inverter output voltages are series of pulses with high harmonic content. It is obvious that a low-pass filter must be used to limit this harmonic content to an acceptable level in the injected grid current. It is important to note that the dead-times, which are small time delays inserted before the PWM rising-edges, are not considered for the work herein.

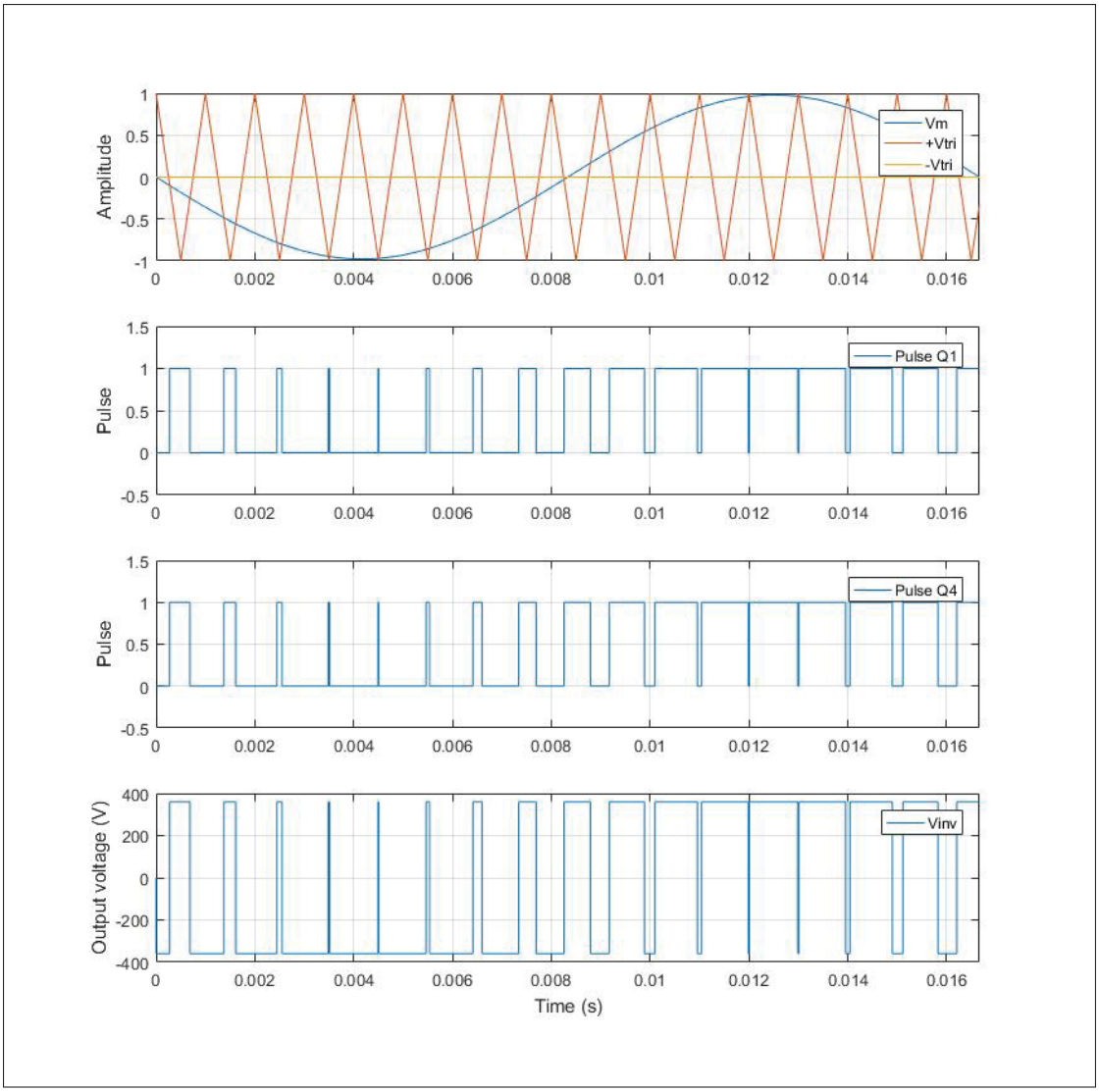

Figure 2.3 Bipolar SPWM waveforms

2.2 Filter design procedure

Although it provides many advantages compared to other topologies, the LCL filter illustrated in Figure 2.4 is more complex to design. In order to alleviate this issue, an automated design procedure composed of scripts and models is developed in the Matlab/Simulink environment. It allows to use an iterative test for multiple passive components or system parameters combinations and to validate the resulting filter performance in very little time. The overall design procedure is presented in Figure 2.5 and the developed scripts and models are presented in Appendix I.

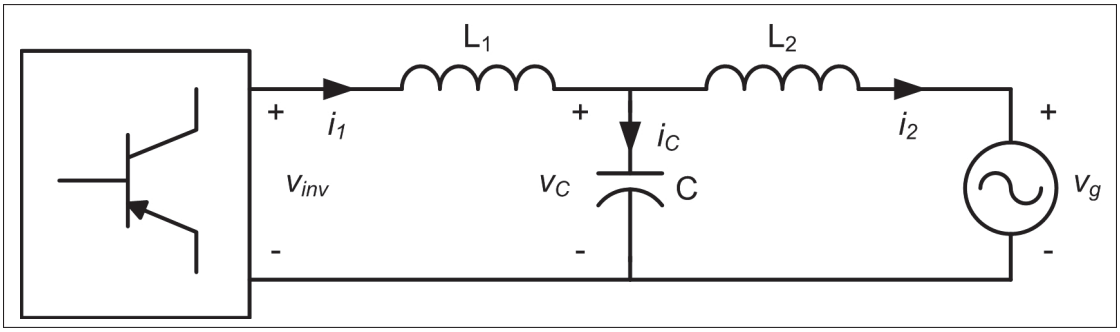

Figure 2.4 LCL filter

The first step of the procedure is to define the inverter system parameters, namely the nominal output (grid) RMS voltage, rated active power, DC link voltage, grid frequency, switching frequency and SPWM technique, as well as the desired filter performance metrics, namely the maximum current ripple coefficient and percentage of reactive power introduced by the capacitor. Once these parameters are defined, mathematical expressions for the extremum values of each filter passive component, presented in the following sections, are evaluated automatically and provide acceptable ranges to select from. Finally, once that every component has been selected, the filter performance is evaluated by simulation to validate that the resulting current THD after filtering is within the acceptable range.

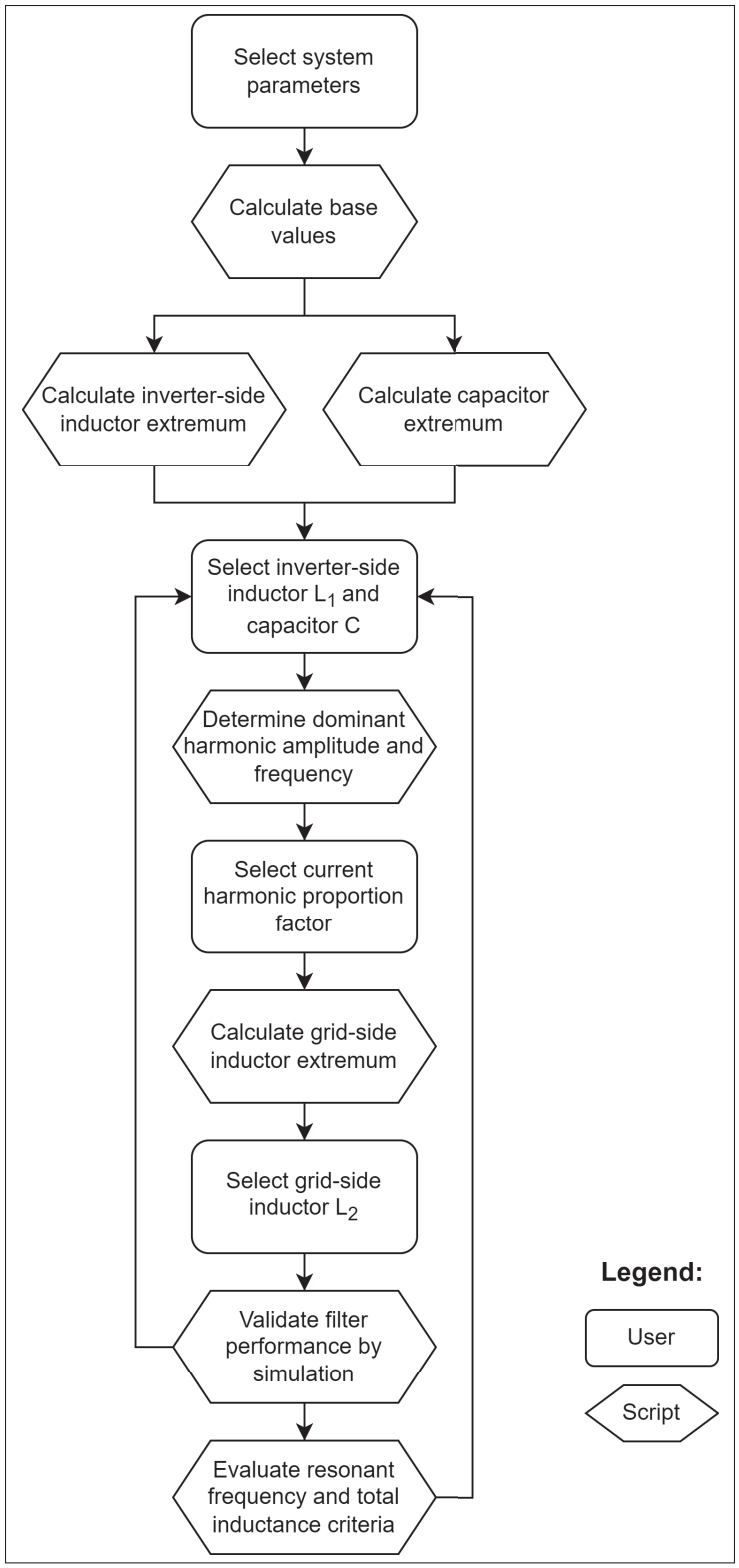

Figure 2.5 LCL filter design procedure

2.2.1 Inverter-side inductor

The inverter-side inductor L_1 is first selected and is designed in order to limit the ripple in the inverter output current. This is desirable, not only to improve power quality, but to reduce also the stress on the switching devices and the losses from the passive elements. The current ripple is caused by the charges flowing through the inductor depending on the voltage applied at the semiconductor bridge output as shown in Figure 2.6 for the unipolar SPWM technique.

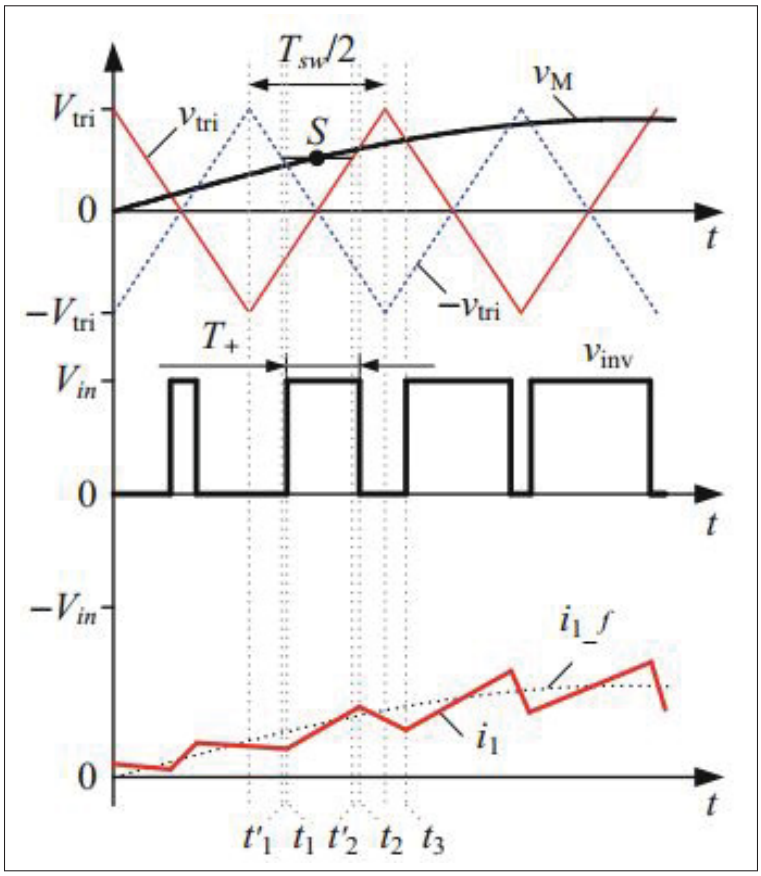

Figure 2.6 Unipolar PWM waveforms and inverter-side inductor current (Ruan *et al.*, 2017)

From this Figure and as described in relationship (2.1), it can be observed that when the modulating signal is greater than both triangular carriers $+v_{tri}$ and $-v_{tri}$, switches Q_1 and Q_4 are simultaneously ON and the inverter output voltage is $v_{inv} = V_{in}$, so the voltage across the inverter-side inductor is

$$v_{L_1} = L_1 \cdot \frac{di_1}{dt} = v_{inv} - v_C = V_{in} - v_C \tag{2.3}$$

During this interval, defined as T_+, the inverter-side inductor current i_1 increases and this positive increment can be expressed as

$$\Delta i_{1(+)} = \frac{V_{in} - v_C}{L_1} \cdot T_+ \tag{2.4}$$

where v_C is the capacitor voltage. From Figure 2.6, the ratio of the T_+ interval and the half switching period can also be defined as (2.5).

$$\frac{T_+}{T_{sw}/2} = M_r \cdot \sin(\omega_o \cdot t) \tag{2.5}$$

where M_r is the ratio of the modulating signal and carrier waveform

$$M_r = \frac{v_M}{V_{tri}} = \frac{V_s}{V_{DC}} \tag{2.6}$$

As previously mentioned, one of the advantages of the LCL filter compared to other topologies is that it allows to use smaller passive elements, so that the voltage drops across the filter inductors are negligible. The capacitor voltage can then be approximated to the fundamental grid voltage, expressed as

$$v_C \approx v_g = M_r \cdot V_{in} \cdot \sin(\omega_o \cdot t) \tag{2.7}$$

By using expressions (2.7) and (2.5) into (2.4), the current increment in the inverter-side inductor can be defined as (2.8).

$$\Delta i_{1(+)} = \frac{V_{in} \cdot T_{sw}}{2 \cdot L_1}(1 - M_r \cdot \sin(\omega_o \cdot t)) \cdot M_r \cdot \sin(\omega_o \cdot t) \tag{2.8}$$

From this expression, it can be deducted that the maximum increment in current happens when $\sin(w_o \cdot t) = \frac{1}{2 \cdot M_r}$ which yields (2.9).

$$\Delta i_{1\_max} = \frac{V_{in} \cdot T_{sw}}{8 \cdot L_1} \tag{2.9}$$

Using expression (2.9) for the maximum increment in the inductor current, a minimum value for the selection of the inverter-side inductor can be defined in order to limit the current ripple. Defining the desired current ripple coefficient as the ratio of the current ripple and the fundamental current $\lambda_{rip} = \Delta i_{1\_max}/I_1$ and substituting in (2.9), the minimum inverter-side inductor value for the unipolar PWM driven inverter is expressed as (2.10).

$$L_{1min} = \frac{V_{in} \cdot T_{sw}}{8 \cdot \lambda_{rip} \cdot I_1} \tag{2.10}$$

Ideally, the current ripple coefficient should be selected to be around 20-30% (Holmes, 1998).

On the other hand, the maximum inverter-side inductor value is calculated based on the desired maximum voltage drop across the inductor which should be kept small, usually around 5% of the nominal grid voltage. Defining this ratio as $\lambda_{v\_L1} = \Delta v_{L1}/V_g$ yields expression (2.11).

$$L_{1max} = \frac{V_g \cdot \lambda_{v\_L1}}{\omega_o \cdot I_1} \tag{2.11}$$

The two expressions in (2.10) and (2.11) allow us to select the filter inverter-side inductor within a range of acceptable values based on the system parameters and the filter performance. It is important to note that in practice, and in contrast to what is shown in Figure 2.4, this inductance

is implemented as two inductors, one in each branch of the inverter output. The total inductance remains the same but it allows to use smaller components which also improves the power losses.

2.2.2 Capacitor

The filter capacitor inevitably adds a phase shift in the current flowing through the filter which results in additional reactive power and decreased power factor. It is then desirable to use a smaller capacitance in order to limit this reactive power. The maximum capacitor value is given by

$$C_{max} = \lambda_C \cdot \frac{P_{nom}}{\omega_o \cdot V_g^2} \tag{2.12}$$

where λ_C is the percentage of reactive power induced by the capacitance, P_{nom} is the nominal inverter output power, ω_o is the nominal grid angular frequency and V_g is the nominal inverter output RMS voltage. As explained, λ_C should be kept small, generally around 5% (Liserre, Blaabjerg & Hansen, 2005).

2.2.3 Grid-side inductor

The last filter component, the grid-side inductor, is designed based on the required limits in injected current harmonic content. The IEEE Std 1547-2018 (IEEE, 2018) specifies current distortion limits as detailed in Table 2.1. To select a proper inductor value, the spectrum of the inverter output voltage must be known in order to determine the amplitude and angular frequency of the dominant voltage harmonic to be mitigated. The minimum grid-side inductor value can then be calculated using expression (2.13) (Ruan *et al.*, 2017).

$$L_{2min} = \frac{1}{L_1 C \omega_h^2 - 1} \cdot \left(L_1 + \frac{|V_h| \cdot V_{in}}{\omega_h \lambda_h I_2} \right) \tag{2.13}$$

where ω_h and $|V_h|$ are the angular frequency and amplitude of the dominant voltage harmonic and λ_h is the maximum allowed current harmonic ratio which, in our case, is selected from Table 2.1. The dominant voltage harmonic could be determined theoretically by expressing the inverter output voltage with a Fourier series expansion. However, in order to greatly simplify and automate the design procedure, a Simulink model of the inverter bridge is used (as presented in Appendix I) to generate and record the output voltage waveform and a Fast Fourier Transform (FFT) is then performed on the recorded signal to easily determine the dominant harmonic amplitude and frequency.

Table 2.1 Maximum odd harmonic current distortion in percent of rated current(IEEE, 2018)

Individual odd harmonic order	$h < 11$	$11 \leq h < 17$	$17 \leq h < 23$	$23 \leq h < 35$	$35 < h$
Percent %	4.0	2.0	1.5	0.6	0.3

2.2.4 Additional design criteria

The LCL filter introduces a resonant frequency, f_{res}, given by (2.14). To avoid interactions with the grid or inverter dynamics, this resonance should be located within the range of frequencies given by expression (2.15) (Reznik, Simões, Al-Durra & Muyeen, 2014).

$$f_{res} = \frac{1}{2\pi}\sqrt{\frac{L_1 + L_2}{L_1 L_2 C}} \tag{2.14}$$

$$10 \cdot f_o < f_{res} < 0.5 \cdot f_{sw} \tag{2.15}$$

Furthermore, the per unit filter total inductance, given by equation (2.16), should be less than 10% to avoid unnecessary voltage drop across the filter.

$$Z_{LCL} = (L_1 + L_2) \cdot \frac{\omega_o P_{rated}}{V_g^2} \tag{2.16}$$

2.3 Results and discussion

2.3.1 Applied design procedure and simulation results

Following the procedure shown in Figure 2.5, the output filter can now be designed. The first step is to select the desired inverter parameters, which are given in Table 1.1. The base values can then be calculated as

$$Z_{base} = \frac{V_s^2}{P_{nom}} = 11.52\Omega \tag{2.17}$$

$$C_{base} = \frac{1}{\omega_o \cdot Z_{base}} = 230\mu F \tag{2.18}$$

Using equation (2.10) with $T_{sw} = \frac{1}{20kHz} = 50\mu s$ and selecting a desired current ripple coefficient of 20%, the minimum inverter-side inductor value is calculated to be $L_{1min} = 660\mu H$. Its maximum value can then be evaluated using equation (2.11) and setting $\lambda_{v\_L1} = 5\%$, which yields $L_{1max} = 1.53mH$. Referring to standard and commercially available inductors, a value of $L_1 = 680\mu H$ is selected. The technical specifications for a commercially available inductor of $\frac{640\mu H}{2} = 340\mu H$ are given in Annex II.

The filter capacitor can then be selected using equation 2.12 and limiting the induced reactive power to 5%, which gives $C_{max} = 11.5\mu F$. A value of $C = 8\mu F$ is chosen.

The next step is to determine the amplitude and angular frequency of the dominant voltage harmonic, which is done by simulating the inverter full-bridge model presented in Figure I-1 of Appendix I and performing a FFT on the output voltage waveform to plot its frequency spectrum.

As previously mentioned, for unipolar SPWM switched inverters, the induced harmonics are located particularly at around twice the switching frequency, which can be observed on Figure 2.7. The smallest dominant voltage harmonic frequency is $\omega_h = 39940Hz$, which is the $666th$ harmonic order on a $60Hz$ basis, and its amplitude is $V_h = 42.8\%$ of the fundamental voltage. Referring to Table 2.1, the maximum allowed current harmonic ratio is $\lambda_h = 0.3\%$ for harmonic orders over 35 in order to comply with the standard. In our case, a current harmonic ratio of $\lambda_h = 0.2\%$ is selected. Using equation 2.13 with the aforementioned values, the minimum grid-side inductor is calculated to be $L_{2min} = 42.3\mu H$. A value of $L_2 = 100\mu H$ is chosen.

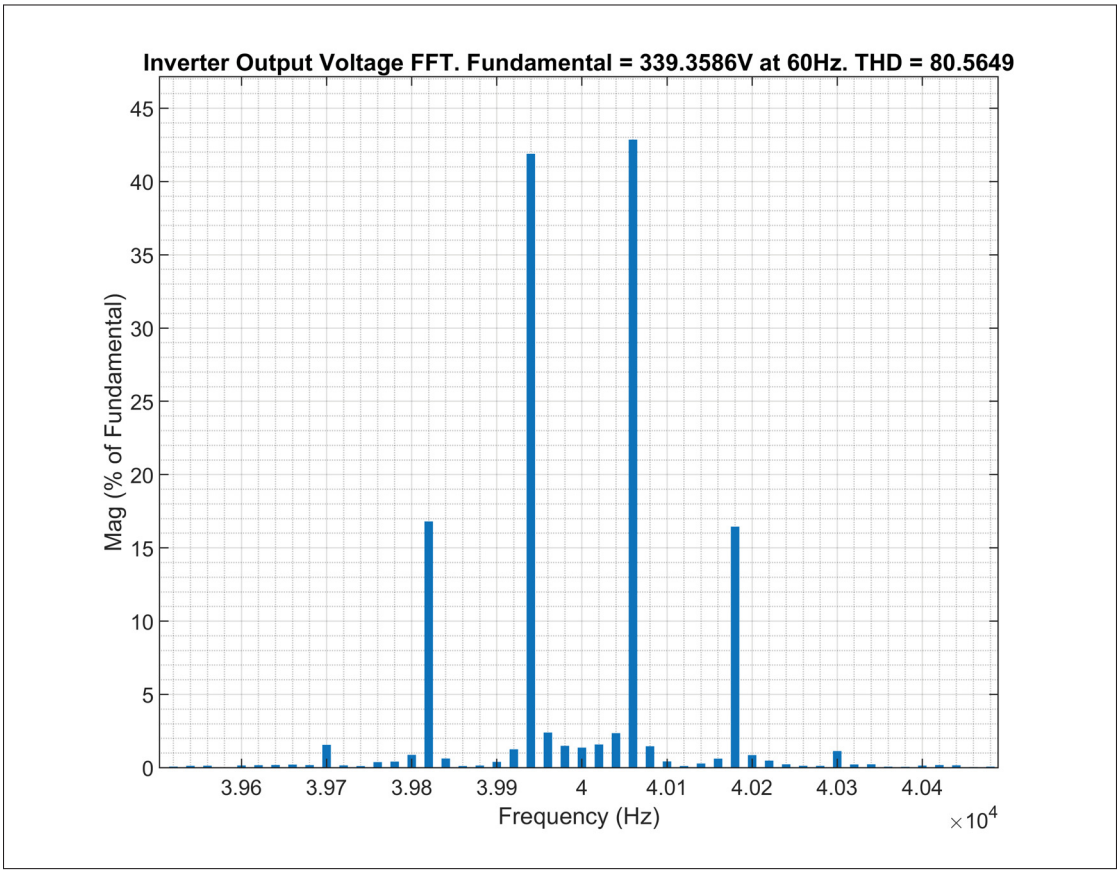

Figure 2.7 Output voltage spectrum of unipolar SPWM switched full-bridge inverter

Table 2.2 LCL filter parameters

Parameter	**Value**
Inverter-side inductor L_1	$680\mu H$
Capacitor C	$8\mu F$
Grid-side inductor L_2	$100\mu H$

2.3.2 Simulation results

The designed LCL filter parameters are summarized in Table 2.2 and its performance is evaluated by simulating the model presented in Figure I-4. Simulation results are presented in Figure 2.8, where the waveforms of the output voltage between the inverter bridge and filter as well as the currents in the inverter-side inductor, grid-side inductor and capacitor branch are shown. If one zooms on the inverter-side current, the current ripple can be observed, as shown in Figure 2.9, and is measured to be around $\Delta i_{1\_max} = 4.1A$. Considering that the fundamental RMS current is $I_1 = \frac{P_{nom}}{V_s} = 20.83A$, the resulting current ripple coefficient is calculated to be $\lambda_{rip} = \frac{4.1}{20.83} = 19.7\%$, which is below the selected value of 20%.

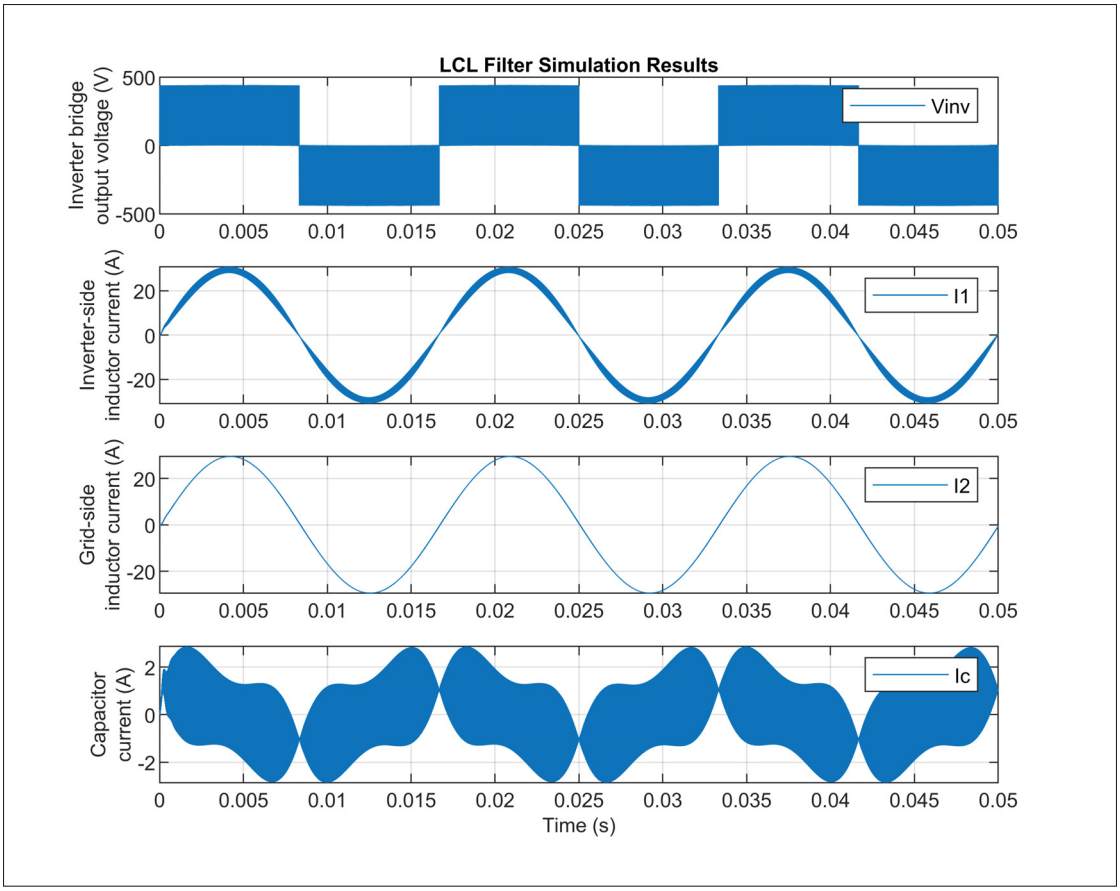

Figure 2.8 LCL filter simulation results

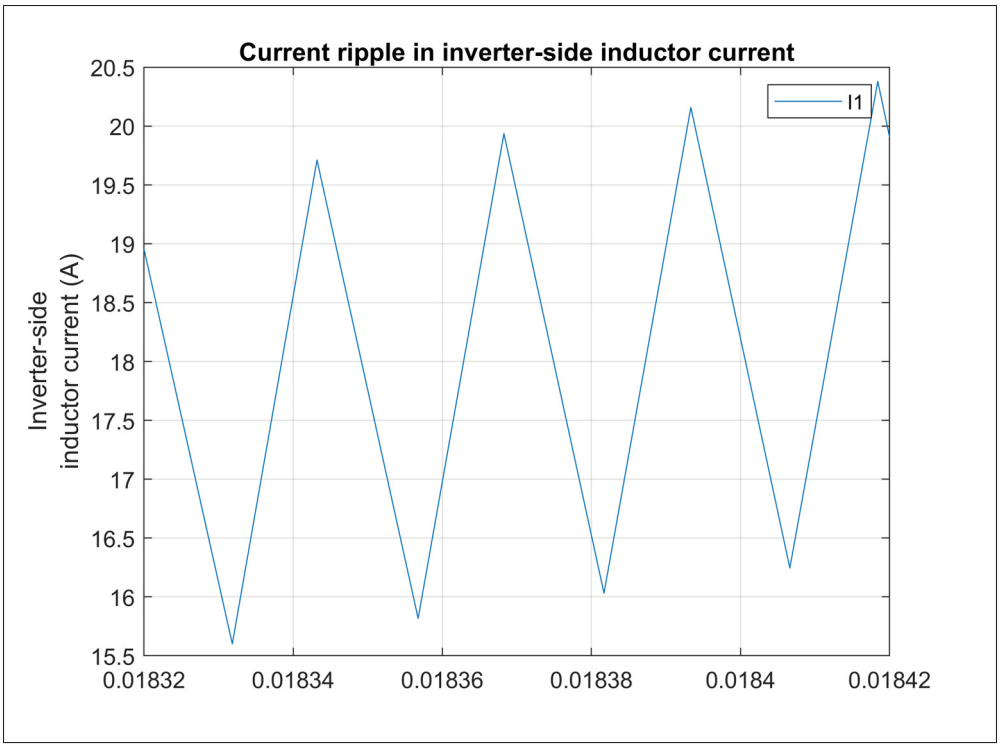

Figure 2.9 Current ripple in inverter-side inductor current

It can be seen just by looking at Figure 2.8 that the grid-side inductor current has a lower harmonic content than the inverter-side inductor current since most of the harmonics have been attenuated by the LC stage. By performing a FFT and plotting its harmonic spectrum, shown in Figure 2.10, it can be observed that the amplitudes of all harmonic orders are damped well below the required values specified in Table 2.1. More specifically, one can also observe that the amplitude of the dominant harmonic located at 39940Hz is reduced to approximately 0.017% as shown in Figure 2.11, which is in agreement with the specifications. Furthermore, the resulting output current THD is evaluated at 0.104%, which is well below the required value of 5%. specified in (IEEE, 2018).

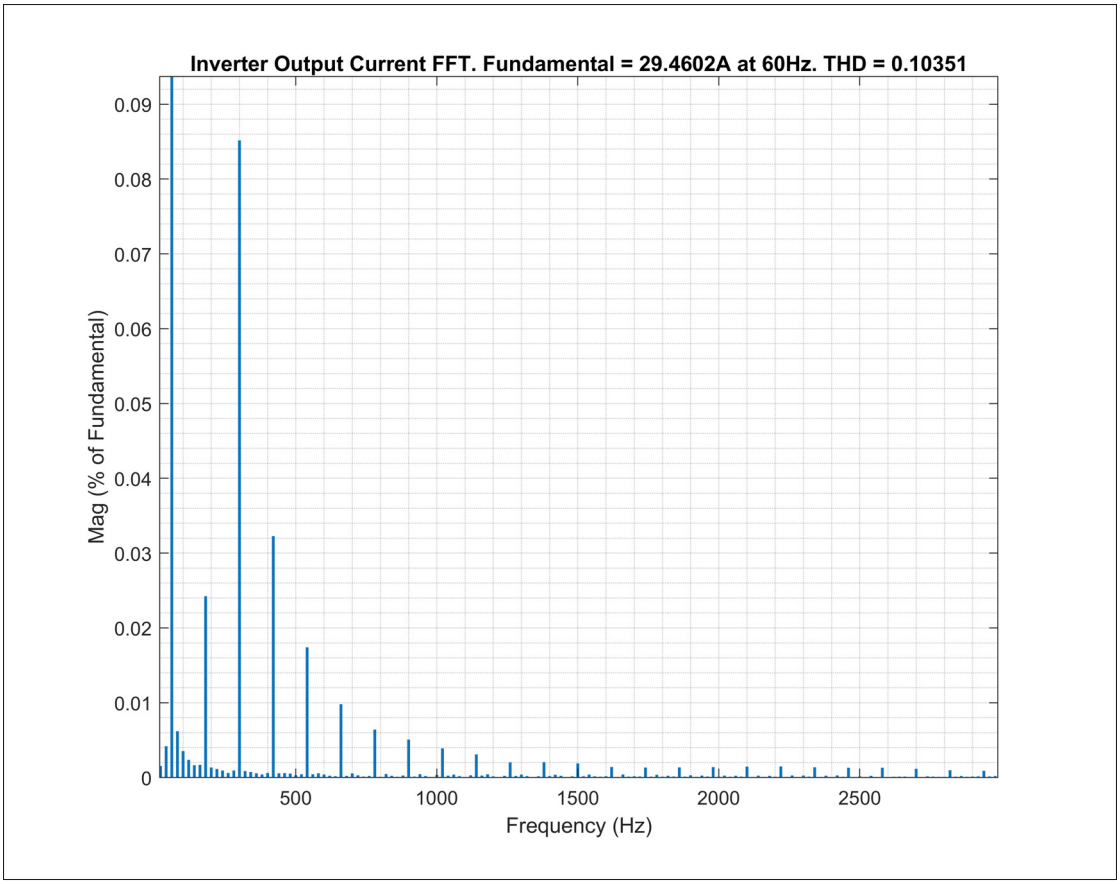

Figure 2.10 Frequency spectrum of the output current

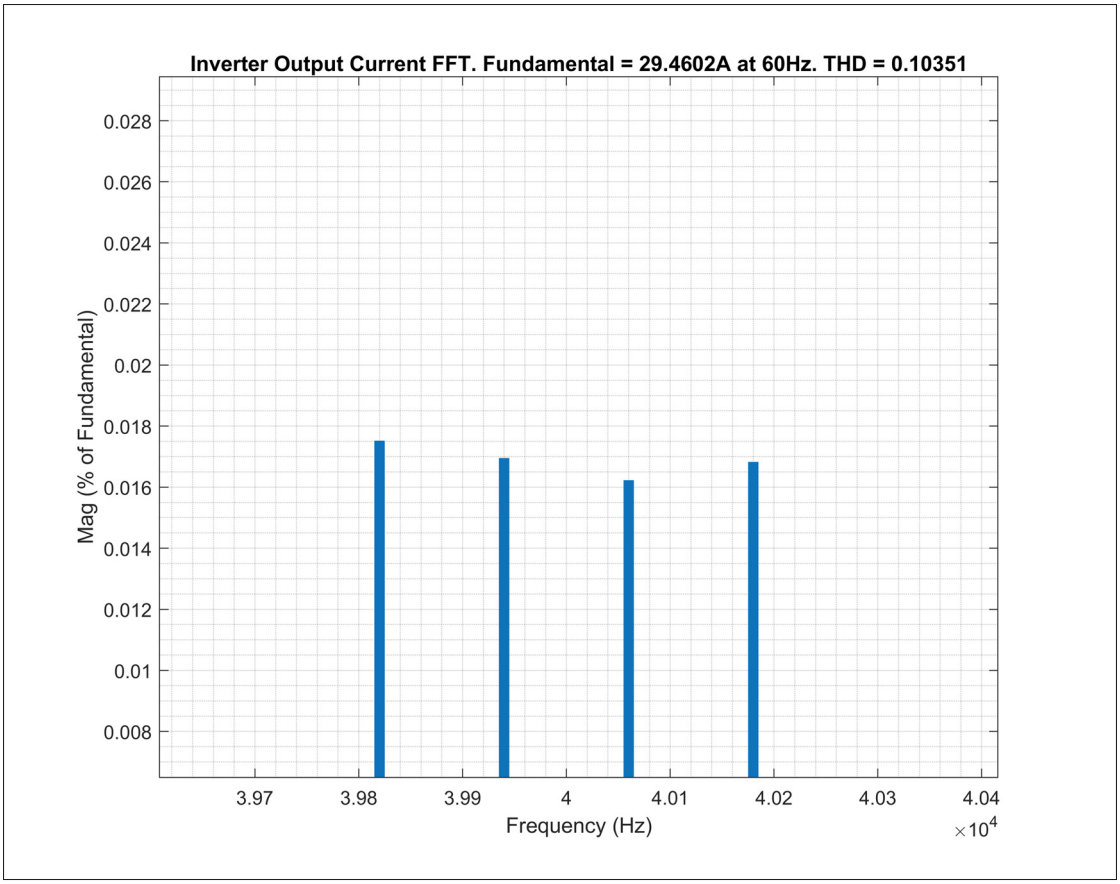

Figure 2.11 Frequency spectrum of the output current around the dominant harmonic

Using equation 2.14, the calculated filter resonant frequency is approximately $f_{res} = 6027Hz$, which satisfies the criterion of expression 2.15. Finally, the total per unit filter inductance, calculated with equation 2.16, is $Z_{LCL} = 2.55\%$, which is below the maximum value of 10%. In conclusion, the simulation results demonstrate that the designed filter successfully meets all the performance and design criteria previously established.

2.3.3 LCL filter resonance damping

As previously mentioned, the LCL filter introduces a resonant frequency in the system response. One can observe the resonant peak on the Bode diagram of the filter's transfer function which

expresses the relationship between the output current and the input voltage. This transfer function is given by expression 2.19. The Bode diagram of the designed filter is shown in Figure 2.12.

$$T_{LCL} = \frac{i_2}{v_{inv}} = \frac{1}{L_1 L_2 C s^3 + (L_1 + L_2)s} \tag{2.19}$$

This inherent resonant peak needs to be dealt with in order to insure the overall system stability. Various damping methods exist to mitigate the LCL filter resonance. Passive damping using a resistor in series or parallel with the filter's elements can provide satisfactory resonance damping, but the resulting frequency response present disadvantages depending on the resistor location, including inferior high-frequency harmonics attenuation. Placing the resistor in parallel with the filter capacitor provides the best passive damping solution since the filter frequency response magnitude remains unchanged for frequencies other than the resonance. However, it results in higher power losses, particularly with lower inverter switching frequencies (Peña-Alzola, Liserre, Blaabjerg, Sebastián, Dannehl & Fuchs, 2013) which translate into heat that needs to be handled by a cooling system. Furthermore, the use of additional passive elements for damping purpose increases the filter size, weight and cost.

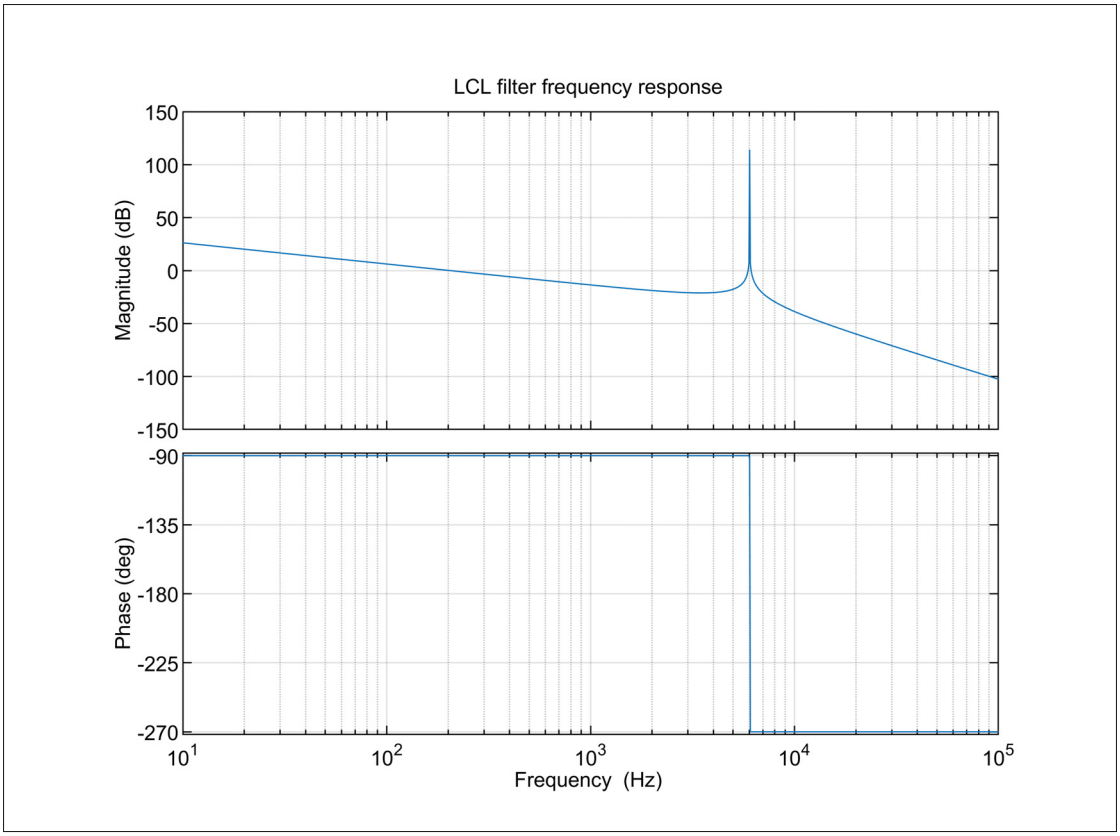

Figure 2.12 LCL filter Bode diagram

Alternatively, active damping methods using state-variable feedback are used in order to emulate the resistor in parallel with the filter capacitor in the current control loop (Dannehl, Fuchs, Hansen & Thøgersen, 2010). This method is chosen for the current work as demonstrated in Chapter 3, using the filter capacitor current as the state-variable. It is preferred to other system measurements like capacitor voltage or grid current because it provides a good damping performance and also presents a simpler implementation. Indeed, the feedback path transfer function of the capacitor current is a simple proportional gain.

2.4 Conclusion

In this chapter, the most common SPWM techniques used for single-phase grid-connected inverters using a full-bridge converter topology were first reviewed. The bridge output waveforms

were presented to demonstrate the need of a filter to limit the harmonic content of the inverter output current below acceptable limits defined by interconnection standards. A comprehensive step-by-step design procedure was presented in order to alleviate the complexity of designing a LCL filter as the one used herein. It uses the inverter system parameters and desired performance metrics, i.e. maximum current ripple, reactive power and harmonic current distortion, to derive mathematical expressions for the extremum values of each filter passive component. Additional design criteria pertaining to the filter size and resonant frequency were introduced. The design procedure was then applied to the inverter system under study and simulated in Matlab/Simulink to demonstrate its efficacy and evaluate the filter performance. It was shown that the designed filter effectively reduces the inverter output current THD well below the required limits established in the standards. Using scripts and simulation models, the filter design procedure was automated in the Matlab/Simulink environment as presented in Annex I.

The resonant frequency resulting from the use of a LCL filter and various damping techniques were introduced. Active damping using state-variable feedback was shown to provide many advantage over passive damping methods. It will be used as part of the inverter control system to mitigate this resonance.

With the output filter now designed, the electrical portion of the inverter system is established and it is now possible to design the control system, which is presented in the next chapter.

CHAPTER 3

CURRENT CONTROLLER

The objective of this chapter is to present the grid-connected inverter control system and to detail the design procedure of the current controller. To do so, a mathematical model of the inverter system will be developed, allowing us to derive expressions that will be used to design and analyze the control system. The procedure will then be applied to the inverter under study and the system performance and stability will be analyzed theoretically and by simulation.

3.1 Grid-connected inverter model

The inverter electrical and control system diagram is presented in Figure 3.1. The physical components are represented with black lines and the blue lines denote components pertaining to the control system. It is important to note that only the faster, inner current control loop is shown. This feedback loop is responsible in controlling the output current i_2 in amplitude and phase to track the current reference, namely i_2^*. The reference signal is generated using the phase angle provided by the PLL so that it is synchronized to the grid voltage and its amplitude, I_{ref}, can be generated by an outer, slower voltage control loop which will be presented in Chapter 5 when the grid support functions are addressed. The error between the measured and reference current is passed to the current controller, whose transfer function is denoted as G_i, and its output is adjusted to generate the modulating signal sent to the SPWM. As previously mentioned in Chapter 2, the measured filter capacitor branch current i_C is fed back into the current control loop through a proportional gain H_{i1} in order to emulate a resistor in parallel with the filter capacitor and actively damp its resonance. As shown in Figure 3.1, the feedback is subtracted from the modulating signal generated by the current controller.

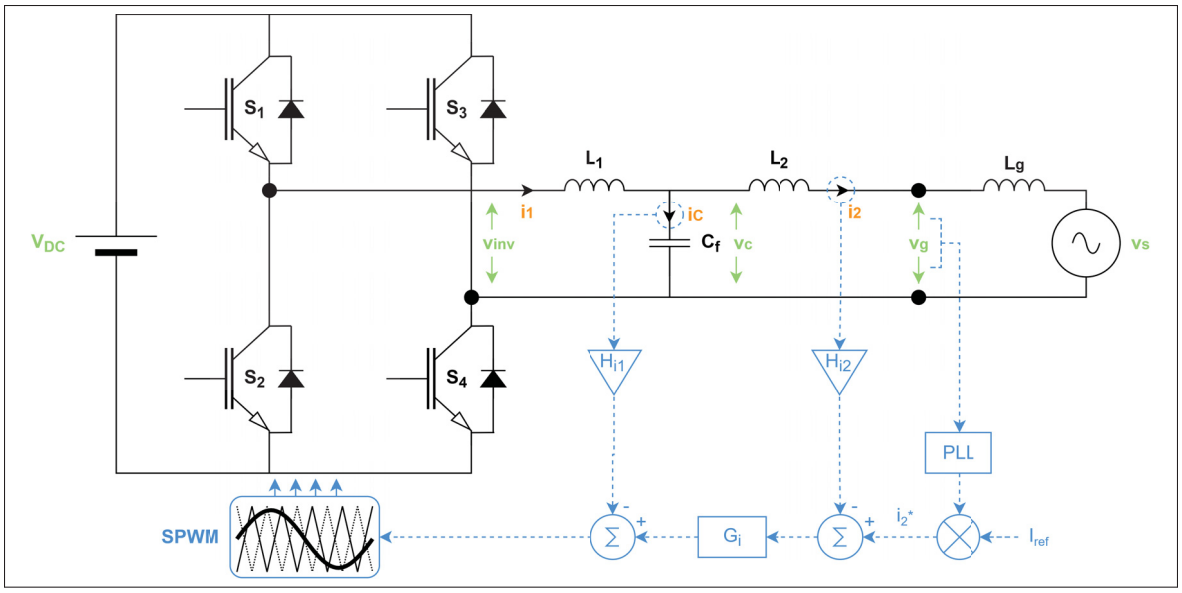

Figure 3.1 Electrical and control diagram of the single-phase grid-connected inverter

From Figure 3.1, a block diagram is derived, representing the mathematical model of the inverter and its control system, as shown in Figure 3.2 where K_{PWM} is the transfer function between the modulating signal and the inverter bridge output voltage which can be considered as a simple gain:

$$K_{PWM} = \frac{V_{DC}}{V_{tri}} \tag{3.1}$$

The filter and grid impedances can be represented in the Laplace domain as:

$$Z_{L1}(s) = sL_1, \quad Z_{L2}(s) = sL_2, \quad Z_C(s) = \frac{1}{sC}, \quad Z_g(s) = sL_g \tag{3.2}$$

The following expressions can be derived to represent the currents and voltages shown in Figure 3.1:

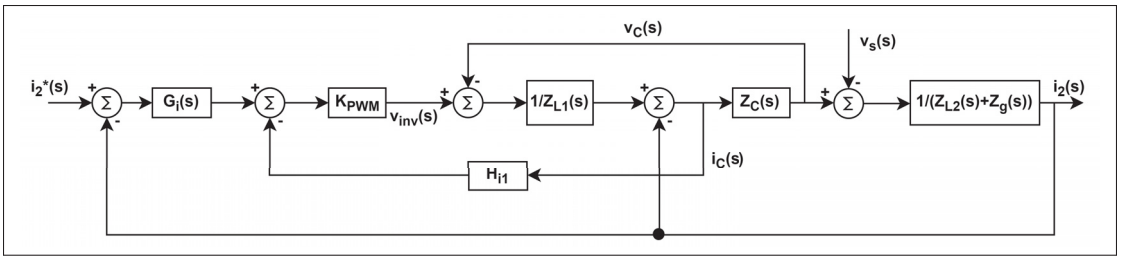

Figure 3.2 Inverter system block diagram

$$i_2(s) = \frac{v_C(s) - v_s(s)}{Z_{L2}(s) + Z_g(s)} \tag{3.3}$$

$$i_C(s) = \frac{v_C(s)}{Z_C(s)} \tag{3.4}$$

$$i_2^*(s) - i_2(s) = \epsilon_i \tag{3.5}$$

$$v_{inv}(s) = K_{PWM}(G_i(s) \cdot \epsilon_i - H_{i1} \cdot i_C(s)) \tag{3.6}$$

$$v_C(s) = Z_C\left(\frac{v_{inv}(s) - v_C(s)}{Z_{L1}(s)} - i_2(s)\right) \tag{3.7}$$

Using expressions 3.4 to 3.7 into 3.3 and rearranging, the inverter output current can be expressed as:

$$i_2(s) = \frac{Z_C(s) \cdot K_{PWM} \cdot G_i(s) \cdot \epsilon_i - (Z_{L1}(s) + Z_C(s) + K_{PWM} \cdot H_{i1}) \cdot v_s(s)}{Z_C(s) \cdot (Z_{L1}(s) + Z_{L2}(s) + Z_g(s)) + (Z_{L1}(s) + K_{PWM} \cdot H_{i1}) \cdot (Z_{L2}(s) + Z_g(s))} \tag{3.8}$$

To simplify the notation and the analysis of the inverter system, the block diagram can be manipulated to group multiple terms together and yield the simplified block diagram presented in Figure 3.3. The output current $i_2(s)$ can then be expressed as:

$$i_2(s) = G_i(s) \cdot G_1(s) \cdot G_2(s) \cdot \epsilon_i - G_2(s) \cdot v_s(s) \tag{3.9}$$

The inverter system loop gain can also be obtained by forcing the external perturbation to $v_s(s) = 0$, yielding:

$$T(s) = G_i(s) \cdot G_1(s) \cdot G_2(s) \tag{3.10}$$

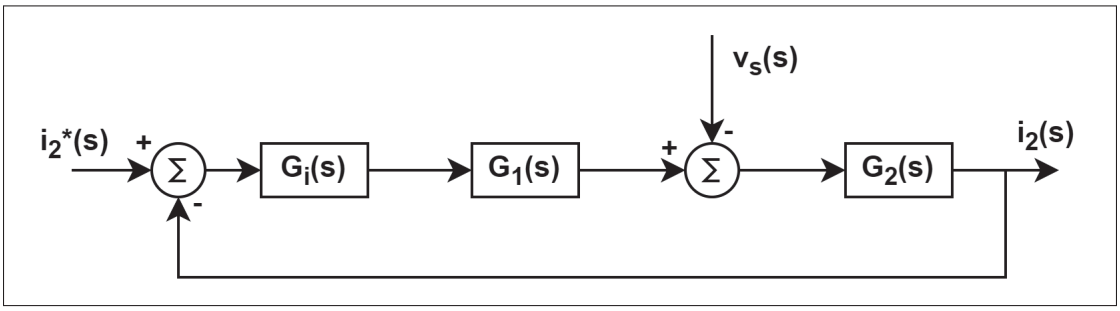

Figure 3.3 Simplified inverter system block diagram

Furthermore, to simplify the notation, impedances can be expressed without their Laplace operator suffix simply as Z_{L1}, Z_{L2}, Z_C and Z_g. By identification with expression (3.8), one defines the following transfer functions.

$$G_1(s) = \frac{Z_C \cdot K_{PWM}}{Z_{L1} + Z_C + K_{PWM} \cdot H_{i1}} \tag{3.11}$$

$$G_2(s) = \frac{Z_{L1} + Z_C + K_{PWM} \cdot H_{i1}}{Z_C \cdot (Z_{L1} + Z_{L2} + Z_g) + (Z_{L1} + K_{PWM} \cdot H_{i1}) \cdot (Z_{L2} + Z_g)} \tag{3.12}$$

Replacing expressions (3.11) and (3.12) into (3.10), expression (3.13) is obtained for the inverter system loop gain, that will be used to analyze its stability.

$$T(s) = G_i(s) \cdot \frac{Z_C \cdot K_{PWM}}{Z_C \cdot (Z_{L1} + Z_{L2} + Z_g) + (Z_{L1} + K_{PWM} \cdot H_{i1}) \cdot (Z_{L2} + Z_g)} \tag{3.13}$$

It is important to emphasize that, although it is not part of the inverter system, the grid impedance is included in the inverter model equations to take it into account when analyzing the system stability as a whole when it is grid-connected. However, as demonstrated later in this chapter, when designing the current controller, the grid impedance will be omitted from the equations so that the current control loop performance and stability is evaluated notwithstanding this external factor. Ignoring the grid impedance and representing the impedances in the Laplace domain, the system loop gain of expression (3.13) can be rewriten as (3.14):

$$T(s) = G_i(s) \cdot \frac{K_{PWM}}{L_1 L_2 C \cdot s^3 + L_2 C H_{i1} K_{PWM} \cdot s^2 + (L_1 + L_2) \cdot s} \tag{3.14}$$

One also further rewrites the expression for the output current using the loop gain transfer function as:

$$i_2(s) = \frac{T(s)}{1 + T(s)} \cdot i_2^*(s) - \frac{G_2(s)}{1 + T(s)} \cdot v_s(s) \tag{3.15}$$

As observed, the first term in expression 3.15 is impacted by the variations in the current reference $i_2^*(s)$ while the second term is related to the variations in grid voltage $v_s(s)$. Two other distinct transfer functions can be defined from these terms, namely the tracking and disturbance transfer functions, allowing to analyze the inverter response to changes in the current reference and grid voltage.

$$i_{2T}(s) = \left.\frac{i_2(s)}{i_2^*(s)}\right|_{v_s(s)=0} = \frac{T(s)}{1+T(s)} \tag{3.16}$$

$$i_{2D}(s) = \left.\frac{i_2(s)}{v_s(s)}\right|_{i_2^*(s)=0} = -\frac{G_2(s)}{1+T(s)} \tag{3.17}$$

The frequency response of the open-loop gain of equation (3.14) is shown on the Bode diagram of Figure 3.4 for an uncompensated system, meaning that the current controller transfer function is set to $G_i(s) = 1$ (no controller) and the capacitor current feedback gain is set to $H_{i1} = 0.001$ (no active damping). A very stiff, almost ideal grid, i.e. $L_g = 0.001mH$ is considered. The inverter and output filter parameters of Tables 1.1 and 2.2 are used to plot the frequency response. One observes the output filter resonance around $f_{res} = 6.03$kHz, which introduces a high gain and a $-180°$ phase shift. Furthermore, it can be seen that the system is inherently unstable with a negative phase margin of $-90°$ at the crossover frequency $f_c = 9.5$kHz.

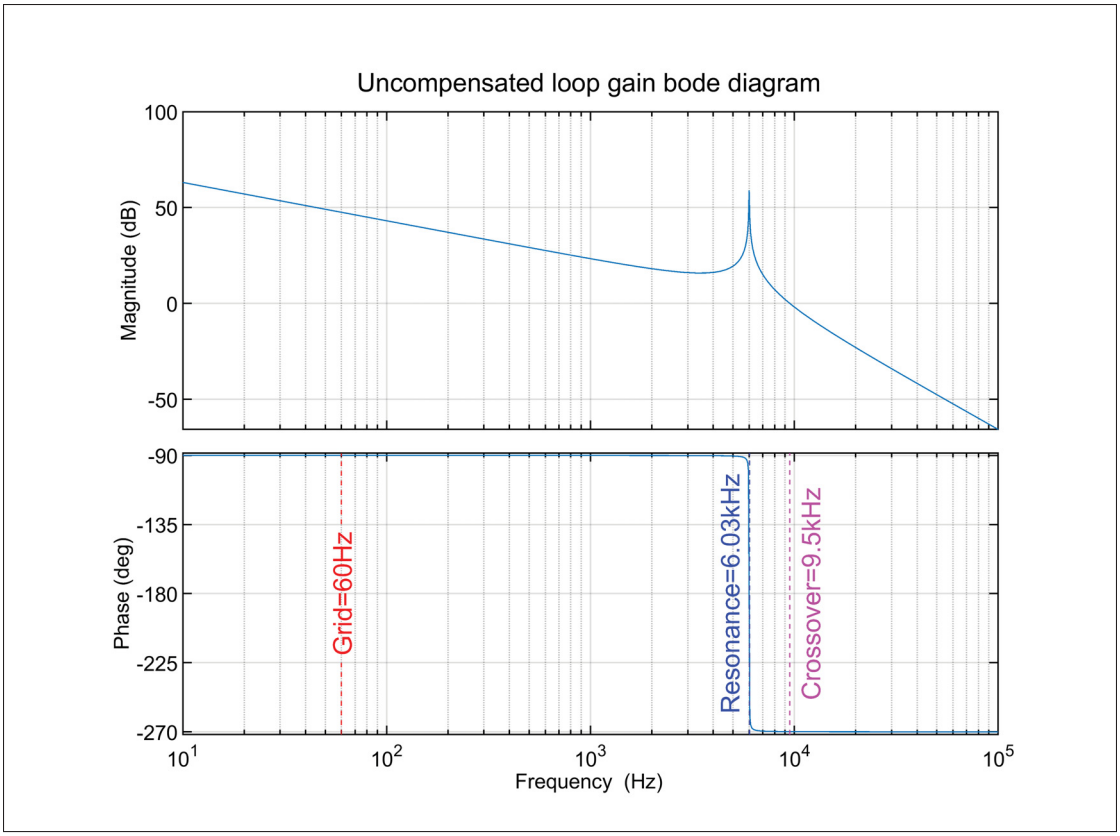

Figure 3.4 Uncompensated loop gain Bode diagram

By adjusting the capacitor current feedback gain to an arbitrary value of $H_{i1} = 0.25$, the output filter resonance is effectively damped as shown on the Bode diagram of Figure 3.5, where the resonant peak is significantly reduced. The system is obviously still unstable, with a negative phase margin of approximately $-50°$ at the crossover frequency $f_c = 8.95$kHz. To stabilize the system, one sees that the current controller must move the crossover frequency of the loop gain to a lower frequency than the resonance in order to maintain a positive phase margin despite the phase shift introduced by the resonance. It should also be noted that using active damping introduces an additional negative phase shift at frequencies lower than the resonance. Hence, it emphasizes the importance to optimally size the H_{i1} gain to avoid reducing the system phase margin to a critical point.

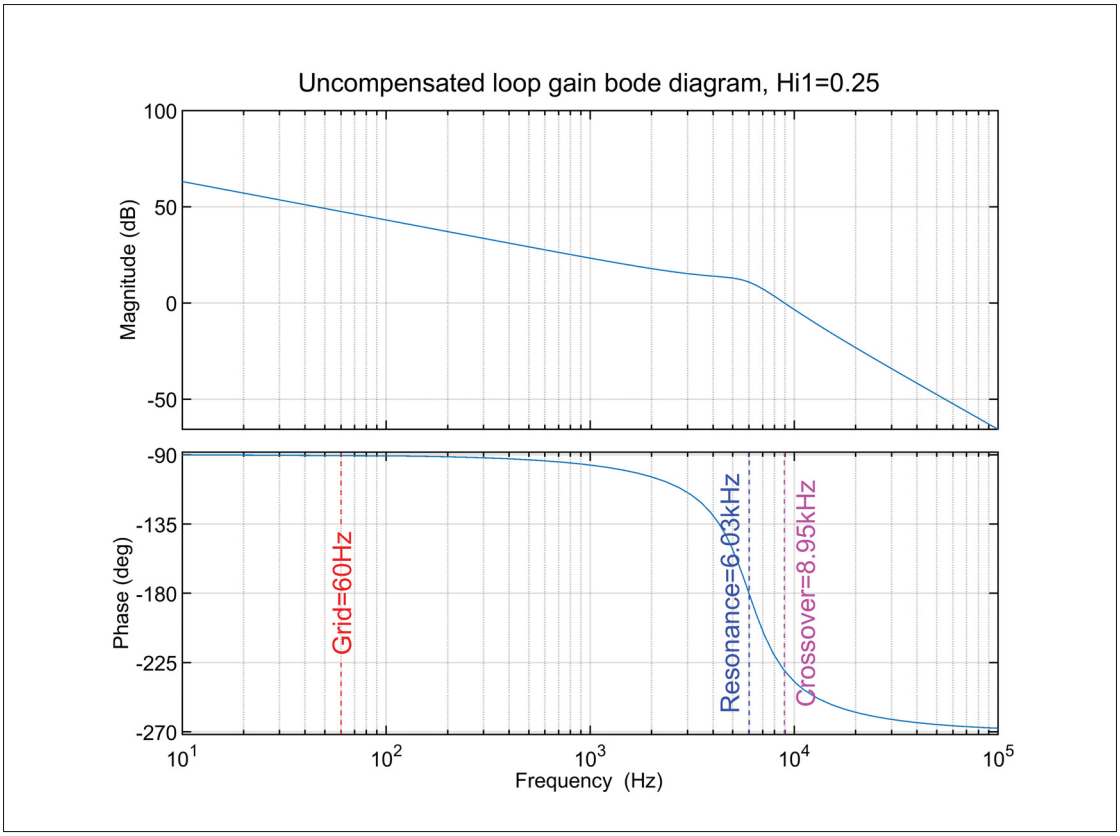

Figure 3.5 Uncompensated loop gain Bode diagram with active damping

Furthermore, the inverter resonance frequency induced by the output filter varies with the grid impedance, hence the reason the term Z_g is included in the system modeling of equation (3.13). Indeed, it can be seen from Figure 3.1 that the filter grid-side inductor can be considered as the combination of the L_2 and L_g in series. Referring to equation (2.14), this translates to a change in the resonance frequency, which also changes the crossover frequency of the system loop gain of equation (3.13) as illustrated in the frequency response of Figure 3.6 where the capacitor current feedback gain is set to $H_{i1} = 0.001$ to show the resonant peak and the grid inductor is set to $L_g = 1$mH. By comparing with Figure 3.4, it can be observed that the increase in grid inductance reduces the resonance and crossover frequencies, which are now 2.75kHz and 4.3kHz respectively. It will also be demonstrated later in this chapter how the change in grid inductance impacts the system phase margin once the current controller is designed.

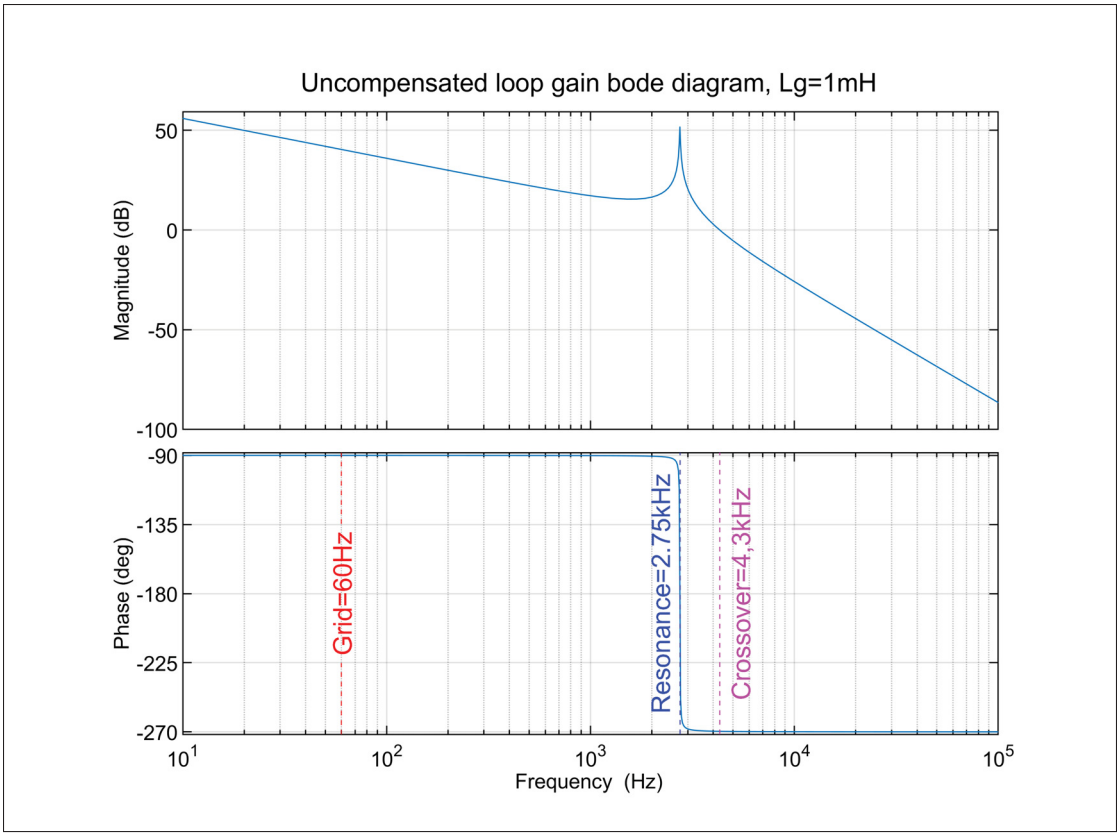

Figure 3.6 Uncompensated loop gain Bode diagram with increased grid inductance

3.2 Proportional-resonant controller

As mentioned in Section 1.7, the proportional-resonant controller provides advantageous characteristics for the control of single-phase inverters, mainly for its ability to introduce a very high gain at the grid frequency, resulting in accurate tracking of a sinusoidal reference without steady-state error and good dynamic performance. The PR controller transfer function $G_{PR}(s)$ is expressed as:

$$G_{PR}(s) = K_p + \frac{K_r 2\omega_i s}{s^2 + 2\omega_i s + \omega_r^2} \tag{3.18}$$

This transfer function has two terms: the controller proportional gain K_p and the resonant term where K_r is the resonant gain, ω_r is the resonance frequency and ω_i is the resonance frequency bandwidth in rad/s. In other words, the frequency band around the resonance frequency for which an attenuation of -3dB will be achieved. The PR controller frequency response for $\omega_r = \omega_o$ is presented in the Bode diagram of Figure 3.7. By selecting $\omega_r = \omega_o$, the PR controller has a high gain at the grid nominal frequency, providing accurate tracking of the sinusoidal reference with zero steady-state error. However, it should be noted that a negative phase shift is introduced at higher frequencies surrounding the resonance. It will be important that the crossover frequency of the designed system be located high enough so that this negative phase shift has minimal impact on the overall phase margin.

As demonstrated in (Zmood & Holmes, 2003), the controller bandwidth w_i should be kept as small as possible in order to improve the PR controller frequency response, i.e. retaining a high gain at the controller resonance (grid nominal frequency) while still providing good performance for small frequency deviations around it. The Bode diagrams of Figure 3.8 show how an increasing bandwidth impacts the frequency response when all other controller parameters are kept constant. It becomes evident from the frequency response that a larger bandwidth may amplify off-nominal frequencies and decrease overall inverter system stability for a constant resonant gain K_r. A value of $w_i = 0.001 \cdot \omega_o = 0.38 rad/s$ is used for the controller designed herein.

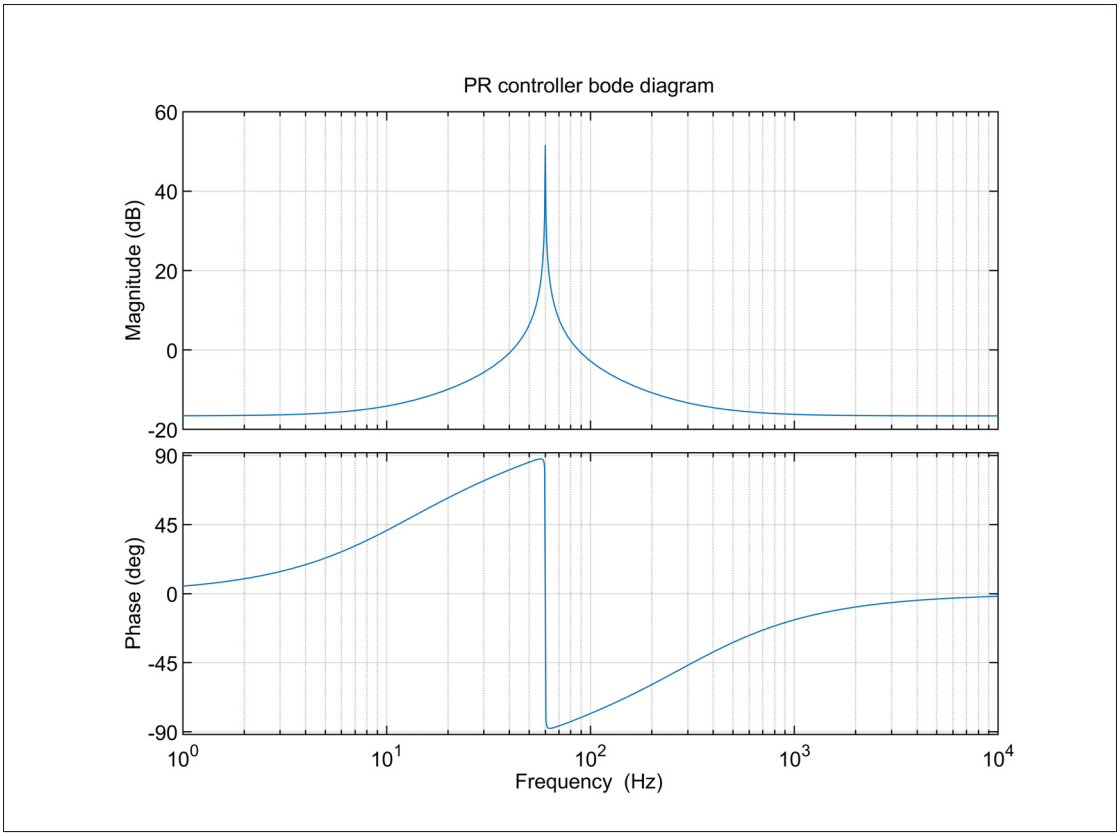

Figure 3.7 Proportional-resonant controller Bode diagram

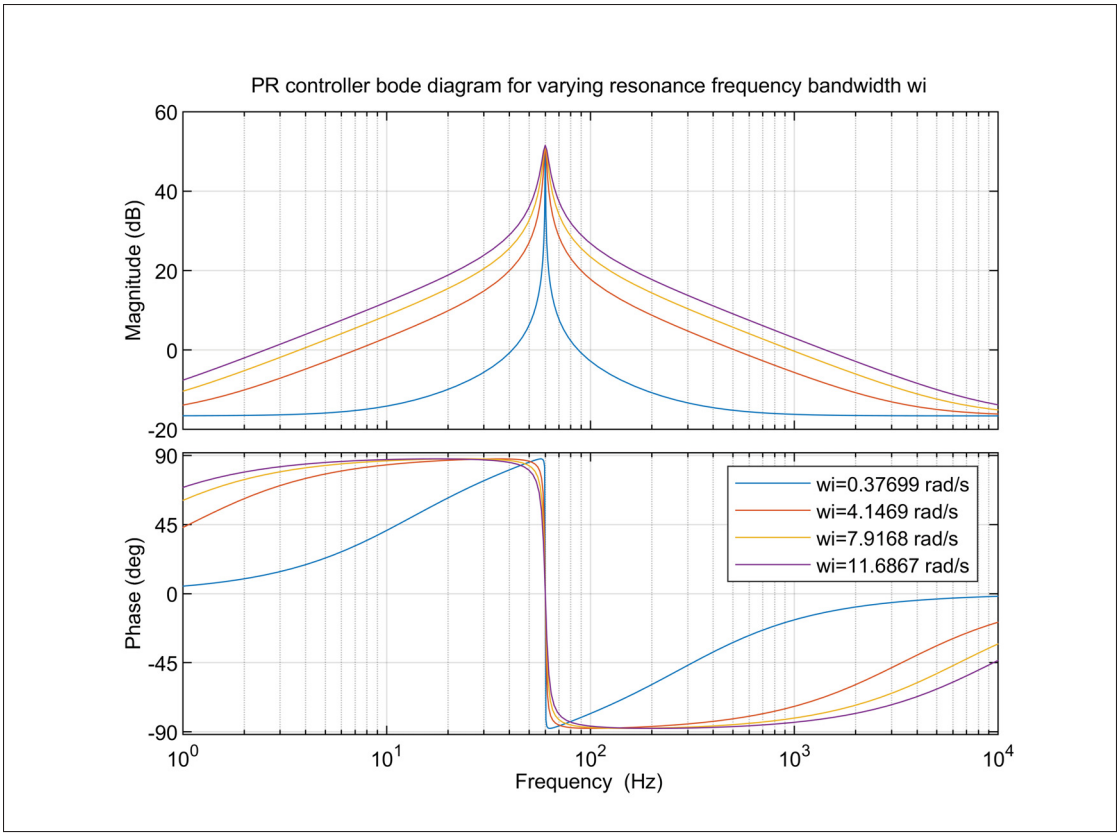

Figure 3.8 Frequency response of proportional-resonant controller for increasing bandwidth ω_i

From the PR controller transfer function of equation (3.18), it can be seen that the controller parameters that need to be selected are the proportional and resonant gains, namely K_p and K_r. Additionally, from the loop gain expression of (3.14), the capacitor current feedback coefficient H_{i1} is the third variable to be selected in order to shape the whole inverter system frequency response and comply with the required performance. The design procedure of the current controller must take into account this coefficient since the frequency response of the actively damped filter resonance inevitably interacts with the controller frequency response.

3.3 Current controller design procedure

A similar procedure as the one presented in Chapter 2 is used to design the current controller, i.e. an automated design procedure composed of scripts and models is developed in the Matlab/Simulink environment. As previously stated, it allows to run iterative tests for multiple controller performance constraints or system parameters combinations and to validate the resulting control system performance in very little time. The overall design procedure is adapted from the work in (Bao, Ruan, Wang, Li, Pan & Weng, 2014) and is summarized in the workflow of Figure 3.9. The developed scripts and models are presented in Appendix IV.

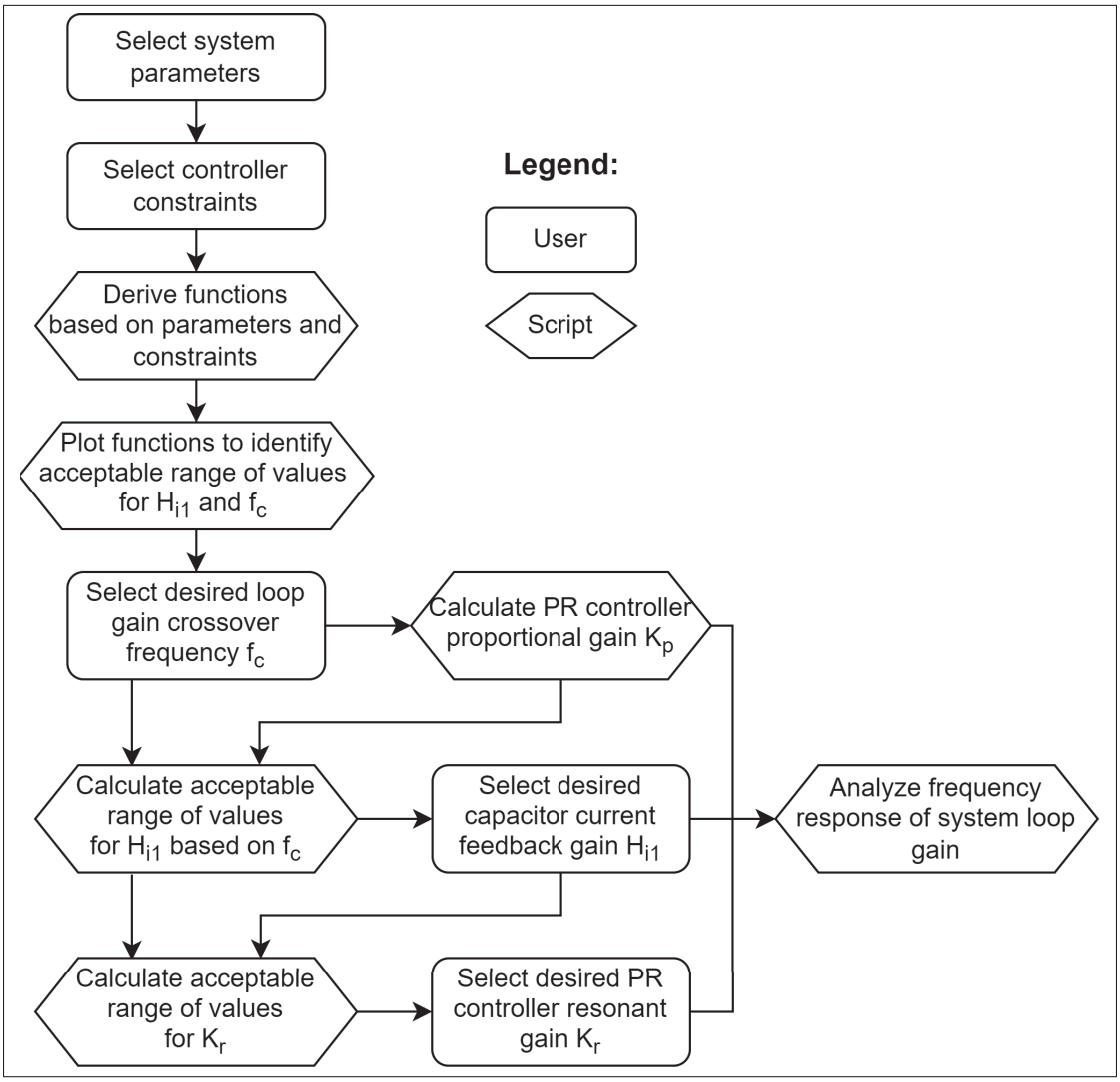

Figure 3.9 Current controller design procedure

The first step of the procedure is to define the inverter system parameters, which are summarized in Tables 1.1 and 2.2, so that the system equations presented in the previous sections of this chapter can be derived. The controller performance constraints are then selected, namely the minimum magnitude of the loop gain at fundamental frequency as well as the minimum phase and gain margins. Based on these constraints and parameters, a set of functions is derived to graphically represent the acceptable range of values for the capacitor current feedback coefficient H_{i1} and loop gain crossover frequency f_c. Once the desired crossover frequency is selected, the controller proportional gain K_p is calculated and the corresponding extremum values for H_{i1} are given so that the desired value can be selected. From these selections, an acceptable range of values for the controller resonant gain K_r is calculated and can be chosen. With all three parameters selected, the system loop gain is analyzed and its frequency response is plotted to graphically represent the designed system performance. The following subsections detail each step of the procedure.

3.3.1 Controller constraints

It is desirable to establish constraints for the final controller performance metrics at the beginning of the design procedure so that the control variables are delimited by extremum that will insure a specific and desired system frequency response. In this case, the constraints are:

1. The minimum value of the magnitude of the loop gain at fundamental frequency, denoted T_{f_o}, to insure minimal steady-state error and fast response time;
2. The minimum phase margin to provide a good dynamic performance;
3. The minimum gain margin to insure controller stability and robustness;

The following sections present the functions that are derived from these constraints to determine extremum values for the control variables.

3.3.1.1 Steady-state error constraint

The steady-state error of the current at the fundamental frequency is effectively related to the magnitude of the loop gain at the fundamental frequency T_{f_0}, as demonstrated in (Bao *et al.*, 2014) and summarized in Annex III. As previously mentioned, the designed controller should move the system crossover frequency f_c to a value low enough so that the phase margin is not impacted by the negative phase shift introduced by the filter resonance and high enough so that it is not impacted by the negative phase shift introduced by the PR controller resonance. Hence, as shown in Figure 3.10, at the crossover frequency and lower, the equivalent impedance of the filter capacitor branch becomes high enough compared to the grid-side inductor impedance that it may be considered as an open circuit. In this case, the magnitude of the loop gain of equation (3.14) can be expressed as:

$$|T(s)| \approx \left| \frac{G_i(s) \cdot K_{PWM}}{(L_1 + L_2) \cdot s} \right| \tag{3.19}$$

Furthermore, at the fundamental frequency, the PR controller transfer function of equation (3.18) can be simplified as:

$$G_{PR}(2\pi f_o) = K_p + K_r \tag{3.20}$$

The magnitude of the loop gain at the fundamental frequency can then be expressed by replacing $G_i(s)$ in equation (3.19) by (3.20) as:

$$T_{f_0} = 20 \log |T(2\pi f_o)| = 20 \log \left| \frac{(K_p + K_r) \cdot K_{PWM}}{(L_1 + L_2) \cdot 2\pi f_o} \right| \tag{3.21}$$

As observed in the Bode diagram of Figure 3.7, at the crossover frequency and higher, the resonant term of the PR controller transfer function of equation (3.18) becomes negligible and the controller magnitude can be approximated as:

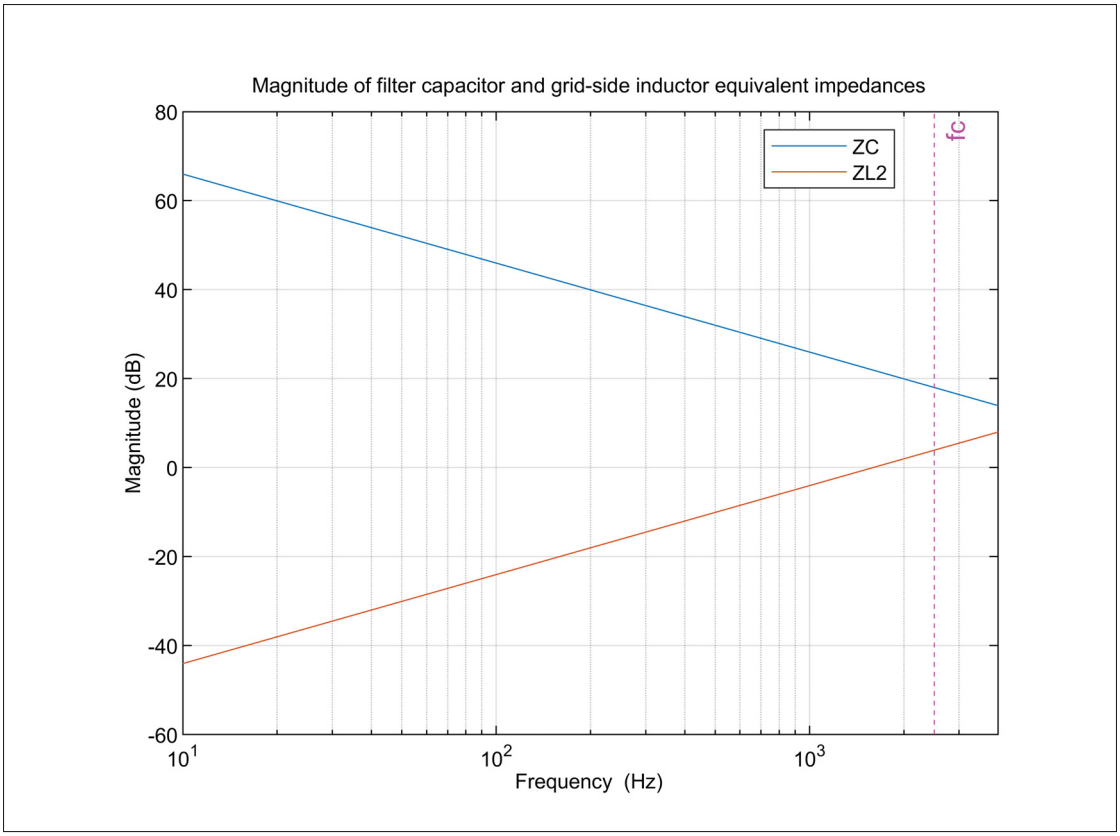

Figure 3.10 Magnitude of filter capacitor and grid-side inductor equivalent impedances

$$|G_{PR}(2\pi f_c)| \approx K_p \tag{3.22}$$

Considering that the magnitude of the loop gain at the crossover frequency is unitary and substituting $G_i(s)$ given by (3.22) in equation (3.19) yields expression (3.23) for the PR controller proportional gain as a function of the crossover frequency:

$$K_p \approx \frac{(L_1 + L_2) \cdot 2\pi f_c}{K_{PWM}} \tag{3.23}$$

Using (3.23) in (3.21), one can derive expression (3.24) for the PR controller resonant gain considering the steady-state error constraint:

$$K_{r\_T_{fo}} = \left(10^{\frac{T_{fo}}{20}} f_o - f_c\right) \cdot \frac{(L_1 + L_2) \cdot 2\pi}{K_{PWM}} \tag{3.24}$$

3.3.1.2 Stability constraint

To evaluate the stability of the system at this stage of the design process, one may refer to a derivation of the Nyquist stability criterion that allows to predict the system closed-loop stability using the loop gain of equation (3.14) in the frequency domain. To summarize the criterion, it can generally be concluded that the closed-loop system is stable if the loop gain frequency response has a positive gain margin and phase margin. Larger positive margins translate into greater system stability and robustness, implying that it can withstand larger perturbations. Furthermore, increasing the phase margin of a system reduces the percent overshoot in the transient response, hence improving its dynamic performance (Nise, 2000).

The phase margin (PM) is defined as the number of degrees above -180°at the crossover frequency, or:

$$PM = 180^\circ + \angle T(j2\pi f_c) \tag{3.25}$$

Applying this definition to the system loop gain equation of (3.14) yields:

$$PM = 180^\circ + \angle \left(G_i(s) \cdot \frac{K_{PWM}}{L_1 L_2 C \cdot s^3 + L_2 C H_{i1} K_{PWM} \cdot s^2 + (L_1 + L_2) \cdot s}\right)\Bigg|_{s=j2\pi f_c} \tag{3.26}$$

Since the crossover frequency is much larger than the controller bandwidth ω_i and the resonance frequency $\omega_r = \omega_o$, the PR controller transfer function of (3.18) at the crossover frequency can be approximated as (3.27):

$$G_{PR}(2\pi f_c) \approx K_p + \frac{K_r \omega_i}{\pi f_c} \tag{3.27}$$

Substituting $G_i(s)$ in (3.26) by (3.27) and simplifying, the system phase margin can be rewritten as:

$$PM = \arctan\left(\frac{2\pi L_1 (f_{res}^2 - f_c^2)}{H_{i1} K_{PWM} f_c}\right) - \arctan\left(\frac{K_r \omega_i}{\pi f_c K_p}\right) \tag{3.28}$$

One observes that the phase shift induced by the filter resonance is taken into account in the phase margin calculation. Solving (3.28) for K_r, expression can be derived for the PR controller resonant gain considering the stability constraint of the phase margin:

$$K_{r\_PM} = \frac{\pi f_c K_p}{\omega_i} \cdot \frac{2\pi L_1 (f_{res}^2 - f_c^2) - H_{i1} K_{PWM} f_c \tan(PM)}{H_{i1} K_{PWM} f_c + 2\pi L_1 (f_{res}^2 - f_c^2) \tan(PM)} \tag{3.29}$$

The two expressions that were obtained in (3.24) and (3.29) allow to derive values for the PR controller resonant gain as a function of the system loop gain crossover frequency and constraints of T_{f_o} (i.e. steady-state error) and PM (i.e. stability). By combining them, the resulting resonant gain complies with both constraints at the same time, that is to say $K_{r\_T_{fo}} = K_{r\_PM}$. Furthermore, substituting K_p in (3.29) by (3.23) and solving for H_{i1}, one gets the first expression for the capacitor current feedback gain constrained by the requirements of T_{f_o} and PM:

$$H_{i1\_T_{fo}\_PM} = \frac{2\pi L_1 (f_{res}^2 - f_c^2)}{K_{PWM} f_c} \cdot \frac{\pi f_c^2 - (10^{\frac{T_{fo}}{20}} f_o - f_c)\omega_i \tan(PM)}{(10^{\frac{T_{fo}}{20}} f_o - f_c)\omega_i + \pi f_c^2 \tan(PM)} \tag{3.30}$$

The gain margin (GM) of a system is defined as the number of decibels (dB) below 0 of the loop gain magnitude when the phase crosses -180°, or:

$$GM(dB) = -20\log|T(j2\pi f_{180^\circ})| \tag{3.31}$$

As observed on the Bode diagram of Figure 3.4, the loop gain frequency response crosses -180°at the resonance frequency f_{res}. Applying the definition of the gain margin to the system loop gain equation of (3.14) and substituting the PR controller proportional gain K_p by its equation given in (3.23), one solves and derives the second equation for the capacitor current feedback gain considering the stability constraint of the gain margin:

$$H_{i1\_GM} = 10^{\frac{GM}{20}} \cdot \frac{2\pi f_c L_1}{K_{PWM}} \tag{3.32}$$

3.3.1.3 Pulse-width modulation constraint

Another function is derived to limit the maximum value of the capacitor current feedback gain based on a constraint given by the pulse-width modulator. As shown on Figures 3.1 and 3.2, the control system output is the modulating signal sent to the PWM system to produce the inverter output voltage. To avoid multi pulses switching resulting in output signal degradation, the rate of change of the modulating signal must be inferior to the rate of change of the PWM carrier (Zmood & Holmes, 2003). This constraint translates into the following equation:

$$\frac{H_{i1}V_{DC}}{L_1} < 4V_{tri}f_{sw} \tag{3.33}$$

Equation (3.33) is rewritten to obtain the third equation for the capacitor current feedback gain limited by the PWM constraint:

$$H_{i1\_PWM} = \frac{4f_{sw}L_1}{K_{PWM}} \tag{3.34}$$

To summarize, a set of three equations comprised of (3.30), (3.32) and (3.34) were derived in order to establish a relationship between the system loop gain crossover frequency f_c and the capacitor current feedback gain H_i1 based on the constraints of steady-state error and stability. Plotting this set of equations allows to graphically observe the range of acceptable values for f_c and H_i1, which is the area bounded by the resulting curves as shown in the next section.

3.4 Results and discussion

3.4.1 Applied design procedure

Following the procedure shown in Figure 3.9 and detailed in the previous section, the current controller can now be designed. The first step is to select the desired inverter parameters, which are given in Table 1.1. The controller constraints given in Section 3.3.1 are then selected as follows:

1. The magnitude of the loop gain at fundamental frequency $T_{f_o} = 75dB$ to insure high reference tracking accuracy and minimal steady-state error;
2. The minimum phase margin $PM = 45°$ to insure stability and good dynamic performance;
3. The minimum gain margin $GM = 6dB$ to insure stability and robustness;

Substituting these constraints in equations (3.30), (3.32) and (3.34) and plotting the resulting functions, the graph shown in Figure 3.11 is obtained, where one clearly observes the range of acceptable values for f_c and H_i1.

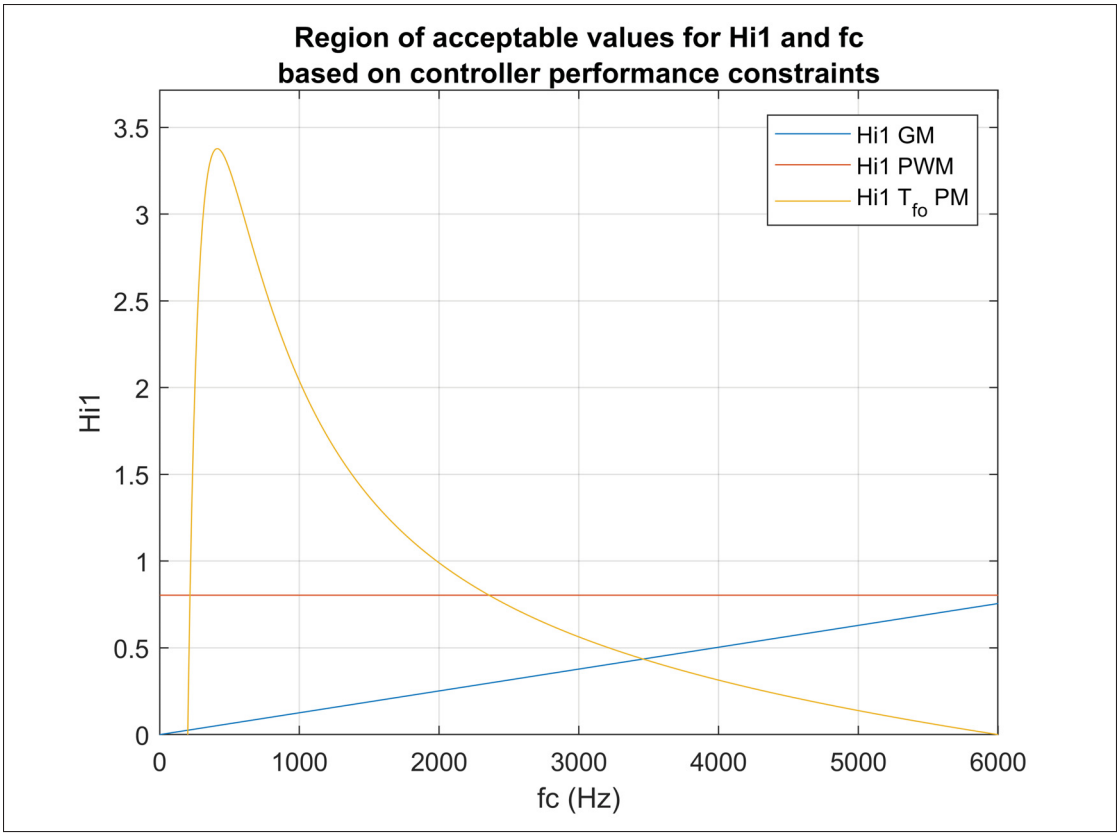

Figure 3.11 Region of acceptable values for H_{i1} and f_c based on controller performance constraints

A crossover frequency of $f_c = 2.5$kHz is selected, which corresponds to an acceptable range of $0.3148 \leq H_{i1} \leq 0.7416$ for the capacitor current feedback gain. A value of $H_{i1} = 0.35$ is selected. From equation (3.23), the controller proportional gain is calculated to be $K_p = 0.181$. With f_c, K_p and H_{i1} selected, equations (3.24) and (3.29) are used to calculate the range of acceptable values for the controller resonant gain, which results in $24.25 < K_r < 1373.91$. As demonstrated in (Castilla, Miret, Matas, Garcia de Vicuna & Guerrero, 2009), setting $K_r = \omega_r = \omega_o$ yields good dynamic response, $K_r = 377$ is then selected. This completes the design of the control variables, which are summarized in Table 3.1.

Table 3.1 Control system parameters

Parameter	**Value**
PR controller proportional gain K_p	0.181
PR controller resonant gain K_r	377
Loop gain crossover frequency f_c	2.5kHz
Capacitor current feedback gain H_{i1}	0.35

3.4.2 Frequency response analysis

Substituting the values contained in Tables 1.1, 2.2 and 3.1 in the system loop gain of equation (3.14), the frequency response of the compensated is obtained, as shown on the Bode diagram of Figure 3.12. The uncompensated loop gain ($G_i = 1$ and $H_{i1} = 1e^{-6}$) frequency response is also shown. It can be observed that the compensated system characteristics are all in agreement with the constraints that were given. More specifically, the gain margin $GM = 6.58$, the phase margin $PM = 56.15$ and the magnitude of the loop gain at fundamental frequency $T_{f_o} = 98.8dB$. Furthermore, the LCL filter resonance is effectively damped. The compensated system crossover frequency is located at $f_c = 2.81$kHz, which is slightly different than the theoretical value of 2.5kHz that was selected during the design process. This difference is due in part to the approximations made for the derivation of the controller constraints equations, particularly (3.22), (3.23) and (3.27). Nonetheless, the result is satisfactory and it can concluded, based on the Nyquist stability criterion, that the inverter system will be stable in closed loop.

The stability of the designed system can be analyzed further by using the tracking and disturbance transfer functions that were defined in section 3.1 and repeated here for convenience.

$$i_{2T}(s) = \frac{T(s)}{1 + T(s)} \tag{3.35}$$

$$i_{2D}(s) = -\frac{G_2(s)}{1 + T(s)} \tag{3.36}$$

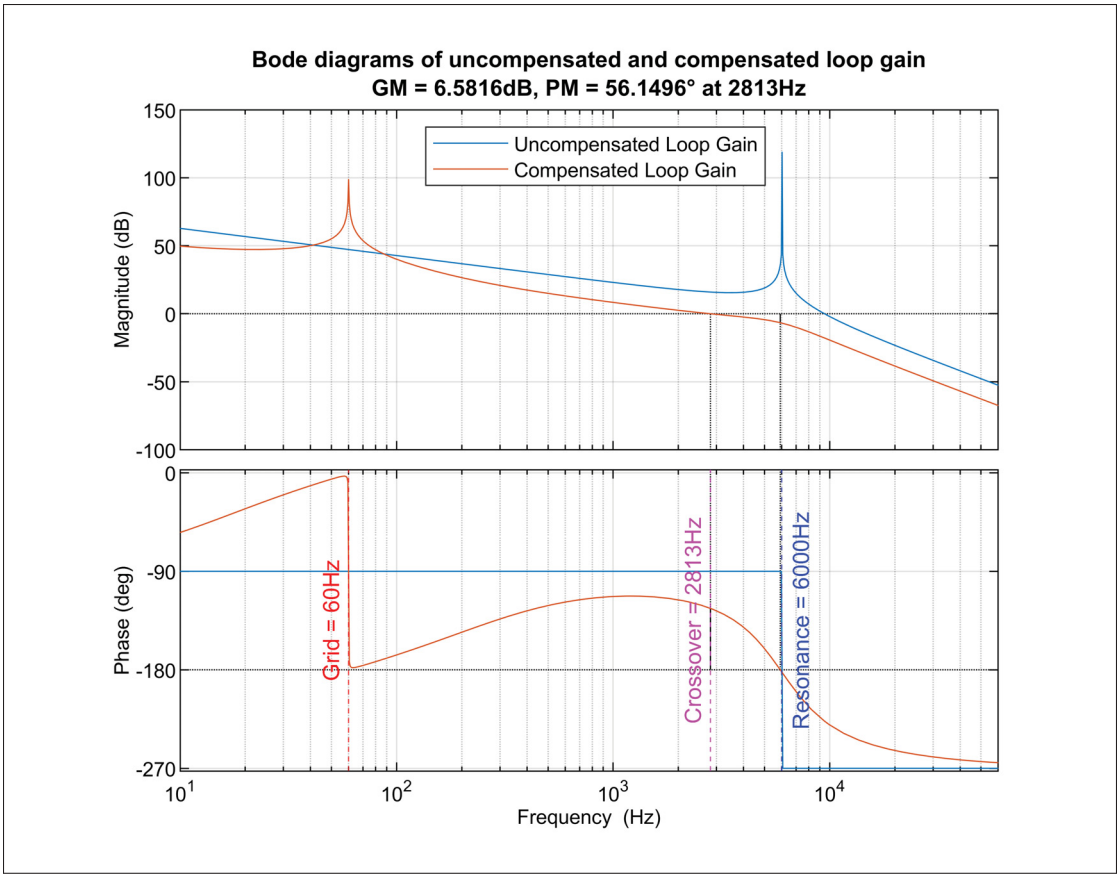

Figure 3.12 Bode diagrams of the compensated and uncompensated loop gain

The tracking transfer function of equation (3.35) establishes the relationship between the inverter output current and the current reference. Its frequency response is shown in the Bode diagram of Figure 3.13. One can observe that at the nominal grid frequency the gain and phase are both $0dB$ and $0°$ which means that the output current will effectively track the reference without steady-state error.

The disturbance transfer function of equation (3.36) establishes the relationship between the inverter output current and the grid voltage. Its frequency response is shown in the Bode diagram of Figure 3.14. It presents a low gain at lower frequencies and particularly at the nominal grid frequency where the gain is $-87.6dB$, which means that the designed system presents good rejection capabilities against perturbations in the grid voltage.

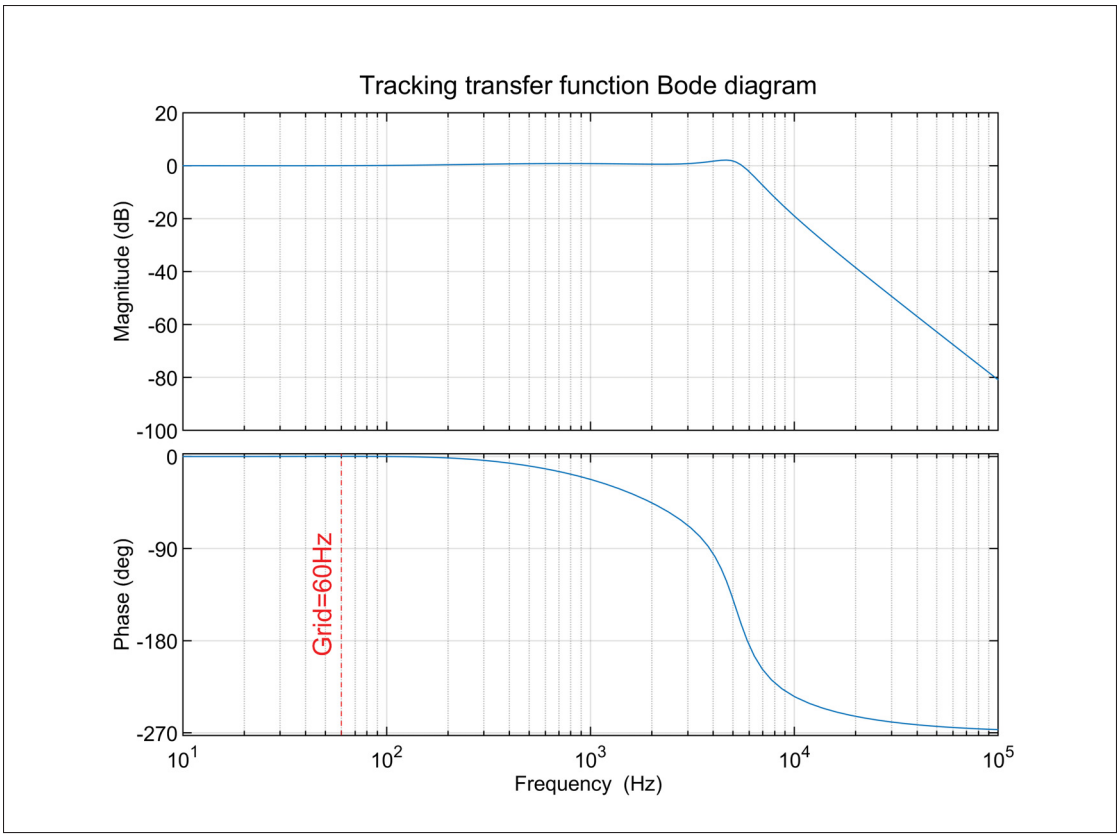

Figure 3.13 Tracking transfer function Bode diagram

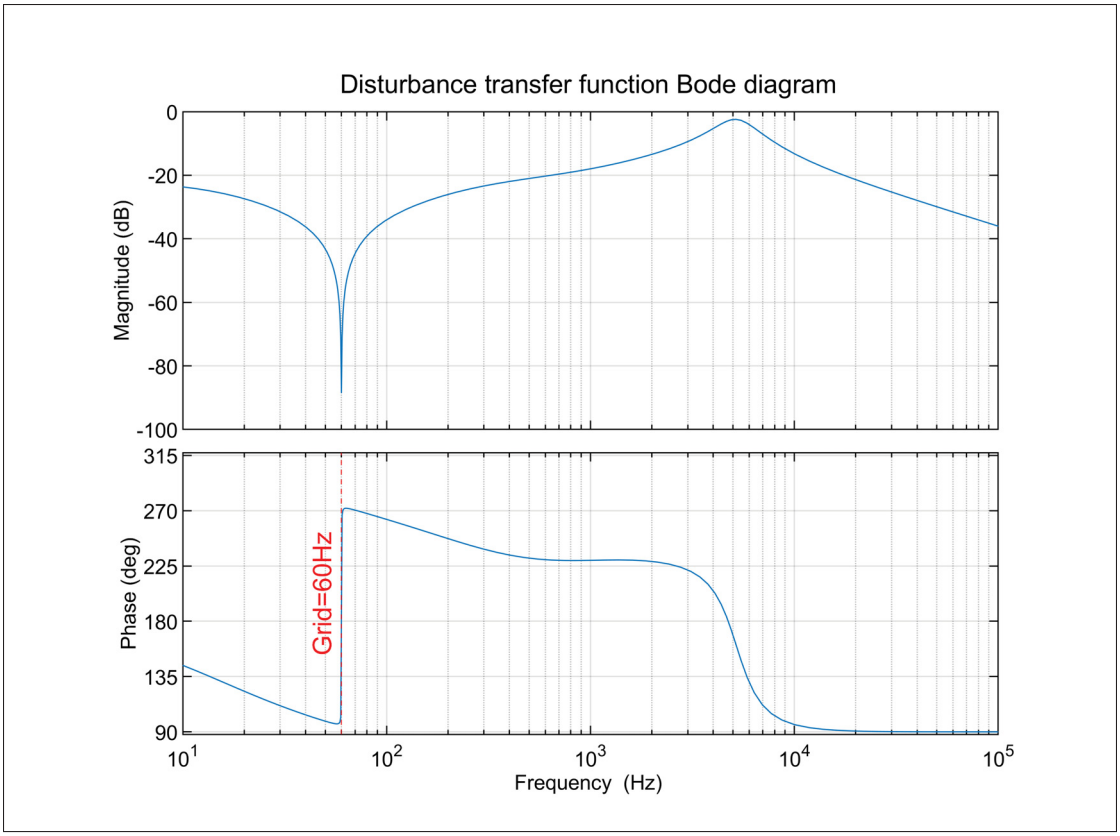

Figure 3.14 Disturbance transfer function Bode diagram

3.4.3 Impact of grid impedance

The performance and stability of grid-connected inverters are impacted by the strength of the grid as seen from the point of connection (PoC) of the inverter, which can be defined by the short-circuit ratio (SCR). As implied by its name, the SCR is the ratio between the short-circuit power at the PoC, $S_{PoC} = \frac{V_s^2}{Z_g}$, and the nominal inverter apparent power S_{nom}, or:

$$SCR = \frac{S_{PoC}}{S_{nom}} = \frac{V_s^2}{Z_g \cdot S_{nom}} \tag{3.37}$$

By convention, it is considered that the inverter is connected to a strong grid if $SCR \geq 20$ and a weak grid if $SCR \leq 10$ (Etxegarai, Eguia, Torres, Iturregi & Valverde, 2015). From equation

(3.37), it can be seen that an increase in Z_g reduces the SCR. This corroborates what is shown in the Bode diagram of Figure 3.6, where an increase in grid inductance reduces the loop gain resonance and crossover frequencies, hence the system bandwidth and phase margin. Figures 3.15 and 3.16 further demonstrate how a variation of the grid inductance from a strong, near ideal grid ($L_g = 0.01mH$, $SCR \approx 3000$) to a weak grid ($L_g = 8mH$, $SCR \approx 3.8$) impacts the loop gain frequency response and phase margin. The latter sharply decreases from 55° to 35° then slowly keeps decreasing. The loop gain of equation (3.13) is used in order to take into account the grid impedance.

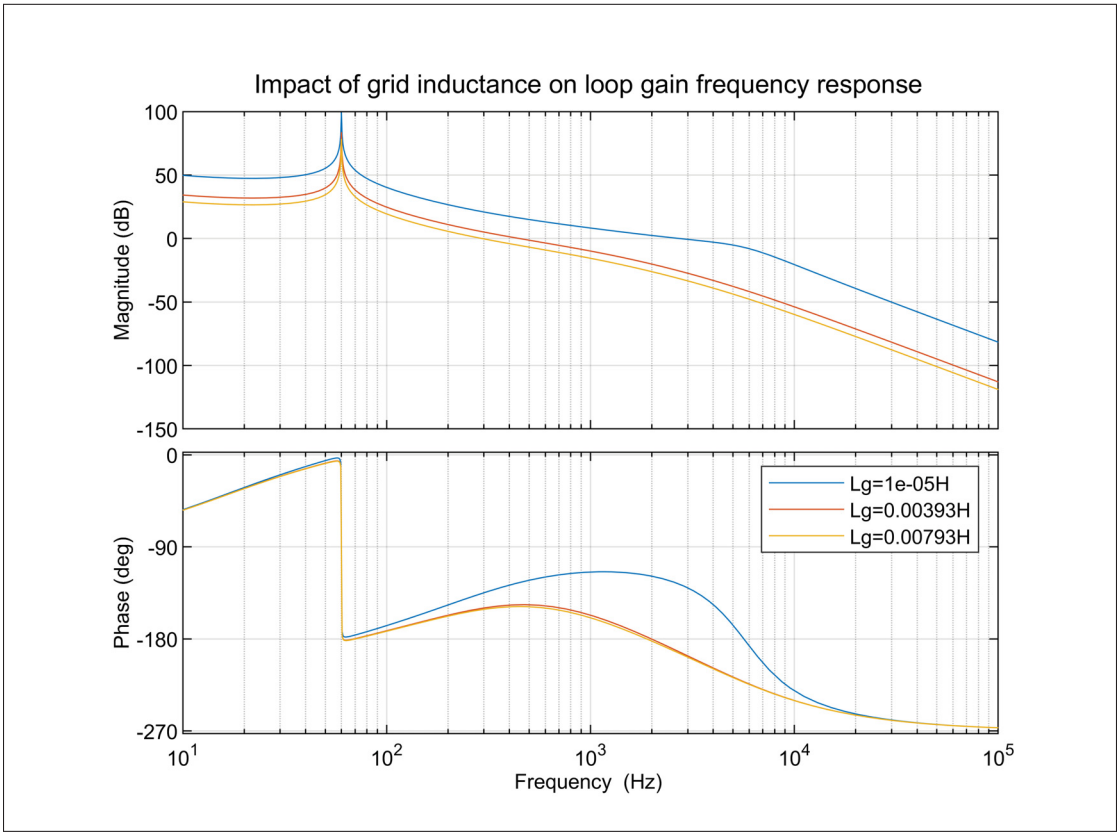

Figure 3.15 Bode diagram of loop gain frequency response for varying grid impedance

The script used to evaluate the impact of the inverter output filter and equivalent grid impedance on the loop gain phase margin is presented in Annex V. For the current work, in order to properly demonstrate the effectiveness of inverter grid support functions on voltage and frequency, a

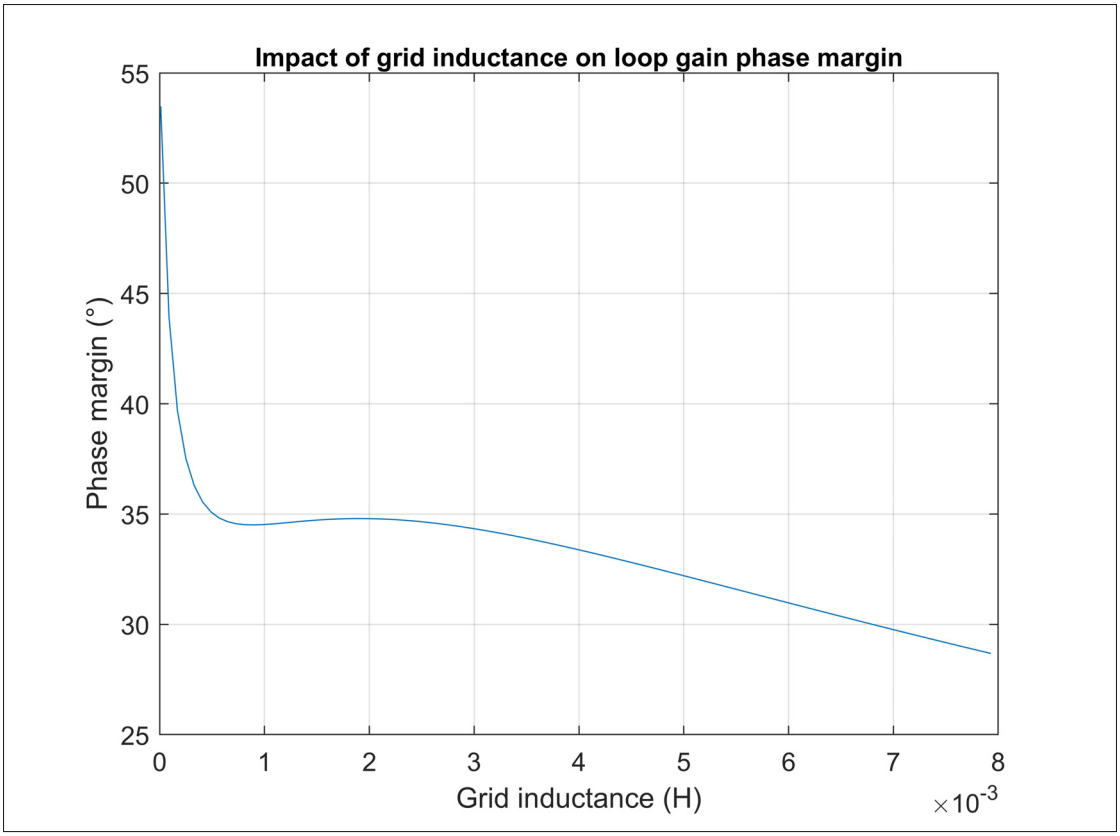

Figure 3.16 Loop gain phase margin for varying grid impedance

weak grid will be used in the simulation models. Indeed, when an inverter is connected to a strong grid, changes in its active and reactive power have virtually no impact. Using a SCR of 10, the equivalent grid inductance will be:

$$L_g = \frac{\frac{V_s^2}{SCR \cdot S_{nom}}}{\omega_o} = 3.1mH \tag{3.38}$$

The loop gain frequency response of the system under study is shown in the Bode diagram of Figure 3.17. Compared to the Bode diagram of the system connected to an ideal grid, shown in Figure 3.12, it can be observed that, as demonstrated, the crossover frequency and phase margin have decreased to $f_c = 518Hz$ and $PM = 34.3°$ respectively. Although this reduction in bandwidth indicates that the system will have a slower response time to changes in the reference,

one can still conclude that the inverter system will be closed-loop stable based on the Nyquist stability criterion. The tracking and disturbance transfer functions frequency responses shown in Figures 3.18 and 3.19 also indicate that the output current will still effectively track the reference without steady-state error and that the designed system presents good rejection capabilities against perturbations in the grid voltage at nominal frequency.

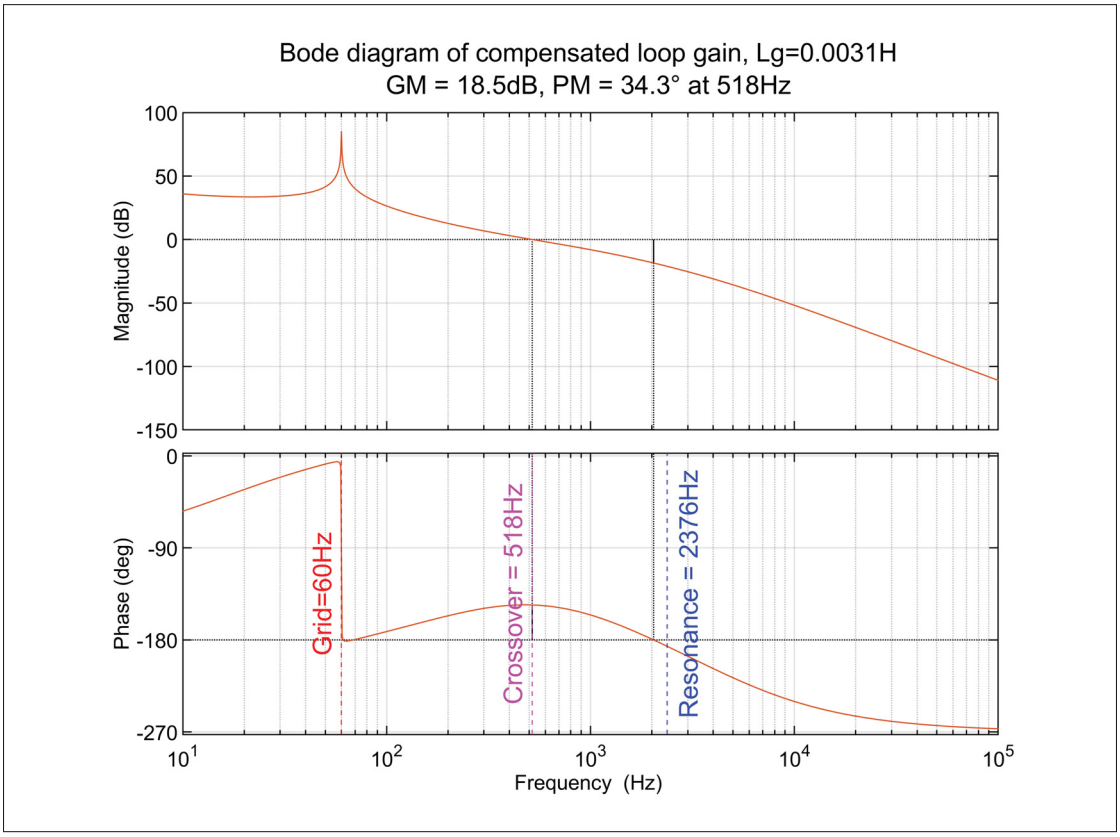

Figure 3.17 Bode diagram of loop gain frequency response with $L_g = 3.1mH$

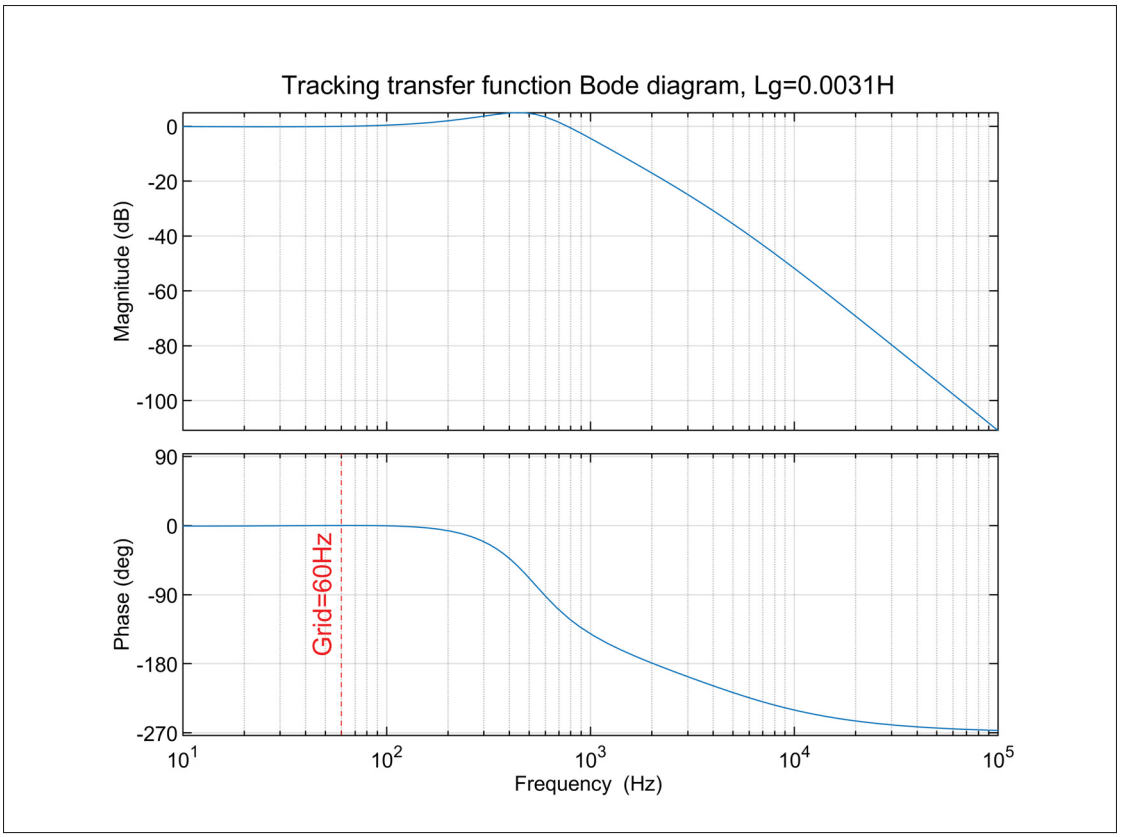

Figure 3.18 Bode diagram of tracking transfer function with $L_g = 3.1mH$

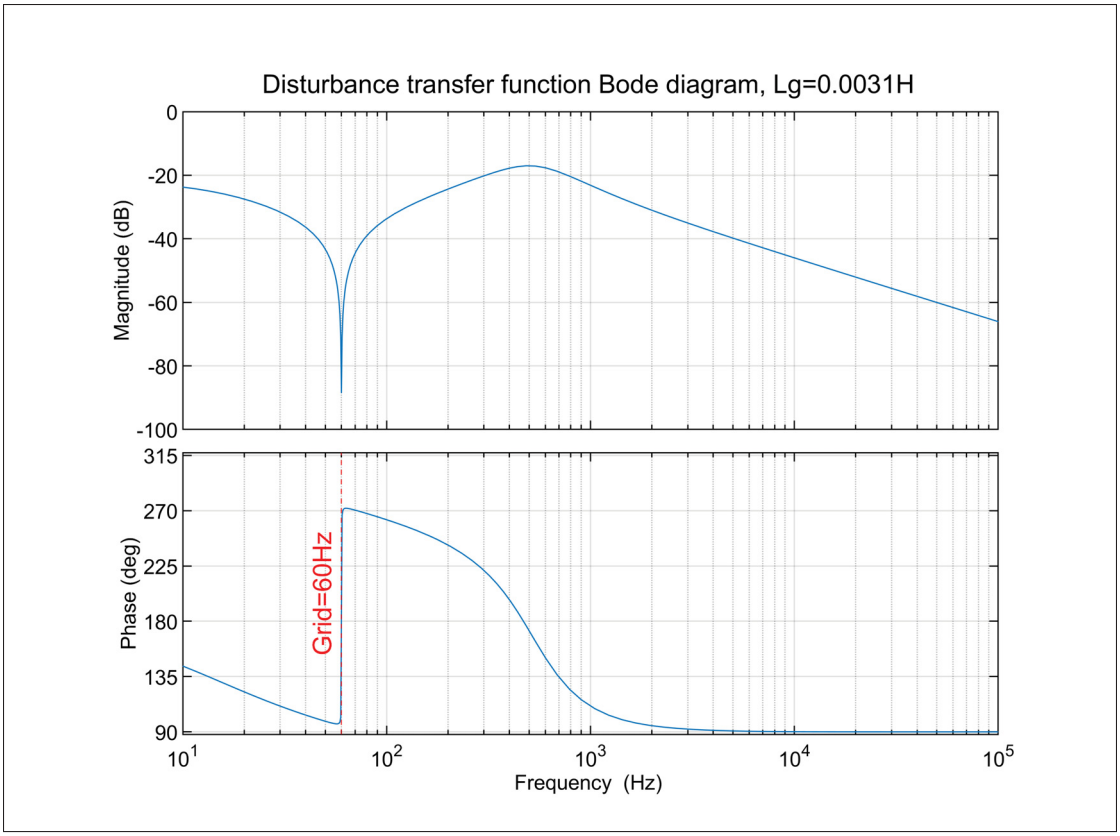

Figure 3.19 Bode diagram of disturbance transfer function with $L_g = 3.1mH$

3.4.4 Simulation results

The designed current controller performance is further evaluated by simulating the model presented in Figure IV-1.

3.4.4.1 Step change in current reference

The first test performed is a -80% step change in the current reference in order to evaluate the dynamic response and stability of the controller. The step is applied at the peak of the rated current value while the inverter is operating at unity power factor. Simulation results are presented in Figure 3.20. The upper graph shows the current reference (orange curve) and the resulting inverter output current (blue curve), while the middle graph shows the error, in

amperes, between the two signals and the bottom graph presents the controller output, i.e., the modulation signal sent to the SPWM. It can be observed that the inverter output current presents zero steady-state error and stabilizes in less than $3ms$ after the step change with a maximum overshoot of $10.9A$ or 36.5% of the rated current. Figure 3.20 also shows the current reference and output current as well as the voltage at the PoC. The step change in inverter output current is reflected in the voltage waveform, due to the weak grid condition. These results demonstrate that the designed controller has a good dynamic response and is stable even when connected to a weak grid and for a large step change.

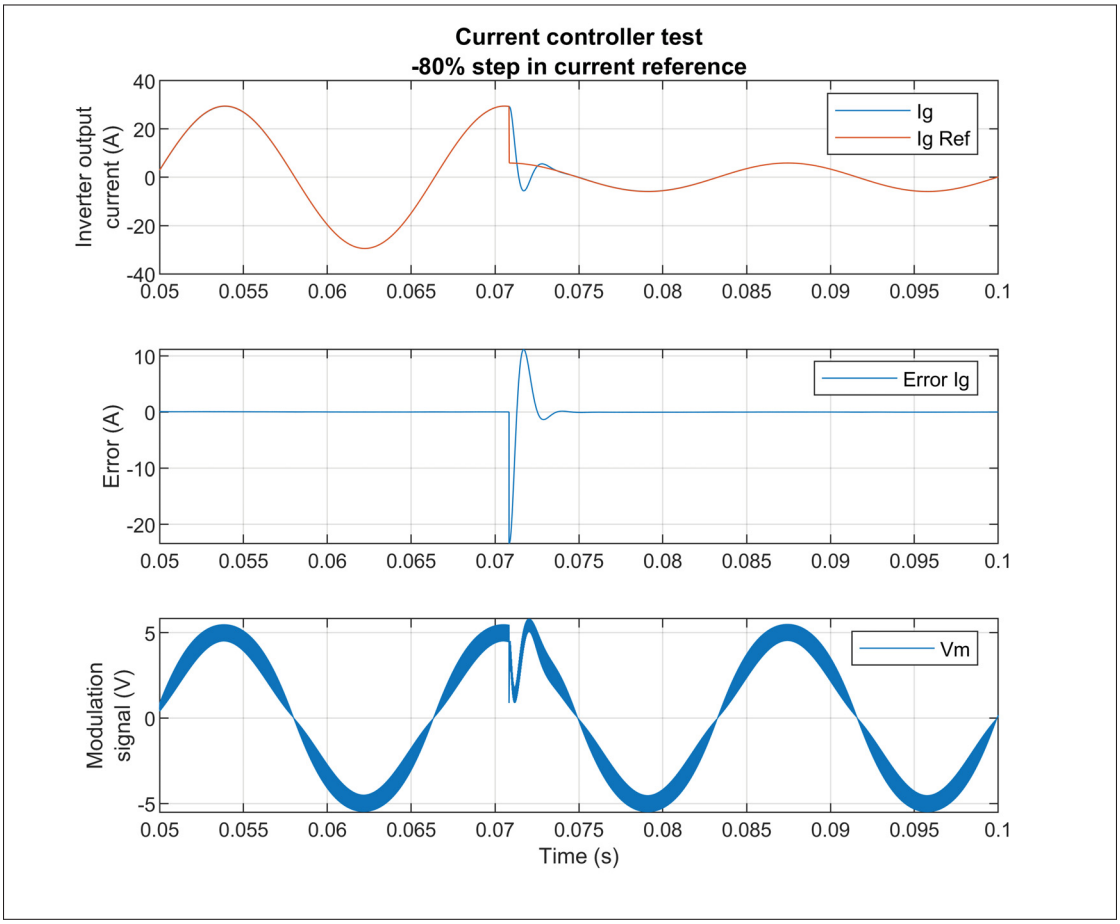

Figure 3.20 Current controller simulation results, -80% step change in current reference. Output current, error and duty cycle

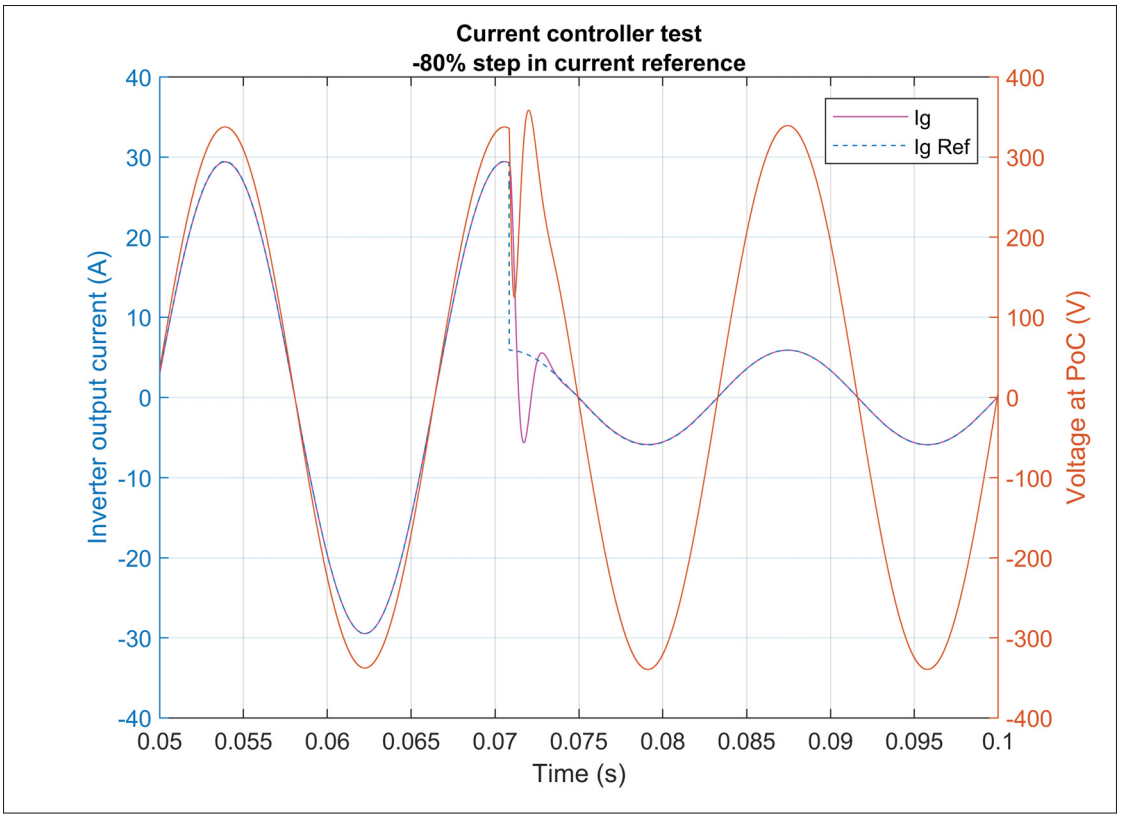

Figure 3.21 Current controller simulation results, -80% step change in current reference. Output current and voltage at PoC

3.4.4.2 Negative step change in grid voltage

The second test performed is a -60% step change in the grid voltage (from nominal value to $0.4p.u.$) in order to evaluate the controller response to external perturbations. According to the voltage ride-through requirements of (IEEE, 2018), the inverter shall be able to operate at a voltage level of $0.5p.u.$. The step is applied at the peak of the grid voltage instantaneous value while the inverter is operating at unity power factor. Simulation results are presented in 3.22 where the upper graph shows the current reference (orange curve) and the resulting inverter output current (blue curve), while the middle graph shows the error, in amperes, between the two signals and the bottom graph presents the controller output, i.e., the modulation signal sent to the SPWM and Figure 3.23 where the voltage at the PoC and the inverter reference and output

currents are shown. It can be observed that the inverter output current stabilizes in less than a half-cycle, or $7ms$ after the step change is applied, with a maximum overshoot of $16.2A$ or 55% of the rated current. These results demonstrate that the designed controller has a good rejection capability and is stable even when submitted to large perturbations in the grid voltage, which indicates that the under-voltage ride-through requirements of the interconnection standard are met.

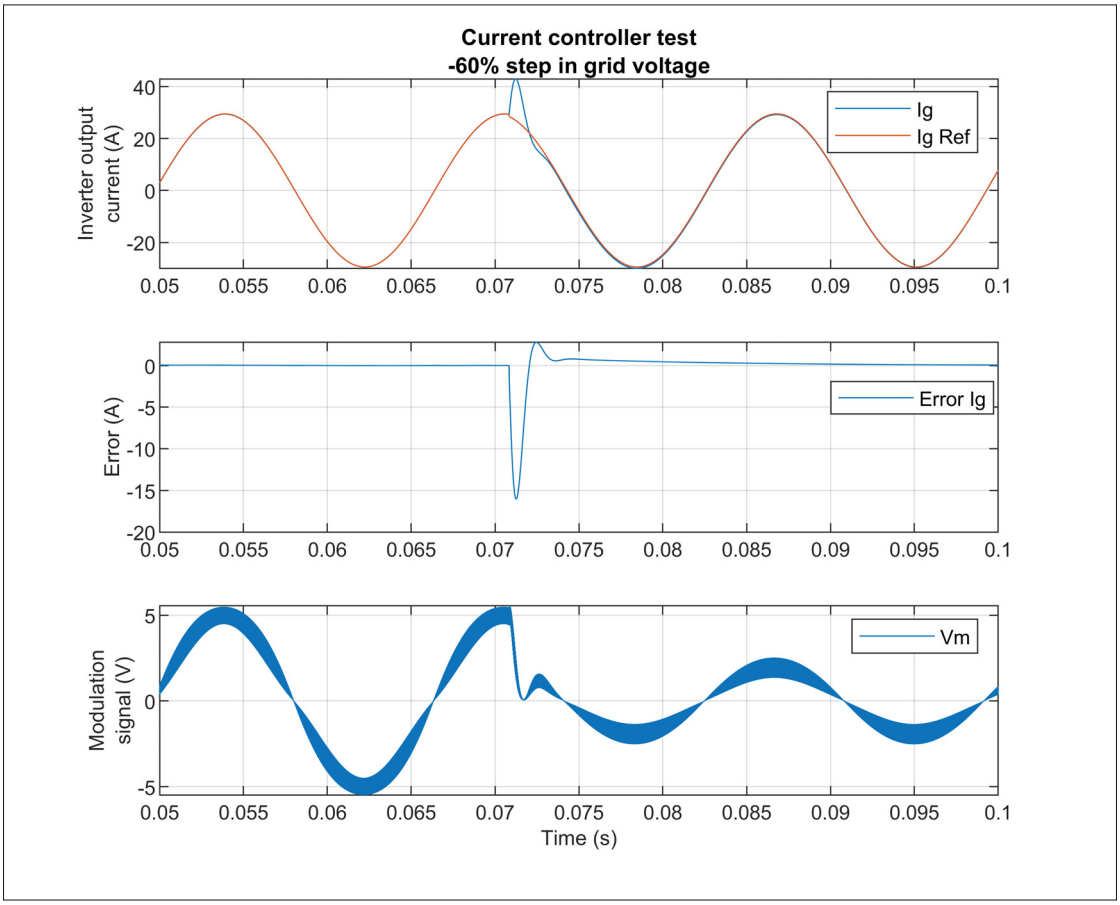

Figure 3.22 Current controller simulation results, -60% step change in grid voltage. Output current, error and duty cycle

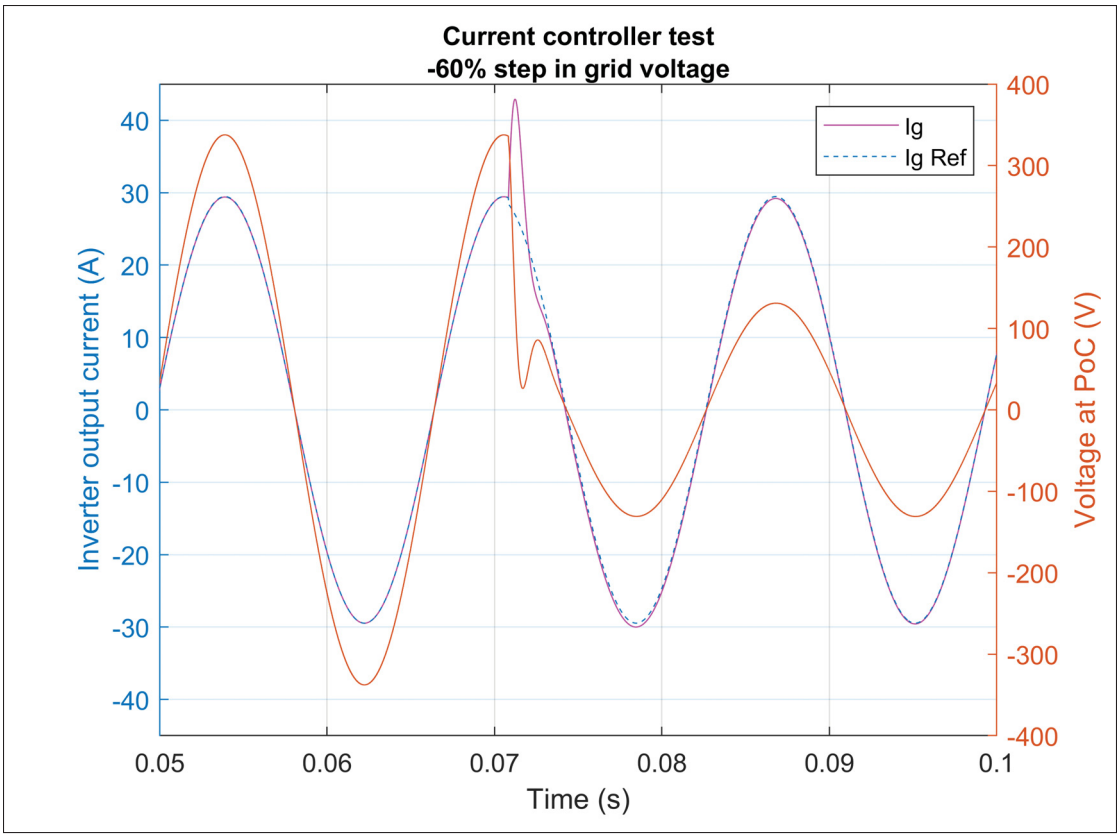

Figure 3.23 Current controller simulation results, -60% step change in grid voltage. Output current and voltage at PoC

3.4.4.3 Positive step change in grid voltage

The third test performed is a +25% step change in the grid voltage (from nominal value to $1.25p.u.$). According to the voltage ride-through requirements of (IEEE, 2018), the inverter shall be able to operate at a voltage level of $1.1p.u.$. The step is applied at the peak of the grid voltage instantaneous value while the inverter is operating at unity power factor. Simulation results are presented in 3.24 where the upper graph shows the current reference (orange curve) and the resulting inverter output current (blue curve), while the middle graph shows the error, in amperes, between the two signals and the bottom graph presents the controller output, i.e., the modulation signal sent to the SPWM and Figure 3.25 where the voltage at the PoC and the inverter reference and output currents are shown. The inverter output current stabilizes in

less than a half-cycle, or $7ms$ after the step change is applied, with a maximum overshoot of $6.5A$ or 22% of the rated current. These results demonstrate that the over-voltage ride-through requirements of the interconnection standard are met.

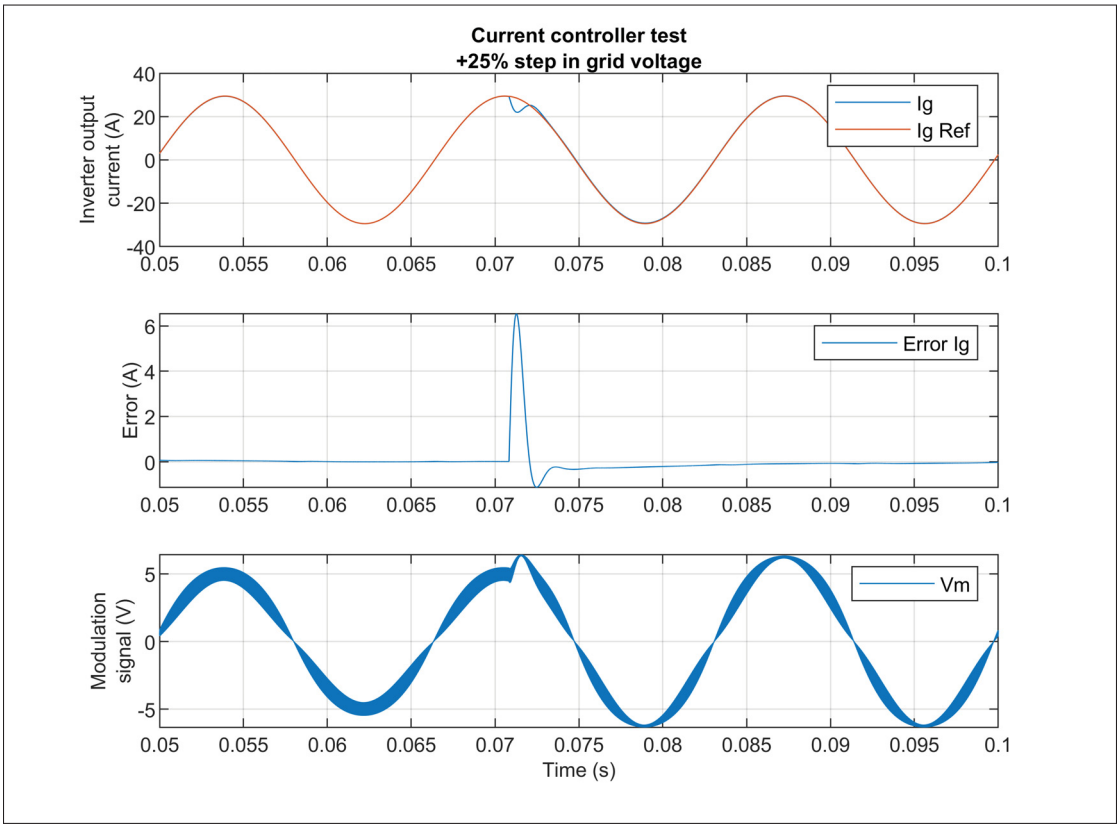

Figure 3.24 Current controller simulation results, +25% step change in grid voltage. Output current, error and duty cycle

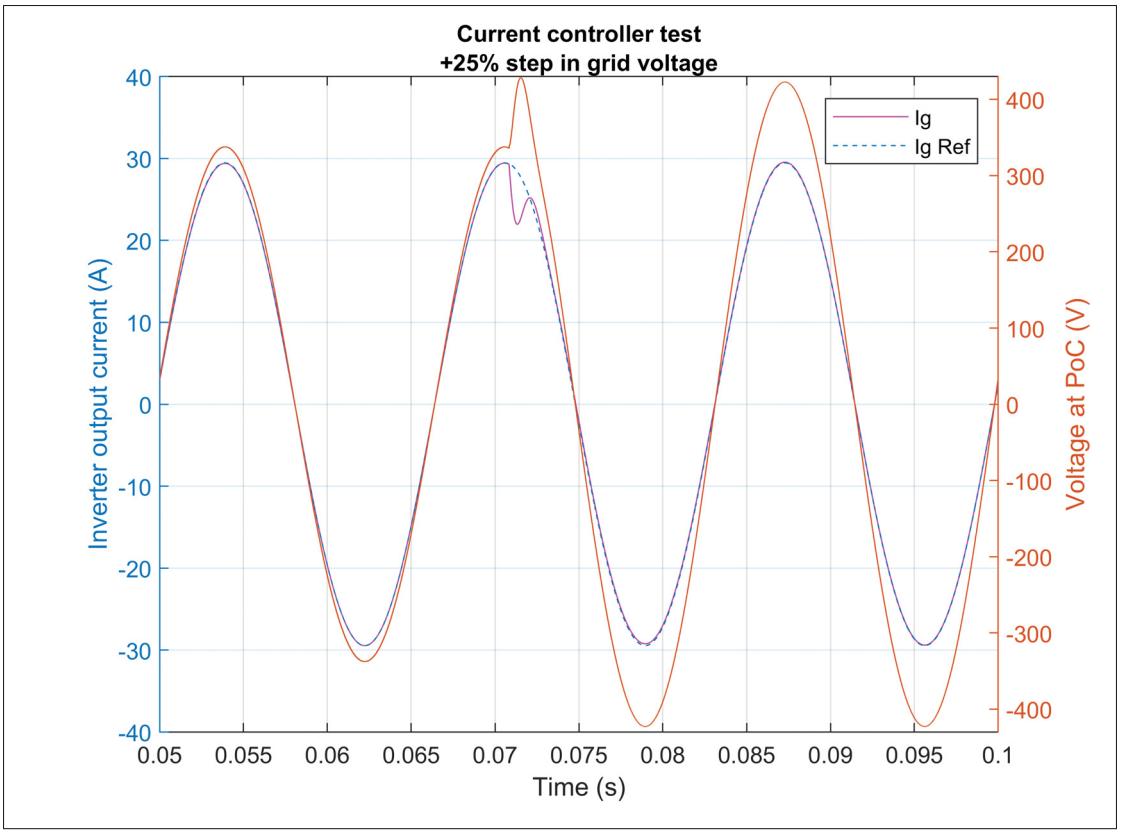

Figure 3.25 Current controller simulation results, +25% step change in grid voltage. Output current and voltage at PoC

3.5 Conclusion

In this chapter, the mathematical model of the grid-connected inverter system was first derived and the required transfer functions and expressions were derived to analyze its stability once the current controller is designed. The proportional-resonant controller was then presented and a step-by-step procedure was introduced in order to optimally design the controller with regards to the desired closed-loop performance requirements (i.e., steady-state error, gain and phase margins) and system constraints (i.e. PWM maximum rate of change). The design procedure was applied to the system under study and the current controller parameters were calculated. Previously derived transfer functions were used to theoretically analyze the system frequency response and the impact of various system parameters on the stability and performance

were discussed, namely the grid impedance and capacitor-current feedback gain. A simulation model of the grid-connected inverter was developed in Matlab/Simulink to perform various tests on the current controller. It was demonstrated that even when connected to a weak grid, the designed inverter system is stable, provides good dynamic performance and perturbation rejection capabilities which indicates that it can meet the interconnection standard requirements in terms of response to abnormal conditions.

CHAPTER 4

PHASE-LOCKED LOOP

The previous chapter details how the current controller modulates the inverter current output so that it follows a current reference. This current reference must be synchronized to the grid voltage signal in order to allow the inverter to effectively control the power exchange with the grid at its point of connection. A phase-locked loop (PLL) is a control system that can track a sinusoidal signal at its input by controlling and minimizing the error in the phase of its output signal. Using a PLL, the phase and frequency of the grid voltage can then be obtained and used to generate the current reference signal, allowing to control the inverter output frequency, active and reactive power and concomitantly implement the advanced grid support functions detailed in Chapter 5.

The objective of the current chapter is to present the general structure of a PLL and to detail the topology of the one used for the inverter under study. The key performance factors will be outlined and the designed PLL performance will be evaluated using simulations.

4.1 PLL topology, modeling and design

The PLL topology used for the current work is presented in the block diagram of Figure 4.1. It is essentially composed of three parts, namely the phase detector, the loop filter and the voltage-controlled oscillator (VCO). The phase detector generates an error signal proportional to the angle error between the sensed grid voltage signal $v_g(t)$ and the VCO output signal $v'_g(t)$. The error is then passed to the loop filter, which is typically a proportional-integral (PI) controller that allows to control and eliminate the phase error in steady state and filter out the high-frequency components in the error signal since the PI controller provides low-pass filter characteristics in its frequency response. Finally, the VCO calculates the phase angle, θ_{out}, and generates a sine wave, $v'_g(t)$, from the loop filter output signal and nominal grid angular frequency ω_o, which is in phase and locked with the measured grid voltage signal in steady state.

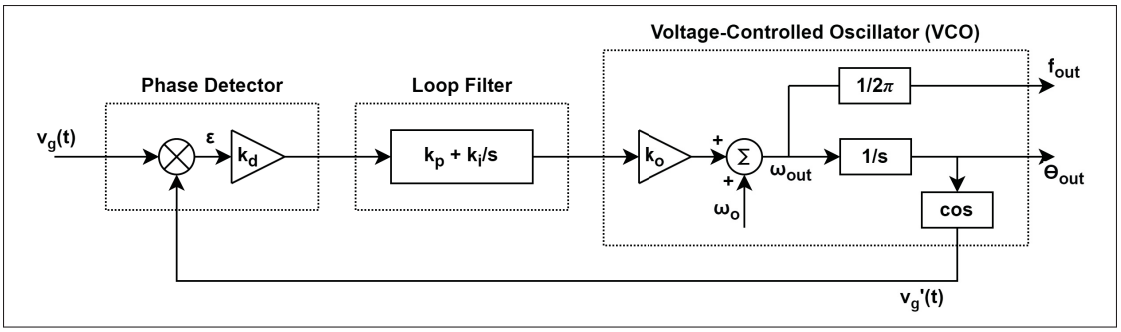

Figure 4.1 PLL general topology

For the current work, the phase detector and VCO gains, namely k_d and k_o, will be considered as unitary so that only the loop filter gains will need to be selected. The measured grid voltage and VCO output can be written as equations (4.1) and (4.2) respectively:

$$v_g(t) = V_g \sin\left(\omega_g t + \theta_g\right) \tag{4.1}$$

$$v'_g(t) = \cos\left(\omega_{PLL} t + \theta_{PLL}\right) \tag{4.2}$$

Where V_g is the measured grid voltage amplitude, ω_g and ω_{PLL} are the grid and estimated angular frequency respectively. θ_g and θ_{PLL} are the grid and estimated phase angle respectively. From the diagram of Figure 4.1, the error calculated by the phase detector is given by equation (4.3).

$$\epsilon = v_g(t) \cdot v'_g(t) = V_g sin(\omega_g t + \theta_g) \cdot cos(\omega_{PLL} t + \theta_{PLL}) \tag{4.3}$$

Using product-to-sum identities, (4.3) can be written as:

$$\epsilon = \frac{V_g}{2}\left[sin((\omega_g + \omega_{PLL})t + (\theta_g + \theta_{PLL})) + sin((\omega_g - \omega_{PLL})t + (\theta_g - \theta_{PLL}))\right] \tag{4.4}$$

It can be observed that the error signal of equation (4.4) is non-linear and contains a term at twice the grid frequency, $sin((\omega_g + \omega_{PLL})t + (\theta_g + \theta_{PLL}))$. As previously mentioned, the loop filter has a low-pass characteristic allowing to filter out higher frequency components in the error signal. However, the PI controller used herein has a low-order transfer function and its frequency roll-off is not sufficient to filter out the term at twice the grid frequency which in this case corresponds to $120Hz$. In order to eliminate this term and linearize equation (4.4), a notch filter, presented in Section 4.1.1, is introduced between the phase detector and loop filter as proposed in (Bhardwaj, 2015). Considering that the term at twice the grid frequency is filtered out, equation (4.4) can be rewritten as:

$$\epsilon = \frac{V_g}{2} sin((\omega_g - \omega_{PLL})t + (\theta_g - \theta_{PLL})) \tag{4.5}$$

During steady-state, the PLL is locked and the error between the measured and approximated signals is considered to be close to zero, so the angular frequency term $\omega_g - \omega_{PLL}$ can be omitted. Furthermore, the small angle approximation indicates that for small angles, $sin(\theta_g - \theta_{PLL}) \approx (\theta_g - \theta_{PLL})$. The error calculated by the phase detector can then be expressed by the linearized equation of (4.6).

$$\epsilon = \frac{V_g}{2}(\theta_g - \theta_{PLL}) \tag{4.6}$$

The PLL closed-loop transfer function between the phase angle approximated value and measured value is given by (4.7):

$$H_{PLL}(s) = \frac{\theta_{out}(s)}{\theta_g(s)} = \frac{V_g(k_{p_{PLL}}s + k_i)}{s^2 + V_g k_{p_{PLL}} s + V_g k_{i_{PLL}}} \tag{4.7}$$

By identification with a generalized second-order transfer function given by (4.8), it is possible to define equations for the damping ratio (ζ) and natural frequency (ω_n) of the PLL, given by equations (4.9) and (4.10) respectively, which relate to the loop filter gains.

$$H_{PLL}(s) = \frac{2\zeta\omega_n s + \omega_n^2}{s^2 + 2\zeta\omega_n s + \omega_n^2} \tag{4.8}$$

$$\zeta = \frac{V_g k_{p_{PLL}}}{2\sqrt{V_g k_{i_{PLL}}}} \tag{4.9}$$

$$\omega_n = \sqrt{V_g k_{i_{PLL}}} \tag{4.10}$$

Solving for the loop filter gains yields equations (4.11) and (4.12).

$$k_{p_{PLL}} = \frac{2\omega_n\zeta}{V_g} \tag{4.11}$$

$$k_{i_{PLL}} = \frac{w_n^2}{V_g} \tag{4.12}$$

The design methodology presented in (Bruyant-Rozoy, 2019) was used to select the loop filter gains. To summarize, this methodology allows to graphically represent the evolution of the PLL response when its damping ratio and natural frequency are varied. More specifically, it verifies the overshoot and settling time in response to a step in the input signal, as well as the cutoff frequency of the PLL. It is then possible to select, from the graphs, optimal values for ζ and ω_n and hence k_p and k_i according to equations (4.11) and (4.12). The selected parameters are summarized in Table 4.1.

Table 4.1 PLL loop filter parameters

Parameter	**Value**
PLL damping ratio ζ	0.9
PLL natural frequency ω_n	200
Loop filter proportional gain $k_{p_{PLL}}$	1.5
Loop filter integral gain $k_{i_{PLL}}$	166.67

These parameters are selected to obtain a settling time around $t = 70ms$ and an overshoot of 10% and the resulting PLL frequency response is shown in the Bode diagram of Figure 4.2, where it can be observed that the magnitude at twice the grid frequency is $G(120Hz) = -9.38$dB, which does not provide enough damping to suppress the component induced at this frequency, hence the need for additional filtering as presented in the next section.

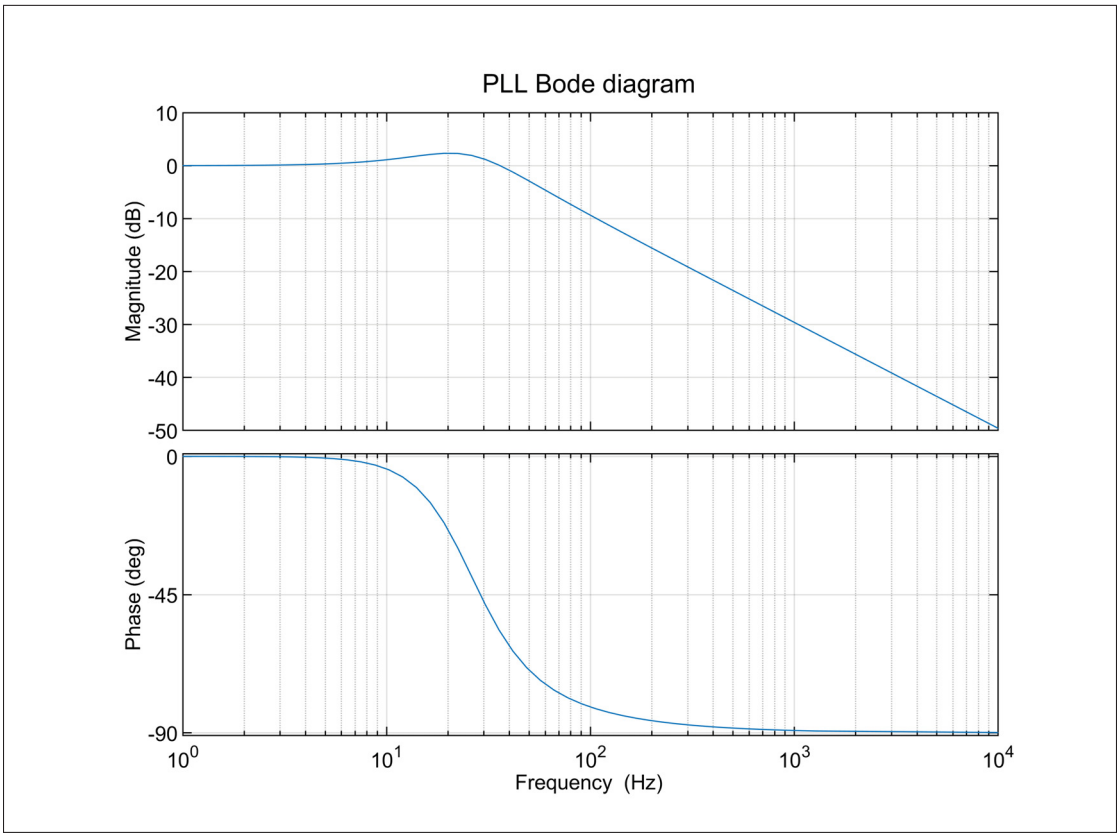

Figure 4.2 PLL Bode diagram

4.1.1 Notch filter

A notch filter has the ability to attenuate components of a signal at and around a specific frequency. This characteristic allows eliminating the term at twice the nominal grid frequency found in equation (4.4) by implementing such filter between the phase detector and loop filter in the PLL topology, as shown in Figure 4.3. Furthermore, by making the notch filter adaptive to the frequency approximated by the PLL, it allows to effectively improve the PLL performance when the grid frequency is off-nominal and the inverter to remain operational in such case.

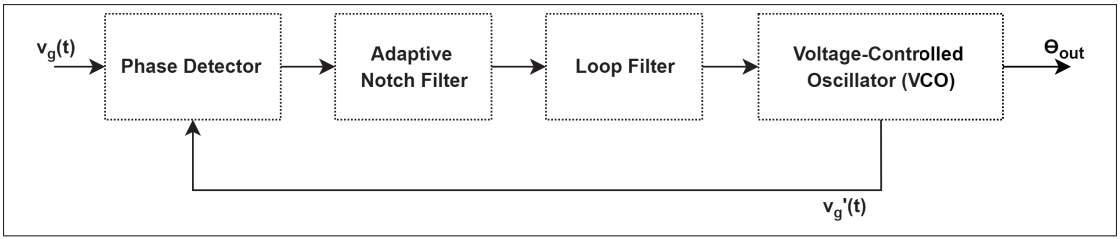

Figure 4.3 PLL topology with adaptive notch filter

The general notch filter transfer function is given in equation (4.13), where K_n is the gain at the notch frequency, ζ_n is the damping ratio and ω_n is the notch frequency.

$$H_{notch}(s) = \frac{s^2 + 2K_n\zeta_n\omega_n s + \omega_n^2}{s^2 + 2\zeta_n\omega_n s + \omega_n^2} \tag{4.13}$$

The damping ratio ζ_n effectively impacts the width of the filter stop band, i.e. bandwidth, to which it is directly proportional. Ideally, this value should be kept small in order to have a narrower bandwidth and avoid interactions with the PLL response and its cutoff frequency. A value of $\zeta_n = 0.7$ is selected, resulting in a bandwidth of 170Hz. In order to eliminate the component at the notch frequency, a small value should be selected for the gain K_n. A gain of -100dB is selected, which corresponds to a gain of $K_n = 1E^{-5}$. The designed filter frequency response is shown in the Bode diagram of Figure 4.4. In order to make the filter adaptive, the notch frequency ω_n is fed back to the filter implementation from the estimated PLL output.

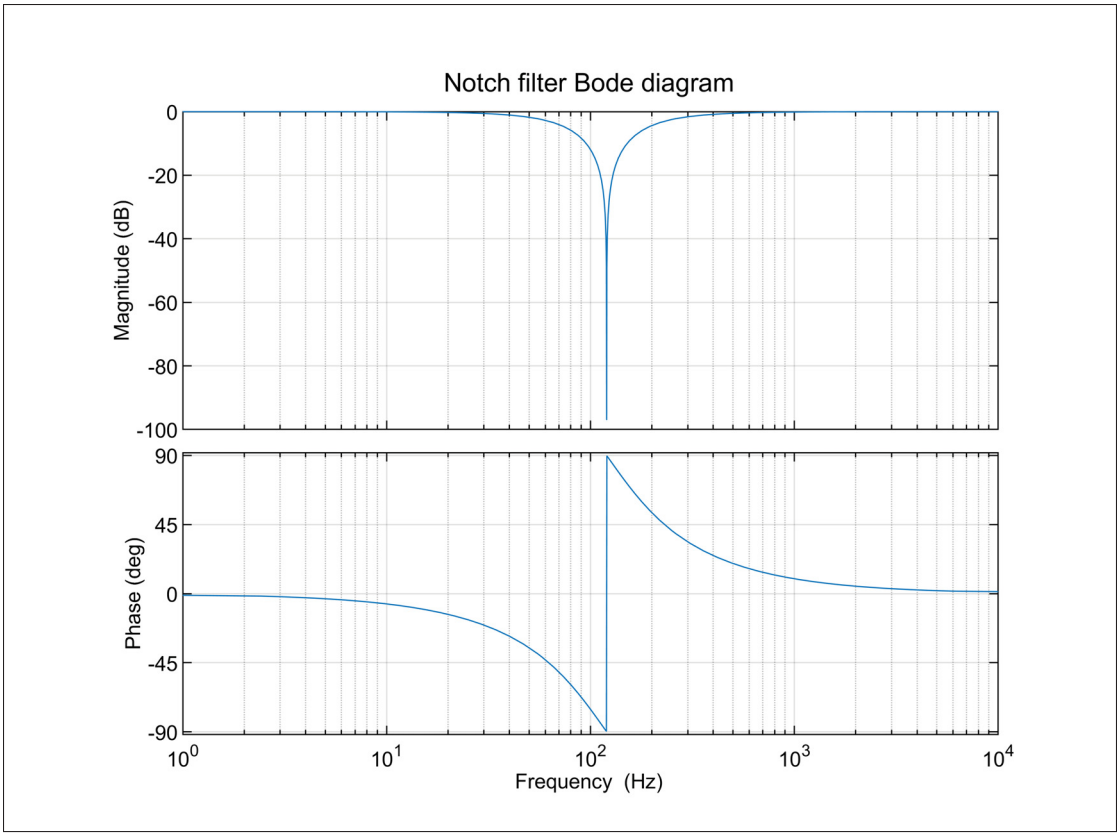

Figure 4.4 Notch filter Bode diagram

4.2 Simulation results

The designed PLL performance is evaluated by simulating the model presented in Figure VI-2 in Annex VI.

4.2.1 Step change in frequency

The first test performed is a +4Hz step change in the reference signal frequency in order to evaluate the dynamic response of the PLL. The step is applied at $t = 0.05$s. Simulation results are presented in Figure 4.5. The upper graph shows the reference signal frequency (blue curve) and the PLL estimated frequency (orange curve), while the second graph shows the error between the reference and estimated frequency, in Hz. The third graph presents the input signal waveform

(blue curve) superimposed with the reconstructed sine waveform at the PLL output (orange curve), while the bottom graph presents the error between the two signals. It can be observed that the error in the estimated frequency is completely eliminated within approximately $70ms$ with a minimal overshoot. This result indicates that the PLL has a satisfactory dynamic response to perturbations in frequency, considering that the interconnection standard (IEEE, 2018) requires that the inverter detects over-frequency conditions of +2Hz and disconnects within $t = 160ms$.

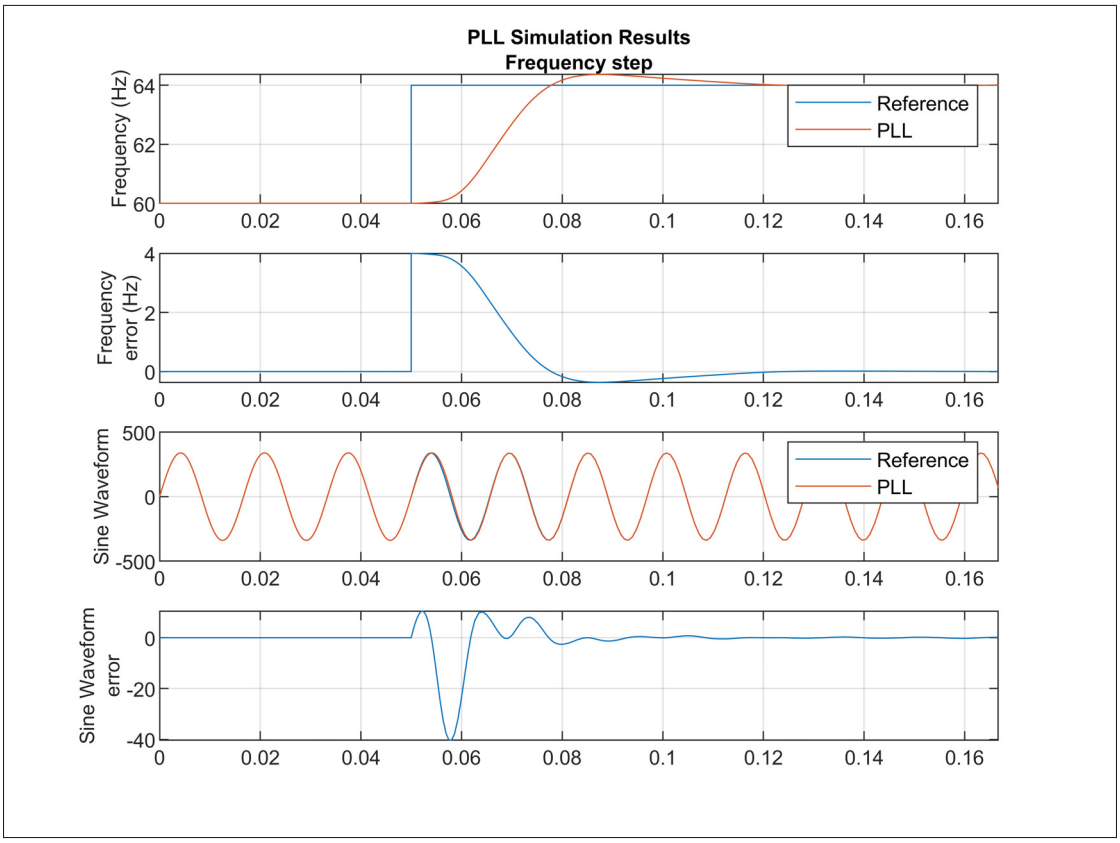

Figure 4.5 PLL simulation results, +4Hz step change in frequency. PLL output frequency, frequency error, sine wave and sine wave error

4.2.2 Step change in phase angle

The second test performed is a +45° step change in the reference signal phase angle in order to once again evaluate the PLL dynamic response to perturbations. The step is applied at $t = 0.05s$.

Simulation results are presented in Figure 4.6. The results are presented in the same order as the previous test. It can be observed that in this case the error in the estimated frequency is completely eliminated within approximately $80ms$. Although it is slower than in the previous test, it is still satisfactory and well within the requirement of $t = 160ms$.

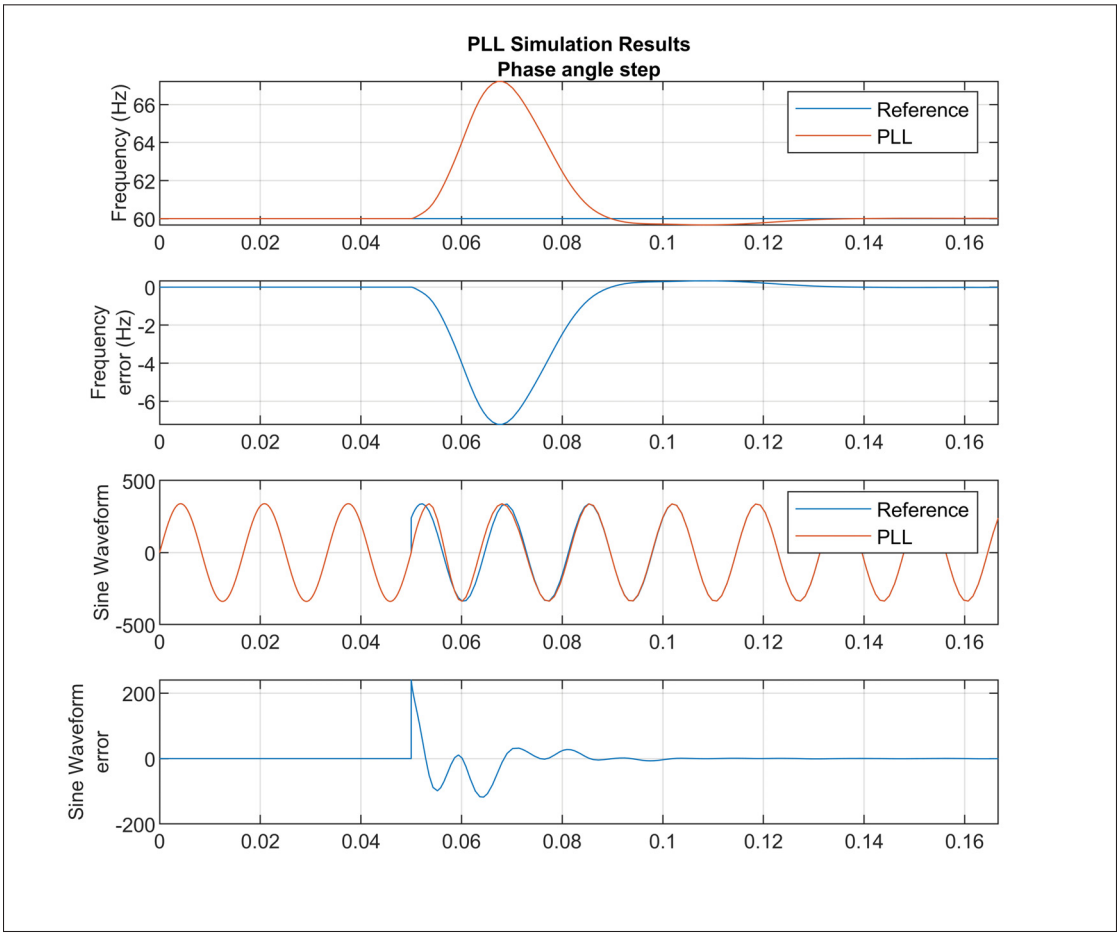

Figure 4.6 PLL simulation results, +45° step change in phase angle. PLL output frequency, frequency error, sine wave and sine wave error

4.3 Conclusion

In this chapter, the general structure and topology of a single-phase phase-locked loop used to synchronize the inverter to the grid voltage was first presented. Each of its components and their respective role were introduced, namely the phase detector, the loop filter and the

voltage-controlled oscillator (VCO). The PLL mathematical model for this topology was then presented and the loop filter gains equations were derived from the PLL transfer function by comparison to a generalized second-order transfer function. The gains were selected in order to obtain a satisfactory dynamic response to a step change in the frequency in terms of overshoot and settling time. From the equations also appeared the component at twice the grid frequency in the PLL output. An adaptive notch filter was implemented between the phase detector and loop filter in order to eliminate this undesirable component even when the grid voltage is off-nominal. The designed PLL performance was then tested by applying step changes in the input signal frequency and phase angle. It was demonstrated that it has a satisfactory dynamic response with minimal overshoot and fast settling time to harsh test conditions that are unlikely to represent real grid dynamics that would occur following contingencies.

CHAPTER 5

GRID SUPPORT FUNCTIONS

This chapter focuses on the implementation and testing of inverter grid support functions as described in the interconnection standard (IEEE, 2018), which aim to enable inverter-based resources to dynamically contribute to grid voltage and frequency stability by means of active and reactive power control, ride-through capabilities and unintentional islanding detection. These functions represent an additional layer of control and logic implemented on top of the inverter system that was designed so far. The outer power control loops will first be presented, followed by these inverter grid support functions:

1. Voltage - Reactive Power (Volt-VAR)
2. Frequency - Watt (Droop)
3. Voltage Ride-Through (VRT)
4. Islanding Detection

The roles of these functions, their implementation in the control system and their parameters will be described. Their performance and effectiveness will then be demonstrated through simulations based on test sequences adapted from the standard conformance test procedures of (IEEE, 2020).

5.1 Active and reactive power control

In order to control the active and reactive power exchange between the inverter and the grid, a power control loop is implemented as shown in the diagram of Figure 5.1. This loop generates the current reference i_2^* used by the current controller presented in Chapter 3. It contains two separate proportional-integral controllers for the active and reactive power, which generate two references, namely the active power current reference I_p and the reactive power current reference I_q, in order to eliminate the error between the measured power and the references. The current reference is generated from these according to equations (5.1) to (5.3) and a limiter is used to

limit its magnitude in order to protect the power semiconductors. The active and reactive power references are calculated and generated from the grid support functions logic, presented in the following sections, which use various measurements at the inverter PoC as inputs, namely the voltage amplitude, frequency, phase angle and active and reactive power.

$$I_{mag} = \sqrt{I_p^2 + I_q^2} \tag{5.1}$$

$$\phi = \arctan \frac{I_q}{I_p} \tag{5.2}$$

$$i_2^* = I_{mag} \sin(\omega t + \phi) \tag{5.3}$$

The dynamic response of the power control loop is designed to be much slower than the inner current control loop and without overshoot and steady-state error. In fact, referring to the interconnection standard (IEEE, 2018), the range of allowable settings for the open-loop response time of grid support functions is in seconds. The open-loop response time is defined as the duration from a step change in the control signal input until the output changes by 90% of its final change. The power controller gains were selected by an empirical approach in order to obtain a satisfactory response to step changes in active and reactive power. They are summarized in Table 5.1.

Table 5.1 Active and reactive power controllers parameters

Parameter	**Value**
Active power controller proportional gain k_{pp}	2
Active power controller integral gain k_{ip}	25
Reactive power controller proportional gain k_{pq}	1
Reactive power controller integral gain k_{iq}	25

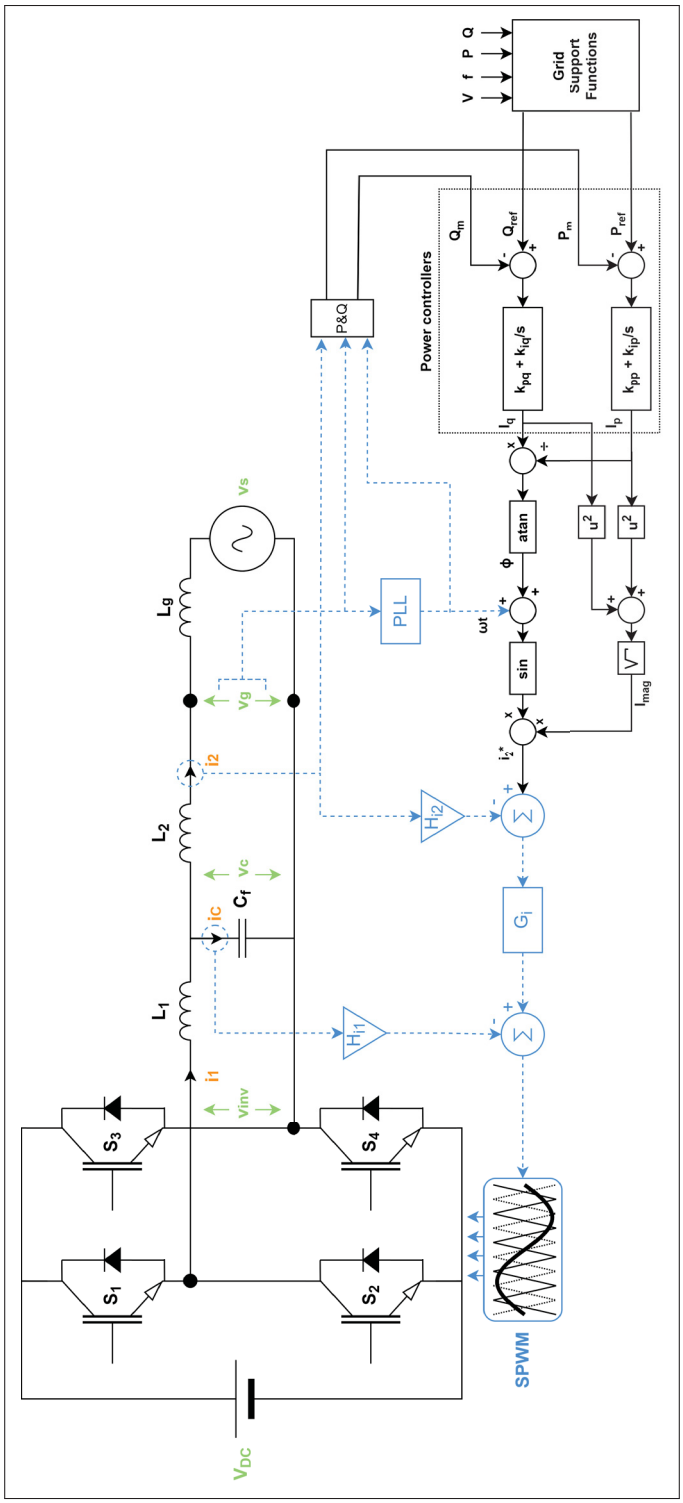

Figure 5.1 Grid support functions implementation diagram

5.2 Voltage - Reactive Power (Volt-VAR)

5.2.1 Description

The role of the Volt-VAR (VVAR) function, as its name implies, is to regulate the voltage level at the point of connection of the inverter (or in some cases a remote node on the system) by either absorbing or injecting reactive power. In the particular case of photovoltaic production, when several inverters are connected to the same feeder while operating with a constant power factor close to unity, overvoltages can occur at mid-day due to the load being minimal and the photovoltaic production being at its maximum. By operating the inverter in Volt-VAR mode instead of constant power factor, these overvoltages may be mitigated by absorbing reactive power without the need to curtail as much active power, as long as the resulting apparent power remains within the inverter rated value.

5.2.2 Implementation

The Volt-VAR function is implemented using a predetermined piecewise linear curve that changes the inverter reactive power setpoint as function of the measured voltage, as shown in Figure 5.2. A positive reactive power setpoint value implies the inverter injects reactive power (in case of undervoltage), while negative values means the inverter absorbs reactive power (in case of overvoltage). A deadband is usually present around the nominal voltage, where the inverter does not absorb nor inject reactive power. Table 5.2 summarizes the Volt-VAR curve parameters used for the tests herein.

In some cases, the inverter is required to autonomously adjust the nominal reference voltage to a value other than 1 per unit. This allows the inverter to adjust its Volt-VAR curve based on the measured voltage at the point of connection, which may vary along a feeder depending on: 1)the distance to the substation and 2)the proximity to voltage regulators or the presence of other inverter-based resources, amongst other factors. This autonomous adjustment is implemented

using a moving average filter with an adjustable time constant that measures the voltage at the PoC and adjusts the voltage reference over this time period.

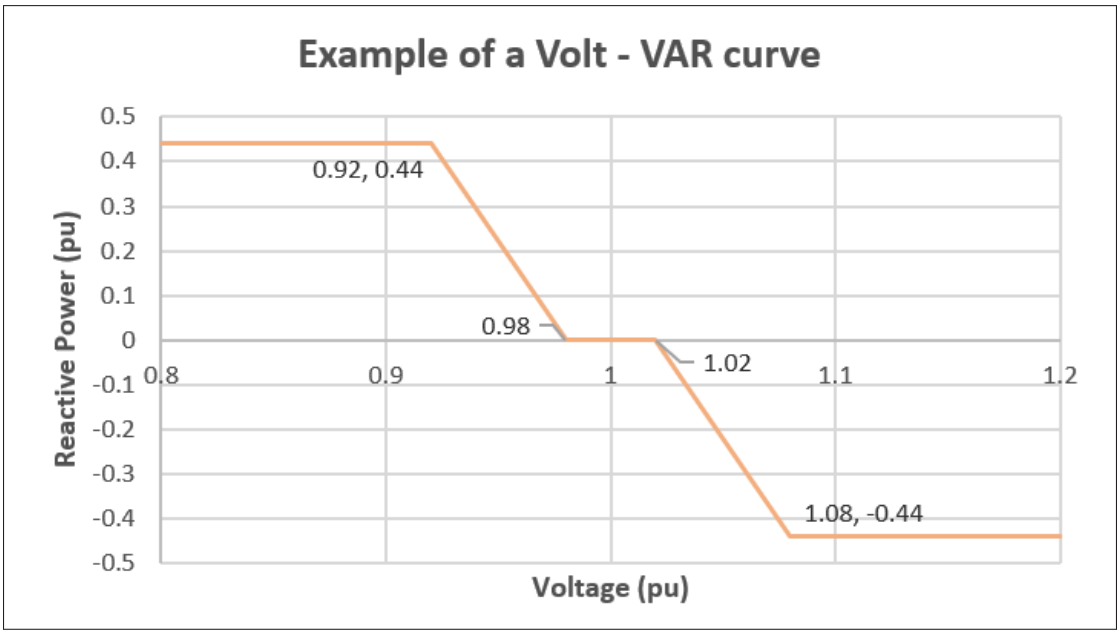

Figure 5.2 Example of a Volt-VAR curve (IEEE, 2018)

Table 5.2 Volt-VAR function parameters (IEEE, 2018)

VVAR Parameters	**Settings**
V_{ref}	1 p.u.
V_1	$.92 \cdot V_{ref}$ p.u.
Q_1	+0.44 p.u.
V_2	$0.98 \cdot ref$ p.u.
Q_2	0 p.u.
V_3	$1.02 \cdot V_{ref}$ p.u.
Q_3	0 p.u.
V_4	$1.08 \cdot V_{ref}$ p.u.
Q_4	-0.44 p.u.
Response Time	0.05s

5.2.3 Simulation results

5.2.3.1 Static Volt-VAR curve

In order to demonstrate the effectiveness of the Volt-VAR function, a test sequence is used with the inverter first operating in constant power factor (CPF) mode with PF=1, then in Volt-VAR mode. The test sequence is as follows:

1. The available power is kept constant at 1p.u. throughout the sequence
2. The inverter is brought to steady-state
3. The grid voltage ramps down from 1p.u. at $t = 1$s to 0.8p.u. at $t = 1.5$s
4. The grid voltage ramps up from 0.8p.u. at $t = 2.5$s to 1.2p.u. at $t = 3$s

The simulation results are presented in Figure 5.3. It can be observed on the bottom graph that when the grid voltage ramps down, the reactive power reference ramps up to the required $Q_1 = 0.44$p.u. The active power reference is then curtailed to $P_{ref} = 0.9$p.u., as shown in the middle graph, in order to maintain the inverter apparent power within the inverter rated power, i.e. $\sqrt{0.44^2 + 0.9^2} = 1$p.u. Similarly, when the voltage ramps up, the reactive power reference decreases until it reaches the required $Q_4 = 0.44$p.u. The effect of the Volt-VAR curve deadband around the voltage reference can be seen between $2.5 \leq t \leq 3$s when the grid voltage crosses between $0.98 \leq V_{grid} \leq 1.02$p.u. The effectiveness of the Volt-VAR function can be observed on the top graph. It can be seen that when operating in Volt-VAR mode, the injected or absorbed reactive power from the inverter can support the voltage at its PoC (orange curve) unlike when it is operating in CPF mode (yellow curve). Indeed, the under-voltage is limited to 0.85p.u. and the over-voltage to 1.16p.u.

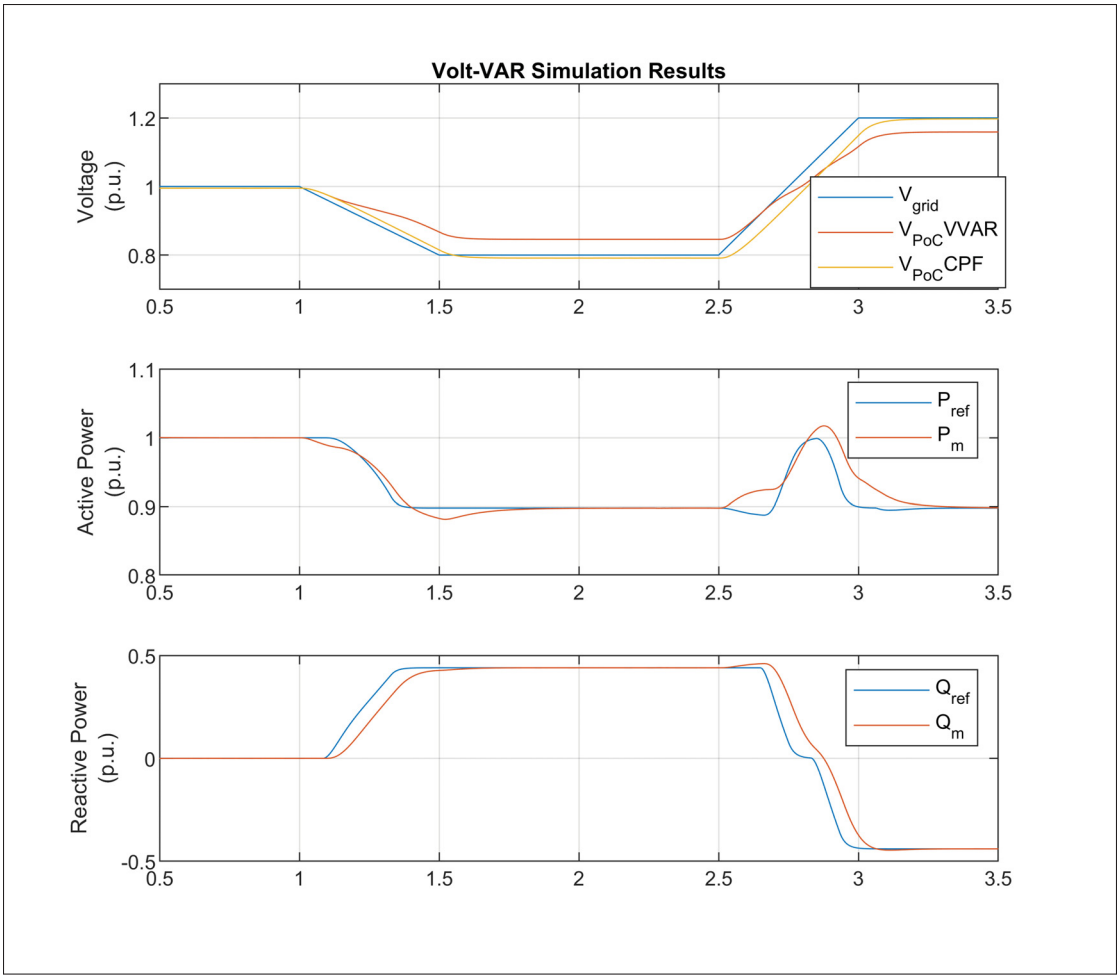

Figure 5.3 Volt-VAR simulation results

5.2.3.2 Autonomously adjusted Volt-VAR curve

According to the standard (IEEE, 2018), the autonomous voltage reference adjustment time constant shall be adjustable over a range of at least 300s to 5000s. For testing purposes, the time constant is set to 5s in order to quickly demonstrate the functionality principle. The test sequence is the following:

1. The available power is kept constant at 1p.u. throughout the sequence
2. The inverter is brought to steady-state
3. The grid voltage ramps up from 1p.u. at t = 1s to 1.05p.u. at t = 2s

4. The grid voltage is kept constant at 1.05p.u.

The simulation results are presented in Figure 5.4. It can be observed on the bottom graph that when the grid voltage ramps up, the reference and measured reactive power immediately ramp down as a response to the over-voltage, following the programmed Volt-VAR curve. The reactive power reference is then readjusted every second over the span of the 5s time constant as a response to the Volt-VAR curve voltage reference being autonomously adjusted to the measured grid voltage. After 5s at t = 6s, V_{ref} has been adjusted to 1.05p.u. and the resulting reactive power reference is set to 0p.u., demonstrating how the autonomous adjustment of the voltage reference can effectively shift the Volt-VAR curve.

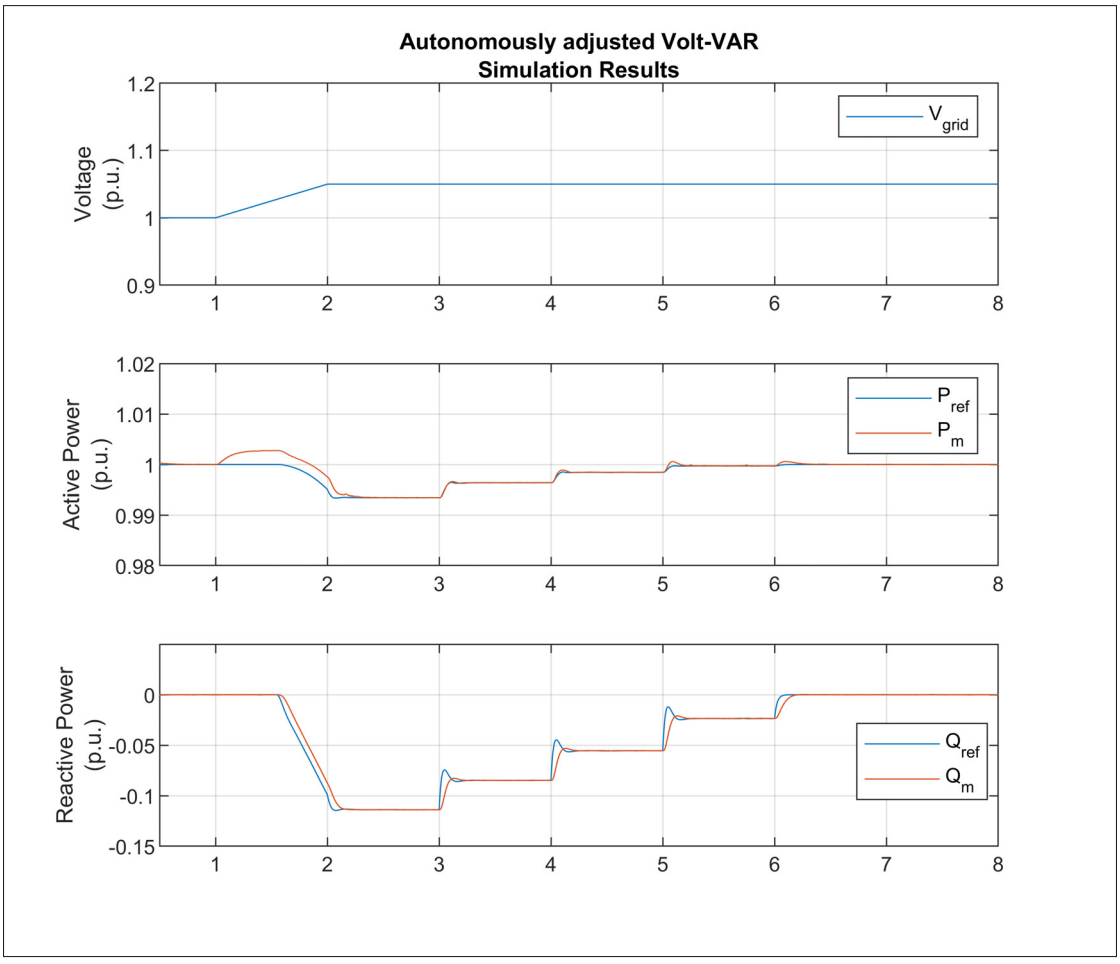

Figure 5.4 Autonomously adjusted Volt-VAR simulation results

5.3 Frequency - Watt (Droop)

5.3.1 Description

The role of the Frequency-Watt function is to support grid frequency regulation by adjusting the inverter output active power in response to measured over/under-frequency, similar to the speed droop control of a synchronous generator. Frequency deviations may occur on a power system when there is a mismatch between the load and generation. For example, the sudden loss of a large load may lead to a temporary over-frequency, during which a reduction in generation would help to re-achieve a balance and mitigate the frequency deviation. This function becomes particularly important when a growing number of inverter-based resources are connected to a feeder.

5.3.2 Implementation

The Frequency-Watt function adjusts the inverter active power reference following equation (5.4) during under-frequency conditions and equation (5.5) during over-frequency conditions. When the measured grid frequency is within the deadband, no adjustment is made to the active power reference. However, when the frequency is outside this zone, the active power reference is adjusted from its pre-disturbance value based on these equations:

$$P_{ref} = \min_{f<60-db_{uf}} \left\{ P_{pre} + \frac{(60 - db_{uf}) - f}{60 \cdot k_{uf}}; P_{avail} \right\} \tag{5.4}$$

$$P_{ref} = \max_{f>60+db_{of}} \left\{ P_{pre} - \frac{f - (60 + db_{of})}{60 \cdot k_{of}}; P_{min} \right\} \tag{5.5}$$

Where f is the measured grid frequency, P_{avail} is the available active power in per unit, P_{pre} is the pre-disturbance active power output in per unit, P_{min} is the minimum allowed active power, db_{of} and db_{uf} are the deadband values for over and under-frequency respectively and k_{of} and

k_{uf} are the droop coefficients for over and under-frequency respectively. Graphically, these equations yield a curve as shown in Figure 5.5.

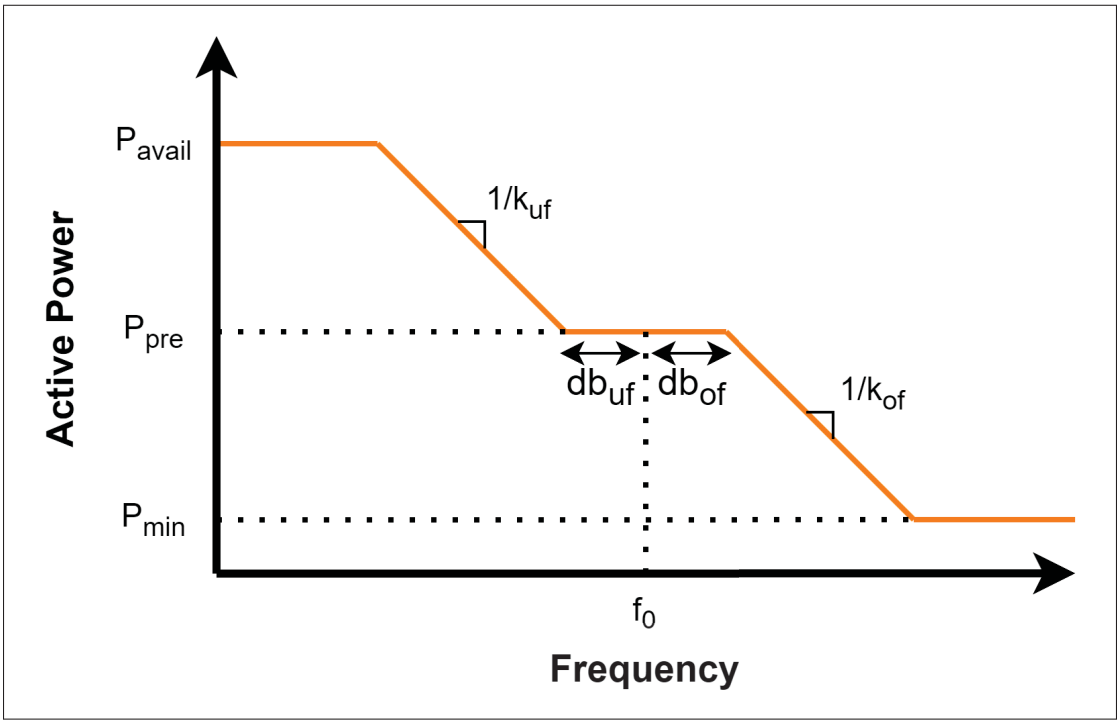

Figure 5.5 Example of a Frequency-Watt curve (IEEE, 2018)

Table 5.3 summarizes the Frequency-Watt curve parameters used for the tests herein.

Table 5.3 Frequency-Watt function parameters (IEEE, 2018)

FW Parameters	**Settings**
db_{of}, db_{uf} (Hz)	0.036
k_{of}, k_{uf}	0.05
P_{min}	0.1p.u.
Response Time	0.05s

5.3.3 Simulation results

The Frequency-Watt function is tested using the following sequence:

1. The available power is kept constant at 1p.u. throughout the sequence
2. The inverter is brought to steady-state
3. The grid frequency ramps down from 60Hz at t = 1s to 58Hz at t = 1.5s
4. The grid frequency ramps up from 58Hz at t = 2s to 62Hz at t = 2.5s

Simulation results are presented in Figure 5.6. The top graph presents the measured grid frequency, the middle graph shows the reference and measured active power in per unit of rated inverter active power and the bottom graph shows the reference and measured reactive power in per unit of rated inverter apparent power. It can be observed that when the grid frequency ramps down, the active power reference is left unchanged since it is already operating at rated active power and hence has no headroom to increase according to (5.4). On the other hand, when the grid frequency ramps up and reaches the over-frequency value of 60.036Hz and above, the active power is curtailed until it reaches its reference value of P_{ref} = 0.345p.u., which is calculated from equation (5.5):

$$P_{ref} = \max_{f>60.036} \left\{ 1 - \frac{62 - (60 + 0.036)}{60 \cdot 0.05}; 0.1 \right\} = 0.345 \tag{5.6}$$

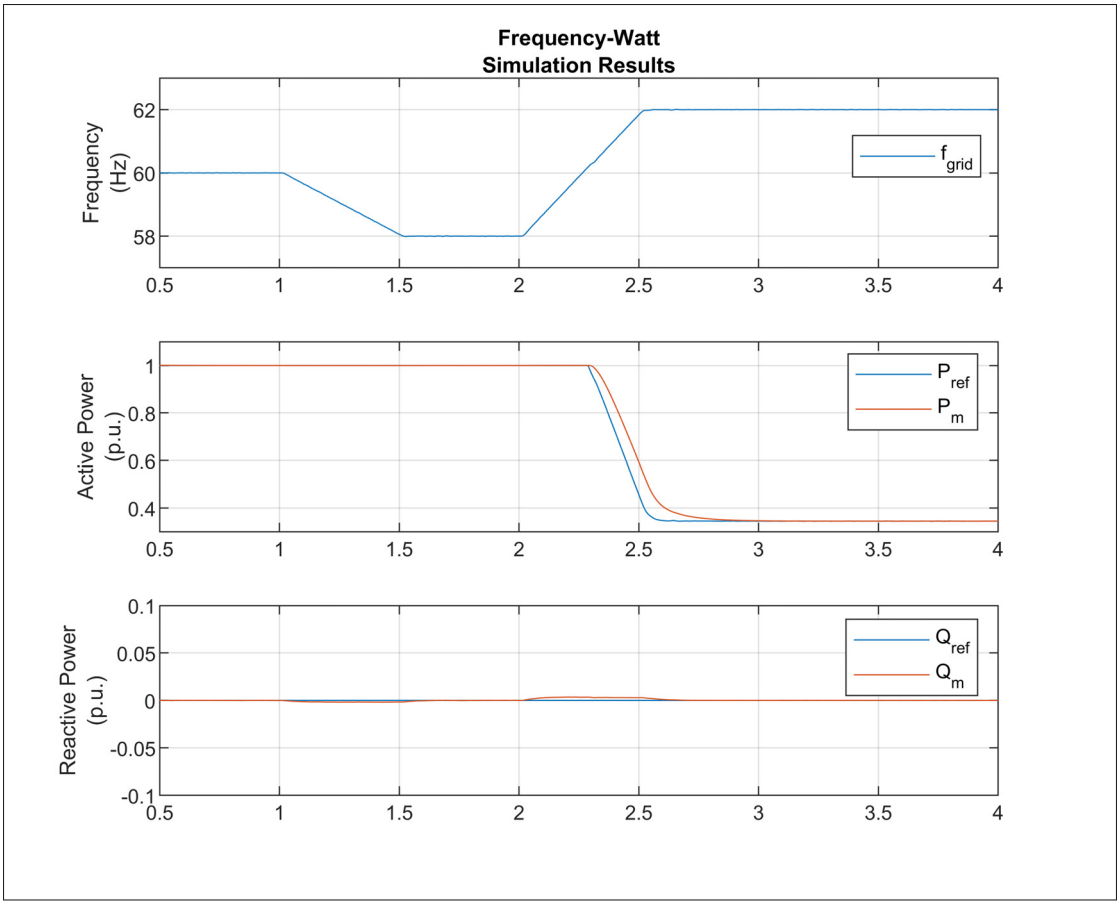

Figure 5.6 Frequency-Watt simulation results

5.4 Voltage Ride-Through (VRT)

5.4.1 Description

As opposed to previous interconnection standards where inverters were required to trip or disconnect from the grid during voltage disturbances, they must now be able to ride-through such events. With the increasing number of inverter-based resources connected to the grid, voltage ride-through capabilities are essential to limit the loss of generation during a disturbance, which could lead to further grid instability and cascaded failure, and to allow a quick recovery.

5.4.2 Implementation

The voltage ride-through logic is implemented as operating regions which are defined by pairs of corresponding voltage and time. For each region, a mode of operation is specified which dictates how the inverter shall behave while in this region. The voltage thresholds and their corresponding ride-through time, response time and operation mode used for the inverter system herein are summarized in Table 5.4 and illustrated in Figure 5.7. While in continuous or mandatory operation modes, the inverter shall continue to exchange active and reactive current with the grid as prescribed and following the references resulting from voltage/frequency support functions. While in the momentary cessation mode, the inverter shall temporarily cease to energize, i.e. cease current exchange with the grid, while remaining connected to it and synchronized with its voltage. It shall also restore its current output to 80% of the pre-disturbance level within 0.4s of when the voltage returns to the continuous or mandatory operating regions. Finally, while in the cease to energize operation mode, the inverter may behave as in the momentary cessation mode or may trip.

Table 5.4 Voltage ride-through requirements (IEEE, 2018)

Voltage (p.u.)	**Operation mode**	**Min. ride-through time (s)**	**Max. response time (s)**
$V > 1.20$	Cease to energize	N/A	0.16
$1.10 < V \leq 1.20$	Momentary cessation	12	0.083
$0.88 \leq V \leq 1.10$	Continuous operation	N/A	N/A
$0.70 \leq V < 0.88$	Mandatory operation	20	N/A
$0.50 \leq V < 0.70$	Mandatory operation	10	N/A
$V < 0.50$	Momentary cessation	1	0.083

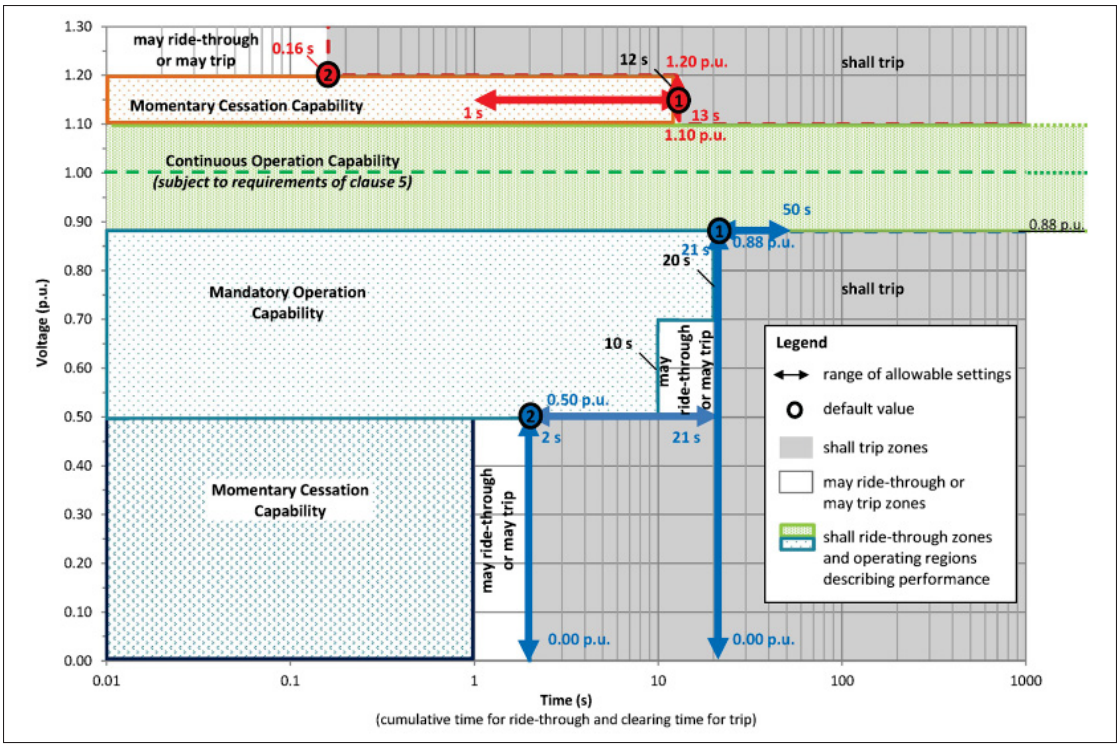

Figure 5.7 Voltage ride-through requirements and operating regions (IEEE, 2018)

5.4.3 Simulation results

5.4.3.1 Low voltage ride-through (LVRT)

The inverter LVRT capability is tested using the following procedure:

1. The available power is kept constant at 1p.u. throughout the sequence
2. The ride-through time for $V < 0.50$p.u. is set to 2s
3. The Volt-VAR function is activated with the parameters given in Table 5.2
4. The inverter is brought to steady-state
5. The grid voltage is stepped from 1p.u. to 0.05p.u. at $t = 5$s
6. The grid voltage is stepped from 0.05p.u. to 0.52p.u. at $t = 6.5$s
7. The grid voltage is stepped from 0.52p.u. to 0.65p.u. at $t = 15$s

8. The grid voltage is stepped from 0.65p.u. to 0.9p.u. at $t = 25$s

The voltage test signal sequence described in steps 5 to 8 of the previous procedure is illustrated in Figure 5.8.

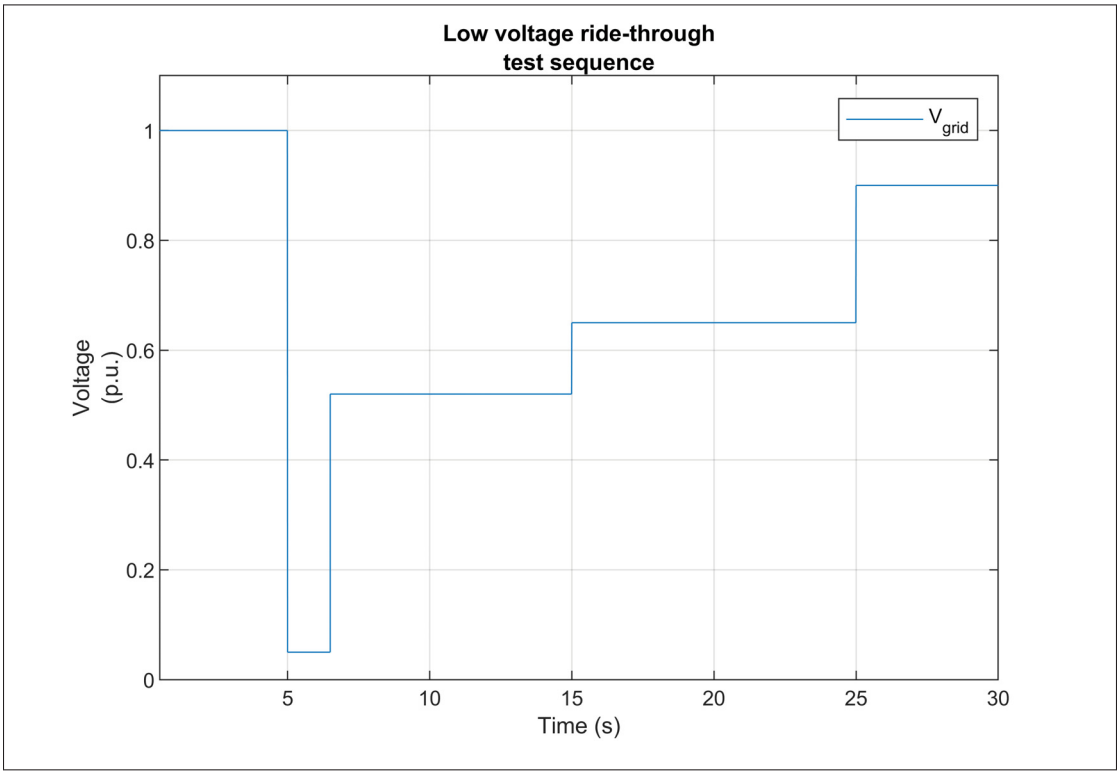

Figure 5.8 Low voltage ride-through test signal

Simulation results are presented in Figure 5.9. The top graph shows the measured grid voltage in per unit at the inverter PoC, the second graph shows the inverter output current in amperes and the last two graphs show the measured output active and reactive power in per unit respectively. It can be observed that when the grid voltage is stepped down to 0.05p.u. between $5s < t < 6.5s$, the momentary cessation operation mode is activated and the inverter ceases to inject current. Once the grid voltage is stepped above 0.5p.u. at $t = 6.5$s, the inverter is in the mandatory operation region and restores its current output in less than 0.1s as shown in Figure 5.10, which is in agreement with the requirements. It can be seen that the current is restored above the pre-disturbance level. This is because the low-voltage condition is still present and the Volt-VAR

function is active and requires the inverter to inject 0.44p.u. of reactive current to support the voltage, as shown on the bottom graph of Figure 5.10. The active power is then curtailed in order to limit the injected current to its rated value considering the low voltage at the PoC. When the grid voltage is stepped up to 0.65p.u. between $15s < t < 25s$, while the reactive power reference remains at 0.44p.u., additional active power can be injected as shown in the third graph. Finally, when the voltage is stepped up to 0.9p.u. at $t = 25$s, the injected reactive power is reduced to 0.35p.u. following the programmed Volt-VAR curve and the active power does not need to be curtailed anymore to remain within the inverter rated current. This test demonstrates that the designed inverter complies with the aforementioned LVRT requirements. Indeed, it ceases to inject current and remains connected and synchronized to the grid while a low voltage condition is present during the prescribed minimum ride-through time. It then quickly restores its output current when the grid voltage returns to the mandatory operation region.

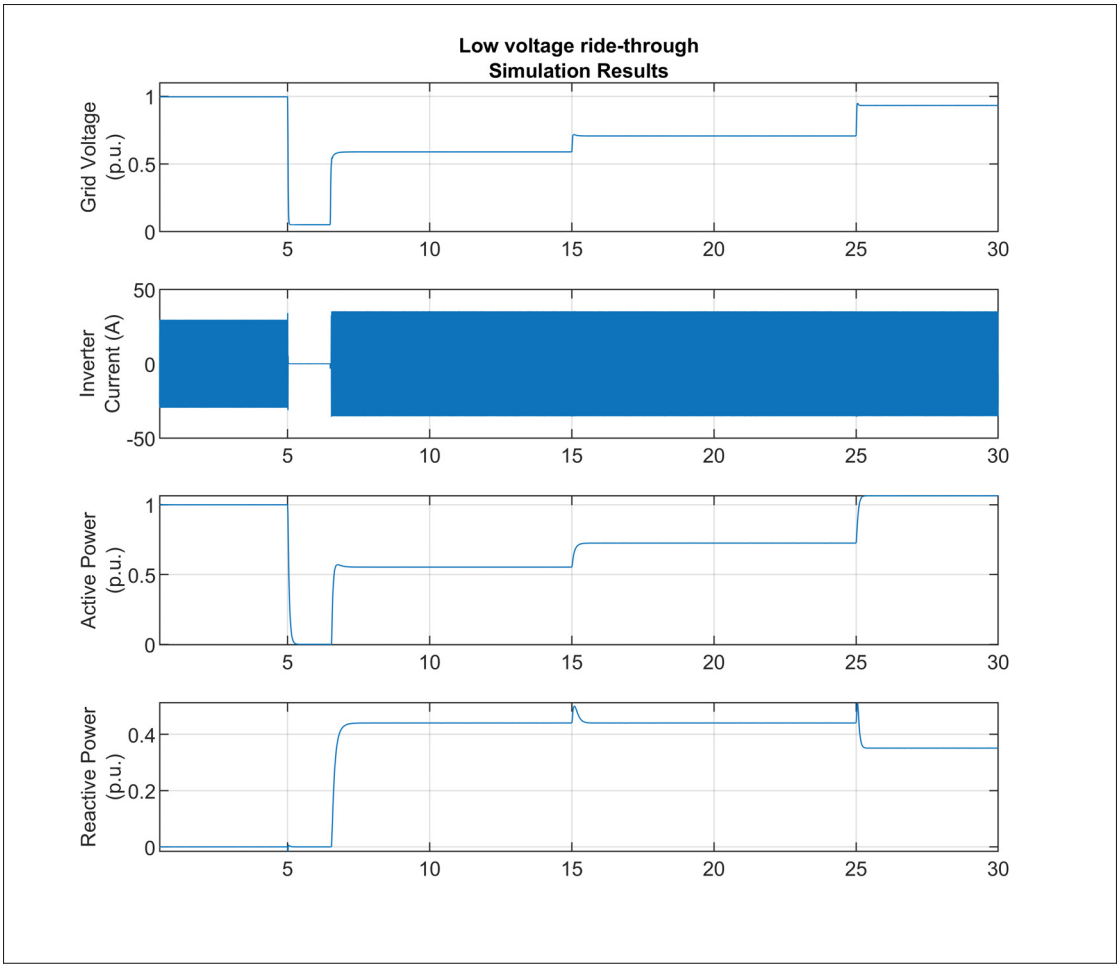

Figure 5.9 Low voltage ride-through simulation results

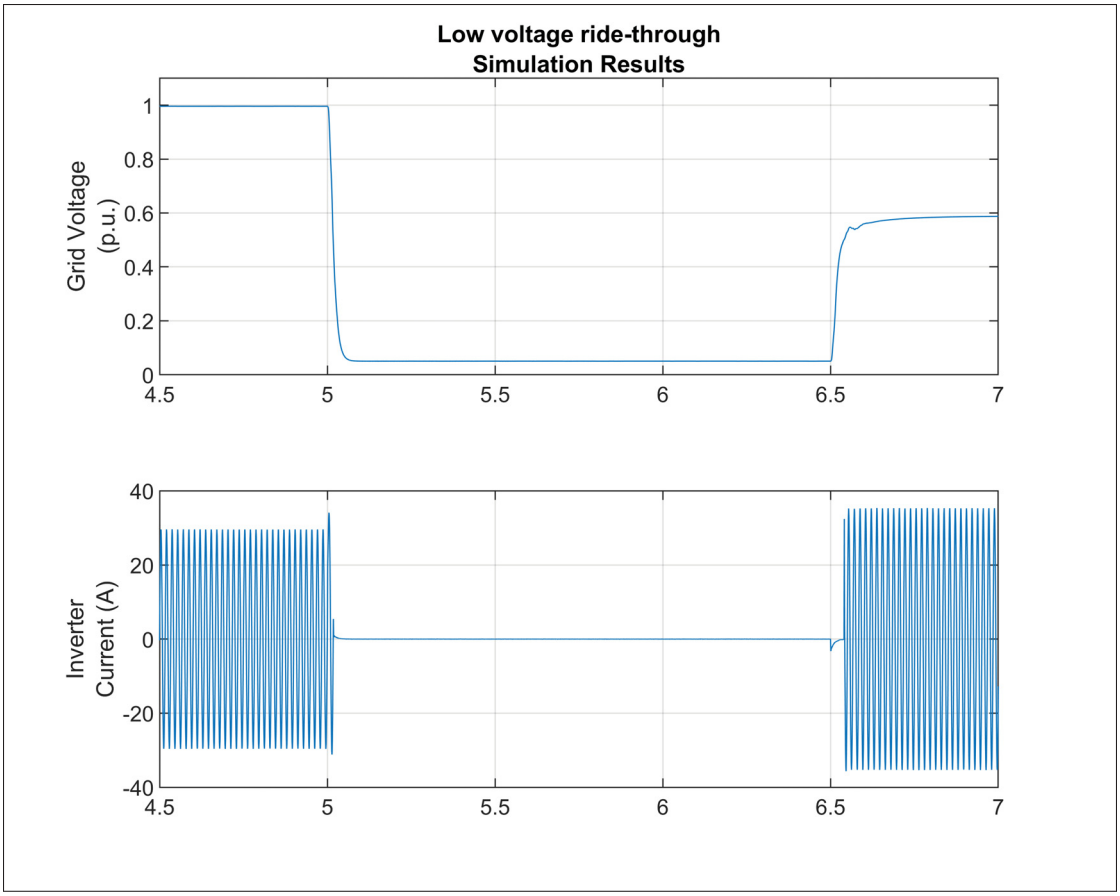

Figure 5.10 Low voltage ride-through simulation results, zoom on current output restoration

5.4.3.2 High voltage ride-through (HVRT)

The inverter HVRT capability is tested using the following procedure:

1. The available power is kept constant at 1p.u. throughout the sequence
2. The ride-through time for $1.10 < V \leq 1.20$p.u. is set to 13s
3. The Volt-VAR function is activated with the parameters given in Table 5.2
4. The inverter is brought to steady-state
5. The grid voltage is stepped from 1p.u. to 1.16p.u. at $t = 5$s
6. The grid voltage is stepped from 1.16p.u. to 1p.u. at $t = 17$s

The voltage test signal sequence described in steps 5 and 6 of the previous procedure is illustrated in Figure 5.11.

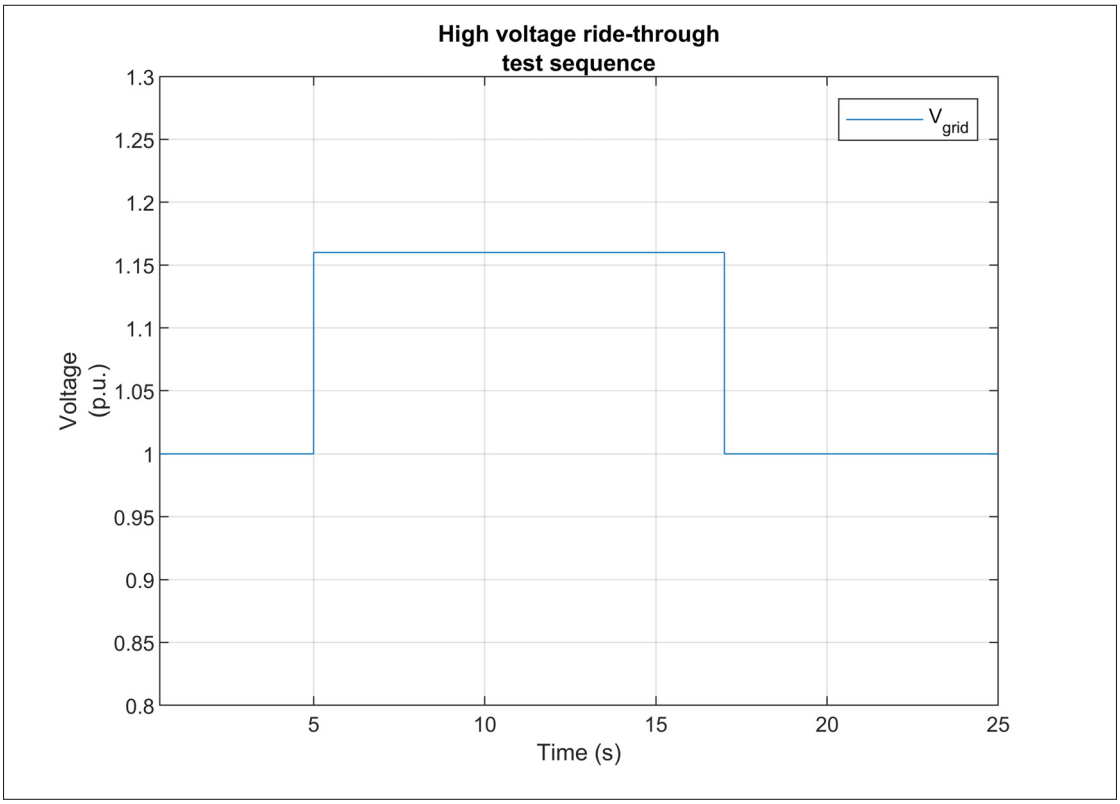

Figure 5.11 High voltage ride-through test signal

Simulation results are presented in Figure 5.12. The top graph shows the measured grid voltage in per unit at the inverter PoC, the second graph shows the inverter output current in amperes and the last two graphs show the measured output active and reactive power in per unit respectively. It can be observed that when the grid voltage is stepped up to 1.16p.u. between $5s < t < 17s$, the momentary cessation operation mode is activated and the inverter ceases to inject current. Once the grid voltage is stepped back to 1p.u. at $t = 17$s, the inverter returns in the continuous operation region and restores its current output to the pre-disturbance level in less than 0.3s as shown in Figure 5.13, which is in agreement with the requirements. This test demonstrates that the designed inverter complies with the aforementioned HVRT requirements by ceasing to inject current and remaining connected and synchronized to the grid while a high voltage condition

is present during the prescribed minimum ride-through time and quickly restoring its output current when the high voltage condition is cleared.

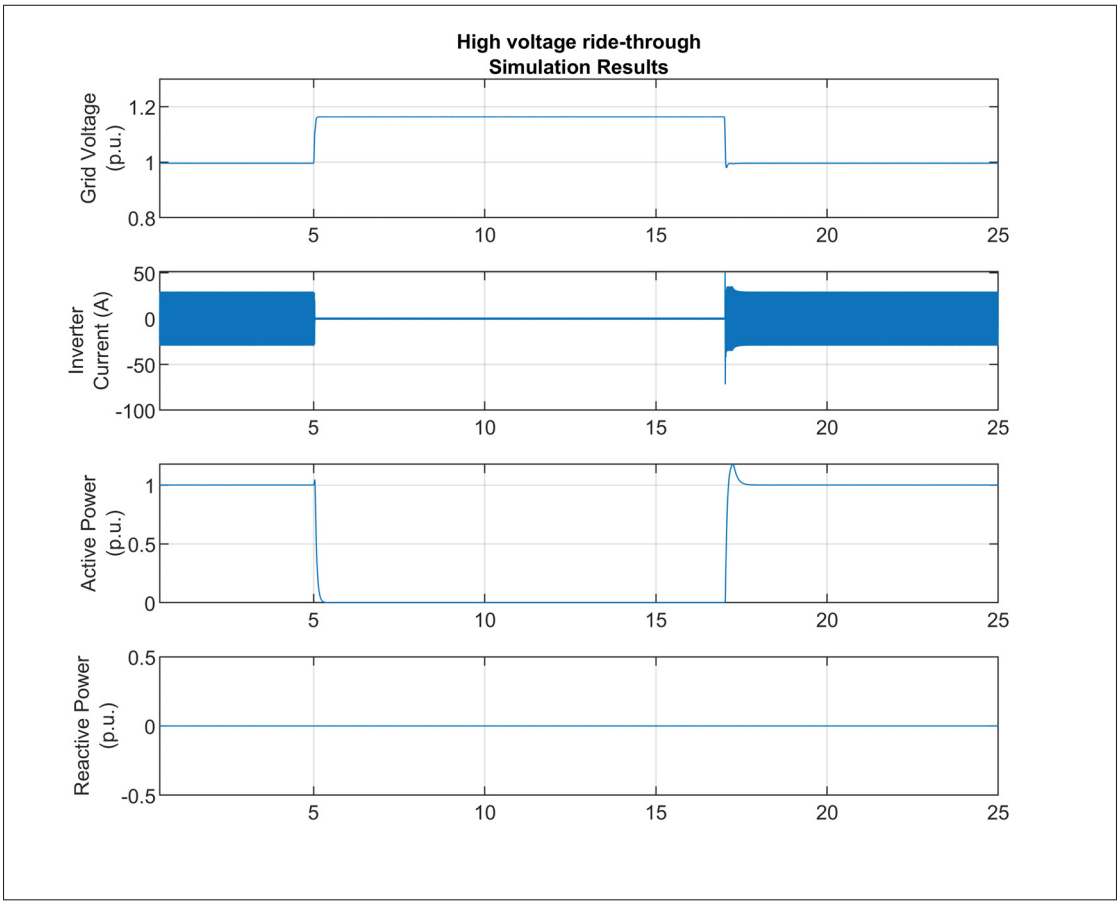

Figure 5.12 High voltage ride-through simulation results

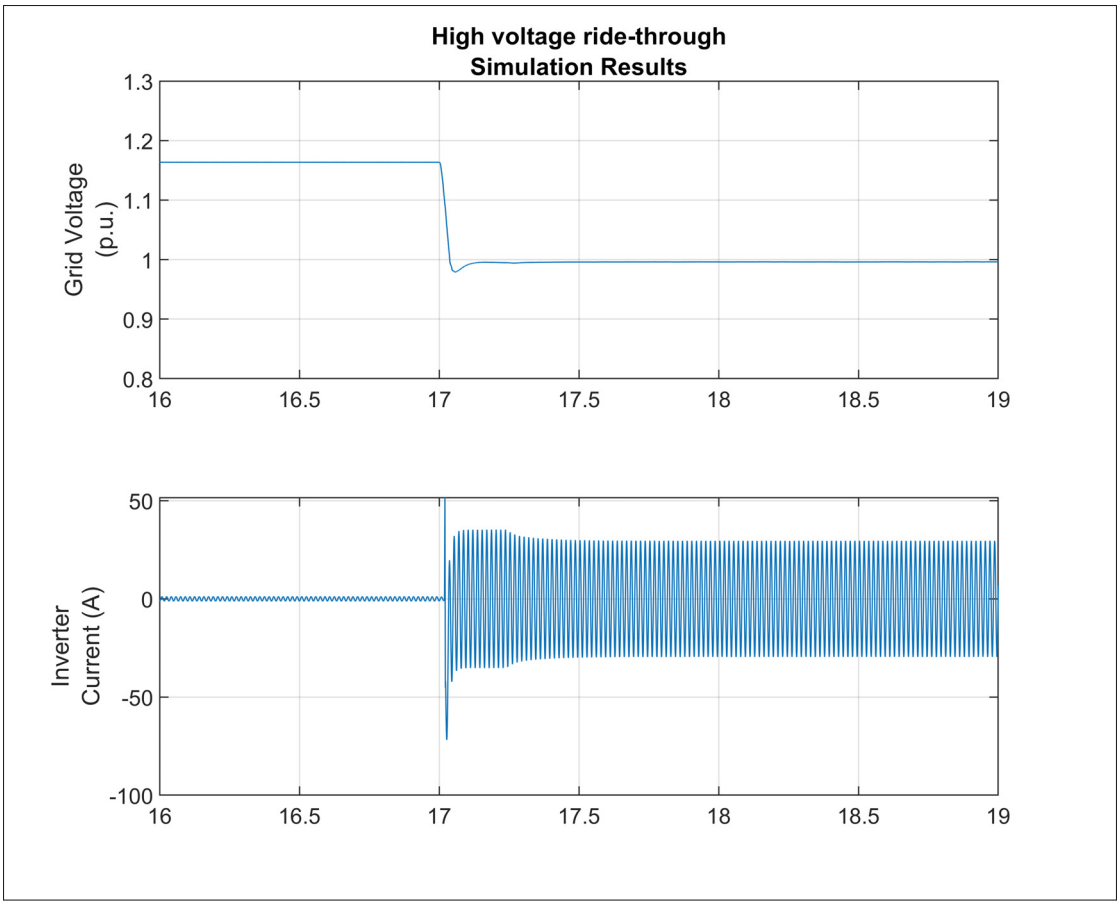

Figure 5.13 High voltage ride-through simulation results, zoom on current output restoration

5.5 Islanding Detection

5.5.1 Description

In the case of a PV inverter, an island is defined as the condition created when it is supplying power to a load while being disconnected from the grid. For safety reasons and to prevent damage to other equipment, the inverter shall be able to autonomously detect an unintentional island condition, cease to inject current and trip within 2s of the formation of the island. A wide variety of islanding detection methods (IDM) have been developed as shown in (Bower & Ropp, 2002). Active detection methods usually rely on the addition of a small perturbation in the current

reference signal to drive the voltage and/or the frequency out of the allowed operating range when the inverter is islanded. This abnormal condition is then detected by the protection system which disconnects the inverter. Although these methods usually deteriorate the injected current power quality due in part to the perturbation in the reference, they are shown to provide better and faster island detection by reducing the non-detection zone compared to passive methods. Since it is not the main focus of this thesis, a single active detection method is implemented, parameterized and tested for the inverter herein, namely the Sandia Frequency Shift (SFS) method (Reis, Barros, Moreira, Nascimento F., Ruppert F. & Villalva, 2015). It is shown to be very effective and provide a fast detection of the island with one of the smallest non-detection zone and minimal impact on the power quality.

5.5.2 Implementation

The Sandia Frequency Shift is a variation of the active frequency drift islanding detection method, where the current reference waveform is modified in order to force the inverter output voltage frequency to drift away from its nominal value when it is islanded. More specifically, it is implemented by adding a dead-time, t_z, at every half-cycle in the current reference waveform as shown in Figure 5.14.

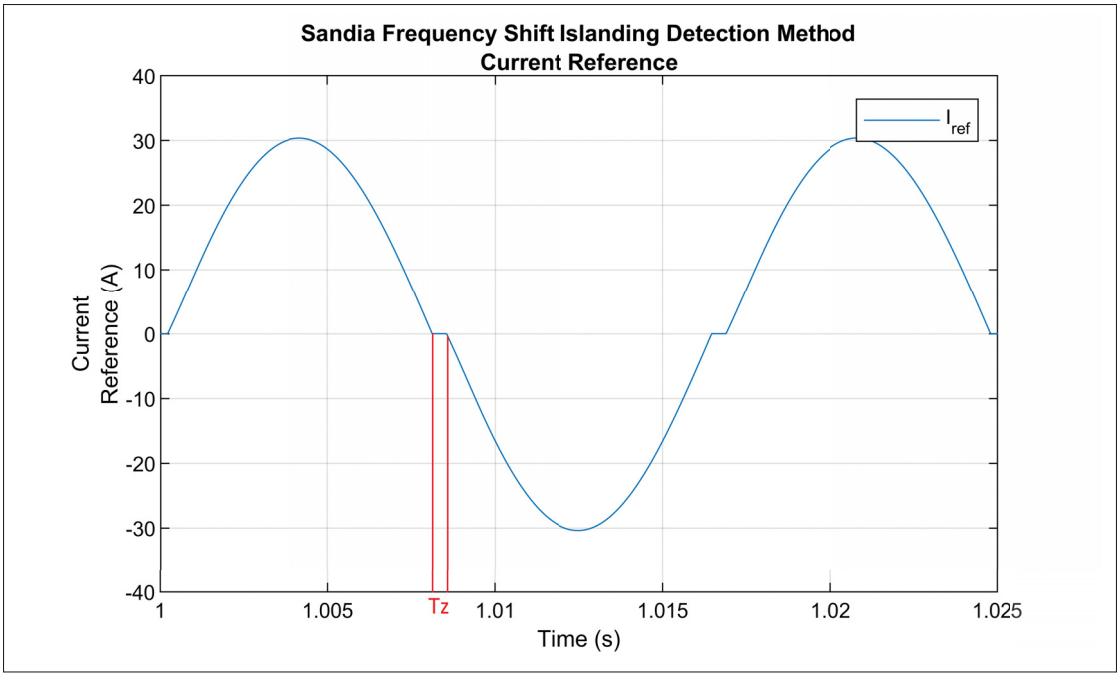

Figure 5.14 Sandia Frequency Shift Islanding Detection Method Current Reference

While it is grid-connected, the frequency is imposed by the grid and this small perturbation only impacts the injected current THD. However, when disconnected from the grid, it causes the frequency to drift until it reaches the protection system threshold (either the under/over-frequency or the rate-of-change-of-frequency (ROCOF) limit), which trips the inverter. Moreover, the SFS method accelerates this frequency drift by using a positive feedback of the measured grid frequency to modify the current reference. This feedback increases the chopping factor c_f given by equation (5.7).

$$c_f = c_{f_0} + K(f - f_o) \tag{5.7}$$

Where c_{f_0} is the chopping factor at nominal frequency, K is the acceleration factor, f is the measured frequency and f_o is the grid nominal frequency.

Considering that $T_o = \frac{1}{f_o}$ is the period of the grid voltage at nominal frequency f_o, then the period of the half-cycle of the modified current waveform is defined as equation (5.8):

$$\frac{T_{SFS}}{2} = \frac{T_o}{2} - t_z \tag{5.8}$$

Which can be rewritten as a function of the chopping factor as given in equation (5.9):

$$\frac{T_{SFS}}{2} = \frac{T_o}{2}(1 - c_f) \tag{5.9}$$

The modified current waveform half-cycle frequency can then be expressed by (5.10):

$$f_{SFS} = \frac{1}{T_{SFS}} = \frac{f_o}{1 - c_f} \tag{5.10}$$

Table 5.5 summarizes the SFS IDM parameters used for the tests presented herein. These parameters were selected by simulating the test circuit shown in Figure 5.18 for the test conditions presented in section 5.5.3.1 and comparing the inverter output current frequency spectrum with and without the IDM activated. The objective was to have a fast islanding detection for all test conditions with a minimal impact on output current THD. The inverter output current frequency spectrum when operating at rated power and unity power factor without and with the IDM activated are shown in Figures 5.15 and 5.16 respectively and a comparison is presented on Figure 5.17. It can be observed that the THD is increased from 0.45% to 0.70%, which is well below the required value of 5% specified in (IEEE, 2018).

Table 5.5 Sandia Frequency Shift Islanding Detection Method parameters

SFS IDM Parameters	**Settings**
SFS nominal frequency f_o (Hz)	60
SFS acceleration factor K	0.05
SFS chopping factor at nominal frequency c_{f_0}	0.005

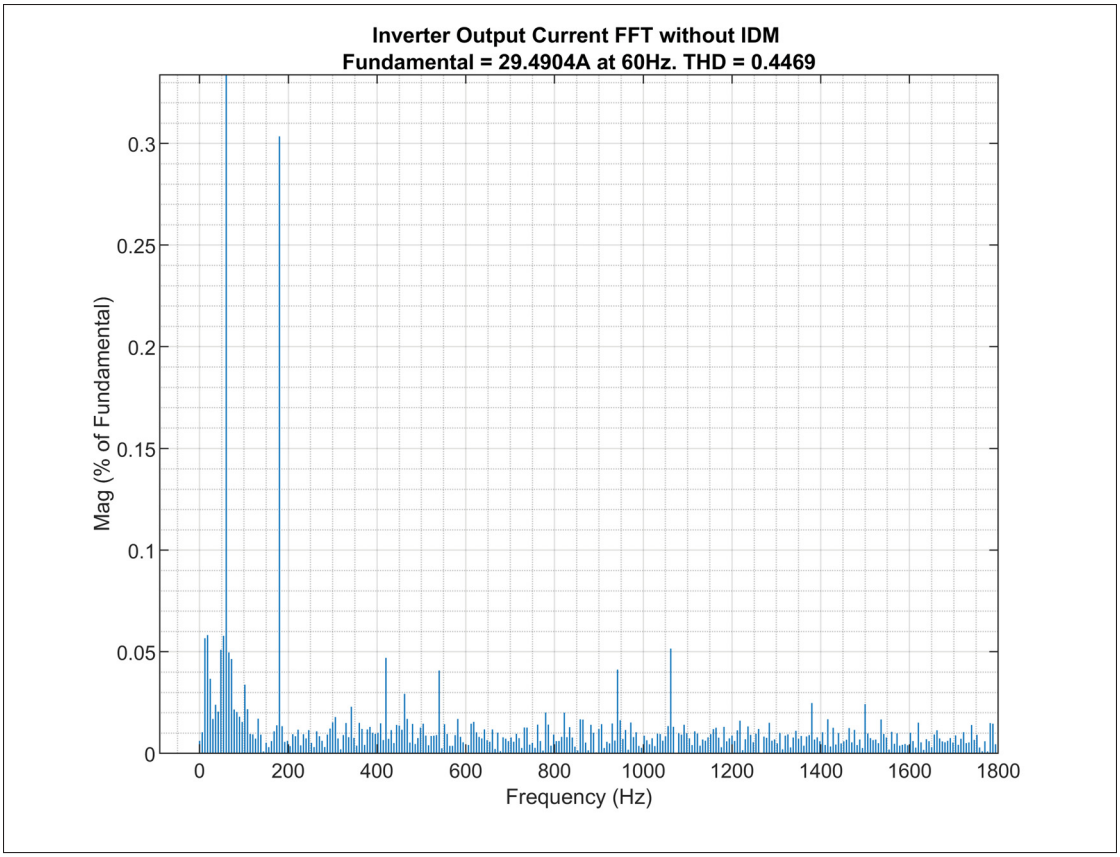

Figure 5.15 Inverter output current frequency spectrum without IDM

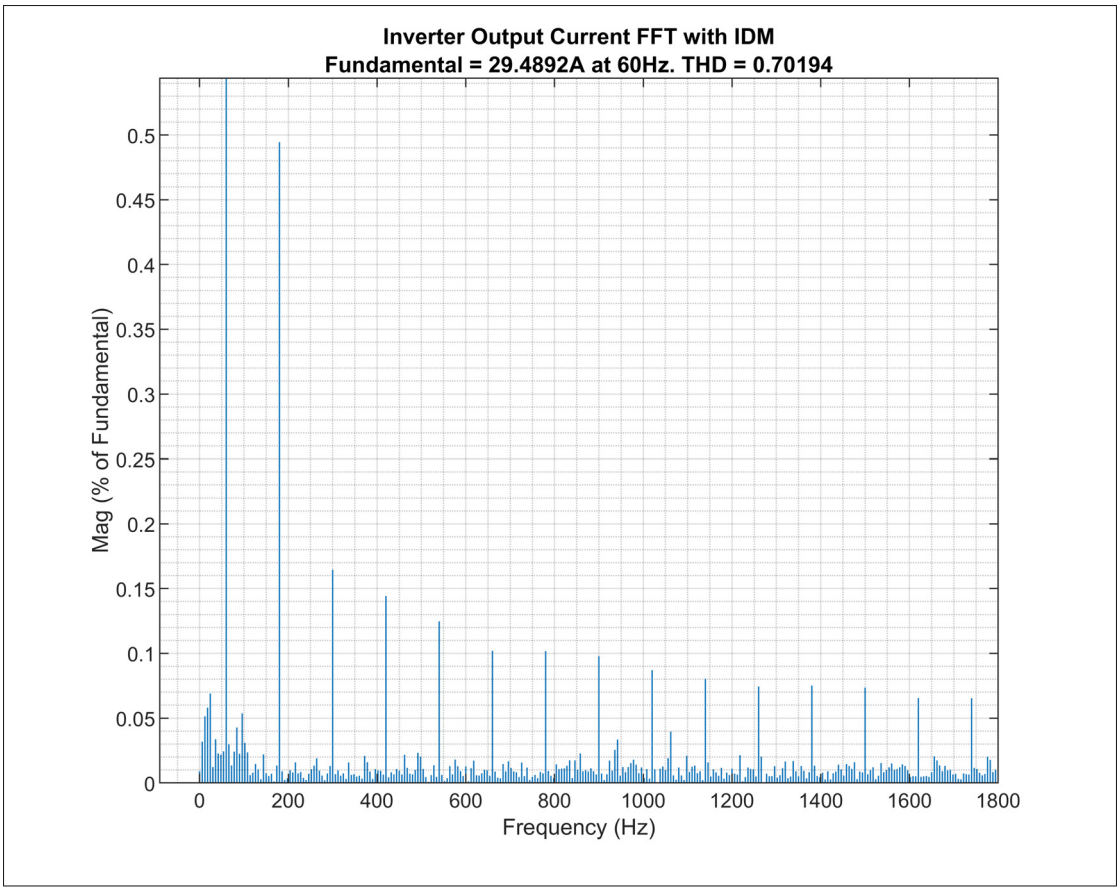

Figure 5.16 Inverter output current frequency spectrum with IDM

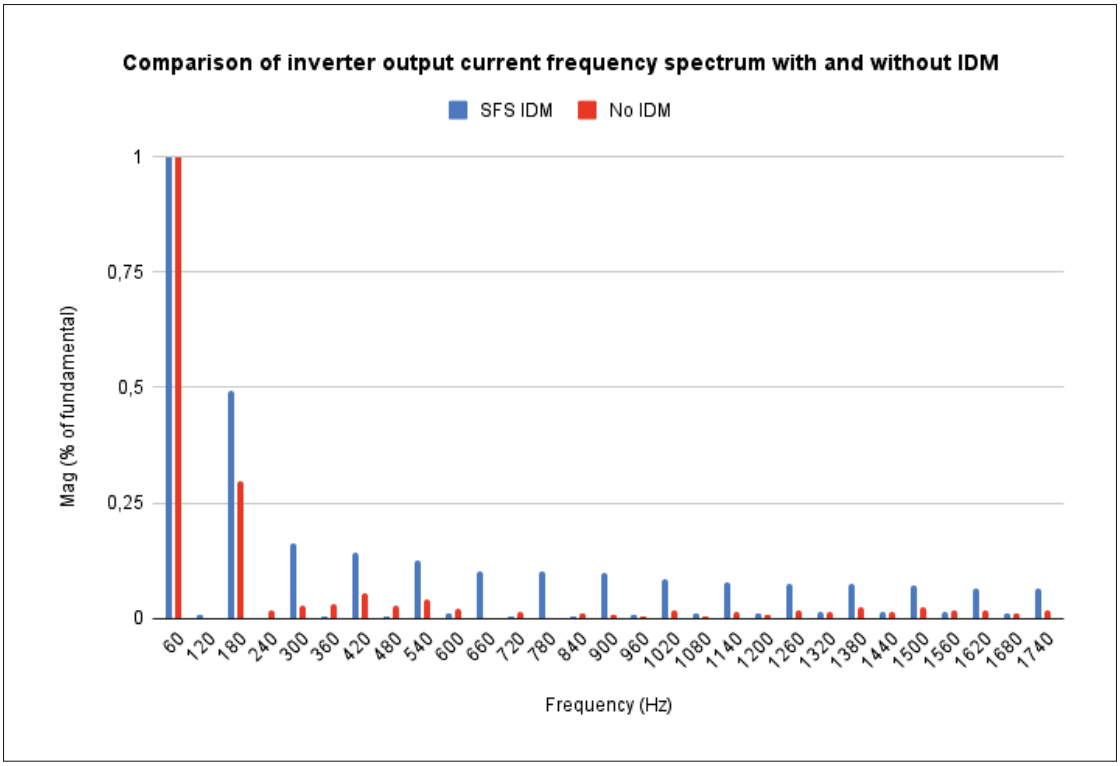

Figure 5.17 Comparison of inverter output current frequency spectrum with and without IDM

5.5.3 Simulation results

Figure 5.18 shows the circuit configuration used to test the islanding detection method. A RLC load is connected in parallel to the inverter output and to the grid through a circuit breaker. The island condition is created by opening the circuit breaker. It is known that a balanced inverter generation to load condition creates the most difficult island to detect. Since the power mismatch between the inverter generation and load is small, a minimal amount of current is flowing through the circuit breaker and its opening will not result in a significant change in voltage or frequency at the PoC. In order to properly test the islanding detection capability of the inverter when the generation and load are equal, different test cases are defined to evaluate its effectiveness for multiple combinations of inverter power levels, grid support functions and

loads. These test cases are a subset of the test matrix given in (IEEE, 2020) and are summarized in Table 5.6.

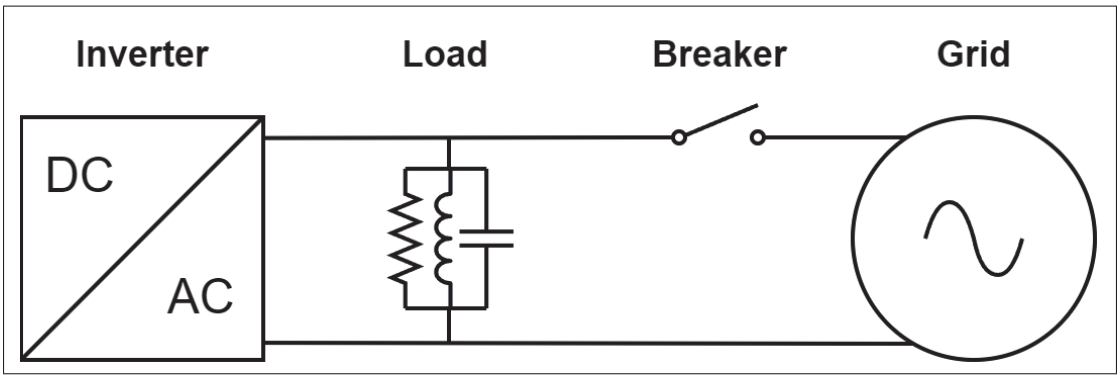

Figure 5.18 Islanding detection test circuit

Table 5.6 Islanding Detection Test Cases

Test case	P_{inv}	Q_{inv}	**Reactive Power GSF**	**Active Power GSF**	P_R	Q_C	Q_L	Q_f
1	1.00	0.00	CPF	None	-1.00	1.00	-1.00	1.00
2	0.50	0.00	CPF	None	-0.50	0.50	-0.50	1.00
3	0.90	-0.44	CPF	FW	-0.90	0.90	-0.46	1.00
4	0.90	0.44	CPF	FW	-0.90	0.46	-0.90	1.00
5	1.00	0.00	VVAR	FW	-1.00	1.00	-1.00	1.00
6	0.50	0.00	VVAR	FW	-0.50	0.50	-0.50	1.00

P_{inv} and Q_{inv} are the inverter active and reactive power operating points respectively, while P_R, Q_C and Q_L are the load active power, capacitive and inductive reactive powers. A negative power means that it is absorbed by the load. Finally, the load quality factor Q_f is defined by equation (5.11).

$$Q_f = \frac{\sqrt{Q_L \cdot Q_C}}{P_R} \tag{5.11}$$

The inverter is tested with the voltage ride-through parameters given in Table 5.4 and the frequency ride-through parameters given in Table 5.7. The Volt-VAR and Frequency-Watt grid support function parameters that are used are given in Tables 5.2 and 5.3 respectively.

Table 5.7 Frequency ride-through requirements

Frequency (Hz)	**Operation mode**	**Min. ride-through time (s)**	**Max. response time (s)**
$f > 62$	Cease to energize	N/A	0.16
$61.2 < f \leq 61.8$	Mandatory operation	299	300
$58.8 \leq f \leq 61.2$	Continuous operation	N/A	N/A
$57.0 \leq f < 58.8$	Mandatory operation	299	300
$f < 57.0$	Cease to energize	N/A	0.16

Furthermore, the rate of change of frequency (ROCOF) protection is set to $4.0Hz/s$, measured over an averaging window of 0.1s. As its name implies, this protection element operates and trips the inverter when the ROCOF is greater than the setting.

The same procedure is used for each test case and is the following:

1. The inverter is brought to steady-state under the conditions enumerated in Table 5.6
2. The load to generation balance is validated by making sure that the power flowing through the circuit breaker is less than 2% of the inverter rated power
3. The circuit breaker is opened to form an island

5.5.3.1 Test case 1

Test case 1 is first simulated without the IDM enabled in order to show that the inverter can sustain an islanded condition and to demonstrate the necessity of implementing an islanding detection method. Figure 5.19 presents the active and reactive powers measured at the load and circuit breaker. Figure 5.20 presents the measured inverter output voltage, current and frequency as well as the circuit breaker command signal and the inverter trip signal. The circuit breaker opens when its command signal goes from 1 to 0, while the inverter trips when the trip signal goes from 0 to 1.

It can be seen that the generation and load are balanced prior to the circuit breaker opening at $t = 1$s and that once the island is formed, the inverter keeps energizing the load and remains connected without any perturbation on voltage or frequency.

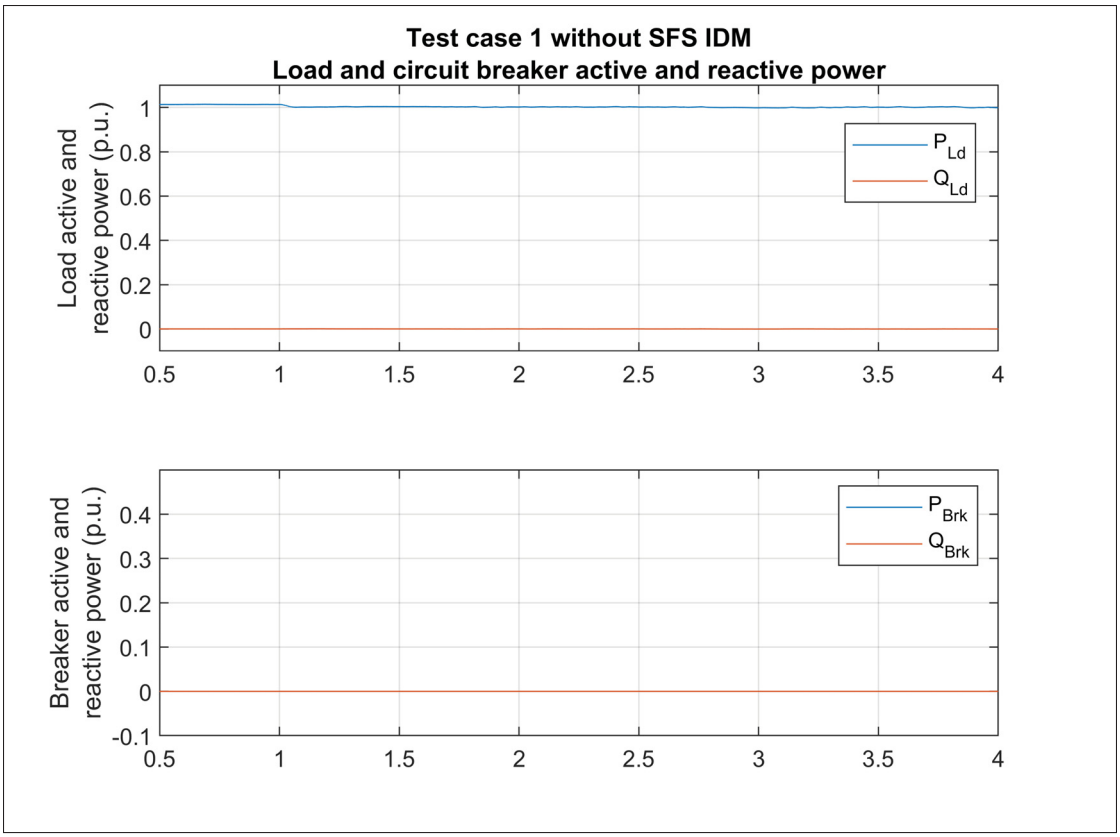

Figure 5.19 Test case 1 without SFS IDM. Load and circuit breaker active and reactive power

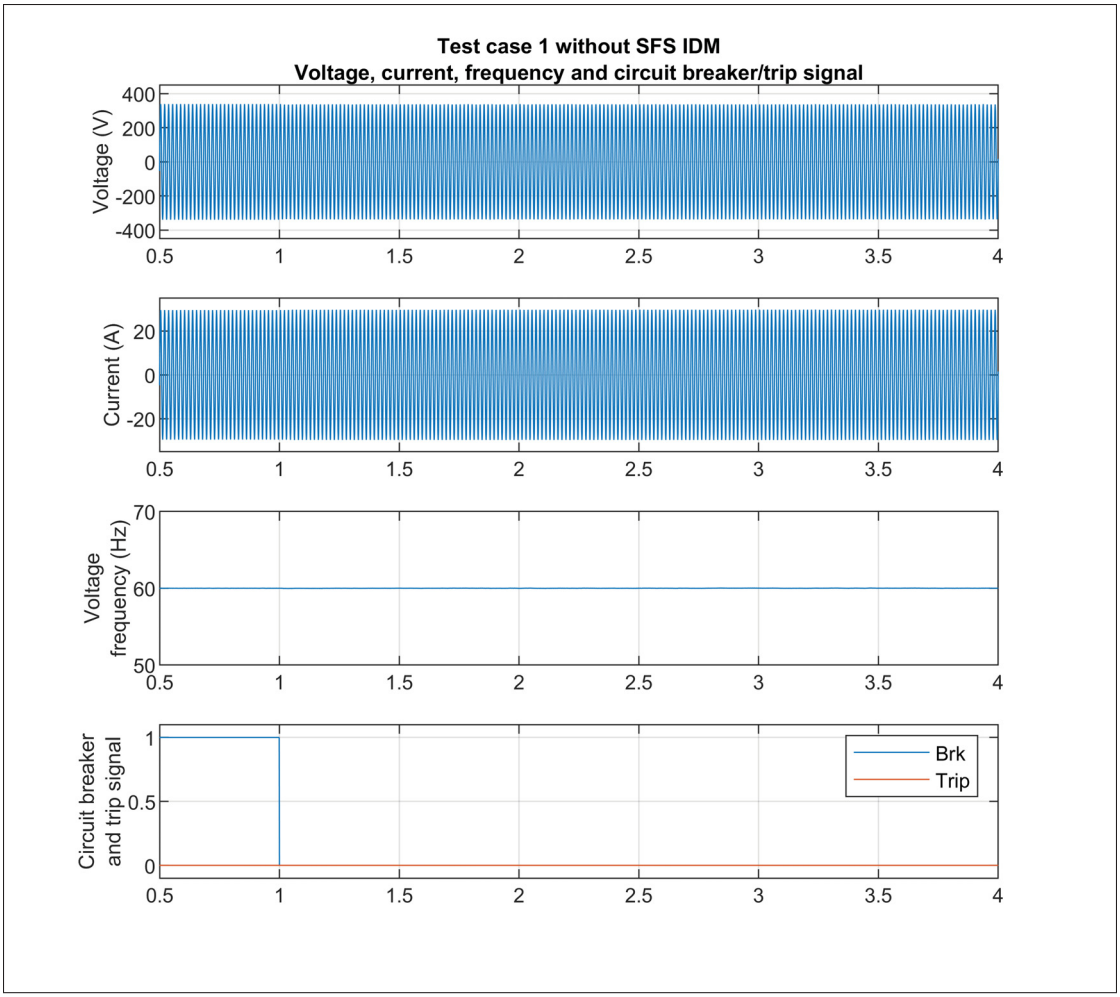

Figure 5.20 Test case 1 without SFS IDM. Voltage, current, frequency and circuit breaker/trip signal

Test case 1 is run once again with the SFS IDM enabled and the simulation results are presented in Figures 5.21 and 5.22. As soon as the circuit breaker is opened and the island is formed, the SFS IDM forces an accelerated frequency drift until the ROCOF protection element operates and trips the inverter within 105ms, which is below the required value of 2s. It should be noted that low-pass filters with a time constant of 0.05s are used for the load and circuit breaker power measurements, which explains the response time observed in the load active power of Figure 5.21.

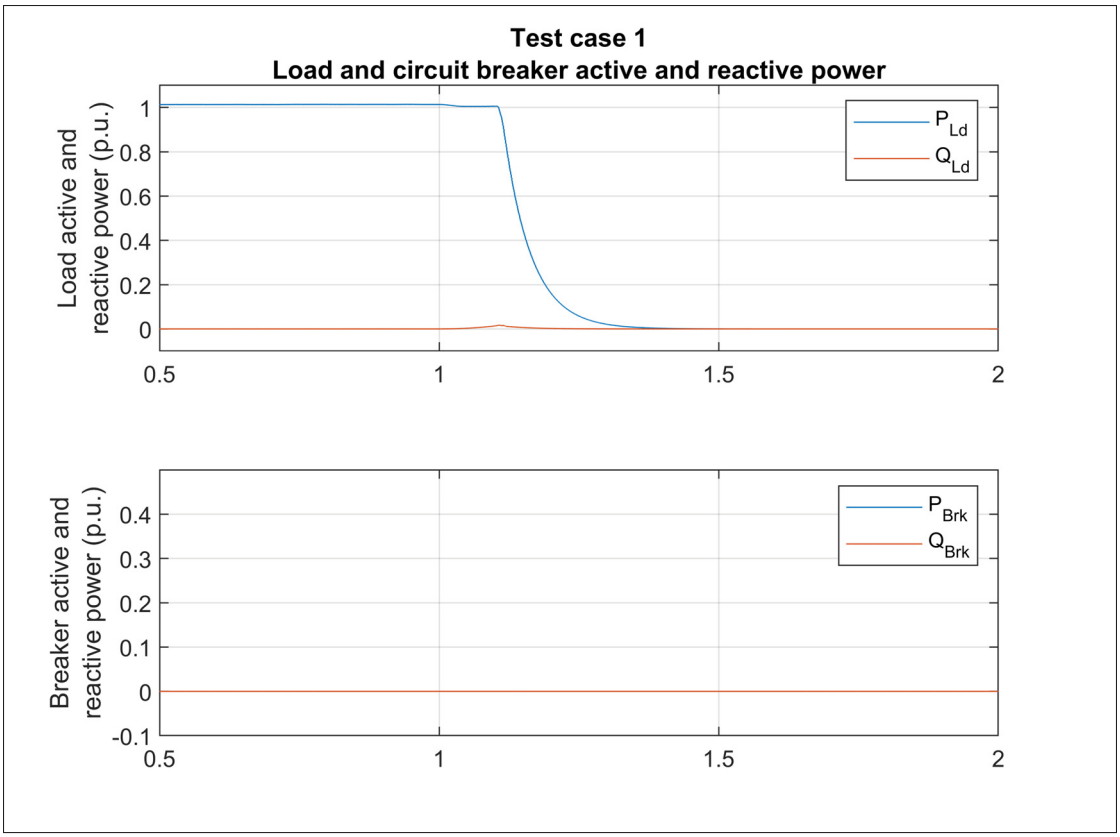

Figure 5.21 Test case 1. Load and circuit breaker active and reactive power

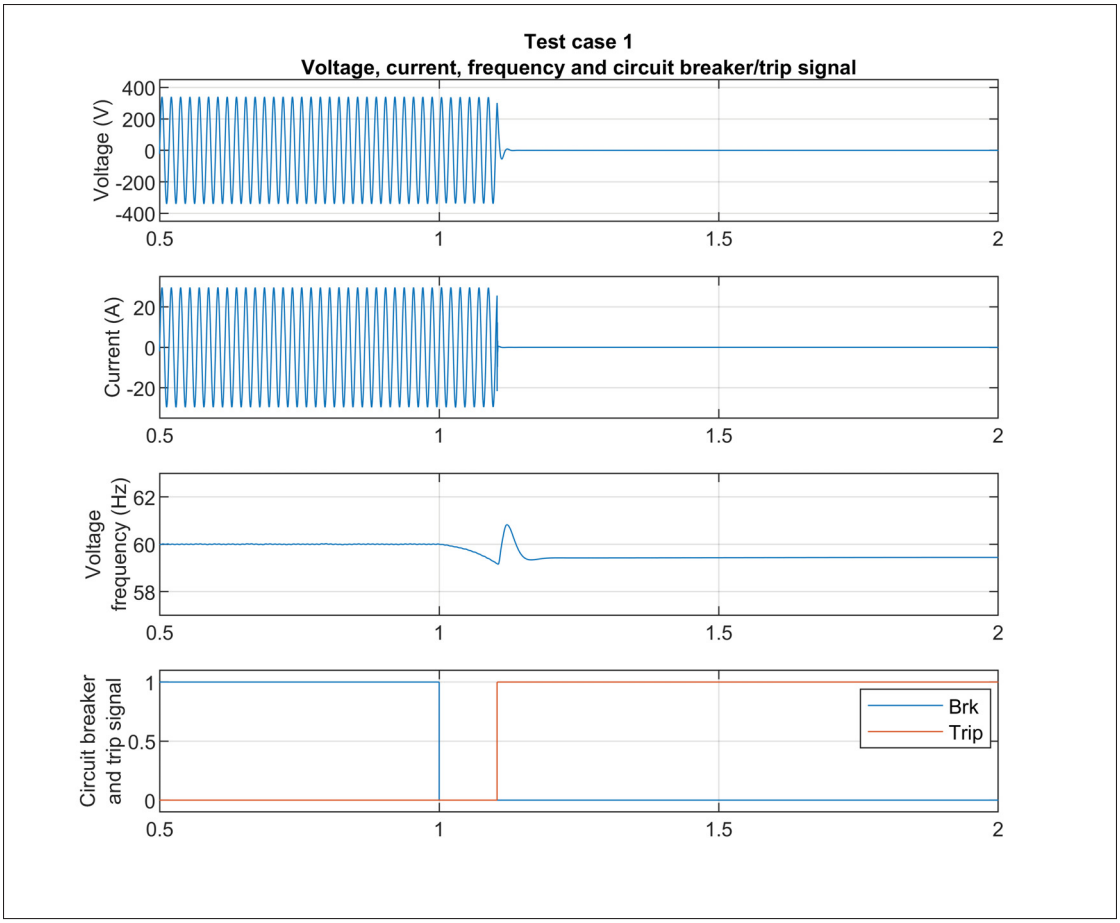

Figure 5.22 Test case 1. Voltage, current, frequency and circuit breaker/trip signal

5.5.3.2 Test case 2

Simulation results for test case 2 are presented in Figures 5.23 and 5.24 respectively. The inverter active power output is set to 0.5p.u. by limiting the available PV array power with the irradiance at $500W/m^2$. The island is formed at $t = 1$s and once again the ROCOF protection algorithm operates, caused by the frequency drift accelerating and tripping the inverter within $225ms$.

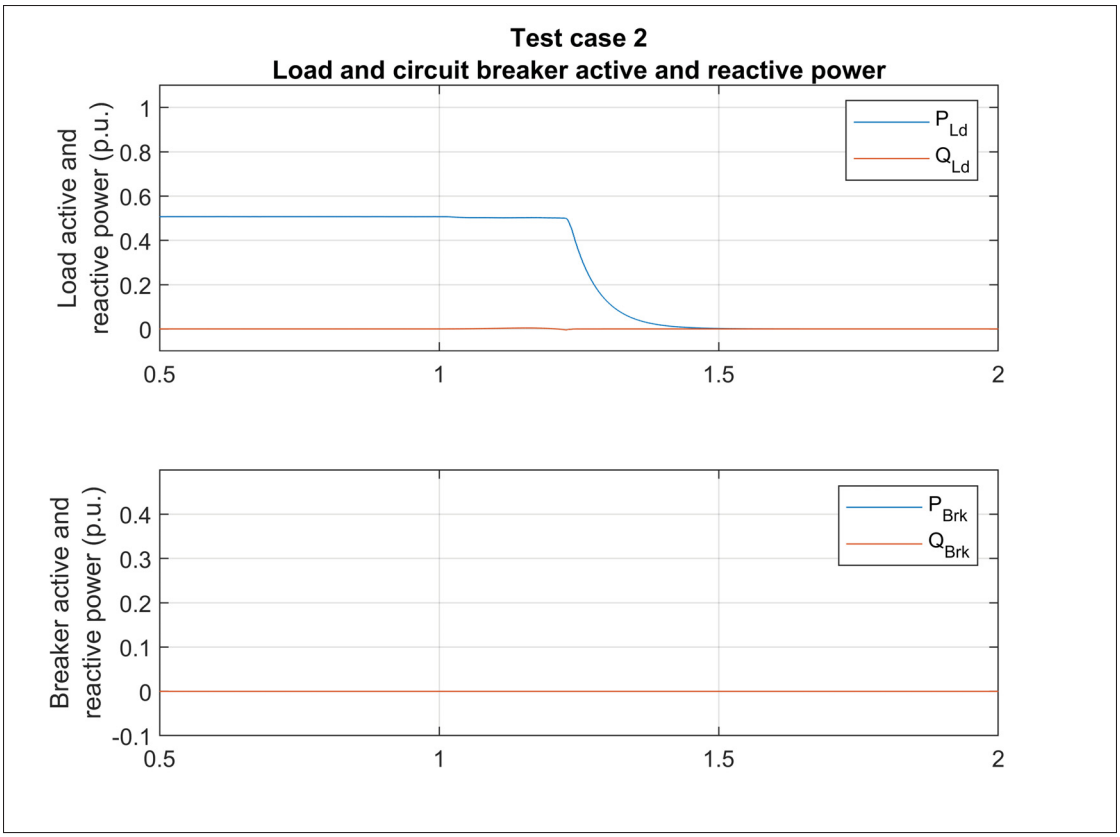

Figure 5.23 Test case 2. Load and circuit breaker active and reactive power

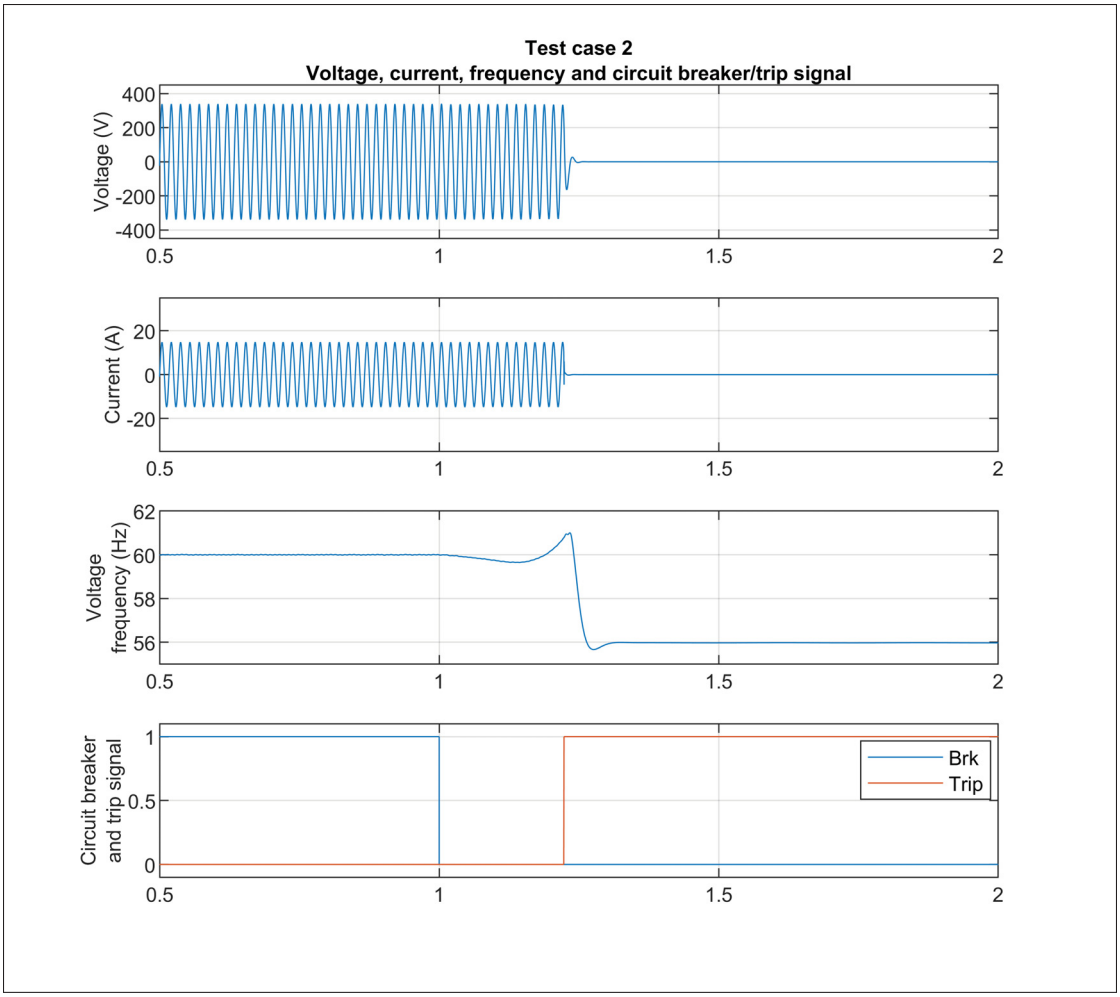

Figure 5.24 Test case 2. Voltage, current, frequency and circuit breaker/trip signal

5.5.3.3 Test case 3

Simulation results for test case 3 are presented in Figures 5.25 and 5.26 respectively. The inverter absorbs reactive power to balance the capacitive load. The island is formed at $t = 1$s and, as observed in Figure 5.26, the ROCOF protection element operates and trips the inverter within $110ms$. Even with the Frequency-Watt grid support function activated, the SFS IDM forces the frequency to drift fast enough to detect the island without giving time for the FW function to curtail power and ride-through the disturbance.

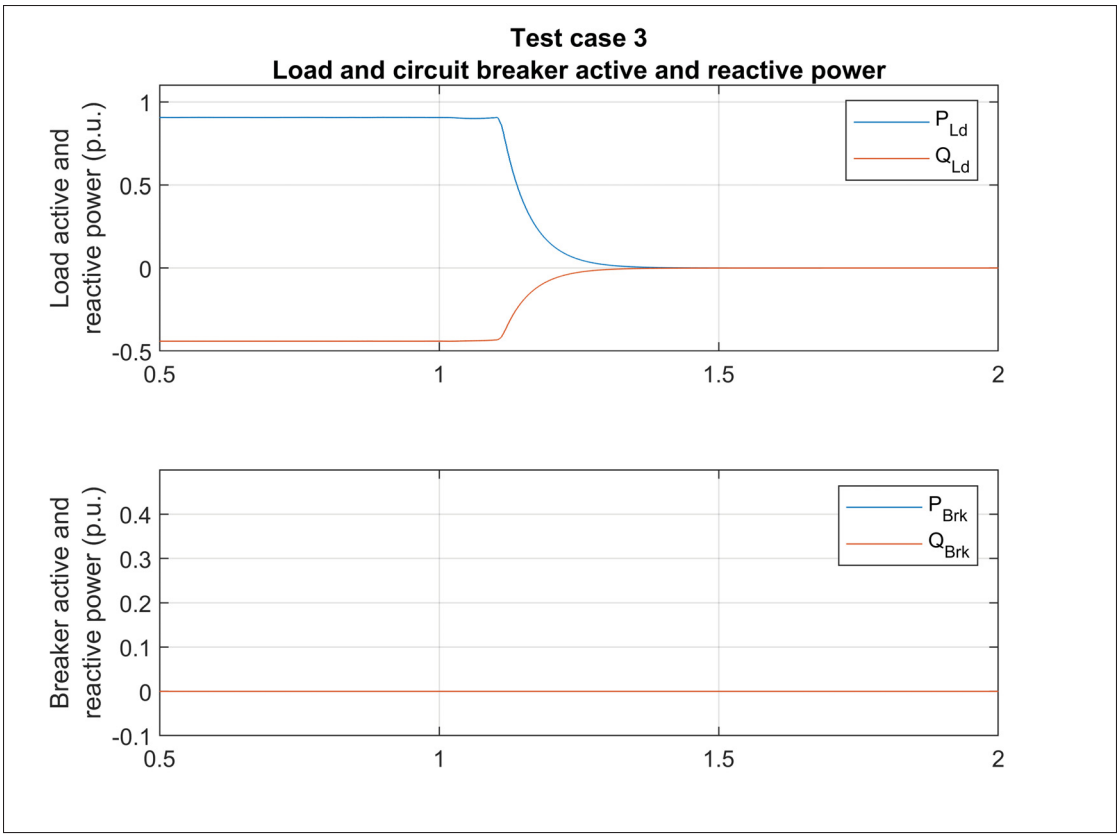

Figure 5.25 Test case 3. Load and circuit breaker active and reactive power

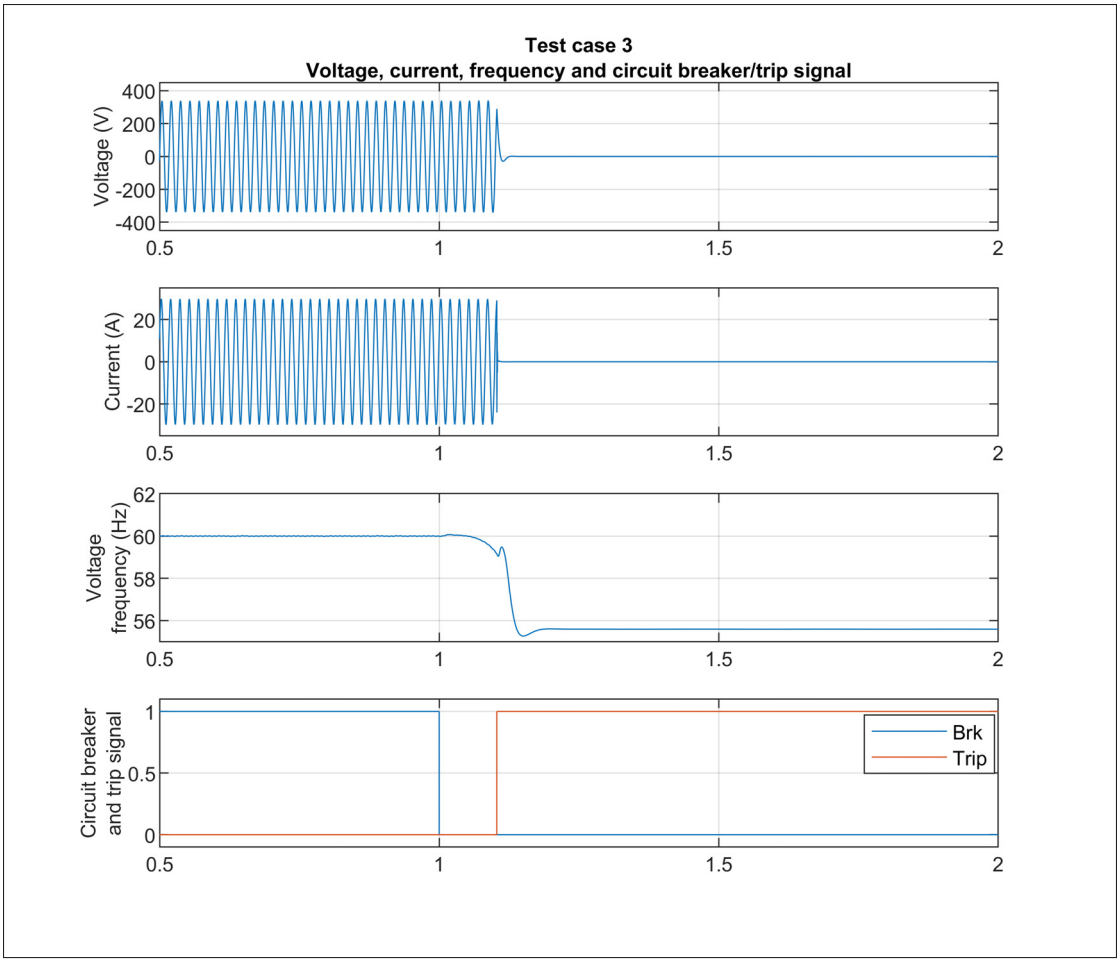

Figure 5.26 Test case 3. Voltage, current, frequency and circuit breaker/trip signal

5.5.3.4 Test case 4

Simulation results for test case 4 are presented in Figures 5.27 and 5.28 respectively. This time, the inverter injects reactive power to balance the inductive load. The island is formed at $t = 1$s and, as observed in Figure 5.28, the ROCOF protection element operates and trips the inverter within $73ms$.

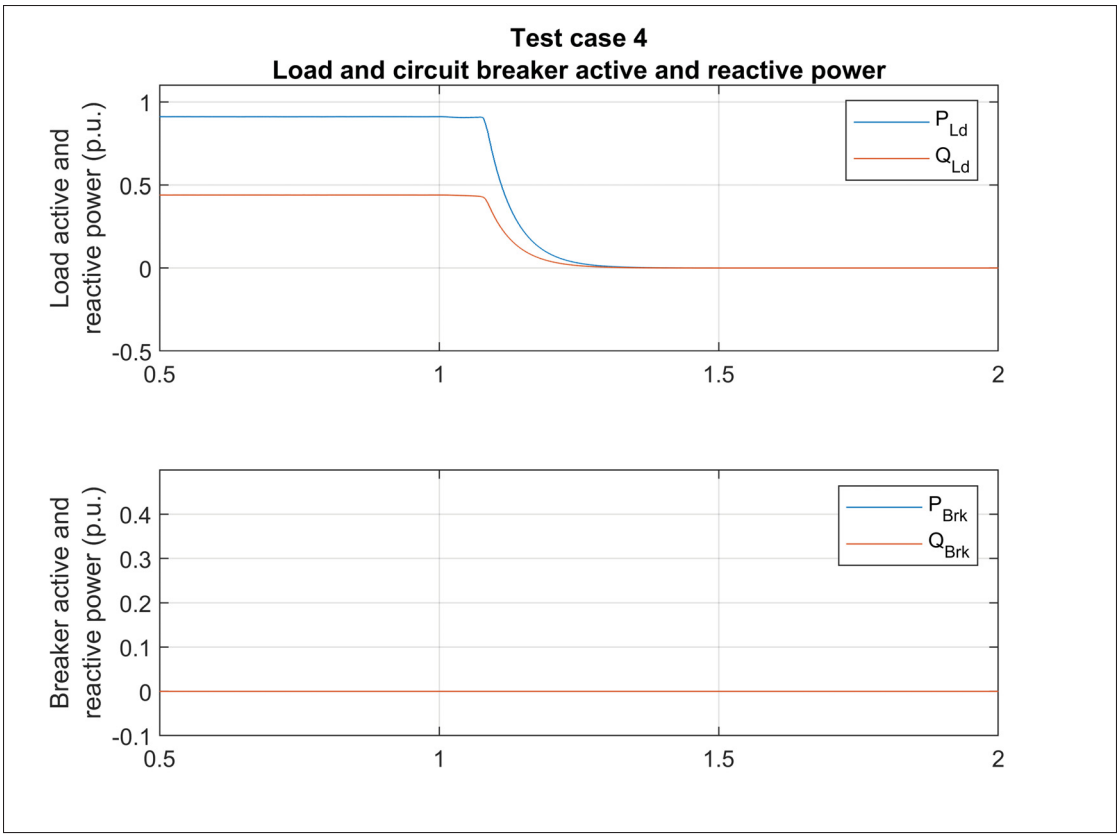

Figure 5.27 Test case 4. Load and circuit breaker active and reactive power

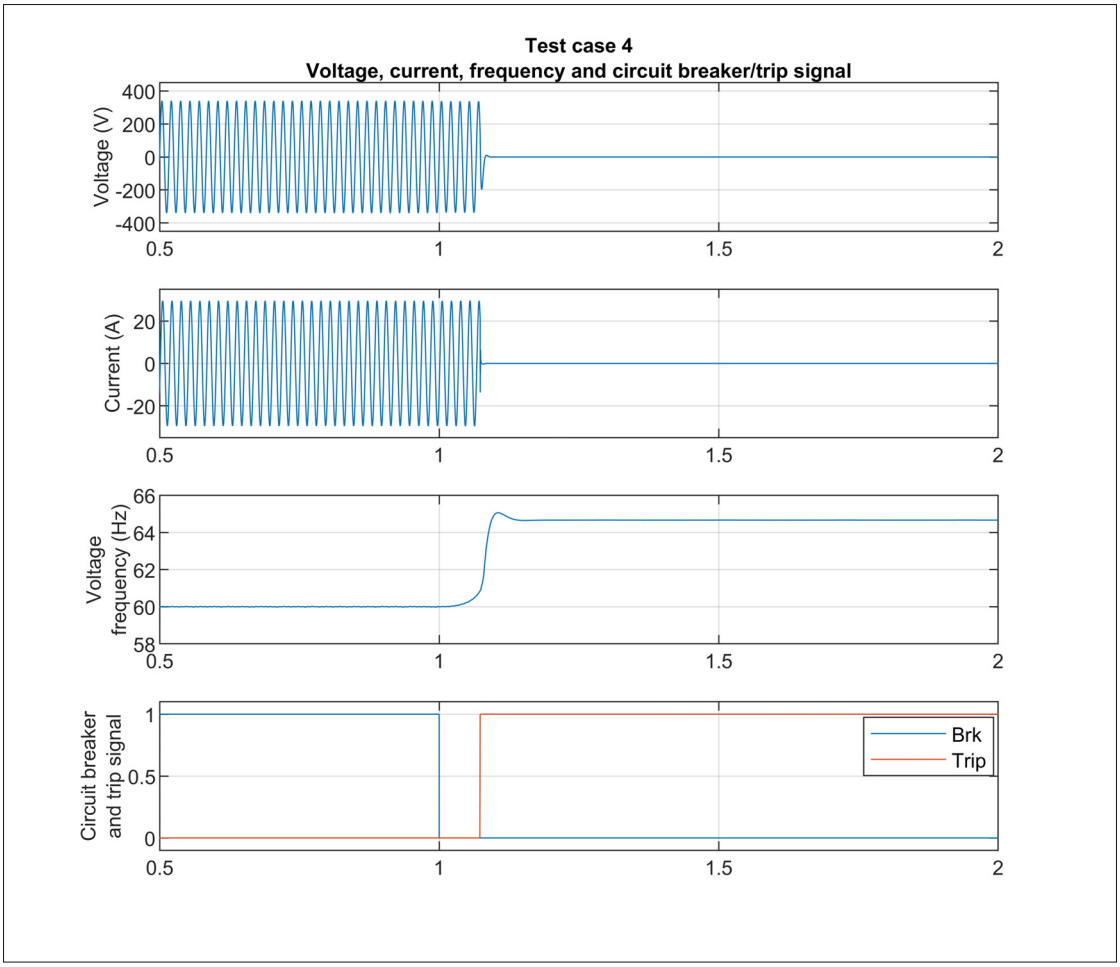

Figure 5.28 Test case 4. Voltage, current, frequency and circuit breaker/trip signal

5.5.3.5 Test case 5

Simulation results for test case 5 are presented in Figures 5.29 and 5.30 respectively. The Volt-VAR grid support function is activated to verify its impact on the inverter islanding detection capability. The island is formed at $t = 1$s and, as observed in Figure 5.30, the ROCOF protection element operates and trips the inverter within $120ms$. Once again, the VVAR grid-support function has little impact on the island detection time.

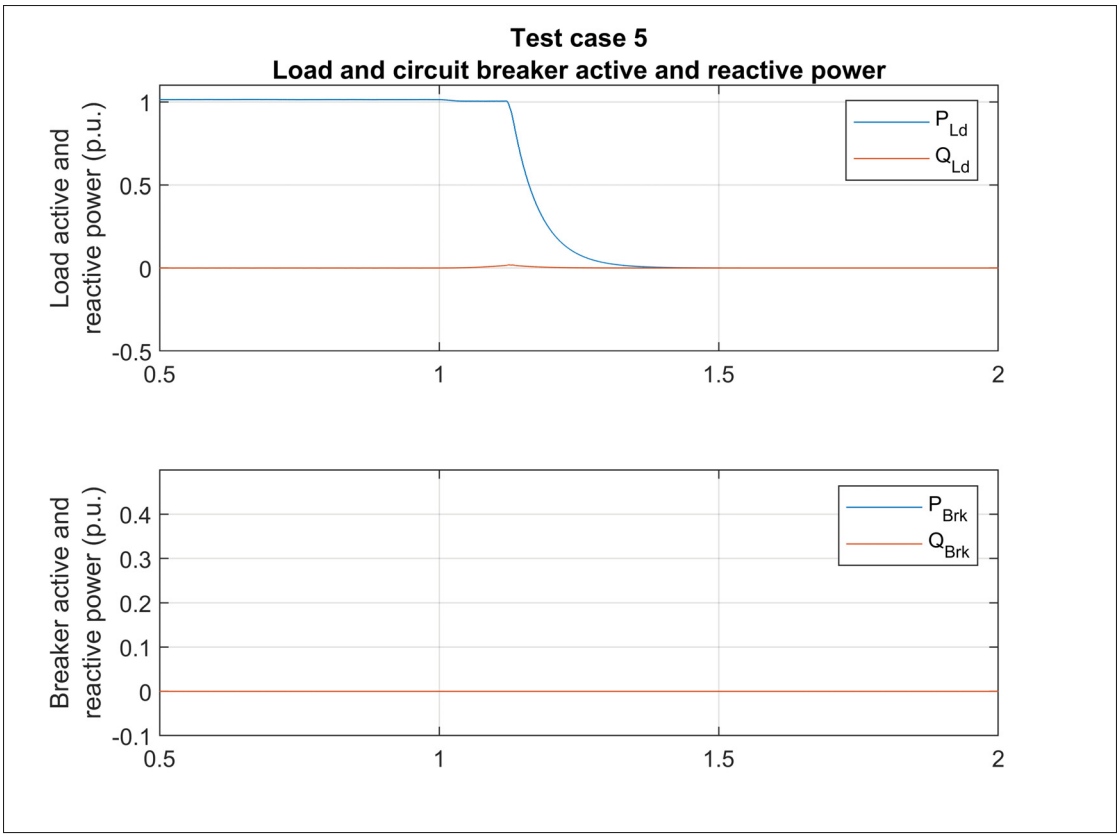

Figure 5.29 Test case 5. Load and circuit breaker active and reactive power

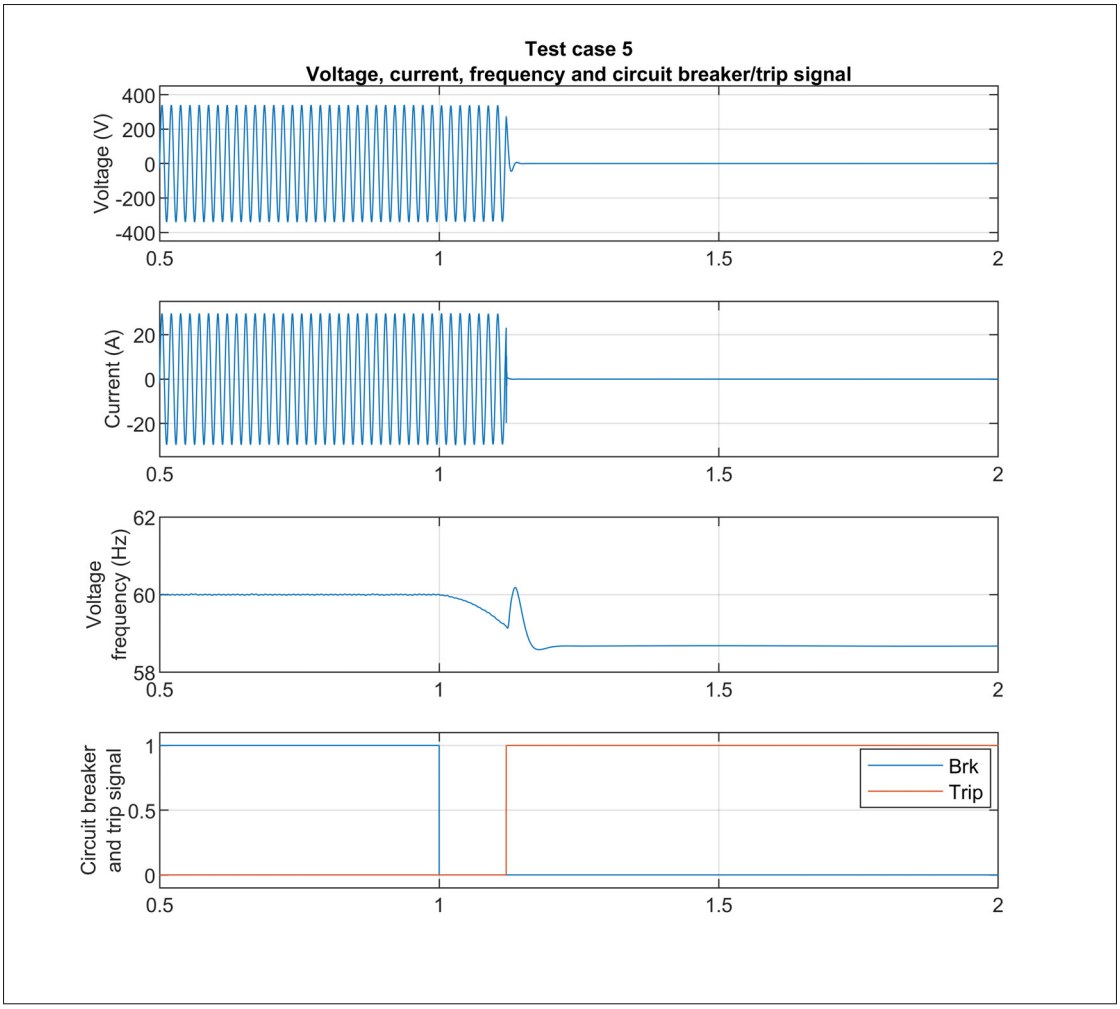

Figure 5.30 Test case 5. Voltage, current, frequency and circuit breaker/trip signal

5.5.3.6 Test case 6

Simulation results for test case 6 are presented in Figures 5.31 and 5.32 respectively. The same grid support functions as the previous test are activated while the inverter active power output is set to 0.5p.u. by limiting the available PV array power with the irradiance at $500W/m^2$. The island is formed at $t = 1$s and, as observed in Figure 5.32, the ROCOF protection element operates and trips the inverter within $215ms$. Once again, the VVAR grid-support function has little impact on the island detection time.

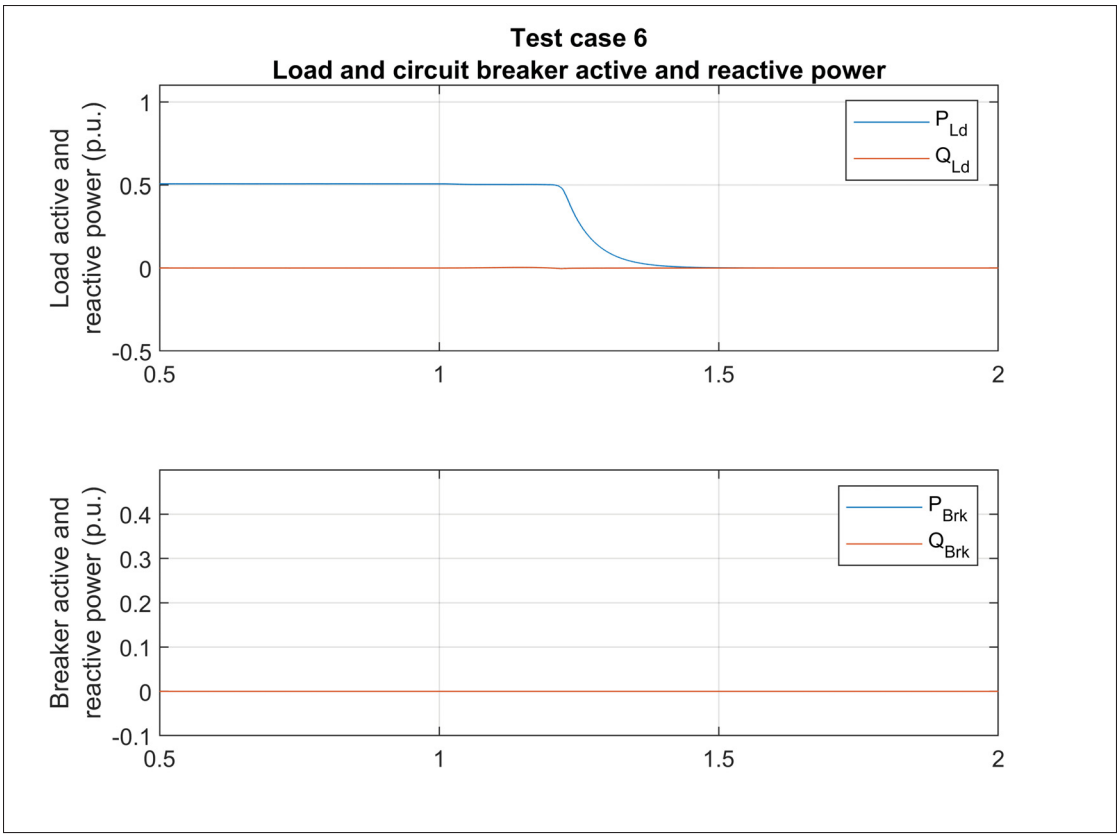

Figure 5.31 Test case 6. Load and circuit breaker active and reactive power

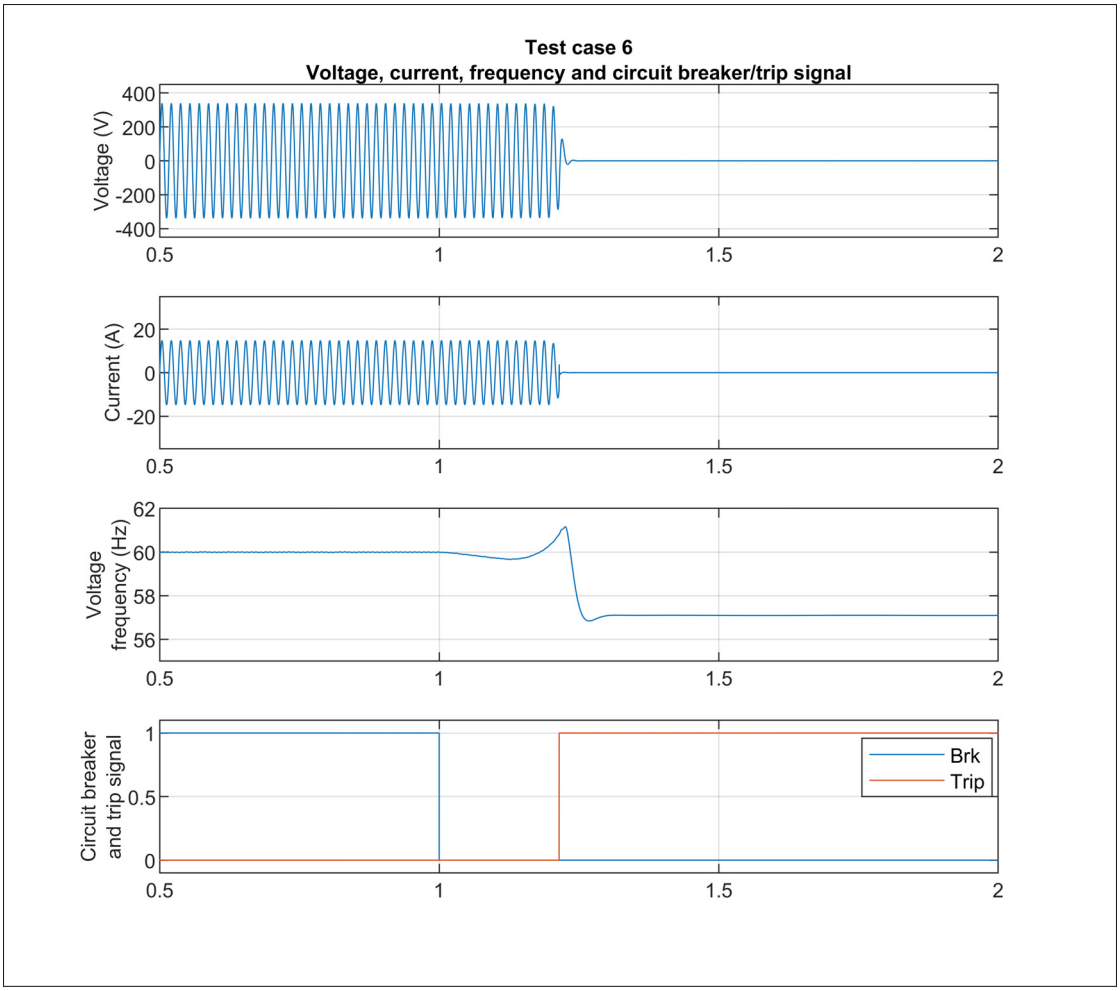

Figure 5.32 Test case 6. Voltage, current, frequency and circuit breaker/trip signal

5.6 Conclusion

In this chapter, grid support functions were added to the designed inverter and tested in order to validate their proper implementation. It was also demonstrated how they can contribute to grid stability by actively supporting the voltage and frequency while riding through voltage perturbations and finally detecting unintentional islanding. First, the outer active and reactive power control loops used to generate the current reference based on the grid support functions logic were introduced. The voltage-reactive power (Volt-VAR) function was then implemented

and tested to demonstrate how it enables the inverter to contribute to voltage regulation at its PoC by either absorbing or injecting reactive power based on a predefined piecewise linear curve. Comparison with the Constant Power Factor function have shown the effectiveness of the Volt-VAR to limit voltage excursions. Furthermore, the inverter ability to autonomously adjust the Volt-VAR curve to the measured PoC voltage was presented. The Frequency-Watt grid support function was also implemented and tested, which enables the inverter to mitigate frequency deviations by curtailing active power following a droop curve in case of high-frequency caused by events on the grid such as the loss of large loads. The inverter capability to ride-through voltage excursions was then demonstrated. The test sequence showed that the inverter maintains synchronism with the grid and continues to supply power or cease to energize depending on the magnitude of the voltage excursions for the minimum ride-through times as required by the interconnection standard (IEEE, 2018), without tripping. Finally, the inverter ability to detect unintentional islanding was demonstrated. The Sandia Frequency Shift active islanding detection method was introduced and parameterized in order to limit its impact on the inverter output power quality while offering a fast and efficient islanding detection. Multiple test cases were simulated to verify its performance for balanced generation to load conditions with different combinations of grid support functions.

CONCLUSION AND RECOMMENDATIONS

This thesis presented the design of a low-voltage (residential scale) grid-connected single-phase inverter for the interconnection of photovoltaic resources. An overview of the inverter system topology under study was provided in the first chapter along with details pertaining to its fundamental components. The design of the output LCL filter was first carried out to limit the harmonic content of the inverter output current. To do so, a step-by-step design procedure that uses the inverter system parameters and desired performance metrics as inputs was developed and applied to the inverter under study. Simulation of the designed filter demonstrated that it successfully reduces the inverter output current THD well below the required limits established in the standards while using compact passive components that are commercially available.

The mathematical model of the grid-connected inverter system in the Laplace domain was derived and used as the theoretical basis to design and analyze the proportional-resonant current controller. This controller type was selected for its demonstrated ability to provide accurate reference tracking in the natural reference frame without steady-state error. Furthermore, active damping of the output filter resonant frequency was discussed and implemented using the feedback of the filter capacitor current in the current control loop. Another step-by-step design procedure was introduced in order to optimally design the controller parameters with regards to the desired closed-loop performance requirements. It was demonstrated that the performance and stability of grid-connected inverters are impacted by the strength of the grid as seen from the point of connection (PoC) of the inverter. The current controller design was then carried out using the developed procedure and considering a weak grid to ensure that the inverter would perform well over a wide range of operating conditions. Simulation of the inverter system validated that it is stable, provides good dynamic performance and perturbation rejection capabilities.

The general structure and topology of a single-phase phase-locked loop used to synchronize the inverter to the grid voltage was then presented along with its mathematical model. Equations were derived from the PLL transfer function to establish the relationship between the loop filter gains and the PLL dynamic response in terms of overshoot and settling time, allowing to select appropriate values. Additionally, an adaptive notch filter was implemented in the PLL structure to eliminate the component at twice the nominal frequency that appears in its output. Once again, the designed PLL performance was tested in simulation and it was demonstrated that it has a satisfactory dynamic response.

Finally, grid support functions were added to the designed inverter. The voltage-reactive power (Volt-VAR), frequency-watt (droop), voltage ride-through (VRT) and islanding detection functions were discussed and implemented. Test procedures adapted from the standards were used to validate the proper behaviour of these functions and demonstrate how an inverter can actively contribute to grid stability.

It was shown that the designed system is compliant with the interconnection standards and meets the established objectives, namely:

1. Have good dynamic performance.
2. Provide appropriate power quality, i.e. low output current distortion.
3. Remain stable over a wide range of equivalent output impedance at the point of connection.
4. Ride-through under- and over-voltage events.
5. Support grid voltage and frequency through advanced active and reactive power control.

To extend this research further, one could perform tests with the inverter when connected to a grid with an increased voltage THD. Changes in the current controller topology or design process would be required in order to damp the resulting additional harmonics.

The interoperability and interactions between multiple inverters connected to the same feeder could also be studied to determine the impact of grid support functions on grid stability and voltage/frequency regulation in the presence of an increased penetration of inverter-based resources at low-voltage.

The designed inverter could also be modified to be used with a battery energy storage system as the primary source. That would allow a bi-directional active power flow and extend the capabilities of some grid support functions like the Frequency-Watt, where active power could be absorbed during over-frequency. By implementing an external voltage control loop, the inverter could also be used as a grid-forming device while islanded, controling the voltage and frequency at its PoC and allow it to power critical loads while disconnected from the grid. Other control strategies that provide further grid support also exist and could be studied, most notably to emulate inertia and provide a more robust frequency regulation capability in areas with a high penetration of inverter-based resources.

Finally, additional emphasis could also be given to the DC side of the inverter. Since the focus of this project was the design and control of the inverter, the PV array was simulated with constant operating conditions and was connected to the DC-link through an average buck-boost converter modeled using a switching-function model controlled by the MPPT. By replacing this converter by a detailed model using switching devices and by modeling the variability of the primary source, i.e. the solar irradiance and/or operating temperature, other details would need to be considered for the design of the inverter system, including:

1. Optimal selection of the DC-link capacitor.
2. Design of the DC/DC converter input filter.
3. Impact of primary source variability (e.g. partial shading) on the selection and tuning of the MPPT algorithm and on power quality.

APPENDIX I

LCL FILTER DESIGN SCRIPTS AND MODELS

This appendix details the functions, scripts and models that were developed in order to automate the design procedure of the inverter output filter as presented in Chapter 2.

A first model, shown in Figure I-1, was developed to simulate the switching of a single-phase full-bridge inverter connected to a resistive load in order to record the output voltage waveform to be analyzed using a FFT and to ultimately determine the dominant harmonic order used to design the filter grid-side inductor.

It is possible to select which SPWM technique is used. The unipolar and bipolar subsystem models are presented in Figures I-2 and I-3 respectively. The DC-link is modeled using constant DC voltage sources and the full-bridge uses simplified models of insulated gate bipolar transistors (IGBT) with antiparallel diodes.

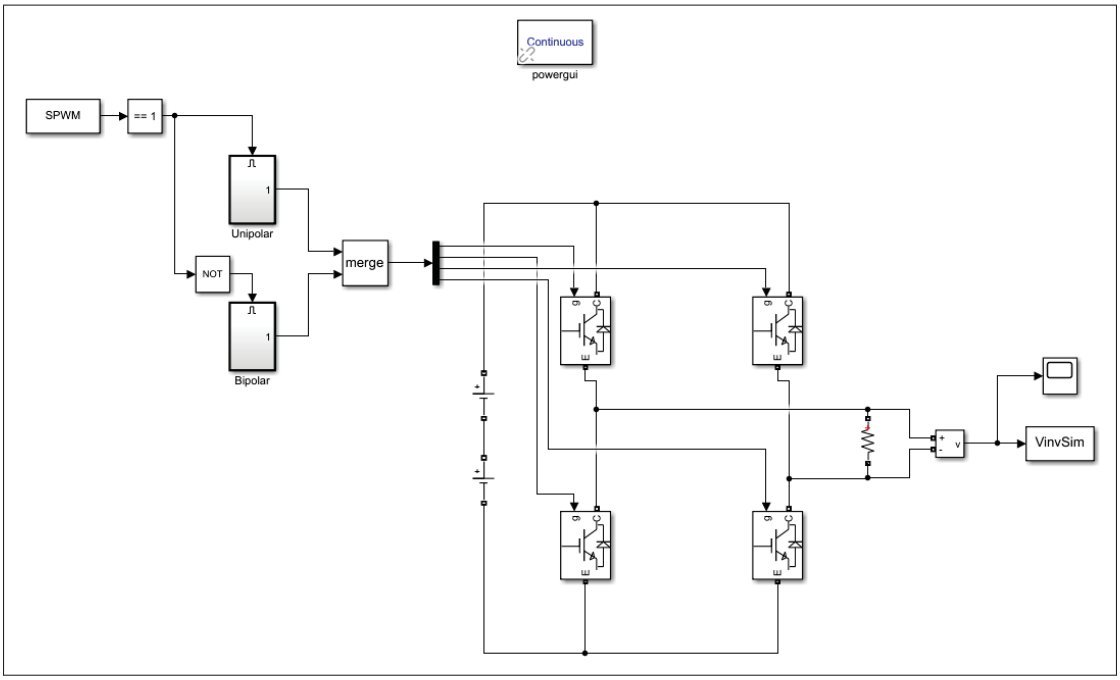

Figure-A I-1 Simulink model of the single-phase full-bridge inverter

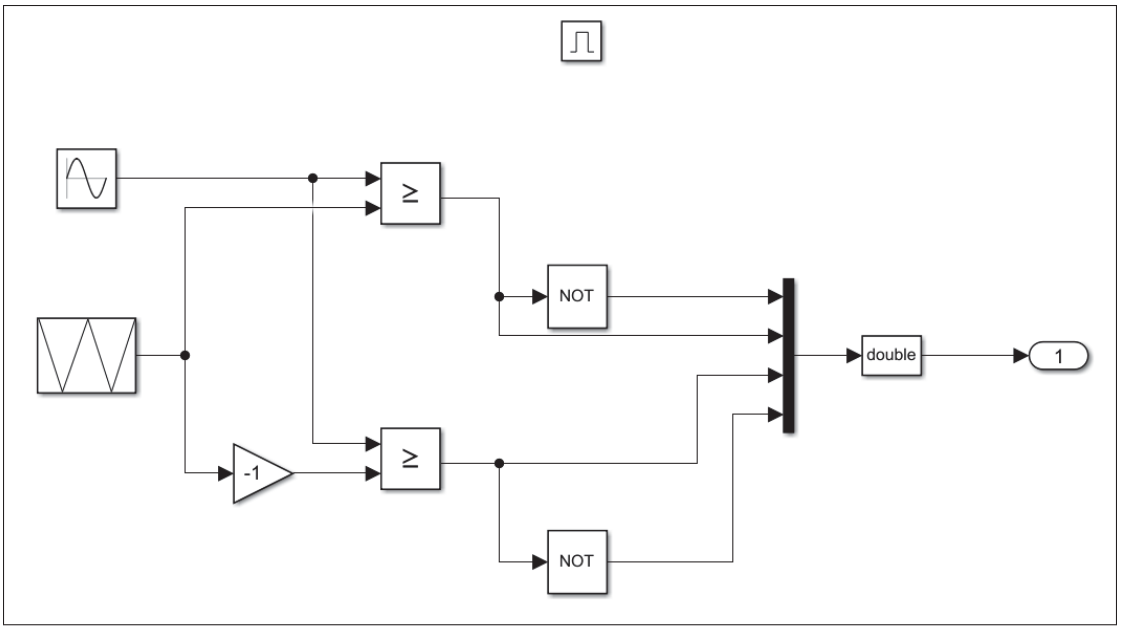

Figure-A I-2 Simulink model of the unipolar subsystem

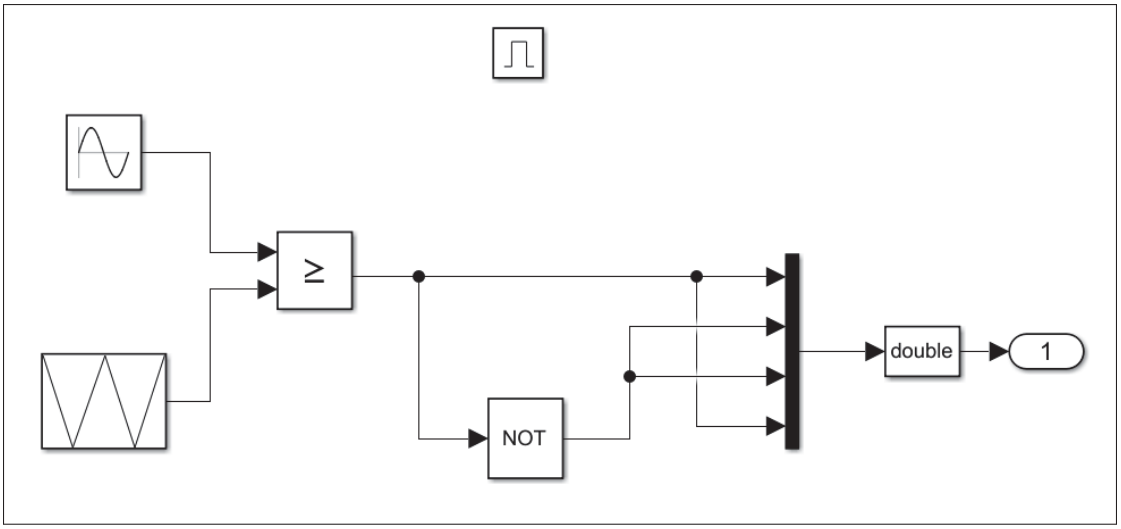

Figure-A I-3 Simulink model of the bipolar subsystem

The second model, shown in Figure I-4, is identical to the previous one, except it contains the LCL filter at the inverter output. The resistive load is sized to consume the rated inverter power of 5kW. This model is used to simulate the output filter, record the relevant voltages and currents and validate the performance of the designed filter.

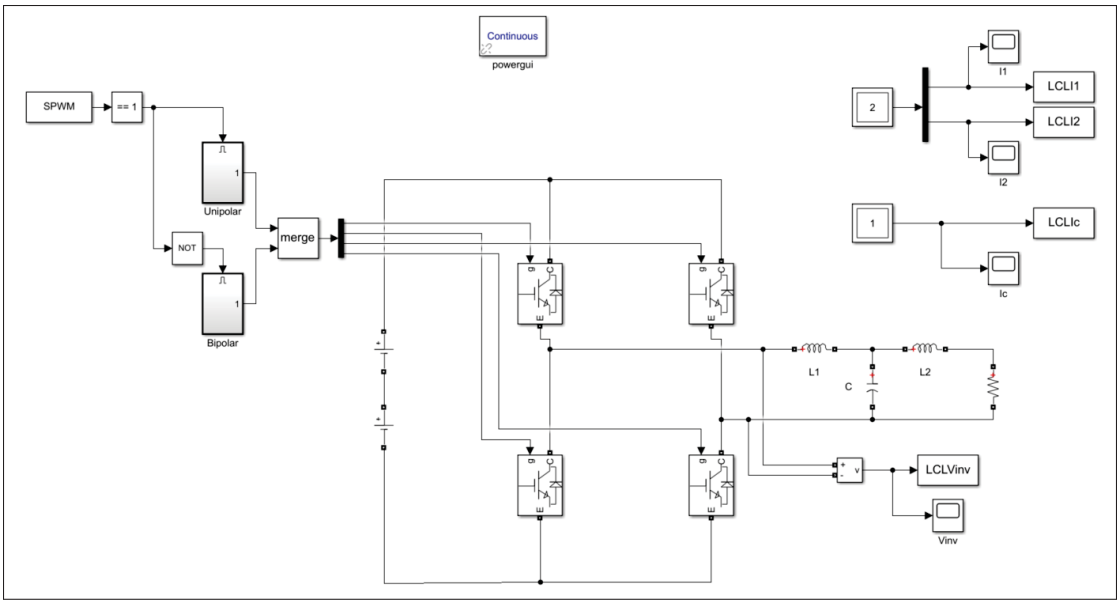

Figure-A I-4 Simulink model for the validation of the LCL filter performance

As explained, the filter design procedure was automated by developing a Matlab function, LCL_design.m, presented hereafter. The function inputs are the inverter system parameters, namely the nominal output (grid) RMS voltage, rated active power, DC link voltage, grid frequency, switching frequency and SPWM technique, as well as the desired filter performance metrics, namely the desired current ripple coefficient and percentage of reactive power introduced by the capacitor. The functions outputs are the values of the inverter and grid-side inductors and the capacitor.

```
function [L1,L2,Cf] = LCL_design(Vnom,Pnom,Vdc,Fnom,Fsw,SPWM,Rip,X)
%%
%   This function helps designing a LCL filter for single-phase ...
    inverters
%   with sinusoidal PWM
%
%   Input parameters:
%
%   Vnom = Inverter output RMS voltage, V
%   Pnom = Inverter rated active power, W
```

```
%   Vdc = DC link voltage, V
%   Fnom = Grid nominal frequency, Hz
%   Fsw = Inverter switching frequency, Hz
%   SPWM = SPWM type: 0 = Bipolar, 1 = Unipolar
%   Rip = Desired current ripple coefficient, usually around 20-30%
%   X = Percentage of reactive power introduced by the filter capacitor,
%       usually around 5%
%
%   References:
%   Ruan X, Wang X, Pan D, Yang D, li W, Bao C. Control Techniques for
%   LCL-Type Grid-Connected Inverters: Springer Singapore; 2018.
%
%

clc

%% Input parameters

wg = Fnom*2*pi;   % Grid angular frequency, rad/s
wsw = Fsw*2*pi; % Inverter switching angular frequency, rad/s
Mr = Vnom*sqrt(2)/Vdc;  % Modulation ratio

%% Base values calculation

Zb = Vnom^2/Pnom;    %Base impedance, ohm
Cb = 1/(wg*Zb); %Base capacitance, F

%% Components values calculation

%% Inverter side inductor L1
I1 = Pnom/Vnom; % Inverter rated RMS current

if SPWM==0
    L1_min = (Vdc*(1/Fsw))/(2*Rip*I1); % Minimum inductance of L1 ...
        for Bipolar SPWM
```

```
44 else
45     L1_min = (Vdc*(1/Fsw))/(8*Rip*I1); % Minimum inductance of L1 ...
           for Unipolar SPWM
46 end
47
48 LamvL1 = 0.05; % Ratio of inverter side inductor fundamental voltage ...
       and filter capacitor voltage
49 L1_max = (LamvL1*Vnom)/(wg*I1); % Maximum inductance of L1
50
51 L1 = input(['Select value of L1 between ' num2str(L1_min) 'H and ' ...
       num2str(L1_max) 'H:'])
52
53 %% Capacitor
54 Cf_max = X*Cb;   % Maximum capacitor value, F
55
56 Cf = input(['Select value of C < ' num2str(Cf_max) 'F:'])
57
58 %% Grid side inductor
59 I2 = sqrt(I1^2-(wg*Cf*Vnom)^2);
60
61 [Amph,Freqh]=L2_Params(Vnom,Vdc,Mr,Fnom,Fsw,SPWM);  % Determine ...
       dominant harmonic amplitude and frequency
62
63 % Determine maximum harmonics proportion factor Lamh based on ...
       IEEE1547-2018
64 % requirements
65
66 hord = Freqh/Fnom;  % Dominant harmonic order
67
68 if hord<11
69     Lamh_max = 0.04;
70 elseif hord<17
71     Lamh_max = 0.02;
72 elseif hord<23
73     Lamh_max = 0.015;
```

```
74 elseif hord<35
75     Lamh_max = 0.006;
76 else
77     Lamh_max = 0.003;
78 end
79
80 Lamh = input(['Select current harmonic proportion factor < ' ...
       num2str(Lamh_max) ':'])
81
82 L2_min = ...
       1/(L1*Cf*(2*pi*Freqh)^2-1)*(L1+(Amph*Vdc)/((2*pi*Freqh)*Lamh*I2)); ...
         %Grid side inductor value, H
83
84 L2 = input(['Select value of L2 > ' num2str(L2_min) 'H:'])
85
86 %% Validate the LCL filter design by simulation
87
88 Tend = 5*(1/Fnom);  % Simulation end time
89 options = simset('SrcWorkspace','current');
90 sim('ValidationLCL.slx',[],options);
91
92 % Inverter Output Voltage FFT
93 [FFTVinv] = power_fftscope(LCLVinv);
94 FFTVinv.cycles = 3;
95 FFTVinv.fundamental = Fnom;
96 FFTVinv.maxFrequency = 5*Fsw;
97 [FFTVinvResults] = power_fftscope(FFTVinv);
98 power_fftscope(FFTVinv);  % Perform Vinv FFT
99 title(['Inverter Output Voltage FFT. Fundamental = ' ...
100     num2str(FFTVinvResults.magFundamental) 'V at ' ...
101     num2str(FFTVinvResults.fundamental) 'Hz. THD = ' ...
102     num2str(FFTVinvResults.THD)])
103
104 % L1 current FFT
105 [FFTL1] = power_fftscope(LCLI1);
```

```
106 FFTL1.cycles = 3;
107 FFTL1.fundamental = Fnom;
108 FFTL1.maxFrequency = 5*Fsw;
109 [FFTL1Results] = power_fftscope(FFTL1);
110 power_fftscope(FFTL1);  % Perform L1 current FFT
111 title(['Inverter-side Inductor Current FFT. Fundamental = ' ...
112     num2str(FFTL1Results.magFundamental) 'A at ' ...
113     num2str(FFTL1Results.fundamental) 'Hz. THD = ' ...
114     num2str(FFTL1Results.THD)])
115
116 % L2 current FFT
117 [FFTL2] = power_fftscope(LCLI2);
118 FFTL2.cycles = 3;
119 FFTL2.fundamental = Fnom;
120 FFTL2.maxFrequency = 5*Fsw;
121 [FFTL2Results] = power_fftscope(FFTL2);
122 power_fftscope(FFTL2);  % Perform L1 current FFT
123 title(['Inverter Output Current FFT. Fundamental = ' ...
124     num2str(FFTL2Results.magFundamental) 'A at ' ...
125     num2str(FFTL2Results.fundamental) 'Hz. THD = ' ...
126     num2str(FFTL2Results.THD)])
127
128 %% Evaluate if the resonant frequency respects the criteria
129 %  10*Fg < Fres < 0.5*Fsw
130
131 wres = sqrt((L1+L2)/(L1*L2*Cf));    %Resonance angular frequency, rad/s
132 Fres = wres/(2*pi) %Resonance frequency, Hz
133
134 if Fres>10*Fnom && Fres<0.5*Fsw
135     Fcrit='Yes';
136 else
137     Fcrit='No';
138 end
139
```

```
fprintf('Does the filter resonant frequency respect the 10*Fg < Fres ...
    < 0.5*Fsw criteria?: %s \n', Fcrit)

%% Evaluate if the total inductance is less than 10%

% Total inductance in p.u.
ZLtot = (L1+L2)*wg/Zb

if ZLtot<0.1
    Lcrit='Yes';
else
    Lcrit='No';
end

fprintf('Is the total filter inductance less than 0.1 pu?: %s \n', ...
    Lcrit)

%% Plot the filter frequency response

% Filter transfer function
s = tf('s');
T_LCL = 1/(L1*Cf*L2*s^3+(L1+L2)*s);

% Bode plot options
opts = bodeoptions;
opts.Grid = 'on';
opts.FreqUnits = 'Hz';
opts.XLim = [10,10e4];

figure()
bode(T_LCL,opts)
hold on
title('LCL filter frequency response')

end
```

The LCL_design function calls another function, L2_params.m, which was developed to automatically simulate the model presented in Figure I-1, perform a FFT on the recorded voltage waveform and return the dominant harmonic amplitude and frequency for the design of the grid-side inductor. The function is presented below.

```
function [Amph,Freqh] = L2_Params(Vnom,Vdc,Mr,Fnom,Fsw,SPWM)
%%
%   This function helps designing the grid-side inductor of the LCL ...
    filter
%   by determining the dominant voltage harmonic amplitude and frequency
%
%   Input parameters:
%
%   Vnom = Inverter output RMS voltage, V
%   Vdc = DC link voltage, V
%   Mr = Modulation ratio
%   Fnom = Grid nominal frequency, Hz
%   Fsw = Inverter switching frequency, Hz
%   SPWM = SPWM type: 0 = Bipolar, 1 = Unipolar
%

options = simset('SrcWorkspace','current');
sim('InverterFFT.slx',[],options);

% Set the FFT parameters
[FFTDATA] = power_fftscope(VinvSim);
FFTDATA.cycles = 3;
FFTDATA.fundamental = Fnom;
FFTDATA.maxFrequency = 5*Fsw;
FFT = power_fftscope(FFTDATA);  % Perform FFT

% Find dominant harmonic amplitude and frequency
idx=find(FFT.freq==Fsw);     % Find index of Fsw in FFT results
```

```
28 HarmArr = FFT.mag([idx:size(FFT.mag)]); % Resize array of harmonic ...
      magnitudes
29 [Amphmax,idxhmax] = sort(HarmArr/(Vdc),'descend');   % Sort ...
      harmonics from largest magnitude
30 idxh = min(idxhmax(1:2)) ;   %Find index of smallest dominant harmonic
31 Amph = HarmArr(idxh)/(Vdc);    % Find smallest dominant harmonic ...
      amplitude |Vinv(jwh)|/Vdc
32 Freqh = FFT.freq(idx+idxh-1);   % Find smallest dominant harmonic ...
      frequency
33
34 end
```

APPENDIX II

OUTPUT FILTER INDUCTORS TECHNICAL SPECIFICATIONS

This appendix presents the technical specifications of commercially available inductors as designed in 2.

1. Inverter-side inductor

	INDUCTOR DESIGN 1	
PARTNUMBER	**OD-400090-2**	
Material	OD	
Availability	N	
DateCreated	Jun 13, 2022 12:07 PM	
N	66	
AWG	8	
Strands	1	
Stack	1	
I peak-peak (A)	5.657	
Duty Cycle	–	
L_0 (uH)	762.63	
L_{dc} (uH)	342.50	
% (L_{dc} / L_0)	45	✔
Ipp(A) vs Phase	–	
L(uH) vs Phase	–	
Bpk (G), fswitch	417	
B (G) at I_{max}	10095	✔
Core Loss (W)	7.558	
R_{dc} (Ω)	0.01585	

R_{ac} Factor	2.753	
Cu Loss (W)	10.08	
Total Loss (W)	17.64	
ΔT(C)	32.9	✔
Thermal Aging Check	✔	
Lifetime (hrs)	>1000000	
Core Dim A (in)	4	
Core Dim C Stack (in)	0.65	
Ae (cm^2)	3.52	
Le (cm)	24.271	
Ve (cm^3)	85.4	
Wound Length (mm)	109.58	
Wound Width (mm)	109.58	
Wound Height (mm)	26.25	
Mean Length Turn (cm)	9.91	
Surface Area (cm^2)	265.97	
Full or Single Layer	Full	

ID Use Ratio	0.17	✔
% Window Fill	24	✔
Dconductor(mm)	3.26	
Dwirehvyins(mm)	3.35	
Dwirebundle (in)	0.132	
Part Grams	632	
Total Grams	1120	
Core $	13.00	
(Core+Conductor)$	22.25	
(Core+Conductor+Loss)$	37.7	

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Part Number:	OD-400090-2

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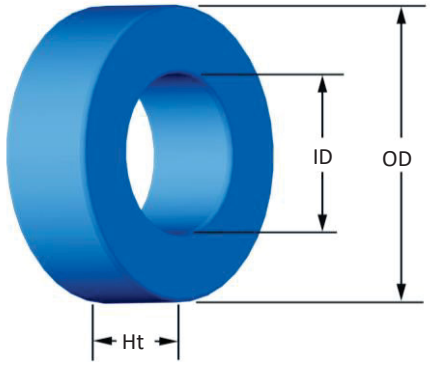
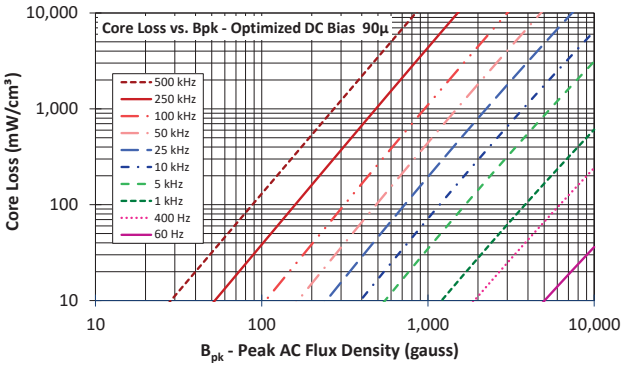
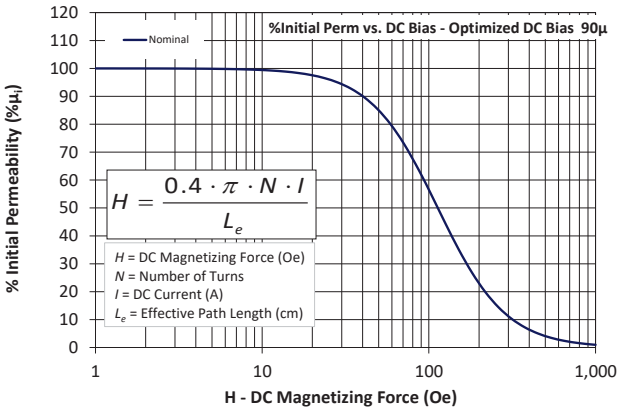
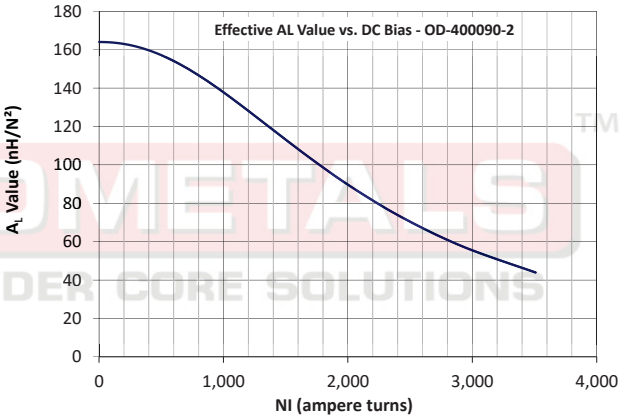


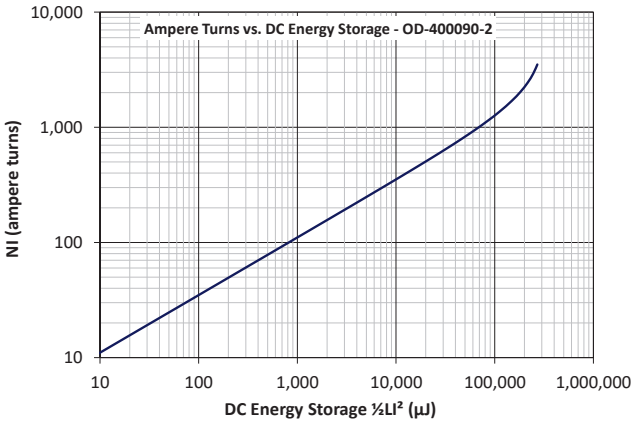
(If coated, Max./Min. includes coating)

OD	(nom. - bare core)	101.60 mm	4.000 in
	(max.)	102.87 mm	4.050 in
ID	(nom. - bare core)	57.15 mm	2.250 in
	(min.)	55.75 mm	2.195 in
HT	(nom. - bare core)	16.51 mm	0.650 in
	(max.)	17.78 mm	0.700 in
Mass	(approximate)	630 grams	
Magnetic Dimensions	A_e - Eff. Mag. Cross Section	3.52 cm²	
	L_e - Eff. Mag. Path Length	24.271 cm	
	V_e - Eff. Core Volume	85.5 cm³	
	WA - Min. Eff. Window Area	24.4 cm²	
	sa - Surface Area	303 cm²	
	mlt - mean length per turn	11.1 cm	
Inductance	μ_i(reference)	90	
	A_L value (nominal)	164 nH/N²	
	Test Winding	N=140, #18 AWG	
	Frequency	10 kHz	
	Voltage on Agilent 4284A	2.2 V	
	AL tolerance	±8%	
Core Loss	Core Loss(mW/cm³)= $\frac{f}{\frac{a}{Bpk^3}+\frac{b}{Bpk^{2.3}}+\frac{c}{Bpk^{1.65}}}+d\cdot Bpk^2\cdot f^2$		
	where B_{pk} expressed in gauss, f expressed in hertz, and:		
	a=1.000E+06, b=7.629E+08, c=4.688E+06, d=4.273E-14		
	B_{pk}	1000 G	
	frequency	50 kHz	
	Core Loss (nominal)	443 mW/cm³	
	Core Loss (maximum)	510 mW/cm³	
DC Saturation	$\%\mu_i \frac{1}{a+b\cdot H^c}+d$		
	where H expressed in oersteds, and:		
	a=1.000E-02, b=4.343E-07, c=2.124, d=0.000		
	H_{DC}	50 Oe	
	Percent Initial Perm(nom.)	85.0%	
	Percent Initial Perm(min.)	79.4%	
Coating/Pkg	Coating Type:	Blue Epoxy	
	Voltage Breakdown (min.)	1000 Vrms	
	Limit	0.1 mA, 5 s	
	Package Quantity	16 Pcs/Box	









Winding Table	**Wire Size**	AWG	8	10	12	14	16	18	20	22	24	26	28
		mm	3.150	2.500	2.000	1.600	1.250	1.000	0.800	0.630	0.500	0.400	0.315
	Single Layer	Turns	44	56	70	88	110	138	172	215	268	335	417
		Rdc(Ω)	10.0 m	20.2 m	40.2 m	80.5 m	160.0 m	319.2 m	632.7 m	1.3	2.5	5.0	9.8
	Full Winding	Turns	128	198	306	474	733	1,135	1,756	2,719	4,208	6,512	10,079
		Rdc(Ω)	29.1 m	71.6 m	175.9 m	433.4 m	1.1	2.6	6.5	15.9	39.1	96.4	237.2

2. Grid-side inductor

	INDUCTOR DESIGN 1	
PARTNUMBER	**OD-184060-2**	
Material	OD	
Availability	N	
DateCreated	Jun 13, 2022 12:17 PM	
N	20	
AWG	12	
Strands	1	
Stack	1	
I peak-peak (A)	5.657	
Duty Cycle	–	
L_0 (uH)	57.83	
L_{dc} (uH)	50.88	
% (L_{dc} / L_0)	88	
Ipp(A) vs Phase	–	
L(uH) vs Phase	–	
Bpk (G), fswitch	362	
B (G) at I_{max}	5676	

Core Loss (W)	1.131
R_{dc} (Ω)	0.008824
R_{ac} Factor	1.854
Cu Loss (W)	5.576
Total Loss (W)	6.707
ΔT(C)	38.2 ✔
Thermal Aging Check	✔
Lifetime (hrs)	>1000000
Core Dim A (in)	1.84
Core Dim C Stack (in)	0.71
Ae (cm^2)	1.99
Le (cm)	10.743
Ve (cm^3)	21.4
Wound Length (mm)	51.97
Wound Width (mm)	51.97
Wound Height (mm)	23.26
Mean Length Turn (cm)	7.08
Surface Area (cm^2)	84.63
Full or Single Layer	Single

ID Use Ratio	0.19	✔
% Window Fill	17	✔
Dconductor(mm)	2.05	
Dwirehvyins(mm)	2.17	
Dwirebundle (in)	0.085	
Part Grams	151	
Total Grams	193	
Core $	3.31	
(Core+Conductor)$	4.12	
(Core+Conductor+Loss)$	9.99	

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Part Number:	OD-184060-2

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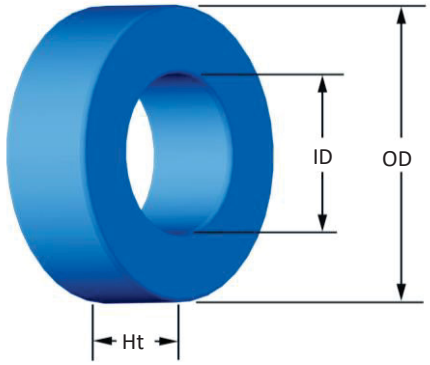
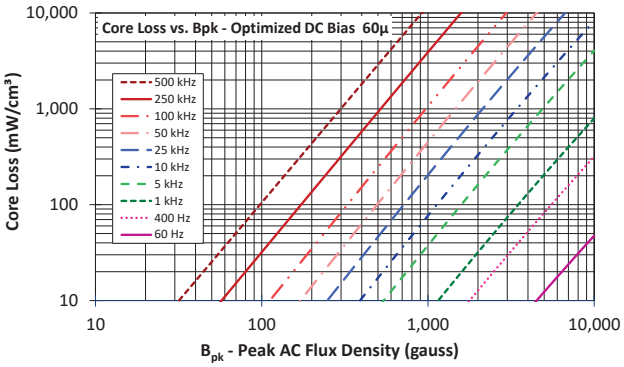
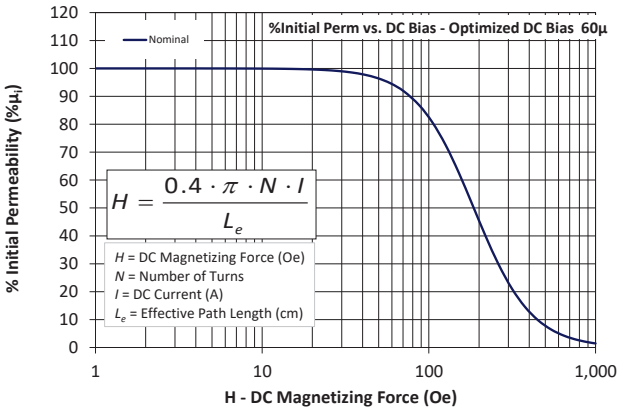
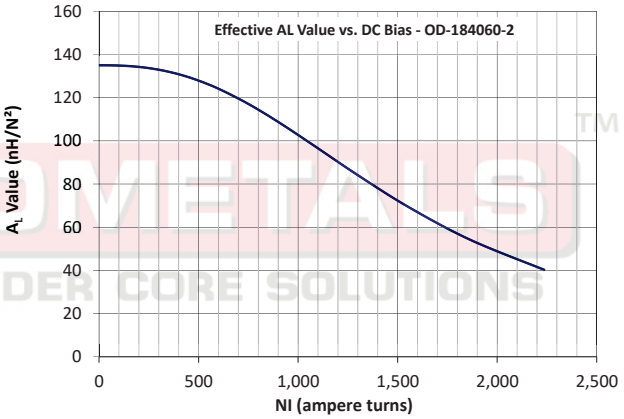


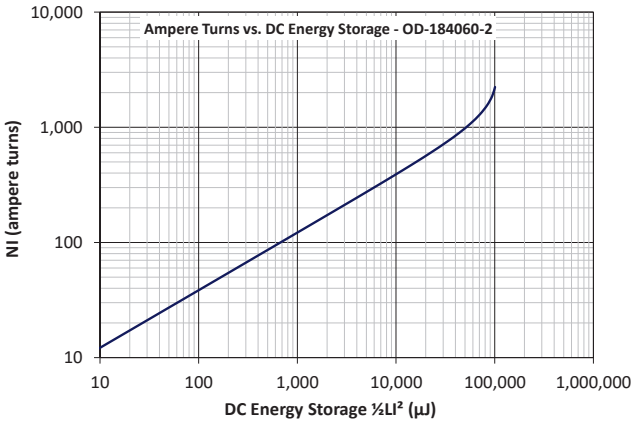
(If coated, Max./Min. includes coating)

OD	(nom. - bare core)	46.74 mm	1.840 in
	(max.)	47.63 mm	1.875 in
ID	(nom. - bare core)	24.13 mm	0.950 in
	(min.)	23.32 mm	0.918 in
HT	(nom. - bare core)	18.03 mm	0.710 in
	(max.)	18.92 mm	0.745 in
Mass	(approximate)	150 grams	
Magnetic Dimensions	A_e - Eff. Mag. Cross Section	1.99 cm²	
	L_e - Eff. Mag. Path Length	10.743 cm	
	V_e - Eff. Core Volume	21.4 cm³	
	WA - Min. Eff. Window Area	4.27 cm²	
	sa - Surface Area	81.7 cm²	
	mlt - mean length per turn	7.38 cm	
Inductance	μ_i(reference)	60	
	A_L value (nominal)	135 nH/N²	
	Test Winding	N=70, #20 AWG	
	Frequency	10 kHz	
	Voltage on Agilent 4284A	0.62 V	
	AL tolerance	±8%	
Core Loss	Core Loss(mW/cm³)= $\frac{f}{\frac{a}{Bpk^3}+\frac{b}{Bpk^{2.3}}+\frac{c}{Bpk^{1.65}}}+d\cdot Bpk^2\cdot f^2$		
	where B_{pk} expressed in gauss, f expressed in hertz, and:		
	a=1.000E+06, b=8.154E+08, c=2.976E+06, d=3.292E-14		
	B_{pk}	1000 G	
	frequency	50 kHz	
	Core Loss (nominal)	450 mW/cm³	
	Core Loss (maximum)	517 mW/cm³	
DC Saturation	$\%\mu_i \frac{1}{a+b\cdot H^c}+d$		
	where H expressed in oersteds, and:		
	a=1.000E-02, b=2.111E-08, c=2.501, d=0.000		
	H_{DC}	100 Oe	
	Percent Initial Perm(nom.)	82.5%	
	Percent Initial Perm(min.)	74.9%	
Coating/Pkg	Coating Type:	Blue Epoxy	
	Voltage Breakdown (min.)	1000 Vrms	
	Limit	0.1 mA, 5 s	
	Package Quantity	100 Pcs/Box	









Winding Table													
Wire Size	AWG	8	10	12	14	16	18	20	22	24	26	28
	mm	3.150	2.500	2.000	1.600	1.250	1.000	0.800	0.630	0.500	0.400	0.315
Single Layer	Turns	17	22	28	35	45	56	70	88	111	138	173
	Rdc(Ω)	2.6 m	5.3 m	10.7 m	21.4 m	43.7 m	86.5 m	171.9 m	343.7 m	689.5 m	1.4	2.7
Full Winding	Turns	22	35	54	83	128	199	307	476	736	1,139	1,764
	Rdc(Ω)	3.3 m	8.4 m	20.7 m	50.7 m	124.3 m	307.3 m	753.9 m	1.9	4.6	11.3	27.7

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APPENDIX III

RELATIONSHIP BETWEEN THE STEADY-STATE ERROR OF THE CURRENT AND THE MAGNITUDE OF THE LOOP GAIN

This appendix demonstrates that, as mentioned in Section 3.3.1.1, the steady-state error of the current at the fundamental frequency is effectively related to the magnitude of the loop gain at the fundamental frequency T_{f_0}.

It was shown that the output current can be expressed using the loop gain transfer function in equation (3.15) repeated here for convenience:

$$i_2(s) = \frac{T(s)}{1+T(s)} \cdot i_2^*(s) - \frac{G_2(s)}{1+T(s)} \cdot v_s(s) \tag{A III-1}$$

It is composed of two other distinct transfer functions, namely the tracking (A III-2) and disturbance (A III-3) transfer functions:

$$i_{2T}(s) = \frac{T(s)}{1+T(s)} \cdot i_2^*(s) \tag{A III-2}$$

$$i_{2D}(s) = -\frac{G_2(s)}{1+T(s)} \cdot v_s(s) \tag{A III-3}$$

Considering that the magnitude of the loop gain at the fundamental frequency is large enough to obtain a good reference tracking, the tracking transfer function of equation (A III-2) can be considered as a scalar in phase with i_2^*. It was also shown that at the fundamental frequency, the filter capacitor branch may be considered as an open circuit due to its high impedance, meaning that the magnitude of the loop gain can be expressed as (A III-4) and the $G_2(s)$ transfer function as (A III-5).

$$T(s) \approx \frac{G_i(s) \cdot K_{PWM}}{(L_1 + L_2) \cdot s} \tag{A III-4}$$

$$G_2(s) = \frac{1}{(L_1 + L_2) \cdot s} \tag{A III-5}$$

Using equations (A III-4) and (A III-5), the magnitude of the tracking transfer function of (A III-2) at the fundamental frequency f_0, I_{2D}, can be written as (A III-6).

$$I_{2D} \approx \frac{V_s}{2\pi f_o \cdot (L_1 + L_2) \cdot |T(2\pi f_o)|} \tag{A III-6}$$

The magnitude of the loop gain at the fundamental frequency, T_{f_0}, can then be expressed as (A III-7).

$$T_{f_0} = 20 \log |T(2\pi f_o)| = 20 \log \frac{V_s}{2\pi f_o \cdot (L_1 + L_2) \cdot I_{2D}} \tag{A III-7}$$

This proves that the steady-state error of the current at the fundamental frequency is effectively related to the magnitude of the loop gain.

APPENDIX IV

CURRENT CONTROLLER DESIGN SCRIPTS AND MODELS

This appendix details the scripts and models that were developed in order to automate the design procedure of the inverter current controller as presented in Chapter 3.

A Simulink model, shown in Figure IV-1, was developed to test the current controller performance. It simulates the switching model of a grid-connected single-phase full-bridge inverter. The grid is modeled as a Thevenin equivalent circuit (voltage source behind an impedance), the DC-link is modeled using a constant DC voltage source and the inverter bridge uses simplified models of insulated gate bipolar transistors (IGBT) with antiparallel diodes. The output current is measured and fed back into the current controller subsystem, highlighted in green, which is shown in Figure IV-2. It is compared to the current reference and the resulting error is input to the PR current controller which outputs the unipolar SPWM duty cycle reference. The measured filter capacitor current is fed back through the H_{i1} gain and subtracted from this reference to implement active damping of the filter resonance. The orange subsystem contains the logic to generate the test signals, namely the grid voltage and current reference.

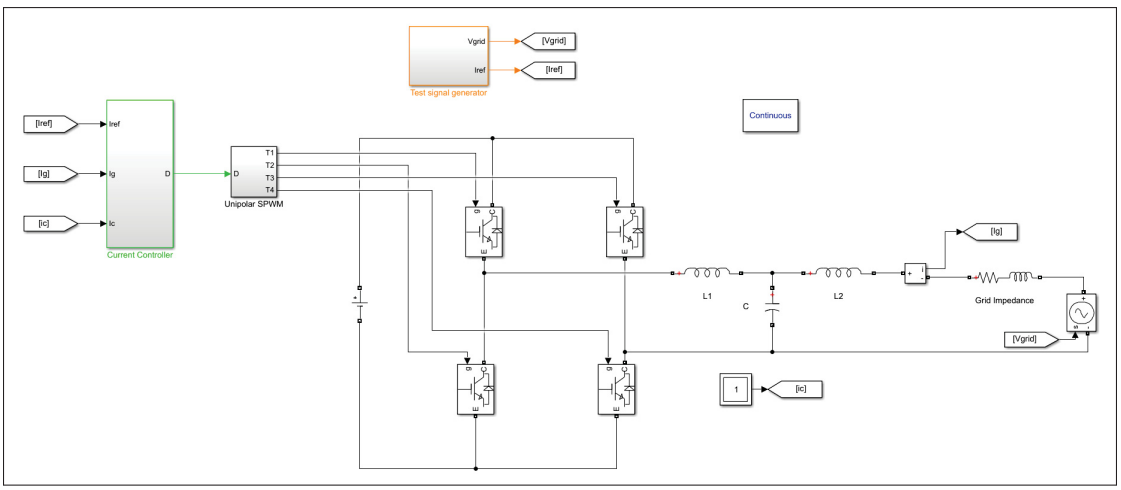

Figure-A IV-1 Simulink model for the validation of the current controller performance

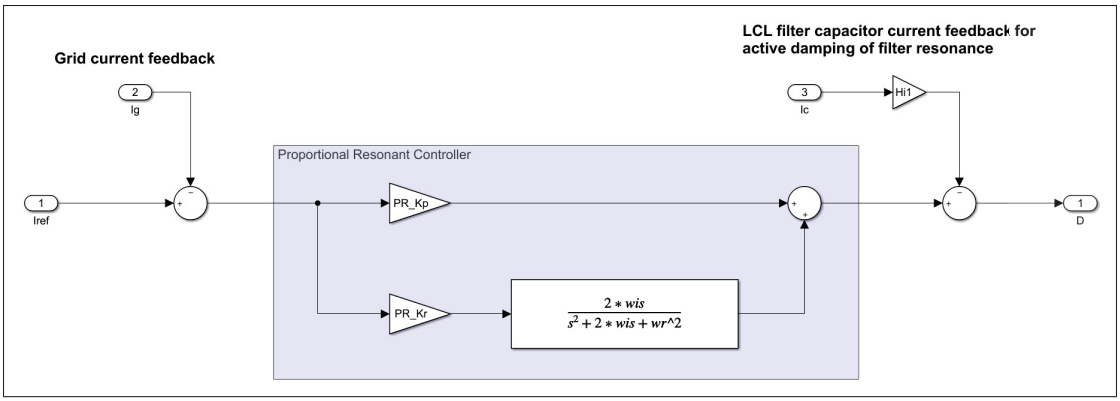

Figure-A IV-2 Simulink model of the proportional-resonant current controller

The following script was created in order to automate the design of the PR current controller presented in Chapter 3. Based on the inverter parameters presented in Table 1.1 and the desired performance requirements, the script calculates the range of acceptable values for f_c and H_i1 and plots the resulting region as shown in 3.11.

```
%% ********************************************************************
%                           Script Description
%  ********************************************************************
%  This script allows to automatically design the PR current controller
%  parameters for a single-phase inverter

clear
close all
clc

run('InverterParamsNew')

% Design requirements
Tfo = 75; % Desired minimum magnitude of loop gain at fundamental ...
    frequency
PM = 45; % Desired minimum phase margin in degrees
GM = 6; % Desired minimum gain margin in dB
```

```
17
18 % Initialize test range and results arrays
19 fc_range = 1:fr;
20 Hi1_GM = zeros(1,length(fc_range));
21 Hi1_Tfo_PM = zeros(1,length(fc_range));
22
23 for fc = 1:length(fc_range)
24     Hi1_GM(fc) = 10^(GM/20)*(2*pi*fc*L1)/Kpwm;
25     Hi1_Tfo_PM(fc) = ...
           (((2*pi*L1*(fr^2-fc^2)))/(Kpwm*fc))*((pi*fc^2-(10^(Tfo/20)...
26          *fo-fc)*wi*tand(PM))/((10^(Tfo/20)*fo-fc)*wi+pi*fc^2*tand(PM)));
27 end
28
29 Hi1_PWM = (4*fsw*L1)/(Kpwm);
30
31 %% Plot constrained region to identify satisfactory Hi1 and fc values
32
33 figure()
34 plot(fc_range,Hi1_GM)
35 hold on
36 plot(fc_range,ones(size(fc_range))*Hi1_PWM)
37 plot(fc_range,Hi1_Tfo_PM)
38 xlim([0 fr])
39 ylim([0 max(max(Hi1_Tfo_PM),Hi1_PWM)*1.1])
40 legend('Hi1 GM','Hi1 PWM','Hi1 T_f_o PM')
41 xlabel('fc (Hz)')
42 ylabel('Hi1')
43 grid on
44 title({'Region of acceptable values for Hi1 and fc', 'based on ...
       controller performance constraints'})
45
46 %% Control system parameters selection
47
```

```
48 fc_sel = input(['Select desired loop gain crossover frequency fc ...
       based on constraints and less than or equal to ' ...
       num2str(2*fsw/10) ':'])
49
50 Kp = (2*pi*fc_sel*(L1+L2))/(Hi2*Kpwm); % PR controller proportional gain
51
52 Hi1_min = 10^(GM/20)*(2*pi*fc_sel*L1)/Kpwm; % Minimum value of Hi1
53 Hi1_max = min([Hi1_PWM ...
       (((2*pi*L1*(fr^2-fc_sel^2)))/(Kpwm*fc_sel))*((pi*fc_sel^2-...
54      (10^(Tfo/20)*fo-fc_sel)*wi*tand(PM))/((10^(Tfo/20)*fo-fc_sel)*wi...
55          +pi*fc_sel^2*tand(PM)))]); % Maximum value of Hi1
56
57 Hi1_sel = input(['Select capacitor current feedback gain Hi1 between ...
       ' num2str(Hi1_min) ' and ' num2str(Hi1_max) ' :'])
58
59 Kr_Tfo = (10^(Tfo/20)*fo-fc_sel)*((2*pi*(L1+L2))/(Hi2*Kpwm));
60      % Minimum value of Kr constrained by Tfo
61 Kr_PM = ...
       ((pi*fc_sel*Kp)/wi)*((2*pi*L1*(fr^2-fc_sel^2)-Hi1_sel*Kpwm*fc_sel...
62      *tand(PM))/(Hi1_sel*Kpwm*fc_sel+2*pi*L1*(fr^2-fc_sel^2)*tand(PM)));
63      % Maximum value of Kr constrained by PM
64
65 Kr = input(['Select value of resonant gain Kr between ' ...
       num2str(Kr_Tfo) ' and ' num2str(Kr_PM) ' :'])
66
67 %% Loop gain analysis
68
69 s = tf('s');
70 Zc = 1/(s*C);
71 ZL1 = s*L1;
72 ZL2 = s*L2;
73 % Zg = s*Lg+rg;
74
75 G1 = (Kpwm*Zc)/(ZL1+Zc+Hi1_sel*Kpwm);
76 G2 = (ZL1+Zc+Kpwm*Hi1_sel)/(ZL1*ZL2+Zc*(ZL1+ZL2)+Kpwm*Hi1_sel*ZL2);
```

```
77 Gi_Res = Kp+(Kr*2*wi*s)/(s^2+2*wi*s+wo^2); % PR controller transfer ...
       function
78 T_uncomp = (Hi2*Kpwm*1)/(L1*L2*C*s^3+L2*C*1e-6*Kpwm*s^2+(L1+L2)*s); ...
       % Uncompensated loog gain transfer function
79 T_comp = ...
       (Hi2*Kpwm*Gi_Res)/(L1*L2*C*s^3+L2*C*Hi1_sel*Kpwm*s^2+(L1+L2)*s); ...
       % Compensated loop gain transfer function
80
81
82 opts = bodeoptions;
83 opts.Title.String = 'Bode plots of uncompensated and compensated ...
       loop gain';
84 opts.Title.FontSize = 10;
85 opts.Title.FontWeight = 'Bold';
86 opts.Grid = 'on';
87 opts.FreqUnits = 'Hz';
88 opts.XLim = [10,10*fr];
89
90 figure()
91 bode(T_uncomp,opts)
92 hold on
93 margin(T_comp)
94 [TGm,TPm,TWcg,TWcp] = margin(T_comp);
95 fc_r = round(TWcp/(2*pi),0);
96 fr_r = round(fr,0);
97 fo = xline(60,'--r','Grid = 60Hz');
98 fc = xline(fc_r,'--m',"Crossover = "+fc_r+"Hz");
99 fres = xline(fr_r,'--b',"Resonance = "+fr_r+"Hz");
100 fo.LabelVerticalAlignment = 'middle';
101 fo.LabelHorizontalAlignment = 'left';
102 fc.LabelVerticalAlignment = 'middle';
103 fc.LabelHorizontalAlignment = 'left';
104 fres.LabelVerticalAlignment = 'middle';
105 fres.LabelHorizontalAlignment = 'right';
106 legend('Uncompensated Loop Gain','Compensated Loop Gain')
```

```
107 title({'Bode diagrams of uncompensated and compensated loop gain', ...
      "GM = "+20*log10(TGm)+"dB, PM = "+TPm+" at "+fc_r+"Hz"})
```

APPENDIX V

SCRIPT TO EVALUATE THE IMPACT OF VARIOUS PARAMETERS ON THE SYSTEM'S PHASE MARGIN

This appendix presents the script designed to evaluate the impact of the inverter output filter and grid equivalent impedances on the phase margin of the system loop gain frequency response, as presented in Section 3.4.3. The script varies the value of each impedance over a predefined range then plots the resulting frequency responses as well as a graph of the phase margin as a function of the impedance, as shown in Figure 3.16.

```
%% ****************************************************************
%                          Script Description
%  ****************************************************************
%  The purpose of this script is to graphically demonstrate how various
%  parameters impact the system's phase margin


clc
clear all
close all

run('InverterParamsNew')

s = tf('s');

% Filter and grid impedances
Zc = 1/(s*C);
ZL1 = s*L1;
ZL2 = s*L2;

% PR controller parameters
kp = 0.1481; %Proportional gain
kr = 377; %Resonant gain
```

```
Gi_Res = (kr*2*wi*s)/(s^2+2*wi*s+wo^2); % Resonant transfer function
Gi = kp + Gi_Res;           % P+Res TF

H1 = 0.3; %Capacitor current feedback gain

% Define test range
Lg_max = 8e-3; % Maximum evaluated grid inductance
Lg_range = 10e-6:Lg_max/100:Lg_max; % Range of grid inductances
L1_range = 525e-6:0.0015279/100:0.0015279; % Range of inverter-side ...
    filter inductor
L2_range = 2.2e-5:1e-3/100:1e-3; % Range of grid-side filter inductor
C_range = 5e-6:1.15e-5/100:1.15e-5; % Range of filter capacitor

%% Impact of grid inductance

% Initialize results array
denom_G2 = tf(zeros(1,length(Lg_range)));
G2 = tf(zeros(1,length(Lg_range)));
ig1 = tf(zeros(1,length(Lg_range)));
ig2 = tf(zeros(1,length(Lg_range)));
T = tf(zeros(1,length(Lg_range)));
GM = zeros(1,length(Lg_range));
PM = zeros(1,length(Lg_range));

% Define constant transfer functions for this test
num_G1 = (Kpwm*Zc);
denom_G1 = (ZL1+Zc+H1*Kpwm);
G1 = num_G1/denom_G1;
num_G2 = (ZL1+Zc+H1*Kpwm);
iter = 0;

% Variation of the grid inductance
for n = 1:length(Lg_range)
    Zg(n) = s*Lg_range(n);
    % G2 TF
```

```
58      denom_G2(n) = (Zc*(ZL1+ZL2+Zg(n))+(ZL1+Kpwm*H1)*(ZL2+Zg(n)));
59      G2(n) = num_G2/denom_G2(n);
60      % Loop gain TF
61      T(n) = Gi*G1*G2(n)*Hi2;
62      T(n) = minreal(T(n));   % Pole-zero pair cancellation of Loop ...
            gain TF
63      % Tracking and disturbance TF
64      ig1(n) = (1/Hi2)*T(n)/(1+T(n)); % Tracking TF
65      ig2(n) = -G2(n)/(1+T(n));   % Disturbance TF
66      [GM(n),PM(n)] = margin(T(n));
67      iter = iter+1;
68      prog = 100*iter/length(Lg_range);
69      clc
70      disp('Progress [%] :')
71      disp(prog)
72  end
73
74  % Plot results
75  figure()
76  plot(Lg_range,PM)
77  grid on
78  xlabel('Grid inductance (H)')
79  ylabel('Phase margin')
80  title('Impact of grid inductance on loop gain phase margin')
81
82  % Bode plot options
83  opts = bodeoptions;
84  opts.Grid = 'on';
85  opts.FreqUnits = 'Hz';
86  opts.XLim = [10,10e4];
87
88  figure()
89  bode(T(1),opts)
90  hold on
91  grid on
```

```
92 bode(T(length(Lg_range)/2))
93 bode(T(length(Lg_range)))
94 legend('Lg=1e-5H','Lg=3.9e-3H','Lg=8e-3H')
95 title('Impact of grid inductance on loop gain frequency response')
96
97 %% Impact of inverter-side filter inductor
98
99 % Initialize results array
100 num_G1 = tf(zeros(1,length(L1_range)));
101 denom_G1 = tf(zeros(1,length(L1_range)));
102 num_G2 = tf(zeros(1,length(L1_range)));
103 denom_G2 = tf(zeros(1,length(L1_range)));
104 G1 = tf(zeros(1,length(L1_range)));
105 G2 = tf(zeros(1,length(L1_range)));
106 ig1 = tf(zeros(1,length(L1_range)));
107 ig2 = tf(zeros(1,length(L1_range)));
108 T = tf(zeros(1,length(L1_range)));
109 GM = zeros(1,length(L1_range));
110 PM = zeros(1,length(L1_range));
111
112 % Define constant transfer functions for this test
113 Zg = s*1e-3;
114 num_G1 = (Kpwm*Zc);
115 iter = 0;
116
117 % Variation of the inverter-side filter inductor
118 for n = 1:length(L1_range)
119     ZL1(n) = s*L1_range(n);
120     % G1 TF
121     denom_G1(n) = (ZL1(n)+Zc+H1*Kpwm);
122     G1(n) = num_G1/denom_G1(n);
123     % G2 TF
124     num_G2(n) = (ZL1(n)+Zc+H1*Kpwm);
125     denom_G2(n) = (Zc*(ZL1(n)+ZL2+Zg)+(ZL1(n)+Kpwm*H1)*(ZL2+Zg));
126     G2(n) = num_G2(n)/denom_G2(n);
```

```
127     % Loop gain TF
128     T(n) = Gi*G1(n)*G2(n)*Hi2;
129     T(n) = minreal(T(n));   % Pole-zero pair cancellation of Loop ...
            gain TF
130     % Tracking and disturbance TF
131     ig1(n) = (1/Hi2)*T(n)/(1+T(n)); % Tracking TF
132     ig2(n) = -G2(n)/(1+T(n));   % Disturbance TF
133     [GM(n),PM(n)] = margin(T(n));
134     iter = iter+1;
135     prog = 100*iter/length(L1_range);
136     clc
137     disp('Progress [%] :')
138     disp(prog)
139 end
140
141 % Plot results
142 figure()
143 plot(L1_range,PM)
144 grid on
145 xlabel('Inverter-side filter inductance (H)')
146 ylabel('Phase margin')
147 title('Impact of inverter-side filter inductance on loop gain phase ...
        margin')
148
149 figure()
150 bode(T(1),opts)
151 hold on
152 grid on
153 bode(T(length(L1_range)/2))
154 bode(T(length(L1_range)))
155 legend('L1=525e-6H','L1=1e-3H','L1=1.5e-3H')
156 title('Impact of inverter-side filter inductance on loop gain ...
        frequency response')
157
158 %% Impact of grid-side filter inductor
```

```
159
160 % Initialize results array
161 num_G1 = tf(zeros(1,length(L2_range)));
162 denom_G1 = tf(zeros(1,length(L2_range)));
163 num_G2 = tf(zeros(1,length(L2_range)));
164 denom_G2 = tf(zeros(1,length(L2_range)));
165 G2 = tf(zeros(1,length(L2_range)));
166 ig1 = tf(zeros(1,length(L2_range)));
167 ig2 = tf(zeros(1,length(L2_range)));
168 T = tf(zeros(1,length(L2_range)));
169 GM = zeros(1,length(L2_range));
170 PM = zeros(1,length(L2_range));
171
172 % Define constant transfer functions for this test
173 Zg = s*1e-3;
174 ZL1 = s*680e-6;
175 num_G1 = (Kpwm*Zc);
176 denom_G1 = (ZL1+Zc+H1*Kpwm);
177 G1 = num_G1/denom_G1;
178 num_G2 = (ZL1+Zc+H1*Kpwm);
179 iter = 0;
180
181 % Variation of the grid-side filter inductor
182 for n = 1:length(L2_range)
183     ZL2(n) = s*L2_range(n);
184     % G2 TF
185     denom_G2(n) = (Zc*(ZL1+ZL2(n)+Zg)+(ZL1+Kpwm*H1)*(ZL2(n)+Zg));
186     G2(n) = num_G2/denom_G2(n);
187     % Loop gain TF
188     T(n) = Gi*G1*G2(n)*Hi2;
189     T(n) = minreal(T(n));   % Pole-zero pair cancellation of Loop ...
          gain TF
190     % Tracking and disturbance TF
191     ig1(n) = (1/Hi2)*T(n)/(1+T(n)); % Tracking TF
192     ig2(n) = -G2(n)/(1+T(n));   % Disturbance TF
```

```
193     [GM(n),PM(n)] = margin(T(n));
194     iter = iter+1;
195     prog = 100*iter/length(L2_range);
196     clc
197     disp('Progress [%] :')
198     disp(prog)
199 end
200
201 % Plot results
202 figure()
203 plot(L2_range,PM)
204 grid on
205 xlabel('Grid-side filter inductance (H)')
206 ylabel('Phase margin')
207 title('Impact of grid-side filter inductance on loop gain phase margin')
208
209 figure()
210 bode(T(1),opts)
211 hold on
212 grid on
213 bode(T(length(L2_range)/2))
214 bode(T(length(L2_range)))
215 legend('L2=22e-6H','L2=500e-6H','L2=1e-3H')
216 title('Impact of grid-side filter inductance on loop gain frequency ...
      response')
217
218 %% Impact of filter capacitor
219
220 % Initialize results array
221 num_G1 = tf(zeros(1,length(C_range)));
222 denom_G1 = tf(zeros(1,length(C_range)));
223 num_G2 = tf(zeros(1,length(C_range)));
224 denom_G2 = tf(zeros(1,length(C_range)));
225 G1 = tf(zeros(1,length(C_range)));
226 G2 = tf(zeros(1,length(C_range)));
```

```
ig1 = tf(zeros(1,length(C_range)));
ig2 = tf(zeros(1,length(C_range)));
T = tf(zeros(1,length(C_range)));
GM = zeros(1,length(C_range));
PM = zeros(1,length(C_range));

% Define constant transfer functions for this test
Zg = s*1e-3;
ZL1 = s*680e-6;
ZL2 = s*100e-6;
iter = 0;

% Variation of the filter capacitor
for n = 1:length(C_range)
    Zc(n) = s*C_range(n);
    % G1 TF
    num_G1(n) = (Kpwm*Zc(n));
    denom_G1(n) = (ZL1+Zc(n)+H1*Kpwm);
    G1(n) = num_G1(n)/denom_G1(n);
    % G2 TF
    num_G2(n) = (ZL1+Zc(n)+H1*Kpwm);
    denom_G2(n) = (Zc(n)*(ZL1+ZL2+Zg)+(ZL1+Kpwm*H1)*(ZL2+Zg));
    G2(n) = num_G2(n)/denom_G2(n);
    % Loop gain TF
    T(n) = Gi*G1(n)*G2(n)*Hi2;
    T(n) = minreal(T(n));   % Pole-zero pair cancellation of Loop ...
        gain TF
    % Tracking and disturbance TF
    ig1(n) = (1/Hi2)*T(n)/(1+T(n)); % Tracking TF
    ig2(n) = -G2(n)/(1+T(n));   % Disturbance TF
    [GM(n),PM(n)] = margin(T(n));
    iter = iter+1;
    prog = 100*iter/length(C_range);
    clc
    disp('Progress [%] :')
```

```
261     disp(prog)
262 end
263 
264 % Plot results
265 figure()
266 plot(C_range,PM)
267 grid on
268 xlabel('Filter capacitance (F)')
269 ylabel('Phase margin')
270 title('Impact of filter capacitance on loop gain phase margin')
271 
272 figure()
273 bode(T(1),opts)
274 hold on
275 grid on
276 bode(T(round(length(C_range)/2)))
277 bode(T(length(C_range)))
278 legend('C=5e-6H','C=8e-6H','C=11e-6H')
279 title('Impact of filter capacitance on loop gain frequency response')
```

APPENDIX VI

PLL TEST MODEL

This appendix presents the Simulink models of the PLL and its test environment that were developed and used to generate the results presented in Chapter 4. Figure VI-1 shows the topology of the single-phase PLL with adaptive notch filter. It is the same logic that is packaged under a mask in Figure VI-2 (blue outline), where a signal generator is connected to the PLL input. The signal generator contains the logic to simulate a sine wave with programmable step changes in frequency and phase angle.

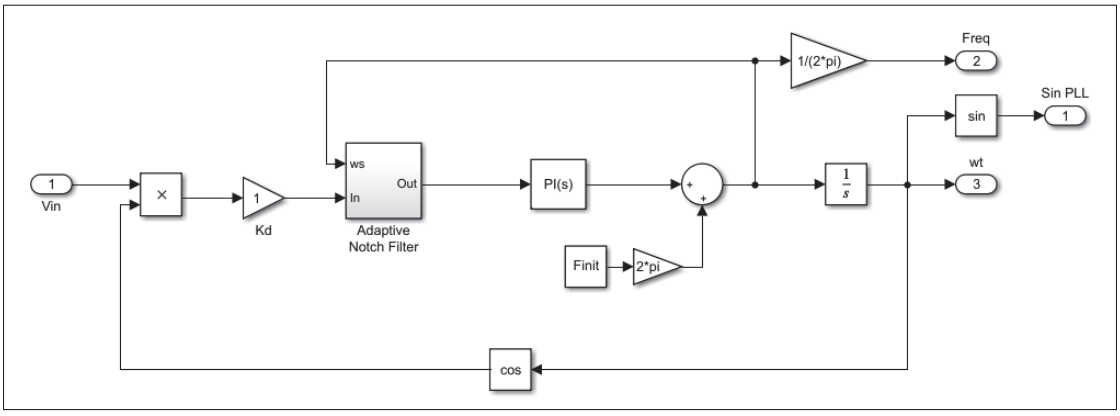

Figure-A VI-1 Simulink model of the PLL with adaptive notch filter

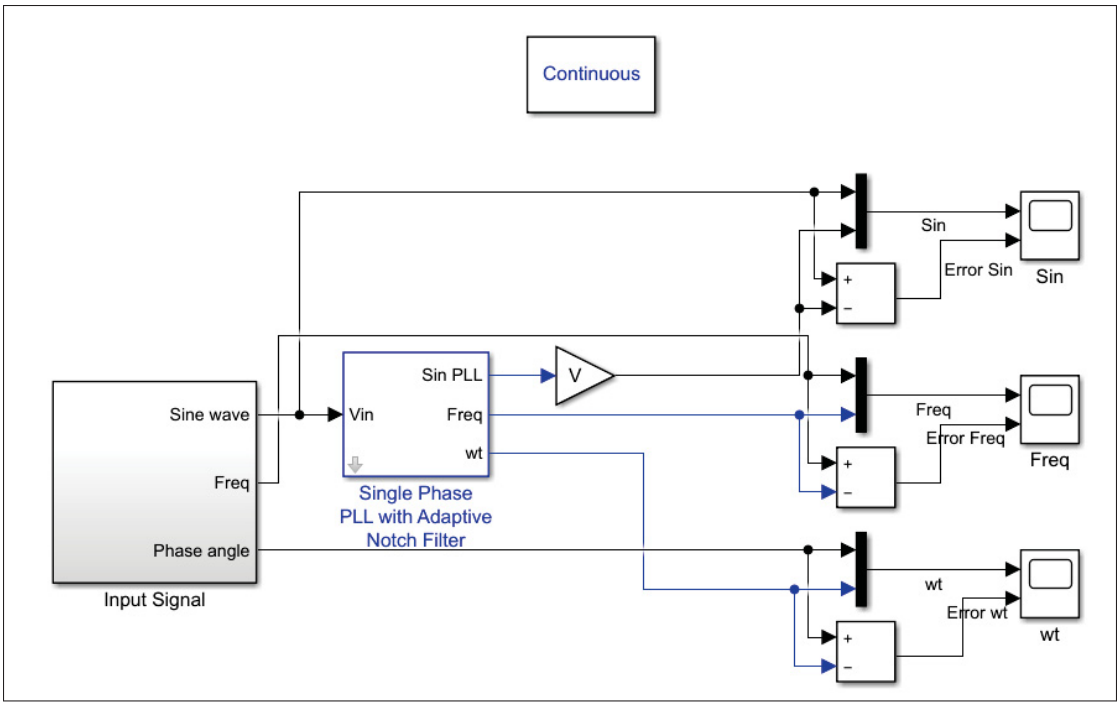

Figure-A VI-2 Simulink model for PLL testing

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