Design and Development of Advanced Model-based Robust Multi-Objective Controllers for Multilevel Converters

by

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Conception et développement de contrôleurs robustes multi-objectifs basés sur des modèles avancés pour les convertisseurs multiniveaux

Mohammad BABAIE

RÉSUMÉ

Considérant le rôle essentiel des convertisseurs multiniveaux (MLC) dans l'avenir des distributions des énergies renouvelables, des véhicules électriques, et de l'automatisation, cette thèse contribue au développement de contrôleurs multi-objectifs avancés et de topologies pour les MLC afin d'améliorer leur performance, leur stabilité et leur fiabilité dans les modes d'opération reliés au réseau et opération. En conséquence, dans le premier travail de recherche de cette thèse, un contrôleur à mode glissant optimisé (OSMC) est introduit pour traiter le problème d'équilibrage de la tension du convertisseur à sept niveaux de cellules en U emballées (PUC), reconnu comme une référence, sans impliquer un contrôleur de boucle de voltage externe. Une analyse de stabilité plus poussée est également réalisée pour garantir la stabilité et la robustesse de l'algorithme OSMC sans capteur dans des conditions dynamiques et des incertitudes paramétriques.

En ce qui concerne l'absence de méthode analytique efficace pour régler les facteurs de pondération dans les stratégies de contrôle prédictif de modèle (MPC), une technique basée sur l'intelligence artificielle (IA) entraînée hors ligne est développée dans le deuxième travail en utilisant l'algorithme de colonie d'abeilles artificielle (ABC) pour améliorer les performances de contrôle multi-objectif des contrôleurs prédictifs, qui sont dédiés aux MLC. Les résultats de l'application du MPC à apprentissage supervisé (SLMPC) à un convertisseur triphasé à point neutre bloqué (NPC) démontrent que l'IA est assez efficace pour traiter le réglage fastidieux des algorithmes basés sur le MPC. Malgré cela, l'apprentissage hors ligne ne peut pas garantir la performance de contrôle optimale du MPC dans des conditions dynamiques. C'est pourquoi une stratégie de réglage en ligne est développée dans les travaux de recherche suivants, basée sur réseau neuronal artificiel (RNA), afin d'adapter les facteurs de pondération d'un contrôleur MPC, qui est appliqué à un redresseur actif à sept niveaux de type PUC modifié (MPUC). Une nouvelle stratégie d'auto-apprentissage sans données est également établie à l'aide de l'algorithme d'optimisation par essaims de particules (PSO) pour former le régulateur basé sur le RNA. La stratégie d'entraînement proposée améliore considérablement la contribution des RNA aux problèmes de contrôle de l'électronique de puissance. Malgré l'étonnante performance multi-objectifs offerte par les contrôleurs prédictifs de modèle à ensemble de contrôle fini (FCSMPC), l'analyse de stabilité de Lyapunov n'est pas prise en charge en raison de la structure de contrôle discrète. Pour résoudre ce problème, une nouvelle fonction de Lyapunov prédictive est développée dans le même travail de recherche afin de garantir la stabilité des contrôleurs prédictifs multi-objectifs. L'objectif de stabilité proposé étant indépendant, il n'a aucun impact sur les performances de la commande optimale multi-objectifs des contrôleurs prédictifs.

Pour réduire la sensibilité de la méthode d'auto-apprentissage aux paramètres initiaux, une stratégie avancée d'auto-apprentissage rapide multicœur (FSTS) est construite par l'algorithme compétitif impérialiste (ICA) dans le travail de recherche suivant. En utilisant la nouvelle FSTS généralisée, un contrôleur multi-objectif prédictif intelligent (IPMOC) est développé pour les MLC, qui peut suivre plus de sept objectifs de contrôle simultanément. En outre, un nouvel objectif d'atténuation prédictive sélective des harmoniques (SPHM) est formulé dans le même travail pour les contrôleurs basés sur le MPC afin de supprimer directement tout ordre harmonique. Le SPHM proposé est généralisé et fonctionnel pour divers MLC.

Enfin, la topologie boost packed E-cell (BPEC), version modifiée de la conventionnelle packed E-cell (PEC), est introduite pour fournir une MLC compacte rentable (CMLC) pour les services auxiliaires de qualité de l'énergie. Malgré le PEC original, le BPEC proposé domine le point de couplage commun (PCC) en utilisant des voltages de liaison CC plus faibles. Par conséquent, le volume et le coût du convertisseur sont remarquablement réduits car des composants de moindre puissance sont nécessaires. Dans le cadre d'une étude de cas, un filtre de puissance actif compact (CAPF) est conçu en utilisant le BPEC proposé pour vérifier sa faisabilité. Les résultats des tests correspondants montrent que l'utilisation d'un contrôleur multi-objectif basé sur le MPC pour le BPEC conduit à un CAPF avantageux, qui peut répondre à toutes les attentes en matière de services auxiliaires.

Les performances des contrôleurs multi-objectifs développés, ainsi que la topologie BPEC, ont été largement évaluées à l'aide de divers scénarios de test appliqués à des bancs d'essai spécifiques conçus sur la base de dSPACE 1104, Microlabox 1202, OPAL-RT OP8662, Chroma 61086, et la carte de puissance des convertisseurs, y compris le PUC à sept niveaux, le MPUC à sept niveaux, le NPC triphasé, et le BPEC à 11 niveaux.

Mots-clés : RNA, réseau, stabilité de Lyapunov, commande prédictive de modèle (MPC), multi-objectifs, convertisseurs multiniveaux, optimisation, commande par mode glissant (OSMC), qualité de l'énergie, apprentissage

Design and development of advanced model-based robust multi-objective controllers for multilevel converters

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ABSTRACT

Considering the essential role of multilevel converters (MLC) in the future of distributed renewable energy resources, electric vehicles, and automation, this thesis contributes to developing advanced multi-objective controllers and topologies for MLCs to enhance their performance, stability, and reliability in grid-tied and stand-alone modes of operation. Accordingly, in the first research work of this dissertation, an optimized sliding mode controller (OSMC) is introduced to address the voltage balancing issue (recognized as a benchmark) of the seven-level packed U-cell (PUC) converter without involving an outer voltage loop controller. Further stability analysis is also accomplished to guarantee the stability and robustness of the sensorless OSMC algorithm under dynamic conditions and parametric uncertainties.

Concerning the lack of an effective analytical method to tune the weighing factors in model predictive control (MPC) strategies, an offline artificial intelligent-based (AI) training technique is developed in the second work using the artificial bee colony (ABC) algorithm to enhance the multi-objective control performance of predictive controllers, which are dedicated to MLCs. The implementation results of applying the supervised learning MPC (SLMPC) to a three-phase neutral point clamped (NPC) converter demonstrate that AI is quite effective in dealing with the tedious tuning of the MPC-based algorithms. Even so, offline training cannot guarantee the optimal control performance of the MPC under dynamic conditions. Regarding this fact, an online tuning strategy is developed in the following research work based on Artificial Neural Network (ANN) to adapt the weighing factors for an MPC controller, which is applied to a seven-level modified PUC (MPUC) active rectifier. A novel data-free self-training strategy is also established using the particle swarm optimization (PSO) algorithm to train the ANN-based regulator. The proposed training strategy significantly improves the contribution of ANNs in power electronics control problems. Despite the astonishing multi-objective performance offered by finite control set model predictive controllers (FCSMPC), Lyapunov stability analysis is not supported due to the discrete control structure. To address this issue, a novel predictive Lyapunov function is developed in the same research work to guarantee the stability of multi-objective predictive controllers. Since the proposed stability objective is independent, it causes zero impact on the optimal multi-objective control performance of the predictive controllers.

To reduce the sensitivity of the self-training method to the initial parameters, an advanced multi-core fast self-training strategy (FSTS) is constructed by the imperialist competitive algorithm (ICA) in the next research work. Using the new generalized FSTS, an intelligent predictive multi-objective controller (IPMOC) is developed for MLCs, which can track over

seven control objectives simultaneously. In addition, a novel selective predictive harmonic mitigation (SPHM) objective is formulated in the same work for MPC-based controllers to suppress any harmonic order directly. The proposed SPHM is generalized and functional for various MLCs.

Finally, boost back E-Cell (BPEC) topology as the modified version of the conventional packed E-Cell (PEC) is introduced to provide a cost-effective compact MLC (CMLC) for power quality ancillary services. Despite the original PEC, the proposed BPEC dominates the point of common coupling (PCC) using lower DC link voltages. As a result, the volume and cost of the converter remarkably reduce as lower power components are required. As a case study, a compact active power filter (CAPF) is designed using the proposed BPEC to verify its feasibility. The corresponding test results show that using an MPC-based multi-objective controller for the BPEC leads to an advantageous CAPF, which can meet all the expectations for the ancillary services.

The performance of the developed multi-objective controllers, as well as the BPEC topology, has been extensively evaluated using various test scenarios applied to specific testbeds designed based on dSPACE 1104, Microlabox 1202, OPAL-RT OP8662, Chroma 61086, and the power board of the converters, including the seven-level PUC, seven-level MPUC, three-phase NPC, and 11-level BPEC.

Keywords: ANN, grid, Lyapunov stability, model predictive control, multi-objective, multilevel converters, optimization, sliding mode control, power quality, training

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LIST OF ABBREVIATIONS

ABC	Artificial Bee Colony
AC	Alternative Current
AMPC	Adaptive Model Predictive Control
ANFIC	Adaptive Neuro-Fuzzy Inference Control
ANN	Artificial Neural Network
ANPC	Active Neutral Point Clamped
APF	Active Power Filter
APM	Autonomous Power Management
BCMLC	Boost Compact Multilevel Converter
BIBO	Bounded-Input Bounded-Output
BMC	Bidirectional Multilevel Converter
BPEC	Boost Packed E-Cell
BSC	Back-Stepping Control
CAPF	Compact Active Power Filter
CB	Control Based
CBPWM	Carrier-Based Pulse Width Modulation
CHB	Cascaded H-Bridge
CMLC	Compact Multilevel Converter
CMPC	Conventional Model Predictive Control
CMV	Common Mode Voltage
DC	Direct Current
DG	Distributed Generator
ESR	Equivalent Series Resistance

EV	Electric Vehicles
FACTS	Flexible AC Transmission System
FC	Flying Capacitor
FCSMPC	Finite Control Set Model Predictive Control
FFT	Fast Fourier Transform
FOSMC	First Order Sliding Mode Control
FSMPC	Finite Set Model Predictive Control
FSTS	Fast Self-Training Strategy
HBM	Hysteresis Band Modulation
HVDC	High-Voltage Direct Current
ICA	Imperialist Competitive Algorithm
IEA	International Energy Agency
IPMOC	Intelligent Predictive Multi-Objective Control
ISE	Integral of Squared Error
ITAE	Integral of Time-weighted Absolute Error
LQG	Linear Quadratic Gaussian
LQR	Linear Quadratic Regulator
LVQ	Learning Vector Quantization
MB	Modulator Based
MBADPC	Model-Based Adaptive Direct Power Control
MLC	Multilevel Converter
MLP	Multilayer Perceptron
MMC	Modular Multilevel Converter
MPC	Model Predictive Control

MPUC	Modified Packed U-Cell
MR	Multilevel Rectifiers
MRAC	Model Reference Adaptive Control
NPC	Neutral Point Clamped
OF	Objective Function
OSMC	Optimized Sliding Mode Control
PCC	Point of Common Coupling
PEC	Packed E-Cell
PF	Power Factor
PI	Proportional Integral
PID	Proportional Integral Derivative
PLL	Phase-Locked Loop
PR	Proportional Resonant
PSO	Particle Swarm Optimization
PUC	Packed U-Cell
PV	Photovoltaic
PWM	Pulse Width Modulator
RBF	Radial Basis Function
RBFC	Radial Basis Function Controller
RBFPM	Radial Basis Function Power Manager
RBFR	Radial Basis Function Regulator
RMS	Root Mean Square
SHE	Selective Harmonic Elimination
SLMPC	Supervised Learning Model Predictive Control

SMC	Sliding Mode Control
SOM	Self-Organizing Map
SOSMC	Second-Order Sliding Mode Control
SPHM	Selective-Predictive Harmonic Mitigation
SPWM	Sinusoidal Pulse Width Modulator
STATCOM	Static Synchronous Compensator
SVM	Support Vector Machines
SVPWM	Space Vector Pulse Width Modulator
THD	Total Harmonic Distortion
TMLC	Transformerless Multilevel Converter
TSK	Takagi-Sugeno-Kang
UPS	Uninterruptible Power Supply
VAR	Voltage Ampere Reactive
VBO	Visual-Based Optimization
VLMM	Voltage Level Multiplier Module
VLSM	Voltage Level Switching Mode
Z-PUC	Z Packed U-Cell

INTRODUCTION

The international energy agency (IEA) estimates that 90% of the world's electricity is expected to be generated through renewable energy resources by 2050 (*IEA 2021*, *Net Zero by 2050*, 2021). This domination is indeed a global-scale energy revolution with constructive impacts on climate change, geopolitical crises, energy generation/distribution prices, and labor markets. Regarding, statistics provided in Figure 0.1 shows that the world is ready to move forward and reach the IEA goal by the middle of the current century even though COVID-19 delayed the progress. The IEA reports in Figure 0.1 also reveal that wind and solar-distributed generators are the most developed and used renewable energy resources in countries with the largest economy. Photovoltaic (PV) panels and wind turbines are popular due to efficiency, modularity, accessibility, controllability, and safety reasons. According to the United Nations' energy reports in 2022, the cost of electricity from solar and wind resources respectively dropped by 85% and 48% between 2010 and 2020 (*IRENA (2022), World Energy Transitions Outlook 2022*, 2022). In addition to the renewable energy development, another wave of the industrial revolution has begun, which changes the faces of the automotive industry permanently. Electric Vehicles (EV) including cars, trains, airplanes, and ships, as the results of this transportation technology revolution, cause minimum sound pollution and zero CO_2 emission. As a part of the net zero program planned by IEA, EVs should be accounted for 60% of new car sales by 2030 (*IEA (2022), Electric Vehicles*, 2022). Figure 0.2 provided by IEA also indicates the exponential growth of registered EVs across the globe between 2016 and 2021.

Power electronic systems contribute to converting, controlling, stabilizing, and managing electricity in renewable energy resources as well as EVs. In addition to renewable generators and EVs, power electronic systems are almost involved in any other electrical or electro-mechanical devices in the form of DC-DC, DC-AC, AC-DC, and AC-AC converters (Rashid, M. H., 2017). From the statistics reported by IEA in Figure 0.1 and Figure 0.2, one can be concluded that the applications of power electronics converters are rapidly increasing and

becoming indispensable, as electricity demand grows exponentially. Consequently, fulfilling the net zero program without using high-quality power electronic converters is impossible.

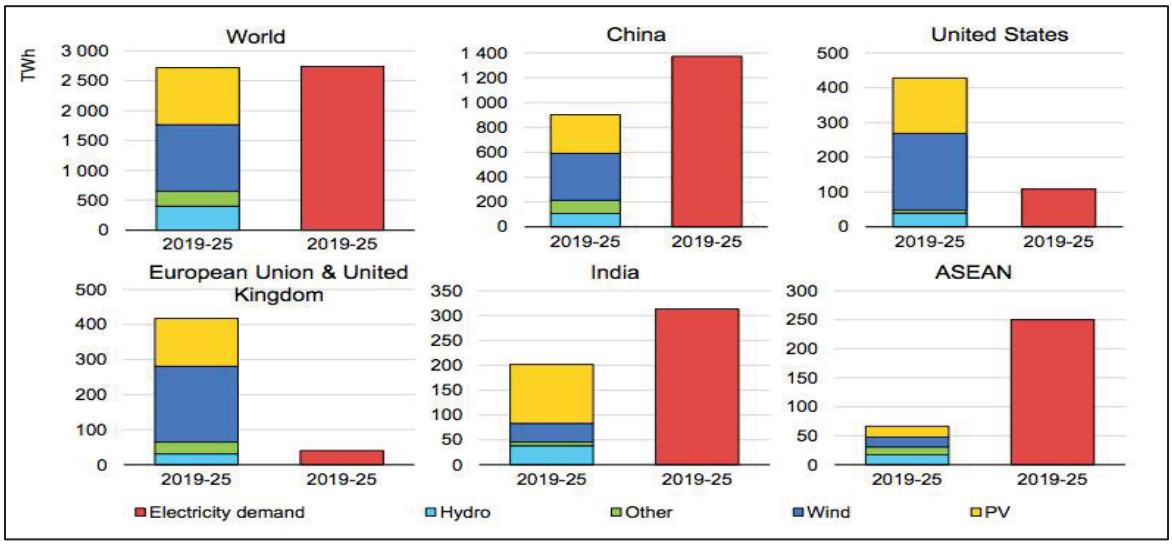

Figure 0.1 Electricity demand versus renewable energy generation
Adapted from Josh (2020)

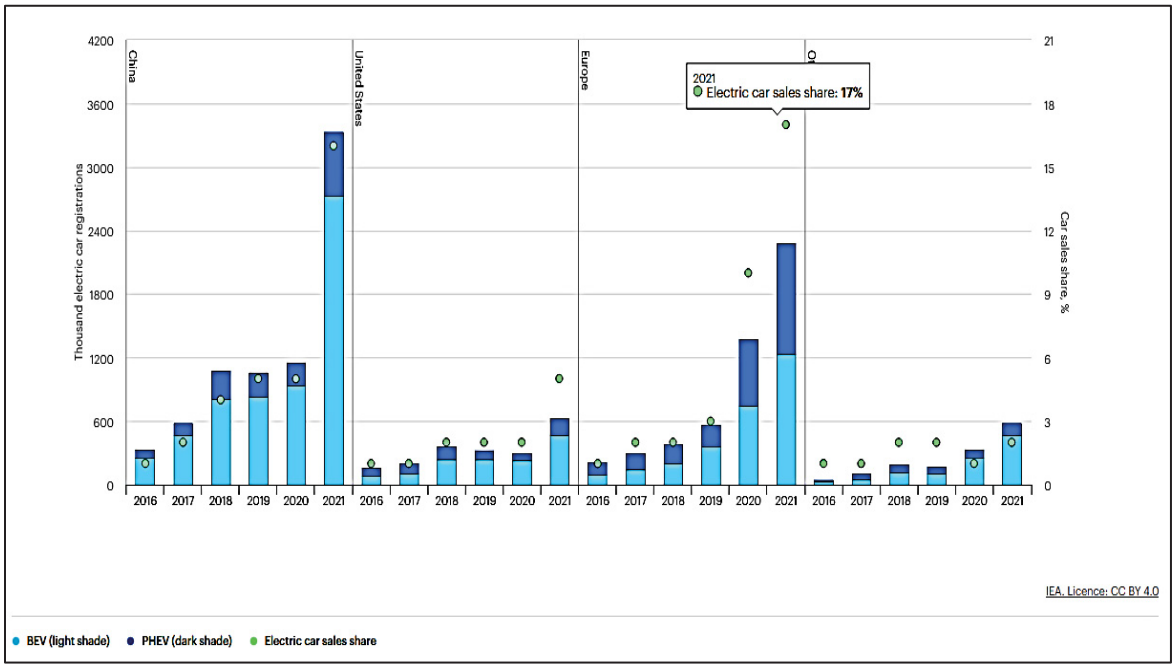

Figure 0.2 Electric cars registrations in 2016-2021
Adapted from IEA-2022 (2022)

A power converter is built using semiconductor switches, diodes, and passive components, such as capacitors, inductors, and transformers. The number and type of active and passive components used in power electronic converters depend on the application, operational power level, and power quality requirements (Rashid, M. H., 2017). Concerning this fact, the design and development of DC-AC inverters and AC-DC rectifiers are much more complicated than the other power electronic converters due to the variousness of applications and interaction with the grid.

Inverters are vastly used in renewable energy-based distributed generators to convert and control the power injected into stand-alone loads or the grid (Emadi et al., 2008; Sharifzadeh, Vahedi, Portillo, Franquelo, & Al-Haddad, 2018; Babaie, Sharifzadeh, Kanaan, & Al-Haddad, 2020; Babaie, Sharifzadeh, Mehrasa, & Al-Haddad, 2019; Vahedi, & Al-Haddad, 2015). In EVs, inverters control the torque and speed applied to the wheels by the motor. Inverters also contribute to improving the power quality of the grid, especially micro-grids, in the form of active power filters, electric springs, and static synchronous compensators (Singh et al., 2014; Abu-Rub et al., 2014; Kaymanesh, Babaie, Chandra, & Al-Haddad, 2021). On the other hand, rectifiers are used as battery chargers in EVs or power supplies for arc furnaces, energy storage systems, and DC microgrids (Hemavathi et al., 2022; Wei et al., 2019; Babaie, Mehrasa, Sharifzadeh, & Al-Haddad, 2021; Mehrasa, Sharifzadeh, Babaie, & Al-Haddad, 2020). The combination of rectifiers and inverters is also used in uninterruptable power supplies to feed critical medical and security systems (Guerrero et al., 2008). Regarding the growing, crucial influence of inverters and rectifiers on the future of electricity, the rest of this thesis concentrates on DC-AC and AC-DC systems and refers to them as power converters.

Power electronic converters can be classified based on their AC voltage waveform; in conventional two-level converters, the AC voltage immediately changes from the positive polarity to the negative one with variations equal to the switching frequency. The generated high-frequency square voltage waveform in two-level converters is highly polluted by harmonics. The volume and power rate of passive components on the both DC and AC sides of the converter are adversely affected by the harmonics. In addition, harmonics increase power

losses, cause thermal problems, reduce the lifetime of components, and decrease the efficiency of the converter as well as loads.

To improve the harmonic profile of the voltage waveform, a high-order filter, such as LC or LCL should be joined to the converter (Liserre et al., 2005; Tran et al., 2023). Unfortunately, filters increase the converter volume, weight, and cost. Filters also cause resonance disorders, decrease the converter efficiency, and impose an extra burden on the cooling system in high-power applications. Increasing the switching frequency is a common solution to reduce the size of filters and push back the frequency of harmonics; even so, this strategy intensifies the switching losses and voltage stress over the switching components. The voltage stress in two-level converters is pernicious due to high-frequency switching transitions occurring between the positive and negative poles. As a result, two-level converters are practically restricted to low- or medium-voltage applications due to the limited voltage operation of semiconductor switches, the bulky size of components, and power losses (Franquelo et al., 2008).

In comparison with conventional two-level converters, multilevel converters (MLC) (Li, Y., & Li, Y. W., 2021), such as neutral point clamped (NPC) (Nabae, et al., 1981), cascaded H-bridge (CHB) (Liu, Ma, Song, & Peng, 2022), packed U-cell (PUC) (Ounejjar, Al-Haddad, & Gregoire, 2010), packed E-cell (PEC) (Sharifzadeh, & Al-Haddad, 2019), and voltage level multiplier module (VLMM) (Abarzadeh, & Al-Haddad, 2019) are quite competitive in terms of efficiency, power quality, volume, and power delivery capacity. Indeed, the superiority of MLCs is because of generating a quasi-sinusoidal voltage waveform using lower voltage levels provided by low-power DC sources and capacitors. Nonetheless, involving more semiconductors switches and passive components complicates the modeling and control of MLCs, especially in grid-tied applications.

Motivation and Challenges

As discussed before, MLCs offer promising improvements in terms of power quality, power density, operating voltage range, dynamic response, voltage stress, and switching losses.

However, these fundamental improvements come with the cost of involving more active and passive components in the structure of MLCs, which leads to further modeling, controllability, and stability challenges. From a modeling point of view, MLCs are known as variable structure systems including discontinuous dynamics. The variable structure of MLCs is undesirably exposed to parametric/structural uncertainties and disturbances caused by switching transitions, harmonics, dynamic loads, and voltage stress. In addition, each passive component in MLCs is considered a state variable and should be measured and then involved in the control loop. Increasing the number of sensors on the other hand causes new challenges for MLCs in terms of reliability and affordability. Therefore, using advanced robust controllers with multi-objective control capability is essential for MLCs, especially in the grid-connected mode of operation since more uncertainties, disturbances, and dynamics are imposed on the system.

On the other hand, the design of an advanced multi-objective controller is grueling as the variable structure modeling of MLCs in the presence of uncertainties and disturbances is much more complicated than conventional two-level converters. e.g., sliding mode control (SMC) is ideal to overcome the model uncertainties and reject the noise effects; even so, SMC is not able to provide effective multi-objective control for MLCs with floating DC links (Babaie, Sharifzadeh, Kanaan, & Al-Haddad, 2020).

Model predictive control (MPC) as a discrete control algorithm is highly compatible with the variable structure behavior of the MLCs; MPC provides fast dynamic response and multi-objective control, which makes it more suitable for this class of power electronic converters. Nonetheless, MPC is a model-based controller with sensitivity to uncertainties and variations of the parameters (Babaie, Mehrasa, Sharifzadeh, & Al-Haddad, 2021). Moreover, the multi-objective performance of MPC is adversely affected by the tedious tuning of its weighting factors (Dragičević, & Novak, 2018).

Intelligent control as an emerging model-free control concept in the field of power electronics has demonstrated promising robust, multi-objective control performance for MLCs in various applications (Zhao, Blaabjerg, & Wang, 2020; Mehrasa, Babaie, Zafari, & Al-Haddad, 2021;

Babaie, & Al-Haddad, 2020a). Recent related research works reveal the high potential of intelligent control algorithms to address the modeling and control problems of MLCs. However, the development of intelligent controllers needs further improvements in terms of training and data acquisition, especially for MLCs due to the considerable number of variables, discontinuous behavior of system trajectories, structural/parametric uncertainties, and fast dynamic performance.

Consequently, advanced multi-objective, robust control algorithms have to be developed since power electronic technology is going toward designing and employing more efficient MLCs to meet the net zero program. For that reason, there is a high motivation to address the modeling, controllability, and stability problems of MLCs using the most recent advanced modeling and control algorithms and strategies.

Research Objectives

This thesis concentrates on the modeling, control, and development of MLCs for stand-alone and grid-tied applications. The grid-tied applications of MLCs studied in this thesis are related to solar system integration, multiple outputs active rectifiers, active power filters, and power ancillary services. Seven-level PUC (PUC7), modified seven-level PUC (MPUC7), nine-level PEC (PEC9), and three-phase NPC are selected as the case studies due to drastic modeling, controllability, and stability challenges. Indeed, various case studies are considered to verify the generalizability of the contributions. Concerning the aforementioned applications and challenges, the following sub-objectives are theoretically and practically developed and investigated in the rest of this thesis:

Enhancing the contribution of intelligent control algorithms in power electronics problems through the development of a novel data-free self-training strategy for artificial neural networks (ANN).

Studying and developing the stability conditions and criteria for predictive-based nonlinear controllers, which are applied to power electronics converters, especially MLCs, based on a model-based discrete definition of Lyapunov stability theory.

Developing and implementing a robust sensor-less control algorithm for MLCs with floating dc-link capacitors like PUC7 and PEC9 in both stand-alone and grid-tied applications using sliding mode control theory.

Hybridizing artificial intelligence and MPC to mitigate the training difficulties of the weighting factors used in the cost function besides improving its robustness and multi-objective control performance in the presence of uncertainties and parametric variations.

Designing, modeling, and controlling a new compact MLC with boost capability and simple DC link voltage balancing for power quality ancillary services, such as active power filter (APF) and static synchronous compensator (STATCOM), based on the existing topologies of compact MLCs.

Methodology

To fulfill the main objectives of this thesis, the following literature review, design, simulation, and implementation steps are considered:

The first step is dedicated to investigating the state of the art of MLCs and control techniques for grid-connected and stand-alone applications. Regarding, the chosen MLC topologies, including PUC, PEC, and NPC, have been investigated from the aspect of modeling, control, and application.

To determine the controllability and stability issues of the MLCs, the candidate research works have been thereafter simulated, from a control point of view. The applied control strategies, including robust, predictive, and intelligent, have been investigated in terms of robustness,

multi-objective performance, and stability to distinguish the best candidates with high effectuality in addressing the controllability, stability, and efficiency challenges of the MLCs. This literature review remarkably promotes the contribution of this thesis to developing advanced multi-objective robust control algorithms for grid-tied MLCs. Thus, this step lasted until this research program was completed.

Concerning the outcomes of the literature review, several advanced multi-objective robust control strategies have been mathematically developed for the selected grid-tied MLCs, in the second step. The main research objectives of this thesis have been considered as the criteria to develop and evaluate the proposed multi-objective robust control algorithms. For the preliminary evaluations of the controllers and converters, different simulation setups, including various test scenarios, have been precisely created in MATLAB/Simulink environment; The simulation results have been then used to improve the performance of controllers and converters before any practical implementation to ensure safety and reduce implementation expenses.

In the end, the feasibility and reliability of the proposed multi-objective robust control algorithms and the boost MLC topology have been experimentally investigated using a well-equipped, modern setup, including dSPACE 1103, dSPACE MicroLabBox (1202), Chroma 61086, OPAL-RT OP8662, a Power Analyzer, a four-channel oscilloscope with 2Gs, 8kW RLC load banks, a three-phase autotransformer for the grid ($120V_{rms}$), and a 400V bidirectional DC power supply. The tested converters are PUC7, MPUC7, three-phase NPC, PEC9, and a developed eleven-level Boost Packed E-Cell (BPEC11), with a power range between 1kW and 3kW. This setup is provided and supported by the groupe de recherche en électronique de puissance et commande industrielle (GRÉPCI) located at école de technologie supérieure (ÉTS), in Montreal, Canada.

Thesis Contribution

The contributions of this thesis are detailed below:

A novel sensorless multi-objective control algorithm using the first-order sliding mode control theory is proposed for the PUC7 converter in grid-connected and stand-alone modes of operation. Despite the existing methods, the proposed SMC-based algorithm regulates the auxiliary DC link voltage of the PUC7 converter without measuring it. This technique can be applied to MLCs with serially extended switched capacitors to reduce the number of sensors and guarantee stability. The experimental results demonstrate the robustness of the sensorless SMC algorithm under dynamic conditions and parametric mismatch of the grid filter.

The stability of the sensorless controller is mathematically evaluated and ensured through Lyapunov theory applied to a parametric model of the PUC7 in both stand-alone and grid-connected modes of operation.

A new model-based impedance estimator is developed to calculate the peak amplitude of the reference current based on the variation of loads for MLCs in stand-alone and rectifier modes of operation.

A novel unsupervised, fast self-training strategy (FSTS) is proposed based on metaheuristic algorithms, such as artificial bee colony (ABC) and particle swarm optimization (PSO) to enhance the contribution of artificial intelligence to model-free controlling of power electronic converters, especially MLCs. The proposed self-training strategy remarkably facilitates the training process of ANN-based controllers and eliminates the data acquisition requirements in power electronics design problems.

An advanced, mature version of the FSTS is proposed based on the imperialist competitive algorithm (ICA) as a virtual multicore processor to accelerate the training process of ANNs with a significant level of complexity.

A hybrid intelligent predictive control algorithm using MPC and ANNs is proposed to fulfill the multi-objective control requirement of MLCs, particularly for grid-tied applications. The proposed intelligent predictive multi-objective control method incredibly improves the performance of the conventional MPC in terms of tuning difficulties, modeling sensitivities, variable switching frequency, voltage stress, and computational burden.

A vulgarized tuning strategy using the ABC algorithm is proposed for MPC to set the best optimal values of the weighting factors without using any analytical model.

An original discrete Lyapunov function is proposed to predict and ensure the stability of MPC-based control algorithms during each sampling period. The proposed discrete Lyapunov function forms a decoupled term from the other objectives, in the cost function of MPC, without increasing the weighting factors. The decoupled term imposes an infinite value on the cost function for switching vectors with destabilizing impact. As a case study, the experimental results of applying the proposed Lyapunov-based MPC method to a double outputs MPUC7 rectifier demonstrate its feasibility and effectiveness practically.

Concerning the rapid growth of grid-tied distributed generators (DG), an advanced communication-based power management system with security layers is required to ensure that the grid power quality is maintained. Under this situation, the design of a secure, centralized power management system will be sophisticated, as the number of DGs is growing. To relieve this problem a novel decentralized ANN-based power management strategy is proposed to regulate the power factor of the grid, autonomously. The proposed ANN-based autonomous power management system is also trained through the FSTS algorithm without data acquisition.

An original predictive model of harmonics is formulated for MPC-based control algorithms to mitigate selective harmonics in grid-tied transformerless MLCs. The proposed selective-predictive harmonic mitigation method improves the harmonic profile of the current and

minimizes the size of DC link capacitors in transformerless MLCs supplied by capacitors. This is the first time that the predictive model of harmonics is suggested without using any fast Fourier transform (FFT) algorithm.

The concept of intelligent converters for smart grids is substantially developed by proposing advanced model-free neural and fuzzy controllers with the ability to implement expert knowledge.

On the subjects of controllability and stability challenges of MLCs, a novel 11-level boost converter with fault tolerance capability and voltage level switching performance based on the E-cell arrangement of floating capacitors (Babaie, & Al-Haddad, 2022a) is introduced. The proposed bidirectional boost converter is precisely detailed in terms of operational principles, power losses, voltage stress, boost ratio, dynamic model, and hardware implementation. As a case study, a compact active power filter with a reactive power compensation feature is designed and controlled based on a multi-objective predictive controller to provide power-quality ancillary services for the grid.

Formulating application-oriented mathematical models for advanced intelligent controllers, including ANNs, fuzzy, and adaptive neuro-fuzzy inference control (ANFIC).

Comprehensive comparisons between MLC topologies and the applied advanced multi-objective controllers for different applications.

Substantial examination of the MLCs and advanced multi-objective robust controllers through an experimental setup, including the most reliable laboratory equipment.

The results of this thesis have been published in the most prestigious peer-reviewed IEEE journals. The first paper titled “Switching-Based Optimized Sliding-Mode Control for Capacitor Self-Voltage Balancing Operation of Seven-Level PUC Inverter” has been published in IEEE Transactions on Industrial Electronics (Babaie, Sharifzadeh, Kanaan, & Al-Haddad,

2020). The second paper titled “Supervised Learning Model Predictive Control Trained by ABC Algorithm for Common-Mode Voltage Suppression in NPC Inverter” has been published in the IEEE Journal of Emerging and Selected Topics in Power Electronics (Babaie, Sharifzadeh, Mehrasa, Chouinard, & Al-Haddad, 2020). The third paper titled “Floating Weighting Factors ANN-MPC Based on Lyapunov Stability for Seven-Level Modified PUC Active Rectifier” has been published in IEEE Transactions on Industrial Electronics (Babaie, Mehrasa, Sharifzadeh, & Al-Haddad, 2021). The fourth paper titled “Boost Packed E-Cell: A Compact Multilevel Converter for Power Quality Ancillary Services” has been published in IEEE Transactions on Industry Applications (Babaie, & Al-Haddad, 2022a). The last journal paper titled “Self-Training Intelligent Predictive Control for Grid-Tied Transformerless Multilevel Converters” has been published in IEEE Transactions on Power Electronics (Babaie, & Al-Haddad, 2023).

Moreover, the supplementary results of this thesis, including 23 conference papers, have been submitted and presented at well-known international events, such as IEEE Energy Conversion Congress and Exposition (ECCE), IEEE International Conference on Industrial Technology (ICIT), IEEE Applied Power Electronics Conference and Exposition (APEC), IEEE International Symposium on Industrial Electronics (ISIE), IEEE Electrical Power and Energy Conference (EPEC), International Symposium on Power Electronics, Electrical Drives, Automation and Motion (SPEEDAM), IEEE Power & Energy Society General Meeting (PESGM), International Conference on Smart Energy Systems and Technologies (SEST), IEEE Industry Applications Society Annual Meeting (IAS), and IEEE Transportation Electrification Conference & Expo (ITEC).

Thesis Outlines

The rest of this thesis is divided into six chapters. CHAPTER 1 is dedicated to presenting a comprehensive literature review on topologies, applications, modeling, and control of MLCs. Capacitor voltage balancing, as the most intricate control problem of compact MLCs, is extensively studied and addressed using a sensorless multi-objective robust control strategy in

CHAPTER 2. The sensorless control algorithm has been experimentally evaluated through the PUC7 converter for both grid-tied and stand-alone modes of operation. CHAPTER 3 elaborates on the optimal selection of the weighing factors through metaheuristic optimization for multi-objective MPC algorithms applied to MLCs. CHAPTER 4 and CHAPTER 5 are focused on enhancing the contribution of artificial intelligence to controlling power electronic converters. Accordingly, a novel self-training strategy is developed in CHAPTER 4 for the control applications of ANNs in power electronics. The proposed self-training strategy is unsupervised and does not need data acquisition. In addition, the stability of model predictive control is thoroughly studied and addressed in CHAPTER 4; indeed, a novel decoupled stability term based on a discrete Lyapunov function is proposed to predict and guarantee the stability of the control loop per each sampling period. As a case study, the proposed self-trained, robust ANN-MPC has been practically applied to an MPUC7 active rectifier and evaluated through various experimental test scenarios to prove its merits. CHAPTER 5 presents an advanced, mature version of the self-training strategy based on the ICA algorithm known as a virtual multicore processor to accelerate the training process of ANN-based controllers. Real-time Selective Harmonic Mitigation and autonomous power management using smart MLCs are also studied in CHAPTER 5. Considering improving power density, efficiency, and voltage stability of switched capacitors MLCs for power quality ancillary services, a novel 11-level boost topology with fault tolerance and voltage level switching performance is introduced in CHAPTER 6. The proposed boost packed E-cell (BPEC) MLC is developed regarding operational principles, modeling, control, hardware, and application. In the end, conclusions, remarks, and future works are presented.

CHAPTER 1

LITERATURE REVIEW OF MULTILEVEL CONVERTER TOPOLOGIES AND APPLIED CONTROL STRATEGIES

1.1 Introduction

Power electronics converters play the key roles of controlling, converting, purifying, and securing electricity in various power systems, such as renewable energy resources, active power filters (APF), uninterruptible power supplies (UPS), electric motor drives, electric springs, voltage sag/swell static synchronous compensators (STATCOM), electric vehicles (EV), and arc furnaces (Abu-Rub et al., 2010; Yacoubi et al., 2005; Singh, Chandra, & Al-Haddad, 2000; Vahedi, Kanaan, & Al-Haddad, 2015; Singh, Al-Haddad, Chandra, 1999). The research and development of modern power converters mainly focus on new cost-effective multilevel topologies and multi-objective robust control algorithms to achieve maximum power quality, power density, energy conversion efficiency, reliability, stability, and flexibility (Franquelo et al., 2008; Li, Y., & Li, Y. W., 2021; Abu-Rub, et al., 2010). Neutral point clamped (NPC) (Sebaaly, Vahedi, Kanaan, Moubayed, & Al-Haddad, 2016a), cascade H-bridge (CHB) (Vahedi, Al-Haddad, Labbe, & Rahmani, 2014), flying capacitors (FC) (Dargahi et al., 2012), modular multilevel converter (MMC) (Mehrasa, Pouresmaeil, Zabihi, & Catalão; 2016), packed U-cell (PUC) (Babaie, Sharifzadeh, Mehrasa, Chouinard, & Al-Haddad, 2019), packed E-cell (PEC) (Babaie, Mehrasa, Sharifzadeh, Melis, & Al-Haddad, 2020), voltage level multiplier module (VLMM) (Babaie, Abarzadeh, & Al-Haddad, 2022a, October), and recently the Z-PUC (Arazm, & Al-Haddad, 2020), are some promising multilevel topologies proposed to replace conventional two-level converters for the aforementioned application.

Since semiconductor switches are the only controllable elements in power converters, their switching control is required to attain desired power quality, efficiency, reliability, stability, flexibility, and dynamic response. Conventionally, an open-loop pulse width modulator-based technique (PWM), such as sinusoidal PWM (SPWM), space vector PWM (SVPWM), selective

harmonic elimination (SHE), or hysteresis band modulation (HBM) is used to control the switching transitions of a power converter. Nonetheless, to maintain the stability of passive components used in DC links and filters, a closed-loop control structure including a controller and a PWM modulator is always preferred, especially for grid-tied applications. In a closed-loop control strategy, the controller modifies the switching reference signal for the PWM modulator based on errors between the desired references and the measured variables, like capacitors' voltages, inductors' currents, the fundamental frequency, and the power factor. To design an appropriate closed-loop control technique, a mathematical model of the converter is first acquired concerning the application, and then a proper control strategy is selected. In this regard, various linear, nonlinear, and intelligent strategies, including proportional integral control (PI) (Wu, Chang, Hung, & Chiu, 2023), linear quadratic regulator (LQR) (Arab, Vahedi, & Al-Haddad, 2019), model predictive control (MPC) (Babaie, Sharifzadeh, & Al-Haddad, 2020, October), sliding mode control (SMC) (Delghavi, & Yazdani, 2017), second-order SMC (SOSMC) (Babaie, & Al-Haddad, 2021, October; Tabart, Vechiu, Etxeberria, & Bacha, 2017), feedback linearization (Mehrasa, Babaie, Sharifzadeh, & Al-Haddad, 2021), model reference adaptive control (MRAC) (Mukherjee, et al., 2017), backstepping control (Ahmadijokani, et al., 2021; Babaie, & Al-Haddad; 2021, June), self-tuning control (Cichowski, & Nieznanski, 2005), variable structure control (VSC) (Babaie, Rahmani, & Rezaie, 2018), Lyapunov control (Babaie, Sharifzadeh, Mehrasa, & Al-Haddad, 2020, March), artificial neural network control (ANN) (Fu, & Li, 2015), and fuzzy control (Wai, et al., 2015; Babaie, Sharifzadeh, Mehrasa, Baillargeon, & Al-Haddad, 2018) are available to design closed-loop controllers for power converters. To select the best control algorithm, many factors including the number of state variables, the model accuracy, implementation expenses, environmental conditions, and desired dynamic response should be considered. On one hand, linear control methods like PI and LQR are simple to implement and less sensitive to model accuracy; however, they show weak dynamic performance, including destabilizing transitions, for nonlinear systems encountered with variable parameters, discrete states, and environmental disturbances. On the other hand, despite the robust performance and fast dynamic response, the sensitivity of nonlinear methods, such as conventional SMC and MPC, to model accuracy and control/weighting factors causes control distortions like chattering and harmonics, which

adversely impact the efficiency and stability of the controller as well as the system. As a result, compromising between control performance and design difficulties is essential. Fortunately, several alternative methods have been developed during the last two decades to address the destructive problems of conventional linear and nonlinear control techniques. e.g., SOSMC strategies, including twisting and super-twisting, are able to mitigate the chattering phenomenon and form a control loop with less sensitivity to uncertainties (Babaie, & Ranjbar, 2019). As another example, MPC is combined with other control and optimization algorithms, such as SMC, metaheuristic algorithms, and ANNs to reduce its sensitivity to model uncertainties, mismatches, and weighting factors (Akpolat et al., 2021; Zhang, Mijatovic, Cai, & Dragičević, 2021; Mehrasa, Babaie, Zafari, & Al-Haddad, 2021).

From a control point of view, power electronics converters are known as variable structure nonlinear, underactuated systems polluted by uncertainties and environmental disturbances. Moreover, the coexistence of continuous and discontinuous trajectories in power electronics systems intensifies the nonlinear behavior of dynamics and complicates the design and tuning of controllers. These challenges become severely problematic in the case of MLCs, as the number of state variables is rapidly growing due to using more switches and passive components. Consequently, developing MLC topologies toward improving power quality, power density, conversion efficiency, reliability, stability, and flexibility is feasible only with the simultaneous development of advanced robust multi-objective control strategies. Regarding this, researchers have been working on different control techniques for more than two decades to address the controllability and stability challenges of MLCs. Following the previous efforts, this thesis has been dedicated to addressing the crucial need for advanced controllers besides modifying the topology of MLCs. Considering the main goal of this thesis, in the rest of this chapter, the most applicable MLCs and control techniques are studied for different applications to have a thorough overview of the state of the art.

1.2 Multilevel Converter Topologies

Regardless of the topology and application, power converters are built using semiconductor switches and passive components, including capacitors and inductors. Figure 1.1 presents a conventional topology of two-level power converters. This half-bridge-based converter generates a controlled two-level voltage waveform on the AC side using two switches per phase, a DC source, and an LCL filter, to supply a three-phase load. The PWM voltage waveform is generated and controlled by an open-loop or closed-loop modulator as shown in Figure 1.2.

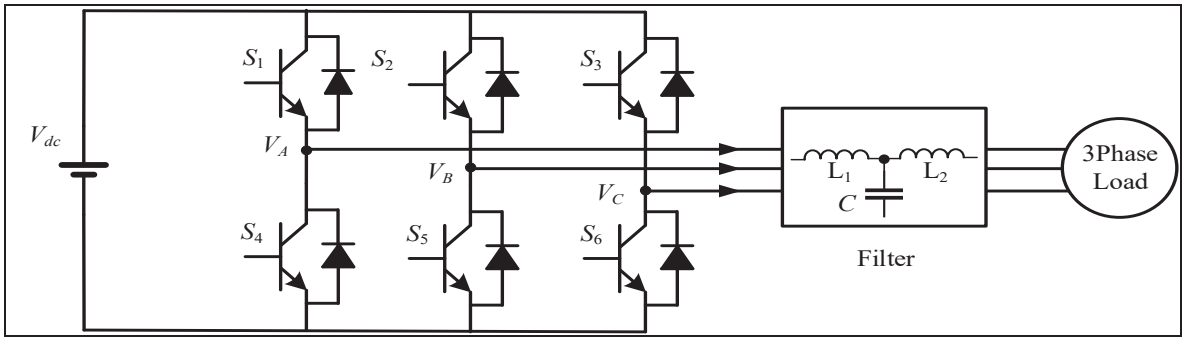

Figure 1.1 Conventional two-level converter

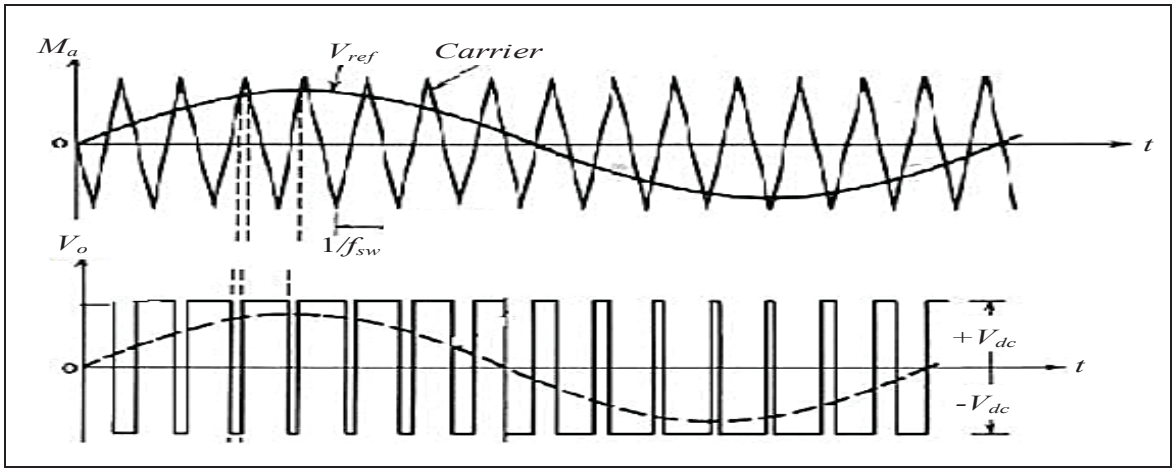

Figure 1.2 Two-level voltage waveform generated by conventional half-bridge converter
Taken from Aboadla (2016)

The pair power switches, including (S_1, S_4), (S_2, S_5), and (S_3, S_6), operate complementary to prevent the short circuit of the DC source while the squared voltage waveform is generated. This unique switching operation of the converters allows the output voltage to only change between $+V_{dc}$ and $-V_{dc}$ without providing the zero level. Considering the extreme level of harmonics generated by this two-level voltage waveform, a high-order filter like the LCL shown in Figure 1.1 must be established on the AC side of the converter to meet the power quality requirements. Unfortunately, the filter imposes more complexity on the control loop, as more state variables require to be controlled. Moreover, the filter increases the volume, weight, and implementation costs of the converter, causes resonance disorders, diminishes the conversion efficiency, and complicates the cooling system in high-power applications. Increasing the switching frequency is widely used to shrink the filter by shifting harmonics to high-frequency levels; however, this strategy intensifies the switching losses and voltage stress over the switching components. Alternatively, increasing the voltage levels, including zero, leads to a quasi-sinusoidal voltage waveform with less harmonic pollution. Figure 1.3 depicts an *n*-level voltage waveform, which can be generated by a multilevel converter (MLC).

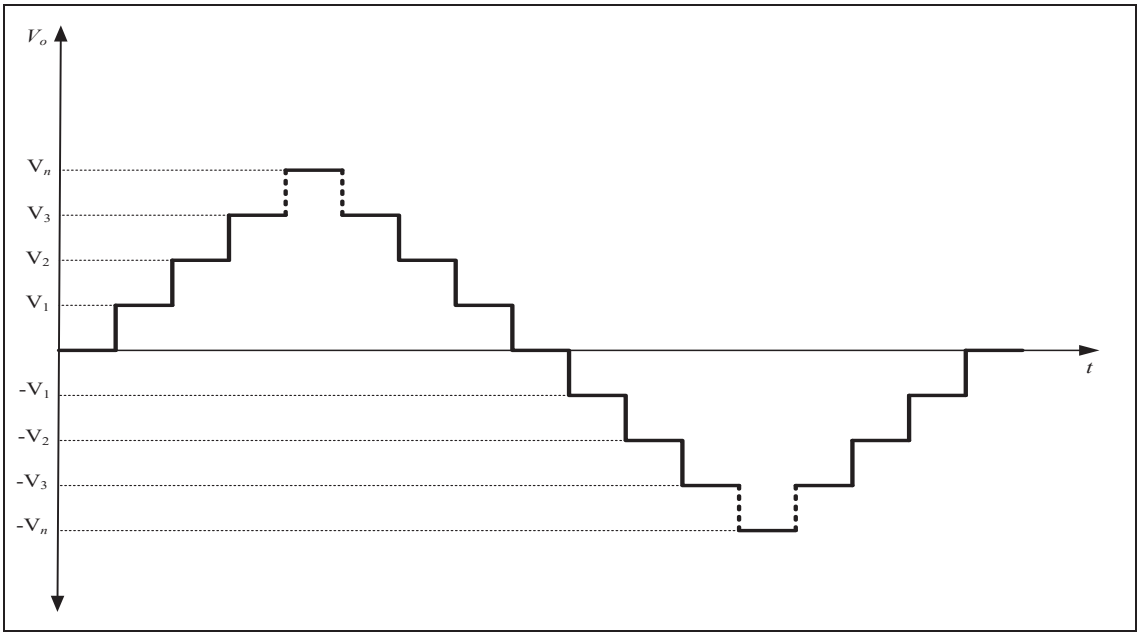

Figure 1.3 Quasi-sinusoidal voltage waveform generated by a multilevel converter

The multilevel voltage waveform is a promising solution to address many problems that conventional two-level topologies suffer from. Since the multilevel voltage waveform is generated using lower voltage levels, lower voltage stress is also imposed on switches. As a result, low-power, cost-effective switches are required to handle high-voltage applications. In addition, the switching frequency can be decreased while the power quality is sustained using low-volume, first-order filters. Reducing the switching frequency also contributes to improving the efficiency of the converter since power losses are mitigated concurrently. With a certain level of voltage resolution, the AC-side filter can be remarkably shrunk or even eliminated, which results in a wide bandwidth converter with an immediate dynamic response suitable for different applications, such as very high-speed motor drives and electric springs. The multilevel voltage waveform is generated and controlled using lower voltage DC sources, capacitors, and switches. Accordingly, increasing the voltage levels demands more active and passive components. Considering a compromise between voltage levels (resolution) and component count, countless topologies have been introduced (Franquelo et al, 2008; Li, Y., & Li, Y. W., 2021; Abu-Rub, et al., 2010). In the following subsections, the most successful industrialized, cost-effective MLC topologies are studied in terms of configuration, switching operation, and control.

1.2.1 Neutral Point Clamped Converter

Neutral point clamped is a bidirectional three-level topology, which has been proposed by Nabae in 1981 (Nabae et al., 1981). Because of using a single DC source, including two capacitors, NPC is still a popular, cost-effective converter in multiphase applications, such as drives, renewable energies, battery chargers, APFs, and STATCOMs (Dyanamina, & Kakodia, 2021; Lee, Lee, & Blaabjerg, 2014; Babaie, Sharifzadeh, & Al-Haddad, 2020, August; Vodyakho et al, 2009; Khatri, & Singh, 2016). The conventional topology of NPC provides a bidirectional three-level topology with the ability to operate in rectifier and inverter modes. The conventional schematic diagram of a three-phase NPC converter is presented in Figure 1.4; this converter is formed by three legs, including four semiconductor power switches and two clamped diodes. The clamped diodes are connected to the middle point of the DC link to

generate the zero-voltage level. The three legs of NPC are supplied by a DC link containing two capacitors and an active DC source. The voltage of the DC source is equally divided between the capacitors C_1 and C_2 to generate the positive and negative polarities for the three-level voltage waveform.

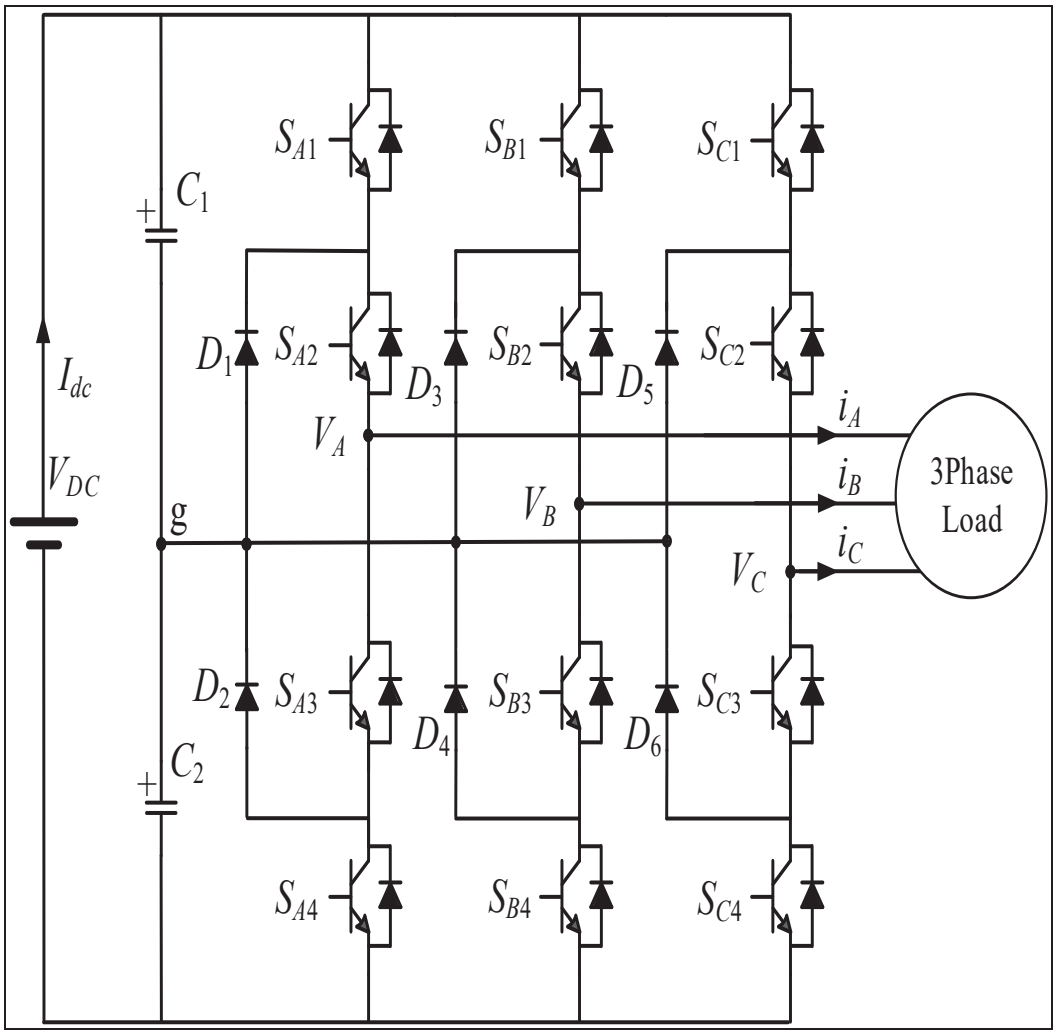

Figure 1.4 Three-phase configuration of a three-level NPC converter

The voltage levels and switching vectors of the three-phase NPC converter are presented in Table 1.1. The power switches including (S_{x1}, S_{x3}) and (S_{x2}, S_{x4}) operate complementary to avoid damaging the capacitors as well as the DC source.

Table 1.1 Possible switching states and voltage levels of NPC ($x\epsilon${A, B, C})

States	S_{x1}	S_{x2}	S_{x3}	S_{x4}	V_{out}
1	1	1	0	0	$+V_{DC}/2$
2	0	1	1	0	0
3	0	0	1	1	$-V_{DC}/2$

Despite conventional two-level converters, only half of the DC source voltage is switched in NPC, which results in lower voltage stress and switching loss. Moreover, the harmonic content is improved besides total harmonic distortion (THD) due to generating the zero-voltage level. Using a single DC source in three-phase applications is another prominent advantage of the NPC topology. However, this topology suffers from capacitor voltage balancing and a dramatically increasing number of components to generate more than three voltage levels. In addition, the three-level voltage resolution of NPC cannot sufficiently suppress harmonics to achieve a compact low-order filter on the AC side of the converter. Active NPC (ANPC) was later introduced to increase the voltage levels through flying capacitors (Abarzadeh, Khan, Weise, Al-Haddad, & El-Refaie, 2020); nonetheless, ANPC imposes extra control complexity on the system since the flying capacitors require a direct wide bandwidth controller to be stabilized under dynamic conditions.

1.2.2 Flying Capacitor Converter

Flying capacitor (FC) is another multilevel bidirectional topology inspired form NPC to generate a multilevel voltage waveform using floating capacitors instead of clamped diodes (Stillwell, Candan, & Pilawa-Podgurski, 2019). A single-phase five-level FC topology is illustrated in Figure 1.5. The depicted FC topology is built by ten capacitors besides eight power switches to generate the five-level voltage waveform.

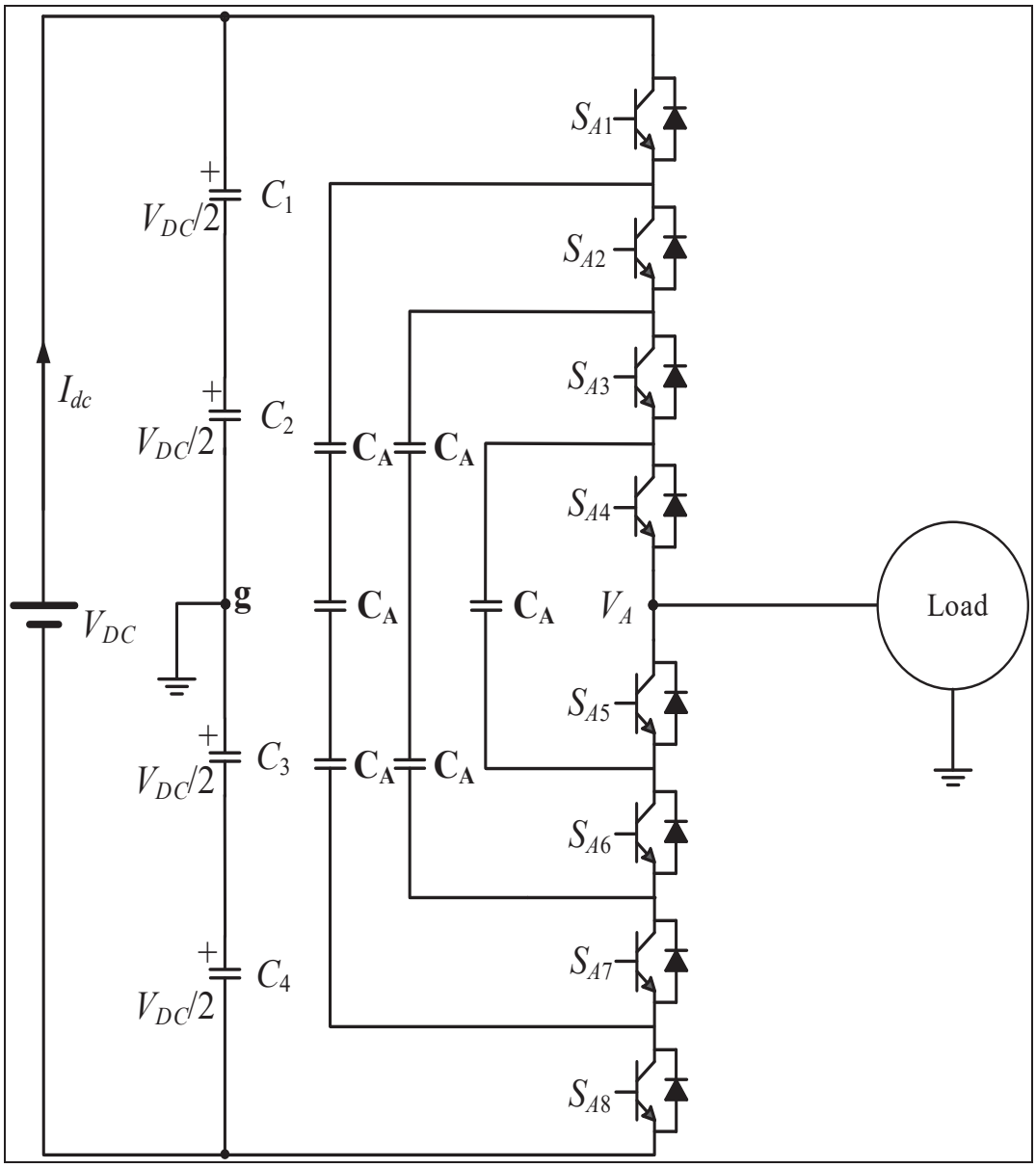

Figure 1.5 Single-phase configuration of FC converter

The switching states and corresponding voltage levels are also shown in Table 1.2. Compared to the NPC topology, replacing the diodes with capacitors in FC improves the conversion efficiency. Concerning the lack of switching redundancy in Table 1.2, regulating the capacitors' voltages is the major drawback of the FC converter. Accordingly, FC is not an affordable topology to design high-resolution voltage waveforms.

Table 1.2 Switching states and voltage levels of FC converter

States	S_{A1}	S_{x2}	S_{A3}	S_{A4}	S_{A5}	S_{A6}	S_{A7}	S_{A8}	V_{out}
1	1	1	1	1	0	0	0	0	$+V_{DC}$
2	1	1	1	0	1	0	0	0	$+V_{DC}/2$
3	1	1	0	0	1	1	0	0	0
4	1	0	0	0	1	1	1	0	$-V_{DC}/2$
5	0	0	0	0	1	1	1	1	$-V_{DC}$

1.2.3 Cascaded H-Bridge Converter

The cascaded H-bridge (CHB) is an interesting bidirectional multilevel topology with widespread industrial and domestic applications, like PV-based distributed generators, drives, APFs, STATCOMs, and high-voltage DC networks (HVDC) (Villanueva et al., 2009; Yang, Sun, Zha, & Tang, 2018; Elsanabary et al., 2020; Wang, & Liu, 2019; Barrena et al., 2008). CHB is popular because of its modular structure and simple extension of the voltage levels. This topology is designed by serial connection of multiple H-bridge cells; the general structure of CHB topology is illustrated in Figure 1.6. Each phase of CHB contains a DC link and four switches per cell; similar to a two-level converter, the switches in CHB operate complementary, as (S_{x1}, S_{x4}), (S_{x2}, S_{x3}). Each cell generates three voltage levels, including $+V_{DC}$, 0, $-V_{DC}$; thus, the output voltage is the summation of all cells. In CHB, the number of voltage levels is specified using (1.1).

$$N_V = 2^{Ce} + 1 \tag{1.1}$$

where N_V is the number of voltage levels and Ce is the number of cells. Considering (1.1), a CHB converter with two cells is able to generate a five-level voltage waveform. In consequence, the five-level CHB needs eight switches and two DC sources. The possible switching vectors and related voltage levels for a five-level CHB are shown in Table 1.3.

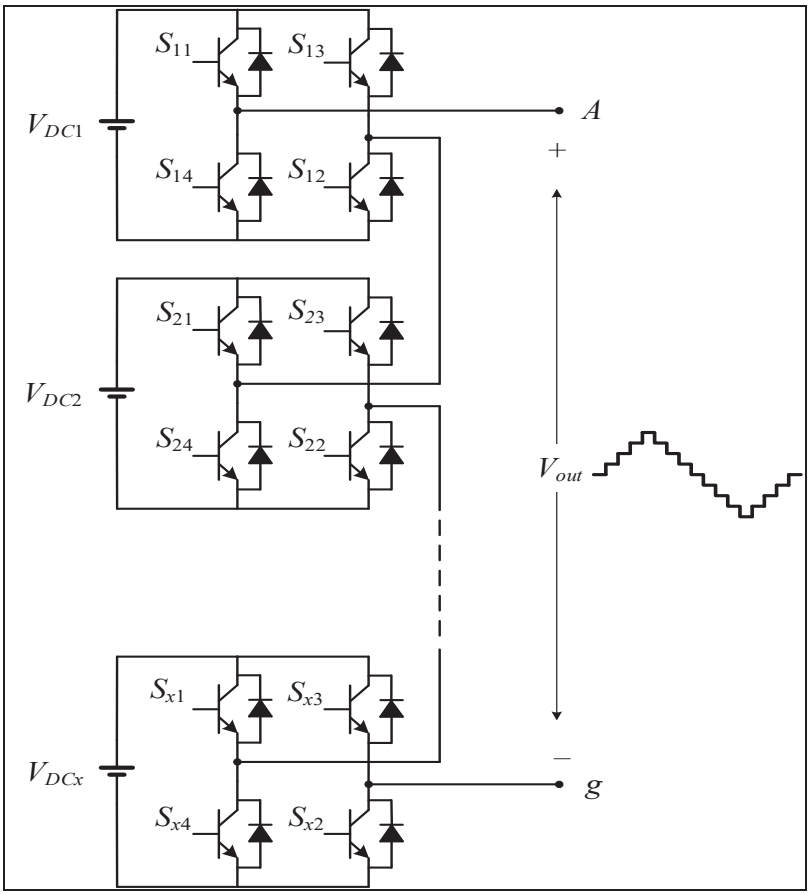

Figure 1.6 Schematic diagram of a single-phase CHB

Table 1.3 Switching states and voltage levels of five-level CHB converter

States	S_{11}	S_{12}	S_{13}	S_{14}	S_{21}	S_{22}	S_{23}	S_{24}	V_{out}
1	1	1	0	0	1	1	0	0	$+2V_{DC}$
2	1	1	0	0	0	1	0	1	$+V_{DC}$
3	1	0	1	0	1	0	1	0	0
4	0	1	0	1	0	0	1	1	$-V_{DC}$
5	0	0	1	1	0	0	1	1	$-2V_{DC}$

Even though CHB requires a large number of components, including several isolated DC sources, its voltage level balancing is not as problematic as NPC and FC. Indeed, the symmetric switching operation of the H-bridge cells allows the floating capacitors to be equally charged

or discharged, which alleviates the voltage regulation problem. Thanks to this unique feature, an advanced type of MLCs, the so-called modular multilevel converter (MMC), has been introduced, which can operate in high-voltage applications with excellent fault tolerance capability (Sharifzadeh, Mehrasa, Babaie, & Al-Haddad, 2019; Meng et al., 2019). A general structure of MMC is presented in Figure 1.7 for grid-tied applications.

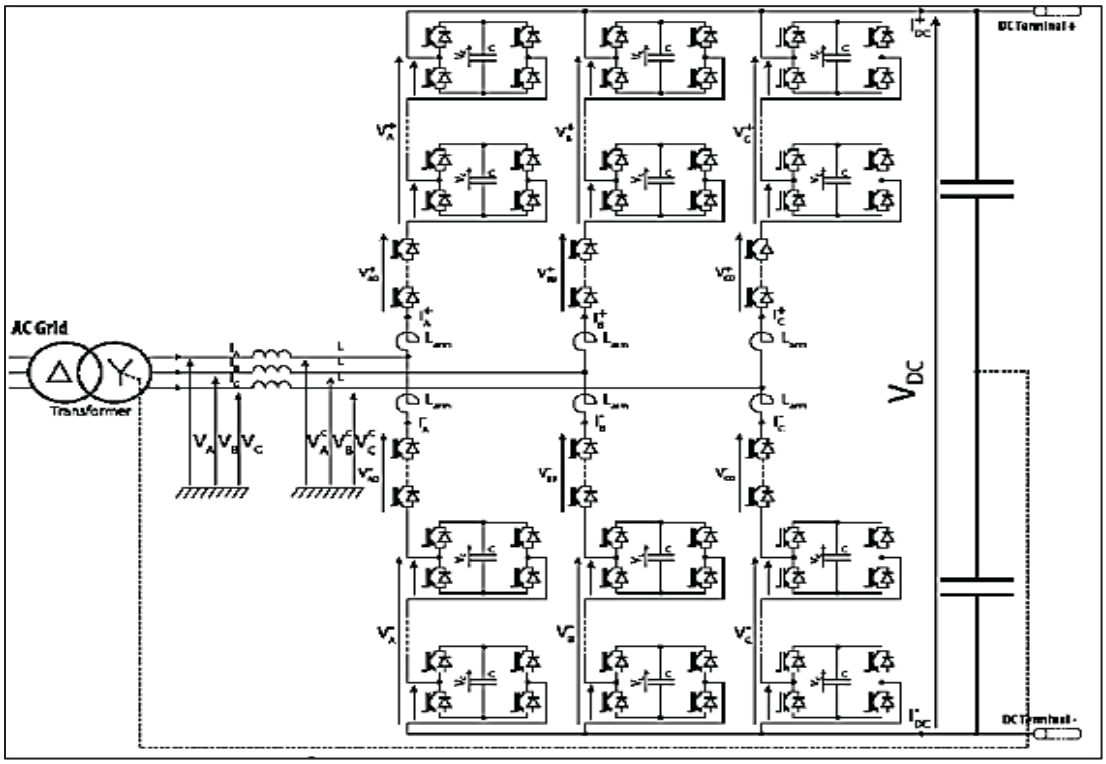

Figure 1.7 Three-phase MMC topology for grid-tied applications
Taken from Merlin (2014)

As shown in this figure, the H-bridge cells are used in the upper and lower arms of the converter to generate the positive and negative levels, respectively. MMC is not limited to H-bridge cells; other topologies, such as half-bridge, modified ANPC, the cross-connected submodule, Z-PUC (Arazm, & Al-Haddad, 2020), and the clamped double submodule, are also applicable to configure the positive and negative arms of the converter. It is worth mentioning that since MMC is not the main focus of this thesis, interested readers are referred to IEEE Xplore for more details.

1.2.4 Packed U-Cell Converter

Inspired by the hierarchical configuration of CHB, packed U-cell topology was introduced in 2010 to design the most compact, bidirectional MLCs. In spite of the aforementioned MLC topologies, PUC uses the minimum possible active and passive components to generate the maximum feasible voltage levels. PUC was first introduced as a seven-level topology, the so-called seven-level PUC (PUC7). The conventional configuration of PUC7 includes six switches, an active DC source, and an auxiliary floating DC capacitor. The overall schematic diagram of the PUC7 is depicted in Figure 1.8. Similar to other elaborated MLC topologies, the switching signals for (S_1, S_4), (S_2, S_5), and (S_3, S_6) are complementary to protect the main and auxiliary DC links from short-circuit.

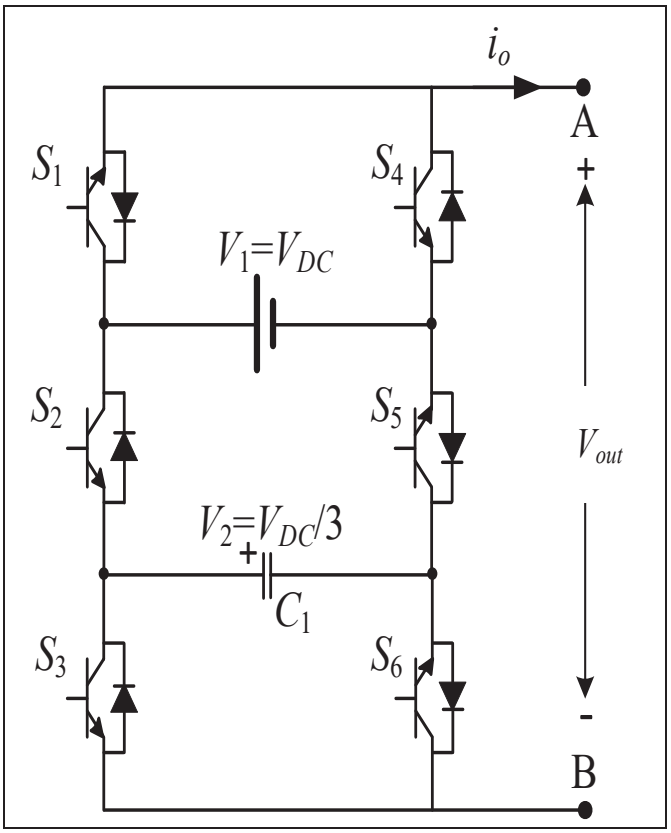

Figure 1.8 Conventional topology of PUC7

To generate the seven-level voltage waveform, the capacitor's voltage must be regulated at one-third of the DC source. Table 1.4 presents the switching states and voltage levels besides the charging and discharging modes of the floating capacitor for the PUC7 converter.

Table 1.4 Switching vectors and voltage levels of PUC7

States	S_1	S_2	S_3	S_4	S_5	S_6	V_{out}	C_1
1	1	0	0	0	1	1	$+V_{DC}$	Floating
2	1	0	1	0	1	0	$+V_{DC}-V_{C1}$	Charging
3	1	1	0	0	0	1	$+V_{C1}$	Discharging
4	0	0	0	1	1	1	0	Floating
5	1	1	1	0	0	0	0	Floating
6	0	0	1	1	1	0	$-V_{C1}$	Discharging
7	0	1	0	1	0	1	$V_{C1}-V_{DC}$	Charging
8	0	1	1	1	0	0	$-V_{DC}$	Floating

The charging and discharging modes of the capacitor depend on its position; it charges when connected to the DC source and discharges when it supplies the load. Considering Table 1.4, the PUC7 does not have redundant switching states for the capacitor charging and discharging modes. Accordingly, using a closed-loop advanced controller is mandatory for PUC7 to maintain the stability of its capacitor voltage. Concerning the underactuated structure of the PUC7, the direct control of the capacitor's voltage beside other state variables is a big challenge such that controlling the PUC7 has become a benchmark case to evaluate the performance of advanced control strategies (Metri et al., 2016; Vahedi, & Al-Haddad, 2015; Vasu et al., 2020; Makhamreh, Trabelsi, Kükrer, & Abu-Rub, 2019; Makhamreh, Trabelsi, Kükrer, & Abu-Rub, 2020). Later, the five-level PUC (PUC5) topology was introduced to overcome the capacitor voltage balancing problem of PUC7 (Vahedi, Labbé, & Al-Haddad, 2015). Compared with PUC7, the capacitor's voltage in PUC5 is regulated at half of the DC source to create redundant switching vectors for the charging and discharging modes of the capacitor. As a result, the capacitor's voltage in PUC5 becomes self-balanced without involving any direct control. Nonetheless, more THD, voltage stress, and volume are imposed on the power converter since

two voltage levels are dropped. The PUC topology can be optimally used to generate quasi-sinusoidal voltages with higher resolution, such as nine-level (Babaie, Sharifzadeh, & Al-Haddad, 2019, October; Niu et al., 2019), 15-level (Arazm, Kamwa, & Al-Haddad, 2019), 23-level (Sorto-Ventura et al., 2020), 31-level (Babaie, & Al-Haddad, 2022, September), and 49-level (Meraj et al., 2019). PUC as a reliable topology has been used in different applications such as single-phase and three-phase grid-connected and stand-alone modes of operations (Babaie, Mehrasa, Sharifzadeh, & Al-Haddad, 2019, September; Arazm, & Al-Haddad, 2021; Schuetz et al., 2021), renewable energy integration (Mishra et al., 2021), APFs (Vahedi, Shojaei, Dessaint, & Al-Haddad, 2017), active rectifiers (Vahedi, & Al-Haddad, 2016; Makhamreh, Trabelsi, Kükrer, & Abu-Rub, 2020; Babaie, Mehrasa, Sharifzadeh, & Al-Haddad, 2021), electric springs (Kaymanesh, Rezkallah, Chandra, & El-Bayeh, 2020; Kaymanesh, Babaie, Chandra, & Al-Haddad, 2021a; Kaymanesh, & Chandra, 2020), and STATCOMs (Kaymanesh, Chandra, & Al-Haddad, 2021b; Al-Qatouni et al., 2018). Despite being compact and cost-effective, PUC suffers from voltage balancing difficulties.

1.2.5 Packed E-Cell Converter

Packed E-Cell is an emerging compact and cost-effective MLC topology to generate quasi-sinusoidal voltage waveforms with voltage level switching operation from five to 11 (Babaie, Abarzadeh, & Al-Haddad, 2022b, October; Sharifzadeh, & Al-Haddad, 2019). Indeed, PEC topology is the modified version of PUC to tackle the voltage balancing issue using E-cells instead of U-cells. Figure 1.9 shows the nine-level PEC (PEC9) converter used in the grid-connected mode of operation. The PEC9 converter requires eight switches, an active DC source, and two capacitors connected in series to form the E-cell. In this topology, S_7 and S_8 build a four-quadrant switch to conduct the current through both capacitors of the auxiliary DC link during the entire voltage cycle.

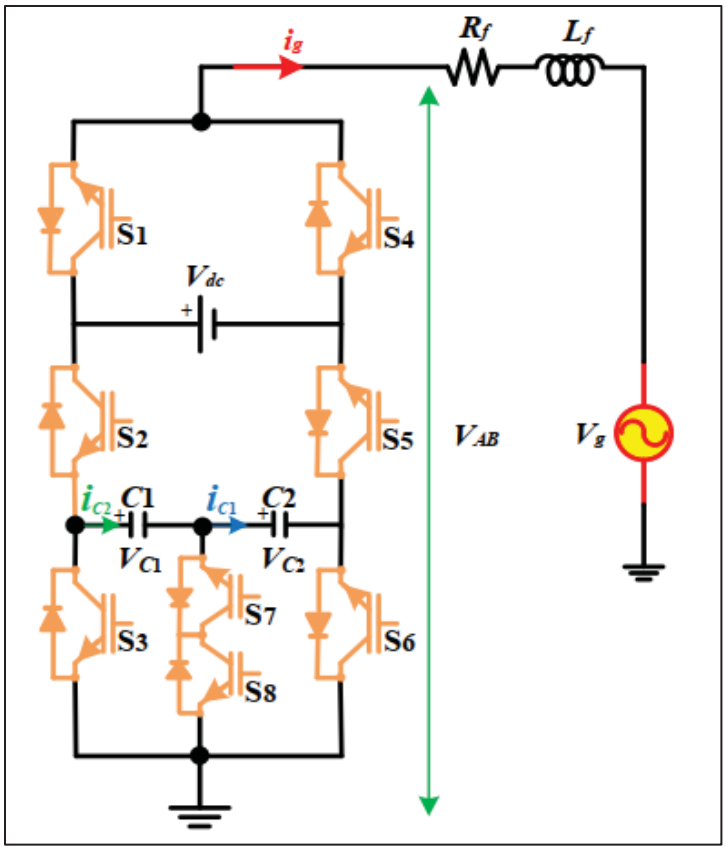

Figure 1.9 Grid-tied configuration of PEC9

The prominent feature of PEC9 is to balance the capacitors' voltages using redundant switching states. Considering the topology of PEC9 shown in Figure 1.9, the capacitors are horizontally extended inside a single auxiliary DC link to generate the redundant switching states. As a result, the DC-link voltage balancing problem is effectively simplified by charging and discharging the capacitors using the redundant switching vectors. Besides, only the auxiliary DC link voltage needs to be measured and balanced to half of the DC source while both capacitors are inherently regulated to one-quarter of the main DC link. Table 1.5 shows the voltage levels and switching states, including the redundant vectors for the PEC9 converter. This table also demonstrates the symmetrical charging and discharging cycles of the capacitors. Although PEC9 has been lately introduced, it has attained significant attention in the research field of renewable energy-distributed generators (Mehrasa, Babaie, Sharifzadeh, Bacha, & Al-Haddad, 2021; Babaie, Sharifzadeh, Mehrasa, Chouinard, & Al-Haddad, 2020, February; Mehrasa, Sharifzadeh, Babaie, Sebaaly, & Al-Haddad, 2020, February; Babaie,

Saeidi, Sharifzadeh, Hamadi, Al-Haddad, & Chandra, 2020, June), power quality (Sharifzadeh, Babaie, Mehrasa, Chouinard, & Al-Haddad, 2020, February; Sharifzadeh, Babaie, Sebaaly, Mehrasa, Chouinard, & Al-Haddad, 2020, October; Sharifzadeh, Babaie, Chouinard, & Al-Haddad, 2020, October), and active rectifiers (Babaie, & Al-Haddad, 2021, September; Guler et al., 2021, October).

Table 1.5 PEC9 switching characteristics: Switching vectors, voltage levels, and charging/discharging cycles (F=floating, C=charging, D=discharging)

States	S_1	S_2	S_3	S_4	S_5	S_6	S_7	S_8	V_{out}	C_1	C_2
1	1	0	0	0	1	1	0	0	$+V_{DC}$	F	F
2	1	0	0	0	1	0	1	1	$+V_{DC}-V_{C2}$	F	C
3	1	0	1	0	1	0	0	1	$+V_{DC}-V_{C1}-V_{C2}$	C	C
4	1	1	0	0	0	1	0	0	$V_{C1}+V_{C1}$	D	D
5	1	1	0	0	0	0	1	1	$+V_{C1}$	D	F
6	0	0	0	1	1	1	0	0	0	F	F
7	1	1	1	0	0	0	0	1	0	F	F
8	0	0	0	1	1	0	1	1	$-V_{C2}$	F	D
9	0	0	1	1	1	0	0	1	$-V_{C1}-V_{C2}$	D	D
10	0	1	0	1	0	1	0	0	$-V_{DC}+V_{C1}+V_{C2}$	C	C
11	0	1	0	1	0	0	1	1	$-V_{DC}+V_{C1}$	C	C
12	0	1	1	1	0	0	0	1	$-V_{DC}$	F	F

1.2.6 Voltage Level Multiplier Module

Compact MLC topologies like PUC and PEC are mainly suitable for single-phase applications due to using independent, isolated DC sources per phase. Voltage balancing is another design challenge of PUC and PEC, which is intensified as the number of levels increases. Voltage-level multiplier module (VLMM) is an affordable power electronics design concept that combines a conventional (mainly three-phase) MLC topology as the main converter with a compact MLC topology as a voltage multiplier module to enhance the resolution of the

multilevel output voltage waveform using minimum components count and voltage balancing difficulties (Abarzadeh, & Al-Haddad, 2019). Figure 1.10 illustrates a 21-level grid-tied VLMM converter based on ANPC and PUC5 converters. Regarding Figure 1.10, the VLMM-based converter is configured using a conventional ANPC as the first stage and a PUC5 as the multiplier module. The ANPC operates with the fundamental switching frequency and generates a symmetrical five-level voltage waveform with a peak amplitude equal to the principal DC source. The PUC5 generates an asymmetrical five-level voltage waveform with the switching frequency using the second dc source.

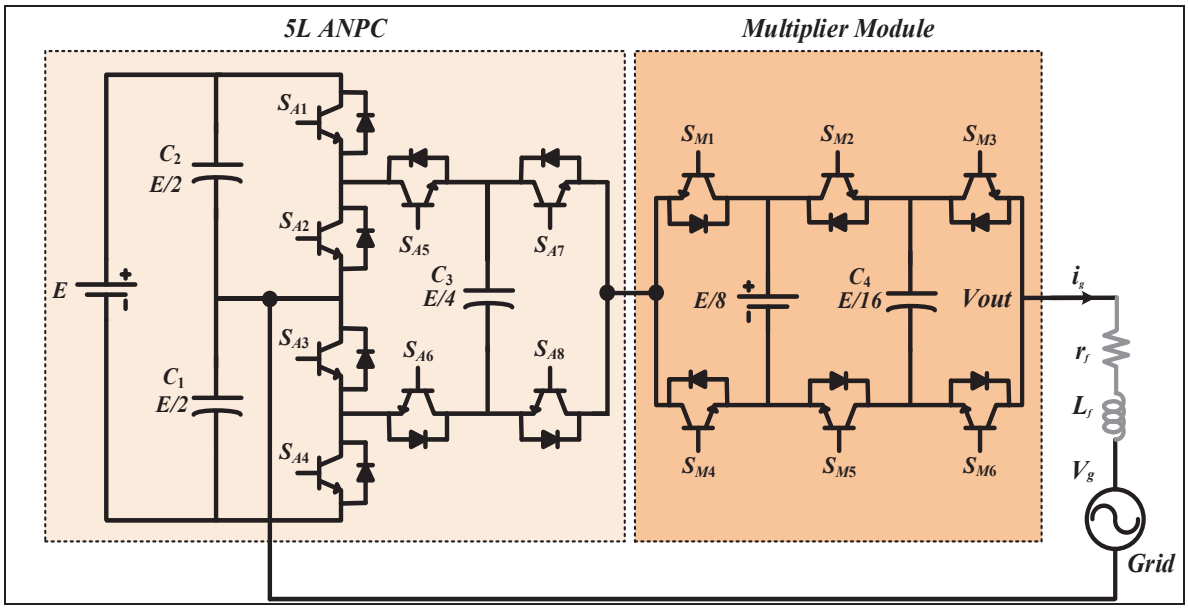

Figure 1.10 Single-phase, 21-level VLMM converter for grid-tied applications

In VLMM, the switching sequences of the main converter and the multiplier module are separately controlled through a decomposed modulator to simplify the control loop design complexity. Table 1.6 and Table 1.7 provide the switching states and voltage levels for the main converter as well as the multiplier module, respectively. Considering the symmetrical and asymmetrical voltage waveforms of the ANPC and PUC5, the VLMM-based converter can generate a staircase voltage waveform with a 21-level resolution. This topology can be developed using the first single DC source for three-phase applications; however, the second DC source used in the multiplier module is required in each phase without using an advanced

controller. To reduce the implementation costs, an advanced multi-objective controller is required to replace the second DC source with a floating capacitor.

Table 1.6 Switching vectors and voltage levels of the ANPC part

States	S_{A1}	S_{A3}	S_{A5}	S_{A7}	V_{out}	$C_{1,2}$	C_3
1	1	1	1	1	+E/2	Charging	Floating
2	1	1	1	0	+E/4	Charging	Charging
3	1	1	0	1	+E/4	Charging	Discharging
4	1	1	0	0	0	Floating	Floating
5	0	0	1	1	0	Floating	Floating
6	0	0	1	0	-E/4	Discharging	Discharging
7	0	0	0	1	-E/4	Discharging	Charging
8	0	0	0	0	-E/2	Discharging	Floating

Table 1.7 Switching vectors and voltage levels of the multiplier module

States	S_{M1}	S_{M2}	S_{M3}	V_{out}	C_4
1	0	1	1	+E/8	Floating
2	0	1	0	+E/16	Charging
3	0	0	1	+E/16	Discharging
4	1	1	1	0	Floating
5	0	0	0	0	Floating
6	1	1	0	-E/16	Discharging
7	1	0	1	-E/16	Charging
8	1	0	0	-E/8	Discharging

1.3 Linear, Nonlinear, and Intelligent Control Algorithms

Control theory has been extensively used in electrical engineering, mechanical engineering, chemistry, financial systems, medical science, and any other phenomenon, which can be

mathematically modeled as a system, including inputs, outputs, and dynamics. Using the control theory, systems are investigated from stability aspects to reach control laws or conditions that ensure the steadiness of state variables toward achieving desired objectives. Controllers can be designed in open-loop and closed-loop forms. The open-loop controllers are mainly applicable to inherently stable systems. Consequently, open-loop controllers do not need feedback from the system's state variables, which significantly reduces the implementation costs and complexity of the control unit. Even so, open-loop controllers are unsuitable for MLCs due to switching transitions, discontinued dynamics, environmental disturbances, and uncertainties. Accordingly, using closed-loop controllers is essential for unstable systems like MLCs. The general block diagram of a closed-loop controller is depicted in Figure 1.11; as demonstrated, the state variables are measured by several sensors and then applied to the controller as the feedback to calculate the proper control signal for actuators based on desired references.

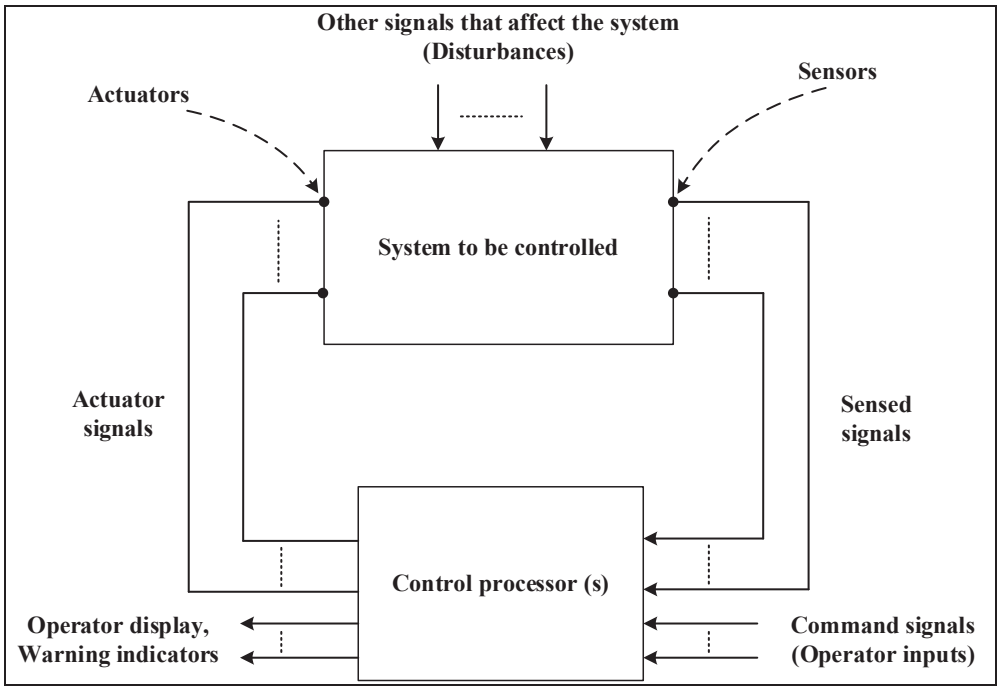

Figure 1.11 General structure of a closed-loop controller
Taken from Boyd (1991)

Linear, nonlinear, and intelligent control theories are the most common methods to analyze the stability of systems and design optimal controllers for tracking and regulation purposes. Linear controllers are designed based on an equilibrium point of the system where the linear performance is achieved. Despite simple design and implementation, there is no guarantee to preserve the stability of the controlled system when the system is out of the equilibrium point due to parametric variations and disturbances. As a result, to effectively use linear controllers, dynamics should be approximately explainable by simple mathematical models while uncertainties and disturbances are limited or observable. Proportional integral (PI), proportional integral derivative (PID), proportional resonant (PR), linear quadratic regulator (LQR), and linear quadratic gaussian (LQG) are some of the well-known linear control methods, which have been successfully implemented for various systems, including power electronics converters.

1.3.1 PID Control

Beyond question, PID is the most popular control strategy in the industry due to its simple structure and satisfactory performance. The conventional equation of a PID controller is presented in (1.2). According to (1.2), it is obvious that PID is a simple controller, in which the control factors k_p, k_i, and k_d can be adjusted without using an accurate mode of the system. The proportional term (k_p) is used to minimize $e(t)$; however, it causes a steady-state error in $y(t)$. To solve this issue, the integrator term (k_i) is added to (1.2); nonetheless, it makes some fluctuations, including undershoots and overshoots in $y(t)$. Accordingly, the derivative term is added to mitigate the undesired oscillations caused by the integrator. The derivative part is also sensitive to disturbance and causes instability or severe transients for systems with inherent oscillations like the converters. Thus, the derivative term should be removed from the control loop and a simple PI controller is tuned instead for power electronics systems.

$$\begin{cases} u(t) = k_p e(t) + k_i \int_0^t e(t)dt + k_d \dfrac{de(t)}{dt} \\ e(t) = r(t) - y(t) \end{cases} \tag{1.2}$$

where $r(t)$ and $y(t)$ are respectively the desired reference signal and the output of the system measured by a sensor or observer. The control factors should be adjusted regarding the required bandwidth of the controller to reach the desired objective with minimum transient effects in terms of settling time, overshoot, undershoot, and steady-state error. The control factors can be tuned based on Ziger-Nichol's method, metaheuristic algorithms, and even trial and error. Long settling time (delay), significant over/undershoots, sensitivity to high-frequency noises, narrow bandwidth, and complicated tuning can be considered as the disadvantages of PID.

1.3.2 Proportional Resonant Control

To apply infinite damping gain to the steady-state error in systems with natural oscillation, such as power converters, RR control is used instead of PI or PID. The non-ideal, filter-based structure of PR shown in (1.3) is highly compatible with power electronics applications because it empowers the control loop to mitigate harmonics besides tracking desired voltage and current references. With respect to this fact, PR control has been extensively employed in grid-tied converters, motor drives, and APFs to improve the power quality of converters.

$$\begin{cases} G_c(s) = k_p + \sum_{h=1}^{M} \dfrac{2k_i^h \omega_c s}{s^2 + 2\omega_c s + \left(\omega_0^h\right)^2} \\ h = 1,\ 3,\ 5,\ ...,\ 2n+1 \end{cases} \tag{1.3}$$

where ω_c, ω_0, k_p, k_i, and h are respectively the cutoff frequency, resonant frequency, the control factors, and harmonic order. The harmonic mitigation using PR control requires multiple resonant filters, which escalates the design difficulties of the control loop.

1.3.3 Linear Quadratic Regulator

LQR is another linear control method, which is designed using the control signal defined in (1.4) and the linear state-space model of the system. In (1.4), x is the state vector of the system, u is the control signal, and K=[k_1, k_2,…, k_n] is the LQR coefficients vector selected by the following cost function defined in (1.5).

$$u(t) = -Kx(t) \tag{1.4}$$

$$J = \int (\underline{x}^T Q \underline{x} + u^T R u) dt \tag{1.5}$$

where R is a symmetric positive constant matrix and Q represents a positive semi-definite constant matrix. After minimization of the cost function (J), matrix K is obtained below:

$$K = R^{-1} B^T P \tag{1.6}$$

In (1.6), Q and R are selected arbitrarily, B represents the system input matrix, A is the system matrix, and P is designated from the following equation:

$$A^T P + PA - PBR^{-1} B^T P + Q = 0 \tag{1.7}$$

From (1.4) to (1.7), one can be concluded that the optimal performance of LQR depends on the observability level of the state variable and the accuracy of the state-space model. As a result, for systems polluted by uncertainties, designing the LQR is exhausting.

Despite linear control methods, nonlinear dynamics, uncertainties, disturbances, and variable parameters can be considered and compensated in nonlinear control strategies. Indeed, nonlinear control methods, such as SMC, MPC, backstopping, and Lyapunov control, are designed based on modern control theory, which studies the nonlinear behavior of systems

through state-space modeling. Therefore, nonlinear control algorithms can be considered a promising alternative for linear rivals since the modeling inaccuracy can be effectively compensated through advanced stability analysis or adaptive laws.

1.3.4 Sliding Mode Control

Sliding mode is a robust, variable structure control technique that ensures stability and fast dynamic performance by involving uncertainties and environmental disturbances in the control law (Babaie, Rahmani, & Rezaie, 2019). SMC theory aims to define an imaginary surface and force the error signals to slide along it so that the system dynamics or phase trajectories track desired references. The design of SMC includes two steps; first, defining a sliding surface and then determining a proper control law based on the dynamic equations of the system. The general form of the sliding surface is presented in (1.8).

$$S(x) = P^T x = \sum_{i=1}^{n} \mu_i x_i(t) = \mu_1 x_1(t) + \ldots + \mu_n x_n(t) \tag{1.8}$$

where $x=[x_1, x_2,\ldots, x_n]^T$, and $P=[\mu_1, \mu_2,\ldots, \mu_n]^T$ are the state variables of the system and the sliding gains, respectively. The sliding factors can be constant or variable depending on the control design requirements. In the second step, an appropriate control law is achieved based on the Lyapunov theory to guarantee system stability and minimum steady-state error. The overall structure of the control law (u_g), including the continuous (u_{eq}) and discontinuous (u_d) terms, is shown (1.9).

$$u_g(t) = u_{eq}(t) + u_d(t) \tag{1.9}$$

The equivalent term is obtained from the system state-space model and is used to maintain the system phase trajectories on the sliding surface. The general form of the equivalent control is as below:

$$u_{eq}(t) = -\left(p^T g(x)\right)^{-1} p^T f(x) \tag{1.10}$$

where $f(x)$ and $g(x)$ as two nonlinear functions describe the dynamic behavior of the system. The nonlinear equations are defined in (1.11) in which $d(x)$ is an external disturbance bounded by $\tilde{d}$.

$$\begin{cases} \dot{x} = f(x) + g(x)u + d(x) \\ \|d(x)\| \le \tilde{d} \end{cases} \tag{1.11}$$

The discontinuous control term described as a high-frequency function in (1.12) is considered to conduct the system phase trajectories on the sliding surface.

$$u_d(t) = -ksign(s) \tag{1.12}$$

where k is a positive constant control factor. The sliding control law can be rewritten using (1.10) and (1.12) as below:

$$u_g(t) = -\left(p^T g(x)\right)^{-1} p^T f(x) - ksign(s) \tag{1.13}$$

The conventional SMC suffers from a chattering effect, which is generated by the sign function of the discontinuous control law. The chattering known as high-frequency oscillations around the sliding surface stimulates the high-order dynamics of the system, which are neglected in stability analysis. Consequently, chattering degrades the control performance and stability of the control loop while reducing the actuators' lifetime. Using a saturation function instead of a sign helps to mitigate the chattering at the cost of increased steady-state error. Alternatively, second-order SMC algorithms, including twisting and super-twisting, can effectively compensate for the chattering effects.

1.3.5 Lyapunov Control

Besides stability analysis, Lyapunov theory can be used to design a robust controller. Lyapunov control theory aims to find an appropriate control law to ensure system stability and track control objectives, concurrently. To this end, a system with a general form presented in (1.14) is considered; this system may be subject to uncertainties and environmental disturbances.

$$\begin{cases} \dot{x} = f(x,u),\ x \in R^n \\ f(0,0) = 0 \end{cases} \tag{1.14}$$

where x is the system's state variable and u is the input. To design the proper control law for u, a positive definite Lyapunov function ($V(x)$) in the form of V: $R^n \rightarrow R$ is first defined as below:

$$V(x) > 0,\ \forall\ x \neq 0,\quad V(0) = 0 \tag{1.15}$$

Afterward, the derivative of the Lyapunov function is calculated using (1.16) to obtain the control law.

$$\nabla V(x).f(x,u) = \beta(x) \tag{1.16}$$

where ∇ calculates the gradient of $V(x)$ on $f(x, u)$. $\beta(x)$ as a negative definite function should meet the Lyapunov stability criteria besides reaching desired control performance. Designing the control law using (1.16) provides global asymptotic stability for the system; nonetheless, it does not guarantee perfect control performance. Accordingly, $\beta(x)$ should be selected adequately since it crucially affects control performance.

1.3.6 Backstepping Control

Backstepping is a robust control algorithm, which is formulated based on the Lyapunov stability theory. Backstepping is structurally similar to the Lyapunov controller discussed previously. Even so, backstepping is designed based on two or more Lyapunov functions to control multiple state variables through a single control signal. Considering the underactuated structure of power electronic converters, backstepping is an ideal controller to apply direct control on the state variables, which cannot be directly controlled through the available inputs of the system. e.g., in (Babaie, & Al-Haddad, 2021, June) backstepping was used to apply direct control on the auxiliary DC link of a grid-tied PEC9 inverter. Regarding the implementation results provided in (Babaie, & Al-Haddad, 2021, June), backstepping can effectively contribute to reducing the size of floating capacitors in compact MLCs. Nevertheless, finding multiple Lyapunov functions is a sophisticated, time-consuming process because the stability condition and dynamic response should be satisfied concurrently.

1.3.7 Model Predictive Control

Model predictive control is a nonlinear algorithm with the unique ability of multi-objective control on the system state variables. The multi-objective control is fulfilled through a cost function containing the state variables and weighting factors. Because of the multi-objective control performance, MPC has been extensively involved in different control problems, including power electronics (Vazquez et al., 2014). Finite control set MPC (FCSMPC) is a discrete, straightforward type of MPC suitable for variable structure systems with limited control actions, such as power converters. Designing an FCSMPC for converters is realized in four steps as follows: 1) determining all possible switching states, 2) defining a discrete model of the converter regarding the control targets, 3) designing the cost function and tuning its weighting factors, 4) evaluating all possible switching states in the cost function to select the best one in each sample period. The cost function, as well as the block diagram of FCSMPC, are respectively depicted in (1.17) and Figure 1.12.

$$G = \lambda_1\left(x_1(k+1) - x_1^*(k+1)\right) + \lambda_2\left(x_2(k+1) - x_2^*(k+1)\right) + \ldots \\ + \lambda_{n-1}\left(x_{n-1}(k+1) - x_{n-1}^*(k+1)\right) + \lambda_n\left(x_n(k+1) - x_n^*(k+1)\right) \quad (1.17)$$

where λ_n is the weighting factor of the cost function; $x_n(k+1)$ and $x^*_n(k+1)$ are the predicted state variable and its desired reference for the nth control object, respectively.

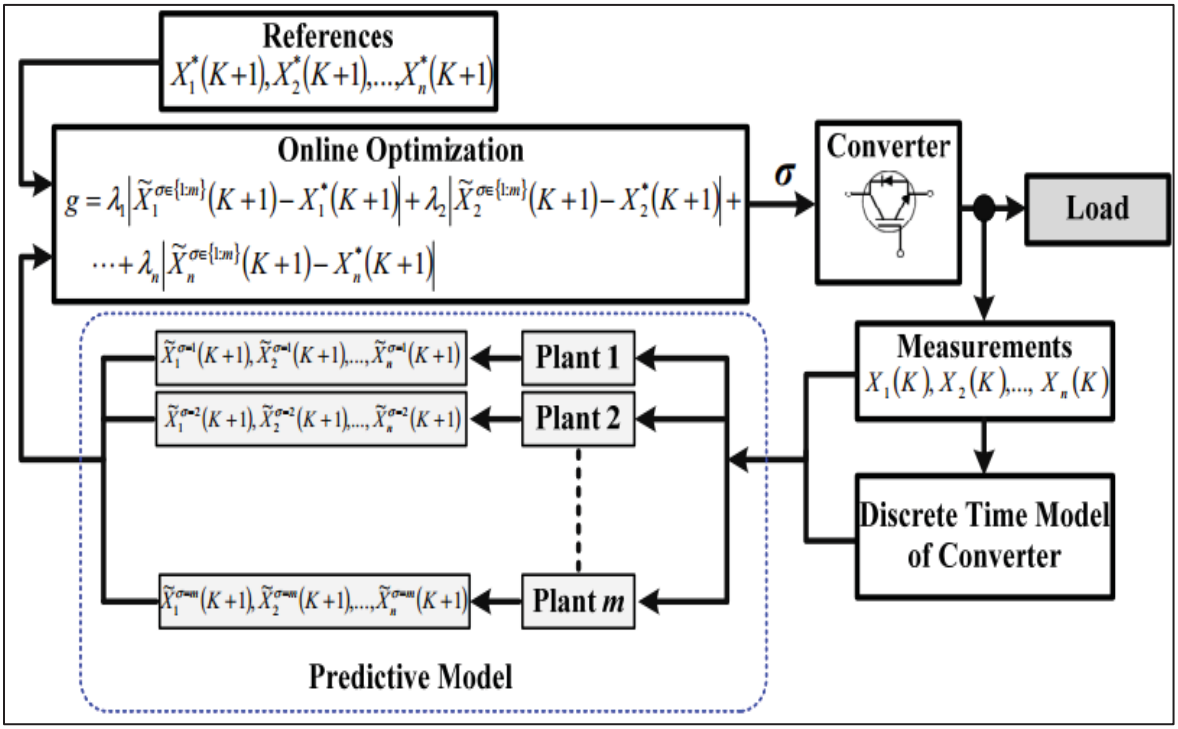

Figure 1.12 General structure of FCSMPC used in power electronic applications
Taken from Metry (2016)

Despite fast dynamic response and multi-objective control capability, conventional MPC suffers from several drawbacks, such as sensitivity to model accuracy, heavy computational burden, and tiresome tuning process of the weighing factors. Voltage stress and variable switching frequency are other side-effects of using conventional MPC in power electronics control problems.

1.3.8 Intelligent Control

The technology trends demonstrate rapidly increasing attention to Artificial Intelligence (AI) in control applications due to its high performance and unique features (Qashqai et al., 2019; Babaie, Sebaaly, Sharifzadeh, Kanaan, & Al-Haddad, 2019, February). Intelligent control methods formed based on fuzzy and Artificial Neural Networks (ANN) led to novel model-free robust controllers, which have been vastly applied to power electronics, robotics, chemistry, and mechanic systems (Ahmadi et al., 2020; Bose et al., 2020; Ahmadi et al, 2021). These controllers are designed based on predefined training data or based on expert knowledge. Nonlinear modeling, fast transient response, multi-objective control, robust performance, and simple development to use in multivariable systems are the prominent advantages of intelligent controllers. A classic ANN is built by several artificial neurons organized in the input, hidden, and output layers. In an ANN controller, the measured signals are applied to the input layer and processed in the hidden layer; the corresponding decisions, as the control signal, appear in the output layer. The number of neurons in each layer, especially the hidden one, should be determined regarding the complexity of the control problem. Neuron deficiency results in weak performance while using too many neurons increases the implementation expenses and causes overtraining issues. Multilayer Perceptron (MLP), Hopfield, radial basis function (RBF), support vector machines (SVM), self-organizing map (SOM), and learning vector quantization (LVQ) are some of the prevalent ANN structures, which are practically used in different applications, including power electronics. Figure 1.13 illustrates the generalized structure of an MPL. In this figure, $[x_1, x_2,\ldots, x_k]$ is the input vector, w^p_{ij} is the weighting factor from the ith input to the jth neuron in the pth layer. N_n and N_r are respectively the hidden and output neurons. $[y_1, y_2,\ldots, y_r]$ is the output vector and $[b_1, b_2,\ldots, b_n]$ is the bias vector for all neurons.

Since the weighting factors and biases determine the behavior of the neural network, a proper training strategy is required to achieve the desired performance. To this end, training strategies, including supervised, unsupervised, and reinforcement learning, are available (Babaie, Mehrasa, Sharifzadeh, & Al-Haddad, 2021). Supervised learning is the most popular strategy among all, which is designed based on a classic or metaheuristic optimization algorithm and

training data. Because of data acquisition, supervised training is offline and easy to implement (Babaie, Sharifzadeh, & Al-Haddad, 2020, August). Even so, data acquisition is an exhausting process since multiple test scenarios should be considered to collect appropriate data from a reliable reference model (Dragičević, & Novak, 2018). Unsupervised training methods are much faster and more accurate than supervised ones because data acquisition is not required. Unsupervised methods reach the optimal performance by online evaluation of the ANN in the control loop through a cost function minimized by optimization algorithms. Reinforcement learning is indeed a hybrid algorithm that benefits from the advantages of both previous methods with a cost of more complexity.

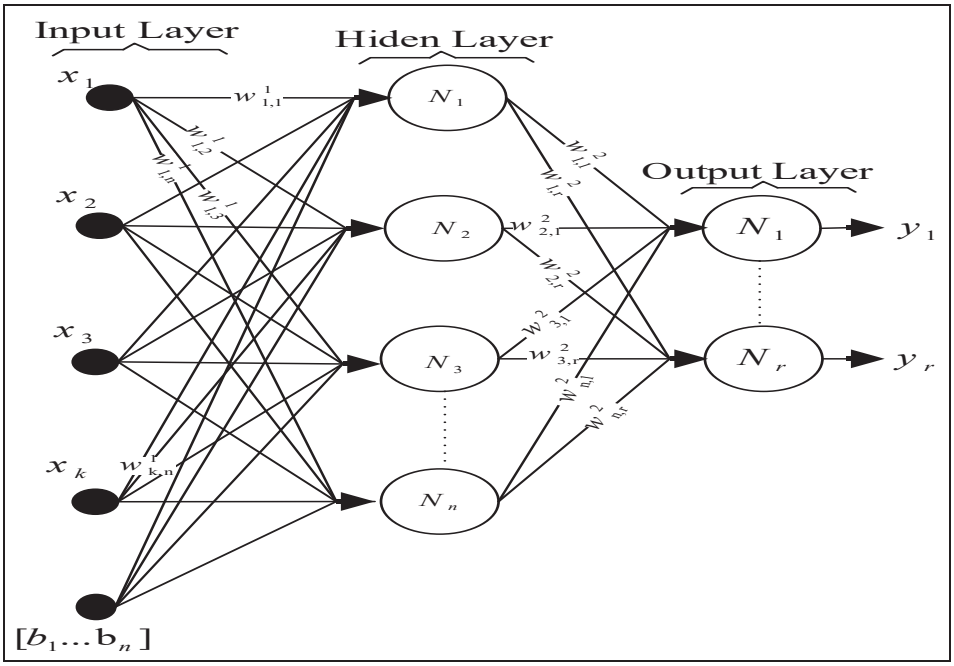

Figure 1.13 Typical structure of multilayer Perceptron neural network

Fuzzy control theory is another intelligent method widely used in control problems, including power electronics (Hou et al., 2021). Fuzzy is ideal for implementing human knowledge or expert experience in diverse problems like modeling, control, identification, and classification, regardless of the system's complexity. Figure 1.14 presents a fuzzy system containing three units: the so-called fuzzifier, fuzzy inference engine, and defuzzifier. The first block converts the numerical input signals to linguistic values; the fuzzy inference engine then evaluates the

converted data to make a proper decision. The inference engine uses a reasoning bloke to generate decisions on the input signals based on several linguistic IF-THEN fuzzy rules. The third block translates the linguistic values generated by the inference system into numerical quantities, which can be used to stimulate actuators or print on monitors. Takagi-Sugeno-Kang (TSK), Mamdani, and type-2 are three types of fuzzy systems available to design an intelligent controller. TSK is a simple fuzzy system in which the defuzzifier is designed using constant values. In a Mamdani type, the defuzzifier is designed using fuzzy membership functions. Accordingly, the output signals change smoothly while they experience a semi-discrete transition in a TSK model. Similar to the Mamdani version, the type-2 fuzzy benefits fuzzy membership functions on both input and output sides; however, the membership functions have dimensions to compensate for uncertainties (Chaoui et al., 2017).

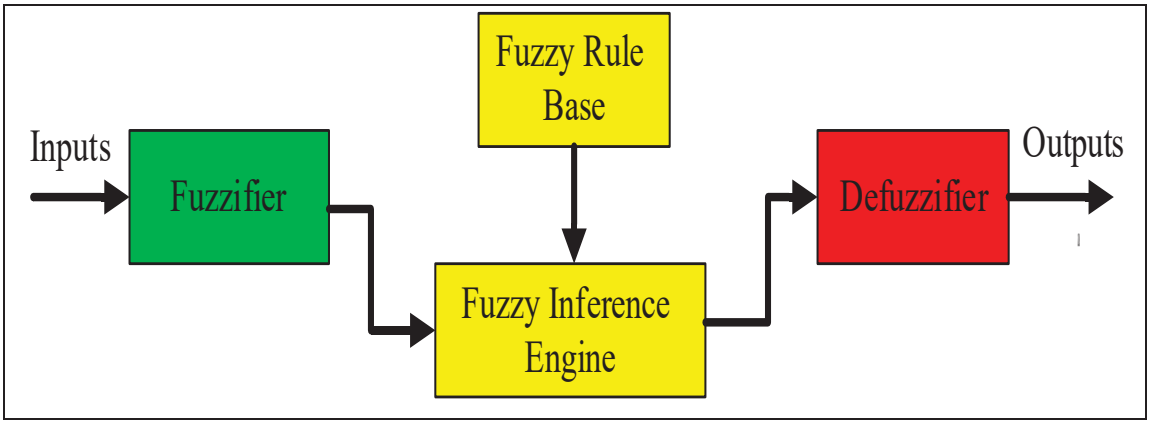

Figure 1.14 General structure of a fuzzy system

Unfortunately, there is a lack of training strategy to design a fuzzy controller despite its capability to address various control problems. Subsequently, the performance of a fuzzy controller is directly affected by the training approach, the number of membership functions, and the rules, which need to be defined based on expert knowledge. Combination of ANN and fuzzy leads to a new generation of intelligent controllers, the so-called adaptive neuro-fuzzy inference system (ANFIS), which benefits the advanced training strategies of ANN to design optimal fuzzy systems (García et al., 2013).

1.4 State of the Art

Linear, nonlinear, and intelligent control algorithms have been vastly used in power electronics converters to address the controllability and stability challenges. In this thesis, advanced control techniques applied to multilevel converters are particularly discussed. Neutral point clamped, cascaded H-bridge, packed U-cell, and packed E-cell are the main MLC topologies regarded as case studies due to their popularity and the variety of applications. Stand-alone and grid-connected modes of operation of the converters are considered to select, study, and develop the control algorithms. Grid-tied current synchronization, active/reactive power control, common mode voltage (CMV) suppression, harmonic mitigation, voltage stress reduction, switching frequency regulation, and DC link voltage balancing are the principal control objectives considered to assess the performance of the controllers.

Three-phase NPC, as a pioneer multilevel topology, has been successfully used for different industrial and domestic applications, such as active rectifiers (Bendre, & Venkataramanan, 2006), motor derives (Zhang, Zhu, Zhao, Xu, & Dorrell, 2010), renewable energy integration (Teymour, Sutanto, Muttaqi, & Ciufo, 2014), shunt active power filters (Benazza, & Ouadi, 2016, November), and STATCOMs (Zhou, & Cheng, 2019). A first-order SMC was designed in (Sebaaly, Vahedi, Kanaan, Moubayed, & Al-Haddad, 2016b) to control a three-phase grid-connected NPC inverter. The conventional SMC was modified based on Gao's reaching law to mitigate the chattering frequency. Besides the SMC, an auxiliary PI controller was also tuned and employed to balance the capacitors' voltages. However, the PI controller increases the tuning difficulties and challenges the stability of the SMC controller, as it operates in parallel. In another research work, the DC link voltage balancing was addressed through SVPWM to remove the PI controller (Sebaaly, Vahedi, Kanaan, Moubayed, & Al-Haddad, 2016a). Even though the hybrid SMC-PI and SMC-SVPWM methods meet the control objectives, the experimental results in (Sebaaly, Vahedi, Kanaan, Moubayed, & Al-Haddad, 2016a) and (Sebaaly, Vahedi, Kanaan, Moubayed, & Al-Haddad, 2016b) show a significant level of chattering, which can intensify voltage stress and cause variable switching frequency. In addition, CMV mitigation was ignored in (Sebaaly, Vahedi, Kanaan, Moubayed, & Al-

Haddad, 2016b; Sebaaly, Vahedi, Kanaan, Moubayed, & Al-Haddad, 2016a) due to the multi-objective control limitations of SMC-PI and SMC-SVPWM. Several MPC algorithms were also reported in the literature to control NPC and ANPC for renewable energy integration (Yaramasu et al., 2013), three-phase active rectifiers (Gao et al., 2018, May; Barros et al., 2012), motor control (Geyer et al., 2012), and grid-connected inverters (Donoso et al., 2017). Compared with the SMC and PI-SMC, MPC, as a multi-objective controller, precisely tracks the reference current, regulates the DC link voltages, and mitigates CMV with faster dynamic performance. Considering the significant number of switching vectors, which need to be evaluated for NPC and ANPC per sampling period, the conventional MPC suffers from computational burden (Vazquez et al., 2014; He et al., 2022). As a result, a relatively expensive microcontroller or processor is required to compensate for the computational delay caused by MPC. Tedious tuning of the weighting factors is another design challenge of MPC, which was ignored in (Yaramasu et al., 2013; Gao et al., 2018, May; Geyer et al., 2012). To address the tuning difficulties, MPC was combined with ANN to estimate the weighting factors online (Machado et al., 2017). However, the accuracy of the supervised training methods applied to the ANN estimators relies on numerous time-consuming data acquisition scenarios. ANN as a controller was also used to control an NPC-based active power filter (Salim et al., 2011), a three-phase NPC rectifier (Langer, Bhat, & Agarwal, 2014), and a grid-tied inverter (Babaie, Sharifzadeh, & Al-Haddad, 2020, August). The ANN controllers were designed based on MLP topology and trained by supervised methods (Langer, Bhat, & Agarwal, 2014; Salim et al., 2011). The corresponding experimental and simulation results illustrate considerable amounts of THD, CMV, and voltage stress because of the non-optimized performance of the ANN controllers. Fuzzy control theory as an intelligent technique was also used for various applications of NPC, including APFs (Saad, & Zellouma, 2009), renewable energy integration (Altin, & Ozdemir, 2013), motor derives (del Toro et al., 2004), and rectifiers (Hamed et al., 2015). e.g., two Mamdani-based fuzzy controllers were designed to track the reference current and balance the capacitors' voltages in an NPC-based APF (Saad, & Zellouma, 2009). Model-free design and robustness were noted as promising advantages of the fuzzy controllers. Nonetheless, the fuzzy controllers increase hardware complexity. To improve the dynamic response of PI control, a fuzzy estimator was introduced by (Altin, & Ozdemir, 2013); the

proposed fuzzy estimator adjusts the inverter reference current so that the maximum power point (MPP) is tracked while the PV-based NPC inverter injects active power into the grid. Model-based adaptive direct power control (MBADPC) is a nonlinear adaptive controller proposed by (Hamed et al., 2015) to control a three-phase bidirectional NPC converter. Although MBADPC involves grid uncertainties in the control equations, the resulting controller generates variable switching frequency with adverse impacts on the switching loss and the stability of the filter. Backstepping is a robust control method proposed by (Benazza, & Ouadi, 2016, November) to control the harmonic current as well as the neutral point current of a three-phase NPC-based APF. A detailed review by (Benazza, & Ouadi, 2016, November) demonstrates a significant level of complexity which can be compared to more straightforward control strategies with similar performance.

Considering the cascaded structure of DC links in CHB, using advanced controllers is crucial for grid-tied applications. In order to enhance the dynamic performance of a CHB-based three-phase STATCOM, an MPL neural network trained by a supervised strategy was used to adapt the PI gains with respect to the grid voltage fluctuations (Reddy et al., 2012). Grid-connected operation is another industrial application of CHB in which an online Selective Harmonic Elimination (SHE) modulator based on MLP was reported (Aravind, & Alexander, 2013, April). Since the SHE-MLP modulator used conventional SHE to generate the necessary training data, its performance directly depends on the accuracy of the data acquisition scenarios and the reference modulator. A Fuzzy controller with several inputs and outputs was developed by (Farivar, Agelidis, & Hredzak, 2014, March) to balance the capacitors voltage of a grid-connected CHB inverter. The proposed fuzzy controller can be modified to control CHB inverters with higher voltage resolution. However, this requires more expensive hardware since the number of membership functions and fuzzy rules exponentially increases. Alternatively, an optimized Mamdani-based Fuzzy controller was introduced by (VijayaSamundeeswari, & Gopinath, 2017, March) to adjust the power flow of a fifteen-level CHB inverter for a stand-alone application. The literature review demonstrates the superiority of MPC over previously discussed control methods to address the controllability challenges of high-resolution CHBs for different applications. e.g., a conventional MPC was formulated to control a 27-level CHB

inverter applied to a three-phase induction motor (Perez, Cortés, & Rodríguez, 2008). A modified MPC was proposed by (Cortes et al., 2010) to reduce the number of switching vectors, which need to be evaluated during each sampling period. Therefore, the computational delay of conventional MPC can be compensated without affecting the control performance. In addition, the presented simulation and experimental results in (Cortes et al., 2010) prove that CMV has been remarkably suppressed thanks to the optimal multi-objective control performance of the new MPC. Even so, the modified MPC is restricted to three-phase applications. Regardless of the chattering issue, SMC has been used for grid-tied applications of CHB to reach fast dynamic performance and ensure system stability with less complexity than an MPC algorithm (Wu et al., 2013; Negroni et al., 2010, March). To meet the multi-objective control requirement of a grid-connected, capacitor-based CHB inverter, SMC was combined with a feedback linearization algorithm to control the grid current and the capacitors' voltages concurrently (Negroni et al., 2010, March). Nonetheless, the examination results reveal that the linear feedback causes considerable overshoots and undershoots in currents and voltages of the inverter during dynamic operation modes.

Because of the compact structure, PUC has drawn much attention from industry and academia, especially for single-phase applications. Moreover, it has been considered a benchmark to evaluate the performance of advanced controllers from the aspects of stability, multi-objective control performance, robustness, and dynamic response (Vahedi, Labbé, & Al-Haddad, 2015; Sebaaly, Vahedi, Kanaan, & Al-Haddad, 2018; Trabelsi, Alquennah, & Vahedi, 2022; Trabelsi, Vahedi, & Abu-Rub, 2021). The reliability, compatibility, and efficiency of PUC have been investigated for different applications, such as single-phase or three-phase inverters to supply the grid and stand-alone loads (Vahedi, & Al-Haddad, 2015; Metri, Vahedi, Kanaan, & Al-Haddad, 2016), PV-based distributed generators (Mishra, Singh, Yadav, & Tariq, 2023), single-phase APFs (Vahedi, Shojaei, Dessaint, & Al-Haddad, 2017), single-phase rectifiers (Babaie, Mehrasa, Sharifzadeh, & Al-Haddad, 2021), electric springs (Kaymanesh, & Chandra, 2020), and STATCOMs (Kaymanesh, Chandra, & Al-Haddad, 2021b). The control trend of PUC has begun with PI due to structural simplicity (Vahedi, Labbé, & Al-Haddad, 2015). However, the literature review reveals that the application of PI is restricted to PUC5,

MPC5, and PUC9 since the auxiliary DC links can be controlled through the redundant switching vectors. LQR is another linear controller reported in the literate for a grid-tied PUC5 inverter (Arab, Vahedi, & Al-Haddad, 2019). In comparison with linear controllers applied to PUC and MPUC, the intelligent rivals, including ANN (Babaie, Mehrasa, Sharifzadeh, & Al-Haddad, 2021), fuzzy (Babaie, Sharifzadeh, Mehrasa, Baillargeon, & Al-Haddad, 2018, October), and ANFIS (Babaie, Sharifzadeh, Mehrasa, Chouinard, & Al-Haddad, 2019, October), demonstrate much better dynamic performance and less sensitivity to uncertainties and disturbances. Even so, linear and intelligent control algorithms were not reported for grid-tied PUC7 and MPUC7, to the best of the author's knowledge. Accordingly, PUC7 and MPUC7, as the most challenging topologies of PUC, demand an advanced multi-objective control strategy to achieve maximum efficiency and guarantee the stability of the auxiliary DC link. Referring to the state of the art of PUC7 and MPUC7, MPC-based control algorithms like finite control set MPC (FCSMPC) (Metri, Vahedi, Kanaan, & Al-Haddad, 2016; Babaie, Mehrasa, Sharifzadeh, & Al-Haddad, 2019, September), SMC-MPC (Makhamreh, Trabelsi, Kükrer, & Abu-Rub, 2019), and Lyapunov-MPC (Makhamreh, Trabelsi, Kükrer, & Abu-Rub, 2020) are the control algorithms, which can handle the voltage balancing issue in the grid-connected mode of operation. However, the proposed MPC-based control algorithms cause negative impacts on the current harmonic profile, the volume of the passive components, switching loss, and voltage stress.

Although nine-level PEC has one more capacitor in the auxiliary DC link, it is more controllable than seven-level PUC because of its redundant switching vectors. As a result, the linear control of the nine-level PEC is feasible for grid-connected applications (Sharifzadeh, & Al-Haddad, 2019). However, to achieve a lower level of voltage ripple, faster dynamic response, minimum transient effects, and more stability margin, advanced control algorithms, such as Lyapunov (Babaie, Sharifzadeh, Mehrasa, & Al-Haddad, 2020, March), SMC (Babaie, Sharifzadeh, Mehrasa, & Al-Haddad, 2020, September), passivity control (Mehrasa, Babaie, Zafari, & Al-Haddad, 2021), backstepping (Babaie, & Al-Haddad, 2021, June), MPC (Sebaaly, Sharifzadeh, Kanaan, & Al-Haddad, 2020; Babaie, Sharifzadeh, & Al-Haddad, 2020, October), and Intelligent Control (Babaie, & Al-Haddad, 2020, October; Babaie, Mehrasa,

Sharifzadeh, Melis, & Al-Haddad, 2020, June; Babaie, & Al-Haddad, 2021, October) have been recommended.

It is worth mentioning that elaborated literature reviews on the advanced control of PUC, PEC, and NPC are provided in the following chapters since these topologies have been selected as case studies to develop and evaluate several novel advanced controllers in this thesis.

1.5 Conclusion

The preliminary literature review provided in this chapter demonstrates the growing penetration of MLCs in the most strategic power electronic-related industries, including smart grids, renewable energy-based distributed generators, motor drives, power quality ancillary services, and EVs. Considering the complex structure of MLCs, the impact of control on their controllability, stability, and efficiency is announced as crucial. e.g., PUC and MPUC offer the most affordable seven-level bidirectional converters for single-phase applications; even so, without advanced multi-objective control, their application is limited to supplying stand-alone loads because of the voltage-balancing problem. Accordingly, nowadays, researchers have concentrated more on control aspects than topology to ensure the optimal performance of MLCs in the future. Figure 1.15 summarizes the control algorithms applied to the selected MLC topologies for the mentioned strategic applications. In summary, model-based hybrid nonlinear control algorithms are more compatible with the variable structure of MLCs than conventional linear, nonlinear, and intelligent rivals. In other words, emerging hybrid strategies like intelligent-predictive algorithms can apply the most effective multi-objective control to MLCs regardless of the application.; however, conventional design or training of the hybrid controllers becomes extremely time-consuming and even infeasible as the number of objectives increases. Therefore, hybridizing the advanced control methods toward achieving an optimal multi-objective, robust control algorithm is quite challenging and needs further research and development.

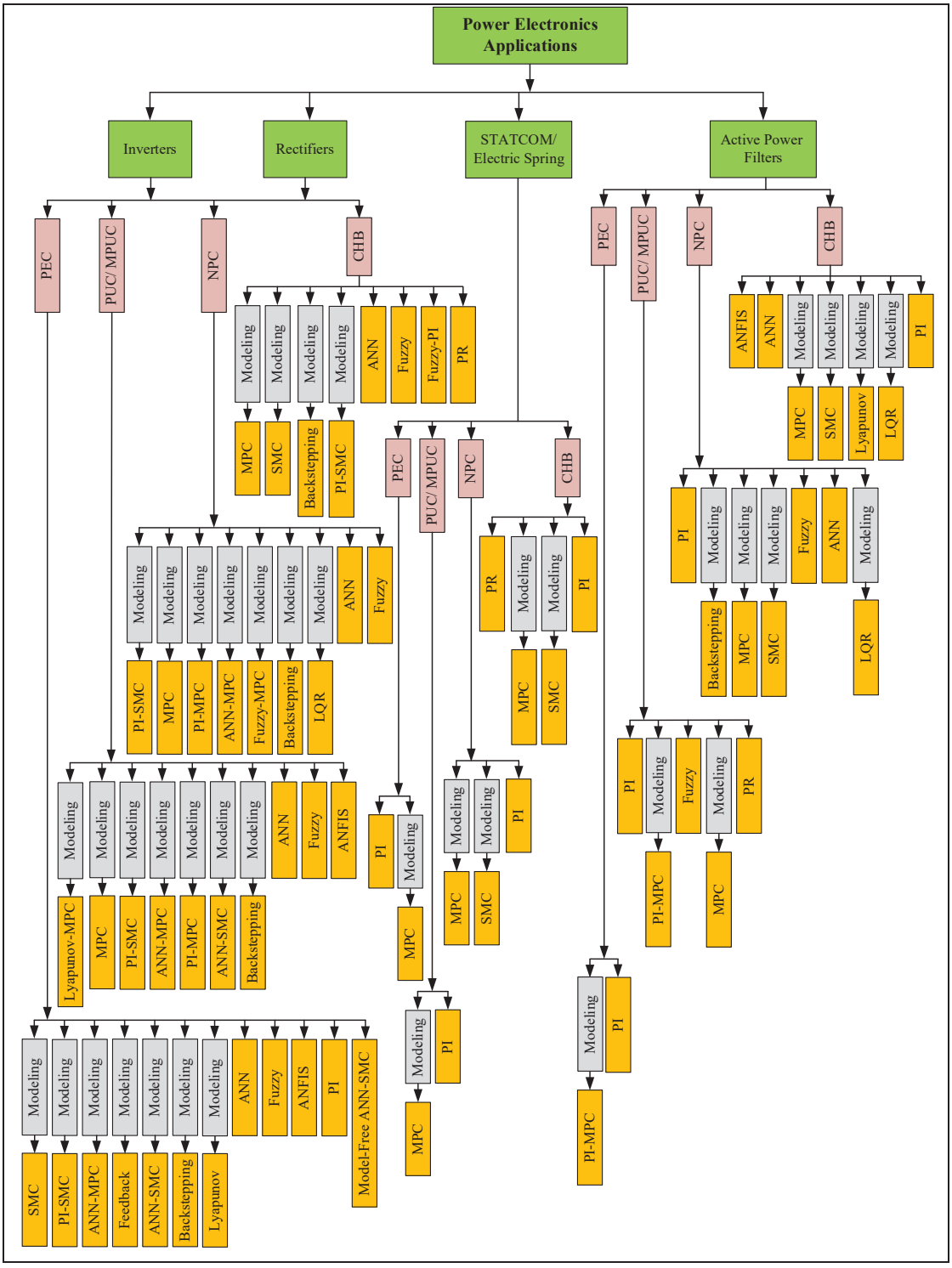

Figure 1.15 Summary of linear and advanced control algorithms applied to MLCs

CHAPTER 2

Switching-Based Optimized Sliding Mode Control for Capacitor Self-Voltage Balancing Operation of Seven-Level PUC Inverter

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Abstract

Seven-level Packed U-Cell (PUC7) is one of the most cost-effective, compact multilevel converter topologies for single-phase applications. Even so, this converter is severely challenged by the capacitor voltage balancing in such a way an additional voltage controller as the outer loop cascaded to an inner current control loop is required to maintain its stability. The controllability of PUC7 is much more problematic in the grid-tied mode due to the dynamic behavior of the grid, unknown disturbances, and uncertainties. This paper proposes a novel current-based optimized sliding mode control algorithm (OSMC) to guarantee the stability of the PUC7 and regulate its capacitor's voltage for grid-connected and stand-alone applications. Surprisingly, by optimizing the OSMC control factor using a visual-based optimization (VBO) method, the PUC7 switching operation is appropriately controlled so that self-balancing of the capacitor's voltage becomes feasible without involving the sensor-based voltage controller. An adaptive control law is also proposed for the self-tuning of the reference current to track the load and DC source variations in the stand-alone mode. In the end, experimental and simulation results demonstrate the promising performance of the proposed OSMC algorithm for sensorless control of the floating capacitor, accurately tracking the reference current, and ensuring the stability of the converter.

2.1 Introduction

Nowadays, multilevel converters are widely used in various industrial and domestic applications, such as renewable energy integration, electric vehicles, uninterruptable power supply, and power quality regulators (Abu-Rub, et al., 2010; Kouro, et al., 2010). Even though modeling and control of conventional two-level converters are straightforward, they cause harmonic pollution, switching loss, and voltage stress; subsequently, they increase the implementation and maintenance costs, demand large volume passive components, and restrict the nominal power of the converter (Rodriguez, Lai, & Peng, 2002). Thus, it is necessary to design a high-order passive filter for two-level converters; using the filter comes with harmonic disorders, voltage stability issues, and bandwidth limitations.

Multilevel converters, especially single DC-source ones, are a sustainable solution to compensate for the problems caused by conventional two-level converters without using extra high-order filters (Gupta et al., 2015; Franquelo et al., 2008). The rapid penetration of MLCs in the industry started with the three-level Neutral Point Clamped (NPC), recognized as one of the most successful MLC topologies in the literature (Nabae et al., 1981). NPC is configured by a single DC source, two capacitors in the DC link, two diodes, and four switches per phase. This topology can be used for single-phase or multi-phase applications in both inverter and rectifier modes of operation (Rodriguez et al., 2009). NPC is able to generate more than three voltage levels per phase; nonetheless, its cost and complexity to design a proper controller dramatically increase (Rodríguez et al., 2007). Despite NPC, a flying capacitor (FC) topology is constructed based on capacitive loops instead of diode loops to compromise between voltage resolution and component count (Wang, Zheng, Fan, Xu, & Li, 2018). Voltage balancing of the floating capacitors is the greatest challenge of FC, which limits its voltage resolution. Concerning the voltage generation limitations of the previous MLCs, PUC was introduced by (Ounejjar, Al-Haddad, & Gregoire, 2010) as a novel bidirectional compact MLC topology to design cost-effective converters with the maximum possible voltage resolution. Accordingly, PUC provides prominent advantages, such as minimum components count and higher voltage resolutions, including five-level (Sharifzadeh, Vahedi, & Al-Haddad, 2018), seven-level

(Vahedi, & Al-Haddad, 2015), nine-level (Ounejjar, & Al-Haddad, 2018, October), 15-level (Trabelsi, Bayhan, Refaat, Abu-Rub, & Ben-Brahim, 2016, September), 23-level (Sorto-Ventura, Abarzadeh, Al-Haddad, & Dessaint, 2020), 31-level (Babaie, & Al-Haddad, 2022, September), and 49-level (Meraj, Rahman, Iqbal, Tariq, Lodi, & Ben-Brahim, 2019). PUC has been used in various applications, including single-phase and three phases grid-connected and stand-alone converters (Vahedi, Labbé, & Al-Haddad, 2015; Sebaaly, Vahedi, Kanaan, & Al-Haddad, 2018; Arab, Vahedi, & Al-Haddad, 2019; Babaie, Sebaaly, Sharifzadeh, Kanaan, & Al-Haddad, 2019, February), renewable energy sources (Patnaik, Tagore, & Chaitanya, 2017, February), active power filters (Vahedi, Shojaei, Dessaint, & Al-Haddad, 2017), active rectifiers (Vahedi, & Al-Haddad, 2016), static voltage ampere reactive (VAR) compensators (Vahedi, Dehghanzadeh, & Al-Haddad, 2018), and electric springs (Kaymanesh, Babaie, Chandra, & Al-Haddad, 2021a).

Using six power switches and one auxiliary DC capacitor, PUC can produce five-level voltage while the capacitor voltage is self-balanced to half of the input DC voltage (Babaie, Sharifzadeh, Mehrasa, Baillargeon, & Al-Haddad, 2018, October). The exact configuration of PUC is also able to generate a seven-level voltage waveform if the capacitor voltage is actively regulated at one-third of the DC source. Therefore, PUC7 enhances the power quality, reduces voltage stress, and improves the voltage ratio of the converter. Since the load current flows through the capacitor directly, the capacitor's voltage can be balanced at any desired level by controlling the switching operation of the converter or the load current itself. However, the switching operation causes a nonlinear, discontinuous relation between the capacitor voltage and load current, which exhaustingly complicates the control design problem, as the capacitor voltage and the reference current must be regulated simultaneously (Sathik, Bhatnagar, Sandeep, & Blaabjerg, 2019). Accordingly, two main strategies, including the current-based and the switching-based control methods, were proposed to overcome the controllability problems of PUC7 in both stand-alone and grid-connected modes.

The current-based methods are constructed by two PI controllers and a modulation technique, such as sinusoidal PWM (SPWM), level shift PWM, phase shift PWM, and selective harmonic

elimination (Vahedi, & Al-Haddad, 2015; Patnaik, Tagore, & Chaitanya, 2018; Tariq, Meraj, Azeem, Maswood, Iqbal, & Chokkalingam, 2018; Zid, & Bacha, 2018, March; Onizuka, García, Pinto, & da Silva, 2016, December; Iqbal, Meraj, Tariq, Lodi, Maswood, & Rahman, 2019). The first PI controller is used to balance the capacitor's voltage, where its control signal is applied to the second PI loop as the reference current to regulate the load current. However, due to the nonlinear relation between the capacitor voltage and load current, control factors tuning is tedious for the cascaded methods. In addition, the implementation results in (Vahedi, & Al-Haddad, 2015) reveal that the cascaded control loop causes considerable transient effects, containing load current fluctuation and capacitor voltage overshoot and undershoot in dynamical conditions. Further investigations disclosed that the transients are because of using the capacitor's voltage error polluted by voltage ripple as the reference current of the inner current loop. On the other hand, designing a cascaded controller for grid-tied applications is much more sophisticated because the grid as an active load notably intensifies the control tuning problem and leads to the inefficient performance of the PUC7. Regarding this fact, the current-based techniques are suitable for stand-alone applications of PUC7 (Vahedi, & Al-Haddad, 2015; Patnaik, Tagore, & Chaitanya, 2018; Tariq, Meraj, Azeem, Maswood, Iqbal, & Chokkalingam, 2018; Zid, & Bacha, 2018, March; Onizuka, García, Pinto, & da Silva, 2016, December; Iqbal, Meraj, Tariq, Lodi, Maswood, & Rahman, 2019).

In switching-based methods, the capacitor voltage is balanced by directly controlling the PUC7 switching operation. Consequently, an arbitrary reference current is independently defined to control the load current. Finite set model predictive control (FSMPC) is the only switching-based solution available to meet the desired multi-objective control for grid-connected applications of PUC7 (Metri, Vahedi, Kanaan, & Al-Haddad, 2016; qbal, Meraj, Tariq, Lodi, Maswood, & Rahman, Trabelsi, Bayhan, Ghazi, Abu-Rub, & Ben-Brahim, 2016; Abedi, Vahedi, Alfi, & Al-Haddad, 2019; Makhamreh, Trabelsi, Kükrer, & Abu-Rub, 2019; Makhamreh, Trabelsi, Kükrer, & Abu-Rub, 2020). FSMPC evaluates a cost function designed based on the discontinuous dynamic model of the load current and the capacitor's voltage to select the best switching vector per each sampling period. Even so, FSMPC suffers from variable switching frequency, which increases switching loss and voltage stress. Sensitivity to

sampling time and the necessity to measure all involved parameters in the cost function are the other drawbacks of FSMPC, which intensify its design complexity. As discussed by (Cortés et al., 2009, February), tuning the weighting factors becomes exhausting when the cost function is formulated based on multiple control objectives. The tuning problem of the weighting factors is discussed by (Pahnehkolaei, Vahedi, Alfi, & Al-Haddad, 2019) based on an optimization algorithm called the max-min technique. However, using constant weighting factors cannot guarantee the optimized performance of the FSMPC in the presence of uncertainties (Machado, Martín, Rodríguez, & Bueno, 2017). In (Makhamreh, Trabelsi, Kükrer, & Abu-Rub, 2020), the FSMPC is designed using a proper Lyapunov function, including dynamic models of the capacitor's voltage and the load current to improve the stability of the closed-loop system while no weighting factor is involved. Despite applying direct control to the capacitor's voltage with a low sample time implementation, the simulation and experimental results provided by (Makhamreh, Trabelsi, Kükrer, & Abu-Rub, 2020) show voltage ripple and variable switching frequency behavior. A robust control technique based on the Lyapunov stability theory was also proposed by (Makhamreh, Trabelsi, Kükrer, & Abu-Rub, 2019) to eliminate the weighting factors and reduce the computational burden of the cost function. In (Makhamreh, Trabelsi, Kükrer, & Abu-Rub, 2019), two cost functions obtained by the Lyapunov stability theory were used to balance the capacitor's voltage and track the reference current separately. The switching vectors are evaluated in the booth cost functions to preserve the stability of the control loop per each sampling time. Accordingly, the stability of FSMPC in (Makhamreh, Trabelsi, Kükrer, & Abu-Rub, 2019) depends on the switching vector selected during each sampling period. Moreover, selecting the switching vector based on stability criteria can affect the efficiency of the converter, as well as, the control loop. The high switching frequency of the FSMPC proposed in (Metri, Vahedi, Kanaan, & Al-Haddad, 2016; qbal, Meraj, Tariq, Lodi, Maswood, & Rahman, Trabelsi, Bayhan, Ghazi, Abu-Rub, & Ben-Brahim, 2016; Abedi, Vahedi, Alfi, & Al-Haddad, 2019; Makhamreh, Trabelsi, Kükrer, & Abu-Rub, 2019; Makhamreh, Trabelsi, Kükrer, & Abu-Rub, 2020) may also lead to a considerable level of switching loss and voltage stress.

Regarding the aforementioned detailed challenges of the previous methods, this paper proposes an optimized sliding mode controller (OSMC) as a switching-based technique to track the desired reference current and regulate the capacitor's voltage of the PUC7 in both stand-alone and grid-connected modes. The proposed OSMC is designed based on the dynamic model of load current, while the capacitor's voltage is self-balanced through the control factor of the OSMC. The control factor is tuned using a unique non-iterative visual-based optimization (VBO) method obtained based on a mathematical model of the capacitor's voltage. VBO does not need any initialized parameter and is exclusively designed for the OSMC to simplify its control factor tuning process. Despite current-based cascaded control techniques, the reference current in the stand-alone mode is independently selected from the capacitor's voltage using a new adaptive control law defined to estimate the nominal amplitude of load current based on its estimated impedance. Unlike FSMPC techniques, measuring the capacitor's voltage and using its dynamic model are no longer needed in the proposed OSMC algorithm. Therefore, as the contributions of this paper, it is the first time an advanced nonlinear controller has been proposed based on SMC for PUC7 in which the capacitor's voltage is self-balanced in both stand-alone and grid-connected modes. Fixed and low switching frequency, insensitivity to sampling time, the existence of only one control factor, adaptive performance for load variations in stand-alone mode, robustness in terms of stability and efficiency against parameters mismatch, simple implementation, and sensorless operation of capacitor's voltage are the prominent advantages of the proposed OSMC. Experimental and simulation tests conducted in stable and unstable conditions confirm the feasibility of the proposed OSMC in tracking the desired reference current and providing capacitor self-voltage balancing. In the following, Section 2.2 presents the PUC7 topology. Section 2.3 elaborates on the theory of the proposed OSMC strategy. Section 2.4 provides the stability analysis and details the proposed VBO algorithm. Section 2.5 is dedicated to presenting the experimental as simulation results. Finally, Section 2.6 provides the conclusions.

2.2 Seven-Level Packed U-Cell (PUC7) Topology

PUC7 includes six semiconductor switches, antiparallel diodes, an active DC source, and an auxiliary DC capacitor. The overall schematic diagram of the PUC7 in both stand-alone and grid-connected modes is depicted in Figure 2.1 (a) and Figure 2.1 (b), respectively. The gate signals of switches S_1, S_2, and S_3 are complementary to S_4, S_5, and S_6 to prevent short-circuits in both main and auxiliary DC links. Moreover, the capacitor's voltage must be regulated at one-third of the input DC voltage to have seven voltage levels at the AC terminal of PUC7. Table 2.1 illustrates the possible switching states of the PUC7 for the seven-level resolution. Regarding the switching vectors shown in Table 2.1, PUC7 provides a bidirectional path for the load current and generates a symmetric multilevel voltage waveform. The charging and discharging cycles of the capacitor are also determined in Table 2.1. The charging and discharging modes of the capacitor depend on its position; it charges when connected to the DC source and discharges if it only supplies the load. As shown in Table I, the PUC7 converter does not have redundant states for charging and discharging modes. Therefore, PUC7 needs an advanced multi-objective controller to regulate the capacitor's voltage besides tracking the reference current and maintaining the stability and efficacy of the converter. However, designing such an advanced multi-objective controller which considers the controllability restrictions of the PUC7 is a challenge.

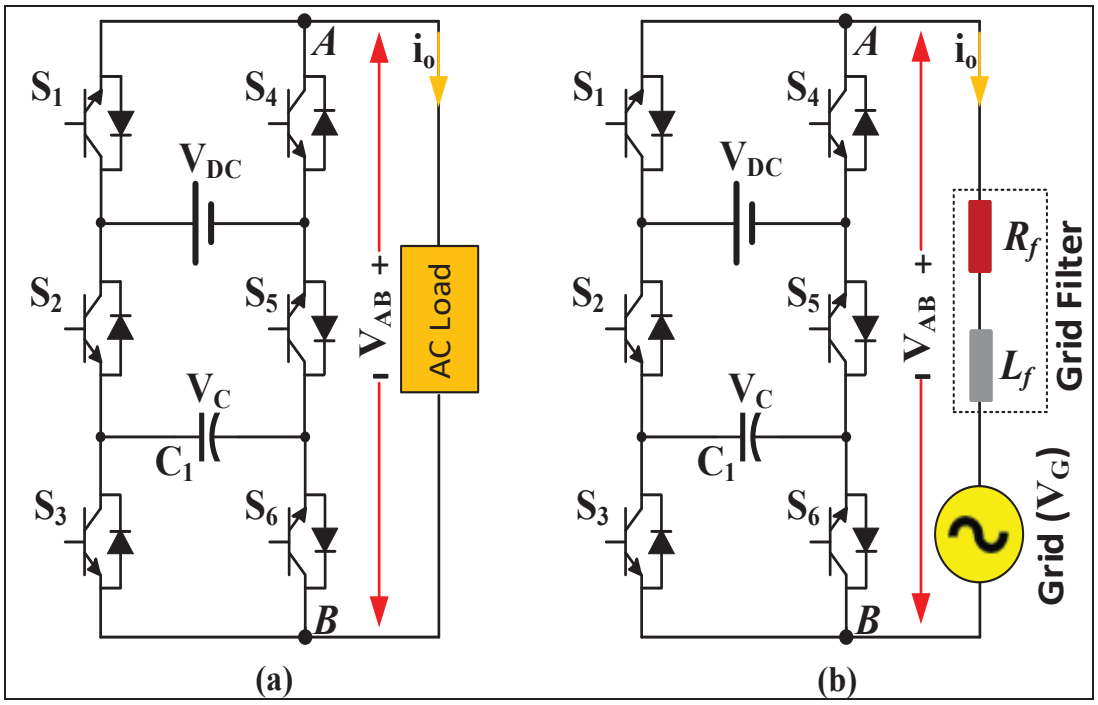

Figure 2.1 Schematic diagram of the PUC7, (a) stand-alone (b) grid-connected

Table 2.1 PUC7 switching states, voltage levels, and charging/discharging cycles

States	S_1	S_2	S_3	S_4	S_5	S_6	V_{out}	C_1
1	1	0	0	0	1	1	$+V_{DC}$	Floating
2	1	0	1	0	1	0	$+V_{DC}-V_{C1}$	Charging
3	1	1	0	0	0	1	$+V_{C1}$	Discharging
4	0	0	0	1	1	1	0	Floating
5	1	1	1	0	0	0	0	Floating
6	0	0	1	1	1	0	$-V_{C1}$	Discharging
7	0	1	0	1	0	1	$V_{C1}-V_{DC}$	Charging
8	0	1	1	1	0	0	$-V_{DC}$	Floating

2.3 Current-based Optimized Sliding Mode Control

From a control point of view, PUC7 is a nonlinear system, which includes discontinuous dynamics besides parametric and structural uncertainties. As discussed earlier, designing an

advanced multi-objective nonlinear control technique for PUC7 significantly enhances its performance. First Order SMC (FOSMC) is a variable structure robust control method designed using a dynamic model of the system polluted by uncertainties and environmental disturbances (Babaie, Rahmani, & Rezaie, 2018; Young, Utkin, & Ozguner, 1999). This paper uses FOSMC to design the proposed switching-based controller for the PUC7 converter in both stand-alone and grid-connected modes.

2.3.1 Sliding Mode Control Theory

To introduce the SMC theory, a nonlinear model of the system in the form of state space shown in (2.1) is required.

$$\begin{cases} \dot{x} = f\ (x) + g\ (x)\ u + d\ (x) \\ \| d\ (x) \| \leq \tilde{d} \end{cases} \tag{2.1}$$

where $x \in R^n$ is the space variable of the system, $f(x) \in R^n$ and $g(x) \in R^m$ are nonlinear functions that describe system dynamics and $d(x)$ is the disturbance function bounded by $\tilde{d}$. Based on the system model presented in (2.1), SMC is designed in two steps; first, a proper sliding surface is defined in (2.2).

$$S\ (x) = Q^T E = \sum_{i=1}^{n} \mu_i e_i\ (t) = \mu_1 e_1\ (t) + \ldots + \mu_n e_n\ (t) \tag{2.2}$$

where $Q^T=[\mu_1, \mu_2, \ldots, \mu_n]$ is the SMC coefficients' vector including positive constant values used to adjust the SMC performance. E is an error function as $e_i=x_i-x_{di}$, which is defined between a measured state variable and its reference (x_d). Thus, regulatory and tracking control modes are obtained by defining x_d as constant and variable signals, respectively. In the second step, a proper control law should be defined to lead the system trajectories on the sliding

surface and then force them to track the surface. In order to absorb the system trajectories on the sliding surface, a discontinuous control law (u_d) must be defined in (2.3).

$$u_d(t) = -\lambda \operatorname{sgn}(S) \tag{2.3}$$

where $sgn(S)$ represents the sign function and λ is a positive definite constant used to control the reaching time and guarantee the stability of the control loop based on Lyapunov theory. In addition, an equivalent control law (u_{eq}) based on the derivative of the sliding surface ($dS/dt=0$) is designed in (2.4) to force the system trajectories to track the sliding surface.

$$u_{eq}(t) = -\left(Q^T g(x)\right)^{-1} Q^T f(x) \tag{2.4}$$

Eventually, the generalized control law (u_g) of SMC is expressed in (2.5) for a nonlinear system like PUC7 to generate the modulation index.

$$u_g(t) = -\left(Q^T g(x)\right)^{-1} Q^T f(x) - \lambda sgn(S) \tag{2.5}$$

2.3.2 Optimized Sliding Mode (OSMC) for Stand-Alone Operation of PUC7

The nonlinear model of the stand-alone PUC7 shown in Figure 2.1 (a) is obtained in (2.6) by applying the KVL law from point A to point B.

$$L_L \frac{di_o}{dt} = V_{AB} - R_L i_o \tag{2.6}$$

where V_{AB} and i_o are the measured output voltage and load current of the PUC7 converter, respectively. R_L and L_L are also the load resistance and inductance, respectively. Since the maximum voltage level generated by PUC7 is V_{dc}, V_{AB} is rewritten in (2.7) based on the modulation index.

$$V_{AB} = V_{dc} u \tag{2.7}$$

where u is the modulation index generated by SMC to select the best switching vector among eight possible switching vectors of PUC7 listed in Table 2.1. Using (2.7), the nonlinear model of PUC7 presented in (2.6) is rewritten as follows:

$$\frac{di_o}{dt} = \frac{1}{L_L} \left(V_{dc} u - R_L i_o \right) \tag{2.8}$$

The dynamic model of the load current presented in (2.8) is used to track the desired reference current (i_d) by OSMC. To this end, a proper sliding surface is proposed in (2.9).

$$S = i_o - i_d \tag{2.9}$$

The equivalent control law for the stand-alone PUC7 is also obtained in (2.10).

$$u_{eqS}(t) = \frac{1}{V_{dc}} \left(R_L i_o + L_L \frac{di_d}{dt} \right) \tag{2.10}$$

The generalized control law ($u_{gS}(t)$) in stand-alone PUC7 is attained using (2.3) and (2.10) in (2.11).

$$u_{gS}(t) = \frac{1}{V_{dc}} \left(R_L i_o + L_L \frac{di_d}{dt} \right) - \lambda_S sgn \left(S \right) \tag{2.11}$$

where λ_s is the factor of the discontinuous control term in the stand-alone mode of operation. As shown in (2.9) and (2.11), the load current can be desirably controlled by i_d. Concerning the dynamic model of the capacitor's voltage shown in (2.12), it is also obvious that the load current and the switching states S_2 and S_3 directly affect this floating voltage. Therefore, without requiring the voltage control loop, the capacitor voltage can be self-balanced to one-

third of the DC source voltage if the PUC7 switching operation and load current amplitude are controlled appropriately.

$$\begin{cases} C\ \dfrac{dV_C}{dt} = i_c \\ i_c = (S_3 - S_2)i_o \end{cases} \tag{2.12}$$

where C, V_C, and i_c respectively show the capacitor's capacitance, capacitor's voltage, and current, respectively. S_2, S_3 are also the switching variable shown in Table 2.1. In the case of the load current control for stand-alone PUC7, i_d has to be accurately defined so that the demanded power is delivered to the load while the modulation index is not saturated. Indeed, i_d must be defined using the peak value of load current in the stand-alone mode (i_{dn}). In this case, i_{dn} can be constantly determined by considering the load impedance and the DC source voltage. However, using a constant value is not practical when the load and DC source are variable. In the previous efforts detailed in (Vahedi, & Al-Haddad, 2015; Patnaik, Tagore, & Chaitanya, 2018; Tariq, Meraj, Azeem, Maswood, Iqbal, & Chokkalingam, 2018; Zid, & Bacha, 2018, March; Onizuka, García, Pinto, & da Silva, 2016, December; Iqbal, Meraj, Tariq, Lodi, Maswood, & Rahman, 2019), a PI controller was employed to adjust i_{dn} using the capacitor's voltage error. However, because of the capacitor's voltage ripple and the non-optimized performance of the PI controller, the estimated i_{dn} fluctuates, which increases switching loss, intensifies THD, and causes destructive transient effects in the load current and the capacitor's voltage. To address these problems caused by the conventional PI-based estimator, an adaptive control term is defined using Ohm's law to estimate i_{dn} while the sensorless voltage balancing of the capacitor is achieved. According to Ohm's law, the amplitude of the load current is a function of the load's impedance, as well as, the converter's voltage. Thus, in the proposed adaptive control term, i_{dn} is self-tuned using the root mean square of the output current ($i_{o\text{-}rms}$), input DC voltage (V_{dc}), and the estimated impedance of the load (Z^*), as formulated in (2.13).

$$\begin{cases} Z^* = \dfrac{V_{dc}}{i_{o-rms}\sqrt{2}} \\ i_{dn} = \dfrac{V_{dc}}{Z^*} \end{cases} \tag{2.13}$$

Consequently, i_d in stand-alone mode is generated based on the estimated i_{dn} with desired fundamental frequency (f_0) as presented in (2.14).

$$i_d = i_{dn} \sin(2\pi f_0) \tag{2.14}$$

Since Z^* is the load impedance, the system dynamic defined in (2.8) can be updated to (2.15).

$$\frac{di_o}{dt} = \frac{1}{L_L}\left(V_{dc}u - Z^* i_o \right) \tag{2.15}$$

Subsequently, $u_{gS}(t)$ defined in (2.11) is rewritten in (2.16).

$$u_{gS}(t) = \frac{1}{V_{dc}}\left(Z^* i_o + L_L \frac{di_d}{dt} \right) - \lambda_S sgn\ (\ S\ ) \tag{2.16}$$

Using the generalized control law shown in (2.16), OSMC provides an adaptive performance against the load and DC source voltage variations. The OSMC control loop for the stand-alone PUC7 is finally illustrated in Figure 2.2. As shown, the load current and DC source voltage are measured, and then i_{dn} and Z^* are estimated to generate the reference current for the OSMC technique. Afterward, the OSMC produces a sinusoidal reference signal required for the PWM method as the modulation index to generate the proper switching pulses.

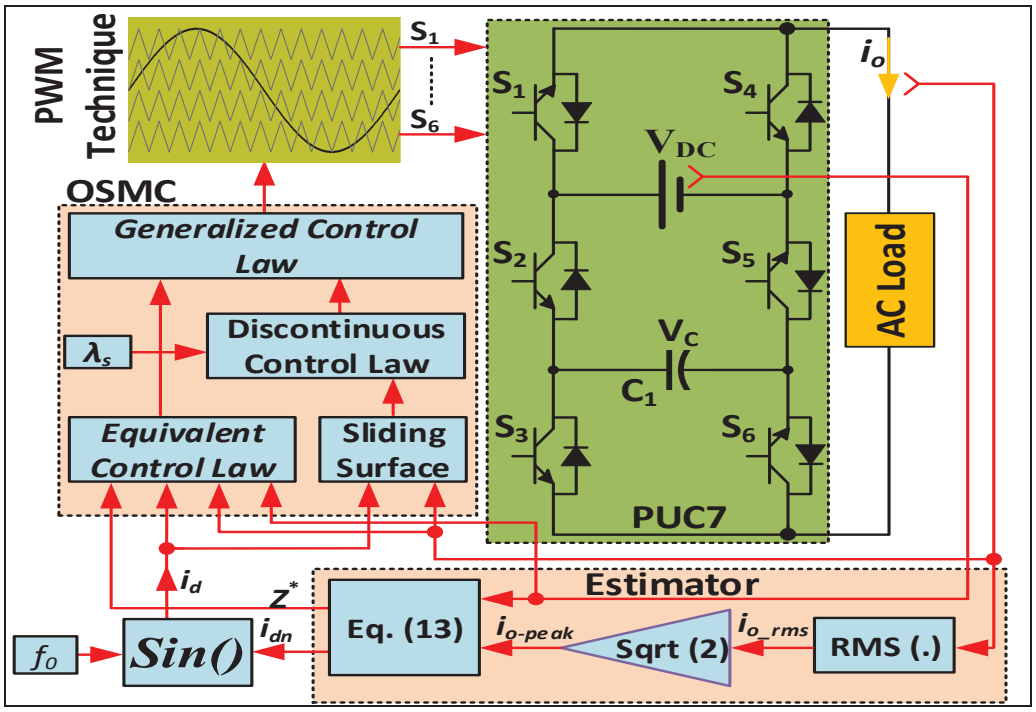

Figure 2.2 Block diagram of the proposed OSMC for the stand-alone PUC7

2.3.3 Optimized Sliding Mode (OSMC) for Grid-Connected Operation of PUC7

Because of the dynamic behavior of the grid and the necessity of synchronizing the inverter current with the grid voltage, controlling the capacitor voltage in grid-connected PUC7 is much more complicated than in the stand-alone mode. Thus, OSMC is also developed for the grid-connected PUC7 to challenge its sensorless voltage regulation ability. Regarding, the grid-connected model of PUC7 shown in Figure 2.1 (b) is obtained as below:

$$\frac{di_o}{dt} = \frac{1}{L_f}\left(V_{dc}u - V_G - R_f i_o \right) \tag{2.17}$$

where V_G is grid voltage; R_f and L_f are resistance and inductance of the grid filter, respectively. The sliding surface defined in (2.9) is used to design the equivalent control law (u_{eqG}(t)) as below:

$$u_{eqG}(t) = \frac{1}{V_{dc}} \left(R_L i_o + V_G + L_L \frac{di_d}{dt} \right) \tag{2.18}$$

Consequently, the generalized control law for the grid-connected PUC7 is acquired in (2.19).

$$u_{gG}(t) = \frac{1}{V_{dc}} \left(R_f i_o + V_G + L_f \frac{di_d}{dt} \right) - \lambda_G sgn\ (\ S\ ) \tag{2.19}$$

where λ_G is the control factor of the discontinuous term in the grid-connected mode. Similar to the stand-alone design, the capacitor voltage in the grid-connected configuration is directly affected by the load current (i_o) and the switching states, as defined in (2.12). Since the impedance of the grid is negligible, the reference current in the grid-connected PUC7 can be assigned desirably or based on the maximum power provided by the DC source. Therefore, λ_G as the second effective parameter of the OSMC has to be accurately tuned to balance the capacitor voltage at the desired level.

The block diagram of the proposed OSMC for the grid-connected PUC7 is depicted in Figure 2.3. As shown, the reference current is designed based on the grid voltage angle detected by the phase-locked loop (PLL) unit and multiplied by a constant value as the desired amplitude ($i_{d\text{-}peak}$) of the reference current. Afterward, the reference current and its derivative are applied to the OSMC to track the control objectives.

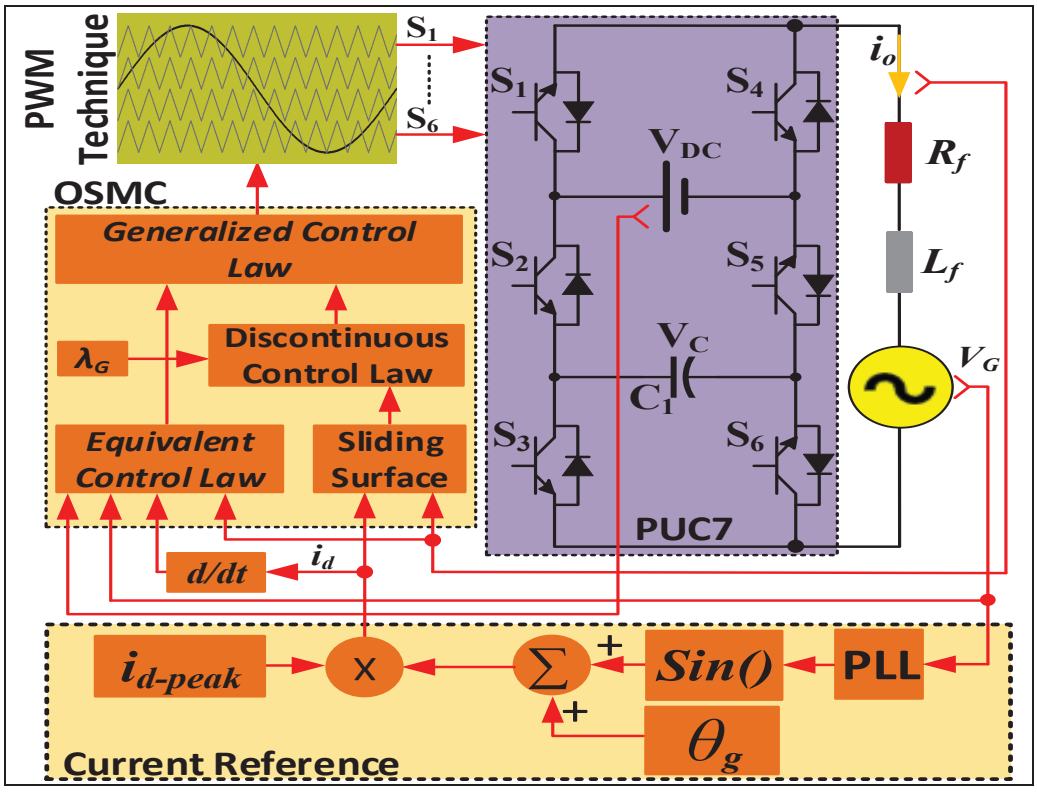

Figure 2.3 Block diagram of the proposed OSMC for the grid-connected PUC7

2.4 Stability Analysis of the OSMC and Control Coefficient Tuning

Lyapunov stability theory provides powerful mathematical tools to investigate certain conditions where the control loop establishes asymptotic stability for the unstable system. The reliability of the stability conditions depends on the accuracy of the model. Thus, the dynamic model should sufficiently describe the real system. As shown in (2.15) and (2.17), in the case of PUC7, a non-ideal model of components can be used in the dynamic equations presented; even so, satisfactory results obtained by an approximated model in (Metri, Vahedi, Kanaan, & Al-Haddad, 2016; Iqbal, Meraj, Tariq, Lodi, Maswood, & Rahman, Trabelsi, Bayhan, Ghazi, Abu-Rub, & Ben-Brahim, 2016; Abedi, Vahedi, Alfi, & Al-Haddad, 2019; Makhamreh, Trabelsi, Kükrer, & Abu-Rub, 2019; Makhamreh, Trabelsi, Kükrer, & Abu-Rub, 2020) reveal that using exact model would dramatically complicate the controller while the control performance would not enhance significantly. Consequently, (2.15) and (2.17) present reliable nonlinear models for stability analysis. In addition, the stability analysis in this section

indicates that the positive definite constant (λ) has the maximum effect on the stable performance of OSMC and the self-balancing operation of the capacitor's voltage. Finally, the provided mathematical analyses guarantee the OSMC stability by selecting the optimum value for λ in both grid-connected and stand-alone modes.

2.4.1 Stability Analysis of The Proposed OSMC Technique

The proposed OSMC can be analyzed to find the valid domains of the control coefficient (λ) where the globally asymptotically stability of the converter is ensured. To this end, the Lyapunov function formulated in (2.20) is considered the candidate function to select the optimal value of λ.

$$V = \frac{1}{2} S^2 \tag{2.20}$$

According to Lyapunov stability theory, λ should be chosen, as the derivative of (2.20) becomes negative to confirm the globally asymptotically stability of the OSMC under all conditions. Therefore, the derivative of the candidate Lyapunov function shown in (2.20) is obtained as below:

$$\begin{cases} S\dot{S} < 0 \\ \dot{S} = \dfrac{di_o}{dt} - \dfrac{di_d}{dt} \end{cases} \tag{2.21}$$

Derivative of the sliding surface emerged in (2.21) is extended to (2.23-a) and (2.23-b) based on the exact model of the system defined in (2.22-a) and (2.22-b) for stand-alone and grid-connected PUC7 converter, respectively.

$$\begin{cases} a) \quad \dfrac{di_o}{dt} = \dfrac{1}{L_{Lm}} \left(V_{dc}u - Zi_o \right) \\ b) \quad \dfrac{di_o}{dt} = \dfrac{1}{L_{fm}} \left(V_{dc}u - V_G - R_{fm}i_o \right) \end{cases} \tag{2.22}$$

where L_{Lm} and Z are the actual values of the load inductor and impedance in the stand-alone model. R_{fm} and L_{fm} are also the true values of the grid filter resistor and inductor in the grid-connected model. The nonlinear model of the PUC7 is used for the stability analysis to obtain more reliable results.

$$\begin{cases} a)\, S \left(\dfrac{1}{L_{Lm}} \left(V_{dc}u - Zi_o \right) - \dfrac{di_d}{dt} \right) < 0 \\ b)\, S \left(\dfrac{1}{L_{fm}} \left(V_{dc}u - V_G - R_{fm}i_o \right) - \dfrac{di_d}{dt} \right) < 0 \end{cases} \tag{2.23}$$

In the next step, the generalized control laws of OSMC should replace u as the input signal of the real system in (2.23) to evaluate the stability of PUC7 in stand-alone and grid-tied modes. To this end, the generalized control signal of (2.16) and (2.19) are modified as (2.24-a) and (2.24-b) to be placed into (2.23).

$$\begin{cases} a)\, V_{dc}u = Z^*i_o + L_{Lc} \dfrac{di_d}{dt} - V_{dc}\lambda_S sgn \left(S \right) \\ b)\, V_{dc}u - V_G = R_{fc}i_o + L_{fc} \dfrac{di_d}{dt} - V_{dc}\lambda_G sgn \left(S \right) \end{cases} \tag{2.24}$$

where L_{Lc} is the estimated load inductance in the stand-alone controller. R_{fc} and L_{fc} are the estimated values of the grid filter in the grid-connected control loop. Then, (2.23) is extended by (2.24) as (2.25).

$$\begin{cases} a)\ S\left(i_o\ \left(Z^{*}\text{-}Z \right) + \dfrac{di_d}{dt}\ \left(L_{Lc}\text{-}L_{Lm} \right)\ \text{-}V_{dc}\lambda_S\ \ \text{sgn}(S) \right) < 0 \\ b)\ S\left(i_o\ \left(R_{fc}\text{-}R_{fm} \right) + \dfrac{di_d}{dt}\ \left(L_{fc}\text{-}L_{fm} \right)\ \text{-}V_{dc}\lambda_G\ \ \text{sgn}(S) \right) < 0 \end{cases} \tag{2.25}$$

Equation (2.25) shows a mismatch between Z^{*}, R_{fc}, L_{Lc}, L_{fc} emerged in the control equations and Z, R_{fm}, L_{Lm}, L_{fm} measured from the real system. Thanks to (2.13), the mismatch between Z^{*} and Z is negligible. Even though the mismatch appears in (R_{fc}, R_{fm}), (L_{fc}, L_{fm}), and (L_{Lc}, L_{Lm}), (2.26) shows that inequalities of (2.25) remain as negative definite functions since V_{dc} is much bigger than other terms and λ_S>0 and λ_G>0. Consequently, the proposed OSMC provides global asymptotic stability for PUC7 in both stand-alone and grid-connected modes even under parametric mismatches.

$$\begin{cases} a)\ V_{dc}\lambda_S\ \ \text{sgn}(S) \gg \left(i_o\ \left(Z^{*} - Z \right) + \dfrac{di_d}{dt}\ \left(L_{Lc} - L_{Lm} \right) \right) \\ b)\ V_{dc}\lambda_G\ \ \text{sgn}(S) \gg \left(i_o\ \left(R_{fc} - R_{fm} \right) + \dfrac{di_d}{dt}\ \left(L_{fc} - L_{fm} \right) \right) \end{cases} \tag{2.26}$$

Moreover, generalized control laws obtained in (2.16), (2.19), and the stability conditions provided in (2.25) show that the capacitor mismatch challenge is eliminated in the proposed OSMC. Consequently, OSMC provides robust performance against variations of C along with sensor-less voltage balancing operation in PUC7. Further investigations for the mismatch impact on the control loop stability and efficiency are presented in section 2.5. It is worth mentioning that the Lyapunov stability theory does not assure the efficiency of OSMC to attain the desired control objectives. Therefore, more analysis should be accomplished to determine the optimal values of λ_S and λ_G to guarantee the optimum performance of the OSMC.

2.4.2 Tuning λ_S and λ_G based on the VBO Algorithm

Although the capacitor voltage balancing is the big challenge of PUC7, (2.15) and (2.17) show that OSMC is only designed using the dynamic model of load current. Even so, the dynamic

model of capacitor voltage provided in (2.12) shows that its voltage variation depends on the switching operation of S_2, S_3, and i_o. Thus, it is possible to balance the capacitor voltage by tuning the PUC7 switching operation and controlling the load current without using any voltage controller and voltage measurement. As the first step to tune the OSMC control factors, the following capacitor voltage error (e_{VC}) is considered.

$$e_{VC} = V_C - V_C^* \tag{2.27}$$

where V^*_C is the desired capacitor's voltage set to one-third of the DC source. Using the capacitor voltage model defined in (2.12), the voltage balancing error in (2.27) can be rewritten as (2.28).

$$e_{VC} = \int \frac{u}{C} i_o dt - V_C^* \tag{2.28}$$

Substituting the generalized control signals of OSMC presented in (2.16) and (2.19) for stand-alone and grid-connected modes, the capacitor's voltage error is as below:

$$\begin{cases} e_{VC-G} = \dfrac{1}{CV_{dc}} \int \left(\left(\begin{array}{l} \left(R_f i_o + V_G + L_f \dfrac{di_d}{dt} \right) \\ -\lambda_G sgn\ (S) \end{array} \right) i_o dt \right) - V_C^* \\ e_{VC-S} = \dfrac{1}{CV_{dc}} \int \left(\left(\begin{array}{l} \left(R_L i_o + L_f \dfrac{di_d}{dt} \right) \\ -\lambda_S sgn\ (S) \end{array} \right) i_o dt \right) - V_C^* \end{cases} \tag{2.29}$$

Equation (2.29) indicates that the capacitor's voltage error is controlled using the current-based generalized control law of the OSMC. The generalized control law provides the sinusoidal reference signal for the SPWM modulator utilized in the control loop in Figure 2.2 and Figure 2.3 to generate the PWM pulses. Therefore, the capacitor's voltage error in the grid-connected ($e_{VC\text{-}G}$) and stand-alone ($e_{VC\text{-}S}$) PUC7 is minimized by adjusting the generalized control laws of

the OSMC using λ_G and λ_S. A Visual Based Optimization (VBO) technique supported by (2.29) is proposed to optimize λ_G and λ_S so that e_{VC} is minimized in the stand-alone and grid-connected modes. To implement the VBO technique, the error signal of e_{VC} is respectively plotted in Figure 2.4 and Figure 2.5 for the stand-alone and grid-connected PUC7 concerning the variation of λ_S and λ_G.

The simulation results in Figure 2.4 and Figure 2.5 have been captured in steady-state conditions with the system parameters provided in Table 2.2. In Figure 2.4 and Figure 2.5, λ_S and λ_G are increased by the steps of 0.01 where the voltage errors vary from 108-to-50 and 106-to-55 in stand-alone and grid-connected modes, respectively. However, the minimum error value (e_d) is obtained for unique values determined by red points.

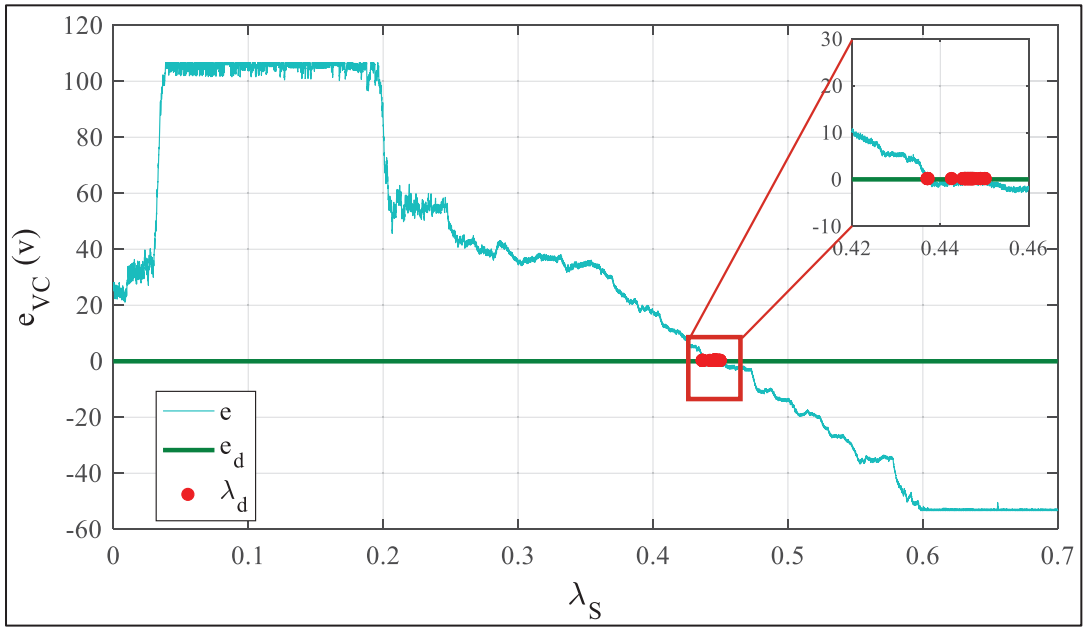

Figure 2.4 The proposed VBO method for optimizing λ_S in the stand-alone PUC7

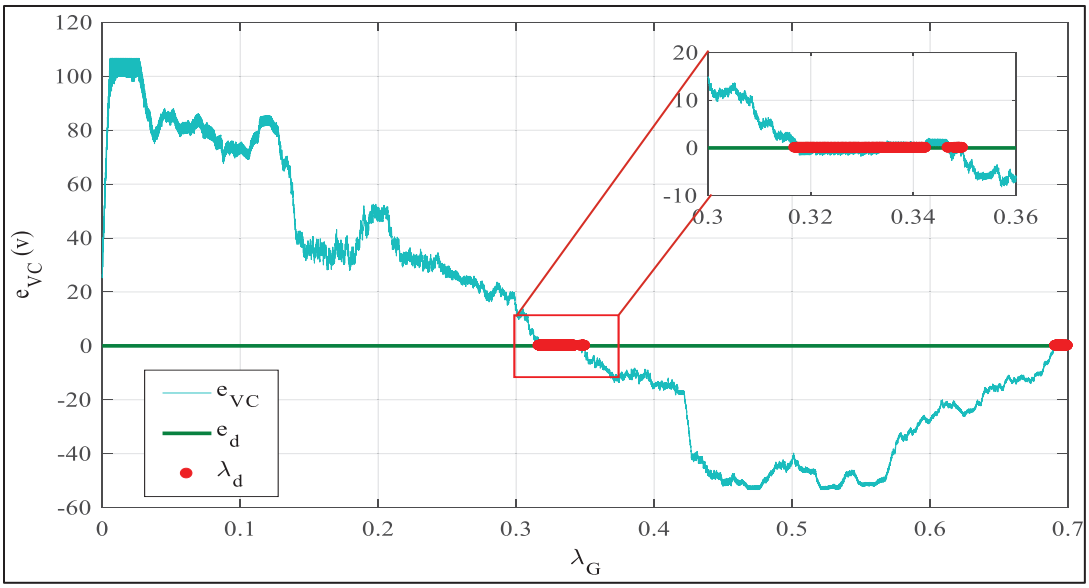

Figure 2.5 The proposed VBO method for optimizing λ_G in grid-connected PUC7

Table 2.2 Experimental and simulation test parameters

DC source and AC grid voltages (V_{dc}, V_G)	160 V & 130 V(peak)
DC capacitor (C_1) in experimental tests	900 µF
AC load inductor & resistor (R_L, L_L)	80 Ω & 50 mH
Diode rectifier as nonlinear load (R_{dc}, L_{dc})	80 Ω & 50 mH
Grid filter inductor & resistor (R_f, L_f)	0.1 Ω & 2.5 mH
Fundamental and switching frequency	60 Hz & 2000 Hz
Experimental and simulation sampling time	80 µs, 25 µs

Indeed, these points indicate the best value (λ_d) for λ_S and λ_G by which the capacitor voltage will inherently track its desired reference. Considering the performed analysis shown in Figure 2.4 and Figure 2.5, the final value for λ_G and λ_S is obtained as 0.448 and 0.318, respectively. The tuning results in Figure 2.4 and Figure 2.5 confirm that the VBO is a fast and accurate technique to optimize the control factor of OMSC through mathematical modeling where no iteration and initial values are required. Finally, using the optimized control factors, OSMC generates an appropriate sinusoidal reference for the SPWM modulator to track the desired

reference current and balance the capacitor's voltage in both stand-alone and grid-connected modes while the voltage control loop, including its voltage measurement, is no longer required.

2.5 Experimental and Simulation Tests and Results

This section is dedicated to evaluating the performance of the proposed OSMC control algorithm through various experimental and simulation test scenarios. MATABL 2016b has been used to run the simulations while the experiments have been accomplished using a prototype constructed based on dSPACE 1104, as shown in Figure 2.6. The system parameters for experiments and simulation are also presented in Table II.

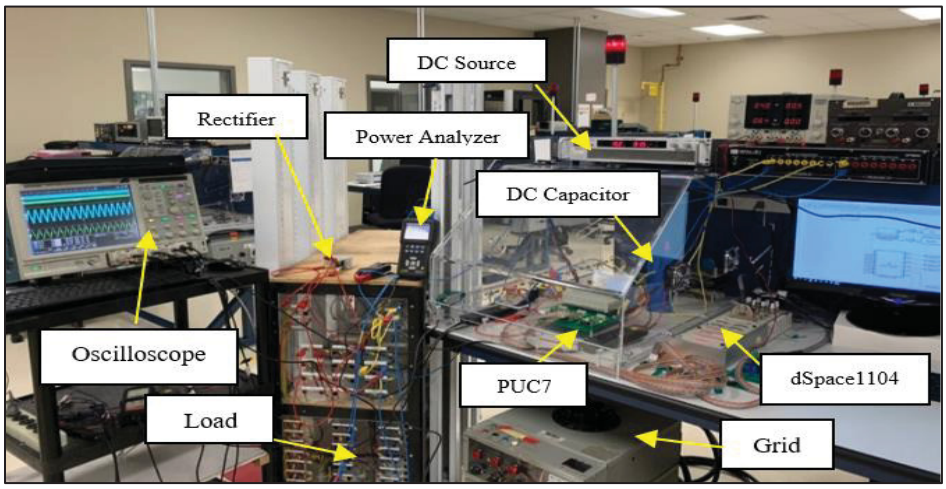

Figure 2.6 Experimental setup of the proposed OSMC applied to PUC7 in both stand-alone and grid-connected modes

2.5.1 Test I: Stand-Alone Mode

The proposed OSMC algorithm is first evaluated in the stand-alone mode of operation. The load impedance in the first test changes from 40Ω to 80Ω and vice versa. The corresponding experimental and simulation results of this dynamic test are depicted in Figure 2.7 and Figure 2.8, respectively. Figure 2.7 demonstrates the capacitor's voltage, load current, and the seven-level voltage waveform in the presence of the load variations.

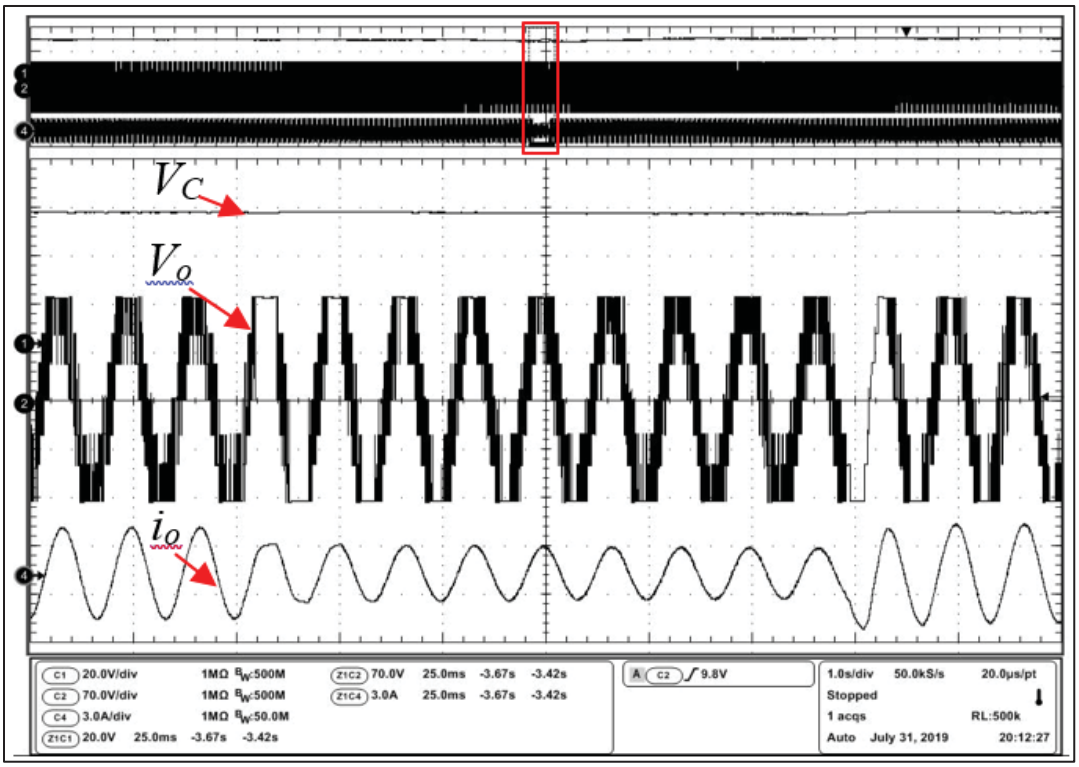

Figure 2.7 Experimental results of V_C, i_o, and V_o under load variations

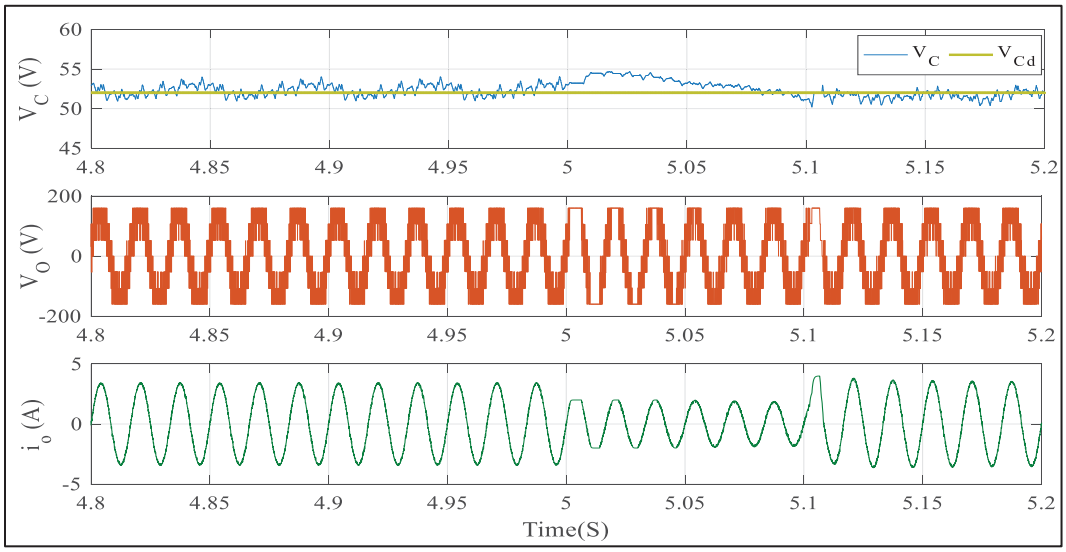

Figure 2.8 Simulation results under load variations when C=900µF, T_S=25µs

As shown, the converter perfectly supplies the load variations without any notable transient effect and fluctuation in the current and voltages. Moreover, Figure 2.8 shows the capacitor's

voltage with a ripple of less than 5%. This voltage is self-balanced to the one-third of DC source without any destructive fluctuation during the load impedance changes. The symmetrical seven-level output voltage (V_o) in Figure 2.7 and Figure 2.8 also indicates the successful sensor-less operation of the proposed OSMC to balance the capacitor voltage even under load uncertainties. The desired reference current (i_d) and the measured load current (i_o) during the load variation are also shown in Figure 2.9. It is depicted that the load current tracks the variation of the desired reference current with a negligible transient effect when PUC7 operates in the stand-alone mode.

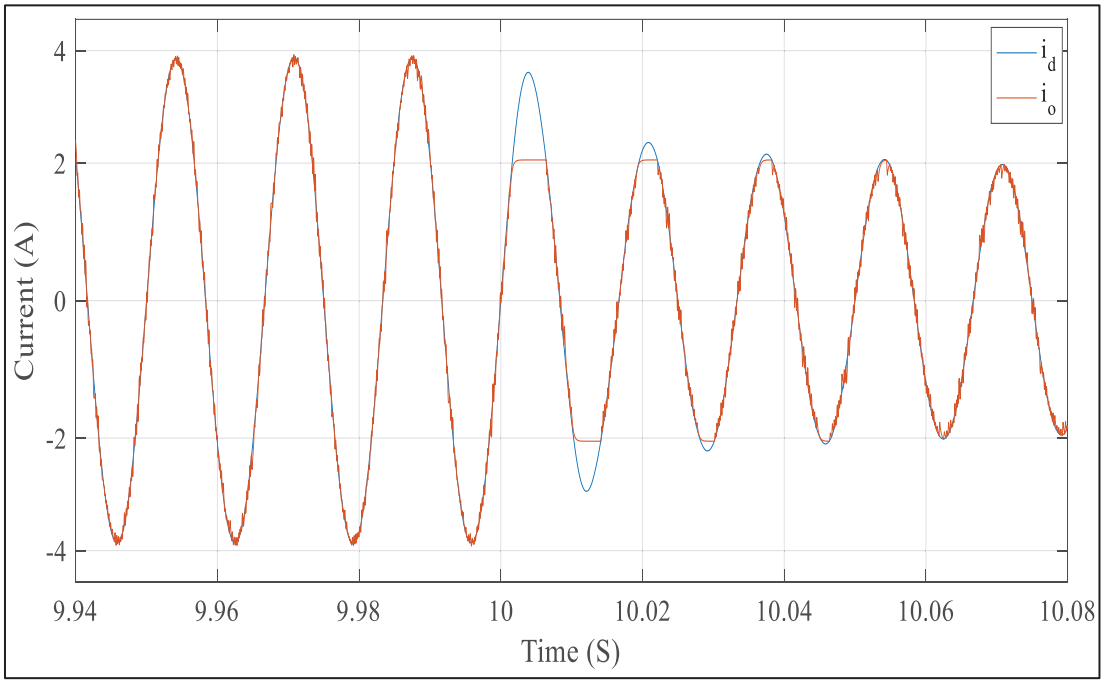

Figure 2.9 Estimated reference and measured load currents during the load variations in the stand-alone PUC7

The harmonics spectrum analysis for the output voltage and current in stand-alone mode is captured using the power analyzer and shown in Figure 2.10. According to the power quality analysis, the THD is within the standard range. It should be noted that the THD analysis has been performed for the first 50th harmonic orders.

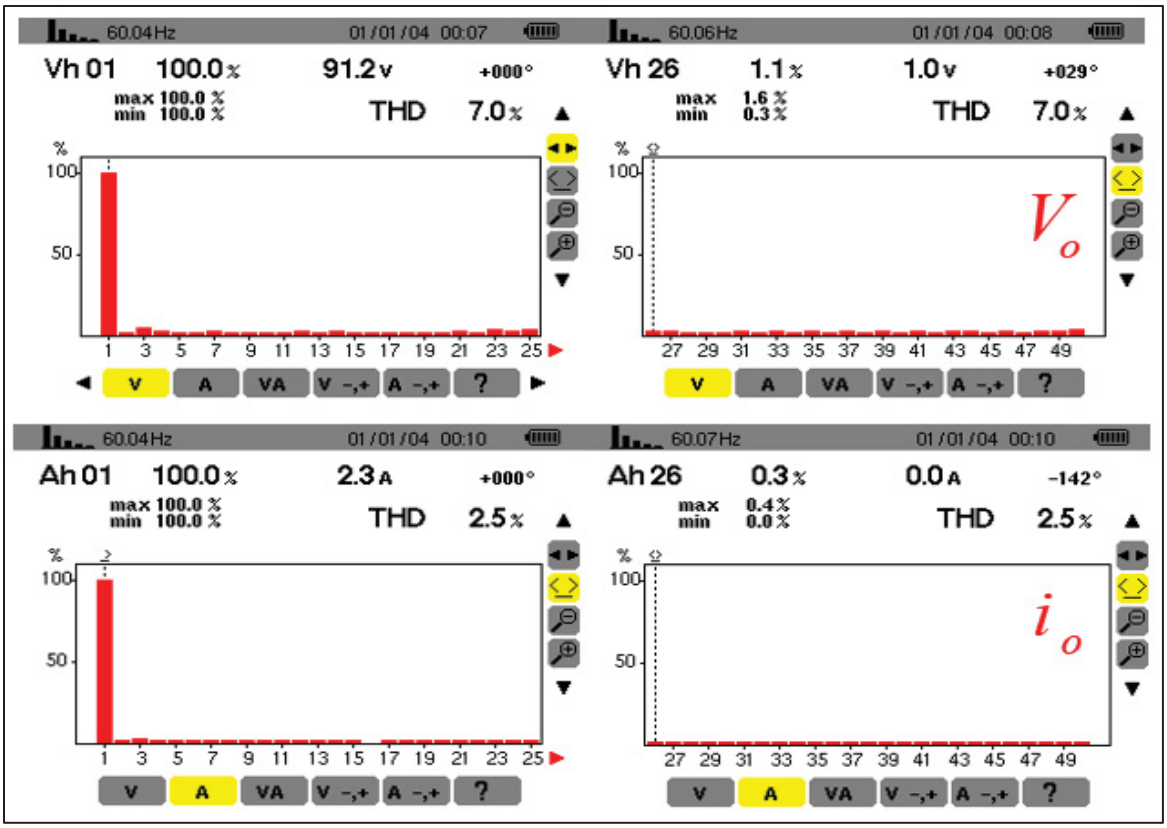

Figure 2.10 Harmonic spectrum analysis for V_o and i_o in the stand-alone PUC7

To further analyze the OSMC under dynamic conditions, the stand-alone PUC7 is tested under the DC source voltage variation; the corresponding experimental and simulation results are shown in Figure 2.11 and Figure 2.12, respectively. As shown in Figure 2.11, the load current follows the voltage variations appropriately. In the simulation results depicted in Figure 2.12, the DC voltage is stepped up from 180V to 300V; the results demonstrate that the OSMC overcomes this dynamic mode by regulating the capacitor's voltage at the new level with the voltage ripple of less than 5%. Thus, it can be inferred that since the load current and the switching operation of PUC7 are controlled by OSMC, the capacitor's voltage inherently tracks its reference even under DC-source variation.

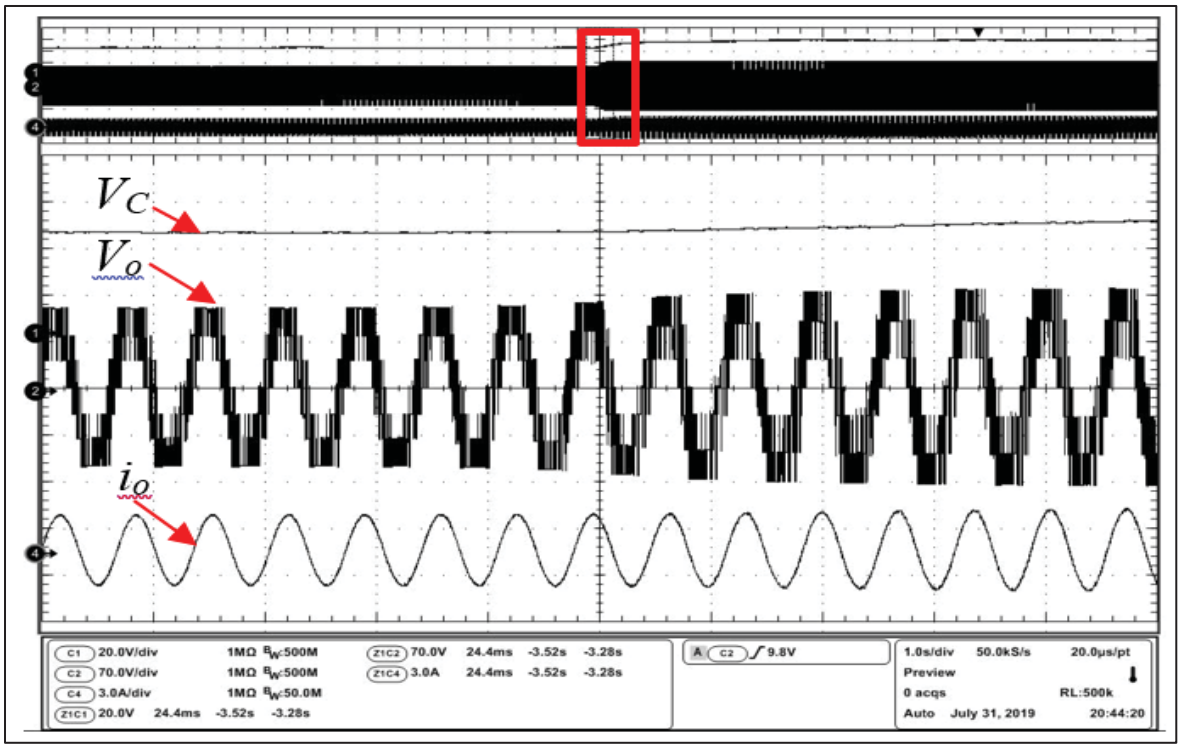

Figure 2.11 Experimental results of V_C, i_o, and V_o under the DC-source voltage variation

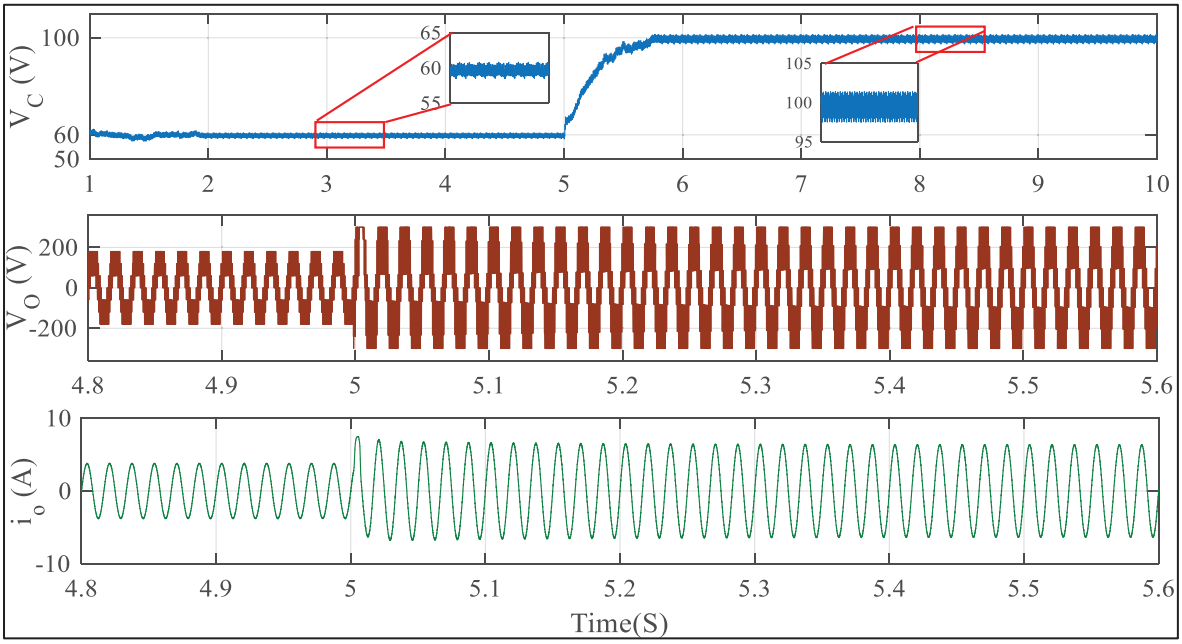

Figure 2.12 Simulation results of DC source voltage variation in the stand-alone PUC7 when C=900µF, T_S=25µs

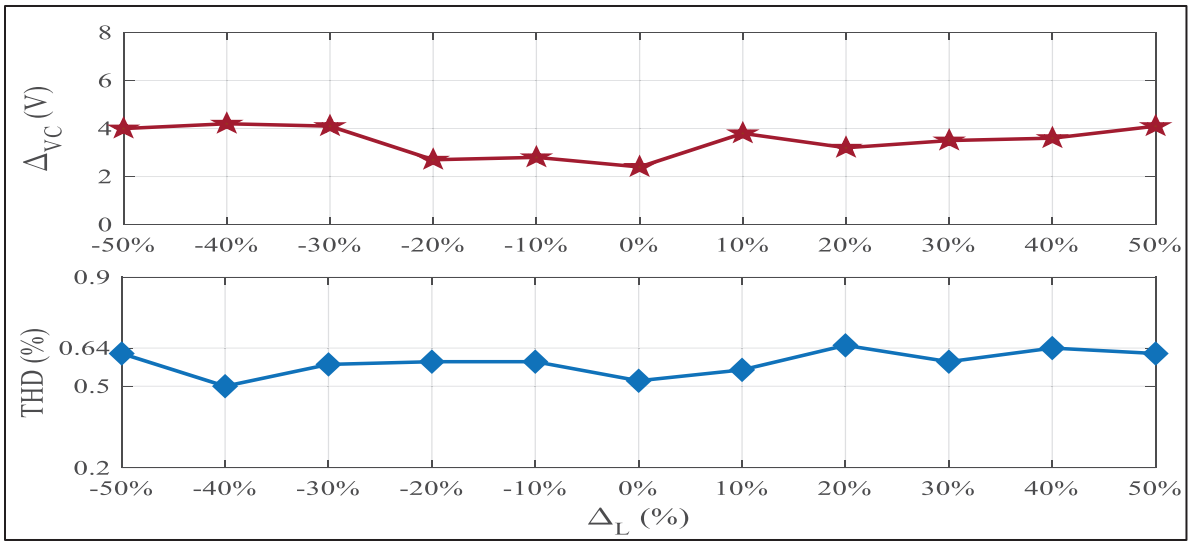

Figure 2.13 Parametric mismatch test for the load inductance in the stand-alone PUC7 with T_S=25µs

In the next test, the inductance size is changed by ±50% with steps of 10% to evaluate the robustness of OSMC against parametric mismatches. Figure 2.13 displays the mismatch effects on the current THD and the capacitor voltage ripple. The results prove the acceptable robustness of the proposed OSMC algorithm in the presence of the inductance mismatch. Regarding the capacitor mismatch, (2.16) confirms that C does not appear in the control law because of the self-balancing operation; thus, the control loop is insensitive to its mismatch. To evaluate the sensorless operation of OSMC, the DC voltage changes from zero to 160V as a start-up condition. The experimental results depicted in Figure 2.14 prove that the self-voltage balancing operation of the OSMC is independent of the initial level of capacitor charge without considering any pre-charged. As the final test, a nonlinear load, including a single-phase rectifier, is connected to the PUC7 terminals in parallel to the linear load (RL, LL) defined in Table 2.2 to analyze the OSMC performance under harmonic pollutions. The rectifier feeds an RL load on the DC side, as R_{dc} and L_{dc} with values defined in Table 2.2. While the harmonics are visible in the load current, the results provided in Figure 2.15 show that the capacitor self-voltage balancing operation is stable when the nonlinear load is connected and disconnected.

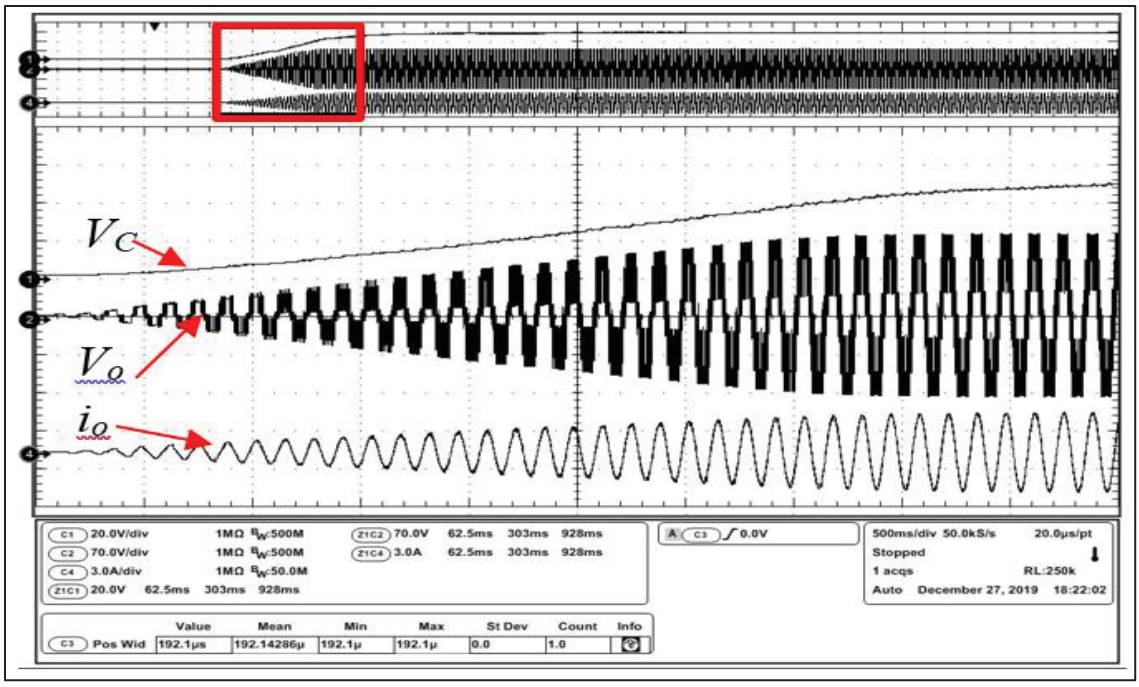

Figure 2.14 Experimental results of the capacitor voltage, seven-level waveform, and the load current in the stand-alone PUC7 during the start-up test

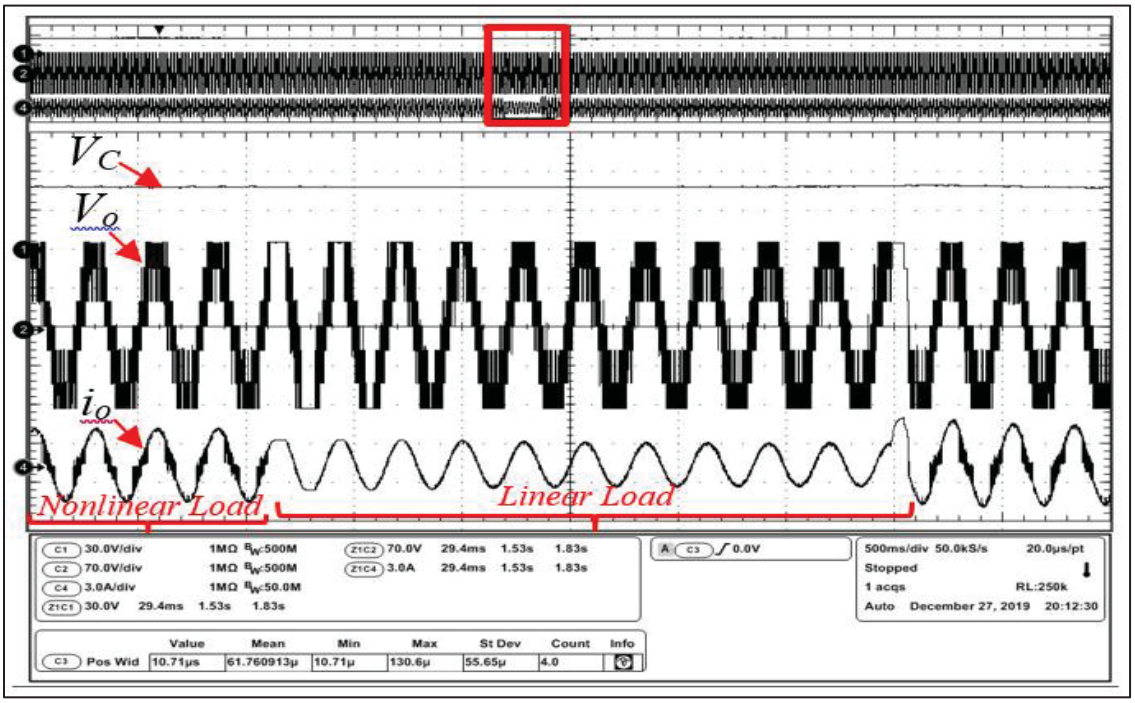

Figure 2.15 Experimental results of stand-alone PUC7 under the nonlinear load

2.5.2 Test II: Grid-Connected Mode of Operation of PUC7

The results in this section belong to the OSMC, which is applied to the grid-connected PUC7 converter. Figure 2.16 illustrates the steady-state results, including the capacitor's voltage, inverter current, multilevel waveform, and grid voltage. As demonstrated in Figure 2.16, the capacitor's voltage is accurately self-balanced with a voltage ripple of less than 5%. The grid voltage and injected current are also synchronized to attain the unity power factor. The harmonic spectrum analysis for the injected current and grid voltage are presented in Figure 2.17 (a). The results demonstrate THD below 5% obtained for the current and voltage. To show the effects of the sampling time on the grid's current power quality, another THD analysis is done for different sampling times, and the results are presented in Figure 2.17 (b).

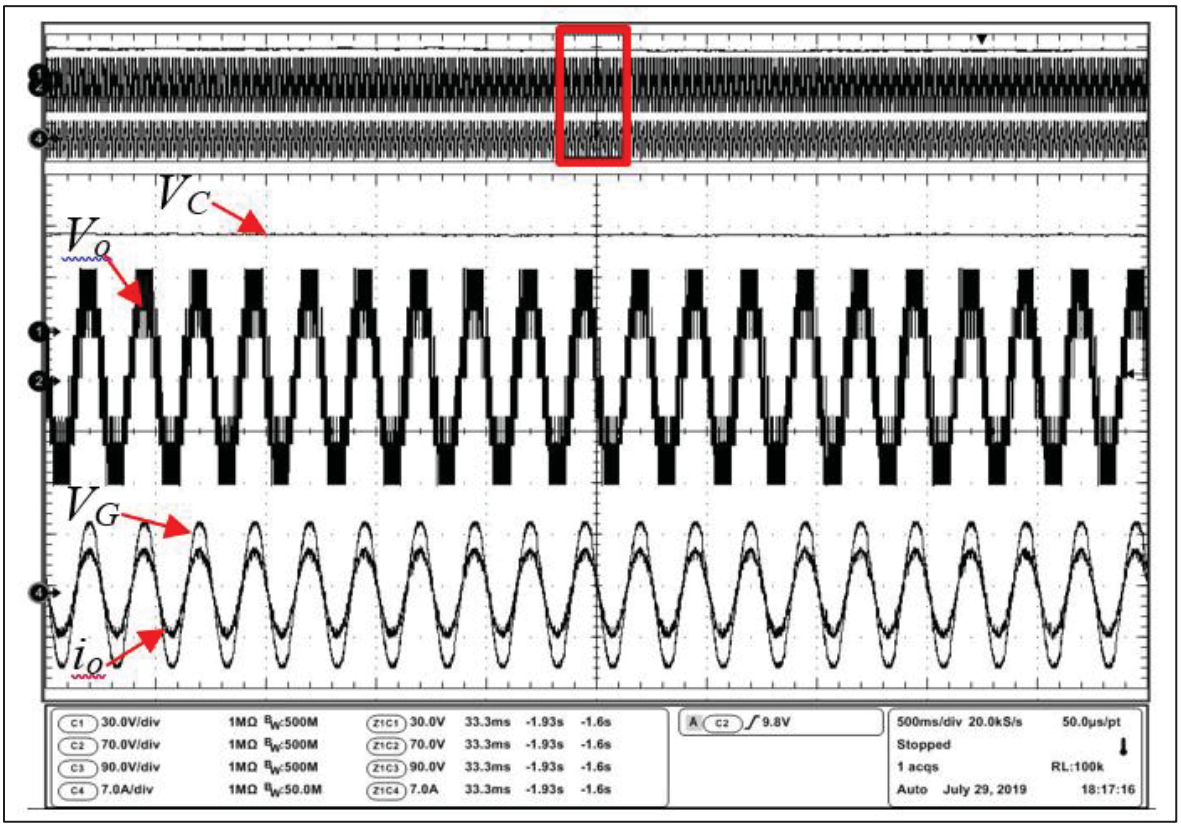

Figure 2.16 Experimental results of the grid-connected PUC7 in steady-state conditions

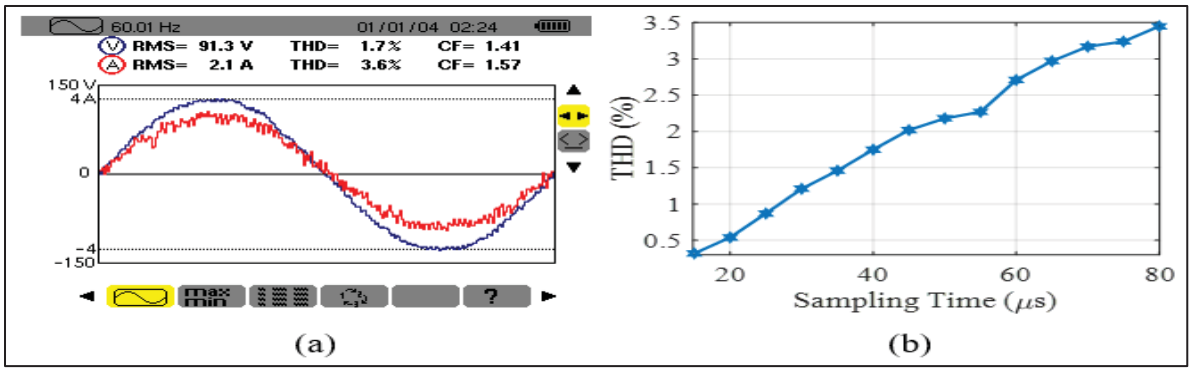

Figure 2.17 Power quality evaluations (a) harmonic spectrum analysis for i_o and V_G, (b) THD analysis of i_o versus sampling time variations for the OSMC algorithm

As depicted in Figure 2.17 (b), increasing the sampling time will increase the THD and vice versa. The results prove that the proposed OSMC generates THD values less than the conventional MPC and PI-based control methods with a similar sampling time.

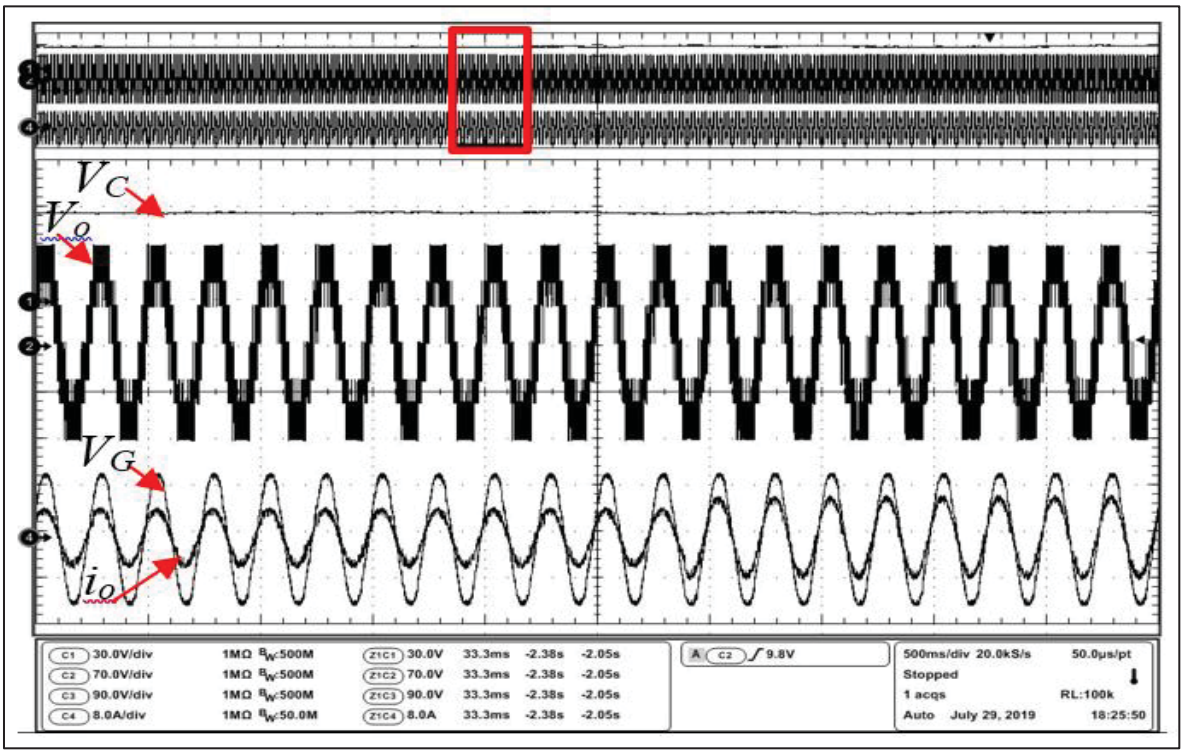

Figure 2.18 Experimental results of the grid-connected PUC7 under the reference current step change

In the second test of the grid-connected PUC7 converter, the OSMC is evaluated under a dynamic mode, where the reference current is increased from 5A to 7A; the related experimental and simulation results are shown in Figure 2.18 and Figure 2.19, respectively. As illustrated in Figure 2.18, the capacitor voltage is constantly self-regulated to one-third of the DC source with minimum voltage ripple. In addition, the simulation results provided in Figure 2.19 depict that the capacitor's voltage is desirably balanced at one-third of the DC source amplitude (160V) with the voltage ripple under 5% during the current reference variation. The comparison analysis presented in Figure 2.20 proves that the injected current precisely tracks the desired reference in the grid-connected mode. A mismatch analysis same as the stand-alone mode is done in Figure 2.21 for the grid filter inductance. Regarding Figure 2.21, the inductance size is changed by ±50% while its effect on the capacitor voltage ripple and the THD of the injected current is negligible. Moreover, (2.18) reveals that C is not involved in the controller; thus, it proves the robustness of the proposed OSMC against the capacitor mismatch.

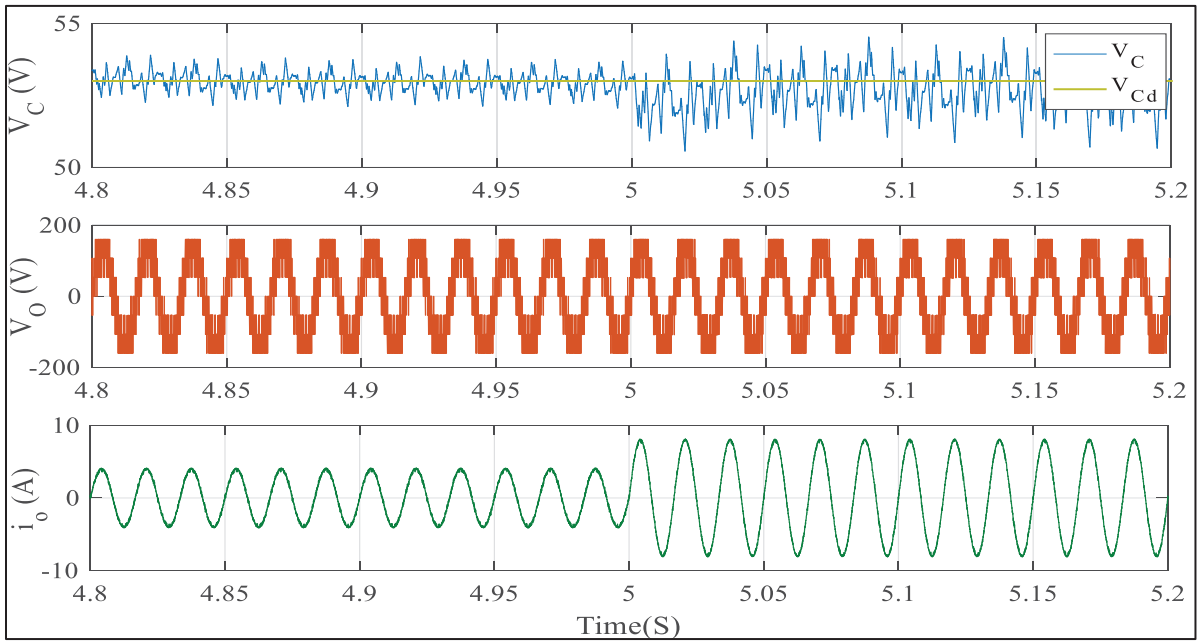

Figure 2.19 Simulation results of the grid-connected PUC7 under reference current step change when T_S=25µs, C=900µF

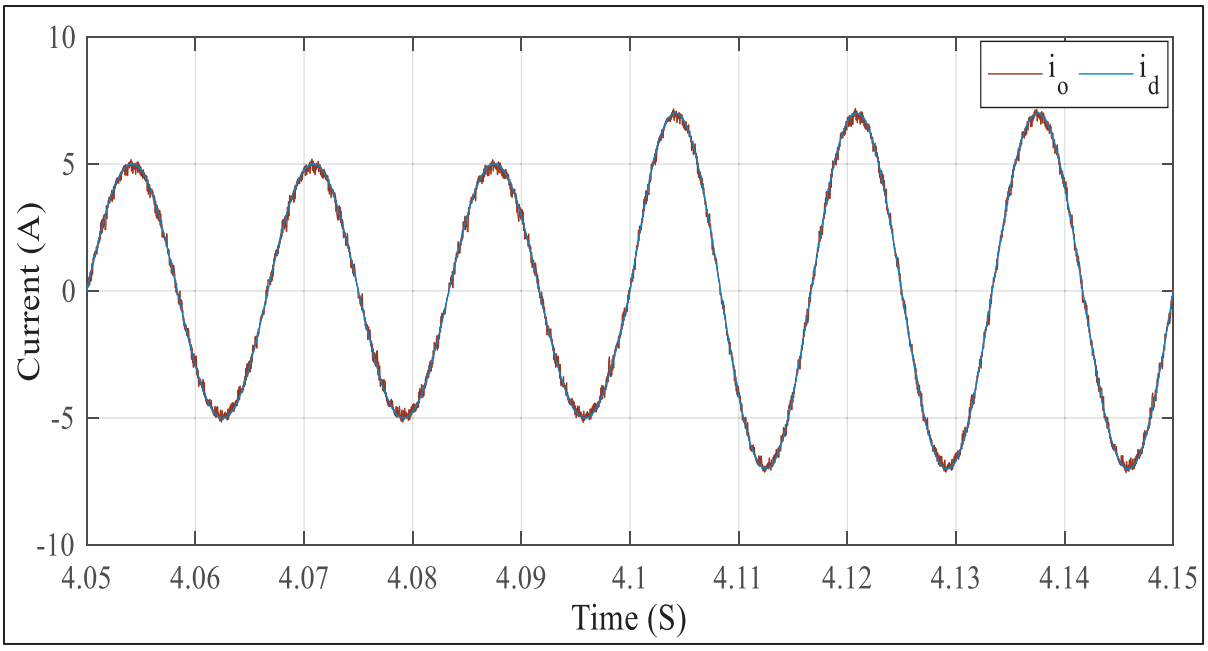

Figure 2.20 Simulation results of the grid-connected PUC7 under reference current step change when T_S=25µs, C=900µF

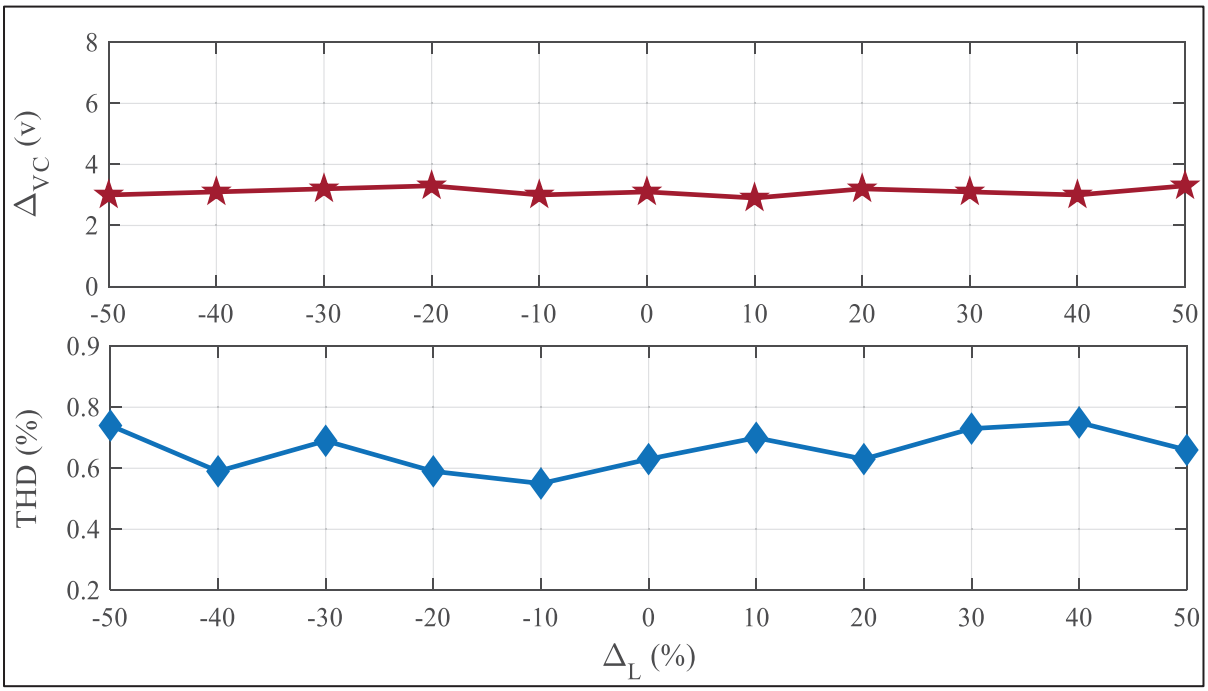

Figure 2.21 Parametric mismatch investigation for the filter inductance in the grid-connected PUC7 with T_S=25µs

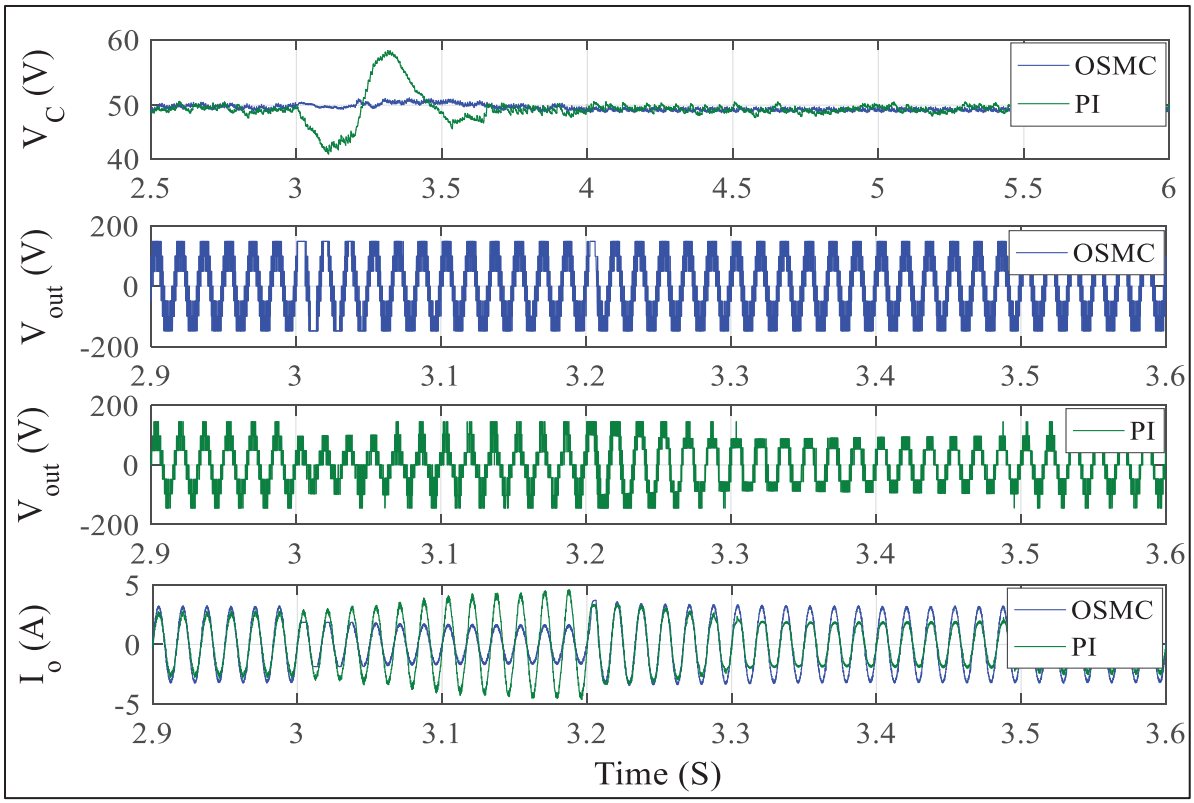

Figure 2.22 Comparison analysis between the cascaded PI controller and the proposed OSMC for the stand-alone mode of operation of the PUC7 converter

2.5.3 Comparison Simulation Results between OSMC and PI

The OSMC performance is also compared with the cascaded controller developed by (Vahedi, & Al-Haddad, 2015) when both control strategies are used for the stand-alone application of PUC7. The system parameters are chosen as V_{dc}=150V and f_{sw}=2kHz. Two PI controllers with control factors as k_{P1}=3, k_{P2}=30, k_{I1}=10, and k_{I2}=0.1 are chosen, as detailed in (Vahedi, & Al-Haddad, 2015). The simulation analysis is performed when the load changes from 80Ω to 40Ω and vice versa; the results are provided in Figure 2.22. As it is obvious, OSMC balances the capacitor's voltage and tracks the desired reference current without transient effects including overshoot/undershoot in the capacitor voltage. Even though PI directly controls the capacitor's voltage, it is not stable in the presence of parametric variations, as a fluctuation appears in the capacitor's voltage and subsequently in the current and the multilevel waveforms. On the other

hand, the current fluctuations are removed by the OSMC while the capacitor voltage is also self-balanced even in the presence of load uncertainty. As depicted in (Vahedi, & Al-Haddad, 2015), the transient effects are destructive when the cascaded controller is practically implemented.

2.6 Conclusion

In this article, it has been proved that the relation between the capacitor's voltage, switching states, and load current in the PUC7 topology is nonlinear. Therefore, OSMC as a switching-based, robust, and adaptive controller was developed to acquire capacitor self-voltage balancing and reference current tracking in both grid-connected and stand-alone modes. According to the OSMC principle, the capacitor's voltage is self-balanced only by tuning the control factor and estimating the nominal current of the load; thus, direct control of the capacitor's voltage is no longer required. Moreover, the mathematical relationships of the capacitor's voltage, load current, and switching operation are developed to design the proposed VBO. The VBO optimizes the control factors without any iteration and initialization. The comprehensive experimental and simulation results of the proposed OSMC confirm its feasibility and robustness even under dynamic modes, nonlinear load, and parametric mismatch.

CHAPTER 3

Supervised Learning Model Predictive Control Trained by ABC Algorithm for Common Mode Voltage Suppression in NPC Inverter

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Abstract

Training the weighting factors of model predictive control in multi-objective problems is a time-consuming and sophisticated process. In this paper, conventional model predictive control (CMPC) is developed as a supervised learning model predictive control (SLMPC) to cancel common mode voltage (CMV) in a three-phase NPC inverter while other control objectives are desirably tracked. SLMPC is accurately and quickly trained through the artificial bee colony (ABC) algorithm to optimize the weighting factors. Using the optimized weighting factors, transient response is minimized and CMV is surpassed. After training the weighting factors, SLMPC containing the optimized waiting factors is applied to the three-phase NPC inverter without considering the ABC algorithm in the control loop. By applying the optimized weighting factors to the cost function, SLMPC has been evaluated under several experimental and simulation tests to show that desired control objectives, particularly CMV suppression, are attained. The proposed training process can be generalized and used for MPCs with more control objectives to obtain the best possible performance.

3.1 Introduction

Nowadays, multilevel converters are known as the new generation of power electronics systems, which can operate in medium and high voltage DC/AC applications due to generating a quasi sinusoidal voltage waveform, smoother output voltage with lower THD and less voltage stress on power switches (Kouro et al., 2010; Franquelo et al., 2008). Multilevel converters have emerged by introducing three-level bidirectional Neutral Point Clamped (NPC) which is one of the most interesting topologies still employed in the industry (Rodriguez, Bernet, Steimer, & Lizama, 2009). NPC utilizes a single DC supply with small capacitors in the DC link and fewer number of capacitors compared to the other three-level topologies. NPC has been employed as a single-phase or three-phase converter in standalone and grid-connected modes of operation controlled by different methods (Rodriguez, Bernet, Steimer, & Lizama, 2009). One of the imposing challenges in three-phase inverters, including NPC topology, is common mode voltage (CMV), which causes serious problems such as voltage stress and overvoltage on power switches, harmonic distortion, bearing and leakage currents, electromagnetic interference, breakdown of motor insulation and motor shaft voltages (Kim, Lee, & Sul, 2001).

To overcome the CMV effects, two general solutions including modulator-based (MB) and control-based (CB) techniques were proposed. The MB techniques such as space vector pulse width modulation (SVPWM) and carrier-based pulse width modulation (CBPWM) eliminate CMV by ignoring some voltage vectors; even so, removing the voltage vectors intensifies harmonic distortion in output voltages and currents and increases capacitor voltages ripple (Chen et al., 2016). Therefore, CMV reduction instead of cancelation was considered in MB techniques proposed by (Ezzeddine et al., 2017, October; Nguyen et al., 2017; Le, & Lee, 2016; Lim et al., 2016; Liu et al., 2017; Sindhu et al., 2017, May; Wang, Zhai, Wang, Jiang, Li, Li, & Huang, 2018; Xing, Li, Gao, Qin, & Zhang, 2018; Wang, Cui, Zhang, Shi, & Xia, 2016) to satisfy different control objectives. But, the CMV reduction methods designed by (Ezzeddine et al., 2017, October; Nguyen et al., 2017; Le, & Lee, 2016; Lim et al., 2016; Liu et al., 2017; Sindhu et al., 2017, May; Wang, Zhai, Wang, Jiang, Li, Li, & Huang, 2018; Xing, Li, Gao,

Qin, & Zhang, 2018; Wang, Cui, Zhang, Shi, & Xia, 2016) need to combine various MB strategies with supplementary features for supporting dynamic modes in a complete range of modulation index (Chen et al., 2016). MB techniques also need CMV filters to improve power quality in some practical applications whereas these additional components increase the converter cost (Chen et al., 2016).

Despite proposed MB techniques, different targets are simultaneously tracked in CB strategies by designing proper control laws based on the dynamic model of the system without discarding any voltage vector. Model predictive control is a well-known class of CB techniques designed based on a discrete model of the inverter and selects the best switching vector in the next sampling time according to the control objectives defined in the cost function. MPC does not need a modulator since the proper switching vector is selected directly by minimizing its cost function (Kouro, Cortés, Vargas, Ammann, & Rodríguez, 2008; Vazquez et al., 2014). Since several control objectives can be easily involved in the MPC cost function, it has been utilized in different converters for various applications (Vazquez et al., 2014). However, allocating the optimal values to the cost function weighting factors significantly affects the efficiency of MPC techniques in tracking control objectives (Cortés et al., 2009, February). Even though empirical methods like trial and error are still used to set the weighting factor, they provide a very time-consuming and inaccurate training process, which cannot guarantee the optimized performance of MPC to track desired objectives (Karamanakos et al., 2019). Moreover, training by empirical methods becomes more complicated when several weighting factors related to different independent control objectives are considered in the cost function (Uddin et al., 2017, November; Rubinic et al., 2015, September). Acquired results provided by (Saeed et al., 2016, February; Kakosimos, & Abu-Rub, 2017; Dabour et al., 2017, December; Hoseini, Adabi, & Sheikholeslami, 2014; Wang, Fang, Lin, Lin, & Yang, 2019; Xing, & Chen, 2019) show that using empirical methods for tuning the weighting factors leads to CMV reduction instead of cancelation due to the nonlinear relation, which existed among the objectives defined in the cost function. Indeed, the nonlinear relation of control objectives in the cost function cannot be easily covered by the empirical techniques to optimize the weighting factors.

In this paper, MPC is trained for a three-phase NPC inverter as a supervised learning MPC (SLMPC) with optimized weighting factors to suppress CMV, regulate the DC link voltage, and track the reference current. In the proposed SLMPC technique, the artificial bee colony (ABC) algorithm with multi-objective optimization capability is used to supervise the learning process of MPC. Fast convergence rate and ignoring local minimums are the appealing advantages of the ABC algorithm. In the proposed supervised training procedure, the model predictive control loop, including the NPC inverter, is placed in the ABC optimization loop in MATLAB/Simulink environment to desirably adjust the weighting factors after several iterations of the optimization process. The main criteria to evaluate the performance of the optimization loop are error functions defined based on the CMV suppression, capacitors voltages regulation, and tracking of the load reference current. Therefore, the ABC training loop will be continued until the error functions are minimized. Afterward, the supervised ABC-based tuner is removed from the main control loop. The trained MPC as SLMPC is then implemented to track the desired control objectives defined for the three-phase NPC inverter.

The simulation and experimental results of implementing the SLMPC technique with optimized weighting factors confirm the complete CMV suppression, the accurate reference current tracking, and capacitors voltage balancing with small ripple and fast dynamic response during steady-state and variable-state conditions.

In Section 3.2 the NPC topology is discussed and modeled in terms of three-phase currents, capacitors' voltages, and CMV. The MPC technique is detailed and designed in Section 3.3. The proposed supervised training loop and SLMPC technique are discussed in Section 3.4. Section 3.5 also presents the experimental and simulation results of the SLMPC applied to the three-phase NPC inverter. Conclusions are also presented in Section 3.6.

3.2 Three-Phase NPC Topology and Modeling

The three-phase NPC configuration is illustrated in Figure 3.1. Each leg represents one phase and produces a three-level branch voltage measured between the output terminals (*A*, *B*, and

C) and the neutral point of the DC link (*g*) as V_{Ag}, $V_{Bg,}$ and V_{Cg}. Table 3.1 lists the corresponding switching states of each leg of the three-phase NPC inverter to generate the three-level voltage waveform.

Table 3.1 Switching vectors and voltage levels generated by NPC

States	Switching Sing	S_{x1}	S_{x2}	S_{x3}	S_{x4}	V_{out}
1	+	1	1	0	0	$+V_{DC}/2$
2	neutral	0	1	1	0	0
3	-	0	0	1	1	$-V_{DC}/2$

The equal number of switching states for all legs provides 27 switching vectors for the three-phase NPC as illustrated in Figure 3.2. Regarding Figure 3.2, similar vectors for the same voltage level like (0, 0, 0), (-, -, -), (+, +, +) at the zero, are called redundant states. In addition to CMV, the dynamic model of the load current and capacitors' voltages of the three-phase NPC inverter are also required to guarantee proper tracking of the reference current and DC link voltage balancing when CMV is suppressed.

3.2.1 Load currents modeling

The three-phase load currents (i_a, i_b, and i_c) are modeled based on the three-phase voltages V_{An}, V_{Bn}, and V_{Cn}. The phase voltages of the inverter are expressed with respect to the branch voltages and common mode voltage as shown in (3.1). CMV is also measured between the common point of loads (*n*) and the neutral point of DC link (*g*), V_{ng}, as depicted in Figure 3.1.

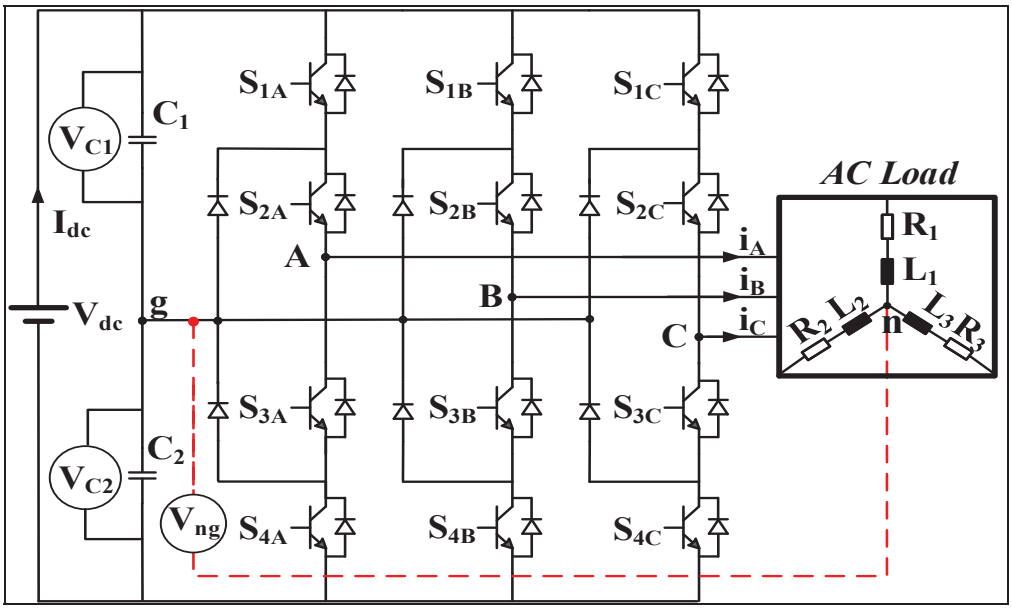

Figure 3.1 Three-phase, three-level NPC topology

$$\begin{cases} V_{an} = V_{ag} - V_{ng} \\ V_{bn} = V_{bg} - V_{ng} \\ V_{cn} = V_{cg} - V_{ng} \end{cases} \tag{3.1}$$

By applying the KVL law from the outputs of the inverter to the common point of load (n), the dynamic model of the load current is achieved in (3.2).

$$\begin{cases} L\dfrac{di_a}{dt} + Ri_a = V_{ag} - V_{ng} \\ L\dfrac{di_b}{dt} + Ri_b = V_{bg} - V_{ng} \\ L\dfrac{di_c}{dt} + Ri_c = V_{cg} - V_{ng} \end{cases} \tag{3.2}$$

where L and R are respectively inductance and resistance of the load. To simplify the calculations of the MPC technique in the three-phase system, the dynamic model of the load currents acquired in (3.2) is transformed into $\alpha\beta$-model using (3.3), (3.4).

$$\begin{cases} V_{\alpha\beta} = \frac{2}{3}\left(V_{ag} + aV_{bg} + a^2V_{cg}\right) \\ i_{\alpha\beta} = \frac{2}{3}\left(i_a + ai_b + a^2i_c\right) \\ a = e^{j\frac{2\pi}{3}} = -\frac{1}{2} + j\frac{\sqrt{3}}{2} \end{cases} \tag{3.3}$$

where α is the unit vector and describes the phase shift of 120° among the three-phase voltages and currents; $V_{\alpha\beta}$ is chosen from the 27 voltage vectors depicted in Figure 3.2.

$$L\frac{di_{\alpha\beta}}{dt} + Ri_{\alpha\beta} = V_{\alpha\beta} - V_{ng} \tag{3.4}$$

Despite the presence of CMV in (3.1) and (3.2), it is removed in Eq. (3.5) when the dynamic model of the load currents is defined in the $\alpha\beta$ frame.

$$L\frac{di_{\alpha\beta}}{dt} + Ri_{\alpha\beta}\frac{2}{3}\left(1 + a + a^2\right) = 0 \tag{3.5}$$

Thus, the dynamic model of the load currents in (3.4) is eventually presented in the form of the $\alpha\beta$-model as detailed in (3.6).

$$L\frac{di_{\alpha\beta}}{dt} = -Ri_{\alpha\beta} + V_{\alpha\beta} \tag{3.6}$$

3.2.2 Capacitor Voltage Modeling

DC link voltage balancing is one of the main objectives that should be considered in the control equations for three-phase NPC.

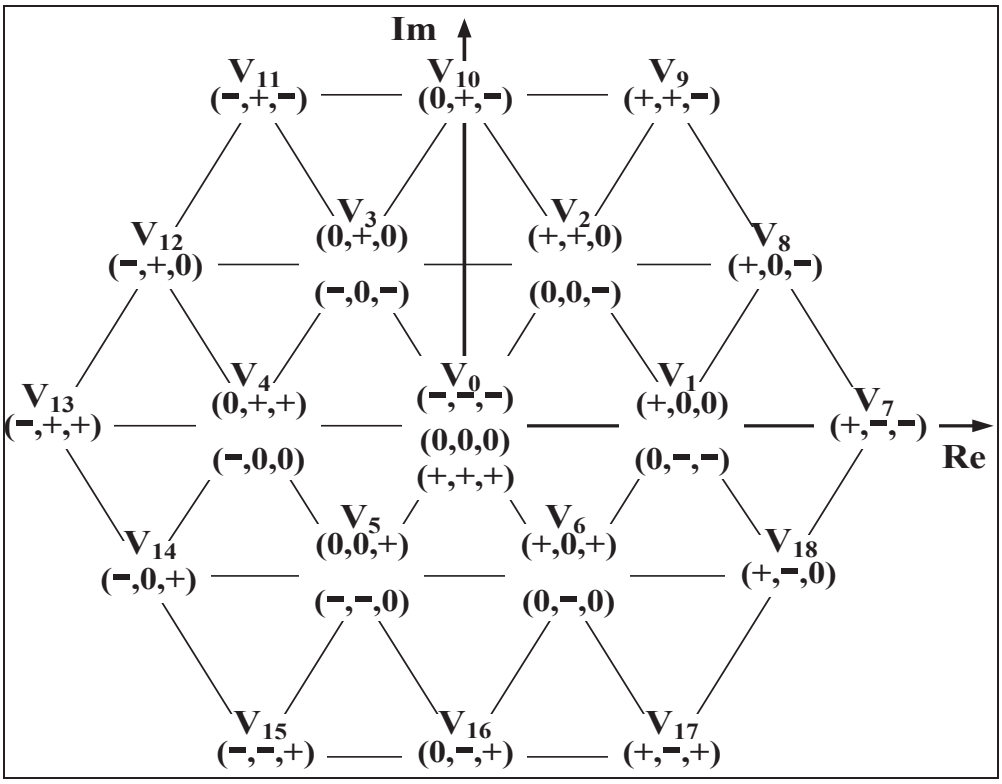

Figure 3.2 The voltage vectors of the three-phase three-level NPC inverter

Accordingly, the dynamic model of capacitors' voltages is defined in (3.7) where C is the capacitance; V_{C1}, V_{C2}, i_{C1}, and i_{C2} are also the capacitors' voltages and currents, respectively.

$$\begin{cases} C\ \dfrac{dV_{C_1}}{dt} = i_{C_1} \\ C\ \dfrac{dV_{C_2}}{dt} = i_{C_2} \end{cases} \tag{3.7}$$

3.2.3 Common Mode Voltage Modeling

CMV is defined between the midpoint of the DC link (g) and the neutral point of the load (n). By simplifying the right and left sides of (3.2), the dynamic model of CMV is attained as below:

$$V_{ag} + V_{bg} + V_{cg} = L \frac{d}{dt}(i_a + i_b + i_c) + R(i_a + i_b + i_c) + 3\mathrm{V_{ng}} \tag{3.8}$$

Since the summation of the three-phase balanced currents is zero, the CMV model can be simplified as below:

$$V_{ng} = \frac{V_{ag} + V_{bg} + V_{cg}}{3} \tag{3.9}$$

Regarding the control objectives, MPC is defined using the dynamic models of the load currents, capacitors' voltages, and CMV. The conventional MPC (CMPC) is designed in the next section; however, it cannot suppress CMV because of the non-optimized weighting factors. Thus, it is improved as supervised learning MPC (SLMPC) in this article. Indeed, the SLMPC is a trained version of CMPC, in which the optimized weighting factors are attained using the proposed ABC optimization loop to achieve CMV elimination.

3.3 Model Predictive Control for Multi-Objective Implementation

According to the MPC design procedure, a cost function is first formalized based on the model of the inverter in terms of the three-phase currents, voltages, switching frequency, CMV, or even harmonics. Then, the best switching vector among all possible ones is selected to minimize the cost function per each sampling time. Since the load currents; capacitors' voltages and CMV are assumed to be control objectives, the cost function is defined as below:

$$G = \lambda_1 g_1 + \lambda_2 g_2 + \lambda_3 g_3 \tag{3.10}$$

where g_1, g_2, and g_3 are respectively defined to track the reference current, regulate the capacitors' voltages, and eliminate CMV. λ_1, λ_2, and λ_3 are also the corresponding weighting factors to adjust the impact of each term on the cost function. Considering the load current model defined in (3.6) and k as the current sampling time, g_1 is defined in (3.11).

$$g_1 = \left| I^*_\alpha(k) - I^p_\alpha(k+1) \right| + \left| I^*_\beta(k) - I^p_\beta(k+1) \right| \tag{3.11}$$

where $I^*_\alpha(k)$ and $I^*_\beta(k)$ are the real and imaginary parts of the reference current; $I^p_\alpha(k+1)$ and $I^p_\beta(k+1)$ are also the real and imaginary parts of the predicted current calculated through the load current model presented in (3.6). Afterward, the discrete model of the load current is computed as shown in (3.12) by employing the Euler-forward equation ($\frac{di}{dt}=\frac{i(k+1)-i(k)}{T_s}$) at T_s. $V_{\alpha\beta}(k)$ is also the $\alpha\beta$-voltage vector selected among the ones shown in Figure 3.2.

$$I^p_{\alpha\beta}(k+1) = (1 - \frac{RT_s}{L})i_{\alpha\beta}(k) + \frac{T_s V_{\alpha\beta}(k)}{L} \tag{3.12}$$

where g_2 is considered to control capacitors' voltages of the DC link. The predictive model of the voltages is defined with respect to (3.7) and the Euler-forward equation, as (3.13).

$$\begin{cases} V^p_{C_1}(k+1) = V_{C_1}(k) + \dfrac{1}{C}\ i_{C_1}(k)T_s \\ V^p_{C_2}(k+1) = V_{C_2}(k) + \dfrac{1}{C}\ i_{C_2}(k)T_s \end{cases} \tag{3.13}$$

where $V^P_{C1}(k+1)$, $V^P_{C2}(k+1)$ and $i_{C1}(k)$, $i_{C2}(k)$ are the predicted capacitors' voltages and currents, where the capacitors' currents depend on the switching states and the load currents as shown in (3.14).

$$\begin{cases} i_{C_1}(k) = i_{dc}(k) - H_A i_a(k) - H_B i_b(k) - H_C i_c(k) \\ i_{C_2}(k) = i_{dc}(k) + H_A i_a(k) + H_B i_b(k) + H_C i_c(k) \end{cases} \tag{3.14}$$

where i_{dc} is the measured dc source current, H_A, H_B, and H_C are the switching functions of NPC defined as below:

$$H_A = \begin{cases} 1 \\ 0 \end{cases}, \; H_B = \begin{cases} 1 \\ 0 \end{cases}, \; H_C = \begin{cases} 1 \\ 0 \end{cases} \tag{3.15}$$

In the case of g_3, the predicted model of CMV is employed in (3.16) using the switching functions defined in (3.15) based on the predicted equations of the branch voltages defined in (3.17).

$$V_{ng}^{p} = \frac{V_{ag}^{p} + V_{bg}^{p} + V_{cg}^{p}}{3} \tag{3.16}$$

$$V_{ag}^{p} = H_A \frac{V_{dc}}{2}, \quad V_{bg}^{p} = H_B \frac{V_{dc}}{2}, \quad V_{cg}^{p} = H_C \frac{V_{dc}}{2} \tag{3.17}$$

By substituting (3.11), (3.13), and (3.16) into (3.10) the cost function for CMV-based multi-objective control is obtained in (3.18).

$$\begin{aligned} G_{MPC} = {} & \lambda_1^{CMPC}\left(\left| I_{\alpha}^{*}(k) - I_{\alpha}^{p}(k+1) \right| + \left| I_{\beta}^{*}(k) - I_{\beta}^{p}(k+1) \right| \right) \\ & + \lambda_2^{CMPC} \left| V_{C_1}^{p}(k+1) - V_{C_2}^{p}(k+1) \right| + \lambda_3^{CMPC} \left| V_{ng}^{P} \right| \end{aligned} \tag{3.18}$$

Figure 3.3 illustrates the block diagram of the CMPC with the cost function presented in (3.18). the Effective performance of the CMPC in controlling the targeted objectives (g_1, g_2, g_3) is highly related to the proper selection of the weighting factors (λ_1^{CMPC}, λ_2^{CMPC}, λ_3^{CMPC}). The CMPC weighting factors are usually determined by empirical methods, which leads to non-optimized performance. To overcome the imposed drawbacks of CMPC, the SLMPC is proposed in the next section to find optimal values of the weighting factors.

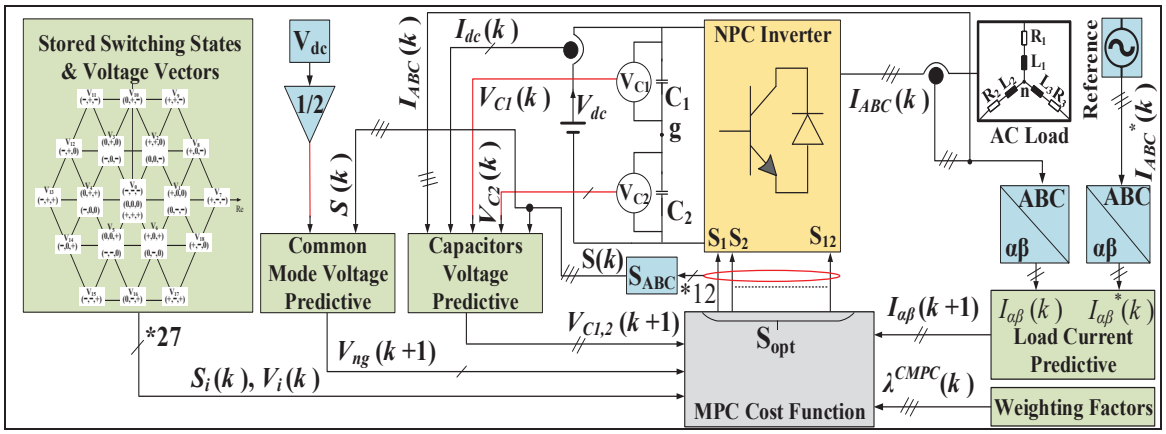

Figure 3.3 Block diagram of CMPC technique applied to the NPC inverter

3.4 Supervised Learning Model Predictive Control for Optimizing the Weighting Factors

Adjusting the weighting factors using empirical methods, such as trial and error, is possible when the MPC cost function is made by two terms, like the capacitor's voltage and load current. Indeed, the voltages of the capacitors described in (3.14) depend on the load currents; thus, accurate tracking of the reference current also results in better voltage balancing. However, involving independent control objectives like CMV in the cost functions and using several weighting factors causes a complicated optimization process, which cannot be easily solved by empirical techniques. It is clear that using an empirical method to set the weighting factors is a time-consuming procedure and leads to non-optimal results (Cortes et al., 2010; Karamanakos, & Geyer, 2019). Alternatively, the weighting factors in multi-objective control problems can be tuned through artificial intelligent-based optimization methods, such as the ABC algorithm. Thus, the desired control objectives can be ensured by the optimal performance of the MPC. Since the MPC is in a training process supervised by an intelligent algorithm, the obtained MPC is called supervised learning model predictive control (SLMPC).

3.4.1 Multi-Objective Artificial Bee Colony Algorithm

To train the CMPC and obtain the optimal values for the weighting factors, the ABC algorithm is considered. The ABC is a metaheuristic optimization algorithm established based on the

swarm intelligence of honey bees. Fast convergence and multi-objective optimization capability are the prominent features of ABC achieved by the unique behavior of bees (Karaboga et al., 2014). The bees are classified into three groups including employed, onlooker, and scout. Bees are assigned to random areas in the search space of the optimization problem and then they look for nectar as the possible solution to the problem. The ABC algorithm consists of four steps described as follows:

a) *Initializing Stage*: For a problem with a D dimension, N number of foods (nectar) are randomly quantified as the possible solutions. Positions of foods are also defined by (3.19).

$$X_{ij}=x_j^{\min}+\ \text{rand}(0,\ 1)(\text{x}_j^{\max}\ -\ \text{x}_j^{\min}),\ \ i=1,\ ...,\ N,\ \&\ \ j=1,\ ...,\ D \tag{3.19}$$

where x_j^{max} and x_j^{min} are respectively the lower and upper bounds of possible values, which can be chosen as foods.

b) *Employed Bee Stage*: In this step, one employed bee is allocated to each food. Then, the employed bees search among the foods and neighborhoods to find new sources using (3.20).

$$V_{ij}\ =\ x_{ij}\ +\ \varphi(x_{ij}\ -\ x_{rj}) \tag{3.20}$$

where V_{ij}, x_{ij}, x_{rj}, and φ are the new food, current food, random food, and a random amount between [-1 1], respectively. Then, the original and new foods found by the employed bees are evaluated through an objective function (f_i) to calculate the fitness (P_i) of bees, using (3.21). A counter as a Limit Index (LI) for each bee's movement is also defined to remove foods with big cost values. Thus, the related bee returns to the previous food, and its performance index increases for one unit.

$$fit_i\ =\ \begin{cases} \dfrac{1}{1+f_i} & f_i\ >\ 0 \\ 1+\left|\,f_i\,\right| & f_i\ <\ 0 \end{cases},\qquad P_i\ =\ \frac{fit_i}{\sum_{i=1}^{N} fit_i} \tag{3.21}$$

c) *Onlooker Bee Stage*: Based on the overall employed bees' fitness calculated by (3.21), the onlooker bees select the best foods found by employed bees and then search around them to find new foods with better fitness. It should be noted that the onlookers are the same as employed bees; they use (3.20) to find new foods and they have a limit index.

d) *Scout Bee Stage*: When the *LI* for an employed or onlooker bee exceeds a level (because of choosing foods with weak fitness), the bee is transformed to scout one and it moves to a random food determined by (3.19) to find a better solution. The quadruple stages are continued until the stop conditions of the ABC algorithm are satisfied.

3.4.2 Training the CMPC Using the ABC Algorithm

As depicted in Figure 3.4, the ABC optimization loop operates in parallel to the MPC control loop to train the weighting factors. ABC requires to be first initialized by parameters listed in Table 3.2.

Table 3.2 Initial parameters of the optimization loop

No. of Bees	**No. of Foods**	**Limit Index**	**Iteration**	$\boldsymbol{\lambda_{1,2,3}}$	$\boldsymbol{\mu_{1,2,3}}$	$\boldsymbol{t_f}$
40	20	7	10	[0 0.9]	1.5, 1.5, 2	0.3

According to Table 3.2, 20 foods (i=1, … ,20) with three dimensions (j=1, 2, 3) are randomly initialized by (3.22) as candidate values for λ_1, λ_2, and λ_3. Possible values of the foods are restricted to [0 1] as an acceptable range for the weighting factors.

$$P_i = \frac{fit_i}{\sum_{i=1}^{N} fit_i} \quad \begin{cases} \lambda_{ij}(k) = \lambda_j^{\min} + \text{rand}(0,\ 1)(\lambda_j^{\max} - \lambda_j^{\min}) \\ i=1,\ \ldots,\ 20\ \&\ j=1,\ 2,\ 3 \end{cases} \tag{3.22}$$

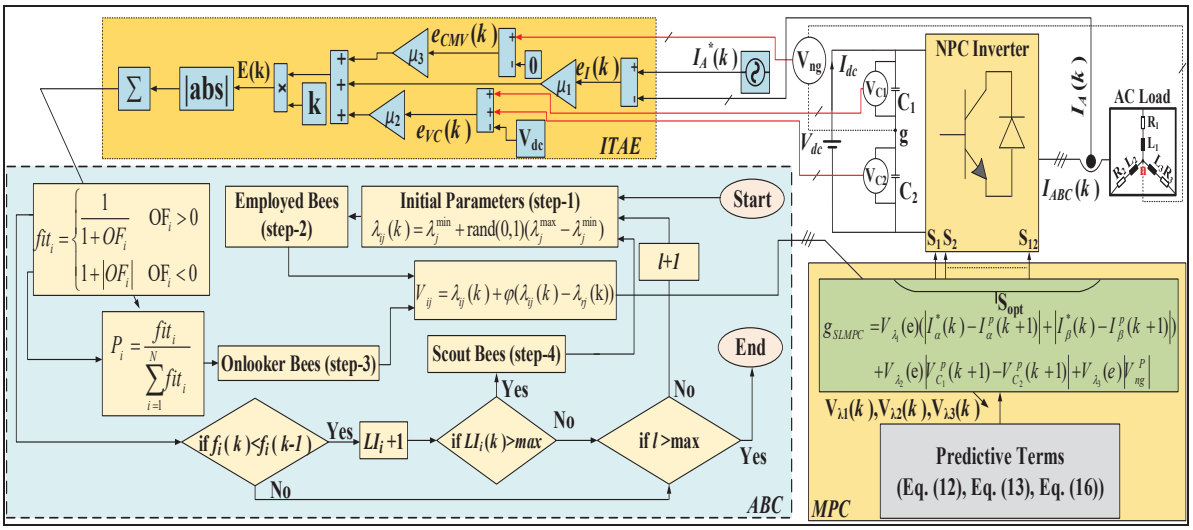

Figure 3.4 Training block diagram of MPC technique based on the ABC algorithm

Forty particles, including 20 employed and 20 onlooker bees, are assigned to the initialized foods generated by (3.22) and their neighborhoods using (3.23) to modify the initial weighting factors in each iteration of the ABC optimization loop.

$$\begin{cases} V_{i1} = \lambda_{i1}(k) + \varphi(\lambda_{i1}(k) - \lambda_{r1}(\mathrm{k})), & i=1, \ldots, 20 \\ V_{i2} = \lambda_{i2}(k) + \varphi(\lambda_{i2}(k) - \lambda_{r2}(\mathrm{k})), & i=1, \ldots, 20 \\ V_{i3} = \lambda_{i3}(k) + \varphi(\lambda_{i3}(k) - \lambda_{r3}(\mathrm{k})), & i=1, \ldots, 20 \end{cases} \tag{3.23}$$

where V_{i1}, V_{i2}, and V_{i3} are some functions used to update λ_1, λ_2, and λ_3, respectively. The updated foods in each iteration are substituted into the cost function as the new weighting factors. Afterward, the fitness function (P_i) defined in (3.24) is calculated for the ith food in the lth iteration to determine the cost for each food applied to the cost function as the weighting factors. P_i is calculated based on an objective function (OF) used in the ABC to measure the performance of the NPC controlled by MPC. Thus, OF should provide an accurate description of the control loop performance for the ABC optimization; Regarding this fact, the following equation is suggested.

$$fit_i = \begin{cases} \dfrac{1}{1 + OF_i} & OF_i > 0 \\ 1 + \left| OF_i \right| & OF_i < 0 \end{cases}, \qquad P_i = \frac{fit_i}{\sum_{i=1}^{N} fit_i} \tag{3.24}$$

where OF_i is the ABC objective function (OF) calculated for all foods during each iteration. Integral of time-weighted absolute error (ITAE) is chosen as the ABC objective function to evaluate the control loop performance in terms of transient response and steady-state error for the measured parameters, like CMV, DC link voltages, and three-phase currents. The ITAE as the proposed objective function of the ABC is defined in (3.25) to calculate P_i.

$$OF(E(t)) = \int_0^{t_f} t \left| E(t) \right| dt \tag{3.25}$$

where $E(t)$ is an error function related to the control objectives, and t is the sampling time of the error signal. t_f is also the time window of the ABC for training the weighting factors per each food applied to the MPC cost function in each iteration. ITAE calculates OF using $E(t)$; therefore, steady and transient errors have a major impact on the optimization process. In fact, optimization of the weighting factors based on the ITAE leads to a fast transient response of the controller with minimum steady-state error in tracking the reference current, regulating the voltages besides CMV cancellation. The accuracy of ITAE for evaluation of the control loop performance directly depends on t_f and $E(t)$. Accordingly, t_f must be selected large enough so that all transient dynamics are sampled. Moreover, $E(t)$ should adequately measure the error of the control objectives. Since the weighting factors directly affect the optimization performance of the MPC, $E(t)$ is defined based on the control objectives, as shown in (3.26), to measure the effects of the ABC optimization loop on the control performance.

$$E(t) = \mu_1 e_{i_a}(t) + \mu_2 e_{V_C}(t) + \mu_3 e_{Vng}(t) \tag{3.26}$$

where $e_{ia}(t)$, $e_{Vc}(t)$, and $e_{Vng}(t)$ are the tracking errors between (i_a and i^*_a), (V_{C1} and V^*_{C1}), and (V_{ng} and V^*_{ng}), respectively. V^*_{ng} is the desired reference for CMV, which is zero. i^*_a and V^*_{C1}

are the desired references for the current in phase-A and the voltage of C_1. By obtaining the desired amplitude for i_a and V_{C1}, other phase currents and voltage will follow their reference. In addition, three coefficients, including μ_1, μ_2, and μ_3 are defined in (3.26) to intensify the corresponding terms. According to (3.13) and (3.14), the phase currents affect the capacitors' voltages; thus, their corresponding coefficients including μ_1 and μ_2 are considered equally. However, μ_3 has to be selected larger to suppress CMV by amplifying its error in the ABC optimization process. Thus, the coefficients of the error functions in (3.26) should be adjusted as shown in (3.27). Although the weighting factors are tuned by the same objective function, the coefficients prioritize the error terms ($e_{ia}(t)$, $e_{Vc}(t)$, $e_{Vng}(t)$) defined in (3.26). Therefore, ABC mainly focuses on minimizing errors with larger coefficients.

$$\mu_3 > \mu_1, \quad \mu_2, \text{ where } \mu_1 = \mu_2 \tag{3.27}$$

The selected coefficients in (3.27) are shown in Table 3.2; μ_1, and μ_2 magnify e_{ia} and e_{Vc} to minimize the steady-state error in phase currents and capacitors' voltages. In addition, μ_3 is selected larger to suppress CMV as the main objective. By calculating the fitness of the foods using (3.24), the onlooker bees are assigned to foods with the minimum cost to modify them using (3.23) to provide further optimal solutions. Thus, similar to the employed bees, the weighting factors are updated by the new foods in the third step. In the fourth step, *LI* in all employed and onlooker bees is checked so that bees with exceeded index are transformed to scout bees and reinitialized by (3.22). Therefore, the newly employed bees find more optimized values for the weighting factors. At the end of all iterations, a food with minimum fitness in all employed, onlooker, and scout bees is selected as the best-optimized vector for the weighting factors. Finally, after 10 iterations the weighting factors are optimized as λ_1^{SLMPC}=0.8217, λ_2^{SLMPC}=0.3226, and λ_3^{SLMPC}=0.3515.

Simulation results of the weighting factor variations during the training process are depicted in Figure 3.5. This figure shows that in eight epochs the weighting factors are optimized. Moreover, the brown curve in Figure 3.6 shows the variations of the OF defined in (3.25) during all iterations. The OF plotted in Figure 3.6 is significantly large because the ITAE

function gathers the sampled data in a wide time window (t_f). However, $E(t)$ plotted as the blue curve in Figure 6 illustrates satisfactory results in acquiring minimum total error to track the desired reference of load currents, capacitors' voltage, and CMV.

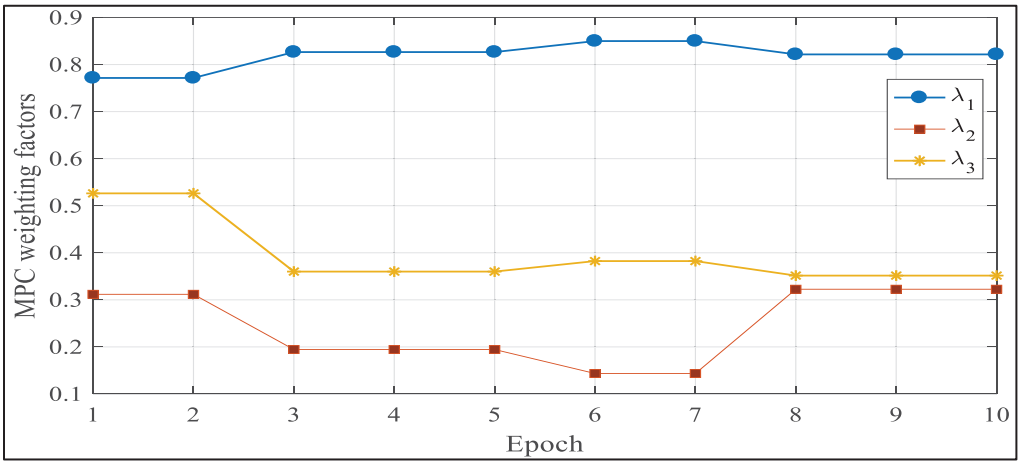

Figure 3.5 Variations of the weighting factors during all epochs

When the optimized weighting factors are obtained, the ABC optimization loop is removed from the main control loop of the NPC. The new cost function of SLMPC including the optimized weighting factors ($\lambda_{1,2,3}^{SLMPC}$) is formulated in (3.28).

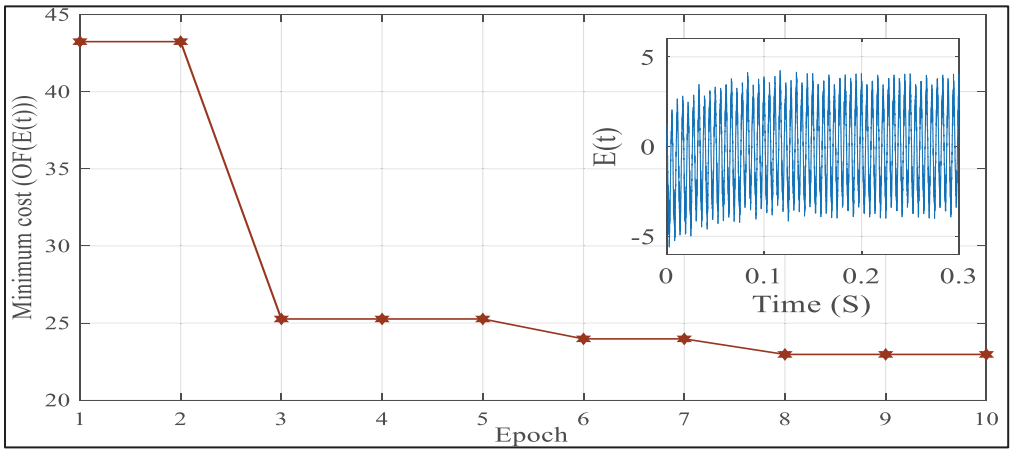

Figure 3.6 ABC objective function (OF) during ten iterations (brown curve) and the variations of $E(t)$ under the optimized weighting factors (blue curve)

3.4.3 Implementation of SLMPC on Three-Phase NPC Inverter

$$G_{SLMPC} = \lambda_1^{SLMPC}\left(\left| I_\alpha^*(k) - I_\alpha^p(k+1)\right| + \left| I_\beta^*(k) - I_\beta^p(k+1)\right|\right) + \lambda_2^{SLMPC}\left|V_{C_1}^p(k+1) - V_{C_2}^p(k+1)\right| + \lambda_3^{SLMPC}\left|V_{ng}^P\right| \quad (3.28)$$

Figure 3.7 illustrates the schematic diagram of the SLMPC controller. As shown, the three-phase and DC source currents are measured beside the voltages of the capacitors. Then, the measured values are applied to the SLMPC to select the best switching vector during each sampling period.

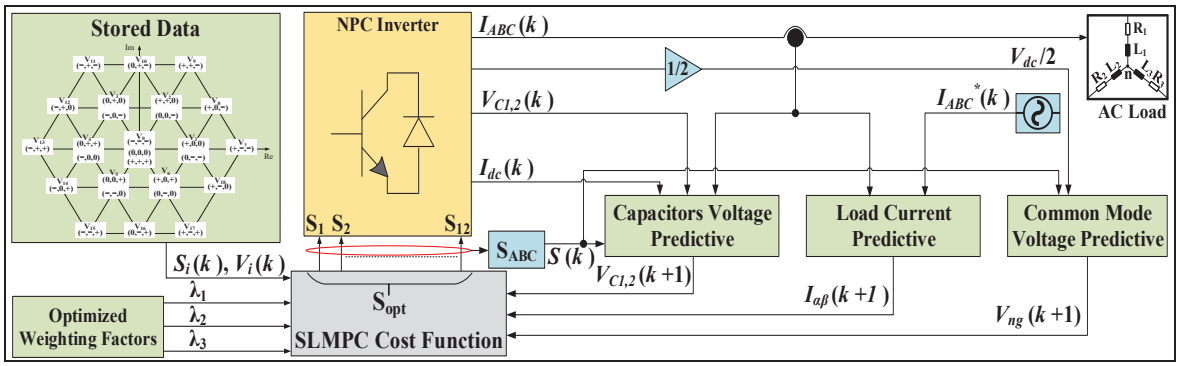

Figure 3.7 Block diagram of SLMPC applied to the NPC inverter

3.5 Experimental and Simulation Results

In this section, the experimental and simulation results of applying different test scenarios to the three-phase NPC controlled by SLMPC and CMPC techniques are provided. These tests have been planned to confirm the accuracy of the optimized weighting factors in achieving the control aims, including CMV suppression, capacitor voltage balancing, and reference current tracking. The system parameters used in the experimental and simulation setups are listed in Table 3.3. In addition, the SLMPC shown in Figure 3.7 has been implemented through dSPACE 1104, as the real-time hardware controller. Figure 3.8 presents the experimental setup.

Table 3.3 Experimental and simulation test parameters

DC source voltage (V_{dc})	300 V
DC link capacitor (C_1, C_2)	650 µF
AC load inductor & resistor (R_L, L_L)	40 Ω & 20 mH
Experimental and Simulation sampling time	45 µs, 20 µs
Fundamental and switching frequency	60 Hz

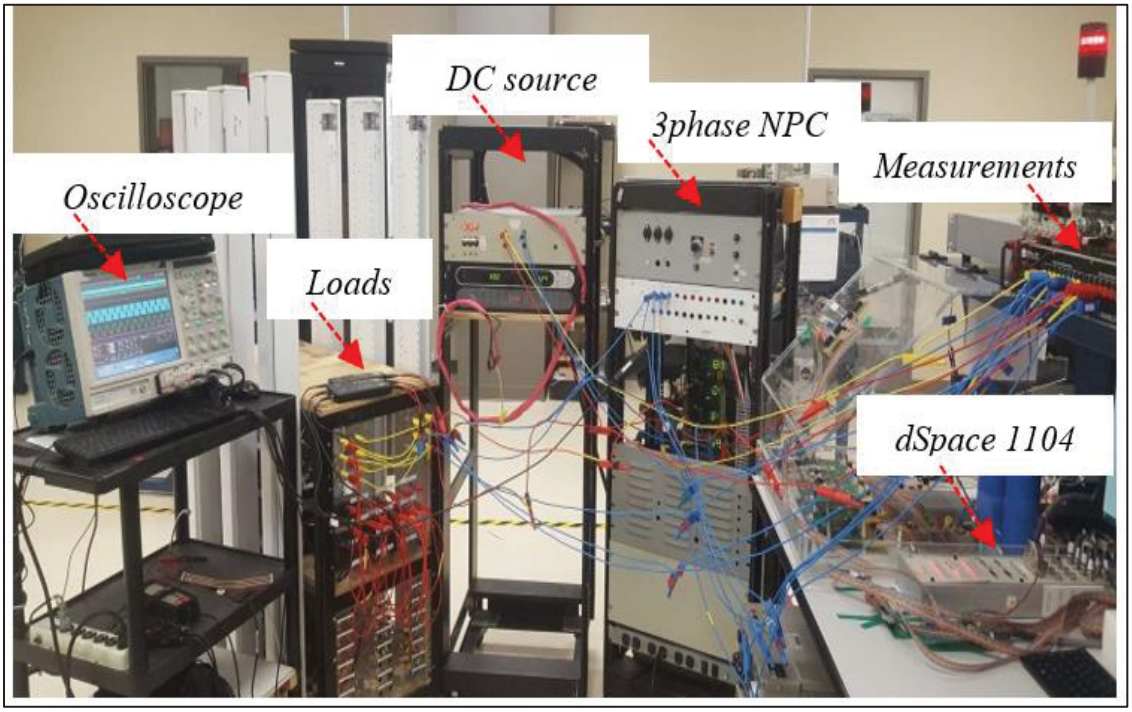

Figure 3.8 Experimental setup of the system including the dSPACE 1104, oscilloscope, load bank, DC power supply, and OPAL-RT measurements

Simulation results of the NPC voltages, currents, and CMV in stable conditions are depicted in Figure 3.9. As shown in this figure, CMV is practically eliminated by using t_s=20µs while V_{ag}, V_{an}, and V_{AB} are desirably generated. Figure 3.10 shows the experimental results for the same parameters as Figure 3.9 while the three-phase NPC inverter supplies a linear RL load. In Figure 3.10, λ_3 is first assumed zero in the cost function; thus, there is no control on CMV. Afterward, the optimized value of λ_3 is applied to suppress the CMV. As shown in Figure 3.10, CMV with a high amplitude appears when it is not controlled in the cost function.

However, CMV is suppressed when the right weighting factor is applied to the corresponding term.

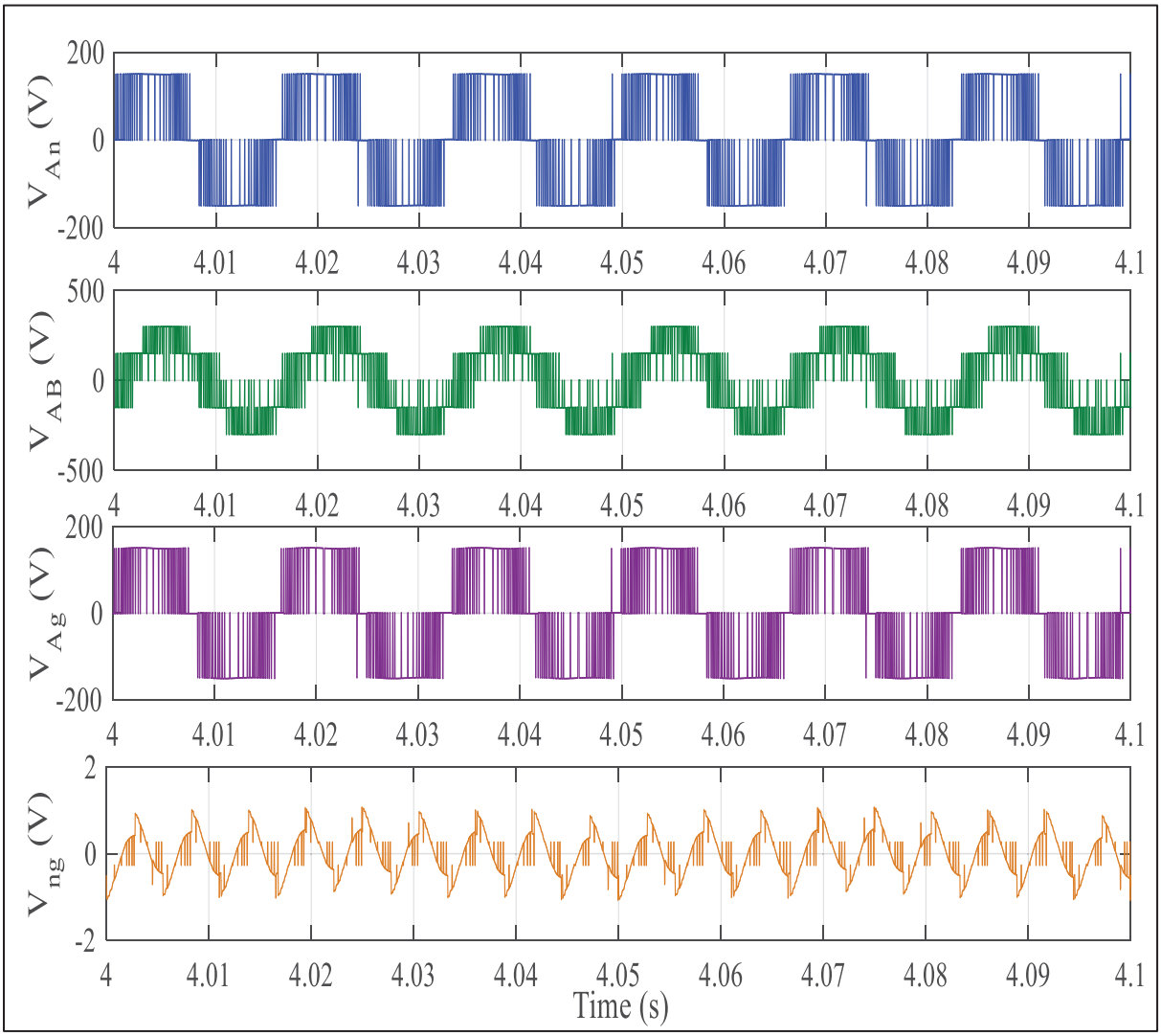

Figure 3.9 Simulation results for the phrase, line, branch, and common mode voltages when NPC operates in stable conditions

Figure 3.10 Experimental results of CMV, V_{Ag}, V_{AB}, and V_{An} when CMV is ignored and when it is eliminated

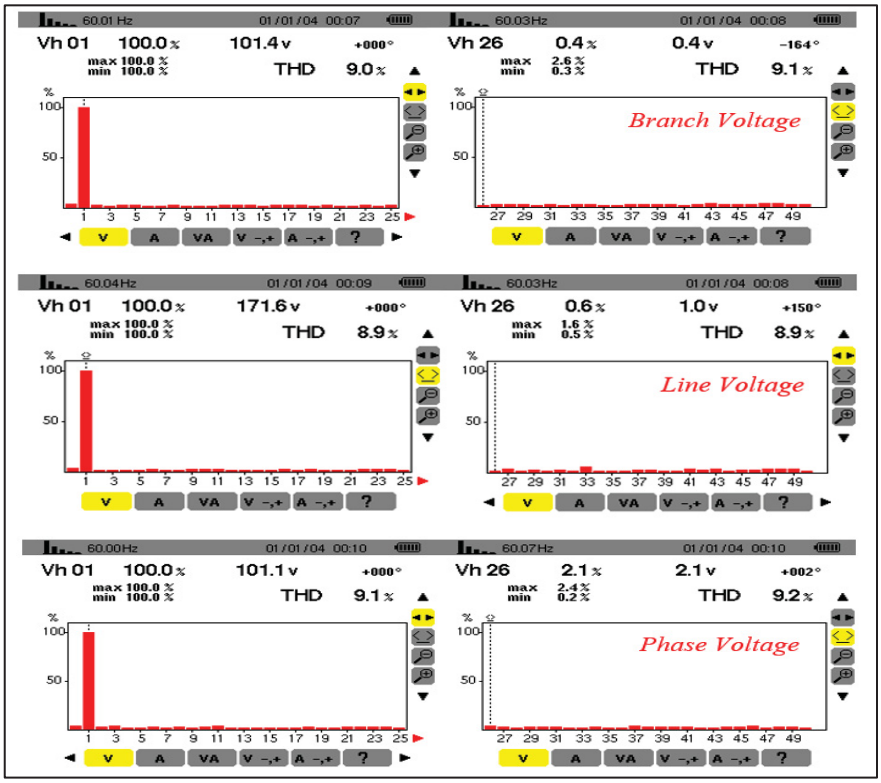

Figure 3.11 Experimental results of THD analysis for the branch, line, and phase voltages

In the absence of CMV, the phase voltages become equal to the branch voltages in terms of the voltage level. Figure 3.11 also shows the corresponding harmonic spectrum analysis of V_{ag}, V_{AB}, and V_{an}; the power quality analysis reveals that the branch and phase voltages approximately have similar harmonic content and THD because of CMV cancellation.

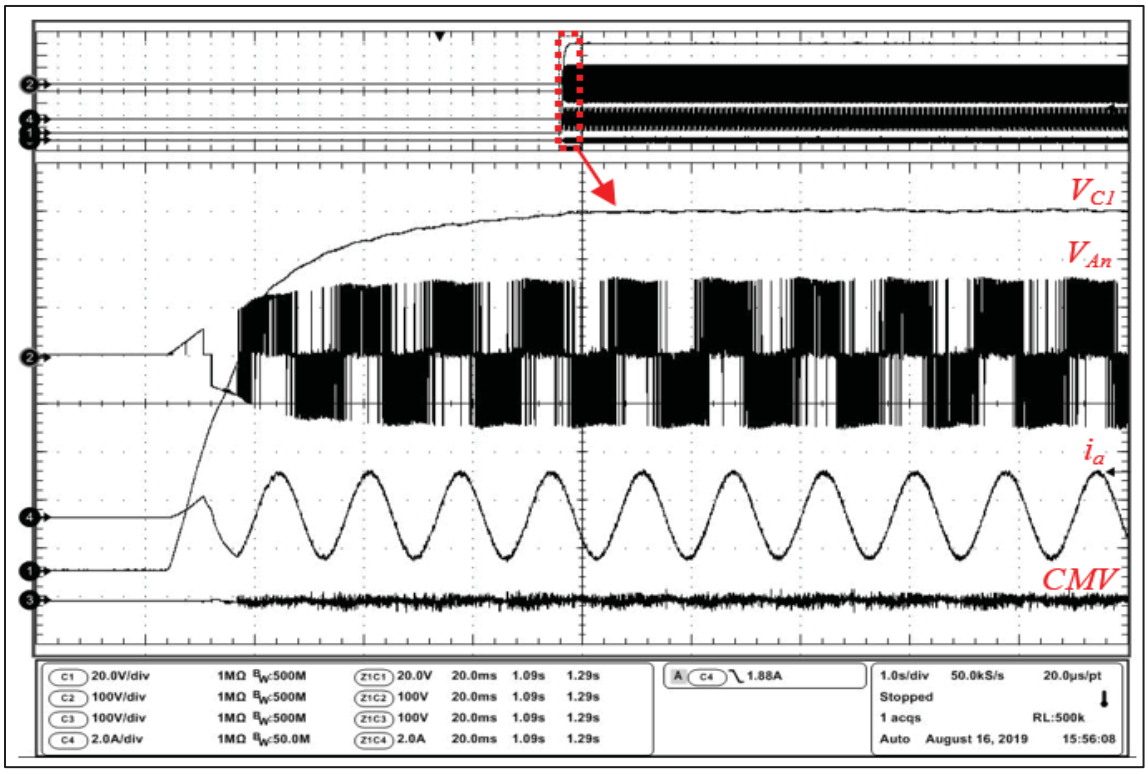

Figure 3.12 Experimental results of V_{C1}, V_{An}, i_a, and CMV during the start-up of the inverter

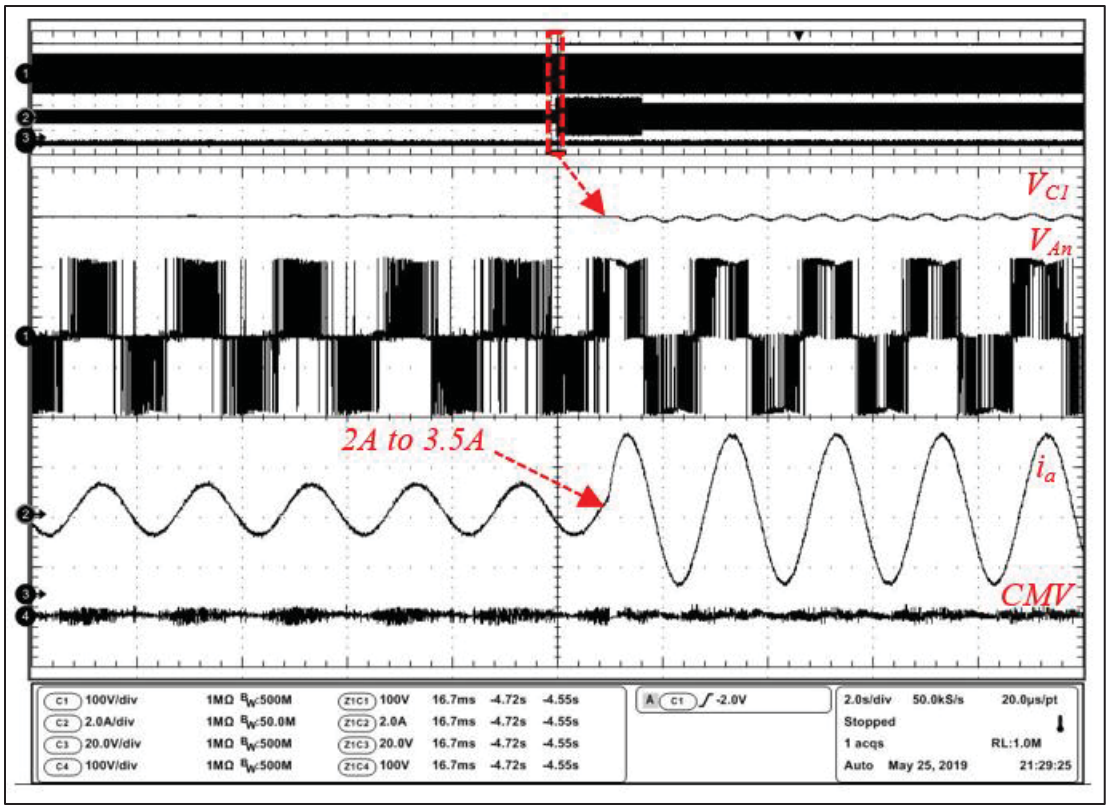

Figure 3.13 Experimental results of V_{C1}, V_{An}, i_a, and CMV under the reference current variation

In the next test, the DC voltage changes from zero to 300V as a start-up condition to evaluate the dynamic operation of the SLMPC technique in dealing with harsh circumstances caused by an inrush current. As depicted in Figure 3.12, there are no fluctuations in the measured voltages and currents when the extreme change of the DC source occurred. To further analyze the controller in dynamic conditions, NPC is tested under both current reference and three-phase load changes to prove that SLMPC guarantees CMV suppression under various dynamic modes. Regarding, Figure 3.13 and Figure 3.14 show related experimental results when the three-phase NPC inverter operates under the reference current and load changes, respectively. In the case of the reference variation, it is increased from 2A to 3.5A. Figure 3.13 shows that the reference step change is tracked without any notable transient response and voltage and current overshoots/undershoots. The resistance of the three-phase load is suddenly increased from 40Ω to 80Ω and the corresponding results are shown in Figure 3.14 (a). The inductance is also stepped up from 10mH to 20mH and the related experimental results are presented in

Figure 3.14 (b). As shown in Figure 3.14, CMV suppression is perfectly maintained during the load variations. Moreover, the capacitors' voltages are accurately balanced to half of the input DC voltage in both dynamic modes.

For the last test, the proposed SLMPC is compared with CMPC while both techniques deal with CMV. The CMPC weighting factors are assigned using the guidelines discusses in (Cortes et al., 2010; Karamanakos, & Geyer, 2019). The guidelines are actually some empirical methods, which simplify the tuning process. The weighting factors in CMPC are determined by plotting the tracking error ($e_{io}(t)$) of the current, the balancing error ($e_{VC}(t)$) of the capacitors, and CMV for different values of λ_1^{CMPC}, λ_2^{CMPC}, and λ_3^{CMPC} as explained in (Cortes et al., 2010). Therefore, using the empirical tuning techniques, the best values which minimize all the error functions are chosen for weighting factors of the CMPC.

Figure 3.15 (a) and Figure 3.15 (b) respectively represent the simulation results for the DC link capacitors' voltages, line voltage, three-phase load currents, and CMV when the CMPC and the proposed SLMPC are separately employed as the NPC controller. Figure 3.15 (a) depicts that even though CMPC successfully balances the voltages of the capacitors and tracks the desired reference current, notable initial transient effects appear in the voltages of the capacitors, and severe spicks occur in CMV amplitude because of the non-optimized weighting factors. However, simulation results in Figure 3.15 (b) demonstrate that the initial transient effects in the voltages of the capacitors are significantly reduced and the undesired spikes disappear when the proposed SLMPC with the optimized weighting factors is employed.

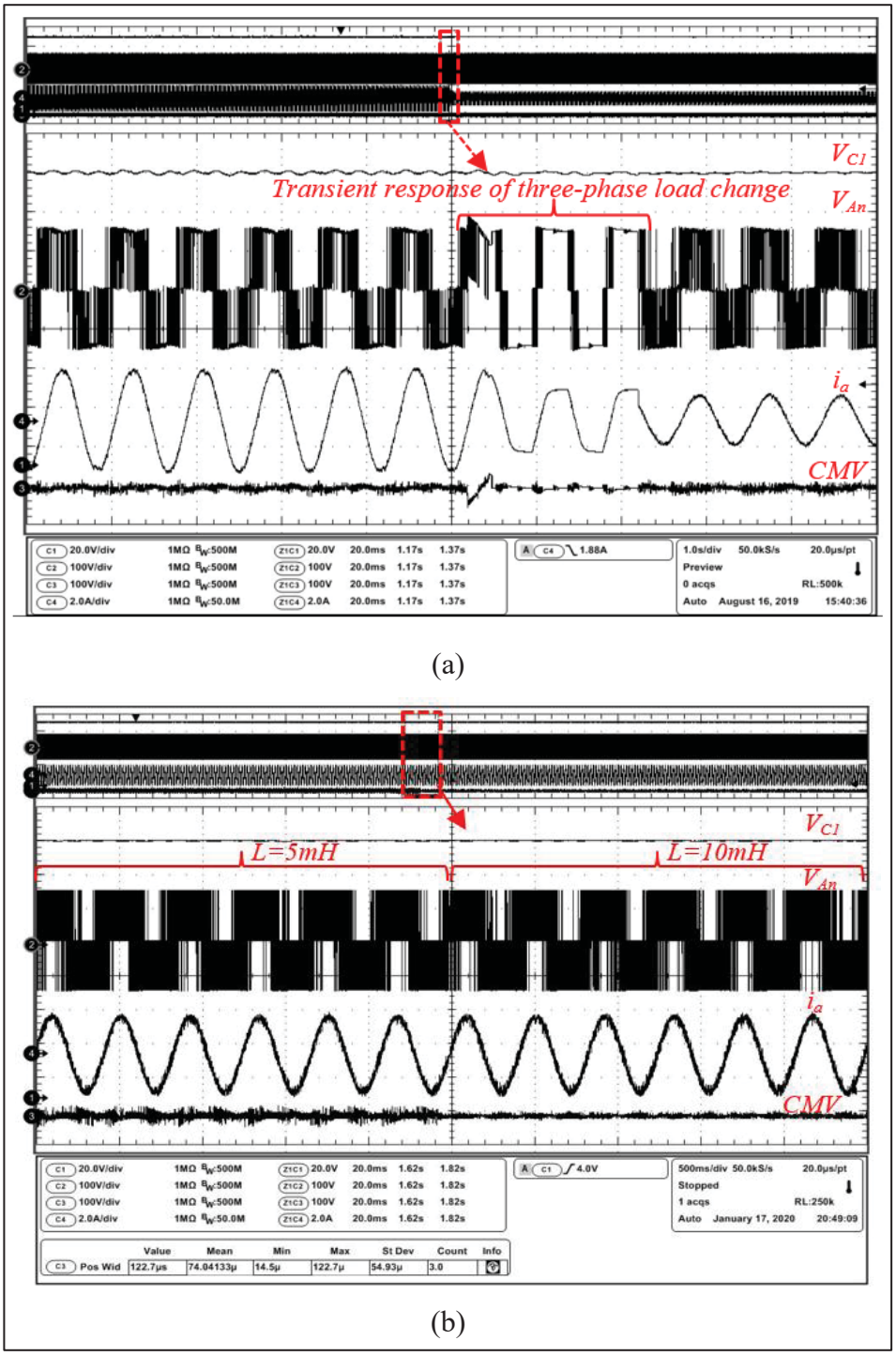

Figure 3.14 Experimental results of V_{C1}, V_{An}, i_a, and CMV, (a) under the load impedance variation, (b) under the load inductance variation

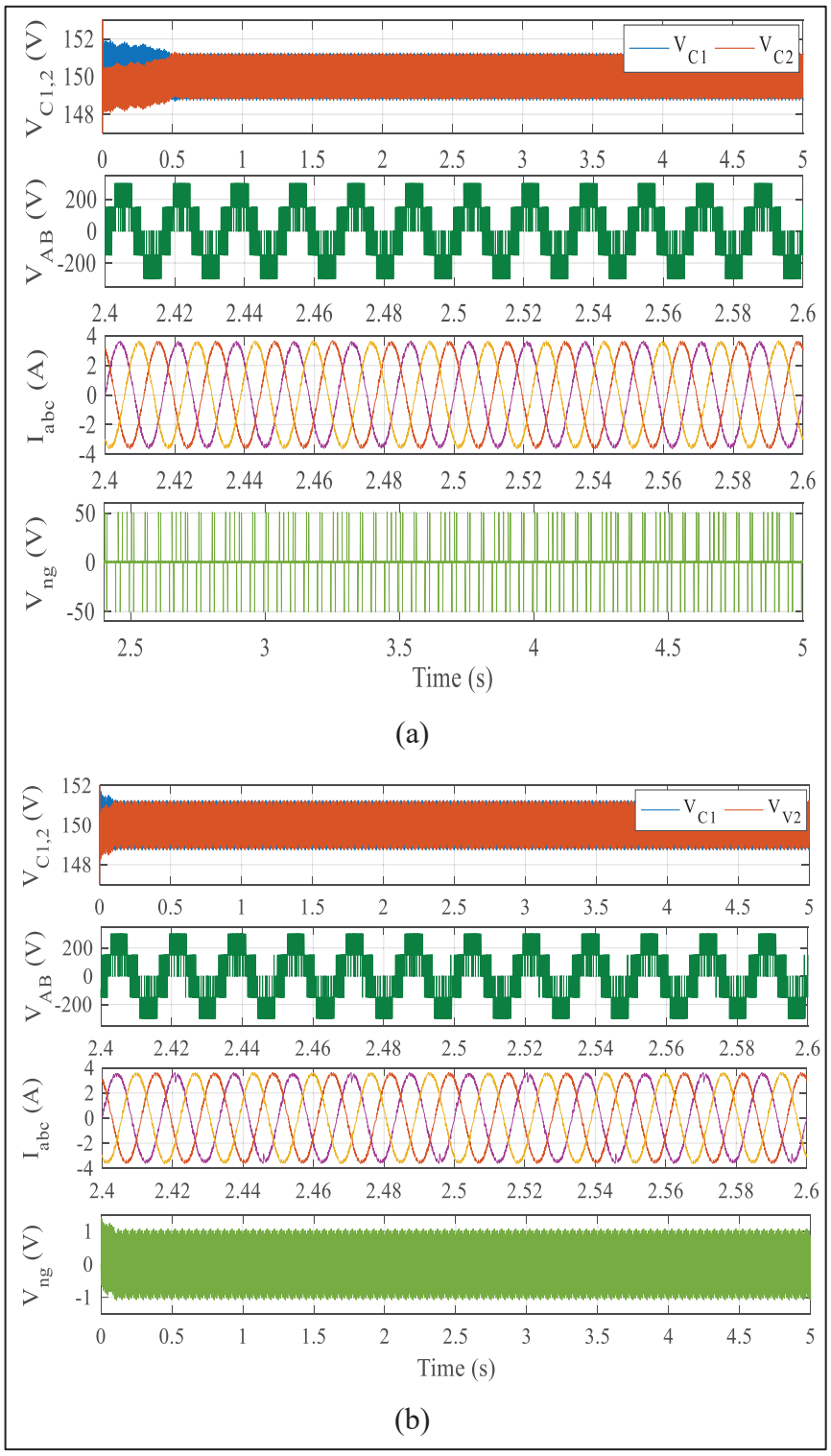

Figure 3.15 Comparison simulation results for the NPC voltages and currents using (a) CMPC (b) SLMPC

Moreover, the simulation result of $E(t)$ obtained by the proposed SLMPC and CMPC are compared in Figure 3.16. Thanks to the proposed optimization technique, Figure 3.16 shows that the SLMPC provides a faster transient response with less $E(t)$ compared with the CMPC. The optimization process reveals that the ABC algorithm uses less computational burden and converges to the optimal solution faster than the empirical tuning methods discussed in (Cortes et al., 2010; Karamanakos, & Geyer, 2019).

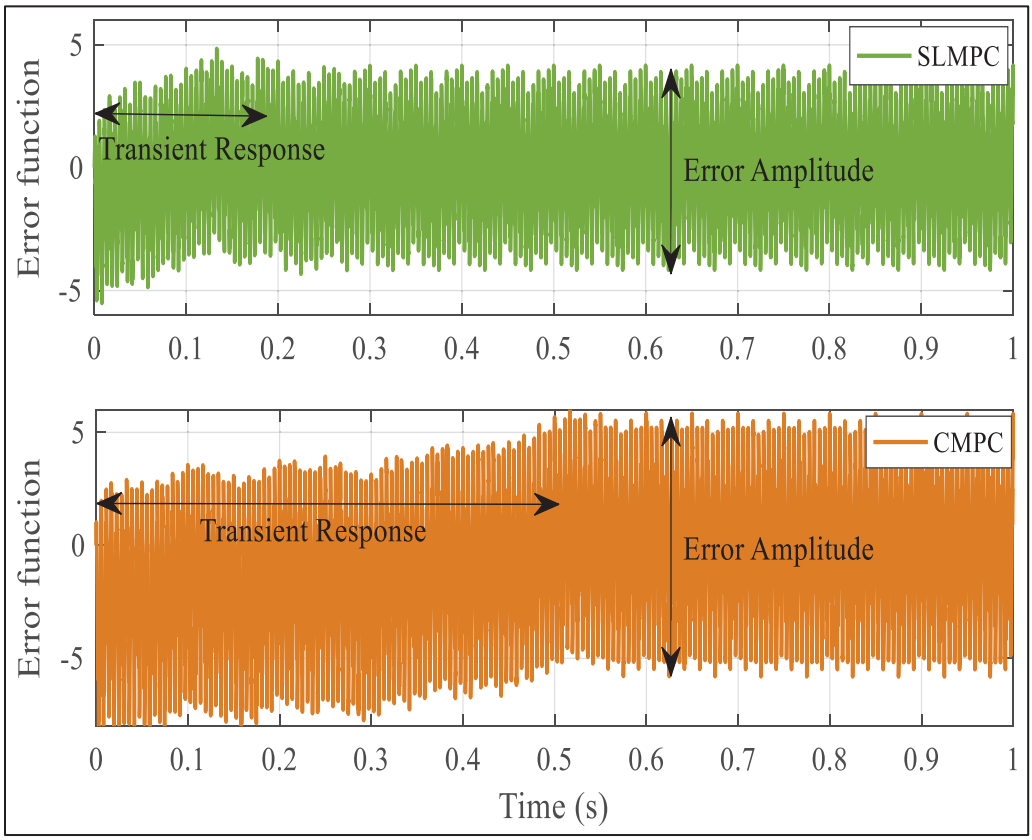

Figure 3.16 Comparison results of $E(t)$ generated by the SLMPC and CMPC

3.6 Conclusion

Even though the appropriate performance of MPC highly depends on its weighting factors, they are conventionally adjusted by empirical methods. Using the empirical techniques is tedious and inaccurate, particularly if several independent weighting factors are involved.

Thus, in this paper, the MPC strategy has been trained through the ABC algorithm to achieve supervised learning on MPC so that optimal values are ensured for the weighting factors. The proposed SLPMC technique has been applied to a three-phase NPC inverter to track three main control objectives, including capacitors voltages balancing, reference current tracking, and CMV suppression. The performance of the proposed technique has been investigated through experimental and simulation tests, where the results confirmed the feasibility and effectiveness of the SLMPC algorithm. The proposed training process can be performed for different MPC algorithms to meet the desired multi-objective control performance.

CHAPTER 4

Floating Weighting Factor ANN-MPC based on Lyapunov Stability for Seven-Level Modified PUC Active Rectifier

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Abstract

Despite being cost-effective, the seven-level Modified Packed U-Cell (MPUC7) active rectifier is unstable due to using unequal floating DC links. Thus, a multi-objective controller is required to stabilize its voltages and currents besides preserving its efficiency and power quality. Although conventional finite set model predictive control (FSMPC) supports multi-objective control, it cannot assure system stability and efficiency because of tiresome tuning of the weighing factors and the lack of stability analysis. This paper presents a low-frequency adaptive FSMPC (AMPC) stabilized based on the Lyapunov stability theory to overcome the design problems of FSMPC. AMPC handles four control objectives in addition to a decoupled stability term. The control objectives assure the standard performance of the MPUC7 in terms of switching losses, dv/dt, THD, and DC link voltage ripple. The stability objective guarantees the controller's reliability under unstable conditions. The weighting factors in the AMPC are floating to tackle the tuning challenges, where a radial basis function neural network controller (RBFC) adjusts their variations. The proposed RBFC is trained by a novel self-training method, including the PSO algorithm and some mathematical analyses without using any training data.

Several experimental and simulation tests are also applied to the AMPC in different conditions to confirm its feasibility.

4.1 Introduction

In comparison with conventional fixed and variable angle rectifiers made by diodes or thyristors, bidirectional multilevel converters (BMC) provide a new generation of low and medium-power active rectifiers, the so-called multilevel rectifiers (MR), which can control DC power with minimum distortion on the AC side. Therefore, MRs notably mitigate harmonics as the main source of power losses. By suppressing the harmonics, passive and active power filters are no longer required, which desirably results in a compact power system. In addition, MRs are able to regulate the DC voltage when the grid is unstable. MRs have been evaluated in different applications like DC arc furnaces (Ladoux, Postiglione, Foch, & Nuns, 2005), active power filters (APF) (Alfaris, & Bhattacharya, 2019), static synchronous compensators (STATCOM) (Farivar, Townsend, Pou, & Hredzak, 2018), electric vehicles (EV) (Drobnič et al., 2018, November), high-speed gen-set applications (Foti et al., 2019), and wind turbines (Khan et al., 2018). Neutral point clamped (NPC), flying capacitor (FC), cascaded H-bridge (CHB), packed E-cell (PEC), and modified packed U-cell (MPUC) are the prominent BMCs, which can operate as MRs in industrial applications (Sharifzadeh, Chouinard, & Al-Haddad, 2019; Khazraei et al., 2012; Sharifzadeh, & Al-Haddad, 2019; Babaie, Mehrasa, Sharifzadeh, & Al-Haddad, 2019, September; Moeini, Zhao, & Wang, 2016). From a structural point of view, MPUC utilizes fewer components in comparison with others. MPUC has been derived from the PUC topology to boost the multilevel voltage amplitude by summing its DC link voltages (Babaie, Sharifzadeh, Kanaan, & Al-Haddad, 2020). Therefore, MPUC is appealing to design a compact rectifier in systems with restricted space like EVs, turbines, and UPSs. In addition, MPUC is able to operate in no-load modes, such as APF and STATCOM (Vahedi, Shojaei, Dessaint, & Al-Haddad, 2017; Vahedi, Dehghanzadeh, & Al-Haddad, 2018, April).

From the control point of view, BMCs, including MRs, are considered variable structure systems because of their switching operation. Such dynamic behavior brings out a nonlinear

relation between the capacitors' voltages and the rectifier current so that increasing the number of voltage levels results in a complicated system and demands advanced nonlinear controllers to stabilize the capacitors' voltages besides tracking the other control objectives. A hybrid control strategy using an algebraic estimator and a linear controller was proposed by (Juárez-Abad et al., 2018) for a five-level single-phase CHB rectifier. The control technique in (Juárez-Abad et al., 2018) provides a robust performance against load uncertainties using the algebraic estimator. In (de Freitas et al., 2016), an adaptive space vector modulator was designed for a six-leg seven-level rectifier in single-phase mode to balance the average values of the DC link voltages. Existing the redundant switching states in (de Freitas et al., 2016) is the main advantage to improving the control loop performance in balancing the capacitors' voltages. A direct power control method with a simpler resultant modulation stage was implemented in (Montero-Robina, Umbría, Salas, & Gordillo, 2018) to balance the capacitors' voltages using their dynamic equations in a three-phase diode-clamped rectifier. Feedback linearization was proposed by (Mehrasa, & Ahmadigorji, 2012, May) to track the control objectives in a three-phase NPC rectifier. A dual dynamic model of the rectifier was introduced by (Mehrasa, & Ahmadigorji, 2012, May) to improve the accuracy of the control loop in attaining minimum voltage ripple for the DC link capacitors. Using a passivity-based PI technique, a stable control loop was designed for a three-phase two-level rectifier in (Pérez, Ortega, & Espinoza, 2004) and a full-bridge diode-based DC-DC boost rectifier in (Cisneros et al., 2015) to regulate the output DC voltage and current. The linear-based methods involve simple mathematics and computation burden somehow simple hardware is required in practice compared with nonlinear control strategies. However, hybridizing the linear techniques with other control strategies to adjust the control factors and preserve the control loop stability makes the control design process as difficult as nonlinear control strategies, especially when there is a multi-objective control problem. Lyapunov-based finite set model predictive control (FSMPC) is a nonlinear technique proposed in (Makhamreh, Trabelsi, Kükrer, & Abu-Rub, 2020) to stabilize the capacitors' voltages in a seven-level PUC rectifier by using the switched dynamic model of the converter. High switching frequency, significant dv/dt, and asymmetrical seven-level voltage waveform in (Makhamreh, Trabelsi, Kükrer, & Abu-Rub, 2020) intensify switching loss and shorten the lifetime of switches.

The literature review of MRs shows that increasing the capacitors and switches to achieve more voltage levels escalates the nonlinearity of the model, threatens the reliability of the converter, and complicates the control loop structure. According to this fact, MPUC properly compromises between the components count and voltage levels so that fewer dynamics need to be involved in the control loop compared with the other MRs (Vahedi, & Al-Haddad, 2016). However, this topology still requires a multi-objective robust controller because of the following reasons. First, there is a lack of redundant charging and discharging switching paths to control the capacitors' voltages when MPUC operates in the seven-level mode. Second, the rectifier current in MPUC7 directly flows through both capacitors during the seventh-level period while the voltages and loads of DC links are unequal. Therefore, an unknown discontinuous dynamic behavior related to the loads, rectifier current, and capacitors' voltages appears in the converter that challenges the stability and efficiency of the controller. Moreover, the dynamic of capacitors cannot be directly controlled by a single control signal.

Concerning the control problems of MPUC7, FSMPC seems a suitable solution since it directly controls the power switches based on a cost function including desired control objectives and constraints (Kouro, Cortés, Vargas, Ammann, & Rodríguez, 2008). Although the other techniques need the continuous dynamic model of the converter to reach the control law, FSMPC uses the switched model, which is highly compatible with the discontinuous structure of the MPUC7 active rectifier. Indeed, FSMPC decentralizes the converter model and provides individual PWM control signals for each switch to reach the desired objectives. Even so, because of its discrete non-differentiable dynamics, FSMPC does not support the conventional Lyapunov theory to determine the stability conditions. Moreover, FSMPC uses several weighting factors in the cost function to set priority among the control objectives. Thus, the optimal performance of FSMPC directly depends on the weighting factors. Increasing the control objectives also turns the tuning of the weighting factors into an exhausting process and limits the multi-objective control capability of FSMPC (Karamanakos, & Geyer, 2019; Cortés et al., 2009, February). Hybrid PI-FSMPC is the technique, which was proposed by (Sleiman et al., 2015, November) to regulate the capacitors' voltages and the current for the MPUC7

active rectifier. PI as the auxiliary controller was employed in (Sleiman et al., 2015, November) to regulate the capacitors' voltages where its control signal was applied to the FSMPC as the reference current. Thus, a single weighting factor was used in the cost function to adjust the contribution of the current control objective. However, the PI controller decreases the robustness of the control loop by causing an untestable reference current so that notable overshoots/undershoots appear in the voltages and currents during dynamic conditions (Sleiman et al., 2015, November).

In (Karamanakos, & Geyer, 2019; Cortés et al., 2009, February; Guazzelli et al., 2018; Babaie, Sharifzadeh, Mehrasa, Chouinard, & Al-Haddad, 2020), several generalized guidelines and meta-heuristic optimization techniques have been introduced for static adjustment of the weighting factors. However, constant factors cannot guarantee control efficiency during unstable conditions (Machado, Martín, Rodríguez, & Bueno, 2017). Thus, new dynamic tuning techniques using fuzzy (Villarroel et al., 2012), ANN (Machado, Martín, Rodríguez, & Bueno, 2017; Dragičević, & Novak, 2018), and mathematical modeling (Shadmand, Jain, & Balog, 2018; Karamanakos, & Geyer, 2018) have been recommended recently. Despite the satisfactory performance, the modeling-based methods involve complex mathematics to obtain the adaptive equations. In addition, the mathematical design difficulties become worse as the control objectives increase. In comparison with ANN, fuzzy suffers from a lack of advanced training techniques. Therefore, ANN is more applicable and flexible than fuzzy in nonlinear modeling problems. Despite the fair performance, the ANN-based techniques in (Machado, Martín, Rodríguez, & Bueno, 2017; Dragičević, & Novak, 2018) propose supervised learning strategies including a reference model and a huge database to train the ANN parameters. Therefore, the ANN-based techniques involve a time-consuming design process and their accuracy undesirably depends on the training data. Thus, tuning the weighting factors still is problematic, especially for the MPUC7, since multi-objective control cannot be effectively implemented.

To address the stability problem, a Lyapunov-based cost function was proposed by (Makhamreh, Trabelsi, Kükrer, & Abu-Rub, 2020; Makhamreh, Sleiman, Kükrer, & Al-

Haddad, 2018) to preserve the stability of the FSMPC designed for a bidirectional PUC7 converter. The Lyapunov-based FSMPC technique is valuable because it has opened a new path to developing stability tools for discrete controllers. However, it increases the computation burden of FSMPC somehow involving more control objectives significantly complicates the control design problem. Moreover, the optimal switching vector in (Makhamreh, Trabelsi, Kükrer, & Abu-Rub, 2020; Makhamreh, Sleiman, Kükrer, & Al-Haddad, 2018) is mainly selected based on the stability criteria so that the impact of the control objectives on the cost function decreases due to mixing the stability and control objectives.

This paper proposes a low-frequency Adaptive FSMPC (AMPC) technique based on a discrete form of Lyapunov stability theory and Artificial Neural Network (ANN) to dominate the stability and tuning problems of FSMPC for the MPUC7 active rectifier. The cost function in AMPC includes four control objectives and a decoupled stability condition. The control objectives guarantee the desired performance of the MPUC7 active rectifier in terms of switching losses, dv/dt, THD, and voltage ripple while the stability objective assures the reliability of the controller during unstable conditions. The stability objective is obtained through a novel predicted Lyapunov function. Thus, as the first contribution, it is the first time that stability is assured in an FSMPC technique while the control objectives are decoupled from the stability condition without using any additional weighting factor. The weighting factors in AMPC are also assigned floating to overcome the tuning difficulties where a radial basis function neural network controller (RBFC) adjusts their variations using the errors of the rectifier current and the capacitors' voltages. As the second contribution, a self-training technique (without using any reference model and training data) configured by particle swarm optimization (PSO) algorithm and some mathematical analyses is proposed, which trains the RBFC much faster and more accurately than conventional ANN techniques introduced in (Machado, Martín, Rodríguez, & Bueno, 2017; Dragičević, & Novak, 2018). The RBFC properly manipulates the nonlinear relation between the capacitors' voltages and the rectifier current. In addition, a mathematical estimator using average to peak transfer function is employed in AMPC to tune the reference current amplitude instead of the PI. The current

reference estimator (CRE) precisely generates the reference current such that all damaging transient effects disappear.

In the following, Section 4.2 presents the MPUC7 rectifier, Section 4.3 provides the proposed AMPC design procedure, and the results for different experimental and simulation tests are given in Section 4.4. Section 4.5 also provides the conclusions.

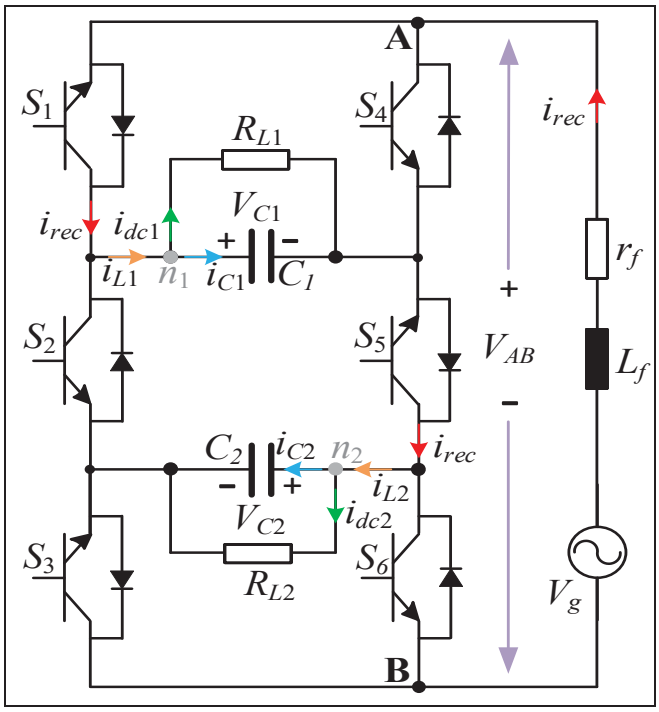

Figure 4.1 Schematic diagram of the MPUC active rectifier including detailed current flows

4.2 Modified Packed U-Cell Active Rectifier

As depicted in Figure 4.1, six power switches and two capacitors configure the MPCU rectifier. The DC links are able to supply two different loads (R_{L1}, R_{L2}). Table 4.1 shows all possible switching states and voltage levels for the MPUC. The switches are classified into three complementary pairs, including (S_1, S_4), (S_2, S_5), and (S_3, S_6) to prevent short circuits in the DC links.

Table 4.1 Switching states, voltage levels, and charging/discharging cycles of MPUC7

States	S_1	S_2	S_3	S_4	S_5	S_6	V_{out}	C_1	C_2
1	1	0	1	0	1	0	$+V_{C1}+V_{C2}$	Charging	Charging
2	1	0	0	0	1	1	$+V_{C1}$	Charging	Discharging
3	0	0	1	1	1	0	$+V_{C2}$	Discharging	Charging
4	0	0	0	1	1	1	0	Discharging	Discharging
5	1	1	1	0	0	0	0	Discharging	Discharging
6	1	1	0	0	0	1	$-V_{C2}$	Discharging	Charging
7	0	1	1	1	0	0	$-V_{C1}$	Charging	Discharging
8	0	1	0	1	0	1	$-V_{C1}-V_{C2}$	Charging	Charging

Changing the switch direction in S_3 and S_6 allows MPUC to boost the output voltage. Thus, small DC links, including small capacitors, can generate higher voltage amplitudes. By using two DC links, MPUC is able to generate a quasi-sinusoidal voltage waveform with five or seven levels. The voltages of the DC links determine the number of levels; according to Table 4.1, equal voltages generate a five-level waveform. The Seven-level waveform is also made by adjusting the second DC link voltage to half of the first one. In comparison with the seven-level mode of operation, the second DC link voltage in the five-level mode is self-balanced because of existing the redundant switching vectors in states 2, 3, 6, and 7. Thus, a simple control loop is enough to track the objectives. However, removing two voltage levels intensifies harmonics and undesirably affects the voltage ripple. Accordingly, using MPUC in the seven-level mode of operation (MPUC7) is ideal to improve the power quality.

4.3 The Proposed Adaptive MPC Technique

This section is dedicated to designing the AMPC technique using the discontinuous dynamic model of the MPUC7 active rectifier in terms of the capacitors' voltages, the input current, and the switching operation. The modeling and the control objectives are developed in the first subsection, the stability objective is formulated in the second subsection, the variations effects of weighting factors on the control performance are analyzed in the third subsection, RBFC is

configured and trained in the fourth subsection and the proposed AMPC is described in the last subsection.

4.3.1 Discrete Modeling and the Control Objectives

The discrete dynamic model of the MPUC7 is required to formulate the desired control objectives in the AMPC. Regulating the DC voltages, tracking the reference current, and reducing the switching frequency are considered the main control objectives. Thus, the capacitors' voltages in the DC links, the inductor current in the grid filter, and the switching operation of the whole converter should be properly modeled to fulfill the objectives. In this regard, the discrete model of the multilevel voltage (V_{AB}) based on the switching states and the capacitors' voltages presented in Table 4.1 is first extracted as shown in (4.1). This equation is subsequently used to formulate the inductor current.

$$V_{AB} = (S_1 - S_2)V_{C1}^{*} + (S_3 - S_2)V_{C2}^{*} \tag{4.1}$$

where S_1, S_2, and S_3 are the fundamental switching variables defined in Table 4.1. The variables logically change between one and zero when the related switch is ON and OFF respectively. The references for the DC voltages of C_1 and C_2 are also depicted by V^{*}_{C1} and V^{*}_{C2}, respectively. Equation (4.2) discloses that the capacitors generate the voltage levels for the multilevel waveform. Thus, they must be properly balanced to have a symmetrical waveform and minimum distortion in the rectifier current (i_{rec}). In this regard, the dynamic models of the capacitors' voltages are required to stabilize them and control their ripple. Applying the KCL law to n_1 and n_2 in Figure 4.1 results in the DC links' currents equation as presented in (4.2).

$$\begin{cases} i_{L1} = i_{C1} + i_{dc1} \\ i_{L2} = i_{C2} + i_{dc2} \end{cases} \tag{4.2}$$

where i_{L1}, i_{L2}, i_{dc1}, i_{dc2}, i_{C1}, and i_{C2} respectively indicate the currents of the DC links, the loads, and the capacitors. Since the capacitors' voltages are related to their currents, their dynamic models are calculated as (4.3) using (4.2).

$$\begin{cases} \dfrac{dV_{C1}}{dt} = \dfrac{1}{C_1}\left(i_{L1} - i_{dc1} \right) \\ \dfrac{dV_{C2}}{dt} = \dfrac{1}{C_2}\left(i_{L2} - i_{dc2} \right) \end{cases} \tag{4.3}$$

To avoid measuring the DC links' currents and using additional sensors, (4.3) is modified as (4.4) in which i_{L1} and i_{L2} are calculated based on i_{rec} and S_1, S_2, and S_3.

$$\begin{cases} \dfrac{dV_{C1}}{dt} = \dfrac{1}{C_1}\left((S_1 - S_2)i_{rec} - i_{dc1} \right) \\ \dfrac{dV_{C2}}{dt} = \dfrac{1}{C_2}\left((S_3 - S_2)i_{rec} - i_{dc2} \right) \end{cases} \tag{4.4}$$

Afterward, the forward Euler approximation function is used to transform the first-order derivative terms of (4.4) into discontinuous forms as (4.5) to obtain the predictable models of the capacitors' voltages.

$$\begin{cases} \dfrac{V_{C1}(k+1) - V_{C1}(k)}{\Delta t} = \dfrac{1}{C_1}\left((S_1 - S_2)i_{rec} - i_{dc1} \right) \\ \dfrac{V_{C2}(k+1) - V_{C2}(k)}{\Delta t} = \dfrac{1}{C_2}\left((S_3 - S_2)i_{rec} - i_{dc2} \right) \end{cases} \tag{4.5}$$

where $V_{C1,2}(k)$ and $V_{C1,2}(k+1)$ are the capacitors' voltages in the present and the next sampling periods; Δt is the time variations. Since the rectifier input current also changes over time, its predictive equation is required to obtain the predicted models for the capacitors' voltages. Accordingly, (4.5) is modified as (4.6) to predict the capacitors' voltages for the next sampling instance. In (4.6), $i_{rec}(k+1)$ and T_s are the predicted values of the rectifier input current and

sampling time respectively. $i_{rec}(k+1)$ is acquired as (4.7) by applying the forward Euler method to the continuous dynamic model of the inductor current in (4.8).

$$\begin{cases} V_{C1}(k+1) = V_{C1}(k) \\ \qquad + \dfrac{T_s}{C_1}\left((S_1(k+1) - S_2(k+1))i_{rec}(k+1) - i_{dc1}(k) \right) \\ V_{C2}(k+1) = V_{C2}(k) \\ \qquad + \dfrac{T_s}{C_2}\left((S_3(k+1) - S_2(k+1))i_{rec}(k+1) - i_{dc2}(k) \right) \end{cases} \tag{4.6}$$

$$i_{rec}(k+1) = i_{rec}(k) + \frac{T_s}{L_f}\left(V_g(k) - V_{AB}(k+1) - r_f i_{rec}(k) \right) \tag{4.7}$$

$$L_f \frac{di_{rec}}{dt} = V_g - V_{AB} - r_f i_{rec} \tag{4.8}$$

where $V_g(k)$, L_f, and r_f are respectively the grid voltage, the grid filter inductance, and resistance. $V_{AB}(k+1)$ is the predicted model of the MPUC7 voltage formulated in (4.9) using (4.1).

$$V_{AB}(k+1) = (S_1(k+1) - S_2(k+1))V_{C1}^{*} + (S_3(k+1) - S_2(k+1))V_{C2}^{*} \tag{4.9}$$

Regarding the MPUC topology, the switching frequency in S_1 and S_3 depends on the controller performance, which is equal to the switching frequency, while S_2 should operate in the fundamental frequency of the converter (Vahedi, Shojaei, Dessaint, & Al-Haddad, 2017). Nevertheless, high switching frequency occurs for all switches in the design proposed by (Makhamreh, Trabelsi, Kükrer, & Abu-Rub, 2020; Sleiman et al., 2015, November; Makhamreh, Sleiman, Kükrer, & Al-Haddad, 2018) because of the non-optimized performance of the controllers. In this paper, the switching operation of MPUC7 is controlled using (4.10)

in the cost function to minimize the switching frequency so that the switching loss is reduced and THD is improved.

$$S_T{}^P(k+1) = \left| S_1(k+1) - S_1(k) \right| + \left| S_2(k+1) - S_2(k) \right| + \left| S_3(k+1) - S_3(k) \right| \tag{4.10}$$

$S^P{}_T(k+1)$ is the predicted switching model in the next sampling time; $S_1(k+1)$, $S_2(k+1)$, $S_3(k+1)$ and $S_1(k)$, $S_2(k)$, $S_3(k)$ are respectively the next and the present switching states for S_1, S_2, and S_3. To minimize dv/dt in terms of voltage variation, the following conditions related to (4.10) are considered in the AMPC:

$$\begin{cases} \mu(k+1) = 2, & \text{if } \mu(k) = 1 \ \& \ \mu^p(k+1) = 3 \\ \mu(k+1) = 2, & \text{if } \mu(k) = 3 \ \& \ \mu^p(k+1) = 1 \\ \mu(k+1) = 7, & \text{if } \mu(k) = 8 \ \& \ \mu^p(k+1) = 6 \\ \mu(k+1) = 7, & \text{if } \mu(k) = 6 \ \& \ \mu^p(k+1) = 7 \end{cases} \tag{4.11}$$

where $\mu(k)$, $\mu(k+1)$, and $\mu^p(k+1)$ are respectively the present switching vector already applied to the converter, the next switching vector in the upcoming sampling period, and the predicted candidate switching vector for the next sampling instance. The candidate switching vector is chosen from the eight vectors defined in Table 4.1. According to the control objectives defined in (4.6), (4.7), and (4.10), the AMPC cost function can be derived as below:

$$G_{AMPC}(k+1)=\lambda_1 \left| V_{C_1}(k+1)-V^*_{C_1}(k) \right| + \lambda_2 \left| V_{C_2}(k+1)-V^*_{C_2}(k) \right| + \lambda_3 \left| i_i(k+1) - i^*_{rec}(k) \right| + \lambda_4 S^P_T(k+1) \tag{4.12}$$

where $i^*_{rec}(k)$ is the desired reference for the rectifier input current; λ_1, λ_2, λ_3, and λ_4 are respectively the weighting factors for the predicted tracking errors of the capacitors, the inductor current, and the switching frequency. The reference current in (4.12) has critical impacts on the control loop performance; thus, its amplitude should be appropriately

determined somehow nominal required power is delivered to the DC loads. Indeed, inaccurate current amplitude causes unknown behavior in the DC loads, distorts the grid current, and destabilizes the DC voltages. Traditionally, a PI controller generates the reference current based on the error of the capacitors' voltages (Makhamreh, Trabelsi, Kükrer, & Abu-Rub, 2020; Sleiman et al., 2015, November; Vahedi, & Al-Haddad, 2016). It sets the reference current as the error of the DC voltages tends to zero. However, the ripple of capacitors' voltages changes the estimated peak current amplitude, which results in damaging voltage and current variations in the DC loads during the dynamic operation of the loads and grid. In this paper, the reference current is made by CRE defined in (4.13) as a novel and simple technique.

$$\begin{cases} i^{*}_{rec}(k) = sat\ \left(f\ \left(i_{dc1},\ i_{dc2} \right) \right) \sin(\omega t) \\ f\ \left(i_{dc1},\ i_{dc2} \right) = \dfrac{\pi\ \left(i_{dc1} + i_{dc2} \right)}{2} \\ sat\ \left(f\ \left(i_{dc1},\ i_{dc2} \right) \right) = \begin{cases} i^{\max}_{rec}, & \text{if} \quad f\ \left(i_{dc1},\ i_{dc2} \right) > i^{\max}_{rec} \\ \dfrac{\pi\ \left(i_{dc1} + i_{dc2} \right)}{2}, & \text{if} \quad f\ \left(i_{dc1},\ i_{dc2} \right) \le i^{\max}_{rec} \end{cases} \end{cases} \tag{4.13}$$

where ωt is the angular velocity of the grid voltage measured by a phase-locked loop (PLL) to synchronize the rectifier current with the grid voltage. In (4.13), the DC load currents are measured and then the desired AC peak amplitude is estimated using the average-to-peak transfer function. Regarding (4.13), the maximum current amplitude is always bounded to a predetermined value ($i^{max}{}_{rec}$), which is set in accordance with the loads' requirement. Equation (4.13) also reveals that since the proposed CRE is formulated using the DC currents, FSMPC receives a smooth reference, which is insensitive to the oscillations of capacitors' voltages. As a result, the undesired transient effects in the DC voltages and currents are suppressed by employing the CRE.

4.3.2 The Stability Objective

Concluded from (4.14), AMPC inherently provides a bounded-input bounded-output (BIBO) form of stability for the MPUC7 since the control signals and the output voltage are always restricted to the predetermined switching vectors (μ) and the voltage levels defined in Table 4.1. Compared with the BIBO stability concept, the Lyapunov stability theory provides the most reliable and accurate tools to design controllers with global asymptotic stability. Regarding the Lyapunov stability theory, the controlled system is stable if and only if a definite positive and continuously differentiable function exists in such a way that its derivative always becomes negative. However, the derivative of the definite positive function is not available in the case of the AMPC since it is a discrete controller.

$$\begin{cases} V_{AB}\ \left(\ \mu(k),\ V_{C1}(k),\ V_{C2}(k)\ \right) \le V_{C1}(k) + V_{C2}(k) \\ \quad \forall \mu(k) \in \left[\ 1,\ ...,\ 8\ \right],\quad \forall k \in \mathbb{Z} \\ i_{rec}(k) \le \left(\pi \left(\dfrac{V_{C1}(k)}{2R_{L1}} + \dfrac{V_{C2}(k)}{2R_{L2}} \right) \right) \sin(\omega k) \quad \forall k \in \mathbb{Z} \\ V_{C1}(k) \le V_g(k) \quad \forall k \in \mathbb{Z} \\ V_{C2}(k) \le V_{C1}(k) \quad \forall k \in \mathbb{Z} \end{cases} \tag{4.14}$$

To address the stability problem, this paper proposes a discontinuous definite positive Lyapunov function where its derivative with respect to its predicted value for the next sampling period is obtained to design a decupled stability objective. To develop this stability objective, the following positive definite function in (4.15) is proposed:

$$\varphi(t) = \frac{1}{2} \left(\mathrm{e}_{VC1}^2(t) + \mathrm{e}_{VC2}^2(t) + e_{i\_rec}^2(t) \right) \tag{4.15}$$

where e_{VC1}, e_{VC2}, and e_{i_rec} are respectively the error functions for the voltages of the capacitors and the rectifier input current as detailed in (4.16).

$$\begin{cases} \mathrm{e}_{VC1}(t) = V_{C1}(t) - V_{C1}^{*} \\ \mathrm{e}_{VC2}(t) = V_{C2}(t) - V_{C2}^{*} \\ \mathrm{e}_{i\_rec}(t) = i_{rec}(t) - i_{rec}^{*}(t) \end{cases} \tag{4.16}$$

The controlled system is globally asymptotically stable if the derivative of (4.15) is a negative definite function. Accordingly, the derivative of (4.15) is calculated in (4.17) to evaluate the stability criteria.

$$\frac{d\,\varphi(t)}{dt} = \frac{\mathrm{de}_{VC1}(t)}{dt}\ \mathrm{e}_{VC1}(t) + \frac{\mathrm{de}_{VC2}(t)}{dt}\ \mathrm{e}_{VC2}(t) + \frac{de_{i\_rec}(t)}{dt}\ e_{i\_rec}(t) \tag{4.17}$$

Since the references of the capacitors' voltages are constant, (4.17) is simplified as below:

$$\begin{aligned} \frac{d\,\varphi(t)}{dt} = &\left(\frac{dV_{C1}(t)}{dt} \right) \mathrm{e}_{VC1}(t) + \left(\frac{dV_{C2}(t)}{dt} \right) \mathrm{e}_{VC2}(t) \\ &+ \left(\frac{di_{rec}(t)}{dt} - \frac{di_{rec}^{*}(t)}{dt} \right) e_{i\_rec}(t) \end{aligned} \tag{4.18}$$

Equation (4.18) is not suitable to evaluate the AMPC stability condition because of existing the continuous-time dynamics. However, the discretized form of the Lyapunov function and its derivative could be considered in the AMPC cost function to predict the stability condition for the next sampling period. Accordingly, the predicted Lyapunov function for the next horizon is obtained in (4.19) by using the forward Euler method and some simplifications.

$$\begin{aligned} \varphi(k+1) = &\ \varphi(k) + \left(V_{C1}(k+1) - V_{C1}(k) \right) \mathrm{e}_{VC1}(k) \\ &+ \left(V_{C2}(k+1) - V_{C2}(k) \right) \mathrm{e}_{VC2}(k) \\ &+ \begin{pmatrix} i_{rec}(k+1) - i_{rec}(k) - 2i_{rec}^{*}(k) \\ - \dfrac{T_S \pi}{2} \left(i_{dc1}(k) + \mathrm{i}_{dc2}(k) \right) \cos(\omega k) \end{pmatrix} e_{i\_rec}(k) \end{aligned} \tag{4.19}$$

where $\varphi(k)$ is the discrete Lyapunov function in the current sampling time calculated by means of the following equation:

$$\varphi(k) = \frac{1}{2}\left(\mathrm{e}_{VC1}^2(k) + \mathrm{e}_{VC2}^2(k) + e_{i\_rec}^2(k) \right) \tag{4.20}$$

The derivative of the discrete Lyapunov function with respect to its predicted value in the next sampling period is obtained in (4.21) based on (4.20) and (4.19).

$$\dot{\varphi}(k) = \frac{\varphi(k+1) - \varphi(k)}{(k+1)T_s - kT_s} \tag{4.21}$$

This equation is to assess the octet switching vectors shown in Table 4.1 through the predicted equations of the capacitors' voltages and the rectifier input current to find the switching state that guarantees the stability of the closed-loop system for the next sampling instance. Since (4.21) is a non-zero negative value, it cannot be directly used in the AMPC cost function. Consequently, (4.22) is developed in the next step to generate $\phi(k+1)$, which is a variable in the range of $[0+ \infty+]$. ζ in (4.22) as a positive constant factor generates large values of $\phi(k+1)$ when the derivative of $\varphi(k)$ is positive, and it causes a negligible value of $\phi(k+1)$ when the derivative of $\varphi(k)$ is negative. Thus, the stability objective has a zero effect on the cost function when the selected switching vector is stable while it makes the maximum effect on the optimization process if the candidate-switching vector causes a positive error in the next sampling period. In other words, the efficiency of AMPC in fulfilling the desired control objectives is significantly improved since the stability objective is completely decoupled from the control objectives.

$$\begin{cases} \phi(k+1) = e^{\zeta\dot{\varphi}(k)} \\ \zeta > \mathbb{R}^+ \end{cases} \tag{4.22}$$

Concerning (4.22), the AMPC cost function is modified as (4.23) to include the stability objective.

$$\begin{aligned} G_{AMPC}(k+1) = \lambda_1 \left| V_{C_1}(k+1) - V_{C_1}^*(k) \right| + \lambda_2 \left| V_{C_2}(k+1) - V_{C_2}^*(k) \right| \\ + \lambda_3 \left| i_i(k+1) - i_i^*(k) \right| + \lambda_4 S_T^P(k+1) + \phi(k+1) \end{aligned} \tag{4.23}$$

Because of using the exponential function in (4.22), the cost function requires no additional weighting factors to set priority among the stability and the control objectives.

4.3.3 The Weighting Factors Variation Effects

The capacitors' voltages in (4.6) are related to the input and the load currents. On the other hand, the switching operation of MPUC7 directly affects both capacitors' voltages and the input current. Therefore, a nonlinear correlation exists among the main control objectives, which causes a sophisticated training process for the weighting factors. In the following, variation effects of the weighting factors on the cost function are studied using some mathematical analyses to determine the optimal range of values for the weighting factors; aftermath, RBFC is trained based on the mathematical analyses.

In the first step, the following predicted errors for state variables of MPUC7 are considered.

$$\begin{cases} e_{C_1}(k+1) = V_{C_1}(k+1) - V_{C_1}^*(k) \\ e_{C_2}(k+1) = V_{C_2}(k+1) - V_{C_2}^*(k) \\ e_i(k+1) = i_i(k+1) - i_i^*(k) \end{cases} \tag{4.24}$$

To simplify the error terms in (4.24), the following relationships are defined:

$$\begin{cases} \left| V_{C_1}\ (k+1) - V_{C_1}^{*}(k) \right| = sign(e_{C_1}(k+1))e_{C_1}(k+1) \\ \left| V_{C_2}\ (k+1) - V_{C_2}^{*}(k) \right| = sign(e_{C_2}(k+1))e_{C_2}(k+1) \\ \left| i_i\ (k+1) - i_i^{*}(k) \right| = sign(e_i(k+1))e_i(k+1) \end{cases} \tag{4.25}$$

By substituting (4.25) into (4.24), it can meet (4.26) in which the stability objective is ignored since it does not affect the control objectives.

$$\begin{aligned} G_{AMPC}(k+1) = {} & \lambda_1 e_{C_1}(k+1)sign(e_{C_1}(k+1)) \\ & + \lambda_2 e_{C_2}(k+1)sign(e_{C_2}(k+1)) \\ & + \lambda_3 e_i(k+1)sign(e_i(k+1)) + \lambda_4 S_T^P(k+1) \end{aligned} \tag{4.26}$$

Using (4.26), the relationship between e_{C2} and λ_z ($z\epsilon\{1, 2, 3, 4\}$) can be stated as below:

$$\begin{aligned} & e_{C_2}(k+1)sign(e_{C_2}(k+1)) = \\ & \left[\begin{array}{l} G_{FMPC}(k+1) - \lambda_1 e_{C_1}(k+1)sign(e_{C_1}(k+1)) \\ -\lambda_3 e_i(k+1)sign(e_i(k+1)) - \lambda_4 S_T^P(k+1) \end{array} \right] / \ \lambda_2 \end{aligned} \tag{4.27}$$

It should be first stated that the relationship in (4.27) can be governed by the other errors including e_{C1} and e_i as well. Equation (4.27) leads to the three-dimension curves illustrated in Figure 4.2. This figure exhibits the three-dimension curves of the error e_{C2} based on λ_2 and λ_3 with various values of $S_T^P(k+1)$ for $0<\lambda_2, \lambda_3<1$. According to Figure 4.2(a), the smaller values for λ_2 and λ_3 in the interval $0<\lambda_2, \lambda_3<1$ will propel the error e_{C2} toward very large levels. To specify more effective weighting factors in the interval $0<\lambda_2, \lambda_3<1$, the three-dimension curves of e_{C2} are plotted in Figure 4.2(b) in the interval $0.7<\lambda_2, \lambda_3<1$. In this interval, as can be seen from Figure 4.2(b), the error e_{C2} is noticeably reduced as the $S_T^P(k+1)$ changes accordingly. From Figure 2(a) and Figure 2(b), one can be concluded that the error e_{C2} increases when $S_T^P(k+1)$ decreases. Figure 4.2(c) demonstrates the three-dimension curves of the error e_{C2} in various intervals for λ_2 and λ_3.

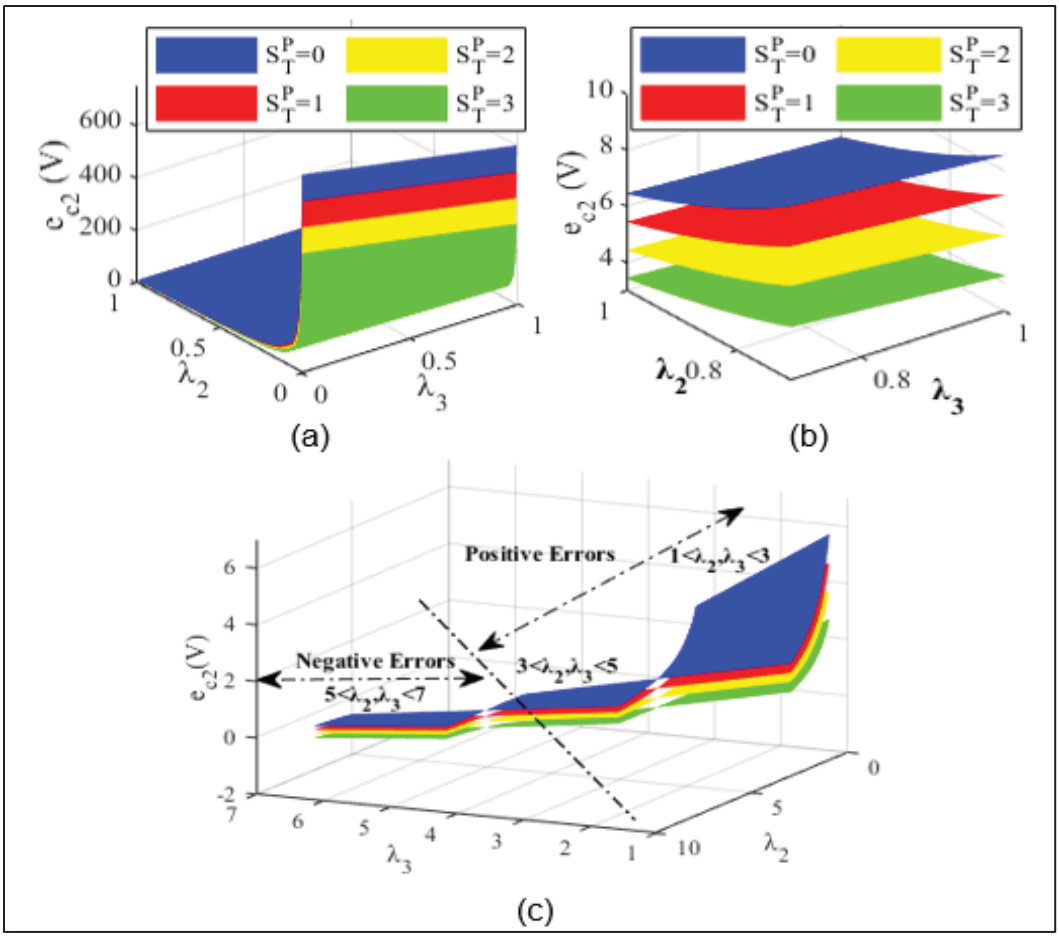

Figure 4.2 Three-dimension curves of the error e_{C2} based on the weighting factors of λ_2 and λ_3 with various predicted switching models when, (a) $0 < \lambda_2, \lambda_3 < 1$, (b) $0.7 < \lambda_2, \lambda_3 < 1$, and (c) $1 < \lambda_2, \lambda_3 < 7$

In the interval $1<\lambda_2, \lambda_3<3$, the error e_{C2} is quickly decreased by the increment of the weighting factors. This trend approximately happens for the middle values of the interval $3<\lambda_2, \lambda_3<5$ as depicted in Figure 2(c). Based on this figure, the other values of $3< \lambda_2, \lambda_3<5$ and the whole interval $5< \lambda_2, \lambda_3<7$ will lead to negative values for the error e_{C2}, which are not acceptable as can be found accordingly from (4.27). Figure 4.3 indicates the effects of the increment of the MPUC7 current error upon the three-dimension curves of the error e_{C2} for various intervals of the weighting factors λ_2 and λ_3 with S_T^P=3.

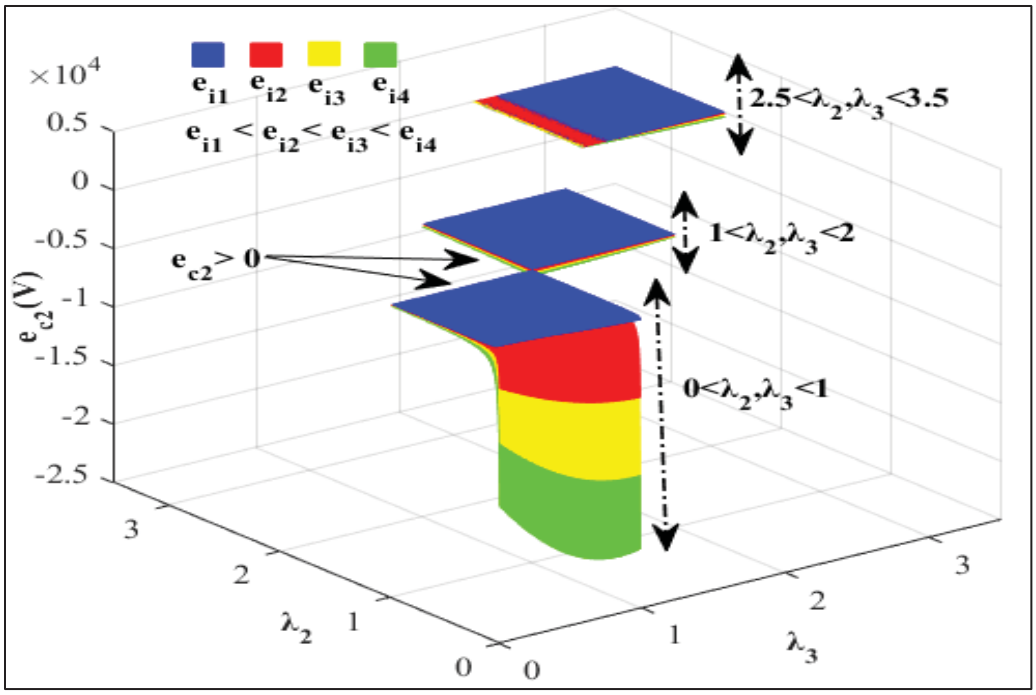

Figure 4.3 The effects of increasing the MPUC7 current error on the three-dimension curves of the error e_{C2} for various intervals of the weighting factors λ_2 and λ_3 with S_T^P=3

$$
\begin{aligned}
& e_{C_2}(k+1)sign(e_{C_2}(k+1)) = \\
& \left[\begin{array}{l}
G_{FMPC}(k+1) - \lambda_1 e_{C_1}(k+1)sign(e_{C_1}(k+1)) \\
-\lambda_3 \left[i_i(k) + \dfrac{T_s}{L_f} \left(\begin{array}{l} V_g(k)- \\ V_{AB}(k+1) \\ -R_f i_i(k) \end{array} \right) - i_i^*(k) \right] sign(e_i(k+1)) \Big/ \lambda_2 \\
-\lambda_4 S_T^P(k+1)
\end{array} \right]
\end{aligned}
\tag{4.28}
$$

To attain these curves, (4.7) is situated within (4.27) leading to (4.28). As can be realized from Figure 4.3, larger values of the error e_{C2} are resulted from increasing the weighting factors. The majority of weighting factors in the interval $0< \lambda_2, \lambda_3<1$ are not acceptable because of negative values of the error e_{C2} as can be seen from Figure 4.3. In addition, Figure 4.2 and Figure 4.3 reveal that the most and least effects are respectively associated with the interval $0<\lambda_2, \lambda_3<1$ and $1< \lambda_2, \lambda_3<2$, due to the current error increment.

The mathematical analysis results provided in Figure 4.2 and Figure 4.3 also discover that λ_2 and λ_3 are the critical weighting factors with major impacts on the capacitors' voltages and input current. Moreover, these analyses prove that increasing the switching frequency reduces the balancing error of capacitors. However, it should be noted that the switching loss is directly related to the switching frequency.

4.3.4 The Proposed Radial Basis Function Controller

Since the nonlinear relation among the predicted terms defined in (4.23) is unknown and unique, no accurate and generalized mathematical techniques are available to adjust the weighting factors. In this case, the capability of ANN theory as a powerful tool in modeling and identification of nonlinear systems can be considered to design a model-free online estimator for the weighting factors.

ANN as a flexible computational network is able to operate in different physical and mathematical problems like control, clustering, identification, simulation, and prediction. Among all neural network topologies, RBF is mostly used in control problems due to its simple structure, short learning process, and smooth output signal (Dash, Mishra, & Panda, 2000). As shown in Figure 4.4 three layers, including the input, hidden, and output, construct the RBF network. The measured signals are applied to the input layer, they are processed in the hidden layer and the results are available in the output layer.

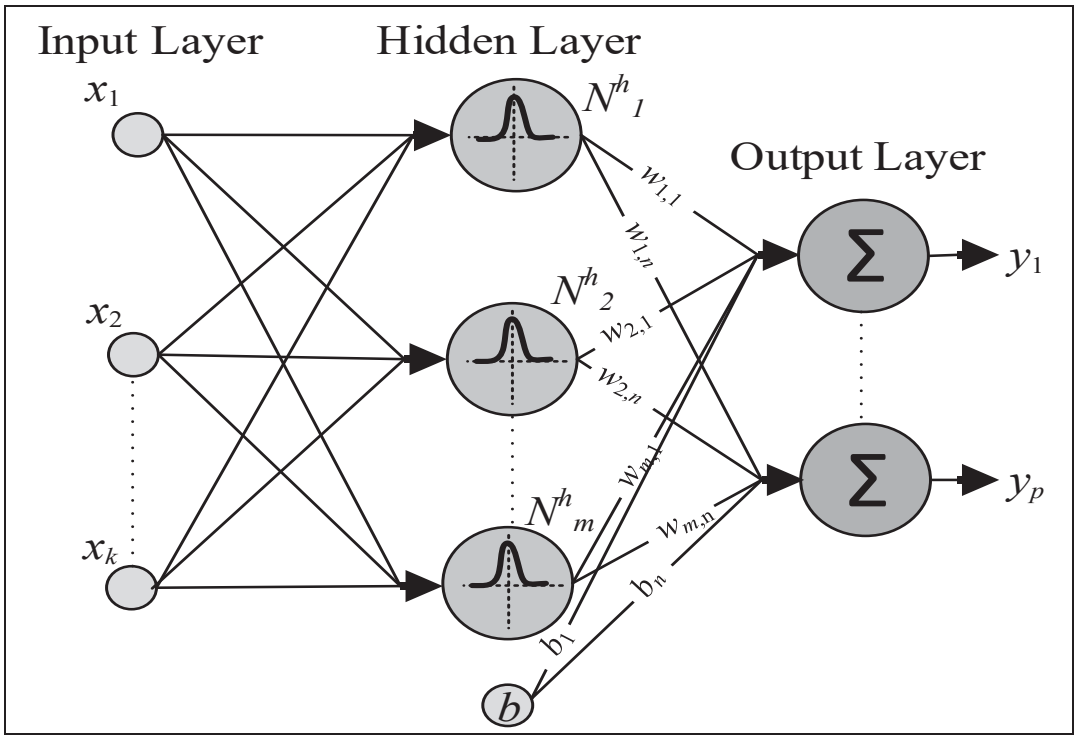

Figure 4.4 General structure of the radial basis function artificial neural network

Neurons are placed in the hidden layer and they are connected to the outputs through weighting factors. The outputs are also biased by constant values to regulate their levels. Equation (4.29) presents the generalized model of the RBF.

$$y_i = \sum_{i}^{n} \sum_{j}^{m} w_{ji} \psi_j \left(\bar{x} \right) + b_i \tag{4.29}$$

where y_i is ith output, $\bar{x} = [x_1, x_2, \dots, x_k]$ is the inputs vector, w_{ij} presents the weighting factor from the jth neuron to the ith output, b_i depicts the bias for the ith output and ψ_j shows the activation function for the jth neuron. Despite other ANN topologies, the activation function in RBF must be only a decreasing function. This feature is used to measure Euclidean distance among the activation function centers and the sampled input data. In this regard, Gaussian as an appropriate decreasing function is proposed in (4.30) to measure the Euclidean distance.

$$\psi_j = \exp\left(- \frac{\left\| x_k - c_j \right\|^2}{2\sigma_j^2} \right) \tag{4.30}$$

where c_j and σ_j are the center and field width for the jth activation function. In comparison with other topologies like multilayer Perceptron, RBF generates a smoother control signal using minimum neurons since ψ_j is calculable for any input value. The RBF weighting factors, biases, and Gaussian parameters determine the RBF network behavior. Thus, they must be properly trained to have the desired performance. In previous efforts (Machado, Martín, Rodríguez, & Bueno, 2017; Dragičević, & Novak, 2018), supervised techniques using tremendous data obtained from a reference model were employed to train the ANN parameters. The supervised methods used by (Machado, Martín, Rodríguez, & Bueno, 2017; Dragičević, & Novak, 2018) suffer from two major defects during the training process. First, a reliable reference model or an analytical method is required to attain the training data that is difficult to find. Second, the training data must sufficiently include the dynamic behavior of the model, which results in a huge database and causes a time-consuming training process. In this paper, a novel self-training technique based on the PSO algorithm is proposed without using any reference model and training data to adjust the RBF parameters. This technique is much faster and more accurate than the supervised techniques (Machado, Martín, Rodríguez, & Bueno, 2017; Dragičević, & Novak, 2018) proposed to design an ANN-based auto-tuner for the FSMPC weighting factors. In the first step of the proposed self-training technique, the following cost function, the so-called integral of squared error (ISE), is formulated using the error of the capacitors' voltages and the rectifier current to provide proper optimization feedback for the PSO algorithm:

$$ISE = \int_0^{t_o} e_t^2(t)dt \tag{4.31}$$

where t_o is the operation time for the PSO during each iteration and $e_t(t)$ is the training error signal defined in (4.32). ISE specifically magnifies large transient errors; thus, the training

process mainly focuses on the suppression of overshoots and undershoots in the voltages and currents of the rectifier.

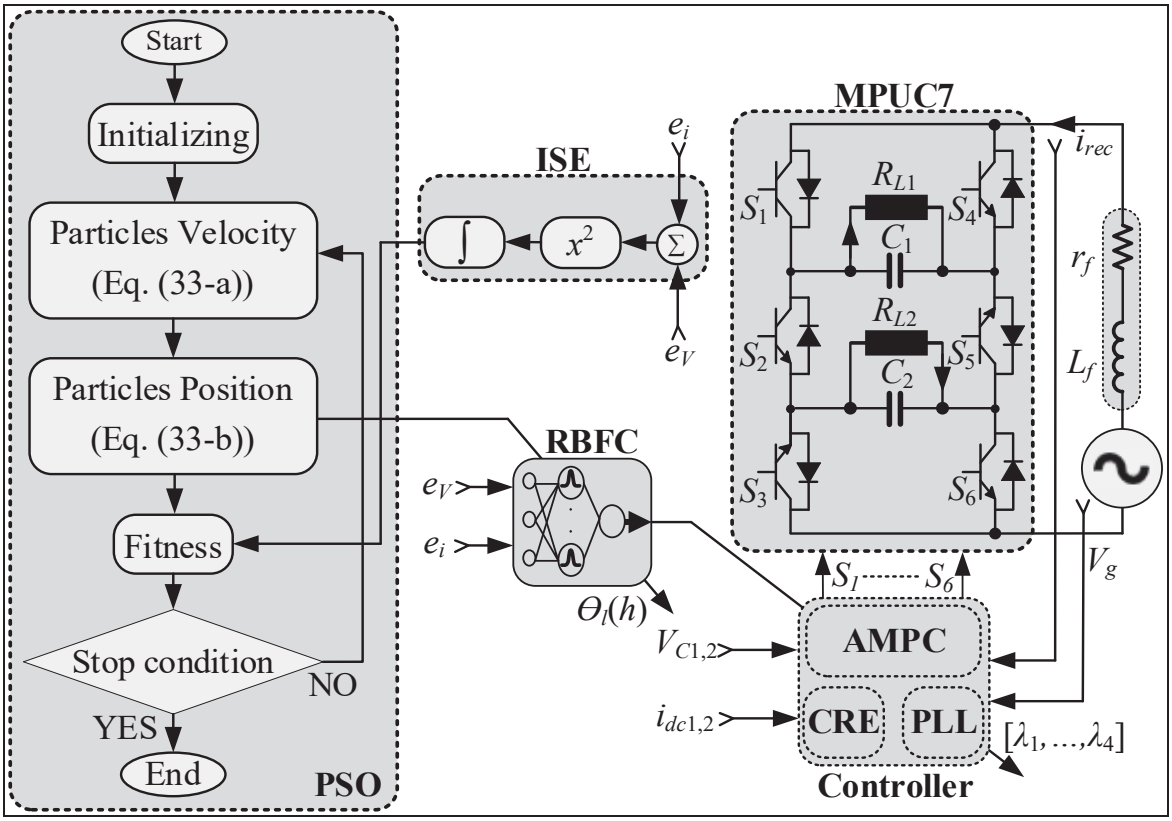

Figure 4.5 Block diagram of the self-training technique, including the PSO algorithm and ISE cost function applied to the RBFC during the operation of the AMPC

$$e_t(t) = \left(V_{C1}(t) - 2V_{C2}(t) \right)^2 + (i^*_{rec}(t) - i_{rec}(t))^2 \tag{4.32}$$

In the second step, the PSO equations, including the particles' positions and velocities are formalized using the RBF parameters as shown in (4.33-a) and (4.33-b), respectively.

$$\begin{cases} a)\ V_{\theta_l}(h+1)=V_{\theta_l}(h)+\varepsilon_1\tau_1(\theta_l^b-\theta_l(h))+\varepsilon_2\tau_2(\theta_G-\theta_l(h)) \\ b)\ P_{\theta_l}(h+1)=\theta_l(h)+V_{\theta_l}(h+1) \end{cases} \tag{4.33}$$

where $V_{\theta l}(h+1)$, $P_{\theta l}(h+1)$, $V_{\theta l}(\mathrm{h})$, and $b_{\theta l}(h)$ are the next and the present velocities and positions for the lth particle in the hth iteration respectively. ε_1 and ε_2 are the PSO factors bounded to [0 2] and τ_1, and τ_2 are random values restricted to [0 1]. $\theta_l(h)$ is the lth particle in the hth iteration, including the RBF parameters as below:

$$\theta_l = \left[W,\ \bar{b},\ \beta \right] \tag{4.34}$$

Regarding (4.34), each particle includes the weighting factors matrix (W), biases vector ($\bar{b}$), and the Gaussian parameters matrix (β) as defined in (4.35). The proposed self-training technique is designed in Figure 4.5 to set the RBF parameters shown in (4.35) using the ISE cost function defined in (4.31) and the PSO algorithm customized in (4.33).

$$W = \begin{pmatrix} w_{11} & \cdots & w_{j1} & w_{m1} \\ \vdots & \ddots & & \vdots \\ w_{1i} & \cdots & w_{ji} & w_{mn} \end{pmatrix},\quad B = \begin{pmatrix} b_1 \\ \vdots \\ b_i \\ b_n \end{pmatrix},\quad \beta = \begin{pmatrix} c_1 & \sigma_1 \\ \vdots & \vdots \\ c_j & \sigma_j \\ c_m & \sigma_m \end{pmatrix} \tag{4.35}$$

Regarding Figure 4.5, the control loop, including ASMPC, CRE, and RBFC, generates proper switching signals for the MPUC7 rectifier while the learning loop, including ISE and PSO, modifies the RBFC parameters during the training process. The training process is online and operates in parallel to the control loop. The RBFC is configured by two inputs to measure the balancing error of the capacitors' voltages (e_V) and the tracking error of the reference current (e_i) as presented in (4.36), and four outputs to control the FSMPC weighting factors.

$$\begin{cases} e_V(t) = V_{C1}(t) - 2V_{C2}(t) \\ e_i(t) = i^*_{rec}(t) - i_{rec}(t) \end{cases} \tag{4.36}$$

It is worth mentioning that a reference current step change is intentionally applied to the control loop during each iteration of the training process in order to increase the RBFC robustness in

unstable conditions. The self-training loop operates beside the control loop until RBFC provides optimal weighting factors for the AMPC.

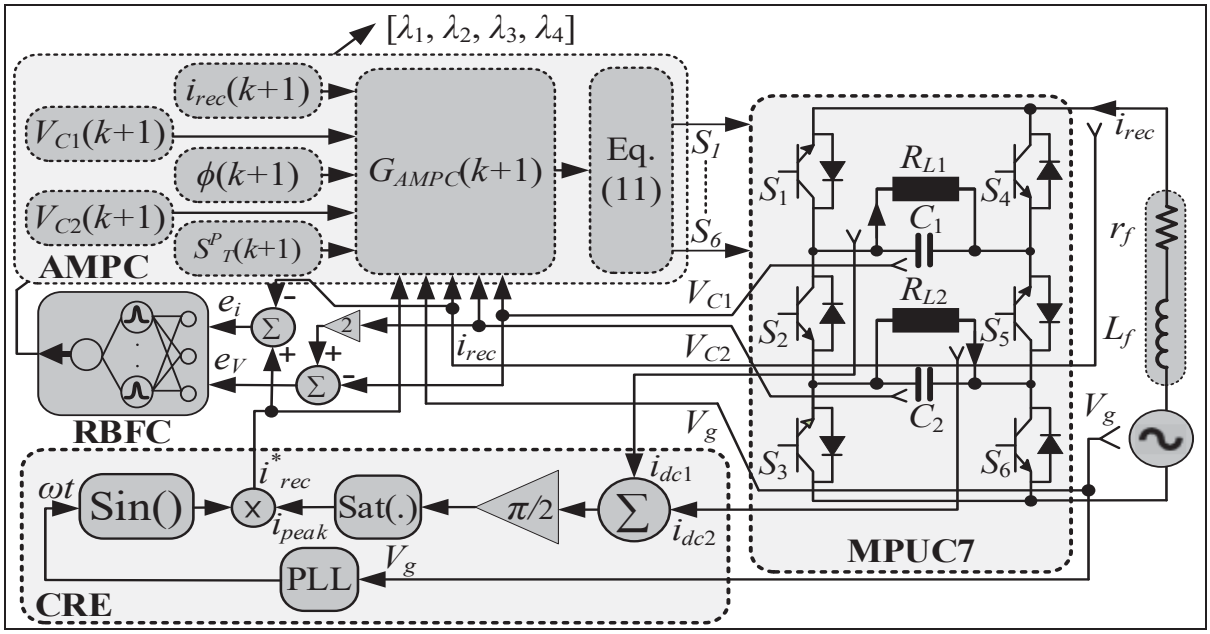

Figure 4.6 The proposed AMPC technique implemented for the MPUC7 active rectifier using dSPACE-1202 and MATLAB

Since no training data is used to adjust the RBFC, the initial values for the proposed unsupervised training technique should be properly determined to reduce the learning time. Thus, the self-training loop is initialized by the parameters provided in Table 4.2; the initial values are inspired by the mathematical analyses provided in Section III-C. Accordingly, the RBFC is properly trained so that the weighting factors are dynamically assigned within the suggested ranges during stable and unstable conditions.

Table 4.2 Initial parameters for the self-training technique

No. of Iterations	**No. of Particles**	**No. of Neurons**	$\varepsilon_1, \varepsilon_2$	W_{ji}	b_i
100	20	10	1.5	[0.1 0.5]	[0.1 0.2]

4.3.5 Trained Adaptive MPC Controller

After 100 epochs of running the self-training technique shown in Figure 4.5, the appropriate RBFC is obtained. Using the error signals of the input current and capacitors' voltages, RBFC adapts the AMPC floating weighting factors online. Thus, the unsupervised training loop is no longer required to be a part of the control loop. In terms of practical implementation, since RBFC uses fewer neurons, it is much simpler than the multilayer Perceptron ANN-based techniques proposed by (Machado, Martín, Rodríguez, & Bueno, 2017; Dragičević, & Novak, 2018). The block diagram of the proposed AMPC applied to the MPUC7 active rectifier is illustrated in Figure 4.6; as shown, the grid voltage, the input current, and the capacitors' voltages are measured and used in the control loop to generate the proper switching pulses for the power switches. The DC currents are also measured to track the load changes using the CRE equation.

4.4 Experimental and Simulation Test Results

To validate the reliability and feasibility of the proposed AMPC technique shown in Figure 4.6, several experimental and simulation tests under different conditions are performed, and the corresponding results are presented in this section. The experimental setup has been implemented using dSPACE-1202 and OPAL-RT measurements as shown in Figure 4.7. MATLAB has been also used to run the simulations. In addition, the MPUC7 and AMPC have been initialized by the parameters defined in Table 4.3.

The first test is done in stable conditions in which the DC loads are considered 80Ω. Figure 4.8 demonstrates the related experimental results for the first capacitor voltage (V_{C1}), the multilevel voltage waveform (V_{AB}), the grid voltage (V_g), and the rectifier current (i_{rec}), respectively. As depicted in Figure 4.8 (a), the capacitor voltage is accurately balanced, a symmetrical seven-level voltage waveform is formed because of the stabilized DC voltages, and the grid voltage and the rectifier current are properly synchronized to meet the unity power factor. Figure 4.8 (b) presents three cycles of V_{AB}, as well as, a short time window of the

capacitors' voltages to investigate the performance of the proposed rectifier and its control loop in terms of DC voltage ripple and the switching incidents.

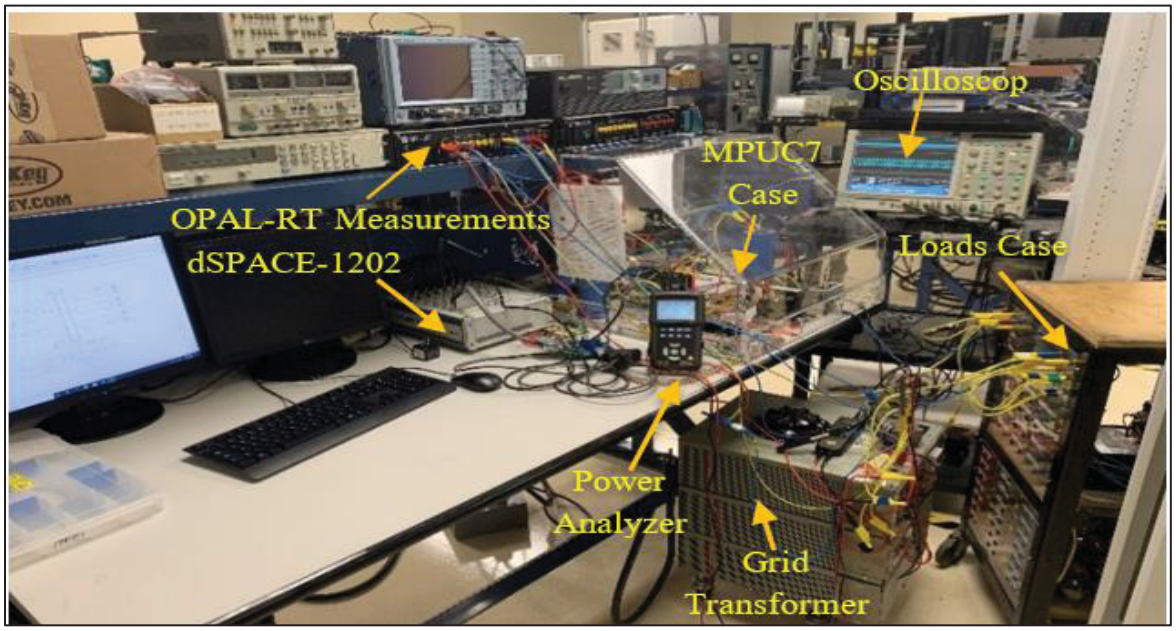

Figure 4.7 Experimental setup including dSPACE-1202 and OPAL-RT measurements for the MPUC7 active rectifier controlled by the proposed AMPC technique

Table 4.3 Experimental and simulation test parameters

Grid voltage (rms)	120 V
DC link capacitor (C_1, C_2)	2100 µF, 1000 µF
The voltage reference for the Dc links (V^*_{C1}, V^*_{C2})	150V, 75V
Fundamental frequency	60 Hz
The grid filter inductance and resistance (L_f & R_f)	5mH and 0.1Ω
DC loads (R_{L1}, R_{L2})	80 Ω
Average switching frequency	2.8 kHz
Sampling time	35 µs
The stability factor (ζ)	50

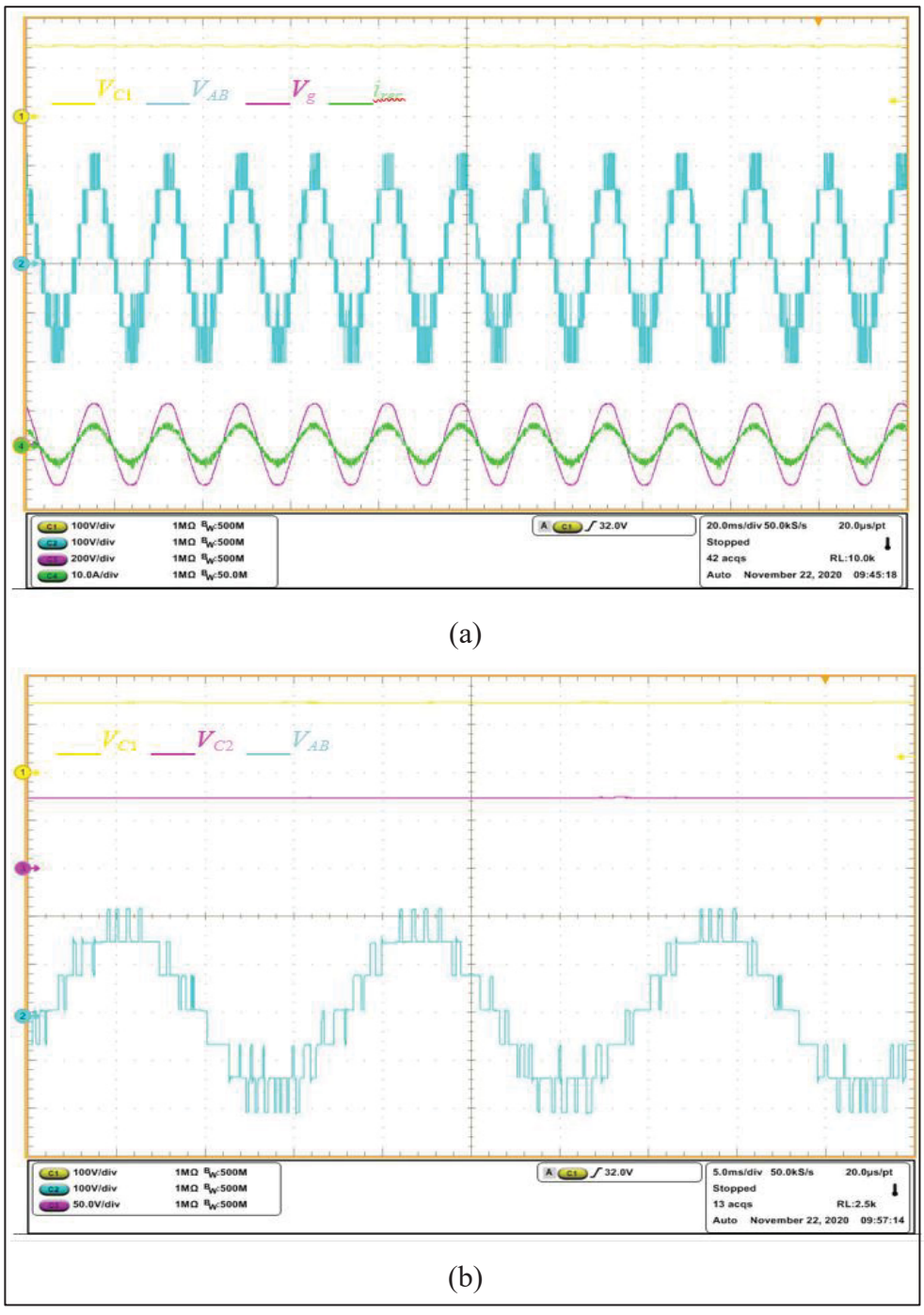

Figure 4.8 Experimental results for the DC-links' voltages (V_{C1}, V_{C2}), seven-level voltage (V_{AB}), and the synchronized grid voltage (V_g) with the rectifier current (i_{rec}); (a) the system performance in stable condition (b) more details about the DC voltage ripple and the switching incidents in the multilevel voltage waveform

As illustrated in Figure 4.8 (b), the voltage ripple is measured at less than 5%. Moreover, the switching incidents in the seven-level waveform prove that the switches in the proposed MPUC7 rectifier are exposed to minimum switching frequency and dv/dt thanks to (4.10) and (4.11). Consequently, lower power rate switches are required compared with the control techniques proposed by (Vahedi, & Al-Haddad, 2016; Sleiman et al., 2015, November). Moreover, the experimental results in Figure 4.8 prove that the MPUC7, including the AMPC loop, remarkably improves the capacitors' size, voltage ripple, and switching frequency compared with the PUC7 rectifier proposed by (Makhamreh, Trabelsi, Kükrer, & Abu-Rub, 2020). The THD analysis for the grid voltage and current shown in Figure 4.9 also discloses that the MPUC7 controlled by AMPC causes a low level of harmonics and power quality distortion.

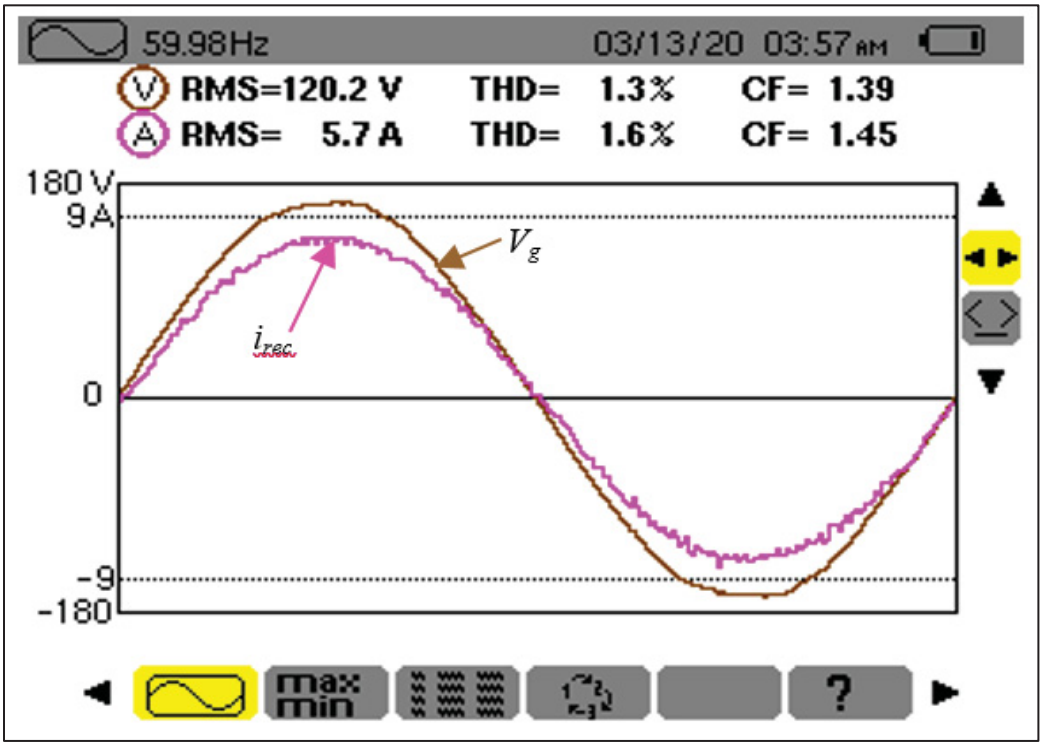

Figure 4.9 THD analysis for the grid voltage (V_g) and current (i_{rec}) under the operation of AMPC

The second test scenario investigates the effects of load variations on the control loop performance. Accordingly, R_{L1} is reduced to 60 Ω as the first step change, and later RL2 is also

stepped down to the same amount. The corresponding experimental results in Figure 4.10 illustrate that the DC voltages are stable without any significant transient while the DC currents precisely track the variations with no damaging transient effects.

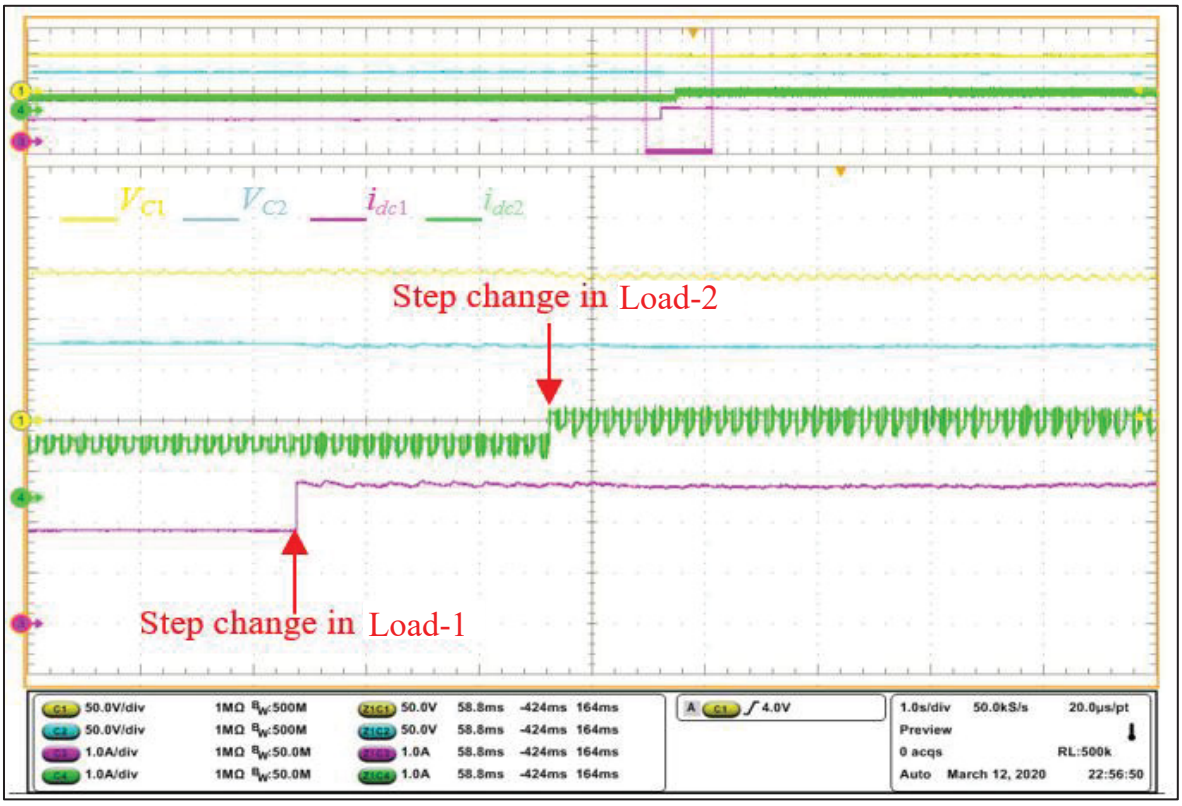

Figure 4.10 Experimental results for the DC voltages and currents during the load variations

Figure 4.11 shows the experimental results for V_{C1}, V_{C2}, i_{rec}, and V_g when the grid voltage peak amplitude oscillates for 20% as an undesired common phenomenon. Regarding Figure 4.11, AMPC desirably regulates the DC voltages in the presence of grid voltage fluctuations. Since AMPC is a model-based controller, its performance directly depends on the model's accuracy. In this case, the proposed control loop is evaluated under parametric mismatches to investigate its robustness.

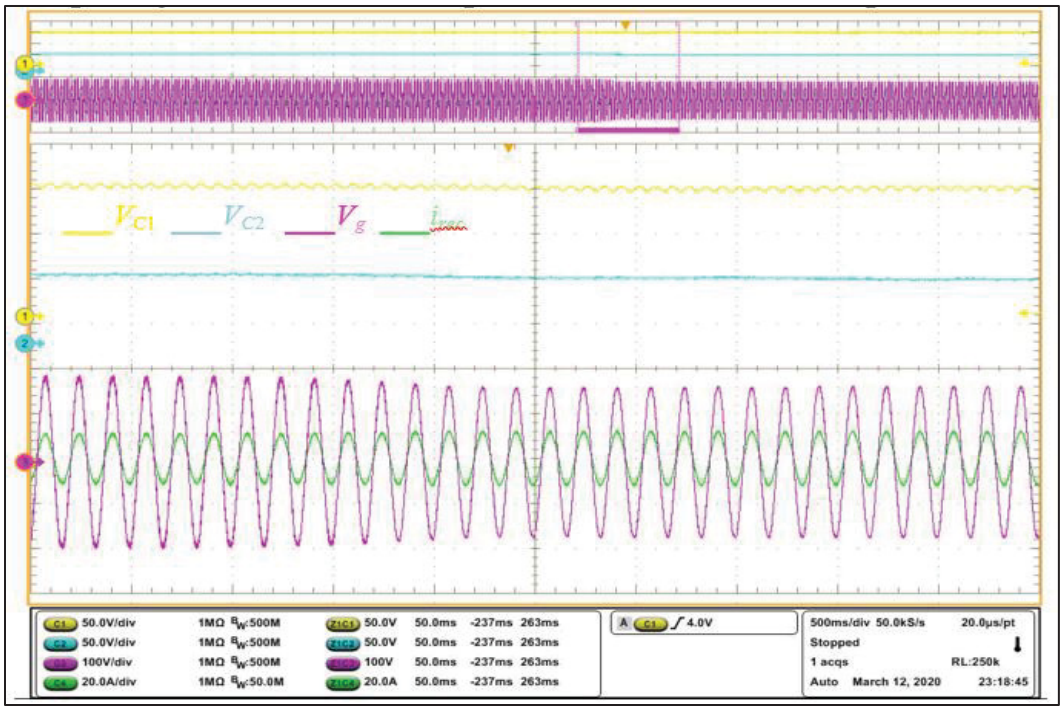

Figure 4.11 Experimental results for the DC voltages as well as the rectifier current and the grid voltage under the grid voltage variations

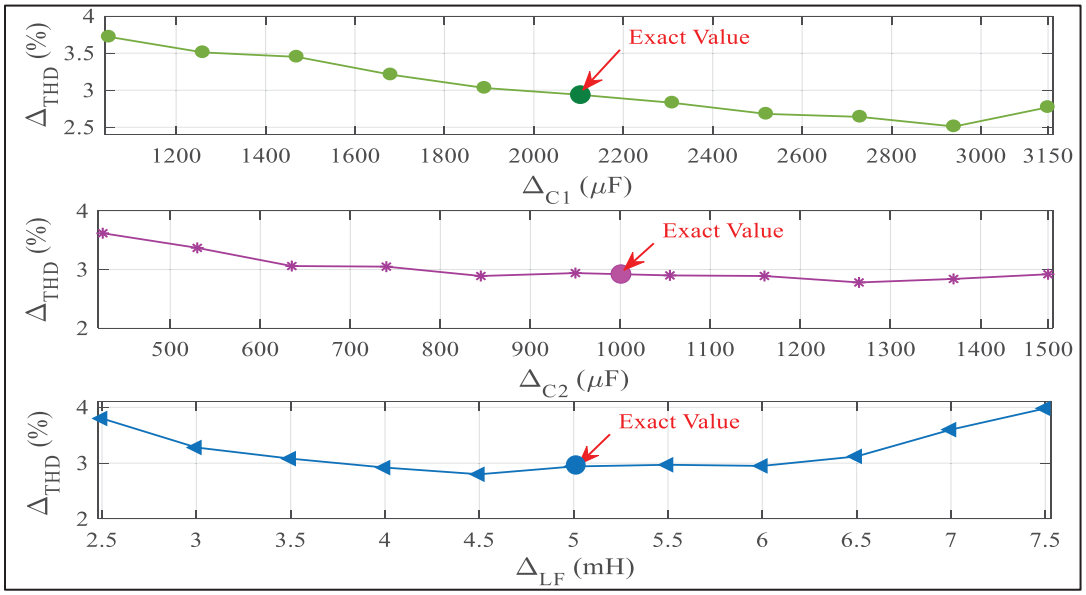

Figure 4.12 THD variations according to the mismatch caused in C_1, C_2, and L_f

Figure 4.12 provides the simulation results of THD variations for ±50% (by 10% step change) mismatch in C_1, C_2, and L_f. Although extreme mismatch has been applied to the MPUC7

parameters, THD is still under 4%. In another test scenario, the switching operation of S_1, S_2, and S_3 is evaluated under two different conditions. First, the predicted model of the switching operation is ignored in the cost function shown in (4.23). Figure 4.13 (a) shows that the switching frequency in S_2 is not equal to the system's fundamental frequency; moreover, S_1 and S_3 operate with different frequencies.

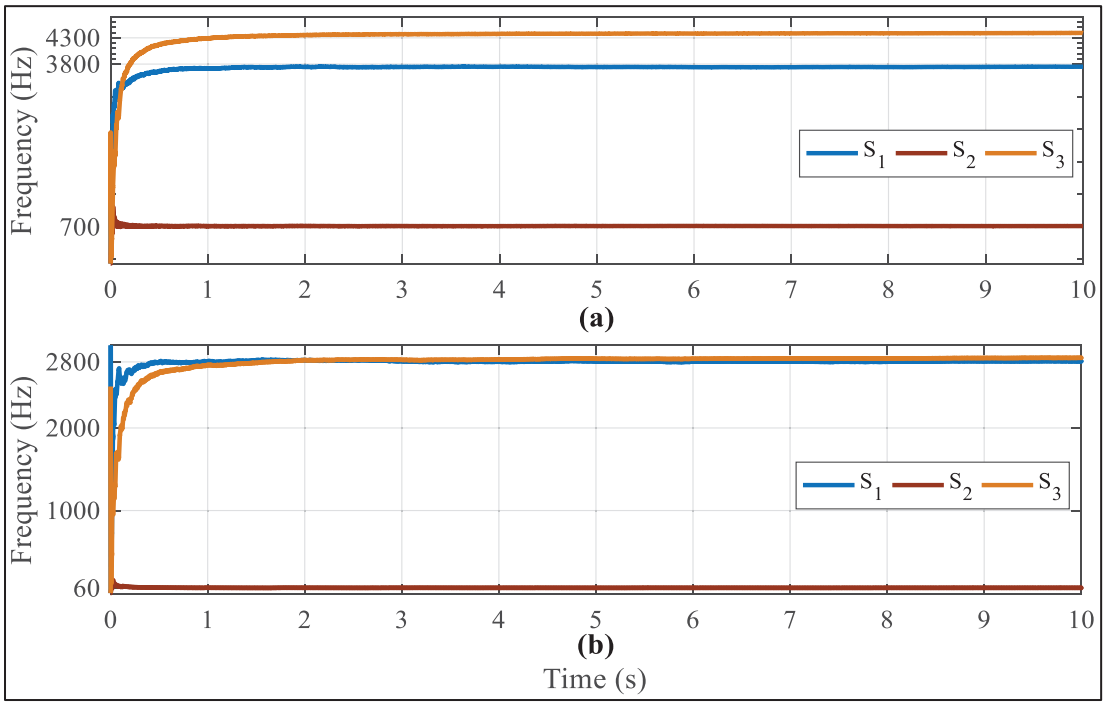

Figure 4.13 Switching operation of S_1, S_2, and S_3 (a) when the predicted switching term is not employed in the AMPC cost function (b) when it is employed

In the second scenario, the cost function formulated in (4.23) is fully employed in the AMPC loop. Figure 4.13 (b) proves that involving the predicted model of the switching operation in AMPC decreases the system average switching frequency and leads to the fundamental frequency in S_2, as well as, the equal switching frequency of S_1 and S_3. In comparison with the FSMPC techniques introduced in (Makhamreh, Trabelsi, Kükrer, & Abu-Rub, 2020; Sleiman et al., 2015, November), the average switching frequency is remarkably reduced from 25 kHz to 2800 Hz by using the proposed AMPC technique. As a result, lower switching loss is attained and the heat dissipation is uniformly distributed among the high-frequency switches (S_1, S_3) so that the design of the cooling system becomes much simpler. For the last

examination, the AMPC performance is evaluated during the startup mode of the converter when the voltages of the capacitors are zero and low power loads are connected to the MPUC7 active rectifier. The related experimental results for V_{C1}, V_{AB}, V_g, and i_{rec} during the initial period are provided in Figure 4.14. According to this figure, AMPC preserves the stability of voltages and currents until the grid voltage reaches the nominal amplitude (120V) and then starts tracking the references in stable conditions. These results reveal that the stability of the DC link is well preserved under large step changes.

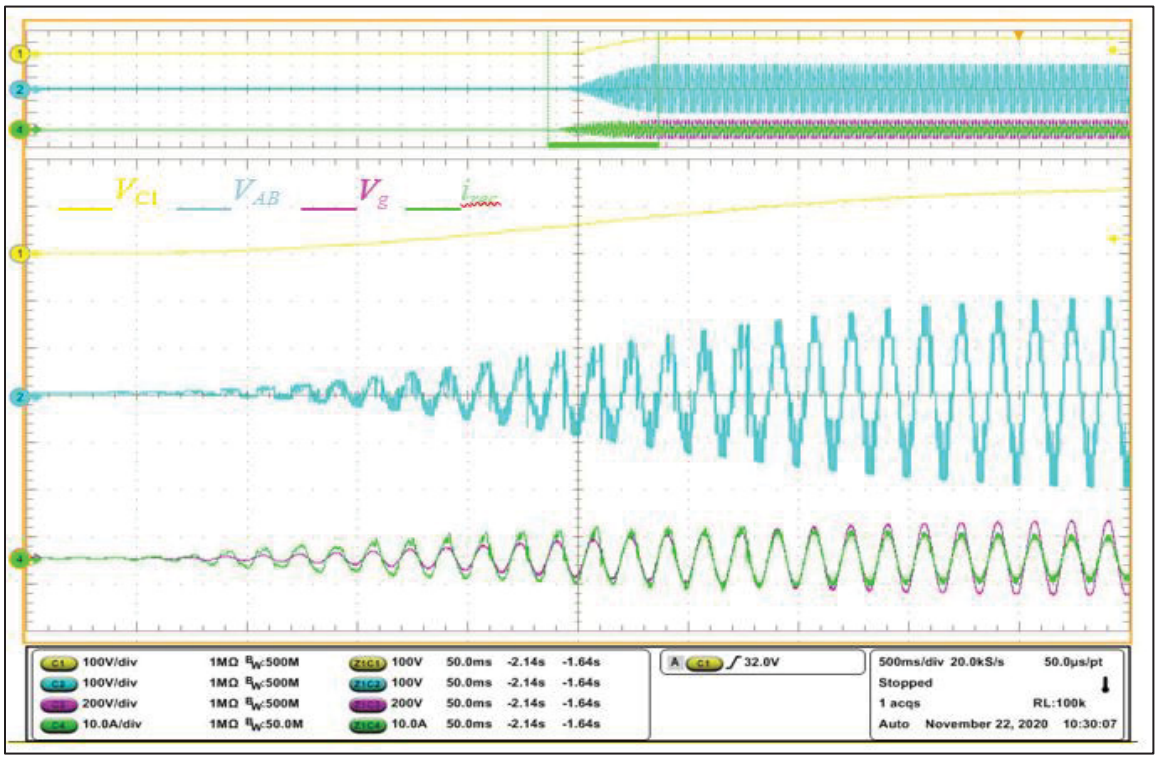

Figure 4.14 Experimental results for the seven-level voltage, the capacitors' voltages, rectifier input current, and the grid voltage during the startup time when $R_1 = R_1 = 80\Omega$

4.5 Conclusion

The reliability and efficiency of the MPUC7 as a promising, cost-effective active rectifier could be guaranteed only if direct control is applied to the capacitors' voltages, input current, and the switching operation of the converter. The literature review reveals that FSMPC is the technique, which can meet such a multi-objective control problem. However, it suffers from

tuning and stability problems. FSMPC inherently provides BIBO stability for the controlled system, but it is not enough to assure its reliability and efficiency in dynamic conditions. This paper shows that the discrete form of a Lyapunov function can be used to provide certain conditions in which the stability of FSMPC is predictable for the next sampling period. The proposed stability analysis in this paper has led to a stability objective in the AMPC cost function, which is separated from the control objectives. As a result, the stability evaluation does not affect the AMPC control performance. On the other hand, the implementation results verify that defining floating weighting factors in the cost function significantly improves the FSMPC dynamic performance and robustness in unstable conditions. The feasibility of ANNs to adjust the floating weighting factors has been formerly proved by (Machado, Martín, Rodríguez, & Bueno, 2017; Dragičević, & Novak, 2018) and developed in this paper (RBFC); however, this research work has remarkably improved the training process of ANNs by proposing the self-training technique. The proposed self-training algorithm is accurate, optimum, fast, and generalizable for other converters and applications because it does not need any training data, modeling, and reference model.

CHAPTER 5

Self-Training Intelligent Predictive Control for Grid-Tied Transformerless Multilevel Converters

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Abstract

Literature reviews affirm the constructive influence of intelligent predictive multi-objective control (IPMOC) on the power quality, power ancillary services, efficiency, and reliability expected from grid-tide transformerless multilevel converters (TMLC). Regarding, this paper contributes to developing the IPMOC concept in terms of training, autonomous power management (APM), and real-time harmonic mitigation. In the proposed IPMOC, model predictive control (MPC) adjusts the power, regulates the DC link capacitors' voltages, reduces the switching transitions, suppresses CMV, and alleviates harmonics using a novel real-time selective-predictive harmonic mitigation (SPHM) objective. As the intelligent part, two artificial neural networks (ANN) trained by a novel data-free, fast, self-training strategy (FSTS) reinforce the MPC to handle the multi-objective task. The first one adapts the weighting factors of the MPC dynamically, while the second one as a model-free controller autonomously adjusts the active and reactive power references of the MPC to assure the unity power factor of the grid in the presence of unknown loads. The proposed IPMOC has been applied to a three-phase neutral point clamped converter and evaluated via various test scenarios run by dSPACE 1202 and MATLAB to verify its effectiveness and feasibility.

5.1 Introduction

With the growing penetration of renewable energy-based transformerless converters and re-active loads into the grid especially microgrids, the power system is adversely affected in terms of voltage stability, power quality, power resilience, and maintenance costs (Cochran et al., 2014; Xiao, 2020). The common-mode voltage (CMV), reactive power, and harmonics distortions are some of the reasons why transformerless converters and re-active loads violate the grid codes (Xiao, 2020). In grid-tied converters, CMV causes leakage current, as the parasitic capacitors connect PV panels to the ground (Rojas et al., 2017). The leakage current leads to electromagnetic interference, destructive harmonics, and malfunctioning performance. Reactive loads, like induction motors, domestic appliances, and electric vehicles also cause voltage oscillation, power factor degradation, and transmission losses (Park, Kwon, & Choi, 2014).

The switching transitions of the converters alongside the nonlinear loads' activities escalate harmonic pollution and reduce the grid power quality. The harmonics caused by the switching transitions in power electronics converters also impact the size of passive components used on both the DC and AC sides of converters. Harmonics increase power losses, cause thermal problems, reduce the components' lifetime, and diminish the converters' efficiency. Since conventional converters generate a two-level voltage waveform, maximum harmonic pollution occurs. As a compromise, a high-order low-pass filter like the LCL needs to be attached to the converter (Kouro et al., 2010). In addition to increasing the device dimension, weight, and cost, the filter also causes resonance disorders, decreases the converter efficiency, and imposes an extra burden on the cooling system in high-power applications. Increasing the switching frequency is a common solution to reduce the size of filters and push back the frequency of harmonics; nonetheless, this strategy intensifies the switching losses and voltage stress over the switching components (Kouro et al., 2010).

5.1.1 Grid-Tied Transformerless Multilevel Converters

Grid-tied transformerless multilevel converters (TMLC), such as neutral point clamped (NPC), active NPC, cascaded H-bridge (CHB), and compact multi-levels prevail over conventional two-level converters in terms of power quality, harmonic distribution, and volume ((Kouro et al., 2010); Vahedi, Shojaei, Dessaint, & Al-Haddad, 2017; Kaymanesh, Babaie, Chandra, & Al-Haddad, 2021a; Kumari, & Jain, 2022; Abarzadeh, & Al-Haddad, 2019). e.g., the voltage level multiplier module proposed by (Abarzadeh, & Al-Haddad, 2019) generates a voltage waveform with up to 85 levels somehow the AC-side filter is no longer required while the grid current THD remains below the standard level. Despite two-level converters, reliability, affordability, efficiency, and power quality in TMLCs rely on the control loop performance due to involving multiple DC links, voltage vectors, and switches. Thus, the development of control algorithms is vital for the future of grid-tied renewable energy-based TMLCs. Modulation-based techniques, multi-objective controllers, and hardware modifications are the prominent solutions proposed so far to enhance the performance of TMLCs for grid-tied applications.

5.1.2 Classic Control Methods

The modulation-based techniques are the most common, practical strategies to diminish CMV, control reactive power, and mitigate low-order harmonics due to the simplicity of implementation (Han et al., 2016). Selective harmonic elimination and mitigation are two popular low-frequency modulation techniques that remarkably improve the THD level and reduce the filtering costs (Sharifzadeh, Vahedi, Portillo, Franquelo, & Al-Haddad, 2018). However, these harmonic reduction techniques are only applicable to the stand-alone mode of operation of TMLCs (Sharifzadeh, Vahedi, Portillo, Franquelo, & Al-Haddad, 2018). A linear control loop including a phase-shift PWM algorithm was introduced in (Liang, Liu, & Peng, 2020) to manage active and reactive power for a grid-tied renewable energy-based quasi-Z-source CHB converter. Concerning a weak grid condition, a normalized Laplacian kernel adaptive Kalman filter was studied by (Kumar et al., 2019) to manage the power of PCC (Point

of Common Coupling) in the presence of reactive loads. A new clamping PWM technique in (Sharma, & Das, 2019) also investigated the possibility of reactive power compensation through a transformerless CHB converter with faulty cells. Although the proposed techniques in (Liang, Liu, & Peng, 2020; Kumar et al., 2019; Sharma, & Das, 2019) properly met the power factor and quality goals, CMV remained unsolved.

Fortunately, many papers proposed various modulation-based techniques to address CMV as well. e.g., the studies by (Du, Wu, & Zargari, 2018) show that asymmetrical grid faults generate a significant level of CMV that is destructive for inductive loads. Thus, a hybrid-linear-PWM strategy based on the CMV model of a grid-connected modular multilevel converter (used as a drive system) was proposed by (Du, Wu, & Zargari, 2018) to mitigate CMV up to one-third of the main dc bust voltage. Phase-disposition PWM as a zero-sequence modulator-based was studied by (Xu, Zheng, Wang, Yang, & Li, 2019) to reduce CMV in back-to-back NPC converters. The implementation results in (Xu, Zheng, Wang, Yang, & Li, 2019) disclose that CMV can be reduced to one-six of the rectifier side voltage. The main idea behind PWM techniques including space vector PWM and carrier-based PWM is to neglect the switching states those result in CMV (Du, Wu, & Zargari, 2018; Xu, Zheng, Wang, Yang, & Li, 2019; Pham, & Van Nguyen, 2019; Le, & Lee, 2018; Chen, & Zhao, 2016). Focusing on CMV or power quality as the main objective in the modulation-based techniques adversely affects the voltage ripple, switching loss, and harmonic distortion somehow using bulky DC capacitors and filters is inevitable.

Alternatively, several hardware modifications like CMV choke (Chen, & Zhao, 2016), inductor-based electrical connection (Grigoletto, 2019), and LCL-based virtual ground (Rahimi et al., 2020) were suggested to suppress CMV besides improving the grid power quality in grid-tied TMLCs. Although the hardware attachments effectively block the leakage current and improve the grid power quality, they may increase power losses, intensify the resonant disorders, and complicate the system dynamic order, especially in the case of multilevel converters due to the essential use of model-based advanced controllers.

5.1.3 Multi-Objective Control

Unlike the previous techniques, advanced multi-objective control methods can overcome the reliability, affordability, efficiency, and power quality issues in grid-tied TMLCs, concurrently. The state of the art demonstrates that MPC is a well-established multi-object control method for grid-tied TMLCs (Karamanakos, Liegmann, Geyer, & Kennel, 2020; Kouro et al., 2008). Conventional MPC however suffers from voltage stress, sensitivity to mismatch, heavy computational burden, tedious tuning, and variable switching frequency (Karamanakos, Liegmann, Geyer, & Kennel, 2020; Kouro et al., 2008; Karamanakos, & Geyer, 2019; Kakosimos, & Abu-Rub, 2017). An optimal sequence MPC was introduced by (Zheng, Dragičević, Zhang, Rodriguez, & Blaabjerg, 2020) to fix the switching frequency. Two-layer MPC (Wang, Li, & Tong, 2019), computational-efficient MPC (Yang et al., 2020), double vector MPC (Liu, Chen, Qin, Chen, & Li, 2020), virtual vector MPC (Yu, Song, Guo, Li, & Saeed, 2020), fast processing MPC (Xing, & Chen, 2019), optimized-vector MPC (Wang et al., 2017), and long prediction horizon MPC (Forestieri, Farasat, & Mitra, 2021) are the techniques that mitigated the computational burden and eliminated the weighting factors. Technically, in the weighting factor-less MPC methods, the cost function is formulated based on a universal objective to remove the weighting factors. To design the universal objective, the relations among all the dynamics need to be mathematically formulated. Nonetheless, designing a universal objective based on dynamics with minimum correlation, such as the switching frequency, CMV, power factor, harmonics, and voltage stress is exhausting or somehow infeasible. As a result, it can be observed that the available weighing factors-less MPC algorithms mostly concentrate on two or three objectives like the converter current, capacitor voltages, and CMV (Liu, Chen, Qin, Chen, & Li, 2020; Yu, Song, Guo, Li, & Saeed, 2020; Xing, & Chen, 2019; Jin, Dai, Xie, Wu, & Guo, 2022; Xiao et al., 2021).

Even though MPC suffers from voltage stress, sensitivity to model uncertainties, computational burden, and variable switching frequency, it has been proven that the drawbacks can be addressed by considering a persistent adjustment to the impact of each control objective on the cost function (Rojas et al., 2017; Kaymanesh, Chandra, & Al-Haddad, 2021b). Using

the weighting factors, the impact of the control objectives on the cost function can be directly controlled or temporarily canceled. This feature however is not available in MPC algorithms with a universal control objective. Regarding, the previous attempts to eliminate the weighting factors or use optimal static ones (Babaie, Sharifzadeh, Mehrasa, Chouinard, & Al-Haddad, 2020; Fretes et al., 2021) adversely affected the optimal performance of the converter and resulted in using bulky components, auxiliary hardware (Wang, Li, & Tong, 2019; Liu, Chen, Qin, Chen, & Li, 2020; Xing, & Chen, 2019; Wang et al., 2017), voltage stress (Yang et al., 2020; Liu, Chen, Qin, Chen, & Li, 2020; Xing, & Chen, 2019), partial CMV suppression (Wang, Li, & Tong, 2019; Liu, Chen, Qin, Chen, & Li, 2020; Yu, Song, Guo, Li, & Saeed, 2020; Wang et al., 2017), and power quality degradation (Yu, Song, Guo, Li, & Saeed, 2020).

The combination of artificial neural networks (ANN) with MPC as an Intelligent Predictive Multi-Objective Control (IPMOC) concept has been widely studied in several papers to observe the nonlinear behavior of the cost function and adapt the weighting factors dynamically (Machado, Martín, Rodríguez, & Bueno, 2017; Dragičević, & Novak, 2018; Vazquez et al., 2021; Liu, Qiu, Wu, Ma, Fang, Peng, & Wang, 2021; Wu, Qiu, Liu, Guo, Rodriguez, Ma, & Fang, 2022). Investigations based on various TMLCs in (Machado, Martín, Rodríguez, & Bueno, 2017; Dragičević, & Novak, 2018; Vazquez et al., 2021; Liu, Qiu, Wu, Ma, Fang, Peng, & Wang, 2021) demonstrate that IPMOC techniques are effective in dealing with the multi-objective design difficulties of TMLCs because ANN can provide a robust, model-free regulator with a smooth transition for several weighting factors regardless of the cost function's nonlinearity. Moreover, TMCLs empowered by ANNs can independently provide smart power management, which is ideal to keep the centralized power management system simple and enhance cybersecurity in smart grids. Even so, the state of the art reveals that ANN-based control methods in power electronics applications are trained through supervised, offline algorithms. The accuracy and efficiency of offline training strategies highly depend on training data as well as on expert knowledge. Note that many scenarios under various operating conditions should be considered by an expert to attain the best training data (Dragičević, & Novak, 2018). In the case of TMLCs, the data acquisition and training are exhausting because of the considerable number of variables, discontinuous behavior of system

trajectories, structural/parametric uncertainties, and fast dynamic performance. Subsequently, increasing the number of weighting factors exponentially complicates the conventional offline training strategies so that commercial computers may not be able to train an ANN with multiple inputs and outputs in a reasonable time (Dragičević, & Novak, 2018).

5.1.4 Novelties and Improvements

Following the previous efforts toward developing a mature IPMOC for grid-tied TMLCs, this paper first contributes to developing a novel data-free, fast, self-training strategy (FSTS) for ANNs used in power electronics control problems, especially TMLCs. Second, a decentralized Autonomous ANN-based power management (APM) strategy is designed for TMLCs to independently regulate the power factor of the grid in the presence of unknown loads. As for the third contribution, a novel real-time selective-predictive harmonic mitigation (SPHM) objective is developed for MPC-based control algorithms to mitigate harmonics in grid-tied TMLCs.

The proposed FSTS transforms the training problem of ANN into an optimization one and then evolves the imperialist competitive algorithm (ICA) (Atashpaz-Gargari, & Lucas, 2007, September) to optimize the parameters of ANN using a proper cost function. The cost function evaluates the control loop performance during the optimization process. Thanks to FSTS, ANN can serve as a regulator for the weighting factors or an independent model-free robust controller for tracking purposes without any restriction to expand the inputs and outputs.

Concerning the expected rapid growth of grid-tied DGs, and their importance for transportation and electrification applications along with renewable energy applications, an advanced communication-based power management system with high-security layers is required to ensure that the grid exchange of power and the power quality are ensured and safely maintained. Regarding, the proposed APM appears effective, as TMLCs can autonomously regulate the grid power factor and provide power ancillary services.

The proposed real-time SPHM improves the harmonic profile of the current and minimizes the size of DC link capacitors in TMLCs. To the best of the authors' knowledge, this is the first time that the predictive model of harmonics is suggested without using any FFT algorithm (Xue, Ding, & Li, 2020; Aggrawal et al., 2011, November). Since the FFT-based harmonic mitigation algorithms calculate the instantaneous value of the harmonics based on a time window including at least several samples of the waveform, an additional computational delay is imposed on the controller. Thus, more expensive hardware is required to compensate for the computational delay and store the sampled waveforms. Concerning the hardware requirements, the complexity of the FFT-based methods dramatically increases when more harmonics need to be mitigated.

5.1.5 Case Study

As a case study, a grid-connected system, including a transformerless three-phase NPC, is considered to practically evaluate the proposed IPMOC technique in terms of training, autonomous power management, and selective-predictive harmonic mitigation. The proposed IPMOC is designed to eliminate CMV, regulate the grid power factor, mitigate harmonics, and preserve the converter efficiency by reducing the switching frequency, DC voltage ripple, and voltage stress. The multi-objective task in the IPMOC is handled by the MPC term in which the cost function is defined based on the predictive dynamic models of the objectives. The weighting factors in the complex cost function of the IPMOC are dynamically adjusted by the first ANN unit, as a regulator. The second ANN unit as a controller also intelligently adjusts the active and reactive reference powers for the MPC term to assure the unity power factor of the grid. Since NPC is industrial, applying the proposed HIPC to this converter yields more reliable conclusions. After a detailed introduction to multi-objective control algorithms, in the following, Section 5.2 provides necessary information about the case study. Section 5.3 details the IPMOC including the proposed FSTS, APM, and SHMO. Section 5.4 demonstrates the implementation outcomes and Section 5.5 presents the conclusions.

5.2 Modeling and Descriptions of the System

A transformerless grid-tied multilevel converter can provide desired power ancillary services if a reliable multi-objective control strategy effectively controls the converter based on the PCC condition. On the other hand, the objectives and dynamic model of the grid-connected system greatly influence the multi-objective performance of the controller. Thus, the candidate power system including NPC is properly modeled in this section based on the desired objectives. Figure 5.1 illustrates a three-phase PV-based transformerless NPC connected to the grid along with several unknown linear and nonlinear loads. As shown, NPC provides power ancillary services for the grid using a renewable energy source when the loads are connected to the PCC. Each leg of NPC represents one phase and generates a three-level voltage, which is between the neutral point of the DC link (g) and the output terminals A, B, and C. Table 5.1 shows the switching states and corresponding voltage levels for one leg of NPC. As shown in Figure 5.2, three-phase NPC generates 27 switching and 18 voltage vectors. Eight switching vectors such as (-, -, -), (+, +, +) in zone V_0 are called the redundant switching vectors because they generate the same voltage level. The switching vectors should be properly selected by the control loop to meet the desired objectives. The modeling is performed on the schematic shown in Figure 5.1 and applied to the fundamental variables including the three-phase current, the branch voltages, the DC capacitor voltages, and CMV. To simplify the dynamic equations of the grid-tied converter, the reactive and nonlinear loads are considered unknown. However, the impact of loads on the PCC is considered in the control design problem.

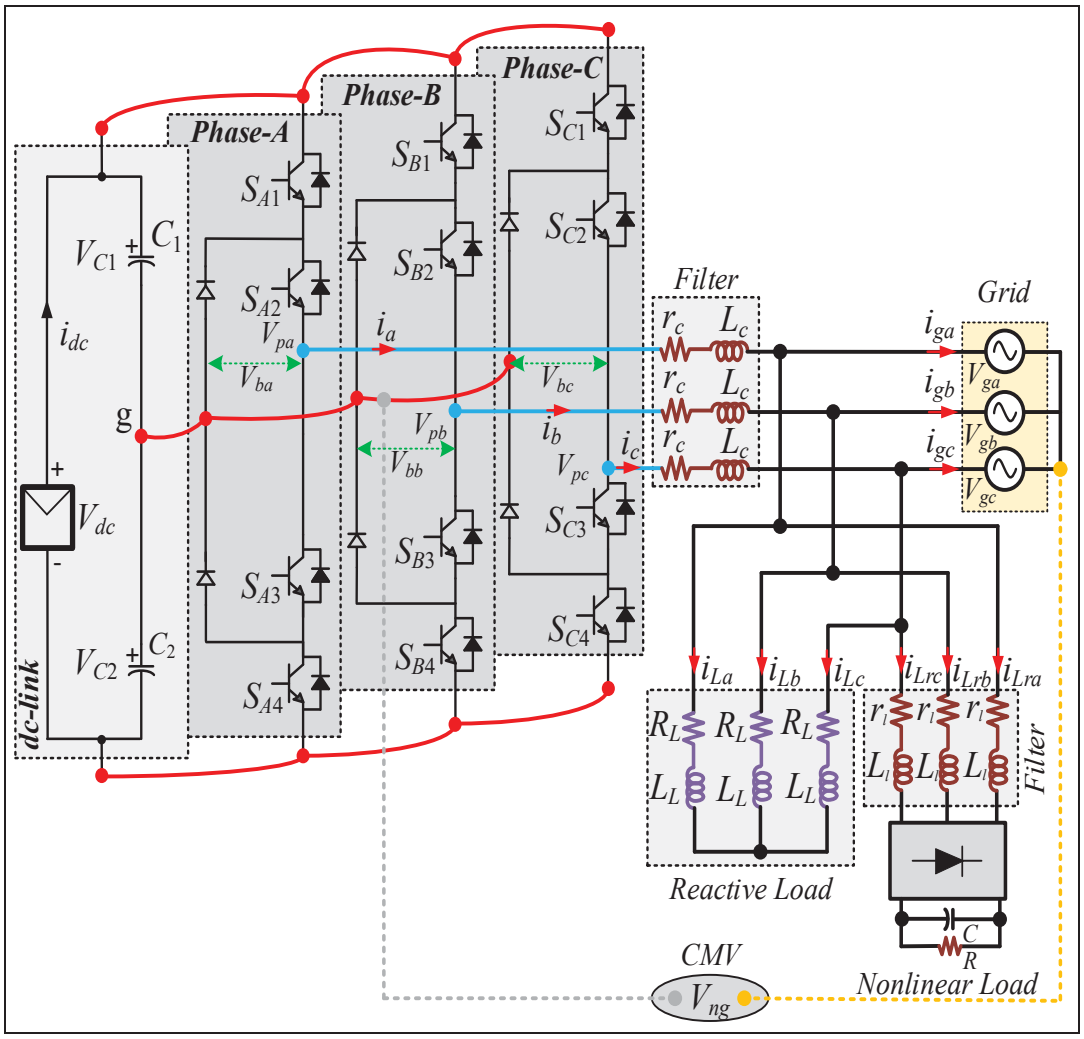

Figure 5.1 Schematic diagram of a three-phase transformerless NPC converter in a power ancillary service mode of operation

Table 5.1 Switching states and voltage levels for the NPC legs ($x \epsilon \{A, B, C\}$)

Voltage Polarity	S_{x1}	S_{x2}	S_{x3}	S_{x4}	V_{out}
+	1	1	0	0	V_{C1}
0	0	1	1	0	0
-	0	0	1	1	V_{C2}

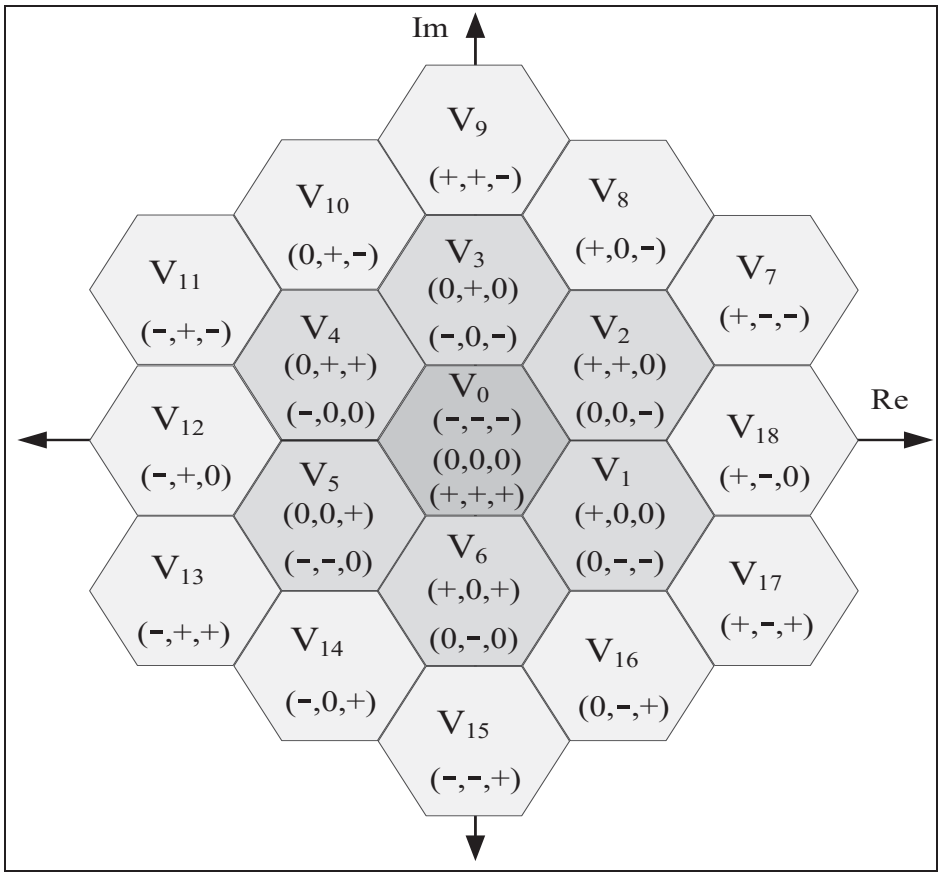

Figure 5.2 Voltage zones including the voltage vectors and switching states for a three-phase NPC converter

5.2.1 Dynamic Model of the Three-Phase Current

The phase currents, including i_a, i_b, and i_c, are formulated using the dynamics of phase voltages. The phase voltages (V_{pa}, V_{pb}, V_{pc}) are expressed as the potential difference between the branch voltages (V_{ba}, V_{bb}, V_{bc}) generated by NPC, the grid voltages (V_{ga}, V_{gb}, V_{gc}), and the voltage of the common-mode node (V_{ng}), as shown by (5.1).

$$\begin{cases} V_{pa} = V_{ba} - V_{ga} - V_{ng} \\ V_{pb} = V_{bb} - V_{gb} - V_{ng} \\ V_{pc} = V_{bc} - V_{gc} - V_{ng} \end{cases} \tag{5.1}$$

Regarding (5.1), the phase currents are modeled in (5.2) by applying Kirchhoff's voltage law from the branch voltages to the neutral point of the grid.

$$\begin{cases} \dfrac{di_a}{dt} = \dfrac{1}{L_c}\left(V_{ba} - r_c i_a - V_{ga} - V_{ng} \right) \\ \dfrac{di_b}{dt} = \dfrac{1}{L_c}\left(V_{bb} - r_c i_b - V_{gb} - V_{ng} \right) \\ \dfrac{di_c}{dt} = \dfrac{1}{L_c}\left(V_{bc} - r_c i_c - V_{gc} - V_{ng} \right) \end{cases} \tag{5.2}$$

where r_c and L_c represent the filter resistance and inductance, respectively. To reduce the IPMOC design complexity, the state-space model of the phase currents is transformed into an $\alpha\beta$-model in (5.3).

$$\frac{di_{\alpha\beta}}{dt} = \frac{1}{L_c}\left(V_{c(\alpha\beta)} - r_c i_{\alpha\beta} - V_{g(\alpha\beta)} \right) \tag{5.3}$$

where $V_c(\alpha\beta)$ as the $\alpha\beta$-based voltage of NPC must be selected from 27 vectors shown by the graphical table in Figure 5.2. $V_g(\alpha\beta)$ and $i(\alpha\beta)$ are also the $\alpha\beta$-model of the grid voltage and the inverter current, respectively.

Equation (5.4) shows the $\alpha\beta$-transform function, which calculates $V_g(\alpha\beta)$ and $i_{\alpha\beta}$ from their corresponding measured values. κ_1=1/3 and κ_2=√3/3 are used as constant factors in the transform function.

$$\begin{cases} V_{g(\alpha)} = \kappa_1 \left(2V_a - V_b - V_c \right) \\ V_{g(\beta)} = \kappa_2 \left(V_b - V_c \right) \end{cases}, \qquad \begin{cases} i_\alpha = \kappa_1 \left(2i_a - i_b - i_c \right) \\ i_\beta = \kappa_2 \left(i_b - i_c \right) \end{cases} \tag{5.4}$$

5.2.2 Dynamic Model of the Common Mode Voltage (CMV)

CMV is molded by applying some modifications to (5.2), as below:

$$V_{ba} + V_{bb} + V_{bc} = L_c \frac{d}{dt}\left(i_a + i_b + i_c \right) + r_c \left(i_a + i_b + i_c \right) + \left(V_{ga} + V_{g_b} + V_{gc} \right) + 3V_{ng} \tag{5.5}$$

In a three-phase balanced system, the summation of the phase voltages, grid voltages, and currents is zero; thus, CMV is calculated using the branch voltages in (5.6).

$$V_{ng} = \frac{V_{ba} + V_{bb} + V_{bc}}{3} \tag{5.6}$$

Since CMV depends on the branch voltages, it can be controlled or eliminated if the controller applies a proper set of voltage vectors to the converter during each switching cycle.

5.2.3 Dynamic Model of the Capacitor Voltages

The dynamic model of the DC link capacitor voltages in a three-phase NPC is defined in (5.7). This equation shows that the capacitors are supplied by the main DC source while the switching operation of the converter and the three currents directly affect their voltages. Thus, the switching operation of the converter should be controlled so that the DC link voltages are stabilized to half of the main source. In (5.7), C is the capacitance of the capacitors; the DC link voltages and currents are defined as V_{C1}, V_{C2}, and i_{C1}, i_{C2}, respectively. i_{dc} is the main DC source current. S_x is a discontinuous variable related to the switching state of the xth leg.

$$\begin{cases} C\ \dfrac{dV_{C_1}}{dt} = i_{dc} - \sum\ S_x i_x \\ C\ \dfrac{dV_{C_2}}{dt} = i_{dc} + \sum\ S_x i_x \end{cases}, \quad x \in \{\ a,\ b,\ c\ \} \tag{5.7}$$

5.2.4 Capacitor Voltage Ripple

Equation (5.7) shows that the capacitor voltages are influenced by the phase currents. The equivalent series resistance (ESR) of the capacitors depends on the harmonic content of the phase currents (Dragičević, & Novak, 2018). ESR increases under the low order harmonics, which leads to voltage ripple and conduction losses. Considering a sinusoidal PWM, the root mean square (rms) of the voltage ripple in a three-phase NPC is calculated in (5.8). Despite the harmonics appearing around the switching frequency, the low-order ones have the most impact on the voltage ripple. e.g., the third harmonic causes the largest fluctuations in the dc voltages.

$$\begin{cases} \Delta V_{C-rms} = \sqrt{\sum_{n=q+1}^{m} \left(\left(\dfrac{I_C^L}{2\pi n f_1 C} \right)^2 + \left(I_C^L \times ESR^n \right)^2 \right) + \left(\dfrac{I_C^H}{2\pi f_{sw} C} \right)^2 + \left(I_C^H \times ESR^{sw} \right)^2} \\ q \in \mathbb{N} \end{cases} \tag{5.8}$$

where f_1, and f_{sw} are the fundamental and the switching frequencies. ESR^n and ESR^{sw} are respectively the equivalent series resistance values of the capacitors caused by the nth low-order harmonic as well as the switching frequency harmonics. $I^L{}_C$ and $I^H{}_C$ respectively defined in (5.9) and (5.10) are the low and high-frequency rms currents of the capacitors.

$$\left(I_C^L \right)^2 = \frac{9M^2 I_m^2}{16\pi^2} \left(\cos^2\ (\ \phi\ ) \left(\frac{\pi}{3} - \sqrt{3} \right) + \frac{2\pi}{3} - \frac{\sqrt{3}}{2} \right) \tag{5.9}$$

$$\left(I_C^H \right)^2 = \frac{3I_m^2 M}{4\pi} \left(\sqrt{3} + \frac{2}{\sqrt{3}} \cos\left(2\phi \right) \right) - \frac{9I_m^2 M^2}{16} \cos^2\left(\phi \right) - \frac{9M^2 I_m^2}{16\pi^2} \left(\cos^2\left(\phi \right) \left(\frac{\pi}{3} - \sqrt{3} \right) + \frac{2\pi}{3} - \frac{\sqrt{3}}{2} \right) \tag{5.10}$$

where M, I_m, and ϕ are respectively the modulation index, the peak amplitude of the current, and the power factor angle. Interested readers are referred to (Gopalakrishnan et al., 2017) to achieve more details.

5.3 Intelligent Predictive Multi-Objective Control

This section describes the proposed IPMOC concept using the dynamic model of the grid-connected system presented in (5.1) to (5.8). Accordingly, a multi-objective MPC is first developed in Section II-A; the SPHM is formulated in Section III-B. The FSTS is then detailed using the first ANN that is devoted to regulating the MPC weighting factors. After that, the APM strategy is designed using the second ANN; the generalized IPMOC is also described in the last subsection.

5.3.1 Multi-Objective Model Predictive Control

Model predictive control is established based on a quadratic cost function, which includes the desired control objectives. The control objectives including the PCC power management, DC link voltage regulation, CMV elimination, switching loss reduction, harmonic mitigation, and voltage stress suppression are formulated using the models discussed in Section 5.2 for the system illustrated in Figure 5.1. Equation (5.11) presents a general formulation of the quadratic cost function, which is required to implement the multi-objective predictive controller.

$$G = \sum_{i=1}^{m} \sigma_i (k+1) g_i^2 (k+1) \tag{5.11}$$

where $\sigma_i(k+1)$ is the weighting factor for the ith objective called $g_i(k+1)$ in the next sampling period; $m=5$ is the number of control objectives. Equation (5.11) shows that the weighting factors dynamically adjust the influence of the objectives on the control loop performance regarding the system condition. Power management based on the dynamic model of the $\alpha\beta$-based currents is obtained in (5.12). Indeed, active and reactive power at PCC is managed through the phase currents.

$$\begin{aligned} g_1(k+1) &= \sigma_1 \left(k+1 \right) \\ &* \left(\left(i_\alpha^*(k+1) - i_\alpha^P(k+1) \right)^2 + \left(i_\beta^*(k+) - i_\beta^P(k+1) \right)^2 \right) \end{aligned} \tag{5.12}$$

where $i_\alpha{}^P(k+1)$ and $i_\beta{}^P(k+1)$ as the real and the imaginary terms of the predicted currents are calculated through (5.13) by applying the forward Euler method to the dynamic model of the phase currents defined in (5.3). $i_\alpha{}^*(k+1)$ and $i_\beta{}^*(k+1)$ are also the components of the complex reference current. The reference current is calculated using the APM in Section 5.3.4.

$$\begin{aligned} i_{\alpha\beta}^P(k+1) &= (1 - \frac{r_c T_s}{L_c}) i_{\alpha\beta}(k) \\ &+ \frac{T_s}{L_c} \left(V_{c(\alpha\beta)}^P(k+1) - V_{g(\alpha\beta)}(k+1) \right) \end{aligned} \tag{5.13}$$

where T_s is the sampling period; $V_g(\alpha\beta)(k+1)$ is the predicted grid voltage, which is assumed to be equal to $V_g(\alpha\beta)(k)$ since the sampling period is much less than the operating frequency of the grid. $V^P{}_c(\alpha\beta)(k+1)$ as the predicted $\alpha\beta$-based voltage of NPC is calculated by applying all the possible voltage and switching vectors respectively presented in Table 5.1 and Figure 5.2 to (5.14) during each sampling period.

$$\begin{cases} V^{P}_{c(\alpha\beta)}(k+1) = S\ (\ i,\ a\ )\ \dfrac{V_{dc}}{2} + \Delta S\ (\ i,\ b\ )\ \dfrac{V_{dc}}{2} + \Delta^2 S\ (\ i,\ c\ )\ \dfrac{V_{dc}}{2} \\ i \in [\ 1,\ 2,\ ...,\ 26,\ 27\ ] \\ \Delta = e^{j\frac{2\pi}{3}} = -\ \dfrac{1}{2} + \mathrm{j}\ \dfrac{\sqrt{3}}{2} \end{cases} \tag{5.14}$$

where $S(i,a)$, $S(i,b)$, and $S(i,c)$ are respectively the switching status of the three phases defined in Table 5.1 as "1", "0", and "-1" with respect to the ith switching vector. V_{dc} is the input DC voltage divided by two using the DC link capacitors. The next objective is defined in (5.15) to regulate the capacitors' voltages. Equation (5.15) shows that the DC voltage regulation is fulfilled through the predicted voltages of the capacitors, without considering a reference.

$$g_2(k+1) = \sigma_2\ (\ k+1\ )\ \left(\ V^{p}_{C_1}(k+1) - V^{p}_{C_2}(k+1)\ \right)^2 \tag{5.15}$$

where $V^{P}_{C1}(k+1)$ and $V^{P}_{C2}(k+1)$ respectively defined in (5.16-a) and (5.16-b) are the predicted voltages of the DC link capacitors.

$$\begin{cases} a)\ \ V^{p}_{C_1}(k+1) = V_{C_1}(k) + \dfrac{1}{C}\ i_{C_1}(k)T_s \\ b)\ \ V^{p}_{C_2}(k+1) = V_{C_2}(k) + \dfrac{1}{C}\ i_{C_2}(k)T_s \end{cases} \tag{5.16}$$

where $i_{C1}(k)$, $i_{C2}(k)$ as the capacitor currents are defined according to the NPC switching states and phase currents as below:

$$\begin{cases} i_{C_1}(k) = i_{dc}(k) - |\ S(i,\ a)\ |\ i_a(k) - |\ S(i,\ a)\ |\ i_b(k) - |\ S(i,\ a)\ |\ i_c(k) \\ i_{C_2}(k) = i_{dc}(k) + |\ S(i,\ a)\ |\ i_a(k) + |\ S(i,\ a)\ |\ i_b(k) + |\ S(i,\ a)\ |\ i_c(k) \\ i \in [\ 1,\ 2,\ ...,\ 26,\ 27\ ] \end{cases} \tag{5.17}$$

CMV elimination as the third objective is formulated in (5.18) based on the mathematical model provided in (5.6).

$$\begin{cases} g_3(k+1) = \sigma_3(k+1)\left(\frac{1}{6}\left(S(i,\ a)V_{dc}+S(i,\ b)V_{dc}+S(i,\ c)V_{dc}\right)\right)^2 \\ i \in [\,1,\ 2,\ ...,\ 26,\ 27\,] \end{cases} \tag{5.18}$$

As the fourth objective, switching transitions are predicted and reduced using (5.19) to mitigate the switching losses of the converter. In (5.19), the switching vectors of each NPC leg in the present and the next sampling instants are compared to select the vector that makes the least switching transitions.

$$\begin{cases} g_4(k+1) = \sigma_4(k+1)\left(\begin{array}{l}\left(S(i,\ a) - S_a(k)\right)^2 + \left(S(i,\ b) - S_b(k)\right)^2 \\ + \left(S(i,\ c) - S_c(k)\right)^2\end{array}\right) \\ i \in [\,1,\ 2,\ ...,\ 26,\ 27\,] \end{cases} \tag{5.19}$$

where $S_a(k)$, $S_b(k)$, and $S_c(k)$ are respectively the present switching states selected in the previous sampling instant for leg-*A*-to-*C*. The fifth control objective is to suppress the voltage stress over the switching components as well as to reduce the computational burden of the cost function. It should be noted this objective is not involved in the cost function; indeed, the fifth objective is defined to adjust the number of switching vectors, which need to be evaluated per sampling instant. In addition, this objective avoids the selection of switching vectors that cause opposite voltage polarity in the upcoming sampling period. Regarding the hexagonal structure proposed for the switching vectors in Figure 5.3, six vectors around the present vector will be nominated for evaluation. Thus, seven switching vectors including the present vector will be evaluated per sampling period instead of 27. Regarding, each hexagonal segment in Figure 5.2 represents seven adjacent vectors that will be evaluated in the next sampling period. The voltage stress over the switches is mitigated by applying the following conditions to the cost function:

$$\begin{cases} S_x(k+1) = 0, & \text{if } S_x(k) = + \;\&\; S_x^P(k+1) = - \\ S_x(k+1) = 0, & \text{if } S_x(k) = - \;\&\; S_x^P(k+1) = + \\ x \in \{ a, b, c \} \end{cases} \tag{5.20}$$

where $S_x(k+1)$ and $S^P{}_x(k+1)$ are respectively the certain and the predicted switching states for the xth leg of the NPC in the next sampling instant.

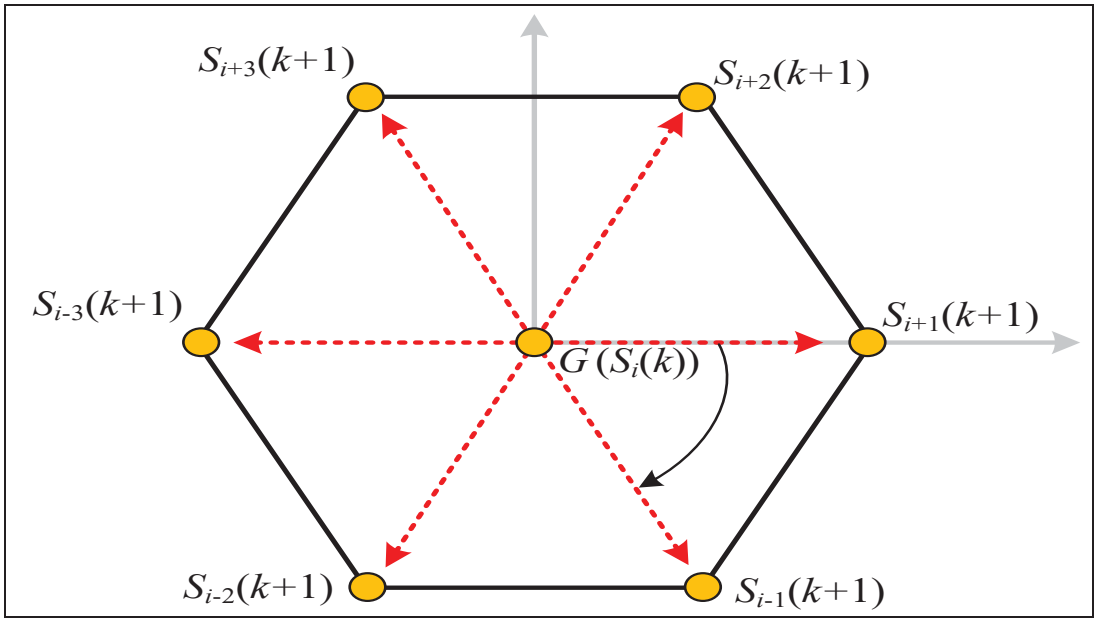

Figure 5.3 Candidate switching vectors in each voltage zone for the next sampling period based on the location of the present vector on the geometrical switching map of the converter shown in Figure 5.2

5.3.2 Real-Time Selective Harmonic Mitigation Objective

The last control objective in the MPC cost function deals with harmonics. The $\alpha\beta$-based, orthogonal band-pass filter shown in (5.21) is used as the primary layer of the proposed SPHM to observe the harmonic profile of the current. In the second layer, a novel predictive harmonic model is developed for grid-tied TMLCs to mitigate selective harmonics without using any FFT algorithm or lookup table. As shown in (5.22), since the harmonic model is predictive, it can be easily integrated into MPC-based algorithms as a control objective to achieve

instantaneous selective harmonic mitigation. Thus, in MPC, selective harmonics are first extracted by the orthogonal filter and then they are injected into the predicted harmonic model to find a switching vector, which mitigates the harmonics.

$$\begin{bmatrix} F_{h_x\alpha}(k) \\ F_{h_x\beta}(k) \end{bmatrix} = \begin{bmatrix} \kappa_1 \ \dfrac{a_{h_x} z - b_{h_x}}{z^2 - c_{h_x} z + d_{h_x}} \ \left(2i_a(k) - i_b(k) - i_c(k) \right) \\ \kappa_2 \ \dfrac{a_{h_x} z - b_{h_x}}{z^2 - c_{h_x} z + d_{h_x}} \ \left(i_b(k) - i_c(k) \right) \end{bmatrix} \tag{5.21}$$

where a_{hx}, b_{hx}, c_{hx}, and d_{hx} are the band-pass filter parameters to be tuned for the xth-order harmonic. Thanks to the orthogonal structure of the band-pass filter, the same tuned parameters can be used for both α and β-axis.

$$SPHM(k+1) = \eta \left(\begin{array}{l} \left| \xi \left(F_{h_3\alpha}(k) + jF_{h_3\beta}(k) \right) + \psi(k+1) \right| \\ + \left| \xi \left(F_{h_5\alpha}(k) + jF_{h_5\beta}(k) \right) + \psi(k+1) \right| \\ +\ldots + \left| \xi \left(F_{h_{2n+1}\alpha}(k) + jF_{h_{2n+1}\beta}(k) \right) + \psi(k+1) \right| \end{array} \right) \Bigg|_{n > 3} \tag{5.22}$$

For TMLCs with an RL filter, ξ and $\psi(k+1)$ are formulated in (5.23). The impact of the SPHM on the MPC cost function is controlled by its weighting factor η; the more this weighting factor increases, the more the harmonics mitigate. Even so, η must be optimized to compromise among the control objectives in the cost function.

$$\begin{cases} \xi = (1 - \dfrac{r_c T_s}{L_c}) \\ \psi(k+1) = \dfrac{T_s}{k_f L_c} \left(V^P_{c(\alpha\beta)}(k+1) - V_{g(\alpha\beta)}(k+1) \right) \end{cases} \tag{5.23}$$

where k_f as a damping factor is used to mitigate the switching spikes which appear in the predicted harmonic. The tuning of k_f is simply started by gradually increasing its value until minimum spikes remain in the predicted waveform of the harmonic. Considering (5.21) to (5.23), the SPHM is a generalizable algorithm for mitigating selective harmonics in any type of MPC algorithm applied to TMLCs with an RL filter.

A customized version of SPHM is defined in (5.24) and (5.25), as the fifth control objective in the cost function to target the third-order harmonic. Since the third-order harmonic increases the voltage ripple of the DC link, its mitigation leads to a major reduction in the volume of the capacitors.

$$g_5(k+1) = \sigma_5(k+1) \left(\begin{array}{l} (1 - \frac{r_c T_s}{L_c}) \left(F_{h_3\alpha}(k) + jF_{h_3\beta}(k) \right) \\ + \frac{T_s}{k_f L_c} \left(V^P_{c(\alpha\beta)}(k+1) - V_{g(\alpha\beta)}(k+1) \right) \end{array} \right)^2 \tag{5.24}$$

$$\begin{bmatrix} F_{h_3\alpha}(k) \\ F_{h_3\beta}(k\ \ ) \end{bmatrix} = \begin{bmatrix} \kappa_1 \ \frac{a_{h_3} z - b_{h_3}}{z^2 - c_{h_3} z + d_{h_3}} \left(2i_a(k) - i_b(k) - i_c(k) \right) \\ \kappa_2 \ \frac{a_{h_3} z - b_{h_x}}{z^2 - c_{h_3} z + d_{h_3}} \left(i_b(k) - i_c(k) \right) \end{bmatrix} \tag{5.25}$$

5.3.3 Fast Self-Training Strategy for ANN: Detailed Design based on the Weighting Factors Tuning Problem of the MPC

An ANN is indeed a composition of weighting factors that connect the inputs to the outputs through activation functions. ANNs can flexibly act as a black-box model, robust controller, or regulator by properly adjusting the activation functions, weighting factors, biases, and the number of inputs/outputs. Thus, the configuration of ANNs is not unique and depends on expert knowledge and design requirements. In this research work, two ANN units are

considered to adapt the MPC weighting factors besides controlling the active and reactive power of the PCC. The first ANN as a regulator is configured with three inputs, five outputs, and 20 neurons in the hidden layer. The inputs measure the tracking errors of CMV, capacitor voltages, and the PCC power while the outputs adapt the weighting factors defined in (5.11). The second ANN as the APM system is constructed using 10 neurons in the hidden layer, two inputs, and two outputs to measure and manage the active and reactive power of the PCC. The number of neurons in each ANN has been determined based on the complexity of the control objectives. Radial basis function (RBF) is the neural network topology, which is considered in this paper to design the ANN regulator and the APM system due to its simple structure and short training process. The proposed ANN-based regulator and the APM system are respectively called radial basis function regulator (RBFR) and radial basis function power manager (RBFPM). The mathematical model related to the RBFR is shown in (5.26).

$$\sigma_i(k+1) = \sum_{h=1}^{m} w_{hi} \left(\sum_{j=1}^{n} \rho_h \left(e_j(k) w_{jh} \right) + \delta_h \right) + \delta_i \tag{5.26}$$

where w_{jh}, w_{hi}, are the weighting factors that connect the jth input signal to the hth neuron in the hidden layer and the hth neuron in the hidden layer to the ith neuron in the output layer, respectively. δ_h and δ_i are the biases for the hth and ith neurons in the hidden and the output layers, respectively. m and n are respectively the maximum numbers of neurons and inputs. The inputs are defined by $e_j(k)$ for the tracking errors of the active and reactive power, CMV, and capacitors' voltages. $\rho_h(.)$ in (5.27) represents the Gaussian activation functions.

$$\rho_h = \exp\left(- \frac{\left(e_j(k) w_{jh} - \tau_h \right)^2}{2\gamma_h^2} \right) \tag{5.27}$$

where τ_h and γ_h are respectively the center and field width of the hth Gaussian function. Equations (5.26) and (5.27) show that w_{jh}, w_{hi}, δ_h, δ_i, τ_h, and γ_h are the parameters that must be

properly adjusted to achieve the desired regulation performance of RBFR on the MPC weighting factors.

Considering the significant number of ANN parameters, using offline training strategies is an exhausting and time-consuming process (Dragičević, & Novak, 2018). Thus, FSTS is proposed in this paper to train the parameters without using any reference model or training data. The FSTS transforms the training problem of ANN into an optimization problem and then evolves the Imperialist Competitive Algorithm (ICA) to optimize the ANN parameters using a proper cost function that measures the control loop performance during the optimization process. ICA benefits from swarm intelligence inspired by imperialism strategies that were used to colonize the countries with the best resources and geographical locations across the globe (Atashpaz-Gargari, & Lucas, 2007, September). The searching strategy of ICA is very effective because, at the same time, several empires independently evaluate the search space to find the global optimum point. Using this unique feature, ICA acts as a virtual multicore processor and accelerates the optimization process so that a commercial computer is able to solve the optimization problem in a short time. Multi-objective structure, short training process, and parallel exploration are the main reasons that ICA has been selected to design the FSTS. In the rest of this subsection, FSTS is described by elaborating on the training steps of RBFR.

According to the ICA instructions, N vectors as countries (numerical vectors with possible optimal values for ANN parameters), with Z elements are defined in (5.28) and then initialized randomly.

$$\begin{cases} P = [\ p_1,\ p_2,\ \ldots,\ p_{N-1},\ p_N\ ] \\ p_i = rand\ (\ min,\ max\ )\ [\ w_{jh},\ w_{hi},\ \delta_h,\ \delta_i,\ \tau_h,\ \gamma_h\ ] \end{cases} \tag{5.28}$$

where *rand* (*min*, *max*) for each type of element is calculated within its maximum and minimum allowable boundaries. In the next step, the primary random values defined by (5.28) are applied to RBFR in a simulator setup like MATLAB, and then, the following cost function in (5.29) is calculated for each country to find the ones with minimum cost. The candidate cost

function should precisely describe the performance of the ANN that is used in the control loop; otherwise, desired performance cannot be achieved. Regarding, the integral time-weighted absolute error (ITAE) is considered the cost function to measure the steady-state error of the main control objectives with high precision during the training process.

$$v_i = \int_{t=0}^{t_m} t \left(e_p(t) + e_{cmv}(t) + e_{VC}(t) \right) dt \tag{5.29}$$

where $e_p(t)$, $e_{cmv}(t)$, and $e_{VC}(t)$ are respectively the tracking errors of the active/reactive power, CMV, and capacitor voltages. v_i and t_m are the cost of the ith country and the time window of the training loop during each iteration of ICA, respectively. In the next step, the countries are sorted based on their costs to select the first M countries as the imperialists (Vectors including the best values for ANN parameters). The imperialists provide the best possible values for the RBFR parameters. Afterward, the rest of the countries are distributed among the imperialists by using (5.30) to generate the empires. Each empire, including an imperialist plus several countries, forms a virtual search engine to find the optimal values for the ANN parameters.

$$\begin{cases} C_n = v_i - \max_{i=1}^{F}(\mathrm{v}_i) \\ H_n = \left| \dfrac{C_n}{\sum_{i=1}^{M} C_i} \right| \end{cases} \tag{5.30}$$

where C_n and H_n are the normalized cost the power of the nth imperialist, respectively. Imperialists with more power will gain more countries as colonies. The distribution of the colonies is randomly performed by (5.31).

$$NC_n = round \left(H_n * N_{col} \right) \tag{5.31}$$

where NC_n is the number of colonies assigned to the nth imperialist and N_{col} is the total number of colonies. After that, colonies make a move toward their imperialists using (5.32) during each iteration.

$$Pc_i = Pc_i + rand(-\vartheta, \vartheta) * rand\left(0, \varepsilon(\left| Pim_n - Pc_i \right|)\right) \tag{5.32}$$

where ϑ is the movement angle, which should be chosen less than $\pi/4$ (rad) (Atashpaz-Gargari, & Lucas, 2007, September). $\varepsilon>1$ is a positive constant; Pim_n and Pc_i are respectively the nth imperialist and its ith colony. During the movements, if a colony reaches a lower cost than the imperialist has, the imperialist moves to the location of the colony and vice versa. After each movement, the total power for each empire is calculated by (5.33-c) based on (5.29) to find the best one. In (5.33), TC_n, NTC_n, and TH_n are respectively the total cost, the normalized total cost, and the total power of the nth empire. After each movement and calculating the total power of the empires, NC_n is updated. Empires with less TH_n will lose their colonies. An empire with zero colonies turns into a colony and is removed from the imperialistic competition.

$$\begin{cases} a)\ TC_n = v_n(pim_n) + k\ \dfrac{\sum_{i=1}^{NC_n} v_i(pc_i)}{NC_n} \\ b)\ NTC_n = TC_n - \max_{n=1}^{F}(TC_n) \\ c)\ TH_n = \dfrac{NTC_n}{\sum_{n=1}^{F} NTC_n} \end{cases} \tag{5.33}$$

The training process of ICA stops if only a single empire remains which means all colonies have similar costs and going toward the best solution. In this paper, the proposed unsupervised training loop including ICA as well as the neural network shown in (5.26) are configured by the parameters defined in Table 5.2 to train the RBFR. The initiation of FSTS can be started

with desired values; if the training fails, then larger values should be selected for initiation in the next round of training.

Table 5.2 Initial parameters for the training loop of the RBFR

Ite.	N	t_m	F	ε	k	ϑ	w_{jh}, w_{hi}	δ_h, δ_i	m	n	τ_h, γ_h
800	100	2s	10	2	0.1	$\pi/6$	[-4 4]	[0 2]	20	3	[-5 5]

5.3.4 Power Management using Intelligent Control

Considering the adverse impacts of reactive loads on the grid, a power management strategy is suggested to be used alongside the main controller (MPC), to regulate the power factor on the grid side of the PCC. To do so, the second RBF unit (RBFPM) is dedicated to fulfilling the power management task through the NPC converter. The RBFPM measures the grid's reactive power and then adjusts the desired reference power of the converter so that the unity power factor is always assured. The active reference power is also controlled based on the available DC power somehow the active power is intelligently distributed among loads and the grid at PCC. Equation (5.34) presents the desired predicted $\alpha\beta$-based references that are used in (5.12) to control the three-phase currents of the converter.

$$\begin{cases} i_{\alpha}^{*}(k+1) = \dfrac{V_{g(\alpha)}(k)P^{*}(k+1) + V_{g(\beta)}(k)Q^{*}(k+1)}{V_{g(\alpha)}^{2}(k) + V_{g(\beta)}^{2}(k)} \\ i_{\beta}^{*}(k+1) = \dfrac{V_{g(\beta)}(k)P^{*}(k+1) - V_{g(\alpha)}(k)Q^{*}(k+1)}{V_{g(\alpha)}^{2}(k) + V_{g(\beta)}^{2}(k)} \end{cases} \tag{5.34}$$

where $P^{*}(k+1)$ and $Q^{*}(k+1)$ are respectively the active and reactive reference powers generated by RBFPM through (4.35):

$$\begin{cases} P^*(k+1) = \sum_{l=1}^{E} w_{lP} \left(\sum_{z=1}^{X} \rho_l \left(sat \left(e_z(k) \right) w_{zl} \right) + \delta_l \right) + \delta_P \\ Q^*(k+1) = \sum_{l=1}^{R} w_{lQ} \left(\sum_{z=1}^{X} \rho_l \left(sat \left(e_z(k) \right) w_{zl} \right) + \delta_l \right) + \delta_Q \end{cases} \tag{5.35}$$

where w_{lP} and w_{lQ} are the weighting factors from the lth neuron in the hidden layer to the outputs assigned to the active and the reactive reference powers, respectively. w_{zl} is the weighting factor from the zth input to the lth neuron in the hidden layer. δ_l is the bias for the lth hidden neuron; δ_P and δ_Q are also the biases for the two output neurons. The two inputs of RBFPM are as below:

$$\begin{cases} e_1(k) = \frac{3}{\sqrt{2}} \left(\left| V_{pa}(k) \right| \left| i_a(k) \right| \cos\left(\varphi_c \right) \right) - P_c \\ e_2(k) = \frac{3}{\sqrt{2}} \left(\left| V_{ga}(k) \right| \left| i_{ga}(k) \right| \sin\left(\varphi_g \right) \right) - Q_g \end{cases} \tag{5.36}$$

where P_c, Q_g=0, φ_c, and φ_g are the desired reference powers, as well as, the phase degrees between the voltages and currents of the converter and the grid, respectively. The active reference power is set according to the maximum available power of the DC source. RBFPM is trained by the proposed FSTS with the same procedure detailed in Section 5.3.3 based on the cost function formulated in (5.37) and the initial parameters defined in Table 5.3. After 500 iterations, RBFPM can realize the APM when the reactive loads are fed through PCC.

$$v = \int_{t=0}^{t_m} t \left(e_1(t) + e_2(t) \right) dt \tag{5.37}$$

Table 5.3 Initial Parameters for the Training Loop of the RBFPM

Ite.	N	t_m	F	ε	k	ϑ	w_{lP}, w_{lQ}, w_{zl}	δ_P, δ_Q, δ_l	m	n	τ_h, γ_h
500	100	0.5s	10	2	0.1	$\pi/6$	[-20 20]	[0 10]	10	2	[-15 15]

Figure 5.4 provides an overview of the nonlinear performance of RBFPM based on e_1 and e_2. Considering the red and green arrows, the saturation functions in (5.35) restrict the power management performance of RBFPM to valid domains.

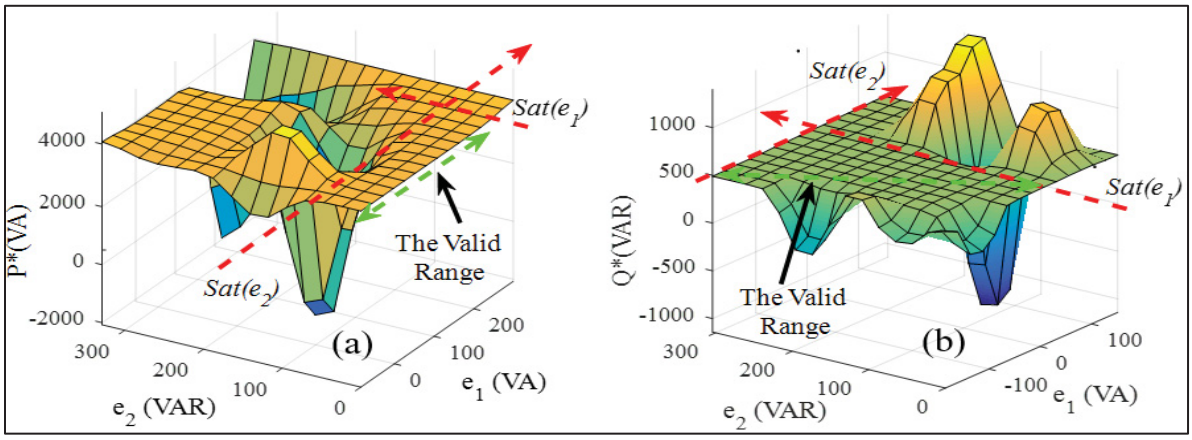

Figure 5.4 Nonlinear performance of RBFPM, (a) in terms of active power (b) in terms of reactive power

Figure 5.5 illustrates the power system including the proposed IPMOC and the training loops. The training process first starts with RBFR including constant reference powers for the MPC, and then, RBFPM is trained in the second step. Finally, the training loops are removed and the control loop, including the MPC, RBFR, and RBFPM, is implemented practically. Notice that the training is realized by means of a simulator setup due to safety reasons.

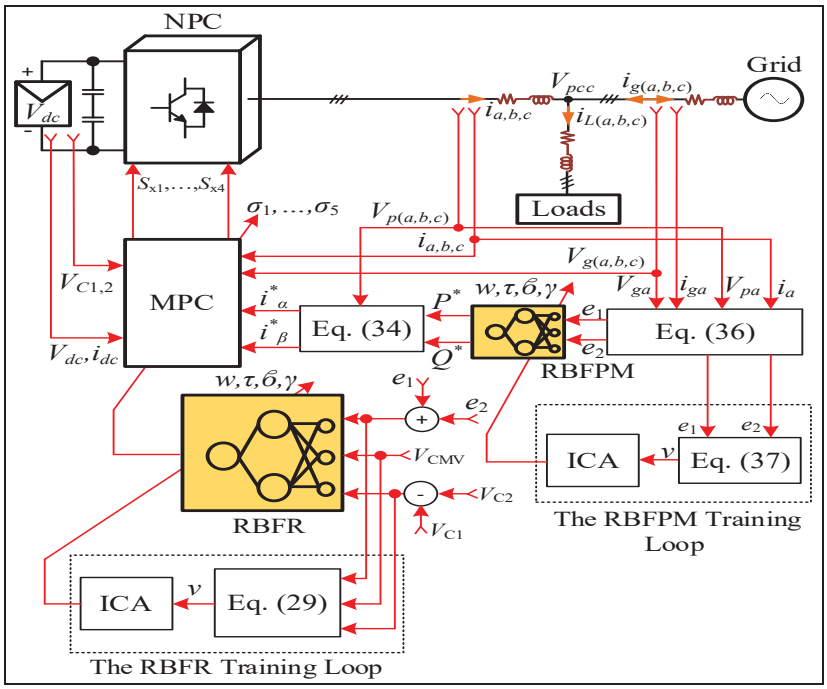

Figure 5.5 Block diagram of the proposed IPMOC including the training loops of RBFR and RBFRPM

5.3.5 Generalized Hybrid Intelligent Predictive Controller

The proposed IPMOC can be customized for TMLCs with different topologies. The IPMOC is a composition of four parts including a conventional MPC, SPHM, ANN, and FSTS, which are designed in order. The MPC term has been already developed for many power converter topologies in various applications. The SPHM can be developed for TMLCs with higher-order filters, such as LC or LCL. Even so, due to the page limits, this will be considered a future work. Therefore, MPC and SPHM as unique parts should be formulated based on the dynamic model of the converter. RBFR and RBFPM need to be properly configured with the right number of neurons, inputs, and outputs respecting the design requirements. Figure 5.6 shows the generalized training flowchart of FSTS which has been also employed in this research work to train RBFR and RBFPM. At the end of iterations, if the FSTS fails to satisfy the objectives, the configuration of ANN and ICA should be modified by revising the number of neurons and the search-space domain, before starting the next training cycle.

5.4 Experimental and Simulation Tests and Results

In this section, the feasibility of the proposed IPMOC shown in Figure 5.5 is assessed using several experimental and simulation test scenarios. Experimentations have been conducted using the setup depicted in Figure 5.7 with initial parameters defined in Table 5.4. OPAL-RT OP-8662, dSPACE-1202, a load bank, and an autotransformer configure the prototype of the grid-tied system. In addition, MATLAB 2021b has been used to run the simulations.

Table 5.4 System parameters used in the experiments and simulations

Input DC voltage (V_{dc})	400 V
Grid phase voltage (V_g)	120V(rms)
Capacitors' capacitance (C_1 & C_2)	470μF
Linear loads	40-80Ω & 10-20mH
Nonlinear load (rectifier with DC load)	40-80Ω, 1000μF
Filters (r_c, L_c, r_l, L_l)	2.5mH, 0.1Ω
Sampling period	35μs
Fundamental frequency	60Hz
Digital filer parameters (a, b, c, d)	(7.53*10-4, 7.53*10-4, 1.997, 0.9992)
Damping factor (k_f)	25

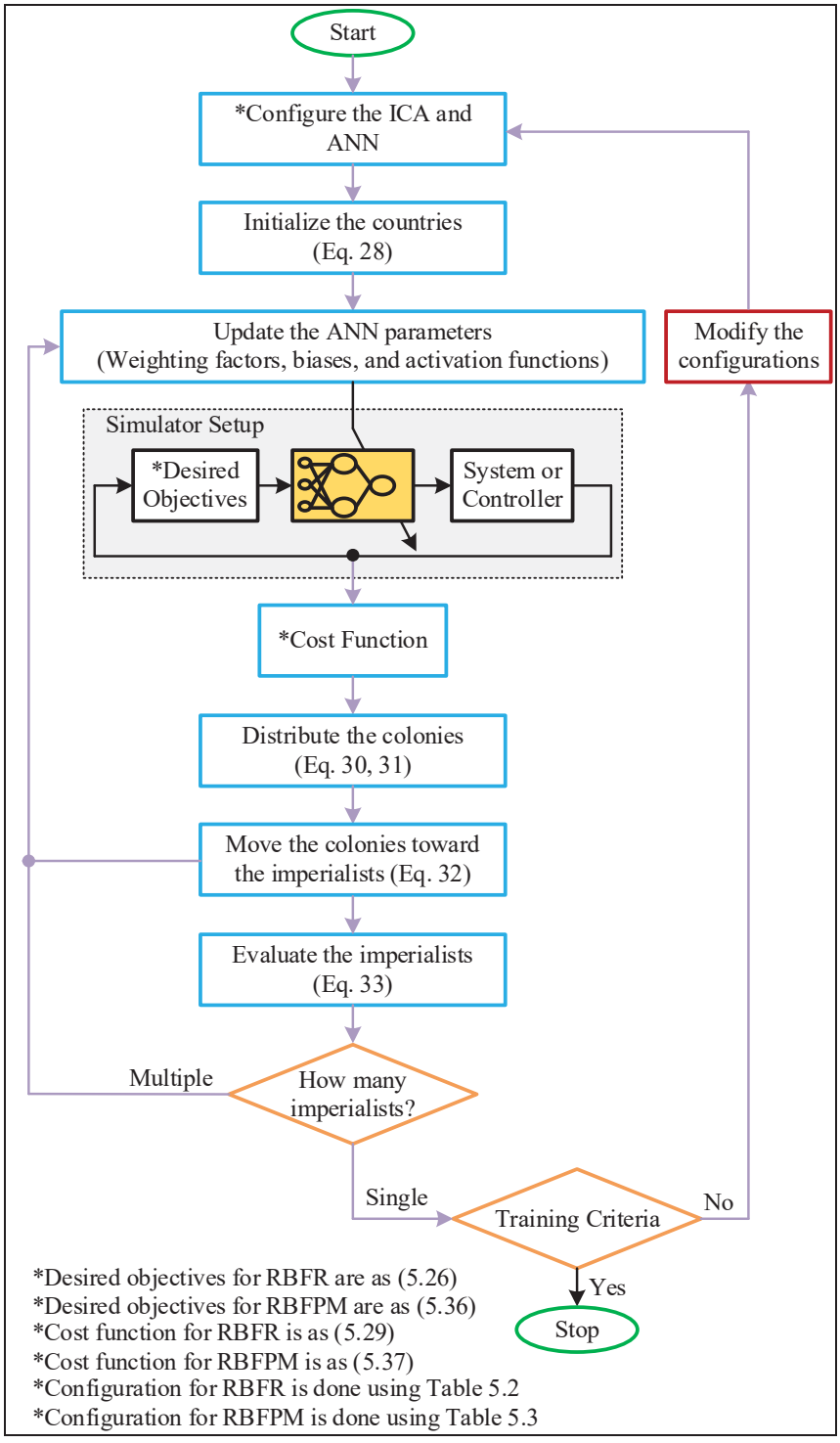

Figure 5.6 Generalized training flowchart of the proposed FSTS

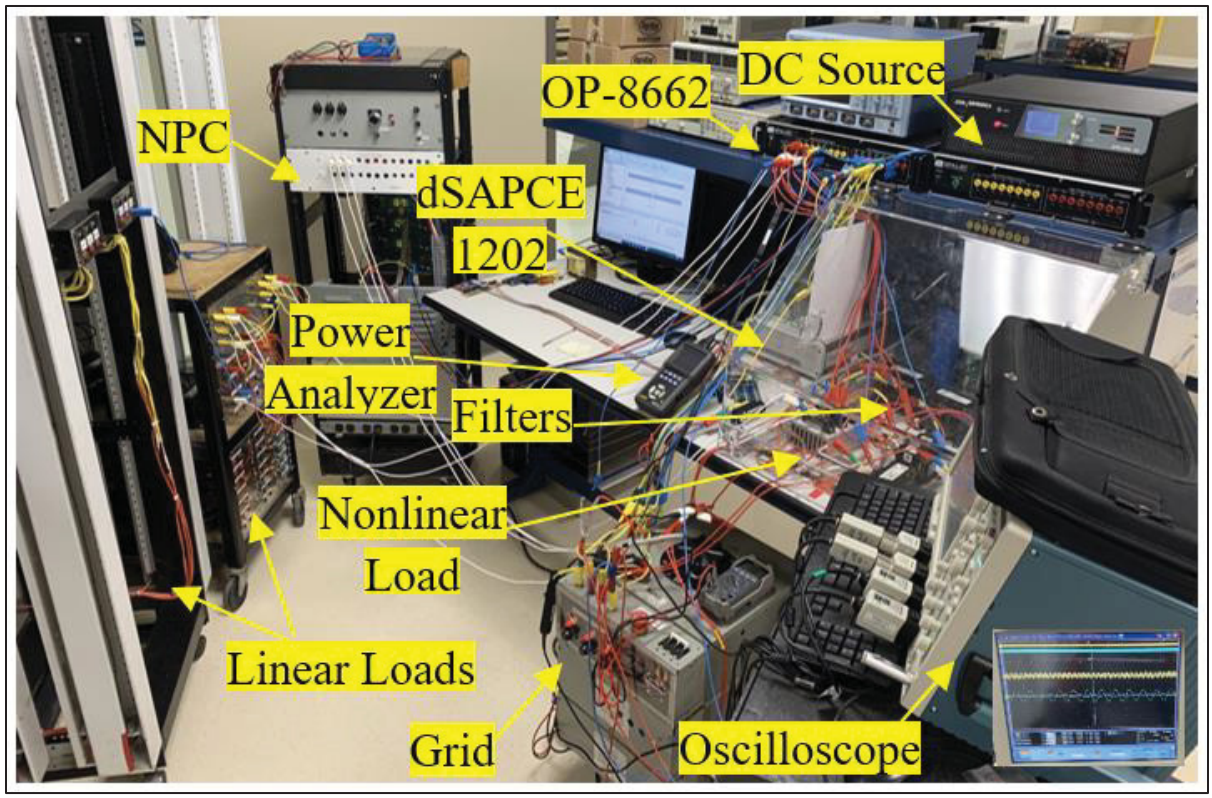

Figure 5.7 Experimental prototype including NPC, linear and nonlinear loads, DS-1202, OP-8662, grid, DC source, oscilloscope, and power analyzer

5.4.1 Switching Control and Dynamic Response

This subsection investigates the impact of the IPMOC on the switching performance and dynamic response of the converter using different experimental and simulation-based test scenarios. The first scenario ignores the reactive and nonlinear loads so that the NPC injects the whole power into the grid. In addition, CMV is not controlled. The corresponding voltage and current waveforms of the system in steady-state conditions are presented in Figure 5.8. The voltage waveforms are related to the line (V_{AB}), branch (V_{ba}), and capacitors ($V_{C1,2}$) of the converter. The 180-degree phase difference between the grid voltage and current represents the power injection from the converter into the grid. The peak amplitude of the grid currents is 11.5A, the reactive power is negligible, and the power factor is unity because the converter is perfectly synchronized with the grid. Considering the spikes that appeared in the CMV

waveform, the amplitude of CMV is about $400V_{p\text{-}p}$, which is large enough to damage the power system.

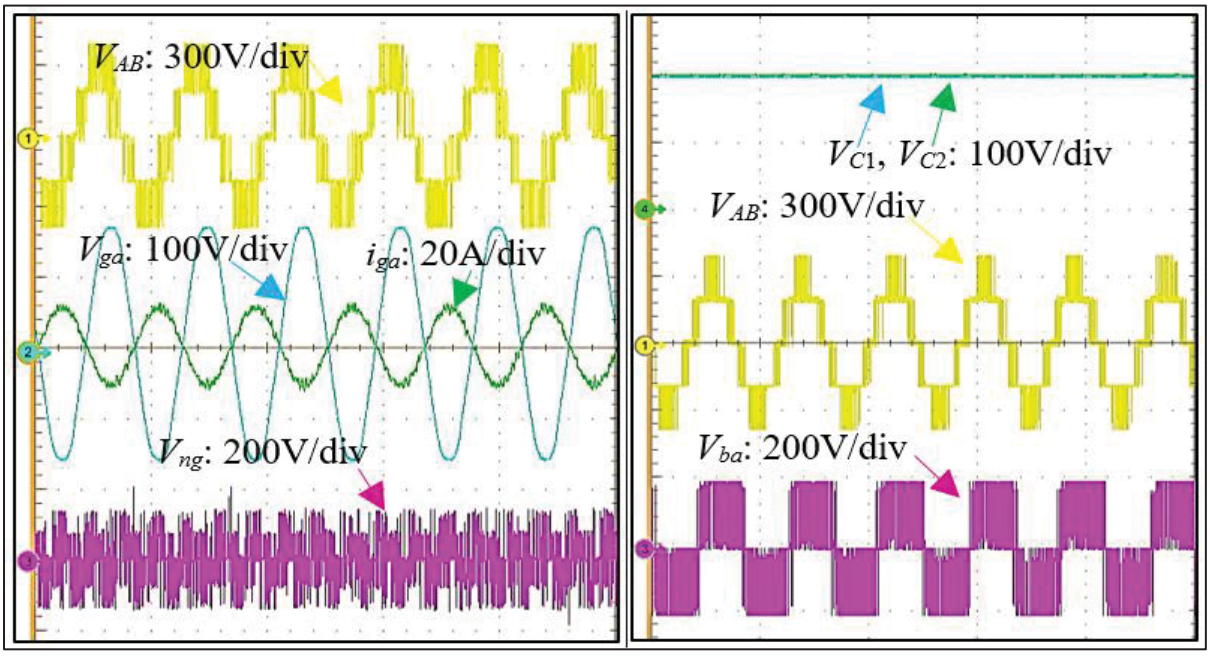

Figure 5.8 Experimental waveforms of the converter and grid, when CMV is not controlled and linear/nonlinear loads are disconnected

The capacitor voltage waveforms however reveal that despite using low-volume capacitors, the voltage ripple is less than 5% because of the third-order harmonic suppression. The switching analysis in Figure 5.9 confirms the constructive impacts of (5.19) and (5.20) on the switching operation of NPC, as the switching frequency and voltage stress are remarkably mitigated. It should be noted the phase voltage (V_{pa}) in Figure 5.9 has nine levels because CMV is not eliminated in this test scenario.

In the second test scenario, the switching frequency mitigation objective is first deactivated and then it becomes effective after a few seconds. The corresponding detailed analysis in Figure 5.10(a) shows a 55% reduction in the switching frequency when (5.19) is activated at t=3(s). This figure also reveals that the switching frequency almost becomes equal in all switching devices when (5.19) is engaged.

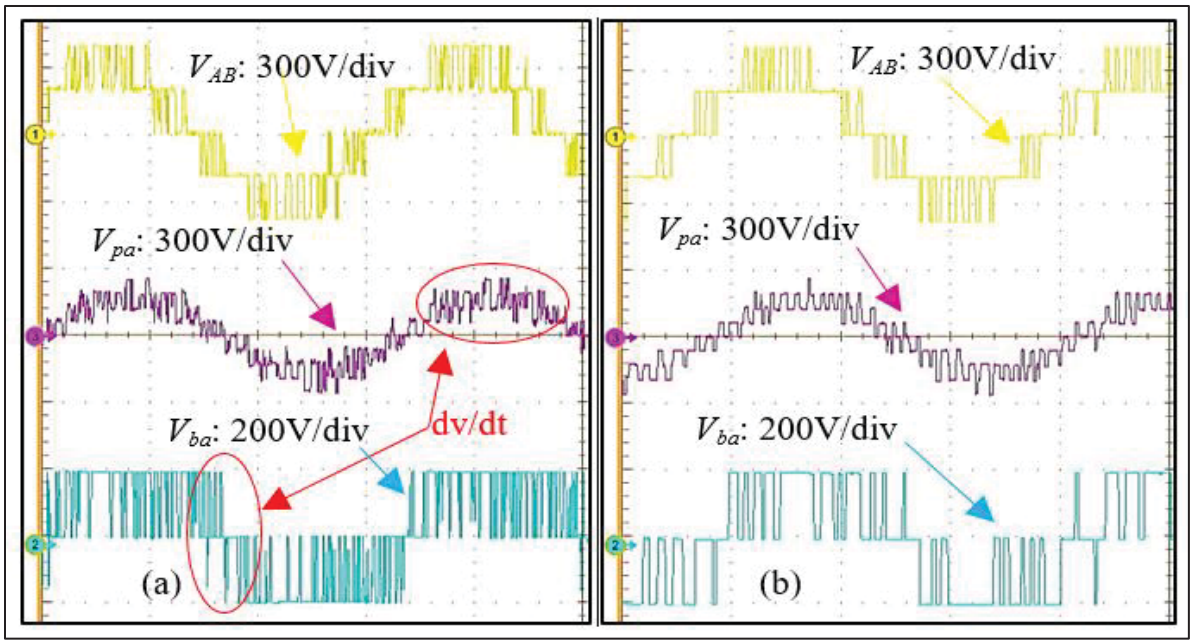

Figure 5.9 The impact of switching frequency and voltage stress on the inverter voltage waveforms (a) without the switching correction (b) with the switching correction

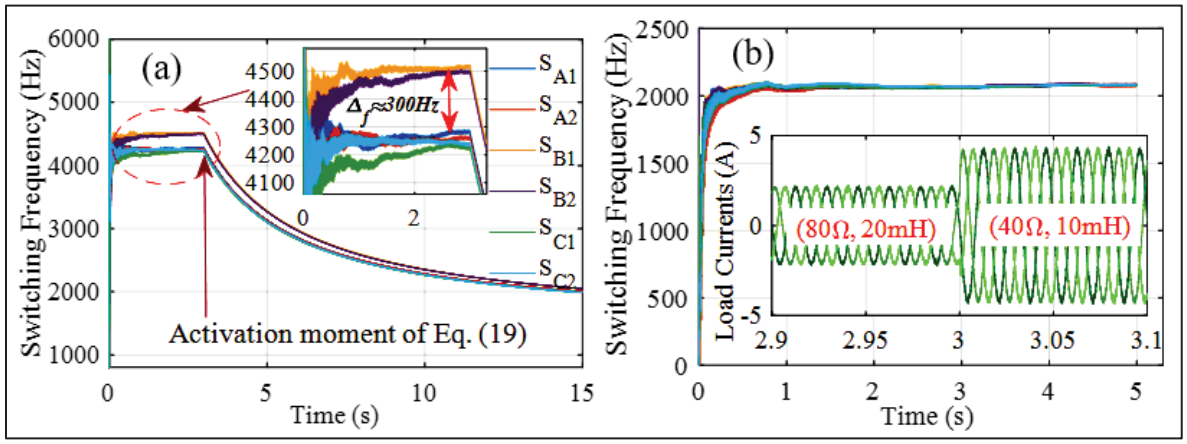

Figure 5.10 Switching analysis of the converter (a) switching frequency minimization at t=3(s) (b) switching frequency variation when the linear load suddenly drops by 50%

The equal switching frequency is important because it simplifies the heat sink design problem for the converter. It must be mentioned that the long transient that appeared in Figure 5.10(a) is not a concern because switching variation is not an option. In the third test scenario, Figure 5.10(b) nearly indicates constant switching frequency in the presence of a reactive load change.

Accordingly, IPMOC limits the switching frequency variations, improves the filtering efficiency, and relieves resonance disorders. Without the switching frequency regulation, harmonics may move to the cutoff frequency region of the filter, which leads to resonance disorders, especially during transient modes.

5.4.2 Power Quality, and Robustness

This subsection provides power quality and robustness-oriented test results for the IPMOC. The results have been collected under different test scenarios. The first and second test scenarios respectively study the adverse impacts of the reactive and nonlinear loads on the grid power quality when the APM is disabled and CMV is not controlled. Figure 5.11(a) shows the voltage and current waveforms of the converter and grid when an unknown linear load is connected to PCC. Figure 5.11(a) shows that the 180-degree phase difference disappeared because NPC is not able to supply the load without the APM assistance. As a cost, the grid power factor is reduced to 0.86. Figure 5.11(b) provides further results when a nonlinear load is also connected to the PCC and the generated power is manually increased to supply the loads and grid concurrently. Figure 5.11(b) shows more power factor degradation besides power distortion in the grid current due to the activity of the loads. The power distortion is however relieved because the third-order harmonic is successfully mitigated by SPHM.

In the third test scenario, the APM is activated when the linear/nonlinear loads are connected to the PCC; compared with Figure 5.11, the experimental results in Figure 5.12(a) and (b) supported by the power analysis in Figure 5.13(a) illustrate that RBFPM intelligently distributes the active and reactive power of the NPC between the loads and grid so that the unity power factor of the grid is maintained.

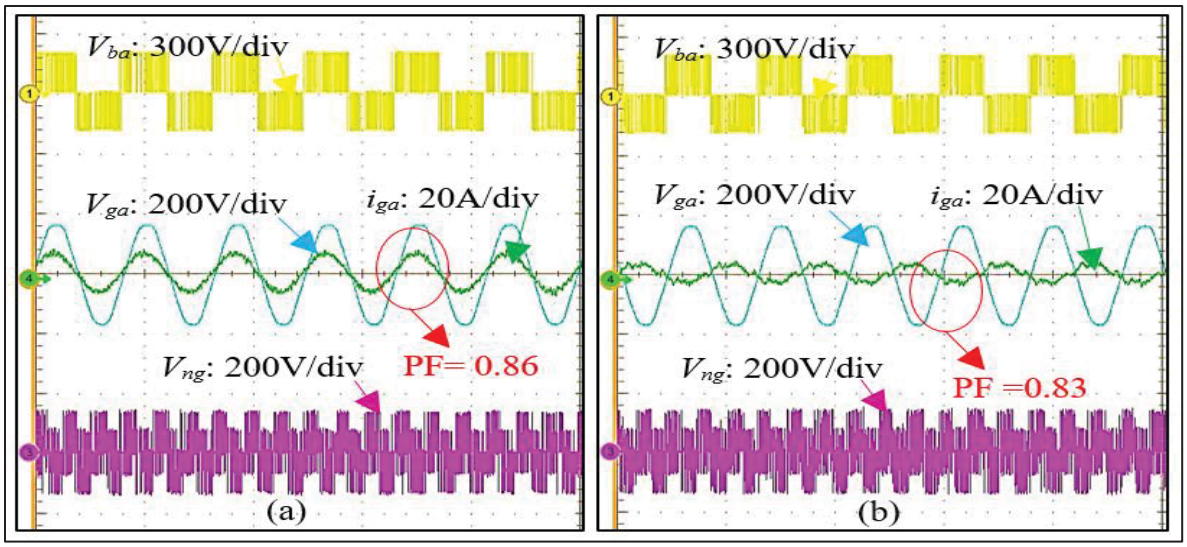

Figure 5.11 Experimental results of the inverter and grid waveforms while CMV elimination and power management are deactivated (a) the effects of the linear load (b) the effects of the linear and nonlinear loads

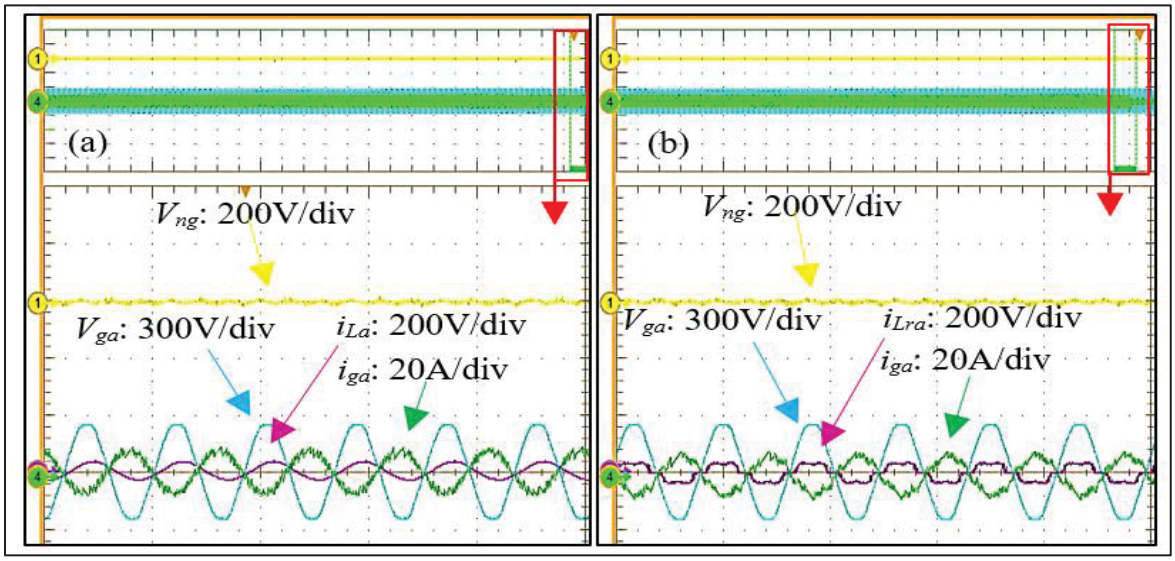

Figure 5.12 Power management performance of the IPMOC (a) in the presence of the linear (i_{La}) load (b) in the presence of linear and nonlinear (i_{Lra}) loads

The robustness analysis in Figure 5.13 (b) also proves that the parametric uncertainties and dynamic operation cause minimum effects on the control performance of the IPMOC because RBFR properly adapts the weighting factors to track the objectives.

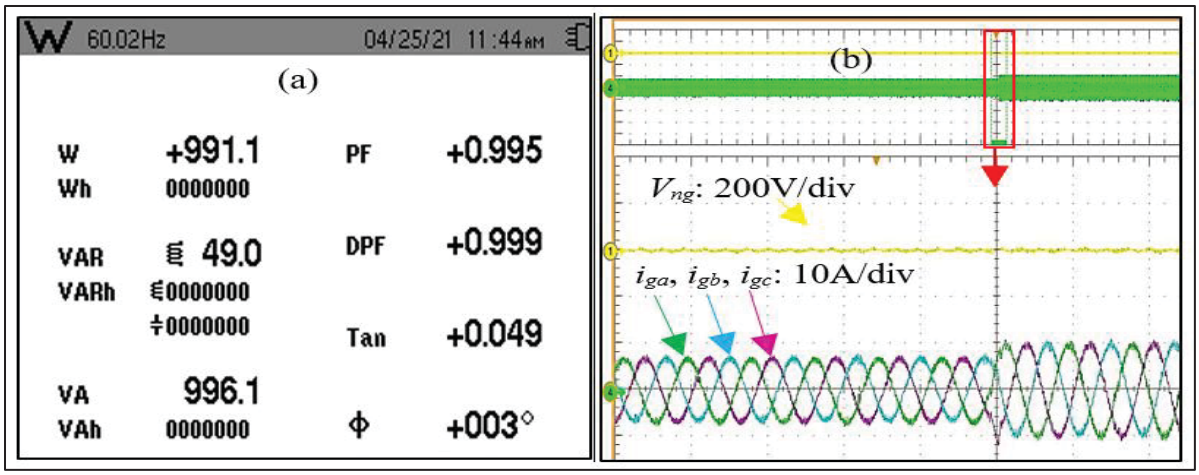

Figure 5.13 (a) Power analysis for the first phase of the grid when the linear and nonlinear loads are supplied through the PCC (b) robustness analysis of the IPMOC when a 100% mismatch has been applied to the filters and the active power suddenly increased by 20%

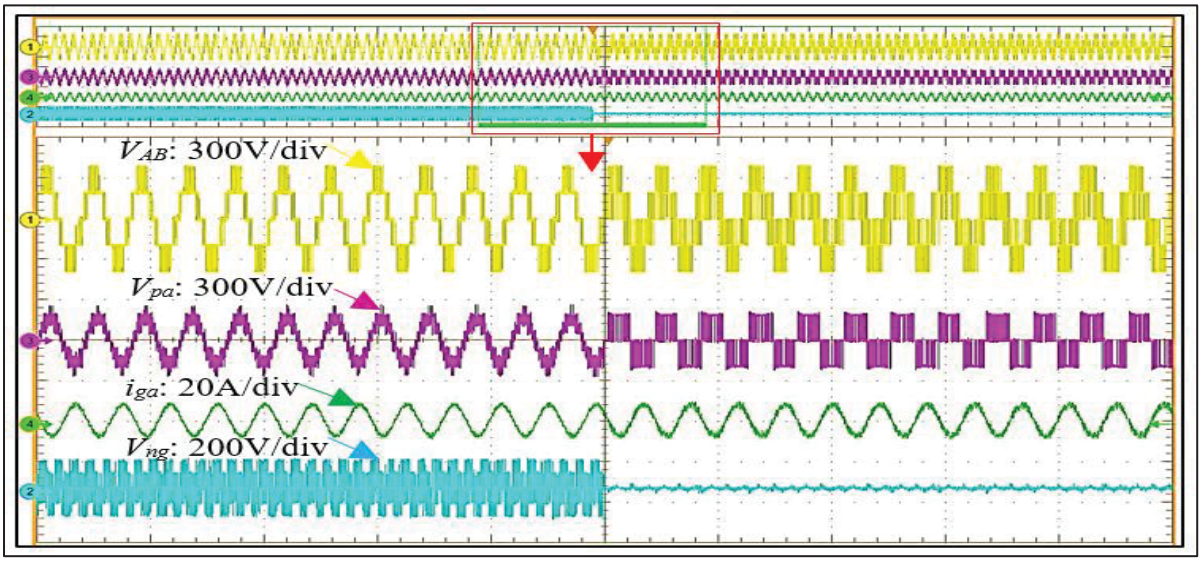

Figure 5.14 Implementation results of the inverter voltages, CMV, and the grid current when CMV is suddenly suppressed

The next scenario verifies the CMV elimination capability of the IPMOC and studies the impact of CMV elimination on the power quality. Regarding, Figure 5.14 provides the voltage and current waveforms of the system when CMV is suddenly suppressed. As an adverse consequence, the power quality of the grid current is attenuated because the number of levels in the phase voltage is reduced to three. However, Figure 5.15 depicts that the quality reduction

is not a concern as the grid current THD is still less than 5%. Thus, the IPMOC is able to eliminate CMV with minimum negative impacts on the power quality.

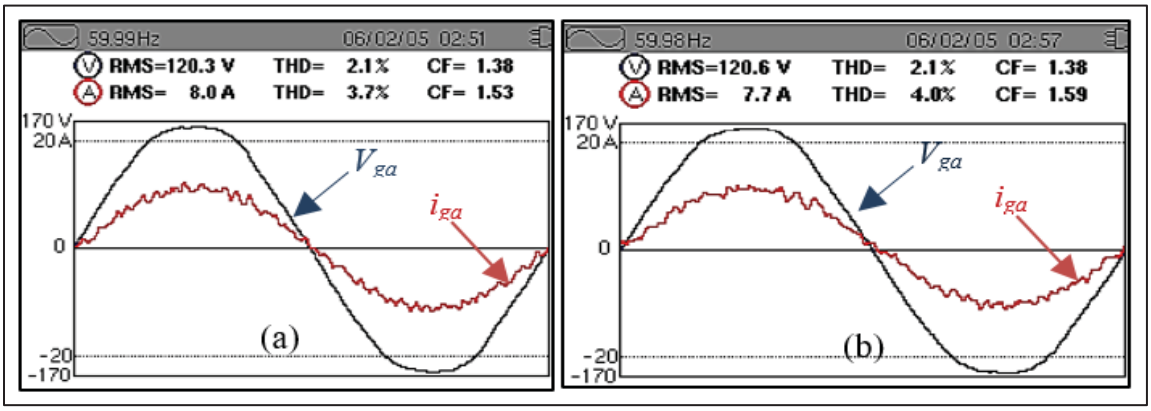

Figure 5.15 THD analysis of the grid voltage and current (a) before CMV suppression (b) after CMV suppression

5.4.3 Selective Harmonic Mitigation

The last test scenario explores the generalization capability of the real-time SPHM through harmonic analysis of the phase current. Figure 5.16 (a) illustrates the harmonic mitigation performance of SPHM by different colored bins respectively labeled as SPHM-3rd, SPHM-3rd, SPHM-5th, SPHM-7th, SPHM-9th, and SPHM-11th for low-order harmonics including 3rd, 5th, 7th, 9th, and 11th. The red bins (labeled as Normal-1st) also represent the same harmonic orders when SPHM is not involved. As shown in Figure 5.16(a), the red bins with the largest amplitudes cause the worst THD while the others significantly mitigate the targeted harmonics. e.g., SPHM-3rd mitigates the third-order harmonic by 80% and improves the THD level by 15%. From Figure 5.16(a) it can be also concluded that SPHM indirectly affects the other harmonic orders besides the targeted ones; for instance, SPHM-7th mitigates the 3rd, 5th, and 11th besides a 79% reduction of the 7th while it intensifies the even-order components. Fortunately, the adverse impact of SPHM on the other harmonics is negligible. Figure 5.16(b) indicates the THD analysis for the first phase current of NPC when SPHM with all the low-order harmonics (SPHM-All) is considered in the IPMOC. Figure 5.16(b) then compares the corresponding results of SPHM-All with the Normal-1st. The results in Figure 5.16(b) show

that involving all the low-order harmonics in the IPMOC leads to a 31% THD reduction for the phase current. This harmonic mitigation capability leads to a significant reduction in the size of the DC link capacitors as well.

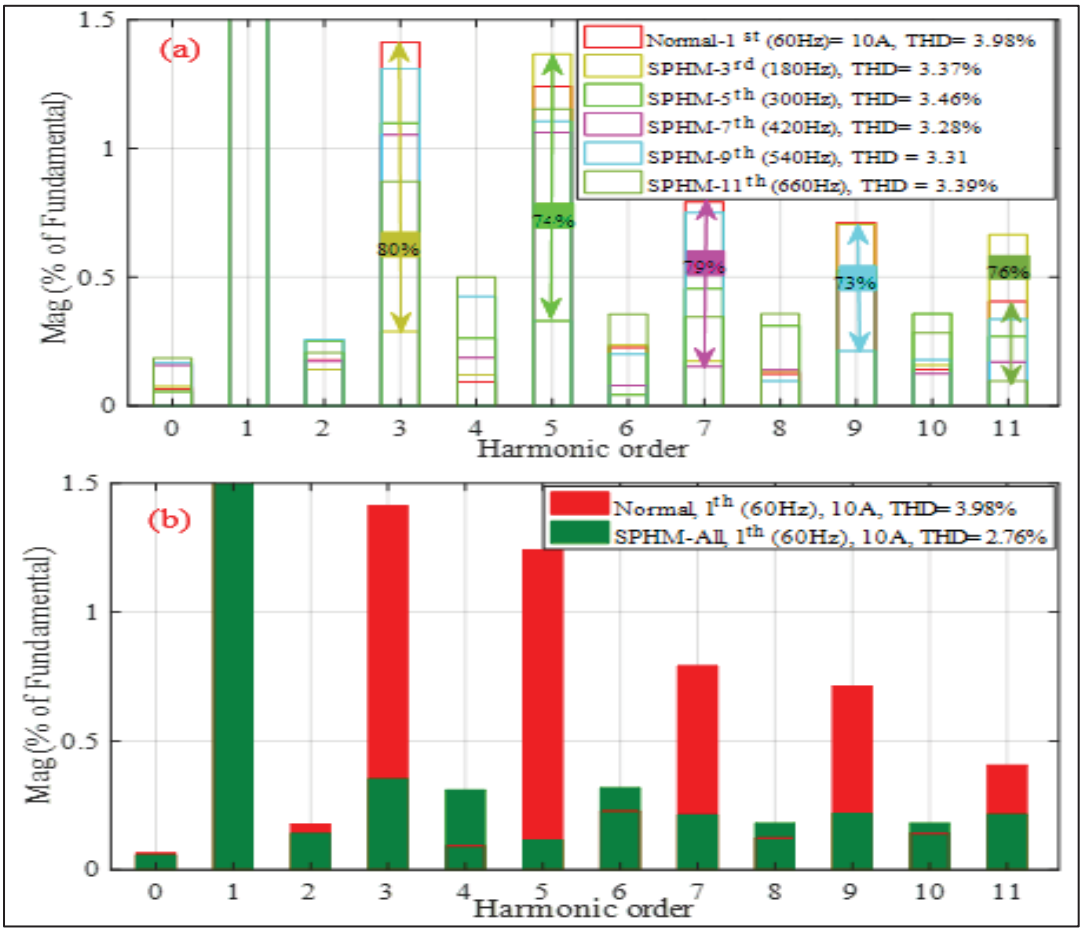

Figure 5.16 Harmonic mitigation performance of SPHM for the first five, odd, components of i_a (a) individual mitigation results (b) group mitigation results

5.4.4 Comparison

Thanks to the FSTS, APM, and SPHM, the proposed IPMOC technique shows a promising performance, which can be compared with the other MPC-based multi-objective techniques applied to the NPC converter. Regarding, a hybrid quantitative/linguistic comparison between the proposed IPMOC algorithm and the other similar controllers is provided in Table 5.5. The

compared control algorithms are CMPC (Kakosimos, & Abu-Ru, 2017)], CEMPC (Yang et al., 2020), DVMPC (Liu, Chen, Qin, Chen, & Li, 2020), FPMPC (Xing, & Chen, 2019), FAMPC (Rojas, Aguirre, Kouro, Geyer, & Gutierrez, 2017), SLMPC (Babaie, Sharifzadeh, Mehrasa, Chouinard, & Al-Haddad, 2020), ANN-MPC (Machado, Martín, Rodríguez, & Bueno, 2017), SSMPC (Chowdhury et al., 2021), DDMPC (Wu, Qiu, Liu, Guo, Rodriguez, Ma, & Fang, 2022), and FFSMPC (Silva et al., 2020). The comparison criteria are the size of the capacitors (C), the size of the filter inductor (L_c), THD, CMV, voltage stress (dv/dt), power factor (PF), harmonic mitigation (HM) capability, voltage ripple (VR) suppression capability, switching frequency (SF) regulation, and sampling time (T_s). From this comparison, it can be concluded that the best trade-off is offered by the proposed IPMOC, while more objectives are simultaneously controlled.

5.5 Conclusion

Although there is a computational burden, implementation results in this paper confirmed that FSTS, APM, and SPHM as the main contributions of this paper can optimally enhance the multi-objective control performance of the IPMOC and consolidate the key role of TMLCs in the future of grid-tied renewable energy-based systems. Moreover, FSTS as a data-free training technique will improve the contribution of ANNs to designing robust, model-free multi-objective controllers in power electronic applications. The AMP demonstrates that TMCLs empowered by ANNs can independently provide smart power management, which is ideal to simplify centralized power management systems and enhance cybersecurity in smart grids. SPHM as a generalized control objective can be used in MPC-based techniques to mitigate selective harmonics for TMLCs with RL filter. The proposed IPMOC operates with a stable switching frequency, improves the grid power quality, and mitigates the switching losses even though a simple RL filter is employed. Nonetheless, the fixed switching frequency may not be guaranteed in all circumstances and needs further development which is beyond the scope of this paper. Thus, the future work is to achieve a fixed switching frequency and develop the SPHM for grid-tied TMLCs with higher-order filters.

Table 5.5 Comparison of the proposed IPMOC with other multi-objective controllers

Control	***C***	L_c	***THD***	***CMV***	**d*v*/d*t***
CMPC	2200μF	5.85mH	1.81%	Mitigated	NI
CEMPC	500μF	5mH	3.45%	Mitigated	NI
DVMPC	3760μF	5mH	3.69%	Mitigated	NI
FPMPC	3760μF	10mH	3.63%	Mitigated	NI
FAMPC	3900μF	3mH	4.98%	Mitigated	Mitigated
SLMPC	650μF	20mH	1.6%	Eliminated	NI
ANN-MPC	2000μF	1mH	9.48%	Eliminated	NI
SSMPC	2000μF	5mH	2.7%	NI	NI
DDMPC	2700μF	7mH	3.23%	NI	NI
FFSMPC	9400μF	15mH	1.6%	NI	Mitigated
IPMOC	470μF	2.5mH	3.7%	Eliminated	Mitigated
Control	***PF***	***HM***	***VR***	***SF***	T_s
CMPC	NI	NI	NI	NI	20μs
CEMPC	NI	NI	Mitigated	Regulated	50μs
DVMPC	NI	NI	Mitigated	NI	100μs
FPMPC	NI	NI	NI	NI	100μs
FAMPC	NI	NI	NI	Regulated	32μs
SLMPC	NI	NI	NI	NI	20μs
ANN-MPC	NI	NI	Mitigated	Regulated	100μs
SSMPC	NI	NI	NI	Regulated	50μs
DDMPC	NI	NI	NI	Regulated	100μs
FFSMPC	NI	NI	Mitigated	Regulated	100μs
IPMOC	Regulated	Regulated	Mitigated	Regulated	35μs

CHAPTER 6

Boost Packed E-Cell: A Compact Multilevel Converter for Power Quality Ancillary Services

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Abstract

This paper presents boost packed E-cell (BPEC) as an affordable compact multilevel converter (CMLC) for power quality ancillary services. BPEC is a transformerless bidirectional CMLC topology and can generate symmetrical and asymmetrical multilevel voltage waveforms with 5-to-11-level resolution using only three low-voltage DC capacitors and eight power switches. Thanks to the serial expansion of the two DC capacitors, BPEC has two DC links, which means two voltage sensors are enough to control three DC capacitors. Despite other CMLCs, BPEC does not need a fault detector and inherently generates a symmetrical 5-level or an asymmetrical 7-level voltage waveform in the event of a fault of the middle switches. As a case study, a single-phase compact active power filter (CAPF) is designed in this paper based on the BPEC to compensate for harmonics and reactive power caused by unknown non/linear loads, simultaneously. Finite control set predictive control strategy is also adopted based on the switched model of the power system containing the grid, unknown non/linear loads, and the BPEC to address the grid power quality concerns. The experiments performed by a prototype, including the BPEC power board, MicroLabBox, OPAL-RT OP8662, and Chroma 61086 verify the merits of the proposed CAPF in practice.

6.1 Introduction

In light of rapid growth and massive penetration of renewable energy sources, electric vehicles, and non/linear loads, maintaining the power quality has become a priority for grids and smart grids (Nejabatkhah, Li, & Tian, 2019; Khadkikar, Xu, & Cecati, 2017). Thus, power quality ancillary services (PQAS) have been approved and recognized as essential services for the grid. The PQASs are mainly provided through flexible AC transmission systems (FACTS), reactive power banks, advanced passive filters, and active power filters (APF) for voltage regulation, reactive power compensation, and harmonic mitigation at the point of common coupling (PCC) of the grid, renewable energy sources, and non/linear loads (Jiang, Guo, Sun, & Ge, 2021; Knezović, Martinenas, Andersen, Zecchino, & Marinelli, 2016; Arya et al., 2015; Sinvula, Abo-Al-Ez, & Kahn, 2019; Ku et al., 2020). Nowadays, power electronics converters supplied by active or passive sources provide the majority of the PQASs because of their superiority over the reactive power banks and passive filters in terms of flexibility, controllability, efficiency, costs, and dynamic response (Tanaka, Ma, Wang, & Blaabjerg, 2018; Pires, Cordeiro, Foito, & Silva, 2021; Mortezaei et al., 2018). The state of the art demonstrates that the PQASs have been mainly supported using classic two-level converters due to controllability and reliability concerns. Nonetheless, the switches in two-level converters experience a significant level of voltage stress and switching loss since high levels of voltage and switching frequency are required to reduce the size of the AC-side filter and dominate the grid voltage at the PCC (Wang, Lam, & Wong, 2016; Amerise et al., 2020; da Silva Fischer et al., 2018; Badoni et al., 2018; Salem et al., 2020; Gnanasambandam et al., 2016). The high voltage amplitude of the converter also increases the size and cost of the system, as a bulky DC source or capacitor is required. Instead, a coupling transformer can be used to reduce the voltage amplitude of the converter and voltage stress of the power switches simultaneously; even so, the transformer increases the cost and volume of the system (Geng et al., 2019; Ferreira et al., 2017; Chilipi, Al Sayari, & Alsawalhi, 2019; Babu, & Fernandes, 2014; Alfaris, & Bhattacharya, 2017, October).

The literature shows that multilevel converters (MLC) like modular multilevel converters (Ota, Shibano, Niimura, & Akagi, 2014; Behrouzian, Bongiorno, Svensson, & Mohanaveeramani, 2021), cascaded H-bridge (CHB) (Wang, & Liu, 2019), delta CHB (Su, & Cheng, 202), and neutral point clamped (NPC) (Zhou, & Cheng, 2019) dominate the two-level opponents for PQASs thanks to generating a multilevel voltage on the AC-side that remarkably helps to reduce the DC-link voltages, AC-side filter, THD, voltage stress, and switching frequency. However, enhancing the resolution of the multilevel voltage needs more switches and floating DC capacitors, which adversely influences MLCs in terms of controllability, costs, reliability, and stability (Salem et al., 2020; Trabelsi, Vahedi, & Abu-Rub, 2021).

Compact Multilevel Converters (CMLC), such as switched-capacitor CHB (Jahan, Abapour, & Zare, 2018), packed U-cell (PUC) (Babaie, Sharifzadeh, Kanaan, & Al-Haddad, 2020; Babaie, Sharifzadeh, & Al-Haddad, 2019, October), 11-level DC-DC-based buck converter (Sotoodeh, & Miller, 2013), 11-level modified H-bridge (Cahyosaputro, & Heru, 2018, September), compact module multilevel converter (Lee, Sidorov, Idris, & Heng, 2017), and packed E-cell (PEC) (Sharifzadeh, & Al-Haddad, 2019) compromise between the multilevel voltage resolution and the components count. e.g., PUC as a generalized CMLC can be configured using six switches and two DC capacitors to generate a multilevel waveform with a 5-to-7-level voltage resolution. PUC can be also modified to generate a nine-level voltage waveform; however, the voltage regulation problem is intensified, as three floating capacitors are required in this case (Babaie, Sharifzadeh, & Al-Haddad, 2019, October). As another example, PEC optimally generates a 9-level voltage waveform by eight switching devices and two capacitors.

The new generations of CMLCs, including modified packed U-cell (MPUC) (Babaie, Mehrasa, Sharifzadeh, & Al-Haddad, 2021), switched capacitors 5level (Saeedian, Hosseini, & Adabi, 2018), 7L (Siddique et al., 2020), 9L (Jahan, Abapour, & Zare, 2018; Barzegarkhoo et al., 2017), and 11L (Priyadarshi, Kar, & Karanki, 2020; Lee, Lim, & Lee, 2019; Sharifzadeh, Ahmadijokani, Mehrasa, Sadabadi, & Al-Haddad, 2021, October), can boost the AC side voltage using lower voltage DC-links that result in reducing the size of the DC link capacitors,

suppressing the voltage stress, and eliminating the coupling transformer. Regarding this fact, boost CMLCs (BCMLCs) are the future power electronics converters that provide PQASs for high-power medium voltage applications. MPUC as one of the most optimal BCMLCs has been successfully utilized as a shunt APF (Vahedi, Shojaei, Dessaint, & Al-Haddad, 2017), electric spring (Kaymanesh, & Chandra, 2020), and static synchronous compensator (Kaymanesh, Chandra, & Al-Haddad, 2021b). Regarding the boost capability of MPUC and the unique features of the PEC like the equivalent voltage balancing, fault tolerance, and voltage level switching mode (Sebaaly, Sharifzadeh, Kanaan, & Al-Haddad, 2020), this paper contributes to introducing boost packed E-cell (BPEC) as a new single-phase BCMLC topology for PQASs.

The proposed BPEC is able to dominate the PCC voltage using two lower voltage floating capacitors and eight power switches without involving a coupling transformer. The single-phase BPEC generates a symmetrical 11-level voltage waveform using eight power switches and three capacitors in two DC links. Two capacitors in BPEC are connected in series and form the second DC link so that only a single voltage sensor is required to measure the equal voltage of the capacitors. This unique structural feature of BPEC mitigates the implementation costs, enhances the reliability of the converter, and simplifies the control loop design problem. In addition, BPEC does not need a fault detector and automatically changes the voltage levels from 11-level to an asymmetrical 7-level if any fault occurs in the power switches connected to the middle point of the second DC link. As a result, BPEC is competitive in the voltage levels resolution, size, fault-tolerance, components count, controllability, and reliability, compared with the other BCMLCs, like MPUC, PEC, and switched capacitors topologies (Priyadarshi, Kar, & Karanki, 2020; Lee, Lim, & Lee, 2019; Sharifzadeh, Ahmadijokani, Mehrasa, Sadabadi, & Al-Haddad, 2021, October; Vahedi, Shojaei, Dessaint, & Al-Haddad, 2017) for PQASs.

As a case study, the proposed BPEC is used to design a hybrid Compact APF (CAPF) (Ferreira et al., 2017; Babaie, & Al-Haddad, 2022, January) for harmonic elimination and reactive power compensation at the PCC where several unknown linear and nonlinear loads severely affect

the grid power quality. The finite control set model predictive controller (MPC) is also formulated according to the dynamic model of the power system to ensure the effectiveness of the CAPF and the grid power quality in stable and unstable conditions. Two supplementary objectives are also considered in the MPC to minimize the voltage stress and regulate the switching frequency. The weighting factors of MPC are also continuously adjusted through a set of simple error-based functions. Thanks to the optimal structure of the BPEC and the digital equations of the MPC, the control loop can be easily implemented using commercial digital hardware. A prototype containing the power board of BPEC as CAPF, MicroLabBox as the control hardware, OPAL-RT OP8662 as V/I measurements, Chroma 61086 as the grid emulator, and several reactive and nonlinear loads has been provided to verify the feasibility and effectiveness of the proposed boost compact topology for power quality ancillary services. Given the state of the art of the CMLCs and their compatibility with PQASs, the major contributions of this paper can be sorted below:

- BPEC is proposed and precisely detailed in terms of switching performance, modeling, control, fault tolerance, and practical implementation.

- Following the detailed instructions provided in this paper, BPEC is theoretically and practically developed for PQASs, especially for hybrid transformerless compact active power filters.

In the following, Section 6.2 details the proposed BPEC topology, Section 6.3 presents the case study and the corresponding MPC controller, Section 6.4 provides the implementation results, and Section 6.5 concludes this article.

6.2 Single Phase Boost Packed E-Cell Topology

Figure 6.1(a) and Figure 6.1(b) respectively depict the topologies of the conventional PEC and the proposed BPEC besides distinguishing their structural differences. Eight power switches and two DC links configure these topologies; two serial switches connected at the middle point

of the second DC link set up a bidirectional track for the bipolar current of the converters. Despite the conventional topology, the modified BPEC benefits a capacitor in the first DC link instead of an active DC source to reduce fabrication and maintenance costs. Therefore, BPEC as a passive converter is more suitable for PQASs. In addition, the colored parts in Figure 6.1(b) illustrate polarity differences between the power switches and DC links in the BPEC topology. As depicted, the polarity of the second DC link in BPEC is different from the first one, which allows the converter to boost the output ac voltage by adding the first DC link voltage to the second one. Accordingly, large multilevel voltages can be generated using lower DC link voltages with less volume, weight, and cost, resulting in less voltage stress and improved reliability.

6.2.1 Switching Sequences and Structural Features

Eight power switches including (S_1, S_4), (S_2, S_5), (S_3, S_7), and (S_6, S_8) operate complementary to protect the DC links from short circuits. Considering the complementary operation of the power switches, Table 6.1 presents the possible 12 switching vectors of the BPEC that lead to generating symmetrical multilevel voltage waveforms with 5-to-11-level resolutions. The switching vectors and the voltage levels include three zones, positive (orange), zero (gray), and negative (Blue). The bipolar zones also contain five sections, which means the maximum voltage resolution is 11 levels. The 11-level resolution is achieved based on the conditions shown in (6.1).

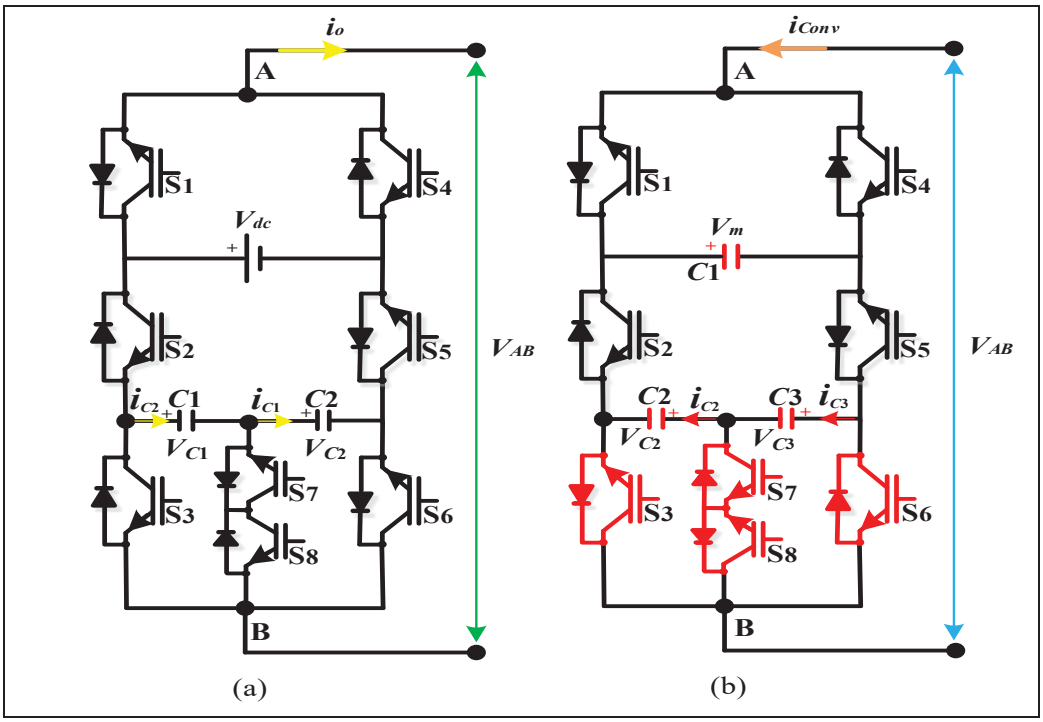

Figure 6.1 Visual comparison between schematic diagrams of (a) conventional packed E-cell and (b) the proposed boost packed E-cell (BPEC)

$$\begin{cases} V_m = \dfrac{V_{PCC}}{\sqrt{2}} \\ V_{C2} = V_{C3} = \dfrac{V_{PCC}}{3\sqrt{2}} \end{cases} \tag{6.1}$$

where V_m, V_{C2}, V_{C3}, and V_{PCC}, are the voltages of C_1, C_2, C_3, and the PCC, respectively.

Considering Table 6.1, Figure 6.2 shows the corresponding switching sequences of the BPEC that lead to different connections of the DC links to the AC side of the converter. Assuming S_7 and S_8 as a single bidirectional switch, only three power switches are engaged per switching sequence so that BPEC causes less switching and conduction loss compared with the other MLCs and CMLCs (Jahan, Abapour, & Zare, 2018; Saeedian, Hosseini, & Adabi, 2018; Siddique et al., 2020; Barzegarkhoo, 2017; Priyadarshi, Kar, & Karanki, 2020; Lee, Lim, & Lee, 2019; Sharifzadeh, Ahmadijokani, Mehrasa, Sadabadi, & Al-Haddad, 2021, October).

Table 6.1 Switching states and voltage levels of the BPEC

States	S_1	S_2	S_3	S_4	S_5	S_6	S_7	S_8	V_{out}
1	1	0	1	0	1	0	0	1	$V_m+V_{C2}+V_{C3}$
2	1	0	0	0	1	0	1	1	V_m+V_{C3}
3	1	0	0	0	1	1	1	0	V_m
4	0	0	1	1	1	0	0	1	$V_{C2}+V_{C3}$
5	0	0	0	1	1	0	1	1	V_{C3}
6	1	1	1	0	0	0	0	1	0
7	0	0	0	1	1	1	0	0	0
8	1	1	0	0	0	0	1	1	$-V_{C2}$
9	1	1	0	0	0	1	1	0	$-V_{C2}-V_{C3}$
10	0	1	1	1	0	0	0	1	$-V_m$
11	0	1	0	1	0	0	1	1	$-V_m-V_{C2}$
12	0	1	0	1	0	1	1	0	$-V_m-V_{C2}-V_{C3}$

The first and the last switching sequences in Figure 6.2 generate the peak amplitude of the multilevel voltage waveform in both polarities. Thus, the summation of both DC links determines the converter's peak voltage amplitude and boost factors (BF) for different level resolutions as below:

$$\begin{cases} BF_{11} = 1.67 \left(\dfrac{V_{PCC}}{\sqrt{2}} \right) \\ BF_{7} = 1.5 \left(\dfrac{V_{PCC}}{\sqrt{2}} \right) \\ BF_{5\&9} \simeq 2 \left(\dfrac{V_{PCC}}{\sqrt{3}} \right) \end{cases} \tag{6.2}$$

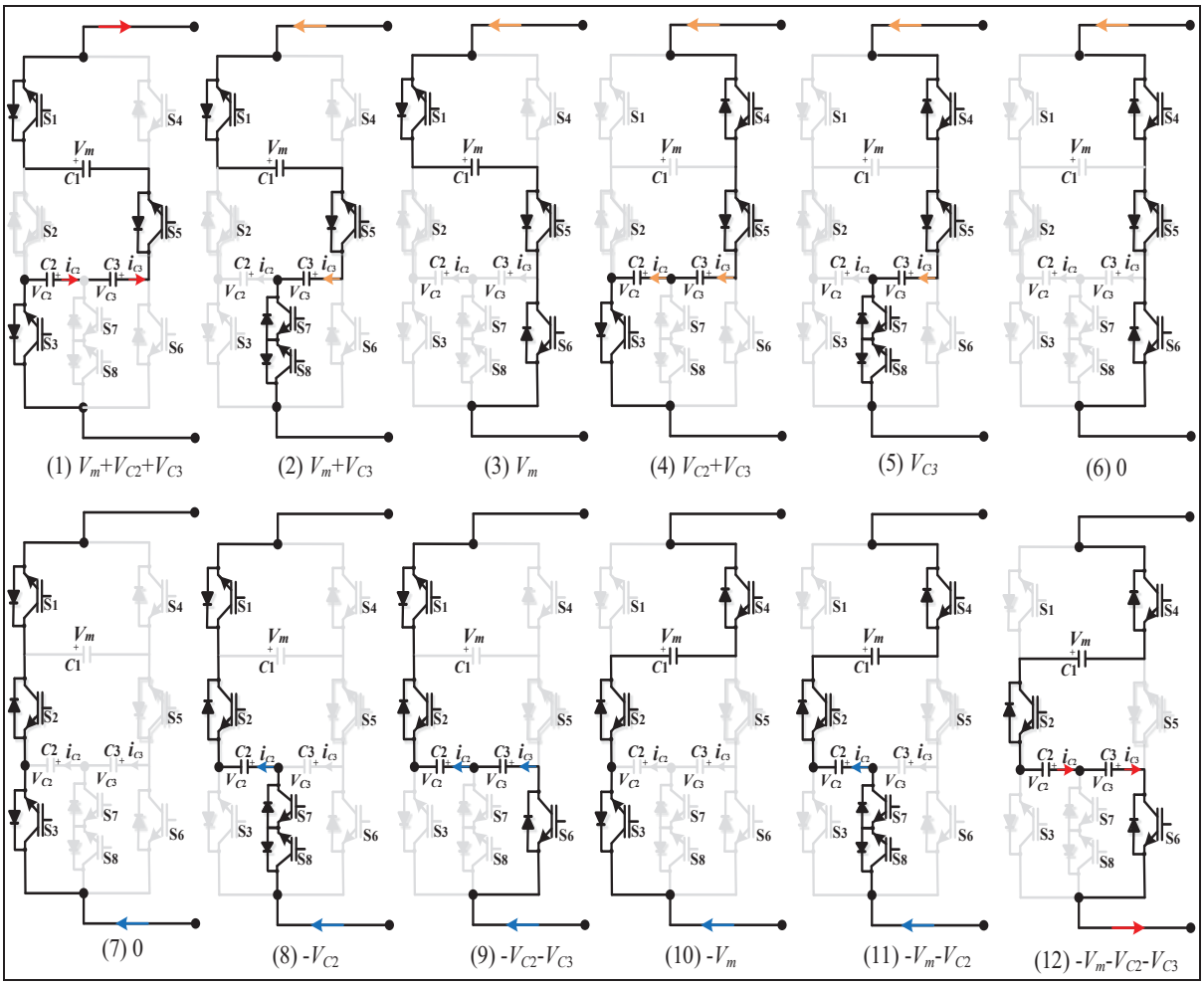

Figure 6.2 Switching sequences and corresponding configurations of the DC links

Equation (6.2) reveals that maximum BF is obtained based on 5- or 9-level resolution while the minimum rate belongs to the 7-level resolution with BF=1.5. However, BF5&9 cost more harmonic distortion, higher voltage stress, and larger capacitors. Consequently, the 11-level resolution offers the best trade-off among power quality, BF, costs, power loss, and the volume of the components. The switching operation of the BPEC regarding the 11-level resolution is detailed in Figure 6.3. As depicted in Figure 6.3(a), three capacitors equally contribute to the switching operation of the converter to generate the required voltage levels. Equation (6.3) presents two equations, which can be practical to estimate the size of the DC link capacitors.

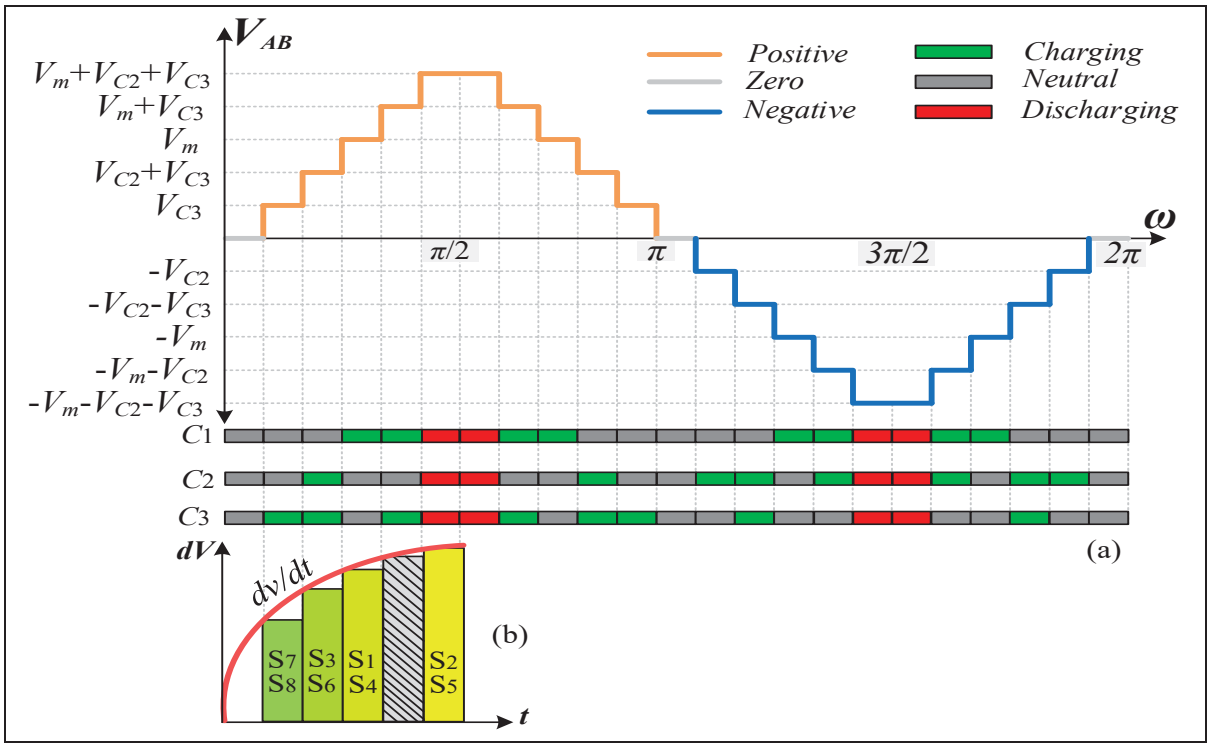

Figure 6.3 Switching operation of the BEPC (a) voltage levels and charging/discharging modes of the capacitors (b) voltage stress in terms of voltage variation over the pair switches

$$\begin{cases} C_1 = \dfrac{i_{Conv}}{8 f_{h1} \Delta V_m} \\ C_2 = C_3 = \dfrac{i_{Conv}}{8 f_{h1} \Delta V_{C2|3}} \end{cases} \tag{6.3}$$

where $i_{Conv}, f_{h1}, \Delta V_m, \Delta V_{C2|3}$ are respectively the input current of the converter, the fundamental frequency of the power system, and the voltage ripple of C_1, C_2, or C_3. Equation (6.3) discloses that C_2 and C_3 should be selected larger than C_1 since i_{Conv} with the same amplitude flows through both DC links while $\Delta V_{C2|3} << \Delta V_{C1}$. This phenomenon also impacts the other CMLCs, such as PUC, PEC, MPUC, and the other switched capacitors (Cahyosaputro, & Heru, 2018, September; Sharifzadeh, & Al-Haddad, 2019). Fortunately, lowering V_{C2} and V_{C3} to $V_{C1}/4$ and increasing the charging cycles (see (6.3)) of the capacitors allow the BPEC to shrink the size of C_1 and $C_{2,3}$. Figure 6.3(b) illustrates the voltage variation (dV) of the power switches based on the multilevel voltage waveform shown in Figure 6.3(a). According to this histogram plot,

S_7 and S_8 experience less voltage stress while S_2 and S_5 are under maximum voltage stress, which is $V_{C1}+V_{C2}+V_{C3}$.

Figure 6.4 demonstrates the relation between voltage stress and the switching performance of the power switches in the BPEC topology. Figure 6.4 reveals that the switching frequency (f_{sw}) and voltage stress are unequal among the power switches. The switching frequency of S_7 and S_8 is equal to f_{sw} while their voltage stress is below 25% of the maximum dV. On the contrary, S_2 and S_5 should tolerate 100% of the voltage stress while their average switching frequency is about 12% of f_{sw}. In conclusion, although f_{sw} and dv/dt are unevenly distributed among the power switches, they have mutual effects and inherently neutralize the adverse impacts of each other on the power loss and switching performance of the converter. In addition, the green curve in Figure 6.4 proves that increasing the voltage levels from 9 to 11 mitigates the voltage stress on S_3 and S_6 by 10%.

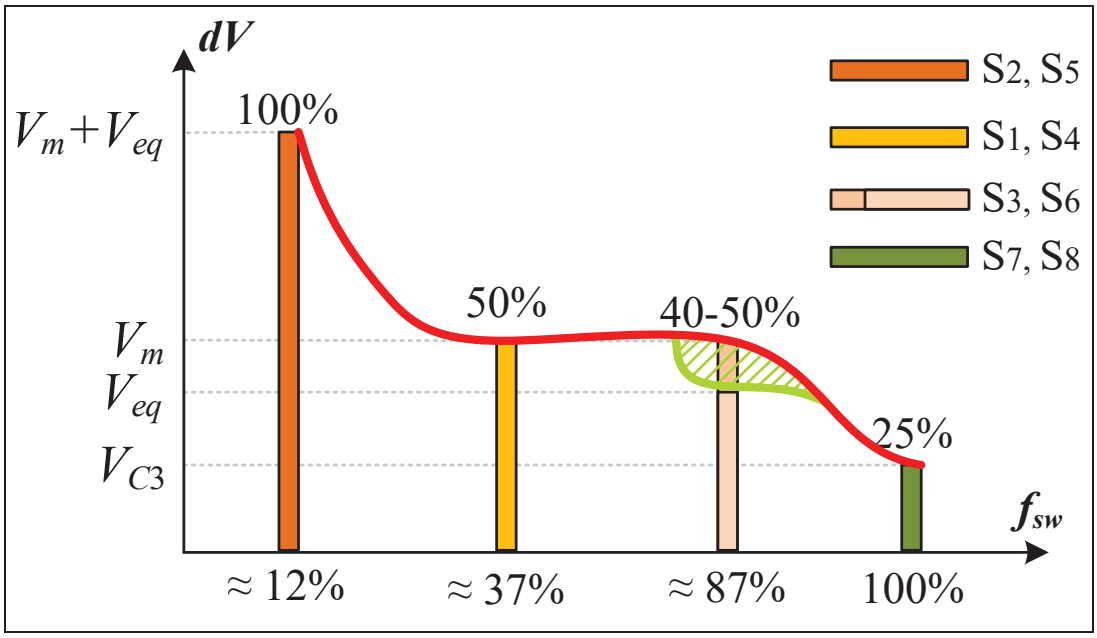

Figure 6.4 Comparison between switching frequency and voltage stress for the power switches of the BPEC ($V_{eq}=V_{C2}+V_{C3}$)

6.2.2 Modeling and Control

Despite conventional two-level converters, modeling and control of MLCs like BPEC are more complicated because of using several switched capacitors. Regarding the inductor current of the input filter and the voltages of the DC link capacitors, BPEC includes four state variables, which should be precisely described and controlled. Sections 6.3 and 6.4 also show that additional parameters like the switching frequency and voltage stress can be considered in the modeling and control of the BPEC to enhance its performance. Figure 6.5 presents an electrical schematic of a power system in which BPEC is used for PQASs and modeled as a voltage-dependent voltage source. The voltage-dependent factor of VAB is also defined in (6.4) for different level resolutions.

$$BF_x\left(\frac{V_{PCC}}{\beta}\right)\begin{vmatrix} BF_{11} = 1.67,\ \beta = \sqrt{2} \\ BF_7 = 1.5,\ \beta = \sqrt{2} \\ BF_{5\&9} = 2,\ \beta = \sqrt{3} \end{vmatrix} \tag{6.4}$$

V_{AB} as the multilevel output voltage of the BPEC is modeled in (6.5).

$$\begin{aligned} V_{AB} &= \left(S_1 - S_2\right) V_m \\ &\quad + \left(S_3 - S_2\right) V_{C2} + \left(S_3 - S_2 + S_8 - S_3S_8\right) V_{C3} \end{aligned} \tag{6.5}$$

V_m is the voltage of the first capacitor, S_1, S_2, S_3, S_8 are the corresponding switching variables of the power switches. V_{AB} is indeed a combination of the switched capacitors used in the DC links. As a result, controlling the voltages of the capacitors is crucial to avoid power quality degradation, severe voltage stress, and power losses. Equations (6.6) to (6.8) present the required dynamic model of the switched capacitors, respectively.

$$C_1 \frac{dV_m}{dt} = \left(S_1 - S_2\right) i_{Conv} \tag{6.6}$$

$$C_2 \frac{dV_{C2}}{dt} = \left(S_3 - S_2 \right) i_{Conv} \tag{6.7}$$

$$C_3 \frac{dV_{C3}}{dt} = \left(S_8 - S_2 \right) i_{Conv} \tag{6.8}$$

Equations (6.6) to (6.8) reveal that BPEC needs three sensors to control the DC link capacitors. However, serial expansion of the capacitors in the second DC link makes it possible to measure and control the equivalent voltage of both capacitors using one sensor. Regarding this fact, (6.7) and (6.8) should be merged as (6.9) to fulfill the sensor reduction objective.

$$\frac{dV_{eq}}{dt} = \frac{1}{C_{eq}} \left(S_3 - S_2 \right) i_{conv} \quad \Big| \quad V_{eq} = V_{C2} + V_{C3}, \quad C_{eq} = \frac{C_2 C_3}{C_2 + C_3} \tag{6.9}$$

According to (6.6) to (6.9), the switching incidents and the input current directly affect the voltage ripple and stability of the capacitors. Thus, the switching operation of the converter and the input current should be appropriately modeled and controlled. Applying KVL and KCL laws to the PCC shown in Figure 6.5 leads to the following dynamic model of the input current.

$$i_{conv} \frac{di_{Conv}}{dt} = \frac{1}{L_C} \left(V_g - V_{AB} - L_g \frac{di_g}{dt} - r_C i_{Conv} - r_g i_g \right) \tag{6.10}$$

where L_C, L_g, r_C, and r_g are respectively the inductance and resistance of the input filters of the converter and grid. V_g also represents the grid voltage.

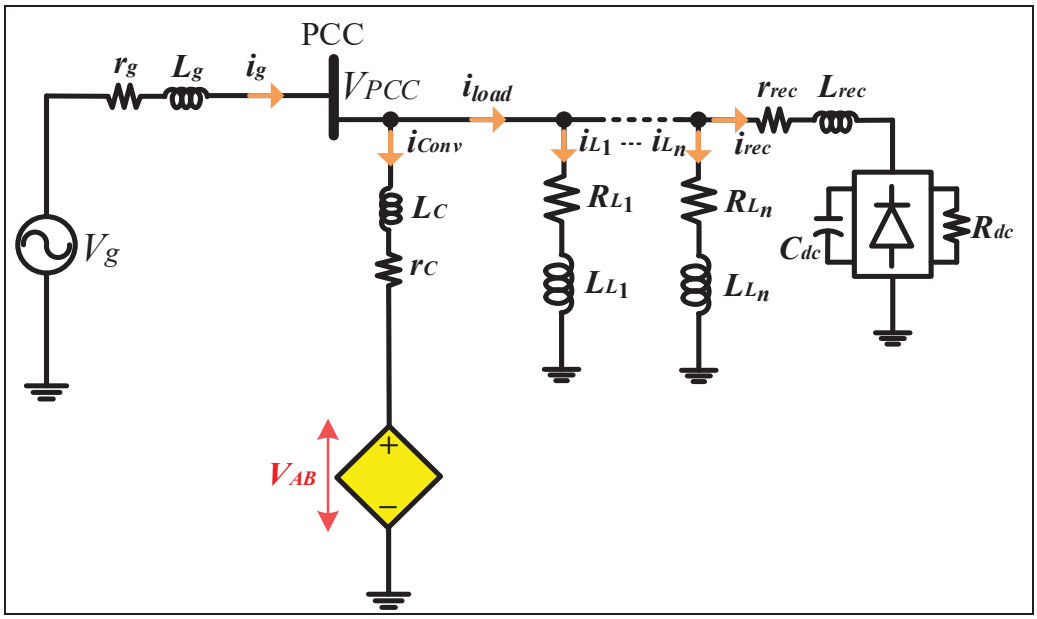

Figure 6.5 Generalized electrical schematic of a power system including the grid, loads, filters, and the equivalent, voltage-dependent model of the BPEC

6.2.3 Fault Tolerance and Voltage Level Switching Mode

Even though CMLCs provide the best trade-off between the components count and voltage levels, fault tolerance is not usually available in this class of multilevel topologies due to the limited number of switches that restricts the redundant paths for the current (Trabelsi, Vahedi, & Abu-Rub, 2021; Sharifzadeh, Ahmadijokani, Mehrasa, Sadabadi, & Al-Haddad, 2021, October; Salem et al., 2020; Lee, Sidorov, Idris, & Heng, 2017; Saeedian, Hosseini, & Adabi, 2018; Vahedi, Shojaei, Dessaint, & Al-Haddad, 2017). Indeed, there are some compact multilevel topologies with fault tolerance capability; however, the number of components including switches, diodes, and DC links is adversely increased (Sotoodeh, & Miller, 2013; Sharifzadeh, & Al-Haddad, 2019; Siddique et al., 2020; Priyadarshi, Kar, & Karanki, 2020; Sharifzadeh, Ahmadijokani, Mehrasa, Sadabadi, & Al-Haddad, 20201, October). As a comparison, the topology of a nine-level PUC in (Cahyosaputro, & Heru, 2018, September) reveals that any fault of switches disables the converter; however, the proposed BPEC with the same number of components remains operational in the event of any fault of the middle switches (S_7 and S_8). Thus, fault tolerance is another promising feature of the BPEC that retains

its functionality under the open-circuit fault of the middle switches. Accordingly, (6.11) shows that the open-circuit fault of S_7 or S_8 turns the BPEC into MPUC topology so that the converter remains operational by generating an asymmetrical seven-level voltage waveform without using a fault detection system. Equation (6.11) is the modified version of (6.5) when S_8=0.

$$V_{AB} = (S_1 - S_2) V_m + (S_3 - S_2) (V_{C2} + V_{C3}) \quad (6.11)$$

Figure 6.6 indicates that in the case of the 11-level resolution, the post-fault multilevel voltage waveform is asymmetrical because V_{C2} and V_{C3} cannot be separately connected to the AC terminals. The asymmetrical waveform slightly impairs the power quality as illustrated and discussed in Section 6.4. Generating symmetrical post-fault multilevel voltage waveforms is also doable thanks to the voltage level switching mode (VLSM) of the operation of the BPEC. The VLSM allows the converter to generate a flexible voltage waveform where the number of the levels is instantly modified using the control loop supported by a fault detection system.

As illustrated in Figure 6.7, the voltage amplitudes of the DC links determine the resolution of the multilevel waveform. e.g., the red oval with the solid outline represents the 11-level resolution. More precisely, the oval shape presents the unequal voltages of the DC links, while its diameters display the voltage amplitude of the DC links that lead to the 11-level waveform. The red oval with the broken outline also demonstrates the voltage conditions of the asymmetrical post-fault 7-level waveform. The blue circle with the solid border shows that a 9-level voltage waveform can be generated when the first and the second DC links are equally set to VPCC/√3. The broken blue circle reveals that although the voltages of the DC links are equal, the resolution of the multilevel waveform reduces to five in the post-fault period. The green oval depicts the voltage conditions in which a symmetrical 7-level voltage waveform is generated. The recommended voltage conditions of the DC links in Figure 6.7 are practical to design a controller, which can enhance the BPEC flexibility to generate various multilevel waveforms pre/post fault circumstances, as discussed later in Section 6.4.

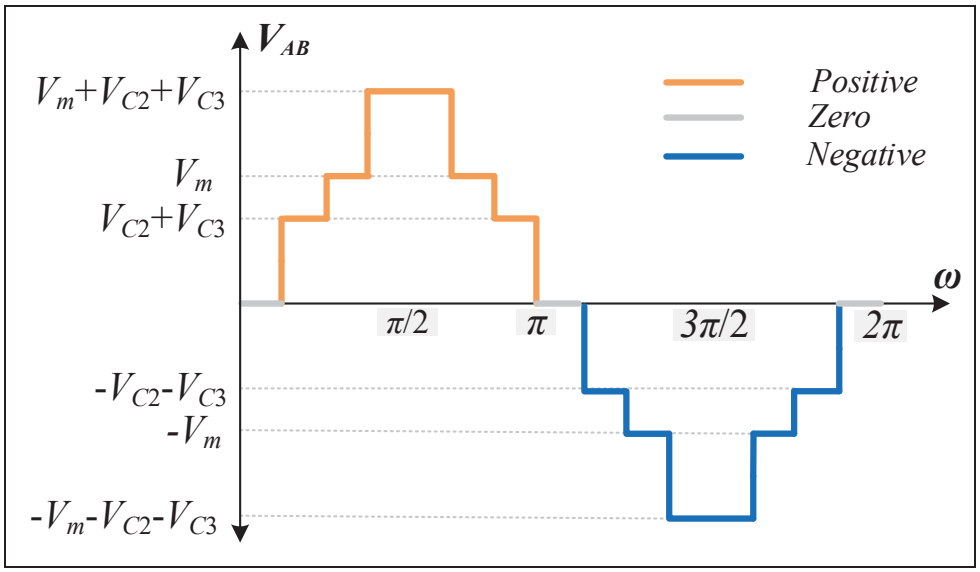

Figure 6.6 Post-fault performance of the BPEC under the open-circuit fault of S_7 or S_8 without using a fault detector

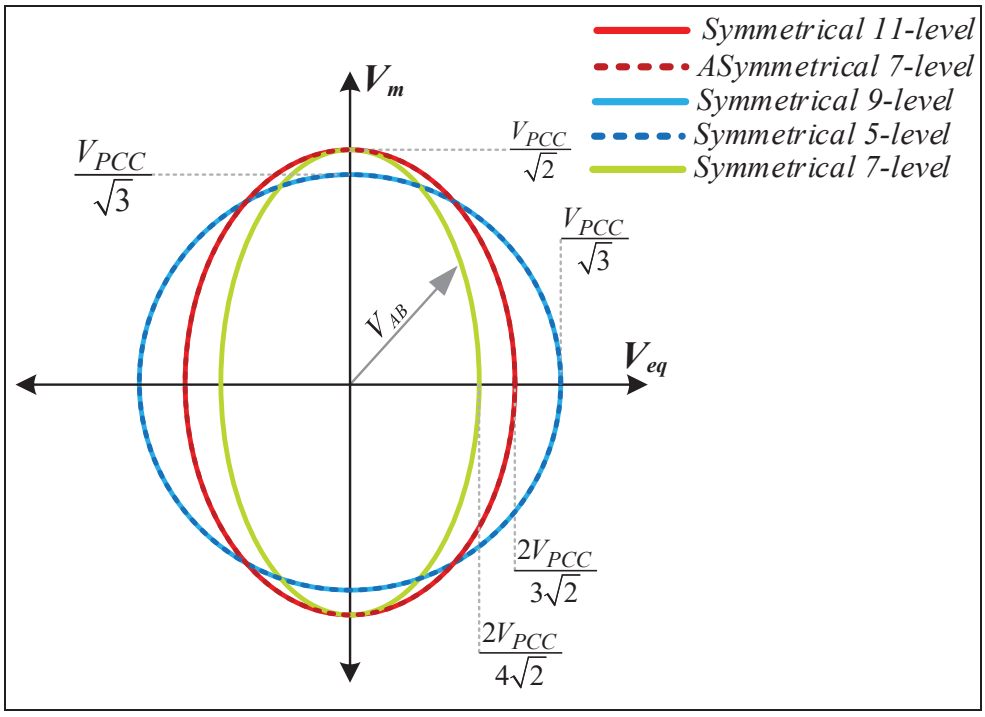

Figure 6.7 Voltage level switching mode of operation of the BPEC regarding the voltage amplitude of the DC links

6.2.4 Laboratory Prototype of the BPEC for PQASs

The feasibility of the BPEC has been investigated by means of a 3kVA prototype shown in Figure 6.8. In this prototype, the power switches are C3M0120090D, and the decoupling capacitors of the DC links are PHE845VW7100MR06L. Moreover, CDV19FF201JO3F and NCR3WSKR-73-15R have been used to implement the RC snubbers. The DC link capacitors are separately connected to specific input terminals prepared on both sides of the converter.

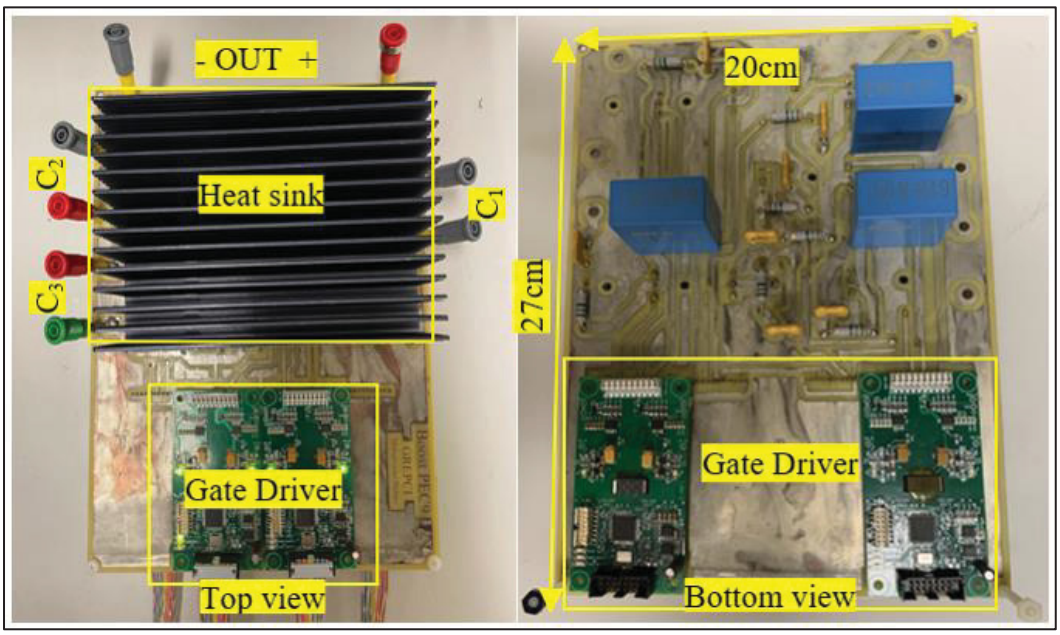

Figure 6.8 3kVA laboratory prototype of the proposed BPEC converter

6.2.5 Competitive Studies

Considering the growing penetration of harmonic loads, increasing the PQASs is essential for modern grids. Without using cost-effective boost converters, the implementation and maintenance cost of PQASs is seriously increased because the reliability of the power systems is reduced, the lifetime of the components is shortened, and the stress voltage is intensified, simultaneously.

Table 6.2 Comparison of the BPEC with the recent CMLC topologies for PQASs

Topology	**VL**	**SC**	**VS**	**FT**	**BF**
BPEC	5, 7, 9. 11	8	$2V_m$	Yes	2
PEC	5, 7, 9	8	$3V_m/2$	Yes	2
PUC	5, 7, 9	6	$3V_m/2$	No	2
MPUC	5, 7	6	$2V_m$	No	2
(Saeedian et al., 2018)	7	7	$2V_m$	No	2
(Siddique et al., 2020)	5, 7	10	$3V_m$	Yes	3
(Barzegarkhoo et al., 2017)	9	10	NA	No	2
(Babaie et al., October)	11	9	$5V_m$	Yes	1
(Sotoodeh et al., 2013)	11	20	$V_m/5$	Yes	1
(Priyadarshi et al., 2020)	11	10	$9V_m$	Yes	9.4
(Lee et al., 2019)	9, 11	12	$2V_m$	Yes	2.5
(Sharifzadeh et al., 2021, October)	9, 11	12	$2V_m$	Yes	2
(Jahan et al., 2018)	9	18	$3.75V_m$	Yes	3.75
Topology	**SeC**	**DC**	**NS**	**BO**	**MV**
BPEC	2	0	3	Yes	$V_{PCC}/\sqrt{2}$
PEC	2	0	3	Yes	$2V_{PCC}/\sqrt{3}$
PUC	2	0	3	Yes	$2V_{PCC}/\sqrt{3}$
MPUC	2	0	2	Yes	$V_{PCC}/\sqrt{2}$
(Saeedian et al., 2018)	0	4	3	Yes	$V_{PCC}/\sqrt{2}$
(Siddique et al., 2020)	0	0	3	Yes	$V_{PCC}/2\sqrt{2}$
(Barzegarkhoo et al., 2017)	0	1	3	No	$2V_{PCC}/3\sqrt{3}$
(Babaie et al., October)	0	5	5	No	$2V_{PCC}/\sqrt{3}$
(Sotoodeh et al., 2013)	6	0	5	Yes	$2V_{PCC}/\sqrt{3}$
(Priyadarshi et al., 2020)	1	9	5	No	$V_{PCC}/9.4\sqrt{2}$
(Lee et al., 2019)	4	0	5	Yes	$2V_{PCC}/\sqrt{3}$
(Sharifzadeh et al., 2021, October)	2	0	3	Yes	$V_{PCC}/\sqrt{2}$
(Jahan et al., 2018)	4	4	5	Yes	$V_{PCC}/3.75\sqrt{2}$

Regarding, this subsection compares the BPEC with the other CMLCs in terms of voltage levels (VL), switches count (SC), voltage stress (VS), fault tolerance (FT), BF, sensors count (SeC), diodes count (DC), number of DC sources (NS), bidirectional operation (BO), and minimum voltage (MV) of the main DC link (V_m) for PQASs. Table 6.2 presents the corresponding comparison results and demonstrates the competitive merits of the BPEC (Jahan, Abapour, & Zare, 2018; Babaie, Sharifzadeh, Kanaan, & Al-Haddad, 2020; Babaie, Sharifzadeh, & Al-Haddad, 2019, October; Sotoodeh, & Miller, 2013; Cahyosaputro, & Heru, 2018, September; Sharifzadeh, & Al-Haddad, 2019; Saeedian, Hosseini, & Adabi, 2018; Siddique et al., 2020; Barzegarkhoo et al., 2017; Priyadarshi, Kar, & Karanki, 2020; Lee et al., 2019; Sharifzadeh, Ahmadijokani, Mehrasa, Sadabadi, & Al-Haddad, 2021, October; Vahedi, Shojaei, Dessaint, & Al-Haddad, 2017). In this Table, V_m represents the largest DC link voltage.

6.3 Case Study: Compact Active Power Filter with Reactive Power Compensation Ability

An active power filter is an essential power electronic device used to provide power quality ancillary services for the grid in the presence of nonlinear loads. APF immediately eliminates the harmonic pollution of nonlinear loads before their penetration into the grid.

As a case study, the proposed BPEC topology is configured as a compact active power filter (CAPF) to investigate its feasibility for power quality ancillary services. Figure 6.9 illustrates a typical power system where the BPEC is used as the CAPF to suppress the adverse impacts of the nonlinear loads on the grid power quality. In addition, the CAPF can provide reactive power for the linear loads besides eliminating the harmonic pollutants. The multi-functional task of the CAPF is realized using a multi-objective control loop designed based on an MPC algorithm. In the first design step of the MPC, the switched model of the BPEC presented in (6.5) to (6.10) is discretized using the forward and backward Euler methods as follows:

$$\frac{i_g(k+1)-i_g(k)}{\Delta t}=\frac{1}{L_g}\begin{pmatrix} V_g(k)-V_{AB}(k+1) \\ -L_C\left(\frac{i_{Conv}(k)-i_{Conv}(k-1)}{\Delta t}\right) \\ -r_C i_{Conv}(k)-r_g i_g(k) \end{pmatrix} \tag{6.12}$$

$$\frac{V_m(k+1)-V_m(k)}{\Delta t}=\left(\frac{S_1(k)-S_2(k)}{C_1}\right) i_{Conv}(k) \tag{6.13}$$

$$\frac{V_{eq}(k+1)-V_{eq}(k)}{\Delta t}=\frac{C_2C_3}{C_2+C_3}\left(S_3(k)-S_2(k)\right) i_{Conv}(k) \tag{6.14}$$

where $V_g(k)$, $i_g(k)$, and $i_g(k+1)$ are respectively the grid voltage and current at kth and $k+1$th time instants. $V_m(k)$, $V_{eq}(k)$, $V_m(k+1)$, and $V_{eq}(k+1)$ are also the measured voltage of C_1, as well as, the equivalent voltage of C_2, and C_3 (C_{eq}) at the kth and $(k+1)$th time instants, respectively. Δt is the time interval between two samples or the sampling time of the controller (T_S). $i_{Conv}(k)$, and $i_{Conv}(k\text{-}1)$ are respectively the measured input current of the CAPF in the kth and the $(k\text{-}1)$th samples. $S_1(k)$, S_2(k), and $S_3(k)$ are the switching variables defined in Table 6.1 in the form of switching vectors. The predictive switching model defined in (6.15) allows the MPC to reduce and regulate the average switching frequency of the CAPF.

$$\begin{aligned} F(k+1) = &\left|S_1(k+1)-S_1(k)\right|+\left|S_2(k+1)-S_2(k)\right| \\ &+\left|S_3(k+1)-S_3(k)\right|+\left|S_8(k+1)-S_8(k)\right| \end{aligned} \tag{6.15}$$

where $S_1(k+1)$, $S_2(k+1)$, and $S_3(k+1)$ are the candidate switching states in the next sampling period. Equation (6.15) is formulated based on the main switching variable to reduce the computational burden. Equation (6.16) shows four simple conditions that alleviate the voltage stress of (S_1, S_4), (S_3, S_7), and (S_6, S_8) in terms of voltage variation. These conditions regulate the switching performance of the MPC regarding minimum voltage variation.

$$\begin{cases} \vec{S}(k+1) = 3, & \text{if } \vec{S}(k) = 4 \quad \& \quad \vec{S}^{P}(k+1) = 2 \\ \vec{S}(k+1) = 3, & \text{if } \vec{S}(k) = 2 \quad \& \quad \vec{S}^{P}(k+1) = 4 \\ \vec{S}(k+1) = 9, & \text{if } \vec{S}(k) = 10 \quad \& \quad \vec{S}^{P}(k+1) = 8 \\ \vec{S}(k+1) = 9, & \text{if } \vec{S}(k) = 8 \quad \& \quad \vec{S}^{P}(k+1) = 10 \end{cases} \tag{6.16}$$

where $\vec{S}(k+1)$ and $\vec{S}(k)$ are respectively the future and current switching vectors in the next and current sampling instants. $\vec{S}(k+1)$ is also the best switching vector determined by MPC for the next sampling period. Using the predictive model of CAPF presented in (6.15) to (6.17), the MPC cost function, including four control objectives, is formulated in (6.18).

$$\begin{cases} i_g(k+1) = \dfrac{T_S}{L_g} \left(\begin{array}{l} V_g(k) - V_{AB}(k+1) - r_C i_{Conv}(k) - r_g i_g(k) \\ -L_C \left(\dfrac{i_{Conv}(k) - i_{Conv}(k-1)}{T_s} \right) \end{array} \right) + i_g(k) \\ V_m(k+1) = \dfrac{T_S}{C_1} \left(S_1(k) - S_2(k) \right) i_{Conv}(k) + V_m(k) \\ V_{eq}(k+1) = T_S \dfrac{C_2 C_3}{C_2 + C_3} \left(S_3(k) - S_2(k) \right) i_{Conv}(k) + V_{eq}(k) \end{cases} \tag{6.17}$$

$$\begin{aligned} G(k+1) = \lambda_1 \left(i_g(k+1) - i_g^*(k+1) \right)^2 + \lambda_2 \left(V_m(k+1) - V_m^*(k+1) \right)^2 \\ + \lambda_3 \left(V_{eq}(k+1) - V_{eq}^*(k+1) \right)^2 + \eta F \left(k+1 \right) \end{aligned} \tag{6.18}$$

where $i^*_g(k+1)$, $V^*_m(k+1)$, and $V^*_{eq}(k+1)$ are respectively the desired references for the CAPF current and the DC link voltages. λ_1, λ_2, λ_3, and η are the weighting factors considered to adjust the impact of the control objectives on the optimization process of the cost function. Since the relation between the input current and the DC link voltages is nonlinear, the tuning of λ_1, λ_2, and λ_3 is exhausting. η is defined as a constant since the switching frequency is independent of the state variables.

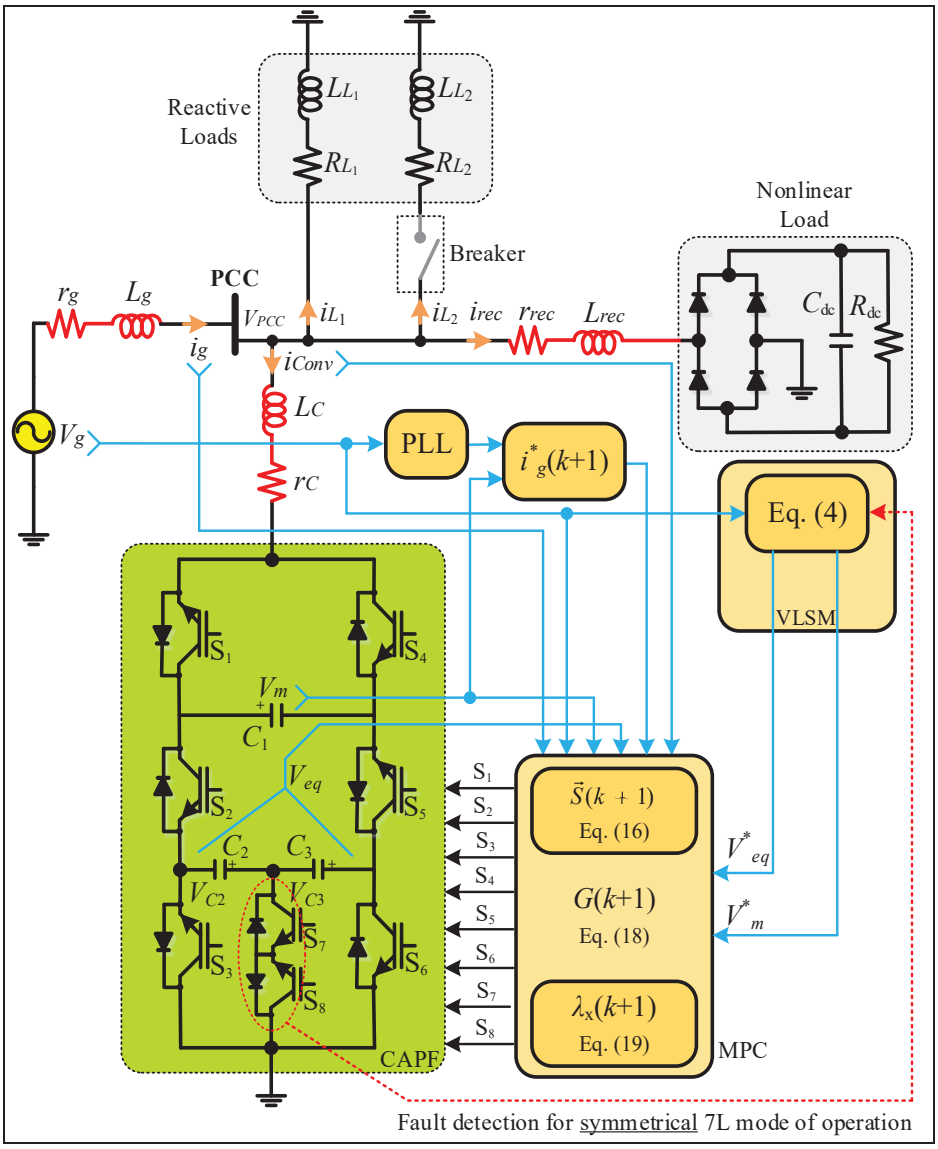

Figure 6.9 APF configuration of the BPEC for power quality ancillary services in the presence of reactive and nonlinear loads

As a solution, three adaptive equations based on the tracking errors of the input current (e_{iconv}) and the DC link voltages (e_{Vm}, e_{Veq}) are suggested in (6.19) to relieve the tuning difficulties of the weighting factors.

$$\begin{cases} \lambda_1(k+1) = Sat\left(\dfrac{e_{i_{Conv}}(k)^2}{e_{i_{Conv}}(k)^2 + e_{Vm}(k)^2 + e_{Veq}(k)^2 + 0.6} \right) \\ \lambda_2(k+1) = Sat\left(\dfrac{e_{Vm}(k)^2}{i_{Conv}(k)^2 + e_{Vm}(k)^2 + e_{Veq}(k)^2 + 0.2} \right) \\ \lambda_3(k+1) = Sat\left(\dfrac{e_{Veq}(k)^2}{i_{Conv}(k)^2 + e_{Vm}(k)^2 + e_{Veq}(k)^2 + 0.4} \right) \end{cases} \tag{6.19}$$

According to (6.19), any increase in the error functions is immediately compensated with the corresponding increase in the weighting factors. This unique tuning strategy turns the conventional constant weighting factors into floating values and significantly improves the robustness of the MPC during unstable conditions. Equations (6.17) to (6.19) can only stabilize the DC link voltages and input current without addressing the harmonics and power factor issues. Indeed, the power quality ancillary services including harmonic elimination and power factor correction are realized using the dynamic reference current defined in (6.20).

$$i_g^*(k+1) = \left(\alpha e_{Vm}(k) + \delta \frac{T_s}{\tau} \sum_{j=0}^{Z} e_{Vm}(j) \right) \sin\left(\omega k \pm \theta \right) \tag{6.20}$$

where α and δ are the PI control factors, τ is the integral time constant of the PI controller, ω_g is the sampled angular velocity of the grid measured by PLL. Z is the total samples of the error signal required to calculate the discrete integral per sampling period. θ represents the desired phase angle and is used to control the converter's reactive power regardless of the grid unity power factor. Equation (6.20) is a simple digital realization of a PI controller that dynamically estimates the amplitude and phase of the CAPF based on e_{Vm} and ω_g so that harmonics and reactive power are immediately compensated without using any complex observer, such as FFT-based algorithms. Technically, (6.20) generates a sinusoidal waveform synchronized with the grid angular velocity, as the reference current, and then this reference is applied to the predictive controller for harmonic cancelation purposes. In the MPC, the grid current is measured and then compared with this reference signal through the cost function defined in

(6.18). As a result, a harmonic current waveform including all the load harmonics with inverse phase is inherently generated by the CAPF that eliminates the existing harmonics of the loads at the PCC.

The reactive power is controlled through the phase of the reference current defined in (6.20). In the case of reactive power, CAPF has three DC link capacitors which can effectively contribute to compensation for the reactive power of the loads. Since the reference current is synchronized with the grid voltage, CAPF is forced to track the grid angular velocity. Accordingly, the reactive power of the loads is immediately compensated by CAPF at the PCC.

In summary, using (6.20), CAPF generates a lagging/leading harmonic current to preserve the grid power quality in terms of THD and power factor without measuring the load side current of the PCC. Figure 6.9 illustrates the block diagram of the control loop beside the CAPF. A digital band-pass filter, a discretized integrator using the forward Euler method, and a specific reset condition as (6.21) are considered to design the PLL unit used in Figure 6.9. This technique is easy to implement and enough accurate to observe the angular velocity of the grid under different conditions. It is worth mentioning that a discrete integrator with a similar structure is available in MATLAB as Discrete-Time Integrator.

$$\begin{cases} \omega\ (\ k\ ) = \omega\ (\ k-1\ ) + \kappa T_s \omega_{ref} \\ \omega_{ref} = 2\pi f_{h1} \\ \text{Reset Condition: } V_g(k)\ \dfrac{2.841e^{-5}z + 2.84e^{-5}}{z^2 - 1.999z + 0.9988} \end{cases} \tag{6.21}$$

where f_{h1} in (6.21) is the grid fundamental frequency and κ is the integrator gain.

6.4 Experimental and Simulation Studies

This section presents the experimental and simulation results of testing the CAPF in a power system, which is drawn in Figure 6.9 and practically implemented in Figure 6.10. In the

experimental setup, the MPC has been implemented using MicroLabBox 1202, and CAPF has been designed using the 3kW prototype of BPEC shown in Figure 6.8. The voltages and currents have been sensed using OPAL-RT OP8662, and Chroma 61086 has been utilized to emulate the grid besides supplying the linear and nonlinear loads. The experimental setup parameters are also detailed in Table 6.3. Regarding Table 6.3, two linear RL loads with variable resistances are considered besides a nonlinear load to form the load side of the PCC.

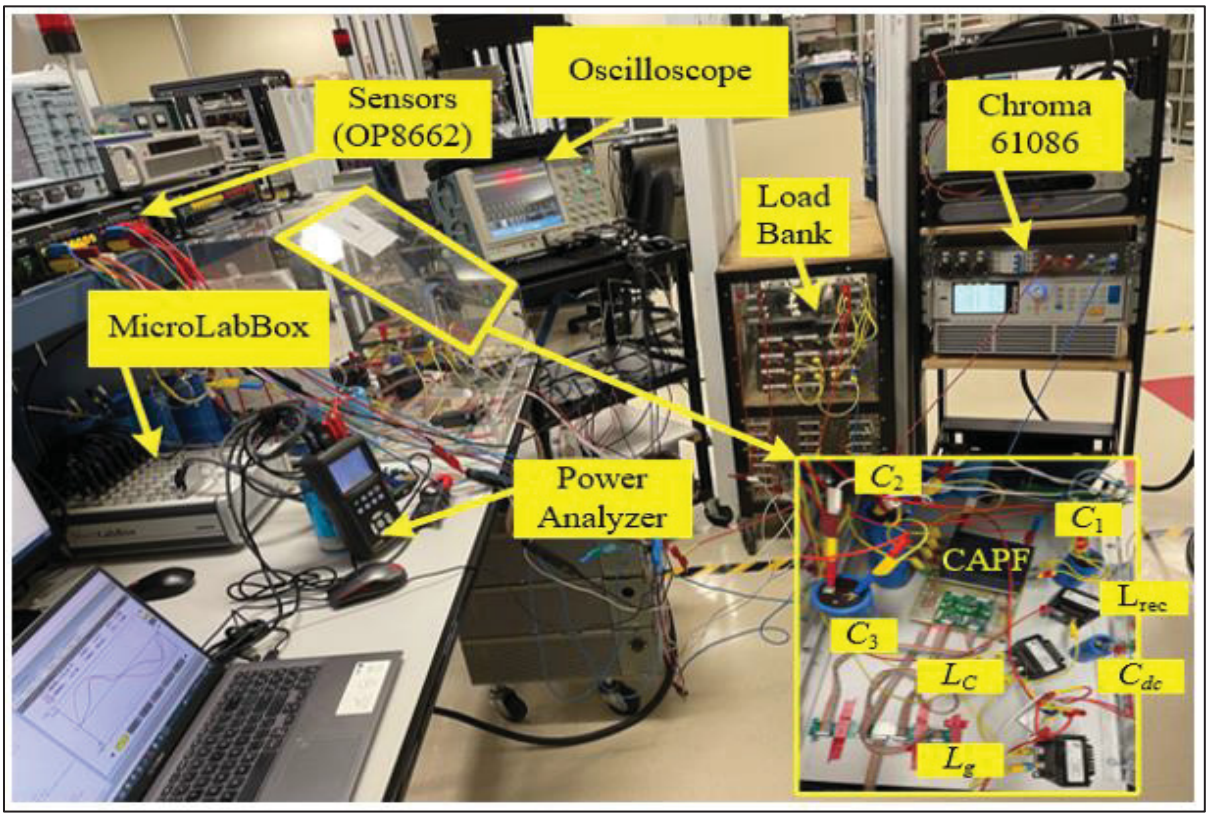

Figure 6.10 A photo from the power system that was used to evaluate the performance of the BPEC as CAPF

The nonlinear load is a single-phase full-bridge rectifier including a resistor and an electrolytic capacitor, where the capacitor is intentionally used to intensify the harmonic pollution of the nonlinear load. Figure 6.11(a) illustrates the voltage and currents of the grid, first load, and the rectifier when the CAPF is disconnected. This figure indicates the importance of PQASs, as the grid current is seriously deformed in the lack of the CAPF.

Table 6.3 Main parameters of the power system and control loop

Grid voltage (rms)	120 V
Grid fundamental frequency (f_{h1})	60 Hz
V_m for the 11-level resolution	120 V
V_{eq} (V_{C2}+V_{C3}) for the 11-level resolution	80 V
Sampling time	20 μs
C_1 (capacitance, maximum voltage)	1500 μF, 200 V
C_2=C_3 (capacitance, maximum voltage)	2100 μF, 100 V
L_C=L_g=L_{rec}, r_C=r_g=r_{rec}	2.5 mH, 0.01 Ω
DC side of the nonlinear load (C_{dc}, R_{dc})	1000 μF, 40 Ω
Linear load-1 (L_{L1}, R_{L1})	10 mH, 40-80 Ω
Linear load-2 (L_{L2}, R_{L2})	30 mH, 40-80 Ω
α, δ, η	0.6, 0.7, 0.1

The detailed results in Figure 6.11(b) and Figure 6.11(c) demonstrate that the power factor (PF) and THD have been respectively reduced to 0.89% and increased to 39%, which are damaging. With the exact configuration of the loads, the results in Figure 6.12 exhibit the promising performance of the CAPF to enhance the grid power quality in light of the reactive and nonlinear loads. The converter's voltages in Figure 6.12(a) verify the optimum performance of the MPC as minimum voltage ripple and spikes appeared in the waveforms. Additional results for the current waveforms of the grid, CPAF, and loads in Figure 6.13 graphically describe how CAPF mitigates the harmonic pollutants and compensates for the reactive power. As shown in Figure 6.13(a), the CAPF generates a harmonic current with controlled phase lag/lead to simultaneously overcome the adverse impacts of the loads on the grid THD and power factor. The test results of connecting the second reactive load in Figure 6.13(b) to Figure 6.13(e) comprehensively verify the robustness of the control loop and the capability of the CAPF to support and ascertain the grid power quality in dynamic circumstances.

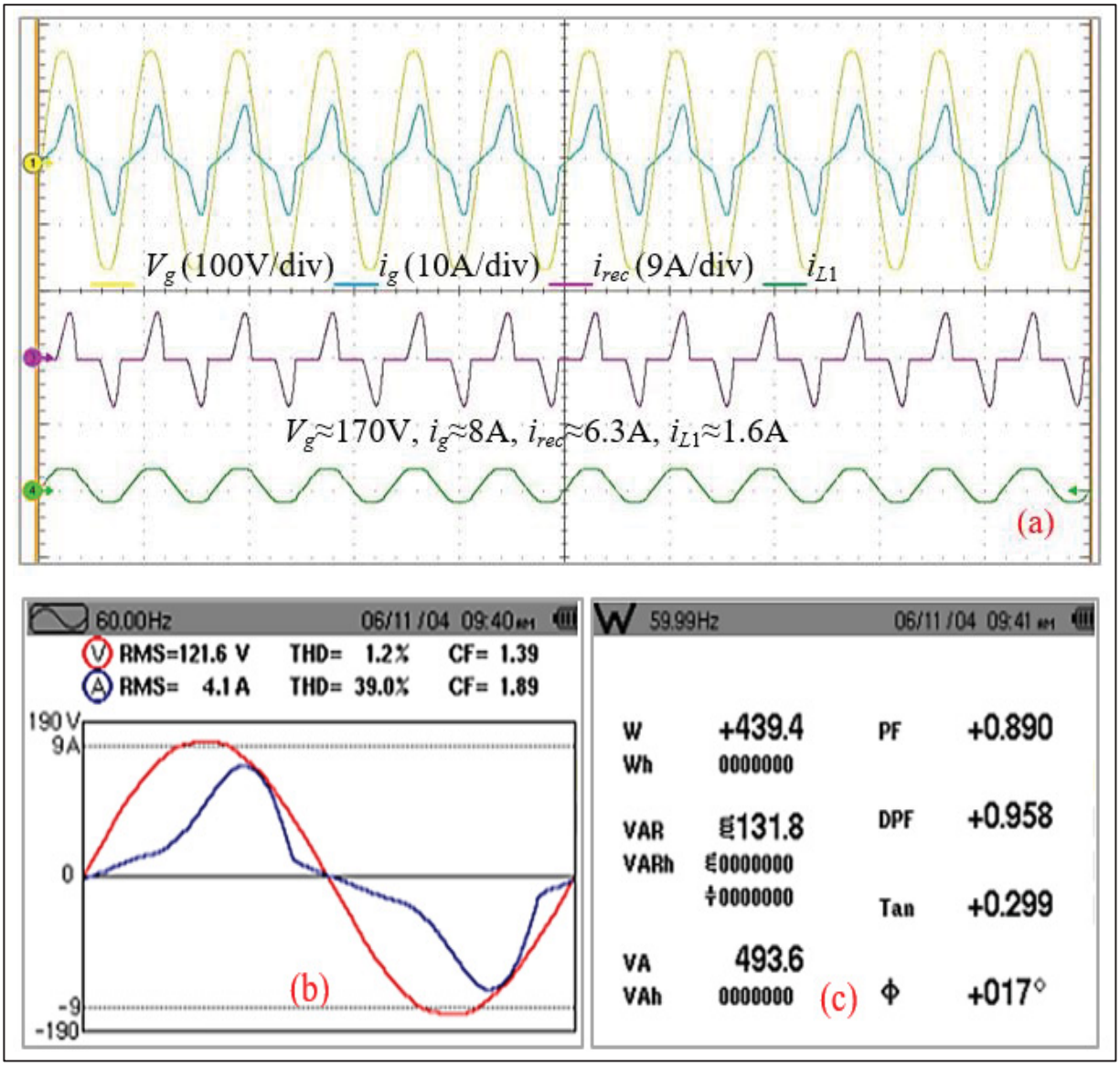

Figure 6.11 Experimental results of the power system when the CAPF is off (a) the voltage and current amplitudes and waveforms (b) THD analysis of the grid voltage and current (c) power quality analysis of the grid

The power quality analysis in Figure 6.13(d) and Figure 6.13(e) illustrates the standard level of THD and unity power factor of the grid in the presence of unknown non/linear loads.

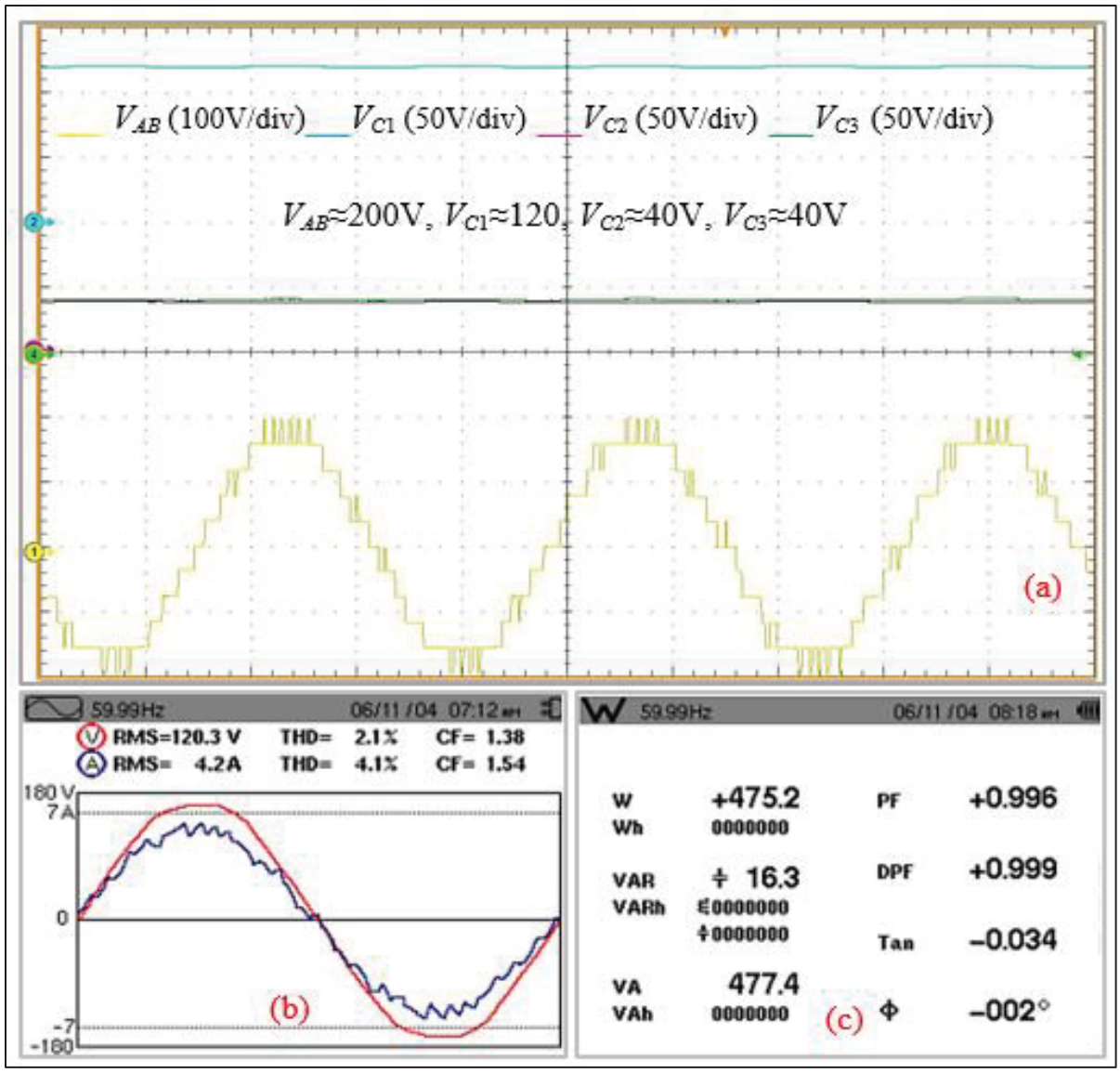

Figure 6.12 Experimental results when BPEC operates as the CAPF in the power system (a) the DC voltages and multilevel waveform (b) THD analysis of the grid voltage and current (c) power quality analysis of the grid

It is worth mentioning that the results in Figure 6.13(d) and Figure 6.13(e) were captured after connecting the second reactive load to the PCC. The loads are considered unknown because the load currents are not measured.

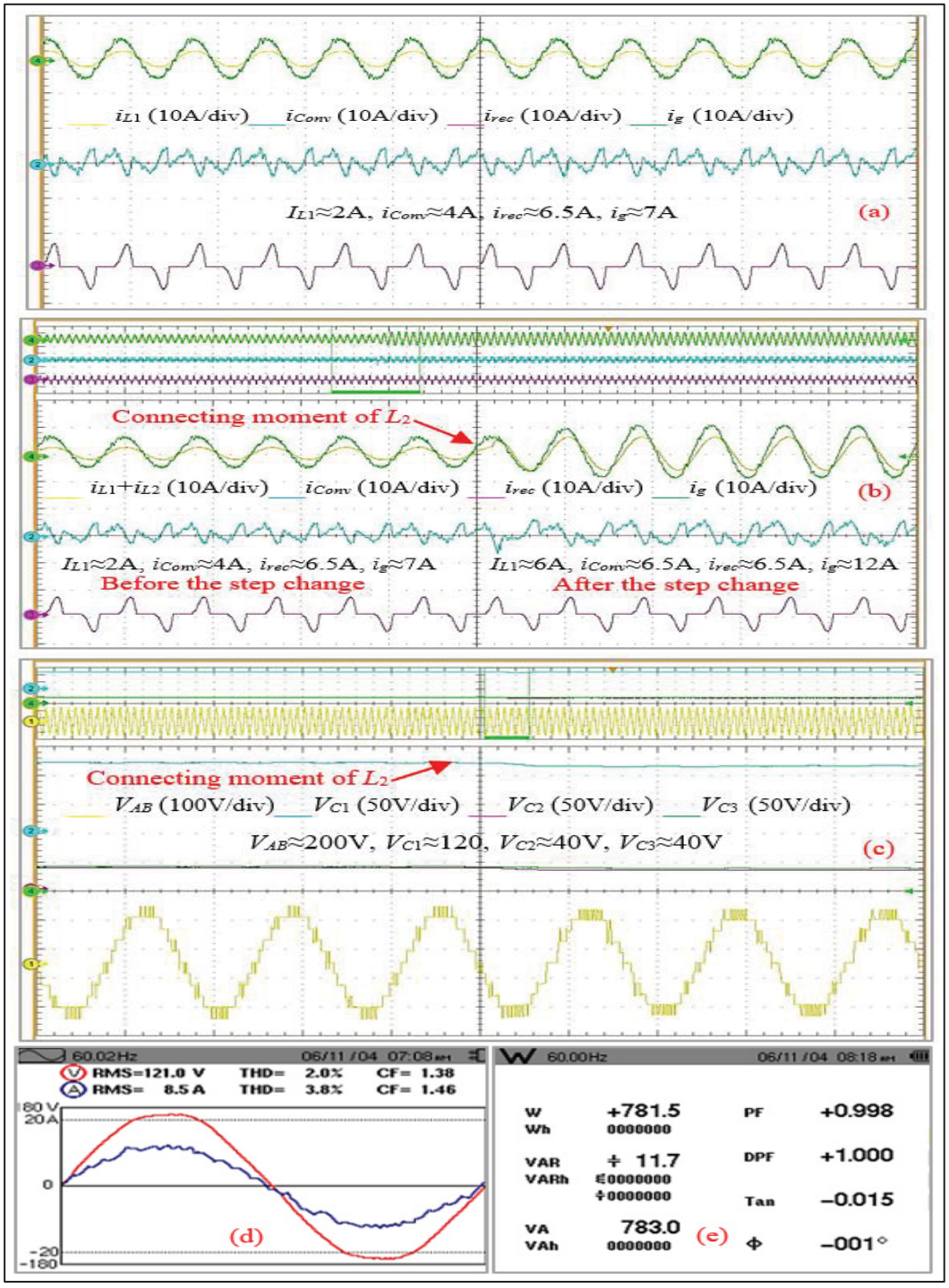

Figure 6.13 Experimental results under a dynamic test (a) current waveforms of the grid, loads, and CAPF in stable condition (b) transient effects on the power system's currents when the second linear load is connected (c) the dc voltages and 11-level waveform in the transient (d) post-transient THD analysis of the grid (e) post-transient power quality analysis of the grid

Fault tolerance and the voltage level switching mode operation of the CAPF have been investigated during the experiments, and the corresponding results are presented in Figure 6.14 and Figure 6.15. Figure 6.14(a) and Figure 6.14(b) respectively depict the pre/post fault performance of the converter without and with a fault detector. The corresponding power quality analysis in Figure 6.14(c) and Figure 6.14(d) indicate a low THD level and acceptable power factor regardless of generating a symmetrical or asymmetrical post-fault multilevel voltage waveform. The experimental results in Figure 6.14 and Figure 6.15 demonstrate the VLSM performance of the BPEC. The VLSM illustrates the flexibility of the BPEC to generate different voltage levels in the event of a fault. The fault tolerance studies presented in this paper are based on two scenarios; in the first scenario, the fault detector is disabled and the results in Figure 6.14(a) show that BPEC decreases the voltage levels from 11 to 7, where the new voltage waveform is asymmetrical. In the second scenario, a fault detector is used, where the corresponding results in Figure 6.14 (b), and Figure 6.15 (a) demonstrate that the BPEC can adjust the voltage levels to 9, 7, or 5 regarding the design concerns related to power quality, voltage stress, and DC link voltages.

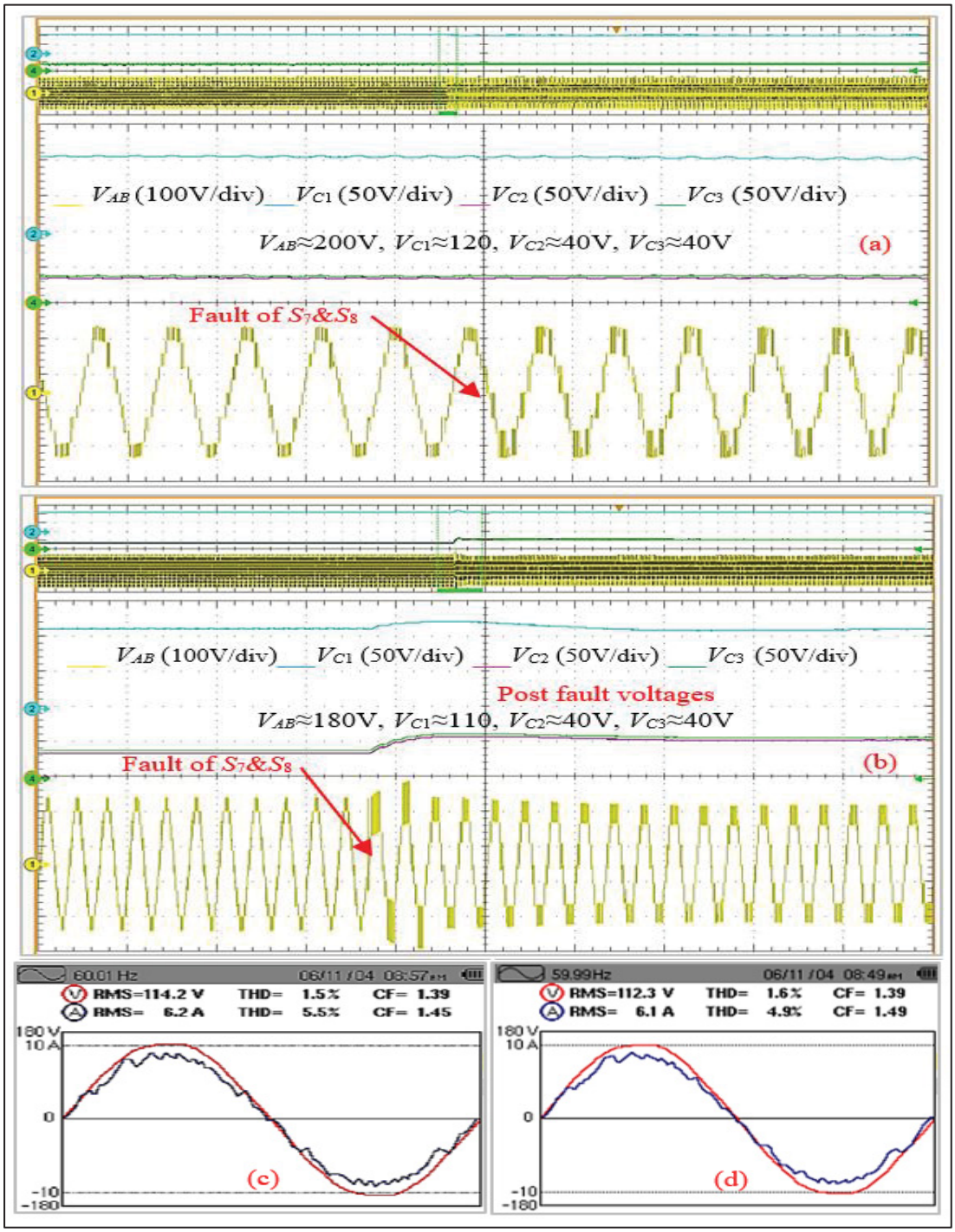

Figure 6.14 Fault tolerance performance of the CAPF (a) asymmetrical post-fault 7-level waveform without using a fault detector (b) symmetrical post-fault 7-level waveform using a fault detector (c) THD analysis of the grid after the asymmetrical post-fault event (d) THD analysis of the grid after the symmetrical post-fault event

It is important to note that the THD level in Figure 6.14 (c) and Figure 6.15 (c) is above the standard level. However, it can be compensated by slightly increasing the grid filter size.
The following test results in Figure 6.16 show the robust performance of the PLL in dealing with the dynamic conditions of the grid in terms of voltage variations.

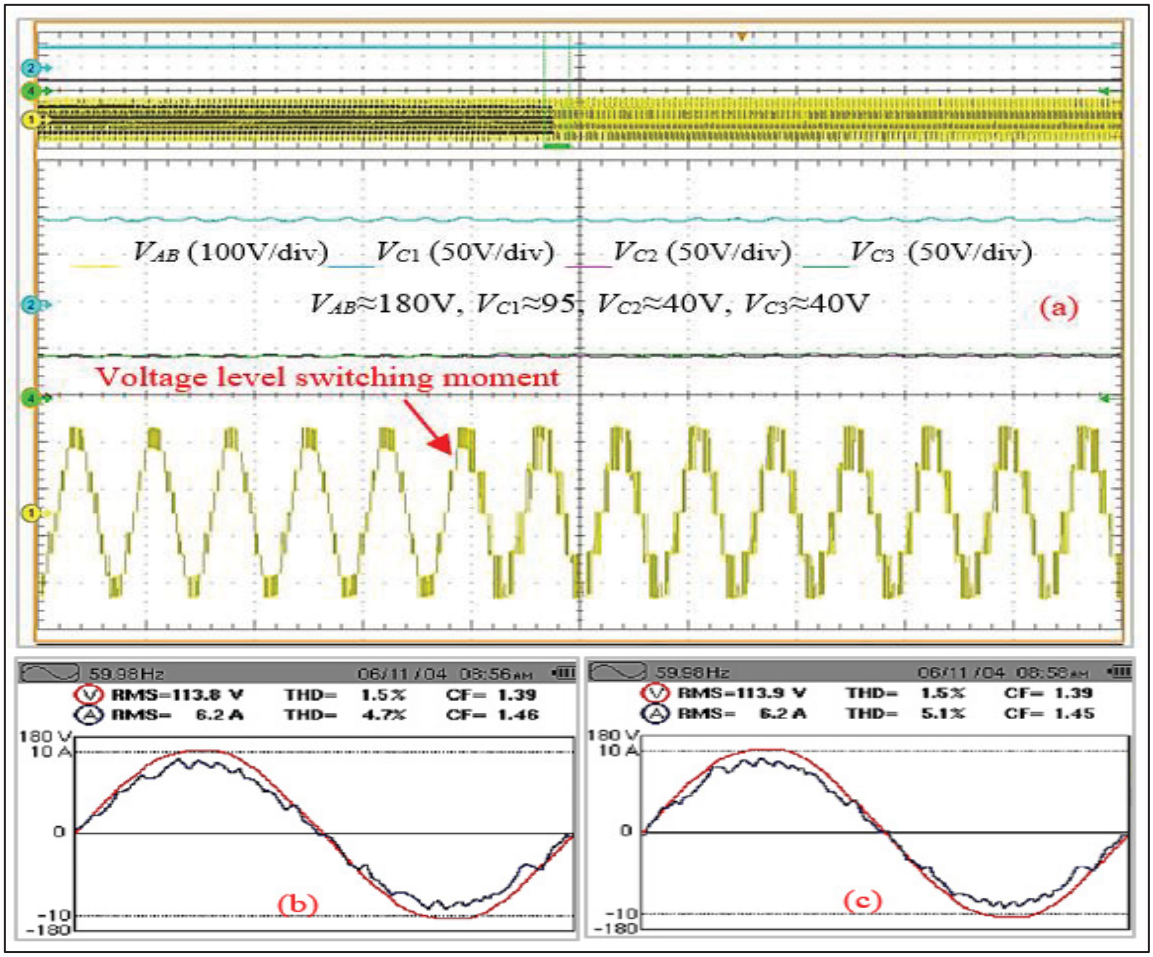

Figure 6.15 Voltage level switching mode performance of the CAPF (a) from 9-level to 5-level (b) THD analysis of the grid for the 9-level mode of operation (c) THD analysis of the grid for the 5-level mode of operation

In this test, the grid voltage suddenly is stepped down from 170V to 120V; the corresponding simulation results in Figure 6.16 show that the whole power system including the multilevel voltage, the capacitor voltages, and the load/grid currents are adjusted based on the new grid voltage amplitude after few cycles, without causing any damaging transient effect.

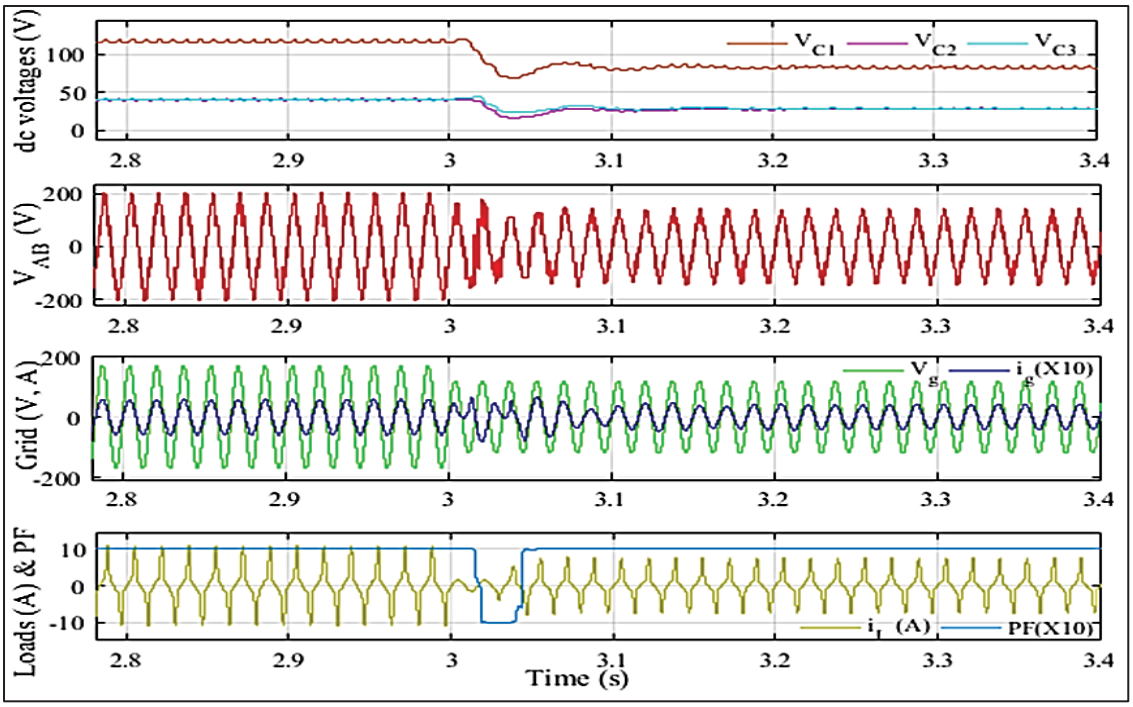

Figure 6.16 Performance of the CAPF including the controller and PLL under the grid voltage drop from 170V to 120V

The power factor (PF) analysis in Figure 6.16 also indicates the stable performance of the CAPF under the grid voltage oscillations after a short transient effect. For comparison with conventional PEC in the APF mode of operation, the proposed BPEC is configured based on the grid conditions (V_g=220V, f_{h1}=50Hz) provided by (Zafari et al., 2021). The corresponding simulation results for the BPEC-based CAPF with the same grid conditions of PEC in Figure 6.17 depict that V_m needs to be 150V, which is 2.66 times lower than the DC voltage (V_m=400V) that was used for conventional PEC-based APF in (Zafari et al., 2021). The second DC link voltage (V_{eq}) in the BPEC-based CAPF is 100V, which is two times lower than the equivalent voltage of the second DC link (200V) in the PEC-based APF. Despite the conventional topology proposed in (Zafari et al., 2021), the modified BPEC benefits a capacitor in the first dc-link instead of an active DC source, which is less expensive. In conclusion, it can be stated that BPEC as a passive converter is more suitable for PQASs. It should be noted that the PF and the grid current are magnified by 10 in Figure 6.16 and Figure 6.17 to present the details.

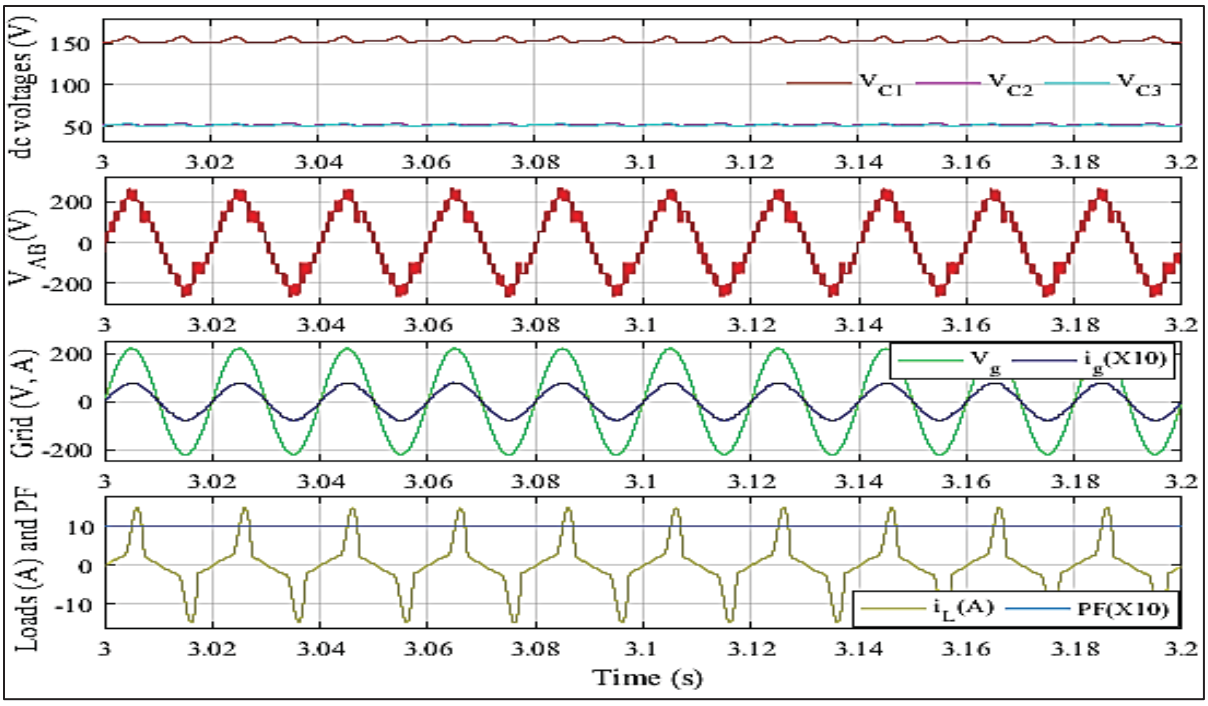

Figure 6.17 Comparative results of testing the CAPF with grid conditions provided for an APF designed based on the conventional PEC converter

6.5 Conclusion

This paper practically and theoretically demonstrated that compact multilevel boost converters are ideal for power-quality ancillary services. According to the technical discussions, comparisons, and literature review provided in this paper, the proposed boost packed E-cell (BPEC) as a compact multilevel topology is suitable for FACTS and APF applications due to low harmonic distortion, boost performance, minimum components, low voltage DC links, low voltage stress, fault tolerance, voltage level switching mode, and small size filter. These features represent BPEC as an affordable and reliable converter. The experimental results practically validated these merits in the CAPF case study. Further improvements in terms of the capacitors' volume, THD, and switching operation could be achieved by optimizing the control loop structure. The improvements will be considered as future work for different applications.

CONCLUSION

The renewable energy industry overview demonstrates the essential contribution of power electronics to the future of energy on a global scale. The fundamental footprint of power electronics, especially DC-AC and AC-DC converters is also observed in domestic, industrial, medical, military, and space environments. Accordingly, power electronics technology has been continuously developed in terms of electronics, topology, control, and application to meet the needs of efficiency, reliability, density, flexibility, and power quality. The comprehensive literature review revealed that developing more effective controllers and topologies is a priority since all the aforementioned design and performance requirements are directly affected. Concerning these priorities, the multilevel concept has become appealing as practical implementations in academia and industry confirm its promising performance. Compared with conventional two-level converters, the multilevel ones, especially CMLCs, such as PUC, MPUC, PEC, and VLMM, can remarkably improve power quality, density, and conversion efficiency. Nonetheless, it has been shown that MLCs suffer from controllability issues caused by their variable structure behavior, floating capacitors, and the limited number of redundant switching vectors. Besides the controllability problems, the lack of boost performance in most MLCs also restricts their applications, especially for renewable energy integration, fast chargers, and power quality ancillary services. To address the controllability issues, various linear, nonlinear, intelligent, and hybrid control algorithms have been reported in the literature, where the majority emphasized the effectiveness of the multi-objective control concept as the best solution to achieve the desired efficiency, dynamic response, resilience, and reliability. From state of the art, one is also concluded that the multi-objective control algorithms require substantial research and development of design, tuning, training, performance, stability, and robustness for future MLCs where the structural complexity, disturbances, uncertainties, and natural instability severely challenge conventional control algorithms.

Following the previous efforts and respecting the merits and drawbacks of existing multilevel converter topologies as well as control algorithms, this thesis has first introduced a robust sliding mode controller to address the voltage-balancing issue of the PUC7 converter in grid-

tied and stand-alone modes. Despite the existing linear and hybrid MPC-based controllers, it has been demonstrated that without involving a voltage controller, the auxiliary DC link voltage of the PUC7 can be self-balanced using the proposed multi-objective, robust OSMC technique. However, involving more objectives in the control equations of the OSMC complicates the Lyapunov-based stability analysis and the design of the equivalent control law since discontinuous functions appear between the DC link voltages and the output current. Accordingly, the focus was switched to control algorithms with much more multi-objective capability, like MPC and ANN. However, the literature review revealed that MPC and ANN suffer from the exhausting tuning/training of the weighting factors and the lack of stability proof, which limits their multi-objective functionality, especially in the case of MLCs since there is a discontinuous nonlinear correlation between dynamics. Thus, in the next step, the intelligent tuning of the weighing factors using the ABC algorithm has been introduced for conventional MPC to control the load power, capacitors' voltages, and CMV for a three-phase stand-alone NPC converter. Further contributions in terms of the stability and online tuning using ANN have been delivered, where the implementation results of applying the resulted controller to the MPUC7 active rectifier confirmed that online tuning of the weighing factors remarkably makes MPC flexible so that multiple control objectives can be involved in the cost function without imposing any tuning difficulties. This outstanding achievement is because of the unique unsupervised training developed for ANNs using metaheuristic algorithms. The stability of MPC has been successfully addressed by developing a discontinuous, decoupled Lyapunov function with zero effect on the control performance. Since PSO is a single-core optimization algorithm, it may be deceived by a local minimum solution; under this situation, the trained ANN cannot meet the expected performance. Thus, several training rounds may be required as PSO is sensitive to the initial parameters. Consequently, this thesis has also developed a novel multi-core, unsupervised training strategy based on the ICA algorithm to accelerate the self-training of ANNs. Thanks to the proposed multi-core training strategy, IPMOC as a mature multi-objective controller, including a novel, online harmonic mitigation objective, has been introduced to provide power quality ancillary services for the grid using a transformerless three-phase NPC converter. The corresponding implementation results proved that a single power converter supported by a mature multi-objective controller completes

multiple tasks expected to be realized using more converters. In the end, the 11-level BPEC topology has been introduced to expand the applications of CMLCs to power quality ancillary services since lower DC links are required to generate higher voltage levels on the PCC side. Combining BPEC and IPMOC leads to an ideal CMLC with power quality ancillary services for single-phase applications.

The fundamental conclusions of the six main chapters of this thesis are briefly highlighted as follows:

In CHAPTER 1, a comprehensive literature review of MLCs, CMLCs, and their control algorithms has been performed. This review demonstrated that applications of multilevel converters have significantly increased in the last decades, especially because of the global attention to renewable energy sources and EVs. The development of MLCs is toward introducing compact topologies with higher resolution and power density. These converters generate higher voltage resolution using floating DC links with minimum possible switches and passive components. Nonetheless, MLCs, especially CMLCs suffer from controllability issues due to the lack of switching redundancy and variable structure dynamic behavior. Accordingly, a significant portion of research in power electronics has been dedicated to developing advanced controllers, like SMC, backstepping, Lyapunov, MPC, ANN, Fuzzy, and their combinations, as hybrid control strategies to enhance the robustness, stability, efficiency, and reliability of MLCs as well as CMLCs. From the overview of advanced controllers, it can be concluded that advanced multi-objective control algorithms are essential for the contribution of MLCs and CMLCs in the future of power electronics. The most successful multi-objective controllers have been constructed based on MPC and ANN; even so, these controllers are severely challenged by tuning, training, and stability issues. Therefore, research and development on the multi-objective control concept with respect to the new topologies of MLCs and CMLCs is always an open problem and needs a special focus.

CHAPTER 2 has been dedicated to addressing the voltage stability problem of PUC7, which is known as one of the most cost-effective single-phase CMLCs. Indeed, the literature review revealed that PUC7 is a benchmark to challenge the multi-objective controllers since its

auxiliary DC link voltage is unstable due to the lack of switching redundancy. The design of the OSMC in this thesis proved that it is possible to regulate the capacitor's voltage of PUC7 without using a voltage controller. This remarkable achievement is because of the natural switching operation of SMC, which inherently allows the converter to switch between the charging and discharging modes of the capacitor. Accordingly, the proposed OSMC is suitable for sensorless voltage balancing of capacitors in CMLCs. Even so, developing a multi-objective controller with SMC is difficult due to the complexity of the equivalent control law and stability analysis in the presence of multiple objectives. Therefore, MPC is recommended for control problems with several control objectives.

Concerning the tuning difficulties of MPC, which becomes exhausting for multi-objective control of MLCs and CMLCs, CHAPTER 3 has proposed an intelligent tuning strategy based on the ABC algorithm. This technique allows MPC to be easily tuned regardless of the number of weighting factors and control objectives. The implementation results of the proposed offline tuning algorithm practically demonstrated the effectiveness of metaheuristic algorithms in resolving the tuning difficulties of the MPC weighting factors. Nevertheless, the effectiveness of the offline tuning of the weighting factors is challenged under parametric mismatch or disturbances since the initial training conditions are invalid. Accordingly, it is recommended to use online training strategies for applications in which the system parameters may change or be exposed to uncertainties and disturbances.

CHAPTER 4, as one of the essential parts of this dissertation, has contributed to addressing the stability and online tuning of MPC besides proposing a novel unsupervised training strategy for ANNs applied to power electronic applications. The implementation results confirmed that using ANNs is a promising solution to enhance the robustness and effectiveness of MPC, as a model-based controller, in dealing with model uncertainties and parametric mismatches. From this chapter, it is also concluded that MPC inherently provides bounded input and bounded output stability. However, thanks to the decoupled stability objective, an asymptotic form of stability can be provided by MPC while it has the minimum impact on the optimal performance of the controller. In addition, it has been shown that since the developed online training strategy

requires no training data, it is much faster and more accurate than conventional supervised algorithms. These unique features of the proposed unsupervised training strategy make it ideal for power electronic control problems since data acquisition is exhausting due to the many parameters, variable structure behavior, environmental disturbances, and limitations to measuring some dynamics. Even so, the proposed PSO-based unsupervised training strategy is sensitive to the initial parameters because of using a single search engine.

Following CHAPTER 4, a new multi-core fast self-training strategy (FSTS) has been introduced in CHAPTER 5 to improve the accuracy and convergence time of the previous PSO-based unsupervised algorithm. Thanks to the multi-core search engine provided by the ICA algorithm, the proposed FSTS can run on commercial computers, which is ideal for researchers with limited equipment. For the first time in the literature, an intelligent predictive multi-objective control strategy was introduced based on the FSTS training algorithm, which can appropriately track eight different control objectives. It has also been shown that a grid-tied renewable energy-based converter supported by the IPMOC method is able to intelligently provide autonomous power ancillary services for the grid, which results in a simplified demand response and energy management system for smart grids. In addition, the proposed online selective harmonic mitigation algorithm allows MPC control algorithms to mimic the harmonic mitigation performance of SHM modulators with much more flexibility for grid-connected applications. Regarding the CMLC concept, the voltage ripple analysis also demonstrated that by targeting the low-order harmonics, especially the third one using the SHMO, smaller capacitors can be used in the DC link of MLCs.

Eventually, a new boost CMLC topology has been introduced in CHAPTER 6 for power quality ancillary services. It has been shown that the proposed BPEC topology is highly compatible with STATCOMs, APFs, and electric springs because of low harmonic distortion, boost performance, compact size, small DC links, low voltage stress, and fault tolerance. Accordingly, a detailed design for a compact active power filter (CAPF) using the proposed BPEC and a multi-objective controller has been provided. The design and analysis of the CAPF have comprehensively covered the most important aspects, including switching sequences,

fault tolerance, components selection, controllability challenges, hardware implementation, and practical evaluations under various test scenarios. The implementation results in this chapter also confirmed that the promising performance of CMLCs highly depends on multi-objective control algorithms.

RECOMMENDATIONS

Although this dissertation has successfully met its key objectives, paving the road for CMLCs and advanced multi-objective controllers toward real-life applications requires years of research conducted by many researchers in well-equipped laboratories. In this regard, the following ideas have been eventuated as future works.

Self-Voltage Balancing of CMLCs Equipped with Serial DC Link Capacitors using the Optimized Sliding Mode Control Theory

The test results in CHAPTER 2 demonstrated the capability of the OSMC algorithm to regulate the voltage of the floating capacitor in the PUC7 converter. The proposed OSMC is not limited to PUC7, as it can be generalized to fulfill a similar self-voltage balancing performance for the other CMLCs. Indeed, the sensorless control of DC link voltages using the OSMC technique is possible for CMLCs in which the capacitors are installed in series. Accordingly, future work will investigate the sensorless control of more floating capacitors for more advanced CMLC topologies, such as PEC, BPEC, and VLMM.

Lyapunov Stability Analysis for MPC-based Multi-Objective Controllers with Non-Singular Prediction Horizon

As shown in CHAPTER 3, CHAPTER 4, and CHAPTER 5, and also concluded from the literature review, model predictive control is ideal for multi-objective control of MLCs and CMLCs. Even so, the applied MPC algorithms suffer from a lack of analytical stability analysis. Regarding, a decoupled stability objective has been introduced in CHAPTER 4 for the floating weighting factor MPC algorithm, which has been developed for the MPUC7 active rectifier. The proposed stability objective is designed based on the predicted values of the state variables in the next sampling period. Thus, developing an advanced stability objective, including multiple prediction steps of the Lyapunov function, is required for multi-objective

MPC-based algorithms with non-singular prediction horizons. This goal is considered an independent future work since extensive research and analysis should be accomplished.

Online Selective Harmonic Mitigation using Model Predictive Control for Compact Multilevel Converters

Compact multilevel converters, such as PUC, PEC, and VLMM, suffer from the bulky size of the floating capacitors in high-power applications because the load current directly flows through all DC links with different voltage levels. On one hand, the voltage ripple analysis in CHAPTER 5 proved that the voltage ripple is directly related to the low-order harmonics of the current, especially the third one. On the other hand, in CHAPTER 5, it has been shown that the size of the DC link capacitors can be reduced by 38% with a similar switching frequency when the third-order harmonic has been mitigated by 80%. Consequently, the constructive impact of the proposed online selective harmonic mitigation (SHMO) technique on CMPLCs can be further investigated to reduce the size of the floating capacitors.

APPENDIX I

Voltage Ripple Analysis for the Self-Voltage Balancing Operation of the Seven-Level Packed U-Cell Converter

The voltage ripple of the floating capacitor in PUC7 depends on several parameters, such as the capacitor's capacitance, load current, switching operation of S_2 and S_3, and intervals of PWM pulses (switching frequency and sampling time). The dynamic of the capacitor's current is obtained by combining two terms of (2.12) as below:

$$C \frac{dV_C}{dt} = (S_3 - S_2) i_o \tag{A I-1}$$

where C is the size of the floating capacitor, V_C is the capacitor's voltage, S_2 and S_3 are the switching variables, and i_o is the output current of the converter. Equation (A I-1) can be rewritten as (A I-2) to calculate the capacitor's voltage.

$$V_C = \int \frac{(S_3 - S_2)}{C} i_o dt \tag{A I-2}$$

i_o can be estimated based on the input DC voltage (V_{dc}) and load impedance (Z) using (A I-3).

$$i_o = \frac{V_{dc}}{Z} \sin\left(\omega t\right) \tag{A I-3}$$

Substituting (A I-3) into Eq. (A I-2) leads to a new definition of the capacitor's voltage without involving the load current dynamic.

$$V_C = \int \frac{(S_3 - S_2)}{C} \left(\frac{V_{dc}}{Z}\right) \sin\left(\omega t\right) dt \tag{A I-4}$$

The capacitor's voltage variations can be formulated if the states of S_3 and S_2 are determined for a complete cycle of the seven-level voltage waveform.

To simplify the calculation for the capacitor's voltage dynamic, a fundamental seven-level voltage waveform depicted in Figure-A I-1 is presumed and the states of both S_3 and S_2 are selected according to Table 2-1.

As observed in the voltage levels 0 and $\pm V_{dc}$, both switches are on; thus, the integral of (A I-4) is zero. For the voltage levels $\pm 1/3 V_{dc}$ and $\pm 2/3 V_{dc}$, one of the switches is on and the integral of (A I-4) is non-zero. Considering Figure-A I-1, the capacitor's voltage is extended as (A I-5) based on the switching angles (α_1-α_3).

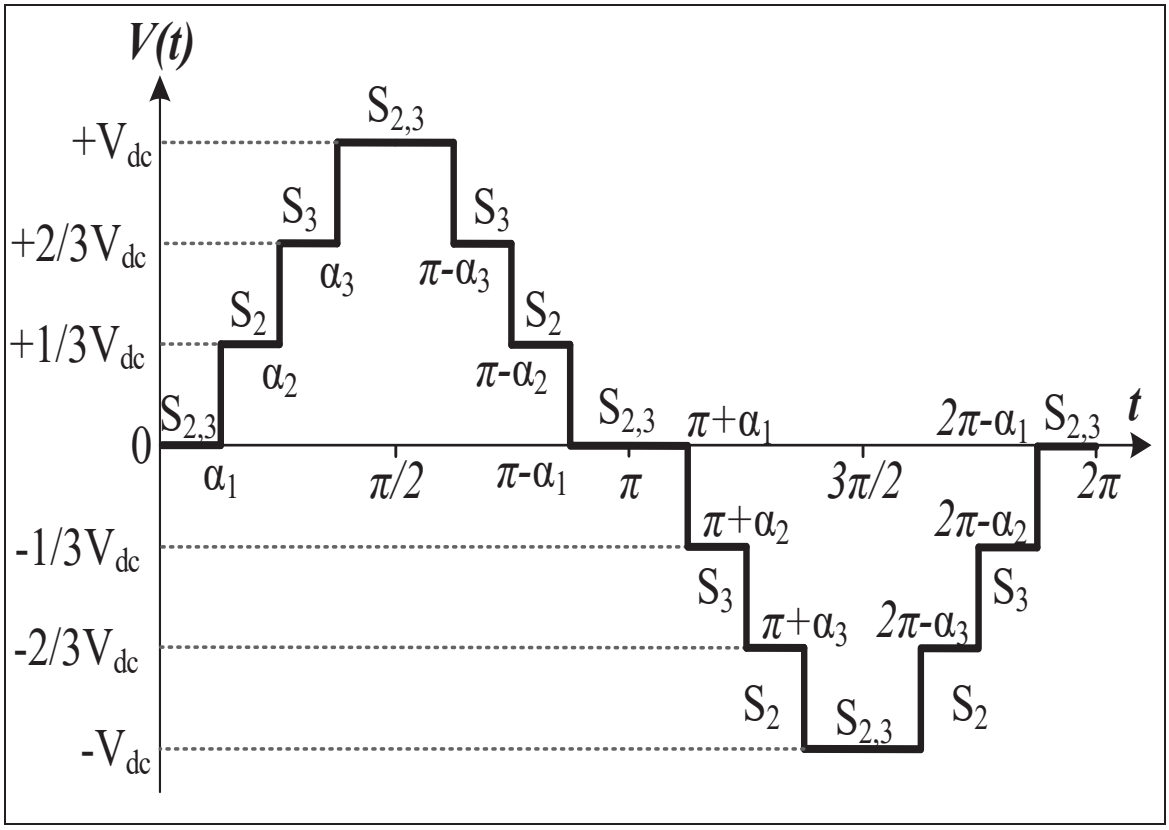

Figure-A I-1 Generalized fundamental seven-level voltage waveform

$$V_C = \left(\frac{V_{dc}}{ZC} \right) \left[\begin{array}{l} \int_{\alpha_1}^{\alpha_3} \sin(\omega t) + \int_{\pi-\alpha 3}^{\pi-\alpha_1} \sin(\omega t) + \int_{\pi+\alpha_1}^{\pi+\alpha_3} \sin(\omega t) \\ + \int_{2\pi-\alpha 3}^{2\pi-\alpha_1} \sin(\omega t) \end{array} \right] d\,\omega t \qquad \text{(A I-5)}$$

Eventually, the capacitor's voltage, including the voltage ripple for a fundamental seven-level voltage waveform, is calculated as shown in (A I-6).

$$V_C = \left(\frac{V_{dc}}{ZC} \right) \left[\begin{array}{l} \left(\cos(\alpha_1) - \cos(\alpha_3) \right) + \left(\cos(\pi-\alpha_3) - \cos(\pi-\alpha_1) \right) \\ + \left(\cos(\pi+\alpha_1) - \cos(\pi+\alpha_3) + \left(\begin{array}{l} \cos(2\pi-\alpha 3) \\ -\cos(2\pi-\alpha_1) \end{array} \right) \right) \end{array} \right] \qquad \text{(A I-6)}$$

As the switching frequency increases, more pulses emerge in the seven-level voltage waveform so that the trigonometric part of the capacitor's voltage changes according to the number of pulses.

Therefore, by increasing the switching frequency and designing a proper control technique, the charging and discharging modes of the capacitor can be controlled to balance the capacitor's voltage at the desired level with minimum ripple. Regarding (Abarzadeh, Vahedi, & Al-Haddad, 2019), since the switching pulses in the proposed OSMC are generated by the conventional SPWM technique, the voltage ripple can be modeled as below:

$$\Delta V_C = \frac{(S_3 - S_2) i_o}{2 f_0 C} \qquad \text{(A I-7)}$$

Equation (A I-7) reveals that the voltage ripple is affected by the capacitor's size (C), switching operation of S_2, S_3, load current (i_o), and fundamental frequency of the system (f_0).

Since the load current and fundamental frequency depend on the load characteristics, the controllability of the voltage ripple in (A I-7) is restricted to the switching operation of S_2 and

S_3. Considering the system parameters provided in Table 2.2 and assuming that the voltage ripple should be less than 5% while the peak amplitude of load current is constantly injected into the load without controlling the switching operation of S_3 and S_2, the capacitor size is calculated using (A I-8) as 25mF (in the worst case scenario), which is huge.

$$C = \frac{(S_3 - S_2)i_o}{2f_0\Delta V_C} \tag{A I-8}$$

Even so, it can be proved that the voltage ripple in the OSMC technique is suppressed. Regarding this, let's assume that the capacitor voltage error (e_{VC}) is defined as (A I-9).

$$e_{VC} = V_C - V_C^* \tag{A I-9}$$

where V^*_C is the desired voltage level, which should be one-third of the DC source amplitude. Using (2.12), the derivative of (A I-9) is calculated as below:

$$\dot{e}_{VC} = \frac{1}{C}\, ui_o \tag{A I-10}$$

As shown in (A I-10) the capacitor's voltage ripple is controlled by u, which is the switching operation of S_2 and S_3. Therefore, the derivative of the voltage ripple defined in (A I-10) is extended as (A I-11) by using both generalized control laws of (2.16) and (2.19).

Equation (A I-11) confirms that the capacitor's voltage ripple is controlled by the generalized control laws of the OSMC developed for grid-connected and stand-alone modes. The experimental and simulation results also illustrate that the voltage ripple is significantly suppressed so that the capacitor's size has been reduced from 25mF to 2.2mF with T_S=80μs in experimental tests and from 25mF to 900μF with T_S=25μs in simulation tests.

$$\begin{cases} \dot{e}_{VC-G} = \dfrac{1}{C}\left(\dfrac{1}{V_{dc}}\left(R_f i_o + V_G + L_f \dfrac{di_d}{dt}\right) - \lambda_G sgn\ (S)\right) i_o \\ \dot{e}_{VC-S} = \dfrac{1}{C}\left(\dfrac{1}{V_{dc}}\left(Z^* i_o + L_L \dfrac{di_d}{dt}\right) - \lambda_S sgn\ (S)\right) i_o \end{cases} \quad \text{(A I-11)}$$

To reduce the capacitor size, the SPWM modulator proposed by (Abarzadeh, Vahedi, & Al-Haddad, 2019) can be used instead of the conventional one. Equation (A I-12) shows that since the switching frequency (f_{sw}) emerges in the capacitor's voltage ripple instead of f_0, the capacitor's size can be further shrunk by increasing f_{sw}.

$$\Delta V_C = \frac{(S_3 - S_2) i_o}{2 f_{sw} C} \quad \text{(A I-12)}$$

According to (A I-12) the capacitor's size for PUC7 with V_{dc}=210V, V_g=170V, i_o=10A, and f_{sw}=20kHz is calculated as 93.8μF. The simulation results of this test for the grid-connected PUC7 are shown in Figure-A I-2. As depicted, the capacitor's voltage is desirably balanced to one-third of the DC source with a voltage ripple of less than 5%, the seven-level voltage is symmetrically generated and the grid voltage and inverter current are precisely synchronized.

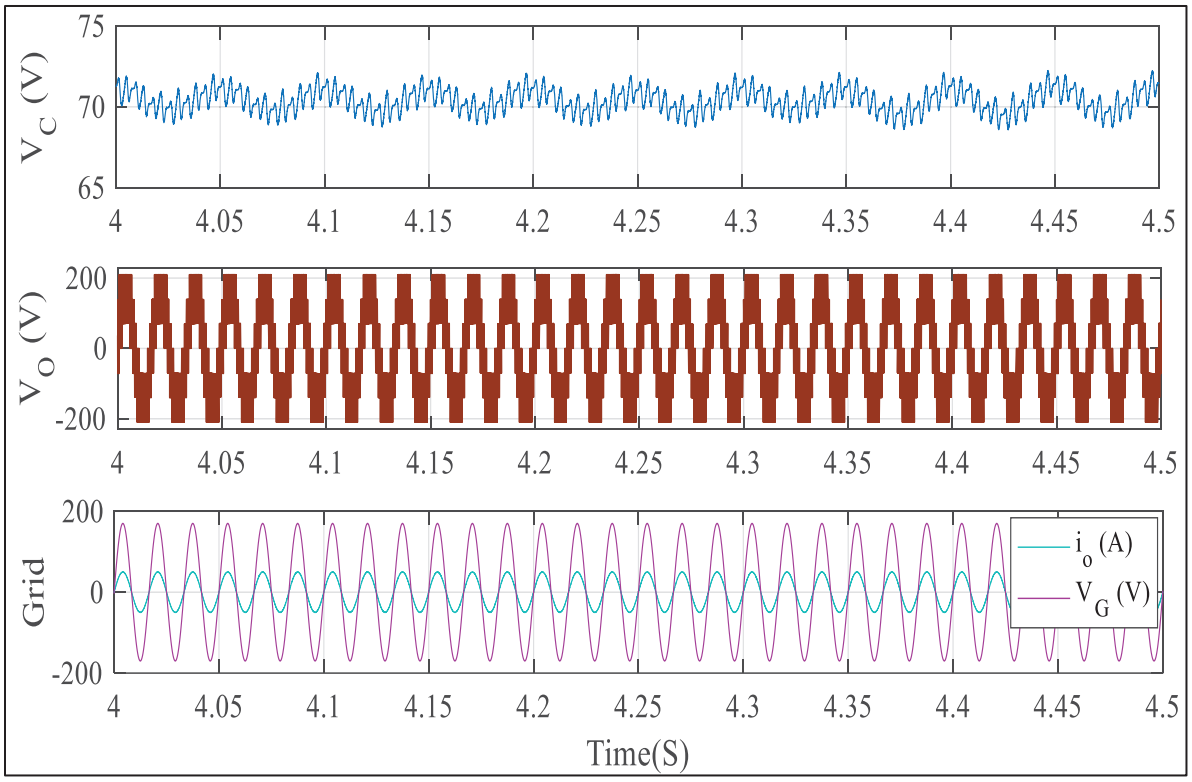

Figure-A I-2 Simulation results of the grid-connected PUC7 for C=100µF and f_{sw}=20kHz

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