GHz-range Characterization and Modeling of Power Integrity in SiP for an Array of Switch-Mode Converters

by

Gabriel NOBERT

THESIS PRESENTED TO ÉCOLE DE TECHNOLOGIE SUPÉRIEURE
IN PARTIAL FULFILLMENT FOR THE DEGREE OF
DOCTOR OF PHILOSOPHY
Ph.D.

MONTREAL, APRIL 10TH, 2024

ÉCOLE DE TECHNOLOGIE SUPÉRIEURE
UNIVERSITÉ DU QUÉBEC

BOARD OF EXAMINERS

THIS THESIS HAS BEEN EVALUATED

BY THE FOLLOWING BOARD OF EXAMINERS

M. Yves Blaquière, Thesis Supervisor
Department of Electrical Engineering, ÉTS

M. Nicolas Constantin, Thesis Co-Supervisor
Department of Electrical Engineering, ÉTS

M. Christian Belleau, Chair, Board of Examiners
Department of Mechanical Engineering, ÉTS

M. Handy Fortin-Blanchette, Member of the Jury
Department of Electrical Engineering, ÉTS

M. Boris Vaisband, External Independent Examiner
Department of Electrical and Computer Engineering, McGill University

THIS THESIS WAS PRESENTED AND DEFENDED

IN THE PRESENCE OF A BOARD OF EXAMINERS AND THE PUBLIC

ON MARCH 19TH, 2024

AT ÉCOLE DE TECHNOLOGIE SUPÉRIEURE

ACKNOWLEDGEMENTS

I want to thank my colleagues from the CPIOS project, without whom there wouldn't have been such a success within the entire team. Thank you to everyone who have contributed to that success: Abdul-Hafiz Alameh, Abdurrashid Shuaibu, Allan Riboullet, Hamid Sadrimanesh, Nam Ly, Nurahmed Omar, Reyhaneh Taherpour, Sudabeh Fotoohi, Tan Pham and Van-Ha Nguyen. I also want to thank the professors involved in the CPIOS project for their kind words and occasional support. You have made this project a success and we, the students, wouldn't have been as successful without you. Aside from my advisor and co-advisor, I would like to specifically thank professors Frédéric Nabki and Glenn Cowan.

J'aimerais remercier chaque personne ayant rendu la rédaction de cette thèse possible. Il y a une quantité inombrable de gens qui ont eu un impact de près ou de loin sur mes travaux et je vous dis tous sincèrement: merci. Plus spécifiquement, merci au laboratoire LACIME et à Normand Gravel, qui a su m'aiguiller dans l'utilisation des équipements nécessaires et me donner de précieux conseils techniques qui m'ont permis de mener à bien mes mesures. Merci également à Mathieu Gratuze: non seulement pour son support immense d'un point de vue technique et en design de banc de mesures, mais également pour avoir été un ami durant toute la durée de mon doctorat. Merci pour toutes les discussions, techniques ou non. Merci à mes anciens et présents collègues du LACIME que j'appelle aujourd'hui mes amis: David Berthiaume, Smarjeet Sharma, Ilshat Shagitov, et encore une fois, Tan Pham et Mathieu Gratuze. Vous avez rendu mon temps à l'ÉTS plus agréable et pour cela, je vous en remercie. Merci aux techniciens du département de Génie Électrique. Plus spécifiquement merci à André Zalzal, Rigoberto Avelar, Jorge Rojas Abad et Youssef Bekbouti pour leur support et leur aide dans mes différentes fabrications et assemblages qui étaient nécessaires à ma recherche. Finalement, je dois remercier mon directeur ainsi que co-directeur: les professeurs Yves Blaquière et Nicolas Constantin. Vos précieux conseils, techniques et en matière de recherche, ont fait de moi un meilleur chercheur et un meilleur concepteur. Je vous serai toujours reconnaissant pour la chance que vous m'avez donnée de compléter un doctorat sous votre supervision.

Caractérisation et modélisation à plusieurs GHz de l'intégrité de la puissance dans un SiP pour une matrice de convertisseurs à commutation

Gabriel NOBERT

RÉSUMÉ

La tendance à la miniaturisation s'est répandue dans une grande variété de circuits. Dans cette perspective, il est nécessaire d'intégrer de manière plus compacte des circuits électroniques de puissance et des convertisseurs à commutation (*switch-mode converter*). Conséquemment, le concept de *Configurable Power Input and Output System* (CPIOS) fut introduit dans le cadre de cette recherche. Ce système intègre sur un même substrat une matrice de convertisseurs à commutation, des circuits analogiques sensibles pour la commande et des capteurs. De nouveaux défis en intégrité de la puissance surgissent alors. En effet, l'activité de commutation du convertisseur génère du bruit sur les rails d'alimentation du CPIOS, affectant du même coup les performances des circuits sensibles. Il est nécessaire de prédire les fluctuations de tension générées par la commutation simultannée des convertisseurs, en termes d'amplitude crête, de forme temporelle et de densité spectrale de puissance, sur ces circuits plus sensibles afin d'évaluer la dégradation des performances. Il y a également un besoin de modèle d'intégrité de la puissance (*power integrity*) qui prédit la forme des fluctuations de tension sur les circuits sensibles dans une matrice de convertisseurs commutant simultanément. De plus, plusieurs convertisseurs peuvent commuter simultanément dans le CPIOS, augmentant la complexité de la prédiction de ce bruit. La caractérisation du courant est également importante pour évaluer l'intégrité de la puissance, car c'est le principal mécanisme de génération de bruit. Par conséquent, il existe également un besoin pour une technique de mesure de courant intégrée avec des provisions minimales pour les mesures et une bande passa4nte supérieure comparativement aux techniques proposées dans la litérature.

L'objectif principal de cette recherche est de modéliser les contraintes d'intégrité de la puissance dans le CPIOS en fonction des différentes conditions de fonctionnement et d'une caractérisation du système. Le premier objectif spécifique est de caractériser le courant de commutation dans les convertisseurs de puissance pour le CPIOS, qui est crucial pour prédire l'intégrité de l'énergie avec une large bande passante. Pour ce faire, une technique de mesure de courant basée sur une ligne de transmission au secondaire d'une structure inductive est proposée. Une analyse du comportement de la structure montre que sa distorsion de mesure (*measurement distortion*) peut être prédite jusqu'à plusieurs GHz et que le point de mesure peut être placé à n'importe quel endroit pratique sur le substrat sans affecter la distorsion de mesure. Les mesures avec la structure proposée, validées avec la technique connue de résistance série, montrent que le courant dans un convertisseur à commutation peut être caractérisé jusqu'à 1,95 GHz avec une distorsion de mesure inférieure à 3 dB. Ces résultats représentent une amélioration par rapport à l'état de l'art en termes de fréquence et de facilité d'intégration de la technique de mesure de courant. Le deuxième objectif spécifique est de prédire les fluctuations sur les rails d'alimentation des circuits sensibles, en termes de forme temporelle et de densité spectrale de puissance. Ainsi, un modèle pour l'intégrité de la puissance et pour prédire les fluctuations de tension pendant

la commutation simultanée des convertisseurs sur les rails d'alimentation est présenté. Pour chaque condition mesurée, une précision meilleure que 10 dB est obtenue entre 0 et 2 GHz, en comparant un signal de référence mesuré et les prédictions, lorsque les fluctuations causées par un ou plusieurs convertisseurs sont mesurées. En termes de forme temporelle, l'erreur quadratique moyenne normalisée par la variance (NMSE) est dans le pire des cas de 0,624 et, dans de nombreuses conditions, meilleure que 0,25. Ce modèle est le premier en son genre à prédire jusqu'à plusieurs GHz l'intégrité de la puissance dans le contexte des convertisseurs de puissance.

Mots-clés: Convertisseur à Commutation, Intégrité de la Puissance, SiP, Système-dans-un-boîtier

GHz-range Characterization and Modeling of Power Integrity in SiP for an Array of Switch-Mode Converters

Gabriel NOBERT

ABSTRACT

The trend of miniaturization has been spread to a vast variety of circuits. Among those, there is a need to integrate in a more compact way power electronic circuits and switch-mode converters. Accordingly, the concept of Configurable Power Input and Output System (CPIOS) is introduced. Such a system integrates into the same compact substrate switch-mode converters, sensitive analog circuits for control and readback together. That type of system brings new challenges in terms of power integrity. Indeed, the switching activity from the switch-mode converters generate noise onto the power rails of the CPIOS, thereby impeding the performances of the more sensitive circuits. There is a need to predict voltage fluctuations generated by the switching activity of one or multiple converters switching simultaneously onto those more sensitive circuits, in terms of shape, peak amplitude and power spectral density, in order to assess the degradation of the performances. Moreover, multiple converters may switch simultaneously in CPIOS, increasing the complexity of predicting that noise. Furthermore, the characterization of the current is equally important in order to assess power integrity due to it being the main noise generation mechanism. Therefore, there is also a need for embedded current measurement technique with minimal required on-board provisions and a bandwidth better than available from the state-of-the-art techniques.

The main objective of this research is to model power integrity constraints in CPIOS based on the different operating conditions and a thorough characterization of the system. The first specific objective is to characterize the switching currents in power converters for the CPIOS, which are critical for predicting power integrity with high bandwidth. Accordingly, a transmission-line-based current measurement technique is proposed. A thorough analytical formulation of the behavior of the structure shows that its measurement distortion can be predicted at up to multiple GHz and that the probing pad can be placed at any convenient location on the substrate without affecting measurement distortion. Measurements with the transmission-line-based structure validated with the well-known resistive shunt technique show that the current in a switch-mode converter can be characterized at up to 1.95 GHz with less than 3 dB measurement distortion. Such results are an improvement over the state of the art in terms of frequency, compactness and ease of implementation of the embedded technique. The second specific objective is to predict fluctuations onto the power rails of sensitive circuits, in terms of shape and energy spectrum. For that purpose, a model for power integrity and voltage fluctuations during simultaneous switching of the converters on power rails is presented. For every condition validated, accuracy better than 10 dB is obtained between 0 and 2 GHz by comparing a measured reference signal and predictions when the fluctuations caused by a single or multiple converters are measured. In terms of overall shape, the variance-normalized mean squared error (NMSE) in the worst case is of 0.624 and under numerous conditions better than 0.25. This model is the first of its kind to predict power integrity in the context of power converters at up to multiple GHz.

Keywords: Switch-Mode Converter, Power Integrity, SiP, System-in-Package

TABLE OF CONTENTS

Page

LIST OF TABLES

Page

LIST OF FIGURES

LIST OF ABBREVIATIONS

AC	Alternating Current
ADC	Analog-to-Digital Converters
BNC	Bayonet Neill–Concelman
BTL	Bridge-Tied Load
CCM	Continuous Conduction Mode
CGD	Configurable Gate Driver
CM	Common-Mode
CMOS	Complementary Metal-Oxide-Semiconductor
CPIOS	Configurable Power Input/Output System
CSP	Current Surface Probes
CSR	Coaxial Shunt Resistors
DC	Direct Current
DM	Differential-Mode
DFT	Discrete Fourier Transform
DPT	Double-Pulse Test
DUT	Device Under Test
EM	ElectroMagnetic
EMC	ElectroMagnetic Compatibility
EMI	ElectroMagnetic Interference

ENOB	Effective Number Of Bits
ÉTS	École de Technologie Supérieure
FET	Field-Effect Transistor
FPGA	Field-Programmable Gate Array
GaN HEMT	Gallium Nitride High-Electron Mobility Transistor
GTM	General Terminal Modeling
GSG	Ground-Signal-Ground
IBIS	Input/output Buffer Information Specification
IC	Integrated Circuits
LTCC	Low-Temperature Co-fired Ceramics
LISN	Line Impedance Stabilization Network
LTI	Linear Time-Invariant
MEMS	MicroElectroMechanical Switch
MOSFET	Metal Oxide Silicon Field-Effect Transistor
NMOS	N-type Metal-Oxide-Semiconductor
NMSE	Variance-Normalized Mean-Squared Error
PCB	Printed Circuit Board
PDN	Power Distribution Network
PEEC	Partial Element Equivalent Circuit
PI	Power Integrity

PMOS	P-type Metal-Oxide-Semiconductor
PPP	Plane-Pair PEEC
PWM	Pulse-Width Modulation
RF	RadioFrequency
RMS	Root Mean Square
SI	Signal Integrity
SiC	Silicon Carbide
SiP	System-in-Package
SMD	Surface-Mount Device
SOIC	Small-Outline Integrated Circuit
SOLT	Short-Open-Load-Through
SPICE	Simulation Program with Integrated Circuit Emphasis
SSN	Simultaneous Switching Noise
THD	Total Harmonic Distortion
TLM	Transmission-line-matrix
VNA	Vector Network Analyzer
WBG	Wide-Band-Gap

LIST OF SYMBOLS AND UNITS OF MEASUREMENTS

A	Ampere
dec	Decade (of frequency)
dB	Decibel
°	Degree
F	Farad
H	Henry
Hz	Hertz
m	Meter
%	Percent
Ω	Ohm
rad	Radian
s	Second
mil	Thousandths of an inch
V	Volt

INTRODUCTION

0.1 Context and motivation for this work: Configurable Power Input/Output System (CPIOS)

In safety-critical automotive, avionic and even in industrial applications, highly reliable electronic systems are used in the control of independent and critical loads, such as high- and low-voltage sensors and actuators. Those sensors and actuators have several requirements in terms of functionality, reliability, configurability and redundancy. For the control of sensors and actuators, not only is the power stage important, but also the read-out circuits. It is important to integrate flexible and accurate read-out in the form of analog-to-digital converters (ADC) and signal conditioning circuits for, as an example, either closed-loop operations of the actuators or conversion of analog signals from the sensors to digital signals in decision-making processes. Those control and decision-making processes are typically taken care of by a digital system such as a field-programmable gate array (FPGA) or microcontroller. That digital system needs to be protected from the high-power domain of the different loads and sensors typically through digital isolators. Such a safety-critical system, with the main blocks described above, is depicted in Figure 0.1.

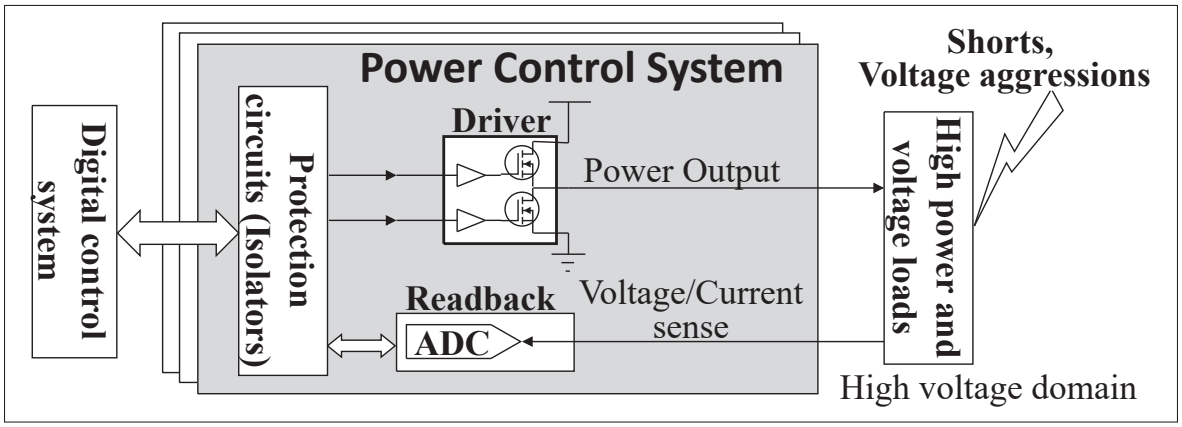

Figure 0.1 System-Level depiction of a safety-critical system

In those applications, reliability is of the utmost importance because human safety is at play. In addition, there is a need to control a variety of loads that range from servo-electric motors and electromechanical systems to driving and reading active sensors, among others. It is therefore practical, in such systems, to have a level of configurability that allows the independent switching converters and amplifiers to be used in a wide range of applications. Finally, due to the need for reliability, redundancy is also important. In addition, adding more converters within a small area helps reduce the size and weight of the overall system. These systems commonly employ electronic modules that are assembled on PCBs for the implementation of switching converter-based power stages with discrete power devices and readback stages using ADC.

There is a need to reduce the size and weight of those subsystems. One of the ways this can be done is through system-in-package (SiP) integration. Accordingly, a configurable power SiP with read-out and power circuits, i.e., a configurable power input and output system (CPIOS), is presented in this thesis.

The power circuits are switch-mode converters with configurable dead times and gate driver strength, where multiple types of power transistors can be used due to a flexible board footprint. A read-out block allows sensing and conversion of analog voltages or currents in loads to the digital domain. The system therefore supports multiple digital control loops for power converter circuits. The digital isolators protect external control circuits against common-mode transients and faulty signal lines between the digital control system and the power domain.

That CPIOS system is the main application in this work and motivates the need for the GHz-range linear modeling of power integrity and the current measurement technique presented in this thesis.

0.2 The challenge of Power Integrity in CPIOS

As mentioned previously, the CPIOS features an array of switch-mode converters integrated alongside more sensitive circuits such as ADC and operational amplifiers for signal conditioning (Figure 0.2). As noise-generating circuits such as those switch-mode converters, are integrated closer to sensitive analog and mixed-mode circuits, the power supply noise coupled to those analog devices increases in magnitude, which in turn affects their performance (Bae *et al.*, 2013). In the literature, power integrity is typically defined as the study of the quality of the supply rails in terms of voltage level and noise on the supply rails. More specifically with CPIOS, the main concern is that the noise generated by the switch-mode converter will either affect other converters, or the sensitive circuits in the form of voltage fluctuations on the power rails. The research question studied in this thesis is the following: *what is an accurate way to assess power integrity in systems that integrate power converters with more sensitive analog and mixed-mode circuits, e.g., CPIOS?*

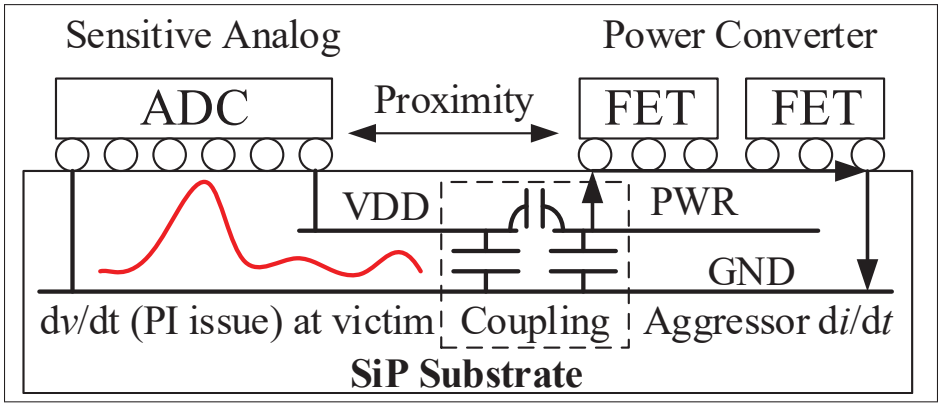

Figure 0.2 Problem of Power Integrity in CPIOS

0.2.1 Modeling Power Integrity in CPIOS

In CPIOS, there is an array of switch-mode converters operating independently. However, integrating multiple switching converters together will exacerbate that switching noise onto

the sensitive analog and mixed-mode circuits. In specific systems that integrate an array of independent switching converters, such as in CPIOS, simultaneous switching of those converters may lead to increased peak voltage fluctuations onto the power rails of sensitive devices. Those switching converters may switch simultaneously or at relative times (referred to as *timing conditions*) short enough that the effect of the current pulled by two independent converters on a victim node overlap each other (*simultaneous switching*). They may also be switching with different strengths (*gate driving conditions*), and load currents (*loading conditions*). All those factors affect the fluctuations generated onto the different power domains of the SiP when the array of converter switches. Predicting those fluctuations both in time and frequency domains under this variety of conditions is of importance in order to assess power integrity (PI) constraints and take appropriate design decisions. Indeed, due to the plurality of conditions, a system-level designer that uses the CPIOS with given timing, gate driving and loading conditions needs to be able to predict by how much it will affect the behavior of, for instance, the control or the noise on the power output of the converters. By being able to predict those fluctuations, it becomes possible to avoid situations where the noise levels exceed the acceptable thresholds in terms of peak level and spectral density.

Those fluctuations could be predicted, in a more generic way, through a mix of circuit-level and electromagnetic simulations. However, for various reasons, it is not an ideal solution in configurable systems. The power transistors, which are simulated through time-domain analysis, are non-linear devices that operate in various operating regions in a converter during switching: cut-off (*off state*), saturation and triode (*on state*). Furthermore, electromagnetic simulations are done in order to accurately model the behavior of the power distribution network (PDN). The result of those electromagnetic simulations can either be an equivalent RLCG network such as with ANSYS Q3D Extractor (ANSYS, 2022) or an S-parameter network, with most tools for EM modeling. In either case, the simulations of the non-linear power transistors need to be augmented with those PDN models and be simulated through, for instance, SPICE-like

simulations (for RLCG network PDN models) or transient and convolution simulations (Keysight, 2022b) for PDN defined as a function of frequency such as with S-parameter network PDN models. It is known in the state-of-the-art that power electronic circuit simulations are prone to convergence problems during switching events and are time-consuming (Tan, 2017). Therefore, augmenting the simulation of multiple switching power devices with complex PDN, having it converge, and be of short duration is challenging even to the seasoned designer. With a large variety of conditions to simulate it becomes a time-consuming task that needs to be repeated even for small design changes if the simulations even converge. For those reasons, a behavioral-model-based approach that requires a one-time characterization with no convergence issue is preferable. Therefore, *there is a need for a model that predicts the voltage fluctuations onto sensitive nodes, specifically for power converters operating under a range of conditions and switching simultaneously*.

0.2.2 GHz-range Current Measurement technique for CPIOS

It is the current transients ($\mathrm{d}i/\mathrm{d}t$) drawn by the power converters that generates the noise on the power rails. For that reason, in order to assess power integrity in the CPIOS, it is critical that the current is properly measured when switching of the converter occurs. Furthermore, for power applications operating at high-voltage levels, transistors that offer a better trade-off between gate charge, i.e., Q_{G} in typical power field-effect transistor (FET) data sheets, dimensions and power handling capabilities are required. For that purpose, devices such as gallium nitride high-electron mobility transistors (GaN HEMT) and silicon carbide (SiC) metal oxide silicon field-effect transistor (MOSFET) are preferred. On such devices, the gate charge is significantly reduced, hence switching times are reduced compared to a silicon device of similar power handling capabilities (Saito *et al.*, 2007). In a specific case, a switching time of less than a nanosecond was reached (Simonaitis *et al.*, 2021). On the other hand, the shorter switching times and smaller output capacitance increase the bandwidth of the switching current transient

to a point where characterizing switching noise in the GHz range may be required. In this context, the measurements of currents at GHz range in switching converters are key to allow the characterization of PI in SiP power electronics systems that combine switching converters and sensitive analog and mixed-mode circuits.

Aside from the bandwidth requirements, it is also critical that the technique is suited for compact power electronics SiP implementations with minimal on-board overhead for probing provisions and low losses in order to assess PI constraints. Indeed, as will be explained in the literature review, while there exist current measurement techniques with high bandwidth, those are based on a resistive shunt, which significantly affect either circuit dimensions or losses and current-handling capabilities. Therefore, *there is a need for a current measurement technique in the GHz range that is suitable for high current levels and specifically for power integrity application in highly integrated systems*.

0.3 Research Objectives

In light of the previous sections, the following main research objective is pursued: *To model power integrity constraints in CPIOS based on diverse operating conditions and a thorough characterization of the system*. More specifically, the following objectives are pursued:

(O1) To characterize the switching current in power converters for the CPIOS, which are critical for power integrity with high bandwidth.

(O2) To predict fluctuations onto the power rails of sensitive circuits, in terms of shape and energy spectrum.

The state-of-the-art is reviewed in the following sections and sub-specific objectives are also derived to assess if each of those objectives are met.

0.4 Key Contributions to State-of-the-Art

This thesis is based on two major contributions, which both have been submitted to scientific journals as well as a conference paper, presented at the International Symposium on Circuits and Systems (ISCAS 2021). The first journal paper, which was accepted, introduces a GHz-range current measurement technique suited for high-density integration.

- Nobert, G., Constantin, N. G. & Blaquière, Y. (2023). A Coupled Transmission-Line-Based Measurement Technique for Currents in Switch-Mode Converters. IEEE Transactions on Electromagnetic Compatibility, 65(5), 1535-1547. doi: 10.1109/TEMC.2023.3300988.

The second contribution, which was submitted for publication in October 2023, is a model for the prediction of supply rail voltage fluctuations under a range of operating conditions in an array of simultaneously switching power converters.

- Nobert, G., Constantin, N. G. & Blaquière, Y. (submitted for publication in IEEE Transactions on Electromagnetic Compatiblity, October 2023). GHz-range Linear Modeling of Power Integrity in an Array of Simultaneously Switching Power Converters.

In the conference paper, the general idea of the CPIOS system is presented along with the analysis of integration technologies and early design constraints: density, self-heating, losses and signal integrity.

- Nobert, G., Alameh, A.-H., Ly, N., Constantin, N. G. & Blaquière, Y. (2021). *Towards an LTCC SiP for Control System in Safety-Critical Applications*. 2021 IEEE International Symposium on Circuits and Systems (ISCAS), pp. 1-5. doi:10.1109/ISCAS51556.2021.9401066.

The following contributions were made for that paper:

- a novel system-level architecture for a CPIOS;
- a comparison between integration technologies is presented for different aspects: density, self-heating, losses and signal integrity for CPIOS;

- three techniques to take advantage of LTCC capabilities: a multi-layer routing technique to circumvent the issue of thin conductors with limited thermal and electrical conductivity.

0.5 Organization of the Thesis

Chapter 1 of this thesis is a review of the state-of-the-art regarding the challenges discussed in the introduction. The different techniques for current sensing in power converters, both based on shunt resistors and mutual inductance are presented along with their main drawbacks. A review of the different methods in the state-of-the-art for the prediction of voltage fluctuations are then presented. The techniques in digital systems for power integrity assessment are first presented, followed by electromagnetic interference (EMI) prediction techniques in power converters.

Chapter 2 of this thesis further introduces the challenges of current measurement techniques as well as power integrity in CPIOS. Simulations and numerical applications are presented in order to motivate the need for power integrity assessment and current measurement in the GHz range.

Chapter 3 presents a GHz-range, high-current measurement technique suited for high-density SiP integration. The technique is first introduced and analyzed. Then the experimental measurement apparatus is described and experimental results as well as the main findings are presented.

Chapter 4 presents a model for the prediction of supply rail voltage fluctuations under a range of operating conditions in an array of simultaneously switching power converters. The model is first presented and analyzed. A system with multiple power converters switching simultaneously is then presented, together with the necessary setup to measure one of the sensitive nodes. The predictions made by the model are compared with experimental measurements and conclusions are drawn. The conclusion chapter explores the different outlooks for the research presented in this thesis.

CHAPTER 1

LITERATURE REVIEW: GHZ-RANGE FREQUENCIES POWER INTEGRITY ASSESSMENT AND CURRENT MEASUREMENT TECHNIQUES

This chapter presents the different state-of-the-art techniques for the measurement of the current in switch-mode converters. Then, the techniques used for the assessment of power integrity in SiP are introduced. The section is based on, with extracts from, the first two sections of (Nobert, Constantin & Blaquière, 2023) and (Nobert, Constantin & Blaquière, submitted for publication) as well as the conference paper (Nobert *et al.*, 2021).

1.1 High-Frequency Current Measurement Techniques

As presented in the introduction, there is a need for a GHz-range current measurement technique applicable to switch-mode converters for power integrity applications in converters based on the use of fast-switching devices such as GaN HEMT and SiC transistors, which allow more compact power systems as needed in SiP. The power integrity characterization at GHz range in SiP of such components leads to some specific requirements in terms of bandwidth, level of integration and current limitations, which are not addressed in state-of-the-art techniques.

The techniques proposed so far in the literature are divided into three different categories in this review:

- Resistive shunt sensing: this category includes the use of surface-mount device (SMD) shunt resistors and coaxial shunt resistors;
- Inductor-based: this category includes mutual-inductance techniques such as pickup coils. It also includes Rogowski coils, which can be integrated on PCB, commercial current transformers and current-surface probes;
- Hall effect sensors: this category includes techniques based on the sensing of magnetic fields through the Hall effect.

1.1.1 Resistive Shunt Sensing and its Limitations

Small shunt resistors can address the problem of characterizing the switching current in power converters for the CPIOS, which are critical for power integrity with high bandwidth. When using shunt-resistor-based techniques, a resistor is placed in series with the current flow (I_1) to measure this current as a voltage (V_2) through the IR drop of the shunt resistor. It can be represented by the equivalent circuit of Figure 1.1(a). There are two main types of resistors that are used for such a purpose: SMD resistors and coaxial shunt resistors.

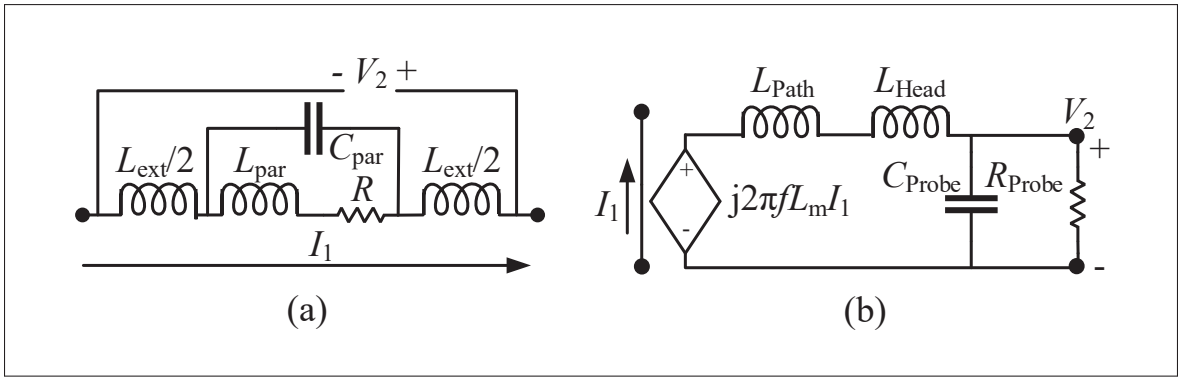

Figure 1.1 Two-port model of two current measurement techniques: (a) resistive shunt technique and (b) mutual inductance-based technique
Taken and adapted from Wang *et al.* (2018, p. 6203)

1.1.1.1 SMD Shunt Resistors

The SMD resistors are, for current sensing applications, either based on a thin metal film or a thin resistive film. In either case, the film is printed on top of a ceramic substrate and terminations on both sides of the resistor allow the connection to a PCB through soldering. The SMD shunt resistor has the advantage of being low-cost. However, a trade-off has to be made between size, bandwidth and current-handling capabilities. Indeed, the larger the SMD resistor package, the greater its equivalent lead inductances (L_{ext} and L_{par}). Consequently, the bandwidth of the current measurement decreases (Vishay Intertechnology, Inc., 2009). Smaller packages have fewer parasitics, which results in a larger bandwidth, but at the expense of lower power-handling capabilities, leading to current limitations in the converter.

In order to circumvent that problem of trade-off between parasitics and current-handling capabilities, multiple SMD shunt resistors can be put in a parallel configuration (Shillaber, Jiang, Ran & Long, 2022), reducing the parasitic inductance of the resistor network while increasing current-handling capability due to having less current in each individual SMD resistor. However, as depicted in Figure 1.2, which shows the implementation in (Shillaber *et al.*, 2022), the area on a substrate for this technique is larger than that of a single shunt resistor.

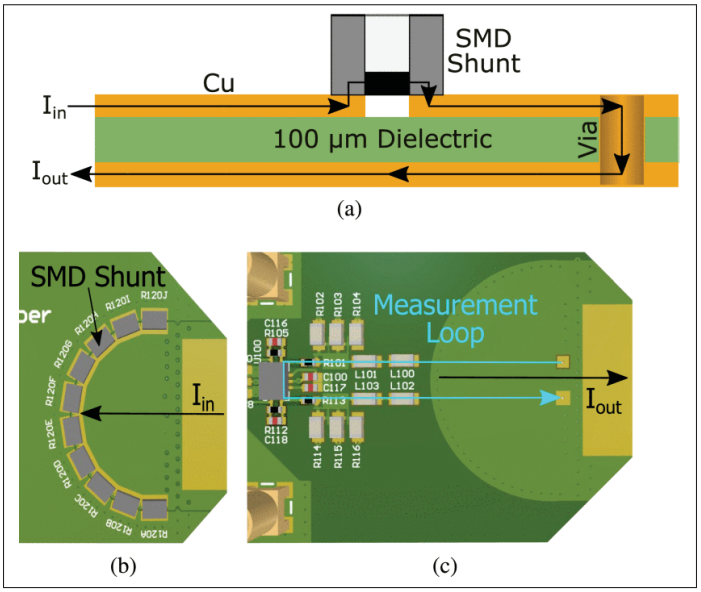

Figure 1.2 Depiction of parallel shunt resistor network: (a) cross-section across a single parallel shunt resistor, (b) top and (c) bottom views
Taken from Shillaber *et al.* (2022)

Another solution to the parasitic inductance of the SMD shunt resistor is to add an LR compensation network in order to mitigate the impact of the parasitic inductances in the SMD resistor (Figure 1.3). However, that LR network requires a large value of series inductance (compensation inductor) in order to properly compensate the parasitic inductance in the shunt resistor. Moreover, larger compensation inductor leads to lower series resonant frequency and thus, bandwidth in those compensation networks is limited. The authors achieve a bandwidth of 85 MHz with such a compensation network (Yang *et al.*, 2020).

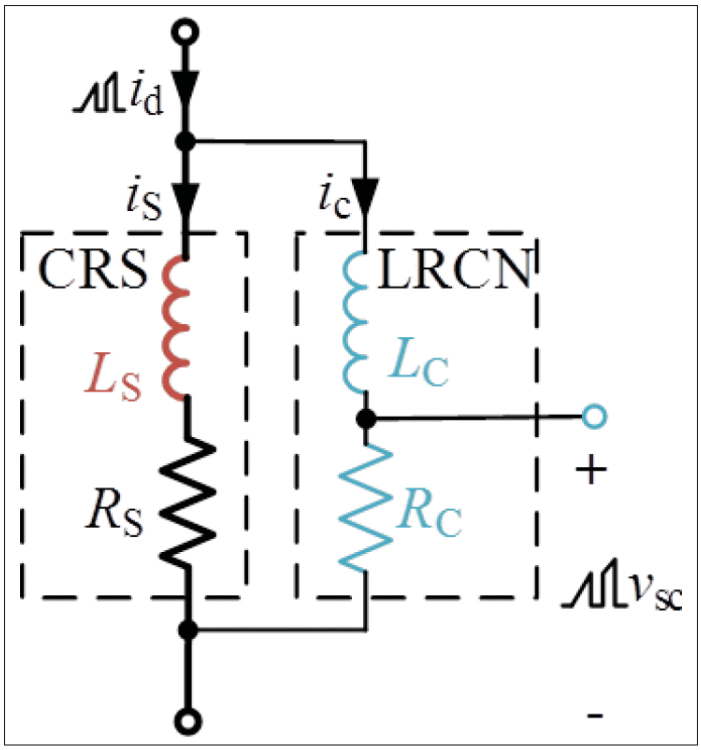

Figure 1.3 LR Compensation network for high bandwidth current shunt sensing
Taken from Yang *et al.* (2020)

1.1.1.2 Coaxial Shunt Resistors

Coaxial shunt resistors (CSR) improve the current-handling capabilities and bandwidth trade-off with SMD shunt resistors. They are resistors that are integrated within a coaxial structure where the inner material is typically a resistive film, while the outer material is a conductive material such as copper. A classical structure of CSR is depicted in Figure 1.4. The coaxial structure has the advantage of canceling magnetic fields and thus not adding significant series inductance when measuring the voltage across the resistive material (Ferreira, Cronje & Relihan, 1992). Therefore, bandwidths reached for CSR are typically higher than their SMD counterparts for similar current-handling capabilities. However, they suffer from disadvantages in terms of size and added inductance to power loop. Indeed, CSR are bulky for SiP applications and are therefore not ideal for integration into smaller systems. They are rather practical in the

characterization of large-area power transistor applications. Those CSR are connected through leads that add significant inductance to the power loop (referred to as *insertion inductance*). In (Liu, Huang, Lee & Li, 2014), the authors used commercial CSR in order to characterize the current in a switch-mode converter in double-pulse test (DPT) configuration. The CSR lead, however, adds a 2 nH insertion inductance, which may affect the behavior of the converter. More recently, leadless surface-mount CSR were implemented in an effort to have lower footprints and insertion inductance.Taking into account the required footprint of the shunt, an inductance of 0.53 nH was obtained (Zhang *et al.*, 2021). While significant insertion inductance reduction was achieved, the size of the CSR is still significant with its diameter being 8.9 mm.

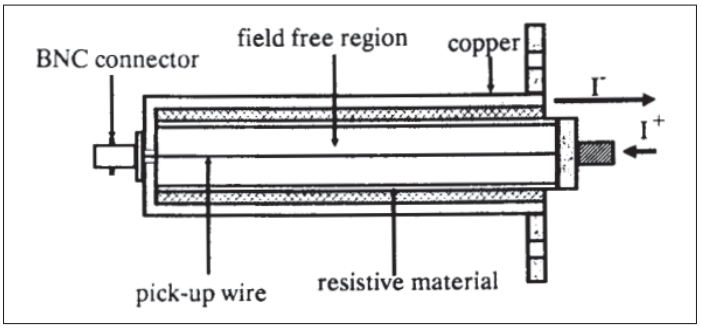

Figure 1.4 Classical structure of coaxial shunt resistors
Taken from Ferreira *et al.* (1992)

It can be concluded for resistive shunt sensing techniques that resistor networks are either too bulky, such as the case in CSR or SMD resistor network, or have limited bandwidth, such as is the case in compensated sense SMD resistors. If a small resistor network or a single small resistor is selected, these limitations are improved at the expense of smaller current-handling.

1.1.2 Inductor-Based Techniques

In inductor-based techniques, the current is measured by capturing its generated magnetic flux. Indeed, in Figure 1.1(b), I_1 is measured, leading to voltage V_2 across the inductor structure. That voltage V_2 is then integrated in order to extract the current I_1. Although still present, the problem of current-handling capabilities observed in resistor-based techniques is significantly reduced

due to the absence of the inherent loss mechanism of shunt resistors, which is proportional to the square of the current. One of the main drawbacks of inductor-based techniques compared to shunt resistor techniques is its inability to measure DC or very low-frequency currents.

1.1.2.1 Current Transformers

In applications where integration level is not critical, current transformers in the form of clamps are commonly used. Those current transformers are typically based on an inductor coil around a toroidal magnetic core. The magnetic flux generated by a current passing through the center of the toroid (*primary*) is coupled into the coil (*secondary*) from which the current can be sensed with a sense resistor. In some cases, the primary may itself be wound onto the core (*wound current transformers*). Commercial probes such as (Pearson Electronics Inc., 2022) have a bandwidth of up to 250 MHz and a maximum root mean square (RMS) current of 10 A. In the case of the Keysight N2783B, a 100 MHz bandwidth is reached with a maximum RMS current of 30 A (Keysight, 2022a). However, current transformers with higher current-handling capabilities typically have bandwidths in the order of tens of kHz to a few MHz. Those bandwidth limitations are typically due to the large leakage inductance and stray capacitance (Kondrath & Kazimierczuk, 2009). In either case, aside from bandwidth limitations, another problem in such current clamps is that they require to pass an electrical cable through the transformer in order to measure the current. Adding a cable passing through the center of the toroid, or a primary winding in the case of wound current transformers, to the power loop increases the insertion inductance by a significant amount, leading to a change to the behavior of the converter when measuring it. In addition, those clamps are not practical, because of their size and the hard-to-integrate magnetic core in the context of SiP. Finally, the magnetic core of current transformers is an issue when magnetic fields become stronger and the core reaches saturation: non-linearity and hysteretic effects occur.

1.1.2.2 Rogowski Coils

Rogowski coils are similar to current transformers, but do not suffer the drawbacks from having a magnetic core. Therefore, they are not subjected to saturation non-linearity and can be integrated on PCB or SiP due to not requiring a magnetic core. Although classically made on a machined circular skeleton (Ramboz, 1996), more modern implementations exist directly on PCB using conductor traces and vias (Shi, Xin, Loh & Blaabjerg, 2020) followed by an integrator circuit. In those implementations, the helical shape of the coil is printed around a via or slot for a cable in the PCB by having traces and vias to alternate between two layers, hence creating a coil shape on PCB, such as depicted in Figure 1.5. According to the coil model of Shi *et al.* (2020), the bandwidth is, however, limited by the self-inductance of the coil and its inductance between the different windings and the current return from the coil. In high-bandwidth Rogowski coils made specifically for wide-band-gap (WBG) transistor characterization (Fritz, Neeb & Doncker, 2015), a bandwidth of 110 MHz and a mutual inductance of 3.89 nH was reached for a 64 mm^2 coil. In (Fritz *et al.*, 2015), the current from the low-side FET located on the bottom layer, to the high-side FET on the top layer is captured with a Rogowski coil around the via. That technique, however, requires a specific layout and the use of a via on the switching node, which increases the power loop inductance in addition to have non-negligible dimensions. In other works, one of the layers of the coil is used as a screen return (Ming *et al.*, 2019) in order to improve the bandwidth of the design and noise immunity. The obtained bandwidth is, however, not reported in the paper.

1.1.2.3 Pickup Coils

As mentioned, the bandwidth of Rogowski coils is mainly limited by the inductive nature of the coil and its stray capacitance. Therefore, shorter coils exhibit superior bandwidths. In (Wang *et al.*, 2018), the authors use a single-winding coil, referred to as a *pickup coil*. Using those pickup coils, superior bandwidth is reached thanks to having negligible stray capacitance and minimal coil self-inductance. In the case of pickup coils, bandwidth is limited by the resonant frequency between the coil self-inductance and the probe capacitance at the output of the coil.

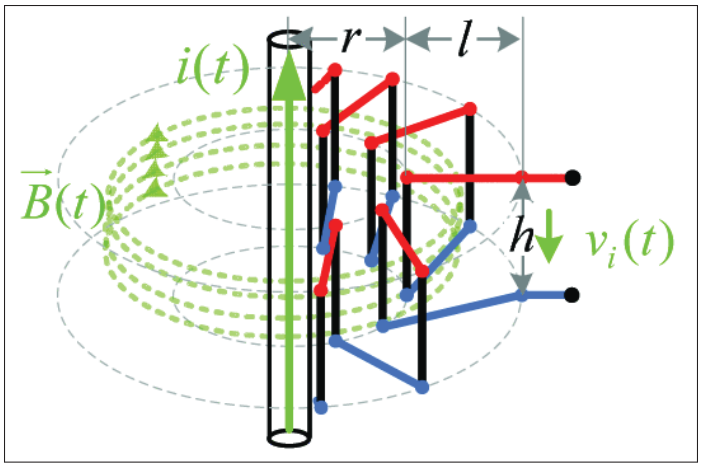

Figure 1.5 Structure of the integrated Rogowski coil on PCB
Taken from Ming *et al.* (2019)

Based on the equivalent circuit for their pickup coil (Figure 1.1(b)) and the data provided in the paper, the bandwidth of their circuit can be estimated to approximately 840 MHz, although that bandwidth is not directly reported, but rather represents a 3 dB deviation from ideal behavior as defined in section 3.1 of this thesis. The pickup coil, however, has several issues. First, the bandwidth of the pickup coil is limited by the probe capacitance and the inductive effects in the probe and the coil. In a context of sub-ns switching times, a GHz-range bandwidth is preferable. In addition, in order to properly probe the coil, the probe must be placed as close as possible to the coil and therefore the converter. A more convenient probing apparatus where the probe could be placed in a safe probing location, meaning where there is no risk of short-circuiting due to mishandling of the probe, is preferable.

1.1.2.4 Current Surface Probe Sensing

One of the main issues with discrete current transformers in the form of clamps and Rogowski coils is that the current carrying trace has to go through a cable and then into the transformer. One of the solutions is to build a current transformer or coil that lies flat on board and would measure the magnetic field generated by a trace: current surface probes (CSP). The CSP would

then be laid flat on the trace that needs to be measured. Using such a probe helps reduce the insertion inductance compared with discrete current transformers and Rogowski coils. However, the probe still has to be laid flat on a componentless area. In the case of SiP or a tightly integrated system, leaving an area without any component may increase the dimensions of the system. In addition, it increases the length of the power loop where the current needs to be characterized. Nevertheless, commercial products such as the Fischer CC F-97-1 have an upper bandwidth of up to 1.5 GHz, while supporting a current of 10 A. In (Li, Videt & Idir, 2015a), the authors use a CSP and a coaxial shunt resistor in order to measure the switching current in a GaN HEMT-based converter. In terms of insertion inductance, they obtain significantly less insertion inductance (4.5 nH) with the CSP compared with a commercial coaxial shunt resistor (14 nH).

In conclusion, with mutual-inductance-based sensing, while it is possible to reach higher bandwidth with minimal losses, there is still an issue of high insertion inductance leading to altered behavior of the converter, because of the overhead required, such as loose cables into a transformer or componentless area for current surface probe sensing. For those same reasons, making measurements of the current often requires a special board design that requires a significant PCB area (e.g., Rogowski coils). While pickup coils partially solve those problems, they are still limited in terms of probing convenience and bandwidth.

1.1.3 Limitations in Hall-Effect Sensors

Hall effect is commonly described as the current flow being deviated when a magnetic field is perpendicular to a conductor plate, hence creating a potential difference across the conductor's cross-section. Hall-effect sensors use that effect in order to measure magnetic fields crossing the conductor, which is the sensor in that case. In current measurement applications, the goal is to measure the magnetic field generated by a direct current (DC), in order to obtain that current. Unlike inductor-based techniques, Hall-effect sensors have the advantage of being able to measure DC. They also do not suffer from the main limitation of shunt resistors, which inherently dissipate power proportional to the current squared. More recently, hall-effect sensors have been integrated in a package (Motz *et al.*, 2012) along with the readout circuit. The authors

manage to achieve a 10 kHz measurement bandwidth and 50 A current-handling capability. In other works, the sensor is integrated directly on an integrated circuits (IC) (Heidari, Bonizzoni, Gatti & Maloberti, 2015) and integrate the sensor and the readout circuit in a 1.16 mm^2 area. However, the main issue of hall-effect sensors is their bandwidth limitation. Indeed, even in integrated applications, a 10 kHz bandwidth is highly insufficient for the CPIOS application. Therefore, while hall-effect sensors allow compact measurement of high currents along with their DC component, they are severely limited in terms of bandwidth and unusable as a current measurement technique in the case of CPIOS.

1.1.4 Conclusion on Current Measurement Techniques

The initial objective for current measurement was to characterize the switching current in power converters for the CPIOS, which are critical for power integrity with high bandwidth. Among the high-frequency current measurement techniques, the ones based on a resistive current shunt present a trade-off between current-handling capabilities, bandwidth and size that is insufficient for the CPIOS application. To solve that problem, an inductance-based solution, such as a current transformer, Rogowski coil, pickup coil or current surface probe sensing could be considered. However, the combination of the probe and inductive secondaries in the case of pickup coils, Rogowski coils and current transformers are limiting the bandwidth of the current measurement structure. Finally, Rogowski coils and current surface probe sensors require significant dimensions either for probing overhead or physical implementation of the coil, which is unfit for the SiP integration of CPIOS. It is therefore necessary to develop a current measurement technique, which doesn't have the limited current-handling capabilities or excessive size of current-shunt resistor. It also needs an improved bandwidth and dimensions compared to inductance-based solutions. Those problems in the literature are summarized in Table 1.1.

Table 1.1 Summary of techniques for switching current measurement

Technique	Description	Drawback
Resitive Shunt Sensing		
SMD Shunt Resistor	Use an SMD shunt resistor alone	Trade-off between bandwidth and current-handling capabilities
	Multiple shunt resistor put in parallel	Requires multiple components Limited Bandwidth
	Use an LR compensation network to improve bandwidth	
Coaxial Shunt Resistor	Coaxial resistor structure to contain magnetic field and limit parasitic inductance	Bulky structure unfit for SiP integration
Inductance-based techniques		
Current Transformers	Capture magnetic flux through a toroidal-shaped inductor coil around magnetic core	Magnetic Core cannot be integrated Limited Bandwidth
Rogowski Coils	Integrated on-board current transformer with no core	Significant Dimensions Limited Bandwidth
Pickup coil	Single-winding Rogowski coil	Limited Bandwidth Probing location must be placed next to the coil itself, and therefore the converter, leading to a complex probing apparatus.
Current-Surface Probe	Current Transformer probe with no core and that lies flat on the board	Requires special layout and large area without components or traces on the substrate, which is unfit for SiP integration
Other Techniques		
Hall-effect sensors	Use the Hall Effect to measure current both at DC and higher frequencies.	Limited bandwidth;

1.2 Techniques for Power Integrity Assessment in System-in-Package

Power integrity PI assessment is of critical importance in SiP. More specifically, there is a need for a model that predicts the voltage fluctuations onto sensitive nodes for a range of conditions under which a converter switches. There are two separate fields of study that are of interest for that challenge: PI in digital systems and electromagnetic compatibility in power systems.

1.2.1 Simultaneous Switching Noise and Power Distribution Network in Digital Systems

In the field of PI in digital systems, so-called simultaneous switching noise (SSN) is the main mechanism that generates voltage fluctuations on the power rails of more sensitive IC such as operational amplifiers, ADC and even other digital circuits. The voltage fluctuations generated by SSN propagate through the different coupling mechanisms and power planes in the PDN, such as depicted in Figure 1.6. Those voltage fluctuations can affect the behavior of operational amplifiers (Shim *et al.*, 2009), the effective number of bits (ENOB) of ADC (Bae *et al.*, 2013) and even the clock jitter (Tripathi *et al.*, 2016) among other metrics (Wen, Cai & Zhuo, 2021) in digital circuits. Although the aggressor source in the CPIOS is not a digital IC, but rather the current transient generated by the switching of different power converters, the switching characteristics of power converters still share similarities with digital IO buffers of digital circuits and core logic.

Indeed, in synchronous digital systems, the output of the different logic elements (logic gates, latches and flip-flops among others) transition from high to low and low to high on clock edges. As a consequence, a current transient ($\mathrm{d}i/\mathrm{d}t$) goes from the VDD and GND pins of the digital IC to the output node of each element, charging and discharging output nodes in the IC (referred to as *core logic* in the example of Figure 1.7(a) with two inverters). Similar behavior is observed on the output pins of the digital IC, where a buffer chain is implemented in order to provide enough current to drive the output capacitance of the node onto which the output pin is placed (referred to as *I/O buffers* in Figure 1.7(b)). In either case, those current transients will take the form of differential-mode and common-mode currents as seen from the power rails that will

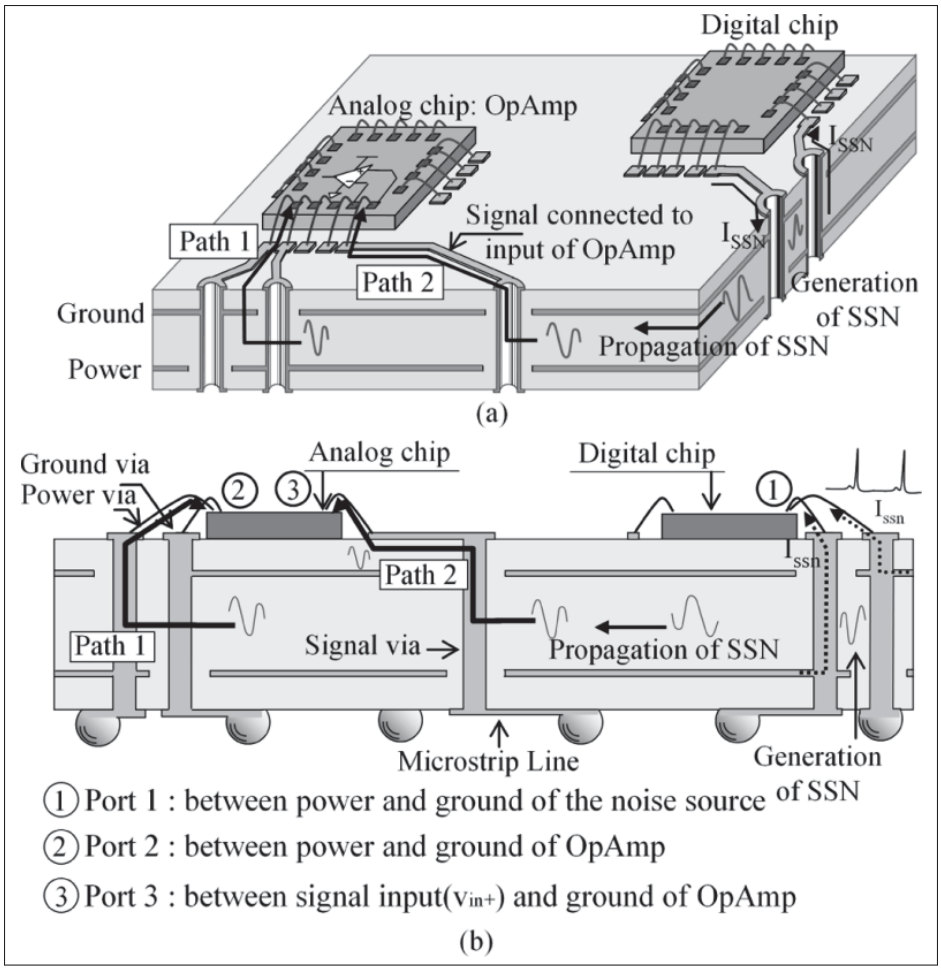

Figure 1.6 Simultaneous Switching Noise in Digital Systems
(a) in 3D and (b) side view
Taken from Shim *et al.* (2009)

create voltage fluctuations on sensitive nodes of the PDN. SSN refers to those current transients ($\mathrm{d}i/\mathrm{d}t$) that are driven from the VDD and GND pins during those clock edges due to core logic and I/O buffer activities. This SSN is considered to be the main *aggressor* noise source for PI in digital systems.

1.2.1.1 Similarities of SSN in Digital Systems With Switch-Mode Converters

SSN behavior in digital systems can very much be likened to the behavior of switch-mode converters. Indeed, power converters are also subjected to strong common-mode (CM) and

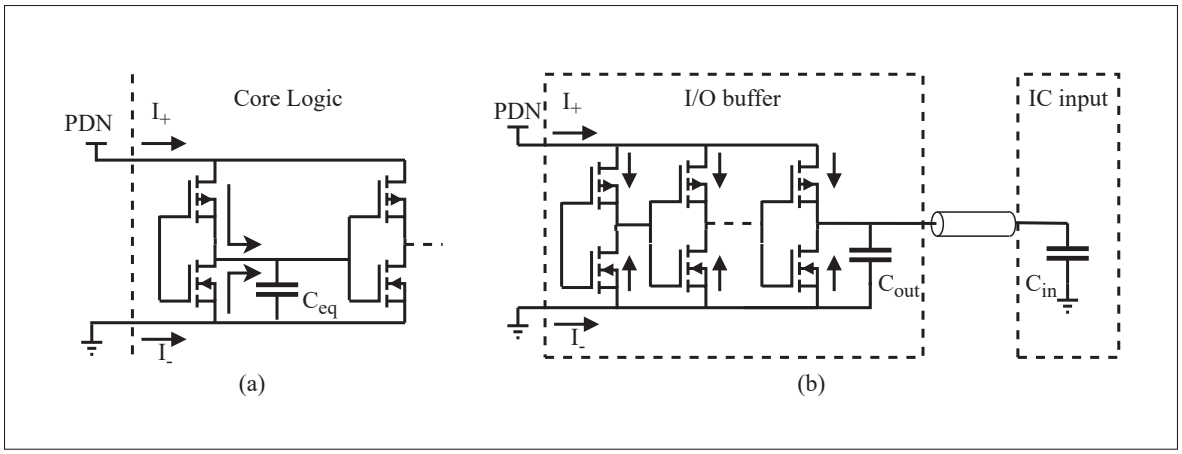

Figure 1.7 Problem of SSN for (a) core logic (with inverters) and (b) I/O buffers

differential-mode (DM) current flows during switching. For example, when a switch-mode half-bridge converter switches, the high side is ON in continuous conduction mode (CCM), the load current starts to flow from the low side (I_-) to the high side (I_+), leading to a differential-mode ($I_{DM} = (I_+ - I_-)/2$) and common-mode ($I_{CM} = (I_+ + I_-)/2$) (Figure 1.8). In addition, in MOSFET devices, a reverse recovery current starts to flow due to the body diode going from the ON to OFF state, leading to a high current transient when the high-side turns ON and the body diode on the low-side is in free-wheeling conduction. In GaN HEMTs, a similar phenomenon occurs. However it is due to the output capacitance of the transistor, rather than the body diode mechanism itself. The current from each terminal and the DM current are depicted in Figure 1.8(b), with the reverse-recovery current in the t_{rr} period of time. In that figure, the current flows through the low-side (I_- is I_L) when the low side is ON. The transistor is then turned off and the transistor is free-wheeling, which doesn't affect the currents in this ideal case. Then, the high-side is turned on and I_+ ramps up, while I_- goes down. Finally, reverse recovery occurs, leading to a peak in the DM current. That DM current is the current transient source (di/dt) in the power converter, while the CM current is a DC, considering no CM returns on the load, in the case of CCM. It is worth mentioning that in the case of a non-DC load (i.e., an RL load or in the case of an LC filter before the load), the common-mode current will be equal to the amount of inductor ripple current going through the load.

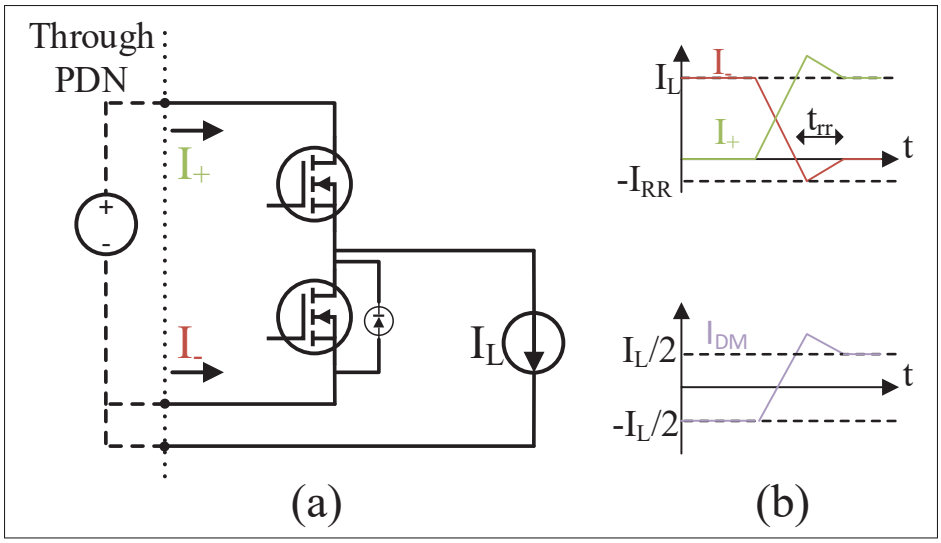

Figure 1.8 Switching noise of converter (a) schematically and (b) simplified waveforms with reverse recovery

When a current transient is drawn from the GND and VDD pins on the digital IC or even a switch-mode converter, that current is drawn or sourced from what is referred to as the PDN, leading to voltage fluctuations at different nodes due to the different couplings on the PDN. It is noteworthy to mention that the PDN, as an ideal behavior, has no coupling between its different ports, and the individual ports have a self-impedance of 0 Ω in alternating current (AC) regime. In real-life applications, it is, however, not possible to obtain zero couplings between the different ports and null self-impedance at every port. As a consequence, capacitor decoupling networks are built in order to minimize the coupling and self-impedance. Models also need to be found in order to predict the effect of SSN onto the different ports in the PDN. The next section discusses the different models that make use of the PDN-SSN combination in order to predict voltage fluctuations on sensitive nodes.

1.2.1.2 SSN Port-Based Models

In several works (Kim, 2011; Kim *et al.*, 2012; Kim, Cho, Achkir & Fan, 2018; Bae *et al.*, 2013; Shim *et al.*, 2009), the SSN is modeled as either a fixed or measured current waveform flowing through the power rails of a digital device and its impact on a sensitive node is calculated from a

given representation of the PDN (lumped-component network, Z-parameters). The combination of that aggressor current (SSN) and path (PDN) is used to calculate the noise on a victim, which can be the digital IC's power rail or another sensitive IC. In this thesis, those models are referred to as *port-based*.

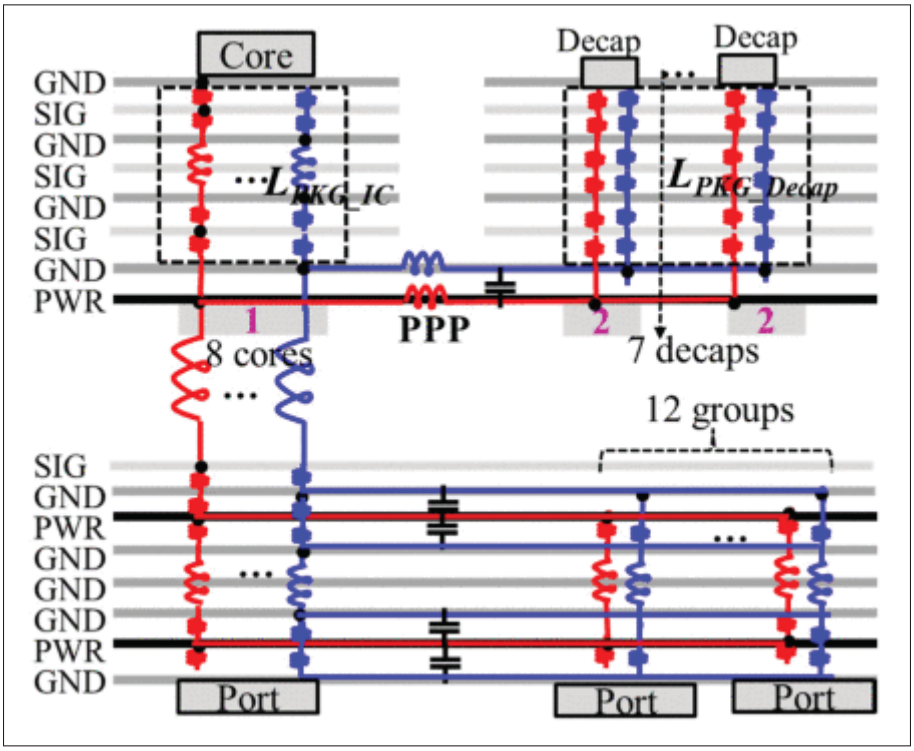

Figure 1.9 Physics-based modeling with Plane-Pair Partial Element Equivalent Circuit (PPP) method
Taken from Zhao *et al.* (2020)

Modeling the PDN can be done using an equivalent circuit extracted from PCB and package features, which are so-called physics-based model (Zhao *et al.*, 2016, 2018; Zhao *et al.*, 2020). The path from the decoupling capacitors to the power planes is modeled in both the package and PCB as inductors, while the parallel power planes are modeled with the Plane-Pair Partial Element Equivalent Circuit (PPP) method (Archambeault & Ruehli, 2001), such as depicted in Figure 1.9 (taken from Zhao *et al.* (2020)). That method is useful for modeling parallel power planes with substrate cavities for vias. It allows us to accurately capture voltage fluctuations when there is a change in the load current on the device under test (DUT), rather than the

fluctuations from the switching activity itself. Also, while this representation is intuitive and suited for time-domain simulations, when analyzing with complex non-linear components such as GaN HEMTs, it can lead to convergence problems and longer simulation times due to the large number of passive components. Therefore, simpler models that predict voltage fluctuations resulting from switching activity would be practical for computational reasons.

In (Kim, 2011), the noise generated by a single-resonance network is studied. That model has the advantage of being significantly simpler in terms of analysis compared with the physics-based model. A formulation is derived for predicting the noise onto the power rails of a digital IC when powered by a single-resonance PDN. The SSN current is modeled as a square pulse followed by a steady-state current, which is consistent with an I/O buffer terminated by a resistive load. The noise onto the power rails is then calculated by doing the convolution product between that square pulse and the impulse response of the PDN. Therefore, a closed-form equation is obtained. A so-called *PDN parameter* is then extracted in order to predict peak interference. The voltage fluctuations onto the power rails of the digital IC can be successfully obtained during switching activity of the IC. They also do it using a closed-form equation, rather than lengthy simulations. However, their model does not predict the voltage fluctuations onto a sensitive node integrated in proximity to the digital IC. Instead, the model only predicts the noise generated by a digital IC on its own power rails.

Simpler networks than physics-based models are studied in (Kim *et al.*, 2012) to predict noise from switching activity. Like with (Kim, 2011), the voltage fluctuations resulting from that noise are predicted in a closed form, not leading to convergence problems. The PDN is modeled as a cascade of T-branches representing the capacitor network: parasitic inductance from traces, resistive losses and ideal decoupling capacitors. A closed-form equation that predicts peak interference from a current pulse aggression of a given rise time and peak amplitude is found. The current resulting from switching activity was obtained by placing a coil on top of the local and bulk capacitors. Several current transients are extracted from that probe activity with various rise times and peak current amplitudes. It is hypothesized that the total peak interference is the sum of the peak interference of each aggression. Therefore, the peak noise stemming

from switching activity is extracted without convergence problems. However, they only predict the noise and the supply fluctuation onto the digital IC and not a victim located elsewhere on the PDN. In addition, the impact of multiple switching transients occurring simultaneously is predicted. These transient are most likely from different output buffers with stronger and weaker driving strengths, and can be likened to the CPIOS problem where multiple switch-mode converters with different driving strengths and load current switch simultaneously. However, they do not provide a method to obtain the overall shape and peak level of voltage fluctuations when such simultaneous switching occurs.

In (Shim *et al.*, 2009), a methodology to predict the impact of SSN onto another IC elsewhere on the PDN is provided. In this work, the effect of SSN on the DC voltage offset of an operational amplifier with a combination of transimpedance models are used for predicting the noise onto the power rails and the input nodes of the operational amplifier and a circuit-level model for predicting the noise. The PDN is modeled using a transmission-line-matrix (TLM) with extracted Z-parameters. The noise onto the two sensitive nodes (input and power rails) is predicted by multiplying the voltage at the aggressor port with the ratio of the transimpedance between the aggressor port and the sensitive nodes over the self-impedance at the aggressor port (Z_{21}/Z_{11} and Z_{31}/Z_{11}). Circuit-level analysis is done to extract the ratio between a given noise amplitude on the sensitive nodes at a given frequency and the impact on DC voltage offset. By doing that, the coupling is extracted and the impact on the DC voltage offset of the operational amplifier as a function of the SSN spectral density is calculated. A similar methodology is used for predicting the ENOB of an ADC in (Bae *et al.*, 2013) with the PDN modeled using a segmentation method (Kim *et al.*, 2010). Therefore, the authors are able to predict noise spectral density onto the sensitive nodes and even correlate them with ADC or operational amplifier performance. However, the proposed model does not predict the noise spectral density of the SSN. Indeed, ENOB of an ADC or DC voltage offset of an operational amplifier can be predicted when the spectral density of SSN is known.

The PDN can also be extracted through commercial solver tools, such as Keysight ADS, ANSYS SIWave, ANSYS Q3D Extractor or Mentor Graphics Hyperlynx. The result of those

solvers can be extracted as multiple forms, namely S-parameters and partial element equivalent circuit (PEEC). That result can then be used in combination with a simulation program with integrated circuit emphasis (SPICE) model of the power transistors to predict voltage fluctuations onto sensitive nodes, either through SPICE simulations with a PEEC or transient-convolution simulations (Keysight, 2022b) in the case of S-parameters. In either case, such simulations lead to large computational complexity and convergence problems.

1.2.1.3 IBIS Models and Other Macromodels for Power Integrity Predictions

The input/output buffer information specification (IBIS) family of models capture the non-linearity of output buffers and make predictions on signal integrity (Casamayor, 2022). They are typically used as a substitute to a transistor-level model and IBIS models are typically compared with their transistor-level equivalent for prediction benchmarking. This family of models is based on current-voltage and time-voltage tables in order to predict the output voltages and currents of digital output buffers depending on loading conditions. Extensions have been proposed in order to also predict power integrity constraints and their impact on the digital IC (Yang, Huq, Arumugham & Park, 2005; Dghais & Rodriguez, 2016; Dghais, Souilem, Zayer & Chaari, 2018; Pulici *et al.*, 2008). In (Yang *et al.*, 2005), it is proposed to consider the equivalent impedance of the network providing the power to the output buffer with the equivalent RLC circuit of Figure 1.10 (taken from Yang *et al.* (2005)) to predict noise onto core logic power rails (VDDQ and GND). With that extension, the voltage fluctuations on the power rails of the IBIS-modeled output buffer and their impact on the voltage and current output are predicted with better accuracy when considering the noise on the power rails of the buffer. This is true even in the case of SiP (Pulici *et al.*, 2008). IBIS models have the advantage of being based on device characterized behavior, rather than a physical description of the buffer, thereby hiding implementation from the user and better protecting intellectual property of the manufacturer. However, like in other works for PI in digital systems, the focus is put on the voltage fluctuations present on the digital circuit itself, rather than on other sensitive nodes such as ADC or operational amplifiers. IBIS models are also made for digital output buffer, typically in complementary metal–oxide–semiconductor

(CMOS) logic. Therefore, the pull-up circuit of the output buffer is typically a P-type transistor. This is different from switch-mode amplifier outputs, which are often based on a half-bridge with N-type pull-up logic. It is worth mentioning that other so-called *macromodels* (Signorini, Siviero, Telescu & Stievano, 2016) exist for I/O buffers. However, like with IBIS, they are not necessarily suited for modeling switch-mode converters because of their fundamental difference with digital output buffer circuits.

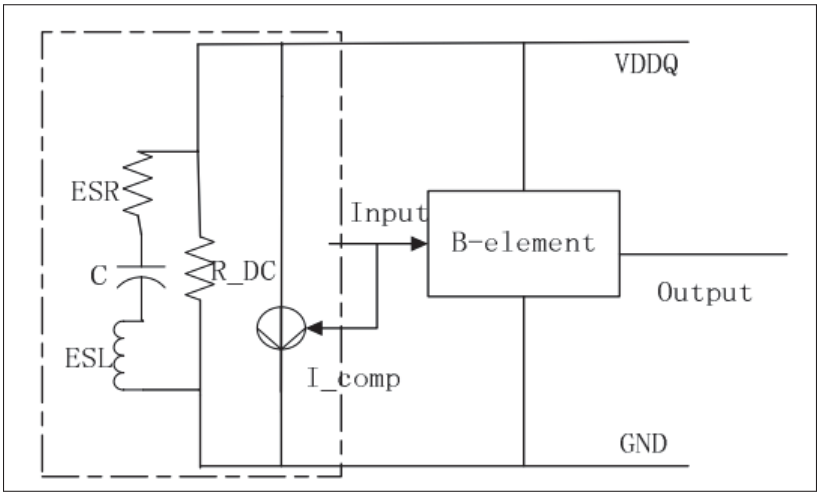

Figure 1.10 Improved model with PDN for IBIS
Taken from Yang *et al.* (2005)

The works presented above, both IBIS models and port-based models show that there are methodologies in order to predict the voltage fluctuations onto the power rails of digital IC and other sensitive IC located elsewhere using simple closed-form models. However, an issue specific to CPIOS remains: Considering the switching behavior of switch-mode converters, rather than digital IC: while digital IC shares similarities with power converters in terms of switching characteristics, they also have major differences such as the converter generating mainly DM currents in CCM and having multiple conditions depending on loads, which leads to different precise switching currents that can be characterized for the purpose of a model.

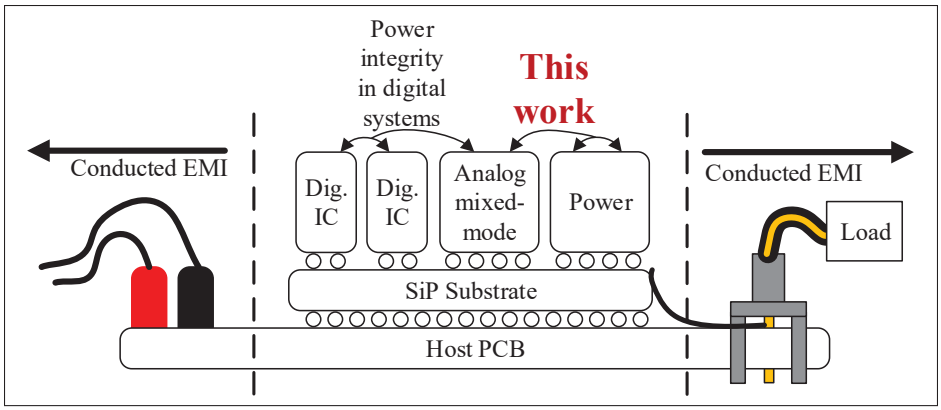

Figure 1.11 Conducted EMI in Power Electronics vs. PI in digital systems and CPIOS

1.2.2 Conducted EMI in Switch-Mode Converters

Predicting PI in SiP with switch-mode converters and sensitive circuits is also akin to the prediction of conducted EMI in power electronics (Figure 1.11). Switch-mode power converters on a given board or electronic equipment will generate conducted noise onto their power supplies through cables and electrical interconnections. The noise spectral density is typically measured with standard equipment such as a line impedance stabilization network (LISN).

1.2.2.1 General Terminal Modeling

Several behavioral models where the switch-mode converter is modeled as a linear current or voltage source in a Thevenin/Norton configuration have been developed to predict conducted EMI onto loads or power supplies. In such models, the source drives a passive network representing the connectivity towards the power source of the device or a LISN (Baisden, Boroyevich & Wang, 2010; Liu, Wang & Boroyevich, 2006; Zhou, Pei, Xiang & Kang, 2020; Ishibashi *et al.*, 2021). Those models are in the category of the so-called *general terminal modeling (GTM)* (Kharanaq, Emadi & Bilgin, 2020). However, when using the GaN HEMT-based switch-mode converters with ns-range switching times and interested in PI on the supply rails of sensitive devices, reaching GHz frequency for characterization and prediction of noise is critical, as will be demonstrated

in section 2.3.2 of this thesis. Such a frequency range is not studied in multi-terminal models because in typical standards for conducted EMI, the applicable frequency range spans in the tens of MHz. In addition, conducted electromagnetic compatibility (EMC) standards define limits based on spectral content of the noise, while in the context of this CPIOS, peak time-domain interference and phase of noise is equally important to ensure the supply voltage does not go above the breakdown voltage of connected devices. Finally, no other work, to the best of our knowledge, exists that study the behavior of those switch-mode converter when switching simultaneously.

1.2.3 Conclusion on Power Integrity Assessment Techniques

The problem of voltage fluctuations generated by switch-mode converters onto power rails of sensitive devices, such as ADC and operational amplifiers is very much akin to that of SSN in digital systems and conducted EMI in power electronics. Those techniques have value in the context of predicting PI in switch-mode converters. The main issue is that core logic and I/O buffers in digital systems inherently have different switching behaviors as converters. Several models also exist for the prediction of conducted EMI in power electronics, which can be compared to the prediction of PI in our context. However, several limitations were found in terms of frequency range and the type of prediction possible with those models. Table 1.2 summarizes those conclusions.

In the following chapter, the problem of power integrity in CPIOS is further explored and quantified. From the issues in the literature, several specifications and needs are derived for current measurement techniques and models for power integrity assessment.

Table 1.2 Summary of models for power integrity assessment

Type of model	Description	Drawback
PI in digital systems		
SSN Port-based Models	Aggressor SSN current, going through a path modeled as a passive network	Predict noise from digital IC, which has inherently different characteristics as switching noise from power converters.
IBIS Models and other Macromodels	Behavioral model with current/voltage tables for I/O buffers in digital IC	
EMC in power systems		
General Terminal Modeling	Model the converter as a Thevenin or Norton source driving a passive network representing connectivity to an LISN	Frequency range limited to tens of MHz Does not predict the overall shape of the voltage fluctuations onto the devices Does not predict the transient generated by multiple simultaneously switching converters

CHAPTER 2

POWER INTEGRITY CONSTRAINTS IN CPIOS

This chapter presents the need for GHz-range techniques for both current measurement and power integrity analysis. First, the CPIOS system is presented with implementation details. Next, the problem of power integrity is defined and put in the context of CPIOS. Then, it is explained how the problem of power integrity is relevant when discussing an array of switch-mode converters in the context of SiP. More specifically, simultaneous switching issues are discussed. After that, the need for GHz-range current measurement technique is presented in the context of power integrity assessment for switch-mode converters integrated in SiP. Finally, the objectives defined in the introduction are revisited based on the context presented in this chapter. This chapter is based on, with extracts from, the first two sections of (Nobert *et al.*, 2023) and (Nobert *et al.*, submitted for publication) as well as the conference paper (Nobert *et al.*, 2021).

2.1 System-Level Summary of CPIOS

As depicted in Figure 2.1, proposed in (Nobert *et al.*, 2021) and (Nguyen *et al.*, 2022), the general idea of the CPIOS is to provide a complete interfacing system for the read-out and control of high-power and voltage loads with a digital control system such as an FPGA in the form of a compact system.

In that system, a configurable gate driver (CGD) designed in XFAB's XT018 process (Ly *et al.*, 2020) drives power GaN devices in switch mode. It is at the core of the configurable power block array. Each CGD has multiple driving strengths and supports real-time control of dead times. A flexible footprint for the power devices allows swapping between different devices. The power devices are in a half-bridge topology, with each drain and source terminal accessible from the SiP pins. Therefore, the configurable power blocks can be put in multiple configurations in terms of topology and trade-offs between driving strength, efficiency, EMI and output power.

A read-out block allows sensing and conversion of analog voltages or currents in loads to the digital domain. The system therefore supports multiple digital control loops for power converter

circuits. The digital isolators protect external control circuits against common-mode transients and faulty signal lines between the digital control system and the power domain.

The following section describes more in detail each of the block presented in Figure 2.1.

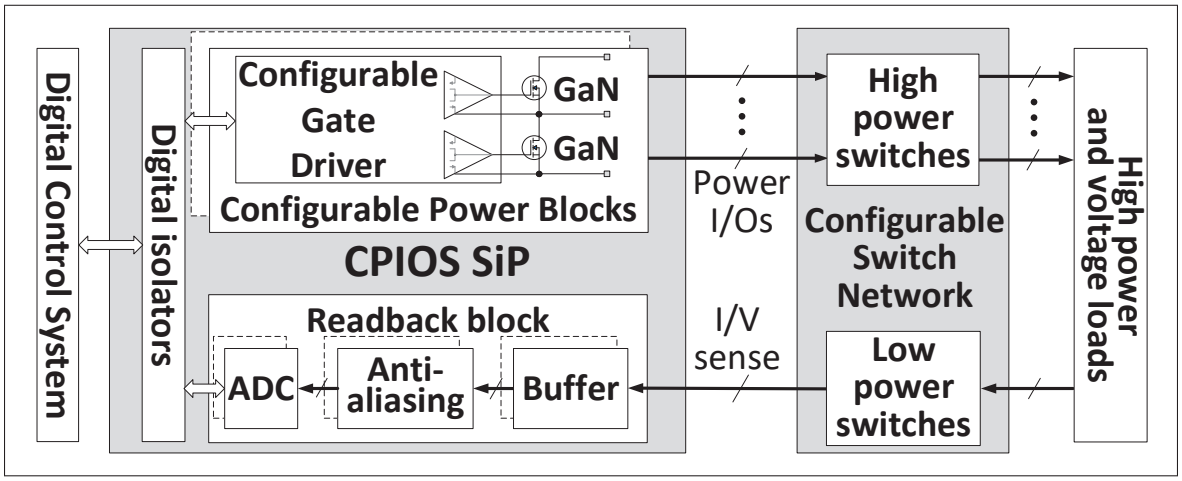

Figure 2.1 System-Level depiction of the CPIOS system

2.2 Detailed block Diagram of CPIOS

The CPIOS SiP is depicted in more detail in Figure 2.2. It is made of three key elements: isolator channels, M configurable half-bridges (HB_1 to HB_M) and L readout channels based on ADC and operational amplifiers for signal conditioning. The different half-bridges and readback channels are connected to K loads, which are made of a single or a combination of half-bridges depending on the selected topology: bridge-tied load (BTL) full bridge, buck converter, buck-boost converter, etc.

As also shown in the diagram of Figure 2.2, the system is connected to a plurality of loads, with their respective load current. However, topologies that require multiple half-bridges, such as buck-boost or a BTL driven by a full bridge, may be implemented with the half-bridge configured accordingly, being merely a building block in the CPIOS system. Therefore, there is a number K of loads, which is less or equal to the amount of half-bridges.

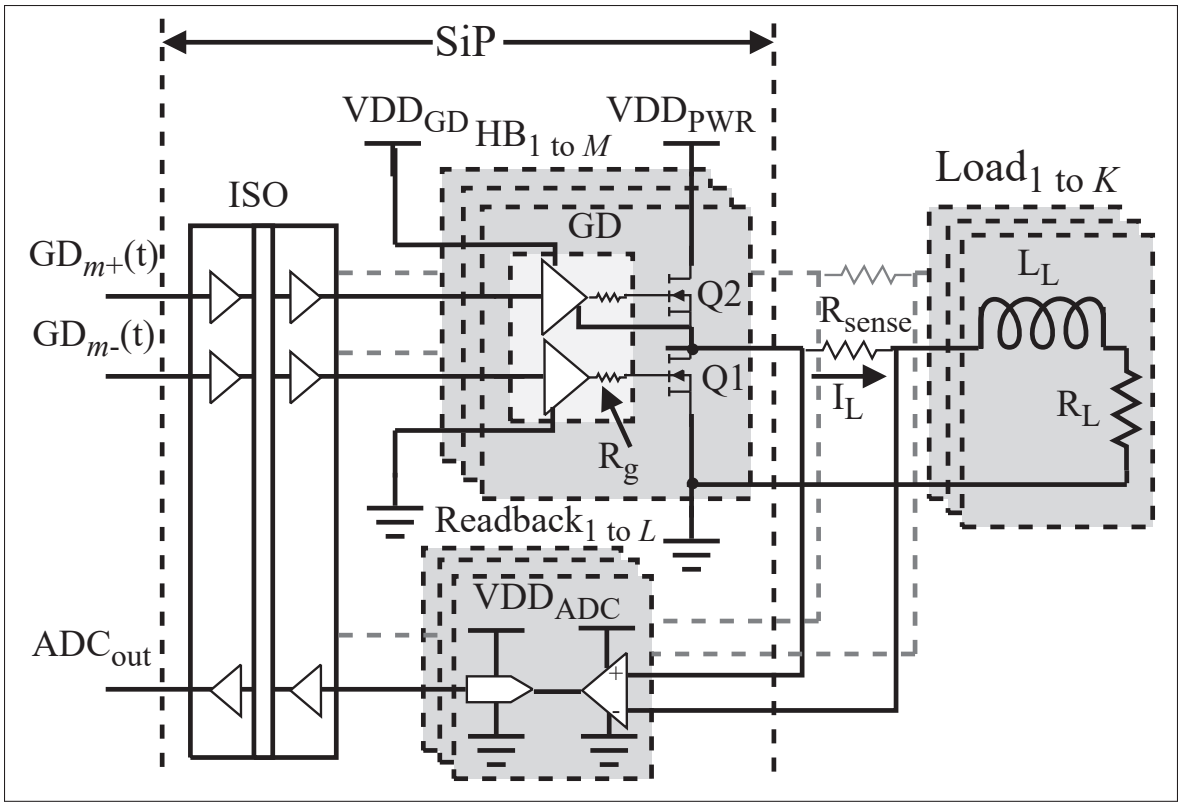

Figure 2.2 Array of M independent half-bridges (HB) in an SiP of configurable switch-mode converters

Different feedback signals are read through the ADC and signal conditioning circuits in one of the L Readback blocks. The signal conditioning circuits are active filtering stages, scaling the signal to the needs of the ADC and ensuring anti-aliasing by applying a low-pass filter with a high attenuation at the Nyquist rate of the ADC. Once converted to digital domain with either I^2C, SPI or parallel signaling, the ADC_{out} data is received by the FPGA or microcontroller through the digital isolators (ISO). A closed-loop algorithm and control logic then feed pulse-width modulation (PWM) (GD) to the digital isolators and into the gate drivers of the power stages in the system.

In order to achieve compactness, the system is integrated within a small area, thereby sharing the same substrate for the different circuits. An example of layout achieved is presented in Figure 2.3. With that layout, which has been fabricated, 3D integration was achieved using a

low-temperature co-fired ceramics (LTCC) substrate, meaning components were not placed on the same plane, but rather spread vertically across multiple layers. Other than for density of integration, which is presented next, thermal performance and signal and power integrity were also among the main advantages of LTCC (Nobert *et al.*, 2021).

A typical 2.5D system includes a substrate and devices integrated on the top layer only. However, by adding cavities, it becomes possible to embed components and achieve 3D integration. A chip-covering technique, as proposed in (Nobert *et al.*, 2021), was used. With chip covering, different IC or passive components are covered with larger, packaged chips on top (Figure 2.3(b)). In this case, a small-outline integrated circuit (SOIC) was put on top of a cavity in Figure 2.3, passive components were put underneath. Sitting on top of that cavity was the ADA4522-4 (*SOIC* label in Figure 2.3(b)), which is an amplifier used for the signal conditioning. The passive components are the ones needed for the anti-aliasing filtering. This technique enhances the density, compared with a typical SiP integration with the components only on the top layer, of the system without requiring intertwined steps between fabrication and assembly. Another technique used to increase the density is to place cavities on the bottom side of the substrate as shown in Figure 2.3(c). In these cavities, other ICs are placed in order to enhance the area efficiency of the SiP. In that implementation, it is the digital isolators that were put underneath. In addition, the cavities also help reduce wire-bonding lengths for the gate driver bare die, and therefore minimize the series parasitic inductances with the gate driver pins. Therefore, compact integration was achieved where converters were tightly integrated with sensitive analog IC and ADC.

Regarding the M configurable half-bridges, those circuits are the main generators of noise and power supply interference in the system, as described in section 1.2.1 of the literature review. Indeed, the power stage draws DM current transients ($\mathrm{d}i/\mathrm{d}t$) from the supply rails, leading to voltage fluctuations on the PDN due to the parasitic inductances, resistance and transmission-line effects in it. Such voltage fluctuations become an issue when considering the readback stages, gate drivers and other converters. Indeed, the different readback stages are made of ADC and operational amplifiers. Both of those are sensitive to power supply fluctuations on their

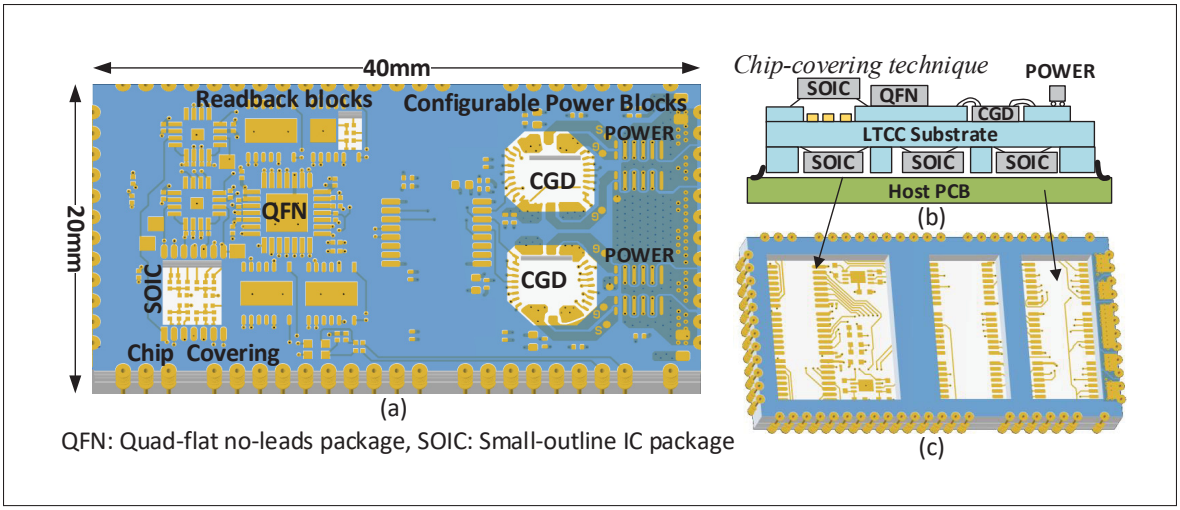

Figure 2.3 3D integration of the CPIOS: (a) top (b) side (c) bottom views

power stage, which can impact their reference voltage, and consequently, their voltage readouts, leading to loss of accuracy on the readback system measurements. Not only can the readback be impacted, but also, as studied in this thesis, noise can also be propagated onto the supply rails of other converters or their gate drivers, also leading to performance impairments. This issue is the main reason for the study of PI constraints in CPIOS, as described next.

2.3 Power Integrity Constraints in CPIOS

Power integrity, as it is defined in this work, is the study of the quality of power delivery to the digital and sensitive analog IC supplies. Such a concept typically applies to digital systems. As presented in the literature review chapter (section 1.2.1), a digital IC, through its core logic and I/O buffers, pulls DM and CM currents from the supply rails, which is the so-called SSN. Those currents lead to disturbances and hence, voltage fluctuations, on the power rails of that digital IC as well as neighboring circuits. Typical requirements for power integrity are formulated in terms of:

- AC-regime fluctuations over certain frequency bands;
- peak amplitude of voltage fluctuations;
- shape of voltage fluctuations.

Failure to meet specifications in terms of those criteria may lead to performance impairment in terms of ENOB in ADC, jitter, failure of timing in digital circuits and DC offset voltage in operational amplifiers (Shim *et al.*, 2009). In order to ensure that those specifications are met, a model for power integrity, more specifically to predict voltage fluctuations onto the power rails of sensitive IC, is in order. Specifically in the case of CPIOS, the main source of current aggression is not digital IC and SSN. Rather, as will be shown in this chapter, it is the switch-mode converter that pulls strong DM currents upon switching that are the main source of aggression. Indeed, this is especially true in the case when using fast-switching transistors such as GaN HEMT.

2.3.1 GaN HEMT Devices for CPIOS

In applications such as the CPIOS, transistors that offer a better trade-off between gate charge, dimensions and power handling capability are required. With the compactness requirements of the CPIOS, WBG transistors such as SiC and GaN HEMT are preferable. In the specific case of GaN HEMT, which are the devices used in the context of CPIOS, those transistors can achieve switching times in the order of less than one ns (Simonaitis *et al.*, 2021). With such switching times, it is possible to reach switching frequencies of 5 MHz in the case of the commercial gate driver LMG1205 (Texas Instruments, 2018) to even 40 MHz in the case of the now-obsoleted PE29102 (pSemi, 2022). Thanks to high switching frequencies, it is possible to further lower the dimensions of switch-mode power systems by reducing the size of the output filter, especially the inductor in the case of a passive LC filter, thereby improving integration density in CPIOS. This advantage of fast switching, however, comes at the cost of GHz-range noise generated on the power rails of the CPIOS.

2.3.2 GHz-range DM current and noise in switch-mode converters for SiP integration

The main drawback of having sub-ns switching times is that GHz-range current spectral density is drawn by the converter when those power devices are switching. As a consequence, noise generating mechanisms in the GHz range are present in the system. The following simulations show that DM currents, meaning in this case a differential flow of current as seen by the power

rails (high-side drain and low-side source), are generated by the switch-mode converters when switching. A simple switch-mode converter circuit (Figure 2.4(a)) containing a DC voltage source and two power transistors was simulated. Figure 2.4(b) depicts the simulated DM current of the circuit assuming the voltage source and the load current return are directly connected through the PDN to the converter. The converter is built with two EPC2037 GaN HEMT power devices, has load currents of 100 mA and 1 A switched at a 50 % duty cycle, with the gate of the low-side GaN HEMT Q1 tied to ground, while the high-side Q2 is driven with a 5 Ω gate resistor. Upon switching, the current signal drawn can be split into two components: a pulse and a square. Those two components are individually analyzed for a 100 mA load current in the dashed orange and yellow lines of Figures 2.4(b) and (c). At low frequency, the spectral density decreases at a rate of −20 dB/dec, as expected for the harmonics of the square component of the signal in Figure 2.4(b). For the 100 mA load current, at higher than 50 MHz, the current spectral density flattens due to the spectral content of the pulse component in the signal (Figure 2.4(b)), which becomes predominant. The pulse component has a duration of 0.5 ns and a triangular shape. It can be numerically shown that the energy spectrum of a symmetrical triangular pulse with a duration of 0.5 ns is 3 dB below its nominal (DC) spectral density at approximately 1.27 GHz. This cutoff frequency is consistent with the plot of Figure 2.4(c), which shows a decrease in spectral density for both the pulse and DM current starting approximately at that frequency.

In silicon devices, the pulse component is associated with the reverse recovery in the low-side freewheeling body diode during the transition to the off state. In GaN HEMT devices, that pulse is associated with the charging of the output capacitance (C_{OSS}) of the low-side transistor. Hence, its amplitude depends on drain-source voltage and device output capacitance but does not depend on the load current. It is observed that the DM current for a 100 mA load (Figure 2.4(b)) has a large pulse component amplitude relative to load current, due to the low-side EPC2037's output capacitance and small on-state resistance on the high-side. The purple trace shows DM current for a load current of 1 A, which is another operating condition closer to the device's maximum ratings. While techniques to mitigate the pulse component can be used, those would result in reduced switching speed and increased losses, besides the need to adding components,

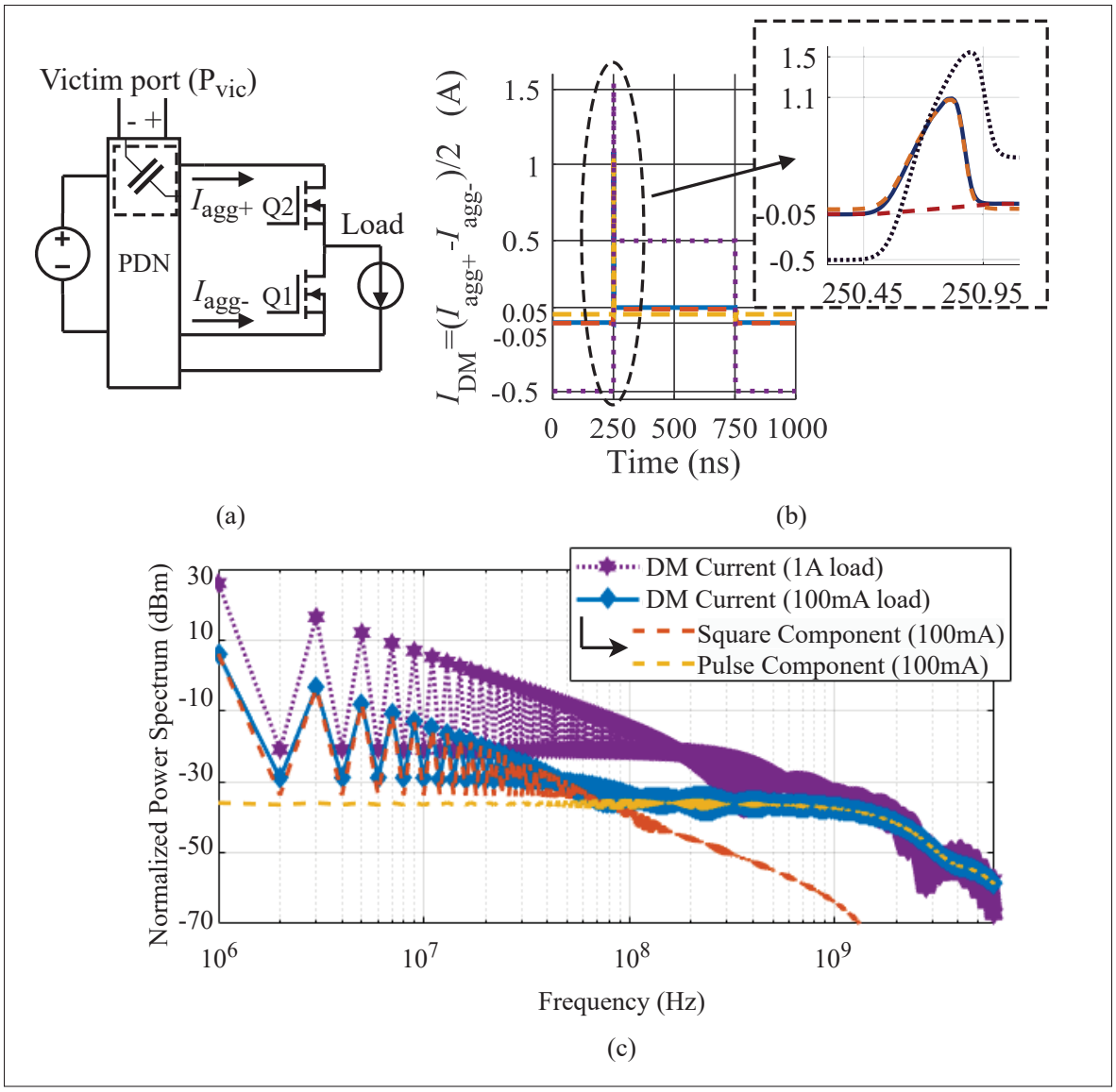

Figure 2.4 Differential mode current in a converter: (a) circuit model of the converter with the coupling current onto a victim, (b) simulated differential-mode current in time domain and (c) its frequency spectrum

which is undesirable in SiP applications. Therefore, noise-generating mechanisms are present in the CPIOS integrated with switch-mode converters based on GaN HEMT devices.

In addition, resonant modes of the power supplies with the converter and sensitive devices can exist in the GHz range. For instance, let us consider an ADC with its power pins connected to a decoupling network, which in turn are connected to power planes through vias. This network

has inductive vias, self-resonant discrete capacitors and capacitive power planes that typically generate parallel and series RLC resonances, thereby creating coupling paths in the PDN from the converter to the victim port (P_{vic} in Figure 2.4(a)) in the GHz range. In highly integrated SiP systems, such as CPIOS, strong coupling can be observed between the aforementioned DM currents and the power rails of a sensitive device. It has been shown ((Bae *et al.*, 2013, Fig. 13(a))), in the context of digital systems, that spectral content well into the hundreds of MHz on the power rails of an ADC can degrade its performances in terms of ENOB. Such a current spectral density together with strong coupling mechanisms and the sensitivity of ADC to switching noise all lead to performance impairments. The above considerations on the spectral content of DM currents and coupling mechanisms justify the need for techniques in order to assess PI constraints.

2.3.3 The problem of simultaneous switching in an array of switch-mode converters for SiP integration

In addition to GHz-range noise, the problem of simultaneous switching is also of importance. As mentioned, the CPIOS contains an array of switch-mode converters. It may occur that multiple independent converters switch with simultaneous or quasi-simultaneous timings in such a system. For instance, a converter A may switch, going from low-side to high-side on, thereby generating a current transient ($\mathrm{d}i/\mathrm{d}t$) that causes ringing onto a sensitive victim node. As that ringing occurs, a converter B, independently controlled, can also switch, thereby also causing ringing on that same victim node. Simultaneous switching is defined in this thesis as when the effect of the current pulled by several independent half-bridges on a victim port overlap each other.

The likeliness of simultaneous switching increases with the number of independently controlled half-bridges and the decrease of switching periods. As an example, consider a switching current ($\mathrm{d}i/\mathrm{d}t$) with strong spectral content at 500 MHz due to ringing induced by significant LC loading effects at the power rails. With an under-damped second-order dynamic, this would translate to a $\mathrm{d}i/\mathrm{d}t$ that can last from approximately 2 ns to longer, potentially tens of nanoseconds, depending

on the quality factor of the LC loading. Under such constraints, in addition to a large number of independent converters, simultaneous switching would be difficult to avoid.

The following simulation example further shows the issues mentioned above, both of GHz-range noise and coupling as well as simultaneous switching. Let us consider a simple system with two half-bridges ($HB_{1,2}$) with their respective gate driver (GD) (Figure 2.5). The *victim*, for simplicity's sake, is the power rails of one of the gate drivers. In a more real-life case, it could be a tightly integrated ADC, an operational amplifier for signal conditioning, or even another converter. The two aggressor sources are half-bridges powered by 20 V that are switching with 100 mA (OUT_1) and 10 mA (OUT_2) strongly inductive loads.

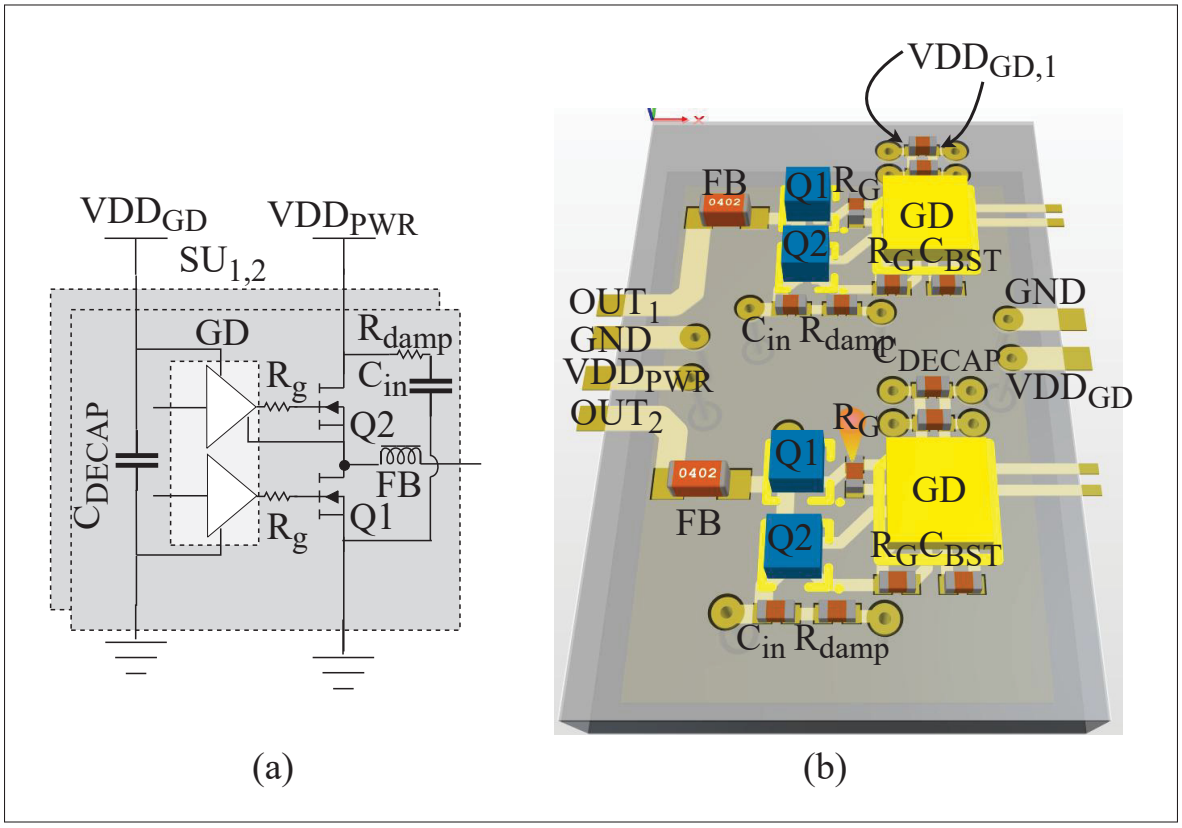

Figure 2.5 Array of two switching units: (a) the schematic and (b) a 3D board view of the simulated passive board in ADS

The system on an FR-4 substrate made of two prepreg dielectrics (0.11 mm) and a core (0.465 mm) at the center of the board is simulated in Keysight Advanced Design Systems (ADS). The two

bottom layers are used as the ground and power plane, while the top layer is used for routing. The power plane is split into two different separate planes: one for converter power and the other for gate driver power. The second layer can be used for current measurement purposes, such as in chapter 3 of this thesis. The 0201 ($20 \times 10\,\text{mil}^2$) capacitors are considered to have an equivalent series inductance of 0.5 nH, while the resistor has a negligible equivalent series inductance. Q2 has the Spectre model of an EPC2037 and is driven by an ideal step voltage source and a resistor R_g series with the gate-source terminal. Transistor Q1 is left in the body diode-like conduction of the GaN HEMT with 0 V on the gate-source terminal of the same transistor model as Q2. Several of those assumptions are made in order to ensure convergence of the simulations.

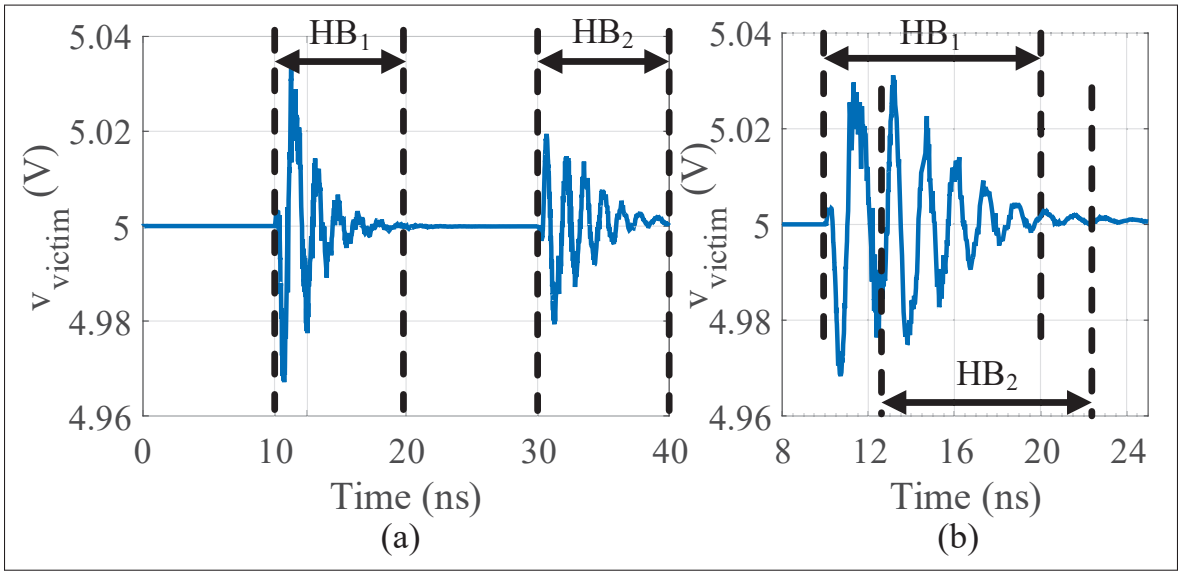

Figure 2.6 Simulated noise on the gate driver supply rails when two units are switching (a) separately and (b) simultaneously

The noise on the gate driver power rails (VDD_{GD} in Figure 2.5(a) and $VDD_{GD,1}$ in (b)), which is the victim port in this case, is shown in the simulation results of Figure 2.6. The impact of each half-bridge (HB_1, HB_2) is shown separately in Figure 2.6(a). Those results have two important elements: first, significant noise (in the tens of mV) in the form of ringing is observed at approximately 500 MHz in Figure 2.6(a) when one of the converters switches; secondly, simultaneous switching, such as depicted in Figure 2.6(b), affects the shape of the transient generated. The former further strengthens the discussion of section 2.3.2, while

the latter requires more discussion. When the two converters switch 20 ns apart from each other, the effect is minimal (Figure 2.6(a)), however, if the two converters switch 2.5 ns apart, constructive interference occurs (Figure 2.6(b)). This phenomenon is referred to in this work as *simultaneous switching*. As the number of converters in the system increases, this problem of simultaneous switching becomes increasingly difficult to avoid. Simultaneous switching also affect power integrity constraints calculations. In fact, without simultaneous switching, total noise power on a given victim node could be calculated by summing the noise power contribution of each individual converter the same way uncorrelated noise power adds up. However, with simultaneous switching, the phase relationship between the contribution of each individual converter may affect total noise power due to constructive or destructive interference on the victim node. Therefore in order to calculate noise power, the phase in each individual transient must be properly asserted. In addition, peak voltage levels cannot be calculated under simultaneous switching conditions without properly asserting the phase. Therefore, not only is predicting the voltage fluctuations spectral density important, but also asserting the phase, and hence shape, is equally important for proper voltage fluctuation predictions under simultaneous switching conditions.

In conclusion, two problems regarding PI in CPIOS were highlighted. First, GaN HEMT power devices generate GHz-range current transient that can cause PI problems in that same frequency band. Second, the effect of those current transient in the GHz range may add up when multiple independently controlled converters switch simultaneously, leading to complex transients that involve the switching of multiple converters with different possible timings. These problems justify the need for a model for power integrity in order to predict those voltage fluctuations onto the power rails of sensitive devices. The objectives defined in the introduction are explained with more details in the following section.

2.4 Detailed objectives

As mentioned in the introduction, the following specific objectives are pursued in this work:

(O1) To characterize the switching current in power converters for the CPIOS, which are critical for power integrity.

(O2) To predict fluctuations onto the power rails of sensitive circuits, in terms of shape and energy spectrum.

Based on the context of the thesis presented in this chapter and based on the literature review, for the first objective (O1), the goal is to have a current measurement technique that fit the following needs:

(SO1.1) Develop a compact embedded technique for use in an SiP, including minimal probing overhead, as it is the problem in several state-of-the-art techniques;

(SO1.2) To reach GHz-range frequencies, as argued in section 2.3.2.

More specifically, for the second objective (O2), we want to predict fluctuations onto the power rails of sensitive circuits with the aim to:

(SO2.1) Predict spectral noise power density of multiple converters switching simultaneously under any condition to assess performance degradation of the switch-mode converters. Given what was argued in section 2.3.2, this means predicting noise up to the GHz range;

(SO2.2) Assess whether we meet breakdown voltage limitations of the IC by predicting the overall shape of the voltage fluctuations.

The following chapters will focus on presenting techniques that fits such needs presented above.

CHAPTER 3

A COUPLED TRANSMISSION-LINE-BASED MEASUREMENT TECHNIQUE FOR CURRENTS IN SWITCH-MODE CONVERTERS

As presented in the first two chapters and the introduction, there is a need for a current measurement structure fit for SiP implementation, specifically for the characterization of DM currents in switch-mode converters such as described in section 2.3.2. More specifically, it was shown in the literature review (section 1.2.3) that there is a need for a less invasive (i.e., less probing overhead) as well as higher bandwidth than state-of-the-art structures. Figure 3.1 shows a simplified view of the application of the current measurement structure needed. In that figure, the current I_{agg-} is measured indirectly through a current sensor, which converts it to a voltage V_{Iagg-}.

In this chapter the concept of measurement distortion is first presented. Afterwards, a novel *transmission-line-based current measurement technique* is presented and analyzed. The analysis of the structure is then validated by doing EM simulations and comparing them with the analytical calculations of the behavior of the structure. It is shown that the structure accurately predicts both parasitic capacitive and inductive as well as transmission-line effects up to more than its

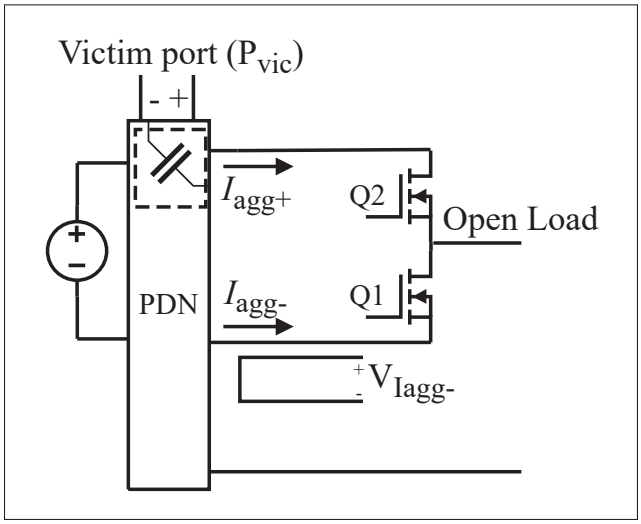

Figure 3.1 Need for current measurement

useful bandwidth. Then, an experimental apparatus to validate the technique is presented: the measurements made with the transmission-line-based structure are compared with an SMD current shunt resistor for small load currents. The measurement distortion is also measured in order to assess the quality of the measurements for both techniques. The results are then presented. The content of this chapter is based on, with extracts from, the last three sections of (Nobert *et al.*, 2023).

3.1 The Metric of Measurement Distortion

The factors that affect the accuracy of both resistive shunt-based and mutual inductance-based current measurement techniques are discussed and the metric of linear measurement distortion is introduced.

Measurement distortion is a convenient way to evaluate the precision of a current measurement technique as a function of frequency. Over the next sections, different key advantages of the transmission-line-based current measurement technique are presented in terms of that metric. Accordingly, the metric of measurement distortion is presented with the case examples of resistive shunt sensing and inductance-based sensing next.

3.1.1 Case Example: Resistive Shunt Sensing

Several techniques, such as using a SMD shunt resistor, can help achieve high bandwidths. When using those particular techniques, a resistor is placed in series with the current flow (I_1) in order to measure it as a voltage (V_2) through the IR drop of the shunt resistor. It can be represented by the equivalent circuit of Figure 3.2(a). The internal parasitics (L_{par}, C_{par}) in a small SMD form factor, such as 0201 ($20 \times 10\,\text{mil}^2$), being in the fF and fH range (Vishay Intertechnology, Inc., 2009), are typically negligible. However, the external connection inductance (L_{ext}) of the resistive shunt circuit may need to be accounted for at higher frequencies. Indeed, the measured voltage (V_2 in Figure 3.2(a)) becomes linearly distorted with respect to the actual current I_1 because of that external inductance.

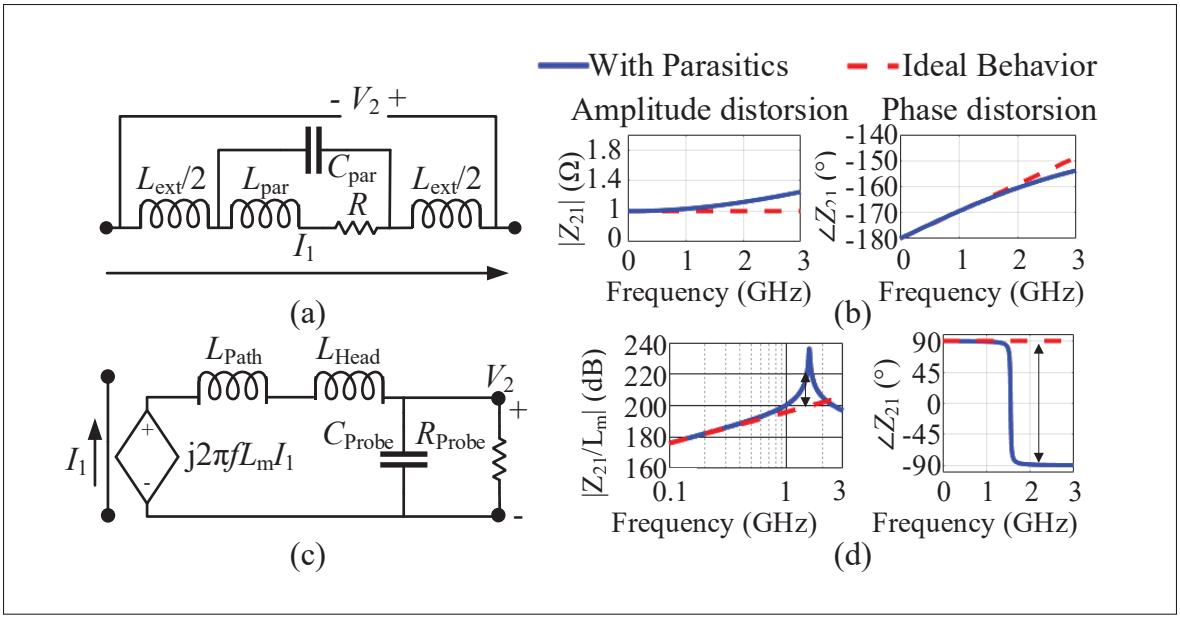

Figure 3.2 Two-port model of two current measurement techniques: (a) resistive shunt technique with (b) its transimpedance and distortion (amplitude and phase), (c) mutual inductance-based technique (Taken and adapted from Wang *et al.* (2018, p. 6203)) with (d) its transimpedance and distortion

In more rigorous terms, in this non-ideal resistive shunt technique, the magnitude of the transimpedance $|Z_{21}| = V_2/I_1$ is not constant over the desired frequency band. Furthermore, the phase of the transimpedance, $\angle Z_{21}$, does not vary proportionally to frequency, which would represent a fixed time delay between V_2 and I_1. Those concepts are referred to in this thesis as linear *measurement distortion*, which can be split into *amplitude distortion* and *phase distortion*. Those are depicted for a shunt resistor in Figure 3.2(b). Either of those distortions constitutes an impairment in the current measurement process. The amplitude and phase distortions are formally defined by (3.2) and (3.3) respectively, where R is the nominal resistivity of the shunt resistor and T_{delay} is a positive or negative constant group delay approximating the phase-shift effect due to parasitic inductance in the resistor.

$$BW_{\text{shunt-resistor}} = \frac{R}{2\pi L_{\text{ext}}} \tag{3.1}$$

$$Distortion_{[\mathrm{dB}]} = \left| 20 \times \log_{10} \left(\left| \frac{Z_{21}(f)}{R} \right| \right) \right| \tag{3.2}$$

$$Distortion_{[\mathrm{rad}]} = \angle Z_{21}(f) - \left(\pi - \left(2\pi f T_{delay} \right) \right) \tag{3.3}$$

3.1.1.1 Another Case Example: Inductive Sensing

As discussed in the literature review, another method for current sensing is through mutual inductance and current transformers. One of the ways this can be done is through the use of a single-winding Rogowski coil, referred to as a *pickup coil* (Wang *et al.*, 2018). The idea is to capture the magnetic flux of the current transient in the power loop, which is considered the primary side of the inductive coupling mechanism, by measuring $\mathrm{d}i/\mathrm{d}t$ with a coil underneath the loop trace, which is considered the secondary side. That secondary side is loaded by the measurement circuit of Figure 3.2(c), which is adapted from (Wang *et al.*, 2018, Fig. 10(c)). As highlighted in (Wang *et al.*, 2018), the secondary side of the structure and the probe head exhibit inductive behavior, and therefore, a high self-impedance as frequency increases. In such conditions, a high-impedance probe (R_{Probe}) must be used. With the probe resistivity being high, an LC resonance between the probe capacitance and the coil inductance occurs.

This resonance causes a large increase in the gain of the measurement circuit at a given resonant frequency determined by the probe capacitance and the inductance of the measurement circuit. However, in the case of pickup coils or any other mutual-inductance-based techniques, the measured voltage has to be proportional to the time-domain derivative of the current. This corresponds, in the frequency domain, to V_2 not being subjected to linear distortion with respect to $j\omega I_1$. Therefore, the magnitude of the transimpedance ($|Z_{21}|$) has to be proportional to the angular frequency, ω, while the phase must reach 90° as ω tends to zero. Consequently, phase and amplitude distortion can be observed in a similar way as with the resistive shunt sensing. Also, in both cases, a constant group delay is not considered distortion. The transimpedance of

the circuit in Fig. 3.2(c), using the same parameters as in (Wang *et al.*, 2018), normalized over the mutual inductance L_{m}, and its deviation from ideal inductive behavior in that circuit are depicted in Fig. 3.2(d). The amplitude and phase distortions are formally defined by (3.4) and (3.3) respectively, where L_{m} is a constant mutual inductance.

$$Distortion_{[\mathrm{dB}]} = \left| 20 \times \log_{10} \left(\left| \frac{Z_{21}(f)}{2\pi f L_{\mathrm{m}}} \right| \right) \right| \tag{3.4}$$

In summary, there is a need to assess $Z_{21}(f)$ in order to obtain a better picture of the quality of current measurement and the bandwidth at which those measurements are valid.

3.2 The Proposed Transmission-Line-Based Technique

The principle behind our proposed transmission-line-based current measurement technique is to use a substrate-embedded mutual inductance coupling mechanism to propagate the measured current (I_1) as a voltage (V_2) to the probe through a transmission line of length l_2, as shown by the simplified physical structure in Fig. 3.3(a) and (b). The magnetic flux generated by current I_1 is coupled into a buried microstrip line of length l_2, referred to as *secondary*. The microstrip line propagates the coupled signal to the probe located where voltage V_2 is measured. The current I_1 is the one flowing at the low-side source of a half-bridge made up of transistors Q1 and Q2. That I_1 current branch is referred to as *primary*. The secondary is made up of three distinct sections. The first segment of length l_0 represents a path towards a Via_2 connected to the ground plane of the transmission line. That section has, in theory, no coupling to the primary. The second segment, of length $l_1 - l_0$, represents the part of the secondary that is coupled to the primary. As will be analyzed, both capacitive and inductive coupling to the primary are present and affect the ability of the transmission-line structure to accurately measure I_1. The third segment, of length $l_2 - l_1$, represents a microstrip line to the probe V_2, which is terminated with impedance Z_0, the characteristic impedance of the microstrip line, series with Via_4.

Three layers are required for the structure: both the primary and secondary share the third layer, the GND plane, as the current return mechanism. The primary generally occupies the top layer, because it is part of the power loop, which is often, for practical purposes, placed on that layer. The secondary is placed underneath the primary, on the second layer from the top, in order to maximize the inductive coupling. Indeed, having the secondary current loop part of the primary current loop ensures that a significant portion of the magnetic flux generated by I_1 enters the secondary current loop, thereby leading to the inductive coupling. However, capacitive coupling is also present between the primary and secondary due to the fact that the primary is superposed atop the secondary. A fundamental difference with the pickup coil technique is that the inductive coupling is maximized through a secondary in the form of a terminated microstrip line. In the pickup coil technique, it is rather a single-winding coil terminated with a high-impedance probe that serves as capturing the magnetic flux from the primary. Transmission-line principles are used in the following section to analyze the broadband behavior, including the impact of the aforementioned capacitive coupling, derive design guidelines and show the main advantages of the transmission-line-based structure over other techniques such as the pickup coil.

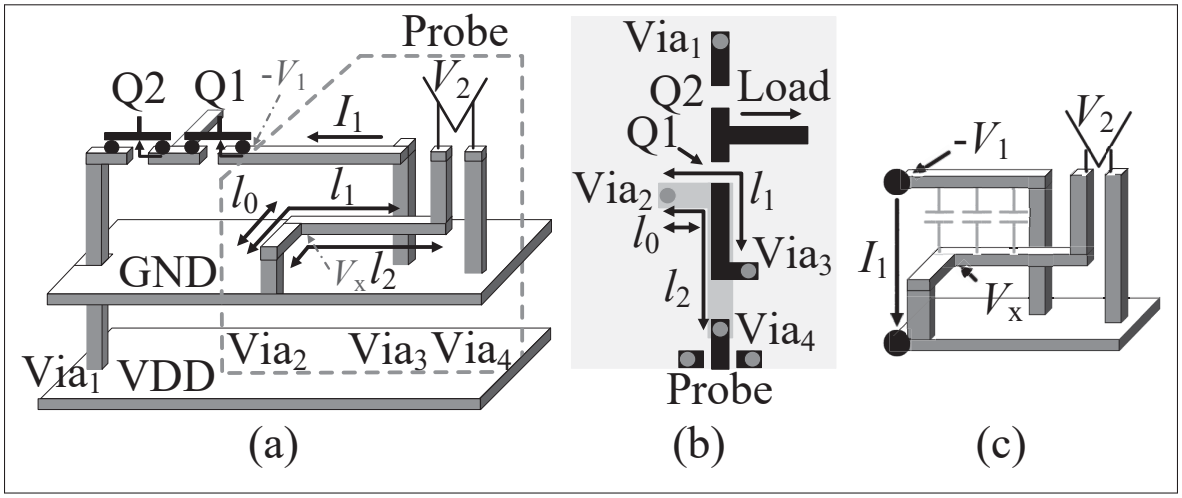

Figure 3.3 Simplified views of the transmission-line-based structure in a switch-mode converter: (a) 3D view, (b) top view, (c) analyzed section of the structure: gray dashed section in (a)

3.2.1 Distributed-Circuit Analysis of the Transmission-Line-Based Technique

The section within gray dashed lines of the transmission-line-based structure in Figure 3.3(a), depicted in Figure 3.3(c), is represented as an equivalent distributed circuit in Figure 3.4(a). The port P1, from which current I_1 flows and where a voltage V_1 is present, defines a reference port of interest, at the location where the source terminal of Q1 is connected to the transmission-line-based structure's primary. The voltage sources in Figure 3.4(a) represent the induced voltages from inductive coupling effects distributed over length l_1, while the current sources represent the displacement currents from capacitive coupling effects through the PCB dielectric, entering the secondary and distributed over that same length. The different elementary capacitors (C_0) and inductors (L_0) at the secondary can be replaced with a lossless transmission-line model. The secondary is terminated with a via, modeled as an inductor (L_{via}), and an impedance-matched probe, modeled as a resistor (Z_{probe}). Given that the circuit of Figure 3.4(a) is linear and time-invariant, each of the induced elementary voltage source can be individually analyzed, as a function of their distance, referred to as l, from the Via_2. The above assumptions allow representing the voltage-induced effects in Figure 3.4(a) by the equivalent elementary circuit of Figure 3.4(b). Regarding the elementary current sources representing the capacitive effects, these depend on the voltage variation between the primary and secondary of the microstrip line. One way to represent these effects at a specific location on the secondary is the use of a voltage $-V_1$, which is the voltage on the primary, driving the mutual capacitance C_{m} from the primary. According to Figure 3.3(c), I_1 represents the current to be measured, which is between the ground plane and primary part in the transmission-line-based structure on top of where Via_2 is located. By definition, voltage V_1 is therefore $I_1 Z_{11}$, where Z_{11} is the power loop self-impedance seen from the port into which current I_1 flows. Accordingly, the equivalent circuit used for each elementary current source is the one of Figure 3.4(c).

A more precise analysis would not consider the voltage to be equal to $-V_1$ across the length of the line, but a distributed model representative of the physical structure would rather be used. For instance, when the voltage on the primary is measured closer to Via_3, it approaches 0 V. For such an irregular structure (Figure 3.3), it is not trivial to formulate the voltage on the primary

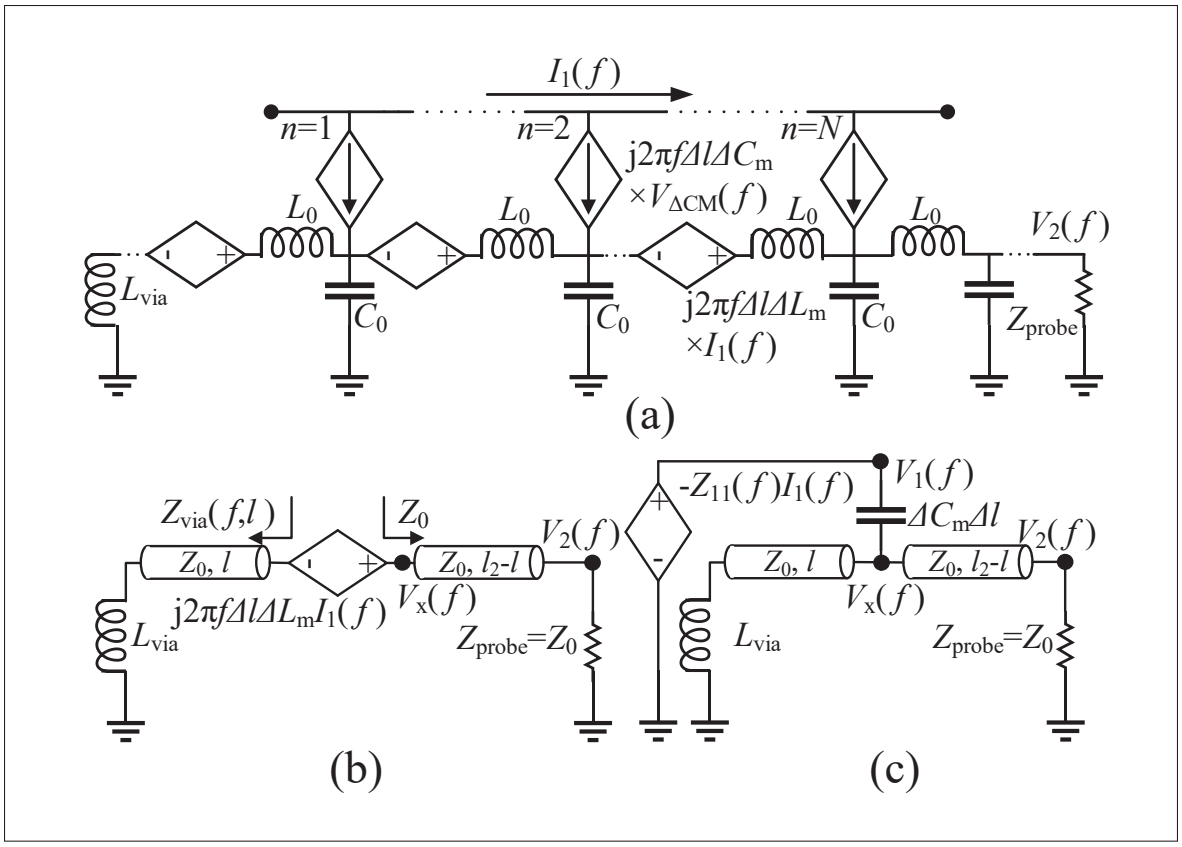

Figure 3.4 Equivalent circuit of the structure in Figure 3.3(c): (a) distributed model of the circuit, (b) equivalent circuit for inductive effects and (c) equivalent circuit for capacitive effects

as a function of distance from Via_3. Instead, the approximation using voltage $-V_1$ is useful and sufficient for the goal of this section, which is to focus on how measurement distortion and bandwidth are related to the lengths in the coupling structure as well as the impact of capacitive and inductive effects as frequency increases. Note also that the length of the segment being significantly less than $\lambda/4$, this constant-voltage approximation of $-V_1$ remains a reasonable assumption for this goal.

In the two equivalent circuits shown in figures 3.4(b) and (c), a transmission line with characteristic impedance Z_0 transforms the impedance of a load Z_L at the end of a d-long line with propagation speed c_ϵ according to (3.5) (Pozar, 2011). In that case, the impedance of the via under the transmission line becomes Z_via (3.6). In the case where the load is matched to Z_0, the impedance

seen from the node V_{X} is Z_0 and constant over frequency. The transformed voltage at the probe (V_2) from the node connected to the current or voltage source (V_{X}) under matched condition is represented by a delay depending on the length d of the line (3.7).

$$Z_{\mathrm{eq}}(f,d) = Z_0 \frac{Z_L + \mathrm{j}Z_0 \tan(2\pi df/c_\epsilon)}{Z_0 + \mathrm{j}Z_L \tan(2\pi df/c_\epsilon)} \tag{3.5}$$

$$Z_{\mathrm{via}}(f,d) = Z_0 \frac{\mathrm{j}2\pi f L_{\mathrm{via}} + \mathrm{j}Z_0 \tan(2\pi df/c_\epsilon)}{Z_0 - 2\pi f L_{\mathrm{via}} \tan(2\pi df/c_\epsilon)} \tag{3.6}$$

$$\frac{V_2(f)}{V_{\mathrm{X}}(f)} = \exp(-\mathrm{j}2\pi f d/c_\epsilon) \tag{3.7}$$

Using those equations and equivalent circuits, the impact on the probe termination of each elementary current source ΔV_{LC} and each elementary voltage source ΔV_{LL} are calculated with (3.8) and (3.9) respectively. The length of the elementary segment is represented by Δl.

$$\begin{aligned}\Delta V_{\mathrm{LC}}(f,l,\Delta l) = &- I_1(f) Z_{11}(f) \times \frac{Z_{\mathrm{via}}(f,l) || Z_0}{\frac{1}{\mathrm{j}2\pi\Delta C_{\mathrm{m}}\Delta l f} + Z_{\mathrm{via}}(f,l) || Z_0} \\ &\times \exp(-\mathrm{j}2\pi f(l_2 - l)/c_\epsilon)\end{aligned} \tag{3.8}$$

$$\Delta V_{\mathrm{LL}}(f,l,\Delta l) = I_1(f)\mathrm{j}2\pi f \Delta L_{\mathrm{m}} \Delta l \frac{Z_0}{Z_0 + Z_{\mathrm{via}}(f,l)} \times \exp(-\mathrm{j}2\pi f(l_2 - l)/c_\epsilon) \tag{3.9}$$

Using the superposition property from linear time-invariant (LTI) systems, the capacitive and inductive effects are summed from distance l_0 to l_1 (Figure 3.3(b)), which represent respectively the beginning and the end of the superimposed lines with their distance relative to the position

of the via termination on the secondary side (Via_2). This allows the calculation of Z_{21} (3.10) in the form of a summation of N segments over length l_0 to l_1 from Via_2.

$$Z_{21}(f) = \frac{\sum_{n=1}^{N} \Delta V_{\text{LC}}(f, l_0 + n\frac{l_1-l_0}{N}, \frac{l_1-l_0}{N})}{I_1(f)} + \frac{\sum_{n=1}^{N} \Delta V_{\text{LL}}(f, l_0 + n\frac{l_1-l_0}{N}, \frac{l_1-l_0}{N})}{I_1(f)} \tag{3.10}$$

The expression of $Z_{21}(f)$ (3.10) can be used to assess measurement distortion. That expression, as well as the expressions for capacitive and inductive effects (3.8) and (3.9), which are part of $Z_{21}(f)$, are also used in order to obtain insight on several design constraints for the transmission-line-based current measurement structure. Several takeaways from this analysis are provided.

3.2.2 Main Takeaways of the Analysis

From (3.8) and (3.9), it can be deduced that increasing the length of the line (l_2) without increasing the length of the rest of the structure (l_0, l_1) does not impact the transimpedance magnitude. This increase only adds a frequency-dependent phase that translates into a constant group delay. Indeed, the exponential terms in (3.8) and (3.9) could be split into two terms, with one of them being a constant when summed over l: $\exp(-\text{j}2\pi f l_2/c_\epsilon)$. That exponential factor can be taken out of the sum in (3.10) and yield a constant group delay. This analytical model clearly shows that increasing l_2 does not impact the measurement distortion of the structure. As a consequence, the probing pads can be placed anywhere on the board without adding measurement distortion as they will only increase the length l_2.

The analysis also highlights two separate mechanisms for coupling onto the secondary line. The main one and most relevant at lower frequencies is the desirable inductive coupling. It can be noted from (3.9) that the system behaves as a mutual inductance until frequencies at which the via impedance ($Z_{\text{via}}(f, d)$) becomes relevant for the further (larger distance d from the via) elementary sources. At those frequencies, the circuit becomes a voltage divider and a band-stop

effect starts to apply, peaking at the frequency at which the electrical length of the line is equal to $\lambda/4 = \frac{c_\epsilon}{4f}$. For elementary current sources, which represent capacitive effects (3.8), they have to be negligible to attain ideal behavior of the structure (with the gain of the term on the second line of (3.8) going towards zero). At low frequencies, the via termination short-circuits those sources at the secondary, canceling any capacitive effect onto the probe termination. At higher frequencies, the impedance $Z_{\text{via}}(f, d)$ (3.6) seen towards the Via_2 increases for further elementary sources from the via termination. The effect at those frequencies is a band-pass effect, peaking when the frequency increases so that the electrical length of the line is equal to $\lambda/4$. Therefore, as the distance increases between the Via_2 and the end of the segment of length l_1, distortion increases because the capacitive effects become more relevant and the inductive effects stray away from their ideal behavior.

In short, several conclusions can be drawn from this analysis:

(C1) Bandwidth is dependent on the length of the structure. While the transmission-line-based structure allows placing the probe at a distance with minimal distortion, maximal bandwidth is achieved when the length of the structure, specifically the parameters l_0 and l_1, are minimized;

(C2) At low frequency, the coupling towards the probe is mainly inductive. As frequency increases, capacitive effects become more relevant. Those capacitive effects are determined by the self-impedance seen at the primary, Z_{11};

(C3) The distance between the probe and the end of the structure, represented by $l_2 - l_1$, does not impact measurement distortion, allowing the designer select any safe probing location.

Coming back to the issues in the literature regarding current measurement techniques, as identified in section 1.2.3, conclusion C1 is of particular importance, because it shows that by reducing the length of the structure, higher bandwidth is achieved, which was one of the needs identified in the literature review. In addition, C3 shows that in terms of probing, it is much simpler to use the transmission-line-based structure because probing overhead can be

brought to a convenient location even in the case of SiP integration. That probing overhead and invasiveness of the current measurement were the other problem identified in the literature.

It is important to recall that one key hypothesis of this analysis is the fact that the voltage over the full length of the primary is approximated as $-V_1$. While such a hypothesis is reasonable for shorter lines and lower frequencies, it is worth comparing the analysis of the structure to EM simulations in order to assess its accuracy over frequency.

3.2.3 Electromagnetic Simulations of the Transmission-Line-Based Technique

The coupled transmission-line-based current measurement structure and its analysis are validated through EM simulations using Keysight ADS software and the S-parameters of P1 and P2 in Figure 3.5 are extracted. The simulated structure shown in Figure 3.3(c) has been laid out in ADS (Figure 3.5). The parameters of Table 3.1, which relate to the fabrication process for the experimental prototype, are used. For instance, the signal velocity, c_ϵ ($1.45 \cdot 10^8$ m/s), is calculated from the relative dielectric constant (ϵ_r) of the FR-4 substrate being 4.3 (3.11). The via inductance (263 pH) is approximated with the via inductance formula from (Johnson, Graham *et al.*, 1993) adapted to metric quantities in (3.12) with a diameter of $d = 200\,\mu$m and a length of $h = 420\,\mu$m (board thickness of the prototype). A thickness of 110 µm separates the top layer and secondary, while 200 µm separates the secondary layer and the ground plane. The mutual inductance per unit length, ΔL_m, is calculated from the nominal mutual inductance of 898 pH in simulations, divided over the length of $l_1 - l_0$ (overlapping length between the primary and the secondary lines). The capacitance per unit length ΔC_m between the primary and secondary is based on the assumption of a parallel plate of a 0.4 mm width and a dielectric layer of a 0.11 mm thickness, including distributed fringing fields, over $l_1 - l_0$.

$$c_\epsilon = \frac{c_0}{\sqrt{\epsilon_\mathrm{r}\mu_\mathrm{r}}} \approx \frac{c_0}{\sqrt{\epsilon_\mathrm{r}}} \tag{3.11}$$

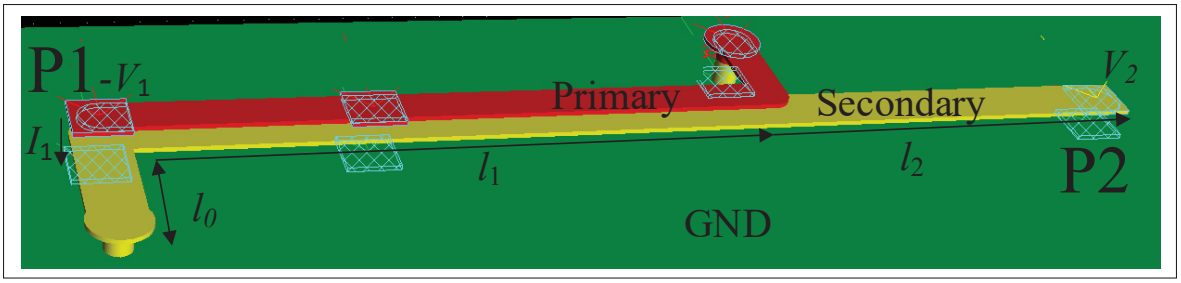

Figure 3.5 Simulated structure for the validation of the analysis

$$L_{\text{via,nH}} = 200h\left[\ln\left(\frac{4h}{d}\right)+1\right] \tag{3.12}$$

The magnitude and phase of Z_{21} shown in Figure 3.6 are extracted from the simulation result and compared with that predicted by the analytical model defined by (3.10), with N=16. The phase and magnitude of Z_{21} plots show consistency with the analytical model (Figure 3.6(a) and (b)) below 3.5 GHz. The total contribution of capacitive ($|\sum \Delta V_{\text{LC}}|$) and inductive ($|\sum \Delta V_{\text{LL}}|$) effects are shown separately in Figure 3.6(c). Predicting Z_{11} is a non-trivial problem given the irregular structure of the primary and its analytical derivation does not add any value to the analysis in this section. Therefore, the Z_{11} used in the analytical formula is the one obtained from simulations, which is provided in Figure 3.6(d) as a reference. It can be observed from Figure 3.6(c) that the capacitive effects become predominant with respect to the inductive effects, at around 2 GHz and the model accurately predicts Z_{21} up to 3.5 GHz. Therefore, the onset of the capacitive effects are properly predicted. However, it is observed that past that frequency, the model starts to fall off. This is mainly due to the approximation done for capacitive coupling, where the primary voltage is estimated to $-V_1$ over the total length of the primary, rather than being a length-dependent voltage, which would reflect the wavelike behavior on the primary at higher frequencies.

As the simulations show, at frequencies at which capacitive coupling between the primary and secondary onsets, the model holds accurately, thereby supporting the main analysis of the transmission-line-based structure. It also supports the hypothesis of the primary voltage being

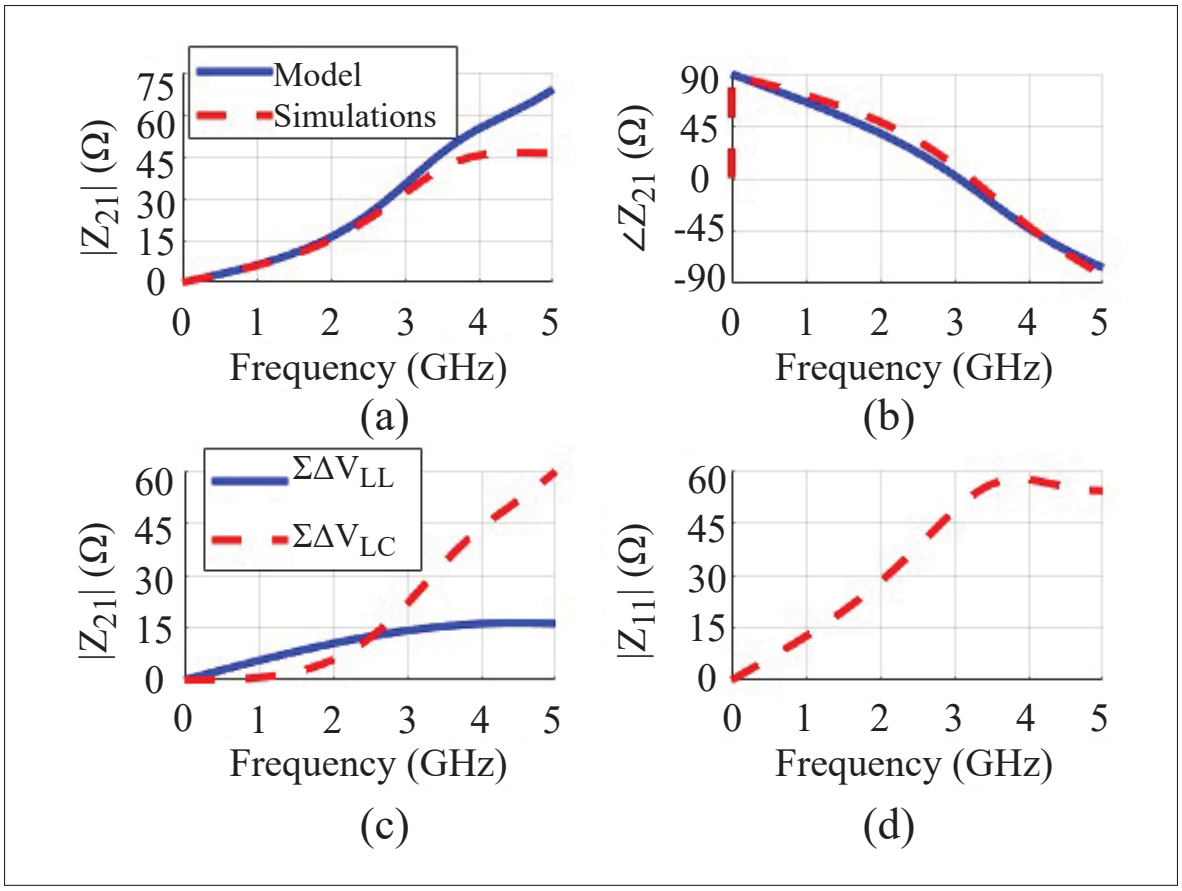

Figure 3.6 (a) EM simulation results compared with the analytical model for $|Z_{21}|$, (b) $\angle Z_{21}$, (c) the contribution of both capacitive and inductive effects to Z_{21} and (d) simulation results of $|Z_{11}|$

Table 3.1 Design parameters used for EM simulations of the current measurement structure in Figure 3.3

Parameter	**Value**	**Parameter**	**Value**
l_0	1 mm	c_ϵ	$1.45 \cdot 10^8$ m/s
l_1	6 mm	L_{via}	263 pH
l_2	9 mm	ΔL_{M}	180 pH/mm
Z_0	50 Ω	ΔC_{M}	181 fF/mm

at $-V_1$ over its length. However, at higher frequencies, it can be deduced from the simulations that the model starts to be inaccurate. It can be concluded that the analytical model presented in

this section and its main takeaways are supported by the simulation results, because the onset of capacitive effects also concur with the end of the accurate bandwidth of the structure. In order to further validate the current measurements made by the structure, an experimental apparatus for the structure is presented.

3.3 Experimental Apparatus for Current Measurement Techniques in Switch-Mode Converters

The three conclusions C1-C3 drawn in section 3.2.2 are used to design a prototype to validate the transmission-line-based structure. As depicted in the circuit-level schematic of the current measurement structure and converter circuit under test in Figure 3.7, the GaN HEMT devices EPC2037 for the low- and high-side, represented respectively by Q1 and Q2, are used along with an LMG1205 gate driver to implement a buck converter. The structure is implemented series with a current shunt resistor at the source of Q1. The circuit was implemented on PCB, driven with a PC, an FPGA development board and the switching currents were measured using a probing station, as depicted in the complete setup photo of Figure 3.8. This section takes an in-depth look at that experimental measurement apparatus. The design of the fabricated PCB is presented in Appendix I, section 1.

First, the dimensions and design constraints for the implementation of the transmission-line-based techniques are presented and justified, including the design particularity of the use of a ferrite bead. Then, a resistive shunt probing apparatus for the validation of the transmission-line-based current measurement structure is presented. Next, the setup for the characterization of measurement distortion is introduced. Finally, the setup for the time-domain measurement of current with both the resistive shunt and transmission-line-based structure is explained.

3.3.1 Dimensions of the Transmission-Line-Based Technique

In order to properly terminate the measurement port (P2 in Figure 3.7, corresponding to V_2 in Figure 3.3), the trace width of 0.4 mm at the secondary side of the coupled transmission-line-based structure is selected for a trace characteristic impedance of 50 Ω. The parameter l_1 in

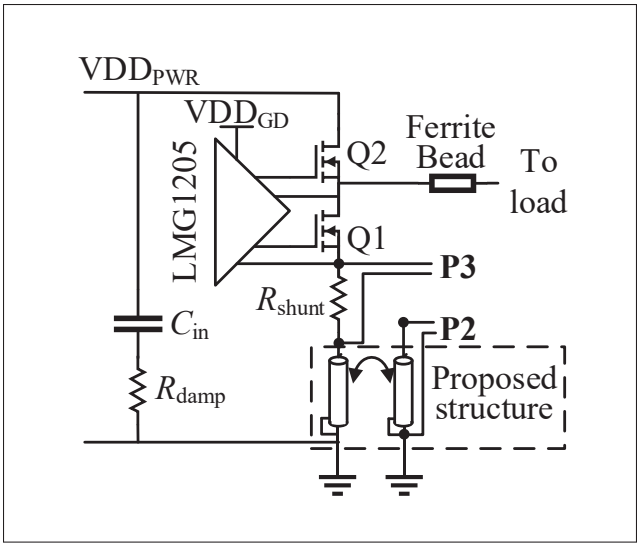

Figure 3.7 Switch-mode converter circuit and transmission-line-based structure implemented on the PCB prototype

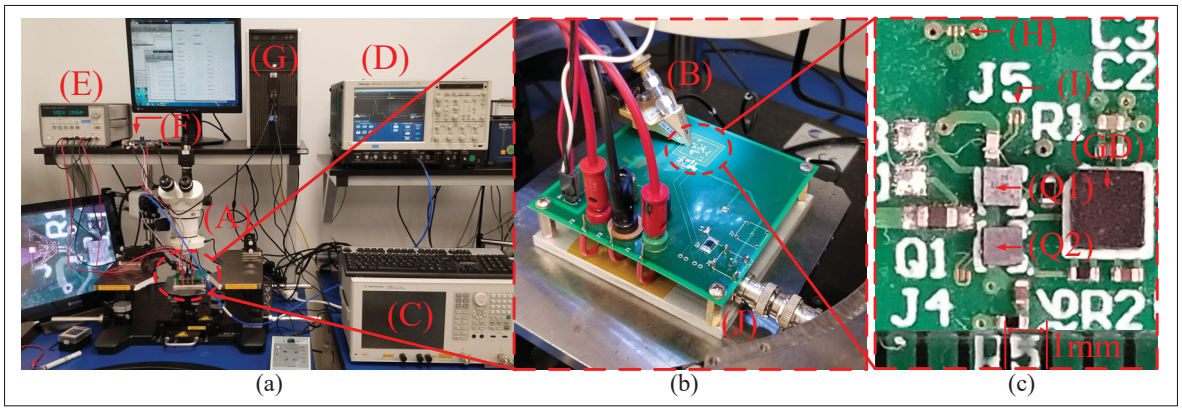

Figure 3.8 Measurement apparatus for time-domain measurements : (a) whole setup, (b) board prototype and (c) the switch-mode converter with the transmission-line-based measurement structure

Figure 3.3 determines the impact of the transmission line effects on the current measurements (conclusion C1 in section 3.2.2). A length of 1.6 mm for $l_1 - l_0$ is selected in order to obtain a measurable coupling and GHz-range bandwidth. Due to the Via_2 of Figure 3.3 being placed at a distance of the power loop, the length of l_0 is 1 mm. With the distance of the probing pad not

impacting measurement distortion (C3), the length l_2 is 4.2 mm in order to measure in a safe probing location. Another particularity of the measurement apparatus is the use of a ferrite bead to ensure ideal current source behavior from the CCM load and the use of the damping resistor in series with the input resistor (C_{in} in Fig.3.7).

3.3.2 Use of a Damping Resistor for Increased Accuracy

Capacitive effects are dependent on the power loop self-impedance Z_{11} (conclusions of section 3.2.2). Furthermore, when dealing with decoupling capacitors and decoupling networks, there is a risk of parallel resonance between the parasitic inductance of a given capacitor and the capacitance of another one, leading to anti-resonance and therefore a peak in Z_{11} at that resonance frequency. One way to prevent that problem, therefore avoiding inaccuracies of the current measurement technique at a given frequency dependent on the decoupling network, it is practical to put decoupling capacitors in series with a damping resistor with a value of a few ohms. That situation of anti-resonance is depicted in Figure 3.9: the drain of the transistor Q2 in Figure 3.7 is connected to a PDN, made of the source of power on the board, e.g., a large bulk decoupling capacitor, the parallel plane capacitance between the VDD and GND series with the connecting via and a local decoupling capacitor (C_{in}). At a given frequency, in this example without damping, the frequency at which the source reactance (i.e., the lead reactance of the bulk capacitor) and the reactance of C_{in} are equal, there will be parallel resonance leading to a peak of impedance seen from the drain of Q2, $|Z|$, equal to the reactance of C_{plane} at that given frequency. By using a damping resistor series with C_{in} (R_{damp} in Figure 3.7), the quality factor of that parallel resonance is decreased, leading to also a reduction in the peak. That allows a given target power loop self-impedance, Z_{11} to be reached at every frequency.

3.3.3 Ferrite Bead for Ideal Current Source Behavior

A ferrite bead is implemented at the switching node to ensure that no flow of current, other than the load current, goes through the output branch. Ensuring that no current except for the load current flows through the output branch has several advantages, which are described in

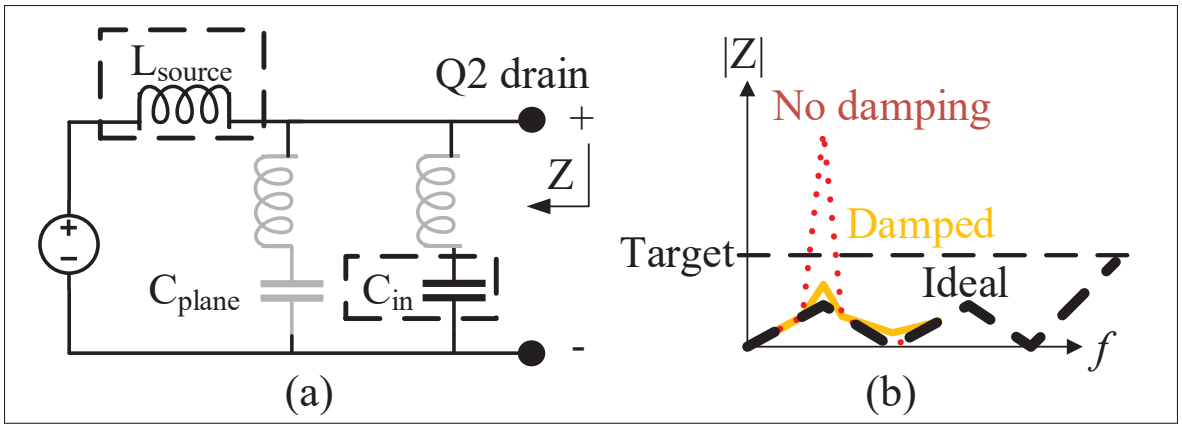

Figure 3.9 Effect of Damping Resistor on Power Loop Self-Impedance

this section. In order to justify the use of the ferrite bead, its effect first has to be explained. Ferrite beads are coils with a ferrite core at their center. When a magnetic flux is generated by the current flowing through the coil, that magnetic flux leads to eddy currents within the ferrite core. Those eddy current serve as a high-frequency loss mechanism within the ferrite bead. Such loss mechanism is the main reason for the use of a ferrite bead in the current application: resistive impedance at high frequency. Indeed, while an inductor would have an imaginary impedance at high frequency, a ferrite bead is lossy and has a real (resistive) component to its impedance. Therefore, if the load cables and the load itself at a given frequency lead to a purely imaginary capacitive impedance in a similar order of magnitude as the inductor, ringing at the load, and therefore loading effects, would occur. On the other hand, a ferrite bead would keep an acceptable impedance at high frequency due to its resistive nature.

The ferrite bead therefore isolates the converter from the load at those frequencies, while not impacting the converter operation when it switches at frequencies in the range of a few MHz. This ensures that no loading effect at hundreds of MHz or GHz range affect the behavior of the converter depending on the load and that it behaves as an ideal current source over a frequency spectrum of a few GHz.

In the context of current measurement, there are several advantages to having an ideal current source as the load:

- **CM currents:** In a context where the need is to measure the DM current such as for the PI assessment model presented in chapter 4, having a high impedance load prevents the flow of high-frequency common-mode currents into the load. That situation is further explained in section 4.1.3. This leads to the measurement of DM currents when either taking the high-side drain branch or the low-side source branch as the primary with the transmission-line-based structure.
- **Load-independent:** When doing system-level characterization, it is not necessarily practical to characterize with a given load. In fact, characterizing DM switching current as a function of only current ensures that loading effects only depend on current and not load passive behavior. This leads to PI assessment and current measurement on a converter based only on load current rather than several unpredictable factors that may affect the current such as cable lengths or load CM/DM impedance.
- **Prevent ringing:** In the CPIOS design, it prevents noise due to the ringing of a given load to affect other converters that are connected to the same supply rail. As a matter of fact, when self-resonance occurs on the load due, for instance, to its inductance and parasitic capacitance or to $\lambda/4$ resonance on the cables, the converter draws a current with a strong component at the self-resonant frequency of that load. This leads to propagation on the power rails of the converters and then leads to voltage fluctuations onto the power rails of other converters or sensitive circuits with coupling to those power rails.

It can be concluded from the above advantages that the use of a ferrite bead is both practical in terms of design and for current measurement purposes.

3.3.4 Resistive Shunt Sensing for Validation

Even if current measurements from the transmission-line-based structure are obtained, those have to be compared against a reference current. In this case, the current measured from a resistive current shunt is used. The measured current with the structure is compared with the one based on a $1\,\Omega$ 0201 ($20 \times 10\,\text{mil}^2$) SMD shunt resistor. Note that the CSR is avoided to prevent the large increase in power loop inductance and dimensions of the system. With the

typical L_{ext}=40 pH (Figure 1.1(a)) (Vishay Intertechnology, Inc., 2009) and negligible parasitic inductance (L_{par}) and capacitance (C_{par}), a 4 GHz 3 dB-bandwidth can normally be reached, as depicted in Figure 1.1(a) and formulated in (3.1). However, in practice, as is observed in the measurement, that bandwidth will be less because that model neglects the electrical length of the film resistor and its interconnect trace on the PCB. These and their associated inductance can have a significant impact on the self-impedance of the shunt resistor in the GHz range. That impact is assessed through the metric of measurement distortion. The setup for the characterization of measurement distortion is explained next.

3.3.5 Measurement Setups for the Characterization of the Current Measurement Structures

As described in section 3.1, in order to properly assess measurement distortion and evaluate the mutual inductance of the structure, the transimpedance and self-impedance measurements are done between the aggressor current (i.e., the current through Q1 and Q2 in Figure 3.7) and the voltage at the measurement points of both current sensing structures (P2 and P3 in Figure 3.7) with the characterization setup depicted in Figure 3.10(a). After the distortion characterization, the circuit is configured in DPT configuration. This allows the characterization of turn-on and turn-off characteristics of transistors in the half-bridge high-side (Salcines, Kruglov & Kallfass, 2018; Wang *et al.*, 2018; Danilovic *et al.*, 2011; Li, Videt & Idir, 2015b). The DPT is performed by using synchronous operation with an R_L load, rather than using a purely inductive load and an asynchronous high-side Q2 as done in other works. Switching current measurements from the transmission-line-based structure and shunt resistor are taken during a turn-on event of the transistor Q1 (Figure 3.10(b)). These are referred to as *large signal measurements*. The PDN block in Figure 3.10(a) and (b) represents the different power planes and decoupling capacitors in the system that distribute both the gate driver and the converter power. The Z-parameters are first obtained through the setup of Figure 3.10(a) and de-embedded in order to consider the 50 Ω probe that is used for the time-domain measurement in Figure 3.10(b).

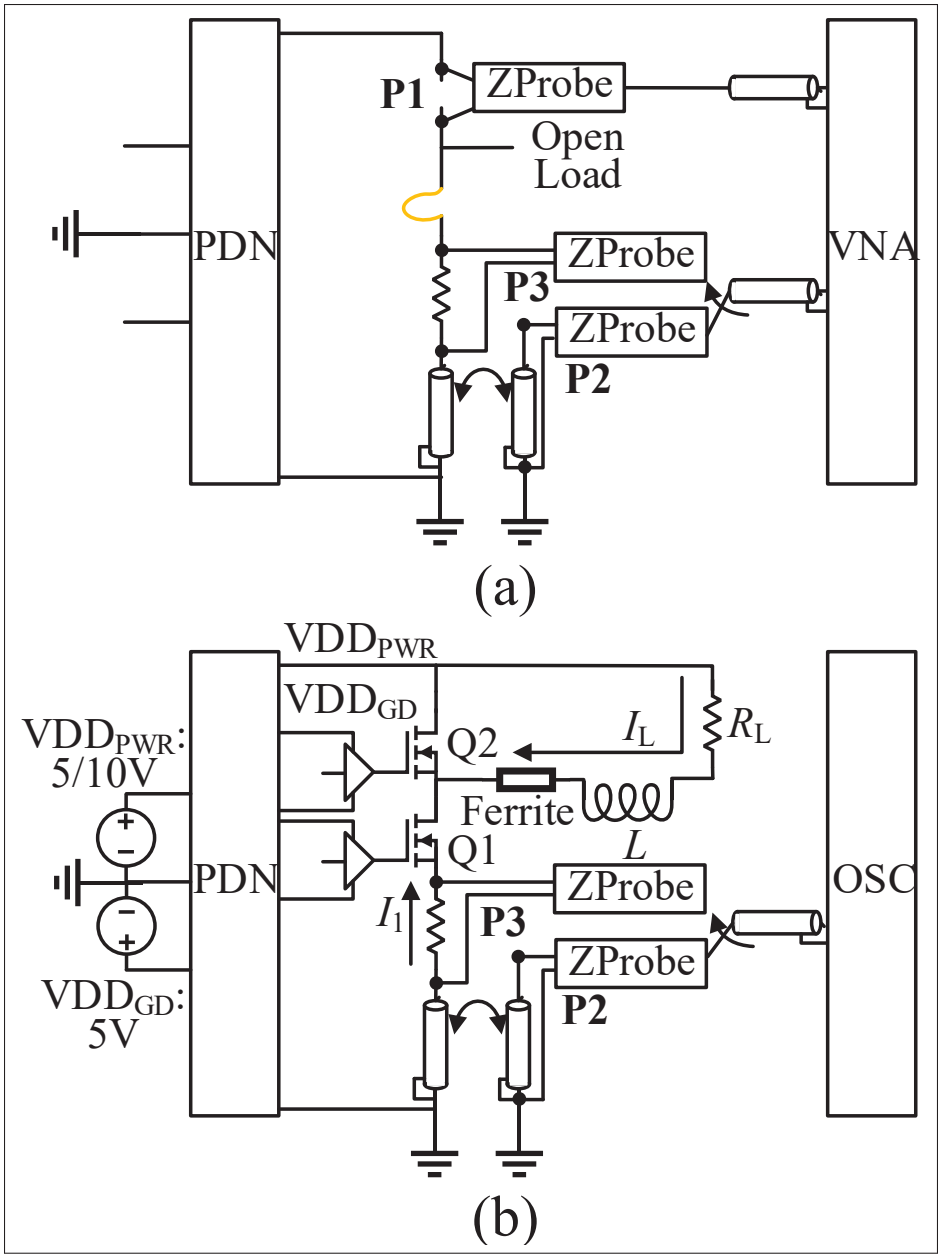

Figure 3.10 Block diagrams of measurement apparatus on the circuit in Figure 3.8 for (a) frequency-domain and (b) and time-domain measurements

3.3.5.1 Measurement Distortion Characterization and Z-Parameters Transformation

Characterization of both current measurement techniques is done through a two-port S-parameter de-embedding and measurement process using a vector network analyzer (VNA), followed

by a Z-parameter conversion. This implies extracting S-parameters between the two pairs of ports P1-P2 (transmission-line-based structure) and P1-P3 (resistive shunt technique), as depicted in Figure 3.10(a). The port P1 is the source of the aggressor current through Q2 and that ultimately needs to be measured with both techniques. Port P2 is at the location of the measured voltage using the transmission-line-based structure, while P3 allows measuring the shunt resistor voltage with the current sense structure. Both P2 and P3 will be represented with the subindex *2* in the results and the remainder of this section when referring to Z-parameters. This means that Z_{21} represents the transimpedance between P1 and either P2 or P3. Using a probe station (A in Figure 3.8), Ground-signal-ground (GSG) ZProbe® coplanar probe heads (B) with 150 µm pitch are laid on a matching pad on the test board and are used for measurements with an E5061B VNA (C). The VNA measurements are de-embedded at the probe heads by using a calibration substrate with Short-Open-Load-Through (SOLT) standards. As shown in Figure 3.10(a), when doing those measurements, the low-side transistor (Q1 in Figure 3.7) is replaced with a short-circuit in the form of a wire bond in order to redirect the current into the resistive shunt and the transmission-line-based structure to measure the voltage at P2 and P3. The high-side transistor is removed and replaced by a VNA port, effectively making it the current source at P1 (I_1). The electrical distance between the source of Q1 and the drain of Q2 is small; hence its impact is not significant. The load is also an open circuit. Therefore, the VNA characterization between port P1 and another port allows characterizing the response in terms of voltage at the other port (such as induced voltage in the case of the transmission-line-based technique) to the current at the source of Q1 through Z-parameters.

The Z-parameters are calculated from the measured S-parameters for both two-port networks P1-P2 and P1-P3 while the third port in each case (P3, P2 respectively) is an open circuit. For the P1-P2 network, Z'_{21} represents a voltage in response to an aggressor current of unity amplitude at P1 assuming a probe behaving like an open circuit at P2. For the P1-P3 network, Z'_{21} represents a voltage in response to the aggressor current assuming the probe is at P3. However, in the time domain, the probe has an impedance of 50 Ω. The loading effect of that probe with impedance Z_{L} on the measurements can be calculated with simple circuit analysis (Figure 3.11), leading to

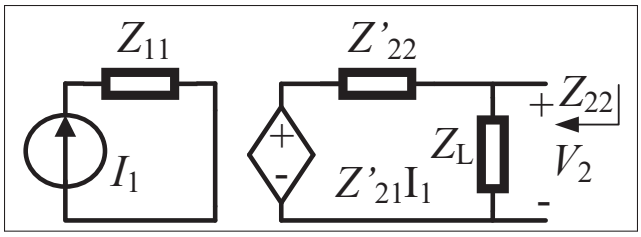

Figure 3.11 Equivalent loaded circuit from the computed two-port Z-parameters

the transformation of the transimpedance Z_{21} in (3.13) and self-impedance Z_{22} in (3.14). In this work, a 50 Ω impedance for Z_{L} is assumed, meaning measurements are taken using a 50 Ω probe. The characterized mutual inductance is obtained by using several measurements of the magnitude of Z_{21} at low frequency and assuming the system is an ideal mutual inductance at those frequencies (3.15). The phase of Z_{21} can be used to characterize the time-domain delay between the current and the voltage measurements at P2 (3.16). Once Z-parameters are obtained and both mutual inductance ($L_{M,\mathrm{char}}(f)$) and delay ($T_{\mathrm{char}}(f)$) are characterized, time domain measurements are performed and those parameters can be used to obtain the aggressor current.

$$Z_{21} = \frac{V_2(f)}{I_1(f)} = Z'_{21}\frac{Z_{\mathrm{L}}}{Z'_{22} + Z_{\mathrm{L}}} \tag{3.13}$$

$$Z_{22} = \frac{Z'_{22}Z_{\mathrm{L}}}{Z'_{22} + Z_{\mathrm{L}}} \tag{3.14}$$

$$L_{M,\mathrm{char}}(f) = \frac{|Z_{21}(f)|}{j2\pi f} \tag{3.15}$$

$$T_{\mathrm{char}}(f) = \frac{-1}{2\pi}\frac{\mathrm{d}\angle Z_{21}(f)}{\mathrm{d}f} \tag{3.16}$$

3.3.6 Time-Domain Current Measurement Setup

In order to perform large signal time-domain measurements of the switching current when the converter is functioning in normal operation with a DC load in CCM, a probe station is used ((A) in Figure 3.8). A GSG ZProbe® probe head (B) is connected to the scope through a SubMiniature A (SMA) cable and the signal is measured by a Tektronix TCA-SMA probe with 50 Ω impedance on a TDS6124C scope (D). The circuit is configured in DPT (Figure 3.10(b)) and powered by an E3631A power supply (E). A Nexys Video FPGA development board (F) configured through USB by a PC (G) sends the driving signal to the gate driver (GD), which drives the transistors Q1 and Q2. The voltage at the ports P2 and P3 are probed when Q2 is turned on using the same 150 µm pitch pads as in VNA measurements (H-I). In order to obtain the current in the time domain at port P1, the voltage at the port P2 is integrated (3.17) considering the characterized mutual inductance $L_{\mathrm{M,char}}$ and delay T_{char}.

$$I_1(t) = I_0 + \int_{t_0}^{t} \frac{V_2(t + T_{\mathrm{char}})}{L_{\mathrm{M,char}}} \mathrm{d}t \tag{3.17}$$

The measurement of the current with the transmission-line-based structure and (3.17) is compared with the resistive shunt measurements. In a turn-on event of Q1, the initial current I_0 is assumed to be 0 A. In the setup for time-domain measurements, there was no way to know the relative time delay of measurements with the resistive shunt and transmission-line-based structures. In fact, both were measured separately, because it is not possible to place a probe head on port P2 (H) and P3 (I) simultaneously without them being in contact (Figure 3.8(c)). Therefore, both measurements are manually aligned in time by applying a delay that would make the peaks of both the resistive shunt measurement and the transmission-line-based structure simultaneous instead of using the time-delay characterization that can be extracted from transimpedance (3.16). The results obtained with the setup introduced in this section are presented next.

3.4 Measurement Results for the Transmission-Line-Based Technique

To assess the distortion in the current measurement structures, Z-parameters are first calculated from S-parameter measurements taken with a VNA. Then, time-domain current waveforms are computed based on voltage measurements at P2 (using (3.17)) and P3 in Figure 3.10(b) using both the transmission-line-based and the shunt resistor structures while the converter is in DPT configuration. The Z_{21} from both structures are also compared against each other in order to validate the behavior of the transmission-line-based structure.

3.4.1 Characterization of Measurement Distortion and Self-Impedance

The measured $|Z_{21}|$ for each structure depicted in Figure 3.10(a) and their theoretically ideal responses over frequency are shown in Figure 3.12(a). The nominal resistivity (1 Ω) is the one of the shunt resistors, while the nominal mutual inductance (340 pH) is characterized by taking the low frequency (0−500 MHz) behavior of the structure (3.15). $\angle Z_{21}$ is displayed in Figure 3.12(b) for the transmission-line-based structure and (c) for the resistive shunt. A nominal delay of 55 ps was characterized with (3.16) at low frequency for the transmission-line-based structure. Figures 3.12(d) and (e) show the calculated measurement distortions according to the definitions in (3.2) to (3.4), i.e., in terms of magnitude and phase deviation calculated from Figure 3.12(a) to (c). Figure 3.12(f) depicts the power loop Z_{11} as well as the reactance of the output capacitance of the low-side transistor (Efficient Power Conversion, 2020) when the drain-source terminals are biased at 5 V.

When observing the transimpedance of the resistive shunt, a significantly larger measurement distortion both in terms of phase and amplitude (Figure 3.12(d) and (e)) is observed at higher frequencies. Indeed, the amplitude distortion of the shunt resistor is 6 dB or larger at 1.67 GHz and higher, with the phase distortion reaching 30°. This observation contrasts with the transmission-line-based structure, which exhibits less than 3 dB amplitude distortion up to a frequency of 1.95 GHz. These results show that the transmission-line-based structure has less

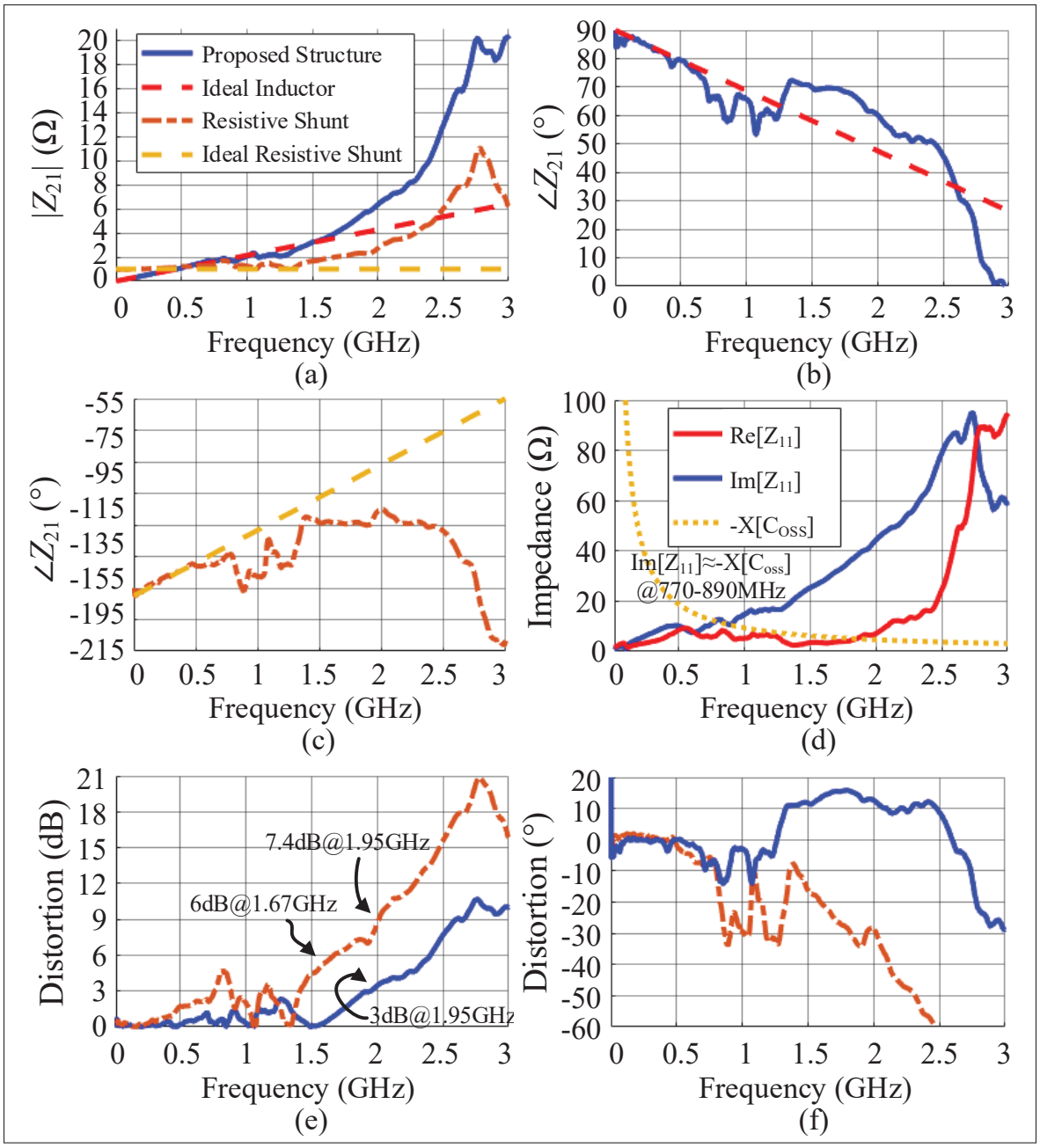

Figure 3.12 Transimpedance Z_{21} measurement results for the shunt resistor and transmission-line-based structures: (a) amplitude, (b) phase for the transmission-line-based structure, (c) phase for the resistive shunt, (d) self-impedance of the power loop, (e) calculated amplitude and (f) phase distortion for the shunt resistor and the transmission-line-based structures

distortion by approximately 5 dB at 1.67 GHz and 4.4 dB at 1.95 GHz, with respect to the shunt structure.

Moreover regarding the self-impedance Z_{11} of the power loop, it can also be observed in Figure 3.12(f) that its imaginary part is equal to the output capacitance of the low-side transistor at approximately 770 to 890 MHz. This means that a peaking in the measured current in the frequency domain should be observed around that frequency due to resonance between the power transistor output capacitance and power loop self-impedance.

3.4.2 Measurement of Currents in a Switch-Mode Converter

Measurements are performed on the converter in Figure 3.10(b) loaded with R_{L}=120 Ω and L=330 µH and biased with $\mathrm{VDD_{PWR}}$ = 5 V and 10 V. The converter is switched with a 50 % duty cycle and a 1 MHz switching frequency. The converter is in DPT configuration and the current through transistor Q1 is measured during its turn-on time. Given that the converter is working in continuous conduction mode and in the operating conditions mentioned above, the load current (I_{L}) will be approximately 21 and 42 mA. Those current values are selected due to the 0201 1 Ω shunt resistor having limited current handling capabilities. The GaN HEMT device-based converter does not exhibit reverse recovery charge. Nevertheless, a large current transient caused by the output capacitance charge on the turn-on and turn-off of the transistor, similar to reverse recovery charge, can still be observed.

The current measured by the transmission-line-based structure is compared to that of the shunt structure with the results shown in Figure 3.13(a) and (d) when biased at 5 V and 10 V respectively. A zoomed-in plot of the results in Figure 3.13(b) and (e) highlights the current pulse, which contains most of the GHz-range content. These time-domain waveforms show that current amplitudes and phases closely match. The normalized energy spectra of these current transients computed by FFT, when a Hamming window is applied, are shown in Figure 3.13(c) and (f). These plots also include the de-embedded spectrum. The de-embedded measurements are calculated by dividing the energy density spectrum by the measured amplitude distortion

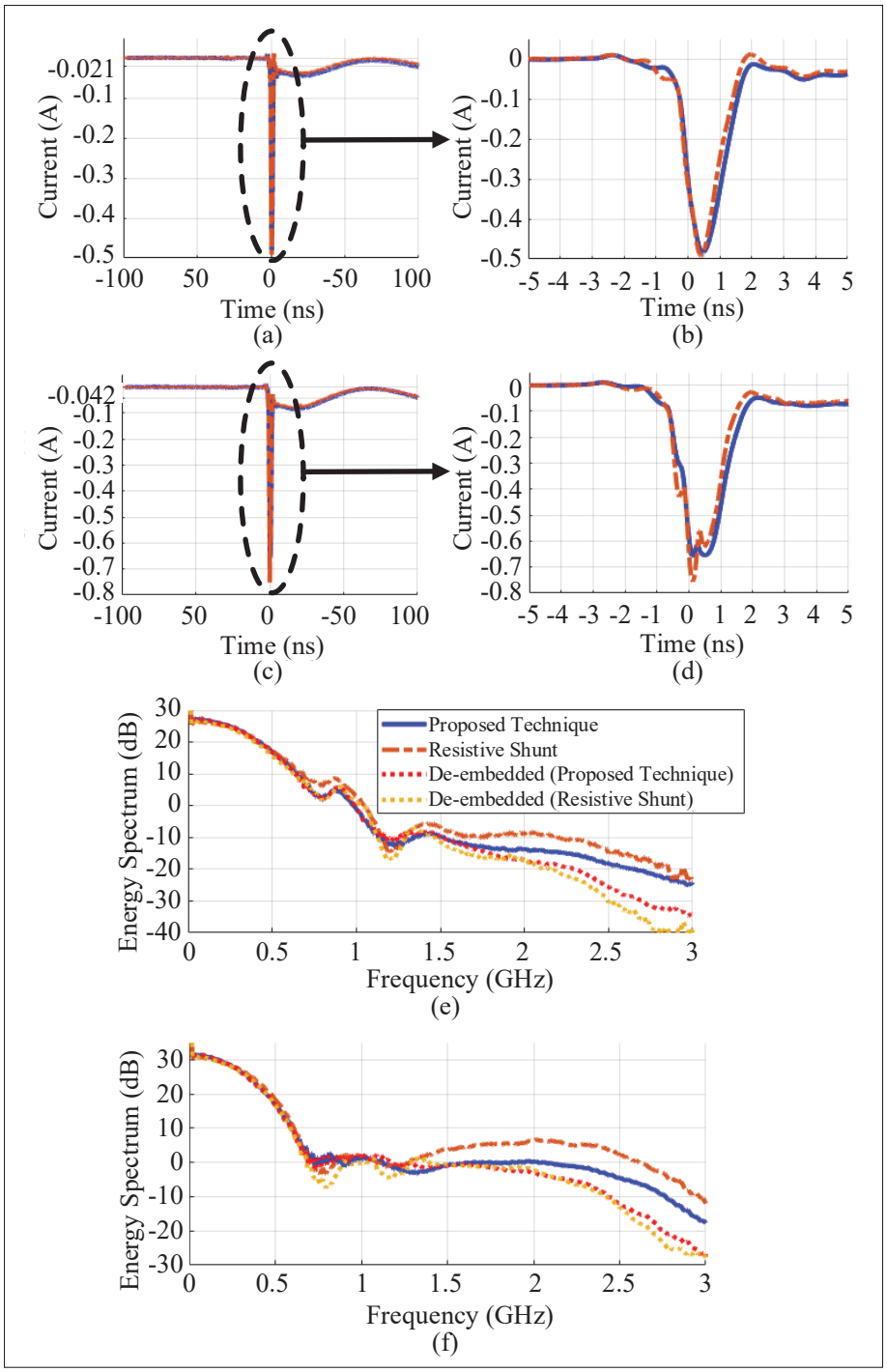

Figure 3.13 Switching currents in time for (a) 5 V and (c) 10 V, zoomed in respectively in (b) and (d) along with their respective energy spectra in (e) and (f)

as per the definition presented in section 3.1. These de-embedded energy spectra are therefore associated to a close approximation of the actual current that is flowing in the transistor Q1. It is observed that over most of the frequency spectrum up to 2 GHz, those two currents are within 2 dB. However, in narrow bandwidths centered at 700 MHz and 1.2 GHz in Figure 3.13(f), the two de-embedded measurements deviate from each other in these narrow bandwidths by 8 dB and 5 dB respectively. Given that these deviations occur over narrow bandwidths only, it is reasonable to conclude that the de-embedded measurements capture the overall spectral distribution and contribute to validating the behavior of the transmission-line-based structure. In the case of the transmission-line-based structure, aside from the aforementioned narrow bandwidths, the embedded and the de-embedded measurements are within 3 dB up to approximately 1.95 GHz. Note also that the time-domain current measurements of Figure 3.13(b) and (e) show very similar measured currents with both techniques, which further confirms that these deviations over narrow bandwidths have limited impact on the ability to measure pulse currents with our technique. It can also be observed on the energy spectrum, in the case of the 5 V bias, that a peak occurs at approximately 800 MHz, in agreement with the self-resonance frequency predicted in section 3.4.1.

3.4.3 Limitations and Drawbacks

Several drawbacks are observed with the transmission-line-based structure. Among those problems, there are namely:

- the imprecision of measurements in narrow bandwidths observed in the measurement results;
- the added parasitic and insertion impedance added by the current measurement structure;
- the layout limitations that the structure entails.

Each of those drawbacks are presented in the following sections.

3.4.3.1 Imprecision of Measurements in Narrow Bandwidths

One hypothesis for the slight discrepancy between de-embedded shunt resistor measurements and de-embedded measurements from the transmission-line-based structure is loading effects. In fact, the time-domain measurements with the current shunt resistor were taken when the secondary of the transmission-line-based structure is in open condition, while the time-domain measurements for the transmission-line-based structure were taken with the secondary loaded by a 50 Ω termination. Such a difference may slightly affect the behavior of the converter when switching, impacting either the quality factor of the ringing in the power loop or its behavior at higher frequencies (2−3 GHz). Another hypothesis that can explain the discrepancy is that the small-signal measurements of the transimpedance, which are used for de-embedding, were taken while the low-side transistor was shorted through wire bonding. In the switching current measurements, the low-side transistor is an actual transistor that is switching. This leads to the self-impedance of the power loop (Z_{11}) to change over time during the switching transient. This change in Z_{11} can affect the measurements taken by the resistive shunt. Another issue with the structure is the added parasitic of that structure, similar to the problem of insertion inductance in the literature. Those added parasitics are simulated for the assessment of their impact.

3.4.3.2 Simulation of Added Parasitics in the Structure

With the transmission-line-based structure being embedded to the converter, even when not characterizing, the converter is still subjected to its impact. While it is desirable that the converter has the same behavior when operating normally as when characterizing, it is important that the structure does not negatively impact the EMC performance of the converter. In that regard, the metric of the self-impedance of the power loop (Z_{11}) is of great importance (Figure 3.12(f)). The transmission-line-based structure requires a 1.6 mm microstrip length between the source of the transistor Q1 and the via leading to the ground plane. This microstrip exhibits transmission-line behavior, which reduces the impact on the low-frequency loop inductance. The impact of that length on the primary equivalent power loop inductance is evaluated.

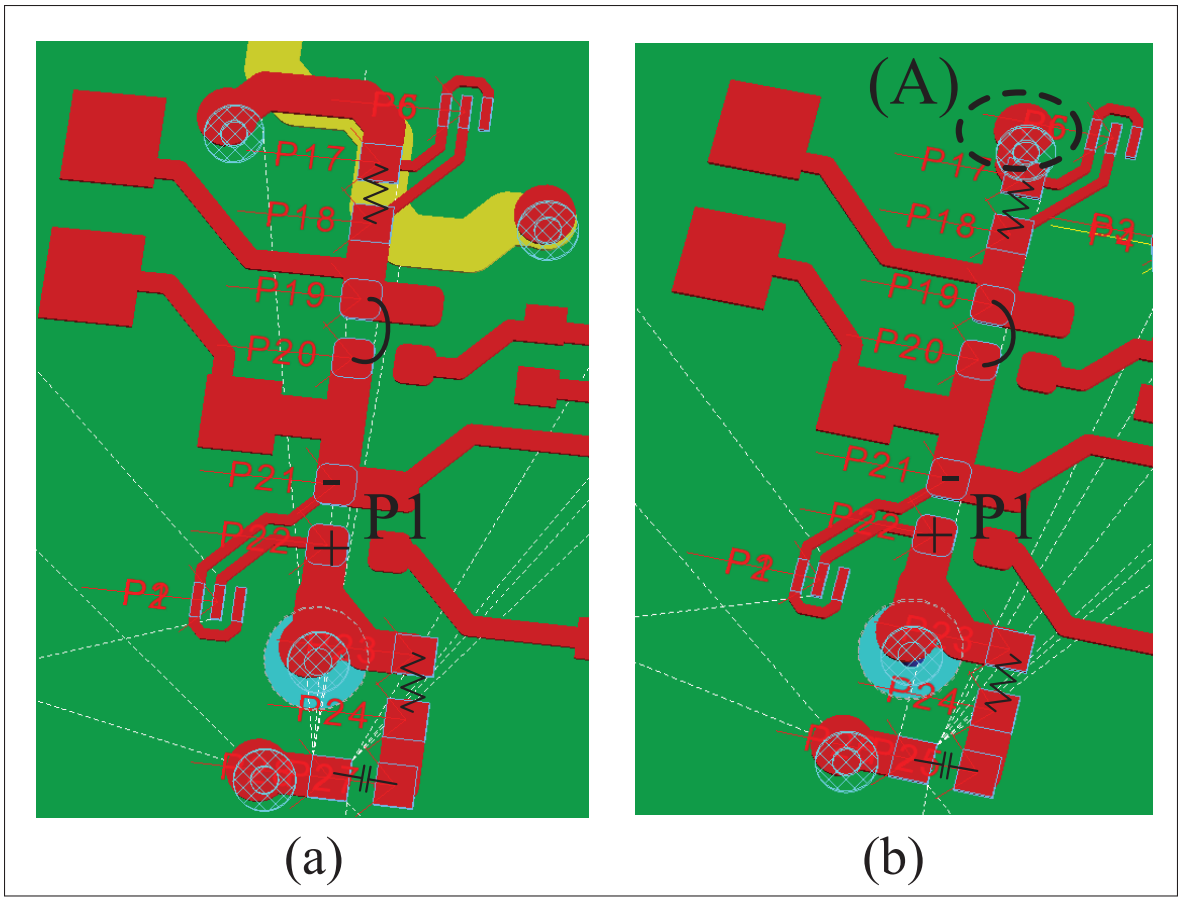

Figure 3.14 Simulation setup for insertion inductance for (a) power loop equivalent inductance with the structure and (b) without the structure

A simulation has been performed at low frequency, i.e., less than 500 MHz, which is way beyond the frequencies at which the converter may be impacted. The layout with and without the transmission-line-based structure are compared, as depicted by the setups of Figure 3.14. The self-impedance of the power loop, Z_{11}, is simulated and the equivalent inductance at low frequency is obtained for both simulations. The equivalent inductance is calculated by measuring the imaginary part of Z_{11} at 500 MHz and dividing it by 2π rad/s. For the simulations with the structure, an equivalent power loop inductance of 2.8 nH was obtained. Without the structure, the equivalent power loop inductance is of 2.4 nH. Therefore, it can be shown in simulations that at low frequencies, a 400 pH inductance is added to the equivalent loop inductance.

The impact of that structure is mostly on the frequency at which transmission line effects occur. Indeed, based on Z_{11} in Figure 3.12(f), it can be observed that resonance occurs at approximately 2.7 GHz. It is hypothesized that the 2.7 GHz is a $\lambda/4$ resonance. Indeed, on an $\epsilon_r = 4.3$ substrate, such a frequency is corresponding to a 1.34 cm power loop length. Such a length is consistent with the dimensions at play in Figure 3.8, especially when considering the shunt resistor and capacitors have longer electrical lengths than their dimensions. If the 1.6 mm trace for the coupling to the secondary of the transmission-line-based structure is removed, the power loop length would go back down to 1.18 cm leading to a $\lambda/4$ resonant frequency of 3.07 GHz.

Circuit level simulations were performed on a half-bridge circuit with an inductance representing the total equivalent power loop inductance series with the voltage source of the converter. The converter drives a current of 1 A. A comparison has been made between a converter with a 1 nH, which is a typical low equivalent power loop inductance, and 1.4 nH power loop inductance. The rise time of the switching node voltage was affected by less than 10 % by that change in power loop inductance. The DM current drawn from the voltage source of the converter was also only slightly affected in terms of the frequency of the ringing, therefore indicating negligible effect on EMC performance. While 10 % increase in rise time may be seen as significant in some applications, in other applications such as the one in this work, requiring a minimally invasive integrated current sensor structure to assess PI in the GHz range, the benefits from the current measurement structure outweigh this 10 % increase in rise time.

It can therefore be concluded that neither the transmission-line effects at high frequencies nor the insertion inductance of the structure add a significant impact on the behavior of a half-bridge that uses the transmission-line-based structure.

3.4.3.3 Layout Limitations

Besides the impact on the rise time, the transmission-line-based structure requires the use of a section of the second layer from the power routing layers (which is typically the top layers) to be reserved for the measurement technique around the power converter, rather than as a ground

plane as would normally be done to reduce the power loop and trace impedance. With the transmission-line-based structure, a full-size ground plane must rather be placed on the third layer from the power routing layers. It is worth mentioning that even though the technique has the aforementioned constraints in terms of PCB design, it does not prevent concurrent load current sensing for control applications. As described in the previous paragraph, the transmission-line-based structure does not significantly affect the behavior of the converter at low frequency. Therefore, in the instance that the technique is used on a system operating in closed-loop operation, the impact on control, which is typically limited to below a few MHz, would be minimal.

3.4.4 Comparison With the State-of-the-Art

The transmission-line-based structure is compared with previous work and a commercial CSP in Table 3.2. The table does not consider CSR since it is impractical for SiP applications, besides its undesirable insertion inductance and added losses. For the work (Wang *et al.*, 2018), only the best performance pickup coil prototype that does not include the CSR, which adds significant parasitic lead inductance to the power loop, is considered. It is noticeable that better mutual inductance (340 pH) is achieved in this work, with a shorter length of structure. Moreover, the small structure and the matched termination probing at the secondary in this work allow to experimentally achieve a 1.95 GHz bandwidth, which is significantly larger than the best theoretical 840 MHz, extracted by circuit analysis of the pickup coil (Wang *et al.*, 2018). Compared with the commercial CSP, the bandwidth with the transmission-line-based structure is higher while at the same time the area occupied by the probing apparatus is significantly smaller. In fact, when the current is not probed, the area overhead in this work is only due to the 2.6 mm secondary line buried in the PCB, whereas with the commercial solution, a large area without component is required to measure the current as the CSP must be laid flat on the board above the trace, which must be as long as the current probe (10 mm). Finally, when compared with a resistive shunt, the transmission-line-based structure has the advantage of having a much higher current-handling capability.

Table 3.2 Comparison with Previous Works

Characteristic	**This work**	**Pickup coil (Wang *et al.*, 2018)**	**FCC F-97-1**
Mutual Inductance	340 pH	120 pH	N/A
3 dB-bandwidth	1.95 GHz	840 MHz*	1.5 GHz
Length of the structure	2.6 mm	8 mm	10 mm
Probing	Probing pad located anywhere	Close to *pickup coil*	Large componentless area

* Not characterized by authors; estimated from data in (Wang *et al.*, 2018) through circuit analysis

3.5 Conclusion

Our high bandwidth coupled transmission-line-based structure for current measurement in switch-mode converters is presented in this chapter. The distributed-circuit analysis of the transmission-line-based current measurement structure shows that it is more convenient in terms of probing compared to a current surface probe(CSP) and a *pickup coil* as it allows an arbitrary distance between the probing location and the converter. As was shown in the literature review, the convenience of the probing apparatus was a missing aspect in the state-of-the-art. The other missing aspect identified in the literature was with regard to the bandwidth. The lengths of the structure are the main factors that impact its bandwidth (section 3.2.2). The structure is validated by comparing the current measurements with those of a resistive current shunt. By using a VNA, the transimpedance was measured and it showed that it achieved a 3 dB-bandwidth of 1.95 GHz. It is also important to note that the probing of the structure can be done from any convenient point on the substrate. Those results show that we meet the two needs identified in section 2.4 and therefore the specific objective of "characterizing the switching current in power converters for the CPIOS, which are critical for power integrity (O1)" is met. In addition, the structure is more convenient in terms of current handling capability than a shunt resistor. Therefore, the structure allows better power integrity assessments in converters with fast switching times, which

is particularly useful when implementing sensitive analog circuits along with those converters in compact SiP.

In summary, the following contributions were made:

- a coupled transmission-line-based structure for current transient measurements is proposed, backed by a thorough high-frequency analysis demonstrating key trade-offs in such a structure for high-bandwidth measurements;
- a demonstration of a half-bridge switching current measurement over a bandwidth of 1.95 GHz with less than 3 dB amplitude measurement distortion and convenient probing location using our proposed coupled transmission-line-based technique, which is an improvement over state-of-art embedded current-measurement techniques, such as a pickup coil.

For the purpose of characterizing power converters in compact SiP and integrated power systems, the transmission-line-based technique will have a great impact. Indeed, as shown in the literature, the superior bandwidth and convenience of probing locations, even in a compact system, make it a highly useful technique for obtaining DM switching current, which is key to predicting power integrity in highly integrated power systems. It is also expected that this research has a great impact when it comes to characterizing GaN HEMT transistors and WBG technology as a whole. As mentioned in chapter 1, state-of-the-art techniques for measuring the current either also add significant insertion inductance or have a resistive component that impact the behavior of the converter. With the transmission-line-based technique, high characterization bandwidth with low measurement distortion can be reached while having almost no effect on the behavior of the converter.

CHAPTER 4

GHZ-RANGE MODELING OF POWER INTEGRITY IN AN ARRAY OF SIMULTANEOUSLY SWITCHING POWER CONVERTERS

The introduction and the first two chapters of this thesis highlighted a problem regarding the characterization of CPIOS and more generally, arrays of switch-mode converters integrated in the same package with a GHz-range bandwidth. More specifically, there is a need in the literature to assess power integrity in such systems to: under any condition, predict spectral noise power density of multiple converters switching simultaneously to assess performance degradation of the switch-mode converters at up to GHz frequencies; and assess whether we meet breakdown voltage limitations of the IC by predicting the overall shape of the voltage fluctuations. This chapter presents a model for the assessment of power integrity constraints in an array of switch-mode converters.

First, the general idea for the model is presented along with the main hypotheses that come along with that model. Second, the measurement setup for the validation of that model is shown. The model is characterized with switching current measurements, as presented in chapter 3, and Z-parameters of the PDN. Finally, predictions of voltage fluctuations are made by the characterized model and compared with measured voltage fluctuations from the same gate driving excitation as characterized. Predictions are also made under simultaneous switching conditions. The content of this chapter is based on, with extracts from, the last three sections of (Nobert *et al.*, submitted for publication).

4.1 Concept of the Proposed Model for Power Integrity Assessment

The objective of the model presented in this section is to make predictions of voltage fluctuations onto the supply rails of different sensitive circuits, such as ADC, operational amplifiers or other converters with frequencies of interest from the switching frequency, to multiple GHz. More specifically, shape, in order to predict peak voltage fluctuations onto the supply rails is of interest. Also, spectral density mismatch between predictions and actual voltage fluctuations (reference signal), for the proper assessment of performance degradation of the sensitive devices connected

to the supply rails, is important. The main idea of the proposed model is to consider each switch-mode converter as an *aggressor port* (P_{am}), which is the source terminal of the low-side transistor (Q1 in Figure 4.1) and the drain terminal of the high-side transistor (Q2 in Figure 2.2). This aggressor is modeled as a transient current source (i_d), referred to as *switching current* in this section. The time domain characteristics of this switching current have a non-linear dependence on the operating conditions, i.e., the load current upon switching (I_L), input voltage, gate driving strength (R_g) and excitation time ($GD_m(t)$), impedance seen from the power rails (high-side drain and low-side source) of the converter. However, a reasonable hypothesis, which is verified in this paper, is that the half-bridge draws a predictable and measurable DM current transient caused by low-side output capacitance charge and change in the flow of the current upon switching at frequencies at which the model is relevant. Therefore, the inherently non-linear half-bridge behaves as a current source with a given transient waveform in the conditions of known gate driving strength, load current and converter DC input voltage. There are two critical parameters to the model. First, there is the DM transimpedance between the aggressor port and a given victim port (P_{vn}), i.e., the node connected to the power rails of a sensitive device. Then, there is the switching current waveform, dependent on gate driving conditions, load current and input voltage of the half-bridge ($i_d\left(t; \left\{R_g, I_L, V_{DD}\right\}\right)$) at the time of switching. Both can be experimentally measured with time-domain waveforms and S-parameters, as described in section 4.1.4. The voltage fluctuations at the victim port (e.g., power rails of an ADC, gate driver or another converter, as depicted in Figure 4.2) are calculated by doing the frequency-domain product between that transimpedance and the switching current on the half-bridge.

On a physical level, the model can be represented as depicted in Figure 4.2: a PDN block with aggressor ports, where each port $P_{am(+/-)}|1 \leq m \leq M$ is connected to the drain and source terminals of two power transistors within the half-bridge HB_m; victim ports, shown in Figure 4.2 as HB gate drivers (P_{v1}); the supply rails of an ADC (P_{v2}) and the supply and ground rails of another converter (P_{v3}). Currents flowing through any P_{am} can affect the victims (P_{v1}, P_{v2} and P_{v3}) due to couplings within the PDN. For the remainder of this section, the port $P_{vn}|1 \leq n \leq N$ represents a victim that needs to be measured. Note that the ground point from the load is

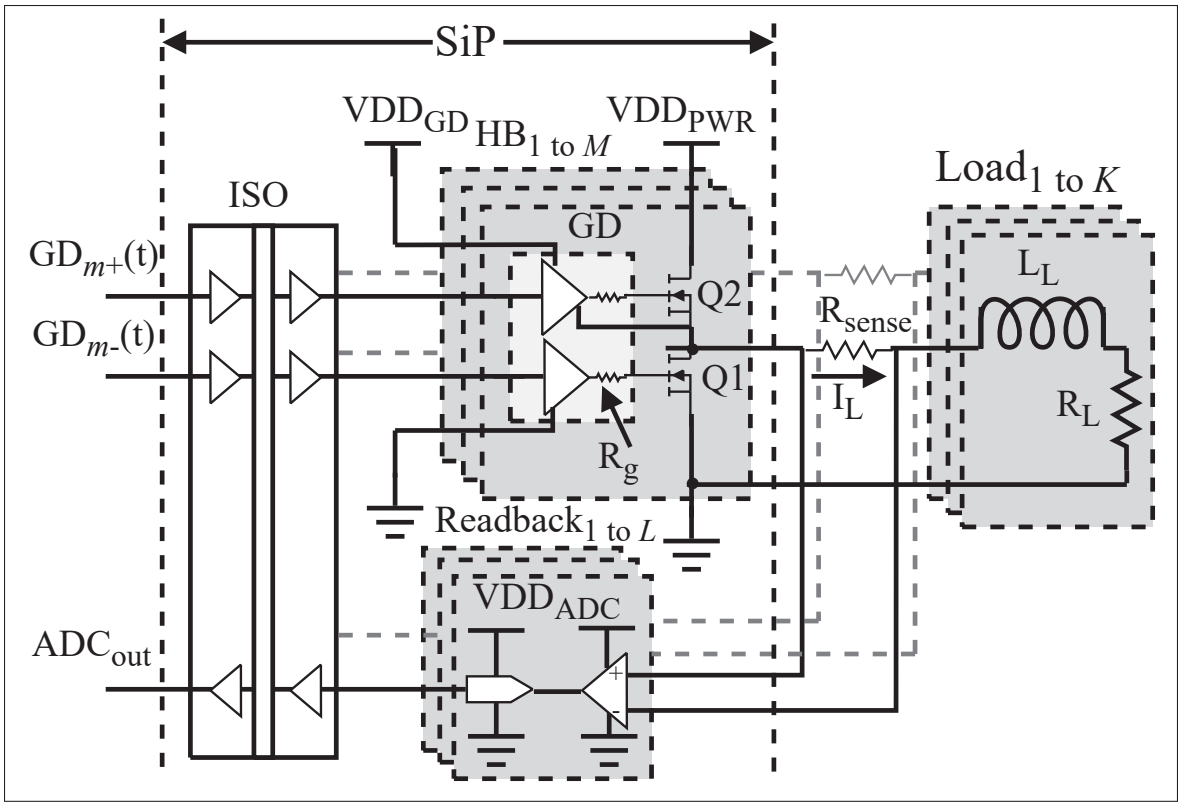

Figure 4.1 Array of M independent half-bridges (HB) in an SiP of configurable switch-mode converters

represented by a common ground point rather than a differential port, because the ground return from the load to the converter path is often more complex to predict.

The parameters of the model are characterized by determining the switching current of every converter under the different operating conditions of each half-bridge ($\mathrm{HB}_m(t)$ in Figure 4.2), $\left\{i_{\mathrm{d},m}\left(t;\left\{R_\mathrm{g}, I_\mathrm{L}, V_\mathrm{DD}\right\}\right) \mid 1 \le m \le M\right\}$, and determining the couplings between aggressors and victim ports, in the form of Z-parameters, as depicted in Figure 4.3. By doing the product between the frequency content of the switching current, $I_\mathrm{d}(f)$, and the transimpedance between a given victim and aggressor, Z_{nm}, a given voltage fluctuation is obtained at a victim n for an aggressor m ($V_{n,m}(f)$, hence $v_{n,m}(t)$). The inputs to the model are the gate driver digital signals $(GD_m(t)|1 \le m \le M)$ and the operating conditions $OP_m(R_\mathrm{g}; I_\mathrm{L}; V_\mathrm{DD})$ of each half-bridge that each gate driver signal controls. Those gate driver signals represent at what time the calculated

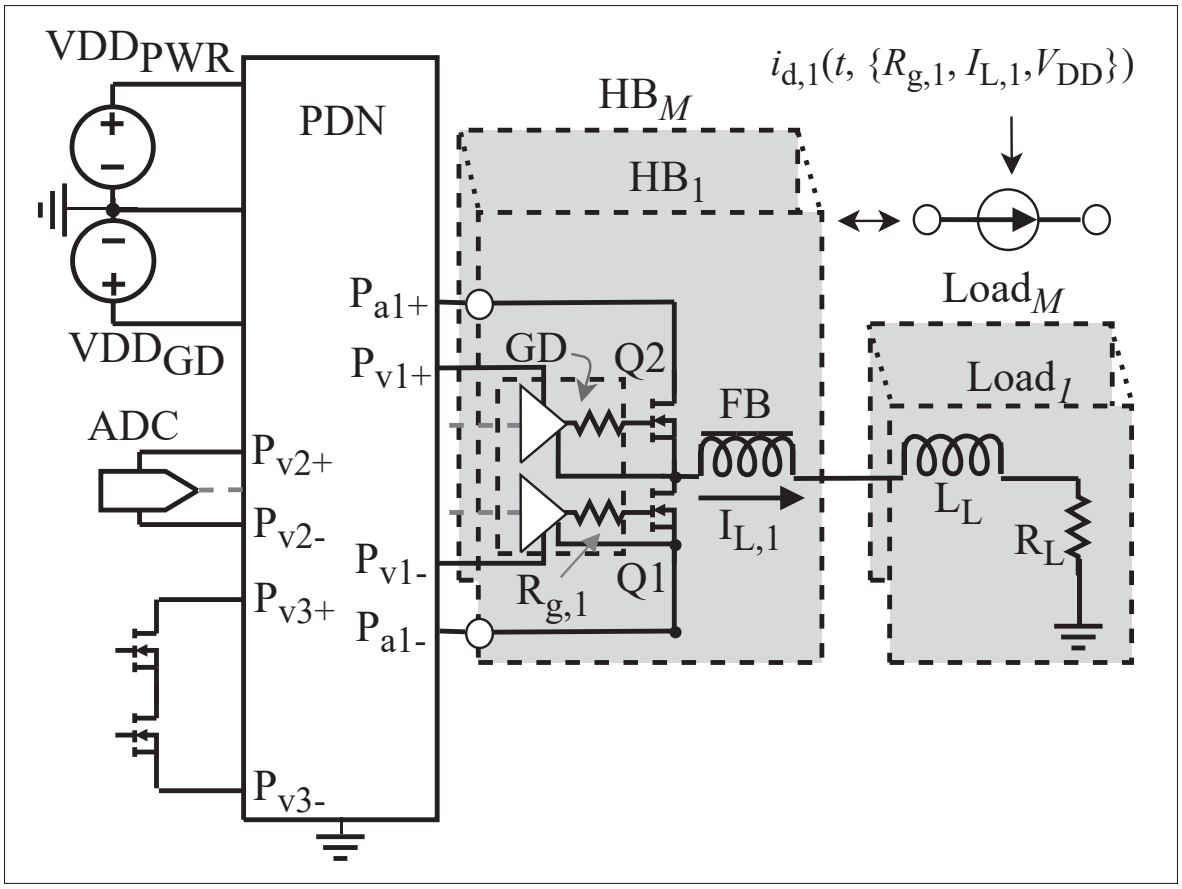

Figure 4.2 Physical representation of the model

voltage fluctuations $v_{n,m}(t)$ are added to the output signals ($v_n(t)$), which symbolize the different voltages coupled to the victims.

4.1.1 Mathematical Formulation of the proposed Model

As is the case in LTI systems, which is a hypothesis justified in the following section, the contribution of the m^{th} half-bridge on the voltage at the n^{th} victim node in the frequency domain, $V_{n,m}(f)$, is represented by (4.1), where $Z_{nm}(f)$ is the transimpedance between the aggressor and the victim. An individual voltage transient in the time domain caused by the switching of the m^{th} half-bridge can be predicted with (4.2) where $\mathcal{F}^{-1}\{\cdot\}$ is the inverse Fourier transform operator. In the case where multiple half-bridges are switching simultaneously, the superposition property of LTI systems is assumed. In that case, the total transient at the n^{th} victim can be calculated

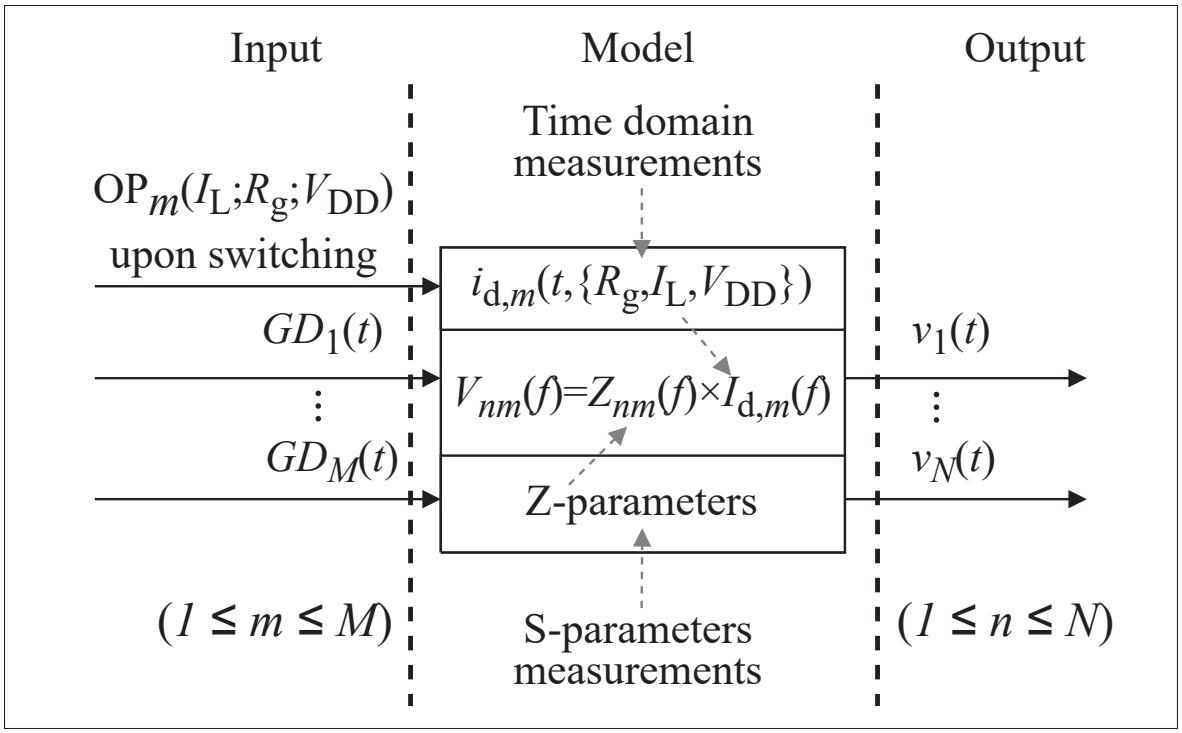

Figure 4.3 High-level diagram of the model

by summing, either in time or frequency domain, each individual transient with a relative time delay of $t_{\mathrm{rel},m}$, which would represent the relative time between the m^{th} gate driver signal and a given reference time t_0. Those summed time-delayed responses are expressed in the Fourier and time domains in (4.3) and (4.4) respectively.

$$V_{n,m}(f) = Z_{nm}(f) I_{\mathrm{d},m}(f, \{R_{\mathrm{g},m}, I_{\mathrm{L},m}, V_{\mathrm{DD},m}\}) \tag{4.1}$$

$$v_{n,m}(t) = \mathcal{F}^{-1}\left\{V_{n,m}(f)\right\} \tag{4.2}$$

$$V_n(f) = \sum_{m=1}^{M} Z_{nm}(f) I_m(f) \exp\left(-j2\pi f t_{\mathrm{rel},m}\right) \tag{4.3}$$

$$v_n(t) = \sum_{m=1}^{M} v_{n,m}(t - t_{\text{rel},m}) \tag{4.4}$$

4.1.2 The Hypothesis of an LTI System

Drawing the hypothesis that the coupling mechanism between the converter and the victim behaves as LTI, as it is done for the model, has several implications. It is assumed that the PDN to which the half-bridge and the victim are connected has LTI behavior under the voltage fluctuations that are predicted. This implies that the impedance seen by the half-bridge on its power rails, or its transimpedance towards the victim, must not change as a function of voltage fluctuations on the power rails or of time, due, for instance, to other half-bridges switching. This hypothesis is validated and the superposition property of (4.3) and (4.4) is verified experimentally, as will be shown in the results of section 4.3. It is also noteworthy to mention that such a hypothesis is also implied, though not explicitly stated in General Terminal Modeling (GTM), where the converter is modeled by a Norton or Thevenin equivalent circuit (Baisden *et al.*, 2010; Liu *et al.*, 2003). Indeed, in GTM, converters are assumed to behave as linear voltage/current DM/CM noise sources, independent of time or noise onto their own power rails, and their coupling towards the LISN (through the PDN) is assumed to be a function of frequency, which is only valid in the case of an LTI PDN.

4.1.2.1 Linearity of Switch-Mode Converters

In order to safely make the assumption that the system behaves as LTI for the currents drawn by the converters and the voltage fluctuations caused by those currents, a reasonable argument for (A) linearity of the power devices that populate the PDN when not switching and (B) time invariance when the power devices are switching must be provided.

First, it is important to remind the impact of the input capacitor (C_{in}) on the converter. As depicted in Figure 2.2, an input capacitor is often placed in parallel with the half-bridge's supply.

In typical applications, the input capacitor ensures that the DM $\mathrm{d}i/\mathrm{d}t$ generated by the converter is drawn from that capacitor, rather than generating voltage ripples on the supply rails due to parasitic inductances and resistance on the PDN (Xie, 2016). Indeed, it plays a similar function to decoupling capacitors in digital systems. It is also important to note that classically, the value of C_{in} is tied to the load current. It is also a reasonable argument to mention that a properly scaled C_{in} should also not be underscaled with respect to the output capacitance of the power device. Indeed, the capacitor C_{in} will provide charge during the switching transient. However, aside from the DM current caused by the change of current flow on the power rails (low-side to high-side on), it is also noteworthy to mention that C_{in} has to provide the charge for the output node and consequently the output capacitance; otherwise it will be drawn from the power rails, thereby generating voltage fluctuations. Therefore, as the dimensions of the transistors will increase, the value of C_{in} will also need to be increased.

Regarding (A), the linearity, it is assumed that each converter operates as a linear device when not switching. Therefore, as seen from the source of the low-side and drain of the high-side, linear behavior must be observed. It is a reasonable assumption that as long as the noise on the power rails is an order of magnitude below the input voltage (V_{DD}). Indeed, an idle converter (not switching) converter would behave as a capacitor (off-state transistor) series with a resistor (on-state transistor). Moreover, the output capacitance (C_{OSS}) is voltage-dependent (non-linear behavior). However, as can be observed for the transistors used in this work, the EPC2037 (Efficient Power Conversion, 2020, Fig. 5) and is true of other devices, a variation of an order of magnitude below the input voltage will only affect the output capacitance by a negligible amount compared with the total output capacitance, hence leading to a linear small-signal capacitive-resistive (RC) behavior.

When a converter is switching, (B), the time invariance of the converter needs to be supported. In that case, the impedance of the switching converter, as seen from the power rails (source of the low-side and drain of the high-side), must not change. While the converter under CCM operation switches, it goes through different operating regions. A half-bridge operating in CCM going from low-side on to high-side on is considered in the following. The high-side transistor

is initially in an open state with capacitance $C_{OSS}(V_{DD})$, while the low-side transistor is closed and behaves as a resistor. The gate of the low-side then turns the channel off and the body diode, or the equivalent mechanism on GaN HEMT, turns on. The body diode exhibits a different behavior than a closed-state transistor, slightly affecting the capacitance seen from power rails as a function of the load current. Then, the high-side gate turns the high-side channel on when the gate-source terminal reaches the threshold voltage. The current starts to flow from the high-side transistor. The high-side transistor is saturated and limited in current by the gate-source voltage, while the body diode conducts the rest of the current. Output node (low-side drain terminal) voltage also begins to rise. The dynamics that influence both switching current and output node voltage during that interval are complex and summarized in (Clemente, Pelly & Isidori, 1982). For the purpose of this analysis, they can be seen as a black box. However, during that interval, the capacitance seen, as a function of time, from the power rails of the transistor may change due to the fluctuation in the output voltage and operating regions of the transistors, leading to time-variant effects. Therefore, time-invariance can no longer be assumed if significant capacitance variation is observed. When the high-side transistor is fully on, the capacitance comes back to its nominal value as a function of V_{DD} ($C_{\mathrm{OSS}}(V_{\mathrm{DD}})$).

The EPC2037 (Efficient Power Conversion, 2020) is used in a simulation that illustrates this behavior and shows the limited impact of the time-variant effects for various operating conditions (Figure 4.4(a)). The converter is loaded with a DC of I_L, switched slowly with an R_{g} of 10 kΩ and a bias voltage of V_{bias} is applied. The simulation is done for (1) an I_L of 10 mA and a V_{bias} of 100 V (Figure 4.4(b)), (2) an I_L of 1 A and V_{bias} of 10 V (Figure 4.4(c)) and finally (3) an I_L of 10 mA and V_{bias} of 10 V (Figure 4.4(d)). A small-signal voltage (ΔV), which is a cosine signal of frequency 2 GHz, is added to the source, at the power rails. The quadrature component of the current I_d relative to ΔV is measured in order to obtain the imaginary part of the impedance seen from the power rails at that frequency. That imaginary part of the impedance is used to estimate the time-varying capacitance seen from the power rails. As it can be observed, for the EPC2037, the capacitance of the power stage only changes by a few picofarads. In addition, that capacitance change may be washed up by the typically significantly larger input

capacitance (C_{in} in Figure 2.6(a), part of the PDN in other figures) of the converter. It therefore is safe to assume that the behavior of other converters will not be affected by a change in the equivalent capacitance shown by the converter as it is switching. Other larger devices can exhibit time-dependent effects that make the capacitance change by a larger amount. However, in those cases the input capacitance to the converter is also scaled accordingly in typical design practices, as explained in the second paragraph of this section.

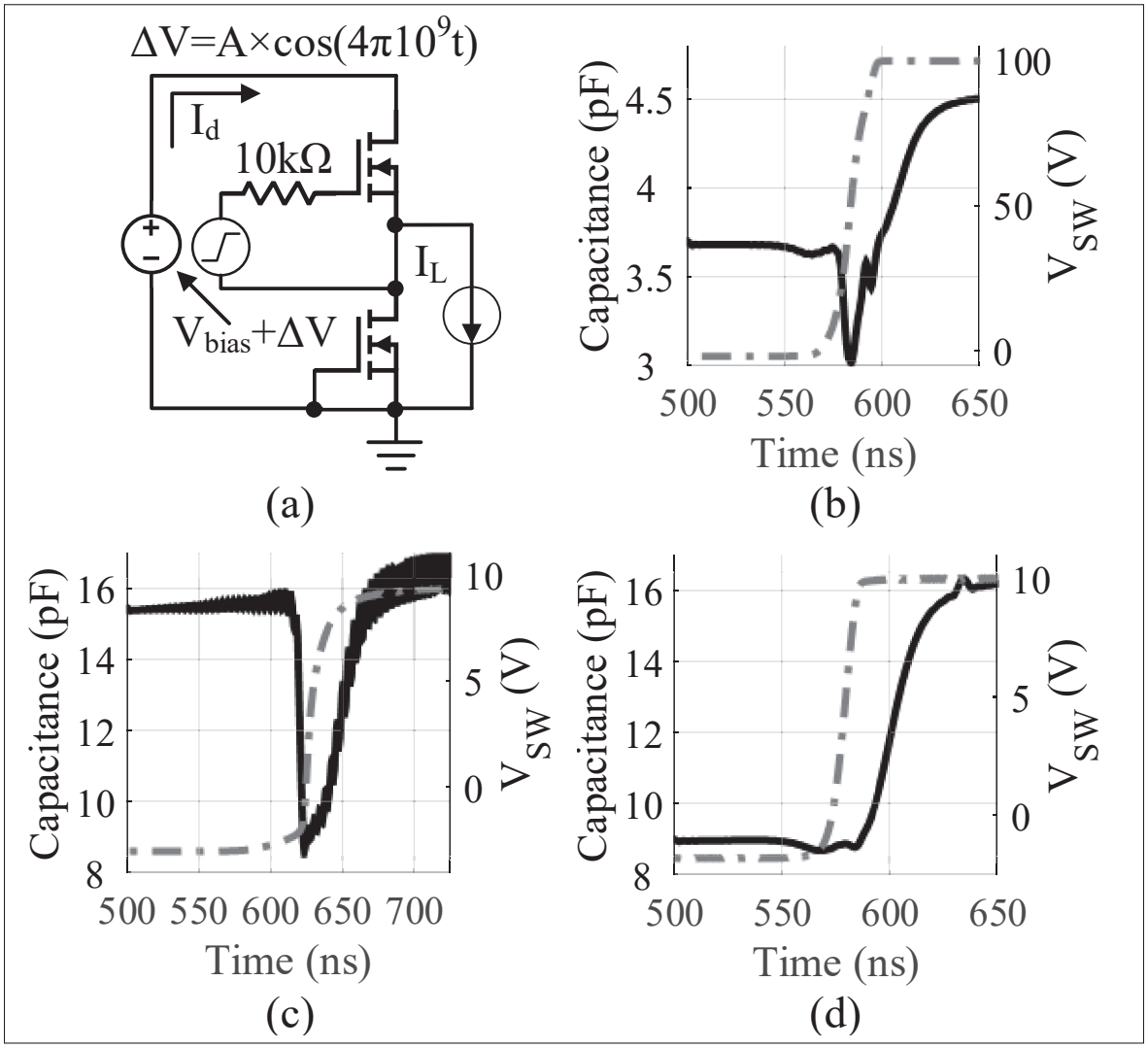

Figure 4.4 (a) Simulation of the capacitance seen from the power rails in a converter, (b) I_L = 10 mA, V_{bias} = 100 V, (c) I_L = 1 A, V_{bias} = 10 V and (d) I_L = 10 mA, V_{bias} = 10 V conditions

It is therefore safe to draw the hypothesis that the PDN of the SiP containing an array of switch-mode converters behaves as an LTI system. Furthermore, as mentioned, that hypothesis is further explored and supported in section 4.3.

4.1.3 The One-Port Assumption Under Simultaneous Switching Conditions

Another important aspect that must be considered with a model using only DM current as described above is that the half-bridge is a three-port device where some amount of current may flow into the load. Depending on that current, a single DM impedance at the power rails to model the power device may not be sufficient. In fact, the current flowing through the load could lead to CM current flowing through the half-bridge and then into the load. When referring to Figure 4.5, it can be noted that there are three terminals (t_1-t_3) for the current to flow in and out from. Therefore, this would be equivalent to three differential ports: $P_1(t_1 \rightarrow t_2)$; $P_{CM,1}(t_1 \rightarrow t_3)$ and $P_{CM,2}(t_2 \rightarrow t_3)$. A differential flow of current into either P_{CM}, or both, would translate into CM current seen from P_1 of Figure 4.5. At low frequencies, i.e., frequencies in the bandwidth of the output signal, such a common-mode current is unavoidable in an unbalanced converter. Given the capacitive nature of the coupling between power domains, noise at those frequencies is, however, less likely to propagate to different power domains such as the one of a more sensitive IC like an ADC. At the frequencies where switching noise may propagate to different power domains, which is in the tens to hundreds of MHz, if the impedance Z_{out} in Figure 4.5 is sufficiently high, no flow of current will flow into terminal t_3.

In conclusion, a condition for the analysis, as described in this paper, is to rely on a high-impedance towards the load at frequencies where the model is used. This can be achieved with the physical implementation of a ferrite bead at the switching node (Z_{BEAD} in Figure 4.5) for higher frequencies, while at lower frequencies, the LC filter at the output of the converter or the load impedance in the case of an inductive load are sufficient (Z_L in Figure 4.5). Under those conditions, the switching current characterized can be seen as a DM current flowing through P_1. It is noteworthy to mention that residual CM noise may still be present due to the finite

impedance of the ferrite bead. It is however unlikely that the residual CM noise effects outweigh the DM effects.

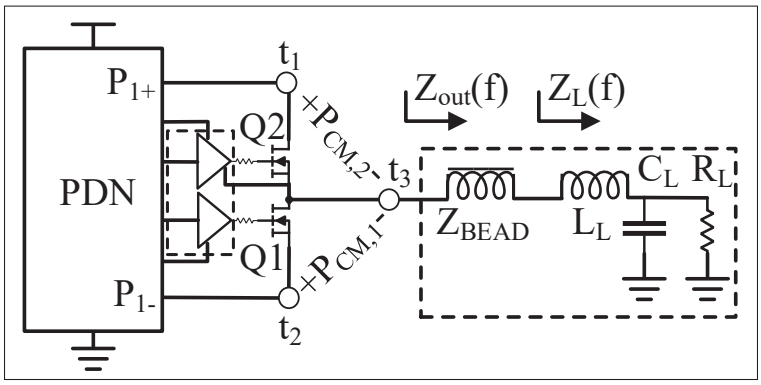

Figure 4.5 Three-port representation of a half-bridge with an LC filter as the load

4.1.4 General Methodology for the Characterization of the Model

As mentioned, there is a need to characterize the two critical non-scalar parameters of the model. The first of those parameters are (A) the Z-parameters of the system, more specifically the transimpedance between every aggressor port in the system and every victim (Z_{nm}) as a function of frequency. The second of those parameters are (B) the different switching currents for each m half-bridge ($i_{\mathrm{d,m}}\left(t;\left\{V_{\mathrm{DD}}, R_{\mathrm{g}}, I_{\mathrm{L}}\right\}\right)$), which is a function of the input voltage (V_{DD}), gate driving strength (R_{g}) and load current (I_{L}).

Regarding (A), the Z-parameters of the system, such parameters are typically characterized through VNA two-port S-parameters characterization that are then converted to Z-parameters. Such a methodology requires $N \times M$ pairs of two-port S-parameter measurements in the case of N victims and M aggressors. A hypothesis can be drawn in order to reduce the number of two-port S-parameter pairs to measure. If only lower frequency characterization is required, half-bridges sharing the same power planes can be characterized as being on the same physical port. For instance, half-bridges A and B, both sharing the same power planes, generate voltage fluctuations onto victim C. In that case, a compromise can be made in terms of bandwidth and Z_{CA}, the transimpedance between aggressor A and victim C, could be used as the transimpedance

between A and C as well as B and C. Indeed, at low frequencies, radiofrequency (RF) effects from the two converters being at a different location on the power planes are minimal.

Regarding (B), multiple techniques exist for the high-frequency characterization of currents, such as transmission-line-based, as presented in chapter 3, with pickup coils (e.g. (Wang *et al.*, 2018)) or based on current shunt resistors (e.g. (Zhang *et al.*, 2021)). In order to have the current measurement structure not affect the behavior of the half-bridge through its insertion impedance, it is preferable to use techniques which are embedded and minimally affect the half-bridge. In addition, the current must be characterized for a large range of condition: input voltage, gate driving strength and load current. One hypothesis that can be drawn to reduce the amount of current characterization required is that the different half-bridges in the system are based on the same power devices, gate drivers and passive components. Therefore, in such a case, it is not unreasonable that each individual half-bridge exhibits the same switching behavior in terms of current. Therefore, only one aggressor half-bridge would have to be characterized under every possible condition.

In the next section, the measurement apparatus for the two critical parameters above is presented and those critical parameters are used in order to make voltage fluctuation predictions in section 4.3. For the purpose of this work, which is to validate the model presented in this section and explore its limits, none of the possible hypotheses presented in this section were explored. Such hypotheses are, however, a reasonable starting point for future works that aims at reducing the amount of measurement to be taken for proper characterization of the model.

4.2 Experimental Apparatus for the Validation of the Model

This section presents a measurement apparatus and the prototype that is used in order to validate the model of the previous section. As defined in Section 4.1, the converter circuit has to be characterized to extract two sets of parameters to build the proposed model. The first set is the Z-parameters of the system, more specifically the transimpedance between every aggressor port in the system and every victim (Z_{nm}) as a function of frequency. The second set is the switching

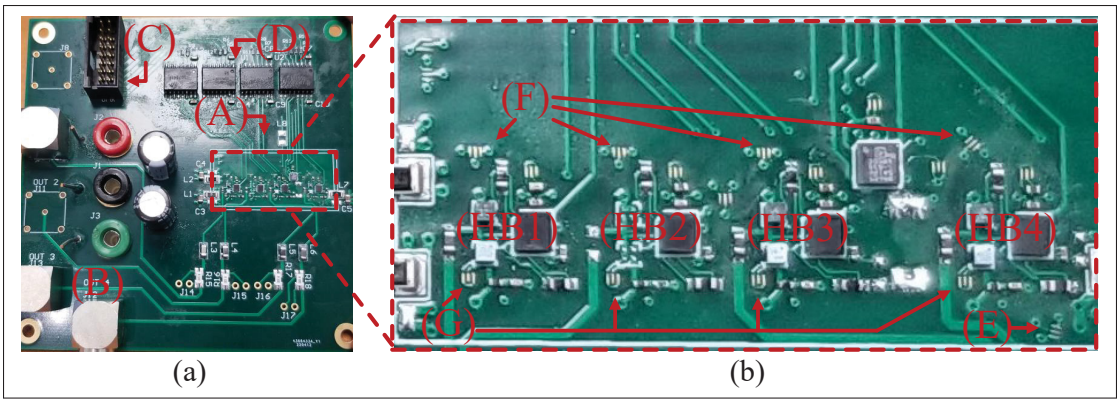

Figure 4.6 Board prototype used for model validation: (a) top view and (b) zoom-in on the converter section

current ($i_d(t)$) in each converter, as a function of the operating conditions: input voltage (V_{DD}), gate driving strength (R_g) and load current (I_L). Then, the predictions of the model are validated through comparison with experimental measurements of fluctuations under those operating conditions. Those characterization and validation steps are described next.

4.2.1 Experimental Design

An experimental board that contains converters to characterize and has a sensitive node to measure was fabricated to validate the model. The design of the board is presented in Appendix I, section 2. It contains the different element (isolators, converters and readback) of Figure 4.1. A total of four switching half-bridges ($M = 4$ in Figure 4.1) based on a Texas Instruments' LMG1205 gate driver and EPC2037 Efficient Power Conversion (2020) transistors (HB1-HB4 in Figure 4.6) are placed on a 35×16 mm^2 PCB section with separated power planes from the rest of the board, as if it were on a SiP (section A in Figure4.6(a), zoomed in Figure 4.6(b)). Different loads can be attached to the switching converters through Bayonet Neill–Concelman (BNC) connectors on the extremities of the board (B). The input signals for the gate drivers enter through the header connector (C) and are brought to the gate driver through digital isolators (D). The victim measured in the results section is at the node (E). This node represents a connection to a possible switching converter. The switching current in each half-bridge is measured on the

ports identified with (F), using the current-sensing process that is explained in subsection 4.2.3. The drain-source terminals defined as aggressor ports are labeled by (G). The measurement setup for the frequency domain characterization is depicted in Figure 4.7. For the frequency domain characterization setup, GSG ZProbe® probe heads (A in Figure 4.7) with 250 µm pitch are placed on a probing station (B) in order to probe the critical points (E-G of Figure 4.6) on a VNA (C). As explained next, only decoupling capacitors are populated on the board for that specific setup.

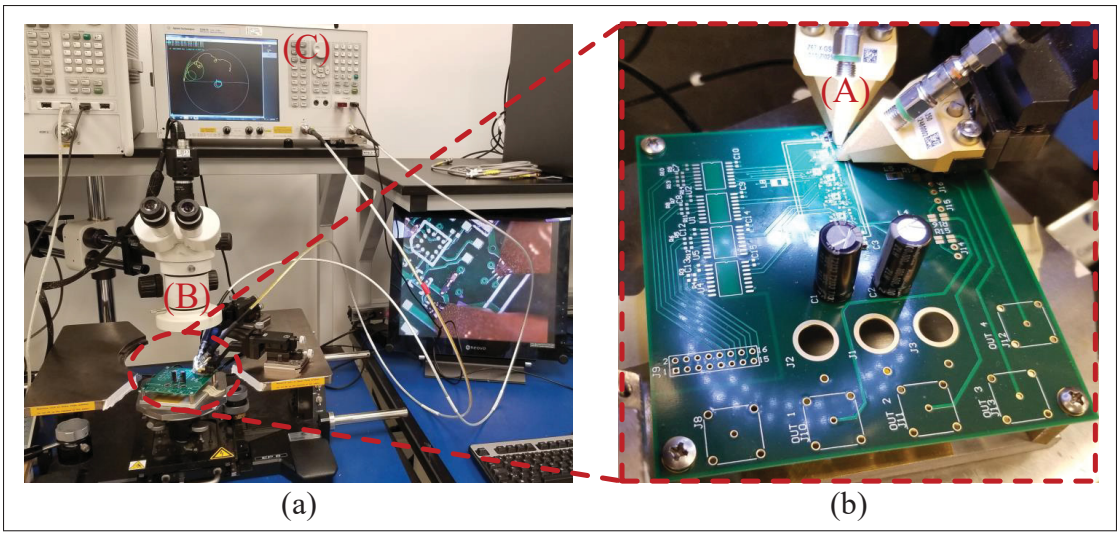

Figure 4.7 Measurement setup for frequency-domain characterization: (a) global view and (b) zoom-in on the probed prototype

4.2.2 Frequency-Domain Measurement Setup

As mentioned, the frequency-domain couplings are first characterized. The following is used: a VNA port is placed at the pads of transistor Q2 (Figure 4.8) of each converter (high-side transistor), depicted as $P_{1\text{-}4}$, while Q1 (low-side transistor) is shorted with a wire bond. Note that an unpopulated board must be used, but with the PDN populated with its decoupling capacitors. Indeed, the decoupling networks must be present as they impact the behavior of the PDN at any frequency. Each of those ports $P_{1\text{-}4}$ are referred to as *aggressor ports*. The transimpedances between the aggressor and the different victim ports are measured ($P_{9\text{-}10}$). The victim port is a specific node on the power rail of one of the converters, labeled (E) in Figure 4.6. With the

ports other than the ones being measured left in open conditions, a Z-parameters matrix can be constructed from sets of two-port S-parameter measurements, which are then converted to Z-parameters. Once the Z-parameters are obtained between each aggressor and victim, the impact of a 50 Ω probe on each of the victims and current measurement port is calculated by using a similar transformation as in section 4.2.2 applied to the measured Z'_{nm} (3.13), which is the measured transimpedance between an aggressor m and a victim n. The VNA characterization is done up to 3 GHz. That characterization frequency allows the prediction of transients at a sampling frequency of up to 6 GHz. Indeed, by knowing the current waveform at a sampling frequency of 6 GHz, that current will be known in the −3-3 GHz band. In order to predict the voltage on a victim node, the couplings in the same band have to be known (LTI system). Furthermore, negative frequencies for transimpedances are assumed to be the complex conjugate of the positive frequencies, making the transimpedance a hermitian function of frequency, as it is for any system with a real-valued impulse response. Therefore, a 3 GHz VNA characterization is required. Once the couplings are extracted, the parameters for the current measurement structure must also be extracted with the same characterization setup.

4.2.3 Design of the Current Measurement Setup

As stated in section 4.1, the switching current of each individual half-bridge ($i_{\mathrm{d},m}$) is a critical parameter in the model for the calculation of voltage fluctuations. Due to the GHz-range bandwidth that needs to be achieved by the model and the SiP context of this work, which requires non-invasive measurements, the coupled transmission-line technique is preferred to measure the current flowing through the drain of each aggressor ports such as in Figure 4.9 ($\mathrm{P}_{1\text{-}4}$), which is the switching current. As mentioned in chapter 3, there is a need for a frequency domain characterization to obtain the bandwidth, mutual inductance (L_{M}) and delay (T) between the aggressor port and a so-called current measurement port ($\mathrm{P}_{5\text{-}8}$) in the current measurement technique. Therefore, the setup from Figure 4.8 is reused for the characterization of those parameters. The parameters are estimated with (4.5-4.6). The characterized mutual inductance and delay, $L_{\mathrm{m,char}}$ and T_{char}, are calculated from the frequency-domain characterization, i.e., the

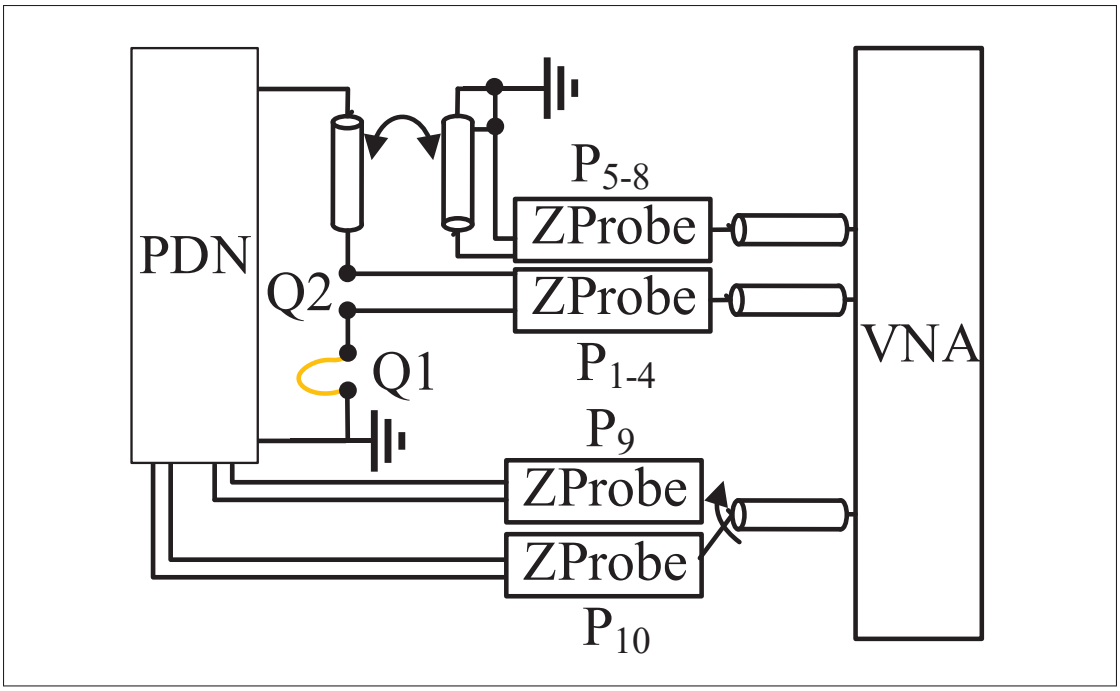

Figure 4.8 Frequency-domain characterization setup for each individual switching half-bridge

VNA measurements of the transimpedance between $P_{1\text{-}4}$ and $P_{5\text{-}8}$: Z_{14-58}. The bandwidth itself can be extracted by evaluating the measurement distortion as presented in section 3.4.1.

$$L_{M,\text{char}}(f) = \frac{|Z_{14\text{-}58}(f)|}{j2\pi f} \tag{4.5}$$

$$T_{\text{char}}(f) = -\frac{1}{2\pi}\frac{\mathrm{d}\angle Z_{14\text{-}58}(f)}{\mathrm{d}f} \tag{4.6}$$

$$i_{\text{d,m}}(t) = I_0 + \int_{t_0}^{t} \frac{v_{P5-8}(t + T_{\text{char}})}{L_{\text{M,char}}}\mathrm{d}t \tag{4.7}$$

Once the parameters $L_{\text{m,char}}$ and T_{char} as well as the bandwidth are obtained, the board is fully populated and the drain current $i_{\text{d},m}$ is measured with the setup of Figure 4.9. For that setup, only the ZProbe® associated with the current measurement ports ($P_{5\text{-}8}$ in Figure 4.9) of the half-bridge that is currently measured is connected. The other ports are left open. A gate driver with output resistance R_g drives Q1 and Q2 of each half-bridge in order to apply the load current

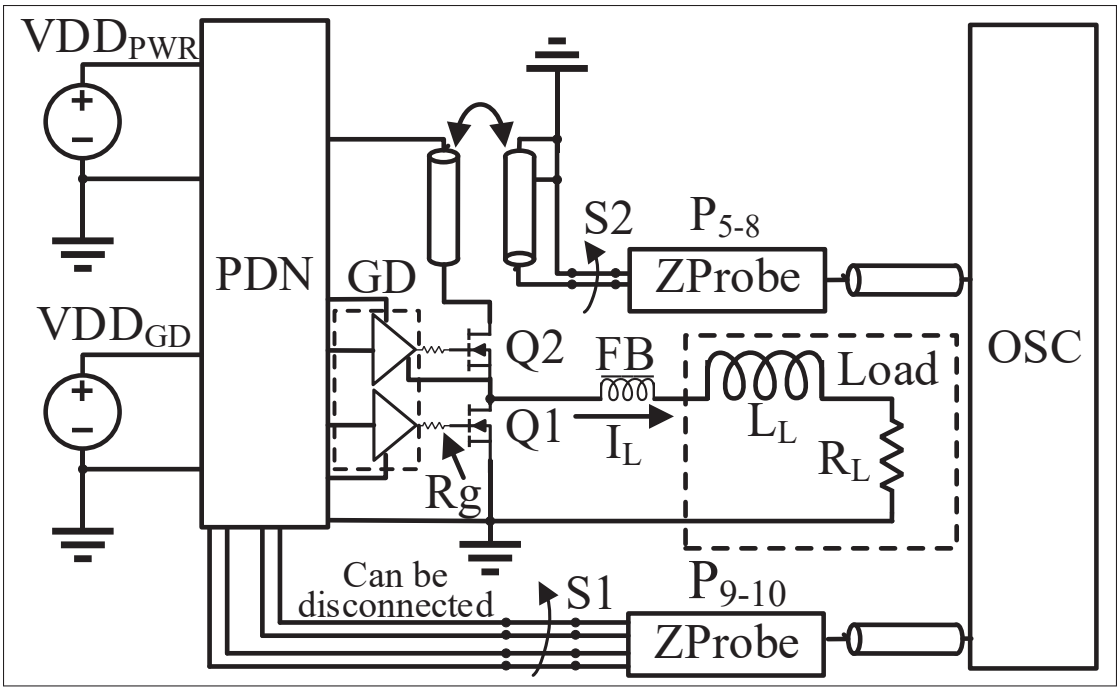

Figure 4.9 Current and noise measurement setup for each individual switching half-bridge

I_{L} into the load inductor. As mentioned in section 3.3.3, a ferrite bead is added to the switching node so that the current waveform pulled by the half-bridge does not depend on specific passive load behavior, but only V_{DD}, $\mathrm{R_g}$ and I_{L}. The ferrite bead ensures that, in the case of CCM, the load, as seen by the power transistor, behaves as an ideal current source at high frequency. The ferrite bead also ensures that no significant DM currents, which are not taken into account by the model, affect voltage fluctuations on the sensitive nodes.

A drain current function $i_{\mathrm{d},m}(t)$ is extracted by integrating the voltage at the current measurement port $v_{\mathrm{P5\text{-}8}}(t)$ (4.7). I_0 is obtained through knowledge of the initial/final conditions of the switching current: switching current is zero before high-side turn-on or after low-side turn-on. One issue remains: the non-zero edges to the current function leading to numerical artifacts during discrete Fourier transform (DFT) operations of the current functions.

4.2.3.1 Windowing Function

Indeed, the current function of the DM current component in a switch-mode converter has a step-function shape. However, the DFT operation considers a periodic signal. This leads to as if there was a step discontinuity at the end and the beginning of the measured current waveform. Therefore, creating a numerical artifact when applying a transfer function such as the transimpedance between the aggressor device and a sensitive node (Z_{nm} in (4.1)).

In order to obtain a drain current function with no discontinuity at the edges for subsequent discrete Fourier transform operations, a $T = 100\,\text{ns}$ Hann window centered near the peak of the drain current function in order to ensure minimal distortion, $w(t)$, is used on $i_{\text{d},m}(t)$, yielding $i_{\text{d,windowed}}(t)$ and its Fourier transform, $I_{\text{d,windowed}}(f)$ in (4.8) to (4.10).

$$w(t) = 0.5 - 0.5\cos\left(\frac{2\pi t}{T}\right) \tag{4.8}$$

$$i_{\text{d,windowed}}(t) = i_{\text{d}}(t) \times w(t) \tag{4.9}$$

$$I_{\text{d,windowed}}(f) = \mathcal{F}\left\{i_{\text{d,windowed}}(t)\right\} \tag{4.10}$$

4.2.3.2 Sampling Rate

The signals are sampled by the oscilloscope at 20 GHz before being downsampled to 6 GHz through linear interpolation. The signals are downsampled at that frequency in order to stay compatible with the 3 GHz frequency-domain characterization of the passive network. The 20 GHz frequency with linear interpolation downsampling has been selected because the oscilloscope does not support a 6 GHz sampling rate or any multiple of it. A significantly higher rate has therefore been chosen.

4.2.4 Time-Domain Switching Fluctuations for Model Validation Setup

Using (4.1) to (4.2), voltage fluctuation on sensitive nodes predictions are obtained based on the model presented in section 4.1, the current characterization of section 4.2.3 and the Z-parameters characterization in section 4.2.2. Experimentally-measured fluctuations on the victim at P_9 are obtained. The predictions and measurements are compared in order to validate the model for the prediction of fluctuations caused by a single converter switching (single transient predictions). The same setup as for current measurement, in Figure 4.9, is used.

The predicted voltage fluctuations are then shifted in time in order to match the beginning of the transient with the experimental one. They are both also compared in the frequency domain by applying the windowing function of (4.8) to the experimentally-measured fluctuations.

4.2.5 Simultaneous Switching Characterization Setup

In addition to performing predictions of voltage fluctuations caused by a single converter switching, it is also possible to predict through (4.3) and (4.4) the voltage fluctuations on the sensitive nodes caused by multiple converters switching simultaneously. Accordingly, two half-bridges are switched in a quasi-simultaneous manner, with two different delays between the switching transients.

4.2.5.1 Quasi-Simultaneous Switching Delays Generation and Characterization

In order to generate offset the delays between the two half-bridges by only a few ns, a resistor is added to the input of the digital isolators driving the gate drivers. That resistor, R_1 or R_2, is normally used to damp the LC dynamic of the cable between the FPGA development board generating the complementary PWM signals (inductive) and the input pin of the digital isolator (capacitive), which is part of the CPIOS system depicted in Figure 2.2. The resistance for one of the channels driving a given half-bridge can be increased in order to add an extra delay with another half-bridge driven by the same digital isolator, such as depicted in Figure 4.10. Indeed, $R_{1/2}$ and C_{in}, the input capacitance to the isolator, form an RC circuit that adds a delay

proportional to $\tau = RC_{\text{in}}$. In order to add a delay in the experimental setup, the value of the resistor R_2 went from 100 Ω to 1 kΩ, while C_{in} for the selected isolator is equal to 2 pF. Without having access to the design of the isolator, it is impossible to predict the delay, but it is reasonable that it falls in the range of $\tau_2 = 2$ ns. In order to know the exact delay, it has to be characterized with the following procedure.

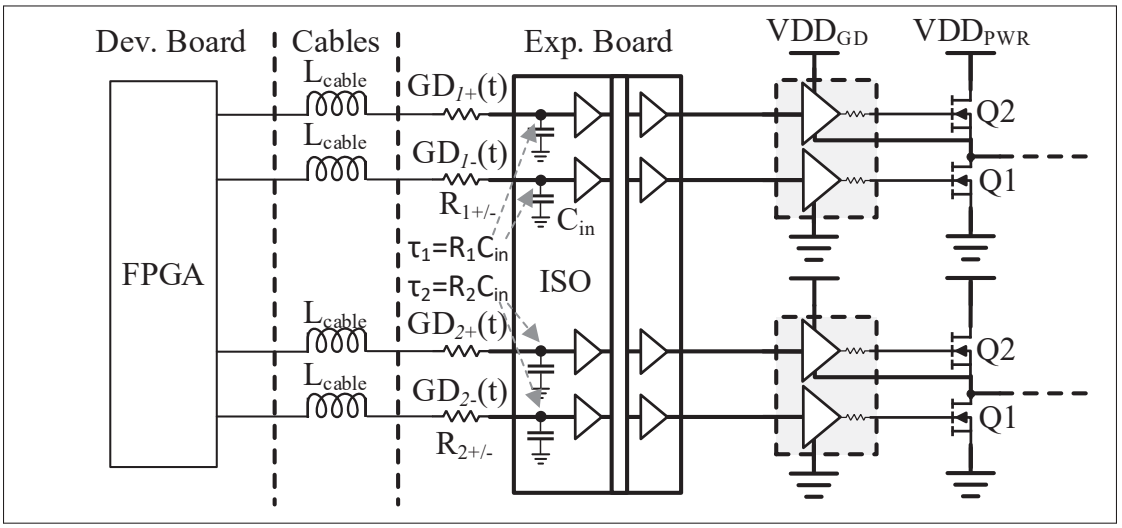

Figure 4.10 Setup for simultaneous and quasi-simultaneous switching

The relative delay between the converter, $t_{\text{rel,m}}$, switching currents must, however, be known. This delay is measured by extracting the drain currents using the current measurement technique on the simultaneously switching converters and comparing the delay between the beginning of the transient and time reference. In this setup, the time reference becomes the beginning of the first current transient ($t_{\text{rel,1}}$ is zero), while the others ($t_{\text{rel,2-}m}$) become the measured time duration between the first and the other transient. It is also possible to further support the hypothesis drawn in section 4.1.2 that the system behaves as LTI and therefore superposition, as in (4.4), holds in the case of two converters switching simultaneously. This is done by having the converters that switch independently and measuring individual fluctuations on a given victim. Those fluctuations are mathematically summed and then compared with the total measured fluctuations when the two converters are switching simultaneously.

4.3 Measurement Results for Predictions of Voltage Fluctuations

This section presents the different results obtained to validate the model by using the methodology of section 4.2. First, the different testing configurations that the model was validated with are defined. Second, the linear passive characterization of the system, which is necessary for making voltage fluctuation predictions, is presented with its main results. Third, the switching current transients for the testing configurations, also necessary for making voltage fluctuations predictions, are shown. Fourth, voltage fluctuation predictions are compared with the measured fluctuations under the different testing configurations. Finally, superposition due to the LTI hypothesis of section 4.1.2 is validated by comparing measured fluctuations under simultaneous switching of two half-bridges with predicted ones.

4.3.1 Metric for the Prediction of Voltage Fluctuations: NMSE

It is important that voltage fluctuations are well predicted both in terms of shape and energy density. Indeed, in an effort to properly predict the amplitude of the transients as well as noise spectral density in the condition of simultaneous switching, not only the spectral density, but also the phase of each individual transient must be well predicted. For that reason, the metric of variance-normalized mean-squared error (NMSE), as defined in (4.11), is used to quantify the quality of the predictions in terms of transient shape. In (4.11), $v(n)$ represents a reference signal, which in the context of this work is a measured voltage fluctuations, while $\hat{v}(n)$ represents the prediction of that fluctuation. The symbol $\overline{v(n)}$ represents the mean value of $v(n)$. By definition, NMSE gives a ratio between the variance of the absolute error (difference between reference and predicted fluctuations) and the variance of the reference signal. Note that a prediction of zero voltage fluctuation would lead to an NMSE of exactly one under that definition. Therefore, an NMSE inferior to one represents an average variance of the error less than the variance of the signal, which can be interpreted in this case as a better-than-nothing approximation.

$$NMSE = \frac{\|v(n) - \hat{v}(n)\|^2}{\|v(n) - \overline{v(n)}\|^2} \tag{4.11}$$

Table 4.1 Testing configurations for single transient fluctuation predictions

Configuration	HB	LS/HS	V_{DD}	R_g	R_L	Duty Cycle
C1	HB1	HS	10 V	0 Ω	10 Ω	50 %
C2	HB4	HS	10 V	20 Ω	6.8 Ω	50 %
C3	HB4	HS	5 V	20 Ω	6.8 Ω	75 %
C4	HB1	LS	5 V	0 Ω	10 Ω	75 %

It is also critical that the aforementioned current transients are properly characterized. Mainly, in order to predict the voltage fluctuations onto the power rails up to the GHz range, the required bandwidth for the characterization of those transients must be in that range with a sufficient accuracy. In order to fulfill that need, the concept of measurement distortion is introduced next.

4.3.2 Conditions for Fluctuation Predictions

In order to validate the model and its predictions, four different testing configurations are selected, which are referred to as C1 to C4. The configurations are presented in table 4.1 in terms of the aggressor half-bridge (HB1-4), high-side or low-side turn-on transient (HS/LS), gate resistance (R_g), load resistivity (R_L) and the duty cycle of the converter. Those four configurations provide a relevant range of testable conditions for the model in terms of load current (375 to 735 mA), input voltage (5 and 10 V) and gate driver resistance (0 and 20 Ω), while being a limited set of configurations to validate and analyze. In order to test that set of configurations, the half-bridges 1 and 4, labeled as (HB1, HB4) in Figure 4.6, are put under test and the voltage fluctuations on the power rails of the converters are measured under different converter duty cycles and power supply (V_{DD}) configurations. Both HB1 and HB4 have different loads and gate driving conditions. A load inductance (L_L=330 µH) is in series with the load resistor R_L, leading to a much longer time-constant $\tau = L_L/R_L$ than the switching period of 1 µs for either value of R_L (33 and 49 µs). The converters are driven until the load current reaches the steady state before any measurement is taken.

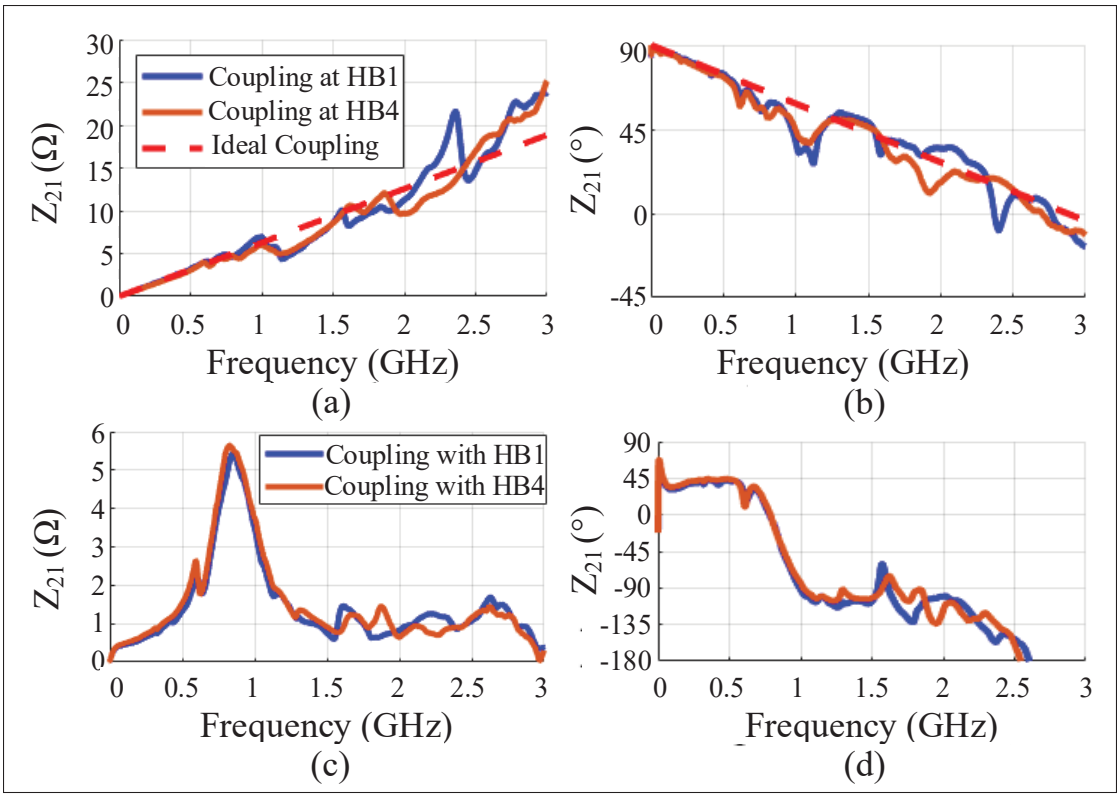

Figure 4.11 Coupling onto current measurement structure (a) in magnitude and (b) phase. Coupling onto victim node (c) in magnitude and (d) phase

4.3.3 Coupling Characterization of the System

The transimpedance magnitude and phase couplings, necessary for the prediction of voltage fluctuations, measured with the methodology of section 4.2.2 (blue and orange traces in Figure 4.11(a) and (b)) between the aggressor ports in HB1, HB4 ($P_{1,4}$ of Figure 4.8) and the current measurement port ($P_{5,8}$) show that the current measurement structure behaves as a mutual inductance of 1 nH with an 87 ps delay. The mutual inductance behavior with a delay is depicted by the red dashed trace of Figure 4.11(a) and (b). The coupling between the aggressor ports in HB1 and HB4 and the power rails of the converters (P_9 of Figure 4.8) both exhibit a resonant peak at approximately 833 MHz and significant coupling (more than 0.5 Ω) up to nearly 3 GHz, as observed in the magnitude and phase coupling plots of Figure 4.11(c) and (d) respectively. Those resonances are expected for self-resonant networks such as power planes,

where the mutual capacitance between the power planes can resonate with the vias that are connected to the power planes.

4.3.4 Characterized Currents for Different Conditions

For the four configurations presented in Table 4.1, the switching current generated by the half-bridge is measured with the transmission-line-based current measurement technique (Figure 4.12(a)). Those currents are windowed using the function in (4.8) to calculate their energy spectra, shown in Figure 4.12(b).

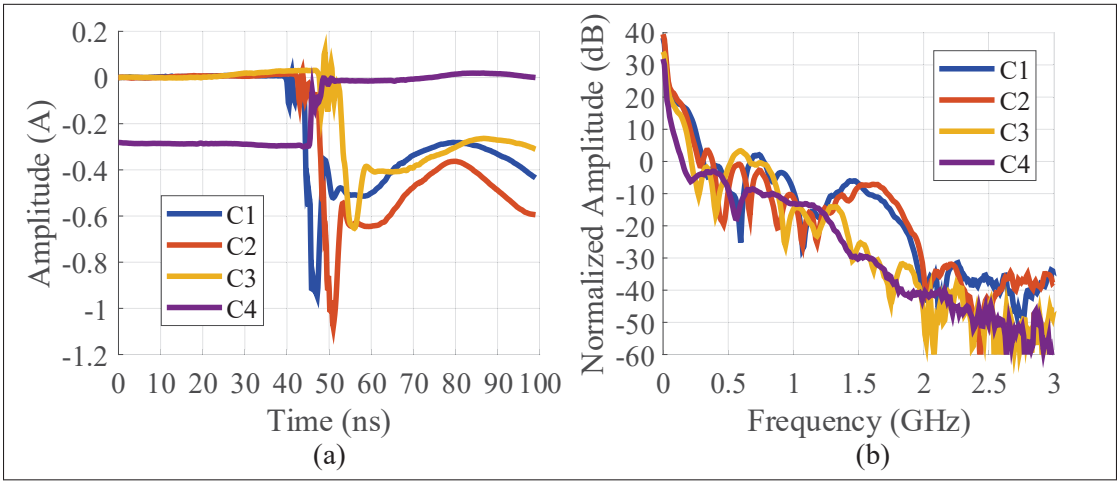

Figure 4.12 Measured switching currents for configurations C1 to C4 in (a) time-domain and (b) frequency-domain

4.3.5 Single Transient Fluctuation Predictions

Predicted and measured fluctuations are obtained for each configuration of Table 4.1 (Figure 4.13). For each prediction, the NMSE (4.11) is calculated in order to quantitatively assess the quality of the predictions. In (4.11), $v(n)$ represents every measured sample for the voltage fluctuations, while $\hat{v}(n)$ represents every sample predicted. It is observed that peak interference and the overall shape of the transient are well captured in the time domain for C1-C3 ($NMSE < 0.25$) and acceptable for C4 ($NMSE = 0.624$). Note that an NMSE of less than 0.25 is considered well-captured because it is significantly below 0.75. Those results show that not only are

the predictions accurate in terms of magnitude in the frequency domain, but also in terms of phase. The energy spectra of Figure 4.14 further confirm the accuracy of the predictions in terms of magnitude as a function of frequency. Indeed, it is observed that for every measured configuration, the predictions are in a worst case within a 10 dB over the whole 2 GHz bandwidth and are even more accurate over most of the spectrum.

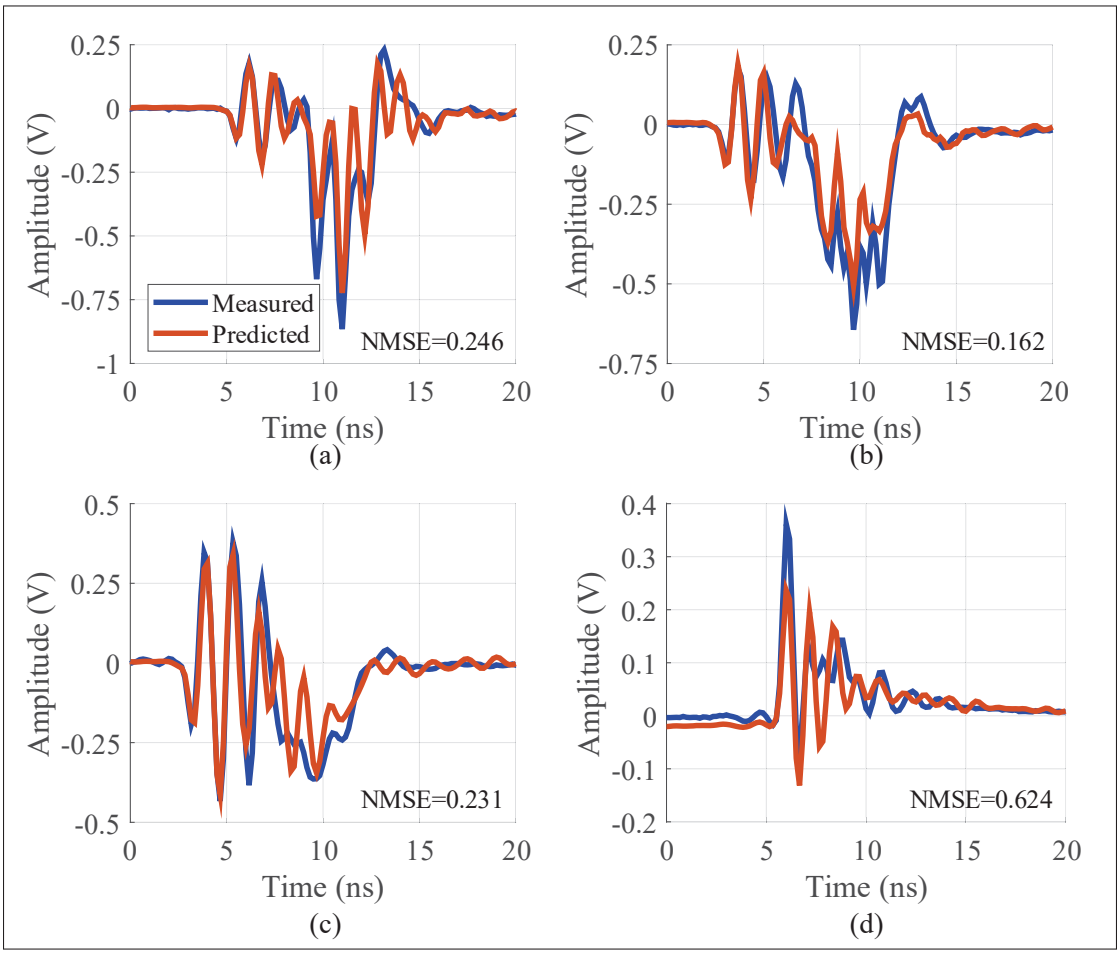

Figure 4.13 Prediction of fluctuations caused by switching under configurations (a) C1, (b) C2, (c) C3 and (d) C4

The higher NMSE for C4, which occurs under low-side turn-on, can be attributed to residual CM effects, such as explained in section 4.1.3. Indeed, it is probable that the CM excitation from $P_{\mathrm{CM},1}$ in Figure 4.5, associated with low-side current flow, has more significant coupling towards than the victim than $P_{\mathrm{CM},2}$, which is associated with high-side current flow. While these

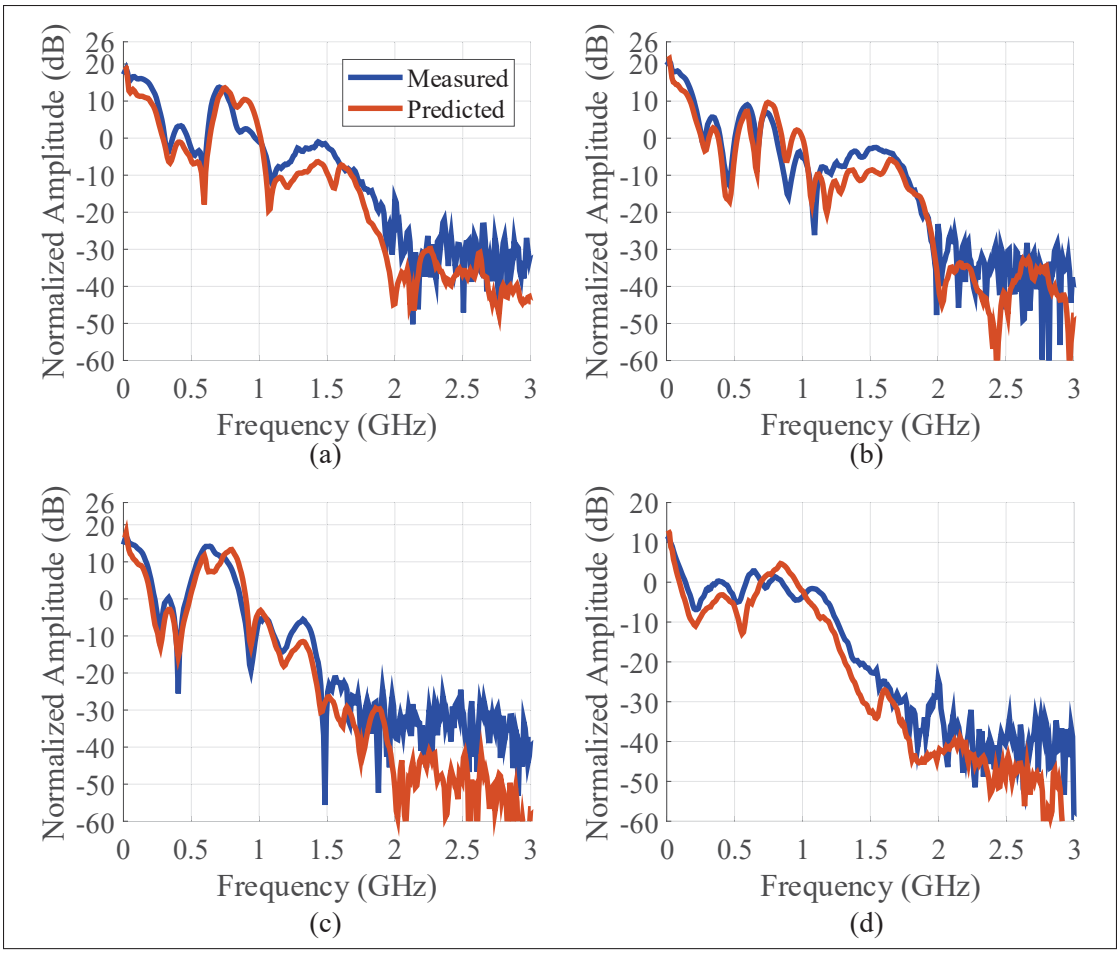

Figure 4.14 Energy spectra of fluctuations caused by switching under configurations (a) C1, (b) C2, (c) C3 and (d) C4

results would indicate that common-mode effects and conduction through $P_{\mathrm{CM},1}$ and $P_{\mathrm{CM},2}$ is still possible, the results obtained show that these residual common-mode effects are small enough to still obtain acceptable NMSE under every configuration of Table 4.1.

4.3.6 Simultaneous Switching and LTI Hypothesis Revisited

While it has been shown that single transient fluctuations can be predicted, it remains to be shown that the model can still be applied to multiple half-bridges switching simultaneously or with quasi-simultaneous delays. First, the characterization of the delay between the two

switching events is presented when switching simultaneously. Then, the measurement results of the fluctuations are presented and compared with the predicted ones.

4.3.6.1 Characterization of Delays for Simultaneous Switching

To characterize the model for simultaneous switching conditions, simultaneous switching was caused and characterized for two different timing conditions with the methodology of section 4.2.5.1, which the main idea was to create a delay between the control signal of the converter and the digital isolators by increasing the value of the resistor at the input of the isolator. The timing conditions were the following: delays between the switching of the converter as small as possible and with a delay in the order of 2 ns. For the first condition, the value of R_1 was matched to R_2 (100 Ω) in Figure 4.10. For the second condition, the value of R_2 was set to 1 kΩ. The current waveform for both converters were then measured and the delay between the beginning of both current transient (when the voltage stops being constant) was characterized. For the first condition, a delay of 0.66 ns was characterized, as depicted in Figure 4.15(a). A delay of 2.83 ns was characterized for the second condition (Figure 4.15(b)).

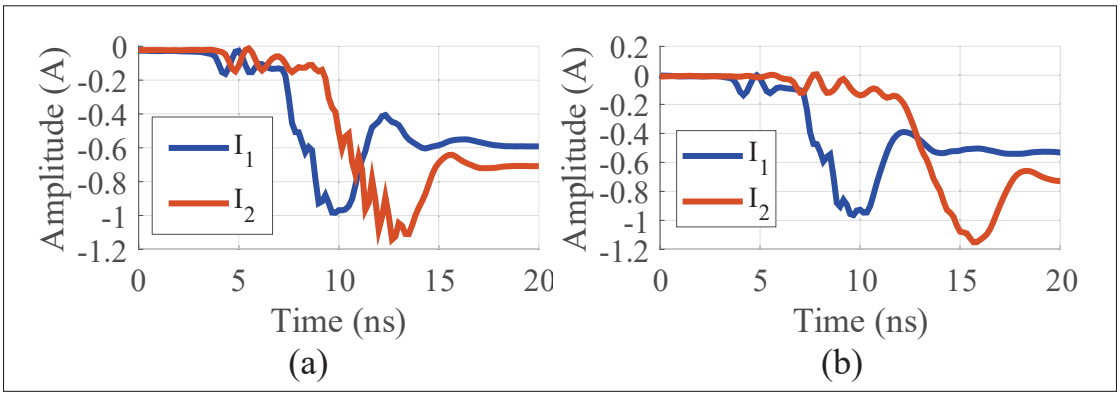

Figure 4.15 Characterized delays between quasi-simultaneous switching events of (a) 0.66 ns and (b) 2.83 ns

4.3.6.2 Measurement Results for Simultaneous Switching

The hypothesis of an LTI system and superposition (Section 4.1.2) are validated with the methodology of section 4.2.5. HB1 and HB4 are switched simultaneously under configurations C1 and C2 respectively. The switching events were done with characterized delays of 0.66 ns and 2.83 ns, leading to the voltage fluctuations on the power rails of the victim in the time-domain plots of Figure 4.16(a) and Figure 4.16(c) for each respective delay. The two measured fluctuations of C1 and C2 were mathematically summed with the 0.66 ns and 2.83 ns delays between each other (trace $T_{C1} + T_{C2}$). The predicted fluctuations with the model of section 4.1 were also summed with the same delays (trace $M_{C1} + M_{C2}$). Both of those traces were compared with the measured fluctuations when the half-bridges were switching simultaneously with the corresponding delays (trace T_{C1+C2}).

When comparing the mathematical sum of individual fluctuations ($T_{C1} + T_{C2}$) with T_{C1+C2}, an $NMSE = 0.125$ for a 0.66 ns delay and $NMSE = 0.264$ for a 2.83 ns delay are observed. Such results strongly support the hypothesis that superposition holds, because similar voltage fluctuation shapes, as reflected by the NMSE, are observed when comparing the sum of individual fluctuations to the measured fluctuations when simultaneously switching. When using the model predictions ($M_{C1} + M_{C2}$), similar overall shapes are obtained with better predictions for a delay of 0.66 ns: $NMSE = 0.189$ for a 0.66 ns delay and $NMSE = 0.616$ for a 2.83 ns delay. The worse prediction for the 2.83 ns delay can be partially explained by the imprecision in the characterization of the delay between the two transients (also supported by the higher NMSE when comparing $T_{C1} + T_{C2}$ with T_{C1+C2}). Accuracy better than 10 dB is observed when comparing $M_{C1} + M_{C2}$ with T_{C1+C2} in the frequency domain, as depicted by the energy spectra both with a delay of 0.66 ns and 2.83 ns respectively in Figure 4.16(b) and (d).

4.4 Conclusion

A power integrity model to predict fluctuations in simultaneous switching conditions on an array of switch-mode converters has been presented. This model allows proper power integrity

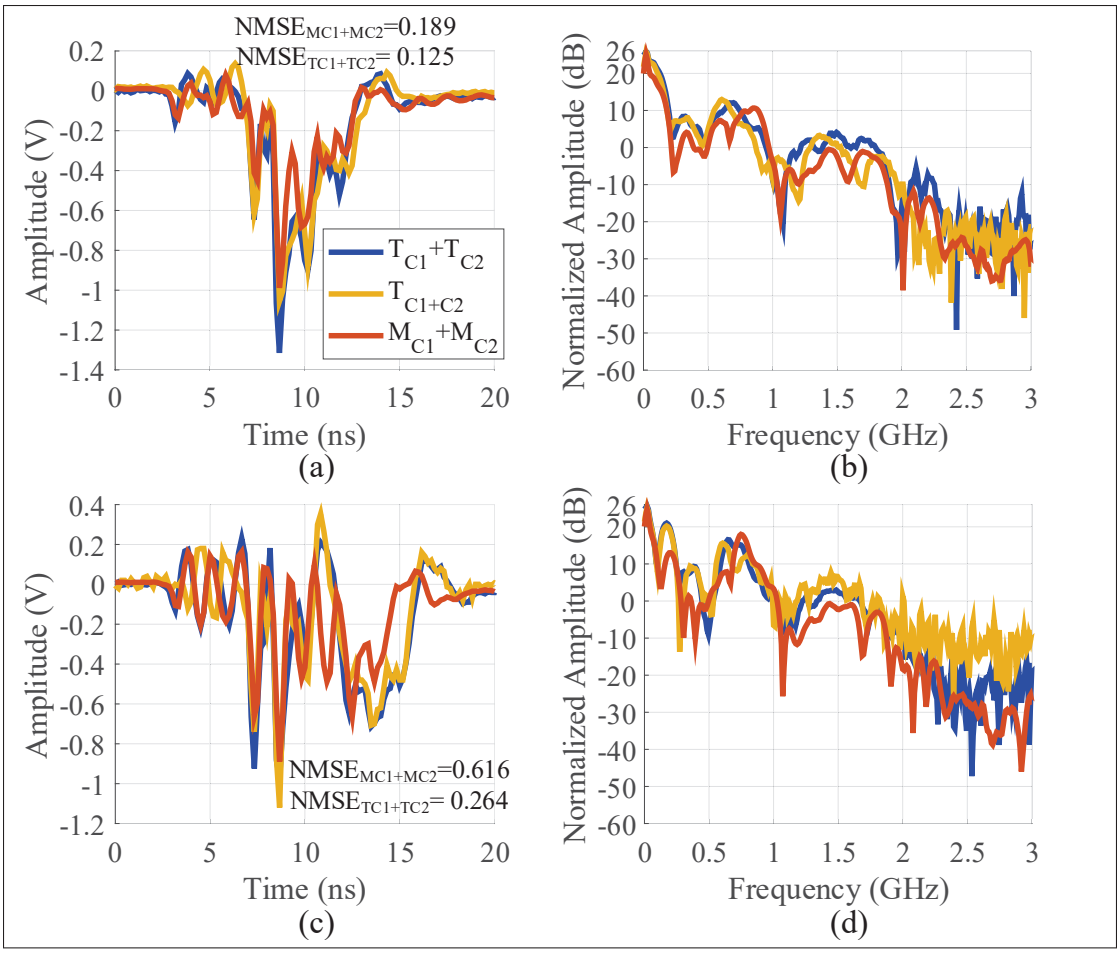

Figure 4.16 Predictions of fluctuations on the power rails under simultaneous switching with delays of (a) 0.66 ns and (c) 2.83 ns along with (b) and (d) their respective energy spectra

assessments in an array of converters with fast switching times, implemented with sensitive analog circuits (e.g., in the context of SiP) and with a range of possible operating conditions in terms of input voltage, gate driving and loading. The general idea of the model is to characterize both the drain current flowing through the converter and characterize the passive network between a given victim and the converter as transimpedance. Then, superposition is applied in order to account for simultaneously switching converters. As was missing the state-of-the-art, the model allows the predictions of the shape of voltage fluctuations onto sensitive devices when converters are switching simultaneously. In this case, it was shown that that an NMSE of at worst 0.616 for simultaneous switching voltage fluctuation predictions. Those predictions were

made with a 10 dB accuracy in terms of spectral density at up to 2 GHz. The specific objective of "predicting fluctuations onto the power rails of sensitive circuits, in terms of shape and energy spectrum" is therefore met. The results also show that superposition holds when attempting to predict the total interference when two converters are switching simultaneously with an NMSE ranging between 0.125 and 0.264 when the voltage fluctuations generated by individual switching events are known. This shows the accuracy of the LTI system and superposition hypothesis that was made in section 4.1.2.

In summary, the following contributions were made:

- a linear model for the time-domain and energy spectrum of the voltage fluctuations onto the power rails of sensitive circuits caused by an array of switch-mode converters switching simultaneously;
- the prediction of fluctuations onto the power rails of converters up to 2 GHz under different loading, gate driving and timing conditions of the power converters using a characterization methodology based on a coupled transmission-line-based current measurement technique and Z-parameter characterization.

As was determined in the literature, especially when referring to Table 1.2, it was shown that in addition to not being able to predict noise at more than tens of MHz, general terminal modeling (GTM) was not meant to predict the overall shape of voltage fluctuations, as was done in this chapter. It also cannot predict the transient generated by multiple converter simultaneously. In addition, PI models in digital systems, while effective at predicting the noise described before, are meant for digital IC, which have inherently different characteristics for switching noise than power converters. Therefore, those contributions make this research unique and novel. It is expected that this research finds its purpose as more and more power systems are integrated into a compact SiP, thanks to WBG technologies such as SiC and GaN HEMT. Indeed, as the need for integrating sensitive circuits such as ADC and operational amplifiers for signal conditioning grows, there will be a need to assess performance degradation in those systems due to the switching activity of power converters. The research presented in this chapter helps in obtaining the exact characteristic, both in time and frequency, of voltage fluctuations caused

by that switching activity. Used in conjunction with models, for instance, for degradation of ENOB relative to noise on power rails (Bae *et al.*, 2013), the model presented in this section is key to assessing the performance of, for instance, readout systems in compact power SiP such as CPIOS.

CONCLUSION AND RECOMMENDATIONS

WBG technology allows the integration of more compact power systems with less losses. Indeed, faster switching leads to reduced switching losses. WBG technology also enables better trade-off between breakdown voltage and on-state resistivity for given dimensions. It is also now possible to integrate those power transistors into more complex systems including ADC and other types of analog and mixed-mode circuits. However, one problem remains: sub-ns switching also causes GHz-range noise onto the power rails of such highly integrated systems, which can impact the behavior of the analog and mixed-mode circuits. For that reason, there is a need to accurately predict the noise in that GHz range in the context of a highly integrated power system SiP.

Accordingly, the concept of CPIOS was presented: an interfacing circuit between high-power loads and a digital system such as an FPGA or a microcontroller for closed-loop operation. This work has shown that it is possible to assess power integrity in CPIOS, answering the research question, "what is an accurate way to assess power integrity in systems that integrate power converters with more sensitive analog and mixed-mode circuits, e.g., CPIOS?". Indeed, by first characterizing the DM switching current flowing through the half-bridge with a novel transmission-line-based current measurement technique, and then using a novel behavioral model to predict voltage fluctuations onto the power rails of sensitive devices in terms of shape and energy spectrum, it is possible to obtain a clear and accurate picture of the power integrity constraints in CPIOS.

The main objective of the research was *to model power integrity constraints in CPIOS based on diverse operating conditions (mainly timing, gate driving and loading) and a thorough characterization of the system*. The following specific objectives were pursued:

(O1) To characterize the switching current in power converters for the CPIOS, which are critical for power integrity with high bandwidth.

(O2) To predict fluctuations onto the power rails of sensitive circuits, in terms of shape and energy spectrum.

Summary of the Thesis

The state-of-the-art regarding the current measurement techniques in the possible application of CPIOS were first reviewed. It was found that there is a lack in the literature regarding several aspects that are key to CPIOS:

- **Minimal on-board overhead for probing provision**: two types of current-measurement techniques were found in the literature for high-bandwidth current measurement: shunt-resistor-based and mutual inductance-based. In either case, the measurement of current requires significant overhead. First, through resistive sensing, more specifically coaxial shunt resistors, there is the problem of bulkiness of the coaxial structure and the minimal size of the resistive element that needs to dissipate an amount of power proportional to the sensed current squared. Through mutual-inductance-based techniques, a coil (such as Rogowski or pickup coil) needs to be implemented on board in order to properly measure the current with an embedded technique. However, such a coil requires a PCB section dedicated to it in addition to adding significant insertion inductance.
- **Improved bandwidth**: for shunt-resistor-based techniques, there is a compromise to be made between bandwidth and dimensions, as was highlighted in the review. In addition, for mutual inductance-based techniques, the authors could not reach GHz-range bandwidth. However, as demonstrated, with GaN HEMT technology such as is used in CPIOS, reaching GHz-range frequency for current characterization is critical to proper PI assessment.

The state-of-the-art regarding predicting voltage fluctuations onto the power rails of sensitive circuits, in terms of shape and energy spectrum, was also studied. Specifically, there is no model

for the prediction of the overall shape of voltage fluctuations onto the supply rails of adjacent devices to multiple simultaneously switching converters.

Then, several aspects of the CPIOS were presented and highlight the power integrity issues encountered in such a system. More specifically, the switch-mode converters are integrated alongside sensitive analog circuits. In order to improve the dimensions of the system, fast-switching power devices were selected. Those power devices can reach sub-ns switching time, leading to switching frequencies of up to 40 MHz with certain gate drivers. When switching, however, the DM current transient generated by the converter, which is the main source of noise aggression in CPIOS, has spectral content that ranges up to multiple GHz. For that reason, there is a need for accurate current measurement technique at these high frequencies.

Several problems for power integrity were also highlighted regarding the prediction of voltage fluctuations in the context of power systems integrating converters and sensitive analog and mixed-mode circuits, e.g., CPIOS. It was argued that simultaneous switching in arrays of switch-mode converters causes additional problems to properly predicting the voltage fluctuations onto the power rails of sensitive devices, which is critical for the operation of analog and mixed-mode ICs integrated alongside the converters.

In the third chapter, the transmission-line-based current measurement technique is presented. It uses a substrate-embedded microstrip line underneath a primary trace from which the current is measured. It is shown in a thorough analysis of the structure that the structure exhibits qualities in terms of improving the minimal on-board overhead for probing provision. The structure was implemented on a PCB with a switch-mode converter based on GaN HEMT devices. In addition to measurement distortion being measured, the measured current was also compared with the one of a resistive current shunt. The results show that the current measurement structure effectively measures currents with a better-than-3 dB accuracy at up to 1.95 GHz, which is extremely close to the targeted specification. In addition, the analysis shows that the structure can be placed

at any location on the probe, which is better than what was being done in the state-of-the-art with Rogowski and pickup coils. In addition, the analysis also shows that the structure can be made arbitrarily small in order to improve its bandwidth. All of those were elements shown to be lacking in the literature regarding current measurement techniques in power converters.

In the final chapter, a model for the prediction of the shape of voltage fluctuations caused by the switching of multiple simultaneously switching converters is presented. The model also assumes that the noise mechanism generating and propagating current transients to sensitive analog domains such as the power rails of analog and mixed-mode IC is LTI. Therefore, the impact of multiple simultaneously switching converters can be calculated through superposition. That hypothesis is motivated by a thorough analysis and explored further in measurement results. Measurement results also show that modeling the voltage fluctuation on the power rails of the sensitive circuits using a single characterized DM current and Z-parameters yield sufficient results in terms of NMSE (less than 0.75), with respect to identified specifications, and in terms of mismatch in the energy spectrum between the reference signal and predicted fluctuations (less than 10 dB over 2 GHz). Such a model improves the state-of-the-art in terms of bandwidth, and also allows the prediction of voltage transients onto sensitive nodes when multiple power converters are switching simultaneously. This has not been done in previous works.

Return on Research Objectives

Regarding the two specific objectives of the research, those were met in the chapters 3 and 4 respectively. Indeed, chapter 3 presented a technique to characterize the switching current in power converters for the CPIOS, which is critical for power integrity. Through characterization, it was shown that the technique both is a compact embedded technique for use in an SiP, including minimal probing overhead, as it is the problem in several state-of-the-art techniques and predicts fluctuations onto the power rails of sensitive circuits, in terms of shape and energy spectrum.

Chapter 4 presented a model to predict fluctuations onto the power rails of sensitive circuits, in terms of shape and energy spectrum. Results have shown that the model predicts spectral noise power density of multiple converters switching simultaneously under any condition up to the GHz range. The overall shape of the voltage is also predicted, rendering it possible to assess whether we meet breakdown voltage limitations of the IC.

It is therefore possible to conclude that the main objective of modeling power integrity constraints in CPIOS based on the different operating conditions and a thorough characterization of the system has been made, thanks to the characterization technique presented in chapter 3, and the model of chapter 4 that takes advantage of that characterization to make predictions regarding voltage fluctuations onto the power rails of sensitive devices, and therefore the relevant aspects of PI for CPIOS.

Communications and Publications

Multiple communications as well as publications stem from the work presented in this thesis. Table 5.1 presents the publications made in the context of this research work.

Table 5.1 List of publications

Title	Authors	Details
A Coupled Transmission-Line-Based Measurement Technique for Currents in Switch-Mode Converters	**Gabriel Nobert**, Nicolas G. Constantin, Yves Blaquière	Published in IEEE Transactions on Electromagnetic Compatibility in October 2023.
GHz-range Linear Modeling of Power Integrity in an Array of Simultaneously Switching Power Converters	**Gabriel Nobert**, Nicolas G. Constantin, Yves Blaquière	Submitted for publication in IEEE Transactions on Electromagnetic Compatibility October 31, 2023.
Towards an LTCC SiP for Control System in Safety-Critical Applications	**Gabriel Nobert**(60%), Abdul-Hafiz Alameh, Nam Ly, Nicolas G. Constantin and Yves Blaquière	Presented at the 2021 IEEE International Symposium on Circuits and Systems (ISCAS)
Modeling of power and signal integrity and gate driver design in Configurable Integrated Power Input/Output Systems for Avionic Applications	**Gabriel Nobert** (50%), Nam Ly, Abdul Hafiz Alameh, Nueraimaiti Aimaier, Frédéric Nabki, Glenn Cowan, Nicolas Constantin, Yves Blaquière	Poster presented at the Communications and Microelectronic Integration Laboratory (LaCIME) 1st Annual Congress - February 21, 2019

Future Works and Recommendations

Multiple issues and points of improvement were, however, encountered:

- In the results for the current measurement technique, a discrepancy between deembedded shunt resistor (reference) and the deembedded transmission-line-based structure was observed in narrow bandwidths (section 3.4.3.1). That discrepancy was not explained by measurement distortion, because the comparison was made by removing the effect of measurement distortion. One hypothesis is that at high frequency, i.e., multiple GHz, the loading condition of the secondary affects the behavior of the converter. Therefore, different measurements

are observed when using the transmission-line-based structure and the secondary is loaded compared to when the shunt resistor is measured and the secondary is not loaded. That hypothesis should be verified by loading the secondary to 50 Ω even when it is not being measured.

- Another hypothesis that should be verified for the problem above is that when evaluating measurement distortion, the low-side transistor is replaced with a wire bond. However, that wire bond has a different behavior than the transistor, making the measurement distortion characterization inaccurate at some frequency because of the difference between the purely inductive wire bond and the behavior of the low-side GaN HEMT. One way to improve those measurements would be to drive a low-side GaN HEMT to a closed state, rather than wire bonding where the low-side transistor would be, thereby accurately modeling the inductance caused by that specific component, and then characterizing measurement distortion.
- One point of improvement for the proposed model for power integrity assessment is regarding the characterization and the impact of CM currents in CPIOS PI concerns: it was hypothesized that CM current would still be present when the converter switches due to non-zero impedance of the load, which is in series with a ferrite bead (section 4.1.3). This leads to a flow of current that goes either from the high-side, or the low-side to the load. The current then comes back through either the load ground or a CM path. That problem explains one main issue with the results obtained in section 4.3.5. Indeed, it was observed that the results were significantly less accurate when attempting to predict the noise generated by the low-side turn-on events. This is consistent with lower the CM impedance in the path from the low-side of the converter to the load, leading to higher CM current, and therefore, more voltage fluctuations that are not taken into account by the DM model. In order to validate that hypothesis, a setup could be made where two current measurement structures are placed on both sides of the converter (low-side and high-side). By simultaneously measuring both

current, it is possible to evaluate both the CM and DM components in the current, thereby validating or not the hypothesis presented in this paragraph.

- Different hypotheses to simplify the characterization methodology may be explored as an interesting starting point for future work aiming at reducing the complexity of the characterization procedure. A few of those hypotheses were discussed in the section 4.1.4.

APPENDIX I

TEST BOARD DESIGN FOR GHZ-RANGE CHARACTERIZATION OF CURRENT AND VOLTAGE FLUCTUATIONS

In the chapters 3 and 4 of this thesis, several experimental setups were presented at a high level. This appendix describes in greater detail the boards that were fabricated in order to do the measurements. First, the board that was used to validate the Transmission-Line-Based current measurement technique is presented. Then, the board that was used to validate the modeling of power integrity in an array of simultaneously switching power converters. It is noteworthy to mention that this section of the thesis is better read in its digital version, which has up-scaled quality for images, rather than the printed version.

1. Validation Board of Current Measurement Technique

The presentation of the board, which is referred to the *current measurement validation board* in this section, is made into three sections, first a block-level description of the board is made. Then, the schematics of the board are presented and several design choices are explained. Finally, the board layout is given, along with explanations.

1.1 Block-Level Description

The board can be split into two main sections: the converter section and the so-called *host* section, which contains all the powering and connectivity. The two sections are separated from each other with only the power being connected through a single point. Those sections are depicted in the figures I-1 and I-2. The color code of these figures is the following. Red represents the power domain of the converter, blue represents the power domain of the gate driver, yellow separations represent ground-connected power domains and white separations represent unconnected grounds. The different section of the circuits are depicted in light gray. The placement in the block diagram is consistent with what is presented in the layout.

1.1.1 FPGA-Based Driving of the Converter

In order to keep the design as simple as possible, the converters will be driven by an FPGA development board. The FPGA development board (Digilent Nexys Video, based on an Artix-7 FPGA) contains an application that generates arbitrary complementary PWM signals with a resolution of 2.5 ns. The PWM signals can have dead times, also with a resolution of 2.5 ns. The PWM signals are output through one of the Peripheral MODule (PMOD) interface on the board, and then connected to a 2x2 header connector on the current measurement validation board. Two pins for power, and two for the complementary PWM signal. Those two complementary PWM signals drive the primary of a digital isolator (ISO7760). In order to prevent ringing at the isolator due to the cable inductance and transmission-line effects between the 2x2 header

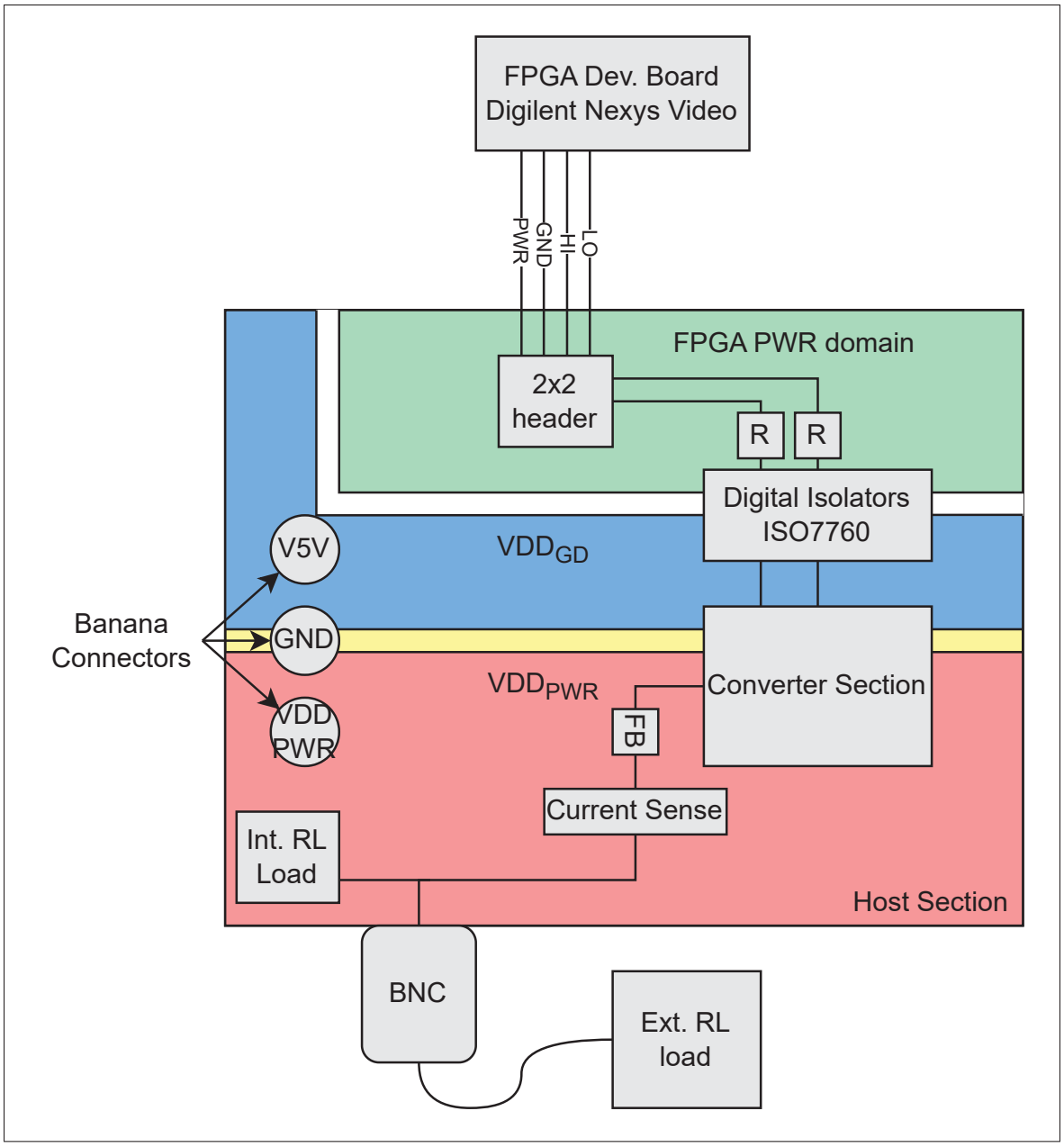

Figure-A I-1 Block Diagram of the host section (current measurement technique validation board)

and the development board, a damping resistor was added before the isolator to add a low-pass characteristic to the signal going to the isolator. The primary is connected to its own power supply, which is in the power domain of the FPGA board. The ground of the primary side is not connected with the rest of the board in order to protect the FPGA development board in case of powering issues. The secondary, which is in the same power domain as the gate driver, is

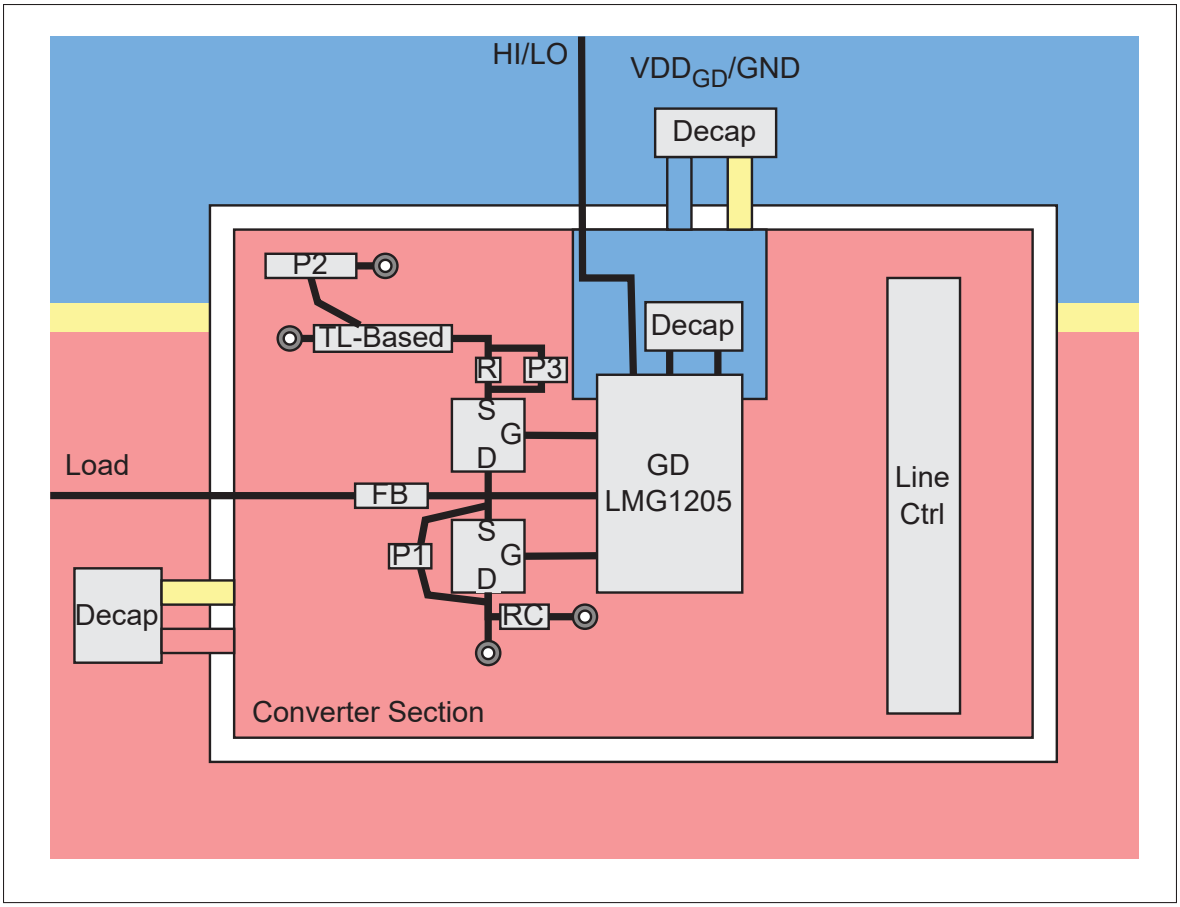

Figure-A I-2 Block Diagram of the converter section (current measurement technique validation board)

then connected to the low-side and high-side input signal pins of the gate driver, which is the LMG1205.

1.1.2 Host and Converter Sections Powering

Three power domains are present on the board, the first one is the FPGA section's, which, as explained in the previous section, is completely separated and not ground-connected. The two other domains are the converter's power domain for gate driving (VDD_{GD}) and the half-bridge's power domain (VDD_{PWR}). Again with the idea of keeping the design as simple as possible, no powering circuit was implemented on the current measurement validation board. Rather, banana connectors were used and the whole board was powered through external power supplies. On the board itself, two bulk decoupling capacitors of approximately 100 µF are placed at the banana connector inputs for each of VDD_{PWR} and VDD_{GD}. A 0 Ω resistor is used in order to make the connection between the converter and the host sections of the board for each power domain. The ground return is also done through a single trace for each of those. This ensures a

better control of the current returns from the load to the converter, which is also believed to be useful to properly characterize the current measurement technique. Before that 0 Ω resistor connection, on the host section of the board, a 4.7 µF decoupling capacitor is placed. On the converter section itself, only local decoupling is used. The gate driver is locally decoupled with 1 µF, while the half-bridge is decoupled with a series combination of a 100 nF and a 2 Ω resistor (RC in Figure I-2) for the reasons explained in section 3.3.2.

1.1.3 Gate Driving Circuit

The gate driver (GD) is Texas Instruments' LMG1205. The device has a pull-up (LOH) and pull-down (LOL) pin for the gate voltage. As recommended by the manufacturer, the pull-down pin is always directly connected to the gate of the device in order to ensure fast turn-off of the transistors. The pull-up pin is put in series with a 0201 resistor pad, which was put to 0 Ω for the experiments, before the gate of the transistor. A bootstrap capacitor of 100 nF has been used. The rest of the bootstrapping circuitry is integrated in the gate driver.

1.1.4 Transmission-Line Impedance Quality Control

Two long microstrip lines with the same length as for the current measurement technique were added in the converter section (Line Ctrl in Figure I-2). They were placed far from the converter, but with the same width and ground layer as with the current measurement technique. The goal is to measure the characteristic impedance of the transmission-line-based current measurement technique and ensure it is indeed 50 Ω. One of the lines terminated with a short and the other was left open. A GSG pad is placed on the other side of those lines for the measurement of S11 with a VNA. The S11 measurement is then used in order to estimate the characteristic impedance.

1.1.5 Converter Loading Circuit

The converter is connected to two BNC connectors. One of them has the shielding connection connected to VDD_{PWR}, while the other is connected to the ground. During the tests, only one of those is connected. As explained in the thesis, the converter is loaded with a resistive-inductive (RL) load. That RL load is connected to the BNC connector. For the measurements presented in the thesis, the converter is put in DPT configuration by using the one that has the shielding connection connected to VDD_{PWR}. Before the load, there are two pads for ferrite beads (FB in figures I-1 and I-2), for which the purpose is explained in section 3.3.3, as well as one pad for a current shunt resistor to measure the load current. During the tests, only one of the ferrite bead pads was populated. The ferrite bead used was a BLM15EX331SN1D, which fits on a 0402-sized pad. The other pad for a ferrite bead was shorted with a 0 Ω resistor. The board itself also has on-board pads for connecting an RL load directly with SMD (Int. RL Load in Figure I-1) component on the board. However, those were unpopulated during the tests.

1.2 Schematics

It is important to note that several passive structures described in the previous sections were implemented directed in the layout. The schematics are presented in Figure I-3, each of the specific circuit in the schematics is explained previously in the block diagram section.

1.3 Layout

The layout of both the converter and host sections are presented in the figures I-4 to I-7. A 3D view of the converter section is shown in Figure I-8. It is important to mention that red represents the top layer, yellow represents the second layer, teal represents the third layer and blue represents the bottom layer. Four vias were placed in the corners of the host section in order to add spacers (Figure I-4), which were later on connected to an aluminum base as can be seen in Figure 4.7(b) and Figure 3.8(b).

Regarding the stackup of the board, the thickness of the board is 0.42 mm with a dielectric core thickness of 0.2 mm connecting the layers 2 and 3. The top and bottom layers were added using a prepreg material with a thickness of 0.11 mm. The substrate was FR-4, which has a typical relative dielectric constant (ϵ_r) of 4.3.

Regarding the converter section of the board, one of the important parts is the microstrip in yellow (second layer) microstrip connected to pad J9 (Figure I-6). That trace has a width of 0.4 mm. It represents the transmission-line-based current measurement structure. It can also be noted that the third layer (teal) is poured with ground, while the fourth layer contains unconnected powers for the gate driver (VDD_{GD}) and the converter (VDD_{PWR}).

2. Validation Board of Power Integrity Modeling

This section follows the same format as in section 1. The block diagram of the system is presented, then the schematics and after that the layout is explained.

2.1 Block-level description

The power integrity modeling validation board, which is depicted in Figure I-9, works in a similar way than for the current measurement technique. Indeed, the board is again split into three power domains. The different elements in the host section are the same. Only two big differences are present:

- Four converters are present instead of one;
- An ADC that is not used in the measurement has been added for future works;

Regarding the ADC connectivity block diagram: it is not explained in this appendix, because it is completely unused and could be removed in future experiments. The goal of that ADC was to

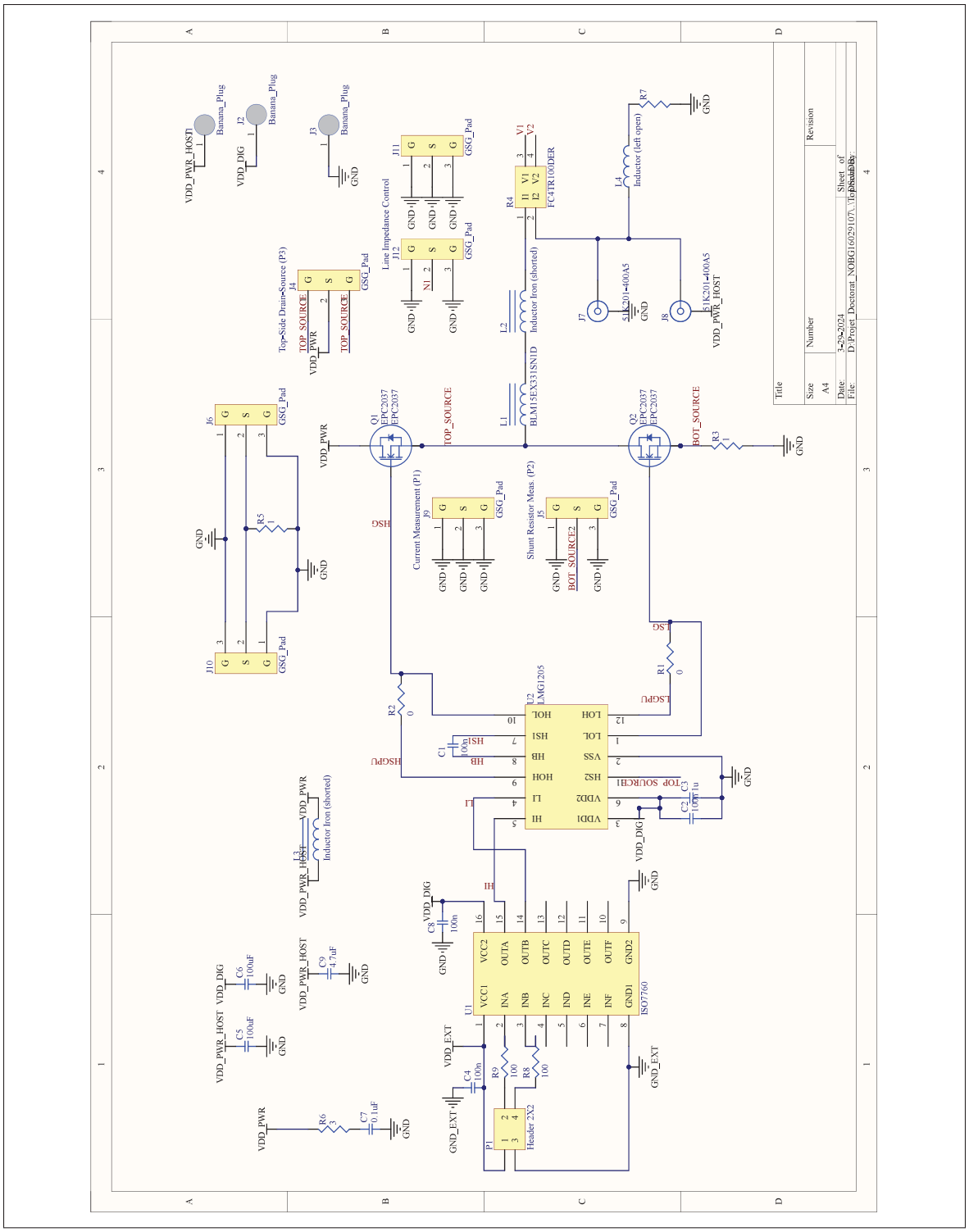

Figure-A I-3 Schematics for the current measurement setup

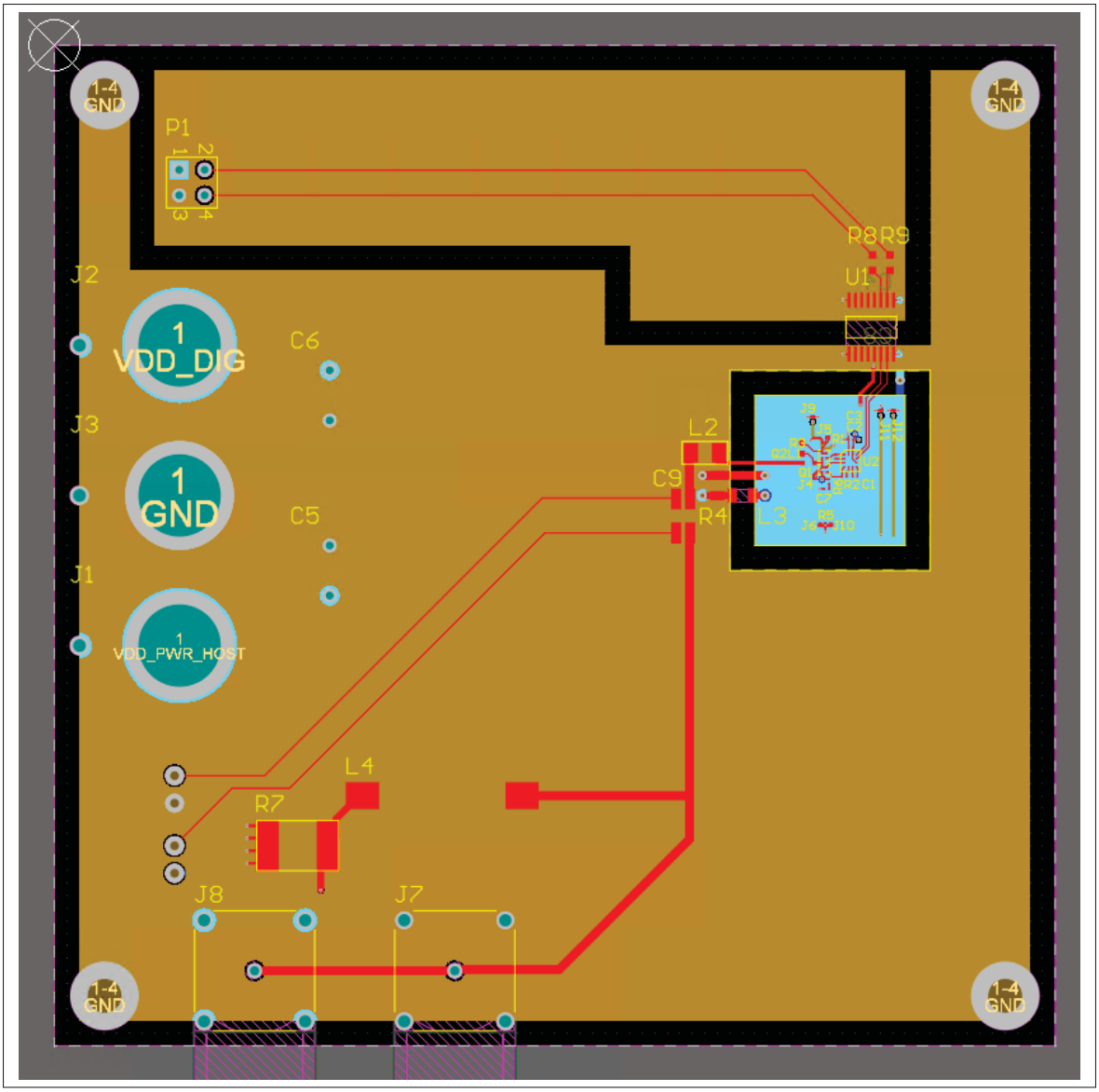

Figure-A I-4 Top-side layout of the host section (current measurement technique validation board)

potentially measure the impact of the voltage fluctuations on its output codes, but it was not done in this work. It is, however, present in the schematics and the layout.

A block diagram of the converter section is presented in the Figure I-10. In order to keep it consistent with the layout of the board, the figure for the block diagram has been made wide, which impedes its readability in a printed format of this thesis. Much like the schematics, this figure can be better read in a digital format of the thesis. In the converter section presented, four converters were implemented (SU1-SU4, as labeled in the layout). One thing that can

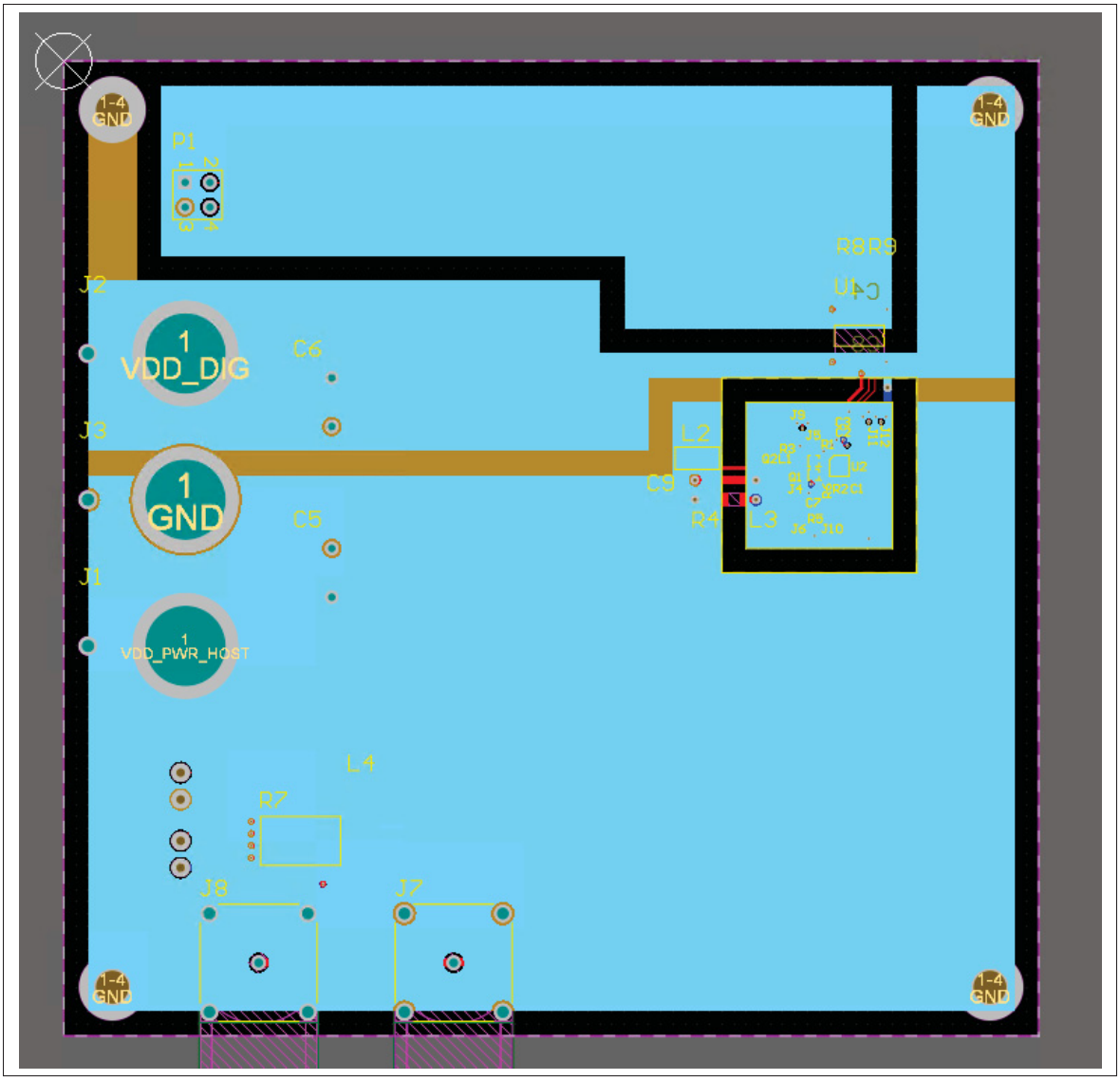

Figure-A I-5 Bottom-side layout of the host section (current measurement technique validation board)

be noticed, when compared with the block diagram of the current measurement technique, is that the shunt resistor for current measurement is no longer present and has been completely replaced with only the transmission-line-based technique. The different ports (P1-P9) follow the same numbering convention as presented in Figure 4.8 of this thesis. Indeed, P9 is the victim, which is the power planes for the powering of the converters. P1 to P4 represent the drain and source terminals of the high-side transistor. P5 to P8 represent the secondary of the transmission-line-based structure. Careful planning needs to be done when probing those ports. Indeed, some of those have been carefully rotated with a given angle in order to be able to probe some of the ports simultaneously, because each GSG probe covers an angle of approximately

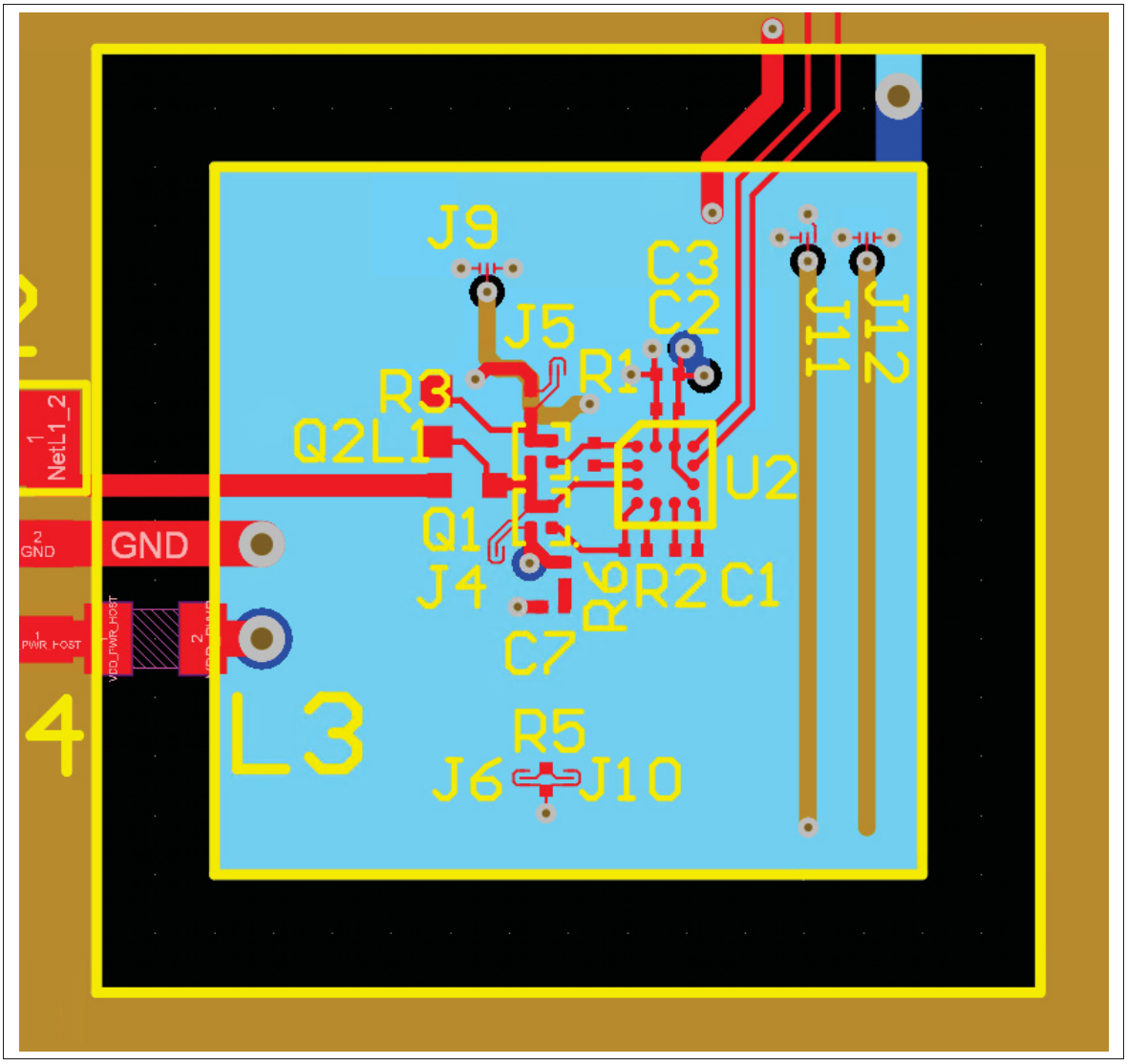

Figure-A I-6 Top-side layout of the converter section (current measurement technique validation board)

60°. Namely, P5 and P8 must be probed simultaneously in order to measure the delay between the two switching transients. In addition, each group of ports (P1-P4, P5-P8 and P9) need to be measured simultaneously, two at a time, either with a VNA or an oscilloscope. The arrows connected to each port represent from which direction the GSG probe head comes from.

2.2 Schematics

The schematics are split on two different sheets: The host section is presented in Figure I-11 and each individual converter of the converter section is presented in Figure I-12. Namely,

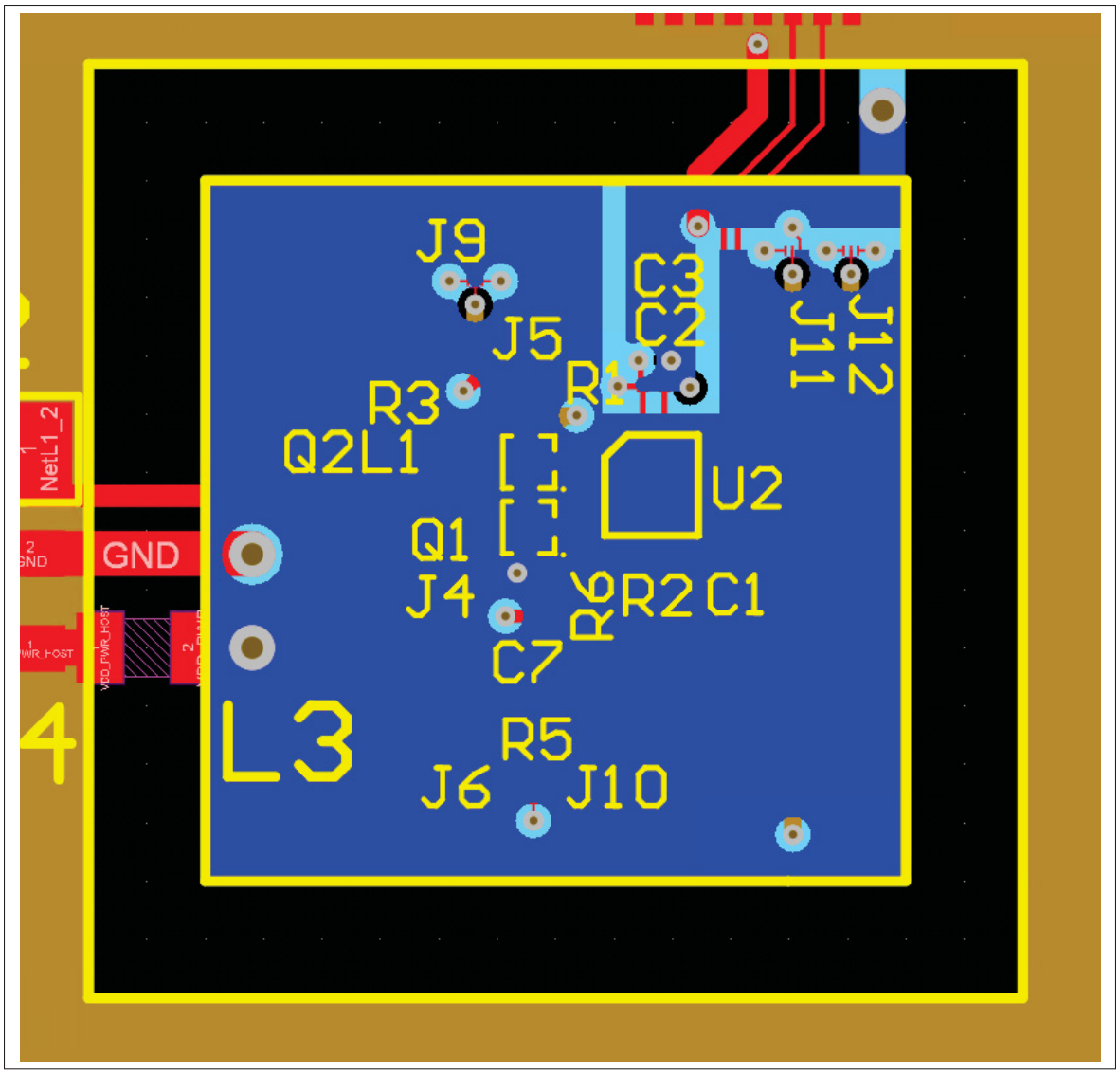

Figure-A I-7 Bottom-side layout of the converter section (current measurement technique validation board)

many components were added as a provision in order not to have to refabricate the board if something was missing. Therefore, in both sections of the board, unpopulated or shorted (with a 0 Ω resistor) components can be seen. Those components can be safely ignored in a redesign of that board.

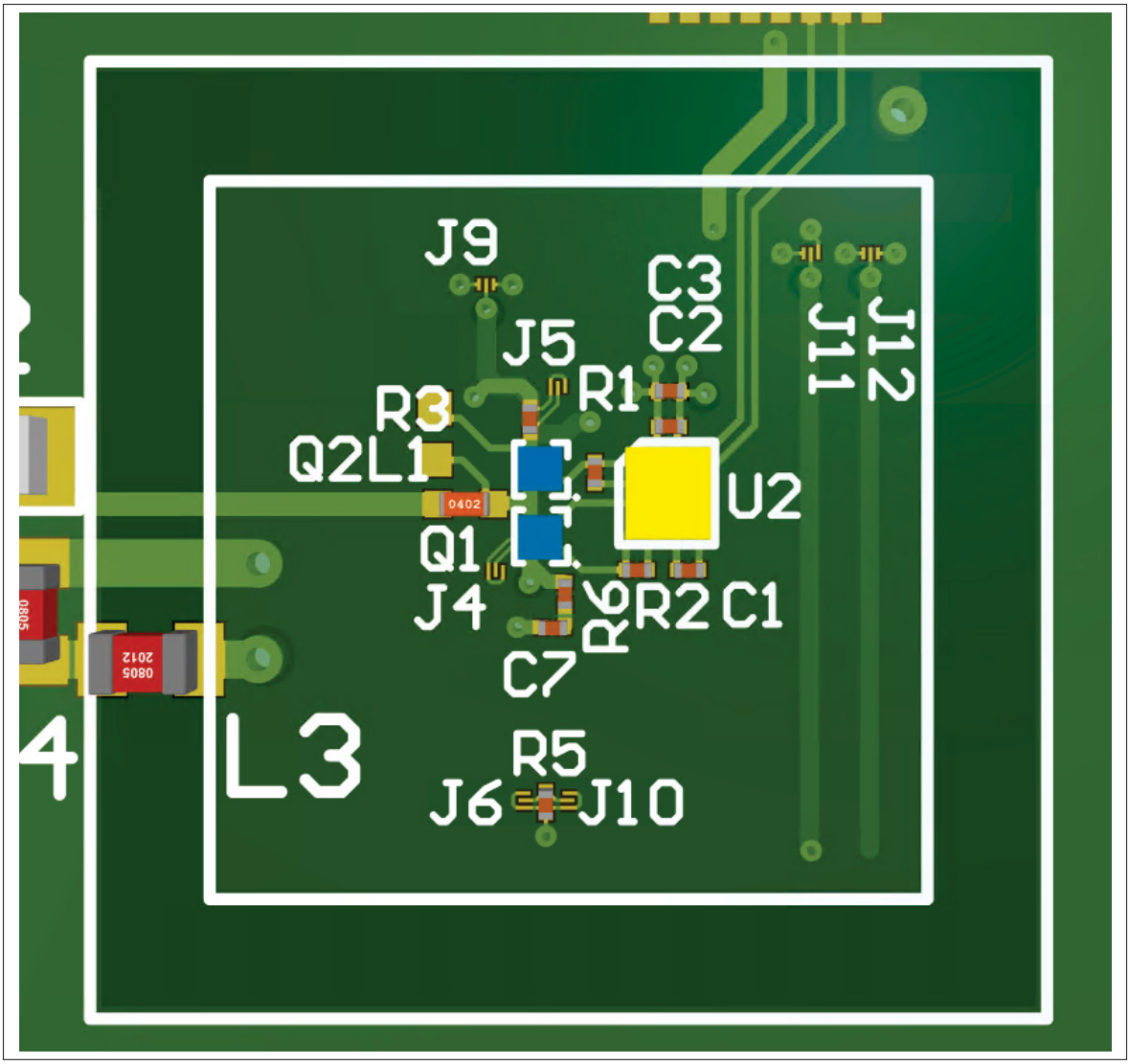

Figure-A I-8 Mechanical layout of the converter section (current measurement technique validation board)

2.3 Layout

The layout again is presented from Figure I-13 to Figure I-16. The different parts of the layout are kept consistent with the block diagrams of figures I-9 and I-10. Mechanical drawings of both sections have also been added in the figures I-18 and I-17.

The stackup of that board was a dielectric core of 0.465 mm between the layers 2 and 3, while the top and bottom were assembled using a 0.1 mm prepreg material with a relative dielectric constant (ϵ_r) of 4.05. The relative dielectric constant of the core was 4.5. The trace width of the current measurement technique is 0.5 mm.

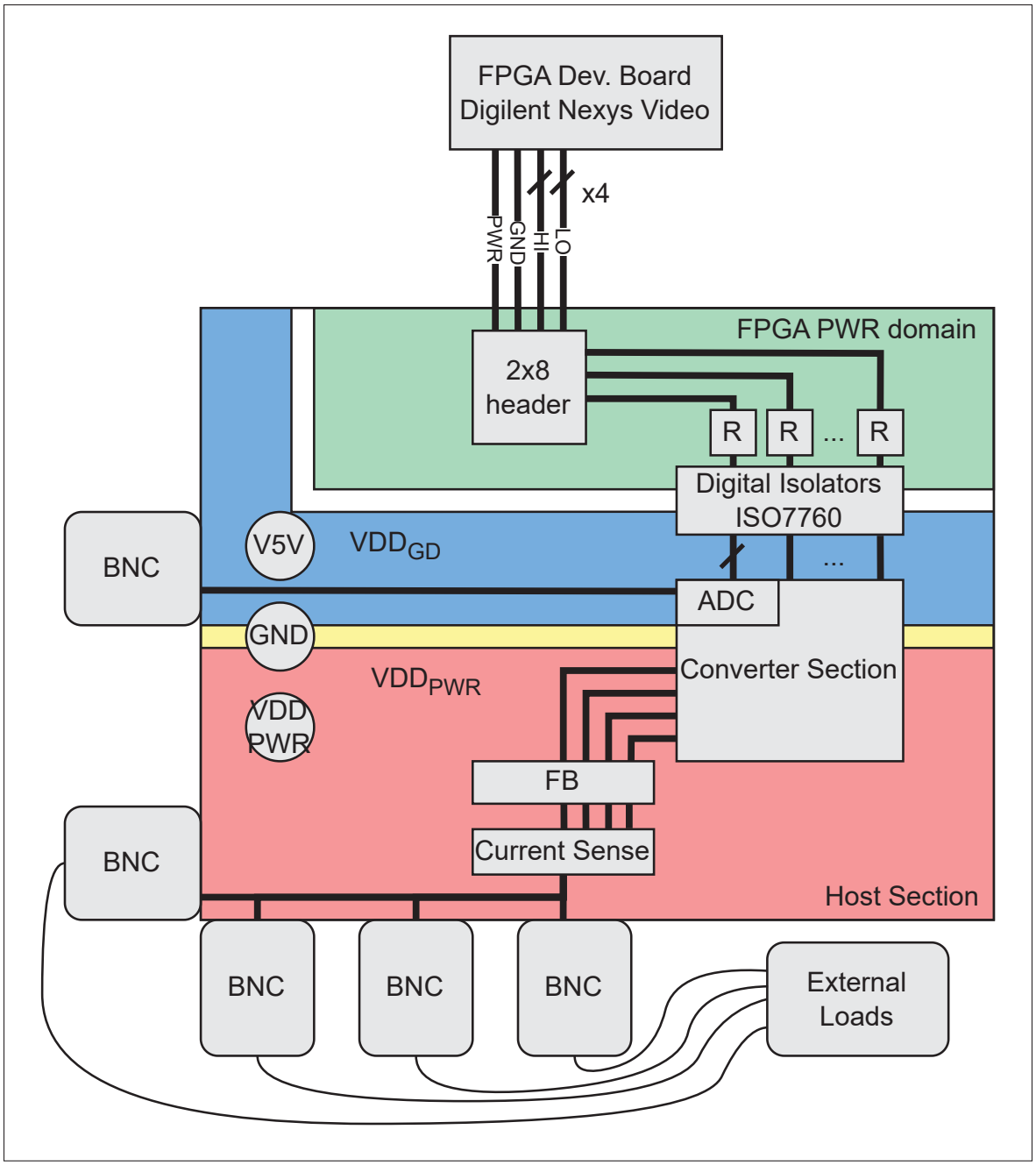

Figure-A I-9 Block Diagram of the host section (power integrity modeling validation board)

Just like the current measurement validation board, four vias are placed in the corners of the boards for connection with a spacer that itself is screwed into a very mechanically robust aluminum base (Figure 4.7(b) and Figure 3.8(b)).

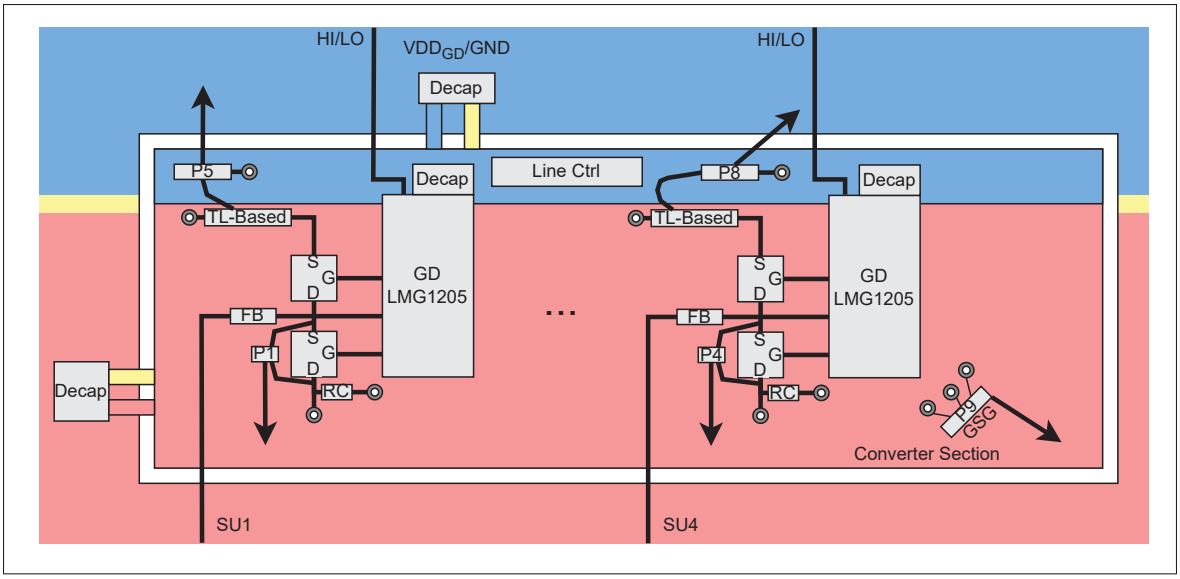

Figure-A I-10 Block Diagram of the converter section (power integrity modeling validation board)

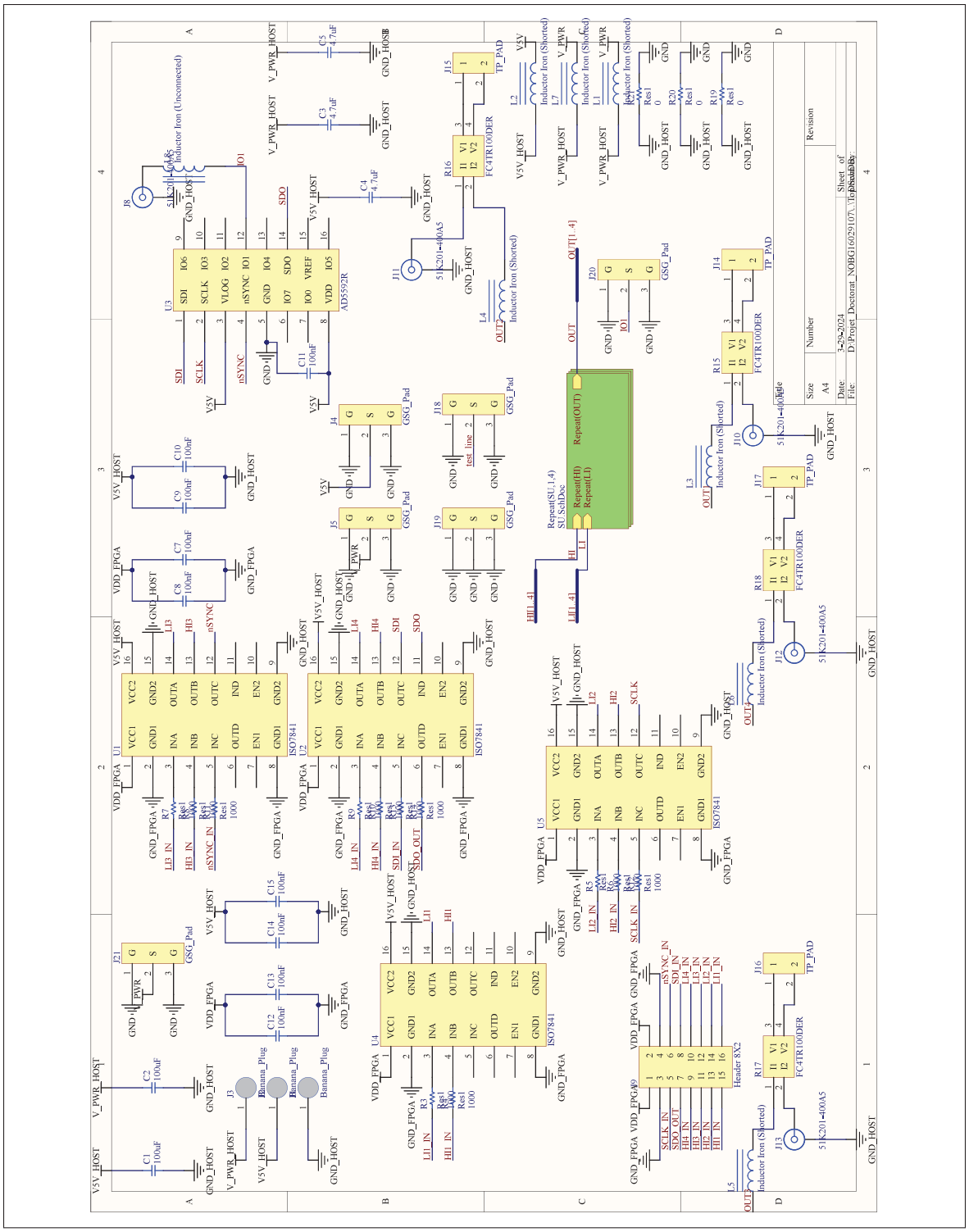

Figure-A I-11 Schematics for the power integrity modeling validation board

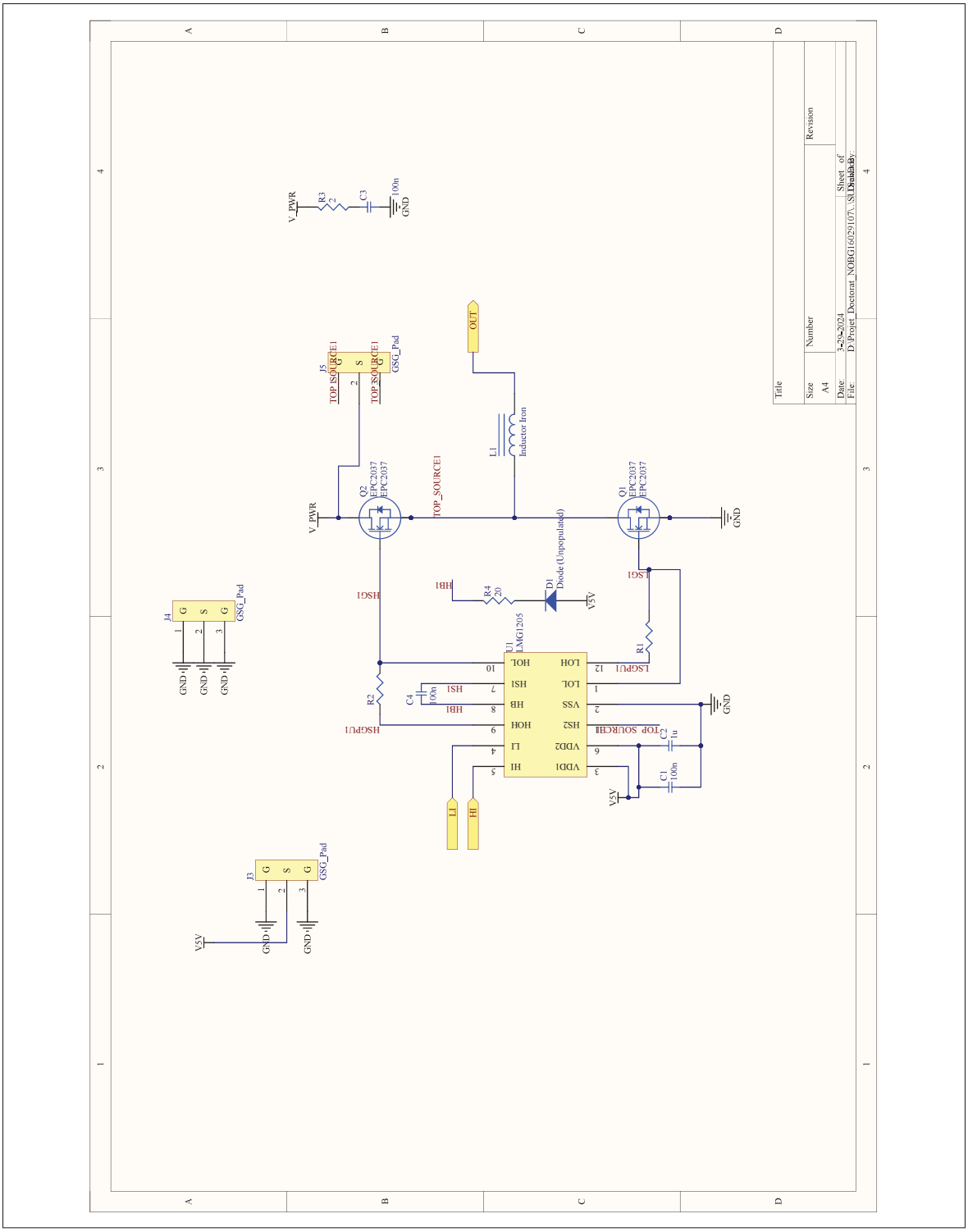

Figure-A I-12 Schematics for the power integrity modeling validation board

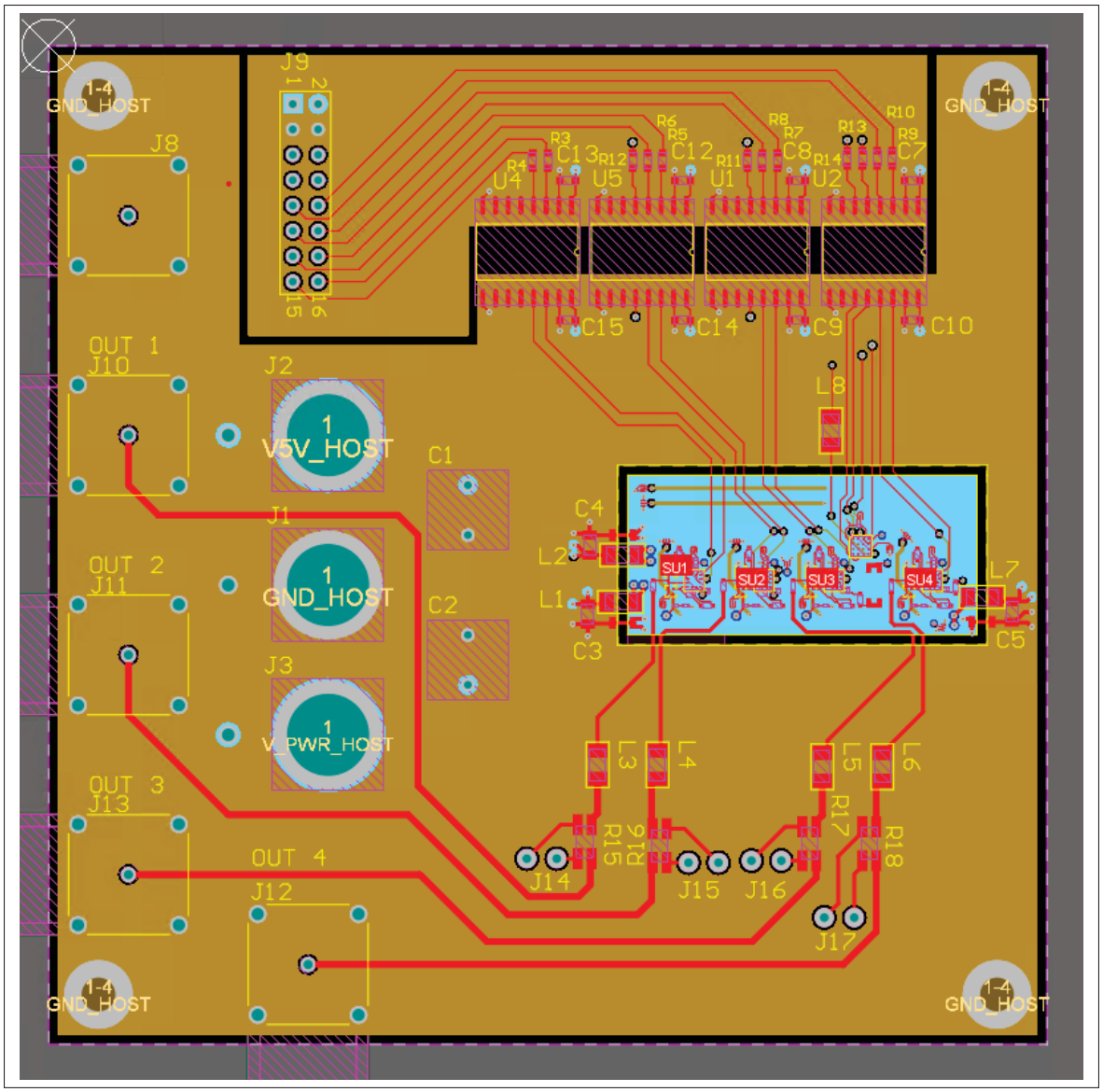

Figure-A I-13 Top-side layout of the host section (power integrity modeling validation board)

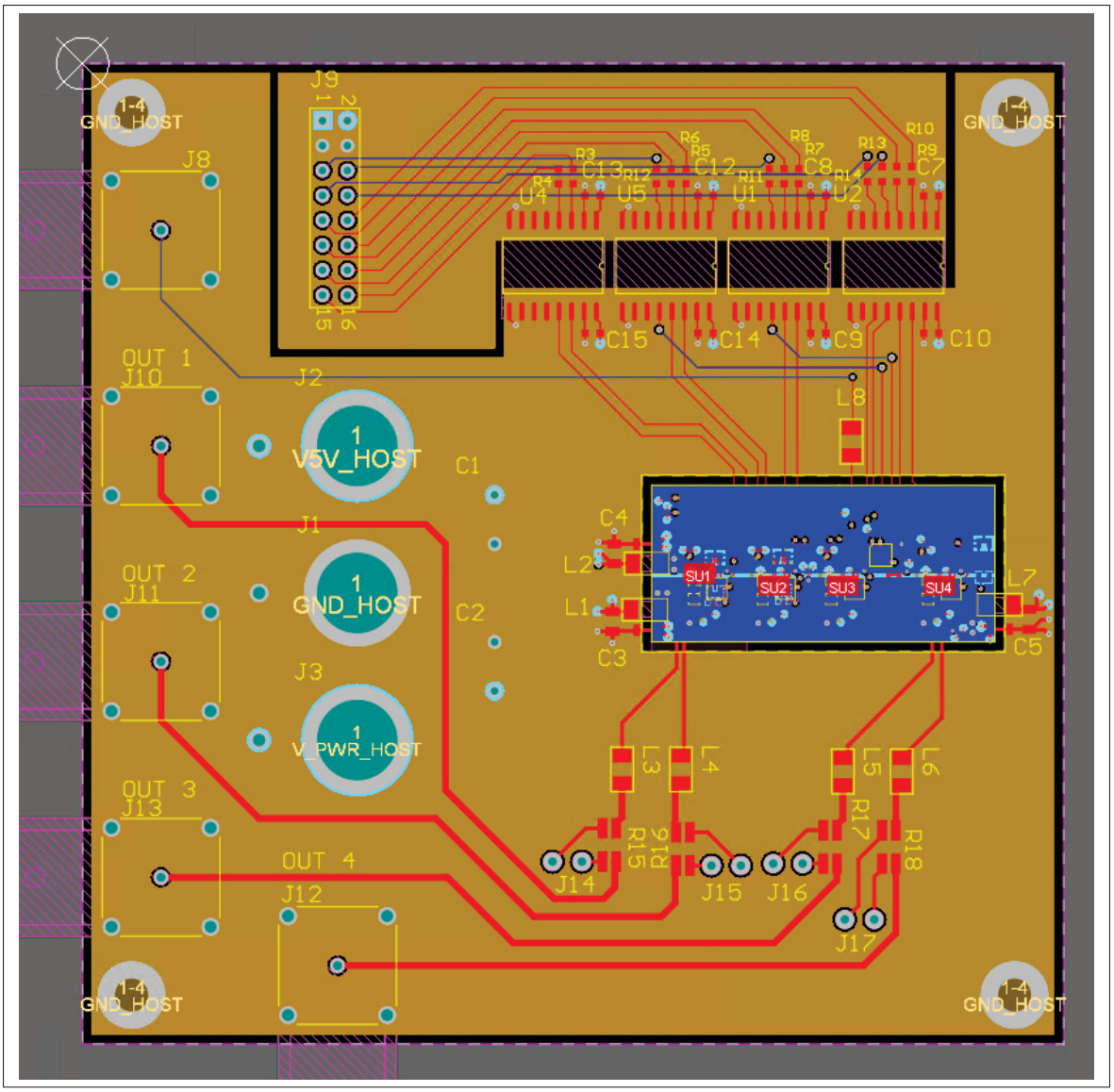

Figure-A I-14 Bottom-side layout of the host section (power integrity modeling validation board)

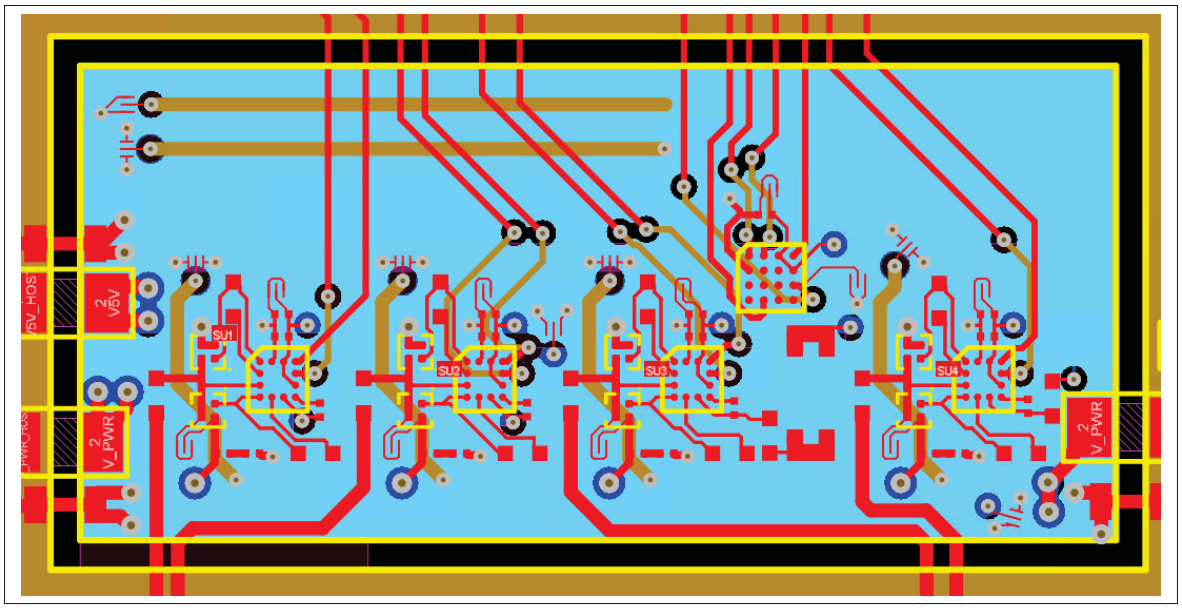

Figure-A I-15 Top-side layout of the converter section (power integrity modeling validation board)

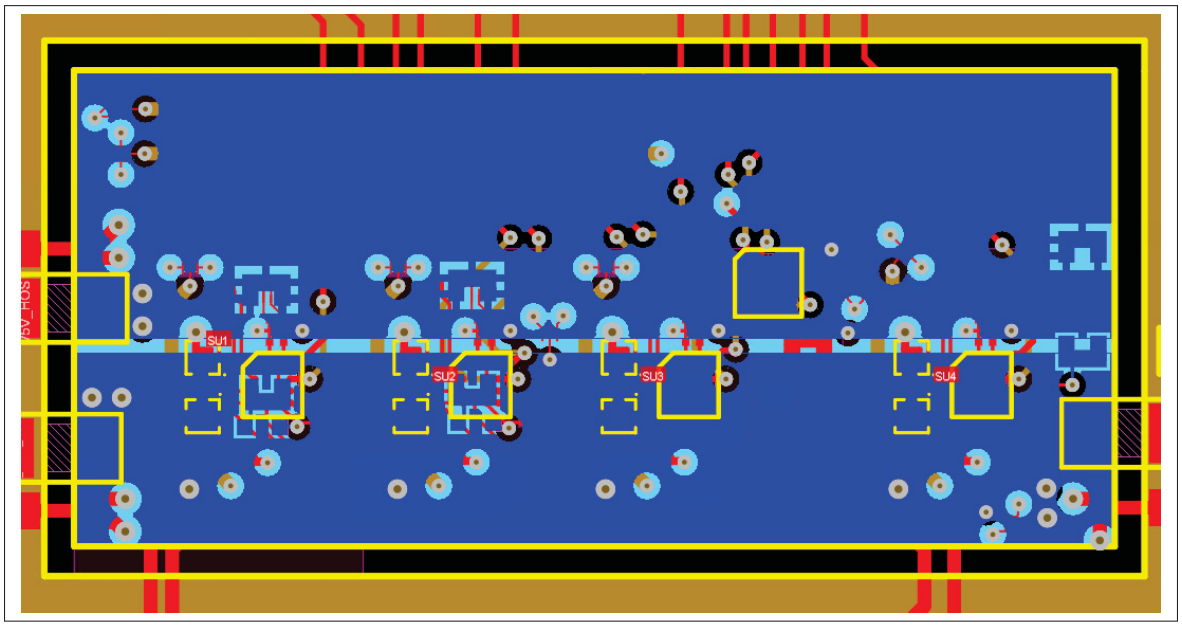

Figure-A I-16 Bottom-side layout of the converter section (power integrity modeling validation board)

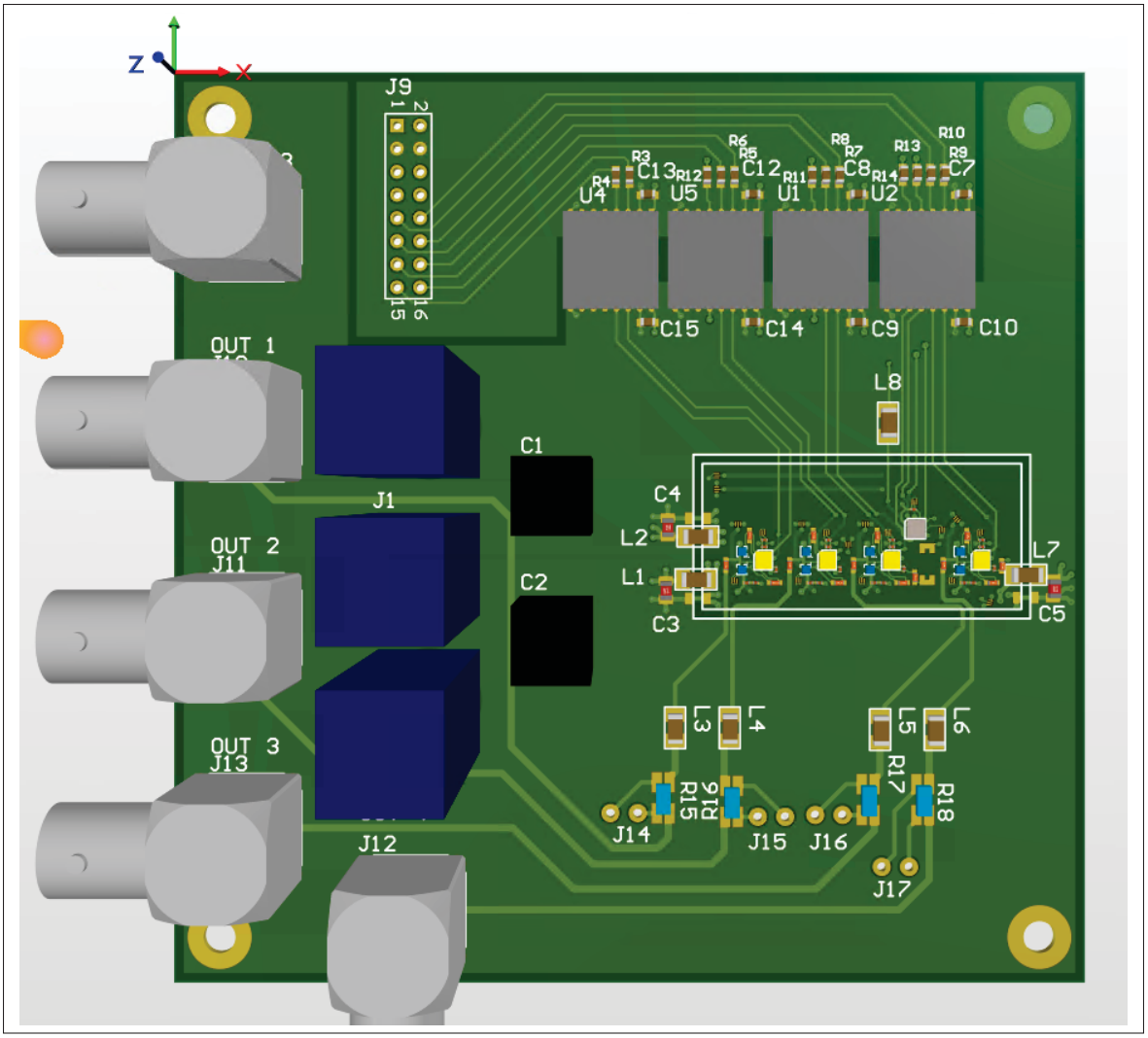

Figure-A I-17 Mechanical layout of the host section (power integrity modeling validation board)

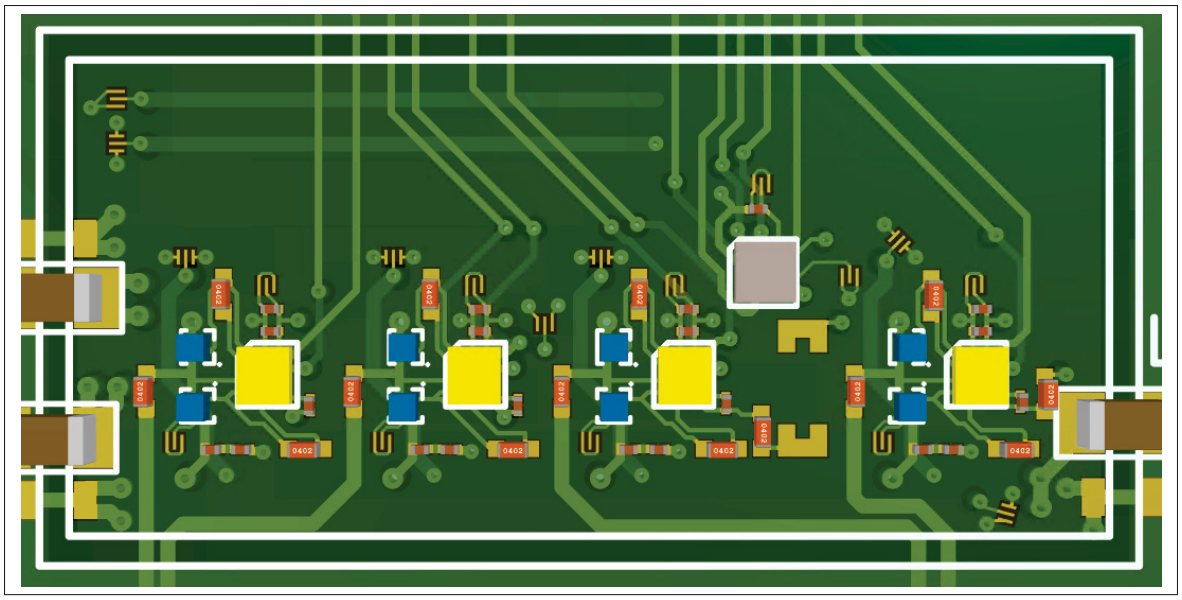

Figure-A I-18 Mechanical layout of the converter section (power integrity modeling validation board)

LIST OF REFERENCES

ANSYS. (2022). Ansys Q3D Extractor. Retrieved on 2022-11-18 from: https://www.ansys.com/content/dam/amp/2022/may/asset-creation/q3d-extractor-datasheet/ansys-q3d-extractor-datasheet.pdf.

Archambeault, B. & Ruehli, A. (2001). Analysis of power/ground-plane EMI decoupling performance using the partial-element equivalent circuit technique. *IEEE Transactions on Electromagnetic Compatibility*, 43(4), 437-445. doi: 10.1109/15.974623.

Bae, B., Shim, Y., Koo, K., Cho, J., Pak, J. S. & Kim, J. (2013). Modeling and Measurement of Power Supply Noise Effects on an Analog-to-Digital Converter Based on a Chip-PCB Hierarchical Power Distribution Network Analysis. *IEEE Transactions on Electromagnetic Compatibility*, 55(6), 1260-1270. doi: 10.1109/TEMC.2013.2250506.

Baisden, A. C., Boroyevich, D. & Wang, F. (2010). Generalized Terminal Modeling of Electromagnetic Interference. *IEEE Transactions on Industry Applications*, 46(5), 2068-2079. doi: 10.1109/TIA.2010.2058836.

Casamayor, M. (2022). A First Approach to IBIS Models: What They Are and How They Are Generated. Retrieved on 2022-12-06 from: https://www.analog.com/media/en/technical-documentation/application-notes/an-715.pdf.

Clemente, S., Pelly, B. R. & Isidori, A. (1982). In *HEXFET Databook - Power MOSFET Application and Product Data* (ch. 8). International Rectifier.

Danilovic, M., Chen, Z., Wang, R., Luo, F., Boroyevich, D. & Mattavelli, P. (2011). Evaluation of the switching characteristics of a gallium-nitride transistor. *2011 IEEE Energy Conversion Congress and Exposition*, pp. 2681-2688. doi: 10.1109/ECCE.2011.6064128.

Dghais, W. & Rodriguez, J. (2016). New Multiport I/O Model for Power-Aware Signal Integrity Analysis. *IEEE Transactions on Components, Packaging and Manufacturing Technology*, 6(3), 447-454. doi: 10.1109/TCPMT.2015.2512911.

Dghais, W., Souilem, M., Zayer, F. & Chaari, A. (2018). Power Supply- and Temperature-Aware I/O Buffer Model for Signal-Power Integrity Simulation. *Mathematical Problems in Engineering*, 2018, 9.

Efficient Power Conversion. (2020). EPC2037 – Enhancement Mode Power Transistor. Retrieved on 2022-11-10 from: https://epc-co.com/epc/Portals/0/epc/documents/datasheets/EPC2037_datasheet.pdf.

Ferreira, J., Cronje, W. & Relihan, W. (1992). Integration of high frequency current shunts in power electronic circuits. *PESC '92 Record. 23rd Annual IEEE Power Electronics Specialists Conference*, pp. 1284-1290 vol.2. doi: 10.1109/PESC.1992.254728.

Fritz, N., Neeb, C. & Doncker, R. (2015). A PCB Integrated Differential Rogowski Coil for Non-Intrusive Current Measurement Featuring High Bandwidth and dv/dt Immunity. doi: 10.17877/DE290R-7459.

Heidari, H., Bonizzoni, E., Gatti, U. & Maloberti, F. (2015). A CMOS Current-Mode Magnetic Hall Sensor With Integrated Front-End. *IEEE Transactions on Circuits and Systems I: Regular Papers*, 62(5), 1270-1278. doi: 10.1109/TCSI.2015.2415173.

Ishibashi, N., Manepalli, L. K., Nath, D., Nayak, B. P., Kadam, S. & Gope, D. (2021). Black-Box DC-DC Integrated Circuit Modeling towards Design for EMC in Automotive Electronics. *2021 IEEE International Joint EMC/SI/PI and EMC Europe Symposium*, pp. 810-814. doi: 10.1109/EMC/SI/PI/EMCEurope52599.2021.9559210.

Johnson, H. W., Graham, M. et al. (1993). *High-speed digital design: a handbook of black magic*. Prentice Hall Englewood Cliffs, NJ.

Keysight. (2022a). Retrieved on 2022-10-28 from: https://www.keysight.com/ca/en/product/N2783B/ac-dc-current-probe-100-mhz-30-arms.html.

Keysight. (2022b). Transient and Convolution Simulation Description. Retrieved on 2022-11-18 from: https://edadocs.software.keysight.com/display/ads2009/Transient+and+Convolution+Simulation+Description.

Kharanaq, F. A., Emadi, A. & Bilgin, B. (2020). Modeling of Conducted Emissions for EMI Analysis of Power Converters: State-of-the-Art Review. *IEEE Access*, 8, 189313-189325. doi: 10.1109/ACCESS.2020.3031693.

Kim, H., Cho, J., Achkir, B. & Fan, J. (2018). Modeling and Measurement of Ground Bounce Induced by High-Speed Output Buffer With On-Chip Low-Dropout (LDO) Regulator. *IEEE Transactions on Electromagnetic Compatibility*, 60(4), 1022-1025. doi: 10.1109/TEMC.2017.2759123.

Kim, J., Lee, W., Shim, Y., Shim, J., Kim, K., Pak, J. S. & Kim, J. (2010). Chip-Package Hierarchical Power Distribution Network Modeling and Analysis Based on a Segmentation Method. *IEEE Transactions on Advanced Packaging*, 33(3), 647-659. doi: 10.1109/TADVP.2010.2043673.

Kim, J., Li, L., Wu, S., Wang, H., Takita, Y., Takeuchi, H., Araki, K., Fan, J. & Drewniak, J. L. (2012). Closed-Form Expressions for the Maximum Transient Noise Voltage Caused by an IC Switching Current on a Power Distribution Network. *IEEE Transactions on Electromagnetic Compatibility*, 54(5), 1112-1124. doi: 10.1109/TEMC.2012.2194786.

Kim, W. (2011). Estimation of Simultaneous Switching Noise From Frequency-Domain Impedance Response of Resonant Power Distribution Networks. *IEEE Transactions on Components, Packaging and Manufacturing Technology*, 1(9), 1359-1367. doi: 10.1109/TCPMT.2011.2157503.

Kondrath, N. & Kazimierczuk, M. K. (2009). Bandwidth of Current Transformers. *IEEE Transactions on Instrumentation and Measurement*, 58(6), 2008-2016. doi: 10.1109/TIM.2008.2006134.

Li, K., Videt, A. & Idir, N. (2015a). Using Current Surface Probe to Measure the Current of the Fast Power Semiconductors. *IEEE Transactions on Power Electronics*, 30(6), 2911-2917. doi: 10.1109/TPEL.2014.2373400.

Li, K., Videt, A. & Idir, N. (2015b). Using Current Surface Probe to Measure the Current of the Fast Power Semiconductors. *IEEE Transactions on Power Electronics*, 30(6), 2911-2917. doi: 10.1109/TPEL.2014.2373400.

Liu, Q., Shen, W., Wang, F., Boroyevich, D., Stefanovic, V. & Arpilliere, M. (2003). Experimental evaluation of IGBTs for characterizing and modeling conducted EMI emission in PWM inverters. *IEEE 34th Annual Conference on Power Electronics Specialist, 2003. PESC '03.*, 4, 1951-1956 vol.4. doi: 10.1109/PESC.2003.1217751.

Liu, Q., Wang, F. & Boroyevich, D. (2006). Modular-Terminal-Behavioral (MTB) Model for Characterizing Switching Module Conducted EMI Generation in Converter Systems. *IEEE Transactions on Power Electronics*, 21(6), 1804-1814. doi: 10.1109/TPEL.2006.882903.

Liu, Z., Huang, X., Lee, F. C. & Li, Q. (2014). Package Parasitic Inductance Extraction and Simulation Model Development for the High-Voltage Cascode GaN HEMT. *IEEE Transactions on Power Electronics*, 29(4), 1977-1985. doi: 10.1109/TPEL.2013.2264941.

Ly, N., Aimaier, N., Alameh, A. H., Blaquière, Y., Cowan, G. & Constantin, N. G. (2020). A High Voltage Multi-Purpose On-the-fly Reconfigurable Half-Bridge Gate Driver for GaN HEMTs in 0.18-μm HV SOI CMOS Technology. *2020 18th IEEE International New Circuits and Systems Conference (NEWCAS)*, pp. 178-181. doi: 10.1109/NEWCAS49341.2020.9159781.

Ming, L., Xin, Z., Yin, C., Loh, P. C. & Liu, Y. (2019). Screen-Returned PCB Rogowski Coil for the Switch Current Measurement of SiC Devices. *2019 IEEE Applied Power Electronics Conference and Exposition (APEC)*, pp. 958-964. doi: 10.1109/APEC.2019.8721915.

Motz, M., Ausserlechner, U., Bresch, M., Fakesch, U., Schaffer, B., Reidl, C., Scherr, W., Pircher, G., Strasser, M. & Strutz, V. (2012). A miniature digital current sensor with differential Hall probes using enhanced chopping techniques and mechanical stress compensation. *SENSORS, 2012 IEEE*, pp. 1-4. doi: 10.1109/ICSENS.2012.6411161.

Nguyen, V. H., Aimaier, N., Nobert, G., Pham, T., Constantin, N., Blaquière, Y. & Cowan, G. (2022). A Reconfigurable Power System-in-Package Module using GaN HEMTs and IC Bare Dies on LTCC Substrate: Design - Implementation - Experiment and Future Directions. *2022 20th IEEE Interregional NEWCAS Conference (NEWCAS)*, pp. 188-192. doi: 10.1109/NEWCAS52662.2022.9842234.

Nobert, G., Alameh, A.-H., Ly, N., Constantin, N. G. & Blaquière, Y. (2021). Towards an LTCC SiP for Control System in Safety-Critical Applications. *2021 IEEE International Symposium on Circuits and Systems (ISCAS)*, pp. 1-5. doi: 10.1109/ISCAS51556.2021.9401066.

Nobert, G., Constantin, N. G. & Blaquière, Y. (2023). A Coupled Transmission-Line-Based Measurement Technique for Currents in Switch-Mode Converters. *IEEE Transactions on Electromagnetic Compatibility*, 65(5), 1535-1547. doi: 10.1109/TEMC.2023.3300988.

Nobert, G., Constantin, N. G. & Blaquière, Y. (submitted for publication). GHz-range Linear Modeling of Power Integrity in an Array of Simultaneously Switching Power Converters.

Pearson Electronics Inc. (2022). Pearson Current Monitor 6585. Retrieved on 2022-10-24 from: http://www.pearsonelectronics.com/pdf/6585.pdf.

Pozar, D. (2011). *Microwave Engineering, 4th Edition*. Wiley.

pSemi. (2022). UltraCMOS® High-speed FET Driver, 40 MHz. Retrieved on 2022-11-09 from: https://www.psemi.com/pdf/datasheets/pe29102ds.pdf.

Pulici, P., Girardi, A., Vanalli, G. P., Izzi, R., Bernardi, G., Ripamonti, G., Strollo, A. G. M. & Campardo, G. (2008). A Modified IBIS Model Aimed at Signal Integrity Analysis of Systems in Package. *IEEE Transactions on Circuits and Systems I: Regular Papers*, 55(7), 1921-1928. doi: 10.1109/TCSI.2008.918203.

Ramboz, J. (1996). Machinable Rogowski coil, design, and calibration. *IEEE Transactions on Instrumentation and Measurement*, 45(2), 511-515. doi: 10.1109/19.492777.

Saito, W., Nitta, T., Kakiuchi, Y., Saito, Y., Tsuda, K., Omura, I. & Yamaguchi, M. (2007). Suppression of Dynamic On-Resistance Increase and Gate Charge Measurements in High-Voltage GaN-HEMTs With Optimized Field-Plate Structure. *IEEE Transactions on Electron Devices*, 54(8), 1825-1830. doi: 10.1109/TED.2007.901150.

Salcines, C., Kruglov, A. & Kallfass, I. (2018). A Novel Characterization Technique to Extract High Voltage - High Current IV Characteristics of Power MOSFETs from Dynamic Measurements. *2018 IEEE 6th Workshop on Wide Bandgap Power Devices and Applications (WiPDA)*, pp. 1-6. doi: 10.1109/WiPDA.2018.8569160.

Shi, Y., Xin, Z., Loh, P. C. & Blaabjerg, F. (2020). A Review of Traditional Helical to Recent Miniaturized Printed Circuit Board Rogowski Coils for Power-Electronic Applications. *IEEE Transactions on Power Electronics*, 35(11), 12207-12222. doi: 10.1109/TPEL.2020.2984055.

Shillaber, L., Jiang, Y., Ran, L. & Long, T. (2022). Ultrafast Current Shunt (UFCS): A Gigahertz Bandwidth Ultra-Low-Inductance Current Sensor. *IEEE Transactions on Power Electronics*, 37(12), 15493-15504. doi: 10.1109/TPEL.2022.3184638.

Shim, Y., Park, J., Kim, J., Song, E., Yoo, J., Pak, J. & Kim, J. (2009). Modeling and Analysis of Simultaneous Switching Noise Coupling for a CMOS Negative-Feedback Operational Amplifier in System-in-Package. *IEEE Transactions on Electromagnetic Compatibility*, 51(3), 763-773. doi: 10.1109/TEMC.2009.2026637.

Signorini, Siviero, Telescu & Stievano. (2016). Present and future of I/O-buffer behavioral macromodels. *IEEE Electromagnetic Compatibility Magazine*, 5(3), 79-85. doi: 10.1109/MEMC.0.7764256.

Simonaitis, J. W., Slayton, B., Yang-Keathley, Y., Keathley, P. D. & Berggren, K. K. (2021). Precise, Sub-Nanosecond, and High-Voltage Switching of Complex Loads Enabled by Gallium Nitride Electronics. *Review of Scientific Instruments*, 92(7). doi: 10.1063/5.0046706.

Tan, D. (2017). Power Electronics in 2025 and Beyond: A Focus on Power Electronics and Systems Technology. *IEEE Power Electronics Magazine*, 4(4), 33-36. doi: 10.1109/MPEL.2017.2760958.

Texas Instruments. (2018). LMG1205 80-V, 1.2-A to 5-A, Half Bridge GaN Driver with Integrated Bootstrap Diode. Retrieved on 2022-11-09 from: https://www.ti.com/lit/ds/symlink/lmg1205.pdf.

Tripathi, J. N., Sharma, V. K., Advani, H., Singh, P. N., Shrimali, H. & Malik, R. (2016). An analysis of power supply induced jitter for a voltage mode driver in high speed serial links. *2016 IEEE 20th Workshop on Signal and Power Integrity (SPI)*, pp. 1-4. doi: 10.1109/SaPIW.2016.7496259.

Vishay Intertechnology, Inc. (2009). Frequency Response of Thin Film Chip Resistors. Retrieved on 2022-10-24 from: https://www.vishay.com/docs/49427/vse-tn00.pdf.

Wang, K., Yang, X., Li, H., Wang, L. & Jain, P. (2018). A High-Bandwidth Integrated Current Measurement for Detecting Switching Current of Fast GaN Devices. *IEEE Transactions on Power Electronics*, 33(7), 6199-6210. doi: 10.1109/TPEL.2017.2749249.

Wen, C., Cai, Y. & Zhuo, C. (2021). Impact of Supply Noise on Nano-Meter VLSI Design: Hard or Soft Threshold? *2021 China Semiconductor Technology International Conference (CSTIC)*, pp. 1-4. doi: 10.1109/CSTIC52283.2021.9461455.

Xie, M. (2016). How to select input capacitors for a buck converter. *Analog Applications Journal*.

Yang, C., Pei, Y., Wang, L., Yu, L., Zhao, C., Zhu, M. & Liu, X. (2020). Analysis and Design of a Low-Cost Well-Performance and Easy-to-Design Current Sensing Circuit Suitable for SiC mosfets. *IEEE Transactions on Power Electronics*, 35(12), 13356-13366. doi: 10.1109/TPEL.2020.2993033.

Yang, Z., Huq, S., Arumugham, V. & Park, I. (2005). Enhancement of IBIS modeling capability in simutanous switching noise (SSN) and other power integrity related simulations - proposal, implementation, and validation. *2005 International Symposium on Electromagnetic Compatibility, 2005. EMC 2005.*, 2, 672-677. doi: 10.1109/ISEMC.2005.1513598.

Zhang, W., Zhang, Z., Wang, F., Brush, E. V. & Forcier, N. (2021). High-Bandwidth Low-Inductance Current Shunt for Wide-Bandgap Devices Dynamic Characterization. *IEEE Transactions on Power Electronics*, 36(4), 4522-4531. doi: 10.1109/TPEL.2020.3026262.

Zhao, B., Huang, C., Shringarpure, K., Bai, S., Makharashvili, T., Cao, Y. S., Achkir, B., Cracraft, M., Cocchini, M., Connor, S., Archambeault, B., Jiang, L., Ruehli, A., Fan, J. & Drewniak, J. (2016). Transient simulation for power integrity using physics based circuit modeling. *2016 Asia-Pacific International Symposium on Electromagnetic Compatibility (APEMC)*, 01, 1087-1089. doi: 10.1109/APEMC.2016.7522952.

Zhao, B., Bai, S., Connor, S., Cecchini, M., Becker, D., Cracraft, M., Ruehli, A., Archambeault, B. & Drewniak, J. (2018). System Level Power Integrity Analysis with Physics-Based Modeling Methodology. *2018 IEEE Symposium on Electromagnetic Compatibility, Signal Integrity and Power Integrity (EMC, SI & PI)*, pp. 379-384. doi: 10.1109/EMCSI.2018.8495206.

Zhao, B., Bai, S., Connor, S., Becker, W. D., Cocchini, M., Cho, J., Ruehli, A., Archambeault, B. & Drewniak, J. L. (2020). Physics-Based Circuit Modeling Methodology for System Power Integrity Analysis and Design. *IEEE Transactions on Electromagnetic Compatibility*, 62(4), 1266-1277. doi: 10.1109/TEMC.2019.2927742.

Zhou, W., Pei, X., Xiang, Y. & Kang, Y. (2020). A New EMI Modeling Method for Mixed-Mode Noise Analysis in Three-Phase Inverter System. *IEEE Access*, 8, 71535-71547. doi: 10.1109/ACCESS.2020.2983084.