High-Performance Flying-Capacitor Multilevel PFC Converters with Reduced Passive Energy Storage and Predictive Control

by

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Convertisseurs PFC multiniveaux à capacités flottantes haute performance avec stockage d'énergie passif réduit et commande prédictive

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RÉSUMÉ

Cette thèse étudie la conception, la commande et la mise en œuvre de systèmes de conversion CA-CC connectés au réseau, privilégiant une haute densité de puissance, une longue durée de vie et une compatibilité avec des contrôleurs numériques à coût réduit. Les travaux se concentrent sur les étages d'entrée monophasés à correction du facteur de puissance (PFC) pour les chargeurs embarqués de véhicules électriques, les redresseurs pour centres de données et télécommunications, et autres interfaces monophasées similaires, tout en étendant les principes de conception sous-jacents à un redresseur PFC triphasé isolé représentatif. Pour l'ensemble de ces applications, les principaux goulots d'étranglement limitant les gains en densité et en fiabilité sont les composants passifs magnétiques et capacitifs requis pour le tamponnage d'énergie, le filtrage des interférences électromagnétiques (IEM) et le découplage de sortie. L'objectif central est de réduire le volume des composants passifs tout en respectant des objectifs stricts de qualité de l'énergie, de rendement et de durée de vie, en utilisant des topologies multiniveaux à capacités flottantes (FCML) combinées à des schémas de commande prédictive (MPC) avancés et optimisés pour les microcontrôleurs.

La thèse développe d'abord un cadre de comparaison compact pour les étages d'entrée PFC monophasés, couvrant les étages totem-pole sans pont (bridgeless), les variantes totem-pole FCML avec différents nombres de niveaux et facteurs d'entrelacement, ainsi que les structures multiniveaux et hybrides associées. Sur la base de spécifications cohérentes de quelques kilowatts et d'un fonctionnement en conduction continue, des lois de dimensionnement analytiques sont introduites pour les inductances boost, les piles de capacités flottantes et les filtres IEM. Ces lois sont combinées à des contraintes de pertes équivalentes et à des métriques de volume simples dérivées de la densité d'énergie, produisant des tableaux structurels qui mettent en correspondance les choix de topologie et de commande avec le volume passif et les implications qualitatives en matière d'IEM. Ce cadre fournit une base systématique pour la sélection de candidats FCML monophasés prometteurs comme leviers de densité.

Côté matériel et commande, un prototype PFC FCML totem-pole monophasé à cinq niveaux de 2,5 kW est conçu et réalisé avec une partition en trois cartes (étage de puissance, carte de capteurs et d'interface, et contrôleur numérique). Une commande linéaire avec modulation de largeur d'impulsion (MLI) déphasée, des boucles de courant et de tension avec anticipation (feedforward), et un équilibrage actif des capacités flottantes sont réalisés sur une plateforme microcontrôleur C2000 et validés expérimentalement avec un rendement élevé, un facteur de puissance proche de l'unité et une ondulation de bus CC maîtrisée. S'appuyant sur cette plateforme, la thèse développe et valide expérimentalement des schémas de commande prédictive à ensemble de contrôle fini (FCS-MPC) pour un étage d'entrée de chargeur embarqué (OBC) FCML à quatre niveaux, prenant en charge un fonctionnement unifié en mode suiveur de réseau (grid-following)

et formateur de réseau (grid-forming) à travers plusieurs modes vehicle-to-everything, ainsi que pour un convertisseur PFC à capacités flottantes à quatre cellules avec tamponnage intégré des pulsations de puissance, incorporant le stockage d'énergie à deux fois la fréquence du réseau dans la pile de capacités flottantes. Une structure MPC lexicographique à deux étages, sans facteurs de pondération, est ensuite introduite pour éliminer le réglage de ces facteurs et garantir une exécution déterministe dans une période d'échantillonnage de 6,66 microsecondes sur un microcontrôleur double cœur, tout en obtenant une réduction substantielle de l'ondulation du bus CC et des économies de volume passif.

Enfin, un redresseur PFC triphasé isolé de type matriciel, avec compensation des pertes de rapport cyclique et support de puissance réactive, est analysé comme exemple d'étage d'entrée à haute densité éliminant le condensateur de bus CC intermédiaire et intégrant l'isolation et le PFC en un seul étage. Les résultats combinés démontrent que les topologies PFC FCML avec tamponnage intégré, soutenues par des implémentations MPC soigneusement structurées sur des microcontrôleurs commerciaux, offrent une voie pratique vers des interfaces CA-CC compactes, efficaces et fiables. La thèse recommande l'utilisation du cadre de comparaison et des architectures de commande proposés comme outils de conception pour les étages d'entrée monophasés et triphasés de nouvelle génération dans la recharge des véhicules électriques, les centres de données et les alimentations de télécommunications.

Mots-clés: correction du facteur de puissance, convertisseur multiniveaux à capacités flottantes, haute densité de puissance, commande prédictive, tampon de pulsation de puissance

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ABSTRACT

This thesis investigates the design, control, and implementation of grid-tied AC-DC conversion systems that prioritize high power density, long lifetime, and compatibility with cost-sensitive digital controllers. The work focuses on single-phase power factor correction (PFC) front ends for electric vehicle on-board chargers, data center and telecom rectifiers, and similar single-phase interfaces, and extends the underlying design principles to a representative three-phase isolated PFC rectifier. Across these applications, the main bottlenecks for further gains in density and reliability are the magnetic and capacitive passive components required for energy buffering, electromagnetic interference (EMI) filtering, and output decoupling. The central purpose is to reduce passive-component volume while meeting stringent power-quality, efficiency, and lifetime targets, using flying-capacitor multilevel (FCML) topologies combined with advanced, microcontroller optimized model predictive control (MPC) schemes.

The thesis first develops a compact comparison framework for single-phase PFC front ends that covers bridgeless totem-pole stages, FCML totem-pole variants with different level counts and interleaving factors, and related multilevel and hybrid structures. Under consistent few-kilowatt specifications and continuous-conduction operation, analytic sizing laws are introduced for boost inductors, flying-capacitor stacks, and EMI filters. These laws are combined with equal-loss constraints and simple volume metrics derived from energy density, yielding structural tables that map topology and control choices to passive volume and qualitative EMI implications. This framework provides a systematic basis for selecting promising single-phase FCML candidates as density levers.

On the hardware and control side, a 2.5 kW single-phase totem-pole five-level FCML PFC prototype is designed and implemented with a three-board partition (power stage, sensor and interface board, and digital controller). Linear control with phase-shifted PWM, current and voltage loops with feedforward, and active flying-capacitor balancing are realized on a C2000 microcontroller platform and validated experimentally with high efficiency, near-unity power factor, and controlled DC-link ripple. Building on this platform, the thesis develops and experimentally validates finite-control-set MPC schemes for a four-level FCML OBC front end that support unified grid-following and grid-forming operation across multiple vehicle-to-everything modes, and for a four-cell flying-capacitor PFC converter with integrated power pulsation buffering that embeds twice-line-frequency energy storage into the FC stack. A two-stage lexicographic, weight-free MPC structure is then introduced to eliminate weighting-factor tuning and guarantee deterministic execution within a 6.66 microsecond sampling period on a dual-core microcontroller, while achieving substantial DC-link ripple reduction and passive-volume savings.

Finally, a three-phase isolated matrix-type PFC rectifier with duty-cycle loss compensation and reactive power support is analyzed as an example of a high-density front end that removes the intermediate DC-link capacitor and integrates isolation and PFC in a single stage. The combined results demonstrate that FCML PFC topologies with integrated buffering, supported by carefully structured MPC implementations on commercial microcontrollers, offer a practical path to compact, efficient, and reliable AC-DC interfaces. The thesis recommends the use of the proposed comparison framework and control architectures as design tools for next-generation single-phase and three-phase front ends in EV charging, data centers, and telecom power supplies.

Keywords: power factor correction, flying-capacitor multilevel converter, high power density, model predective control, power pulsation buffer

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LIST OF ABBREVIATIONS

AC	Alternating current
ADC	Analog-to-digital converter
APPB	Active power pulsation buffer
CLA	Control Law Accelerator
CM	Common-mode
CPU	Central processing unit
DC	Direct current
DM	Differential-mode
DSP	Digital signal processor
EMI	Electromagnetic interference
EV	Electric vehicle
FC	Flying capacitor
FCML	Flying-capacitor multilevel
FCS	Finite control set
FRA	Frequency-response analysis
G2V	Grid-to-vehicle
GaN	Gallium nitride
GSE	Generalized Steinmetz equation
HF	High-frequency

LF	Line-frequency
MCU	Microcontroller
MOMPCC	Multi-objective model-predictive current control
MOSFET	Metal-oxide-semiconductor field-effect transistor
MPC	Model predictive control
OBC	On-board charger
OSG	Orthogonal-signal generator
PFC	Power factor correction
PI	Proportional-integral
PLL	Phase-locked loop
PPB	Power pulsation buffer
PSPWM	Phase-shifted pulsewidth modulation
PV	Photovoltaic
PWM	Pulsewidth modulation
RCP	Rapid control prototyping
RMS	Root-mean-square
SiC	Silicon carbide
SSV	Switching space-vector
SVM	Space vector modulation
THD	Total harmonic distortion

TMR	Tunnel magnetoresistance
TP	Totem-pole
V2G	Vehicle-to-grid
V2H	Vehicle-to-home
V2L	Vehicle-to-load
V2V	Vehicle-to-vehicle
V2X	Vehicle-to-everything
VDC	DC-link voltage
ZOH	Zero-order hold

INTRODUCTION

In an era dominated by artificial intelligence's explosive growth, where AI data centers alone are projected to consume up to 3% of global electricity by 2030 (International Energy Agency (IEA), 2025), power electronics emerges as the unsung hero enabling efficient energy conversion and management. Electric power systems are undergoing a rapid transformation driven by three tightly coupled trends: decarbonization of generation, electrification of transportation, and the digitalization of society. In this environment, power electronic converters provide the indispensable interface between the alternating current (AC) grid and a wide variety of direct current (DC) loads and sources, including electric vehicle (EV) batteries, information technology equipment in data centers, telecom base stations, and residential photovoltaic (PV) systems.

Across these applications, single-phase and three-phase front-end rectifiers are required to perform power factor correction (PFC), shape grid currents in accordance with increasingly stringent harmonic standards, and deliver tightly regulated DC power while satisfying demanding efficiency and power density targets. At the same time, these converters must exhibit long lifetimes, high reliability, and predictable failure modes compatible with automotive and infrastructure qualification requirements. As a consequence, modern front-end rectifiers are no longer limited merely by semiconductor ratings. Instead, their size, cost, and reliability are dominated by the magnetic and capacitive passive components that implement energy buffering, electromagnetic interference (EMI) filtering, and output decoupling.

Figure 0.1 illustrates the role of grid-tied AC-DC interfaces in three representative domains: EV chargers, front-end rectifiers for data centers and telecom power supplies, and residential PV inverters. In EV charging, the single-phase PFC stage in the on-board charger determines the achievable charging power from residential circuits and forms the bottleneck for vehicle-to-everything (V2X) operation. In data centers and telecom systems, front-end rectifiers feeding intermediate DC buses must deliver multi-kilowatt power levels with very high efficiency and

compact form factors. In residential PV and energy storage systems, single- and three-phase inverters must export power to the grid while meeting grid-code requirements on power quality and reactive power support.

The cumulative number of such converters is rapidly increasing. For example, level-2 single-phase EV chargers in the 3.3 kW to 7.2 kW range already dominate public charging infrastructure, and each vehicle is equipped with on-board charger. Similarly, large data centers deploy tens of megawatts of AC-DC conversion capacity, and telecom networks rely on vast fleets of rectifier modules. In all of these cases, even modest improvements in efficiency, volumetric power density, and passive component utilization scale to significant reductions in energy consumption, material usage, and total cost of ownership over the system life cycle.

These trends motivate a unified investigation of circuit topologies, passive-component sizing, and digital control strategies that jointly target high efficiency, high power density, and long lifetime for grid-tied AC-DC conversion systems. The present thesis pursues this goal with an emphasis on reduced passive volume in single-phase PFC front ends and extension to selected three-phase architectures.

Single-phase and three-phase PFC front ends

Functional requirements

A generic grid-tied AC-DC conversion system comprises one or more stages that perform the following functions:

- shaping of input currents to achieve near-unity power factor and low total harmonic distortion (THD),
- conversion between AC grid voltage and regulated DC output voltage or current,
- energy buffering of the twice-line-frequency power pulsation inherent in single-phase systems,

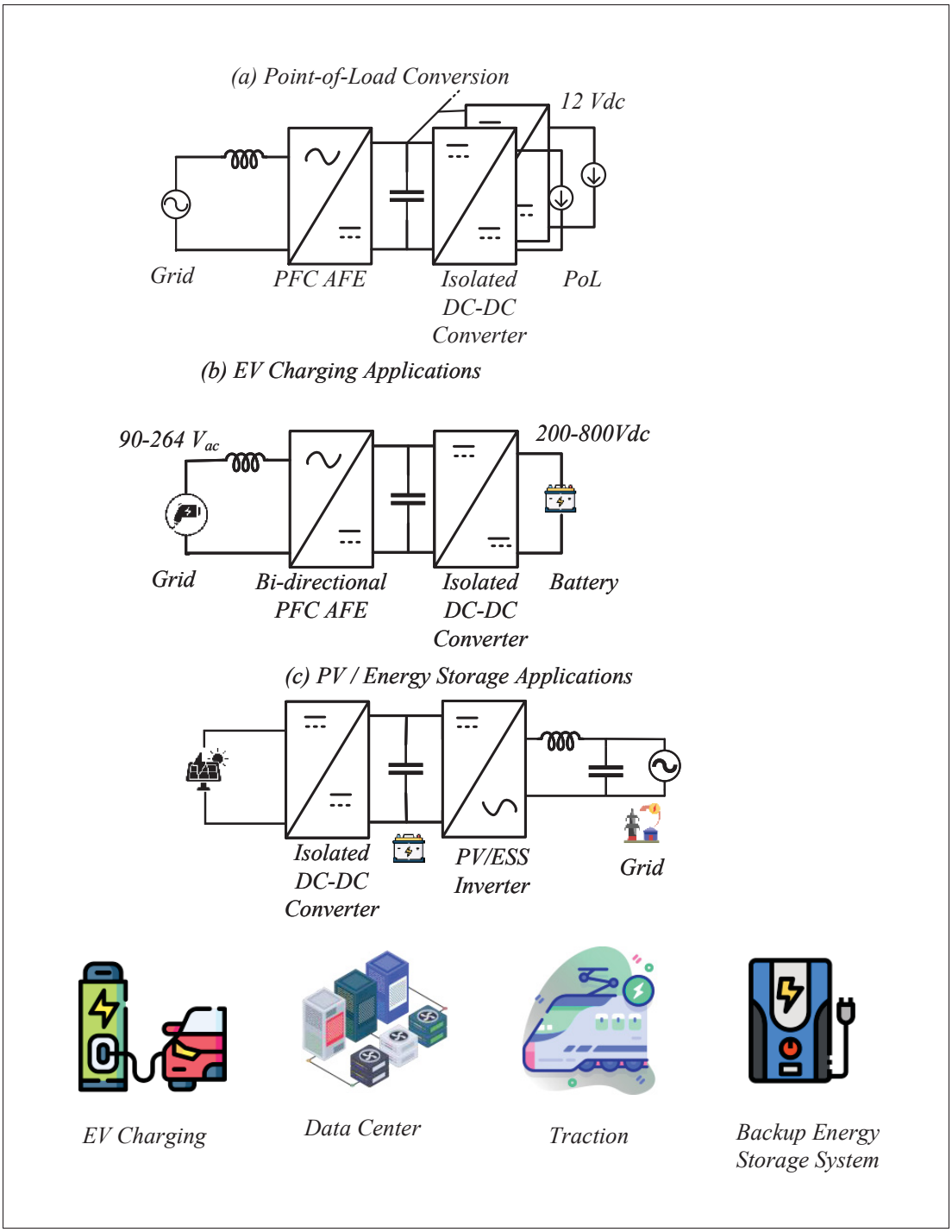


Figure 0.1 Representative single-phase grid-tied conversion stages and end-use domains

- attenuation of conducted EMI to comply with regulatory limits,

- galvanic isolation, when required, to satisfy safety standards and system-level architecture constraints.

In single-phase front ends, the instantaneous input power contains a twice-line-frequency component. Conventional designs use a large electrolytic capacitor bank to absorb this power pulsation. While this approach is simple, the resulting capacitor volume and the limited lifetime of electrolytic capacitors under thermal stress are major obstacles to high power density and long-term reliability (Brooks, Giardine & Pilawa-Podgurski, 2024; Imperiali, Menzi, Kolar & Huber, 2024).

Three-phase front ends do not exhibit a net twice-line-frequency power pulsation in balanced operation, so the role of bulk DC-link capacitance is mainly to decouple load dynamics and provide ride-through capability rather than to cancel a large structured ripple. Nonetheless, high-power three-phase rectifiers still require substantial passive components to meet EMI limits, shape currents, and integrate galvanic isolation (Kolar & Friedli, 2013). In both single-phase and three-phase systems, passive components therefore remain critical design levers for volumetric and gravimetric power density.

Representative PFC topologies

Table 0.1 summarizes representative single-phase PFC front ends, while Table 0.2 extends the comparison to three-phase rectifiers. The comparison is qualitative and emphasizes the implications for passive component volume, control complexity, and suitability for very high power density.

The topologies considered in this thesis fall predominantly into two families. First, single-phase FCML totem-pole structures combined with integrated power pulsation buffering (PPB) are employed to reduce both the boost inductance and the effective DC-link capacitance, while maintaining high efficiency and compliant grid currents. Second, a three-phase isolated matrix-

Table 0.1 Representative single-phase PFC front-end topologies and qualitative comparison

Topology	**Grid interface**	**Advantages for density and lifetime**	**Main challenges**
Single-phase boost PFC with electrolytic DC-link	Single-phase, 2-level, non-isolated	Simple structure and mature design methods; low control complexity; well-established in EV chargers and adapters.	Large electrolytic DC-link capacitor dominates volume and limits lifetime; relatively large boost inductor and EMI filter; constrained switching frequency.
Interleaved single-phase boost PFC	Single-phase, 2-level, non-isolated	Reduced inductor value and ripple via interleaving; improved thermal distribution; lower RMS capacitor current.	Increased switch count and gate driving; EMI filter still sizable; lifetime still limited by electrolytic DC-link.
Single-phase totem-pole PFC	Single-phase, 2-level, non-isolated	Elimination of diode bridge; reduced conduction losses; good fit for SiC and GaN; improved efficiency at high line.	High-frequency switching of bridge legs with hard commutation; EMI and layout more critical; still reliant on large DC-link capacitor unless combined with active buffer or PPB.
Single-phase flying-capacitor multilevel (FCML) totem-pole PFC	Single-phase, 4- to 7-level, non-isolated	Reduced semiconductor voltage stress, higher effective switching frequency at grid interface, and lower boost inductance; flying capacitors enable use of low-voltage, high-FOM devices; suitable for active buffering and integration with power pulsation buffer (PPB).	Increased switch and capacitor count; complex modulation; flying-capacitor voltage balancing; EMI profile more complex; digital control must manage multilevel switching states.
Single-phase two-stage AC-DC with active buffer (e.g., series-stacked buffer)	Single-phase, 2-level PFC plus active buffer	Enables large reduction in bulk electrolytic capacitance by relocating twice-line power buffering to an active stage; supports film or ceramic capacitors and improved lifetime.	Additional active components and control loop; potential efficiency penalty if not co-optimized; buffer dynamics interact with PFC controller.

type PFC rectifier is examined as an example of a front-end architecture that eliminates the intermediate DC-link capacitor and integrates isolation and PFC in a single stage. In both cases,

Table 0.2 Representative three-phase PFC front-end topologies and qualitative comparison

Topology	**Grid interface**	**Advantages for density and lifetime**	**Main challenges**
Three-phase two-level PWM rectifier	Three-phase, 2-level, isolated or non-isolated	High power quality with sinusoidal currents; well understood modulation; suitable for multi-kilowatt front ends in data centers and renewable energy systems.	DC-link capacitor and grid-side filter inductors dominate volume; switching losses increase with higher frequencies; EMI filter design remains non-trivial.
Vienna rectifier and related three-level topologies	Three-phase, 3-level, typically isolated	Reduced voltage stress on semiconductors and lower current ripple; improved efficiency and power density relative to 2-level solutions.	More complex modulation and neutral-point or capacitor balancing; still requires sizable DC-link capacitance.
Three-phase isolated matrix-type PFC rectifier	Three-phase, isolated, single-stage	Direct AC-to-high-frequency-AC conversion avoids a bulky intermediate DC-link; simultaneous PFC and isolation; promising for compact front ends.	Modulation tightly coupled to transformer leakage inductance; duty-cycle loss and current distortion require careful compensation; EMI and control are more demanding.

appropriate modulation and digital control are essential to realize the theoretical benefits of the topology without incurring excessive switching losses or control complexity.

Passive components and power density as design levers

Passive-component bottlenecks

For many grid-tied AC-DC converters, passive components occupy the largest physical volume and contribute significantly to mass and cost. In single-phase PFC front ends, the main contributors are:

- the boost inductor and grid-side filter inductance, which must store sufficient energy and provide adequate ripple attenuation,

- the DC-link capacitor bank, which must buffer twice-line-frequency power and support load transients,
- the EMI filter, which must attenuate both differential-mode (DM) and common-mode (CM) conducted emissions to comply with regulatory limits.

Design methods that treat semiconductor devices and passive components independently often fail to exploit the full system-level design space. For example, increasing switching frequency to reduce inductor size may require new device technologies and packaging to control losses and EMI. Conversely, reducing DC-link capacitance without providing an alternative path for twice-line-frequency energy leads to excessive voltage ripple or compromises in power quality.

In recent years, several approaches have been proposed to address these bottlenecks:

- multilevel and hybrid switched-capacitor converters that increase effective switching frequency and reduce passive requirements, while leveraging low-voltage high-figure-of-merit devices (Lei, Liu & Pilawa-Podgurski, 2018),
- active power pulsation buffer (PPB) circuits that shift twice-line-frequency energy to dedicated active stages and enable the use of smaller, more reliable film or ceramic capacitors (Wang, Wang, Zhu & Blaabjerg, 2020a),
- co-optimization frameworks that trade off conduction and switching losses against passive volume to identify Pareto-optimal designs (Imperiali *et al.*, 2024).

To highlight both component-level and system-level design tradeoffs, Fig. 0.2 compares a representative state-of-the-art converter with a future high-density concept using normalized multi-criteria spider charts for primary converter attributes and general system performance.

Life-cycle and reliability considerations

Beyond instantaneous power density, life-cycle performance and reliability are central design objectives (Falck, Felgemacher, Rojko, Liserre & Zacharias, 2018). In EV chargers, for example,

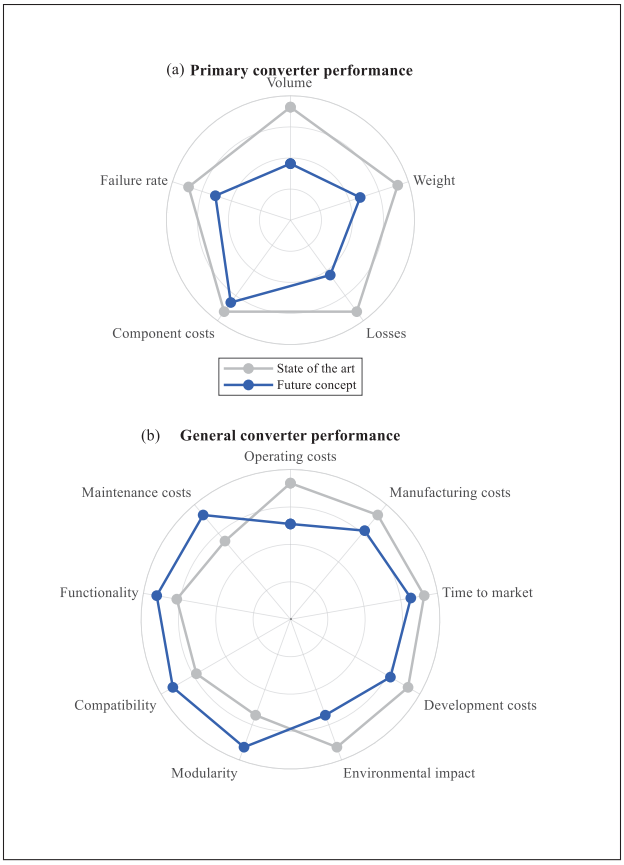


Figure 0.2 Qualitative multi-criteria comparison of a representative state-of-the-art converter and a future high-density concept

automotive qualification standards impose lifetime requirements on the order of ten to fifteen years, under wide ambient temperature ranges and repeated thermal cycling. Electrolytic capacitors are often the limiting components in such systems, with lifetime strongly dependent on ripple current and temperature. Similar considerations apply to telecom and data center rectifiers, where maintenance costs and down-time are critical.

Reducing dependence on electrolytic capacitors, increasing the utilization of film and ceramic capacitors, and operating inductors and transformers at higher flux densities within acceptable loss limits are therefore attractive strategies. However, these approaches must be grounded in rigorous analysis of energy storage requirements, capacitor voltage and current stress, and

thermal behavior. Design-oriented figures of merit that link required energy buffering to capacitor technology, volume, and loss are particularly valuable in this context.

In this thesis, reduced passive volume and improved life-cycle behavior are pursued primarily through:

- embedding power pulsation buffering into multilevel single-phase PFC stages by exploiting the flying-capacitor stack as an integrated PPB,
- reducing the required bulk DC-link capacitance while maintaining acceptable DC-bus ripple and grid-current quality,
- co-designing modulation and control algorithms that minimize RMS currents in critical passive components and manage their thermal stress.

Digital control and model predictive control for multilevel PFC

Control challenges in high-density multilevel PFC

Multilevel converters and active PPB architectures introduce new degrees of freedom in modulation and control. In single-phase FCML PFC front ends, the controller must:

- regulate grid current to follow sinusoidal references with near-unity power factor,
- control the DC-link voltage or power flow to the downstream DC-DC stage or battery,
- maintain balanced flying-capacitor voltages under bidirectional power flow and varying operating modes,
- manage the exchange of twice-line-frequency energy between the DC link and the integrated PPB,
- ensure that switching patterns satisfy device constraints and limit switching losses and EMI.

Classical linear control strategies based on nested voltage and current loops with pulsewidth modulation (PWM) can be extended to multilevel converters, but they often struggle to handle the

discrete nature of the switching states and the multi-objective nature of the regulation problem (Ye, Lei, Liao & Pilawa-Podgurski, 2022; Papamanolis, Neumayr & Kolar, 2017). In particular, regulating grid current and PPB energy steering are difficult to address within purely linear frameworks.

Model predictive control (MPC), and in particular finite-control-set MPC (FCS-MPC), naturally accommodates multilevel converters and multiple objectives. At each sampling instant, the controller evaluates a finite set of candidate switching states using a discrete-time model of the plant, predicts the resulting evolution of currents and capacitor voltages over one or more steps, and selects the state that minimizes a cost function encoding tracking objectives and constraints. This paradigm offers several advantages:

- direct handling of discrete switching states and multilevel voltage vectors,
- explicit inclusion of device constraints and multi-objective criteria in the cost function,
- provides best dynamic performance under critical operating conditions such as load disturbances, startup and shutdown.

However, conventional FCS-MPC formulations also introduce challenges:

- the computational burden scales with the number of candidate switching states and prediction horizon,
- multi-term cost functions require non-trivial tuning of weighting factors, which may vary with operating conditions,
- real-time implementation on cost-sensitive commercial microcontrollers must meet tight execution-time and memory constraints, leaving limited headroom for long prediction horizons or complex optimization routines.

Many reported implementations of MPC for multilevel PFC converters rely on high-performance digital signal processors (DSPs), field-programmable gate arrays (FPGAs), or rapid control prototype (DSpace). Demonstrating high-performance MPC on automotive-grade, cost-

constrained microcontrollers with deterministic execution and modest sampling periods remains a significant practical challenge.

MPC on commercial microcontrollers

A central theme of this thesis is the realization of advanced MPC schemes for multilevel single-phase PFC with integrated PPB on a commercially and widely used C2000 microcontroller platform. The converter prototypes considered here operate with switching frequencies on the order of 65 kHz to 100 kHz and sampling periods of approximately 6.7 microseconds, which leaves only a few microseconds per sampling interval for:

- acquisition and scaling of measurements,
- reference generation and outer-loop computations,
- prediction of candidate switching states and cost evaluations,
- selection and application of the optimal switching state.

To meet these constraints, the predictive control strategies developed in this work:

- explicitly exploit the structure of the multilevel converter and its switching table to reduce the number of candidate states that must be evaluated per sampling instance,
- use physically motivated cost functions that avoid extensive tuning of weighting factors,
- adopt lexicographic evaluation strategies that separate primary objectives (such as current tracking) from secondary objectives (such as flying-capacitor energy steering and switching effort minimization), thereby reducing sensitivity to weight selection,
- partition execution across multiple processing cores and real-time accelerators and co-processor on the microcontroller where appropriate, while maintaining deterministic timing.

By demonstrating such controllers in real time on a fully instrumented 2.5 kW TP-5L-FCML PFC prototype and a four-cell FC PFC with embedded PPB, the thesis aims to bridge the gap between

theoretical MPC formulations and practical implementation in high-density, cost-sensitive front-end rectifiers.

Scope and objectives of the thesis

The overall scope of this thesis is the design, control, and implementation of reduced passive-volume grid-tied AC-DC conversion systems in the few-kilowatt power range. The focus lies on:

- single-phase PFC front ends for EV on-board chargers and similar single-phase AC-DC interfaces, with emphasis on flying-capacitor multilevel (FCML) totem-pole topologies and integrated PPB,
- a representative three-phase isolated matrix-type PFC rectifier that eliminates the intermediate DC-link capacitor and integrates isolation and PFC in a single stage.

Within this scope, the thesis pursues the following specific objectives:

1. Develop and experimentally validate a high-density hardware platform for a single-phase totem-pole five-level FCML PFC converter, including power stage, sensor and control interface board, and digital control implementation on a C2000 microcontroller.
2. Formulate and demonstrate a unified MPC framework for a bidirectional single-phase four-level FCML PFC stage in an on-board charger front end, capable of grid-following and grid-forming operation across multiple V2X modes.
3. Design and implement MPC schemes for an integrated PPB four-cell flying-capacitor PFC converter that reduce the required bulk DC-link capacitance while maintaining DC-link voltage ripple and grid-current quality within acceptable bounds.
4. Introduce and validate a lexicographic, weight-free MPC formulation that eliminates the need for extensive weighting-factor tuning, reduces per-sample computational workload, and preserves deterministic execution on a commercial microcontroller.

5. Analyze and demonstrate a three-phase isolated matrix-type PFC rectifier with duty-cycle loss compensation and reactive power support as an example of a high-power-density front end that removes the need for a bulky intermediate DC-link capacitor.
6. Provide, in a later chapter, a structured comparison of candidate front-end topologies and control strategies in terms of passive volume, efficiency, and lifetime implications, using compact analytic relations for passive sizing and EMI filter volume as practical density levers.

Summary of contributions

The main contributions of the thesis are summarized below:

High-density single-phase FCML PFC hardware platform

A 2.5 kW single-phase totem-pole five-level FCML PFC prototype is developed and characterized. The prototype:

- interfaces a 90 V rms to 265 V rms grid to a regulated 380 V to 420 V DC bus with target efficiency above 98 percent,
- employs a three-board partition (power stage, control interface board, and digital controller) that reflects functional separation and supports rapid control development,
- demonstrates high power factor, low input current THD, and controlled DC-link ripple across a wide operating range.

The platform provides the experimental backbone for the control developments in subsequent chapters.

Unified MPC for bidirectional four-level FCML OBC front end

A bidirectional single-phase four-level FCML front end for an EV on-board charger is modeled and controlled using a unified finite-control-set MPC framework. The contributions include:

- characterization of the admissible V2X operating region in the active-reactive power plane, subject to converter and battery constraints,
- derivation of continuous-time and discrete-time models suitable for predictive control in both rectifier and inverter modes,
- development of mode-dependent reference generation for grid-following and grid-forming operation, integrated with the MPC scheme.

Integrated PPB control for four-cell FC PFC

A single-phase four-cell flying-capacitor PFC converter with integrated PPB is analyzed and controlled using MPC. Key contributions are:

- embedding twice-line-frequency power buffering into the flying-capacitor stack, thereby reducing the required bulk DC-link capacitance,
- discrete-time modeling of the integrated PPB dynamics and formulation of cost functions that simultaneously address current tracking, DC-link ripple, and flying-capacitor voltage regulation,
- experimental demonstration of DC-link ripple reduction and passive-volume savings on a 2.5 kW prototype, together with an assessment of loss and stress distribution among components.

Lexicographic, weight-free MPC for integrated PPB

To address the sensitivity of multi-term cost functions to weighting factors and to reduce computational burden, a lexicographic multi-objective MPC structure is introduced for the integrated PPB four-cell FC PFC. The proposed controller:

- enforces inductor current tracking as the primary objective and flying-capacitor energy steering and switching effort control as secondary objectives within a lexicographic evaluation,
- eliminates the need for manual tuning of weighting factors while preserving buffering performance,
- incorporates tie-breaking strategies based on Hamming distance to limit unnecessary switching transitions,
- is implemented and experimentally validated on the existing 2.5 kW prototype, demonstrating deterministic real-time execution and improved power density potential.

Three-phase isolated matrix-type PFC rectifier with duty-cycle loss compensation

Finally, a three-phase isolated matrix-type PFC rectifier is analyzed as an example of a high-power-density front end that removes the intermediate DC-link capacitor. The work:

- reviews the operation of the three-phase to high-frequency single-phase matrix converter stage with subsequent rectification and output filtering,
- derives duty-cycle loss expressions associated with transformer leakage inductance and formulates compensation strategies,
- introduces modulation schemes that provide limited reactive power support while maintaining sinusoidal input currents and high power quality.

This three-phase study complements the single-phase FCML and PPB work by illustrating how similar design principles extend to different front-end architectures.

Thesis organization

The remainder of the thesis is organized as follows.

- **Chapter 1** will synthesize the single-phase AC-DC comparison framework. It will employ simple analytic relations for inductor and capacitor sizing, and EMI filter volume to compare

candidate topologies and control schemes in terms of passive volume. This chapter will position the proposed FCML solutions against conventional front ends and multilevel alternatives as density levers for future grid-tied AC-DC conversion systems.

- **Chapter 2** details the hardware development and real-time control implementation of the 2.5 kW totem-pole five-level FCML PFC prototype. The chapter covers system specifications, power-stage design, sensor and control interface board, and digital control implementation based on linear control with phase-shifted PWM, including dead-time compensation and active flying-capacitor balancing.
- **Chapter 3** presents the unified MPC framework for a single-phase four-level FCML front end in a bidirectional EV on-board charger. It introduces the V2X operating modes and limits, develops continuous-time and discrete-time models, describes reference generation for grid-connected and standalone operation, and demonstrates the performance of finite-control-set MPC in both rectifier and inverter modes.
- **Chapter 4** introduces MPC for a single-phase four-cell flying-capacitor PFC converter with integrated PPB. The chapter describes the topology and operating principle, derives control-oriented models, proposes cost functions and weighting-factor selection strategies, and provides simulation and experimental validation that highlight DC-link ripple reduction and passive-volume savings.
- **Chapter 5** extends the integrated PPB control concept by introducing a two-stage lexicographic, weight-free MPC scheme. It formulates the lexicographic multi-objective structure, discusses FC voltage-reference generation, analyzes waveforms, energy routing, and device stresses, and presents hardware results illustrating the viability of the approach on a commercial microcontroller with deterministic execution.
- **Chapter 6** analyzes a three-phase isolated matrix-type PFC rectifier with duty-cycle loss compensation and reactive power support. The chapter reviews converter operation, derives output voltage and duty-cycle loss expressions for adjustable power factor, introduces

modulation strategies, and corroborates the analysis with simulations. Within the broader context of the thesis, it serves as an example of a three-phase front-end architecture that eliminates the intermediate DC-link capacitor and contributes to high power density and reliability.

- **The concluding chapter** summarizes the main findings, discusses the implications for the design of high-density single-phase and three-phase front ends, and outlines directions for future research in topology development, passive-component optimization, and microcontroller-friendly predictive control.

Through this structure, the thesis aims to provide a coherent path from system-level motivation and passive-component bottlenecks, through hardware platform development and control design, to experimentally validated high-density AC-DC conversion solutions that reconcile power density, power quality, and life-cycle performance.

CHAPTER 1

SINGLE-PHASE AC-DC TOPOLOGIES & DESIGN LEVERS FOR POWER DENSITY

1.1 Introduction

Passive components in single-phase PFC stages dominate converter volume and mass because they must be sized to meet power-quality targets, load dynamics, and electromagnetic-interference (EMI) requirements. As a result, front-end rectifiers for electric-vehicle chargers, data centers, telecom, and similar power-supply applications are increasingly constrained by power-density and initial cost targets. A wide set of candidate topologies is used in practice, including bridgeless totem-pole stages (Infineon Technologies AG, 2025), flying-capacitor multilevel (FCML) stages (Ishraq & Mallik, 2024a), and various hybrid ANPC (Power Electronic Systems Laboratory (PES), ETH Zurich *et al.*, 2019) or interleaved structures. Their relative benefits as "density levers" depend strongly on the operating conditions and on how inductors, capacitors, and EMI filters are sized. Direct comparison is difficult when each application adopts different specifications and design rules.

Most existing work focuses on a single topology or a narrow family of variants under fixed assumptions. High-density two-level totem-pole PFC prototypes and FCML-based PFC front ends have been optimized for efficiency and footprint in isolation, often with topology-specific design rules, proprietary component libraries, or numerical optimization loops. Detailed small-signal models and time-domain simulations are available for individual candidates (Giardine, Krishnan, Nerenberg & Pilawa-Podgurski, 2025; Ishraq & Mallik, 2024b; Tausif & Dusmez, 2023; Lei *et al.*, 2018), and several high-power-density demonstrators have been reported (Qin, Lei, Ye, Chou & Pilawa-Podgurski, 2019; Barth *et al.*, 2020; Neumayr, Bortis & Kolar, 2020a), but there is no compact framework that compares the main structural options under common specifications while tracking both passive volume and EMI implications for single-phase PFC. In particular, the impact of level count, interleaving, and unfolder structure on required boost inductance, flying-capacitor values, and differential-mode (DM) and common-mode (CM) filter sizing is usually treated case by case rather than within a unified, topology-agnostic set of

estimators. Recent multilevel converter research has also introduced a large number of “compact” topologies (Harbi *et al.*, 2023) that claim reduced semiconductor count for a given number of discrete voltage levels, but these comparisons are typically made at the level of switch count and output levels, not at the level of passive size or the power processed by the inductors and capacitors. The effective switching or commutation frequency seen by the boost inductor, flying capacitors, and EMI filters is often different between such candidates and strongly influences required inductance, capacitance, and filter volume. As a result, the true density benefit of many proposed multilevel topologies remains unclear when evaluated on a common, passive-volume and EMI-aware basis.

This chapter therefore limits its scope to high-power single-phase PFC converters designed for standard distribution-level inputs. First, it standardizes the operating conditions, constraints, and notation for a family of single-phase boost-type PFC front ends so that conventional two-level totem-pole stages, FCML variants, and interleaved implementations can be compared on a consistent basis. Second, it derives compact, first-order relations that map a chosen topology and parameter set to boost inductance, flying-capacitor values, and simple proxies for EMI severity, semiconductor stress, and passive volume. These expressions are intentionally approximate, but they are sufficient to rank candidates, to identify promising “density levers” such as level count and interleaving factor, and to generate reasonable first-pass designs. Third, it defines comparison frameworks and a set of representative design points that are carried forward into detailed simulation and hardware evaluation in later chapters, without claiming exhaustive optimization of every degree of freedom.

The reference operating range is a nominal power of 3.3 kW, input voltage $V_{G,\mathrm{rms}}$ from 90 V to 265 V, and a regulated dc link $V_{dc} = 400$ V. Operation is targeted at unity power factor, with input-current total harmonic distortion below approximately 3 %. Conducted-EMI behavior is evaluated against CISPR Class A and Class B limits and practical ground-leakage constraints typical for single-phase rectifiers. For all candidate designs, the dc-link voltage ripple ΔV_{dc} is limited to about 4 % to 5 %, and the boost-inductor ripple current Δi_L is targeted in the range of 10 % to 20 % of the peak inductor current I_{pk} at nominal operating conditions. For each design

point, the chapter focuses on structural quantities that can be evaluated with compact models: required boost inductance, flying-capacitor requirements where applicable, simple energy-based volume estimates for L and FC stacks, and semiconductor loss under a common switching-technology assumption. These indicators are sufficient to identify promising combinations of level count and interleaving as "density levers" and to screen out clearly unfavorable options. A complete EMI-aware passive-volume evaluation, including detailed DM and CM filter sizing, is defined conceptually but left for future work.

The parameter n_c denotes the number of flying-capacitor cells per high-frequency (HF) leg, so each HF leg has $m = n_c + 1$ discrete voltage levels. The interleaving factor M counts the number of parallel HF legs. The device switching frequency is denoted by f_{sw}, and the effective ripple frequency seen by the boost inductor is denoted by f_{eff}. The overall output level count is written as N (line-to-line or line-to-neutral, as stated when used). Unless explicitly noted otherwise, the analysis assumes phase-shifted PWM (PS-PWM), well-balanced flying-capacitor voltages, and continuous-conduction-mode operation.

Within this scope, the subsequent sections (i) classify the low-frequency unfolder mechanisms and HF cell structures that define the candidate topologies, (ii) derive compact analytical models for ripple, passive sizing, and simple EMI proxies, (iii) introduce fairness frameworks for comparison under common specifications and loss budgets, and (iv) define a small set of representative design points that act as anchors for detailed simulation and prototype evaluation in later chapters.

1.2 Unfolder Mechanisms

In the single-phase AC–DC converters considered here, which synthesize the AC terminal voltage with a high-frequency (HF) power stage, an *unfolder* connects the rectified or synthesized voltage to the grid with the correct polarity over the line cycle. The unfolder leg is operated at the line frequency (50 Hz / 60 Hz) in order to (i) avoid adding appreciable switching loss or thermal burden to this path and (ii) preserve HF switching activity and control complexity

for the main synthesis leg. A second motivation is electromagnetic compatibility: the unfolder choice and its voltage trajectory determine the common-mode (CM) profile (Neumayr *et al.*, 2020a; Neumayr, Bortis & Kolar, 2020b).

1.2.1 Types of Unfolder Mechanisms

1.2.1.1 LF Totem-Pole (Half-Bridge) Unfolder

A half-bridge unfolder (Fig. 1.1) connects one AC terminal to a DC-link rail with line-frequency commutation; the other terminal is driven by the HF synthesis leg (AG, 2025). This minimizes unfolder switching loss but generates a low-frequency CM voltage that exhibits relatively steep transitions near grid zero crossings. As a result, the required CM choke size increases for a given EMI mask.

Merits

Simple device count and low unfolder switching loss; slightly lower conduction loss than an H-bridge unfolder because only one leg conducts in the unfolder path at line frequency.

Drawbacks

LF CM voltage with steep transitions around zero crossings; larger CM choke; more challenging current-control behavior around zero crossings.

1.2.1.2 LF H-Bridge Unfolder

An H-bridge unfolder (Fig. 1.2) commutates both AC terminals symmetrically at 50 Hz / 60 Hz while the HF synthesis remains on a single leg (Lei *et al.*, 2017). To prevent distortion at zero crossings, the bridge can be temporarily driven with HF PWM while the buck output is clamped above a small minimum voltage (for example, $v_{C0,\min} \approx 25$–50 V); since only a small voltage is switched for a brief interval, unfolder switching losses are negligible (Neumayr *et al.*,

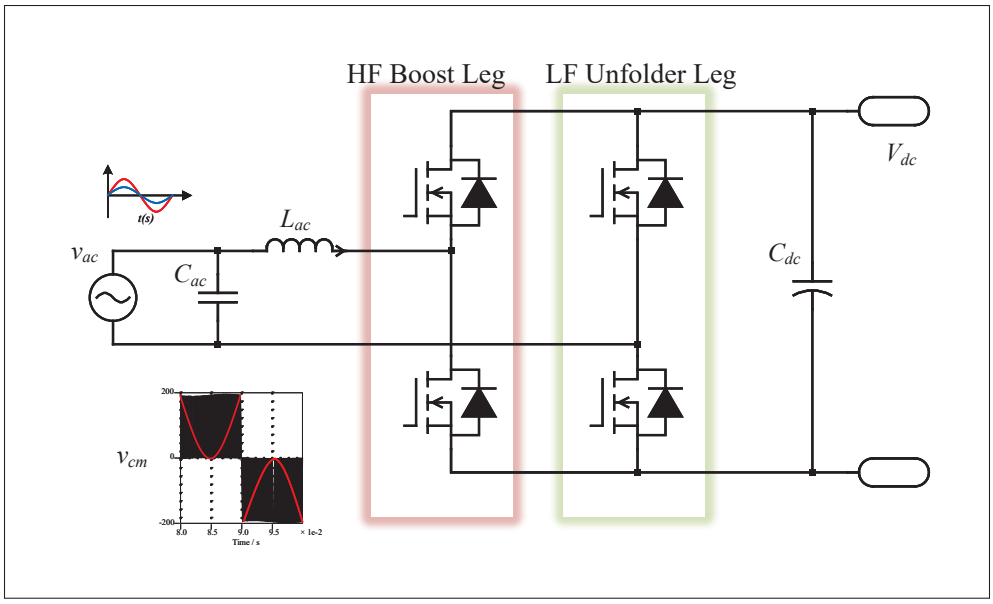


Figure 1.1 Half-bridge (totem-pole) unfolder: LF CM trajectory exhibits high dv/dt around zero crossings

2020a). Compared to the half-bridge unfolder, the LF CM trajectory is smoother (no HF dv/dt components in the CM voltage), and a DC-link-referenced output filter can be applied, which confines a large fraction of CM current inside the converter and reduces CM choke size.

For the boost-stage plus H-bridge unfolder concept, the LF common-mode voltage at the output is

$$v_{\mathrm{cm}}(t) = \frac{\hat{V}_{\mathrm{ac}}}{2} \sin(\omega t), \tag{1.1}$$

which directly sets the LF CM stress on the Y-capacitors and filter.

Merits

Enables DC-link-referenced output capacitors that confine CM current; typically smaller CM choke than the half-bridge unfolder for the same EMI mask; good conducted-EMI behavior.

Drawbacks

Two LF devices in the current path raise conduction loss slightly relative to the half-bridge unfolder; increased device count and gate-drive channels at line frequency.

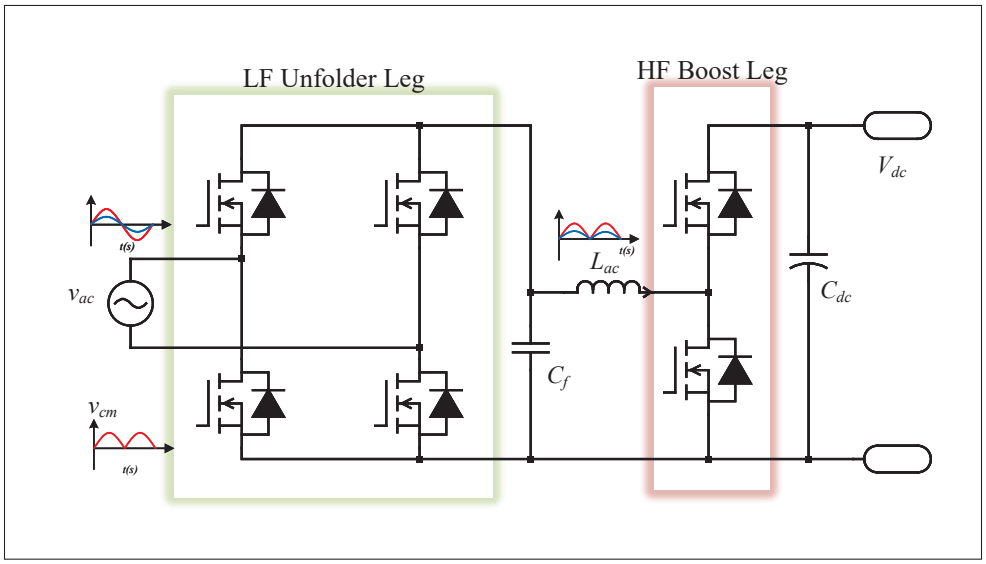


Figure 1.2 LF H-bridge unfolder feeding an |AC|/DC boost stage. LF CM voltage $v_{\mathrm{cm}}(t) = \hat{V}_{\mathrm{ac}}/2\sin(\omega t)$

1.2.1.3 Full-Bridge HF Operation (Both Legs HF)

A two-level H-bridge with both legs operated at HF synthesizes the line-to-line voltage directly. With bipolar PWM, the CM voltage is constant, $v_{\mathrm{cm}} = V_{\mathrm{dc}}/2$, eliminating switching-frequency CM components; with unipolar PWM, the CM voltage exhibits HF components but these can be effectively mitigated by DC-link-referenced capacitors as part of a combined DM/CM filter. This mechanism offers a well-controlled CM trajectory and supports compact EMI filters; however, it requires two HF legs and corresponding HF filter inductors.

Merits

Ideally no LF CM component; constant CM voltage under bipolar PWM; DC-link-referenced filter reduces external CM choke burden; mature modulation options; identical device rating in both HF legs.

Drawbacks

Two HF legs and two HF inductors; higher HF gate-drive count and potentially higher switching loss relative to single-HF-leg concepts.

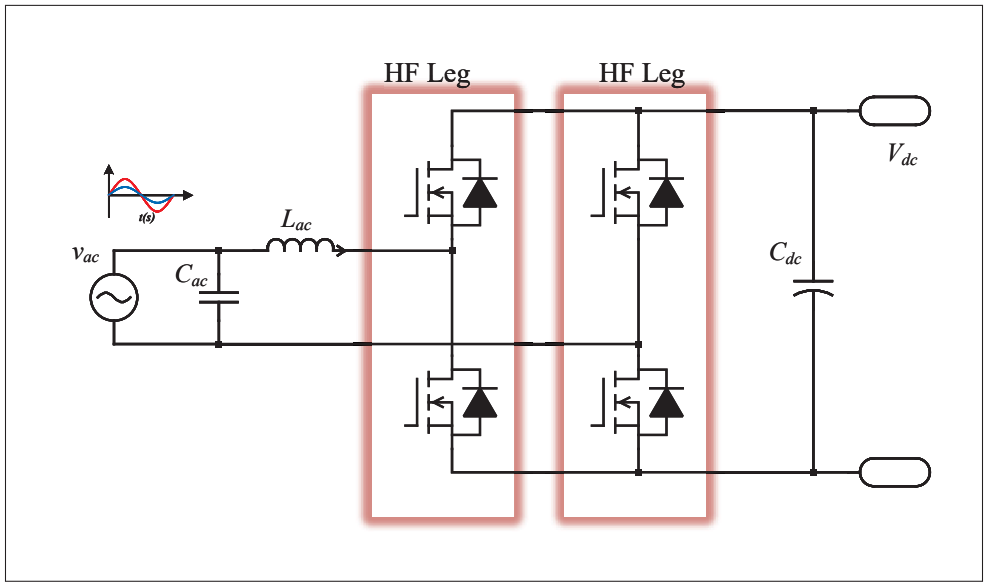


Figure 1.3 2-level H-bridge with both switching legs operated at HF

1.3 Candidate topologies (HF-cell centric)

We classify PFC candidates by the structure of the high-frequency (HF) synthesis leg and by the unfolder mechanism defined in Sec. 1.2. Let n_c denote the number of flying-capacitor (FC) cells per HF leg. A single FCML leg with n_c cells provides $m = n_c + 1$ discrete pole levels. With a line-frequency (LF) unfolder, the line-to-neutral levels become $N = 2m - 1 = 2n_c + 1$; with both legs HF, the line-to-line result is also $N = 2m - 1$. The effective ripple frequency seen by

the boost inductor scales with the number of commutations created by the series levels and by interleaving. This shared N masks important differences: the *step size* at the inductor node, the common-mode (CM) profile, and the per-device blocking voltage differ among topologies, and these differences dominate passive sizing and EMI filtering.

1.3.1 Totem-Pole Two-Level (LF Unfolder + 2L HF Leg) Baseline

The bridgeless totem-pole with a two-level HF pole is the baseline. The inductor must absorb a large volt-second per carrier period at a given f_{sw}; for a fixed ripple target this implies larger L than in multilevel variants. The HF devices block approximately V_{dc}, which typically drives the use of higher-voltage switches with higher $R_{\mathrm{DS(on)}}$. The LF unfolder minimizes LF switching loss but excites a larger CM swing at the grid interface, often increasing CM filter burden. See Fig. 1.1 for the circuit reference and CM example.

1.3.2 Totem-Pole FCML (TP-FCML, LF Unfolder + HF FC Leg)

Replacing the two-level pole with an FCML leg partitions the DC bus into n_c steps (Fig. 1.4) . Nominal HF device stress scales as V_{dc}/m, enabling lower-voltage devices with better switching and conduction figures of merit. The effective ripple frequency at the inductor node increases approximately in proportion to n_c for a single HF leg, so the required boost inductance for a given ripple and THD target reduces compared to the two-level HF leg. In practice, TP-FCML provides a strong density lever via reduced L for fixed THD, at the cost of added FC capacitance and balancing concerns that must be addressed in modulation and control.

1.3.3 H-Bridge Unfolder + HF FC Leg (LF HB-UF + FCML)

Moving from a totem-pole to a full H-bridge at line frequency (Fig. 1.5) reduces CM swing at the grid interface because both input terminals are symmetrically commutated at 50 Hz / 60 Hz while the HF synthesis occurs on a single FCML leg. The HF leg maintains $m = n_c + 1$ pole levels and similar effective-frequency multiplication as TP-FCML, so the inductor benefit is

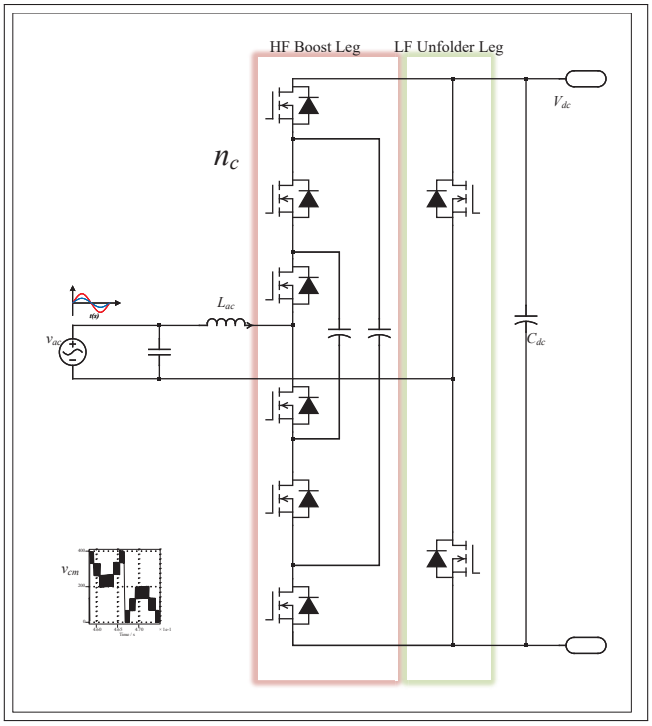


Figure 1.4 Totem-Pole FCML (TP-FCML, LF Unfolder + HF FC Leg)

retained. The penalty is additional LF devices and a modest increase in LF conduction loss; however, at 50 Hz / 60 Hz these losses are typically negligible relative to HF switching and conduction. This topology is attractive when conducted-EMI and ground-leakage constraints dominate, because the CM profile is inherently gentler than in bridgeless arrangements.

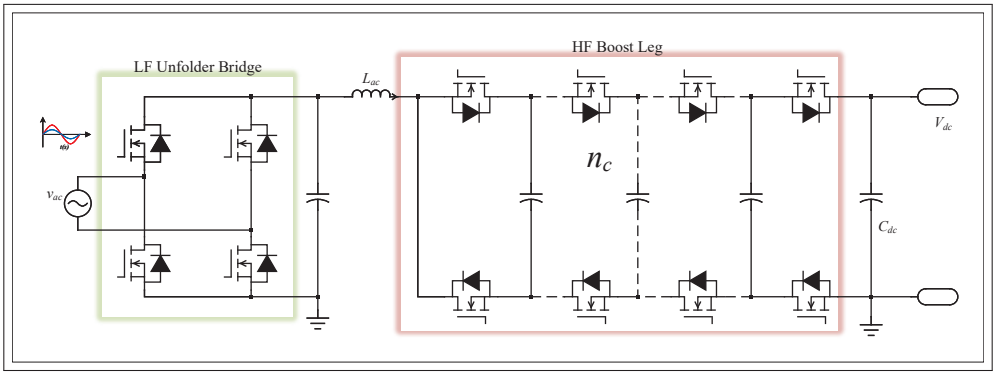


Figure 1.5 H-Bridge Unfolder + HF FC Leg (LF HB-UF + FCML)

1.3.4 Full-Bridge FCML (both legs HF)

Driving both legs at HF (Fig. 1.6) yields $N = 2m - 1$ line-to-line levels. The synthesis node sees smaller step voltage and roughly twice the commutation opportunities compared to a single HF leg, so a first-order model uses $f_{\text{eff}} \approx 2\, n_c\, f_{sw}$ for one phase and $f_{\text{eff}} \approx 2\, M\, n_c\, f_{sw}$ with M interleaved legs. The CM trajectory is the most benign among the candidates because both input terminals move in a balanced way at HF. Device voltage class reduces with $1/m$, enabling lower-voltage devices if FC voltage balancing is guaranteed. The cost is higher HF gate-drive count and stricter FC-voltage balancing dynamics.

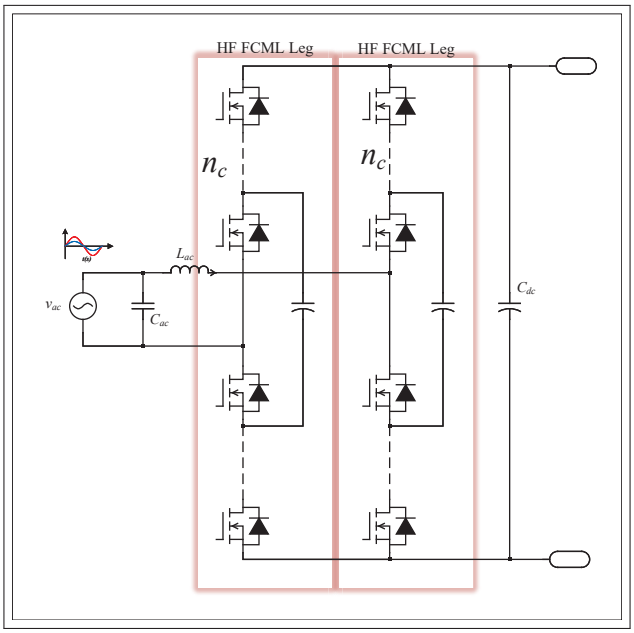


Figure 1.6 Full-bridge FCML (both legs HF)

1.3.5 Parallel-Interleaved FCML (M legs)

Interleaving M parallel HF legs (Fig. 1.7) with phase-shifted carriers multiplies the effective ripple frequency without increasing per-device f_{sw}, improving the tradeoff between boost inductance L, DM filter burden, and semiconductor loss. The same mechanism spreads RMS current and heat across legs; volume gains depend on whether separate inductors or a coupled multiwinding core is used. Co-optimization of L, the DM filter $(L_{\text{DM}}, C_{\text{DM}})$, and f_{sw} can be

carried out in closed form. Recent FCML-based PFC designs (Instruments, 2024b) show that an interleaved four-level TP-FCML can achieve very low AC-side passive volume at an optimized switching frequency.

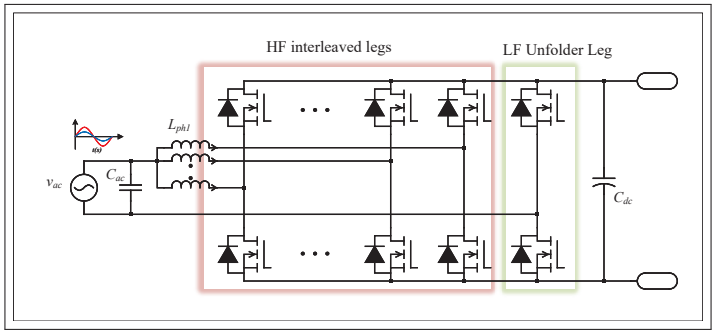


Figure 1.7 Parallel-interleaved FCML (M legs)

1.4 Design levers and compact laws used later

This section collects the compact relations employed later to size passives, normalize semiconductor losses across candidates, and compare density.

1.4.1 Effective ripple frequency

For an FCML leg with n_c flying cells per HF leg, the per-leg level count is $m = n_c + 1$. The switching-node edge multiplicity gives the effective ripple frequency seen by the boost inductor as

$$f_{\text{eff}} \approx \begin{cases} n_c\, f_{sw} & \text{single HF leg} \\ 2\, n_c\, f_{sw} & \text{full-bridge HF} \end{cases} \quad \text{and with interleaving } M: \; f_{\text{eff}} \leftarrow M\, f_{\text{eff}}. \tag{1.2}$$

The multiplication effect and its consequences for passive scaling are standard for FCML stages.

1.4.2 Boost inductor ripple and first sizing

Under CCM with PS-PWM, the worst-case triangular current ripple occurs at $d\,n_c - floor(d\,n_c) = 0.5$ and is represented by

$$\Delta i_{L,\max} \approx \frac{V_{dc}}{4\,L\,n_c\,f_{\text{eff}}} \quad \Rightarrow \quad L \approx \frac{V_{dc}}{4\,\Delta i_{L,\max}\,n_c\,f_{\text{eff}}}. \tag{1.3}$$

Equation (1.3) embeds all topology dependence through f_{eff} of (1.2) and yields the familiar $L \propto 1/n_c^2$ trend.

1.4.3 Device blocking

With balanced FC voltages, the nominal HF device rating scales inversely with the level count:

$$V_{ds,\max} \approx \frac{V_{dc}}{n_c}, \tag{1.4}$$

Lower device class reduces $E_{\text{sw}}(I,V)$ and $R_{\text{DS(on)}}$ at a given thermal limit, which is central to the benefit of higher n_c.

1.4.4 Flying-capacitor sizing

Flying-capacitor values are driven by allowable per-cell ripple Δv_{fc}, peak AC current, and the modulation strategy. Under PS-PWM with distributed switching states, the average charge swing per cell in one effective period scales with the leg current. A useful estimator is

$$C_{fc,min} \gtrsim \frac{I_{\text{ac,pk}}}{V_{dc}\,f_{sw}\,k_{fc}}, \tag{1.5}$$

where $k_{fc} = \Delta v_{fc}/V_{dc}$. The total FC capacitance grows approximately linearly with n_c because m steps require $n_c - 1$ FC. Chemistries with high volumetric efficiency and low ESR at the chosen per-device f_{sw} (e.g., film or high-Q ceramic depending on voltage class) directly reduce FC volume and switching loss.

1.4.5 Device-Technology Lens (SiC, GaN) in the Multilevel converters

As $m = n_c + 1$ increases, the nominal HF device rating decreases, enabling the use of lower-voltage GaN devices with significantly better hard-switching figures of merit than their higher-voltage counterparts. This substitution reduces switching loss at a fixed per-device f_{sw} and often offsets the added gate-drive count in full-bridge multilevel stages. Conversely, the LF unfolder (in H-bridge or ANPC clamps) can remain silicon or SiC, because it switches at 50 Hz / 60 Hz and contributes negligibly to switching loss. The combined effect, namely low per-device f_{sw} *and* high system f_{eff}, is favorable for both density and efficiency when thermal limits and EMI constraints are observed.

1.5 Analytical Comparison Models and Volume Metrics

For each candidate topology, defined by the choice of unfolder, number of flying-capacitor cells n_c, interleaving factor M, and device switching frequency f_{sw}, the models provide:

- the semiconductor loss estimate P_{semi} under a common device-technology assumption;
- required boost inductance and flying-capacitor values, together with simple energy-based volume estimators for these passives.

These models are not intended to replace detailed circuit-level design, but to support a consistent, topology-agnostic comparison under common specifications. EMI behavior and the associated DM/CM filter volumes are treated qualitatively in this chapter and reserved for more detailed analysis of volume comparison in future work.

1.5.1 Semiconductor Loss Model and Equal-Loss Constraint

Following (Lei *et al.*, 2018), the total semiconductor loss is separated into conduction and switching components,

$$P_{\text{semi}}(n_c, M) = P_{\text{cond}}(n_c, M) + P_{\text{sw}}(n_c, M). \tag{1.6}$$

For a given topology and modulation, the rms current in each device and the fraction of time it conducts follow from the ripple and current-splitting relations of Section 1.4. The conduction loss is approximated as

$$P_{\mathrm{cond}}(n_c, M) \approx \sum_k I_{k,\mathrm{rms}}^2 \, R_{\mathrm{on},k}, \tag{1.7}$$

where $I_{k,\mathrm{rms}}$ is the rms current of device k and $R_{\mathrm{on},k}$ is its on-resistance at the operating junction temperature and blocking-voltage rating (for example, using manufacturer data or the device-scaling rules in (Azurza Anderson *et al.*, 2021)).

Switching losses are modeled with energy-per-transition data,

$$P_{\mathrm{sw}}(n_c, M) \approx f_{sw} \sum_k E_{\mathrm{sw},k}\left(I_{k,\mathrm{sw}}, V_{k,\mathrm{sw}}\right), \tag{1.8}$$

where $E_{\mathrm{sw},k}(\cdot)$ is either measured or extracted from datasheet curves for the selected technology and gate-drive conditions. The switching current $I_{k,\mathrm{sw}}$ and voltage $V_{k,\mathrm{sw}}$ follow from the device placement and the per-cell blocking voltage defined in Section 1.4.

In order to compare topologies on a common basis, this chapter adopts an equal-loss constraint:

$$P_{\mathrm{semi}}(n_c, M) = P_{\mathrm{semi,ref}}, \tag{1.9}$$

where $P_{\mathrm{semi,ref}}$ is the total semiconductor loss of a reference design (here, the two-level totem-pole PFC meeting the same operating specifications). For each candidate topology, one design degree of freedom (for example f_{sw} or the parallel-device count) is adjusted so that (1.9) holds at nominal operating conditions.

1.5.2 Inductor and Flying-Capacitor Volume Metrics

Once the equal-loss constraint (1.9) fixes f_{sw} (or an equivalent degree of freedom), Section 1.4 provides the corresponding inductance and capacitance values:

- the boost-inductor value $L(n_c, M)$ from the ripple constraint in (1.3);

- the flying-capacitor stack capacitance and cell voltages from the flying-capacitor sizing relations in Section 1.4.

In line with the energy-density based approach of (Lei *et al.*, 2018), the boost-inductor and flying-capacitor volumes are approximated as

$$E_L(n_c, M) = \frac{1}{2} L(n_c, M)\, I_{L,\mathrm{pk}}^2, \tag{1.10}$$

$$V_L(n_c, M) \approx \frac{E_L(n_c, M)}{\rho_{E,L}}, \tag{1.11}$$

$$E_{\mathrm{FC}}(n_c, M) = \frac{1}{2} \sum_j C_{\mathrm{FC},j}\, V_{\mathrm{FC},j}^2, \tag{1.12}$$

$$V_{\mathrm{FC}}(n_c, M) \approx \frac{E_{\mathrm{FC}}(n_c, M)}{\rho_{E,C}}, \tag{1.13}$$

where $I_{L,\mathrm{pk}}$ is the peak inductor current at nominal power (common to all candidates under the same specifications), $\rho_{E,L}$ is an effective magnetic energy density, and $\rho_{E,C}$ is an effective capacitor energy density. The exact numerical values of $\rho_{E,L}$ and $\rho_{E,C}$ depend on the component technologies but cancel in normalized comparisons.

1.5.3 DM and CM EMI Analytical Models

1.5.3.1 Critical DM and CM design frequencies

For an FCML totem-pole PFC with n_c FC cells, M interleaved legs,the effective ripple frequency is defined as

$$f_{\mathrm{eff}}(n_c, M) = M\, n_c\, f_{\mathrm{sw}}. \tag{1.14}$$

The unified DM harmonic envelope then gives the unfiltered DM noise at any chosen design harmonic index k_{DM} in the conducted-EMI band (Tausif & Dusmez, 2023).

The corresponding *DM design frequency* is

$$f_{\mathrm{D,DM}}(n_c, M) = k_{\mathrm{DM}}\ f_{\mathrm{eff}}(n_c, M) = k_{\mathrm{DM}}\ M\, n_c\, f_{\mathrm{sw}}. \tag{1.15}$$

.

Exact CM prediction requires a detailed parasitic network and layout information, as demonstrated for FCML stages in (Giardine *et al.*, 2025). It derives the CM current spectrum of an N-level FCML stage as a set of harmonics of the switching frequency, with strong content at the fundamental f_{sw} and at the effective switching frequency $f_{\mathrm{eff}} = M\, n_c\, f_{\mathrm{sw}}$.

For the FCML PFC, this is written as

$$f_{\mathrm{D,CM}}(N, M) = k_{\mathrm{CM,crit}}(n_c, M)\, f_{\mathrm{sw}}, \tag{1.16}$$

where $k_{\mathrm{CM,crit}}$ indexes the dominant CM harmonic.

DM attenuation requirement and normalized DM volume metric

Using the unified DM noise method of (Tausif & Dusmez, 2023) yields the unfiltered DM emission at the LISN port for $f_{\mathrm{D,DM}}(n_c, M)$,

$$v_{\mathrm{DM}}\big(f_{\mathrm{D,DM}}; n_c, M\big)\ \ [\mathrm{dB}\,\mu\mathrm{V}],$$

from which (Dey, Mallik & Mishra, 2022) define the required DM attenuation at the design frequency as

$$A_{\mathrm{DM,req}}(n_c, M) = v_{\mathrm{DM}}\big(f_{\mathrm{D,DM}}; n_c, M\big) - \mathrm{Limit}\big(f_{\mathrm{D,DM}}\big) + A_{\mathrm{margin}} \quad [\mathrm{dB}]. \tag{1.17}$$

The corresponding linear attenuation ratio is

$$\mathrm{Att}_{\mathrm{DM,req,lin}}(n_c, M) = 10^{A_{\mathrm{DM,req}}(n_c, M)/20}. \tag{1.18}$$

For an N_f-stage DM LC filter, (Ishraq & Mallik, 2024a) use the standard high-frequency asymptote for cascaded second-order sections and write the DM attenuation at the design frequency as

$$\mathrm{Att}_{\mathrm{DM}}(f_{\mathrm{D,DM}}) = (2\pi f_{\mathrm{D,DM}})^{2N_f} \left(L_{\mathrm{DM}}\, C_{\mathrm{DM}}\right)^{N_f}. \tag{1.19}$$

The attenuation constraint is then

$$\mathrm{Att}_{\mathrm{DM}}(f_{\mathrm{D,DM}}) \;\geq\; \mathrm{Att}_{\mathrm{DM,req,lin}}(n_c, M). \tag{1.20}$$

Since the volumetric cost function for DM inductors and capacitors is monotonic in L_{DM} and C_{DM} (Ishraq & Mallik, 2024a; Dey *et al.*, 2022), a convenient *normalized DM EMI filter volume index* is

$$\Xi_{\mathrm{DM}}(n_c, M) = \frac{\mathrm{Att}_{\mathrm{DM,req,lin}}(n_c, M)}{(2\pi f_{\mathrm{D,DM}}(n_c, M))^{2N_f}}, \tag{1.21}$$

which is proportional to the optimal LC-product and hence to the minimum achievable DM filter volume for a fixed technology set and filter order N_f.

CM attenuation requirement and normalized CM volume metric

(Giardine *et al.*, 2025). derives the CM current harmonic at index k for an N-level FCML cell as $a_{\mathrm{CM},k}(N, \ldots)$. The CM LISN voltage magnitude at the chosen design harmonic $k_{\mathrm{CM,crit}}$ is

$$V_{\mathrm{CM}}\big(f_{\mathrm{D,CM}}; N, M\big) = \big|Z_{\mathrm{LISN}}\big(f_{\mathrm{D,CM}}\big)\big|\,\big|a_{\mathrm{CM},k_{\mathrm{CM,crit}}}(N, \ldots)\big|. \tag{1.22}$$

By direct analogy with the DM case in (Dey *et al.*, 2022), the required CM attenuation at the design frequency is

$$A_{\mathrm{CM,req}}(N, M) = 20\log_{10}\!\left(\frac{V_{\mathrm{CM}}\big(f_{\mathrm{D,CM}}; N, M\big)}{1\ \mu\mathrm{V}}\right) - \mathrm{Limit}\big(f_{\mathrm{D,CM}}\big) + A_{\mathrm{margin}} \quad [\mathrm{dB}], \tag{1.23}$$

with

$$\mathrm{Att}_{\mathrm{CM,req,lin}}(N, M) = 10^{A_{\mathrm{CM,req}}(N,M)/20}. \tag{1.24}$$

For an N_f-stage per-phase CM filter with equivalent inductance L_C and capacitance C_C, Dey et al. write the CM attenuation at the design frequency as (Dey *et al.*, 2022)

$$\mathrm{Att}_{\mathrm{CM}}(f_{\mathrm{D,CM}}) = (2\pi f_{\mathrm{D,CM}})^{2N_f} \left(L_\mathrm{C}\, C_\mathrm{C}\right)^{N_f}, \tag{1.25}$$

with the design constraint

$$\mathrm{Att}_{\mathrm{CM}}(f_{\mathrm{D,CM}}) \;\geq\; \mathrm{Att}_{\mathrm{CM,req,lin}}(N, M). \tag{1.26}$$

Again using the monotonic CM volumetric cost function of (Dey *et al.*, 2022), a *normalized CM EMI filter volume index* is defined as

$$\Xi_{\mathrm{CM}}(N, M) = \frac{\mathrm{Att}_{\mathrm{CM,req,lin}}(N, M)}{(2\pi f_{\mathrm{D,CM}}(N, M))^{2N_f}}, \tag{1.27}$$

which is proportional to the minimum CM filter volume for fixed component technology and stage count.

Topology-comparison metric

For a fixed filter order N_f and a fixed inductor/capacitor technology library, the minimum boxed EMI filter volumes scale as

$$V_{\mathrm{DM}}(n_c, M) \propto \Xi_{\mathrm{DM}}(n_c, M), \qquad V_{\mathrm{CM}}(N, M) \propto \Xi_{\mathrm{CM}}(N, M), \tag{1.28}$$

so that the impact of the FCML topology (n_c, M) on EMI filter volume is completely captured, for comparison purposes, by the two critical design frequencies $f_{\mathrm{D,DM}}(n_c, M)$ and $f_{\mathrm{D,CM}}(N, M)$ and the corresponding attenuation requirements.

1.5.4 Aggregate Passive-Volume Metric

The total ac-side passive volume combines the contributions of the boost inductor, flying capacitors, DM filter, and CM choke,

$$V_{\text{passive,ac}}(n_c, M) = V_L(n_c, M) + V_{\text{FC}}(n_c, M). \tag{1.29}$$

For comparison, a normalized passive-volume index is defined as

$$\Phi_{\text{passive}}(n_c, M) = \frac{V_{\text{passive,ac}}(n_c, M)}{V_{\text{passive,ac}}(1, 1)}, \tag{1.30}$$

where $V_{\text{passive,ac}}(1, 1)$ corresponds to the reference two-level totem-pole PFC.

In this chapter, only $V_L(n_c, M)$ and $V_{\text{FC}}(n_c, M)$ are evaluated explicitly through the energy-density approximation, and DM/CM filter contributions are accounted for qualitatively at the comparison stage. A full EMI-aware evaluation of V_{DM} and V_{CM}, and hence of Φ_{passive}, is reserved for future work.

1.6 Comparison Frameworks

The analytical models of Section 1.5 map each candidate topology and parameter set (n_c, M, f_{sw}) to semiconductor losses, EMI-related indices, and passive-volume estimates such as $V_L(n_c, M)$, $V_{\text{FC}}(n_c, M)$, $V_{\text{DM}}(n_c, M)$, and $V_{\text{CM}}(n_c, M)$, which are combined in the aggregate metric $V_{\text{passive,ac}}(n_c, M)$ in (1.29). The comparison framework specifies how these models are used to obtain fair and interpretable results (Lei *et al.*, 2018; Kolar, Biela & Minibock, 2009; Azurza Anderson *et al.*, 2021), and provides the structure for the summary tables reported in the next section.

All comparisons in this chapter share a common operating specification: nominal power $P_{\text{N}} = 3.3$ kW, input voltage range $V_{G,\text{rms}} \in [90, 265]$ V, regulated dc link $V_{dc} = 400$ V, near-unity power factor, and input-current THD below approximately 3 %, as defined in Section 1.1.

The boost-inductor ripple and dc-link ripple constraints are enforced as in Section 1.4. Device technology (voltage class, conduction and switching figures of merit) is kept consistent with the device-scaling assumptions used in (Lei *et al.*, 2018; Azurza Anderson *et al.*, 2021).

1.6.1 Equal-loss passive-volume comparison

In the primary framework, each candidate topology is designed to satisfy the following constraints.

1. *Equal semiconductor loss.* The total semiconductor loss at nominal operating conditions satisfies the equal-loss constraint

$$P_{\text{semi}}(n_c, M) = P_{\text{semi,ref}}, \tag{1.31}$$

   where $P_{\text{semi}}(n_c, M)$ is obtained from (1.6)–(1.8) and $P_{\text{semi,ref}}$ corresponds to the reference two-level totem-pole PFC under the same operating point and cooling assumptions. For each topology, (n_c, M, f_{sw}) is adjusted within practical limits until (1.31) is met.
2. *Inductor and flying-capacitor sizing.* The boost inductance $L(n_c, M)$ and the total flying-capacitor stack $\sum C_{fc}(n_c, M)$ are obtained from the ripple-based sizing laws of Section 1.4, using the effective ripple frequency f_{eff} in (1.2). A common ripple specification,

$$\Delta i_{L,\max} \in [0.10, 0.20]\ I_{\text{pk}}, \qquad \Delta v_{fc} \le \sigma\, V_{dc}/m,$$

   ensures that inductance and flying-capacitor values are comparable across candidates.
3. *Volume proxies for L and FC stacks.* The corresponding inductor and flying-capacitor volumes $V_L(n_c, M)$ and $V_{\text{FC}}(n_c, M)$ are estimated from (1.10)–(1.13) using common energy-density assumptions, consistent with (Lei *et al.*, 2018). These proxies capture how level count and interleaving redistribute energy storage between magnetics and capacitors.

Under these constraints, the comparison focuses on how (n_c, M) affects the partitioning between inductor and flying-capacitor volume for a fixed semiconductor-loss budget. DM and CM filters

are assumed to meet the relevant conducted-EMI and leakage constraints for each topology, but their detailed volume contributions are not optimized or compared in this chapter.

1.6.2 Reported quantities and tabulated comparison

Under the equal-loss framework described above, the numerical results are summarized purely in tabular form rather than as full optimization plots. Each candidate topology (combination of unfolder, n_c, M, and HF configuration) is represented by a single row in one or more tables that report:

- the structural parameters and operating point (unfolder type, n_c, M, overall level count N, f_{sw}, f_{eff});
- the main sizing outcomes (boost inductance L, total flying capacitance $\sum C_{fc}$);
- the energy-based inductor and FC volume proxies (V_L, V_{FC}) and simple normalized ratios with respect to the two-level reference;
- a compact loss and efficiency screen (equalized P_{semi}, estimated efficiency η at the nominal point).

This tabulated presentation keeps the comparison aligned with the analytical sizing laws while avoiding exhaustive numerical optimization. It provides a direct view of how level count and interleaving influence the partitioning of passive volume between L and flying capacitors for a fixed loss budget.

Table 1.1 Structural comparison of candidate FCML totem-pole PFC topologies at $f_{\text{sw}} = 100$ kHz

n_c	M	**Levels** m	N_{HF}	N_{LF}	N_{FC}	$V_{\text{block,HF}}/V_{\text{dc}}$
1	1	2	2	2	0	1
1	2	2	4	2	0	1
1	3	2	6	2	0	1
1	4	2	8	2	0	1
2	1	3	4	2	1	1/2
2	2	3	8	2	2	1/2
3	1	4	6	2	2	1/3
4	1	5	8	2	3	1/4

Table 1.2 Boost inductors and flying-capacitor requirements for equal inductor current ripple (10% of $I_{\mathrm{ac,pk}}$) and $C_{fc,\min}$ sizing at $f_{\mathrm{sw}} = 100$ kHz, $V_{dc} = 400$ V, $I_{\mathrm{ac,pk}} = 25$ A, and $k_{fc} = 0.05$

Case	$f_{\mathbf{eff}}$ **[kHz]**	N_L	$L_{\mathbf{leg}}/L_{\mathbf{ref}}$	$L_{\mathbf{leg}}$ **[mH]**	$L_{\mathbf{tot}}$ **[mH]**	$N_{\mathbf{FC}}$	$C_{fc,\mathbf{cell}}$ **[μF]**	$C_{fc,\mathbf{tot}}$ **[μF]**
(1,1) ref	100	1	1	0.400	0.400	0	–	0
(1,2)	200	2	1/2	0.200	0.400	0	–	0
(1,3)	300	3	1/3	0.133	0.400	0	–	0
(1,4)	400	4	1/4	0.100	0.400	0	–	0
(2,1)	200	1	1/4	0.100	0.100	1	12.5	12.5
(2,2)	400	2	1/8	0.050	0.100	2	12.5	25.0
(3,1)	300	1	1/9	0.044	0.044	2	12.5	25.0
(4,1)	400	1	1/16	0.025	0.025	3	12.5	37.5

The numerical inductance and flying-capacitor values reported in Table 1.2 are obtained by evaluating the general design relations introduced earlier for a common 3.3 kW specification. The flying-capacitor sizing relation in (1.5) does not depend on the number of FC cells per leg, because it is set only by the peak ac current, dc-link voltage, switching frequency, and the tolerated high-frequency ripple fraction. For the considered design point of $P_{\mathrm{out}} \approx 3.3$ kW with $I_{\mathrm{ac,pk}} = 25$ A, $V_{dc} = 400$ V, $f_{\mathrm{sw}} = 100$ kHz, and a 5% flying-capacitor voltage ripple, (1.5) yields a minimum per-cell capacitance $C_{fc,\min} \approx 12.5$ uF. This value is used as the reference $C_{fc,\mathrm{cell}}$ in Table 1.2, so that the total FC requirement grows linearly with the number of FC cells per phase, N_{FC}, while the blocking voltage of each individual FC capacitor decreases in steps of V_{dc}/n_c as the number of levels increases.

The boost inductance entries are obtained from the inductor design equation (1.3), evaluated for a 10% peak-to-peak inductor current ripple with respect to $I_{\mathrm{ac,pk}}$ at the worst-case point of the line cycle. For each (n_c, M) combination, the effective ripple frequency $f_{\mathrm{eff}} = M n_c f_{\mathrm{sw}}$ is used in (1.3) to determine the required per-leg inductance L_{leg} that preserves the same relative ripple as in the two-level reference case $(n_c, M) = (1, 1)$. In the interleaved topologies with $M > 1$, the total number of boost inductors per phase is $N_L = M$, each with value L_{leg}, so that the total stored-energy capability scales as $L_{\mathrm{tot}} = M L_{\mathrm{leg}}$. At the same time, the core flux and winding current ratings are split across M parallel inductors, allowing each individual inductor to use

a smaller core and reduced copper cross-section. This splitting of current and flux density is reflected in the L_{leg} and L_{tot} columns of Table 1.2 and is relevant when comparing the realizable inductor volume and thermal margins of the different (n_c, M) options from a power-density perspective.

1.7 Summary and Outlook

This chapter has examined single-phase boost-type power factor correction front ends from a topology-agnostic, passive-centric perspective. The emphasis has been on high-power single-phase rectifiers operating from distribution-level input voltages and delivering a regulated dc link around 400 V at approximately 3.3 kW, with near-unity power factor and constrained input-current distortion. Within this operating window, the chapter has classified candidate front ends according to their high-frequency synthesis leg and low-frequency unfolder mechanism, introduced a common notation for the number of flying-capacitor cells per leg and the interleaving factor, and treated level count and interleaving as primary design levers for ac-side passive components.

On the structural side, the chapter has contrasted the conventional two-level totem-pole baseline with flying-capacitor multilevel variants and interleaved implementations. The discussion has highlighted how splitting the dc-link voltage across multiple capacitor cells reduces the blocking requirement of each high-frequency device and enables the use of lower-voltage switch technologies with better conduction and switching characteristics. At the same time, the increased number of discrete voltage steps and the use of interleaving raise the effective commutation frequency seen by the boost inductor, allowing a significant reduction in required inductance for a fixed ripple target. These mechanisms create a structured tradeoff between inductor volume, flying-capacitor volume, and semiconductor count.

On the sizing side, compact design relations have been collected for the boost inductors and flying-capacitor stacks under continuous-conduction operation and phase-shifted modulation. These relations provide simple rules that link the chosen level count, interleaving factor, and

switching frequency to the required inductance and capacitance values, and then map those values to approximate volumes using energy-density arguments. A semiconductor-loss model, based on a separation of conduction and switching contributions and on device-scaling assumptions from the literature, has been used to enforce a common loss budget across all topologies. Under this equal-loss constraint, the tables in the chapter summarize how each combination of level count and interleaving redistributes passive volume between magnetics and capacitors for the same operating point and loss level.

Electromagnetic interference has been treated at the level of qualitative design implications rather than as a fully optimized comparison metric. The discussion has noted that the same mechanisms which increase the effective ripple frequency and reduce boost inductance also tend to shift dominant differential-mode and common-mode noise components toward higher frequencies, which is generally favorable for filter design. At the same time, a rigorous mapping from noise spectra to boxed filter volume depends on detailed parasitic information and a specific component library. To avoid speculative conclusions, this chapter has therefore restricted itself to qualitative EMI considerations and to an aggregate passive-volume definition that explicitly separates inductor and flying-capacitor contributions from the yet-to-be-optimized filter volumes.

Overall, the chapter provides a compact framework for screening single-phase PFC topologies before committing to detailed design. By standardizing operating specifications, introducing a consistent notation for structural parameters, and using simple but physically grounded sizing laws, it clarifies how moderate increases in level count and carefully chosen interleaving factors can substantially reduce boost inductor requirements at the cost of additional flying-capacitor energy storage and high-frequency devices. The resulting structural tables and sizing rules identify a small set of promising flying-capacitor multilevel front ends that offer attractive passive-volume and efficiency potential. Subsequent chapters build on this foundation by selecting one specific FCML topology, detailing its control and hardware implementation, and quantifying its measured performance, including full EMI behavior and total passive volume, against the qualitative trends established here.

CHAPTER 2

HARDWARE DEVELOPMENT AND REAL-TIME CONTROL IMPLEMENTATION OF A TOTEM-POLE 5L-FCML PFC CONVERTER

2.1 Introduction

The previous chapter introduced the flying-capacitor multilevel (FCML) totem-pole power factor correction (PFC) converter, motivated its use in single-phase ac-dc front ends, and compared it against other multilevel candidate topologies. That discussion highlighted the potential of a 5-level FCML totem pole PFC front end to increase efficiency, reduce passive filter volume, and improve input current quality for applications such as on-board chargers and residential ac-dc interfaces(Qin *et al.*, 2019; Lei *et al.*, 2017; Qin, Lei, Barth, Liu & Pilawa-Podgurski, 2017).

This chapter moves from concept to implementation and describes the realization of a 2.5 kW TP 5L-FCML PFC prototype and its digital control platform. The prototype interfaces a 90 to 230 V rms, 50/60 Hz grid to a regulated 400 V dc bus with near unity power factor, low input current total harmonic distortion, and controlled dc bus ripple over a wide operating range. The prototype is a development platform intended primarily for control evaluation; accordingly, several semiconductor and passive components are deliberately over-dimensioned in voltage and current rating relative to their nominal operating stress to improve robustness during fault conditions and repeated experimental debugging.

The control implementation is based on a state of the art linear controller with phase-shifted pulsewidth modulation (PSPWM), an inner current loop with input voltage feedforward, an outer dc-link voltage loop with load feedforward, and active flying capacitor voltage balancing. These algorithms are executed in real time on a TMS320F28379D microcontroller that drives a dedicated power stage and acquires measurements through an isolated-sensor and control interface board.

The remainder of the chapter is organized as follows. Section 2.2 formalizes the key system level specifications and outlines the overall hardware architecture. Subsequent sections describe

the power stage, the control interface board, and the digital control implementation in detail, and present experimental results that validate the performance of the prototype.

2.2 System specifications and architecture

2.2.1 Key system specifications

The FCML totem pole PFC prototype is specified as a single phase front end that shapes the input current to be nearly sinusoidal and in phase with the mains voltage while regulating a high voltage dc bus. Table 2.1 summarizes the key input, output, performance, and protection requirements that serve as numerical design targets for the selection of device ratings, passive components, sensing ranges, and control bandwidths.

Table 2.1 Key system specifications

Category	Specification
Input	Single-phase AC input; 85 V rms to 265 V rms; 47 Hz to 63 Hz;
	Power factor ≥ 0.99 at rated power;
	Line current harmonics less than 2% at 240 V rms and full load
Output	Regulated dc bus in the range 380 V to 420 V;
	2.5 kW at 230 V rms and 400 V; 1.25 kW at 120 V rms and 400 V;
	Output power limited by 13 A rms input current;
	5% regulation around 400 V with 960 μF bus capacitance;
	Target peak efficiency 98.5%, rated efficiency 98.2%
Performance	Full load step settling within approximately one mains cycle;
	Switching frequency 65 kHz; reinforced isolation;
	Sensing of input AC voltage, flying capacitor voltages, and DC bus voltage
Protection	Hardware overcurrent protection and PWM disable latch;
	PLL undervoltage threshold 30 V rms;
	AC overvoltage threshold 266 V rms;
	DC overvoltage threshold 450 V

Device and component ratings are selected with sufficient margins such that these specifications are met under normal operation while allowing safe testing of control functions and fault handling sequences.

2.2.2 Hardware partitioning and architecture overview

The hardware implementation follows a three-board partition that mirrors the functional structure implied by the specifications in Table 2.1:

- *Power board*: Implements the totem pole leg, the high frequency TP 5L FCML leg, the grid side inductance, the dc link capacitor, and the flying capacitor bank. This board carries all high voltage and high current components and is laid out to control parasitic inductances, dv/dt, and creepage and clearance distances.
- *Control interface board*: Provides current and voltage sensing, signal conditioning, isolation, PWM buffer, and hardware protection. It implements the front ends for the input ac voltage, inductor current, flying capacitor voltages, and dc bus voltage, and generates hardware fault and PWM disable signals.
- *Digital controller*: Based on a TMS320F28379D microcontroller. It receives the conditioned measurements, monitors fault inputs, and drives the gate drivers through pulsewidth modulation outputs while executing the linear current and voltage loops, flying capacitor balancing, dead time compensation, and the phase locked loop.

Fig. 2.1 shows the assembled experimental test setup, and Fig. 2.2 details the block diagram and physical interconnection of these three boards together with the main instrumentation. The following sections use this partitioning to present the design of the power stage, control interface board, and digital control implementation.

2.3 Power Stage Design

2.3.1 Topology and ratings

The hardware implementation follows the TP 5L-FCML PFC topology shown in Fig. 2.3. Figure 2.4 shows the realized power stage PCB with the flying capacitors, boost inductor, dc link capacitor, and SiC MOSFETs layout. The key active and passive components, together with their voltage and current ratings, are summarized in Table 2.2.

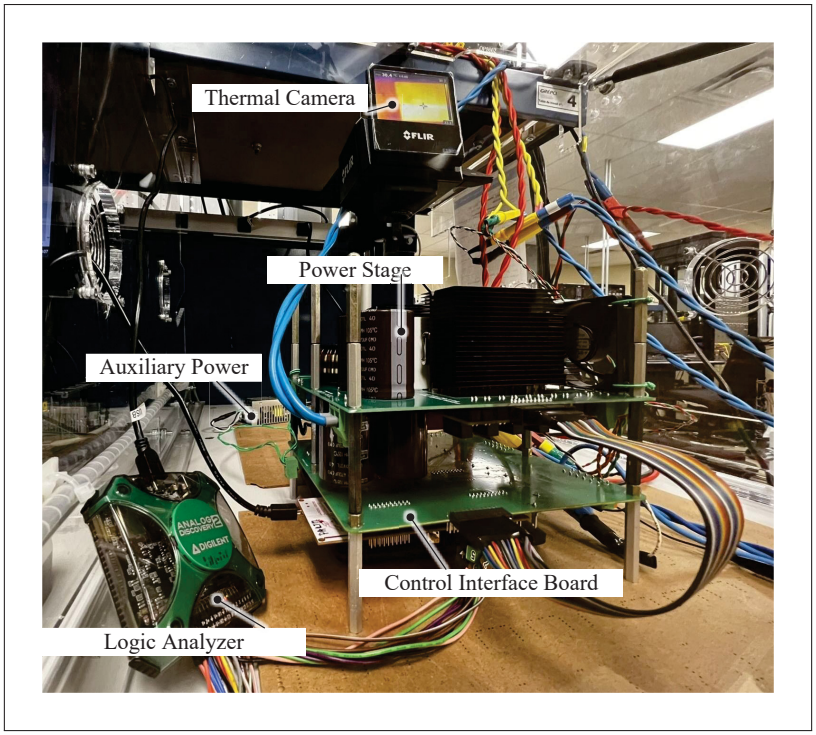


Figure 2.1 Assembled experimental setup of the TP 5L-FCML totem-pole PFC prototype showing the stacked power stage and control interface boards

Table 2.2 Component listing for the 2.5 kW TP-5L-FCML PFC prototype

Component	Part number	Key parameters
SiC MOSFET	10× C3M0060065D	650 V, $R_{ds,on}$ = 60 mΩ
Isolated gate driver	10× UCC23514E	5 kV_{rms}, 4/5 A
Voltage sensor	5× AMC3330QDWERQ1	Isolated voltage amplifier
AC current sensor	1× CT426-HSN820MR	±20 A
DC current sensor	1× CT426-HSN820DR	0–20 A
Boost inductor	1× 760801401	118 μH, 22 mΩ
Flying capacitors	3× C4AQLBW5700A3LK	70 μF, 500 V, 2.1 mΩ
DC-link capacitor	2× B43548A5567M060	960 μF, 450 V
Microcontroller	1× TMS320F28379D	200 MHz, dual C28 cores

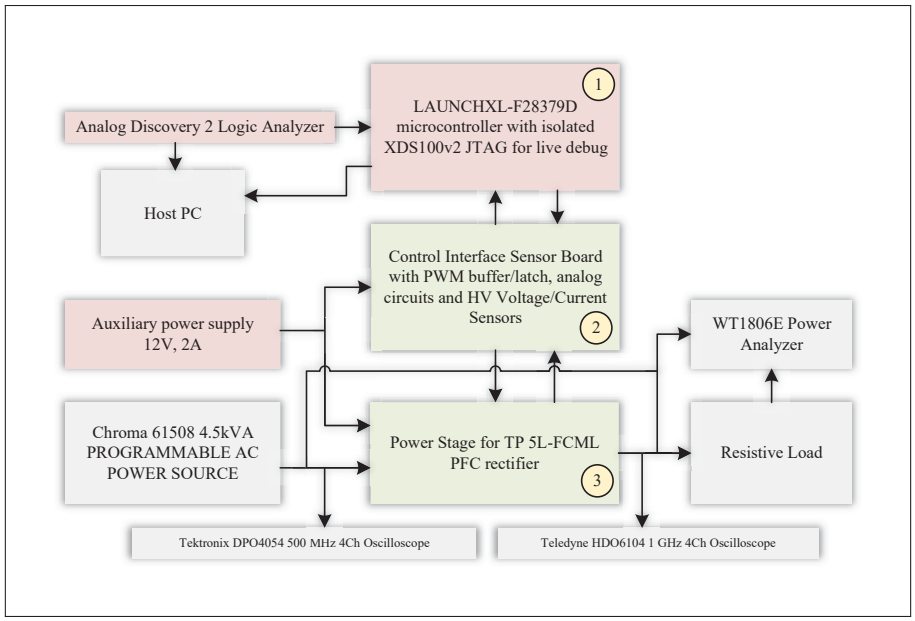


Figure 2.2 System level block diagram

2.3.2 Selection of switching devices

The converter operates from a universal single phase ac input and a regulated dc bus in the 380 V to 420 V range (Table 2.1). The worst case peak of the rectified line is $v_{G,\mathrm{pk,max}} = \sqrt{2}\, v_{G,\mathrm{rms,max}}$, and the commanded maximum dc bus voltage is denoted $V_{DC,\mathrm{max}}$. The low frequency totem-pole leg must withstand at least this value plus transient overshoot, so the device blocking rating is chosen as $V_{sw,\mathrm{LF,rated}} \geq k_{V,\mathrm{LF}}\, V_{DC,\mathrm{max}}$, $k_{V,\mathrm{LF}} \approx 1.6\text{–}1.8$.

In the FCML leg, the four FC cell split the dc link into approximately equal steps of $V_{DC}/4$. Each high frequency device therefore sees at most one step under steady state, $V_{sw,\mathrm{HF,steady}} \approx \frac{V_{DC,\mathrm{max}}}{4}$, and the selected rating satisfies $V_{sw,\mathrm{HF,rated}} \geq k_{V,\mathrm{HF}} \frac{V_{DC,\mathrm{max}}}{4}$, $k_{V,\mathrm{HF}} \approx 1.5\text{–}2$.

The maximum rms input current at low line and rated power is $I_{g,\mathrm{rms,max}} = \frac{P_{\mathrm{rated}}}{v_{g,\mathrm{rms,min}}\ \mathrm{pf}}$, with pf the minimum guaranteed power factor. A device current rating is $I_{sw,\mathrm{rms,rated}} \geq k_I\, I_{g,\mathrm{rms,max}}, \qquad k_I \gtrsim 1.5$. For MOSFET based implementations the conduction and switching losses of each device are estimated as $P_{\mathrm{cond}} \approx I_{sw,\mathrm{rms}}^2 R_{\mathrm{ds,on}}$, $P_{\mathrm{sw}} \approx \frac{1}{2} V_{sw,\mathrm{eff}} I_{sw,\mathrm{pk}} (t_{\mathrm{on}} + t_{\mathrm{off}}) f_{sw}$, and used with datasheet parameters to verify that the junction temperature remains within limits

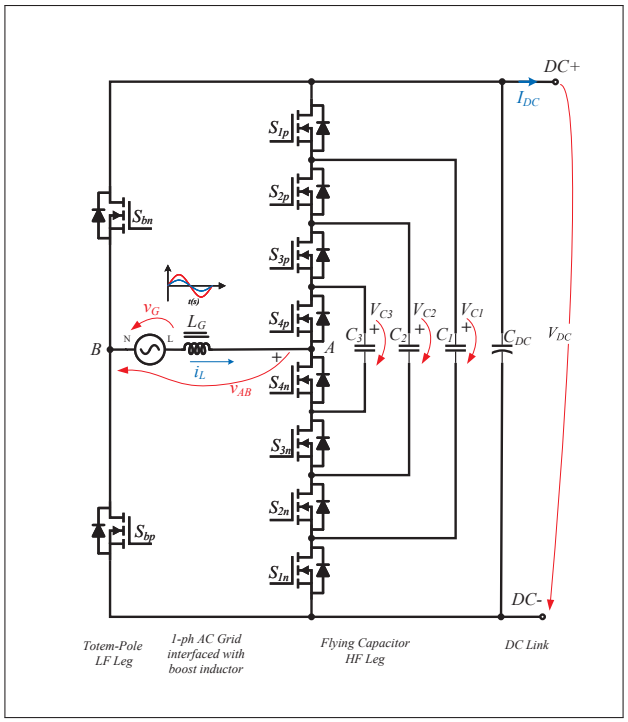


Figure 2.3 Configuration and sign conventions of the TP-5L-FCML PFC converter. Positive directions of v_G, i_L, v_{AB}, V_{Cm}, and I_{DC} are shown by arrows

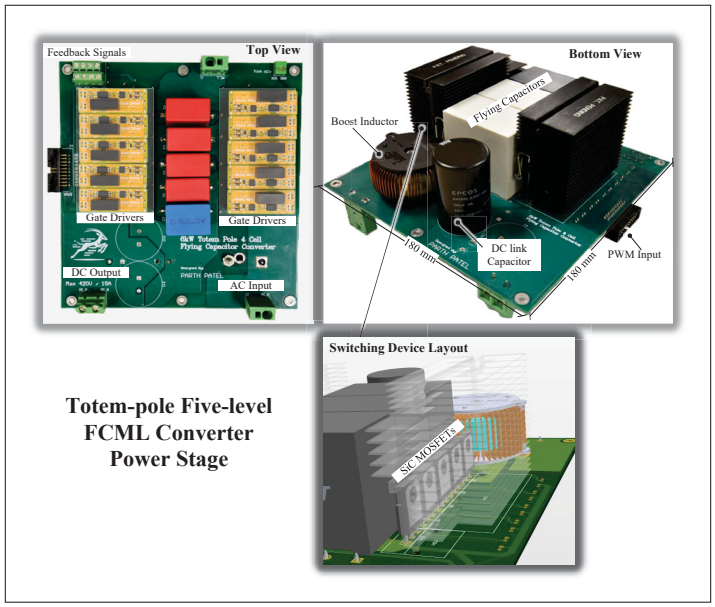


Figure 2.4 Photograph of the TP-5L-FCML PFC power stage board

for the worst case combination of line, load, and ambient temperature. In the implemented prototype all power switches, including the low frequency totem pole devices and the high frequency FCML devices, are realized using 650 V SiC MOSFETs (Wolfspeed, 2024), which satisfy the above blocking requirements with margin.

2.3.3 Gate driver architecture

Gate-drive power delivery is a critical design aspect in FCML converters, because most switches are floating and require isolated supplies. Recent work has demonstrated compact bootstrap and charge pump based solutions that eliminate discrete isolated dc-dc converters for GaN based FCML legs (Ye, Lei, Liu, Shenoy & Pilawa-Podgurski, 2020, 2017). These methods exploit the FCML flying capacitor structure to distribute gate drive power efficiently, but their correct operation depends on the switching pattern, duty ratio, and device characteristics.

In this prototype, a more conservative gate drive architecture is adopted. The hardware is intended as a reusable platform for later implementation of nonlinear control strategies that do not rely on fixed phase shifted PWM. In this work, each SiC MOSFET is supplied from a dedicated isolated dc-dc converter, providing a floating low power rail local to the device. An isolated gate driver with optocoupler based logic input is used for each switch to provide galvanic isolation between the controller PWM signals and the high voltage power stage.

The SiC MOSFETs are driven with a bipolar gate voltage of +15 V turn on and -3.3 V turn off. The gate driver output stage and series gate resistance are selected such that the available peak current $I_{\text{drv,pk}} \approx \frac{Q_g}{t_r}$,where Q_g is the total gate charge and t_r is the targeted voltage rise time, comfortably exceeds the requirement at the maximum switching frequency. Separate turn on and turn off resistors are used where needed to shape the switching transitions and limit overshoot on the drain voltage.

To minimize gate loop inductance and improve common mode immunity, the gate driver and its isolated dc-dc converter are implemented on small modular PCBs that plug directly on top of the corresponding SiC MOSFETs. Each gate driver module receives a single ended logic PWM

signal and a 12 V auxiliary supply from the main power stage board through short connectors. On the power stage PCB, the digital PWM traces are routed with controlled reference planes and kept physically separated from the feedback paths to reduce coupling of high dv/dt gate drive edges.

2.3.4 Design and selection of passive components

The grid side inductor L_G is dimensioned from the allowed peak to peak current ripple at the switching frequency(Lei *et al.*, 2018). For a simplified boost like operating interval near the line peak, the worst case ripple can be written in terms of the number of FC cells n_c as

$$L_G \;\geq\; \frac{V_{DC}}{4\,\Delta i_{L,\text{pk-pk}}}\,\frac{1}{f_{\text{sw}}}\,\frac{1}{n_c^2}, \tag{2.1}$$

where $\Delta i_{L,\text{pk-pk}}$ is the specified peak to peak inductor current ripple. For a chosen ripple ratio $\Delta i_{L,\text{pk-pk}}/I_{g,\text{pk}}$, this expression yields the minimum inductance.

The dc link capacitor C_{DC} is chosen from the allowable low frequency dc-link voltage ripple at twice the line frequency. The required capacitance to limit the ripple ΔV_{DC} at rated power is

$$C_{DC,\text{min}} \approx \frac{P_{\text{rated}}}{\omega_{\text{line}}\,V_{dc,\text{nom}}\,\Delta V_{DC}}, \tag{2.2}$$

with $\omega_{\text{line}} = 2\pi f_{\text{line}}$. The implemented value exceeds $C_{DC,\text{min}}$ to account for tolerance, ageing, and operation at both 50 Hz and 60 Hz.

Each flying capacitor C_{fc} must support its nominal voltage step and a specified peak to peak ripple Δv_{fc} (Modeer, Barth, Lei & Pilawa-Podgurski, 2016). Assuming the capacitor carries the ac component of the phase current $I_{\text{ac,pk}}$ and commutates at an effective frequency $n_c f_{\text{sw}}$, a conservative sizing rule is

$$C_{fc,\text{min}} \;\gtrsim\; \frac{I_{\text{ac,pk}}}{n_c\,f_{\text{sw}}\,\Delta v_{fc}}. \tag{2.3}$$

Box film capacitors with low ESR, low ESL, and high rms current handling capability are selected for this prototype.

2.4 Control Interface Sensor Board

The control interface board, shown in Fig. 2.5, provides the analog front end between the high voltage power stage and the digital controller. It implements all current and voltage measurements required by the control loops and by the hardware protection functions; the measurement signals and sensor types are summarized in Table 2.3. The board is powered from a 12 V auxiliary input that feeds local regulators to generate the 5 V and 3.3 V logic rails, while precision shunt references provide low noise 1.5 V and 3.0 V rails for sensor offsets and comparator thresholds. Integration with the TMS320F28379D controller follows the LaunchPad BoosterPack header layout. A dedicated PWM header routes PWM1A/B to PWM6A/B through level shifted buffers to the gate driver modules, and separate digital lines read the overcurrent detection signal and can disable PWM via a buffer IC.

Table 2.3 Measurements implemented on the control interface board

Variable	Measurement range	Sensor type
Grid / inductor current i_L	±20 A	TMR contact sensor (CT426)
Grid voltage v_G	±680 V	Resistor divider + isolation amplifier
Dc-link voltage V_{DC}	0 to 680 V	Resistor divider + isolation amplifier
FC voltages $V_{C1}...V_{C3}$	V_{dc}/4 steps	Resistor divider + isolation amplifier
Load current I_{DC}	0 to 20 A	TMR contact sensor (CT426)

2.4.1 Voltage sensing

Grid voltage v_g, dc bus voltage V_{DC}, and the flying-capacitor voltages V_{C1} to V_{C3} are measured using resistor dividers that feed integrated DC/DC isolated voltage-sense amplifiers followed by differential-to-single-ended post amplifiers, as shown in Fig. 2.6. The primary resistor dividers scale the high-voltage nodes into the ±1 V input range of the AMC3330 (Instruments, 2025) while keeping the worst-case overvoltage below the clipping level of the isolation amplifier.

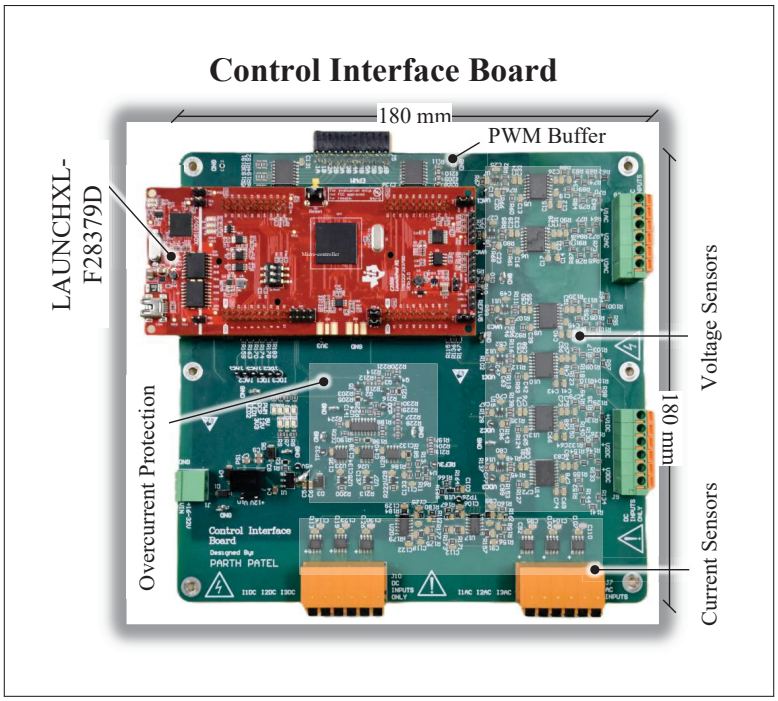


Figure 2.5 Control interface board integrating the LAUNCHXL-F28379D controller, PWM buffer stage, isolated voltage and current sensing channels, and hardware overcurrent protection circuitry

For dc quantities (bus and flying-capacitor voltages) the TLV9001 stages are referenced to ground, so that the 0–3.0 V ADC range directly represents the sensed voltage. For ac grid sensing, the same chain adds a precision 1.5 V reference at the summing node of the TLV9001, shifting the signal so that the bipolar grid voltage is mapped symmetrically around midscale in the ADC domain and its polarity can be reconstructed in software.

All voltage channels include a simple RC anti-alias filter placed close to the ADC pins; the implemented resistor and capacitor values in Fig. 2.6 correspond to a first-order cutoff frequency of approximately 23 kHz. This is well above the outer-loop bandwidths, but sufficiently below the ADC Nyquist frequency to attenuate switching spikes and high-frequency noise.

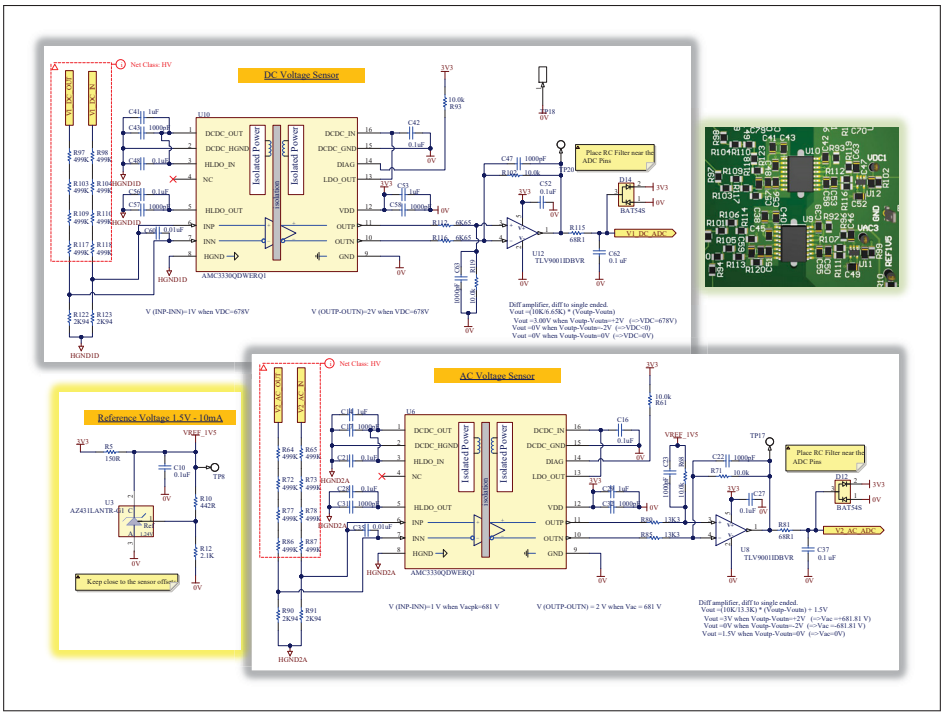


Figure 2.6 Voltage sensing implementation using isolated AMC3330 amplifiers

2.4.2 Current sensing

The ac inductor current and the dc output current are measured using CT426 tunnel magnetoresistance (TMR) current sensors (Allegro MicroSystems, 2024), which provide galvanic isolation, wide bandwidth, and less than 1% full scale error in a compact package. Figure 2.7 shows the signal chain for both dc and ac current channels. The TMR sensors generate a ground referenced voltage proportional to the primary current with a nominal offset of 0.65 V or 1.65 V; this signal is conditioned by an OPA4340 stage that sets the gain and, for the ac channel, adds the required offset so that the bipolar ac current is mapped into the unipolar 0–3.0 V ADC range.

Each channel includes an RC anti alias filter placed at the ADC pin together with BAT54S clamp diodes. In the ac path the filter components correspond to a first order cutoff of approximately 23 kHz, while in the dc path the effective cutoff is approximately 150 Hz. These values are well above the respective control loop bandwidths but low enough to attenuate switching noise from the power stage.

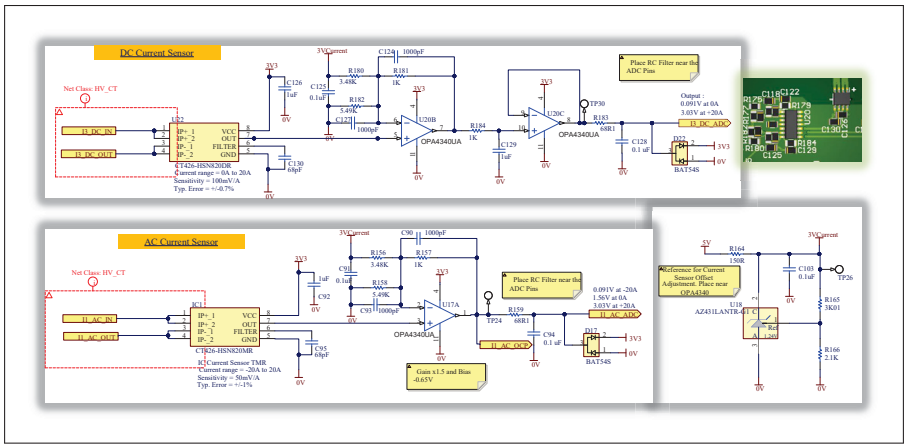


Figure 2.7 Current sensing implementation using TMR contact type current sensor and analog signal chain for signal conditioning

2.4.3 Hardware protections

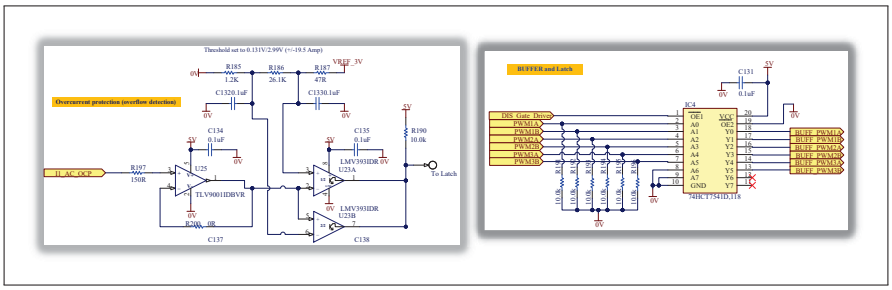


Figure 2.8 Overcurrent protection and PWM interface circuitry with PWM disable input

Hardware overcurrent protection and action via PWM disable are implemented directly on the control interface board, as shown in Fig. 2.8. Each AC current channel feeds a dual LMV393 comparator configured as a window comparator around the nominal zero current offset. A resistor ladder referenced to the 3.0 V rail sets the upper and lower trip voltages, corresponding to current limits $I_{\mathrm{OCP,pos}} \approx +19.5$ A, $I_{\mathrm{OCP,neg}} \approx -19.5$ A.When either threshold is exceeded, the comparator output drives a SR latch. The latched fault state asserts the protection signal, turns on the dedicated fault LED, and, through an OR stage, drives the disable gate driver line high to disable all gate driver inputs. The latch can be cleared only when the microcontroller resets the protection.

PWM1A/B to PWM6A/B from the TMS320F28379D are routed through a 74ACT541 buffer, which also accepts the disable PWM signal so that a latched hardware fault forces all buffered PWM outputs low irrespective of firmware state. The propagation from current threshold crossing to PWM disable is therefore fully hardware bounded, with no dependence on interrupt latency or software execution.

2.5 Digital Control Derivation and Implementation

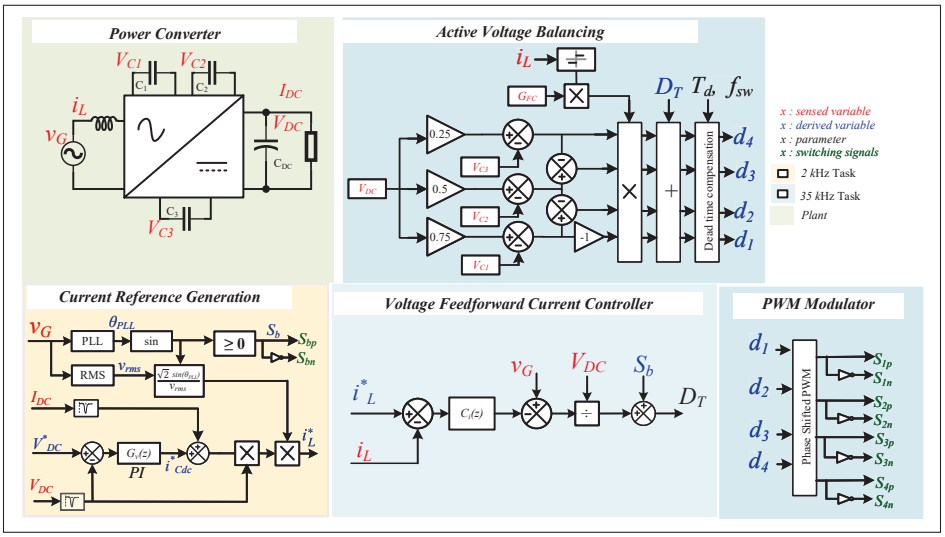


Figure 2.9 Overall digital control architecture of the TP-5L-FCML PFC prototype with inner current loop, outer dc-link voltage loop with load feedforward, flying-capacitor balancing, dead-time compensation, and PLL-based grid synchronization

2.5.1 Control architecture and modeling assumptions

The control structure in Fig. 2.9 employs an inner current loop with input-voltage feedforward and an outer dc-link voltage loop with load-current feedforward. The inner loop regulates the inductor current i_L to track a sinusoidal reference in phase with the rectified grid voltage. The outer loop regulates the dc-link voltage V_{DC} by adjusting the amplitude of the current reference. A voltage feedforward term attenuates the disturbance path from the rectified input to the current dynamics. This multiloop structure is consistent with prior totem-pole bridgeless PFC implementations and enables bandwidth separation such that the inner loop can be approximated

as an ideal current source when synthesizing the outer loop(Chu, Tse, Wong & Tan, 2009; Chen & Sun, 2004; Qin *et al.*, 2019).

The following derivation uses the sign conventions of Fig. 2.3. All node voltages are referred to the negative dc rail. The dc-link magnitude is $V_{DC} > 0$; the grid voltage is $v_G(t)$; the inductor current $i_L(t)$ is defined positive from node B to node A through L_G. The low-frequency totem-pole leg fixes v_B through a polarity flag S_b, with $S_b = 0$ giving $v_B = 0$ and $S_b = 1$ giving $v_B = V_{DC}$. Duty $D_T \in [0, 1]$ is defined for the top high-frequency device stack; the complementary bottom devices include a fixed dead time.

2.5.2 Inner current loop design

2.5.2.1 Plant for the current loop

The averaged high-frequency leg voltage applied to the inductor is

$$\overline{v}_{AB} = \overline{v}_A - \overline{v}_B = (D_T - S_b)\, V_{DC}. \tag{2.4}$$

The inductor dynamic is therefore

$$L_G\, \dot{i}_L = v_G - \overline{v}_{AB} = v_G - (D_T - S_b)\, V_{DC}. \tag{2.5}$$

A full analytic feedforward (Chen & Sun, 2004) based on a sinusoidal reference $i_L^\star = \hat{I} \sin\theta$ and desired inductor voltage $v_L^\star = L_G \frac{di_L^\star}{dt}$ would give

$$D_T^{\mathrm{ff}} = \frac{v_G - v_L^\star}{V_{DC}} + S_b. \tag{2.6}$$

In this prototype a simpler partial feedforward that cancels only the grid term and low-frequency polarity is used,

$$D_T^{\mathrm{ff}} = \frac{v_G}{V_{DC}} + S_b, \tag{2.7}$$

so the inductor dynamics seen by the current controller remain first order and independent of v_G and V_{DC}.

Let the controller output be an inductor-voltage command u (volts), realized through the duty perturbation

$$D_T = D_T^{\mathrm{ff}} - \frac{u}{V_{DC}} \qquad \Longrightarrow \qquad \widetilde{D}_T = -\frac{\widetilde{u}}{V_{DC}}, \tag{2.8}$$

where $\widetilde{x}$ denote small-signal quantities. Substituting (2.7) and (2.8) into (2.5) yields

$$\begin{aligned} L_G\, \dot{i}_L &= v_G - \Big(D_T^{\mathrm{ff}} - \frac{u}{V_{DC}} - S_b\Big)V_{DC} \\ &= v_G - \Big(\frac{v_G}{V_{DC}} + S_b - \frac{u}{V_{DC}} - S_b\Big)V_{DC} \\ &= v_G - (v_G - u) = u. \end{aligned} \tag{2.9}$$

The plant seen by the compensator (including an effective delay $T_{d,i}$ that aggregates PWM, sampling, and computation) is thus approximated as

$$G_{iu}(s) = \frac{\widetilde{i}_L(s)}{\widetilde{u}(s)} = \frac{1}{L_G\, s}\, e^{-sT_{d,i}}. \tag{2.10}$$

The corresponding discrete-time model used for tuning, with sample period T_s and integer delay of n_d samples, is

$$G_{iu}(z) \approx \frac{T_s\, z^{-1}}{L_G\,(1 - z^{-1})}\, z^{-n_d}. \tag{2.11}$$

Equations (2.7)–(2.11) define the intended architecture: the feedforward fixes the operating point by cancelling the instantaneous grid voltage, and the controller output u owns the inductor voltage and absorbs nonidealities, delays, and modeling errors.

Because the flying-capacitor value is relatively small and its balancing control is separated from the current loop (Iyer, Petric, Bayliss, Brooks & Pilawa-Podgurski, 2023; Qin *et al.*, 2018), the plant behavior in the relevant bandwidth closely matches that of a conventional boost PFC stage. The parameters of (2.10) and (2.11) are verified against frequency-response analysis (FRA)

in simulation and on the prototype by injecting a small perturbation on u and measuring the resulting response of i_L. The FRA simulation can yield accurate results when parasitics are modelled correctly and also provides an accurate estimate of the aggregate delay caused by the PWM modulator, sensing chain, and computational latency.

2.5.2.2 Type-II compensator design and discrete realization

The continuous-time current-loop compensator is chosen as a Type-II structure

$$C_i(s) = K_i \frac{1 + s/\omega_z}{s\,(1 + s/\omega_p)}, \tag{2.12}$$

with zero ω_z and high-frequency pole ω_p providing phase lift near crossover and attenuation of switching ripple. For center-aligned PWM at $f_{\mathrm{sw}} = 65$ kHz and sampling rate of $f_{\mathrm{sw}}/2 = 32.5$ kHz, the design targets a current-loop bandwidth $f_{ci} \in [1.8, 3.2]$ kHz and a phase margin close to 60° under the worst-case delay $T_{d,i}$.

A practical choice is

$$\omega_z \approx \frac{\omega_{ci}}{3}, \qquad \omega_p \in [4, 8]\omega_{ci}, \tag{2.13}$$

where $\omega_{ci} = 2\pi f_{ci}$. The proportional gain K_i is then set from the unity-gain condition at crossover,

$$|C_i(j\omega_{ci})\, G_{iu}(j\omega_{ci})| = 1, \tag{2.14}$$

with the exponential delay term in (2.10) included in the phase of $G_{iu}(j\omega)$.

Discretization employs the Tustin mapping with prewarping at $\omega_c = \omega_{ci}$, giving the second-order IIR form

$$C_i(z) = \frac{b_0 + b_1 z^{-1} + b_2 z^{-2}}{1 + a_1 z^{-1} + a_2 z^{-2}}. \tag{2.15}$$

A Direct-Form II transposed realization is adopted in firmware. With internal states $s_1[k]$ and $s_2[k]$, error $e[k] = i_L^\star[k] - i_L[k]$, and output $u[k]$ (volts), the update equations are

$$\begin{aligned} u[k] &= b_0\, e[k] + s_1[k], \\ s_1[k+1] &= b_1\, e[k] - a_1\, u[k] + s_2[k], \\ s_2[k+1] &= b_2\, e[k] - a_2\, u[k]. \end{aligned} \tag{2.16}$$

The relation (2.8) fixes the controller-to-actuator sign through $\partial v_L/\partial D_T = -V_{DC}$. The final discrete coefficients $(b_0, b_1, b_2, a_1, a_2)$ are programmed in the microcontroller and verified by frequency-response measurements. The resulting current-loop gain and phase are shown in Fig. 2.10, which compares the uncompensated plant and the compensated loop.

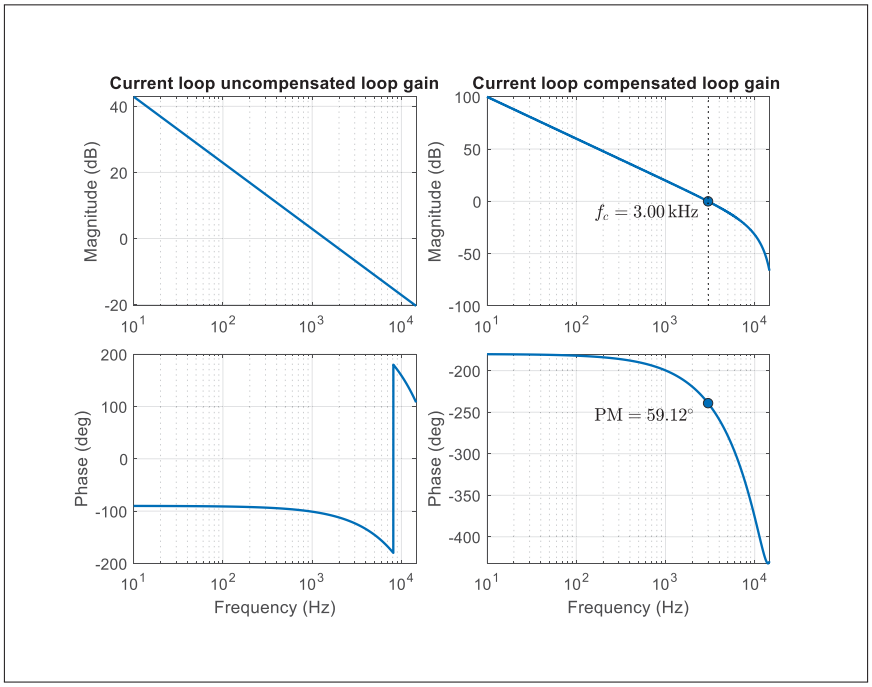


Figure 2.10 Measured current-loop frequency response: uncompensated plant gain (left) and compensated loop gain with the Type-II controller (right)

2.5.3 Duty manipulation and Modulation

2.5.3.1 Active flying-capacitor voltage balancing

Consider an FCML leg with n_c high-frequency switch pairs (here $n_c = 4$) and $n_c - 1$ flying capacitors, yielding $n_c + 1 = 5$ output levels. Let D_T denote the common duty delivered by the current loop and feedforward, and let Δd_m be a small balancing trim applied to the mth pair whose carrier is phase-shifted relative to a common reference (Khazraei, Sepahvand, Corzine & Ferdowsi, 2012).

Low-pass filtered flying-capacitor voltage errors are defined as

$$\varepsilon_m = V_{C_m} - \frac{m}{n_c} V_{DC}, \qquad m = 1, \ldots, n_c - 1.$$

A simple adjacent-pair balancing law chooses preliminary trims

$$\Delta d_{m+1} = G_{FC}\ \mathrm{sgn}(i_L)\,(\varepsilon_m - \varepsilon_{m+1}), \qquad \Delta d_m = G_{FC}\ \mathrm{sgn}(i_L)\,(\varepsilon_{m-1} - \varepsilon_m),$$

with $G_{FC} > 0$ small and boundary placeholders $\varepsilon_0 = \varepsilon_{n_c} = 0$. Over one PWM period T_{sw} the charge increment on capacitor C_m is proportional to the duty difference of adjacent pairs,

$$\Delta Q_{C_m} = (d_{m+1} - d_m)\, i_L\, T_{\mathrm{sw}}, \qquad \Delta V_{C_m} = \frac{\Delta Q_{C_m}}{C_m} = \frac{(d_{m+1} - d_m)\, i_L\, T_{\mathrm{sw}}}{C_m},$$

consistent with the analytical relation $i_{C_m} = (d_{m+1} - d_m)\, i_L$.

To preserve the commanded average leg voltage, the trims are enforced to be zero-sum,

$$\Delta d_m \leftarrow \Delta d_m - \frac{1}{n_c} \sum_{k=1}^{n_c} \Delta d_k, \qquad \sum_{m=1}^{n_c} \Delta d_m = 0,$$

so that the mean $\overline{v}_{AB} = (D_T - S_b)V_{DC}$ remains unchanged. The individual top-device duties presented to the unipolar symmetric ePWM timers are

$$d_m^+ = \mathrm{clip}(D_T + \Delta d_m, D_{\min}, D_{\max}), \qquad d_m^- = 1 - d_m^+,$$

with configured dead time and additional small corrections described in Section 2.5.3.2. Because the carriers are phase-shifted, these per-pair duty skews steer charge between adjacent flying capacitors without perturbing the average leg duty, yielding fast and scalable active balancing.

2.5.3.2 Dead-time compensation

Dead time prevents shoot-through but shortens the effective on-time of the device that conducts after each edge (Jeong & Park, 1991). With center-aligned PWM, the average duty error per complementary pair is well approximated by

$$\Delta d_{\mathrm{dt}} \approx \gamma\, \sigma, \qquad \gamma \triangleq \frac{t_{\mathrm{dt}}}{T_s}, \quad \sigma \triangleq \mathrm{sgn}(i_L), \tag{2.17}$$

where t_{dt} is the configured dead time and T_s is the switching period. A feedforward correction adds $+\Delta d_{\mathrm{dt}}$ to the top device when $\sigma > 0$ and subtracts it when $\sigma < 0$.

In the implemented modulation, the per-pair dead-time correction is summed with the balancing trim before clipping,

$$d_m \leftarrow \mathrm{clip}\left(D_T + \Delta d_m + \Delta d_{\mathrm{dt}},\, d_{\min},\, d_{\max}\right), \qquad |\Delta d_{\mathrm{dt}}| \ll d_{\min}, \tag{2.18}$$

so that modulation linearity is preserved.

For continuous-conduction operation, an adaptive estimate of the optimal dead time that removes the switch output-capacitance charge without incurring body-diode conduction is

$$t_{\mathrm{dt}}^{\star} \approx \frac{2\, C_{\mathrm{oss}}\, V_{\mathrm{out}}}{i_{L,\mathrm{peak}}}, \tag{2.19}$$

and the corresponding duty correction in sample k is $\hat{\gamma}_k = t_{\mathrm{dt}}^{\star}(i_L[k])/T_s$.

2.5.4 Phase-shifted PWM and synchronization

The FCML leg uses symmetric up–down carriers with center-aligned PWM on each ePWM time base. With n_c high-frequency pairs, evenly spaced phase offsets

$$\phi_m = (m-1)\,\frac{\pi}{n_c}, \qquad m = 1, \ldots, n_c,$$

are assigned to the carriers to increase the effective switching frequency seen by L_G and to support natural flying-capacitor balancing.

All ePWMs are synchronized to a common master. ADC sampling is locked to a fixed carrier position (here center of the carrier) so that the discrete plant and delay of the current loop remain invariant across operating points. Around the grid-voltage zero crossing, the high-frequency leg and low-frequency totem-pole devices are briefly disabled near the grid-voltage zero crossing to reduce current distortion caused by the abrupt duty-cycle transition when the totem-pole polarity changes (Sun, 2017).

2.5.5 Outer voltage loop with load feedforward

2.5.5.1 PLL and current-reference generation

A SOGI-PLL runs at the inner current-loop rate and provides $\theta_{\mathrm{PLL}}[k]$ and $\sin\theta_{\mathrm{PLL}}[k]$. The sign of $\sin\theta_{\mathrm{PLL}}[k]$ sets the low-frequency totem-pole polarity S_b. The outer loop executes at $f_v = 2$ kHz with period $T_v = 500\ \mu$s. To remove the deterministic $2\omega_G$ component on the dc side, the bus-voltage and dc-current measurements are prefiltered by narrow notches at $2\omega_G$, producing $\widetilde{V}_{DC}[k]$ and $\widetilde{I}_{DC}[k]$. An RMS estimator yields $v_{\mathrm{rms,eff}}[k]$ and an estimate of the grid peak $\hat{V}_g[k] = \sqrt{2}\,v_{\mathrm{rms,eff}}[k]$.

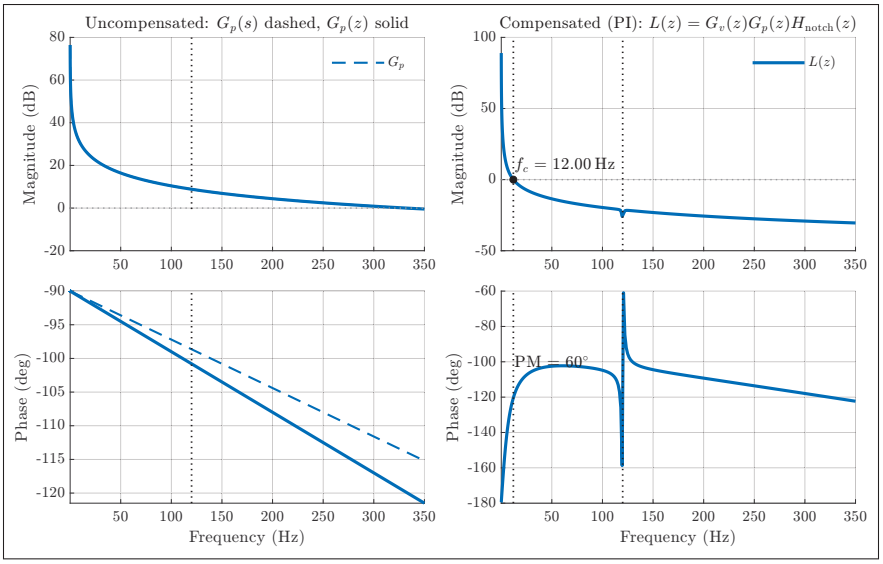


Figure 2.11 Bode plots of the outer voltage loop for the TP-5L-FCML PFC prototype. Left: uncompensated plant $G_p(s)$ (dashed) and sampled plant $G_p(z)$ (solid). Right: compensated loop $L(z) = G_v(z)G_p(z)H_{\text{notch}}(z)$ with crossover frequency $f_c \approx 12$ Hz and phase margin of approximately 60°

The outer loop operates in the current-amplitude domain using a common gain that multiplies both the load feedforward and the voltage-compensator output:

$$k_\Sigma[k] \triangleq \frac{\sqrt{2}\,\widetilde{V}_{DC}[k]}{v_{\text{rms,eff}}[k]}, \qquad \hat{I}_\Sigma[k] = k_\Sigma[k]\big(\widetilde{I}_{DC}[k] + i^*_{\text{cdc}}[k]\big), \tag{2.20}$$

so that the instantaneous current command is

$$\hat{I}^{\text{sat}}_\Sigma[k] = \text{sat}\left(\hat{I}_\Sigma[k], 0, \hat{I}_{\max}\right), \qquad i^\star_L[k] = \hat{I}^{\text{sat}}_\Sigma[k]\ \sin\theta_{\text{PLL}}[k]. \tag{2.21}$$

The bus-voltage setpoint $V^*_{DC}[k]$ is slew-limited from the measured value toward the nominal reference to prevent abrupt excursions in $\hat{I}_\Sigma[k]$ during start-up and line or load steps.

The outer compensator follows the parallel PI with clamped integrator used in firmware, acting in amperes on the dc-voltage error:

$$\begin{aligned} e[k] &= V_{DC}^{*}[k] - \widetilde{V}_{DC}[k], \\ u_P[k] &= K_p\, e[k], \qquad x_I[k] = x_I[k-1] + K_i\, e[k]\, \sigma[k], \\ v[k] &= u_P[k] + x_I[k], \qquad i_{\mathrm{cdc}}^{*}[k] = \mathrm{clip}(v[k], U_{\min}, U_{\max}), \\ \sigma[k] &= \begin{cases} 1, & v[k] = i_{\mathrm{cdc}}^{*}[k] \text{ (unsaturated)}, \\ 0, & \text{otherwise.} \end{cases} \end{aligned} \tag{2.22}$$

The integrator input is frozen whenever saturation is active, providing simple anti-windup. No branch other than (2.20) carries $\hat{V}_g^{-1}$; the PI itself is independent of $v_{\mathrm{rms,eff}}$ and does not require gain scheduling.

2.5.5.2 Voltage compensator design

The dc-link energy $E = \frac{1}{2} C_{DC} V_{DC}^2$ implies $C_{DC} V_{DC}\, \dot{V}_{DC} = P_{\mathrm{in}} - P_{\mathrm{load}}$. Under unity power factor, the averaged input power is $\overline{P}_{\mathrm{in}} = \frac{\hat{V}_g}{2}\, \hat{I}$. Linearizing about $(\bar{V}_{DC}, \bar{\hat{I}})$ with the current amplitude as actuator gives

$$\frac{\widetilde{V}_{DC}(s)}{\widetilde{\hat{I}}(s)} = \frac{\hat{V}_g}{2\, C_{DC}\, \bar{V}_{DC}}\, \frac{1}{s}. \tag{2.23}$$

In the realized path the PI produces a dc-side current command i_{cdc}^{*}, and both i_{cdc}^{*} and $\widetilde{I}_{DC}$ traverse the same amplitude gain k_Σ of (2.20). Consequently, the small-signal map from the PI output to the bus voltage simplifies to

$$\frac{\widetilde{V}_{DC}(s)}{\widetilde{i}_{\mathrm{cdc}}^{*}(s)} = \frac{1}{C_{DC}}\, \frac{1}{s}, \tag{2.24}$$

so the outer-loop plant seen by the PI is a constant-gain integrator, independent of V_g and operating point. A single tuning therefore covers the full universal-ac range.

Table 2.4 Summary of digital control parameters and measured closed-loop characteristics

Loop	Parameters	Measured characteristics
Current loop (Type-II)	$b_0 = 3.029123766$, $b_1 = 0.4199421374$, $b_2 = -2.609181629$, $a_1 = -0.4256768872$, $a_2 = -0.5743231128$	PM $\approx 59.1^\circ$, $f_c \approx 3.0$ kHz
Voltage loop (PI)	$K_p = 3.15 \times 10^{-2}$, $K_i = 1.33 \times 10^{-4}$	PM $\approx 60^\circ$, $f_c \approx 12$ Hz

A continuous-time PI $C_v(s) = K_p^c + \frac{K_i^c}{s}$ with zero $\omega_z = K_i^c/K_p^c$ is selected to meet a closed-loop bandwidth $\omega_{vo}/2\pi \in [8, 15]$ Hz $\ll f_{\text{line}}$, while ensuring adequate phase margin by placing $\omega_z = \omega_{vo}/m$ with $m \in [4, 8]$. With the unit-gain integrator in (2.24), unity loop gain at ω_{vo} gives

$$K_p^c = \frac{\omega_{vo}\, C_{DC}}{\sqrt{1 + (\omega_z/\omega_{vo})^2}}, \qquad K_i^c = K_p^c\, \omega_z. \tag{2.25}$$

Because the implemented recursion integrates explicitly as $x_I[k] = x_I[k-1] + K_i\, e[k]\sigma[k]$ at $T_v = 500\ \mu$s, the discrete coefficients follow directly:

$$K_p = K_p^c, \qquad K_i = K_i^c\, T_v, \tag{2.26}$$

and are used in (2.22). With the notch-filtered measurements, the common gain (2.20), and the slew-limited $V_{DC}^*[k]$, the closed loop exhibits the targeted first-order response while the compensator remains independent of $v_{\text{rms,eff}}$.

Table 2.4 summarizes the implemented discrete current- and voltage-loop controller parameters and the corresponding measured loop characteristics extracted from Figs. 2.10 and 2.11.

2.6 Simulation Results

The tuned current loop, outer voltage loop, and flying-capacitor balancing algorithm are first evaluated in time-domain simulations. The objective is to verify that the linear controller meets the transient specifications while preserving current quality and FC voltage balance over large load and reference steps.

Figure 2.12 illustrates the response to a load step from light load to the rated dc power. The dc-link voltage excursion remains smaller than the steady-state ripple, and V_{DC} settles back to its nominal value in less than one line cycle. Figure 2.13 shows the response to a dc-link reference change from 400 V to 350 V and back to 400 V, confirming that the controller tracks the new reference with approximately 40 ms settling time while maintaining sinusoidal input current and balanced flying-capacitor voltages.

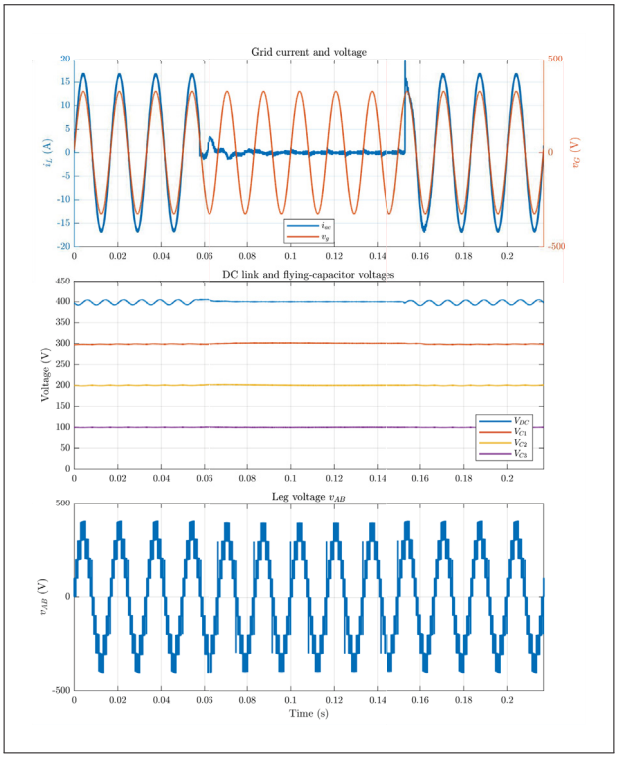


Figure 2.12 Simulated load-step response. The dc load is stepped to the rated value. Top: grid voltage v_g and inductor current i_{ac} remain well aligned and nearly sinusoidal. Middle: dc-link voltage V_{DC} and flying-capacitor voltages V_{C1}–V_{C3} stay balanced; the transient overshoot and undershoot of V_{DC} are smaller than the steady-state ripple, and V_{DC} returns to its nominal value in less than one line cycle ($\approx$ 16 ms). Bottom: corresponding five-level leg voltage v_{AB} waveform

2.7 Experimental Results

The hardware prototype was tested to verify its performance. Steady-state performance at half and rated load power is summarized in Fig. 2.14. Input current remains nearly sinusoidal and in

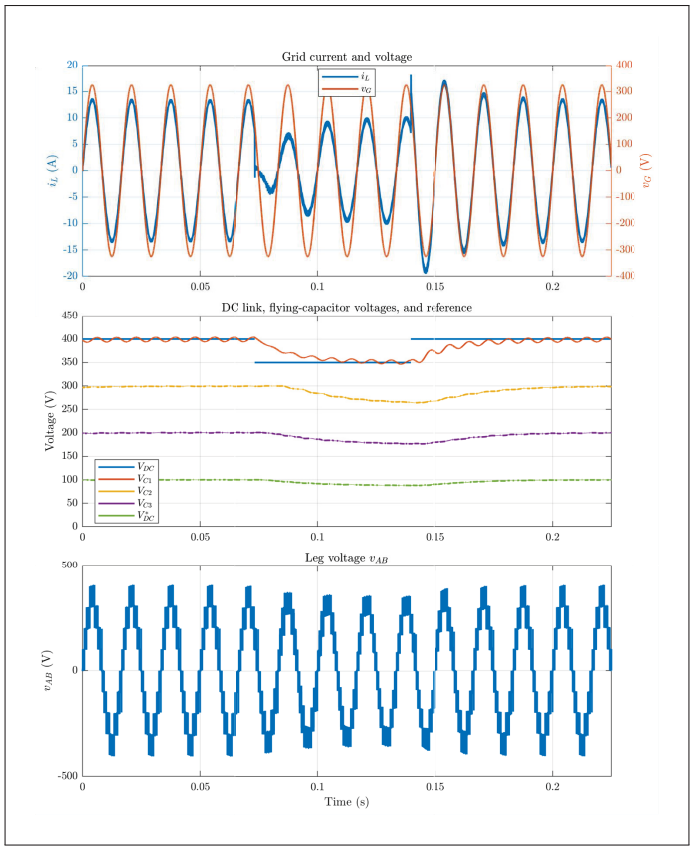


Figure 2.13 Simulation of a dc-link voltage reference step from 400 V to 350 V and back to 400 V. The current i_L remains sinusoidal and in phase with v_g, flying-capacitor voltages stay balanced, and V_{DC} settles to each new reference in approximately 40 ms

phase with the grid voltage at both 1.23 kW and 2.22 kW, with measured power factors above 0.996, input current THD below 4.5 % at mid power and about 1 % near rated power, and efficiencies close to 98 % at 230 Vrms. Low-power operation at 150 W is shown in Fig. (2.15) for both 240 Vrms and 120 Vrms input, confirming that the current loop and FC balancing remain effective over a wide load and line range.

Dynamic behavior is illustrated in Fig. 2.16. A controlled ramp of the dc-link voltage demonstrates stable startup and shutdown with balanced flying-capacitor voltages and no loss of current quality, indicating that the tuned compensators are insensitive to operating point and depend primarily on the design parameters. Finally, Fig. 2.17 presents a representative thermal image

under sustained operation, showing moderate temperature rise on the inductor and heatsink and confirming that the prototype operates within safe thermal limits at the tested power levels.

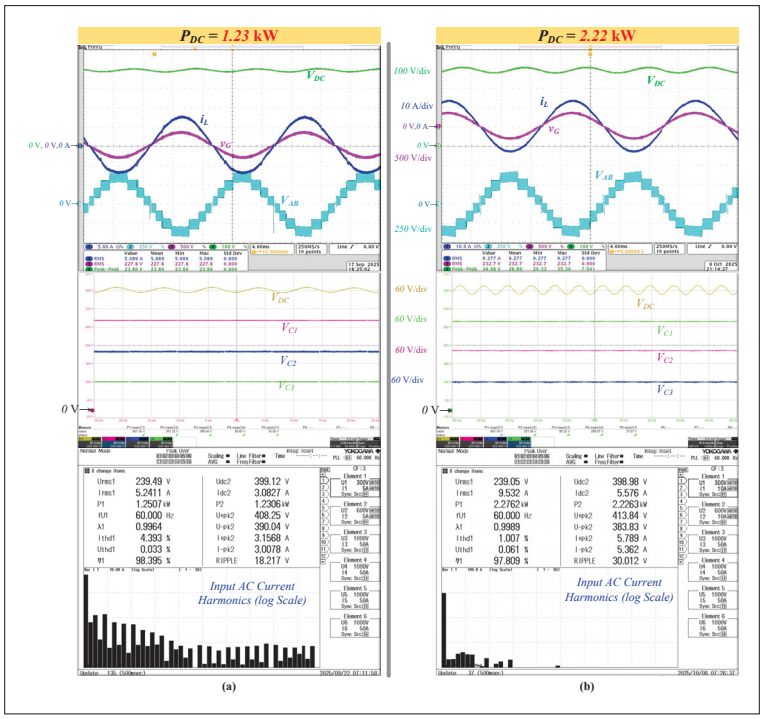


Figure 2.14 Experimental steady-state waveforms and power analyzer results for the TP-5L-FCML PFC prototype at 230 V_{rms} input and 400 V dc-link. (a) $P_{DC} \approx 1.23$ kW: power factor $\lambda \approx 0.996$, input current THD $\approx 4.4\%$, efficiency $\eta \approx 98.4\%$. (b) $P_{DC} \approx 2.22$ kW: power factor $\lambda \approx 0.999$, input current THD $\approx 1.0\%$, efficiency $\eta \approx 97.8\%$

2.8 Conclusion

This chapter presented the hardware realization and real-time linear control design and implementation of a 2.5 kW TP-5L-FCML totem-pole PFC prototype. The power stage and its partitioning into a high-density FCML leg, dc-link, and grid filter were described, along with a dedicated control interface board that provides isolated voltage and current measurements, precision reference rails, and fast hardware overcurrent protection. A TMS320F28379D-based digital controller executes a Type-II inner current loop with input-voltage feedforward, an outer dc-link voltage PI loop with load feedforward, active flying-capacitor voltage balancing, dead-time compensation, and PLL-based synchronization; all control laws were derived from

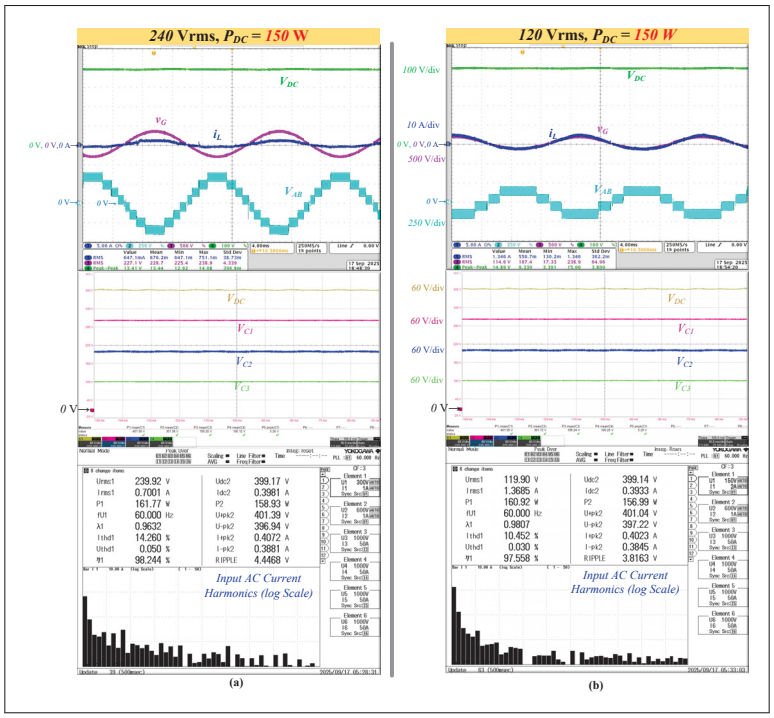


Figure 2.15 Experimental low-power operation of the TP-5L-FCML PFC prototype at $P_{DC} \approx 150$ W and $V_{DC} \approx 400$ V. (a) 240 V_{rms} input: power factor $\lambda \approx 0.963$, input current THD $\approx 14.3\%$, efficiency $\eta \approx 98.2\%$. (b) 120 V_{rms} input: $\lambda \approx 0.981$, input current THD $\approx 10.5\%$, efficiency $\eta \approx 97.6\%$

explicit averaged models and mapped to discrete-time implementations suitable for model-based code generation.

Time-domain simulations confirmed that the controller meets the transient requirements under large load and dc-link reference steps, with dc-link excursions bounded by the steady-state ripple and settling times below one line cycle for load changes and around 40 ms for reference steps. Experimental results at 230 V rms input and 400 V dc-link demonstrated near-unity power factor, input current THD down to approximately 1%, and peak efficiencies above 98 %, while low-power tests and startup ramps verified stable operation and balanced flying-capacitor voltages over a wide operating range with fixed control gains. The resulting hardware and control platform provides a validated baseline for the advanced nonlinear and predictive control strategies investigated in subsequent chapters.

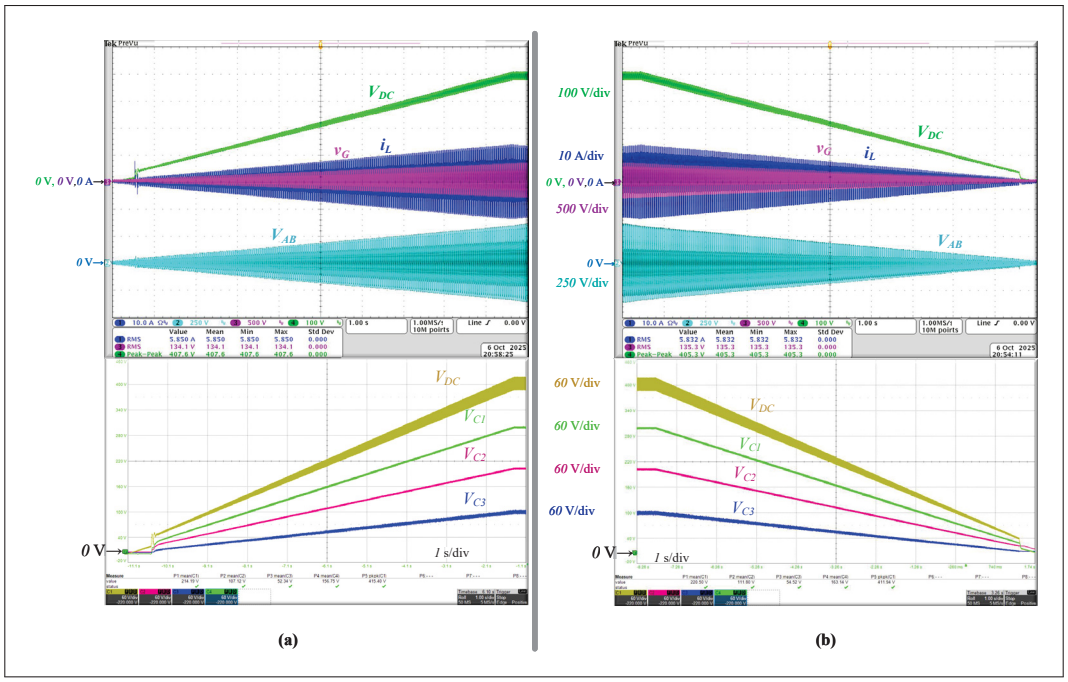


Figure 2.16 Experimental startup and shutdown ramps of the TP-5L-FCML PFC prototype illustrating wide operating-range stability with fixed control gains. (a) Controlled ramp-up of V_{DC} with i_L, v_G, v_{AB}, and flying-capacitor voltages V_{C1}–V_{C3} remaining balanced. (b) Symmetric ramp-down of V_{DC} and V_{C1}–V_{C3} with preserved current quality, confirming that the compensators depend only on design parameters and are effectively independent of the operating point

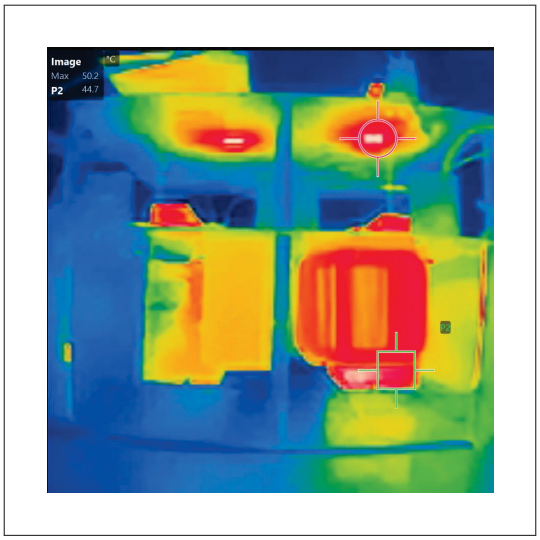


Figure 2.17 Thermal image of the TP-5L-FCML power stage from the side, showing inductor and heatsink temperature distribution under load (hot spots around 50 °C)

CHAPTER 3

OPTIMIZED MODEL PREDICTIVE CONTROL IN SINGLE-PHASE FOUR-LEVEL FLYING CAPACITOR MULTILEVEL CONVERTER FOR BIDIRECTIONAL ON-BOARD CHARGER

This chapter investigates a single-phase bidirectional on-board charger (OBC) in which the ac–dc interface is realized by a totem-pole four-level flying-capacitor multilevel (4L–FCML) power-factor-correction (PFC) stage. The 4L–FCML converter serves as the grid interface and is required to operate in both rectifier and inverter modes over the full set of vehicle-to-everything (V2X) operating points, including grid-to-vehicle (G2V), vehicle-to-grid (V2G), grid-connected vehicle-to-home/vehicle-to-vehicle (V2H/V2V), and standalone vehicle-to-load/vehicle-to-home (V2L/V2H). A unified control architecture is developed in which a mode-dependent reference-generation layer produces ac current or voltage references from high-level active and reactive power commands, while a common finite-control-set model predictive controller (FCS–MPC) regulates the grid current or ac output voltage and simultaneously balances the flying-capacitor voltages using a single discrete-time prediction model and fixed switching table. The admissible V2X operating region is explicitly characterized in the P–Q plane subject to converter and battery constraints, and an averaged plus exact discrete-time model of the 4L–FCML stage is derived for bidirectional operation. The proposed delay-compensated FCS–MPC employs a two-step prediction horizon, incorporates switching-effort penalties, and exploits an extended switching table with explicit capacitor-charging information to improve prediction accuracy and balancing. Switching-level simulations on a 7 kW, 230 V rms, 60 Hz OBC front end demonstrate compliant grid currents, accurate P/Q regulation in grid-following modes, and robust voltage regulation with linear and non-linear loads in grid-forming modes. Experimental results from a scaled laboratory prototype further confirm the feasibility of the unified control framework.

3.1 Introduction

The proliferation of plug-in electric vehicles (EVs) and the increasing penetration of distributed energy resources have intensified the functional requirements placed on on-board chargers (OBCs). All EVs require an OBC with an ac–dc power-factor-correction (PFC) stage to interface

the single-phase utility grid and the high-voltage battery pack. The PFC converter must ensure compliant ac current waveforms and near-unity power factor while delivering regulated dc power to the downstream dc–dc converter. In parallel, emerging vehicle-to-everything (V2X) applications extend the role of the OBC beyond grid-to-vehicle (G2V) charging to include vehicle-to-grid (V2G), vehicle-to-home (V2H), vehicle-to-load (V2L), and vehicle-to-vehicle (V2V) services, all of which require bidirectional power flow between the battery and the grid (Liu, Chau, Wu & Gao, 2013). In practice, most light-duty EVs employ single-phase AC Level 2 charging equipment operating from 208/240 V ac with rated currents up to 80 A, enabling power levels in the 3.3–19.2 kW range, with 7.2 kW from a 40 A residential circuit being particularly common (of Transportation, 2025). These usage patterns make the single-phase OBC a critical bottleneck for both charging performance and V2X functionality. As of 2022, nearly 80% of public EV charging ports in the U.S. were Level 2 (DOE), 2024).

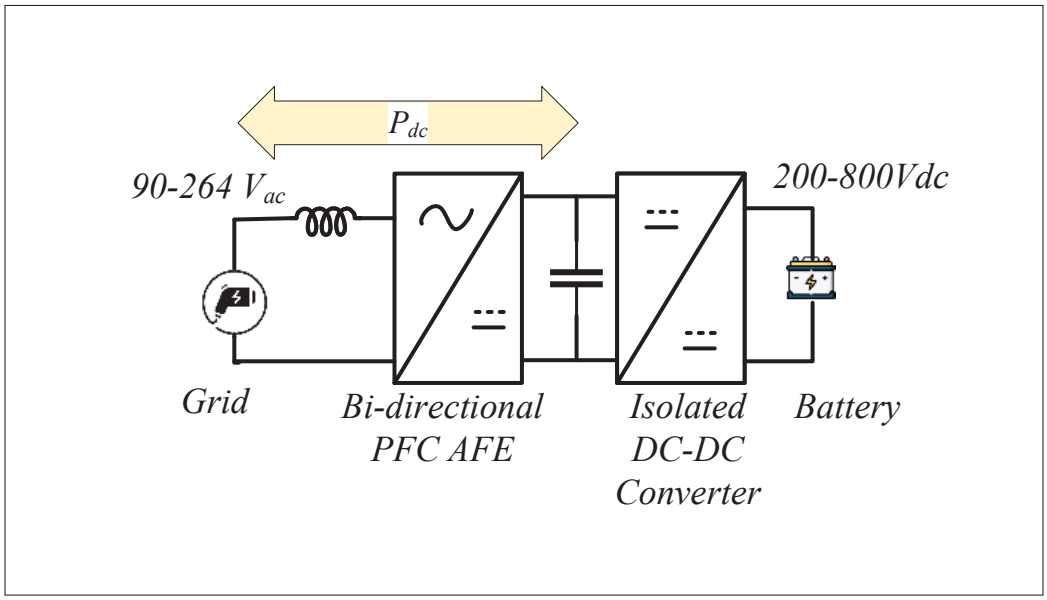


Figure 3.1 Typical on-board charger configuration

Commercial OBCs typically adopt a two-stage architecture in which a front-end single-phase PFC rectifier is cascaded with an isolated dc–dc converter that interfaces the traction battery, as illustrated in Fig. 3.1. The front-end stage is responsible for shaping the grid current and regulating the dc-link voltage, whereas the dc–dc stage controls battery current or voltage.

Various single-phase PFC topologies, including interleaved boost PFC, totem-pole PFC, and multi-phase interleaved PFC, have been deployed at this interface (Gong, Wang & Bhardwaj, 2019; Williamson, Rathore & Musavi, 2015; Instruments, 2024c; Wolfspeed, Inc., 2024; Instruments, 2024a). To increase power density and efficiency, multilevel ac–dc converters have attracted significant attention due to their reduced semiconductor voltage stress, higher effective switching frequency at the ac filter, and lower passive component requirements (Qin *et al.*, 2019; Azurza Anderson *et al.*, 2021). Among these, flying-capacitor multilevel (FCML) structures offer uniform switch-voltage ratings, modular scalability, and efficient capacitor charge/discharge at the switching frequency (Barzegarkhoo, Forouzesh, Lee, Blaabjerg & Siwakoti, 2022; Lei *et al.*, 2017), which is particularly suitable for implementation with fast, low-voltage wide-bandgap devices such as GaN transistors (EPC, 2025).

Despite these advantages, the use of single-phase FCML converters as the sole ac–dc interface of a bidirectional OBC poses several challenges. First, the same hardware must operate as a rectifier and as an inverter over a wide range of operating points associated with the different V2X modes, while respecting current and voltage limits on both ac and dc sides(Kisacikoglu, Kesler & Tolbert, 2015; Dong *et al.*, 2012; Wang, Chen, Li & Chen, 2020b). Second, flying-capacitor voltages must remain balanced under bidirectional power flow, varying grid conditions, and transitions between grid-connected and standalone operation. Third, conventional phase-shifted PWM with linear PI or PR control can struggle to maintain passive capacitor voltage balance, provide fast transient response, and preserve accurate current tracking across all modes (Ye *et al.*, 2022; Kisacikoglu *et al.*, 2015; Dong *et al.*, 2012). These considerations motivate the use of model-based control strategies that can explicitly account for the multilevel switching states and multiple control objectives.

Model predictive control (MPC), and in particular finite-control-set MPC (FCS–MPC), offers a natural framework for such converters (Karamanakos, Liegmann, Geyer & Kennel, 2020; Karamanakos & Geyer, 2020). At each sampling instant, the controller evaluates a cost function over a finite set of candidate switching states using a discrete-time model of the plant and selects the state that minimizes the predicted tracking error and constraint violations. This approach can

directly include grid-current tracking, flying-capacitor voltage regulation, and switching-effort penalties in a single formulation without intermediate modulation stages. However, most reported applications of FCS–MPC to single-phase multilevel converters focus on high-power low-switching-frequency operation or consider only a subset of V2X modes, with control schemes tailored to either rectifier or inverter operation and without a unified treatment of grid-connected and standalone modes.

This chapter addresses these gaps by considering a single-phase bidirectional on-board charger in which the ac–dc interface is realized by a totem-pole four-level flying-capacitor multilevel (4L–FCML) PFC stage. The 4L–FCML converter serves as the only grid interface and operates in both rectifier (G2V) and inverter (V2G/V2H/V2V/V2L) modes. A unified control architecture is developed in which a mode-dependent reference-generation layer produces ac current or voltage references from high-level active and reactive power commands, while a common FCS–MPC algorithm regulates the grid current or ac output voltage and simultaneously balances the flying-capacitor voltages using a single discrete-time prediction model and a fixed set of candidate switching states. The same predictive controller realizes grid-following current control in grid-connected V2X modes and grid-forming voltage control in standalone modes without changing the underlying switching table.

The main contributions of this chapter are as follows. First, a unified description of the V2X operating modes of the single-phase OBC is formulated in terms of ac active and reactive power at the grid interface, together with converter and battery constraints that define the admissible operating region for charging and discharging. Second, an averaged and discrete-time model of the totem-pole 4L–FCML PFC stage is derived for bidirectional operation, explicitly capturing the inductor current and flying-capacitor voltages and providing a common prediction model for all modes. Third, a mode-agnostic FCS–MPC scheme is proposed that employs this model to implement both grid-following current control and grid-forming voltage control using a shared cost-function structure and switching-state set, while enforcing capacitor-voltage balancing and limiting switching effort. Finally, the proposed control framework is validated in simulation

and on a laboratory prototype over representative G2V, V2G, grid-connected V2H/V2V, and standalone V2L operating points.

The remainder of this chapter is organized as follows. Section 3.2 describes the considered V2X operating modes and the corresponding power and current limits of the OBC. Section 3.3 introduces the single-phase totem-pole 4L–FCML converter and its averaged and discrete-time models. Section 3.4 develops the reference-generation schemes for grid-connected and standalone modes. Section 3.5 presents the proposed FCS–MPC formulation for the 4L–FCML stage in both grid-following and grid-forming operation. Section 3.6 reports simulation results, and Section 3.7 presents experimental validation on a hardware prototype. Finally, Section 3.8 concludes the chapter.

3.2 V2X Operating Modes and Limits

This section defines the operating modes of the single-phase bidirectional OBC at the system level and specifies the active and reactive power limits used later for reference generation and control.

3.2.1 Operating Modes

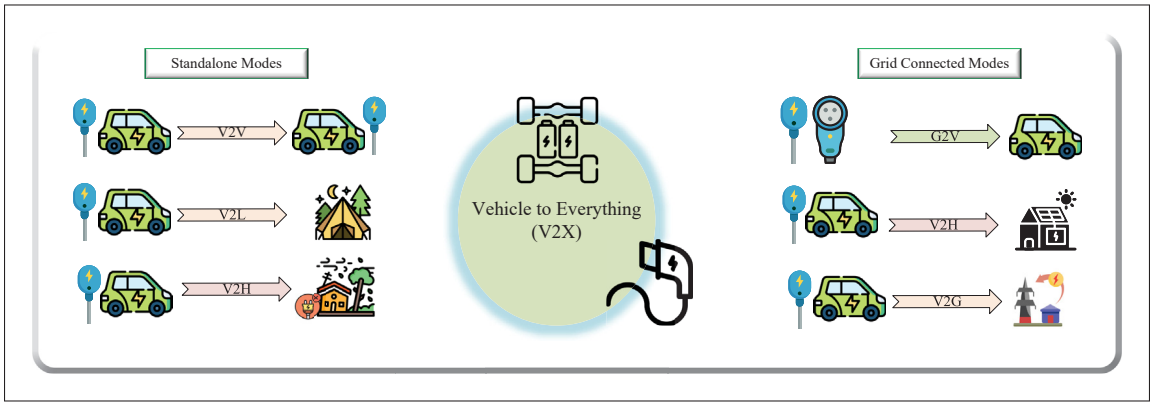


Figure 3.2 V2X operation modes

The OBC PFC stage operates as the ac–dc interface between the utility grid and the traction battery. The V2X modes in Fig. 3.2 are classified in terms of

- grid status: grid-connected vs. standalone,
- power direction: charging ($P > 0$) vs. discharging ($P < 0$),
- ac-side role: grid-following current source vs. grid-forming voltage source.

Table 3.1 summarizes the considered modes. In grid-connected G2V and V2G, and in grid-tied V2H/V2V, the ac–dc stage is synchronized to the grid and controlled as a grid-following converter. The inner loop tracks a sinusoidal current reference derived from active and reactive power commands (P^*, Q^*). In standalone V2L and islanded V2H/V2V, the ac–dc stage is controlled as a grid-forming converter. The inner loop tracks a sinusoidal voltage reference $v_{cf}^*(t)$ with prescribed amplitude and frequency, and the local loads determine the resulting active and reactive power (P_o, Q_o) at the ac port.

Table 3.1 V2X modes, role of the PFC stage, and main control objectives

Mode	Grid status	PFC role	Main control objectives
G2V	Grid-connected, grid-following	Single-phase PFC rectifier	Track commanded active power $P^* \geq 0$ for battery charging. Enforce unity or commanded power factor via Q^*. Regulate dc-link voltage V_{dc} and limit rms and peak grid current.
V2G	Grid-connected, grid-following	Single-phase inverter	Inject commanded active power $P^* \leq 0$ into the grid. Provide reactive power support Q^* within converter current limits. Maintain V_{dc} within the allowable battery window.
V2H	Grid-connected (normal)	Grid-following current-controlled converter	Exchange P and Q with the home grid according to an aggregator or home energy management system, supporting local renewable sources and power quality.
	Standalone islanded	Grid-forming voltage source	Regulate ac bus voltage amplitude and frequency for critical home loads. Track a slow power reference from the dc source while respecting battery state-of-charge (SoC) and dc current limits.
V2V	Grid-connected or islanded microgrid	Either grid-following or grid-forming, depending on the host bus	Transfer energy between vehicles through the ac bus. In grid-connected case the converter behaves as in V2G/V2H. In islanded case it forms or supports the local ac bus similar to standalone V2H.
V2L	Standalone islanded	Grid-forming voltage source	Supply an arbitrary single-phase load directly from the traction battery. Maintain nominal ac voltage and frequency and limit overload currents.

From the perspective of the ac–dc stage, all grid-connected modes share the same structure (current control with (P^*, Q^*)), and all standalone modes share the same structure (voltage control with v_{cf}^*). This unified view is exploited in the control design.

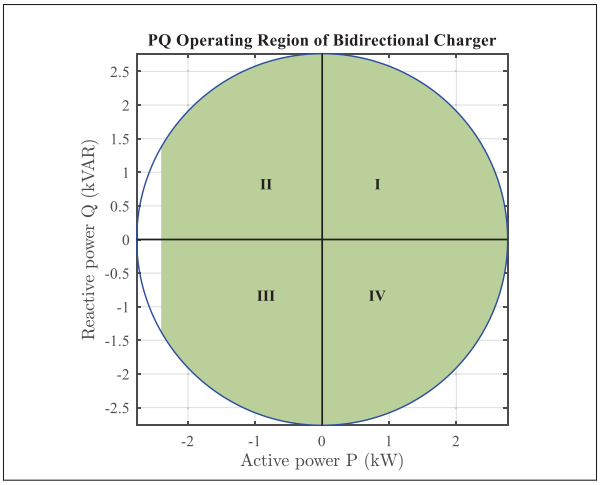


Figure 3.3 Four-quadrant operating region of bidirectional V2X PFC converter

3.2.2 Power and Current Limits

During standalone V2H, V2L, or islanded V2V operation, the PFC stage forms the ac bus from a finite-energy dc source. The continuous discharging capability is therefore limited by:

(i) the maximum rms $I_{g,\mathrm{rms,rated}}$ and peak ac current rating $I_{g,\mathrm{pk}}$ of the AFE, which bounds the maximum admissible apparent power $S_{\max} = V_{g,\mathrm{rms}}\, I_{g,\mathrm{rms,rated}}$, and constrains the (P, Q) operating region,

(ii) the permissible dc current and state of charge (SoC) window of the traction battery,

(iii) the thermal limits of semiconductors and passive components.

The (P, Q) operating region, as shown in Fig. 3.3, is therefore bounded by

$$P^2 + Q^2 \le S_{\max}^2, \tag{3.1}$$

and further restricted by the available dc power $P_{dc,\max} = V_{dc} I_{dc,\max}$. In the standalone V2H/V2L case, the energy management layer must monitor the battery SoC and reduce P^* or shut down discharging when SoC reaches the lower threshold. Short-duration overloads are possible inside

the current limit envelope (3.1), but are constrained by device junction temperature and dc-link capacitor ripple.

For grid-connected modes, battery discharging limits are dynamically set based on state of charge (20–80%), depth of discharge, C-rates, temperature, health metrics, user schedules, and grid demands, using real-time algorithms to minimize degradation while ensuring usability (Liu *et al.*, 2013).

3.3 Four-Level Flying-Capacitor AC-DC Stage and Modeling

This section summarizes the single-phase totem-pole four-level flying-capacitor multilevel (4L–FCML) AC–DC stage and derives the continuous-time and discrete-time models used in the predictive controller. Only the four positive inverter-voltage levels v_{inv} generated by the high-frequency flying-capacitor leg are considered explicitly; the negative half-cycle is obtained by the low-frequency unfolder leg.

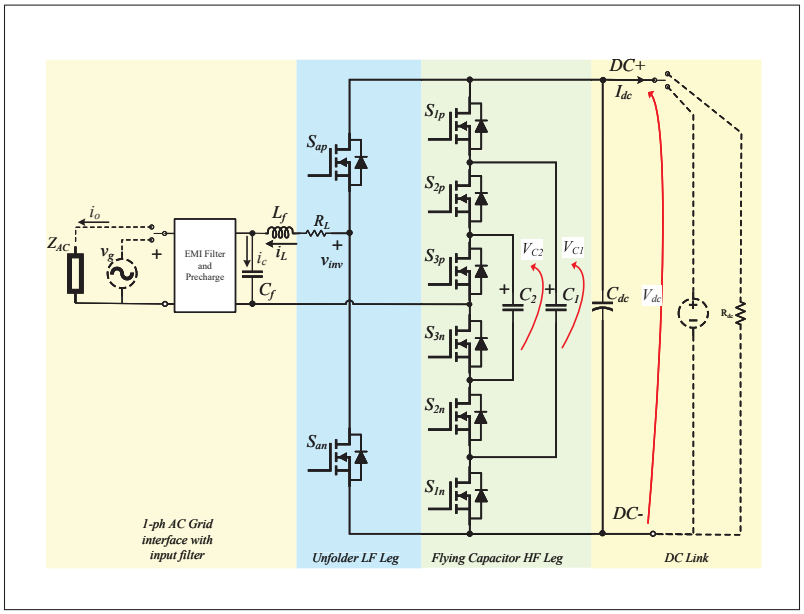


Figure 3.4 Bidirectional single-phase totem-pole four-level FCML topology configuration in OBC PFC stage

3.3.1 OBC Front-End and Topology

Figure 3.4 shows the AC–DC front end of the considered two-stage OBC. The AC port is connected to the single-phase grid through an EMI filter and a series inductor L_f with parasitic resistance R_f. A shunt capacitor C_f is connected at the AC side of the inductor. The node voltage across C_f is denoted $v_{cf}(t)$ and the inductor current is $i_L(t)$, defined positive from the converter towards the AC node. In grid-connected mode the node is tied to the utility grid, so $v_{cf}(t) = v_g(t)$ and the current drawn by the grid is $i_o(t) = i_g(t)$. In standalone mode the node is connected to an AC load Z_{AC} with current $i_o(t)$, which may be linear or non-linear. On the DC side, the front end is connected to the DC-link capacitor C_{dc} of voltage $V_{dc}(t)$. An isolated bidirectional DC–DC converter (not shown) interfaces the traction battery. For grid-to-vehicle (G2V) charging the DC link is represented as a power sink R_{dc}; for discharging modes it is represented as a DC voltage source V_{dc}.

The AC–DC power stage consists of a low-frequency (LF) unfolder leg with switches S_{ap} and S_{an} and a high-frequency (HF) flying-capacitor leg with switches S_{1p}, S_{2p}, S_{3p}, S_{1n}, S_{2n}, S_{3n} and two flying capacitors C_1 and C_2. For each cell, S_{xp} and S_{xn} ($x \in \{a, 1, 2, 3\}$) form a complementary pair so that exactly one device conducts at any time. A single switching function

$$S_x(t) = \begin{cases} 1, & S_{xp} \text{ on, } S_{xn} \text{ off} \\ 0, & S_{xp} \text{ off, } S_{xn} \text{ on} \end{cases} \tag{3.2}$$

fully describes the conduction state of each pair. The instantaneous inverter voltage synthesized at the converter AC terminal is denoted $v_{\text{inv}}(t)$.

The flying-capacitor voltages $v_{c1}(t)$ and $v_{c2}(t)$ are regulated around nominal values

$$V_{dc} : V_{C1}^{*} : V_{C2}^{*} = 3 : 2 : 1, \tag{3.3}$$

so that the HF leg generates four distinct positive inverter-voltage levels with respect to the DC negative terminal in each half-cycle. Various voltage ratios have been suggested in the literature

(Patel, Rezkallah, Hamadi, Tidjani & Chandra, 2022; Kaymanesh, Chandra & Mulligan, 2021) which generates higher number of levels. However, the selected ratio provides the benefit of evenly spreading the voltage stress across the HF power switch. Additionally, the required capacitance is relatively lower since the charging and discharging occur at the switching frequency. With this ratio each HF device is rated for $V_{dc}/3$, and the capacitor references are $V_{C1}^{*} = 2V_{dc}/3$ and $V_{C2}^{*} = V_{dc}/3$. For a given switching state, the instantaneous converter voltage v_{inv} is written as

$$v_{\text{inv}}(t) = \big(S_a(t) - S_1(t)\big)\, V_{dc}(t) + \big(S_1(t) - S_2(t)\big)\, v_{c1}(t) + \big(S_2(t) - S_3(t)\big)\, v_{c2}(t), \qquad (3.4)$$

where $S_a(t), S_1(t), S_2(t), S_3(t) \in \{0, 1\}$. For a given combination of these switching variables, $v_{\text{inv}}(t)$ assumes one of the four allowed positive levels within each half-cycle.The admissible switching states of the HF leg and the associated capacitor charging directions are listed in Table 3.2.

Table 3.2 Possible switching states, output levels, and FC charging directions for four-level FCML converter

Index	S_a	S_1	S_2	S_3	v_{inv}/V_{dc}	C_1	C_2
1	1	0	0	0	+1	neutral	neutral
2	1	0	1	0	+2/3	charging	discharging
	1	1	0	0	+2/3	discharging	neutral
	1	0	0	1	+2/3	neutral	charging
3	1	1	1	0	+1/3	neutral	discharging
	1	0	1	1	+1/3	charging	neutral
	1	1	0	1	+1/3	discharging	charging
4	1	1	1	1	0	neutral	neutral
symmetrical negative levels for $S_a = 0$							

‘‘‘

3.3.2 Unified Continuous-Time Model

The LC interface is described by the inductor current $i_L(t)$ and the capacitor voltage $v_{cf}(t)$, with load/grid current $i_o(t)$ drawn from the AC node. The flying-capacitor voltages are $v_{c1}(t)$ and $v_{c2}(t)$. With the current orientation defined above, the continuous-time dynamics are

$$C_f \frac{dv_{cf}(t)}{dt} = i_L(t) - i_o(t) =: i_C(t), \tag{3.5}$$

$$L_f \frac{di_L(t)}{dt} = v_{\text{inv}}(t) - v_{cf}(t) - R_f\, i_L(t), \tag{3.6}$$

$$C_1 \frac{dv_{c1}(t)}{dt} = -\big(S_1(t) - S_2(t)\big)\, i_L(t), \tag{3.7}$$

$$C_2 \frac{dv_{c2}(t)}{dt} = -\big(S_2(t) - S_3(t)\big)\, i_L(t). \tag{3.8}$$

Equations (3.5)–(3.8) are valid for all operating modes. In grid-connected mode $v_{cf}(t) = v_g(t)$ and $i_o(t) = i_g(t)$, which yields

$$v_{\text{inv}}(t) = v_g(t) + R_f\, i_L(t) + L_f \frac{di_L(t)}{dt}. \tag{3.9}$$

In standalone mode $v_{cf}(t)$ is the synthesized output voltage $v_o(t)$ and $i_o(t)$ is the load current. The same current orientation and inductor-voltage relation (3.6) are kept for both modes; R_f is retained in (3.6) but may be neglected in the standalone LC resonance model used for delay compensation.

3.3.3 Discrete-Time Model for Predictive Control

For grid-connected current control, a forward-Euler discretization with sampling period T_s is sufficient. Denoting sampled quantities at $t = kT_s$ by $i_L(k)$, $v_{c1}(k)$, $v_{c2}(k)$, $v_{cf}(k)$, and $v_{\text{inv}}(k)$,

the one-step predictions are

$$\hat{i}_L(k+1) = i_L(k) + \frac{T_s}{L_f}\Big(v_{\text{inv}}(k) - v_{cf}(k) - R_f\, i_L(k)\Big), \tag{3.10}$$

$$\hat{v}_{c1}(k+1) = v_{c1}(k) - \frac{T_s}{C_1}\big(S_1(k) - S_2(k)\big)\, i_L(k), \tag{3.11}$$

$$\hat{v}_{c2}(k+1) = v_{c2}(k) - \frac{T_s}{C_2}\big(S_2(k) - S_3(k)\big)\, i_L(k). \tag{3.12}$$

In grid-connected operation $v_{cf}(k) = v_g(k)$ and $i_L(k)$ is equal to the measured grid current.

For standalone voltage control and delay compensation, an exact zero-order-hold discrete-time LC model is used. With $R_f = 0$ and $v_{\text{inv}}(t)$ held constant on $[kT_s, (k+1)T_s)$, the ZOH solution of (3.5)–(3.6) can be written directly in the measured v_{cf}, i_L and the (piecewise-constant) load current i_o:

$$v_{cf}(k+1) = c\, v_{cf}(k) + \frac{s_n}{\omega_n C_f}\, i_L(k) + (1-c)\, v_{\text{inv}}(k) - \frac{s_n}{\omega_n C_f}\, i_o(k), \tag{3.13}$$

$$i_L(k+1) = -\frac{s_n}{\omega_n L_f}\, v_{cf}(k) + c\, i_L(k) + \frac{s_n}{\omega_n L_f}\, v_{\text{inv}}(k) + (1-c)\, i_o(k), \tag{3.14}$$

where $\omega_n := 1/\sqrt{L_f C_f}$, $c := \cos(\omega_n T_s)$, and $s_n := \sin(\omega_n T_s)$. Equations (3.13)–(3.14) provide an exact discrete-time LC model in the state variables (v_{cf}, i_C) with the same current orientation as in (3.6).

Using the already applied $v_{\text{inv}}(k-1)$ and the measured pair $\{v_{cf}(k-1), i_L(k-1)\} \to \{v_{cf}(k), i_L(k)\}$,

$$\widehat{i_o}(k-1) = \frac{i_L(k) - c\, i_L(k-1) + \dfrac{s_n}{\omega_n C_f}\Big(v_{cf}(k-1) - v_{\text{inv}}(k-1)\Big)}{1-c}. \tag{3.15}$$

Then set $\widehat{i_o}(k) := \widehat{i_o}(k-1)$ for predictions on $[(kT_s, (k+1)T_s))$.

This model is used to predict the standalone output voltage and to compensate the one-sample actuation delay in the finite-control-set MPC described in Section 3.5.

3.4 Reference Generation in Grid-Connected and Standalone Modes

This section defines the references tracked by the predictive controller in the different operating modes. In grid-connected modes an outer dc-link power loop generates the active power reference $P^*(k)$. Instantaneous power theory is then used to synthesize the grid-current reference $i_g^*(k)$ from (P^*, Q^*). In standalone modes a sinusoidal voltage reference $v_{cf}^*(t)$ is imposed at the AC terminal.

3.4.1 Outer DC-Link Power Loop in Grid-Connected Modes

In grid-connected modes the dc-link voltage V_{dc} is regulated to a reference V_{dc}^* by a slow outer loop. The dc-link dynamics can be approximated by

$$C_{dc}\frac{dV_{dc}}{dt} \approx \frac{1}{V_{dc}}\big(P_{ac} - P_{load}\big), \tag{3.16}$$

where P_{ac} is the instantaneous ac-side power processed by the 4L–FCML stage and P_{load} is the power absorbed by the downstream dc–dc converter and battery. Neglecting high-frequency ripple, the average dc power balance gives $P_{ac} \simeq P_{load}$ at steady state.

A PI controller on the dc-link voltage generates the active power reference at the PCC:

$$P^*(k) = P_{\mathrm{cmd}}(k) + K_p^V\, e_V(k) + K_i^V \sum_{n=0}^{k} e_V(n), \tag{3.17}$$

$$e_V(k) = V_{dc}^* - V_{dc}(k), \tag{3.18}$$

where $P_{\mathrm{cmd}}(k)$ is the slow active-power command imposed by the charging scheduler or V2G/V2H/V2V aggregator. Positive $P^* > 0$ corresponds to G2V charging; negative $P^* < 0$ corresponds to V2G discharging. Without $P_{cmd}(k)$, the loop relies solely on the PI to react to voltage errors caused by load changes, which could lead to slower response or larger V_{dc} deviations. Adding $P_{cmd}(k)$ allows the first stage to anticipate the second-stage power demand, reducing the burden on the integrator and minimizing overshoot/undershoot. The output

of (3.17) is limited so that the pair (P^*, Q^*) remains inside the admissible P–Q region defined in Section 3.2 and that the dc current does not exceed the battery and dc–dc ratings. The reactive power reference Q^* is either set to zero for unity-power-factor G2V operation or commanded by the grid operator for V2G/V2H/V2V services. Q^* can also be used to compensate for the reactive power drawn by the C_f in grid-connected mode.

3.4.2 Grid-Connected Current Reference Generation

In all grid-connected modes the 4L–FCML stage operates as a grid-following converter and relies on a single-phase orthogonal-signal-generator (OSG) PLL for phase and frequency tracking (Ciobotaru, Teodorescu & Blaabjerg, 2006; Ciobotaru, Teodorescu & Agelidis, 2008; Bhardwaj, 2013; Karimi-Ghartemani, Khajehoddin, Jain, Bakhshai & Mojiri, 2012). A phase-locked loop (PLL) tracks the grid voltage phase and frequency, and also supports protection functions such as detecting loss of mains and deciding when to transfer to standalone operation. The dominant contributors to synchronization error are dc offsets, low-frequency harmonics, and high-frequency measurement noise. To mitigate these effects, this work employs a single-phase SOGI–FLL offset rejection structure that provides band-pass–filtered, dc-free orthogonal components of the grid voltage $\left(v_{g\alpha}(k), v_{g\beta}(k)\right)$ and a slowly adapting frequency estimate $\hat{\omega}(k)$. A second-order generalized integrator tuned at ω_n generates two orthogonal, fundamental-selective components $v_{g\alpha}$ and $v_{g\beta}$ according to

$$\begin{aligned} G_\alpha(s) &= \frac{v_{g\alpha}(s)}{v_g(s)} = \frac{k_{\mathrm{SOGI}}\,\omega_n\, s}{s^2 + k_{\mathrm{SOGI}}\,\omega_n\, s + \omega_n^2}, \\ G_\beta(s) &= \frac{v_{g\beta}(s)}{v_g(s)} = \frac{\omega_n^2}{s^2 + k_{\mathrm{SOGI}}\,\omega_n\, s + \omega_n^2}. \end{aligned} \tag{3.19}$$

so that, when ω_n matches the grid frequency, $v_{g\alpha}$ and $v_{g\beta}$ are sinusoids with equal amplitude and 90° phase shift. These $\alpha\beta$ components are then mapped to the synchronous frame using the estimated phase $\hat{\theta}$,

$$\begin{bmatrix} v_d \\ v_q \end{bmatrix} = \begin{bmatrix} \cos\hat{\theta} & \sin\hat{\theta} \\ -\sin\hat{\theta} & \cos\hat{\theta} \end{bmatrix} \begin{bmatrix} v_{g\alpha} \\ v_{g\beta} \end{bmatrix}, \tag{3.20}$$

and a PI loop drives $v_q \to 0$, thereby adapting the estimated frequency $\hat{\omega}$ and locking the internal oscillator to the grid. When locked, the pair $\big(v_{g\alpha}, v_{g\beta}\big)$ is frequency- and amplitude-locked to the fundamental and is used for P–Q current-reference generation.

A SOGI–FLL or PLL provides orthogonal components of the grid voltage, $v_{g\alpha}(k)$ and $v_{g\beta}(k)$, synchronized with the fundamental. The instantaneous active and reactive powers at the PCC are

$$\begin{bmatrix} P(k) \\ Q(k) \end{bmatrix} = \frac{1}{2} \begin{bmatrix} v_{g\alpha}(k) & v_{g\beta}(k) \\ -v_{g\beta}(k) & v_{g\alpha}(k) \end{bmatrix} \begin{bmatrix} i_{g\alpha}(k) \\ i_{g\beta}(k) \end{bmatrix}, \tag{3.21}$$

where $i_{g\alpha}(k)$ and $i_{g\beta}(k)$ are the corresponding current components. Inverting this relation yields the current reference vector

$$\begin{bmatrix} i^*_{g\alpha}(k) \\ i^*_{g\beta}(k) \end{bmatrix} = \frac{2}{v^2_{g\alpha}(k) + v^2_{g\beta}(k)} \begin{bmatrix} v_{g\alpha}(k) & v_{g\beta}(k) \\ -v_{g\beta}(k) & v_{g\alpha}(k) \end{bmatrix} \begin{bmatrix} P^*(k) \\ Q^*(k) \end{bmatrix}. \tag{3.22}$$

For a single-phase system the physical grid current coincides with the α component, so the inductor/grid current reference for the predictive controller is

$$i^*_g(k) = i^*_{g\alpha}(k) = \frac{2}{v^2_{g\alpha}(k) + v^2_{g\beta}(k)} \big(v_{g\alpha}(k)\, P^*(k) + v_{g\beta}(k)\, Q^*(k)\big), \tag{3.23}$$

Equation (3.22) is used in all grid-connected modes (G2V, V2G, and grid-tied V2H/V2V); only the commanded pair (P^*, Q^*) changes with the operating mode. The pair is clipped to respect the apparent-power circle and dc-side limits specified in Section 3.2.2.

3.4.3 Standalone Voltage Reference Generation

In standalone V2L and islanded V2H/V2V modes the 4L–FCML stage acts as a grid-forming converter. The predictive controller regulates the filter-capacitor voltage $v_{cf}(t)$ to follow a sinusoidal reference

$$v^*_{cf}(t) = \sqrt{2}\, V^*_o \, \sin\big(\omega_0 t + \phi_0\big), \tag{3.24}$$

where V_o^* and ω_0 are the desired rms voltage and angular frequency at the ac port (e.g. 120 V/60 Hz or 230 V/50 Hz), and ϕ_0 is the initial phase. In discrete time the reference at sample k is

$$v_{cf}^*(k) = \sqrt{2}\, V_o^* \, \sin\!\left(\omega_0 k T_s + \phi_0\right), \tag{3.25}$$

and is used directly in the cost function of the standalone voltage-forming MPC. More advanced schemes could adjust V_o^* or ω_0 according to droop characteristics or dc-side constraints, but such extensions are outside the scope of this chapter.

3.5 Finite-Control-Set MPC of the 4L–FCML Stage

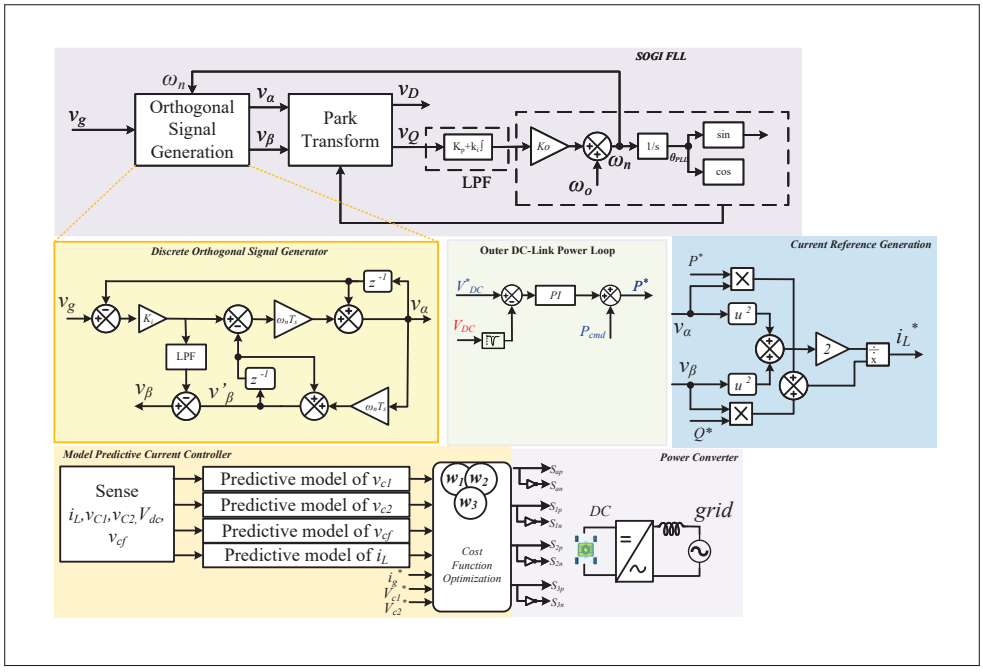


Figure 3.5 Control Scheme for the bidirectional totem-pole four-level FCML converter using the optimized model predictive controller

This section formulates the finite-control-set model predictive controller (FCS–MPC) for the 4L–FCML AC–DC stage. The same discrete-time models from Section 3.3 are used in all modes; only the tracked reference (current or voltage) and the cost function change. The overall control structure is summarized in Fig. 3.5.

3.5.1 Problem Formulation and Prediction

The HF leg switching state at sample k is

$$s(k) = \big(S_1(k), S_2(k), S_3(k)\big) \in \mathcal{S}, \tag{3.26}$$

where $\mathcal{S}$ is the set of admissible combinations listed in Table 3.2. The LF leg state $S_a(k)$ is determined from the ac-side polarity (grid voltage in grid-connected modes, voltage reference in standalone mode) and enters the inverter voltage expression (3.4).

The state vector of the HF leg is

$$x(k) = \begin{bmatrix} i_L(k) & v_{c1}(k) & v_{c2}(k) \end{bmatrix}^{\mathsf{T}}, \tag{3.27}$$

and the discrete-time model (3.10)–(3.12) gives the one-step prediction $x(k+1)$ for a given switching state and measured $v_{cf}(k)$. To account for the one-sample actuation delay of the digital implementation, the cost is evaluated using two-step-ahead predictions. Denoting by $\hat{x}(k+2\,|\,k, s)$ the state obtained by applying (3.10)–(3.12) twice, first with the inverter voltage corresponding to the already-applied state $s(k)$ and then with the candidate $s \in \mathcal{S}$, the resulting predictions are written as

$$\hat{x}(k+2\,|\,k, s) = \begin{bmatrix} \hat{i}_L^{+}(s) & \hat{v}_{c1}^{+}(s) & \hat{v}_{c2}^{+}(s) \end{bmatrix}^{\mathsf{T}}. \tag{3.28}$$

In standalone modes, the output-voltage prediction also uses the exact LC model (3.13)–(3.14). With $\hat{i_o}(k)$ and the inverter-voltage sequence implied by $s(k)$ and a candidate $s \in \mathcal{S}$, the two-step-ahead prediction of the filter-capacitor voltage is denoted $\hat{v}_{cf}^{+}(s)$ and is obtained by two successive applications of (3.13)–(3.14).

3.5.2 Grid-Connected Current-Mode FCS–MPC

In grid-connected modes the 4L–FCML stage operates as a grid-following converter. The control objective is to track the grid-current reference $i_g^*(k)$ from (3.23), while maintaining the flying-capacitor voltages close to their references V_{C1}^* and V_{C2}^*. The measured inductor current coincides with the grid current, $i_g(k) \approx i_L(k)$, given the series placement of L_f and negligible reactance offered by C_f.

The current reference is advanced one sample to match the two-step-ahead prediction,

$$i_g^{*+}(k) := i_g^*(k+1), \tag{3.29}$$

computed from (3.22)–(3.23). For each candidate $s \in \mathcal{S}$ the cost is defined as

$$\begin{aligned} J_{\text{grid}}(s) = w_i \left(\hat{i}_L^+(s) - i_g^{*+}(k)\right)^2 + w_{c1} \left(\hat{v}_{c1}^+(s) - V_{C1}^*\right)^2 \\ + w_{c2} \left(\hat{v}_{c2}^+(s) - V_{C2}^*\right)^2 + w_\Delta \, d_H\big(s, s(k)\big), \end{aligned} \tag{3.30}$$

where w_i, w_{c1}, w_{c2}, and w_Δ are positive weights and $d_H(\cdot,\cdot)$ is the Hamming distance between the candidate and the previously applied HF state, used to penalize unnecessary switching transitions. The optimal switching state is

$$s^\star(k) = \arg\min_{s \in \mathcal{S}} J_{\text{grid}}(s), \tag{3.31}$$

and is applied during the interval $[(k+1)T_s, (k+2)T_s)$.

This formulation uses a single set of weights for all grid-connected V2X modes. The operating point (G2V, V2G, or grid-tied V2H/V2V) is determined solely by the commanded pair (P^*, Q^*) and the associated current reference $i_g^*(k)$.

3.5.3 Standalone Voltage-Forming FCS–MPC

In standalone V2L and islanded V2H/V2V modes the 4L–FCML stage operates as a grid-forming converter. The primary objective is to track the filter-capacitor voltage reference $v^*_{cf}(k)$ from (3.25), while maintaining flying-capacitor balancing and limiting the inductor current under potentially nonlinear loads.

At instant k the controller measures $v_{cf}(k)$ and $i_L(k)$ and computes $\widehat{i_o}(k)$ from (3.15). Two-step predictions $\widehat{v}^{+}_{cf}(s)$ and $\widehat{i}^{+}_{L}(s)$ for each candidate $s \in \mathcal{S}$ are obtained by the ZOH recursions in (3.13)–(3.14).

Stage 1 (applied input) uses $v_{\text{inv}}(k)$ to propagate (3.13)–(3.14) and form the intermediate prediction

$$\widehat{v}^{p}_{cf}(k+1) = c\, v_{cf}(k) + \tfrac{s_n}{\omega_n C_f}\, i_L(k) + (1-c)\, v_{\text{inv}}(k) - \tfrac{s_n}{\omega_n C_f}\, \widehat{i}_o(k), \tag{3.32}$$

$$\widehat{i}^{p}_{L}(k+1) = -\tfrac{s_n}{\omega_n L_f}\, v_{cf}(k) + c\, i_L(k) + \tfrac{s_n}{\omega_n L_f}\, v_{\text{inv}}(k) + (1-c)\, \widehat{i}_o(k). \tag{3.33}$$

Stage 2 (candidate input) evaluates each $s \in \mathcal{S}$ via $v^{(s)}_{\text{inv}}(k+1)$ to obtain two-step-ahead outputs:

$$\widehat{v}^{+}_{cf}(s) := \widehat{v}_{cf}(k+2\,|\,k,s) = c\, \widehat{v}^{p}_{cf}(k+1) + \tfrac{s_n}{\omega_n C_f}\, \widehat{i}^{p}_{L}(k+1) + (1-c)\, v^{(s)}_{\text{inv}}(k+1) - \tfrac{s_n}{\omega_n C_f}\, \widehat{i}_o(k), \tag{3.34}$$

$$\widehat{i}^{+}_{L}(s) := \widehat{i}_L(k+2\,|\,k,s) = -\tfrac{s_n}{\omega_n L_f}\, \widehat{v}^{p}_{cf}(k+1) + c\, \widehat{i}^{p}_{L}(k+1) + \tfrac{s_n}{\omega_n L_f}\, v^{(s)}_{\text{inv}}(k+1) + (1-c)\, \widehat{i}_o(k). \tag{3.35}$$

The standalone cost for candidate s is

$$\begin{aligned} J_{\text{sa}}(s) = {} & w_v \left(\hat{v}^{+}_{cf}(s) - v^{*+}_{cf}(k)\right)^2 + w_{c1} \left(\hat{v}^{+}_{c1}(s) - V^{*}_{C1}\right)^2 \\ & + w_{c2} \left(\hat{v}^{+}_{c2}(s) - V^{*}_{C2}\right)^2 + w_i \left(\hat{i}^{+}_{L}(s)\right)^2 + w_\Delta\, d_H\big(s, s(k)\big), \end{aligned} \tag{3.36}$$

where w_v weights the voltage-tracking term and the term in $\hat{i}_L^+(s)^2$ penalizes excessive inductor current and damps oscillations. The optimal state in standalone mode is

$$s^\star(k) = \arg\min_{s\in\mathcal{S}} J_{\text{sa}}(s), \tag{3.37}$$

and is applied during $[(k+1)T_s, (k+2)T_s)$.

The flying-capacitor balancing terms in (3.30)–(3.36) use the same references V_{C1}^* and V_{C2}^* in both grid-connected and standalone modes.

3.5.4 Per-Sample Implementation

The per-sample finite-control-set MPC routine for the 4L–FCML converter, including both grid-connected and standalone operating modes, is summarized in Algorithm 3.1.

3.6 Simulation Results

This section presents switching-level simulation results for the single-phase 4L–FCML OBC controlled by the FCS–MPC scheme described in Section 3.5. The results are organized by operating mode and use the same converter and control parameters for all cases. The converter, grid, and controller parameters used in all simulations are summarized in Table 3.3. Comprehensive simulations of the 4L–FCML EV on-board charger front end are carried out in PLECS simulation software to validate the operation. In grid connected mode the grid is modeled as a single-phase source with nominal line-to-neutral voltage and frequency representative of AC Level 2 charging. The dc link is connected to a bidirectional dc source that emulates the battery and dc–dc stage in charging mode or constant power resistor R_{dc} in discharging mode.

Fig. 3.6(a) illustrates the switching pulses for S_a and average duty cycles for the HF switches. Fig 3.6(b) shows the optimized index used by the MPC control. It can be observed that the index only changes one step at a time due to switching penalty.

Algorithm 3.1 FCS–MPC for 4L–FCML converter (grid-connected and standalone modes)

Input: $s^\star(k-1)$; mode flag (grid-connected/standalone); measured $v_{cf}(k), i_L(k), v_{c1}(k), v_{c2}(k), V_{dc}(k)$; outer-loop refs $P^*(k), Q^*(k)$ or $v^*_{cf}(k)$

Output: $s^\star(k)$ for $[(k+1)T_s, (k+2)T_s)$

1) Sample & apply previous state
Sample $v_{cf}(k), i_L(k), v_{c1}(k), v_{c2}(k), V_{dc}(k)$;
apply $s^\star(k-1)$ on $[kT_s, (k+1)T_s)$.
2) Outer-loop & mode primitives
if *mode==grid-connected* **then**
    set $v_g(k) \to v_{cf}(k)$;
    update $P^*(k)$ via (3.17);
    set $Q^*(k)$;
    form $i^*_g(k)$, $i^{*+}_g(k)$ by (3.22)–(3.23);
    $S_a(k) \leftarrow \text{sign}\big(v_g(k)\big)$, $S_a(k+1) \leftarrow \text{sign}\big(v_g(k)\big)$;
else
    `// standalone`
    form $v^*_{cf}(k)$, $v^{*+}_{cf}(k)$ by (3.25);
    reconstruct $\widehat{i_o}(k)$ via (3.15);
    $S_a(k) \leftarrow \text{sign}\big(v^*_{cf}(k)\big)$, $S_a(k+1) \leftarrow \text{sign}\big(v^{*+}_{cf}(k)\big)$;
end if
3) Known-input one-step (to $k+1$)
$v_{\text{inv}}(k) \leftarrow$ (3.4) using $S_a(k)$ and $s^\star(k-1)$.
HF/FC leg: use (3.10)–(3.12) with $v_{\text{inv}}(k)$ to obtain $\hat{i}_L(k+1), \hat{v}_{c1}(k+1), \hat{v}_{c2}(k+1)$.
if *mode==standalone* **then**
    LC node (intermediate): form $\hat{v}^p_{cf}(k+1)$, $\hat{i}^p_L(k+1)$ using (3.13)–(3.14) with $v_{\text{inv}}(k)$ and $\widehat{i_o}(k)$.
end if
4) Candidate loop (to $k+2$) & cost
foreach $s \in \mathcal{S}$ **do**
    $v_{\text{inv}}(k+1, s) \leftarrow$ (3.4) using $S_a(k+1)$ and s.
    HF/FC leg: with $v_{\text{inv}}(k+1, s)$ and initial $\hat{i}_L(k+1), \hat{v}_{c1}(k+1), \hat{v}_{c2}(k+1)$, compute $\hat{i}^+_L(s), \hat{v}^+_{c1}(s), \hat{v}^+_{c2}(s)$ via (3.10)–(3.12).
    if *mode==standalone* **then**
        LC node: compute $\hat{v}^+_{cf}(s)$ by applying (3.13)–(3.14) to $\big(\hat{v}^p_{cf}(k+1), \hat{i}^p_L(k+1)\big)$ with $v_{\text{inv}}(k+1, s)$ and $\widehat{i_o}(k)$.
    end if
    if *mode==grid-connected* **then**
        evaluate $J_{\text{grid}}(s)$ by (3.30);
    end if
    else
        evaluate $J_{\text{sa}}(s)$ by (3.36);
    end if
end foreach
5) Selection
$s^\star(k) = \arg\min_{s \in \mathcal{S}} J(s)$;
store $s^\star(k)$ for $[(k+1)T_s, (k+2)T_s)$.

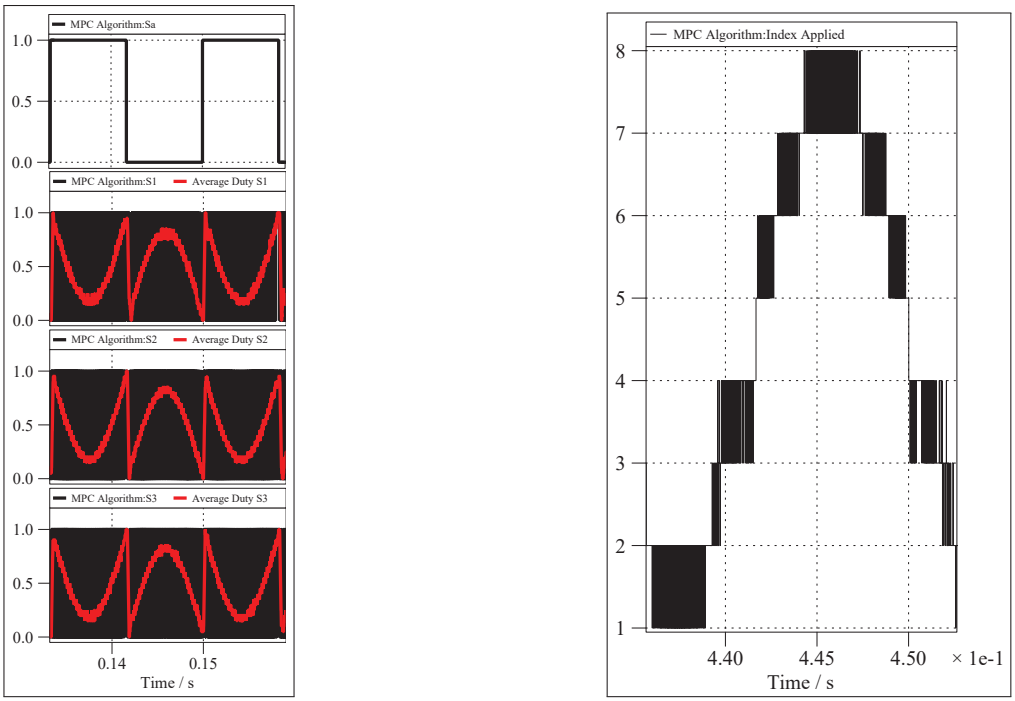
Table 3.3 Simulation parameters

Parameter	Value
Grid voltage v_g	90–265 V_{rms}
Grid frequency f	60 Hz
DC-link voltage V_{dc}	400 V
Grid filter inductance L_f	250 μH
Flying capacitance C_1	20 μF
Flying capacitance C_2	20 μF
Sampling period T_s	5 μs
Nominal power P_N	7 kW at 230 V_{rms}
Rated ac current $I_{g,rated}$	40 A_{rms}
FC reference voltage V_{C1}^*	133.33 V
FC reference voltage V_{C2}^*	266.67 V
Maximum switching frequency $f_{s,max}$	100 kHz

In Fig. 3.8, the startup performance is depicted with capacitors charging from a fully discharged state. The proposed controller exhibits no significant inrush current, and the capacitors stabilize at their final value within one power cycle. Fig. 3.9 illustrates the simulated waveform of the capacitor current to highlight the rationale for the low capacitance requirement. The charging and discharging processes are conducted at the switching frequency level, resulting in minimal voltage ripple. Fig. 3.10 demonstrates the robust operation of the converter following a step change in input voltage from 230 V RMS to 120 V RMS. The control strategy maintains the current at 32A RMS, allowing the converter power to stabilize at 4000 W at the lower voltage.

3.6.1 Grid-Connected G2V and V2G Operation

Figure 3.7 shows steady-state and dynamic waveforms for grid-connected operation in both G2V (charging) and V2G (discharging) modes at representative power levels. In G2V operation ($P^* > 0$, $Q^* = 0$) the grid current i_g is nearly sinusoidal and in phase with the grid voltage v_g, confirming unity power factor. The total harmonic distortion (THD) of the grid current under steady state was found to be 1.87%. To assess the dynamic performance amid changes in power reference, the power setpoint P^* was incrementally adjusted from 4000 W to 7000 W, and



(a) (b)

Figure 3.6 (a)Switching pulses for Sa and HF leg with superimposed average duty cycles; (b) Optimized Index applied selected by MPC over one power cycle

subsequently to −4000 W to facilitate reverse power flow. It was noted that the current promptly aligned with the changes in the current reference without impacting the DC regulation of FCs.

The flying-capacitor voltages v_{c1} and v_{c2} remain tightly centered around V_{C1}^{*} and V_{C2}^{*}, respectively, with switching-frequency ripple determined by the selected capacitance values. The FCS–MPC cost function penalizes deviations from these references, so that the average stress across the HF devices is kept balanced despite the single-phase power pulsation.

In V2G operation ($P^{*} < 0$) the direction of active power is reversed while the same current-control structure is maintained. Figure 3.7 illustrates that i_g is still sinusoidal and now approximately in anti-phase with v_g, while the magnitude of the current follows the commanded $|P^{*}|$. The dc-link voltage remains regulated near V_{dc}^{*} as power flows from the battery to the grid. The

flying-capacitor voltages preserve their average values and ripple envelopes, indicating that the FC balancing mechanism remains effective under both charging and discharging conditions.

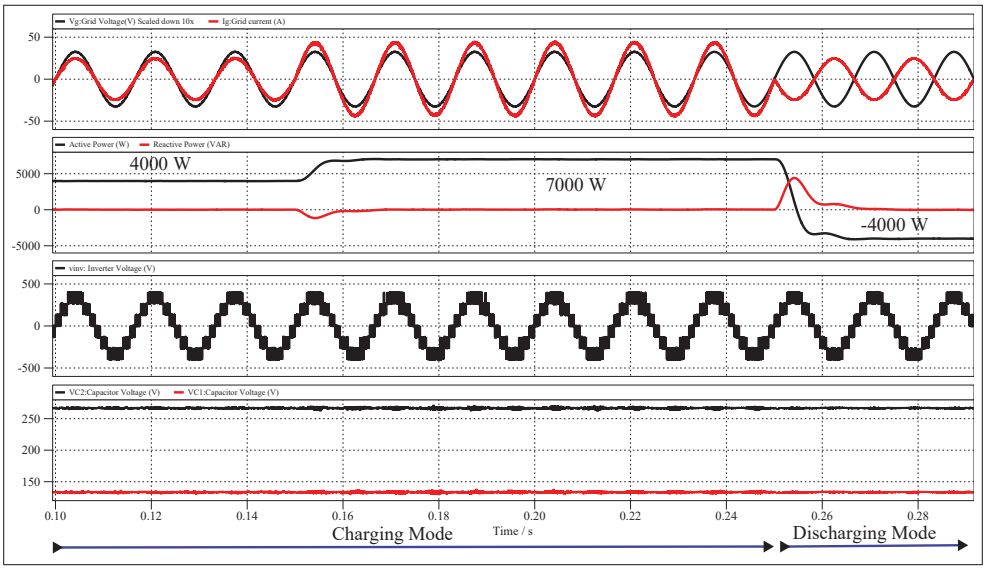


Figure 3.7 Simulation waveforms for grid-connected G2V and V2G modes: with step changes in active power reference (1) Grid current (i_g) and Grid voltage (v_g). (2) Active and reactive power (3) Converter output voltage (v_{inv}) (4) Flying capacitor voltages; during the discharging and charging mode with unity power factor operation

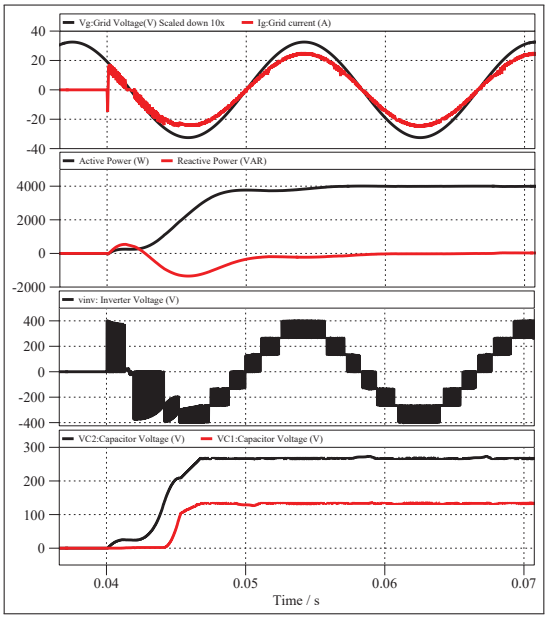


Figure 3.8 Simulation result for system states during startup in G2V Mode

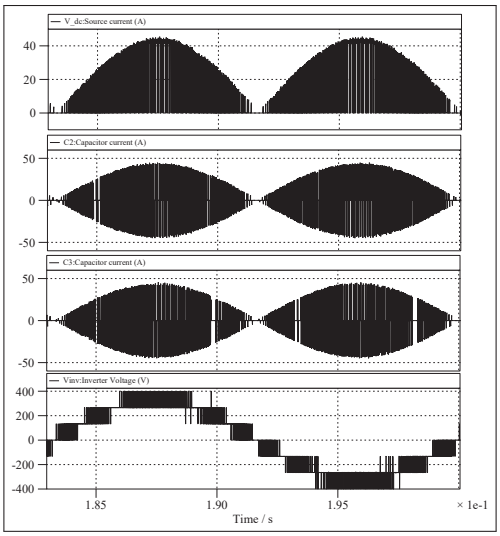


Figure 3.9 Simulation result showing the charging and discharging current for flying capacitors and dc source for one power cycle

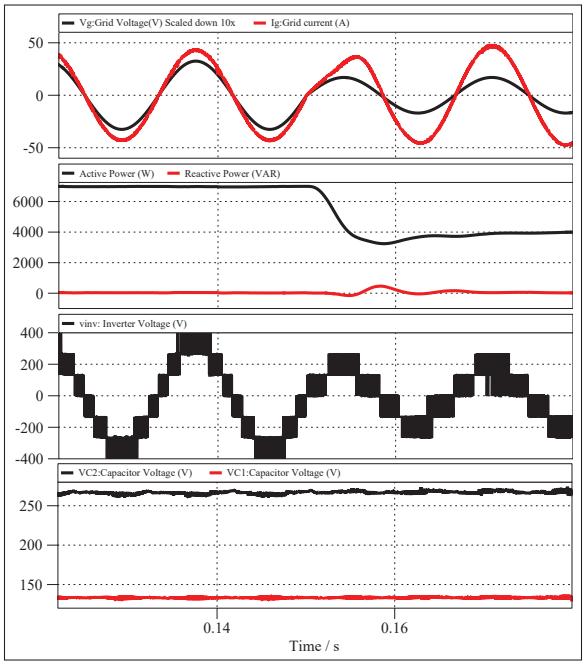


Figure 3.10 Simulation result showing system states during the step change of grid voltage (v_g) from 230V *rms* to 120V *rms* in G2V Mode

3.6.2 Grid-Connected V2H and V2V Operation

To demonstrate non-unity-power-factor operation, a grid-connected V2H/V2V case is simulated with nonzero reactive-power command $Q^* \neq 0$. Figure 3.11 shows the grid voltage v_g, grid current i_g, and the corresponding instantaneous active and reactive powers (P, Q) computed from the measured voltages and currents. The current reference $i_g^*(k)$ is generated from the pair (P^*, Q^*) using (3.22), and the MPC tracks this reference directly.

For inductive operation ($Q^* > 0$) the grid current lags the voltage by the corresponding phase angle, whereas for capacitive operation ($Q^* < 0$) the current leads. In both cases, the measured (P, Q) follow the commanded (P^*, Q^*) with small steady-state error, and the locus of (P, Q) remains within the feasible P–Q region defined in Section 3.2.2. The dc-link voltage is kept within its allowable range, and the flying-capacitor voltages stay close to their references, confirming that the same FCS–MPC formulation can provide V2H/V2V support services without retuning.

3.6.3 Standalone V2L and Islanded V2H Operation

Standalone operation is evaluated by connecting local loads directly to the AC terminal of the 4L–FCML stage and operating the converter in grid-forming mode. Figure 3.12 shows the output voltage $v_o = v_{cf}$ and load current i_o for five representative cases: non-linear rectifier load, a linear resistive load, capacitive load and inductive load.

Under the resistive load, v_o closely follows the sinusoidal reference $v_{cf}^*(t)$ from (3.24), with negligible amplitude droop and low distortion. The corresponding current i_o is nearly sinusoidal and in phase with v_o, and the predicted LC dynamics from (3.13)–(3.14) ensure that the voltage at the capacitor node is accurately regulated despite the one-sample computational delay. Under the non-linear rectifier load, i_o becomes highly distorted and exhibits the expected pulsed shape, while the output voltage v_o remains close to sinusoidal. The FCS–MPC anticipates the effect of the switching state on the LC filter and selects inverter voltages that keep the voltage error small over successive samples. The flying-capacitor voltages stay regulated around V_{C1}^* and V_{C2}^* in

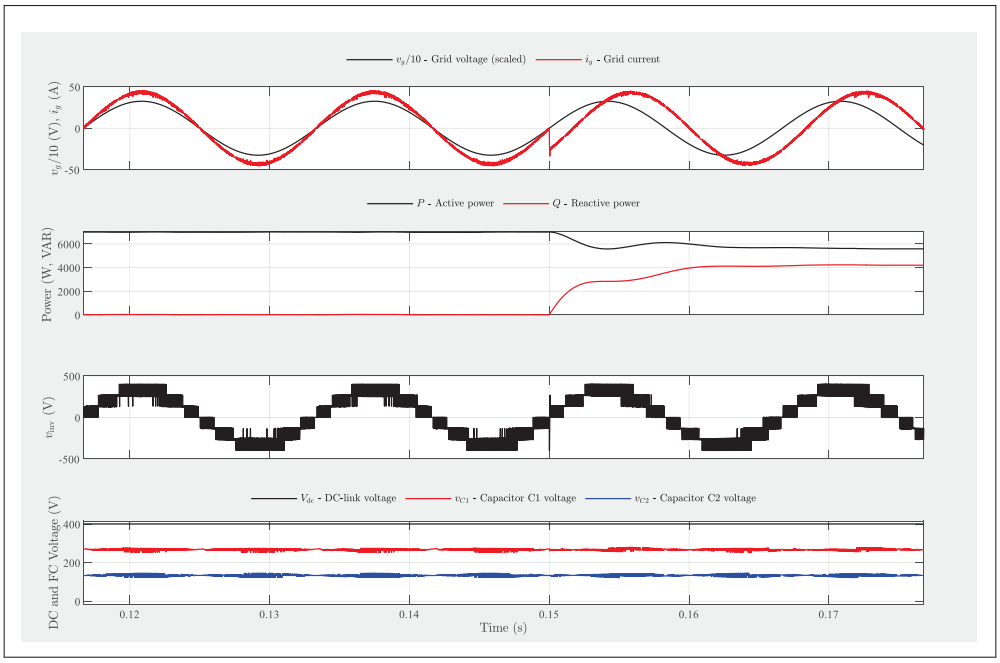


Figure 3.11 Grid connected operation of the proposed single phase 4L FCML converter with a step in the (P^*, Q^*) power reference. Top trace: scaled grid voltage $v_g/10$ and grid current i_g, illustrating the transition from unity power factor to a nonunity power factor following the change in Q^*. Second trace: active and reactive power P and Q; P remains close to its rated value while Q tracks the commanded reference. Third trace: converter output voltage v_{inv}. Bottom traces: dc link and flying capacitor voltages V_{dc}, V_{C1}, and V_{C2}, which stay tightly regulated and well balanced during the Q^* transient

both linear and non-linear cases, indicating that FC balancing is preserved even when supplying distorted load currents.

In standalone mode, the proposed controller regulates the output voltage over a wide range. Figure 3.13 illustrates the steady-state waveforms when the reference ac voltage is stepped from 120 V_{rms} to 230 V_{rms} while supplying a linear load, confirming accurate voltage tracking and stable flying-capacitor voltage balancing.

These simulations confirm that the proposed FCS–MPC and reference generation scheme can operate the same 4L–FCML hardware across the full set of V2X modes, namely G2V, V2G, grid-connected V2H/V2V, and standalone V2L/islanded V2H, without changing the underlying prediction model or switching table.

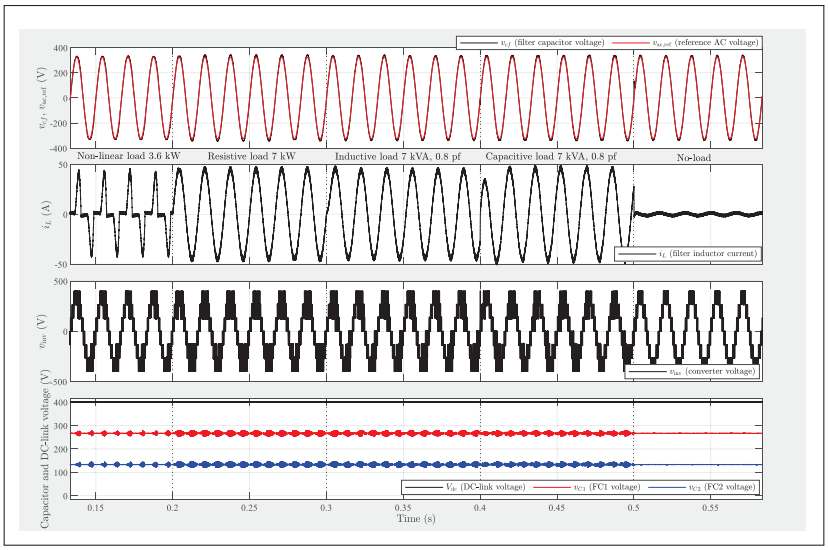


Figure 3.12 Standalone operation of the 4L FCML inverter under successive load changes from nonlinear load (3.6 kW) to resistive load (7 kW), inductive load (7 kVA, 0.8 pf lagging), capacitive load (7 kVA, 0.8 pf leading), and no load. Top trace: filter capacitor voltage v_{cf} and reference voltage v_{cf}^{*+} showing accurate 230 V rms, 60 Hz voltage regulation. Second trace: filter inductor current i_f illustrating the different load conditions. Third trace: converter output voltage v_{inv}. Bottom traces: dc link and flying capacitor voltages V_{dc}, V_{C1}, and V_{C2} demonstrating stable capacitor voltage balancing during all load steps

3.7 Experimental Validation

To demonstrate the feasibility and effectiveness of the proposed unified control, a scaled-down 4L–FCML prototype rated at 1 kW was developed, as shown in Fig. 3.14. The control algorithms were implemented on a TMS320F28379D controller, with the MPC algorithm integrated within the interrupt service routine, which is triggered at a frequency of 200 kHz. The dc-link voltage V_{dc} was set at 200 V, and the experimental setup included a dc voltage source operating in inverter mode. The inverter mode experimental results are shown in Fig. 3.15. Additionally, a second test was conducted with an AC source and resistive load operating in rectifier mode. Due to the unavailability of a bidirectional source for the setup, each mode was tested individually. The rectifier-mode experimental test results are shown in Fig. 3.16.

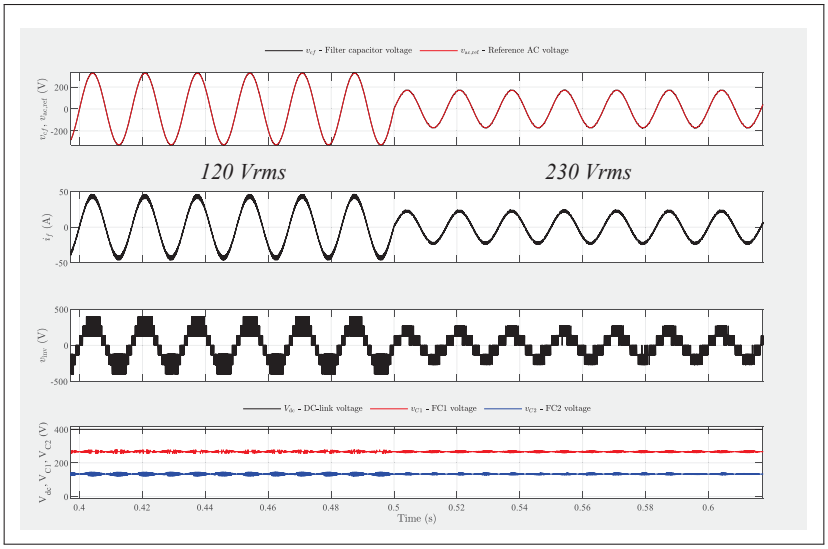


Figure 3.13 Standalone operation of the proposed single-phase 4L FCML inverter when the reference ac voltage is stepped from 230 V_{rms} to 120 V_{rms}. Top trace: v_{cf} and v_{cf}^{*+} showing accurate tracking. Second trace: filter inductor current i_f . Third trace: converter output voltage v_{inv}. Bottom traces: dc-link and flying-capacitor voltages demonstrating stable capacitor-voltage balancing during the voltage step

3.8 Conclusion

This chapter presented a unified model predictive control framework for a single-phase bidirectional on-board charger that uses a totem-pole four-level flying-capacitor multilevel (4L–FCML) PFC stage as the only grid interface. A mode-dependent outer layer generates current or voltage references from active and reactive power commands, while a single finite-control-set model predictive controller (FCS–MPC) regulates the ac side and maintains flying-capacitor voltage balance in all grid-connected and standalone V2X modes.

An discrete-time model of the 4L–FCML stage was derived for bidirectional operation and embedded in a delay-compensated, two-step-ahead FCS–MPC with an extended switching table that encodes capacitor charging information and penalizes switching effort. Switching-level simulations for a 7 kW, 230 V rms, 60 Hz case study demonstrated compliant grid currents, accurate P/Q control, robust standalone voltage regulation with linear and nonlinear loads, and satisfactory capacitor-voltage balancing. Experimental validation on a scaled prototype

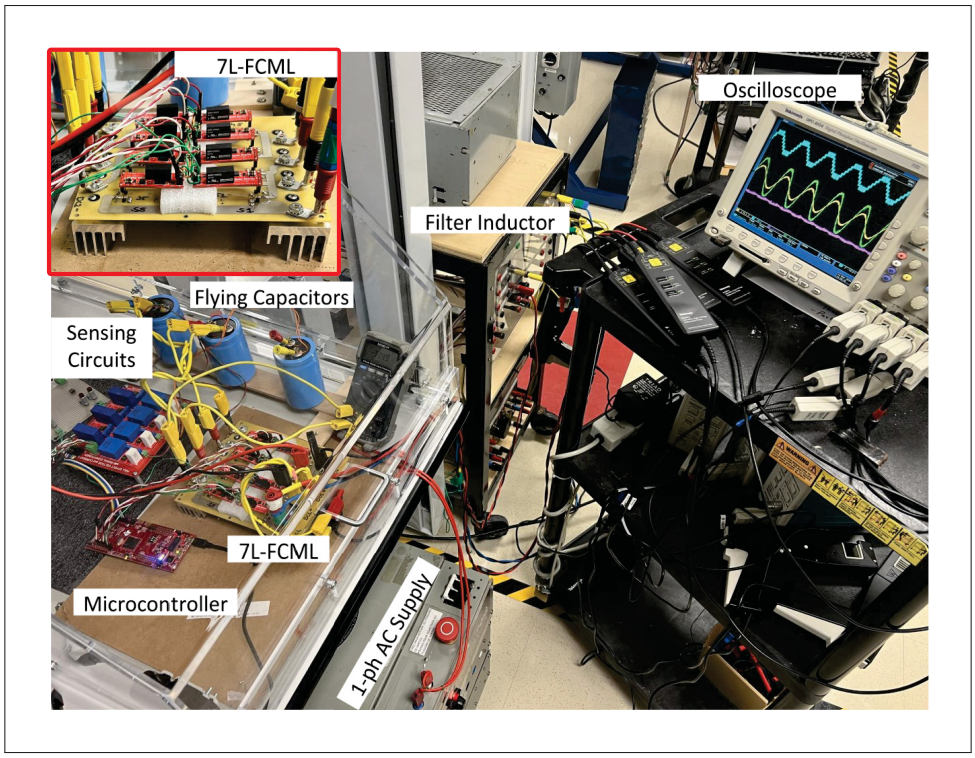


Figure 3.14 Experimental prototype developed for the 4L–FCML converter to validate the proposed control

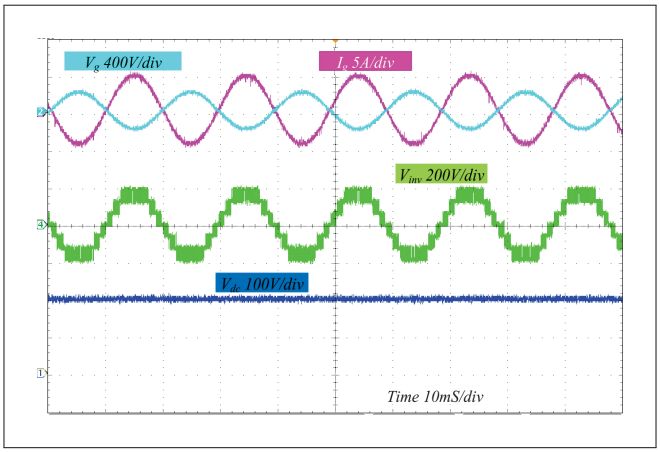


Figure 3.15 Experimental test results for the discharging operation (inverter mode) showing the inverter output voltage (v_{inv}), grid voltage (v_g), grid current (i_g) and DC-link voltage (V_{dc})

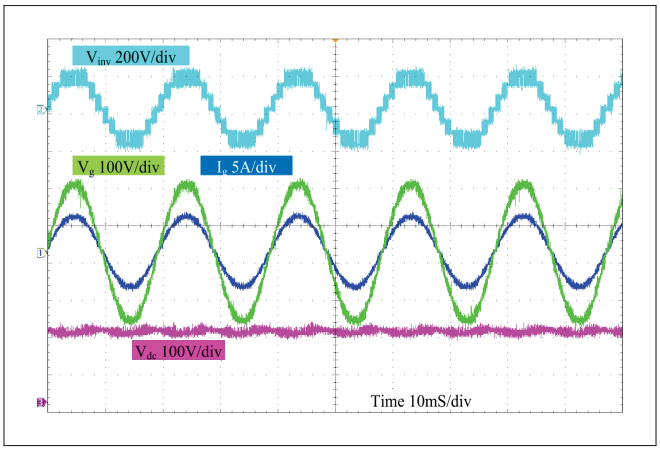


Figure 3.16 Experimental test results for the charging operation (rectifier mode) showing the inverter output voltage (v_{inv}), grid voltage (v_g), grid current (i_g) and DC-link voltage (V_{dc})

confirmed that the unified architecture can be implemented on a digital controller with practical sampling rates, thereby demonstrating the feasibility of using a single 4L–FCML ac–dc stage for V2X-capable on-board chargers.

CHAPTER 4

MODEL PREDICTIVE CONTROL FOR AN INTEGRATED POWER PULSATION BUFFER FOUR-CELL FLYING-CAPACITOR PFC CONVERTER

This chapter demonstrates an integrated power-pulsation buffering (iPPB) approach for a bidirectional single-phase totem-pole four-cell flying-capacitor (TP–4CFC) PFC converter that leverages the intrinsic energy storage of the flying capacitors to reduce electrolytic DC-link requirements without auxiliary PPB hardware. A weighted-sum multi-objective model-predictive current control (MOMPCC) law is formulated to track the grid current while regulating the three flying-capacitor voltages. Partial PPB is realized via an adaptive bang-bang reference for the capacitor voltages driven by instantaneous power deviation. The predictor uses exact ZOH-discretized state dynamics with two-step look-ahead to compensate the one-sample actuation delay, evaluating a finite set of discrete switching states from low-frequency inductor-current measurements. A 2.5 kW, 400 V prototype validates the method at a 6.66 μs sampling period and a 100 kHz switching limit, achieving more than 50% reduction in DC-link voltage ripple and 2.47% grid-current THD under integrated PPB. Hardware complexity is contained to sensing and finite-state evaluation, enabling compact front ends for EV onboard chargers and server supplies.

4.1 Introduction

Single-phase AC-DC conversion systems inherently experience instantaneous power mismatch at twice the line frequency (Fig. 4.1). While the instantaneous input AC power $P_{AC}(t)$ varies sinusoidally, the output DC power P_{DC} is typically constant. This discrepancy necessitates an intermediate energy buffer to absorb and release energy, maintaining DC bus voltage stability and improving power quality.

$$P_{AC}(t) = \frac{V_m I_m}{2} - \frac{V_m I_m}{2}\cos\left(2\omega_G t\right), \tag{4.1}$$

where V_m, I_m, and ω_G denote the peak input voltage, peak input current, and grid angular frequency, respectively.

The power imbalance generating the energy ripple stored in the buffer is given by:

$$p_{buf}(t) \;=\; P_{AC}(t) - P_{DC} \;=\; -\frac{V_m I_m}{2}\cos\left(2\omega_G t\right), \tag{4.2}$$

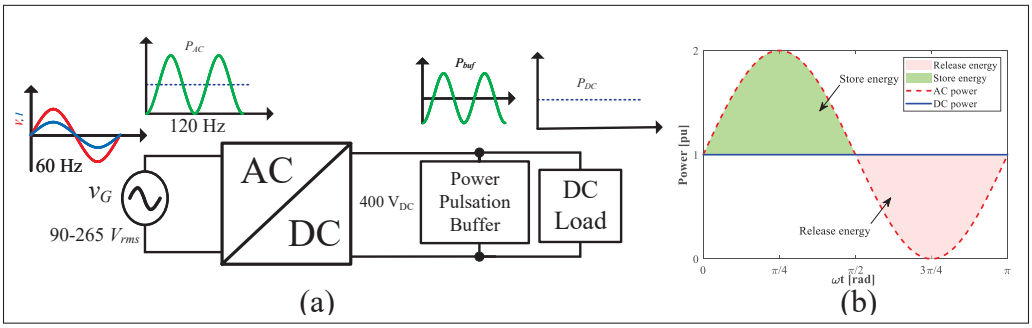


Figure 4.1 (a) Typical single-phase conversion system block diagram with PFC stage and buffering stage. (b) Typical AC-DC power waveforms and energy flow of the energy buffering device

Traditionally, single-phase power pulsations are buffered using large electrolytic DC-link capacitors due to their high capacitance and favorable volumetric and gravimetric energy densities (Instruments, 2024b). This required buffer capacitance C_{DC} (Fig. 4.2) cannot be reduced by increasing the switching frequency, as it depends on the power output, line frequency and desired voltage ripple.

$$C_{DC} \approx \frac{P_{DC}}{\omega_G V_{DC}\,\Delta V_{DC}} \tag{4.3}$$

where P_{DC} is the rated power of the converter, V_{DC} is the DC-link voltage, and ΔV_{DC} is the allowable peak-to-peak voltage ripple.

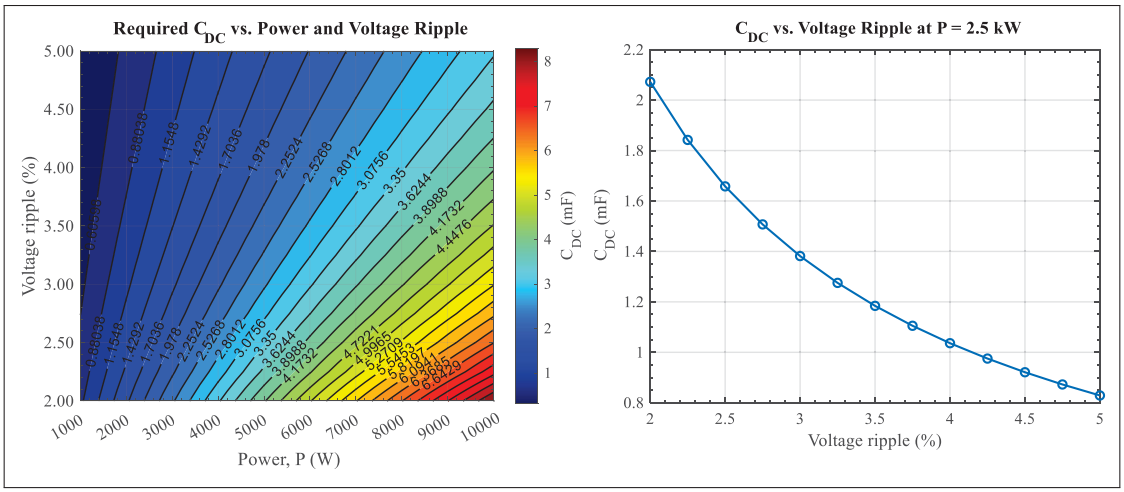


Figure 4.2 Required DC-link capacitance for single-phase 60 Hz, twice-line-frequency power decoupling versus output power and allowable voltage ripple; the right panel shows the capacitance–ripple trade-off at P_{DC} = 2.5 kW

While effective, aluminum electrolytic capacitors are bulky and, under high RMS current and elevated temperature, exhibit accelerated aging and reduced reliability (Brooks *et al.*, 2024). Additionally, as illustrated in Fig. 4.2, incremental increases in passive DC-link capacitance yield diminishing returns, particularly under tightly constrained voltage ripple requirements.

Active Power Pulsation Buffer (PPB) stages alleviate dependence on C_{DC} using film or ceramic capacitors, but they add power components and control overhead that can erode efficiency (Wang *et al.*, 2020a; Neumayr, Knabben, Varescon, Bortis & Kolar, 2021; Lei *et al.*, 2017). Moreover, the DC-link capacitor C_{DC} not only buffers $2\omega_G$ power pulsation; it also stabilizes V_{DC} during fast load transients by sourcing or absorbing sudden power imbalance. Active PPB circuits can reduce or eliminate C_{DC} while meeting steady-state ripple requirements, but the reduced DC-link energy can increase V_{DC} overshoot and undershoot during load steps unless the fast control explicitly compensates.

Recent works have investigated integrated PPB (iPPB) by repurposing embedded energy-storage elements (e.g., flying capacitors (FCs), AC filter capacitors (Serban, 2015), or DC split capacitors (Yao *et al.*, 2017)), thus avoiding additional components. Standard FC multilevel converters (Meynard & Foch, 1992) alternate FC charging and discharging states with fixed

voltage ratios at the switching frequency F_{sw}, enabling reduced FC size at higher switching frequencies (Lei *et al.*, 2017). The number of FC cells (N_c) determines the intermediate discrete voltage levels ($Nc + 1$), effectively multiplying the switching frequency at the boost inductor ($Nc \times F_{sw}$) and reducing the required switch voltage ratings (V_{DC}/Nc). Rather than tightly regulating FCs with fixed voltages, they can provide energy storage to buffer pulsating power. Buffered energy depends on FC capacitance, average voltage and voltage swing; with proper sizing, the topology requires no additional power components and can partially buffer single-phase pulsating power.

A cascaded two-stage three-level (3L) DC–DC FC converter paired with a two-level single-phase inverter has been proposed to achieve full power-pulsation compensation (Watanabe, Sakuraba, Furukawa, Kusaka & Itoh, 2018). Subsequently, a single-stage 3L-FC inverter that employs multiple control modes within each power cycle has been developed to enable integrated FC buffering (Ramos, Serrano, Alou, Oliver & Cobos, 2021). Low-power unidirectional 3L-FC buck–boost (Qi, Li, Tan & Hui, 2019a) and buck converters (Qi, Li, Yuan, Tan & Hui, 2019b) have been introduced, albeit with the trade-off of stricter operational constraints on the FC voltage and DC-link capacitor. An integrated FC-PPB for a unidirectional 3L PFC was demonstrated in (Menzi, Weihe, Anderson, Everts & Kolar, 2022), using a conventional current-loop/PWM framework with redundant switching states driven by the low-frequency inductor current; the 2.2 kW prototype reported a 28% DC-link ripple reduction. The approach is confined to a 3-level leg with partial buffering bounded by duty-ratio limits, leaving unquantified headroom for higher-level FC stages and discrete-state control strategies.

For high-power single-phase applications, the energy buffered by a single FC is insufficient for significant DC-voltage-ripple reduction. The buffer energy that an FC can exchange in one swing is $\Delta E \approx C\, V_{\text{avg}}\, \Delta V$. Higher-level FC stacks raise both V_{avg} (via larger internal discrete levels) and the number of capacitors contributing, while also multiplying the effective inductor-voltage steps and reducing per-device blocking stress, which is beneficial for PFC current tracking. A four-cell leg therefore unlocks materially more iPPB headroom than three-level variants without adding hardware, provided the controller can coordinate multiple dynamic FC voltages.

While previous research predominantly focused on three-level integrated PPB configurations (Menzi *et al.*, 2022; Qi *et al.*, 2019a; Ramos *et al.*, 2021; Qi *et al.*, 2019b; Watanabe *et al.*, 2018), extending this concept to higher-level FC converter structures has been limited by the challenge of simultaneously controlling multiple dynamic FC voltages and the inductor current. Moreover, the conventional phase-shifted pulse width modulator (PS-PWM), while effective for natural voltage balancing in symmetric FC converters, fails with asymmetric dynamic voltage ratios, leading to improper switching-state selection, degraded grid current quality, and the need for larger boost inductance. Model predictive control (MPC) (Karamanakos & Geyer, 2020), with its inherent capability to handle multi-objective dynamic references and deliver superior transient performance under external disturbances without a modulator, is therefore a promising solution for controlling higher-level FC iPPB converters.

However, implementing MPC at practical sampling periods in single-phase front-ends is challenging. Desirable high effective switching frequencies (for smaller passives) increase computational burden, and real-time execution often motivates specialized hardware (Karamanakos *et al.*, 2020). Microcontroller-based realization requires fixed-time algorithms, careful task partitioning, and explicit delay compensation in the predictors. While FPGAs and Rapid Control Prototyping (RCP) systems (e.g., dSPACE) offer parallel processing, FPGAs face communication bottlenecks with other processing units, and RCPs are not viable for commercial designs.

The key contributions of this research are:

1. *Integrated PPB in a 4-cell FC PFC.* An iPPB scheme embedded in the existing FC stack of a single-phase TP–4CFC rectifier transfers ripple energy away from C_{DC} while maintaining multilevel voltage sharing.
2. *Weighted-sum MOMPCC with adaptive FC references.* A modulator-free MPC tracks grid current while regulating dynamic FC voltages using a tuned multi-term objective and an adaptive bang–bang FC-reference generator tied to instantaneous power deviation.
3. *Real-time implementation.* Implementing MOMPCC on a low-cost microcontroller achieving the fastest reported sampling time of 6.66 μs for a four-cell FC converter.

4. *Experimental demonstration.* This work presents the first practical demonstration of a 2.5 kW single-phase bidirectional converter used as an integrated power pulsation buffer, achieving a 50% reduction in DC–link voltage ripple and 2.47% THD, with robust dynamic performance for applications such as electric vehicle onboard chargers and server power supplies.

This chapter is organized as follows. Section II presents the TP-4CFC converter topology and the integrated PPB concept. Section III develops the continuous- and discrete-time models and details the MOMPCC strategy. Section IV discusses the simulation results. Section V describes the hardware prototype, real-time implementation and experimental validation. Finally, Section VI concludes the paper.

4.2 PFC Topology Description with PPB Embedded Control

4.2.1 Circuit Description

As previously discussed, the integrated PPB TP-4CFC converter requires no additional hardware modifications. Fig. 4.3 illustrates the topology of a bidirectional single-phase totem-pole four-cell flying-capacitor (TP-4CFC) converter. The converter consists of two legs: the first, a low-frequency (LF) unfolder leg equipped with two switches (S_{ap} and S_{an}), and the second, a high frequency (HF) four-cell FC leg, which includes eight switches (S_{1p}, S_{2p}, S_{3p}, S_{4p}, S_{1n}, S_{2n}, S_{3n}, S_{4n}). In this configuration, the three flying capacitors (C_1, C_2 and C_3) are repurposed to function as energy buffers, enabling effective mitigation of power pulsations.

4.2.2 Operating Principle

The LF leg is switched based on the polarity of the grid voltage, whereas the HF FC leg is actively controlled to simultaneously achieve PFC and partial PPB objectives by tracking predefined current and capacitor voltage references. Both legs consist of complementary switch pairs S_{xp} and S_{xn} (where $x = a, 1, 2, 3$), ensuring that only one switch within each pair conducts at a given

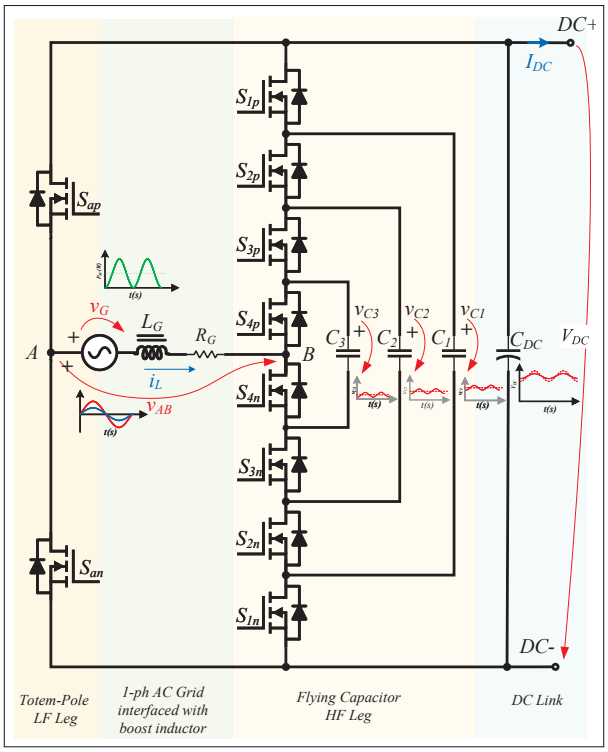


Figure 4.3 Configuration of the single-phase bidirectional totem-pole four-cell flying capacitor (TP-4CFC) PFC rectifier illustrating key waveforms in integrated PPB operation by solid lines and standard operation by dotted lines

moment. Thus, the conduction state of each pair can be represented by a single binary switching function:

$$S_x(t) = \begin{cases} 1, & \text{if } S_{xp} \text{ is on and } S_{xn} \text{ is off} \\ 0, & \text{if } S_{xp} \text{ is off and } S_{xn} \text{ is on} \end{cases} \tag{4.4}$$

During standard operation without PPB functionality, the FC voltages are regulated in a fixed ratio $V_{DC} : V_{C1} : V_{C2} : V_{C3} = 4 : 3 : 2 : 1$. Under these conditions, the converter generates nine discrete voltage levels (including negative levels) at its output, enabling precise voltage synthesis. Current tracking is accomplished by controlling the voltage across the input inductor v_L, which is represented by $v_{AB} - v_G$, where the converter voltage is defined by:

$$v_{AB} = (S_a - S_1)V_{DC} + (S_1 - S_2)V_{C1} + (S_2 - S_3)V_{C2} + (S_3 - S_4)V_{C3}. \tag{4.5}$$

The proposed control strategy is split in three primary components: (1) An outer voltage loop generating the current reference, (2) A partial PPB voltage reference generation scheme, and (3) The multi-objective current controller. Each section of the control is shown in the Fig. 4.4 and will be discussed in detail in the subsequent section.

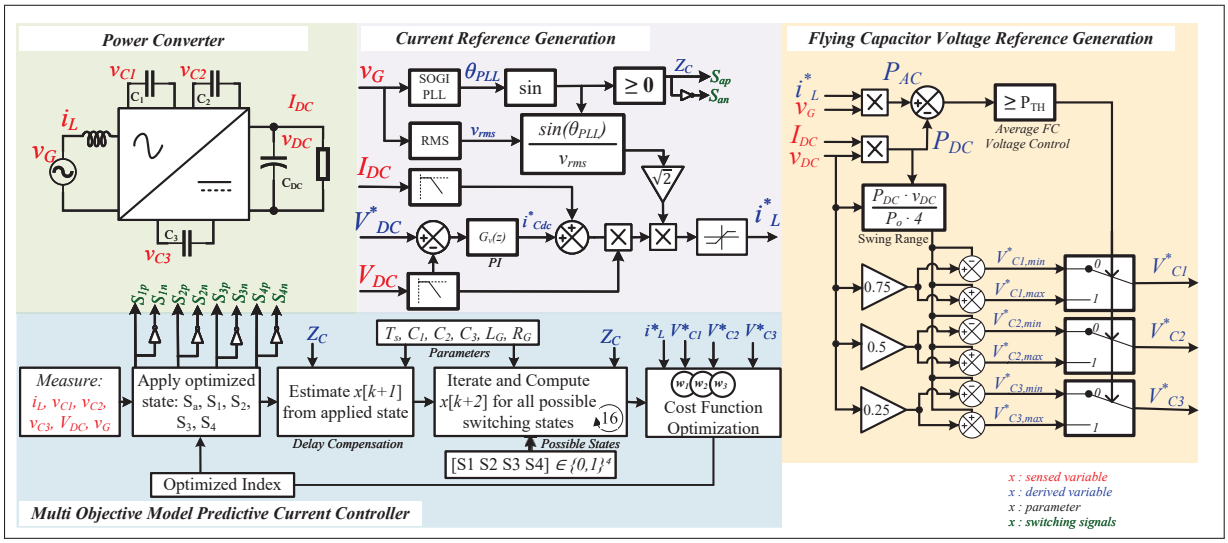


Figure 4.4 Detailed control diagram illustrating the MOMPCC methodology for integrated PPB operation

4.2.3 PFC Current Reference Generation

MOMPCC requires a low-harmonic, in-phase current reference i_L^* to enforce unity power factor and low THD. Phase θ_{PLL} is obtained from a PLL based on an adaptive notch filter (Bhardwaj, 2013), and its zero crossings also drive the LF totem-pole leg. To accommodate wide input and load variation, the sinusoidal template is normalized by the line-cycle rms v_{rms} (Qin *et al.*,

2019), with DC-load feedforward I_{DC}. The reference is

$$i_L^*(t) = \frac{\sqrt{2}\,V_{DC}(t)}{v_{\text{rms}}}\left[I_{DC}(t) + i_{Cdc}^*(t)\right]\sin\!\left(\theta_{\text{PLL}}(t)\right). \tag{4.6}$$

Meanwhile, the outer voltage loop utilizes a proportional-integral (PI) controller, operating at a bandwidth below 10 Hz, to regulate the DC output voltage (here 400 V) by generating i_{Cdc}^*.

$$i_{Cdc}^*(t) = K_p\left[V_{DC}^* - V_{DC}(t)\right] + K_i\int_0^t \left[V_{DC}^* - V_{DC}(\tau)\right]d\tau \tag{4.7}$$

To suppress $2\omega_G$ and $4\omega_G$ feedthrough, the sampled V_{DC} and I_{DC} inputs are prefiltered by narrow notches at $2\omega_G$ and $4\omega_G$, followed by a short moving average.

4.3 Proposed Integrated PPB Control

The MOMPCC employs a model-based control strategy that originates from the online optimization of the dynamic performance behavior of the current system states, considering future state references (Karamanakos *et al.*, 2020; Patel & Chandra, 2024). It evaluates a cost function to choose the optimal switching state that provides the best response within the given constraints. A significant advantage of this control scheme is that it eliminates the need for a switching pulse modulator.

MOMPCC is utilized here for tracking the unity power factor grid current reference generated by the outer slow loop which regulates the dc-link voltage. The PPB function is realized by actively controlling the charging and discharging of the FC to serve as an energy buffer. This integrated approach allows MOMPCC to simultaneously optimize current tracking and the PPB function. Thus, MOMPCC effectively addresses the challenges associated with modulation for multi-switch power converter and achieves efficient PPB functionality.

4.3.1 Modeling of the TP-4CFC PFC Converter

4.3.1.1 Continuous-time Model

To derive a continuous-time model of the TP-4CFC converter, we firstly denote: $u(t) = \begin{bmatrix} S_a(t) & S_1(t) & S_2(t) & S_3(t) & S_4(t) \end{bmatrix}^T$ as the system input. Equations (4.8)-(4.9) capture inductor and flying-capacitor voltage dynamics as functions of the switch states.

$$C_k \dot{v_{Ck}}(t) = i_L(t) \cdot (S_k(t) - S_{k+1}(t)) \qquad k \in 1, 2, 3 \tag{4.8}$$

$$L_G \dot{i_L}(t) + R_G i_L(t) = (S_a(t) - S_1(t))V_{DC}(t) + \sum_{k=1}^{3} (S_k(t) - S_{k+1}(t))V_{Ck}(t) - v_G(t) \tag{4.9}$$

Represent in matrix form,

$$\dot{x} = Ax(t) + Bx(t)u(t) + Ev_G(t) \tag{4.10}$$

$$A = \begin{bmatrix} 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & -\frac{R_G}{L_G} \end{bmatrix}, \quad g = \begin{bmatrix} 0 \\ 0 \\ 0 \\ -\frac{1}{L_G} \end{bmatrix},$$

$$B(x(t)) = \begin{bmatrix} 0 & \frac{i_L}{C_1} & -\frac{i_L}{C_1} & 0 & 0 \\ 0 & 0 & \frac{i_L}{C_2} & -\frac{i_L}{C_2} & 0 \\ 0 & 0 & 0 & \frac{i_L}{C_3} & -\frac{i_L}{C_3} \\ \frac{V_{DC}}{L_G} & -\frac{V_{DC}}{L_G} + \frac{v_{C1}}{L_G} & -\frac{v_{C1}}{L_G} + \frac{v_{C2}}{L_G} & -\frac{v_{C2}}{L_G} + \frac{v_{C3}}{L_G} & -\frac{v_{C3}}{L_G} \end{bmatrix}_{4\times5}.$$

4.3.1.2 Discrete-time Model of the TP-4CFC PFC Converter

Considering the discrete system state as $x[k] = \begin{bmatrix} v_{C1}[k] & v_{C2}[k] & v_{C3}[k] & i_L[k] \end{bmatrix}^T$ and the control input as $u[k] = \begin{bmatrix} S_a[k] & S_1[k] & S_2[k] & S_3[k] & S_4[k] \end{bmatrix}^T$, the discrete-time state-space model of the TP-4CFC converter is obtained by discretizing its continuous-time equations (4.8)-(4.9) using the forward Euler approximation with a sampling period T_s (Lezana, Aguilera & Quevedo, 2009; Patel & Chandra, 2024). The resulting discrete-time affine-bilinear state-space equation can be represented in the matrix form as follows:

$$x[k+1] = Ax[k] + B(x[k])u[k] + g \tag{4.11}$$

$$A = \begin{bmatrix} 1 & 0 & 0 & 0 \\ 0 & 1 & 0 & 0 \\ 0 & 0 & 1 & 0 \\ 0 & 0 & 0 & \alpha \end{bmatrix}, \quad g = \begin{bmatrix} 0 \\ 0 \\ 0 \\ \beta v_G[k] \end{bmatrix},$$

$$B(x[k]) = \begin{bmatrix} 0 & \frac{T_s}{C_1} i_L[k] \\ 0 & 0 \\ 0 & 0 \\ -\beta V_{DC}[k] & \beta(V_{DC}[k] - v_{C1}[k]) \end{bmatrix}$$

$$\begin{bmatrix} -\frac{T_s}{C_1} i_L[k] & 0 & 0 \\ \frac{T_s}{C_2} i_L[k] & -\frac{T_s}{C_2} i_L[k] & 0 \\ 0 & \frac{T_s}{C_3} i_L[k] & -\frac{T_s}{C_3} i_L[k] \\ \beta(v_{C1}[k] - v_{C2}[k]) & \beta(v_{C2}[k] - v_{C3}[k]) & \beta v_{C3}[k] \end{bmatrix}_{4\times 5} \tag{4.12}$$

with parameters defined as $\alpha = 1 - \frac{R_G T_s}{L_G}$ and $\beta = \frac{Ts}{L_G}$. Equation (4.11) and (4.12), will be utilized to estimate the future system states $x[k+1]$ and $x[k+2]$ using sensed variables ($v_G[k]$, $V_{DC}[k]$, $i_L[k]$, $v_{C1}[k]$, $v_{C2}[k]$, $v_{C3}[k]$, $i_L[k]$) and system parameters (L_G, R_G, C_1, C_2, C_3).

4.3.2 Delay Compensation

In practical digital implementation using a real-time microcontroller, the delay between the measurement of system states and the application of the updated switching state is typically close to one full sampling cycle, as the control algorithm utilizes nearly the entire available computation time to maximize CPU performance.

To effectively manage computational delays in digital real-time implementation, a delay-compensation strategy (Cortes, Rodriguez, Silva & Flores, 2012) is incorporated into the MOMPCC algorithm. This strategy accounts for the computational interval by applying the optimized switching state at the next sampling instant. The method is outlined in Algorithm 4.1.

Algorithm 4.1 MOMPCC with delay compensation control

1 Measure i_L, v_{C1}, v_{C2}, v_{C3}
2 Apply the switching state calculated in the previous interval
3 Estimate $x[k+1]$ considering the applied switching state using Eq. 4.11
4 Predict $x[k+2]$ for the next sampling instant for all possible switching states
5 Evaluate the cost function for each prediction
6 Select the switching state that minimizes the cost function

4.3.3 Flying Capacitor Voltage Reference Generation

The voltages of the FCs are regulated by the inductor current i_L flowing in and out of each capacitor controlled by redundant switching states. However, this control becomes ineffective when the grid current approaches zero, i.e. near zero crossing. As a result, the integrated PPB functionality in the TP-4CFC converter cannot achieve full energy buffering but instead focuses on reducing the dc-link voltage ripple, thereby fulfilling the objective of minimizing the required dc-link capacitance C_{DC}.

The reference voltage for each flying capacitor is derived using a bang-bang-type control based on the instantaneous power difference, adapted from the method described in (Menzi *et al.*, 2022). The approach measures the instantaneous power difference between the time-varying input $P_{AC}(t) = i_L(t).V_G(t)$ and the constant output power $P_{DC} = V_{DC}.I_{DC}$. To ensure noise-free power measurements, the reference inductor current (i_L^*) is used instead of the direct measurement i_L.

$$V_{Cx}^* = \begin{cases} V_{Cx,min}^*, & if\ (P_{AC}(t) - P_{DC}) \leq P_{th} \\ V_{Cx,max}^*, & otherwise \end{cases}$$
$$for\ x = 1, 2, 3 \tag{4.13}$$

Introducing the threshold power P_{th} adds an extra degree of freedom, effectively controlling the charging and discharging durations of the FC, and thus influencing its average voltage.

Overcompensation of buffered energy can lead to increased ripple due to excessive charging or discharging. To mitigate this, a swing factor is introduced to derive the $V_{cx,min}$ and $V_{cx,max}$ values. This factor linearly scales down the minimum/maximum FC reference values based on the current power level.

4.3.4 Cost Function and Weighting Factor Selection

In TP-4CFC converter, accurate current tracking with minimal ripple remains the primary control objective since it directly determines the system's performance and power quality. The FCs serve as energy buffers and thus can be assigned lower priority. To handle these multi-priority objectives, a MOMPCC strategy is employed, leveraging its ability to assign different priority levels via weighting factors(Cortes *et al.*, 2009). Given that current distortion is dependent on effective voltage tracking, especially in higher-level FC topologies, the weighting factors in the MPC cost function must be strategically prioritized, assigning the highest priority to V_{C1}, then V_{C2}, and lastly V_{C3}. Determining optimal weighting factors becomes increasingly complex with additional constraints and disparate magnitude errors. Consequently, a Simulink® sensitivity analyzer approach is employed as shown in the Fig. 4.5, utilizing large set of randomly generated weighting factors in known ranges for FC capacitors across numerous offline simulations. The current weighting factor remains constant at 1, while the weighting factors of FCs are optimized to minimize the Total Harmonic Distortion (THD) of the current waveform and DC-link voltage ripple, enabling precise calibration of the MPC cost function to achieve optimal control performance. Note that V_{DC} is excluded from the cost function because the outer loop already regulates the dc-link.

$$G = \left(i_L^* - i_L[k+2]\right)^2 + w_1\left(V_{C1}^* - v_{C1}[k+2]\right)^2 + w_2\left(V_{C2}^* - v_{C2}[k+2]\right)^2 + w_3\left(V_{C3}^* - v_{C3}[k+2]\right)^2 \tag{4.14}$$

where, w_1, w_2, and w_3 are weight factors for the individual constraints in the cost function G.

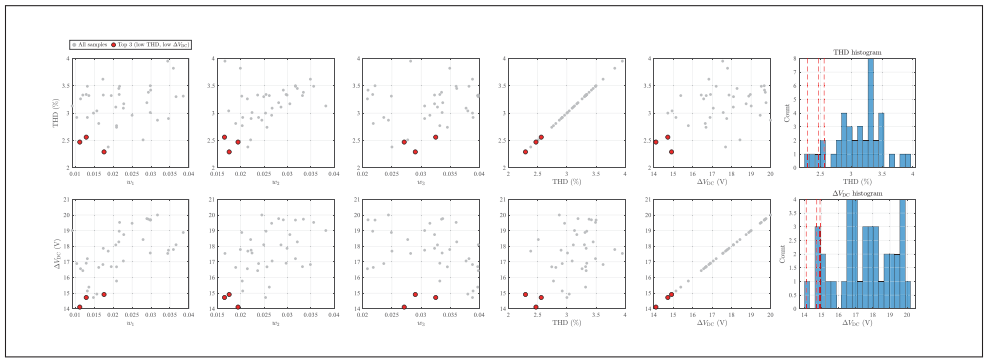


Figure 4.5 Scatter plots of iTHD and DC-link ripple (ΔV_{DC}) versus the MPC weighting factors w_1, w_2 and w_3, together with their marginal histograms. Gray markers represent all offline simulations obtained from random weighting-factor sweeps within prescribed ranges, whereas red markers highlight the three best candidates that jointly minimize THD and (ΔV_{DC})

4.4 Simulation Results

The converter specification and control parameters designed for the simulation studies are detailed in Table 4.1.

For comparison, the initial simulation in Fig. 4.6 shows the waveform of a MOMPCC-controlled PFC rectifier under standard operation. In this scenario, the FCs are actively regulated to maintain a constant nominal voltage ratio of $V_{DC} : V_{C1} : V_{C2} : V_{C3} = 4 : 3 : 2 : 1$, which ensures low voltage stress for FC leg switches but does not provide any PPB by FCs. The voltage ripple considering only energy buffer by DC-link capacitance of $540\mu F$ is 28.8V. The THD of the grid current is observed to be 1.7% with a $250\mu H$ inductor and maximum switching frequency of $100kHz$.

Table 4.1 Simulation Parameters

Parameter Description	Value
Grid Voltage (v_G)	230 V AC RMS, 60Hz
Grid filter inductor (L_G)	$250\mu H$
DC-link Capacitance (C_{dc})	$540\mu F$
Flying Capacitance (C_1, C_2, C_3)	$50\mu F$
DC-link Voltage (V_{DC})	$400V$, 4% Regulation
Nominal Load Power (P_o)	$2.2kW$
Sampling Time (T_s)	5 μS
Maximum Switching Frequency	$100kHz$
Weighting Factors (w_1, w_2, w_3)	0.0112, 0.0194, 0.0271

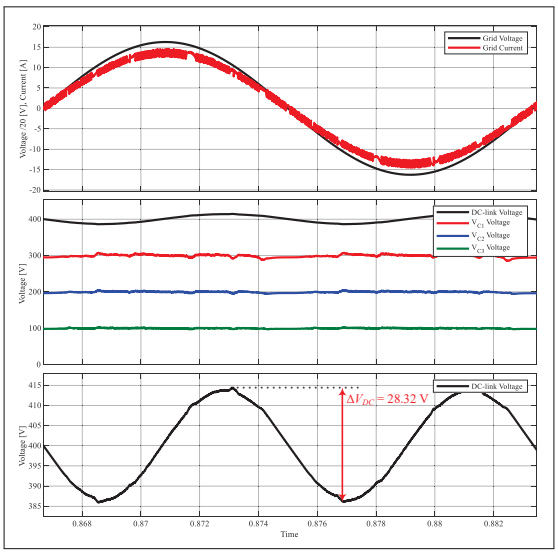


Figure 4.6 Simulated waveforms for the TP-4CFC PFC rectifier under standard operation without PPB functionality controlled by MOMPCC, with grid voltage V_G = $230Vrms$, grid frequency f_G = 60 Hz, DC-link voltage V_{DC} = 400 V, and nominal output power P_{DC} = 2.2 kW. Flying capacitor voltage references are set to V^*_{C1} = 300 V, V^*_{C2} = 200 V, and V^*_{C3} = 100 V. Observed DC-link voltage ripple ΔV_{DC} = 28.8 V

Fig. 4.7 presents the simulated waveforms of TP-4CFC PFC rectifier with integrated PPB functionality under similar conditions. It is observed that the FC voltages dynamically charge and

discharge, effectively functioning as energy buffers to enable PPB resulting in a 53% reduction of DC-link voltage ripple from 28.8 V to 13.52 V. Furthermore, when considering the combined capacitance ($C_{DC} + C_1 + C_2 + C_3 = 690\mu F$), the overall capacitance reduction achieved by integrating PPB functionality in the TP-4CFC topology is quantified to exceed 36.05%, since for achieving the same 13.52 V ripple without PPB, a capacitance of 1.08 mF would have been required.

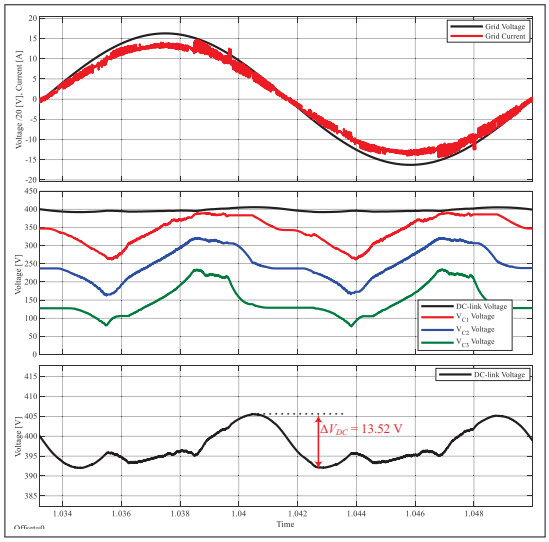


Figure 4.7 Simulated waveforms for the TP-4CFC PFC rectifier demonstrating integrated PPB functionality under identical grid and DC-link conditions as Fig. 5.4. Voltage ripple is significantly reduced to $\Delta V_{DC} = 13.52V$, showcasing effective energy buffering

However, the PPB functionality results in variable flying capacitor voltages, subsequently increasing the switch voltage ratings. Despite this, the grid-current THD under MOMPCC remains acceptable at 2.3%. Moreover, the 5 μs MOMPCC sampling interval limits the FC switches' minimum on-off cycle to 10 μs (100 kHz peak switching frequency). Fig. 4.8 illustrates the variable switching frequency, showing integrated PPB operation reduces average switching frequency and enhances system efficiency.

Fig. 4.9 illustrates converter performance under reduced grid voltage operation (120 V RMS) with integrated PPB. The DC-link ripple remains stable at 13.53 V. It is important to highlight that the controllability of the flying capacitors is proportional to the ratio I_L/C_x. Consequently,

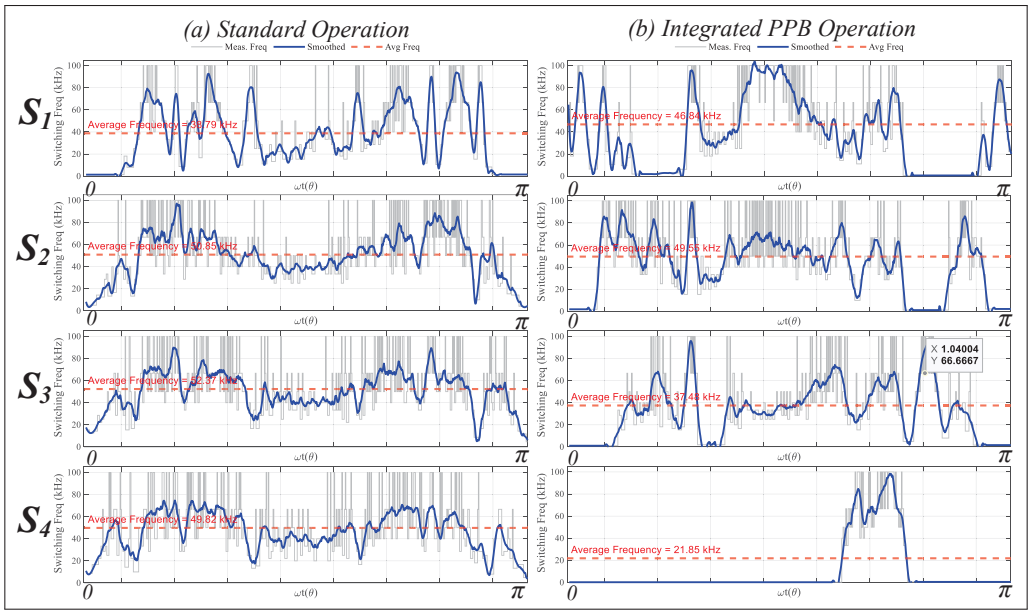


Figure 4.8 Instantaneous Switching frequency profiles over half power cycle of FC leg HF switches S_1— S_4 under (a) standard and (b) integrated PPB operations

ideal buffering performance is achieved during capacitor charging periods due to finite inductor current. However, during discharging intervals, the capacitor voltages become relatively constant as the grid current approaches zero near zero-crossings, temporarily reducing the buffering effectiveness. A similar phenomenon can be observed under reduced voltage operation (120 V RMS, Fig. 4.9), where smoother FC voltage waveforms are noted.

The dynamic robustness of the proposed integrated PPB control are validated under various operating conditions, as depicted in Fig. 4.10–4.11. During load transients between 2.2 kW and 1.7 kW, the DC-link and FCs quickly adjust, demonstrating stable and robust transient behavior (Fig. 4.10). Furthermore, when subjected to a dynamic DC-link voltage reference step from 400 V to 450 V, the system rapidly achieves the new setpoint due to reduced DC-link capacitance and the inherent fast dynamics of MOMPCC, confirming the proposed controller's excellent transient response (Fig. 4.11).

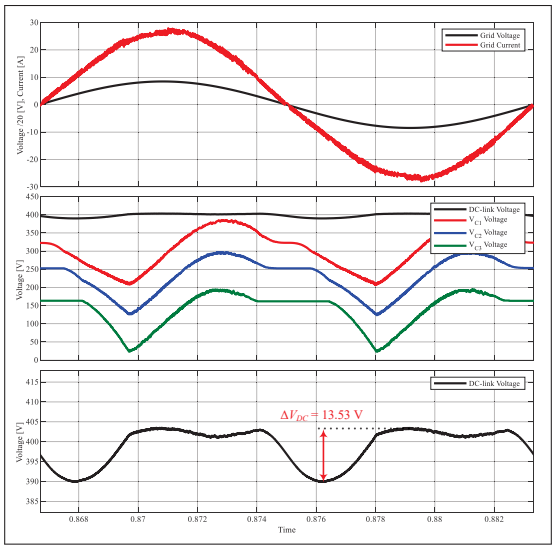


Figure 4.9 Simulated waveforms at reduced grid voltage (120 V RMS) with integrated PPB. DC-link ripple remains effectively controlled at 13.53 V

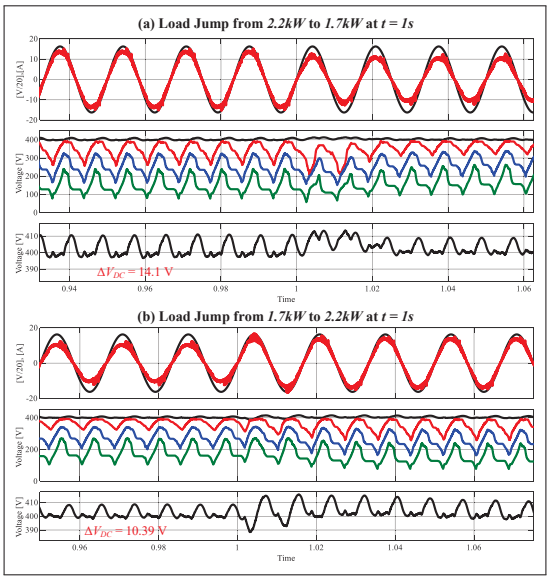


Figure 4.10 (a): Dynamic load reduction from 2.2 kW to 1.7 kW at t = 1 s under integrated PPB operation. DC-link voltage ripple reduces from 14.1 V to 10.39 V, showing adaptive buffering capability. (b): Dynamic load increase from 1.7 kW to 2.2 kW at t = 1 s under integrated PPB operation. DC-link voltage ripple adjusts from 10.39 V to 14.1 V, demonstrating effective transient response

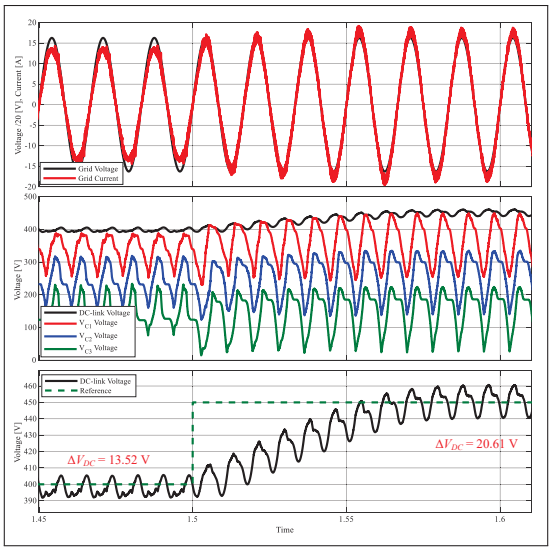


Figure 4.11 System response to dynamic DC-link voltage reference change from $V_{DC} = 400V$ to $450V$ during PPB operation. Due to smaller DC-link capacitance and faster dynamics of MOMPCC, the response is rapid

4.5 Hardware Implementation and Experimental Verification

4.5.1 Hardware Prototype and Experimental Setup

Key hardware components and their specifications are summarized in Table 4.2. The prototype consists of a power converter board housing silicon carbide (SiC) MOSFETs, three film-capacitor-based flying capacitors (FCs), a filter inductor, and gate-driver circuits. The power stage interfaces with a control and measurement board, which incorporates the TMS320F28379D MCU, high-voltage current and voltage sensors, and low-voltage analog circuits for signal conditioning, buffering, and hardware protection.

An overview of the complete laboratory experimental setup, including testing equipment, is presented in Fig. 4.12. A Chroma 61508 programmable AC source (4.5 kVA) provides the grid-side input, while a resistive load bank emulates a constant-power DC load. Computational performance and control timing are validated using a logic analyzer.

Table 4.2 Component listing for TP–4CFC integrated PPB prototype

Component	Part No.	Parameters
SiC MOSFET	10×SCT3120ALHR	650 V, 120 mΩ
Isolated gate drivers	10×UCC23514	5 kV_{rms}, 4 A / 5 A
Voltage sensing	5×AMC3330QDWERQ1	Isolation amplifier
Current sensor	2×CT426-HSN820MR	±20 A
Boost inductor	1×760801101	250 μH, 36 mΩ
Flying capacitors	3×C4AQLBW5900A3OK	90 μF, 500 V
DC-link capacitor	1×B43548A5567M060	480 μF^*, 450 V
Microcontroller	1×TMS320F28379D	200 MHz, 2×C28

4.5.2 Embedded Real time Implementation and Control Partitioning

Implementing the proposed MOMPCC strategy in real time on the TMS320F28379D microcontroller (MCU) demands completing the measurements, entire online optimization and switching-state application within each $6.66\mu s$ control interval. To overcome the computational bottleneck inherent to such a short sampling period on a 200 MHz MCU, we exploit the device's dual-core architecture and its dedicated Control Law Accelerator (CLA) co-processor. By carefully partitioning functions between CPU1, CPU2, and the CLA, all requisite tasks are executed deterministically without exceeding the allowable cycle budget. Fig. 4.13 illustrates the overall implementation on the F28379D MCU.

A 150 kHz ePWM triggers simultaneous ADC conversions, with hardware offset compensation and DMA for direct, zero-wait-state RAM access, minimizing latency. CPU1 manages all real-time critical tasks—ADC data processing, delay compensation, MOMPCC optimization, and output updates. The optimization iteration computation for MOMPCC is split between the CLA and CPU1 core, enabling parallel cost-function evaluations. At each control cycle, an interrupt-driven arbitration selects the optimal result from parallel execution paths of CPU1 and CLA. Since discrete switching states are generated (not duty cycles), standard ePWM modules are bypassed; dead time is implemented in software using atomic port writes.

In parallel, CPU2 handles auxiliary functions: at 150 kHz, it performs PLL synchronization, zero-crossing detection, FC voltage reference updates, and protection, precisely aligned to CPU1

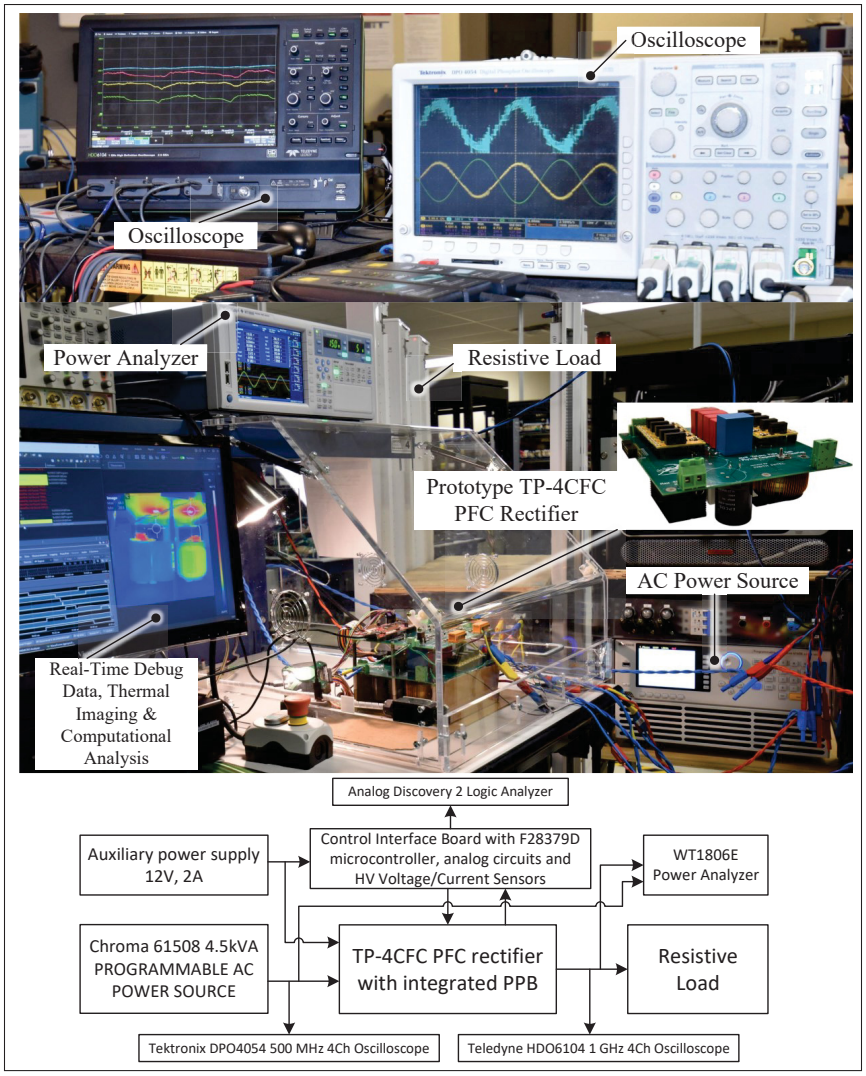


Figure 4.12 Laboratory test bench for the TP-4CFC PFC rectifier with integrated PPB, showing the power stage and control interface under test, instrumentation (oscilloscopes, power analyzer), programmable AC source, resistive load, and real-time debug and thermal imaging

cycles. At 10 kHz, CPU2 runs the outer voltage regulation loop and power measurement. To prevent current overshoot at grid voltage zero crossings, CPU2 temporarily disables PWM outputs. Frequently accessed variables and switching states are stored in zero-wait-state RAM for rapid access. Inter-core data exchange—ADC/MPC states (CPU1→CPU2), voltage references, zero-crossing, and current references (CPU2→CPU1)—is managed via the MCU's IPC peripheral with handshake at 150 kHz..

Appendix I lists the C firmware implementing the MOMPCC for iPPB single-phase TP-4CFC PFC converter on the Texas Instruments TMS320F28379D microcontroller.

The implementation architecture exploits the full potential of the F28379D MCU to implement the entire control strategy on single MCU without requiring an FPGA, making the solution cost-effective and easier to reproduce for industrial adoption.

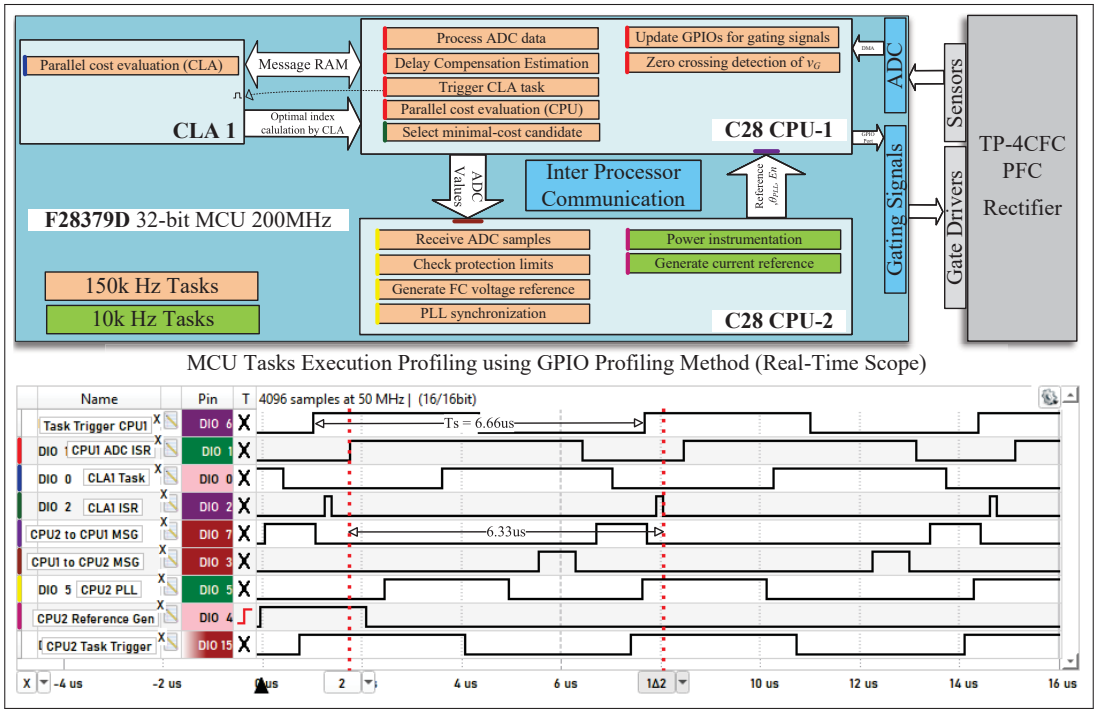


Figure 4.13 Computational timing performance of the F28379D MCU implementation, obtained via GPIO-based task profiling. Top: Functional block diagram of the dual-core + CLA implementation, highlighting how tasks are partitioned between CLA, CPU1, and CPU2. Bottom: Oscilloscope capture of GPIO toggles at a 150 kHz sampling rate (T_s = 6.66μs), showing the sequencing of task triggers, CLA and CPU ISRs, inter-processor communication, PLL updates, and reference-generation routines. Note that the task trigger pulses for CPU1 and CPU2 mark only the start of each cycle and not the internal compute durations

4.5.3 Experimental Results

4.5.3.1 230 V_{rms} AC to 400V DC Operation

Fig. 4.14 compares the converter's performance with and without integrated PPB under nominal grid conditions (230$Vrms$, 60Hz). Enabling PPB reduces the DC-link voltage ripple by 50%, lowering the stress on the electrolytic capacitor and extending its expected lifetime by reducing both RMS current and temperature oscillations. The grid-current THD remains low (2.85%), with only a marginal increase due to the asymmetry in the FC voltages. By enabling PPB, certain flying-capacitor switch pairs remain idle during portions of each cycle, which reduces the switching losses in the FC leg, leading to $\sim$ 1% improvement in overall converter efficiency.

4.5.3.2 120 V_{rms} AC to 400V DC Operation

Fig. 4.15 shows the operation under reduced grid voltage conditions of 120V_{rms}, confirms the PPB scheme's robustness and effectiveness across a wide range of grid conditions.

4.5.3.3 Load Change Dynamics

Fig. 4.16 illustrates the converter's response to step changes in output power—from 1 kW up to 2.2 kW and back down to 1.2 kW—under integrated PPB operation. The MOMPCC strategy swiftly adjusts the allowed voltage swing of the flying capacitors to match the new energy buffering requirement based on current power level. By scaling the swing factor in real time, the algorithm avoids excessive charging or discharging of the capacitors that could otherwise amplify ripple when the load changes. At the same time, the DC-link voltage deviation remains small, demonstrating the controller's ability to suppress overshoot/undershoot.

4.5.3.4 Load Disturbance Rejection

As shown in Fig. 4.17, owing to the load feedforward current reference generation and the high bandwidth of the MOMPCC algorithm, the converter settles a massive 2.3 kW load change in

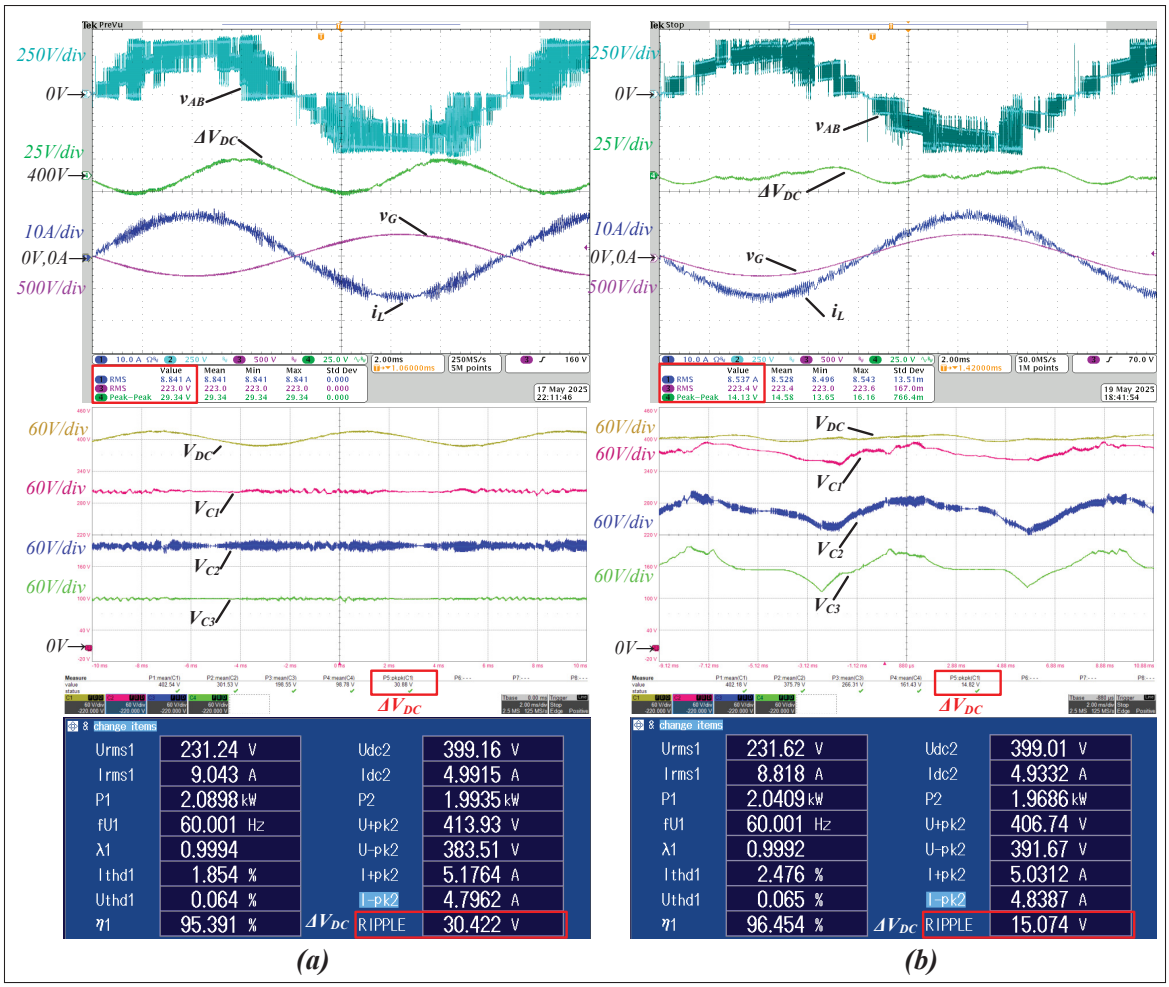


Figure 4.14 Experimental comparison at v_G= 230V_{rms}, 60Hz; V^*_{DC} = 400V, P_{DC} = 2 kW: (a) standard operation with fixed capacitor references controlled by MOMPCC; (b) integrated PPB enabled. Top rows: inverter leg voltage, DC-link voltage ripple, grid voltage, and inductor current. Middle rows: flying capacitor voltages and DC-link voltage. Bottom panels: power-analyzer screenshot showing DC-link ripple and efficiency metrics. Enabling PPB reduces the DC-link ripple from 30.42V to 15.07V

under 50 ms. Under light-load conditions, the swing is minimized, so the capacitor voltages remain nearly constant, avoiding unnecessary charging and discharging.

4.5.3.5 Reference Change Dynamics

Fig. 4.18 presents the transient response of the TP-4CFC PFC rectifier to step changes in the DC-link voltage reference under integrated PPB operation. The MOMPCC strategy effectively

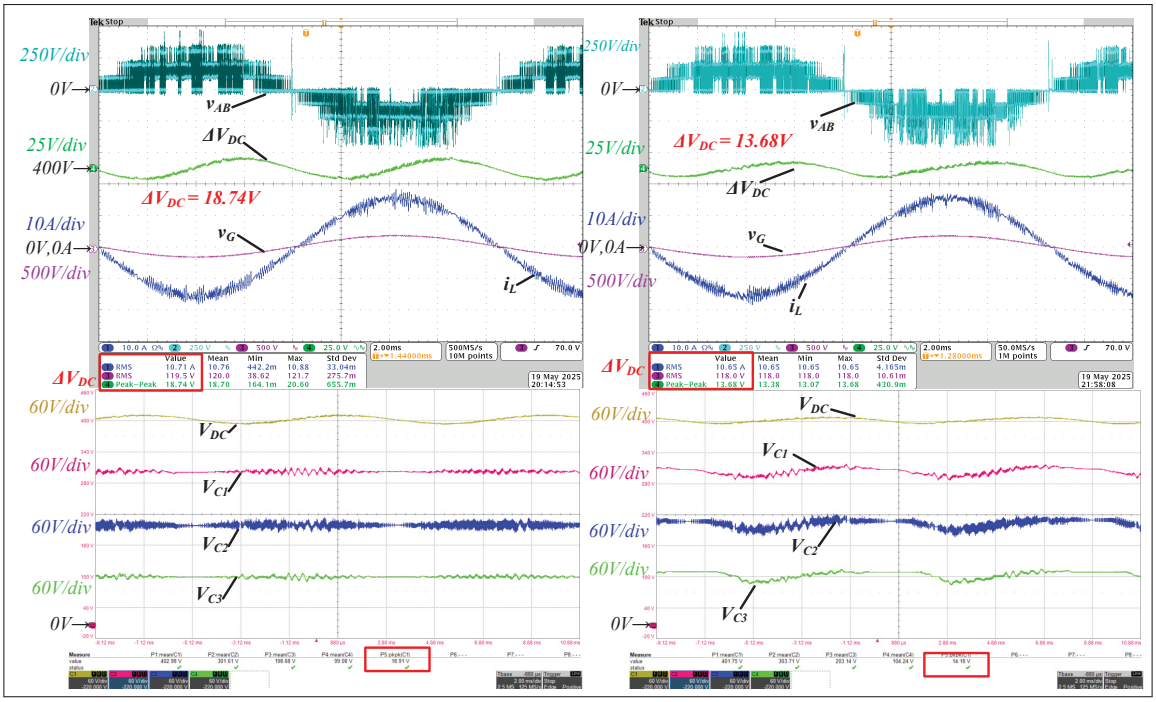


Figure 4.15 Experimental waveforms comparing standard operation (left) and integrated PPB operation (right) under MOMPCC control at reduced grid voltagev_G= 120 V_{rms}, 60Hz, P_{DC} = 1.2 kW. Enabling PPB reduces the DC-link ripple from 18.74V to 13.68V, demonstrating effective pulsation buffering

regulates the output voltage to the new setpoints within approximately 200 ms, demonstrating fast dynamic performance. The variation in FC voltages during the transition highlights the coordinated energy buffering based on load conditions.

These experimental results validate the effectiveness of the proposed integrated PPB with MOMPCC strategy, emphasizing stable operation, rapid transient response, and suitability for implementation on a cost-effective MCU platform.

4.5.4 Comparison

Table 4.3 summarizes two key aspects of this work: (a) the performance of integrated PPB converter topologies that use only embedded energy storage, and (b) the hardware metrics of various MPC implementations for FC PFC converters. Only active PPB topologies that use

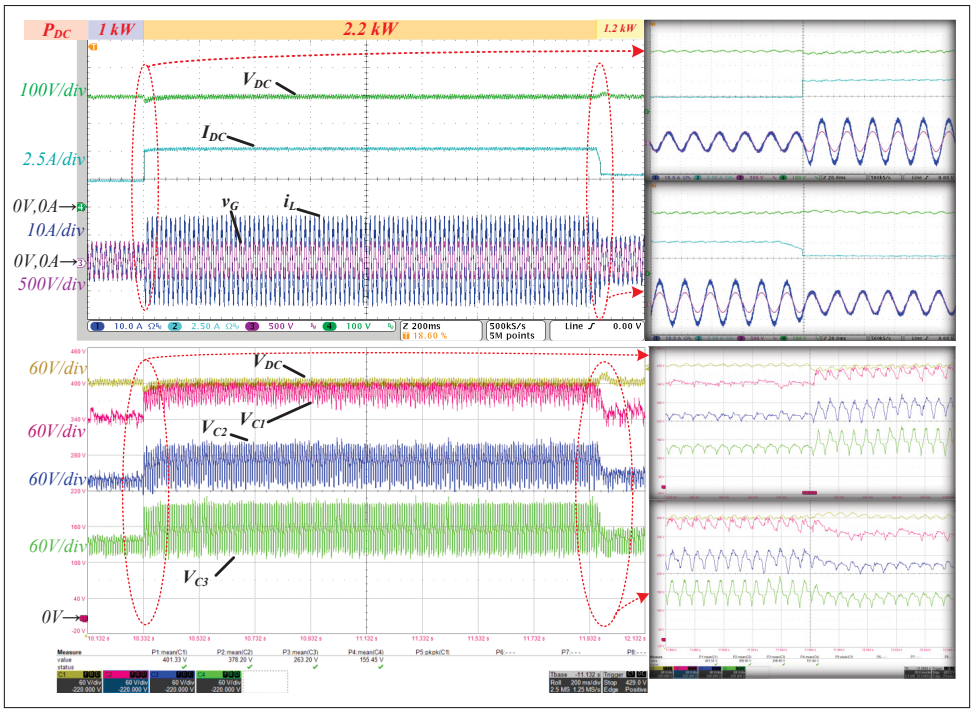


Figure 4.16 Experimental waveforms showing the dynamic load-response under integrated PPB operation. The output power P_{DC} is stepped from 1 kW to 2.2 kW and then to 1.2 kW. The right-hand side panels provide zoomed-in views of each operating point, highlighting stable voltage ripple and rapid capacitor voltage adaptation during load transitions. Test conditions: $v_G = 230V_{rms}, 60Hz$, R_{load} switched to achieve the specified power levels at $V^*_{DC} = 400V$

only integrated energy-storage components are included in Table 4.3a. Two-stage or isolated decoupling architectures, active PPB schemes requiring extra components, and complex multi-inductor configurations are excluded. For MPC, Table 4.3b compares only FC implementations to highlight our contributions: a low sampling period (6.66 μs), low L and C values (250 μH/90 μF/480 μF), and deployment on a low-cost TI F28379D MCU. This achieves 16-state optimization every 6.66 μs, 1.85 % grid-current THD, and fast dynamic settling, whereas FPGA/RCP approaches use longer sampling times (12.5–100 μs) and larger passives.

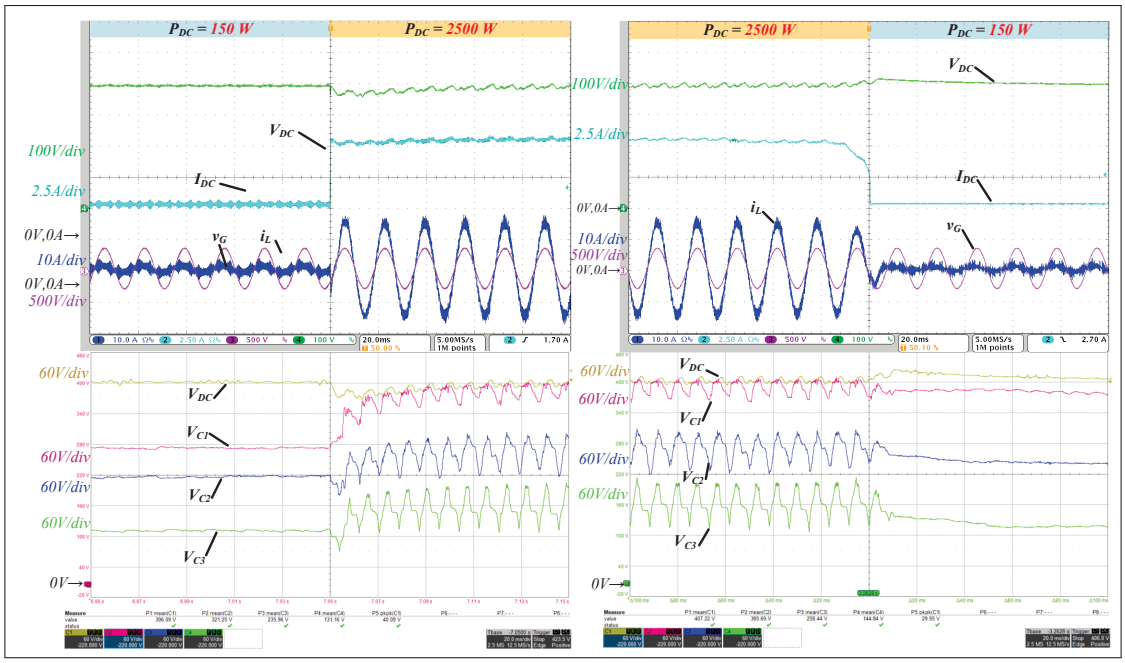


Figure 4.17 Experimental waveforms showing response to a large output power step under integrated PPB control: (left) Power step-up from P_{DC}= 150 W to 2.5 kW; (right) Power step-down from 2.5 kW back to 150 W. Test conditions: $v_G = 230V_{rms}, 60Hz$, R_{load} switched to achieve the specified power levels at $V^*_{DC} = 400V$

4.6 Conclusions

A MOMPCC-based integrated PPB control scheme for a TP-4CFC PFC converter has been developed and validated. By dynamically modulating flying-capacitor voltages without extra hardware, the method buffers twice-line-frequency power pulsations and downsizes DC-link capacitance. The bang-bang power-threshold logic ensures efficient charging/discharging, while MOMPCC provides coordinated current and voltage tracking with optimized weighting factors. Both simulation and experimental results confirm over 50 % reduction in DC-link ripple, acceptable THD, robust transient performance under load and voltage-reference changes, and improved converter efficiency and compactness. This makes the proposed approach highly suitable for high-density, reliability-critical power conversion applications.

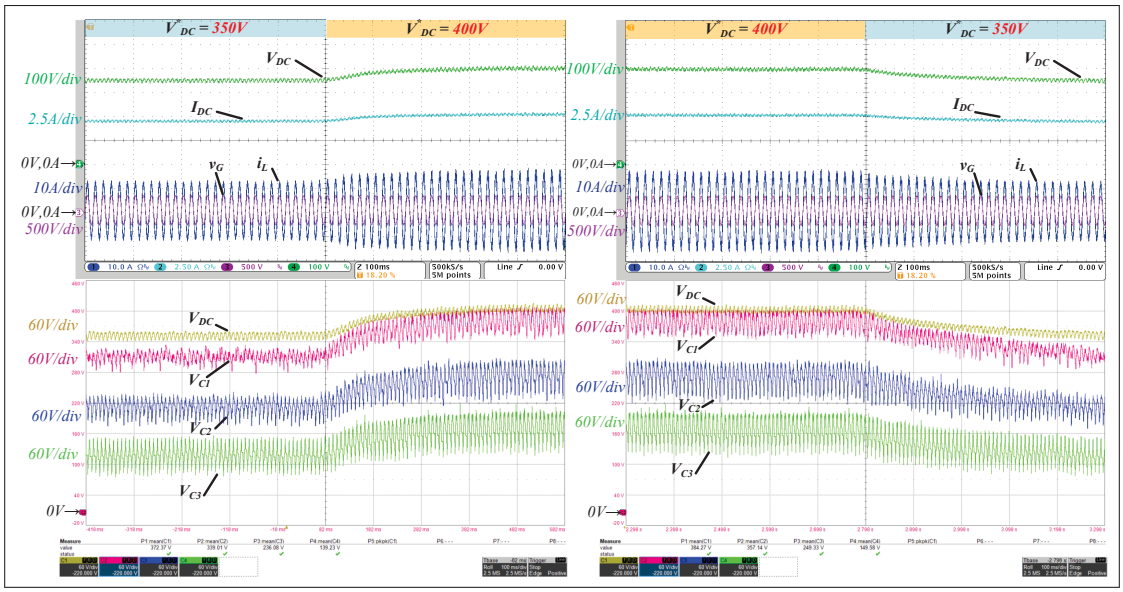


Figure 4.18 Experimental waveforms showing dynamic response under integrated PPB operation during DC-link voltage reference V^*_{DC} steps: (left) voltage increase from 350 V to 400 V, and (right) voltage decrease from 400 V to 350 V. Test conditions: $v_G = 220V_{rms}$, $60Hz$, $R_{load} = 72\Omega$

Table 4.3 Comparison

(a) Active PPB topologies without additional components

Reference	Topology	Power Level (W)	ΔV_{DC} Reduction	$L_G \vert L_{buff} \vert C_{buff} \vert C_{DC}$	Average F_{sw}	Dynamic Settling Time	Max HF Switch Rating
This Paper	5L-FC Integrated PPB PFC	2.5kW	50%	$250\mu H \vert 0 \vert 3\times 90\mu F \vert 480\mu F$	40kHz	2.2kW, 40mS	$0.5V_{DC}$
(Menzi *et al.*, 2022)	3L-FC Integrated PPB PFC	2.2kW	28%	$140\mu H \vert 0 \vert 50\mu F \vert 610\mu F$	35kHz	N.A.	$0.9V_{DC}$
(Wang *et al.*, 2022)	H-bridge with LC decoupling	1kW	89%	$165\mu H + 954\mu H \vert 400\mu H \vert 90\mu F \vert 120\mu F$	50kHz	500W, 100mS	V_{DC}
(Yao *et al.*, 2017)	H-bridge with DC-Split-Capacitor and inductor	1kW	Full Compensation	$2.2mH \vert 1.8mH \vert 2\times 90\mu F \vert 0$	10kHz	400W, 50mS	V_{DC}

Table 4.4 MPC implementation metrics for single-phase FC-PFC converters

Reference	Topology	Controller Platform	States Optimized Online	Sampling Period	$L_G \mid C_{FC} \mid C_{DC}$	THD
This Work	2.5kW 5L-FC Totem Pole	F28379D MCU	16	6.66 μs	250 μH |90 μF| 480 μF	1.85%
(Park & Kim, 2023)	810W Full Bridge 7L-FC PFC	F28377D MCU	20	66.6 μs	20 mH| 820 μF| 820 μF	2.45%
(Kim *et al.*, 2019)	1kW 5L-FC full bridge PFC	F28377D MCU	12	100 μs	20 mH| 800 μF| 800 μF	N.A.
(Tang *et al.*, 2025)	1kW 5L-FC full bridge inverter	FPGA Artix-7	16	100 μs	1 mH| 80 μF| NR	0.52%
(Babaie *et al.*, 2022)	350W Dual Output FC-PFC	dSPACE 1102	8	35 μs	5 mH| 1 mF| 1.2 mF	1.6%

CHAPTER 5

TWO-STAGE LEXICOGRAPHIC WEIGHT-FREE MODEL PREDICTIVE CONTROL FOR AN INTEGRATED POWER PULSATION BUFFER FOUR-CELL FLYING-CAPACITOR PFC CONVERTER

This chapter advances the iPPB control of the TP–4CFC rectifier by replacing the weighted-sum objective with a two-stage lexicographic model-predictive selector that requires no weight tuning and guarantees deterministic per-sample workload. Stage I forms a fixed-size top-K shortlist of admissible switching states using a current-tracking inductor-voltage equivalence; Stage II steers flying-capacitor energies using a common-offset reference that preserves balancing authority near grid-current zero crossings. Ties are resolved by a Hamming-distance rule to limit commutations. The predictors retain exact ZOH-discretized dynamics with two-step look-ahead for delay compensation. The implementation targets a dual-core microcontroller with a 6.66 μs sample period and reports worst-case execution time and memory footprint that scale only with K. Experiments on a 2.5 kW, 400 V prototype over a wide operating range demonstrate up to 54% DC-link ripple reduction, 3.7% grid-current THD, and half-cycle settling under rated load steps, while maintaining bounded runtime and eliminating manual weight tuning. A comparative analysis against the weighted-sum baseline shows preserved current quality with improved determinism and modest efficiency gains corroborated by loss-and-stress evaluation. The results indicate a practical, weight-free MPC path to higher power density in compact single-phase front-end rectifiers.

5.1 Introduction

This chapter builds directly on the integrated PPB (iPPB) framework and TP–4CFC plant established in Chapter 4. The focus is on removing weighting-factor dependencies and reducing the per-sample computational workload of the inner predictive controller while preserving the buffering capability of the four-cell flying-capacitor stack.

In multi-objective finite-set MPC for higher-level FC converters, multi-term costs require weight selection across operating points; ties and near-degeneracies can increase switching effort; and

full-state evaluation leads high computation. These issues are at odds with microcontroller-based realization, where deterministic timing, bounded memory, and predictable execution are required alongside accurate current tracking and FC-energy steering. Weighting-factor selection in multi-objective MPC is challenging: objectives have different physical units and are coupled, so tuning may trade one objective against another. Lexicographic MPC (Chen *et al.*, 2025) addresses this by prioritizing objectives in sequence: first enforcing the primary objective, then optimizing secondary objectives over the admitted set; tolerance-based variants retain multiple first-layer candidates to avoid degeneracy. In this work, a lexicographic scheme is adopted to prioritize current tracking while coordinating FC energy steering under discrete actuation.

Unlike earlier three-level FC or hybrid decoupling approaches (Menzi *et al.*, 2022; Qi *et al.*, 2019a; Ramos *et al.*, 2021; Qi *et al.*, 2019b; Watanabe *et al.*, 2018), this chapter extends iPPB to a four-cell FC PFC and addresses the resulting control problem with a lexicographic MPC scheme. This enables greater energy buffering using only embedded flying capacitors. Furthermore, the lexicographic multi-objective model-predictive current control (MOMPCC) eliminates the weight-tuning dependency typical of multi-term MPC, ensuring fast execution at higher sampling frequencies on low-cost MCUs—an advance not shown in prior MPC implementations. Building on the TP–4CFC iPPB MOMPCC in (Patel & Chandra, 2025), this work adds a weight-free lexicographic structure and deterministic FC-reference generation, together with full 2.5 kW hardware validation.

The key contributions of this research are:

1. *Lexicographic two-stage MOMPCC:* Introduces a modulator-free MPC for integrated PPB in a four-cell FC PFC that enforces current tracking while steering FC energy via lexicographic (priority-based) objective evaluation, avoiding weighting-factor tuning and maintaining deterministic per-sample workload on the MCU.
2. *Deterministic FC-reference generation and hardware validation:* Develops a common-offset FC-reference method that increases usable buffer swing without violating sharing constraints. A 2.5 kW prototype demonstrates $\sim 50\,\%$ DC-link ripple reduction, grid-current THD of

3.7 %, sub-half-cycle settling to rated load steps, bounded device stress, and reduced I_{RMS} through C_{DC}.

3. *Tie-break and switching effort:* A Hamming-distance tie-break with respect to the currently applied state reduces unnecessary commutations without introducing an additional weight in the objective.
4. *Real-time realization on MCU:* Executes 16-state lexicographic MPC every 6.66 μs on a dual-core MCU (no FPGA/RCP), enabling high effective switching frequency with practical passive sizes.

This chapter is organized as follows: Section II presents the TP–4CFC topology and control-oriented model; Section III details the weight-free lexicographic MOMPCC and deterministic FC-reference generation; Section IV reports simulation results; Section V describes the hardware prototype, real-time implementation, and experimental validation, including quantitative comparison with standard operation and prior PPB methods; Section VI concludes.

5.2 Integrated PPB Topology and Discrete Modelling

5.2.1 Topology Description

Fig. 5.1 illustrates the power stage of a bidirectional single-phase totem-pole four-cell flying-capacitor (TP-4CFC) converter. The low-frequency (LF) unfolder leg consists of a complementary pair $(S_{ap},\ S_{an})$ forming node A and commutating at the line frequency. The high-frequency (HF) FC multilevel (FCML) leg consists of four complementary pairs $(S_{1p},\ S_{1n}), \ldots, (S_{4p},\ S_{4n})$ forming node B. A boost inductor L_G with parasitic resistance R_G connects node A to the grid; the DC-link variables are $(V_{DC},\ I_{DC})$. Three flying capacitors C_1, C_2, C_3 sustain voltages v_{C1}, v_{C2}, v_{C3}, respectively.

Each complementary pair is represented by a binary switching function $S_x(t) \in \{0, 1\}$ with $x \in \{a, 1, 2, 3, 4\}$, where $S_x = 1$ denotes the upper device on (lower off). The LF selection S_a follows

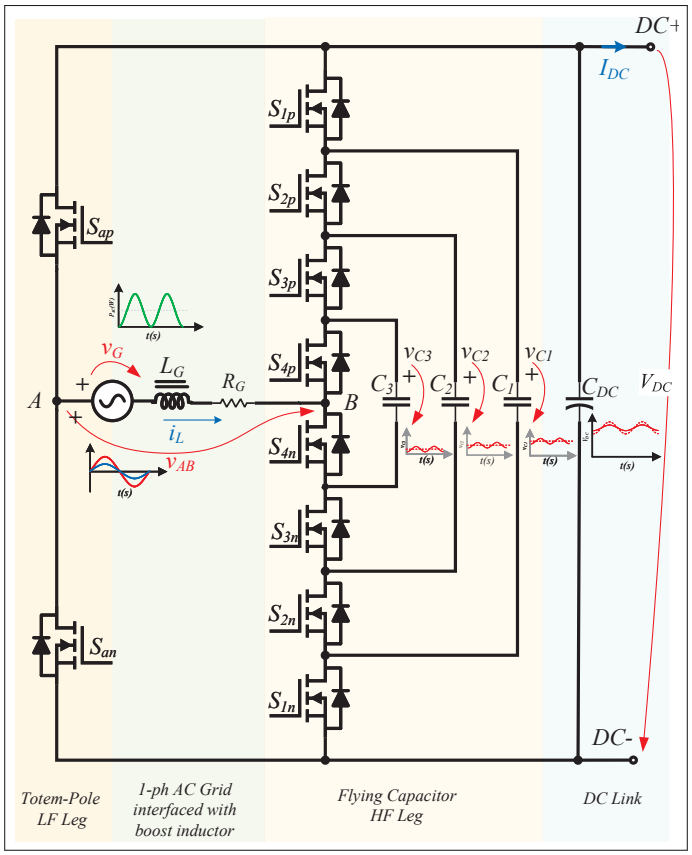


Figure 5.1 Configuration of the single-phase TP-4CFC PFC rectifier illustrating key waveforms in integrated PPB operation by solid lines and standard operation by dotted lines

the grid polarity. The HF selections are collected in the 4-bit vector $\boldsymbol{s} \triangleq [S_1, S_2, S_3, S_4]^\top \in \{0,1\}^4$. The set of admissible HF switching states $\mathcal{S}_{\text{adm}}$ is defined as:

$$\mathcal{S}_{\text{adm}} \triangleq \{0,1\}^4, \qquad |\mathcal{S}_{\text{adm}}| = 16.$$

yielding a total of 16 possible states. Pair-difference indicators $\Delta_k \in \{-1, 0, +1\}$, encoding the oriented conduction path through the FC stack, are defined as:

$$\begin{aligned} \Delta_0 &\triangleq S_a - S_1, \quad \Delta_1 \triangleq S_1 - S_2, \\ \Delta_2 &\triangleq S_2 - S_3, \quad \Delta_3 \triangleq S_3 - S_4. \end{aligned} \tag{5.1}$$

With $v_C \triangleq [v_{C1}, v_{C2}, v_{C3}]^\top$, the converter voltage v_{AB} is expressed as:

$$v_{AB} = \Delta_0 V_{DC} + \Delta_1 v_{C1} + \Delta_2 v_{C2} + \Delta_3 v_{C3}, \tag{5.2}$$

Per the sign convention in Fig. 5.1, the inductor voltage is

$$v_L = v_{AB} - v_G, \tag{5.3}$$

5.2.2 Operating Principle

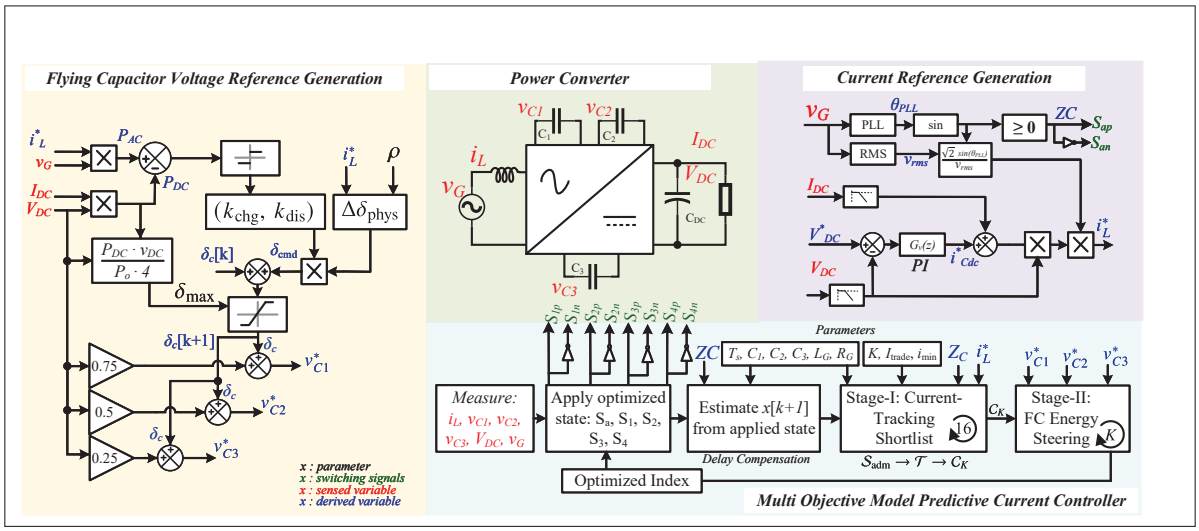


Figure 5.2 Detailed control diagram illustrating the MOMPCC methodology for integrated PPB operation

The LF leg unfolds the AC grid voltage, while the HF FCML leg selects discrete values of v_{AB} given by (5.2). The HF leg shapes the inductor voltage v_L to track a sinusoidal grid-current reference i_L^*, while the FC stack absorbs and releases the $2\omega_G$ power pulsation by tracking time-varying voltage references.

Conventional FCML operation maintains fixed voltage ratios $V_{DC} : V_{C1} : V_{C2} : V_{C3} = 4 : 3 : 2 : 1$ for reduced device voltage stress and level redundancy (Meynard & Foch, 1992; Lei *et al.*,

2017). In contrast, the proposed approach intentionally modulates the FC voltages toward asymmetric, time-varying references to absorb and release $2\omega_G$ energy. As the references evolve over the grid cycle, both the reachable v_{AB} set and the available redundancy become operating-point dependent (Fig. 5.3). This dependence is tracked online and used by a selector to preserve current quality while directing FC energy exchange.

5.2.3 Control-Oriented Model and State Estimation

All signals are sampled at $t_k \triangleq kT_s$, where T_s is the sampling period. The measured state vector at index k is

$$\boldsymbol{x}[k] \triangleq \big[\, i_L[k],\ v_G[k],\ V_{DC}[k],\ v_{C1}[k],\ v_{C2}[k],\ v_{C3}[k] \,\big]. \tag{5.4}$$

5.2.3.1 Grid-branch dynamics

The grid-side branch is modeled as R_G-L_G driven by v_{AB}:

$$L_G \dot{i_L}(t) + R_G i_L(t) = v_{AB} - v_G(t) \tag{5.5}$$

With zero-order hold (ZOH) over $[t_k, t_{k+1})$, exact discretization of (5.5) yields the one-step current predictor:

$$i_L[k{+}1] = \alpha_e\, i_L[k] + \beta_e \big(v_{AB}[k] - v_G[k]\big), \tag{5.6}$$

where $\alpha_e \triangleq e^{-R_G T_s / L_G}$, and $\beta_e \triangleq \frac{1-\alpha_e}{R_G}$. Equation (5.6) is used for both estimation and prediction.

5.2.3.2 Flying-capacitor dynamics

Charge balance in each FC cell yields the continuous-time relations:

$$C_k \, \dot{v}_{Ck}(t) = \Delta_k(t) \, i_L(t), \qquad k \in \{1, 2, 3\}. \tag{5.7}$$

where Δ_k is defined in (5.1). Under ZOH over $[t_k, \, t_{k+1})$, the discrete-time update is:

$$v_{Ck}[k{+}1] = v_{Ck}[k] + \frac{T_s}{C_k} \, \Delta_k[k] \, i_L[k], \quad k \in \{1, 2, 3\}, \tag{5.8}$$

5.2.3.3 Prediction Index and Timing Convention

A one-sample computation latency arises from the digital control implementation. The switching state $\boldsymbol{s}[k] \in \mathcal{S}_{\text{adm}}$ optimized during index $[t_k, \, t_{k+1})$ is applied over $[t_{k+1}, \, t_{k+2})$, while the previously selected switching state $\boldsymbol{s}[k{-}1]$ remains active over $[t_k, \, t_{k+1})$ (Cortes *et al.*, 2012). For a fixed LF polarity within a half-cycle, the two-step current predictor is:

$$\begin{aligned} \hat{i}_L[k{+}1] &= \alpha_e \, i_L[k] + \beta_e \big(v_{AB}\big(\boldsymbol{s}[k{-}1]\big) - v_G[k] \big) , \\ \hat{i}_L[k{+}2] &= \alpha_e \, \hat{i}_L[k{+}1] + \beta_e \big(v_{AB}\big(\boldsymbol{s}[k]\big) - v_G[k{+}1] \big) , \end{aligned} \tag{5.9}$$

where $v_{AB}(\cdot)$ is evaluated using (5.2) at the corresponding state and capacitor voltage estimates. The associated capacitor-voltage predictions follow from (5.8):

$$\hat{v}_{Ck}[k{+}2] = v_{Ck}[k{+}1] + \frac{T_s}{C_k} \, \Delta_k\big(\boldsymbol{s}[k]\big) \, \hat{i}_L[k{+}1], \quad k \in \{1, 2, 3\}. \tag{5.10}$$

Equations (5.9) - (5.10) provide the prediction pair $\big(\hat{i}_L[k{+}2], \, \hat{v}_c[k{+}2]\big)$ used by the online selection policy in Section 5.3.

5.3 Proposed Integrated PPB Control with Lexicographic MPC

This section specifies a three-part controller that (i) enforces grid-current tracking under discrete actuation, (ii) realizes twice-line-frequency $2\omega_G$ energy buffering in the FC stack via integrated PPB (iPPB), and (iii) regulates the DC-link voltage. Each component of the control is summarized in Fig. 5.2 and is discussed in this section. At sampling index k, measurements are acquired, the dual-stage selector evaluates $\mathcal{S}_{\text{adm}}$ with the delay-compensated predictors in (5.9)–(5.10), and the selected state is applied over $\left[t_{k+1},\, t_{k+2}\right]$.

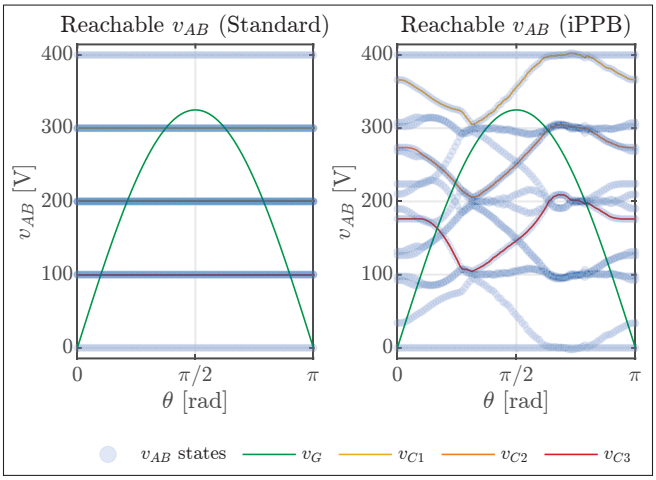


Figure 5.3 Reachable output-voltage levels v_{AB} over positive half-cycle: Standard operation (left) and iPPB operation (right). Points show the instantaneous v_{AB} obtained by enumerating all HF switching states $(S_1 \ldots S_4)$ using the actual FC voltages in one specific case. Standard uses fixed ratios $(0.75, 0.50, 0.25)V_{\text{DC}}$, whereas iPPB uses time-varying references

5.3.1 Problem Statement and Constraints

The controller optimizes over the finite set $\mathcal{S}_{\text{adm}}$: the primary target is one-step current tracking with low THD and unity power factor; simultaneously, the FC voltages follow asymmetric, time-varying $2\omega_G$ PPB references under bounded per-sample computation.

The difficulty arises because the ideal continuous v^*_{AB} from (5.3) is generally synthesized by time-averaging a finite set of discrete v_{AB} levels. However, under iPPB, the FC voltages are time

varying, so the available v_{AB} levels, and their spacing, become operating-point dependent. As a representative example, Fig. 5.3 illustrates the reachable v_{AB} levels: over a positive half-cycle, enumerating all 16 HF states reveals the attainable values of v_{AB}.

Conventional PWM modulators presume symmetric FC voltages and cyclic state modulation; under asymmetric operation their level selection no longer matches the available set, increasing distortion. Consequently, an online finite-set selector is employed: at each sample, candidates in $\mathcal{S}_{\text{adm}}$ are enumerated; those satisfying the current objective are retained; any residual redundancy is used to steer the FC voltages.

A single weighted sum cost function is possible (Karamanakos *et al.*, 2020; Patel & Chandra, 2025), but it requires weight tuning across operating points. Hence, a lexicographic split is adopted, ranking objectives by priority and reducing computation by confining lower-stage predictions to the admitted set.

5.3.2 Lexicographic Multi-Objective Structure

The optimization is separated into two priorities:

1. Stage-I (current tracking). Candidates whose one-step current error lies within a prescribed tolerance.
2. Stage-II (energy steering). On the admitted set, minimize FC-tracking error, with a deterministic tie-break to reduce commutations.

This structure eliminates weight tuning and yields fixed-time execution. The trade tolerance is chosen to retain redundancy for Stage II; when authority is insufficient (e.g., near zero crossings), the Stage I winner is applied directly to preserve current control.

5.3.2.1 Inductor-Voltage Equivalence

For a candidate switching state $s \in \mathcal{S}_{\text{adm}}$, define the inductor voltage contribution at evaluation time as

$$w(s) \triangleq v_{AB}(s) - v_G[k+1]. \tag{5.11}$$

Using the two-step predictor (5.9), the ideal inductor voltage $w_\star$ that can achieve the target $i_L^*[k+2]$ is

$$w_\star \triangleq \frac{i_L^*[k+2] - \alpha_e \hat{i}_L[k+1]}{\beta_e}. \tag{5.12}$$

With $\beta_e > 0$, the one-step current error satisfies

$$i_L^*[k+2] - \hat{i}_L[k+2] = \beta_e \left(w_\star - w(s)\right), \tag{5.13}$$

Hence, minimizing the current error is equivalent to minimizing the misfit $d_w(s)$ where:

$$d_w(s) \triangleq \left| w(s) - w_\star \right|. \tag{5.14}$$

This equivalence underpins the Stage-I admissible-set construction.

5.3.2.2 Stage-I: Current-Tracking Shortlist

Stage-I forms a shortlist $C_K \subset \mathcal{S}_{\text{adm}}$ that satisfies the one-step current objective while preserving redundancy for PPB. The nearest discrete level is

$$s_{\min} = \arg\min_{u \in \mathcal{S}_{\text{adm}}} d_w(u), \qquad w_{\min} = w(s_{\min}). \tag{5.15}$$

When $\left|\hat{i}_L[k+1]\right| \le i_{\min}$ (design parameter), PPB authority is negligible on the next step and the shortlist reduces to $C_K = \{s_{\min}\}$. Otherwise, a small current relaxation $I_{\text{trade}} > 0$ (within THD limits) is mapped to the voltage domain,

$$W_{\text{trade}} = \frac{I_{\text{trade}}}{\beta_e}, \tag{5.16}$$

and candidates within a symmetric band around $w_{\min}$ are admitted,

$$\mathcal{T} = \left\{ s \in \mathcal{S}_{\text{adm}} : \; | w(s) - w_{\min} | \leq W_{\text{trade}} \right\}, \tag{5.17}$$

with the convention $\mathcal{T} \leftarrow \{s_{\min}\}$ if $\mathcal{T} = \varnothing$. To bound runtime, the shortlist contains the K smallest $d_w(s)$ in $\mathcal{T}$ (or all if $|\mathcal{T}| \leq K$):

$$C_K = \text{TopK}\big(\mathcal{T},\, d_w,\, K\big). \tag{5.18}$$

The band W_{trade} limits current deviation to I_{trade} while preserving local redundancy for Stage II; the Top-K step fixes the per-sample workload.

5.3.2.3 Stage-II: Energy Steering and Tie-Breaking

Let $\{v^*_{C_m}[k{+}2]\}_{m=1}^{3}$ denote the FC iPPB references. For each $s \in C_K$, the capacitor-voltage predictions $\hat{v}^{(s)}_{C_m}[k{+}2]$ follow from (5.10) with $\hat{i}_L[k{+}1]$ as the branch current. The Stage-II objective is

$$J_2(s) = \sum_{m=1}^{3} \left(v^*_{C_m}[k{+}2] - \hat{v}^{(s)}_{C_m}[k{+}2] \right)^2, \qquad s \in C_K. \tag{5.19}$$

With identical FC capacitances, weighting is unnecessary since each term has equal priority. The nominal choice is

$$s^\star = \arg\min_{s \in C_K} J_2(s). \tag{5.20}$$

To limit commutations among near-equivalent candidates, an η-tolerance class is employed,

$$\mathcal{E} = \left\{ s \in C_K : \; J_2(s) \leq \min_{u \in C_K} J_2(u) + \eta \right\}, \tag{5.21}$$

and, within $\mathcal{E}$, the element with the smallest Hamming distance to the previously applied state $s[k{-}1]$ is applied.

5.3.2.4 Deterministic Runtime and Complexity

Per-sample workload is linear in $|\mathcal{S}_{\text{adm}}|$. Stage I evaluates $v_{AB}(s)$, $w(s)$, and $d_w(s)$ in one pass and retains at most K candidates; Stage II computes J_2 only on C_K and applies a constant-time tie-break. The resulting complexity is

$$O\big(|\mathcal{S}_{\text{adm}}|\big) + O(K), \qquad K \ll |\mathcal{S}_{\text{adm}}|.$$

This supports fixed-time embedded execution, with Stage I arithmetic parallelizable across auxiliary cores and Stage II confined to a small set.

5.3.3 FC Voltage-Reference Generation

The reference generator produces $\{v^*_{C_i}\}_{i=1}^{3}$ for Stage II by mapping the instantaneous power mismatch into a single common offset δ_c that shifts all FC references together while preserving inter-level spacing and the intended v_{AB} redundancy. Full cancellation of the pulsating power is not targeted because actuation authority vanishes near current zero-crossings. All plant signals are evaluated at $k+1$; references are consumed at $k+2$.

5.3.3.1 Reference Structure

For the sensed DC-link voltage V_{DC}, the nominal centers are

$$c_1 = 0.75\,V_{DC}, \qquad c_2 = 0.50\,V_{DC}, \qquad c_3 = 0.25\,V_{DC}. \tag{5.22}$$

A common-mode offset δ_c shifts all three references,

$$v^*_{C_1} = c_1 + \delta_c, \qquad v^*_{C_2} = c_2 + \delta_c, \qquad v^*_{C_3} = c_3 + \delta_c, \tag{5.23}$$

so the spacings remain $v^*_{C_1} - v^*_{C_2} = c_1 - c_2$ and $v^*_{C_2} - v^*_{C_3} = c_2 - c_3$.

5.3.3.2 Power Mismatch and Physical Authority

A noise-robust mismatch estimate uses the current reference:

$$P_{\text{diff}} = v_G\, i_L^* - V_{DC}\, I_{DC}.$$

Given a switching state, at most two FCs are actively driven at an instant; only a fraction $\rho \in (0, 1]$ of i_L contributes to charge transfer in the next step. For equal FC values C_{ref}, the realizable per-sample offset change satisfies

$$\Delta\delta_{\text{phys}} = \rho\, \frac{\left| i_L^*[k{+}1] \right| T_s}{C_{\text{ref}}}. \tag{5.24}$$

Hence $\Delta\delta_{\text{phys}} \to 0$ as $|i_L^*| \to 0$ (self-gating near zero crossings), and authority scales with operating power, limiting the achievable swing.

5.3.3.3 Asymmetric Update and Saturation

The sign of P_{diff} sets the energy direction; asymmetric gains $(k_{\text{chg}}, k_{\text{dis}})$ bias the trajectory:

$$\Delta\delta_{\text{cmd}} = \begin{cases} k_{\text{chg}}\, \Delta\delta_{\text{phys}}, & P_{\text{diff}} \geq 0 \text{ (charge)}, \\ -\, k_{\text{dis}}\, \Delta\delta_{\text{phys}}, & P_{\text{diff}} < 0 \text{ (discharge)}. \end{cases} \tag{5.25}$$

The offset evolves with symmetric clamps,

$$\delta_c[k{+}1] = \text{sat}\Big(\delta_c[k] + \Delta\delta_{\text{cmd}}, -\delta_{\max}, +\delta_{\max}\Big), \tag{5.26}$$

after which (5.23) yields $\{v_{C_i}^*[k{+}2]\}_{i=1}^{3}$. Thus δ_c remains a slow, physically realizable common-mode motion that does not perturb the Stage I current-tracking band.

5.3.3.4 Parameter Selection and Reachability

The amplitude limit $\delta_{\max}$ sets the allowable swing and PPB headroom, constrained by the targeted DC-link ripple reduction and device voltage stress. The connectivity factor ρ models charge-path availability; a conservative fixed value (e.g., 0.3–0.4) provides consistent scaling for $(k_{\text{chg}}, k_{\text{dis}})$. The asymmetry $(k_{\text{chg}}, k_{\text{dis}})$ shapes charge/discharge cadence; typical ranges are $k_{\text{chg}} \in [0.8, 1.0]$ and $k_{\text{dis}} \in [1.0, 1.3]$. At rated conditions, k_{chg} is selected so that $v^*_{C_m}$ approaches its upper bound by the end of the charge window, while k_{dis} expedites discharge after transition. These choices preserve the reachable v_{AB} set and maintain redundancy for Stage II.

5.4 Simulation Analysis

Table 5.1 Simulation parameters

Parameter	**Value**
Grid voltage v_G	230 V_{rms}, 60 Hz
Boost inductor L_G	250 μH
DC-link capacitance C_{DC}	480 μF
Flying capacitances (C_1, C_2, C_3)	70 μF each
DC-link voltage V_{DC}	400 V
Nominal load power P_o	2.2 kW
Sampling time T_s	5 μs
Trade band, current floor $(K, I_{\text{trade}}, i_{\min})$	6, 1.5 A, 0.8 A
FC-ref. params $(\delta_{\max}, \rho, k_{\text{chg}}, k_{\text{dis}})$	100 V, 0.4, 1.0, 1.5

Table 5.2 Buffered energy shares over half line cycle at P_o=2.2 kW

Mode	ShareC_{DC} [%]	Share$_{\text{FC}}$ [%]	FC split [%] (C1/C2/C3)
Standard	100	0	–
iPPB	28	72	(32.4 / 24.4 / 15.2)

The aim of this section is to quantify ripple reduction, energy routing, and device stresses under the proposed iPPB control, using the operating point specification in Table 5.1. All cases share identical plant and outer loop settings; only the FC-reference parameters $(\beta_{\max}, k_{\text{chg}}, k_{\text{dis}})$ are

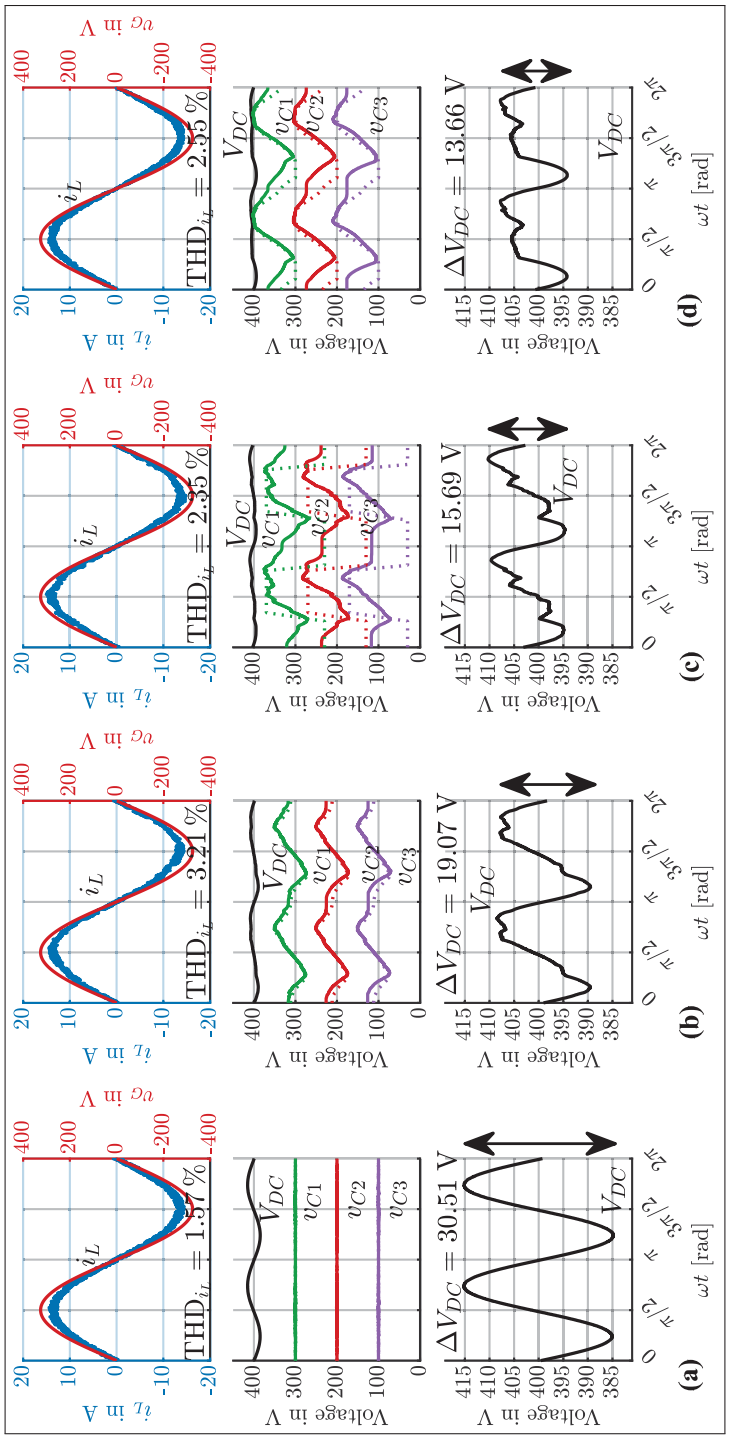


Figure 5.4 TP–4CFC simulated waveforms at the operating point of Table 5.1. Only the FC-reference parameters ($\beta_{\max}$, k_{chg}, k_{dis}) vary across cases

Table 5.3 Per-switch $\overline{f_{\text{sw}}}$ and $V_{\text{off,max}}$: standard vs. iPPB

Switch	$\overline{f_{\text{sw}}}$ [kHz]			$V_{\text{off,max}}$ [V]	
	Standard	iPPB	Δ [%]	Standard	iPPB
S1	39.06	33.90	-13.22	115	110
S2	53.46	57.18	+6.96	100	110
S3	51.42	46.50	-9.57	100	110
S4	47.82	18.06	-62.23	100	200

varied. The DC-link ripple ΔV_{DC} is measured peak-to-peak over a steady-state line cycle. The half-cycle buffering demand is approximated as $E_{buf} \approx P_{dc}/\omega_G$, and the equivalent DC-link sizing relation used for comparison is $C_{DC} \approx P_{dc}/(\omega_G V_{DC} \Delta V_{DC})$.

5.4.1 Waveforms and Ripple Reduction

Fig. 5.4 shows, for each case, the grid current and voltage (i_L, v_G), the DC-link and FC voltages (V_{DC}, v_{C1}–v_{C3}), and V_{DC} ripple over the line cycle.

In the baseline (standard) operation of Fig. 5.4(a), the fixed FC targets $v^*_{C1}/v^*_{C2}/v^*_{C3} = 300/200/100$ V yield $\Delta V_{DC} = 30.51$ V with $\text{THD}(i_L) \approx 1.57\%$. With all $2\omega_G$ energy buffered by the DC link, this case serves as the reference.

Enabling iPPB with a maximum swing around nominal centers in Fig. 5.4(b), using $(k_{\text{chg}}, k_{\text{dis}}) = (0.35, 0.8)$, lowers the ripple to $\Delta V_{DC} = 19.07$ V, a 37.50% reduction relative to the baseline. The FC stack carries a portion of E_{buf}, while authority diminishes near current zero crossings and the discharge correspondingly slows.

Increasing the slew in Fig. 5.4(c) (aggressive $k_{\text{chg}}, k_{\text{dis}} > 1$) yields a bang-bang-like behavior and further reduces the ripple to $\Delta V_{DC} = 15.69$ V, i.e., 48.57% below baseline. In this setting, $\beta_{\max} = 80$ V is used to expose additional v_{AB} levels, which increases the effective FC buffering share and tends to improve current quality, consistent with the higher average FC voltage and wider swing reported in (Menzi *et al.*, 2022).

Finally, setting $\beta_{\max}$ near the allowable limit in Fig. 5.4(d) (here $\beta_{\max} \approx V_{DC}/4$) while maintaining near-equidistant FC spacing achieves the best iPPB performance at rated load: $\Delta V_{DC} = 13.66$ V, a 55.23% reduction compared to standard operation. In this case, the FC stack carries most of the twice-line energy.

5.4.2 Energy Routing

Table 5.2 summarizes the buffering shares over a half line cycle. Under standard operation the DC link bears the full burden. With iPPB enabled, up to 72% of E_{buf} is routed through the FC stack while the DC-link share reduced accordingly.

Achieving $\Delta V_{DC} \approx 13.66$ V without iPPB would require $C_{DC}^{\text{eq}} \approx P_{DC}/(\omega_G V_{DC} \Delta V_{DC}) \approx 1.07$ mF. With iPPB, the available C_{DC}+C_1+C_2+$C_3 \approx 690$ μF suffices, corresponding to about 35% less total capacitance for the same ripple.

5.4.3 Device Stresses and Switching Activity

In MOMPCC, a discrete state is selected each sample; accordingly, the per-device half-cycle average switching frequency (Karamanakos & Geyer, 2020) is defined as $\overline{f}_{\text{sw},j} = N_j/(2T_{1/2})$, where N_j counts gate transitions on device j over a half cycle of duration $T_{1/2}$.

With sampling interval $T_s = 5$ μs, the minimum on/off time is $2T_s = 10$ μs, bounding the average by $\overline{f}_{\text{sw}} \leq 1/(2T_s) = 100$ kHz. Table 5.3 reports $\overline{f_{\text{sw},j}}$ and the worst-case blocking voltage $V_{\text{off,max}}$ for each device.

Under iPPB, the HF-leg mean $\overline{f}_{\text{sw}}$ decreases by about 19% (from 47.94 to 38.91 kHz), while the distribution across S_1–S_4 becomes more uneven (18–57 kHz). As the FC swing increases, $V_{\text{off,max}}$ rises on the lowest-rated position (here S_4 approaches 200 V), whereas upper devices retain their standard ratings when near-equidistant FC spacing is preserved. The totem-pole current path keeps per-pair I_{rms} similar across modes, so conduction losses remain comparable; the efficiency benefit primarily originates from reduced switching energy and lower DC-link

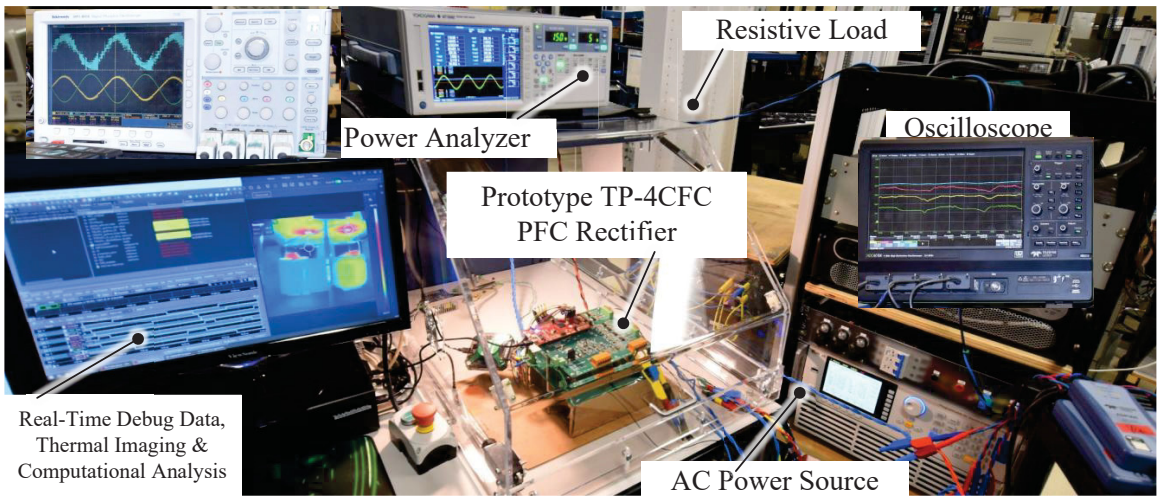


Figure 5.5 Experimental setup of the 2.5 kW TP-4CFC PFC rectifier with integrated PPB

ESR due to the ripple-RMS decrease. In the iPPB case of Fig. 5.4(d), the measured DC-link RMS current falls from 5.78 to 4.91 A ($\approx$ 15%), consistent with the ripple reduction.

5.5 Hardware Implementation and Experimental Verification

5.5.1 Hardware Prototype and Experimental Setup

Table 5.4 Component Listing for TP-4CFC integrated PPB prototype

Component	Part No.	Parameters
SiC MOSFET	10×C3M0060065D	650 V, 60 mΩ
Isolated Gate Drivers	10×UCC23514	5 kVrms, 4 A/5 A
Voltage Sensor	5×AMC3330QDWERQ1	Isolation Amplifier
Current Sensor	2×CT426-HSN820MR	±20 A
Boost Inductor	1×760801101	250 μH , 36 mΩ
Flying Capacitors	3×C4AQLBW5700A3LK	70 μF, 500 V, 2.1 mΩ
DC-Link Capacitor	1×B43548A5567M060	480 μF , 450 V
Microcontroller	1×TMS320F28379D	200 MHz, 2×C28

The power stage integrates SiC MOSFETs, three film flying capacitors (FCs), a boost inductor, and isolated gate-driver circuits. A separate control/measurement board hosts the TMS320F28379D MCU, high-voltage/current sensors, and analog signal-conditioning and protection. The laboratory setup in Fig. 5.5 uses a Chroma 61508 programmable AC source and a resistive load bank; power quality is measured with a power analyzer, and computational timing is verified with a logic analyzer. Key hardware items and ratings are summarized in Table 5.4.

5.5.2 Embedded Real-time Implementation and Control Partitioning

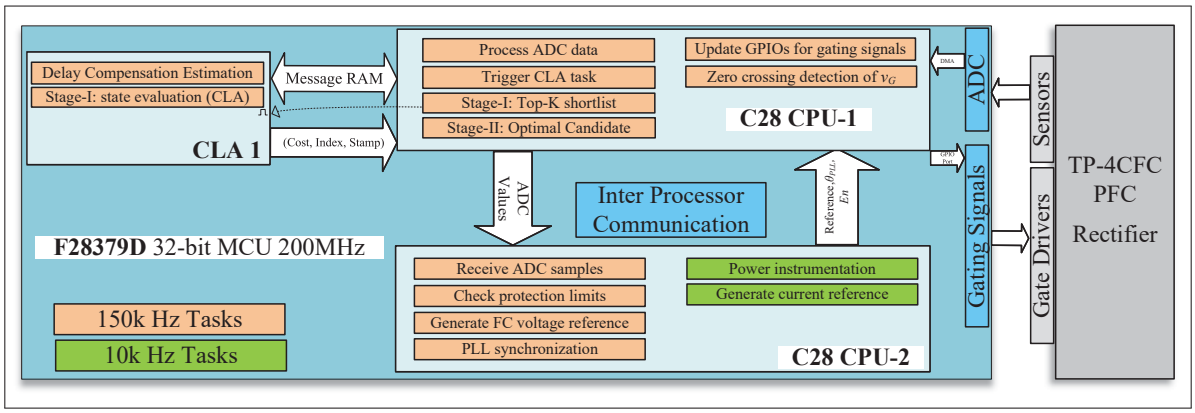


Figure 5.6 Real-time partitioning of the lexicographic MOMPCC

Real-time implementation of the lexicographic MOMPCC at $T_s = 6.66\ \mu$s (150 kHz) on a TMS320F28379D microcontroller requires sensing, online optimization, and switching updates to complete within each interval. The dual-CPU architecture and co-processor Control Law Accelerator (CLA) are utilized to guarantee deterministic timing without exceeding the cycle budget; Fig. 5.6 summarizes the implementation.

A 150 kHz ePWM synchronously triggers ADC conversions; hardware offset removal and DMA provide zero–wait-state RAM access to minimize latency. CPU1 executes time-critical tasks: ADC processing, delay compensation, shortlist maintenance, Stage II evaluation, and gate updates. The CLA performs Stage I arithmetic over all 16 high-frequency states in an unrolled loop and streams (index, d_w) into a shared mailbox with a generation stamp and per-state ready flags. In parallel, CPU1 performs nonblocking polling of the ready mask each cycle and

maintains a fixed-size top-K container (typically K=6) of lowest-misfit candidates under the Stage I tolerance. This streaming design preserves parallelism, avoids full sorting, and bounds the CPU1 workload.

Once the shortlist is available, CPU1 evaluates $J_2(s)$ over C_K, applies a Hamming-distance tie-break to reduce commutations, and selects the resulting index. Discrete switching states are applied (rather than duty cycles); gate outputs and dead time are enforced via atomic port writes.

CPU2 handles PLL synchronization, zero-crossing detection, FC-reference updates, and protection at 150 kHz; the outer voltage loop and power measurements run at 10 kHz. To avoid current surges near grid zero crossings, PWM outputs are temporarily masked. Communication of ADC/MPC states (CPU1→CPU2) and references/flags (CPU2→CPU1) use the IPC peripheral with a lightweight 150 kHz handshake. CLA–CPU1 exchange is lock free: the CLA writes $(\text{cost}, \text{index}, \text{stamp})$, raises the ready bit, and CPU1 accepts entries only when the stamp matches the current generation.

The approach achieves fixed-time execution on a single MCU, removing FPGA requirements and supporting practical adoption in industrial applications.

5.5.3 Experimental Results

5.5.3.1 230 V_{rms} AC to 400 V DC Operation

Fig. 5.7(a) compares operation without iPPB (a.i) and with iPPB (a.ii) at nominal grid conditions ($v_G \approx 230$ V_{rms}, 60 Hz). Enabling iPPB reduces the DC-link ripple from 31.41 V to 14.44 V ($\approx$ 54%). Grid-current THD rises to 3.72% due to FC asymmetry, while efficiency improves by $\approx$ 0.2%. DC-link RMS current decreases, lowering capacitor thermal stress.

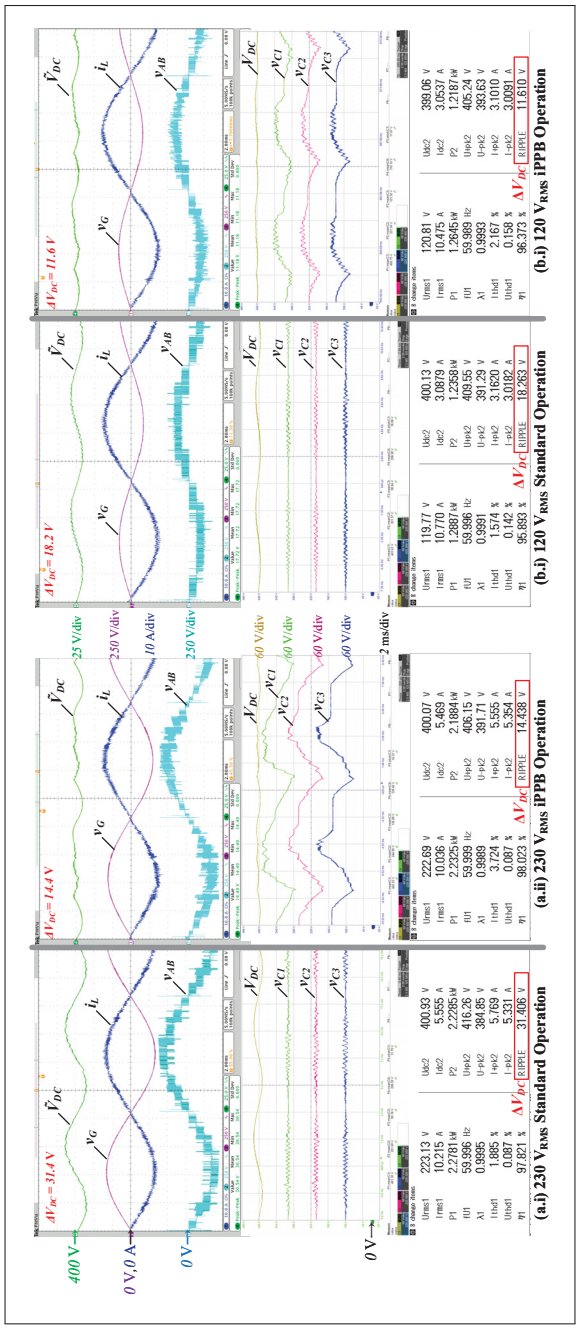


Figure 5.7 Experimental waveforms comparing standard and iPPB-enabled operation under MOMPCC. Top rows: AC-coupled DC-link $\tilde{V}_{DC}$, v_G, i_L, v_{AB}. Middle rows: v_{C1}–v_{C3} and V_{DC}. Bottom panels: power-analyzer readouts with DC-link ripple and efficiency. (a) $v_G = 230\ \mathrm{V_{rms}}$, 60 Hz; $V^*_{DC} = 400$ V; $P_{DC} = 2.2$ kW: (a.i) standard; (a.ii) iPPB enabled—ΔV_{DC} reduced from 31.41 V to 14.44 V ($\approx 54.0\%$ reduction). (b) $v_G = 120\ \mathrm{V_{rms}}$, 60 Hz; $P_{DC} = 1.2$ kW: (b.i) standard; (b.ii) iPPB enabled—ΔV_{DC} reduced from 18.26 V to 11.61 V ($\approx 36.4\%$ reduction)

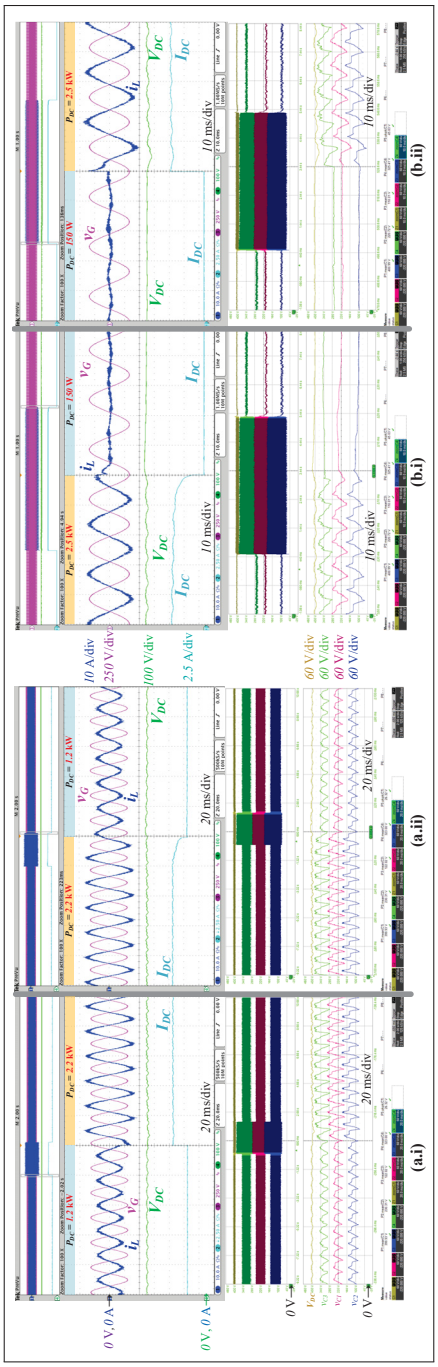


Figure 5.8 Dynamic load response under MOMPCC with iPPB (v_G = 230 V_{rms}, 60 Hz, V^*_{DC} = 400 V). Left (a.i–a.ii): moderate step P_{DC} : 1.2 → 2.2 → 1.2 kW. Right (b.i–b.ii): large step P_{DC} : 150 W ↔ 2.5 kW. Top rows: v_G, i_L, V_{DC}, I_{DC}. Bottom rows: v_{C1}–v_{C3}. Insets show zoomed views; V_{DC} deviations remain bounded and settle within 10 ms

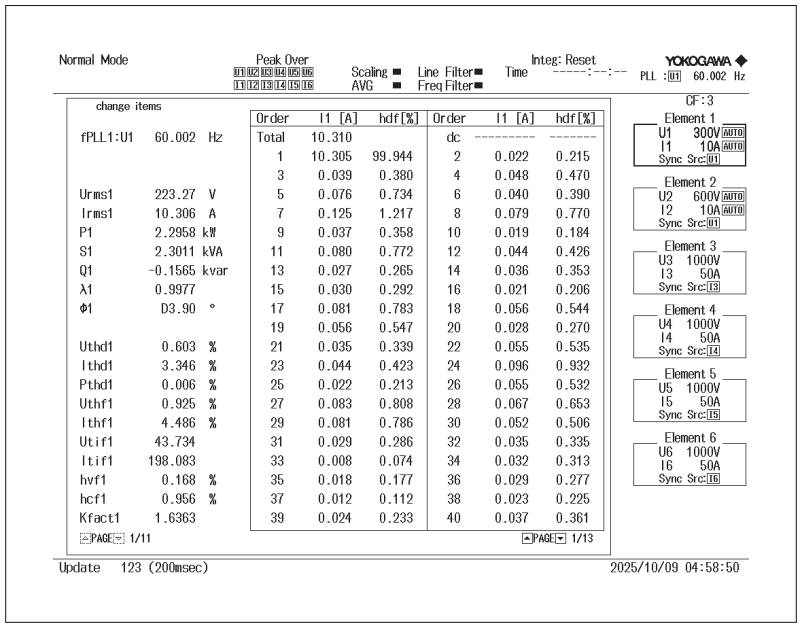


Figure 5.9 Power-analyzer readouts of the grid current harmonics under nominal test conditions: $v_G \approx 230\ \mathrm{V_{rms}}$, $f_G = 60$ Hz; regulated DC-link reference $V_{DC}^{*} = 400$ V; delivered DC power $P_{DC} = 2.2$ kW

5.5.3.2 120 $\mathrm{V_{rms}}$ AC to 400 V DC Operation

Fig. 5.7(b) shows operation at $v_G = 120\ \mathrm{V_{rms}}$ and $P_{DC} = 1.22$ kW (current limited to the rated value), confirming the PPB scheme's robustness across a wide range of grid conditions. With iPPB enabled (b.ii), ΔV_{DC} drops from 18.26 V to 11.61 V ($\approx 36\%$). Measured THD is 2.167%, aided by increased switching-state redundancy and improved FC control authority at this operating point.

5.5.3.3 Load Change Dynamics

Fig. 5.8 presents step responses under iPPB. The controller adjusts the permissible FC swing online to route the required energy while preventing overcompensation. As shown in Fig. 5.8(b), a massive 2.3 kW load step settles in < 10 ms with ~5% V_{DC} deviation from reference value,

owing to high bandwidth of the MOMPCC algorithm and the load feedforward current reference generation

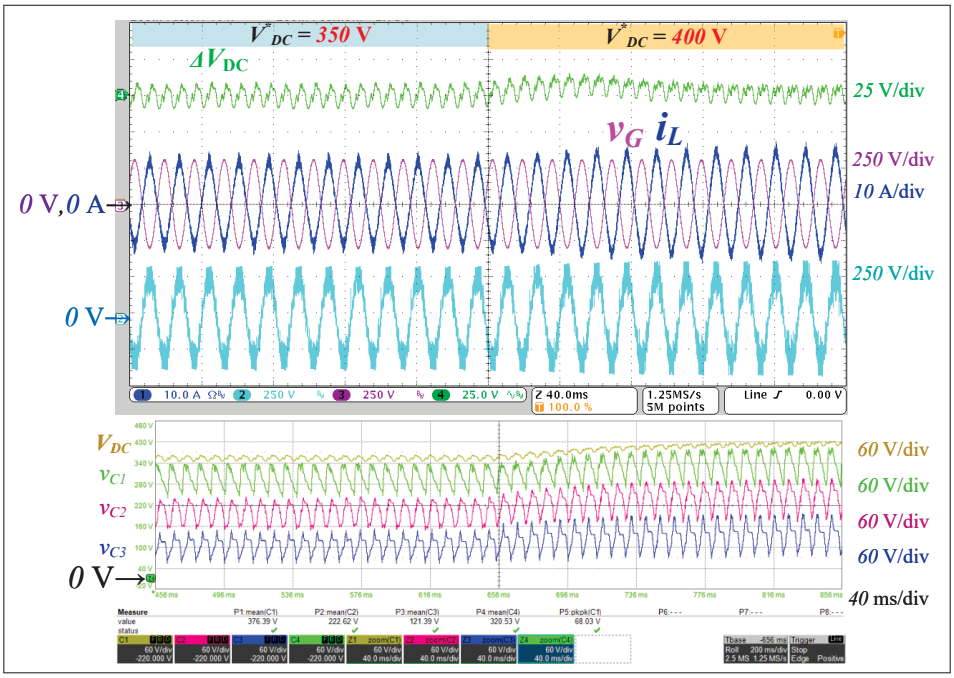


Figure 5.10 Experimental waveforms: dynamic response to a DC-link reference step under integrated PPB. V^*_{DC} stepped from 350 to 400 V. Test conditions: v_G = 230 V_{rms}, 60 Hz; R_{load} = 72 Ω

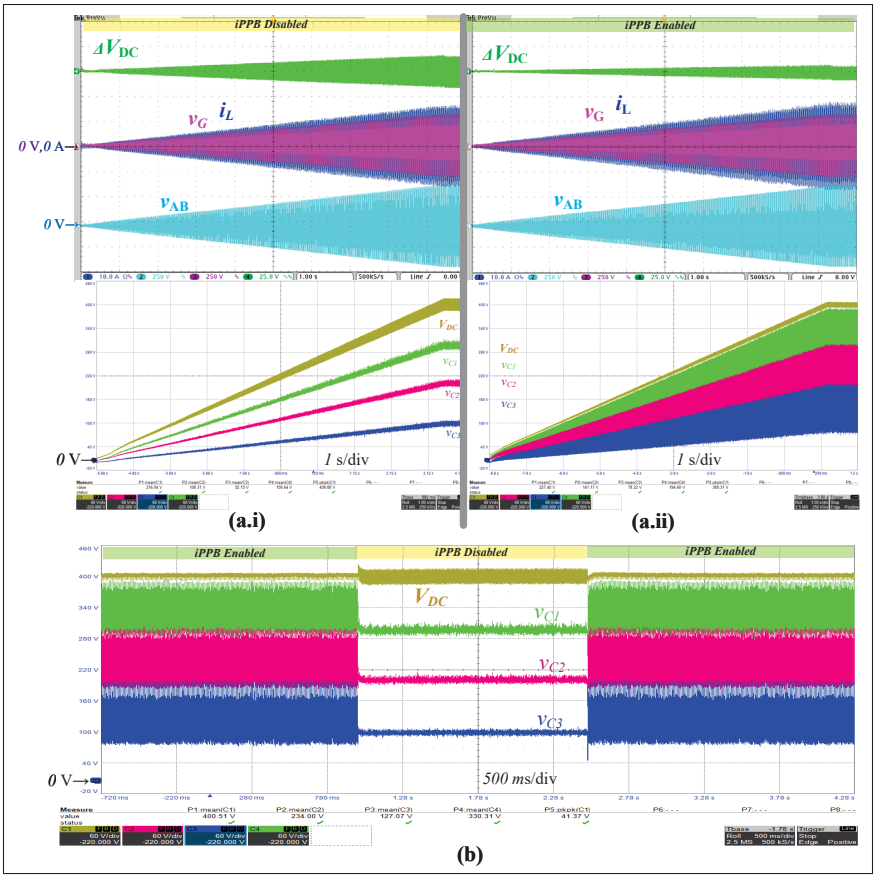


Figure 5.11 v_G ramp and iPPB toggle behavior. (a) DC-link charging and FC swing (1 s/div): top—$\tilde{V}_{DC}$, v_G, i_L, v_{AB}; bottom—V_{DC} and v_{C1}–v_{C3}, showing (a.i) iPPB disabled and (a.ii) iPPB enabled (reduced ripple). (b) iPPB enable/disable sequence (500 ms/div): transient and steady-state responses of V_{DC} and v_{C1}–v_{C3}. Test conditions for (a): $V_{DC}^{*} \approx 1.2\, V_{g,\mathrm{pk}}$ and fixed load $R_{\mathrm{load}} = 72\ \Omega$

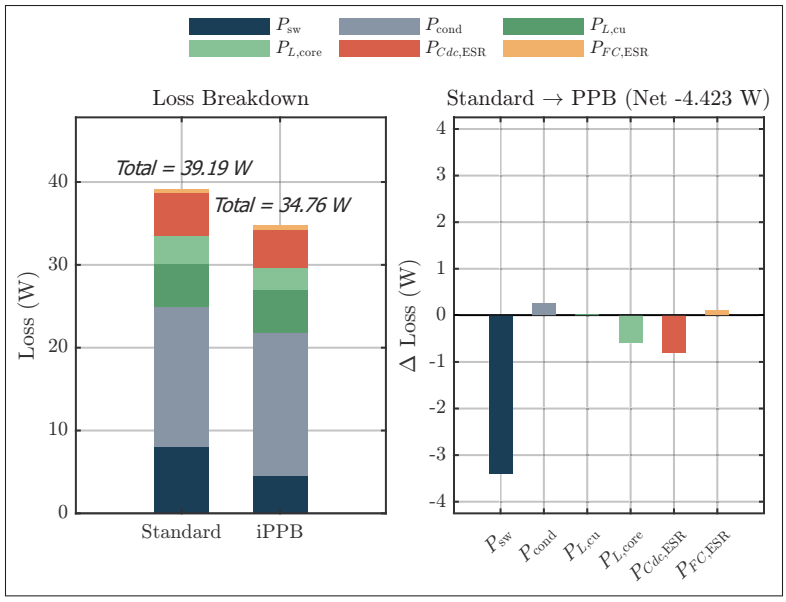


Figure 5.12 Loss breakdown and attribution at 230 V_{rms}, 400 V_{dc}, 2.2 kW. Left: stacked losses for Standard vs. iPPB operation. Right: component-loss differences (iPPB – Standard) show that the efficiency gain is chiefly due to reduced switching loss and DC-link ESR loss

5.5.3.4 Reference Change Dynamics

Fig. 5.11(a) (AC voltage sweep and iPPB toggling; v_G ramp; $V^*_{DC} \approx 1.2V_{g,\text{pk}}$; $R_{\text{load}} = 72\ \Omega$) shows that iPPB can be enabled/disabled at arbitrary operating points without loss of stability; the system re-enters a bounded steady state after each toggle. Fig. 5.10(b) demonstrates V_{DC} setpoint changes completed in ≈ 200 ms (with slew-limited V^*_{DC}).

These experimental results validate the effectiveness of the proposed iPPB with MOMPCC strategy, emphasizing stable operation, measurable ripple reduction, rapid transient response, and suitability for implementation on a MCU platform.

5.5.4 Performance Analysis

Efficiency, THD, ΔV_{DC} were measured on the hardware with a Yokogawa WT1806E power analyzer under steady-state conditions and averaged over ten line cycles. Fig. 5.13 summarizes

steady-state performance versus output power P_{DC}. Fig. 5.13(a) shows that enabling iPPB reduces the DC-link peak-to-peak ripple ΔV_{DC} for wide load range, with the largest absolute reduction at the power $2.2\,kW$. The reduced buffering effectiveness at low power is attributable to the low I_L, although absolute ripple is already small at low loads and remains within design limits. Fig. 5.13(b) reports measured efficiency: iPPB provides a small efficiency gain at high power. Fig. 5.13(c) shows grid-current THD versus P_{DC}; Grid-current THD increases slightly at rated points but remains within limits. Overall, the plots demonstrate consistent ripple reduction across the tested range with efficiency benefits and minor impact on power quality.

5.5.4.1 Loss Breakdown

To gain physical insight into the measured efficiency trends, Fig. 5.12 presents the evaluated loss breakdown at 2.2 kW, 230 V_{rms}, and 400 V_{dc} operation. Stacked bars compare Standard and iPPB operation, partitioned into (P_{sw}, P_{cond}, $P_{L,\text{cu}}$, $P_{L,\text{core}}$, $P_{Cdc,\text{ESR}}$, $P_{FC,\text{ESR}}$)[1].

The loss reduction with iPPB is driven by (i) lower switching energy—fewer effective transitions during the $2\omega_G$ windows—and (ii) reduced DC-link ESR dissipation from lower ripple RMS current. The low-ESR film FCs make the $\sim 9\%$ increase in FC RMS current nearly loss-neutral, and conduction loss remains similar because per-pair device I_{rms} remains unchanged; thus the efficiency gain is primarily due to reductions in P_{sw} and $P_{Cdc,\text{ESR}}$.

[1] Device losses were obtained in PLECS using the C3M0060065D manufacturer loss/thermal models with $R_g = 10\ \Omega$, $R_{\theta,\text{TIM}} = 0.2$ K/W, heatsink $R_\theta/C_\theta = 0.75$ K/W/200 J/K, and $T_{\text{amb}} = 25°\text{C}$. Switching losses use event-based summation $\sum(E_{\text{on}}+E_{\text{off}})$, and conduction losses use $I^2_{\text{rms}}R_{\text{ds,on}}(T_j)$. Inductor copper losses use $I^2_{\text{rms}}R_{\text{ac}}(T)$ with $R_{\text{ac}}(f)$ obtained from a Dowell lookup. Core losses are computed via the generalized Steinmetz equation (GSE) on the flux trajectory reconstructed from the measured inductor voltage $v_L(t)$, using a High-Flux 60μ toroid ($A_e = 153.7\ \text{mm}^2$, $V_{\text{core}} = 14.6\ \text{cm}^3$, $\ell_e \approx 95$ mm, $N = 50$). The GSE exponents are ($k = 246.54,\ \alpha = 1.311,\ \beta = 2.218$), derived from the vendor fit $P_v = kB^b f^c$. Capacitor ESR values are taken from manufacturer datasheets.

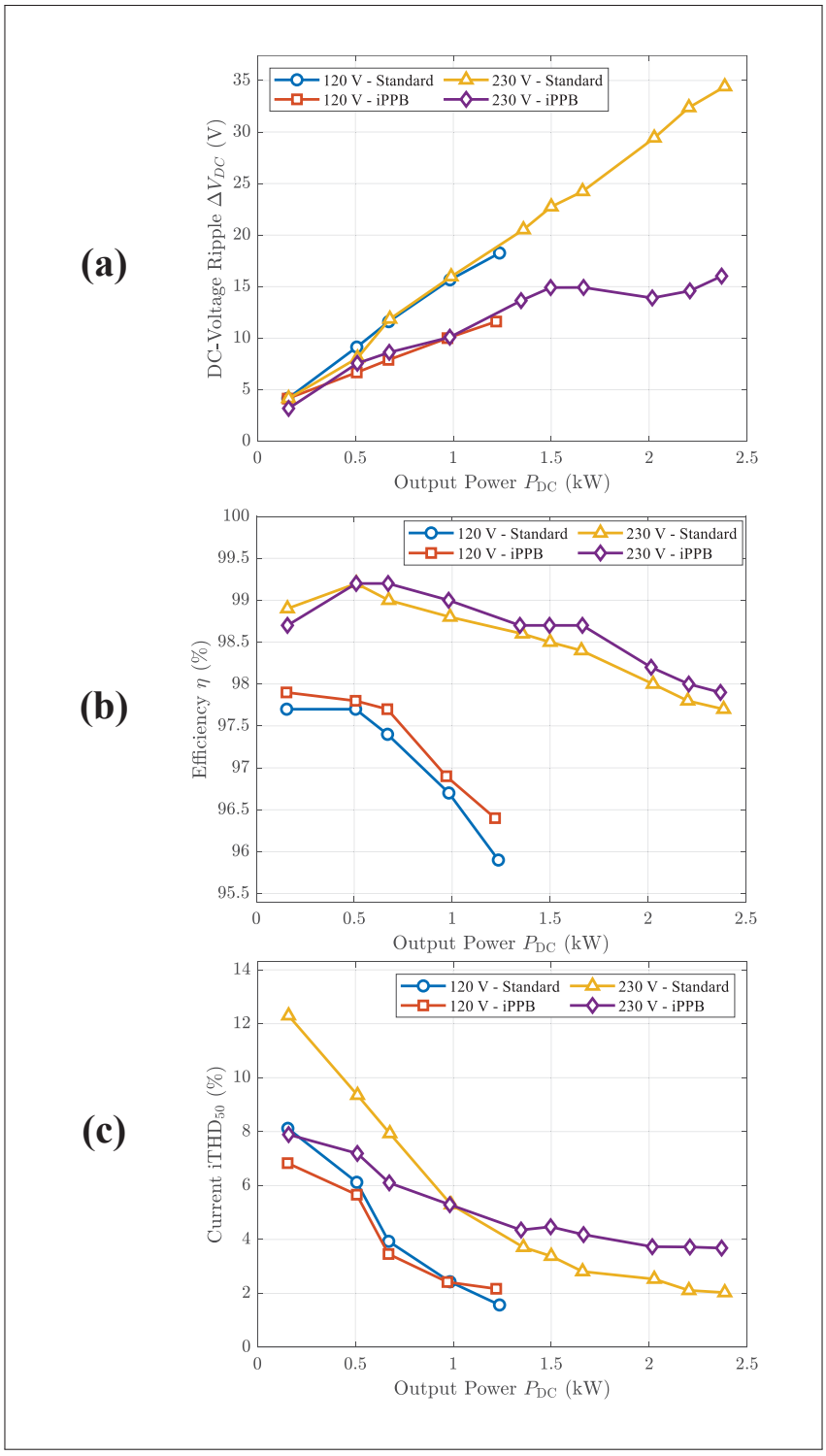


Figure 5.13 Performance versus output power P_{DC}: (a) DC-link ripple ΔV_{DC}, (b) measured efficiency η, and (c) grid-current $i\text{THD}_{50}$. Curves compare standard and iPPB operation at v_G = 120 V_{rms} and 230 V_{rms}

5.5.5 Comparison

Table 5.5 compares integrated PPB in FC PFCs with conventional (no-PPB) front-ends and auxiliary active PPB solutions with roughly similar specifications. The proposed iPPB TP-4CFC regulates V_{DC} to ~3.6% ripple (14.4 V at 400 V) with 55% ripple reduction versus a no-PPB baseline, using no buffer inductor and only 3×70 μF film capacitors in the FC stack. Auxiliary APPB designs (e.g., H-bridge+LC or APPB SSB) achieve higher ripple suppression but add substantial L_{buff} and passives, shifting size and cost to the buffer stage.

The FC-based iPPB keeps C_{DC} moderate and avoids L_{buff}, with bottom FC-cell stress limited to $0.5\,V_{DC}$ and other HF devices at $0.25\,V_{DC}$; auxiliary APPB and conventional PFCs typically operate HF devices at V_{DC} and depend on either added L_{buff} (APPB) or larger C_{DC} (no-PPB). Power quality and dynamics are maintained: THD < 4% at rated, large load-step settling to 2.5 kW in ~10 ms, $\overline{f_{sw}} \approx 39$ kHz, and measured $\eta \approx 98\%$. Several APPB examples with aggressive C_{DC} reduction show slower load-step response with larger V_{DC} deviations.

Table 5.5 Comparison of this work and previous works in literature with selected single-phase PFCs (iPPB/APPB/no-PPB): at comparable operating points

	This Work	(Menzi *et al.*, 2022)	(Kampl & Garcia, 2018)	(Ishraq & Mallik, 2024a)	(Wang *et al.*, 2022)	(Brooks, Liao & Pilawa-Podgurski, 2018)	(Kushwaha, Khadkikar, Shawky El Moursi & Zeineldin, 2025)
Topology	iPPB TP–4CFC	iPPB 3L–FC	Full-bridge TP	Interleaved TP–4L FC	H-bridge + LC APPB	6L–FC + SSB APPB	BL Zeta
Power (W)	2500	2200	2500	2500	1000	1500	500
V_{DC} **&** ΔV_{DC} **(V | %)**	400 | 3.6	400 | 5.3	400 | —	400 | 6.28	400 | 3.8	400 | 2.5	400 | 3.0
ΔV_{DC} **reduction (%)**	55	28	—	—	89	~Full	17
V_{ac} **(V_{rms})**	230	230	230	240	110	240	110
C_{buff} **/** C_{DC} **(μF)**	3×70 / 480	50 / 610	— / 1120	4×11 / 660	90 / 120	430 / 100	10 / 400
L_G **/** L_{buff} **(μH)**	250 / —	140 / —	650 / —	2×85.2 / —	(165 + 954) / 400	44 / 94	1000 / 25
HF $V_{\text{stress,max}}$ **($\times V_{DC}$)**	0.5; 0.25	1.0	1.0	0.33	1.0	0.20	$0.5 + V_{in}$
THD (%)	3.72	3.2	NR	4.33	3.56	2.07	3.6
$\overline{f_{sw}}$ **(kHz)**	39	35	65	94	50	150	20
$P_1 \rightarrow P_2$ **(kW),** t_{settle} **(ms)**	0.15→2.5, 10	NR	0→2.5, 40	1.0→0.5, 200	0.5→1.0, 120	0.10→0.15, 1000	NR
η **(%) at rated power**	98.0	NR	98.5	99.0	NR	98.38	93.08

NR: not reported; — not applicable. V_{ac} is the nominal line voltage. ΔV_{DC} reduction is computed from the reference's reported P, V_{DC}, and measured DC-link ripple relative to a no-PPB baseline. $V_{\text{stress,max}}$ lists HF-device blocking. Load-step entries show commanded step and settling time; when not stated, times are estimated from results. Experimental design values are presented.

5.6 Conclusions

The approach integrates the twice-line-frequency buffer into the FC stack of a single-phase TP–4CFC PFC rectifier, eliminating auxiliary PPB hardware and reducing reliance on large C_{DC}. A weight-free, fixed-time lexicographic MPC with a common-offset FC reference preserves multilevel sharing and expands usable buffering on the existing hardware.

On a 2.5 kW prototype operated over a wide range, the approach achieves up to 54% reduction in DC-link ripple with grid-current THD within limits. Rated load steps settle within a half-line cycle; efficiency gains are confirmed by loss and stress analyses; device stresses remain within ratings; and DC-link RMS current decreases as ripple energy is routed into the FC stack. The method is adaptable to converters with various numbers of FC cells and provides a practical benchmark for iPPB topologies that use low-frequency currents to buffer energy. These results support higher power density and improved reliability for front-end rectifiers, including EV on-board chargers and server/telecom supplies.

CHAPTER 6

THREE-PHASE ISOLATED MATRIX-TYPE PFC RECTIFIER WITH DUTY-CYCLE LOSS COMPENSATION AND REACTIVE POWER SUPPORT

This chapter describes a modified modulation concept for a three-phase isolated pulse-width-modulated (PWM) buck rectifier based on a direct matrix converter. The proposed scheme enables phase-shift operation of the input currents with respect to the mains voltage up to ±30° while compensating grid current distortion at the sector boundaries. The modulation is based on space vector modulation (SVM) and allows the generation of reactive power to compensate the input displacement factor introduced by the grid-side filter, so that a near-unity power factor is maintained even at light-load conditions. The chapter starts with a brief review of the converter operation under SVM. Then, the output voltage of the converter is derived for adjustable power-factor operation, and a generalized duty-cycle loss expression is obtained that remains valid under phase-shift operation. The implementation aspects of the proposed modulation scheme are discussed, and its effectiveness is demonstrated through simulation results for a 400 V (rms), 50 Hz three-phase input supplying a 200 V dc output at power levels up to 6 kW.

Within the context of this thesis, the presented converter exemplifies a three-phase front-end architecture that eliminates the bulky intermediate dc-link capacitor and integrates isolation and power factor correction in a single stage. By compensating duty-cycle loss associated with transformer leakage inductance through appropriate modulation, the converter maintains high power quality without resorting to oversized grid-side and output passive components, contributing to the overall objective of achieving compact and reliable ac–dc conversion systems.

6.1 INTRODUCTION

High-power three-phase isolated dc supplies are usually implemented using two-stage conversion, where the mains ac voltage is first converted into an intermediate dc link and then processed by an isolated dc-dc converter to obtain the required output voltage and galvanic isolation (Kolar & Friedli, 2013). A single-stage three-phase isolated PFC rectifier based on a matrix

converter was proposed in (Vlatkovic, Borojevic & Lee, 1995) and is adopted as the basis for this chapter. The topology is shown in Fig. 6.1. The direct matrix converter (Afsharian, Xu, Wu, Gong & Yang, 2018) converts the grid-frequency ac voltage directly to a high-frequency (HF) ac voltage, so that an intermediate dc-link capacitor is not required. Eliminating the dc-link capacitor and reducing the number of large passive components improves reliability, efficiency, and power density, which is consistent with the objectives of this thesis.

In this topology, the matrix converter can be regarded as a three-phase current source rectifier supplying the primary of an HF transformer. To provide galvanic isolation without transformer core saturation, the transformer primary voltage must satisfy volt-second balance over each switching period. The modulation objectives are to maintain sinusoidal grid currents with a controlled displacement factor at the input and to generate an alternating HF voltage at the transformer primary. A modified SVM scheme is employed to meet these objectives and to explicitly account for the effect of transformer leakage inductance on the converter characteristics.

The leakage inductance causes commutation overlap of the output diodes, which keeps the output current nearly constant, but it also introduces duty-cycle loss and distortion in the grid currents. This distortion is most pronounced at sector boundaries, where the applied line-to-line voltage vectors change. In this chapter, duty-cycle loss compensation is formulated as a function of the displacement factor ϕ, the general behavior of the duty-cycle loss is derived for phase-shift operation, and the converter is operated with limited reactive power support.

Fig. 6.1 shows the matrix-converter-based three-phase isolated PWM buck rectifier power stage. The circuit consists of input filter inductors L_f and capacitors C_f, a three-phase to HF single-phase matrix converter, an HF isolation transformer, a diode bridge rectifier, a dc filter inductor L_o and capacitor C_o, and a dc load. The matrix converter synthesizes the HF voltage v_p at the primary of the HF transformer and shapes the grid currents to be sinusoidal. Each bidirectional switch is implemented using two anti-series MOSFETs. The HF transformer is modeled as a series leakage inductance L_{lk} and an ideal transformer with a turns ratio $1:N$. The dc load is represented by a resistance R_o.

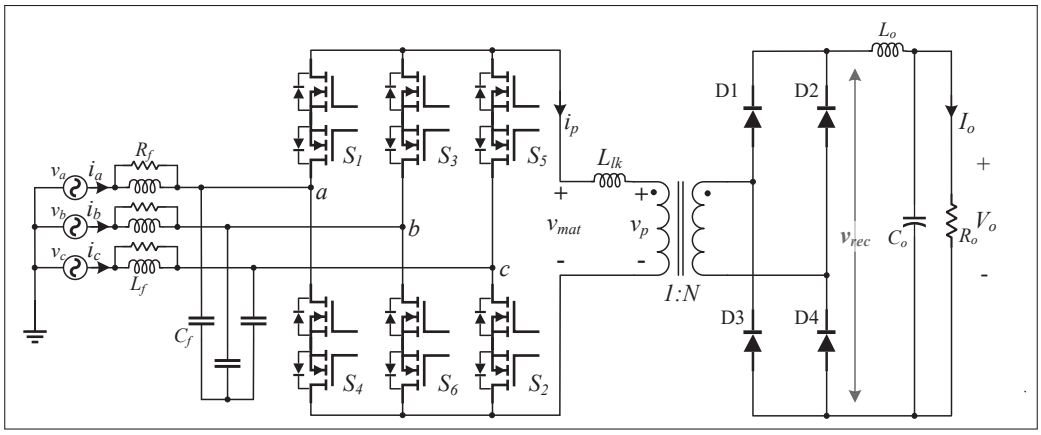


Figure 6.1 Configuration of the three-phase isolated PWM buck rectifier based on a direct matrix converter, illustrating grid-side filter inductors L_f and capacitors C_f, matrix converter stage, HF transformer with leakage inductance L_{lk} and turns ratio $1:N$, output filter inductor L_o and capacitor C_o, and dc load R_o

This chapter is organized as follows. Section 6.2 briefly reviews the converter operation under SVM, including the state vector diagram and the optimal switching pattern. Section 6.3 derives the output voltage and duty-cycle loss expressions and introduces the concept of limited reactive power support. The practical implementation of the modified modulation technique is presented in Section 6.4. Simulation results comparing operation with and without duty-cycle loss compensation are discussed in Section 6.5, and Section 6.6 provides concluding remarks.

6.2 REVIEW OF CONVERTER OPERATION

The converter uses the optimal six-segment PWM modulation scheme proposed in (Afsharian *et al.*, 2018). Within each 60 degree line-voltage sector, the line-to-line voltage with the highest absolute value (for example v_{ac} in sector 1) is applied first at the beginning of the switching period, followed by the line-to-line voltage with the second highest absolute value (for example v_{ab}), as illustrated in Fig. 6.3. This sequence maintains a high-to-low (HTL) transition of the primary voltage v_p over the power cycle.

To avoid flux saturation in the HF transformer, the primary voltage v_p must satisfy volt-second balance within each switching period T_s. To obtain a positive HF transformer primary current i_p,

the adjacent switching states corresponding to the sector in which the rotating reference current vector I_{ref} is located are applied. To obtain a negative i_p, the adjacent switching states of the opposite sector are applied with equal dwell times in order to create an alternating current. The available current switching states and corresponding grid phase currents are listed in Table 6.1. The quantity I_p denotes the magnitude of i_p and is equal to NI_o under the assumption of negligible output current ripple. At any instant, exactly one switch in the upper group and one switch in the lower group conduct.

Table 6.1 Possible Switching States

Switching State	Conducting Switch	i_a	i_b	i_c
I_1	S_6, S_1	I_p	$-I_p$	0
I_2	S_1, S_2	I_p	0	$-I_p$
I_3	S_2, S_3	0	I_p	$-I_p$
I_4	S_3, S_4	$-I_p$	I_p	0
I_5	S_4, S_5	$-I_p$	0	I_p
I_6	S_5, S_6	0	$-I_p$	I_p
I_7	S_1, S_4	0	0	0
I_8	S_3, S_6	0	0	0
I_9	S_5, S_2	0	0	0

Sinusoidal grid phase currents are synthesized by averaging, over each switching period T_s, the constant-magnitude current pulses defined in Table 6.1. The HF components in the phase currents are filtered by the input LC filter. Let i_a, i_b, and i_c be the grid phase currents that lead the phase voltages v_a, v_b, and v_c by the displacement angle ϕ. The phase voltages and currents can be expressed as

$$\begin{bmatrix} i_a \\ i_b \\ i_c \end{bmatrix} = I_m \begin{bmatrix} \cos(\theta) \\ \cos(\theta - 2\pi/3) \\ \cos(\theta + 2\pi/3) \end{bmatrix}, \quad \begin{bmatrix} v_a \\ v_b \\ v_c \end{bmatrix} = V_m \begin{bmatrix} \cos(\theta - \phi) \\ \cos(\theta - 2\pi/3 - \phi) \\ \cos(\theta + 2\pi/3 - \phi) \end{bmatrix} \tag{6.1}$$

where I_m is the fundamental peak phase current and V_m is the peak phase voltage. The modulation index is defined as $m_a = I_m/I_p$.

The current space vector for the three-phase input current is given by

$$\boldsymbol{I}_i = \frac{2}{3}\left[i_a + i_b e^{j2\pi/3} + i_c e^{-j2\pi/3}\right] \tag{6.2}$$

Substituting the switching states from Table 6.1 into (6.2) yields the current switching space vectors (SSV), which are shown in Fig. 6.2 with sector information:

$$I_k = \frac{2}{\sqrt{3}} I_p e^{-j\left((k-1)\frac{\pi}{3}-\frac{\pi}{6}\right)} \tag{6.3}$$

where k is the sector number.

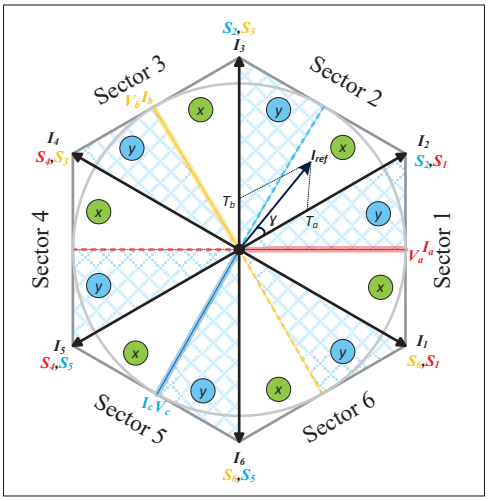


Figure 6.2 Current switching space-vector (SSV) representation with sector numbering

Space vector modulation is used to determine the switching times of the SSV. The rotating current reference vector I_{ref}, which rotates at the grid frequency, is synthesized by applying the two adjacent active vectors I_a and I_b and the zero vector I_0 from the sector where I_{ref} is located and from the opposite sector. The dwell times T_a, T_b, and T_0 are obtained from current-second balancing

$$\boldsymbol{I}_{ref} T_s = \boldsymbol{I}_a T_a + \boldsymbol{I}_b T_b + \boldsymbol{I}_0 T_0 \tag{6.4}$$

which leads to

$$
\begin{aligned}
T_a &= m_a T_s \sin\left(\frac{\pi}{6} - \gamma\right) \\
T_b &= m_a T_s \sin\left(\frac{\pi}{6} + \gamma\right) \quad \text{for } -\frac{\pi}{6} \leq \gamma < \frac{\pi}{6} \\
T_0 &= T_s - T_a - T_b
\end{aligned}
\tag{6.5}
$$

Here $\gamma = \theta - (k-1)\pi/3$ is the local angle that I_{ref} makes with the SSV within a given sector. The resulting switching pattern forms the matrix converter output voltage v_{mat} shown in Fig. 6.3 by dividing the dwell times into equal parts for the positive and negative half-cycles of the HF voltage.

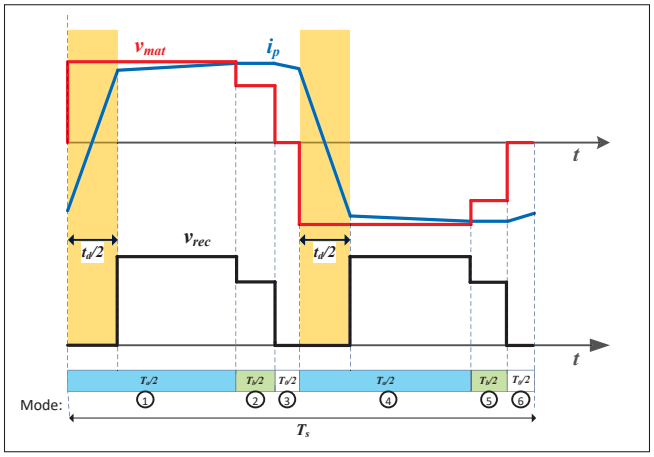


Figure 6.3 Matrix converter output voltage v_{mat}, transformer primary current i_p, and rectified voltage v_{rec} with conduction states and duty-cycle loss duration t_d

To maintain the HTL transition, the switching times must be swapped when the second-largest line-to-line voltage becomes the largest, and vice versa, as illustrated in Fig. 6.4. Each sector is therefore divided into two parts, x and y. Equation (6.5) applies to part x of the sector, while the dwell times T_a and T_b are interchanged in part y. The variation of the dwell times over a sector is shown in Fig. 6.5.

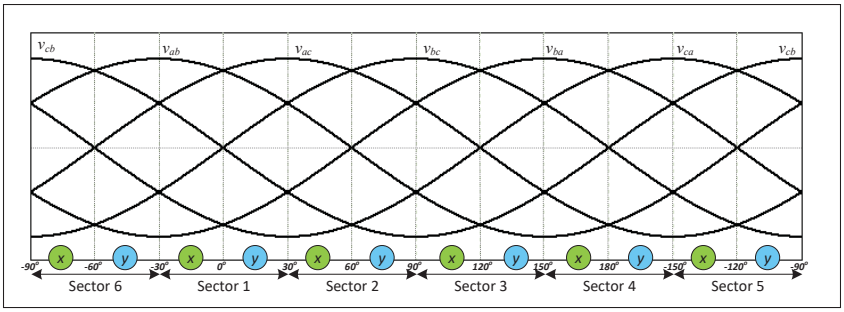


Figure 6.4 Line-to-line voltage variation within a sector

6.3 STEADY STATE ANALYSIS

This section derives the output voltage expression for adjustable power factor operation and formulates the duty-cycle loss caused by transformer leakage inductance, together with a corresponding compensation method.

6.3.1 Derivation of Output Voltage for Adjustable Power Factor

At steady state, the rectifier output voltage is denoted by V_o. The output voltage V_o is assumed to be constant over a switching cycle, which is a valid approximation at high switching frequency. The expression for V_o can be obtained from the volt-second balance across the dc output filter inductor L_o.

The voltage across L_o in the different operating intervals of sector 1, neglecting duty-cycle loss, is listed in Table 6.2.

The volt-second balance equation for L_o is

$$-V_o T_0 + (N v_{ab} - V_o) T_a + (N v_{ac} - V_o) T_b = 0$$

Substituting the phase voltages from (6.1), the dwell times from (6.5), and simplifying, yields

$$V_o = \frac{3}{2} N V_m m_a \cos\phi \tag{6.6}$$

Table 6.2 Voltage across inductor L_o

Mode	Voltage L_o	Duration
1	$-V_o$	$T_0/2$
2	$Nv_{ab} - V_o$	$T_a/2$
3	$Nv_{ac} - V_o$	$T_b/2$
4	$Nv_{ab} - V_o$	$T_a/2$
5	$Nv_{ac} - V_o$	$T_b/2$
6	$-V_o$	$T_0/2$

where V_m is the peak phase voltage, m_a is the modulation index, and ϕ is the displacement angle between the input phase currents and voltages. Equation (6.6) gives the output voltage of the rectifier for adjustable power factor operation and shows that the output voltage decreases as the power factor decreases.

6.3.2 Duty Cycle Loss and its Compensation

Due to the transformer leakage inductance L_{lk}, the primary current I_p requires a finite time to reverse its direction, as illustrated in Fig. 6.3. During this commutation interval, all secondary-side diodes conduct simultaneously to keep the output current I_o approximately constant. As a result, the HF transformer primary and secondary voltages are clamped close to zero (neglecting the diode voltage drops), and there is no net energy transfer from the ac side to the dc side. This condition causes circulating currents in the matrix converter switches and reduces the effective duty cycle of the rectified transformer voltage v_{rec} compared with the matrix converter output voltage v_{mat}, as seen in Fig. 6.3. The associated duty cycle loss reduces the output voltage and produces distortion of the input currents near sector boundaries. The duty-cycle loss becomes more significant at higher switching frequency and can limit the achievable switching frequency in practice.

The duty-cycle loss can be compensated by increasing the effective duty of the transformer secondary voltage. This can be achieved by extending the dwell time of the higher switching state by an amount equal to the time required for the current I_p to change its direction, while reducing the zero-state time accordingly. Here, the higher switching state denotes the active state that is closer to the reference current vector. Duty-cycle loss compensation improves the grid current total harmonic distortion (THD) and decreases the ripple in the output voltage.

Let ΔI_p denote the total change in the primary current I_p when it reverses from positive to negative or from negative to positive. The magnitude of I_p at the instant when its direction changes depends on the load current and is approximately equal to NI_o. The load current I_o is assumed to have negligible ripple due to sufficiently high L_o. The duty-cycle loss duration t_d can then be written as

$$\Delta I_p \cong 2NI_o$$

$$t_d = 2\frac{L_{lk}\Delta I_p}{V_{Lk}(\gamma)} = 4\frac{L_{lk}NI_o}{V_{Lk}(\gamma)} \tag{6.7}$$

where V_{Lk} is the voltage across the leakage inductance during the current transition. The voltage V_{Lk} varies with the local angle γ and, under the HTL transition condition, is equal to the highest absolute value of the line-to-line voltage. From (6.7) it follows that duty-cycle loss is largest when V_{Lk} is minimum. The minimum value of V_{Lk} can be expressed as

$$V_{Lk}(\gamma) = \sqrt{3}V_m\cos(\sigma), \quad \sigma = \begin{cases} \gamma - \dfrac{\pi}{6} & \text{for} \quad \gamma \geq 0 \\ \gamma + \dfrac{\pi}{6} & \text{for} \quad \gamma < 0 \end{cases} \tag{6.8}$$

Combining (6.7) and (6.8) gives

$$t_d = 4\frac{L_{lk}NI_o}{\sqrt{3}V_m\cos\sigma}$$

Using (6.6) to express V_m as a function of the output voltage, the duty-cycle loss duration can be written as

$$t_d = 2\sqrt{3}\frac{N^2 m_a L_{lk}\cos\phi}{R_o\cos\sigma} \tag{6.9}$$

Equation (6.9) gives the duty-cycle loss duration for the six-segment SVM modulation as a function of the power factor angle. This time interval can be added to the higher switching state dwell time to increase the effective duty cycle of the secondary voltage and compensate the duty-cycle loss. The modified switching times, taking into account the swapping of T_a and T_b after the sector part x, can be written as

$$\begin{aligned} T_a' &= m_a T_s \sin\left(\frac{\pi}{6} - \gamma\right) + t_d \quad \text{for } -\frac{\pi}{6} \le \gamma < 0 \\ T_b &= m_a T_s \sin\left(\frac{\pi}{6} + \gamma\right) \end{aligned} \tag{6.10}$$

Figure 6.5 illustrates the modified switching times after duty-cycle loss compensation.

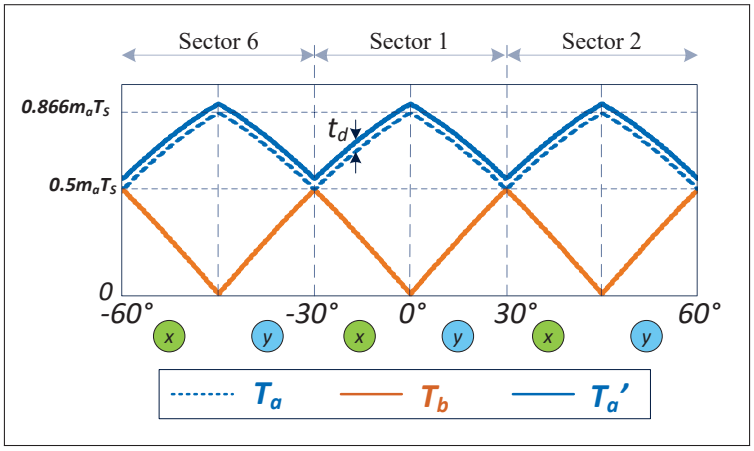


Figure 6.5 Modified switching times after duty-cycle loss compensation

The maximum modulation index m_{max} is now limited to

$$m_{max} = 1 - D_{d(max)},$$

where the maximum duty-cycle loss $D_{d(max)}$ is

$$D_{d(max)} = 4\frac{N^2 m_a L_{lk} \cos\phi}{R_o T_s} \tag{6.11}$$

6.3.3 Limited Reactive Power Support

The SVM technique can also be extended to adjust the phase between the input voltages and currents, and thereby provide reactive power for input displacement factor or power factor correction. The input displacement angle can be obtained as in (Hiti, Vlatkovic, Borojevic & Lee, 1994) and is used as the parameter ϕ in the modulation. Introducing a phase shift ϕ reduces the maximum dc output voltage that can be obtained from the converter.

When a phase shift is applied to the reference current I_{ref}, the corresponding phase input voltage becomes out of phase with the current. The admissible phase shift magnitude is limited to approximately $\pm 30°$, since beyond this value one of the corresponding SSV line-to-line voltages changes polarity (Malesani & Tenti, 1987), as illustrated in Fig. 6.6 by the blue line. For example, in sector 1 the switching pairs (S_6, S_1) and (S_2, S_1) are active and the corresponding line-to-line voltages are v_{ab} and v_{ac}. For a phase shift larger than 30° (with respect to Fig. 6.6), v_{ac} changes polarity, and the modulation pattern of Fig. 6.3 cannot be maintained. The output voltage under phase-shifted operation is still calculated from (6.6).

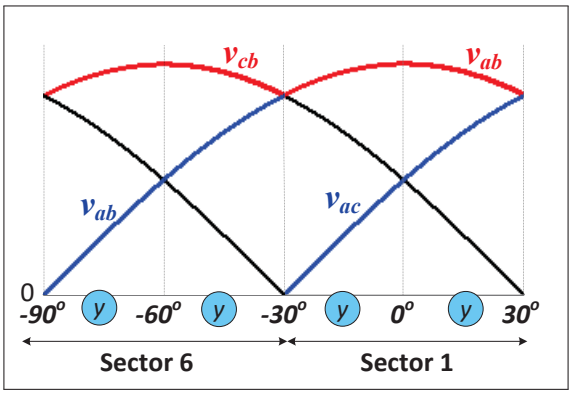


Figure 6.6 Line-to-line voltage variation in a sector for $\phi = -30°$. The red and blue traces indicate the high and low absolute values of the applied line-to-line voltages in the corresponding sector

As discussed earlier, the duty-cycle loss duration t_d is inversely proportional to V_{Lk} during the current transition. The current direction change takes place during the first applied switching state. Maintaining HTL transitions causes the current to rise or fall faster and reduces t_d. To

preserve the HTL property under phase-shifted operation, the sector parts x and y are shifted by ϕ, as shown in Fig. 6.7. For example, in Fig. 6.6 with $\phi = -30°$, the entire sector becomes part y.

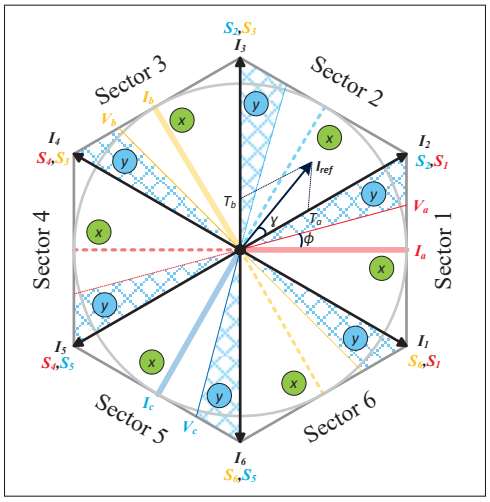


Figure 6.7 Space vector diagram when I_{ref} is phase shifted for power factor correction

6.4 IMPLEMENTATION OF SVM

The block diagram of the SVM implementation for converter pulse generation is shown in Fig. 6.8. The sector location is obtained from the phase angle θ provided by the PLL, which is computed from the measured phase voltages. The reference current space vector is calculated from the PLL output and the phase shift angle ϕ. The sectors are divided into twelve parts as shown in Fig. 6.7, and the local angle γ is computed from θ and the sector information.

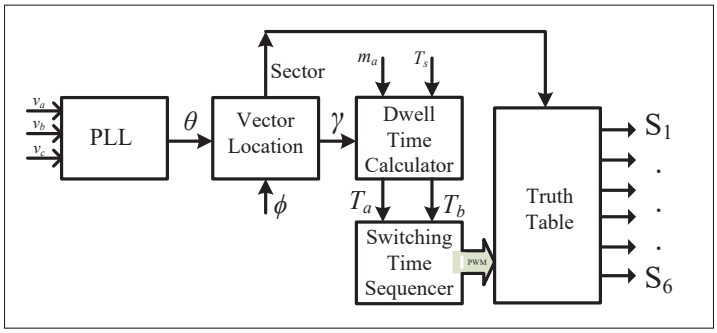


Figure 6.8 Block diagram of SVM implementation for converter pulse generation

The dwell times T_a and T_b are calculated using (6.10) from the input modulation index m_a and the switching frequency of the converter. The switching pattern for one switching cycle is generated by the switching sequencer shown in Fig. 6.9. A carrier waveform with twice the switching frequency is compared with the thresholds $1 - T_b/T_s$ and $1 - (T_a + T_b)/T_s$. Four PWM signals, denoted A, B, Z, and I, are generated with the sequencing discussed in the previous section. The inversion PWM signal I is used to distinguish between the positive and negative half-cycles.

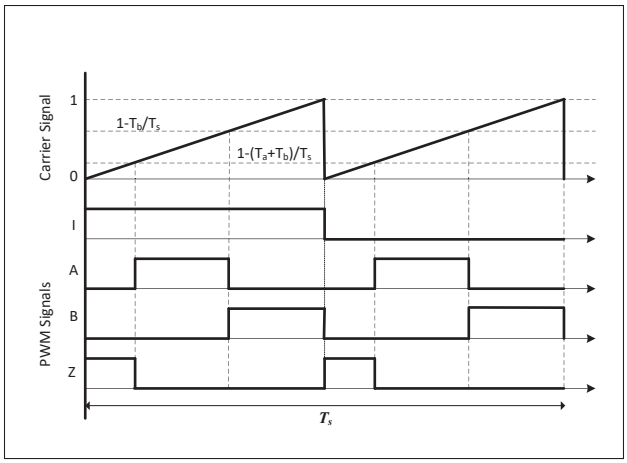


Figure 6.9 Switching-time sequencer for generation of PWM signals A, B, Z, and I

Using the fact that exactly one switch in each leg is always ON within a sector and that the other switches are controlled according to the SVM dwell times, a truth table is defined for the positive and negative half-cycles. The positive half-cycle (I = 1) truth table is given in Table 6.3, and the negative half-cycle (I = 0) truth table is given in Table 6.4. The inputs to the truth tables are the sector index and the PWM signals A, B, Z, and I. From these inputs, six gate pulses are generated for the matrix converter switches.

6.5 SIMULATION RESULTS

A comprehensive simulation model is developed and the performance of the converter is evaluated using the modulation and duty-cycle loss compensation scheme described in Section 6.4, and

Table 6.3 Truth table implementation for inversion signal $I = 1$ (positive cycle)

Sector	S_1	S_2	S_3	S_4	S_5	S_6
1(x)	B	0	Z	0	A	1
1(y)	1	A	0	Z	0	B
2(x)	1	B	0	Z	0	A
2(y)	B	1	A	0	Z	0
3(x)	A	1	B	0	Z	0
3(y)	0	B	1	A	0	Z
4(x)	0	A	1	B	0	Z
4(y)	Z	0	B	1	A	0
5(x)	Z	0	A	1	B	0
5(y)	0	Z	0	B	1	A
6(x)	0	Z	0	A	1	B
6(y)	A	0	Z	0	B	1

Table 6.4 Truth table implementation for inversion signal $I = 0$ (negative cycle)

Sector	S_1	S_2	S_3	S_4	S_5	S_6
1(x)	0	A	1	B	0	Z
1(y)	Z	0	B	1	A	0
2(x)	Z	0	A	1	B	0
2(y)	0	Z	0	B	1	A
3(x)	0	Z	0	A	1	B
3(y)	A	0	Z	0	B	1
4(x)	A	0	Z	0	B	1
4(y)	1	A	0	Z	0	B
5(x)	1	B	0	Z	0	A
5(y)	B	1	A	0	Z	0
6(x)	A	1	B	0	Z	0
6(y)	0	B	1	A	0	Z

for comparison, also without duty-cycle loss compensation. The main converter specification and simulation parameters are summarized in Table 6.5.

Table 6.5 Converter specification and simulation parameters

Parameter	Value
Grid line voltage	400 V, 50 Hz
Switching frequency	50.4 kHz
Power rating	6 kVA
Load resistance R_o	10 Ω
MOSFET on resistance R_{dson}	65 mΩ
Leakage inductance L_{lk}	40 μH
Grid filter capacitance C_f	2 μF
Grid filter inductance L_f	300 μH
Output filter inductance L_o	400 μH
Transformer turns ratio N	0.5

The switching frequency of the converter is selected as an integer multiple of 600 Hz so that an integer number of switching cycles is completed within each 60 degree line-voltage sector. This avoids incomplete switching sequences at sector transitions.

Figure 6.10 shows the simulated grid phase currents without duty-cycle loss compensation. The step changes in effective duty cycle at the sector boundaries cause distortion at those instants and increase the total harmonic distortion (THD). In this case, the THD of the grid current is found to be 5.6%.

Figure 6.11 shows the simulation results for a modulation index of $m_a = 0.85$ and $\phi = 0$ (unity power factor operation) with duty-cycle loss compensation enabled. The phase currents are in phase with the corresponding phase voltages, and the grid current THD is reduced to 1.12%. The figure also shows the HF voltage and current at the transformer primary, together with a zoomed view of the HF waveforms.

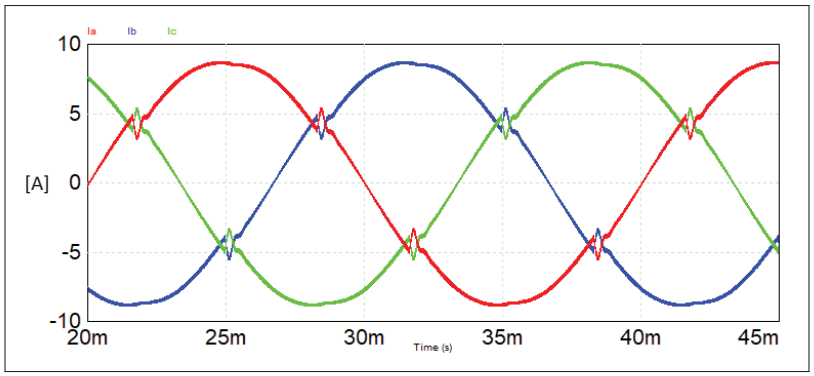


Figure 6.10 Distortion of grid current at sector boundaries without duty-cycle loss compensation, resulting in 5.6% THD

The capability of the converter to support limited reactive power is illustrated in Fig. 6.12. In this case, the phase current leads the corresponding phase voltage by 30° with a commanded displacement angle of $\phi = -30°$. Duty-cycle loss compensation is applied in this phase-shifted operating mode, and the grid currents are found to maintain low THD.

6.6 CONCLUSION

In this chapter a modified SVM concept has been presented for a three-phase isolated PWM buck rectifier based on a direct matrix converter. The modulation enables phase-shifted operation of the input currents with low total harmonic distortion in the grid currents by explicitly accounting for duty-cycle loss caused by the transformer leakage inductance. A duty-cycle loss expression has been derived that captures the dependence on switching frequency, load resistance, leakage inductance, and input displacement angle, and has been used to formulate a dwell-time compensation method that remains valid under phase-shift operation. The implementation of the modulation technique, including sector partitioning, switching sequence generation, and gate signal derivation, has been discussed, and simulation results for a 6 kVA, 400 V, 50 Hz three-phase system have been presented, demonstrating unity power factor operation with grid current THD of approximately 1.12 % and operation with limited reactive power support.

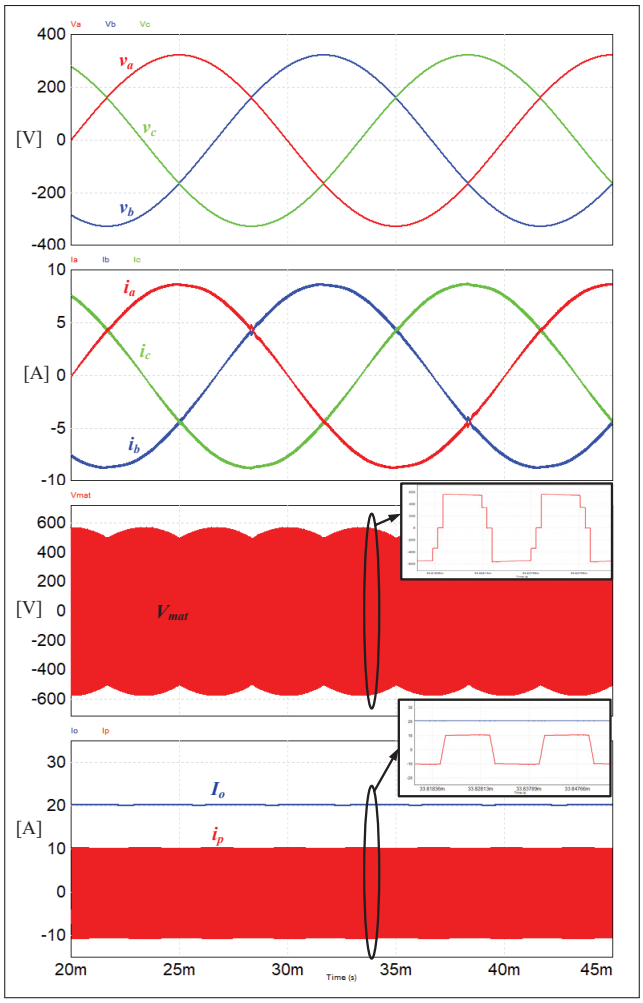


Figure 6.11 Simulation results for the converter with modified SVM and duty-cycle loss compensation, using the parameters in Table 6.5 and $m_a = 0.85$. Shown are the grid phase voltages v_a, v_b, v_c, grid phase currents i_a, i_b, i_c in unity power factor operation, matrix converter output voltage v_{mat}, HF transformer primary current i_p, and output load current I_o

Within the context of the thesis, the presented three-phase isolated front end illustrates how modulation and control of matrix-converter based rectifiers can be used as design degrees of freedom to mitigate duty-cycle related performance limitations and to eliminate the intermediate dc-link capacitor, thereby complementing the passive volume reduction strategies developed for the single-phase PFC topologies in the preceding chapters.

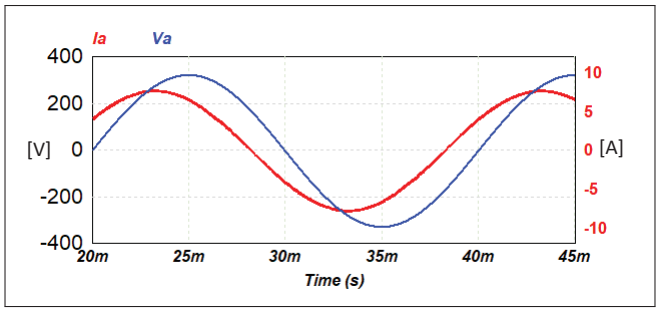


Figure 6.12 Phase-shifted operation of the converter with $\phi = -30°$, showing phase A voltage and current

CONCLUSION AND RECOMMENDATIONS

This thesis has investigated the design, control, and implementation of high power density grid-tied AC–DC conversion systems in which passive components set the dominant constraints on volume, weight, and lifetime. The focus has been on single-phase power factor correction (PFC) stages for electric-vehicle (EV) on-board chargers, data center and telecom rectifiers, and related single-phase interfaces. Across these applications, the initial problem was to reduce magnetic and capacitive energy storage used for power pulsation buffering, electromagnetic interference (EMI) filtering, and output decoupling, while preserving power quality, efficiency, and compatibility with cost-sensitive digital controllers.

The thesis has addressed this problem by combining flying-capacitor multilevel (FCML) topologies, integrated power pulsation buffering (PPB), and model predictive control (MPC) schemes tailored for practical implementation on microcontrollers for industrial applications. At the system level, the work has developed a comparison framework that links topology and control choices to passive volume and qualitative EMI implications under consistent few-kilowatt specifications. At the implementation level, the work has produced and experimentally validated converter prototypes and control architectures that embed twice-line-frequency energy buffering into the multilevel PFC stage and realize microcontroller-optimized MPC with deterministic execution at 6.6 micro seconds.

The main contributions can be summarized as follows.

Single-phase topology comparison and design levers

First, a structured comparison of single-phase AC–DC front ends and associated design levers has been established. Under representative specifications for EV on-board chargers and similar loads, simple analytic sizing laws have been derived for boost inductors, flying-capacitor stacks, and bulk DC-link capacitance, together with qualitative scaling relations for EMI filter volume.

Within this framework, different level counts, interleaving factors, and buffering strategies have been compared under equal-loss assumptions and basic energy-density based volume metrics. The analysis has shown that FCML totem-pole PFC stages combined with integrated buffering concepts shift part of the energy storage from low-frequency electrolytic DC-link capacitors to higher frequency inductors and capacitors with more favorable lifetime characteristics. This framework has provided a quantitative basis for selecting FCML structures as density levers relative to two-level totem-pole converters and other multilevel alternatives.

High-density TP–5L–FCML PFC hardware platform

Second, a 2.5 kW single-phase totem-pole five-level FCML PFC prototype has been designed and implemented as a hardware platform for the subsequent control developments. The converter interfaces a wide input-voltage range to a regulated DC bus using GaN devices and a three-board partition that separates power stage, sensor and control interface board, and digital controller. Small-signal models for current and voltage control have been derived, and nested control loops with phase-shifted PWM, dead-time compensation, feedforward, and active flying-capacitor balancing have been implemented on a C2000 microcontroller. Experimental results have demonstrated high efficiency, near-unity power factor, low input-current distortion, and controlled DC-link ripple over the operating range, with stable flying-capacitor voltages. This platform has served as the experimental backbone for the predictive control work and as a concrete validation of the passive sizing relations developed in the comparison framework.

Unified MPC for a four-level FCML OBC front end

Third, a unified finite-control-set MPC (FCS–MPC) framework has been developed for a single-phase four-level FCML front end in a bidirectional EV on-board charger. The controller covers grid-connected rectifier and inverter operation (G2V, V2G, V2H, V2V) and isolated grid-forming operation (V2L, islanded V2H) using a single switching-state enumeration and

prediction structure. Continuous-time and discrete-time models have been derived, and reference generation for active and reactive power in grid-connected modes and for output voltage in standalone modes has been formulated in a consistent manner. Simulation studies and experimental results on a laboratory prototype have shown that the unified FCS–MPC can track power and voltage references across the admissible operating range while respecting converter, grid, and battery constraints. This contribution demonstrates that a single FCML front end can support the diverse power flow requirements of modern on-board chargers when equipped with an appropriate predictive controller.

Integrated PPB in a TP–4CFC PFC converter with weighted-sum MPC

Fourth, an integrated PPB concept has been implemented in a four-cell flying-capacitor PFC converter (TP–4CFC) by repurposing the flying-capacitor stack to buffer twice-line-frequency power pulsation. A discrete-time model capturing the interaction among grid branch, DC link, and flying capacitors has been derived, and a multi-objective predictive control scheme (MOMPCC) with weighted-sum cost function has been formulated to address current tracking, DC-link voltage ripple, and capacitor voltage regulation simultaneously. Hardware experiments on the 2.5 kW prototype have confirmed that routing a significant fraction of the low-frequency energy into the flying-capacitor stack reduces DC-link ripple and allows a reduction of bulk DC-link capacitance, while maintaining grid-current quality, device stress margins, and efficiency at practical switching frequencies. This validates integrated PPB via flying capacitors as a viable approach to reduce low-frequency energy storage without adding a separate active buffer stage.

Lexicographic, weight-free MPC for integrated PPB

Fifth, to avoid the tuning effort associated with multi-term weighted cost functions and to simplify real-time implementation, a two-stage lexicographic MPC structure has been introduced for the same TP–4CFC converter with integrated PPB. The controller enforces inductor current

tracking as a primary objective in the first stage and evaluates flying-capacitor energy steering and switching effort in a second stage. A common-offset flying-capacitor reference structure has been proposed to extend the usable buffering range while maintaining cell voltage sharing, and a Hamming distance based tie-breaking rule has been adopted to limit unnecessary switching transitions. The resulting algorithm has been implemented on the C2000 microcontroller with deterministic, fixed execution time within a 6.66 microsecond sampling period. Experimental results over a wide operating range have shown substantial DC-link ripple reduction, controlled grid-current distortion, reduced DC-link rms current, and efficiency comparable to or better than the weighted-sum MOMPCC scheme. This demonstrates that advanced multi-objective MPC for integrated buffering can be realized within the timing and memory constraints of automotive and industrial microcontrollers.

Three-phase isolated matrix-type PFC rectifier

Sixth, a three-phase isolated matrix-type PFC rectifier has been analyzed as a representative three-phase front end that eliminates the intermediate DC-link capacitor and integrates isolation and PFC in a single stage. A modified space-vector modulation scheme has been developed that accounts for duty-cycle loss associated with transformer leakage inductance and enables adjustable displacement factor with limited reactive power support. Generalized duty-cycle loss expressions have been derived and used to construct dwell-time compensation strategies. Time-domain simulations for a multi-kilowatt three-phase system have demonstrated that near-unity power factor and low grid-current distortion can be maintained while removing the bulky DC-link capacitor and avoiding oversized grid-side filters and output components. Within the overall thesis, this study indicates how modulation and control of matrix-converter based rectifiers can be used as additional design degrees of freedom for passive-volume reduction in three-phase systems.

Taken together, these contributions address the initial problem of reducing passive energy storage in single-phase and three-phase front ends while maintaining power quality and practical control complexity. The analytic comparison framework clarifies the impact of topology, level count, interleaving, and buffering strategy on passive requirements. The hardware platforms and predictive control implementations demonstrate that FCML PFC stages with integrated PPB can achieve significant DC-link capacitance reduction and prospective power density gains at few-kilowatt power levels, using commercially available microcontrollers and switching devices.

7.1 Recommendations and Future Work

Based on the findings and limitations of this work, several directions for future research and development can be identified.

1. **Multi-objective topology and design-lever optimization.** The single-phase comparison framework should be extended into a systematic multi-objective optimization environment that combines analytic sizing laws with detailed device and magnetic models. Such a framework would generate Pareto fronts over efficiency, passive volume, cost, and reliability for a broader set of topologies, including additional hybrid ANPC, switched-capacitor, and interleaved architectures. This would enable more rigorous selection of front ends for given application constraints and lifetime targets.
2. **EMI filter modeling and validation.** The qualitative EMI metrics used in this thesis should be refined into quantitative EMI filter volume models for both differential-mode and common-mode noise in multilevel PFC front ends. Future work should include systematic measurement campaigns on FCML and reference converters, explicit modeling of layout and parasitics, and co-optimization of EMI filter design with the choice of switching patterns and modulation schemes. This would link passive-volume reduction directly to conducted EMI compliance.

3. **Passive sizing and lifetime assessment.** Detailed electro-thermal models and accelerated aging data for capacitors and magnetics should be integrated into the design process. This would allow FCML and integrated PPB architectures to be compared not only on volume and efficiency, but also on equal lifetime constraints. A combined treatment of thermal cycling, ripple current, and ambient conditions would help quantify the life-cycle benefits of reduced electrolytic usage and increased reliance on film and ceramic capacitors.
4. **Generalization of integrated PPB concepts.** The integrated PPB approach based on flying-capacitor stacks can be generalized to alternative buffer placements and higher power levels. Examples include series-stacked buffer architectures, integration with isolated DC–DC stages, and three-phase active decoupling structures. Future work should quantify the tradeoffs between embedding buffering in the power stage, using separate active buffers, and adopting hybrid approaches, with passive volume, lifetime, and control complexity as explicit objectives.
5. **Advanced MPC and modulation strategies under embedded constraints.** MPC formulations that include additional practical constraints, such as thermal limits, device margins, and grid-code requirements, should be investigated while keeping computational complexity suitable for embedded platforms. Possible directions include explicit MPC, reduced candidate-set strategies, hybrid modulation–prediction schemes, and learning-assisted prediction models that reduce online computation while preserving robustness and deterministic timing.
6. **Portability and scaling of control architectures.** The portability of the proposed MPC and PPB control schemes to alternative digital platforms and larger systems should be examined. This includes implementations on newer microcontrollers, multi-core processors, and FPGA–DSP combinations, as well as extensions to parallel or modular converters in which inter-module coordination and communication delays play a role. Such studies would

clarify how the proposed control structures scale to higher power and to more complex system architectures.

7. **Hardware realization of the three-phase matrix-type rectifier.** The three-phase isolated matrix-type rectifier concept should be moved from simulation to hardware prototyping. A future prototype should characterize steady-state efficiency, grid-current quality, conducted and radiated EMI, sensitivity to parameter variations, and behavior under grid disturbances and load transients. This would test the practical limits of duty-cycle loss compensation and modulation strategies in a realistic environment.
8. **System-level demonstrators and life-cycle metrics.** Finally, the proposed high-density front ends should be integrated into complete application demonstrators, such as full EV on-board chargers or data center rectifier modules. System-level studies should connect passive-volume reduction and control complexity to installation density, thermal management requirements, maintenance intervals, and total cost of ownership over realistic mission profiles. Such demonstrators would close the loop between component-level design and system-level performance.

These recommendations follow directly from the analytic tools, hardware platforms, and control strategies developed in this thesis. Their systematic investigation would further clarify the role of FCML topologies, integrated buffering, and predictive control in next-generation grid-tied AC–DC conversion systems that target high power density, reduced passive energy storage, and extended lifetime.

APPENDIX I

C FIRMWARE FOR IPPB FCML MPC ON F28379D - CHAPTER 4

This appendix lists the C firmware implementing the model predictive control for integrated power pulsation buffering (iPPB) single phase TP 4CFC PFC converter on the Texas Instruments TMS320F28379D microcontroller. The converter is controlled with a sampling period of $T_s = 6.66\ \mu$s, and the total real time execution per control step is approximately 6 μs, with the computational load shared between CPU1, CPU2, and CLA.

The following units are implemented:

- CPU1 real time MPC and voltage reference generation (Listing I.1), which executes the finite control set MPC cost evaluation, switching state arbitration, protection logic, generating control signals, and FC voltage reference generation.
- CPU1–CLA shared data structures (Listing I.2), which define the shared buffers, parameters, and result containers used between CPU1 and CLA.
- CLA task (Listing I.3), which implement the partial candidate evaluation routines executed on CLA1.
- CPU2 Voltage loop and instrumentation firmware (Listing I.4), which implements the dc link voltage regulation loop, PLL, notch filters, RMS and power measurement, and communication tasks.

The execution sequence and implementation details of the PPB MPC framework are discussed in the chapter 4 on PPB MPC; this appendix only provides the corresponding source code for reproducibility.

CPU1 Firmware Real Time MPC and FC Voltage Reference

```
//#############################################################################
// FILE: cpu1_main.c
// TITLE: CPU1 half of dual-core MPC control loop for F28379D
//#############################################################################

#include <float.h>
#include <math.h>
#include <stdbool.h>
#include <stdint.h>

```

```c
#include "f2837xd_device.h"
#include "driverlib.h"
#include "device.h"
#include "board.h"
#include "c2000ware_libraries.h"

#include "cpu1_cla_shared.h"

// ADC channel indices
enum
{
    kAdcGridVoltage   = 0,
    kAdcGridCurrent   = 1,
    kAdcCap1Voltage   = 2,
    kAdcCap2Voltage   = 3,
    kAdcCap3Voltage   = 4,
    kAdcCap4Voltage   = 5,
    kAdcDcLoadCurrent = 6,
    kAdcMpcEnable     = 7,
    kAdcChannelCount  = 8
};

// ADC scaling factors
#define GRID_VOLTAGE_SCALE      (0.331531086f)
#define GRID_CURRENT_SCALE      (0.009860055f)
#define CAP1_VOLTAGE_SCALE      (0.166500167f)
#define CAP2_VOLTAGE_SCALE      (0.166500167f)
#define CAP3_VOLTAGE_SCALE      (0.166500167f)
#define CAP4_VOLTAGE_SCALE      (0.331531086f)
#define IDC_CURRENT_SCALE       (0.004897891f)

// Output GPIO pin positions
#define S2_PIN   (0U)
#define S7_PIN   (1U)
#define S3_PIN   (2U)
#define S8_PIN   (3U)
#define S4_PIN   (4U)
#define S9_PIN   (5U)
#define S5_PIN   (6U)
#define S10_PIN  (7U)

#define OUTPUT_GPIO_MASK  (0x00FFU)

// IPC command identifiers
#define IPC_CMD_READ_MEM   (0x1001U)
#define IPC_CMD_RESP       (0x2001U)

// Protection thresholds
#define IINV_POS_LIMIT      (19.5f)
#define IINV_NEG_LIMIT      (-19.5f)
#define VC1_POS_LIMIT       (450.0f)
#define VC2_POS_LIMIT       (350.0f)
#define VC3_POS_LIMIT       (250.0f)
#define VC4_POS_LIMIT       (150.0f)

typedef enum
{
    kProtectionNone   = 0U,
    kProtectionIinvHi = 1U,
    kProtectionIinvLo = 2U,
    kProtectionVc1Hi  = 3U,
    kProtectionVc2Hi  = 4U,
    kProtectionVc3Hi  = 5U,
    kProtectionVc4Hi  = 6U
} ProtectionStatus_e;

```

```
77 // PPB reference configuration
78 #define PPB_REF_POWER   (0U)
79 #define PPB_REF_SIN     (1U)
80 #define PPB_REF_SLEW    (3U)
81 #define PPB_REF_MODE    PPB_REF_SLEW
82
83 // Global control state
84 volatile uint16_t gLedCounter = 0U;
85 volatile ProtectionStatus_e gProtectionStatus = kProtectionNone;
86 volatile float32_t gFaultMagnitude = 0.0f;
87 volatile bool gFaultLogged = false;
88
89 volatile uint16_t gMpcEnabled = 0U;            //!< 1 when MPC loop is active
90 volatile uint16_t gLoggingEnabled = 0U;
91 volatile uint16_t gPpbEnabled = 0U;
92
93 volatile float32_t gSin2ThetaPi = 0.0f;
94 volatile float32_t gSwingFactor = 0.25f;
95 volatile float32_t gPthFactor   = 0.0f;
96 volatile float32_t gPthFactor2  = 0.0f;
97 volatile float32_t gPthFactor3  = 0.0f;
98 volatile float32_t gPthFactor4  = 0.0f;
99 volatile float32_t gGridFrequencyHz = 60.0f;
100 volatile float32_t gChargeRateC1 = 1.0f;
101 volatile float32_t gChargeRateC2 = 1.0f;
102 volatile float32_t gChargeRateC3 = 1.0f;
103 volatile float32_t gDischargeRateC1 = 1.0f;
104 volatile float32_t gDischargeRateC2 = 1.0f;
105 volatile float32_t gDischargeRateC3 = 1.0f;
106
107 volatile float32_t gVdcFiltered = 0.0f;
108 volatile float32_t gIdcFiltered = 0.0f;
109
110 static float32_t gIrefSatPos = 17.0f;
111 static float32_t gIrefSatNeg = -17.0f;
112
113 static float32_t gSamplePeriod = 0.0f;
114 static float32_t gTsOverLg = 0.0f;
115 static float32_t gOneMinusRgTsOverLg = 0.0f;
116 static float32_t gTsOverC[kCapBankCount] = {0.0f};
117
118 static volatile bool gSwitchPulsesEnabled = true;
119
120 static volatile uint16_t gGlobalOptimalIndex = 0U;
121 static float32_t gCpuCost = FLT_MAX;
122 static uint16_t gCpuOptimalIndex = 0U;
123
124 //--------------------------------------------------------------------------
125 // Shared memory objects for CLA interaction
126 //--------------------------------------------------------------------------
127
128 #pragma DATA_SECTION(gClaMeasurements, "CLADataLS4")
129 volatile ClaMpcMeasurements gClaMeasurements = {0};
130
131 #pragma DATA_SECTION(gClaPrediction, "CLADataLS4")
132 volatile ClaMpcPrediction gClaPrediction = {0};
133
134 #pragma DATA_SECTION(gClaParameters, "CLADataLS4")
135 volatile ClaMpcParameters gClaParameters = {0};
136
137 #pragma DATA_SECTION(gClaResult, "cla1ToCpuMsgRAM")
138 volatile ClaMpcResult gClaResult = {0};
139
140 #pragma DATA_SECTION(gClaPrevSwitchNibble, "CLADataLS4")
141 volatile uint8_t gClaPrevSwitchNibble = 0U;
142
```

```
#pragma DATA_SECTION(gZeroCrossPolarity, "CLADataLS4")
volatile int16_t gZeroCrossPolarity = 0;

#pragma DATA_SECTION(gSkf, "CLADataLS4")
const float32_t gSkf[16][4] =
{
    {0.f, 0.f, 0.f, 0.f}, {0.f, 0.f, 0.f, 1.f}, {0.f, 0.f, 1.f, 0.f}, {0.f, 1.f, 0.f, 0.f},
    {1.f, 0.f, 0.f, 0.f}, {0.f, 0.f, 1.f, 1.f}, {0.f, 1.f, 0.f, 1.f}, {0.f, 1.f, 1.f, 0.f},
    {1.f, 0.f, 0.f, 1.f}, {1.f, 0.f, 1.f, 0.f}, {1.f, 1.f, 0.f, 0.f}, {0.f, 1.f, 1.f, 1.f},
    {1.f, 0.f, 1.f, 1.f}, {1.f, 1.f, 0.f, 1.f}, {1.f, 1.f, 1.f, 0.f}, {1.f, 1.f, 1.f, 1.f}
};

#pragma DATA_SECTION(gSwitchPopCount, "CLADataLS4")
const uint8_t gSwitchPopCount[16] =
{ 0U, 1U, 1U, 2U, 1U, 2U, 2U, 3U, 1U, 2U, 2U, 3U, 2U, 3U, 3U, 4U };

#pragma DATA_SECTION(gSwitchNibbles, "CLADataLS4")
uint8_t gSwitchNibbles[16] = {0};

//-----------------------------------------------------------------------------
// Local look-up tables (CPU only)
//-----------------------------------------------------------------------------

static uint16_t gSwitchSetMask[16] = {0};
static uint16_t gSwitchClearMask[16] = {0};

#pragma DATA_SECTION(gAdcRaw, "MSGRAM_CPU1_TO_CPU2")
volatile int16_t gAdcRaw[kAdcChannelCount] = {0};

// Utility functions
// Clamp a value into the provided range.
static inline float32_t clampf(float32_t value, float32_t lo, float32_t hi)
{
    if (value < lo) return lo;
    if (value > hi) return hi;
    return value;
}

// Build GPIO masks and switch nibbles for each candidate.
static void buildSwitchLookupTables(void)
{
    for (uint16_t index = 0U; index < 16U; ++index)
    {
        const float32_t *row = gSkf[index];
        const uint32_t s0 = (row[0] >= 0.5f) ? 1U : 0U;
        const uint32_t s1 = (row[1] >= 0.5f) ? 1U : 0U;
        const uint32_t s2 = (row[2] >= 0.5f) ? 1U : 0U;
        const uint32_t s3 = (row[3] >= 0.5f) ? 1U : 0U;

        uint32_t setMask = 0U;
        setMask |= (s0 << S2_PIN) | ((1U - s0) << S7_PIN);
        setMask |= (s1 << S3_PIN) | ((1U - s1) << S8_PIN);
        setMask |= (s2 << S4_PIN) | ((1U - s2) << S9_PIN);
        setMask |= (s3 << S5_PIN) | ((1U - s3) << S10_PIN);

        gSwitchSetMask[index] = (uint16_t)(setMask & OUTPUT_GPIO_MASK);
        gSwitchClearMask[index] = (uint16_t)(~setMask & OUTPUT_GPIO_MASK);

        gSwitchNibbles[index] = (uint8_t)((s0 << 3) | (s1 << 2) | (s2 << 1) | s3);
    }
}

// Write GPIO outputs for the selected candidate when allowed.
static inline void applyOutputs(uint16_t index, bool enabled, bool allowPulses)
{
    if (!enabled || !allowPulses || (index >= 16U))
```

```
209     {
210         GpioDataRegs.GPACLEAR.all |= OUTPUT_GPIO_MASK;
211         return;
212     }
213 
214     const uint16_t setMask = gSwitchSetMask[index];
215     const uint16_t clearMask = gSwitchClearMask[index];
216 
217     GpioDataRegs.GPACLEAR.all |= clearMask;
218     __asm(" RPT #29 || NOP");
219     GpioDataRegs.GPASET.all |= setMask;
220 }
221 
222 // Evaluate MPC cost for one candidate on the CPU side.
223 static inline float32_t evaluateCandidate(uint16_t index,
224                                           float32_t zc,
225                                           float32_t khPenaltyQuarter)
226 {
227     const float32_t *row = gSkf[index];
228     const float32_t sk01 = zc       - row[0];
229     const float32_t sk12 = row[0]   - row[1];
230     const float32_t sk23 = row[1]   - row[2];
231     const float32_t sk34 = row[2]   - row[3];
232 
233     const float32_t vc1 = gClaMeasurements.vCap[kCapBank1];
234     const float32_t v2Pred = gClaPrediction.v2Pred;
235     const float32_t v3Pred = gClaPrediction.v3Pred;
236     const float32_t v4Pred = gClaPrediction.v4Pred;
237     const float32_t iTemp  = gClaPrediction.iTemp;
238 
239     const float32_t vGrid   = gClaMeasurements.vGrid;
240     const float32_t current = gClaMeasurements.iInverter;
241 
242     const float32_t tsOverLg  = gClaParameters.tsOverLg;
243     const float32_t tsOverC2  = gClaParameters.tsOverC[kCapBank2];
244     const float32_t tsOverC3  = gClaParameters.tsOverC[kCapBank3];
245     const float32_t tsOverC4  = gClaParameters.tsOverC[kCapBank4];
246     const float32_t vRef2     = gClaParameters.vRef[kCapBank2];
247     const float32_t vRef3     = gClaParameters.vRef[kCapBank3];
248     const float32_t vRef4     = gClaParameters.vRef[kCapBank4];
249     const float32_t iRef      = gClaParameters.iRefPfc;
250     const float32_t k2        = gClaParameters.k2;
251     const float32_t k3        = gClaParameters.k3;
252     const float32_t k4        = gClaParameters.k4;
253     const float32_t k5        = gClaParameters.k5;
254 
255     const float32_t vinv = (sk01 * vc1) +
256                            (sk12 * v2Pred) +
257                            (sk23 * v3Pred) +
258                            (sk34 * v4Pred);
259 
260     const float32_t isk1 = iTemp + (tsOverLg * (vGrid - vinv));
261 
262     const float32_t v2k = v2Pred + (tsOverC2 * sk12 * current);
263     const float32_t v3k = v3Pred + (tsOverC3 * sk23 * current);
264     const float32_t v4k = v4Pred + (tsOverC4 * sk34 * current);
265 
266     const float32_t e2 = vRef2 - v2k;
267     const float32_t e3 = vRef3 - v3k;
268     const float32_t e4 = vRef4 - v4k;
269     const float32_t ei = isk1 - iRef;
270 
271     float32_t cost = (k2 * e2 * e2) +
272                      (k3 * e3 * e3) +
273                      (k4 * e4 * e4) +
274                      (k5 * ei * ei);
```

```
275
276     const uint8_t diff = gSwitchNibbles[index] ^ gClaPrevSwitchNibble;
277     cost += khPenaltyQuarter * (float32_t)gSwitchPopCount[diff & 0x0FU];
278
279     return cost;
280 }
281
282 // Update predicted states for the candidate chosen in the prior step.
283 static void updatePredictionForIndex(uint16_t index, float32_t zc)
284 {
285     const float32_t *row = gSkf[index];
286     const float32_t sk01 = zc       - row[0];
287     const float32_t sk12 = row[0]   - row[1];
288     const float32_t sk23 = row[1]   - row[2];
289     const float32_t sk34 = row[2]   - row[3];
290
291     const float32_t vc1 = gClaMeasurements.vCap[kCapBank1];
292     const float32_t vc2 = gClaMeasurements.vCap[kCapBank2];
293     const float32_t vc3 = gClaMeasurements.vCap[kCapBank3];
294     const float32_t vc4 = gClaMeasurements.vCap[kCapBank4];
295     const float32_t iInv = gClaMeasurements.iInverter;
296     const float32_t vGrid = gClaMeasurements.vGrid;
297
298     const float32_t tsOverLg = gClaParameters.tsOverLg;
299     const float32_t tsOverC2 = gTsOverC[kCapBank2];
300     const float32_t tsOverC3 = gTsOverC[kCapBank3];
301     const float32_t tsOverC4 = gTsOverC[kCapBank4];
302
303     const float32_t vinv = (sk01 * vc1) + (sk12 * vc2) +
304                            (sk23 * vc3) + (sk34 * vc4);
305     const float32_t isk1p = (gOneMinusRgTsOverLg * iInv) +
306                             (tsOverLg * (vGrid - vinv));
307
308     gClaPrediction.v2Pred = vc2 + (tsOverC2 * sk12 * iInv);
309     gClaPrediction.v3Pred = vc3 + (tsOverC3 * sk23 * iInv);
310     gClaPrediction.v4Pred = vc4 + (tsOverC4 * sk34 * iInv);
311     gClaPrediction.iTemp  = gOneMinusRgTsOverLg * isk1p;
312 }
313
314 // Refresh PPB voltage references based on grid/load conditions.
315 static void updateVoltageReferences(void)
316 {
317     gClaParameters.vRef[kCapBank1] = gVdcFiltered;
318     const float32_t vdc = gClaParameters.vRef[kCapBank1];
319
320     gSwingFactor = clampf(gSwingFactor, 0.0f, 0.25f);
321     const float32_t swingRange = gSwingFactor * vdc;
322
323     const float32_t pac = gClaMeasurements.vGrid * gClaParameters.iRefPfc;
324     const float32_t pdc = gVdcFiltered * gIdcFiltered;
325     const float32_t pdel = pac - pdc;
326
327     if (!gPpbEnabled)
328     {
329         gClaParameters.vRef[kCapBank2] = 0.75f * vdc;
330         gClaParameters.vRef[kCapBank3] = 0.50f * vdc;
331         gClaParameters.vRef[kCapBank4] = 0.25f * vdc;
332         return;
333     }
334
335 #if (PPB_REF_MODE == PPB_REF_POWER)
336     const float32_t swing = swingRange;
337     const float32_t threshold = pdc * gPthFactor;
338     const float32_t delta = (pdel > threshold) ? swing : -swing;
339     const float32_t ppbDelta = clampf(delta, -swingRange, swingRange);
340     gClaParameters.vRef[kCapBank2] = 0.75f * vdc + ppbDelta;
```

```
341     gClaParameters.vRef[kCapBank3] = 0.50f * vdc + ppbDelta;
342     gClaParameters.vRef[kCapBank4] = 0.25f * vdc + ppbDelta;
343 #elif (PPB_REF_MODE == PPB_REF_SIN)
344     const float32_t swing = swingRange;
345     const float32_t delta = swing * gSin2ThetaPi;
346     gClaParameters.vRef[kCapBank2] = 0.75f * vdc + delta;
347     gClaParameters.vRef[kCapBank3] = 0.50f * vdc + delta;
348     gClaParameters.vRef[kCapBank4] = 0.25f * vdc + delta;
349 #elif (PPB_REF_MODE == PPB_REF_SLEW)
350     float fgrid = (gGridFrequencyHz >= 1.0f) ? gGridFrequencyHz : 50.0f;
351     const float tFlip = 0.25f / fgrid;
352     const float slopeNorm = (2.0f * swingRange) / tFlip;
353     const float stepNorm = slopeNorm * gSamplePeriod;
354
355     const float pth2 = pdc * gPthFactor2;
356     const float pth3 = pdc * gPthFactor3;
357     const float pth4 = pdc * gPthFactor4;
358
359     const float target2 = (pdel > pth2) ? (+0.95f * swingRange) : (-swingRange);
360     const float target3 = (pdel > pth3) ? (+swingRange) : (-swingRange);
361     const float target4 = (pdel > pth4) ? (+swingRange) : (-swingRange);
362
363     const float up1 = clampf(gChargeRateC1,  0.0f, 3.0f) * stepNorm;
364     const float up2 = clampf(gChargeRateC2,  0.0f, 3.0f) * stepNorm;
365     const float up3 = clampf(gChargeRateC3,  0.0f, 3.0f) * stepNorm;
366     const float dn1 = clampf(gDischargeRateC1, 0.0f, 3.0f) * stepNorm;
367     const float dn2 = clampf(gDischargeRateC2, 0.0f, 3.0f) * stepNorm;
368     const float dn3 = clampf(gDischargeRateC3, 0.0f, 3.0f) * stepNorm;
369
370     static float d2 = 0.0f;
371     static float d3 = 0.0f;
372     static float d4 = 0.0f;
373
374     const float err2 = target2 - d2;
375     const float err3 = target3 - d3;
376     const float err4 = target4 - d4;
377
378     const float step2 = (err2 >= 0.0f) ? clampf(err2, 0.0f, up1) : -clampf(-err2, 0.0f, dn1);
379     const float step3 = (err3 >= 0.0f) ? clampf(err3, 0.0f, up2) : -clampf(-err3, 0.0f, dn2);
380     const float step4 = (err4 >= 0.0f) ? clampf(err4, 0.0f, up3) : -clampf(-err4, 0.0f, dn3);
381
382     d2 = clampf(d2 + step2, -swingRange, swingRange);
383     d3 = clampf(d3 + step3, -swingRange, swingRange);
384     d4 = clampf(d4 + step4, -swingRange, swingRange);
385
386     gClaParameters.vRef[kCapBank2] = 0.75f * vdc + d2;
387     gClaParameters.vRef[kCapBank3] = 0.50f * vdc + d3;
388     gClaParameters.vRef[kCapBank4] = 0.25f * vdc + d4;
389 #else
390 #error "Unsupported PPB reference mode"
391 #endif
392 }
393
394 //-----------------------------------------------------------------------------
395 // Interrupt service routines
396 //-----------------------------------------------------------------------------
397
398 #pragma INTERRUPT (INT_ADC_ISR, HPI)
399 __interrupt void INT_ADC_ISR(void)
400 {
401     GPIO_writePin(myGPIO_Profile, 1);
402
403     applyOutputs(gGlobalOptimalIndex, (gMpcEnabled != 0U), gSwitchPulsesEnabled);
404     gClaPrevSwitchNibble = gSwitchNibbles[gGlobalOptimalIndex & 0x0FU];
405
406     const float32_t khPenaltyQuarter = gClaParameters.kSwitchPenalty * 0.25f;
```

```
407
408     gAdcRaw[kAdcGridCurrent]   = ADC_readPPBResult(ADCDRESULT_BASE, ADC_D_PPB_IG);
409     gAdcRaw[kAdcCap1Voltage]   = ADC_readResult(ADC_A_RESULT_BASE, ADC_A_ADC_V1);
410     gAdcRaw[kAdcCap2Voltage]   = ADC_readResult(ADC_C_RESULT_BASE, ADC_C_ADC_V2);
411     gAdcRaw[kAdcCap3Voltage]   = ADC_readResult(ADC_B_RESULT_BASE, ADC_B_ADC_V3);
412     gAdcRaw[kAdcCap4Voltage]   = ADC_readPPBResult(ADC_C_RESULT_BASE, ADC_C_PPB_V4);
413     gAdcRaw[kAdcGridVoltage]   = ADC_readPPBResult(ADC_B_RESULT_BASE, ADC_B_PPB_VG);
414     gAdcRaw[kAdcDcLoadCurrent] = ADC_readPPBResult(ADC_A_RESULT_BASE, ADC_A_PPB_IDC);
415     gAdcRaw[kAdcMpcEnable]     = (int16_t)gMpcEnabled;
416
417     gClaMeasurements.iInverter = (float32_t)gAdcRaw[kAdcGridCurrent] * GRID_CURRENT_SCALE;
418     gClaMeasurements.vGrid     = (float32_t)gAdcRaw[kAdcGridVoltage] * GRID_VOLTAGE_SCALE;
419     gClaMeasurements.vCap[kCapBank1] = (float32_t)gAdcRaw[kAdcCap1Voltage] *
        CAP1_VOLTAGE_SCALE;
420     gClaMeasurements.vCap[kCapBank2] = (float32_t)gAdcRaw[kAdcCap2Voltage] *
        CAP2_VOLTAGE_SCALE;
421     gClaMeasurements.vCap[kCapBank3] = (float32_t)gAdcRaw[kAdcCap3Voltage] *
        CAP3_VOLTAGE_SCALE;
422     gClaMeasurements.vCap[kCapBank4] = (float32_t)gAdcRaw[kAdcCap4Voltage] *
        CAP4_VOLTAGE_SCALE;
423     gClaMeasurements.iDc       = (float32_t)gAdcRaw[kAdcDcLoadCurrent] * IDC_CURRENT_SCALE;
424
425     if (gMpcEnabled != 0U)
426     {
427         const float32_t zc = (float32_t)gZeroCrossPolarity;
428         updatePredictionForIndex(gGlobalOptimalIndex & 0x0FU, zc);
429
430         CLA_forceTasks(CLA1_BASE, CLA_TASKFLAG_1);
431
432         gCpuCost = FLT_MAX;
433         gCpuOptimalIndex = 0U;
434
435         for (uint16_t index = 11U; index < 16U; ++index)
436         {
437             const float32_t cost = evaluateCandidate(index, zc, khPenaltyQuarter);
438             if (cost < gCpuCost)
439             {
440                 gCpuCost = cost;
441                 gCpuOptimalIndex = index;
442             }
443         }
444     }
445     else
446     {
447         applyOutputs(0U, false, false);
448     }
449
450     IPC_sendCommand(IPC_CPU1_L_CPU2_R,
451                     IPC_FLAG0,
452                     IPC_ADDR_CORRECTION_ENABLE,
453                     IPC_CMD_READ_MEM,
454                     (uint32_t)gAdcRaw,
455                     (uint32_t)kAdcChannelCount);
456
457     const float32_t iInv = gClaMeasurements.iInverter;
458     const float32_t vc1  = gClaMeasurements.vCap[kCapBank1];
459     const float32_t vc2  = gClaMeasurements.vCap[kCapBank2];
460     const float32_t vc3  = gClaMeasurements.vCap[kCapBank3];
461     const float32_t vc4  = gClaMeasurements.vCap[kCapBank4];
462
463     if ((iInv > IINV_POS_LIMIT) || (iInv < IINV_NEG_LIMIT) ||
464         (vc1 > VC1_POS_LIMIT)  || (vc2 > VC2_POS_LIMIT)    ||
465         (vc3 > VC3_POS_LIMIT)  || (vc4 > VC4_POS_LIMIT))
466     {
467         gMpcEnabled = 0U;
468         applyOutputs(0U, false, false);
```

```
469
470         if (!gFaultLogged)
471         {
472             if (iInv > IINV_POS_LIMIT)
473             {
474                 gProtectionStatus = kProtectionIinvHi;
475                 gFaultMagnitude = iInv;
476             }
477             else if (iInv < IINV_NEG_LIMIT)
478             {
479                 gProtectionStatus = kProtectionIinvLo;
480                 gFaultMagnitude = iInv;
481             }
482             else if (vc1 > VC1_POS_LIMIT)
483             {
484                 gProtectionStatus = kProtectionVc1Hi;
485                 gFaultMagnitude = vc1;
486             }
487             else if (vc2 > VC2_POS_LIMIT)
488             {
489                 gProtectionStatus = kProtectionVc2Hi;
490                 gFaultMagnitude = vc2;
491             }
492             else if (vc3 > VC3_POS_LIMIT)
493             {
494                 gProtectionStatus = kProtectionVc3Hi;
495                 gFaultMagnitude = vc3;
496             }
497             else
498             {
499                 gProtectionStatus = kProtectionVc4Hi;
500                 gFaultMagnitude = vc4;
501             }
502
503             gFaultLogged = true;
504         }
505     }
506
507     updateVoltageReferences();
508
509     IPC_waitForAck(IPC_CPU1_L_CPU2_R, IPC_FLAG0);
510
511     ADC_clearInterruptStatus(ADCB_BASE, ADC_INT_NUMBER1);
512     Interrupt_clearACKGroup(INT_ADC_B_1_INTERRUPT_ACK_GROUP);
513
514     GPIO_writePin(myGPIO_Profile, 0);
515 }
516
517 #pragma INTERRUPT (INT_CLA_ISR, HPI)
518 __interrupt void INT_CLA_ISR(void)
519 {
520     GPIO_writePin(CLAEndProfile, 1);
521
522     const float32_t claCost = gClaResult.gMin;
523     const uint16_t claIndex = gClaResult.optimalIndex;
524
525     if (claCost < gCpuCost)
526     {
527         gGlobalOptimalIndex = claIndex;
528     }
529     else
530     {
531         gGlobalOptimalIndex = gCpuOptimalIndex;
532     }
533
534     Interrupt_clearACKGroup(INT_myCLA01_INTERRUPT_ACK_GROUP);
```

```
535     GPIO_writePin(CLAEndProfile, 0);
536 }
537
538 // IPC handler for CPU2 updates and status exchange.
539 interrupt void ipc1_ISR(void)
540 {
541     GPIO_writePin(myGPIO_Profile_IPC_CPU1, 1);
542
543     Interrupt_clearACKGroup(INTERRUPT_ACK_GROUP1);
544
545     uint32_t cmd, addr, data;
546     IPC_readCommand(IPC_CPU1_L_CPU2_R,
547                     IPC_FLAG1,
548                     IPC_ADDR_CORRECTION_ENABLE,
549                     &cmd,
550                     &addr,
551                     &data);
552
553     const float32_t *payload = (const float32_t *)addr;
554     gClaParameters.iRefPfc = payload[0];
555     gVdcFiltered           = payload[1];
556     const uint16_t zcWord  = (uint16_t)payload[2];
557     gSin2ThetaPi           = payload[3];
558     gIdcFiltered           = payload[4];
559
560     uint16_t zcBlanking = (zcWord >> 1) & 0x1U;
561     uint16_t zcPolarity = zcWord & 0x1U;
562
563     gZeroCrossPolarity = (int16_t)zcPolarity;
564
565     if (zcBlanking != 0U)
566     {
567         gGlobalOptimalIndex = zcPolarity ? 15U : 0U;
568     }
569
570     gSwitchPulsesEnabled = (zcBlanking == 0U);
571
572     if (gClaParameters.iRefPfc > gIrefSatPos)
573     {
574         gClaParameters.iRefPfc = gIrefSatPos;
575     }
576     else if (gClaParameters.iRefPfc < gIrefSatNeg)
577     {
578         gClaParameters.iRefPfc = gIrefSatNeg;
579     }
580
581     IPC_ackFlagRtoL(IPC_CPU1_L_CPU2_R, IPC_FLAG1);
582
583     if (++gLedCounter == 0U)
584     {
585         GPIO_togglePin(DEVICE_GPIO_PIN_LED1);
586     }
587
588     GPIO_writePin(myGPIO_Profile_IPC_CPU1, 0);
589 }
590
591 //-----------------------------------------------------------------------------
592 // Initialisation
593 //-----------------------------------------------------------------------------
594
595 static void initialiseMpcParameters(void)
596 {
597     const float32_t fs = 150e3f;
598     const float32_t vdcNom = 400.0f;
599     const float32_t c1 = 480e-6f;
600     const float32_t c2 = 70e-6f;
```

```
601     const float32_t c3 = 70e-6f;
602     const float32_t c4 = 70e-6f;
603     const float32_t lg = 255e-6f;
604     const float32_t rg = 0.2f;
605
606     gMpcEnabled = 0U;
607
608     gClaParameters.k2 = 0.0172f;
609     gClaParameters.k3 = 0.0209f;
610     gClaParameters.k4 = 0.0269f;
611     gClaParameters.k5 = 1.0f;
612     gClaParameters.kSwitchPenalty = 0.0f;
613     gClaParameters.iRefPfc = 0.0f;
614
615     gClaParameters.vRef[kCapBank2] = 0.75f * vdcNom;
616     gClaParameters.vRef[kCapBank3] = 0.50f * vdcNom;
617     gClaParameters.vRef[kCapBank4] = 0.25f * vdcNom;
618     gClaParameters.vRef[kCapBank1] = vdcNom;
619
620     gSamplePeriod = 1.0f / fs;
621     gClaParameters.tsOverLg = gSamplePeriod / lg;
622     gTsOverLg = gClaParameters.tsOverLg;
623     gOneMinusRgTsOverLg = 1.0f - ((rg * gSamplePeriod) / lg);
624
625     gTsOverC[kCapBank1] = gSamplePeriod / c1;
626     gTsOverC[kCapBank2] = gSamplePeriod / c2;
627     gTsOverC[kCapBank3] = gSamplePeriod / c3;
628     gTsOverC[kCapBank4] = gSamplePeriod / c4;
629
630     for (uint32_t i = 0U; i < kCapBankCount; ++i)
631     {
632         gClaParameters.tsOverC[i] = gTsOverC[i];
633     }
634
635     gFaultLogged = false;
636     gFaultMagnitude = 0.0f;
637     gGlobalOptimalIndex = 0U;
638
639     buildSwitchLookupTables();
640 }
641
642 //-----------------------------------------------------------------------------
643 // Application entry point
644 //-----------------------------------------------------------------------------
645
646 void main(void)
647 {
648     Device_init();
649     Interrupt_initModule();
650     Interrupt_initVectorTable();
651
652     EALLOW;
653     CpuSysRegs.PCLKCR0.bit.TBCLKSYNC = 0;
654     CpuSysRegs.PCLKCR0.bit.GTBCLKSYNC = 0;
655     EDIS;
656
657     SysCtl_selectCPUForPeripheralInstance(SYSCTL_CPUSEL_EPWM7, SYSCTL_CPUSEL_CPU2);
658     SysCtl_selectCPUForPeripheralInstance(SYSCTL_CPUSEL_EPWM8, SYSCTL_CPUSEL_CPU2);
659
660     Board_init();
661     DEVICE_DELAY_US(1000);
662
663     IPC_clearFlagLtoR(IPC_CPU1_L_CPU2_R, IPC_FLAG_ALL);
664     IPC_sync(IPC_CPU1_L_CPU2_R, IPC_SYNC);
665
666     EALLOW;
```

```
    CpuSysRegs.PCLKCR0.bit.TBCLKSYNC = 1;
    CpuSysRegs.PCLKCR0.bit.GTBCLKSYNC = 1;
    EDIS;

    C2000Ware_libraries_init();

    initialiseMpcParameters();

    EINT;
    ERTM;

    for (;;)
    {
        __asm(" NOP");
    }
}

//###########################################################################
// End of file
//###########################################################################
```

Listing I.1: CPU1 firmware implementing the real time PPB MPC and FC reference on F28379D

CPU1–CLA Shared Data Structures

```
//###########################################################################
// FILE:   cpu1_cla_shared.h
// TITLE:  Shared CPU/CLA data structures for MPC implementation
//###########################################################################

#ifndef CPU1_CLA_SHARED_H
#define CPU1_CLA_SHARED_H

#include <stdint.h>
#include <stdbool.h>
#include "driverlib.h"

// Helper enumerations
typedef enum
{
    kCapBank1 = 0U,
    kCapBank2,
    kCapBank3,
    kCapBank4,
    kCapBankCount
} ClaCapacitorBank_e;

// Shared data structures
typedef struct
{
    float32_t vGrid;                    //!< Grid voltage measurement
    float32_t iInverter;                //!< Inverter current measurement
    float32_t iDc;                      //!< DC load current measurement
    float32_t vCap[kCapBankCount];      //!< Capacitor voltages C1..C4
} ClaMpcMeasurements;

typedef struct
{
    float32_t v2Pred;                   //!< Predicted capacitor 2 voltage (k+1)
    float32_t v3Pred;                   //!< Predicted capacitor 3 voltage (k+1)
    float32_t v4Pred;                   //!< Predicted capacitor 4 voltage (k+1)
    float32_t iTemp;                    //!< Intermediate current state
} ClaMpcPrediction;

```

```
typedef struct
{
    float32_t kSwitchPenalty;           //!< KH weighting for switching effort
    float32_t k2;                       //!< Voltage weight for capacitor 2
    float32_t k3;                       //!< Voltage weight for capacitor 3
    float32_t k4;                       //!< Voltage weight for capacitor 4
    float32_t k5;                       //!< Current weight
    float32_t vRef[kCapBankCount];      //!< Reference voltages (E1..E4)
    float32_t tsOverLg;                 //!< Ts/Lg
    float32_t tsOverC[kCapBankCount];   //!< Ts/C1..C4
    float32_t iRefPfc;                  //!< Reference current for the inverter
} ClaMpcParameters;

typedef struct
{
    float32_t gMin;                     //!< Best cost value from CLA search
    uint16_t optimalIndex;              //!< Index of the best candidate
} ClaMpcResult;

// Extern declarations
extern volatile ClaMpcMeasurements gClaMeasurements;
extern volatile ClaMpcPrediction   gClaPrediction;
extern volatile ClaMpcParameters   gClaParameters;
extern volatile ClaMpcResult       gClaResult;
extern volatile uint8_t            gClaPrevSwitchNibble;

extern volatile int16_t gZeroCrossPolarity;

extern const float32_t gSkf[16][4];
extern const uint8_t  gSwitchPopCount[16];
extern uint8_t        gSwitchNibbles[16];

//-----------------------------------------------------------------------------
// CLA task prototypes
//-----------------------------------------------------------------------------

__attribute__((interrupt)) void Cla1Task1(void);

#endif // CPU1_CLA_SHARED_H

//###########################################################################
// End of file
//###########################################################################
```

Listing I.2: Shared data structures and parameters used between CPU1 and CLA1 for PPB MPC execution

CLA1 MPC Task parallel execution

```
//###########################################################################
// FILE: cpu1_cla_tasks.cla
// TITLE: CLA tasks for MPC cost evaluation
//###########################################################################

#include <float.h>

#include "cpu1_cla_shared.h"
#include "driverlib.h"
#include "board.h"

// Local helpers
// Evaluate one MPC candidate using CLA-resident data.
static inline float32_t claEvaluateCandidate(uint16_t index,
                                             float32_t zc,
                                             float32_t khPenaltyQuarter,
```

```
                                        const volatile ClaMpcMeasurements *meas,
                                        const volatile ClaMpcPrediction   *pred,
                                        const volatile ClaMpcParameters   *params,
                                        uint8_t previousNibble)
{
    const float32_t *row = gSkf[index];
    const float32_t sk01 = zc       - row[0];
    const float32_t sk12 = row[0]   - row[1];
    const float32_t sk23 = row[1]   - row[2];
    const float32_t sk34 = row[2]   - row[3];

    const float32_t vc1 = meas->vCap[kCapBank1];
    const float32_t vinv = (sk01 * vc1) +
                           (sk12 * pred->v2Pred) +
                           (sk23 * pred->v3Pred) +
                           (sk34 * pred->v4Pred);

    const float32_t vGrid   = meas->vGrid;
    const float32_t current = meas->iInverter;

    const float32_t isk1 = pred->iTemp +
                           (params->tsOverLg * (vGrid - vinv));

    const float32_t v2k = pred->v2Pred +
                          (params->tsOverC[kCapBank2] * sk12 * current);
    const float32_t v3k = pred->v3Pred +
                          (params->tsOverC[kCapBank3] * sk23 * current);
    const float32_t v4k = pred->v4Pred +
                          (params->tsOverC[kCapBank4] * sk34 * current);

    const float32_t e2 = params->vRef[kCapBank2] - v2k;
    const float32_t e3 = params->vRef[kCapBank3] - v3k;
    const float32_t e4 = params->vRef[kCapBank4] - v4k;
    const float32_t ei = isk1 - params->iRefPfc;

    float32_t cost = (params->k2 * e2 * e2) +
                     (params->k3 * e3 * e3) +
                     (params->k4 * e4 * e4) +
                     (params->k5 * ei * ei);

    const uint8_t diff = gSwitchNibbles[index] ^ previousNibble;
    cost += khPenaltyQuarter * (float32_t)gSwitchPopCount[diff & 0x0FU];

    return cost;
}

// CLA Task 1 - Evaluate MPC candidates
__attribute__((interrupt)) void Cla1Task1(void)
{
    GPIO_writePin(myGPIO_CLAProfile, 1);

    const volatile ClaMpcMeasurements *meas   = &gClaMeasurements;
    const volatile ClaMpcPrediction   *pred   = &gClaPrediction;
    const volatile ClaMpcParameters   *params = &gClaParameters;

    const float32_t zc              = (float32_t)gZeroCrossPolarity;
    const float32_t khPenaltyQuarter = params->kSwitchPenalty * 0.25f;
    const uint8_t  previousNibble    = gClaPrevSwitchNibble;

    float32_t bestCost = FLT_MAX;
    uint16_t bestIndex = 0U;

#pragma UNROLL(11)
    for (uint16_t index = 0U; index < 11U; ++index)
    {
        const float32_t candidateCost = claEvaluateCandidate(index,
```

```
                                                                zc,
                                                                khPenaltyQuarter,
                                                                meas,
                                                                pred,
                                                                params,
                                                                previousNibble);
        if (candidateCost < bestCost)
        {
            bestCost = candidateCost;
            bestIndex = index;
        }
    }

    gClaResult.gMin        = bestCost;
    gClaResult.optimalIndex = bestIndex;

    GPIO_writePin(myGPIO_CLAProfile, 0);
}

//###########################################################################
// End of file
//###########################################################################
```

Listing I.3: CLA1 task code implementing partial candidate evaluation for the PPB MPC algorithm

CPU2 Voltage loop and instrumentation firmware

```
// FILE: main_cpu2.c
//
// TITLE: MPC PFC CPU 2 Tasks
//
// CPU2 manages the voltage regulation loop, grid synchronization PLL, and
// instrumentation while sharing measurements and references with CPU1.
// This file provides the control ISRs and helper routines used by CPU2.

#include "driverlib.h"
#include "device.h"
#include "board.h"
#include <math.h>
#include <stddef.h>
#include <stdint.h>
#include "DCLF32.h"
#include "f2837xd_device.h"
#include "power_meas_sine_analyzer.h"
#include "spll_1ph_sogi.h"

#pragma FUNC_ALWAYS_INLINE(POWER_MEAS_SINE_ANALYZER_run)

//=============================================================================
// Configuration constants
//=============================================================================
#define IPC_CMD_READ_MEM 0x1001
#define IPC_CMD_RESP     0x2001

#define ADC_GRID_VOLTAGE_IDX   0
#define ADC_GRID_CURRENT_IDX   1
#define ADC_CAP1_VOLTAGE_IDX   2
#define ADC_CAP2_VOLTAGE_IDX   3
#define ADC_CAP3_VOLTAGE_IDX   4
#define ADC_CAP4_VOLTAGE_IDX   5
#define ADC_DCLOAD_CURRENT_IDX 6
#define MPCEnabled_IDX         7

#define ADC_NUM_CHANNELS 8
```

```
38
39 #define PI_VALUE ((float32_t)3.141592653589)
40
41 // Controller output limits
42 #define FCMLPFC_GV_PI_MAX ((float32_t)0.1)
43 #define FCMLPFC_GV_PI_MIN ((float32_t)-0.02)
44
45 // Controller parameters
46 #define FCMLPFC_GV_PI_KP ((float32_t)1.093)
47 #define FCMLPFC_GV_PI_KI ((float32_t)0.0006868)
48
49 // Run frequencies
50 #define FCMLPFC_CONTROL_ISR_FREQUENCY         ((float32_t)100 * 1000)
51 #define FCMLPFC_INSTRUMENTATION_ISR_FREQUENCY 10000
52 #define FCMLPFC_AC_FREQ                       60
53
54 #define GRID_MAX_FREQ 70
55 #define GRID_MIN_FREQ 40
56
57 // ADC scale factors (CPU2)
58 #define FCMLPFC_ADC_PU_SCALE_FACTOR     (float32_t)(0.000244140625)
59 #define FCMLPFC_ADC_PU_PPB_SCALE_FACTOR (float32_t)(0.000488281250)
60 #define FCMLPFC_ADC_PU_IDC_SCALE_FACTOR (float32_t)(0.000250941028)
61
62 // Sensor scaling factors
63 #define FCMLPFC_VAC_MAX_SENSE_VOLT  (float32_t)677.67
64 #define FCMLPFC_VDCBUS_MAX_SENSE_VOLT (float32_t)681.8181
65 #define FCMLPFC_IL_MAX_SENSE_AMPS   (float32_t)19.49284
66 #define FCMLPFC_IDC_MAX_SENSE_AMPS  (float32_t)19.50
67
68 #define IDC_CURRENT_SCALE 0.004897891f
69
70 // Reference compensation
71 #define FCMLPFC_INPUT_CAP_COMPENSATION           0
72 #define FCMLPFC_HIGH_LINE_INPUT_CAP_COMP_ADJUST ((float32_t)-0.006)
73 #define FCMLPFC_LOW_LINE_INPUT_CAP_COMP_ADJUST  ((float32_t)-0.003)
74
75 // Nonlinear Kp adjustment
76 #define FCMLPFC_NON_LINEAR_VOLTAGE_LOOP          0
77 #define FCMLPFC_NON_LINEAR_V_LOOP_KP_MULTIPLIER ((float32_t)5.0)
78
79 // Control blocks
80 #define FCMLPFC_GV         DCL_PI
81 #define GV_RUN             DCL_runPI_C4
82 #define FCMLPFC_NOTCH_2P2Z DCL_DF22
83 #define NOTCH_2P2Z_RUN     DCL_runDF22_C1
84
85 #define EMAVG_MACRO(in, out, multiplier) out = ((in - out) * multiplier) + out
86
87 //=============================================================================
88 // Local function prototypes
89 //=============================================================================
90 static void FCMLPFC_globalVariablesInit(void);
91 static void computeNotchFltrCoeff(DCL_DF22 *coeff, float32_t Fs,
92                                   float32_t notch_freq, float32_t c1,
93                                   float32_t c2);
94 static inline void FCMLPFC_read_acReturnCurrent(void);
95 static inline void FCMLPFC_read_acVoltage(void);
96 static inline void FCMLPFC_read_busVoltage(void);
97 static inline void FCMLPFC_read_busCurrent(void);
98 static inline void FCMLPFC_acCurrentRef(void);
99 static inline void FCMLPFC_runVoltageLoop(void);
100 static inline void FCMLPFC_SPLL(void);
101 static inline void FCMLPFC_instrumentation(void);
102 static inline void FCMLPFC_runISR2(void);
103 static inline void FCMLPFC_runISR1(void);
```

```
__interrupt void ipc0_ISR(void);
__interrupt void INT_CPU2_EPWM100KHZ_ISR(void);
__interrupt void INT_CPU2_EPWM10KHZ_ISR(void);

//=============================================================================
// Global variables
//=============================================================================
// PI regulator state
volatile FCMLPFC_GV FCMLPFC_gv;

// PLL and notch filters
SPLL_1PH_SOGI FCMLPFC_spll1;
FCMLPFC_NOTCH_2P2Z FCMLPFC_notch1, FCMLPFC_notch2;
FCMLPFC_NOTCH_2P2Z FCMLPFC_notch3, FCMLPFC_notch4;

// Sine analyzer for RMS, current, and power
volatile POWER_MEAS_SINE_ANALYZER FCMLPFC_sine_mains;

volatile int16_t FCMLPFC_initializationFlag;

// Display values
volatile float32_t FCMLPFC_guiVbus_Volts;
float32_t FCMLPFC_guiVbusMax_Volts;
volatile float32_t FCMLPFC_guiVrms_Volts;
float32_t FCMLPFC_guiPrms_W;
float32_t FCMLPFC_guiIrms_Amps;
float32_t FCMLPFC_guiVavg_Volts;
float32_t FCMLPFC_guiFreqAvg_Hz;
float32_t FCMLPFC_guiVema_Volts;
float32_t FCMLPFC_ac_volRmsEma_sensed_Volts;
float32_t FCMLPFC_guiVin_Volts;
float32_t FCMLPFC_guiIL_Amps;
float32_t FCMLPFC_guiPowerFactor;
float32_t FCMLPFC_guiVA_VA;

// Control variables
volatile float32_t FCMLPFC_ac_cur_sensed_pu;
volatile float32_t FCMLPFC_ac_cur_ref_pu;
float32_t FCMLPFC_ac_cur_ref_inst_pu;
float32_t FCMLPFC_ac_cur_ref_inst_Amps;

volatile float32_t FCMLPFC_vBus_sensed_pu;
float32_t FCMLPFC_vBusRef_pu;
float32_t FCMLPFC_vBus_sensedFiltered_notch1;
float32_t FCMLPFC_vBus_sensedFiltered_notch2;

volatile float32_t FCMLPFC_iBus_sensed_pu;
volatile float32_t FCMLPFC_iBus_filtered_Amps;
float32_t FCMLPFC_iBus_sensedFiltered_notch1;
float32_t FCMLPFC_iBus_sensedFiltered_notch2;
float32_t FCMLPFC_FeedforwardGainIDC;

volatile float32_t FCMLPFC_ac_vol_sensed_pu;
volatile float32_t FCMLPFC_thetaOffset_pu;

int32_t FCMLPFC_voltageLoopEnabled;
int32_t FCMLPFC_firstVoltageLoopPass;

volatile float32_t FCMLPFC_acSine;
float32_t FCMLPFC_acSine_Prev;
uint32_t FCMLPFC_nonLinearVoltageLoopFlag;

float32_t FCMLPFC_vBusAvg_pu;
float32_t FCMLPFC_vACRmsMeasAvg_pu;
float32_t FCMLPFC_vBusRefSlewed_pu;
float32_t FCMLPFC_vBusError_pu;
```

```
float32_t FCMLPFC_vBusMeasFiltered_pu;
float32_t FCMLPFC_iBusMeasFiltered_pu;

volatile float32_t FCMLPFC_VBUS_reference;
volatile uint16_t FCMLPFC_refMode = 0;
volatile float32_t FCMLPFC_manualVbusRef = 0.0f;

float32_t FCMLPFC_gv_out;
volatile float32_t FCMLPFC_vBusMeasBuff_pu[10];
volatile float32_t FCMLPFC_iBusMeasBuff_pu[10];
volatile int32_t FCMLPFC_vBusMeasBuffIndex = 0;
volatile int32_t FCMLPFC_iBusMeasBuffIndex = 0;

float32_t FCMLPFC_spll_sine, FCMLPFC_spll_cosine;
int32_t FCMLPFC_ac_sign_filtered;

// IPC data sharing
uint16_t LedCtr2 = 0;
volatile int16_t receivedADC[ADC_NUM_CHANNELS];
volatile uint8_t MPCDisabledCPU2 = 0;

#pragma DATA_SECTION(sharedFloatArray, "MSGRAM_CPU2_TO_CPU1")
volatile float32_t sharedFloatArray[5];

//=============================================================================
// Helper functions
//=============================================================================
/* Initialize controller coefficients, filters, and GUI variables. */
static void FCMLPFC_globalVariablesInit(void)
{
    FCMLPFC_gv.Ki = FCMLPFC_GV_PI_KI;
    FCMLPFC_gv.Kp = FCMLPFC_GV_PI_KP;
    FCMLPFC_gv.Umax = FCMLPFC_GV_PI_MAX;
    FCMLPFC_gv.Umin = FCMLPFC_GV_PI_MIN;
    FCMLPFC_gv.i10 = 0;
    FCMLPFC_gv.i6 = 0;

    SPLL_1PH_SOGI_reset(&FCMLPFC_spll1);
    SPLL_1PH_SOGI_config(&FCMLPFC_spll1, FCMLPFC_AC_FREQ,
                         FCMLPFC_CONTROL_ISR_FREQUENCY,
                         (float32_t)(222.2862), (float32_t)(-222.034));

    POWER_MEAS_SINE_ANALYZER_reset(&FCMLPFC_sine_mains);
    POWER_MEAS_SINE_ANALYZER_config(&FCMLPFC_sine_mains,
                                    FCMLPFC_INSTRUMENTATION_ISR_FREQUENCY,
                                    (float32_t)0.01, (float32_t)GRID_MAX_FREQ,
                                    (float32_t)GRID_MIN_FREQ);

    computeNotchFltrCoeff(&FCMLPFC_notch1,
                          (float32_t)(FCMLPFC_INSTRUMENTATION_ISR_FREQUENCY),
                          (float32_t)(FCMLPFC_AC_FREQ * 2.0f), 0.25f, 0.00001f);
    computeNotchFltrCoeff(&FCMLPFC_notch2,
                          (float32_t)(FCMLPFC_INSTRUMENTATION_ISR_FREQUENCY),
                          (float32_t)(FCMLPFC_AC_FREQ * 2.0f), 0.25f, 0.00001f);
    FCMLPFC_notch1.x1 = 0;
    FCMLPFC_notch1.x2 = 0;
    FCMLPFC_notch2.x1 = 0;
    FCMLPFC_notch2.x2 = 0;

    computeNotchFltrCoeff(&FCMLPFC_notch3,
                          (float32_t)(FCMLPFC_INSTRUMENTATION_ISR_FREQUENCY),
                          (float32_t)(FCMLPFC_AC_FREQ * 2.0f), 0.25f, 0.00001f);
    computeNotchFltrCoeff(&FCMLPFC_notch4,
                          (float32_t)(FCMLPFC_INSTRUMENTATION_ISR_FREQUENCY),
                          (float32_t)(FCMLPFC_AC_FREQ * 2.0f), 0.25f, 0.00001f);
    FCMLPFC_notch3.x1 = 0;
```

```
236     FCMLPFC_notch3.x2 = 0;
237     FCMLPFC_notch4.x1 = 0;
238     FCMLPFC_notch4.x2 = 0;
239
240     FCMLPFC_guiVbus_Volts = 0;
241     FCMLPFC_guiPrms_W = 0;
242     FCMLPFC_guiIrms_Amps = 0;
243     FCMLPFC_guiVrms_Volts = 0;
244     FCMLPFC_guiVavg_Volts = 0;
245     FCMLPFC_guiFreqAvg_Hz = 0;
246     FCMLPFC_guiVema_Volts = 0;
247     FCMLPFC_guiVbusMax_Volts = 440;
248     FCMLPFC_ac_volRmsEma_sensed_Volts = 0;
249     FCMLPFC_guiVin_Volts = 0;
250
251     FCMLPFC_ac_cur_sensed_pu = 0;
252     FCMLPFC_VBUS_reference = 0.0f;
253     FCMLPFC_vBus_sensed_pu = 0;
254     FCMLPFC_vBusRef_pu = 0;
255     FCMLPFC_vBus_sensedFiltered_notch1 = 0;
256     FCMLPFC_vBus_sensedFiltered_notch2 = 0;
257     FCMLPFC_ac_cur_ref_pu = 0.03f;
258     FCMLPFC_thetaOffset_pu = 0;
259     FCMLPFC_voltageLoopEnabled = 0;
260     FCMLPFC_firstVoltageLoopPass = 1;
261     FCMLPFC_acSine = 0;
262     FCMLPFC_acSine_Prev = 0;
263     FCMLPFC_nonLinearVoltageLoopFlag = 0;
264     FCMLPFC_vACRmsMeasAvg_pu = 0;
265     FCMLPFC_vBusAvg_pu = 0;
266
267     FCMLPFC_FeedforwardGainIDC = (1.41421356237f / 0.96f)
268             * (FCMLPFC_VDCBUS_MAX_SENSE_VOLT / FCMLPFC_VAC_MAX_SENSE_VOLT)
269             * (FCMLPFC_IDC_MAX_SENSE_AMPS / FCMLPFC_IL_MAX_SENSE_AMPS);
270 }
271
272 /* Compute coefficients for a 2P2Z notch filter. */
273 static void computeNotchFltrCoeff(DCL_DF22 *coeff, float32_t Fs,
274                                   float32_t notch_freq, float32_t c1,
275                                   float32_t c2)
276 {
277     float32_t temp1;
278     float32_t temp2;
279     float32_t wn2;
280     float32_t Ts = 1 / Fs;
281
282     wn2 = 2 * Fs * tanf(notch_freq * PI_VALUE * Ts);
283
284     temp1 = 4 * Fs * Fs + 4 * wn2 * c2 * Fs + wn2 * wn2;
285     temp2 = 1 / (4 * Fs * Fs + 4 * wn2 * c1 * Fs + wn2 * wn2);
286
287     coeff->b0 = temp1 * temp2;
288     coeff->b1 = (-8 * Fs * Fs + 2 * wn2 * wn2) * temp2;
289     coeff->b2 = (4 * Fs * Fs - 4 * wn2 * c2 * Fs + wn2 * wn2) * temp2;
290     coeff->a1 = (-8 * Fs * Fs + 2 * wn2 * wn2) * temp2;
291     coeff->a2 = (4 * Fs * Fs - 4 * wn2 * c1 * Fs + wn2 * wn2) * temp2;
292 }
293
294 #pragma FUNC_ALWAYS_INLINE(FCMLPFC_read_acReturnCurrent)
295 static inline void FCMLPFC_read_acReturnCurrent(void)
296 {
297     FCMLPFC_ac_cur_sensed_pu = (float32_t)receivedADC[ADC_GRID_CURRENT_IDX]
298             * FCMLPFC_ADC_PU_PPB_SCALE_FACTOR;
299 }
300
301 #pragma FUNC_ALWAYS_INLINE(FCMLPFC_read_acVoltage)
```

```
302 static inline void FCMLPFC_read_acVoltage(void)
303 {
304     FCMLPFC_ac_vol_sensed_pu = (float32_t)receivedADC[ADC_GRID_VOLTAGE_IDX]
305             * FCMLPFC_ADC_PU_PPB_SCALE_FACTOR;
306 }
307
308 #pragma FUNC_ALWAYS_INLINE(FCMLPFC_read_busVoltage)
309 static inline void FCMLPFC_read_busVoltage(void)
310 {
311     FCMLPFC_vBus_sensed_pu = (float32_t)receivedADC[ADC_CAP1_VOLTAGE_IDX]
312             * FCMLPFC_ADC_PU_SCALE_FACTOR;
313 }
314
315 #pragma FUNC_ALWAYS_INLINE(FCMLPFC_read_busCurrent)
316 static inline void FCMLPFC_read_busCurrent(void)
317 {
318     FCMLPFC_iBus_sensed_pu = (float32_t)receivedADC[ADC_DCLOAD_CURRENT_IDX]
319             * FCMLPFC_ADC_PU_IDC_SCALE_FACTOR;
320 }
321
322 /* Generate the instantaneous AC current reference based on PLL phase. */
323 #pragma FUNC_ALWAYS_INLINE(FCMLPFC_acCurrentRef)
324 static inline void FCMLPFC_acCurrentRef(void)
325 {
326 #if FCMLPFC_INPUT_CAP_COMPENSATION == 1
327     FCMLPFC_ac_cur_ref_inst_pu = FCMLPFC_ac_cur_ref_pu * FCMLPFC_spll_sine
328             + FCMLPFC_thetaOffset_pu * FCMLPFC_spll_cosine;
329 #else
330     FCMLPFC_ac_cur_ref_inst_pu = FCMLPFC_ac_cur_ref_pu * FCMLPFC_spll1.sine;
331 #endif
332
333     FCMLPFC_ac_cur_ref_inst_Amps = FCMLPFC_ac_cur_ref_inst_pu
334             * FCMLPFC_IL_MAX_SENSE_AMPS;
335
336     sharedFloatArray[0] = FCMLPFC_ac_cur_ref_inst_Amps;
337     sharedFloatArray[1] = FCMLPFC_guiVbus_Volts;
338     sharedFloatArray[2] = (float32_t)FCMLPFC_ac_sign_filtered;
339     sharedFloatArray[3] = -2.0f * FCMLPFC_spll_sine * FCMLPFC_spll_cosine;
340     sharedFloatArray[4] = FCMLPFC_iBus_filtered_Amps;
341
342     IPC_sendCommand(IPC_CPU2_L_CPU1_R, IPC_FLAG1, IPC_ADDR_CORRECTION_ENABLE,
343                     0, (uint32_t)sharedFloatArray, 5);
344 }
345
346 /* Closed-loop DC bus voltage regulator executed in the 10 kHz ISR. */
347 #pragma FUNC_ALWAYS_INLINE(FCMLPFC_runVoltageLoop)
348 static inline void FCMLPFC_runVoltageLoop(void)
349 {
350     if (FCMLPFC_voltageLoopEnabled == 1) {
351         if (fabsf(FCMLPFC_vBusRef_pu - FCMLPFC_vBusRefSlewed_pu) > 0.0001f) {
352             if (FCMLPFC_vBusRef_pu > FCMLPFC_vBusRefSlewed_pu) {
353                 FCMLPFC_vBusRefSlewed_pu += 0.0001f;
354             } else {
355                 FCMLPFC_vBusRefSlewed_pu -= 0.0001f;
356             }
357         } else {
358             FCMLPFC_vBusRefSlewed_pu = FCMLPFC_vBusRef_pu;
359         }
360
361 #if FCMLPFC_NON_LINEAR_VOLTAGE_LOOP == 1
362         FCMLPFC_nonLinearVoltageLoopFlag = 1;
363 #else
364         FCMLPFC_nonLinearVoltageLoopFlag = 0;
365 #endif
366     }
367
```

```
368     if (FCMLPFC_voltageLoopEnabled == 1) {
369         if (FCMLPFC_firstVoltageLoopPass == 1) {
370             FCMLPFC_vBusRefSlewed_pu = FCMLPFC_vBus_sensed_pu;
371             FCMLPFC_firstVoltageLoopPass = 0;
372         }
373 
374         FCMLPFC_vBusError_pu = fabsf(FCMLPFC_vBusRefSlewed_pu
375                                      - FCMLPFC_vBus_sensedFiltered_notch2);
376 
377         if (FCMLPFC_nonLinearVoltageLoopFlag == 0) {
378             FCMLPFC_gv.Kp = FCMLPFC_GV_PI_KP;
379             FCMLPFC_gv.Ki = FCMLPFC_GV_PI_KI;
380         } else {
381             if (FCMLPFC_vBusError_pu > 0.005f) {
382                 if (FCMLPFC_gv.Kp < (FCMLPFC_NON_LINEAR_V_LOOP_KP_MULTIPLIER
383                                      * FCMLPFC_GV_PI_KP)) {
384                     FCMLPFC_gv.Kp += 0.05f;
385                 }
386             } else if (FCMLPFC_vBusError_pu < 0.001f) {
387                 if (FCMLPFC_gv.Kp > FCMLPFC_GV_PI_KP) {
388                     FCMLPFC_gv.Kp -= 0.05f;
389                 }
390             }
391         }
392 
393         FCMLPFC_gv_out = GV_RUN((DCL_PI *)&FCMLPFC_gv,
394                                 FCMLPFC_vBusRefSlewed_pu,
395                                 FCMLPFC_vBus_sensedFiltered_notch2);
396 
397         float32_t feedforwardTerm = FCMLPFC_FeedforwardGainIDC
398                 * FCMLPFC_iBus_sensedFiltered_notch2;
399 
400         FCMLPFC_ac_cur_ref_pu = (FCMLPFC_gv_out + feedforwardTerm)
401                 * FCMLPFC_vBusAvg_pu / (FCMLPFC_vACRmsMeasAvg_pu);
402     }
403 }
404 
405 /* PLL processing and polarity detection executed in the 100 kHz ISR. */
406 #pragma FUNC_ALWAYS_INLINE(FCMLPFC_SPLL)
407 static inline void FCMLPFC_SPLL(void)
408 {
409     uint16_t polarity;
410     uint16_t blanking;
411     static uint16_t prevPol = 1;
412 
413     SPLL_1PH_SOGI_run(&FCMLPFC_spll1, FCMLPFC_ac_vol_sensed_pu);
414     FCMLPFC_spll_sine = FCMLPFC_spll1.sine;
415     FCMLPFC_spll_cosine = FCMLPFC_spll1.cosine;
416 
417     if ((fabsf(FCMLPFC_spll1.ylf[0]) > 2.0f) || MPCDisabledCPU2) {
418         GpioDataRegs.GPACLEAR.bit.GPIO8 = 1;
419         GpioDataRegs.GPACLEAR.bit.GPIO9 = 1;
420     } else {
421         if (FCMLPFC_spll1.sine > 0.0523359f) {
422             GpioDataRegs.GPASET.bit.GPIO8 = 1;
423             GpioDataRegs.GPACLEAR.bit.GPIO9 = 1;
424             polarity = 1;
425             blanking = 0;
426             prevPol = 1;
427         } else if (FCMLPFC_spll1.sine < 0.0f) {
428             GpioDataRegs.GPACLEAR.bit.GPIO8 = 1;
429             GpioDataRegs.GPASET.bit.GPIO9 = 1;
430             polarity = 0;
431             blanking = 0;
432             prevPol = 0;
433         } else {
```

```
434             GpioDataRegs.GPACLEAR.bit.GPIO8 = 1;
435             GpioDataRegs.GPACLEAR.bit.GPIO9 = 1;
436             polarity = prevPol ^ 1;
437             blanking = 1;
438         }
439     }
440
441     FCMLPFC_ac_sign_filtered = (blanking << 1) | polarity;
442
443     FCMLPFC_acSine_Prev = FCMLPFC_acSine;
444     FCMLPFC_acSine = FCMLPFC_spll_sine;
445 }
446
447 /* RMS, frequency, and power instrumentation executed in the 10 kHz ISR. */
448 #pragma FUNC_ALWAYS_INLINE(FCMLPFC_instrumentation)
449 static inline void FCMLPFC_instrumentation(void)
450 {
451     FCMLPFC_sine_mains.i = FCMLPFC_ac_cur_sensed_pu;
452     FCMLPFC_sine_mains.v = FCMLPFC_ac_vol_sensed_pu;
453     POWER_MEAS_SINE_ANALYZER_run(&FCMLPFC_sine_mains);
454     FCMLPFC_guiIrms_Amps = FCMLPFC_sine_mains.iRms * FCMLPFC_IL_MAX_SENSE_AMPS;
455     FCMLPFC_guiVrms_Volts = FCMLPFC_sine_mains.vRms * FCMLPFC_VAC_MAX_SENSE_VOLT;
456     FCMLPFC_guiPrms_W = FCMLPFC_sine_mains.pRms * FCMLPFC_VAC_MAX_SENSE_VOLT
457             * FCMLPFC_IL_MAX_SENSE_AMPS;
458     FCMLPFC_guiPowerFactor = FCMLPFC_sine_mains.powerFactor;
459     FCMLPFC_guiVA_VA = FCMLPFC_sine_mains.vaRms * FCMLPFC_VAC_MAX_SENSE_VOLT
460             * FCMLPFC_IL_MAX_SENSE_AMPS;
461     FCMLPFC_guiFreqAvg_Hz = FCMLPFC_sine_mains.acFreqAvg;
462     EMAVG_MACRO(FCMLPFC_sine_mains.vRms, FCMLPFC_vACRmsMeasAvg_pu,
463                 (float32_t)0.000528);
464 }
465
466 //=============================================================================
467 // Interrupt service routines
468 //=============================================================================
469 /* 10 kHz ISR: voltage loop, instrumentation, and reference management. */
470 #pragma FUNC_ALWAYS_INLINE(FCMLPFC_runISR2)
471 static inline void FCMLPFC_runISR2(void)
472 {
473     int32_t vBusSensedBuffIndex1;
474     int32_t iBusSensedBuffIndex1;
475
476     FCMLPFC_vBusMeasFiltered_pu = 0;
477     for (vBusSensedBuffIndex1 = 0; vBusSensedBuffIndex1 < 10;
478          vBusSensedBuffIndex1++) {
479         FCMLPFC_vBusMeasFiltered_pu += FCMLPFC_vBusMeasBuff_pu[vBusSensedBuffIndex1];
480     }
481     FCMLPFC_vBusMeasFiltered_pu *= 0.1f;
482     FCMLPFC_vBus_sensedFiltered_notch1 = NOTCH_2P2Z_RUN(&FCMLPFC_notch1,
483             FCMLPFC_vBusMeasFiltered_pu);
484     FCMLPFC_vBus_sensedFiltered_notch2 = NOTCH_2P2Z_RUN(&FCMLPFC_notch2,
485             FCMLPFC_vBus_sensedFiltered_notch1);
486
487     FCMLPFC_iBusMeasFiltered_pu = 0.0f;
488     for (iBusSensedBuffIndex1 = 0; iBusSensedBuffIndex1 < 10;
489          iBusSensedBuffIndex1++) {
490         FCMLPFC_iBusMeasFiltered_pu += FCMLPFC_iBusMeasBuff_pu[iBusSensedBuffIndex1];
491     }
492     FCMLPFC_iBusMeasFiltered_pu *= 0.1f;
493     FCMLPFC_iBus_sensedFiltered_notch1 = NOTCH_2P2Z_RUN(&FCMLPFC_notch3,
494             FCMLPFC_iBusMeasFiltered_pu);
495     FCMLPFC_iBus_sensedFiltered_notch2 = NOTCH_2P2Z_RUN(&FCMLPFC_notch4,
496             FCMLPFC_iBus_sensedFiltered_notch1);
497
498     FCMLPFC_runVoltageLoop();
499
```

```
500     EMAVG_MACRO(FCMLPFC_vBus_sensedFiltered_notch2, FCMLPFC_vBusAvg_pu,
501                 (float32_t)0.000528);
502     EMAVG_MACRO((fabsf(FCMLPFC_ac_vol_sensed_pu) * FCMLPFC_VAC_MAX_SENSE_VOLT),
503                 FCMLPFC_ac_volRmsEma_sensed_Volts, (float32_t)0.00005);
504
505     FCMLPFC_guiVbus_Volts = FCMLPFC_vBus_sensedFiltered_notch2
506             * FCMLPFC_VDCBUS_MAX_SENSE_VOLT;
507     FCMLPFC_guiVin_Volts = FCMLPFC_ac_vol_sensed_pu * FCMLPFC_VAC_MAX_SENSE_VOLT;
508     FCMLPFC_guiIL_Amps = FCMLPFC_ac_cur_sensed_pu * FCMLPFC_IL_MAX_SENSE_AMPS;
509
510     FCMLPFC_instrumentation();
511
512     static uint16_t prevRefMode = 0;
513     if (FCMLPFC_refMode == 0) {
514         FCMLPFC_VBUS_reference = 1.81f * FCMLPFC_guiVrms_Volts;
515         if (FCMLPFC_VBUS_reference > 403.0f) {
516             FCMLPFC_VBUS_reference = 403.0f;
517         }
518     } else {
519         if (prevRefMode == 0) {
520             FCMLPFC_manualVbusRef = FCMLPFC_VBUS_reference;
521         }
522         FCMLPFC_VBUS_reference = FCMLPFC_manualVbusRef;
523     }
524
525     FCMLPFC_vBusRef_pu = FCMLPFC_VBUS_reference / FCMLPFC_VDCBUS_MAX_SENSE_VOLT;
526     prevRefMode = FCMLPFC_refMode;
527 }
528
529 /* 100 kHz ISR: PLL update, measurement acquisition, and current reference. */
530 #pragma FUNC_ALWAYS_INLINE(FCMLPFC_runISR1)
531 static inline void FCMLPFC_runISR1(void)
532 {
533     FCMLPFC_read_acReturnCurrent();
534     FCMLPFC_read_acVoltage();
535
536     FCMLPFC_SPLL();
537     FCMLPFC_acCurrentRef();
538
539     FCMLPFC_read_busVoltage();
540     FCMLPFC_vBusMeasBuff_pu[FCMLPFC_vBusMeasBuffIndex++] = FCMLPFC_vBus_sensed_pu;
541     if (FCMLPFC_vBusMeasBuffIndex >= 10) {
542         FCMLPFC_vBusMeasBuffIndex = 0;
543     }
544
545     FCMLPFC_read_busCurrent();
546     FCMLPFC_iBusMeasBuff_pu[FCMLPFC_iBusMeasBuffIndex++] = FCMLPFC_iBus_sensed_pu;
547     if (FCMLPFC_iBusMeasBuffIndex >= 10) {
548         FCMLPFC_iBusMeasBuffIndex = 0;
549     }
550
551     EPWM_clearEventTriggerInterruptFlag(EPWM8_BASE);
552 }
553
554 /* IPC interrupt: receive ADC samples from CPU1 and toggle the heartbeat LED. */
555 __interrupt void ipc0_ISR(void)
556 {
557     GPIO_writePin(myGPIO_Profile_IPC_CPU2, 1);
558
559     int i;
560     uint32_t command, addr, data;
561
562     Interrupt_clearACKGroup(INTERRUPT_ACK_GROUP1);
563
564     IPC_readCommand(IPC_CPU2_L_CPU1_R, IPC_FLAG0, IPC_ADDR_CORRECTION_ENABLE,
565                     &command, &addr, &data);
```

```
566
567     if (command == IPC_CMD_READ_MEM) {
568         for (i = 0; i < ADC_NUM_CHANNELS; i++) {
569             receivedADC[i] = *((int16_t *)addr + i);
570         }
571     }
572
573     MPCDisabledCPU2 = !((uint8_t)receivedADC[MPCEnabled_IDX]);
574
575     IPC_ackFlagRtoL(IPC_CPU2_L_CPU1_R, IPC_FLAG0);
576
577     if (LedCtr2++ >= 50000) {
578         GPIO_togglePin(CPU2_LED);
579         LedCtr2 = 0;
580     }
581
582     GPIO_writePin(myGPIO_Profile_IPC_CPU2, 0);
583 }
584
585 __interrupt void INT_CPU2_EPWM100KHZ_ISR(void)
586 {
587     GPIO_writePin(myGPIO_Profile_PLL_CPU2, 1);
588     EPWM_clearEventTriggerInterruptFlag(CPU2_EPWM100KHZ_BASE);
589     FCMLPFC_runISR1();
590     Interrupt_clearACKGroup(INTERRUPT_ACK_GROUP3);
591     GPIO_writePin(myGPIO_Profile_PLL_CPU2, 0);
592 }
593
594 __interrupt void INT_CPU2_EPWM10KHZ_ISR(void)
595 {
596     GPIO_writePin(myGPIO_Profile_VMC_CPU2, 1);
597     EPWM_clearEventTriggerInterruptFlag(CPU2_EPWM10KHZ_BASE);
598     FCMLPFC_runISR2();
599     Interrupt_clearACKGroup(INTERRUPT_ACK_GROUP3);
600     GPIO_writePin(myGPIO_Profile_VMC_CPU2, 0);
601 }
602
603 //===========================================================================
604 // Application entry point
605 //===========================================================================
606 int main(void)
607 {
608     Device_init();
609     Interrupt_initModule();
610     Interrupt_initVectorTable();
611
612     EALLOW;
613     CpuSysRegs.PCLKCR0.bit.TBCLKSYNC = 0;
614     EDIS;
615
616     Board_init();
617     IPC_clearFlagLtoR(IPC_CPU2_L_CPU1_R, IPC_FLAG_ALL);
618
619     FCMLPFC_globalVariablesInit();
620
621     EINT;
622     ERTM;
623
624     EALLOW;
625     CpuSysRegs.PCLKCR0.bit.TBCLKSYNC = 1;
626     EDIS;
627
628     IPC_sync(IPC_CPU2_L_CPU1_R, IPC_SYNC);
629
630     for (;;) {
631         NOP;
```

```
632         }
633 }
```

Listing I.4: CPU2 firmware implementing voltage regulation control, PLL, and instrumentation tasks on F28379D

APPENDIX II

REAL-TIME IMPLEMENTATION OF TOTEM-POLE 5L-FCML CONTROL SCHEME - CHAPTER 2

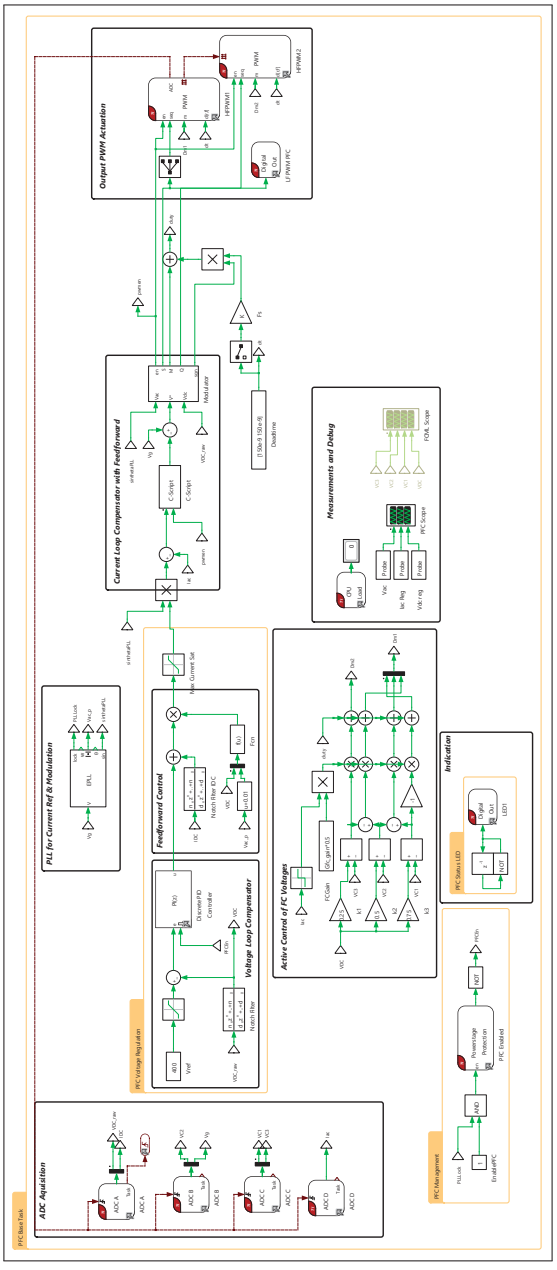


Figure-A II-1 PLECS Coder based digital implementation model of the TP-5L-FCML PFC controller, showing task partitioning (ADC acquisition, PLL and feedforward, current and voltage loop compensators, active flying-capacitor control, and PWM actuation) used for model-based C-code generation and deployment to the TMS320F28379D.

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