New Circuits for Time-Domain Signal Processing in Low-Voltage CMOS

by

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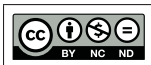
THESIS PRESENTED TO ÉCOLE DE TECHNOLOGIE SUPÉRIEURE
IN PARTIAL FULFILLMENT FOR THE DEGREE OF
DOCTOR OF PHILOSOPHY
Ph.D.

MONTREAL, "NOVEMBER 1, 2018"

ÉCOLE DE TECHNOLOGIE SUPÉRIEURE
UNIVERSITÉ DU QUÉBEC



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ACKNOWLEDGEMENTS

First and foremost, I would like to express my deepest gratitude and respect to my supervisor, Professor Ghyslain Gagnon, for his never ending guidance, encouragement, and support both on a professional level and a personal level through the years we worked together. Thank you for accepting me as your Ph.D. student at ÉTS. It has been an absolute pleasure for me to work with you, and I have truly appreciated your constructive comments throughout my Ph.D. studies. Thank you for giving me all the freedom to pursue my research topic and sharing your thoughts and concern. I wish to acknowledge the Natural Sciences and Engineering Research Council of Canada (NSERC) for their outstanding financial support to Professor Ghyslain Gagnon.

I wish to acknowledge and thank my co-supervisor, Professor Gordon W. Roberts, for all of his tremendous and kind-hearted support over the years that I worked in his Lab. I greatly appreciate for all of the intellectual discussions that we had about my research topic, and I am extremely grateful for all the questions and challenges at every step of my work to give my best. Research discussions with you have always been interesting for me. Thank you very much for patiently reading my papers and sharing your own experiences to help me succeed in my work.

I would also like to thank my Ph.D. committee members, Professor Mohamad Sawan, Professor Frédéric Nabki, and Professor Jérémie Voix for their critical and constructive feedback on this research.

A big thank you to my wife Hasti for her extraordinary love and confidence in my ability to succeed. This thesis would not have been possible without her unwavering support and patience.

I would like to especially thank my parents Zinat and Bahman, my brother Saman, and my families who never hesitate to support me during this journey. Your unconditional love and

support during all the years have been my unique motivation to move forward regardless of setbacks.

I would like to thank Mr. Mohammad Honarparvar for his intuitive and lengthy discussions we had in my first two years at ÉTS. Thank you for your help and encouragement. I hope that we can continue to work on analog and mixed-signal circuit design for the years to come. I would also like to thank Mr. Mohamed Ali who engaged in interesting discussions about the layout design. Thank you very much Mohamed Ali. Without your help, I wouldn't have finished the Layout before the deadline.

Last but not least, I want to thank my friends at LACIME, ÉTS and VLSI, McGill. I have been extremely lucky to be surrounded by a inspiring and brilliant colleagues that have commented on my research work and making our Lab a nice place to study. In particular, thank you to Hassan Mousavi, Mehdi Mozayan, Amir Shahshahani, Moataz Abdelfattah, Ahmed Kira, Mahmood Mohammed, Ahmed Emara.

I dedicate this work to my parents and my wife.

LES NOUVEAUX CIRCUITS POUR LA TRAITEMENT DE SIGNAL DANS LE DOMAINE TEMPOREL SUR DES CMOS DE BASSE TENSION

Soheyl ZIABAKHSH SHALMANI

RÉSUMÉ

Le dimensionnement agressif des technologies CMOS dans des procédés inférieurs à 100 nanomètres est la motivation de remplacer des circuits de traitement de signal en mode-tension et en mode-courant par des approches en mode temporel qui utilise des circuits numériques pour réaliser le traitement de signal. Puisque la différence de temps entre deux signaux est indépendante de leur amplitude, intuitivement, une représentation des signaux en mode temporel (« time-mode » ou TM) est censée d'être plus compatible avec les nouveaux procédés CMOS qui opèrent à des niveaux d'alimentation plus faibles. L'objectif des concepteurs de circuits TM et des chercheurs est d'identifier des nouvelles architectures de circuits pouvant exécuter l'opération élémentaire de traitement de signaux comme des additions, des soustractions, des multiplications, etc. Au cœur de ces efforts est la nécessité d'identifier des circuits TM qui pouvant exécuter ce type d'opération à de hauts niveaux de performance; le niveau qui est égal ou supérieur des circuits en mode-tension (VM) à des niveaux de puissances similaires.

Dans la première partie de la thèse, une revue exhaustive de la littérature est présentée. La revue inclut les spécifications des convertisseurs analogique-numérique-(ADC) et tous les développements majeurs dans le domaine des convertisseurs TMΔΣ au cours de la dernière décennie. Ensuite, nous présentons une comparaison rigoureuse des circuits TM discrets aux circuits VM continus afin d'identifier les lacunes qui à besoin d'être rempli. Comme première contribution, nous proposons une expression analytique pour l'effet de bruit sur la grille de retard de transistors PMOS-NMOS de TM et VM, menant à l'expression du pic-SNR des deux architectures. La théorie proposée sur le bruit est appliquée à différent procédés CMOS et comparés dans Spectre. En plus, nous fournissons l'implémentation du IC avec les résultats de mesuré pour vérifier les résultats de l'analyse.

Ensuite, comme seconde contribution, nous proposons des nouveaux sous-systèmes TM et une extension de certaines ancienne architectures diminuant les défis associés aux technologies CMOS modernes, sans affecter les métriques de performances. Le premier défi est la nécessité de délais d'une demi-période et d'une période complète pour les circuits TM, le second défi est le besoin pour les circuits TM d'effectuer des opérations arithmétiques de base (c.-à-d., addition ou soustraction) dans une large gamme linéaire et le troisième défi est de trouver comment réaliser une rétroaction négative dans le domaine du temps et le processus des signaux de haute fréquence autour de la fréquence intermédiaire (IF).

Comme troisième contribution, nous présenterons une réalisation complétement numérique d'un résonateur basé en intégrateur discret sans perte (LDI) en mode TM. Le résonateur est construit avec des sous-systèmes TM dans une configuration de rétroaction négative. Ce résonateur accomplit du traitement de signal en mode temporel de haute vitesse sans les limitations imposées par des techniques de circuits par commutation du condensateur (SC), tel que

des adaptations de condensateur pour réaliser des gains de signaux précis. La précision du circuit proposé est plutôt assurée par un circuit de délai adaptatif ajustant le délai de boucle dans une large bande de fréquence d'échantillonnage. L'opération du résonateur basé sur LDI du TM est validée avec des simulations au niveau du transistor et comparée au niveau système dans Simulink/MATLAB.

Finalement, nous proposons une nouvelle BPΔΣTDC hautement digital pour des applications IF. Dans un premier temps, l'architecture de la conception proposée est présentée; ainsi que la présentation les performances métriques attendu. Le BPΔΣTDC est capable de modeler le bruit de quantification dans une configuration à rétroaction négative, et n'exige aucun circuit complexe de calibration pour compenser des erreurs de synchronisation. En outre, pour la première fois dans les TMSP, une compensation « direct feed-forward » est utilisée dans un circuit TDC pour atteindre un grand rapport signal sur bruit et rapport de distorsion (SNDR). Nous démontrons le circuit TDC proposé dans le procédé CMOS 130nm d'IBM pour une tension d'alimentation aussi basse que 1.2 V. Une gamme de fréquence d'échantillonnage continue de 4 MHz à 42.8 MHz est réalisée pour numériser un signal centré à un quart de la fréquence d'échantillonnage. Cette conception atteint un sommet de SNDR de 39.5 dB sur une bande passante de 0.2 MHz pour une fréquence d'échantillonnage maximale de f_s=42.8 MS/s tout en consommant une puissance moins faible que 5 mW. De plus, nous identifions des orientations de recherche futures pour des conceptions de circuits en TM et dans la réalisation d'ordre élevé de BPΔΣTDC pour recherche.

Mots-clés: Retard adaptatif, convertisseur de Numérique-à-Temps, VCDU à deux fronts, unité de retard de demi période, gigue de phase, intégrateur discret sans perte, rétroaction négative en mode temporel, mise en forme du bruit, BPΔΣTDC de deuxième ordre, unité de commutation de retard, synchronisation, amplificateur de différence de temps, cellule de mémoire TM, mode Tension.

NEW CIRCUITS FOR TIME-DOMAIN SIGNAL PROCESSING IN LOW-VOLTAGE CMOS

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ABSTRACT

Aggressive scaling of CMOS technology in sub-100 nm process motivates the replacement of voltage or current-mode signal processing with time-mode approaches which uses digital circuits to perform signal processing. As the time difference between two signals is independent of the amplitude of either signal, intuitively, a time-mode (TM) signal representation is believed to be more compatible with newer CMOS processes that operate at lower power supply levels. It is the objective of TM circuit architects and researchers to identify new circuit architectures that can perform basic signal processing operations such as adding, subtracting, multiplications, etc. At the heart of these efforts is the need to identify TM circuits that perform such operation at high performance levels; levels that equal or exceed those of voltage-mode (VM) circuits at similar power levels.

In the first phase of this thesis, an intensive review of the literature is presented. The review includes $\Delta\Sigma$ analog-to-digital converter (ADC) specifications and all the major developments in the area of TM$\Delta\Sigma$ converters in the last decade. Then we present a rigorous comparison between discrete-time TM circuits and continuous-time VM circuits to identify gaps that need to be filled. As a first contribution, we provide an analytical expression for the noise operation of both a VM and TM PMOS-NMOS transistor stack, leading to the expression of the peak-SNR of both architectures. The proposed noise theory is applied to different CMOS process and compared in Spectre. In addition, we provide IC implementations with measurement results to verify the analysis finding.

Then, as a second contribution, we propose new TM building blocks and extensions to some old ones that alleviate the challenges imposed by modern CMOS technologies, without affecting the performance metrics. The first challenge is the need for half-period delay and full-period delay unit for TM circuits; the second challenge is the need for TM circuits to perform basic arithmetic operations (i.e., addition or subtraction) in wide linear range; and the third challenge is how to realize negative feedback in time-domain and process signals at higher frequency around intermediate frequency (IF).

As a third contribution, an all-digital realization of a TM lossless discrete integrator (LDI)-based resonator is presented. The resonator is constructed by new TM building blocks in a negative feedback configuration. This achieves high-speed time-mode signal processing without the limitations imposed by switched-capacitor (SC) circuit techniques such as the matching of capacitors to realize precise signal gains. Instead, circuit precision is realized using an adaptive delay circuit to adjust the loop delay in a wide range of sampling frequencies. The operation of the TM LDI-based resonator is validated with transistor-level simulations and compared with system-level in Simulink/MATLAB.

Finally, we propose a novel highly-digital BPΔ ΣTDC for IF applications. It first introduces the system architecture of the proposed design and presents the expected performance metrics. The BPΔΣTDC is able to shape the quantization noise in a negative feedback configuration, and it does not require any complex calibration circuit to compensate for timing errors. In addition, for the very first time in TMSP, a direct feed-forward compensation is utilized in the TDC to achieve high signal-to-noise and distortion ratio (SNDR). We demonstrate the proposed TDC in an IBM 130 nm CMOS process, while operating from a supply voltage as low as 1.2 V. A continuous sampling frequency range from 4 MHz to 42.8 MHz is achieved to digitize an input signal that is centered at one-quarter of sampling frequency. It achieves a 39.5 dB peak SNDR over a 0.2 MHz signal bandwidth at maximum sampling frequency f_s =42.8 MS/s while consuming lower than 5 mW power. Furthermore, we identify future directions in TM circuit design and high-order realization of BPΔ ΣTDC for research.

Keywords: Adaptive Delay, Digital-To-Time Converter, Double-Edge VCDU, Half-Period Delay Unit, Jitter, Lossless Discrete Integrator, Negative Time-Mode Feedback, Noise-Shaping, Second-Order BPΔΣTDC, Switched-Delay Unit, Synchronization, Time Difference Amplifier, TM Memory Cell, Voltage-Mode

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LIST OF ABREVIATIONS

ADC	Analog-to-Digital Converter
ADPLL	All-Digital Phase-Locked Loop
BPΔΣTDC	BandPass Delta Sigma Time-To-Digital Converter
BSF	Band Selection Filter
CMOS	Complementary Metal Oxide Semiconductor
DFF	D-type Flip Flop
DLL	Delay-Locked Loop
DR	Dynamic Range
DTC	Digital-to-Time Converter
FOM	Figure of Merit
GRO	Gated Ring Oscillator
IC	Integrated Circuit
IF	Intermediate Frequency
LDI	Lossless Discrete Integrator
LP	Low-Pass
LSB	Least Significant Bit
MASH	Multi-Stage Noise-Shaping
MUX	Multiplexer
OSR	LosslessOversampling Ratio

PCB	Printed Circuit Board
PSD	Power Spectral Density
PVT	Process, Voltage, and Temperature
MASH	Multi-Stage Noise-Shaping
SDU	Switched Delay Unit
SFDR	Spurious-Free Dynamic Range
SNDR	Signal-to-Noise-and-Distortion Ratio
SNR	Signal-to-Noise Ratio
SRO	Switched-Ring Oscillator
TVC	Time-to-Voltage Converter
TDA	Time-Difference Amplifier
TDC	Time-to-Digital Converter
TFF	T-type Flip Flop
TLatch	Time Latch
TM	Time-Mode
TMSP	Time-mode Signal Processing
ToF	Time-of-Flight
VTC	Voltage-to-Time Converter
VCDU	Voltage-Controlled Delay Unit
VM	Voltage-Mode

INTRODUCTION

The demand for low-power mixed-signal circuits that can be integrated into nanoscale CMOS technologies is rising constantly. This is driven by the need for longer-lasting portable computing and sensory applications, like smart phones, tablets, IoT, etc.. However, the performance of analog circuits in nanoscaled CMOS processes is degraded due to numerous technological challenges such as a reduction in the intrinsic gain of transistors, increased switching noise because of the closer proximity of circuits, and increased power consumption to maintain the same level of performance as that achieved in older CMOS technologies (Park *et al.*, 2009; M. Ali-Bakhshian and G.W. Roberts, 2012). In contrast, digital circuits have proven to be quite amenable in advanced CMOS technologies working with transistors with such low gains. Billions of transistors are now being integrated on a single chip in the form of digital logic where they are used to realize reliable computing and signal processing algorithms. It is therefore the goal of this thesis to develop analog signal-processing techniques that use digital logic gates as their basic building blocks.

An alternative approach to minimize the aforementioned issues is time-mode signal processing (TMSP) whose performance scales well with advanced CMOS technology as it relies exclusively on the switching principle of digital logic circuits. In this approach, signal information is encoded as the time-difference between the rising edges of two independent digital step-like signals, with one of the digital signals acting as the reference (Yu *et al.*, 2014). As a consequence, the TMSP technique provides analog signal processing capabilities in advanced CMOS technologies such as FinFET technology that are digitally-enhanced using on-chip calibration techniques, phase-locked to the incoming reference signal. By doing so, CMOS circuits that are robust to process variations, supply level changes and temperature excursions, i.e., PVT effects, can be realized. Moreover, TMSP provides a circuit technique whose dynamic range improves with process scaling. For instance, the upper limit to the dynamic range (DR) of a VM circuit can be quantified as the ratio of the power supply level, V_{DD}, to the voltage noise

limit, $\sqrt{KT/C}$. With advances in technology scaling, V_{DD} must be reduced, hence the DR falls in a VM circuit. In contrast, the DR of a TM circuit, being the ratio of reference clock period T_s to the clock jitter, falls at a much slower rate than VM circuits (Figueiredo *et al.*, 2012). In addition, TMSP offers the opportunity to employ highly efficient digital circuits performing sampled-data analog applications, instead of the foreground SC circuits used in analog data converters (i.e., ADCs, DAC, ΔΣ converters, etc.).

Recently, several TM data converters have been reported. Such efforts are exemplified in a VCDU-based ΔΣM (Taillefer and Roberts, 2009), multi-path gated ring oscillator TDC (Straayer and Perrott, 2009), voltage-controlled gated-ring oscillator (VC-GRO) (Yu *et al.*, 2013), voltage-controlled oscillator (VCO)-based with multi-bit quantizer (Kim *et al.*, 2010), delay-locked-loop (DLL) based with voltage-controlled delay line (VCDL) technique as a quantizer (Lin *et al.*, 2012), as well as circuits circuits that operates like a discrete-time filter (Guttman and Roberts, 2009). One of the key building blocks of the TM systems is the time-to-digital converter (TDC), has been used more and more frequently in many applications, such as time-of-flight (ToF) (Vornicu *et al.*, 2017), jitter measurement (Nose *et al.*, 2006), medical imaging (Chen *et al.*, 2017), all-digital PLL (ADPLL) (Cao *et al.*, 2012; Avivi *et al.*, 2017), and time-domain analog-to-digital converters (ADCs) (Naraghi *et al.*, 2010; Daniels *et al.*, 2010; Hsu, *et al.*, 2008; Yu, *et al.*, 2014).

Different types of TDC architectures have been established to process TM information in the range of sub-nanosecond or even sub-picosecond resolution for instrumentation or audio applications. TDCs can be classified into two categories: 1) Nyquist-rate TDCs, which process the TM signals in a memory-less manner; and 2) the oversampled counterparts, which process the previous samples with present TM samples at a rate higher than the minimum Nyquist-rate (Hesener *et al.*, 2007; B. G. Lee, 2015). The simplest design of a Nyquist-rate TDC is a FLASH TDC, which can be implemented by an inverter-based delay-line and a comparator. The main

issue with the FLASH TDC is that its time resolution is limited by the propagation delay of each inverter (Jansson *et al.*, 2009). To achieve a better resolution, pulse shrinking TDC (Chen *et al.*, 2000) and vernier delay line (VDL) TDC (Lu *et al.*, 2012) architectures were developed, where the effective time resolution has been improved to the sub-gate [1] propagation delay timing resolution. Despite these improvements, they consume more power and silicon area as the dynamic range of TDC increases. Another drawback of this approach is that the mismatch between vernier delay elements, limits the application of such designs. In order to facilitate circuit integration and reduce the mismatch, a DLL vernier TDC and vernier-ring oscillator TDC were proposed to stabilize the delay chain in the conventional design against process, voltage, and temperature (PVT) variations (Roberts and Ali-Bakhshian, 2010; Yu *et al.*, 2010). However, time resolution and power consumption in such types of TDCs are identical to the conventional vernier design. To alleviate the aforementioned problems in Nyquist-rate TDCs, two and three dimension vernier TDCs were developed to reduce the length of delay cells for a given full scale range, thus leading to an improvement in reducing the integral nonlinearity (INL) error and jitter (Vercesi *et al.*, 2010; Yu *et al.*, 2010) performance metrics. The main disadvantage of these TDCs is that the frequency range is limited to DC up to a few tens-of-kilo-Hertz.

Oversampling TDCs with quantization noise shaping have recently emerged as a viable alternative approach to improve the time-resolution and overall conversion dynamic range, as in (Young *et al.*, 2010; Gande *et al.*, 2012), that have achieved second-order and third-order noise shaping, respectively. However, these TM$\Delta\Sigma$TDCs rely on analog intensive approaches as the TM signals are converted back and forth between voltage or current signals. These approaches are less attractive in advanced CMOS processes with low supply voltage and relatively unchanged threshold voltage (V_{TH}). For instance, the non-linearity effect of time-to-voltage converter (TVC) or voltage-to-time conversion (VTC) limits the dynamic range of such TDCs. To address this issue, a gated-ring oscillator (GRO) based you TDC was implemented in an

[1] sub-gate is a mismatch between two inverter's individual delay values.

all-digital solution (Straayer *et al.*, 2009). This approach nearly halves the chip area and power consumption compared to the conventional designs. However, the GRO-based TDC has some performance limitations, such as limited time-resolution and skew error due to a dead-zone in its hold-time.

In (Elshazly *et al.*, 2014), an open-loop noise-shaping switched-ring oscillator TDC (SRO-TDC) has been shown to achieve high time resolution with a high oversampling ratio (OSR). In this architecture, the TDC toggles between two high and low frequencies in order to decrease the skew error and charge leakage effects. In (Yu, *et al.*, 2015), a closed-loop 1-3 multi-stage noise-shaping (MASH) TDC was proposed to increase the order of modulator to achieve better performance (e.g., time resolution, rms noise voltage, bandwidth, SNDR). Although this closed-loop TDC topology is elegant, some drawbacks remain. The first-stage of the proposed MASH architecture is always limited to the first-order noise shaping (i.e., 1-1, 1-2, 1-3 MASH architecture) and there is no opportunities to realize 2-1, 2-2, or 3-2 MASH architecture. In addition, the linearity of GRO-based TDC is restricted by the intrinsic errors of the GRO during the hold time.

Thesis Scope and Contributions

This thesis investigates the performance limitations of an existing type of TMΔΣ modulators and compare their performances with the VMΔΣ modulators in term of SNDR, silicon area, signal bandwidth, and power consumption. In addition, the maximum achievable SNR of a PMOS-NMOS transistor stack, used as amplifier (VM) or as delay element (TM) is analyzed and examined. This analysis provides new observation in the design of TM circuits in new technology nodes. It addresses how TM circuit could potentially achieve better SNR with technology scaling. Then, we study TM building blocks and how they used in the development of a complex TM mixed-signal circuits. Then, we propose new TM circuits able to cope with the challenges associated with the previous works. This thesis reveals that by adopting TM

circuits a LDI-based resonator and BPΔΣTDC can be implemented using only digital gates. This will prove beneficial in digitization at higher frequency with little power budget, little chip area, and possibility of high-speed operational frequency.

The main contributions of this thesis which led to a book chapter, two journal papers, and three conference papers could be listed as follows:

(a) A comprehensive surveying and comparing of most recent TMΔΣ modulators is reported (see Chapter 1).

Related publication:

S. Ziabakhsh, G. Gagnon, G. W. Roberts, "Book chapter: Time-Mode Delta-Sigma Converters" of book entitled "Time-Mode Delta-Sigma Converters", by author Fei Yuan., CRC Press, Technology and Engineering - 412 pages, 2015.

(b) An analytical expression for the noise operation of both VM and TM PMOS-NMOS transistor stack is proposed (see Chapter 2).

Related publication:

S. Ziabakhsh, G. Gagnon, G. W. Roberts, "The Peak-SNR Performances of Voltage-Mode versus Time-Mode Circuits: the PMOS-NMOS Stack Use Case," *IEEE Transactions on Circuits and Systems II: Express Briefs*, Accepted March 7, 2018.

(c) Design, fabrication, and measurement of a TM second-order BPΔΣTDC is presented (see Chapter 3).

Related publications:

S. Ziabakhsh, G. Gagnon, G. W. Roberts, "A Second-Order Bandpass ΔΣ Time-to-Digital Converter with Negative Time-Mode Feedback," *IEEE Transactions on Circuits and Systems I: Regular Papers*, Submitted April 19, 2018.

S. Ziabakhsh, G. Gagnon, G. W. Roberts, "A Time-Mode LDI-Based Resonator for a Band-Pass Delta-Sigma TDC", *60th IEEE International Midwest Symposium on Circuits and Systems (MWSCAS)*, Boston, USA, 2017.

(d) New measurement setup to validate the operation of BPΔΣTDC is reported. In this measurement, phase modulated signals are produced in Cadence Spectre and imported to the arbitrary waveform generator. Subsequently, there is no non-linearity effect associated to the input TM signals (see chapter 4).

(e) The new design of VCDU that converts the analog signal into a time-difference signal is proposed. This is achieved by using a signal conditioning circuit to extend the input voltage linear range with very low linearity error (see chapter 5).

Related publication:

S. Ziabakhsh, G. Gagnon, G. W. Roberts, "Wide linear range voltage-controlled delay unit for time-mode signal processing", *IEEE International Symposium on Circuits and Systems (ISCAS)*, Portugal, 2015.

(f) A novel programmable TLatch-based TDA with femtosecond resolution is presented. The proposed circuit uses three TLatches in its structure with digital switches to control the gain of circuit easily (see chapter 5).

Related publication:

S. Ziabakhsh, G. Gagnon, G. W. Roberts, "An All-Digital High-Resolution Programmable Time-Difference Amplifier Based on Time Latch", *IEEE International Symposium on Circuits and Systems (ISCAS)*, Italy, 2018.

Thesis Outline

The thesis is organized into five chapters as follows:

In the first chapter, an overview of the fundamental theory of ΔΣ modulators and important ADC performance metrics are identified and categorized. It explains the concepts of dynamic range, resolution, distortion, and stability. It also describes the first-order,high-order, and multi-bit TM ΔΣ modulators. Chapter two also presents the TM ΔΣ design issues (i.e., non-linearity, mismatch, etc.) and provides a comparison between TM and VM ΔΣ modulators.

The second chapter extends the discussion of comparison of VM versus TM circuits and provides a noise analysis for a PMOS-NMOS transistor stack. It presents a detailed noise analysis which includes both thermal and flicker noises in both domains across different technology nodes. The accuracy of the proposed analysis is demonstrated by measurement results and transistor-level transient noise simulations in Spectre. We end the chapter by showing the maximum achievable SNR for both VM and TM circuits in future CMOS technologies.

Chapter three covers the design of the individual building blocks of the TM LDI-based resonator; namely the half-period delay unit, cascading of two half-period delay units, adaptive time offset correction, TM subtractor, and half-period delay DTC. For each of the aforementioned TM circuits, we present the principle operation, non-idealities, timing-diagram, and transfer characteristic. Monte-Carlo analysis in Spectre of each of these blocks are presented and discussed. In this chapter, a top-down approach for the design of second-order BPΔΣTDC is presented. The design methodology is based on a system-level approach in Simulink/MATLAB and modeling each block with the transistor-level design.

In the fourth chapter, the experimental setup of the BPΔΣTDC is presented. Measurement results from the fabricated chip and simulation results in Spectre and MATLAB are compared and discussed. The TDC covers a sampling frequency range from 4 MHz to 42.8 MHz, and consumed 4.98 mW while operating from a 1.2 V supply voltage.

In chapter five, the design of the wide linear range VCDU needed for the TMSP applications is demonstrated. By doing so, the VCDU utilized a signal conditioning circuit that significantly increases the linear range operation and enhances the SNDR when it is used in a VCDU-based $\Delta\Sigma$ modulator. Furthermore, a novel all-digital time-difference amplifier (TDA) using time latches was proposed which achieves accurate, high resolution, and programmable gains. Simulation results are provided to verify the operation principles of the two circuits.

Finally, this thesis is concluded where the work is summarized and future advancements of the proposed approach are offered.

CHAPTER 1

FUNDAMENTALS OF TMΔΣ MODULATORS

1.1 Introduction

The aim of this chapter is to describe delta-sigma (ΔΣ) converters that adopt TMSP techniques. Recently, several studies on TMΔΣ converters have been conducted showing that such methodology has high potential in low-voltage design. The noise-shaping behavior demonstrated by this technique can be implemented and extended in various ways, including VCDU or GRO-based implementations of TMΔΣ converters. In this chapter, after a brief review of ΔΣ ADC specifications, we will discuss different architectures of TMΔΣ converters that have been recently proposed. The following chapter is based on:

S. Ziabakhsh, G. Gagnon, G. W. Roberts, "Book chapter: Time-Mode Delta-Sigma Converters" of book entitled "Time-Mode Delta-Sigma Converters," by author Fei Yuan., CRC Press, Technology and Engineering-412 pages, 2015.

1.2 Theory of ΔΣ Modulators

The basic architecture of a conventional ΔΣ modulator is shown in Figure 1.1. It consists of a difference amplifier, loop filter and an one-bit quantizer in the feed-forward path, and a one-bit digital-to-analog converter (DAC) in the feedback signal path. The front-end difference amplifier and loop filter are often realized using a high-performance SC circuit, and the quantizer is often realized using a high-speed latched comparator circuit. As the DAC provides only one-bit conversion, a simple set of analog switches is used to realize this element. Through the negative-feedback action provided by the feedback path, the effects of non-linearities in the feed-forward signal path are reduced by the loop gain. This action has come to be known in the ΔΣ modulator literature as noise-shaping (Pavan *et al.*, 2017; Jose *et al.*, 2011; Kozak *et al.*, 2003), where the quantization noise introduced by the quantizer is pushed or shaped away in frequency from the signal band.

In multibit ΔΣ modulators, the quantizer and the DAC operate on more than two levels and, correspondingly, require a more complicated circuit realization. An important implementation issue with the multibit DAC is the requirement for high linearity. To achieve this result over multiple manufacturing runs, very good element matching is required. However, as the dimensions of CMOS transistors scale downward, matching becomes more difficult to achieve (Yuan *et al.*, 2014). In the following, the basic principles of a ΔΣ modulator will be described along with its various performance metrics.

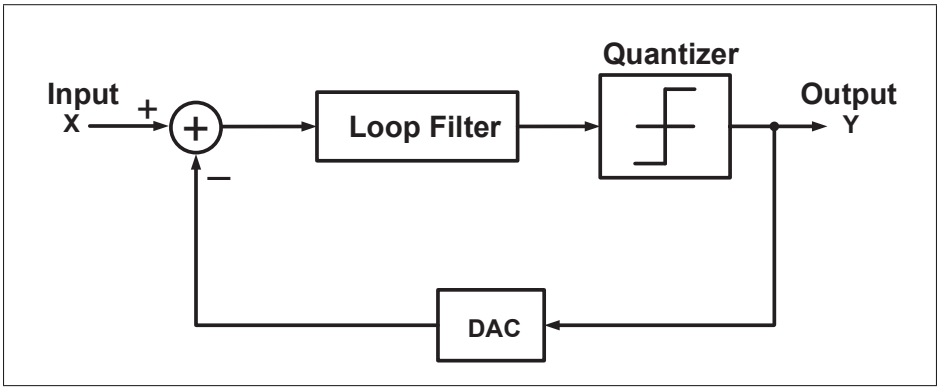
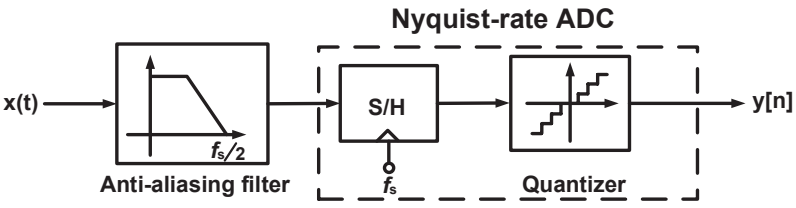


Figure 1.1 Basic architecture of a conventional ΔΣ modulator.

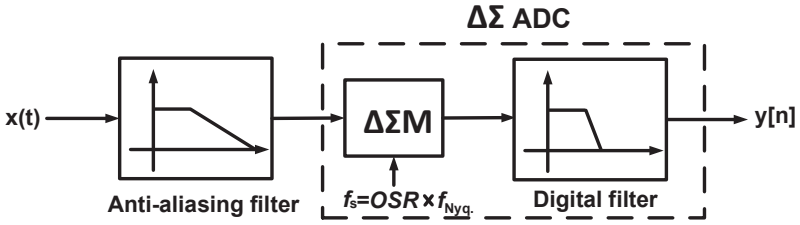
1.2.1 Basic Principles of a ΔΣ Modulator

The process of converting an analog continuous-time signal $x(t)$ into a sequence of digital numbers $y[n]$ requires a front-end anti-aliasing filter circuit, a sample-and-hold (S/H) circuit, and the corresponding multilevel quantizer or ADC circuit as illustrated in Figure 1.2. The front-end low-pass (LP) filter is used to minimize the potential threat of unwanted highfrequency signals from aliasing into the base-band frequency region that the desired signal occupies. The anti-aliasing filter is designed to have a bandwidth equal to the incoming desired signal and a stop-band region very near to one-half the sampling frequency, *fs*—also referred to the Nyquist frequency. In contrast, an ADC constructed using a ΔΣ modulator takes on a slightly different realization. While the front-end requires an anti-aliasing filter and an S/H circuit, the quantizer

is realized using a ΔΣ modulator, followed by a LP brick-wall digital filter used to remove the noise-shaped quantization noise. Unlike a Nyquist-rate ADC that samples the input signal at



a) Nyquist-rate implementation.



b) Oversampling or ΔΣ-based implementation.

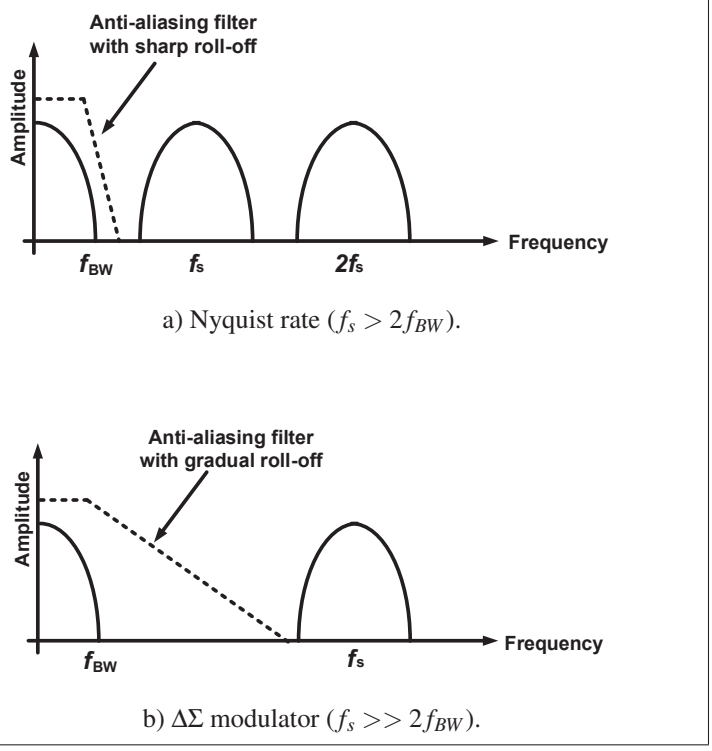
Figure 1.2 Two types of ADC schemes.

twice its signal bandwidth, that is, $f_s = 2 \times f_{BW}$, a ΔΣ-based ADC oversamples the incoming signal at a rate much greater than twice the signal bandwidth. The ratio of one-half of the sampling rate to the signal bandwidth f_{BW} is defined as the OSR, that is,

$$OSR = \frac{f_s/2}{f_{BW}} \tag{1.1}$$

An important advantage of oversampling the incoming signal is that it relaxes the requirements on the anti-aliasing filter circuit. In fact, the anti-aliasing filter is typically implemented with a simple low-order filter that requires little power (Jose *et al.*, 2011). As a means to compare the filter requirements for the two types of ADC schemes, an illustration of the anti-aliasing filter magnitude response is provided in Figure 1.3. In Figure 1.3(a), the magnitude response for the Nyquist-rate ADC filter is shown, and Figure 1.3(b) presents the corresponding response for

the ΔΣ-based ADC implementation. While each filter has the same analog bandwidth, as it is assumed that each ADC will see the same incoming signal, the transition region of the filter is quite different. The stop-band region for the ΔΣ-based ADC would be much higher than that required for the Nyquist-rate ADC. This greatly reduces the complexity of the anti-aliasing filter as mentioned earlier. The error between the information carried by the input analog signal



a) Nyquist rate ($f_s > 2f_{BW}$).

b) ΔΣ modulator ($f_s >> 2f_{BW}$).

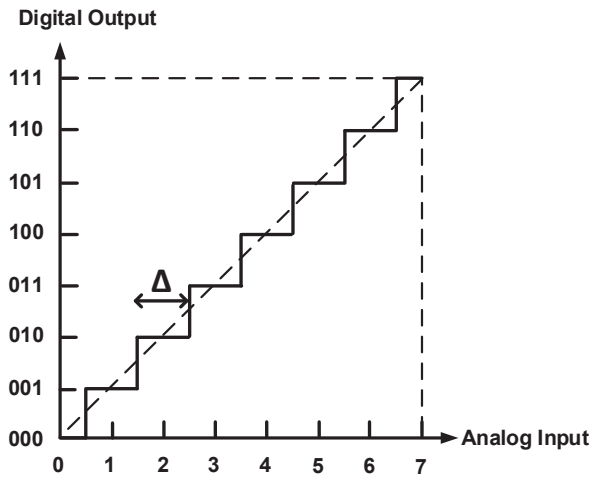
Figure 1.3 Filter requirement.

$x(t)$ and the information carried by an ideal quantized output digital signal $y[n]$ is defined as the quantization error. Such a situation is depicted in Figure 1.4 where the transfer characteristic of an ideal quantizer is shown in Figure 1.4(a). Here we see the quantizer has a staircase-like shape with the width of each staircase equal to Δ, also referred to as the least-significant bit (LSB) of the analog-to-digital conversion process. When subtracted from a perfect conversion process (one without error, as depicted by the dashed line in Figure 1.4(a)), the quantization error curve results as shown in Figure 1.4(b). The quantization error is bounded between -Δ/2

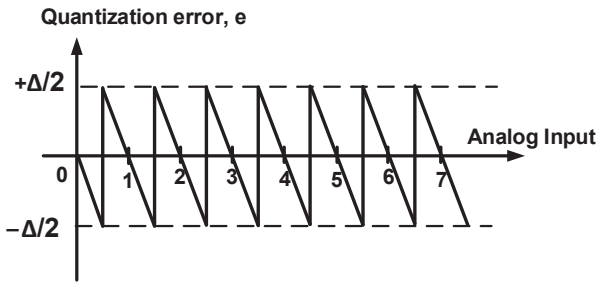
and +Δ/2 for any level of analog input. Also we see that the average error is zero and it has an RMS error defined by

$$e_{rms}^2 = \int_0^1 [e(v_{in})]^2 \, dv_{in} = \frac{\Delta^2}{12} \tag{1.2}$$

Through careful construction, one can show that under certain conditions, this quantization



a) Transfer characteristic of input and output signal.



b) Quantization error.

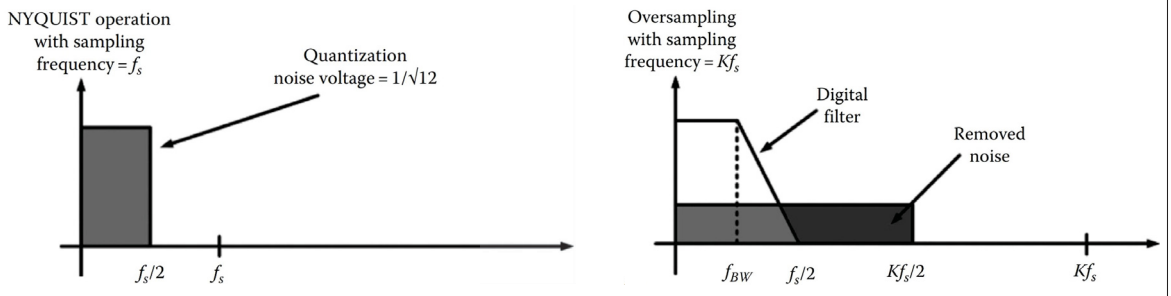
Figure 1.4 Illustrating the quantization process.

noise power is uniformly distributed in the frequency range (0, f_s/2). Based on this criterion, the single-sided quantization noise power spectral density expressed in terms V^2/Hz can be

defined simply as

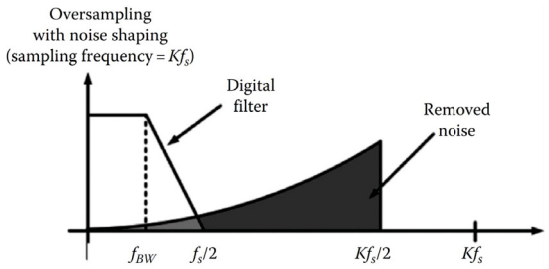
$$N_q = \frac{\Delta^2}{6f_s} \tag{1.3}$$

Figure 1.5(a) illustrates the uniform power-spectral density (PSD) of the ideal quantizer with $\Delta = 1$. Here the total noise power is equal to $1/12\ V^2$, which is equivalent to an RMS noise voltage of $1/\sqrt{12}\ V$.



a) PSD reference quantizer with $\Delta = 1$.

b) PSD of an oversampled quantizer by factor K with digital filter response overlaid.



c) Noise-shaped PSD of quantizer with digital filter response overlaid.

Figure 1.5 Illustrating the effect of oversampling and noise-shaping on the PSD of an ideal quantizer.

From (1.3), the magnitude of the RMS quantization error can be reduced by decreasing the step size of the quantizer. Another approach would be to increase the sampling rate of the quantizer, say by a factor of K, and pass the quantizer output through a LP filter with a bandwidth equal to the signal bandwidth f_{BW}. By doing so, according to (1.3), the PSD of the quantization noise

will be spread over a larger frequency range (0, $Kf_s/2$) with magnitude

$$N_q^{'} = \frac{\Delta^2}{6}\frac{1}{Kf_s} \tag{1.4}$$

Since the noise power is uniform over the frequency range (0, f_{BW}), and since the factor K is equivalent to the OSR parameter introduced earlier, then the total output quantization noise power reduces to

$$e_{rms}^{'} = N_q^{'} \times \frac{f_{BW}}{K \times f_s/2} = N_q^{'} \times \frac{f_{BW}}{OSR \times f_s/2} \tag{1.5}$$

For a digital filter with transfer function $H_d(z)$, the in-band noise power that passes through the filter would be more correctly represented by the integral equation,

$$n_0^2 = \int_{f_1}^{f_2} |H_d(f)| N_q^{'} df \tag{1.6}$$

This situation is depicted in Figure 1.5(b) where the quantization noise PSD is spread over a bandwidth of Kf_s, but only a portion of the noise passes through the digital filter.

Equation (1.5) reveals two important facts related to oversampling, followed by LP filtering: (1) The higher the oversampling factor OSR, the smaller is the output RMS error, and (2) the smaller the signal bandwidth, the smaller is the RMS noise error. To gain, say, a 10 dB improvement in noise reduction would require a 10-fold increase in the sampling rate. Any further noise power reduction would come at the expense of impractical increases in the sampling rate of the quantizer.

$\Delta\Sigma$-based analog-to-digital conversion provides an alternative means in which to reduce the magnitude of the quantization noise at the ADC output. Through the application of noise-shaping, the feedback loop established around the quantizer reduces the amount of quantization that makes its way to the output based on the amount of gain in the feedback loop. Mathematically, this effect can be quantified by writing an expression for the output signal $Y(z)$ in the

z-domain in terms of the input signal $X(z)$ and the quantization error signal $E(z)$, according to

$$Y(z) = STF(z)X(z) + NTF(z)E(z) \tag{1.7}$$

where $STF(z)$ and $NTF(z)$ are denoted as the signal and noise transfer functions, respectively. For a first-order LP ΔΣ modulator, the output signal in the z-domain is expressed as

$$Y_{LP}(z) = z^{-1}X(z) + (1 - z^{-1})E(z) \tag{1.8}$$

leading to $STF = z^{-1}$ and $NTF = 1 - z^{-1}$. The signal transfer function (STF) simply signifies that the output will contain a one-clock period delay of the input signal, essentially with the input information unchanged. In the case of the noise transfer function (NTF), a transmission zero appears at DC, corresponding to a gain of 0. Likewise, at the Nyquist frequency, that is, $f = f_s/2$, the NTF has a gain of 2. For frequencies between DC and Nyquist, the NTF will have a high-pass behavior. Consequently, the quantization noise injected by the quantizer will have little effect on the incoming signal at low frequencies but doubles up for frequencies close to the Nyquist frequency. This situation is illustrated in Figure 1.5(c) whereby noise shaping combined with digital filtering greatly reduces the level of output quantization noise.

For higher-order modulators, whereby the NTF is of order greater than 1, even less quantization noise power will appear at the output. This is illustrated in Figure 1.6 where the quantization noise PSD appears at the output of the ΔΣ modulator for orders of 1, 2, and 3. As is evident from this plot, the higher the modulator order, the lower is the quantization noise PSD at frequencies close to DC.

1.2.2 Some ADC Performance Metrics

The most commonly quoted ADC performance parameters are sampling frequency, DR, resolution, distortion, power dissipation, chip area, and stability. These metrics will be defined and discussed in the following.

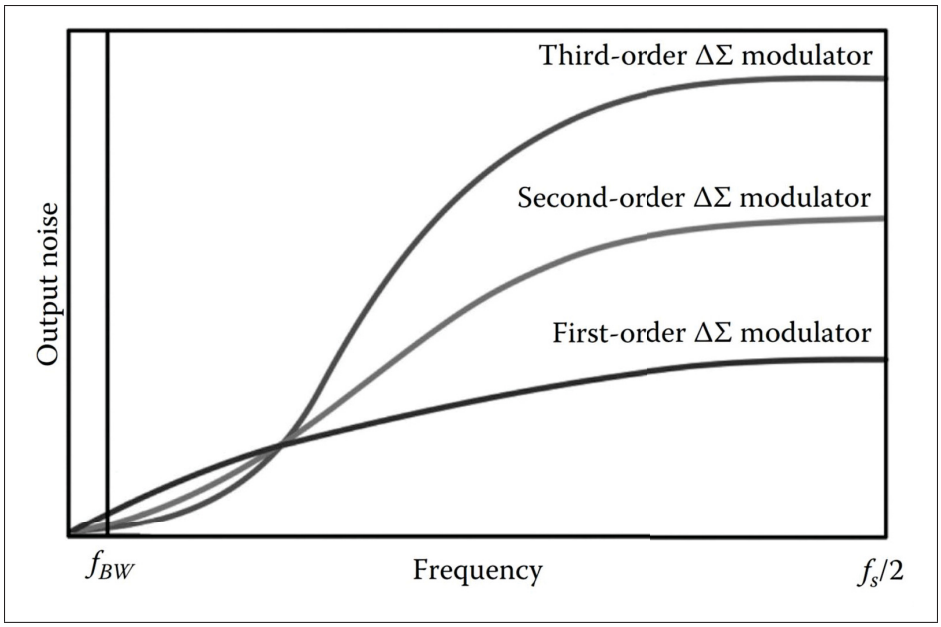


Figure 1.6 High-order noise shaping and its effect on the output quantization noise PSD.

1.2.2.1 Sampling Frequency

Generally speaking, the sampling frequency is defined as the rate at which the sampling process takes place. This parameter in Nyquist-rate ADCs is set to twice the signal bandwidth and in ΔΣADCs is set to higher values to significantly decrease the in-band quantization noise. On the other hand, higher sampling frequencies lead to higher power consumption and increased sensitivities to clock jitter issues. High-order and multibit ΔΣ modulators are two techniques that can be used to compensate for these effects and lead to higher performance ADCs.

1.2.2.2 Dynamic range

Dynamic range (DR) is defined as the ratio between the maximum applied sinusoidal input signal to the smallest that is discernible at the output of the ADC from any other unwanted or undesirable signal created by the ADC, for example, quantization and thermal noise, and distortion. The simplest manner in which to extract the DR metric is to measure the SNDR as a function of the input signal level, such as that shown in Figure 1.7. The DR metric expressed

in dB would then be defined as the difference in the maximum and minimum input levels in dB for which the SNDR=0 dB, that is,

$$DR|_{dB} = V_{in,max,dB} - V_{in,min,dB} \tag{1.9}$$

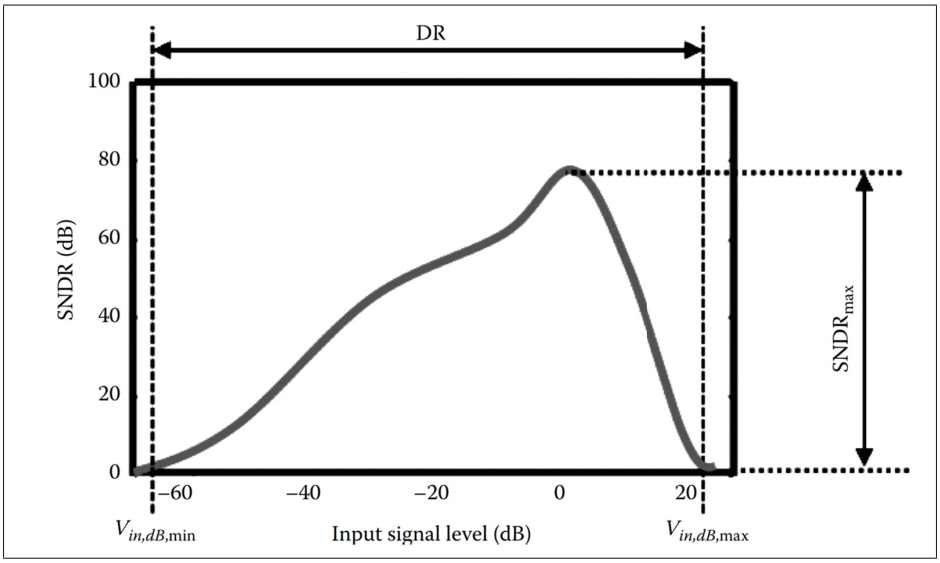


Figure 1.7 High-order noise shaping and its effect on the output quantization noise PSD.

Often, in practice, the maximum input level will be limited by the power supply or some other upper limit instead of the SNDR value falling back to the 0 dB level. Nonetheless, Figure 1.7 conveys the general idea behind the DR metric.

As CMOS technology advances to smaller dimensions, one observes that the DR of ADCs tends to decrease, a result attributed to smaller transistor gate oxide, lower supply voltages, and greater transistor thermal noise levels. Novel signal processing methods like TMSP may help to resolve the DR issue in advanced CMOS processes (Taillefer, *et al.*, 2009).

1.2.2.3 Resolution

The resolution of an N-bit ADC is defined as the smallest change in the analog input voltage that leads to a corresponding consistent change in the digital code output. In terms of our previous discussion related to Figure 1.4, the resolution of an ideal quantizer would simply be equal to the width of the staircase specified by Δ. In the ideal case, Δ would be defined in terms of the full-scale output range (FSR) and the total number of bits specified by the architecture, N, given by the following expression

$$\Delta = \frac{FSR}{2^N - 1} \tag{1.10}$$

A related metric, but one that is easier to extract in practice, is called the effective resolution of the ADC, Δ_{eff}, and is defined in terms of the effective number of bits (ENOBs) of the ADC in the following way:

$$\Delta_{eff} = \frac{FSR}{2^{ENOB} - 1} \tag{1.11}$$

Here ENOB represents the maximum value of the SNDR plot (see Figure 1.7) converted from dBs to equivalent bits (Plassche *et al.*, 2013) using the following formula

$$ENOB = \frac{SNDR|_{max} - 1.76\,dB}{6.02} \tag{1.12}$$

The effective ADC resolution is always less than the ideal ADC resolution, that is, $\Delta_{eff} < \Delta$.

1.2.2.4 Distortion

Signal distortion occurs with increasing input signal level on account of the general nonlinear nature of semiconductor devices, in addition to mismatches between ADC elements. One attractive technique to compensate for component mismatch effects is to include circuits that average out any component mismatch. Some of these approaches are: offset cancellation

(Razavi *et al.*, 1992), DLL (Roberts *et al.*, 2010), dynamic element matching (DEM) (Ninh *et al.*, 2011), and laser trimming during postpackaging manufacturing.

1.2.2.5 Power Dissipation and Chip Area

In the design of ADC circuits, there are two important requirements that must be taken into account. This includes both the ability to achieve good performance and low power operation, as well as a small silicon footprint. With the ongoing scaling-down of CMOS technology, power consumption is expected to decrease as the supply voltage must be reduced. On the other hand, reducing the supply voltage causes several drawbacks in the corresponding analog circuits (such as reducing DR, increasing the switching noise and gate leakage, etc.) especially when the performance requirements are to be maintained, for example, build a 12-bit ADC. One way to overcome these limitations in low-voltage design is to shift the analog design to the digital domain in an attempt to be more compatible with modern CMOS technologies. To this end, in this chapter, we offer several novel techniques that perform analog-to-digital conversion in the time-domain without consuming large amounts of power or die area—hopefully, fulfilling the goal of achieving high-resolution analog circuits in nanometer CMOS technologies.

1.2.2.6 Stability Considerations

It is well known by ADC designers that high-order $\Delta\Sigma$ modulators can become unstable. In (Norsworthy *et al.*, 1997), the stability of a sixth-order modulator is evaluated. They show that changing the gain of quantizer can change the location of closed-loop poles and cause instability. The main reason is that for some unique values of quantizer gain, the poles move outside of the unit circuit in the z-domain and cause the modulator to go unstable. Several works have followed this line of reasoning and have attempted to model this effect in $\Delta\Sigma$ modulators. The basic model is to replace the quantizer with a two-input adder, having one input from the quantizer and the other connected to a source of additive noise modeling the quantization process. While this model defines the noise-shaping process described earlier in the usual way, it places emphasis on the lack of knowledge related to the noise properties of

the quantizer and the fact that the stability of the modulator cannot be determined without this knowledge. Research is presently ongoing and further details can be found in (Bairdy *et al.*, 1994; Macii *et al.*, 2006; Lota *et al.*, 2014).

1.3 First-order Single-Bit TM ΔΣ Modulators

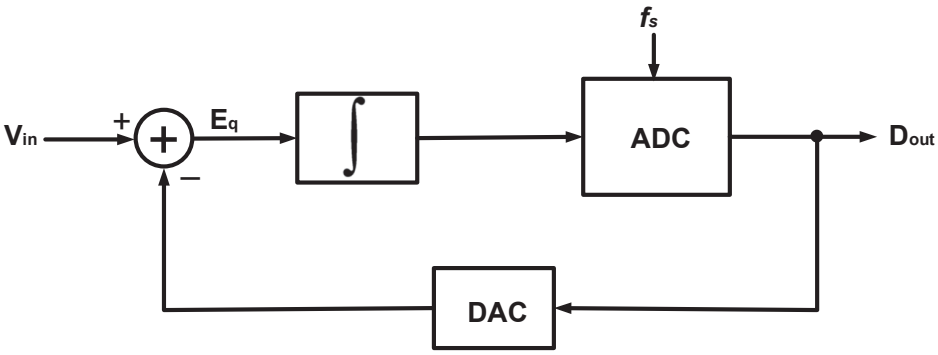
It is the intent of this section to learn about various ΔΣ modulators implemented using TMSP techniques that have been published in recent years. The various architectures have been classified according to either their key building block or some distinguishing architectural feature. This will include a discussion on a VCDU-based ΔΣ modulator, an open-loop ΔΣ modulator design approach, a DLL-based ΔΣ modulator, and a TDC-based ΔΣ modulator.

1.3.1 VCDU-Based ΔΣ Modulator

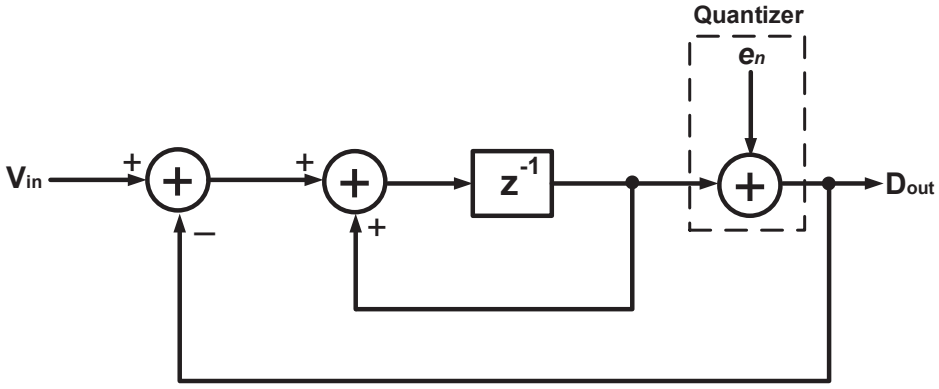
Let us begin by considering a first-order ΔΣ modulator with sampled-data input signal, $v_{in}[n]$, whereby the loop filter is implemented with a first-order discretetime integrator, an analog summer, a quantizer with a 1-linear bit ADC with output $D_{out}[n]$, and a 1-bit DAC in the feedback path as shown in Figure 1.8(a). Assuming a linear model for the quantizer with error $e[n]$, a first-order ΔΣ modulator can be described with the block diagram shown in Figure 1.8(b). Writing the output signal $D_{out}[n]$ in terms of the two inputs $v_{in}[n]$ and $e[n]$, one obtains the following time-difference equation

$$D_{out}[n] = v_{in}[n-1] + (e[n] - e[n-1]) \tag{1.13}$$

The aforementioned equation reveals the error feedback nature of the ΔΣ modulator whereby the digital output is a sum of the input and the first-order time difference of the quantizer error. If the quantizer errors $e[n]$ and $e[n-1]$ are similar, that is, through oversampling, their contribution will be small and the output D_{out} will be a very good approximation to the input v_{in}.



a) Block diagram of a first-order ΔΣ modulator.



b) Linear model of operation.

Figure 1.8 First-order ΔΣ modulator

An approach introduced in (Taillefer *et al.*, 2009) that implements a similar first-order difference equation is shown in Figure 1.9. Here a noise-shaped error behavior is realized by two voltage-controlled ring oscillators that perform phase integration followed by a D-type flip-flop (DFF) and some digital inverters. The two ring oscillators are constructed using two sets of VCDUs whose output is fed back to its input via a single inverter circuit.

The DFF is employed as a 1-bit quantizer.

In this design, the period of oscillation of the bottom-most ring oscillator is governed by the reference voltage, V_{ref}. By keeping this quantity fixed to a constant value, the period or fre-

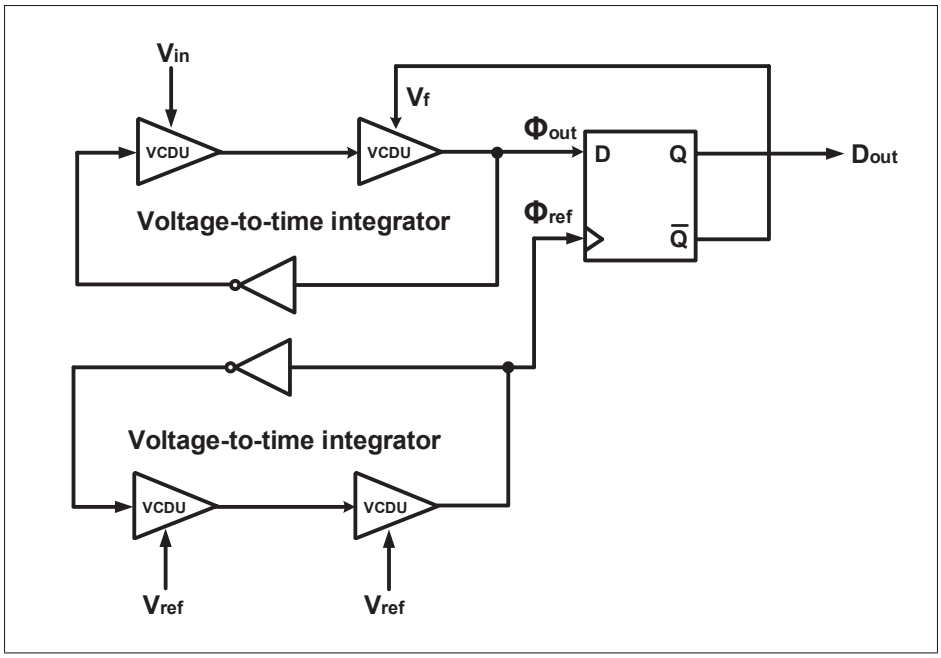


Figure 1.9 Time-mode single-ended ΔΣ modulator with VCDU.

quency of this oscillator is held constant. The period of the top-most integrator is controlled by the input voltage $v_{in}[n]$ and the digital output of the modulator through the two input control terminals via the VCDUs. The difference in phase of the leading edge of the two ring oscillators is compared by the DFF. If the phase of the reference oscillator output denoted by Φ_{ref} lags the phase of the output of the input-controlled oscillator Φ_{out} , the flip-flop will output logic 1, otherwise it will output logic 0. As the output of the flip-flop is also fed back to control the oscillation frequency of the top oscillator, a noise-shaping action occurs. Following the mathematical development given in (Taillefer *et al.*, 2009), the difference equation between the input and output of the ΔΣ modulator is found to be

$$D_{out}[n] = v_{in}[n-1] + \frac{T_e[n] - T_e[n-1]}{G_\phi} \tag{1.14}$$

where

G_ϕ is the voltage-to-time conversion factor of the VCDUs

$T_e[n]$ is the error sequence made by DFF

When compared to the difference equation derived for the first-order modulator provided in (1.15), one finds that they have similar form.

1.3.2 Open-loop TMΔΣ Modulators

Another approach to perform analog-to-digital conversion is based on the application of a VCO or a GRO running in an open-loop manner followed by a digital counter or filter circuit (Kim *et al.*, 2006; Straayer *et al.*, 2008; Kim *et al.*, 2010; Si *et al.*, 2012; Yu *et al.*, 2013). These time-based architectures have some interesting features. For one, they all employ noise shaping but in a very simple and direct manner. Because of their simplicity, they require little power and are easily adapted to advanced CMOS processes. In this section, four types of open-loop approaches for TMΔΣ modulation will be described: (1) VCO-based Open-Loop TMΔΣ modulator, (2) GRO-based Open-Loop TMΔΣ modulator, (3) vernier GRO-Based ΔΣ modulator, and (4) SRO-based ΔΣ modulator.

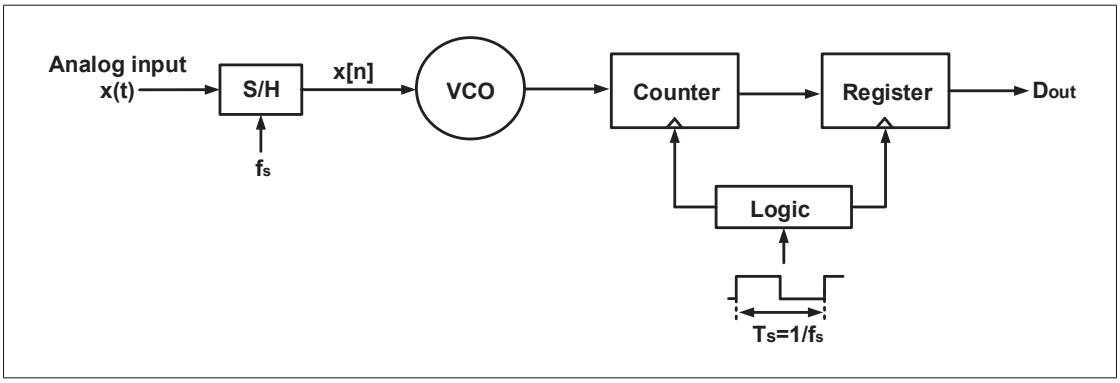


Figure 1.10 VCO-Based Open-Loop ΔΣADC.

1.3.2.1 VCO-Based Open-Loop TMΔΣ Modulator

A VCO-based open-loop ΔΣADC is shown in Figure 1.10, which consists of a front-end S/H stage, followed by a ring-VCO and a counter, register, and some logic (F. Yuan, 2014). Here the output digital count $D_{out}[n]$ represents discrete samples of the input signal of $x[n]$ in some

general form such as

$$D_{out}[n] = a \times x[n] + b \tag{1.15}$$

where a and b are arbitrary coefficients.

The basic principle of this system is that the oscillation frequency of the VCO is set at each sampling instant based on the sampled input value $x[n]$. The counter then counts the number of rising edge transitions associated with the VCO output in the sampling period, T_s. At the end of each sampling phase, the total transition count is latched into the output register and presented as the digital output $D_{out}[n]$. The counter is then reset at the start of the next sampling phase to begin the count all over again.

A timing diagram illustrating the internal action of the VCO-based open-loop ΔΣADC is shown in Figure 1.11, where the input signal and the VCO input and output voltage signals are seen as on an oscilloscope. Also in the plot are the count pulses that correspond to the VCO output crossing the phase threshold of 2π, whereby the total number of count pulses minus one indicates the number of cycles the VCO output completes during the sampling period; we assign this value as the output digital value $D_{out}[n]$.

Also shown in this diagram is the instantaneous frequency and phase of the VCO output as a function of time. During any sampling phase, with the input to the VCO held constant by the input sample $x[n]$, its output will be a clock signal with a specific, but constant, frequency value given by

$$f_{VCO}[n] = K_{VCO} \times x[n] + f_{FR} \tag{1.16}$$

where K_{VCO} represents the voltage-to-frequency gain coefficient expressed in units of Hz/V. f_{FR} represents the free-running oscillation frequency of the VCO expressed in Hz.

The instantaneous VCO frequency $f_{VCO}(t)$ and phase $\Phi_{VCO}(t)$ are related through the derivative operation:

$$f_{VCO}(t) = \frac{1}{2\pi}\frac{d\Phi_{VCO}(t)}{dt} \tag{1.17}$$

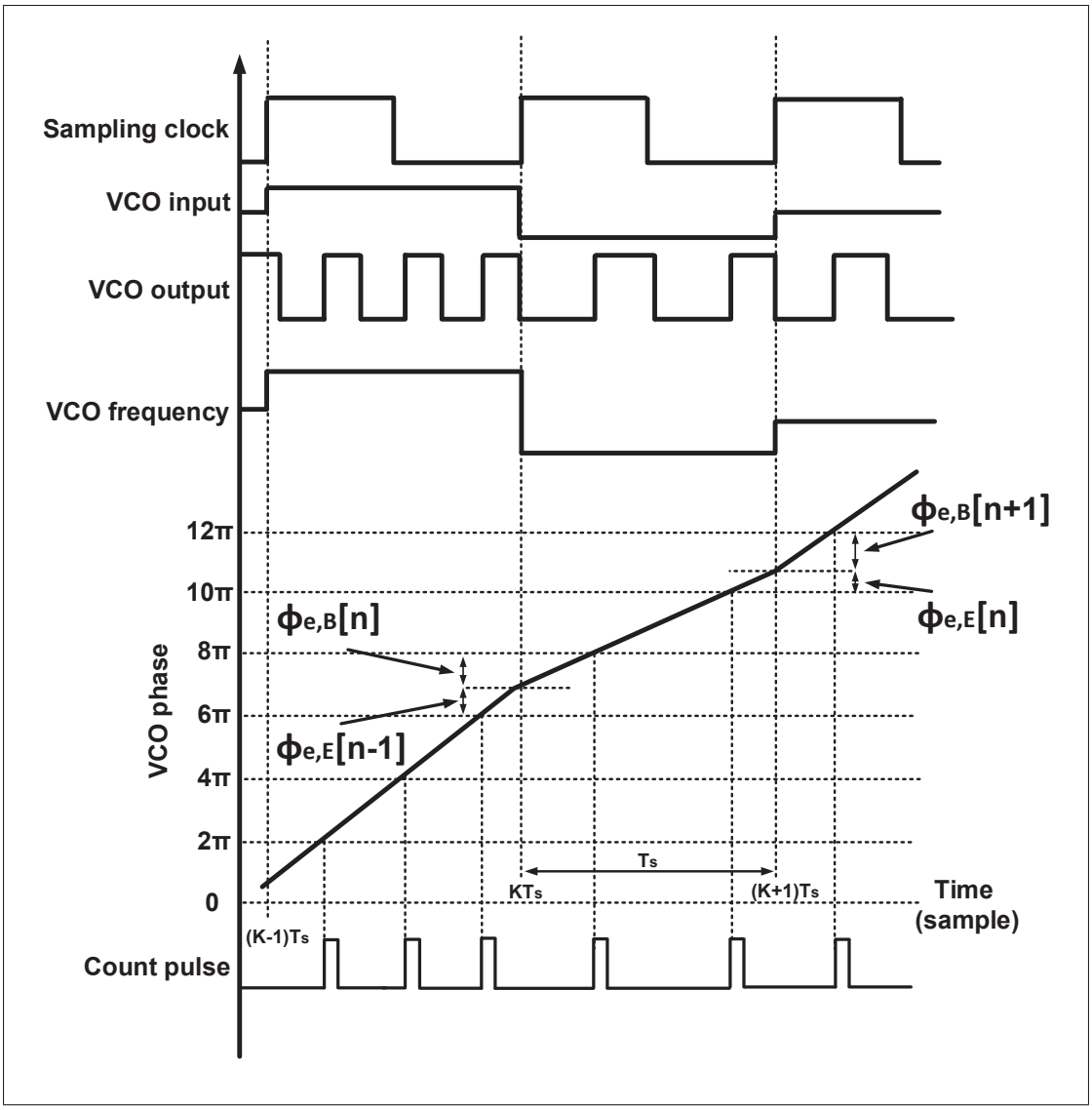


Figure 1.11 Timing diagram for the VCO-based ΔΣADC.

Therefore, the change in the instantaneous phase over the sampling period T_s at any sampling instant can be approximated as

$$\Delta\Phi_{VCO}[n] = 2\pi f_{VCO}[n]T_s \tag{1.18}$$

Substituting (1.18) into the aforementioned equation allows the DT phase change to be written as

$$\Delta\Phi_{VCO}[n] = 2\pi K_{VCO} T_s x[n] + 2\pi f_{FR} T_s \tag{1.19}$$

Referring back to the VCO output phase behavior shown in Figure1.11, one can also write the same phase change $\Delta\Phi_{VCO}[n]$ as a number of full cycles 2π phases changes and a small phase error $\Phi_e[n]$ as follows

$$\Delta\Phi_{VCO}[n] = 2\pi D_{out}[n] + \Phi_e[n] \tag{1.20}$$

Equating (1.21) and (1.22) leads to

$$D_{out}[n] = K_{VCO} T_s x[n] + f_{FR} T_s - \frac{1}{2\pi}\phi_e[n] \tag{1.21}$$

The phase error $\phi_e[n]$ at any sampling instant consists of two components: a start and stop phase error, or what we shall refer to in this chapter as the begin and end phase error. To distinguish each component from one another, we shall denote the start or begin phase error with an additional subscript B appended to the phase error term and write it as $\phi_{e,B}[n]$. Correspondingly, the stop or end phase error will be described with an additional subscript E and write $\phi_{e,E}[n]$. These phase error terms can be seen in Figure 1.11, allowing one to write during any sampling instant

$$\phi_e[n] = \phi_{e,B}[n] + \phi_{e,E}[n] \tag{1.22}$$

In addition, we also observe from the phase plot that the sum of the stop/end phase error during the sampling instant $[n-1]$ and the start/begin phase error at sampling instant $[n]$ must equal 2π. Hence, we can write

$$\phi_{e,E}[n-1] + \phi_{e,B}[n] = 2\pi \tag{1.23}$$

Substituting this back into the total phase error expression of (1.24) leads to

$$\Phi_e[n] = 2\pi + \phi_{e,E}[n] - \phi_{e,E}[n-1] \tag{1.24}$$

Here we see how the total phase error $\phi_e[n]$ depends on the difference in the stop or end phase errors at adjacent sampling instants. This should remind the reader of the difference equations related to $\Delta\Sigma$ modulation and the corresponding noise-shaping effect.

Armed with earlier result, the output digital code $D_{out}[n]$ can be rewritten as

$$D_{out}[n] = K_{VCO}T_s x[n] + f_{FR}T_s - 1 - \frac{1}{2\pi}\left(\phi_{e,E}[n] - \phi_{e,E}[n-1]\right) \tag{1.25}$$

If we define the reference count $D_{out,Ref}$, at $x[n] = 0$, then

$$D_{out,Ref} = f_{FR}T_s - 1 \tag{1.26}$$

and the output count relative to the reference can be written as

$$\Delta D_{out}[n] = D_{out}[n] - D_{out,ref} = K_{VCO}T_s x[n] - \frac{1}{2\pi}\left(\phi_{e,E}[n] - \phi_{e,E}[n-1]\right) \tag{1.27}$$

The corresponding z-transform of the calibrated output count becomes

$$\Delta D_{out}(z) = K_{VCO}T_s X(z) - \frac{1}{2\pi}\left(1 - z^{-1}\right)\Phi_{e,E}(z) \tag{1.28}$$

where $\Phi_{e,B}(z)$ is the z-transform of the forward phase error sequence, $\phi_{e,E}[n]$. The aforementioned equation reveals the first-order noise shaping, as the phase error term is weighted by the frequency dependent term, $(1 - z^{-1})$.

As the step size of the counter/quantizer is 2π, the PSD of the forward phase error sequence in rad^2/Hz can be estimated as

$$N_{\Phi_{e,F}} = \frac{2\pi^2}{3f_s} \tag{1.29}$$

The phase error spread is inversely proportional to the sampling frequency f_s. Therefore, to maximize the noise-shaping benefit, the bandwidth of the incoming signal $x(t)$ should be small in comparison to f_s.

1.3.2.1.1 Improving the Nonlinear Behavior

A major issue associated with the VCO-based ΔΣADC design is its nonlinear operation. While the VCO was assumed to be linear with respect to its voltage input, a more accurate representation is to assume the VCO has the following transfer characteristic

$$f_{VCO}[n] = f_{FR} + K_{VCO,1}x[n] + K_{VCO,2}x^2[n] + K_{VCO,3}x^3[n] + ... \tag{1.30}$$

where the coefficients,$K_{VCO,1}$,..., $K_{VCO,3}$,... represent the terms of the power series expansion around the operating point of the input–output behavior of the VCO. Substituting the aforementioned equation into (1.21), one can write the output phase-difference $\Delta\phi_{VCO}[n]$ as

$$\Delta\phi_{VCO}[n] = 2\pi f_{FR}T_s + 2\pi T_s K_{VCO,1}x[n] + 2\pi T_s K_{VCO,2}x^2[n] + 2\pi T_s K_{VCO,3}x^3[n] + ... \tag{1.31}$$

By transforming the input $x[n]$ into a positive and negative version and applying each one to a separate VCO leads to the following two output phase difference terms, denoted as $\Delta\phi^{+}_{VCO}[n]$ and $\Delta\phi^{-}_{VCO}[n]$, one for the positive input as

$$\Delta\phi^{+}_{VCO}[n] = 2\pi f_{FR}T_s + 2\pi T_s K_{VCO,1}x[n] + 2\pi T_s K_{VCO,2}x^2[n] + 2\pi T_s K_{VCO,3}x^3[n] + ... \tag{1.32}$$

and the other for the negative input as

$$\Delta\phi^{-}_{VCO}[n] = 2\pi f_{FR}T_s + 2\pi T_s K_{VCO,1}(-x[n]) + 2\pi T_s K_{VCO,2}(-x[n])^2 + 2\pi T_s K_{VCO,3}(-x[n])^3 + ... \tag{1.33}$$

Adding a stage that takes the difference in these two phases, that is,

$$\Delta\phi_{VCO}[n] = \Delta\phi^{+}_{VCO}[n] - \Delta\phi^{-}_{VCO}[n] \tag{1.34}$$

the corresponding output phase difference depends only on the odd-order terms, thereby reducing the overall distortion level, that is,

$$\Delta\phi_{VCO}[n] = 0 + 2 \times 2\pi T_s K_{VCO,1} x[n] + 0 + 2 \times 2\pi T_s K_{VCO,3} x^3[n] + \ldots \quad (1.35)$$

Counting the corresponding 2π phase changes, one obtains the system shown in Figure 1.12 digital count value $D_{out}[n]$ becomes

$$D_{out}[n] = 2 \times K_{VCO,1} T_s x[n] + 2 \times K_{VCO,3} T_s x^3[n] + f_{FR} T_s - 1 - \frac{1}{2\pi}\left(\phi_{e,E}[n] - \phi_{e,E}[n-1]\right) \quad (1.36)$$

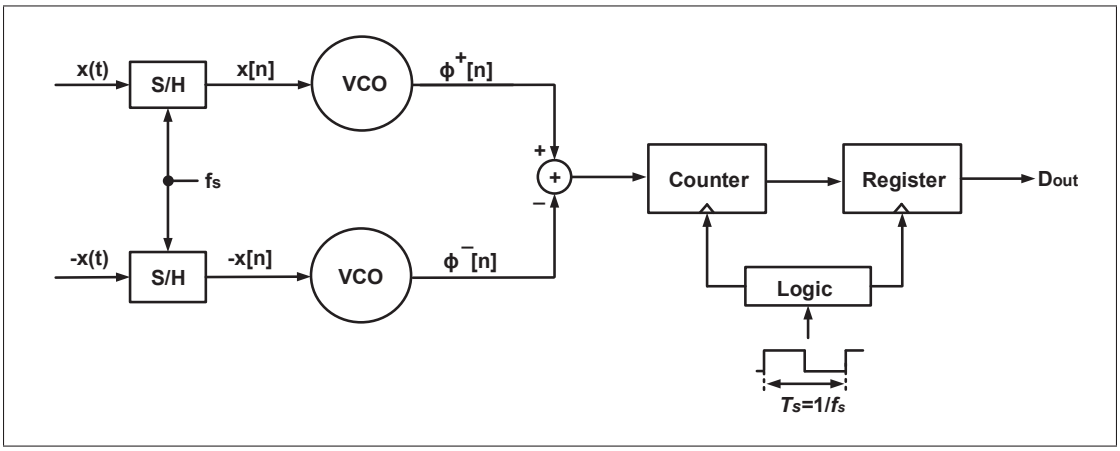
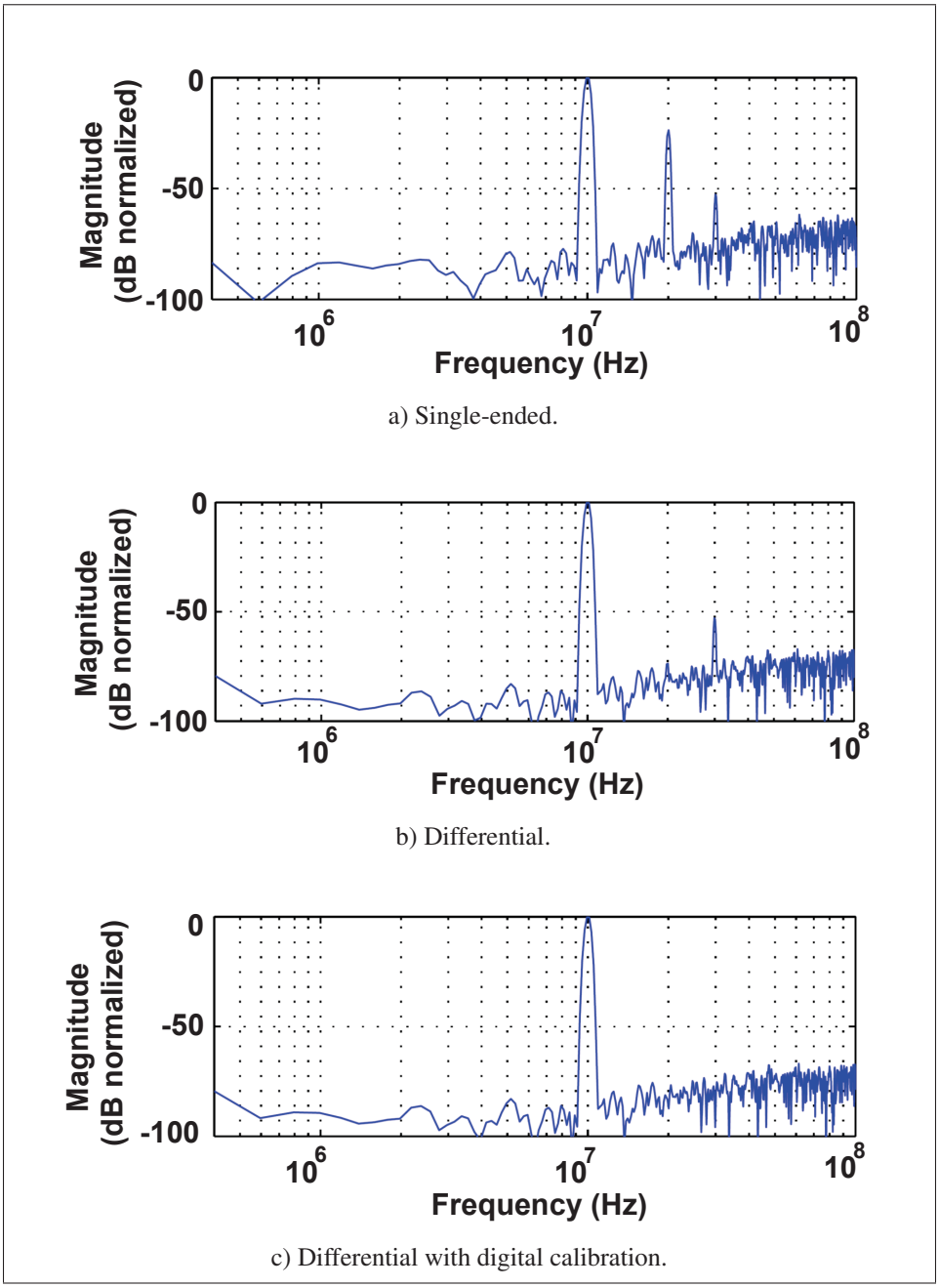


Figure 1.12 Differential configuration of VCO-based ΔΣADC.

Further balancing in the signal path can be performed with digital calibration techniques implemented in the logic block of Figure 1.12. Figure 1.13 displays the output PSD for a VCO-based ΔΣ modulator implemented with both single-ended and differential configurations, with and without digital calibration (Daniels *et al.*, 2010). As is evident from Figure 1.13, the differential implementation reduced the even-order distortion terms below the noise level of the ΔΣ modulator, while the digital calibration further reduces the third-order distortion component.

A main drawback of this approach is of course related to the increase in hardware and power, as two parallel VCOs and a phase differencing circuit are required.



a) Single-ended.

b) Differential.

c) Differential with digital calibration.

Figure 1.13 Measurement results of a VCO-based ΔΣADC.

1.3.2.1.2 Increasing the Maximum Sampling Rate, f_s

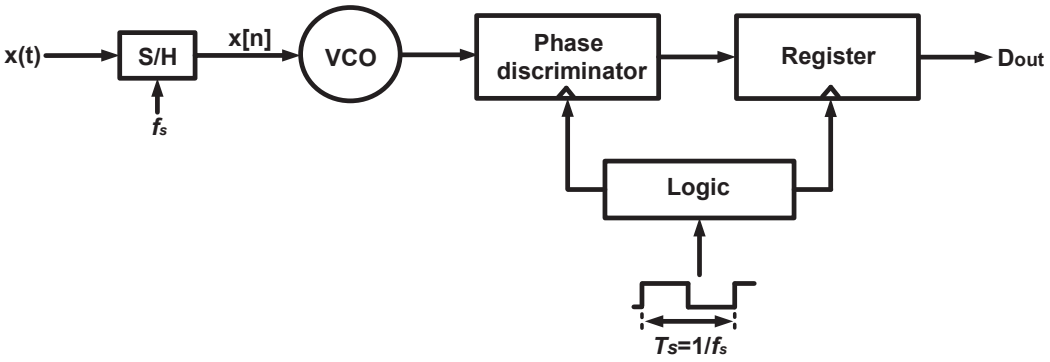
The basic principle behind a VCO-based ΔΣ modulator is that an input signal $x[n]$ is encoded into the frequency of the VCO output, $f_{VCO}[n]$. By measuring the number of cycles that the VCO output completes during the sampling period T_s allows one to estimate the frequency of the VCO and hence to recover the input samples. As the output of the VCO completes $2\pi D_{out}[n]$ radians of phase change during the sampling period, T_s, the discrete-time VCO frequency is estimated from

$$f_{VCO}[n] = \frac{1}{2\pi}\frac{\Delta\phi_{VCO}[n]}{T_s} = \frac{D_{out}[n]}{T_s} \tag{1.37}$$

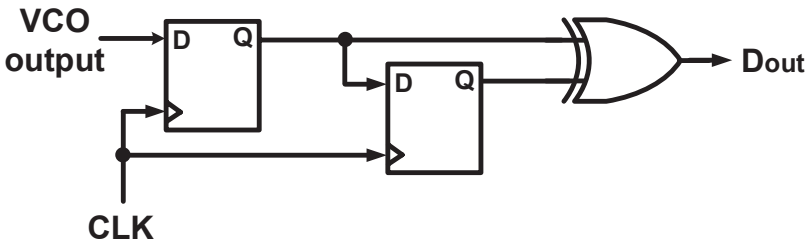
The ultimate speed of this operation depends on the speed at which the counter can count. In practice, this limits the sampling rate of the VCO-based ΔΣ modulator to relative low-frequency operation. Instead, one can use a phase discriminator and estimate a change in the VCO output phase in a shorter time, thereby increasing the maximum sampling rate of the VCO-based ΔΣ modulator. Figure 1.14(a) illustrates the block diagram of this arrangement. It is essentially the same as the implementation in Figure 1.10, except that a phase discriminator circuit shown in Figure 1.14(b) replaces the counter. The phase discriminator generates a pulse with width T_d that, when normalized by the sampling period T_s, is proportional to the VCO output frequency. The phase discriminator is made from two DFFs and an XOR gate. As the propagation delay of this logic gate combination is extremely short in comparison to that of an N-bit counter, this circuit can operate at much higher sampling rates than a counter-phase discriminator circuit.

1.3.2.2 GRO-Based Open-Loop TM ΔΣ Modulators

A GRO-based TMΔΣ modulator quantizes a time-difference interval, for example, time between a start and stop edge transition, rather than some input voltage. Before a discussion about GRO-based TMΔΣ modulator, consider the ring oscillator-based (RO-based) TDC (M.Z. Straayer and M.H. Perrott, 2009) shown in Figure 1.15(a). The RO-based TDC approach consists of four blocks: a ring oscillator, counter, register, and some logic gates. The operation



a) Block diagram.

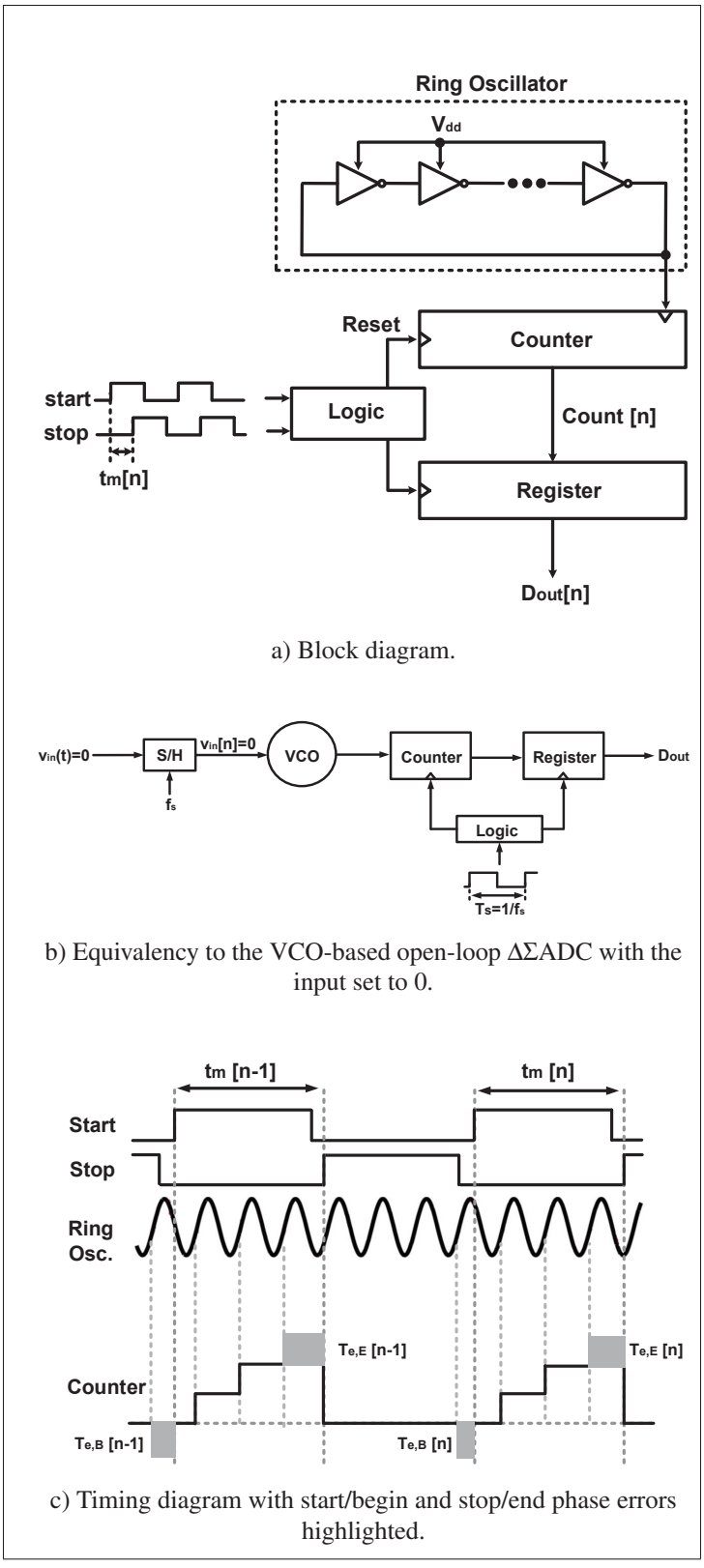


b) Phase discriminator circuit.

Figure 1.14 Using a phase discriminator instead of a counter to extract the VCO phase changes.

of this design is to count the number of clock cycles of the ring oscillator between the time interval defined by the start and stop signals. Once again, the output count will be denoted as $D_{out}[n]$ and the input time-difference interval as $t_m[n]$. This design is essentially identical to that described for VCO-based open-loop ΔΣADC shown in Figure 1.10 with input signal $x[n] = 0$ as depicted in Figure 1.15(b); albeit, there is a time-lag between the instant a count value is ready and the next input sample can be ready for conversion.

Following a similar mathematical development as for the VCO-based open-loop ΔΣADC, consider that the ring oscillator oscillates at some free-running frequency f_{FR}. As the instantaneous frequency of the ring oscillator output is equal to the derivative of the phase, the change



a) Block diagram.

b) Equivalency to the VCO-based open-loop ΔΣADC with the input set to 0.

c) Timing diagram with start/begin and stop/end phase errors highlighted.

Figure 1.15 RO-based TDC.

in phase output over the duration of the start-stop interval $t_m[n]$ can be described as

$$\Delta\phi_{VCO}[n] = 2\pi f_{FR} t_m[n] \tag{1.38}$$

This phase change corresponds to the 2π multiples of the count $D_{out}[n]$, with some quantization error $\phi_e[n]$, which is equivalent to the sum of a start/begin and stop/end phase error component as shown in Figure 1.16, that is, $\phi_e[n] = \phi_{e,B}[n] + \phi_{e,E}[n]$. However, as derived earlier, $\phi_{e,B}[n] + \phi_{e,E}[n-1] = 2\pi$ due to the modulo phase operation of the counter, allowing one to write

$$\Delta\phi_{VCO}[n] = 2\pi D_{out}[n] + (2\pi + \phi_{e,E}[n] - \phi_{e,E}[n-1]) \tag{1.39}$$

Combining (1.40) and (1.41),

$$D_{out}[n] = f_{FR} t_m[n] - 1 - \frac{1}{2\pi}(\phi_{e,E}[n] - \phi_{e,E}[n-1]) \tag{1.40}$$

If we define the reference count $D_{out,Ref}$ for some input time-difference reference condition, say $t_{m,Ref}$, then

$$D_{out,Ref} = f_{FR} t_{m,Ref} - 1 \tag{1.41}$$

Subtracting (1.43) from (1.42), one arrives at the change in the output count relative to some reference pulse width, that is,

$$\Delta D_{out}[n] = D_{out}[n] - D_{out,Ref} = f_{FR}\left(t_m[n] - t_{m,Ref}\right) - \frac{1}{2\pi}(\phi_{e,E}[n] - \phi_{e,E}[n-1]) \tag{1.42}$$

The corresponding z-transform of the calibrated output count becomes

$$\Delta D_{out}(z) = K_{VCO} T_s \Delta T_m(z) - \frac{1}{2\pi}\left(1 - z^{-1}\right)\Phi_{e,E}(z) \tag{1.43}$$

where

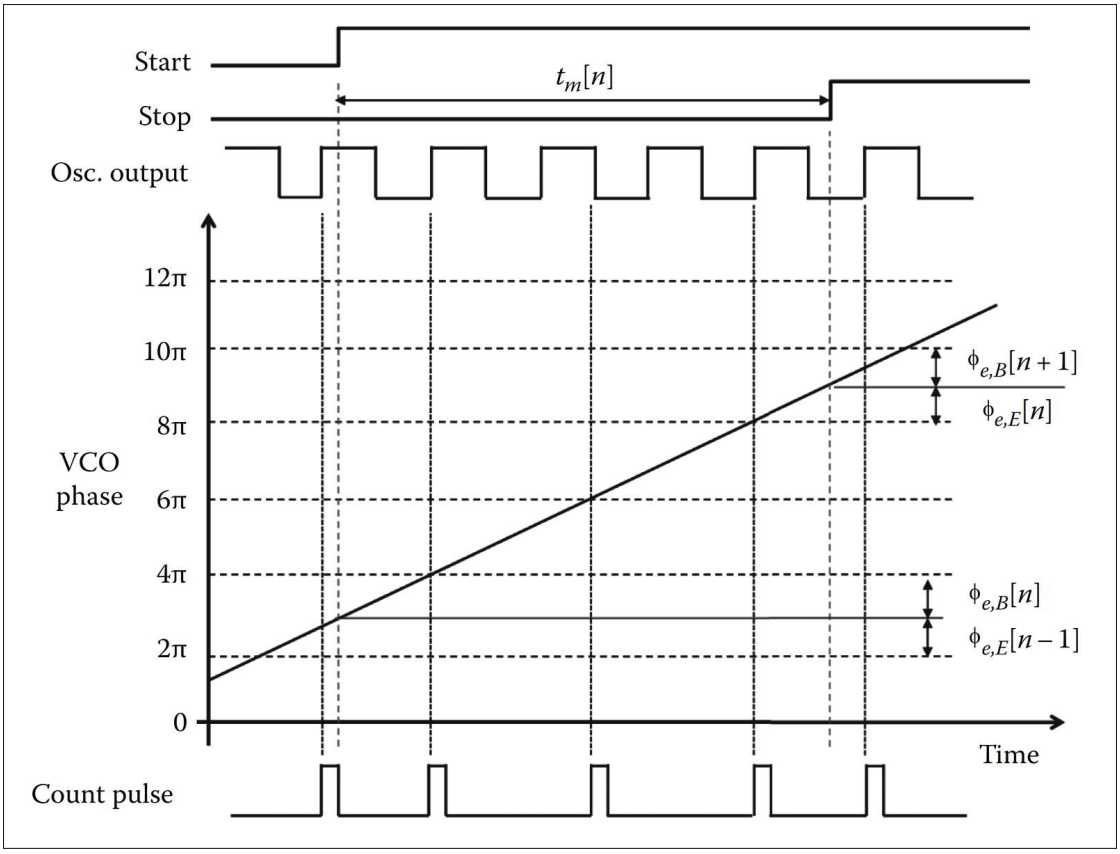


Figure 1.16 Timing diagram of the ring oscillator–based TDC with start/begin and stop/end phase errors highlighted.

$\Delta T_m(z)$ represents the z-transform of the input time change.

$\Phi_{e,E}(z)$ is the z-transform of the stop or end phase error sequence, $\phi_{e,E}[n]$.

Once again, we observe that the quantization error is noise shaped by the factor $\left(1-z^{-1}\right)$. As the step size of the counter/quantizer is again 2π, the PSD of the end phase error sequence in rad^2/Hz is identical to that described by (1.31).

The main reason for the quantization error reduction is that start/begin and stop/end phase errors are highly correlated, so that their combined sum is reduced with averaging. In practice, this is not the case with an RO-based TMΔΣ modulator. Rather, some time must be allotted to account for the time to make a decision and to read and write the data into the appropriate registers, and make sure the circuit is ready for next sampling phase. As a result, the phase

of the oscillator will have changed before the start of the next sampling phase, resulting in a misalignment in the start/begin and stop/end quantization errors.

The GRO-based TMΔΣ modulator approach (M.Z. Straayer and M.H. Perrott, 2009) enables the phase of the ring oscillator to be reset (i.e., through a gated operation) to the value it had at the end of the previous sampling instant and restored some time later so that the stop or end quantization error of the previous time sample is the same as the start/begin quantization error of the next time sample, as illustrated in Figure 1.15(c). It does this by disabling the ring oscillator for a complete integer number of clock cycles from the last sampling instant.

1.3.2.3 Vernier GRO-Based (VGRO) TM ΔΣADC

Generating multiphase signals, for example, ring oscillator, with high resolution is at the core of many TMΔΣ modulator approaches. The simplest method is an inverter chain, but it consumes a great deal of power and has a time resolution equal to twice the propagation delay of a single logic inverter gate. A second approach is a VCO in cascade with a phase interpolator circuit. Such a circuit has a higher resolution than an inverter chain but is sensitive to PVT variations as the phase interpolator operates in an open-loop fashion. A third approach is a phased-coupled VCO used in a phase-locked loop (PLL) negative feedback configuration. This approach is known to have the finest phase resolution and is insensitive to PVT effects. These three methods are well known, so we will defer the reader to visit any graduate level reference on analog design for more details.

A fourth method, which has only recently been introduced, involves a coupled ring oscillator configuration (CRO) (Matsumoto *et al.*, 2008). This design involves the use of multiple rings of inverter chains and an outer ring of NMOS switches as depicted in Figure 1.17. A pseudospherical co-ordinate system is used to describe a particular inverter location in the various rings in terms of an n,m co-ordinate. Here we see that there are seven inner rings of inverters and that each ring contains nine inverters in cascade. The length of these rings, denoted as N_{inv} and the number of rings N_{rings}, can be made arbitrary. This design has better phase reso-

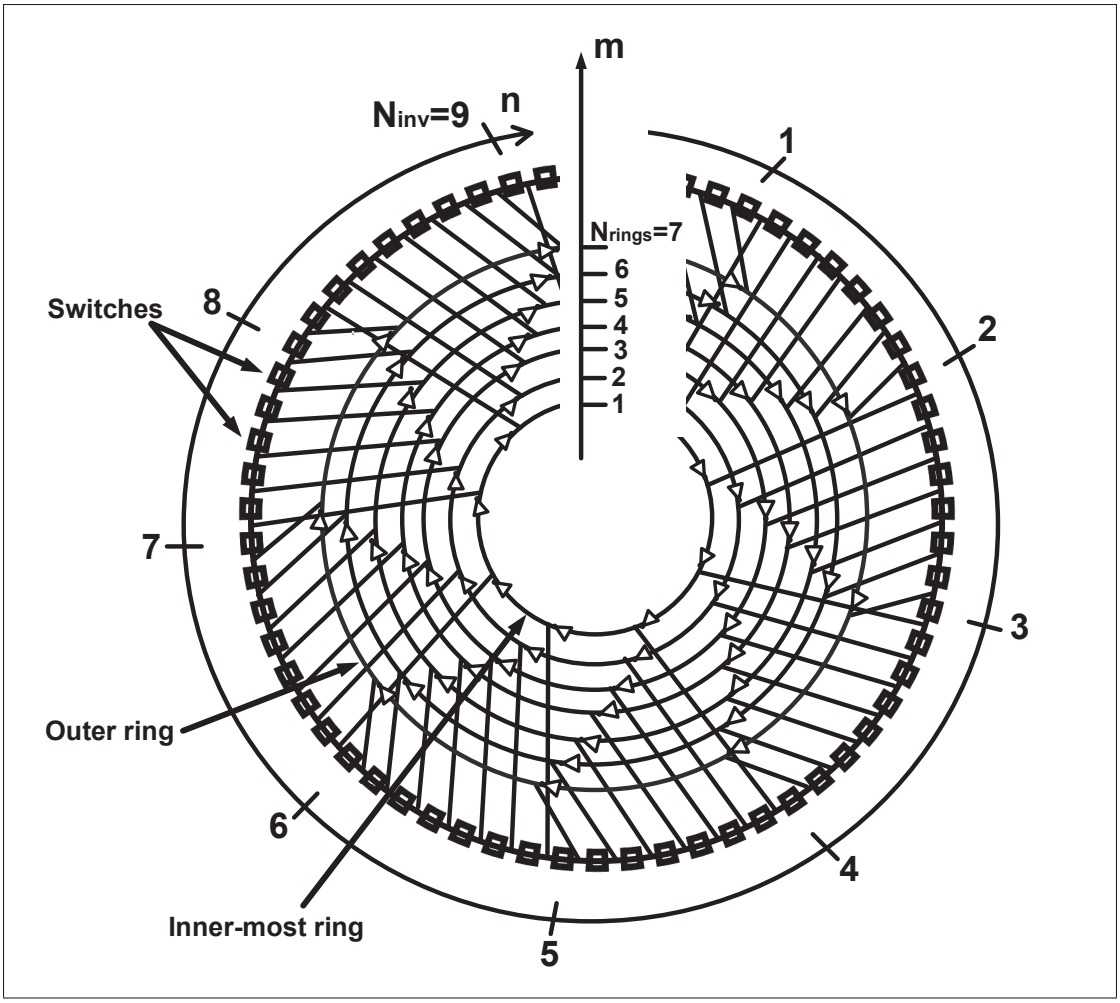


Figure 1.17 General implementation arrangement of a multiphase coupled oscillator configuration.

lution than a single ring of inverter chains involving N_{inv} and an open-loop VCO with a phase interpolator but exhibits a power consumption just a little better than a single inverter chain. The basic principle of a CRO is that two different types of oscillation modes bind their phases together. For the most part, the outer-most or main ring ($m = N_{rings}$) determines the overall oscillation frequency, whereas the other rings (m=1, ..., N_{rings}-1) couple with the phases of the main ring. The phase difference $\Delta\phi$ between any two inverters located in the spherical plane

with co-ordinates (n_1,m_1) and (n_2,$m2$) is given by the following expression:

$$\Delta\phi\,(n_2-n_1,\,m_2-m_1)=(m_2-m_1)\left(\pi+\frac{2\pi}{2N_{inv}N_{rings}}\right)+(n_2-n_1)\left(\pi+\frac{2\pi}{2N_{inv}}\right)\ mod\ 2\pi \tag{1.44}$$

In comparison, a single ring oscillator with N_{inv} inverters in cascade would have a phase difference between two inverters (n_2-n_1) apart from that given by

$$\Delta\phi=(n_2-n_1)\left(\frac{2\pi}{2N_{inv}}\right) \tag{1.45}$$

Another approach to realize a single-loop ring oscillator with a timing resolution less than a unit gate delay is through the application of a negative delay element. Consider the basic CMOS inverter circuit shown in Figure 1.18(a). Here a negative delay is inserted in series with the gate of the PMOS transistor so that this transistor experiences the input signal earlier than the NMOS transistor (Lee *et al.*, 1997). As a result, the net delay of this gate can be made less than a conventional CMOS inverter. This is illustrated in the timing diagrams of Figure 1.18(b). The top plot corresponds to the conventional timing for a single inverter circuit. The timing plot below this illustrates the timing skew introduced by the addition of a negative delay element. The following two plots are for the output signal for the conventional gate and the delay-reduced gate circuit. Different delays have been be achieved by inserting different negative timing skews (Mohan *et al.*, 2005; Straayer *et al.*, 2009).

The final method that we will describe here for increasing the timing resolution of a multiphase generator is the vernier method. The basic principle of the vernier delay line is to use two uncoupled ring oscillators, one oscillating slightly faster than the other by tuning the individual delay units to two separate delays, τ_F and τ_S, as shown in Figure 1.19(a). The instantaneous phase behavior of these two oscillators is displayed modulo 2π as shown in Figure 1.19(b). Here one can see how the "fast" oscillator phase behavior is phased aligned with the "slow" oscillator phase response at the very beginning, then with increasing time the "fast" oscillator phase moves ahead of the "slow" oscillator until the two are again phase aligned (at the end of the time sequence). The smallest separation time or resolution between the two phase responses

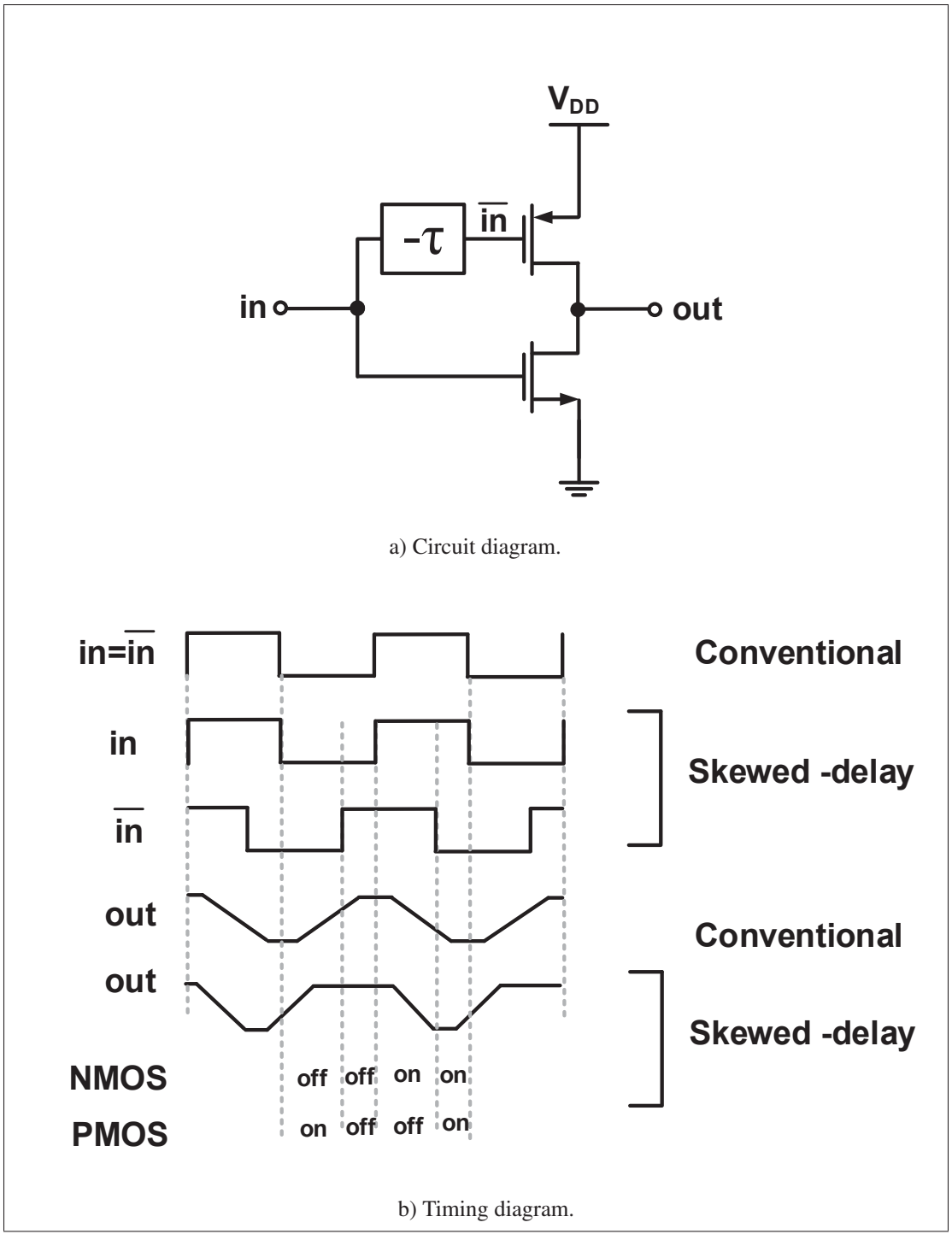
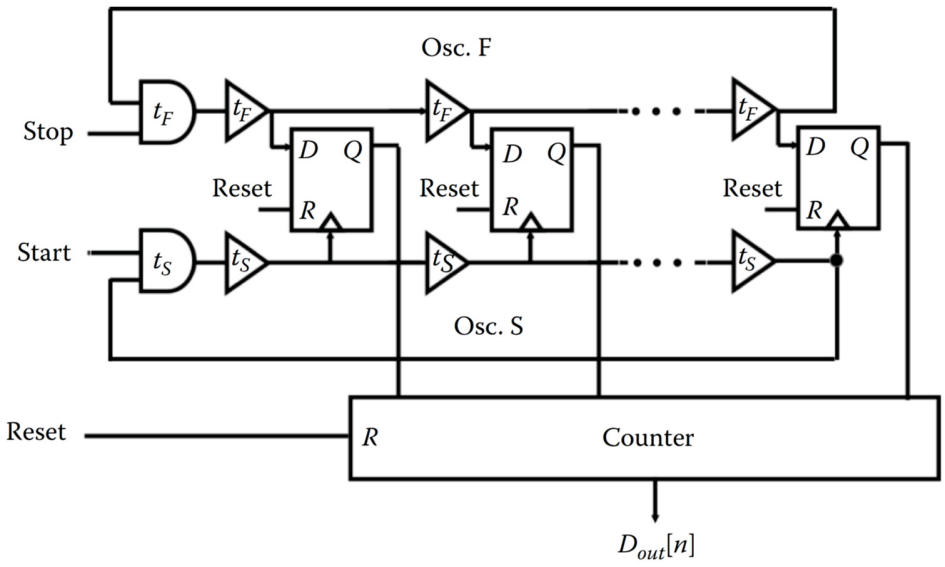


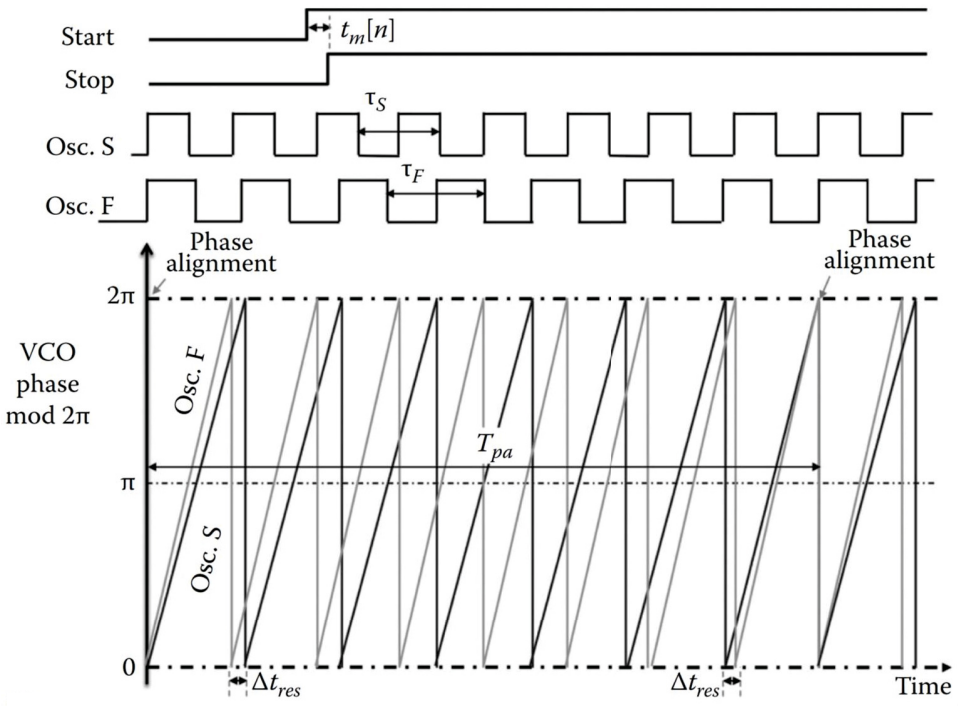
Figure 1.18 Negative-skewed delay cell.

when they are both equal to 2π is Δt_{res} and is given by

$$\Delta t_{res} = \tau_S - \tau_F \tag{1.46}$$



a) Block diagram



b) A corresponding timing diagram of a fast and slow oscillator with a fixed time delay

Figure 1.19 Vernier GRO TDC.

Correspondingly, the relative phase change in this time step is

$$\Delta\phi_{res} = 2\pi\left(\frac{\tau_S - \tau_F}{\tau_S}\right) \tag{1.47}$$

Clearly, the time and phase resolution can be made quite small by simply setting the delays in each ring oscillator to be very close to one another, not equal. Generally, this is done by selecting equal inverter delays, but the "slow" ring oscillator will be constructed with one additional delay element.

A flash-type TDC (i.e., one without noise-shaping) can be constructed using the vernier ring oscillator approach. The basic operation is to apply a start and stop signal to the TDC input such that the initial delay between the phase of the two oscillators equals this time-difference $t_m[n]$. As the phase of the fast oscillator rapidly cycles to catch up with the phase of the slow oscillator, a point is reached when the phase of the two oscillators is phase aligned. At this point, a number of the DFFs have been set to logic one indicating that the D input signal leads its clock input signal. A count of the number of 1s is made and the corresponding value is captured as the output $D_{out}[n]$.

One additional measurement can be made to deduce the resolution of the TDC. By measuring the time duration between adjacent phase alignment events, denoted by T_{pa}, and the total number of 1s captured by the DFFs that occurred in this time, denoted by $D_{out,ea}$, an accurate estimate of the time resolution Δt_{res} can be derived without having to use a measuring instrument with an extremely high resolution (but requires high accuracy, nonetheless), that is,

$$\Delta t_{res} = \frac{\Delta T_{pa}}{D_{out,ea}} \tag{1.48}$$

Hence, the input time difference $t_m[n]$ can then be expressed as

$$t_m[n] = \Delta t_{res} D_{out}[n] \tag{1.49}$$

Conversely, one can write the count $D_{out}[n]$ with a time quantization error included as follows

$$D_{out}[n] = \frac{1}{\Delta t_{res}} t_m[n] + \Delta t_e[n] \tag{1.50}$$

Here the time quantization error is subject to a start/begin and stop/end quantization effect, that is,

$$\Delta t_e[n] = \Delta t_{e,B}[n] + \Delta t_{e,E}[n] \tag{1.51}$$

where each time error component is bounded in magnitude by Δt_{res}. As conversion process is reset after each phase of TDC operation, there is no coupling between the start/begin and stop/end errors between sampling instants, as was seen with the other TM $\Delta\Sigma$ modulators. However, by altering the structure of the flash-type TDC such that the internal states of the two oscillators are stored, the phase difference can be read back during the next conversion cycle, thereby coupling the time quantization errors. This approach was adopted in the vernier GRO introduced in (Lu *et al.*, 2012) resulting in a digital output with first-order noise described by

$$D_{out}[n] = \frac{1}{\Delta t_{res}} t_m[n] + \Delta t_{e,E}[n] - \Delta t_{e,E}[n-1] \tag{1.52}$$

While the vernier technique may appear to considerably improve the TDC resolution, the mismatch between the delay lines severely limits the resolution in practice. Also, a wide measurement range requires many more delay cells compared with a flash TDC with a single oscillator or delay, making it impractical in high-resolution wide-range applications. Therefore, unless a small range is allowed, vernier TDC must be combined with other circuit techniques to improve resolution without significantly increasing power and area. One such approach is based on component-invariant vernier delay line technique. Here the two delay lines are replaced by two gated oscillators, thereby eliminating the matching effort between adjacent delay line cells (Chan *et al.*, 2002; Chan *et al.*, 2004; Roberts *et al.*, 2005).

1.3.2.4 Switched-Ring Oscillator-Based TM ΔΣADC

A GRO-based ADC with first-order noise shaping requires the phase of the oscillator to be preserved so that the start/begin and stop/end quantization errors are coupled. However, due to various charge dynamic mechanisms, errors occur with the charge stored on the parasitic capacitors associated with the delay elements. These manifest themselves as leakages, skew, and dead-band effects (Yu *et al.*, 2013; Elshazly *et al.*, 2014).

To address this limitation, the SRO-based TMΔΣADC was proposed in (Elshazly *et al.*, 2014). Leveraging oversampling and noise shaping, the proposed SRO-TDC achieves high resolution without the need for calibration. Ring oscillators are switched between two frequencies to achieve noise shaping of the quantization error in an open-loop manner. By decoupling the sampling clock and input carrier frequencies, the SRO-based TMΔΣADC is capable of operating at high OSRs, a feature that did not exist in any of the TDCs presented earlier.

A block diagram of the proposed approach is depicted in Figure 1.20. Here the input time difference signal is converted into a continuous-time pulse-modulated signal and applied to the control input of two voltage-controlled ring oscillators.

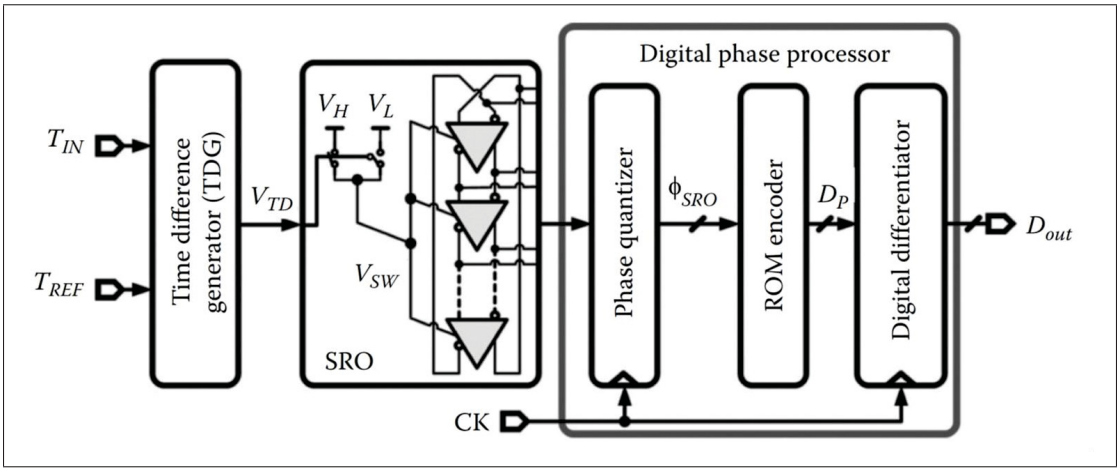


Figure 1.20 Block diagram of SRO-based TM ΔΣADC.

As the pulse-modulated signal is set between two voltage levels, the oscillation frequency of each ring oscillator is set at two different frequencies; albeit for a time duration established by the pulse width of the incoming signal, $t_m[n]$, and the other to reestablish the initial phase of the next conversion cycle—similar in principle to the GRO approach but with a very different implementation (see Figure 1.15(c)). A timing diagram illustrating the VCO input and output behavior is shown in Figure 1.21. Note that the start/begin and stop/end phase quantization errors are arranged to be equal. The output of SRO block is fed to a phase quantizer to determine the output digital value, in much the same way that was done for the other ΔΣADCs described earlier. A ROM encoder and differentiator blocks are responsible for converting the output digital value from the quantize value to its final digital representation.

1.4 High-order TM ΔΣ Modulators

High-order ΔΣ modulators make use of greater amounts of quantization noise history to improve its overall operation. However, high-order ΔΣ modulators come with a higher cost in hardware complexity and silicon area footprint, loop instability, and power consumption. This section provides a brief review of several high-order TMΔΣ modulator designs.

1.4.1 VCO-Based Closed-Loop TM ΔΣ Modulator

In Section 1.2.1, a description of an open-loop VCO-based ΔΣADC was described. One of the main drawbacks to this technique was that it was quite nonlinear. While a method of compensation was proposed based on the cancellation of even-order harmonic terms, an even better approach is to use the VCO-based ADC of Figure 1.10 as a multibit quantizer in a feedback configuration (Iwata *et al.*, 1999; Straayer *et al.*, 2008; Reddy *et al.*, 2012) as shown in Figure 1.22. Here a narrow-band CT loop filter with high DC-gain is used, together with a multibit DAC in the feedback path of the ΔΣ modulator. The loop filter is used to establish the STF and NTF of the overall ΔΣ modulator, as described previously in Section 1.2.1. High-order modulators can be realized by the appropriate selection of the filter order and frequency characteristics. As the VCO-based ΔΣ modulator is now placed in the feed-forward path of a

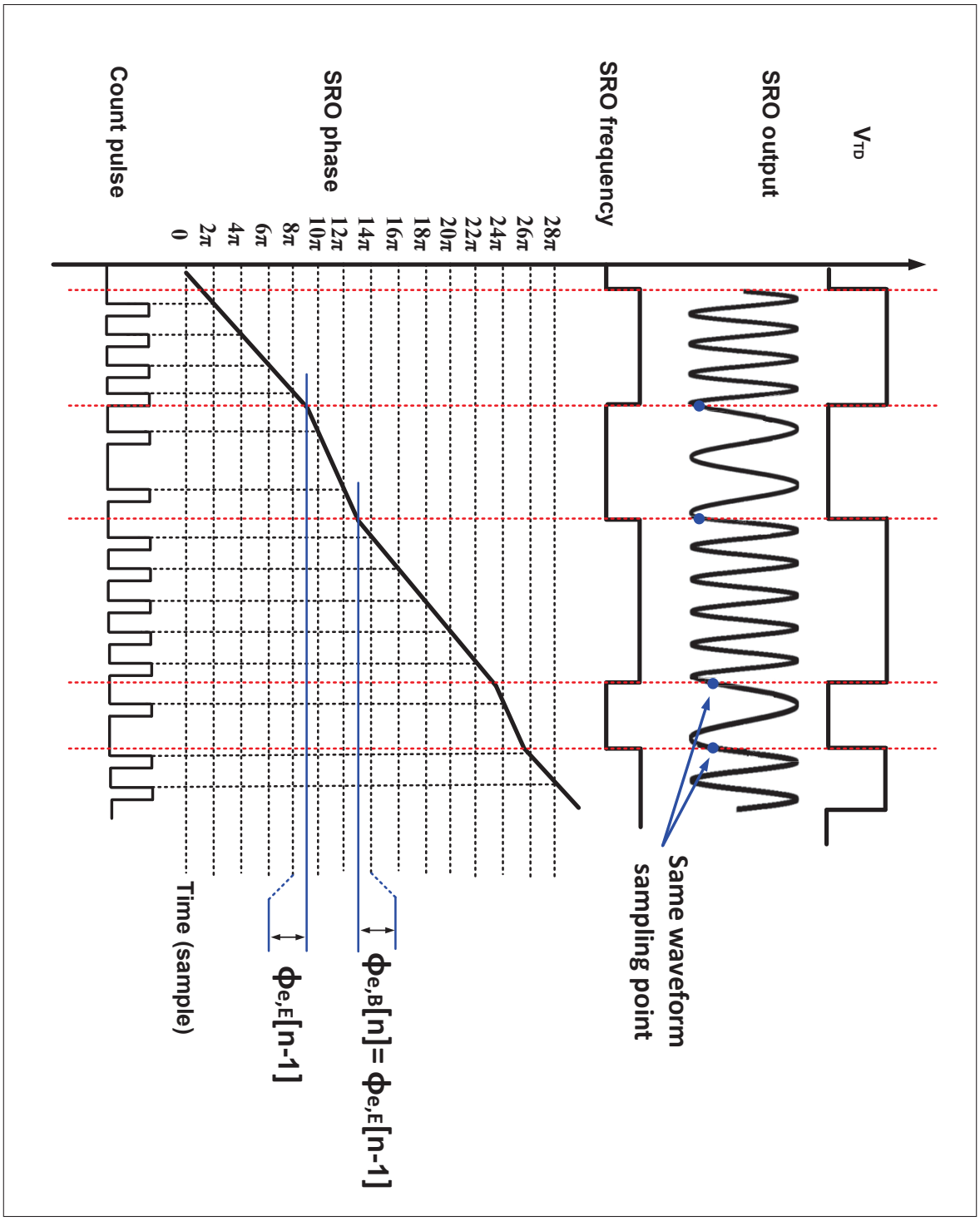


Figure 1.21 Illustrating the timing diagram for the SRO-based ΔΣADC and how the start/begin and stop/end phase errors are made equal.

negative feedback configuration, the nonlinearities of the quantizer are suppressed and made inconsequential.

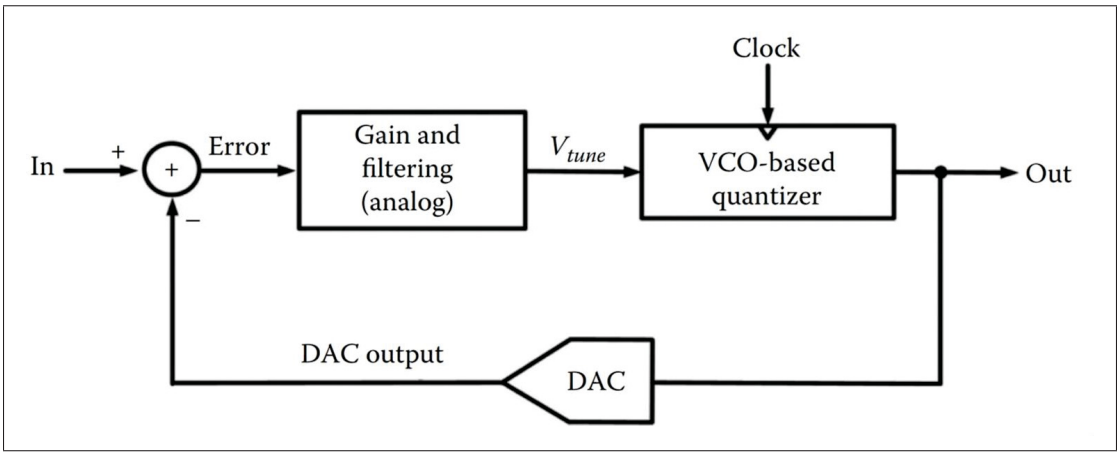


Figure 1.22 Block diagram of VCOΔΣADC used in a closed-loop configuration.

An alternative realization is one that interchanges the sequence of the quantizer and loop filter of Figure 1.22 to that shown in Figure 1.23. Here the loop filter is realized using a digital filter. This realization is referred to as a VCO-based ΔΣ modulator with a tracking-loop quantizer (Colodro *et al.*, 2014). The main goal of this work is to minimize the input signal range at input to the VCO in order to restrict the output frequencies to a very narrow frequency range, and in turn, reduce the level of distortion at its output. A simulation of the proposed approach was performed in (Colodro *et al.*, 2014) and compared to the VCO-based open-loop ΔΣ modulator architecture shown in Figure 1.10. In this simulation, the K_{VCO} coefficient was set to 0.95×33 MHz/V and the nonlinearity of VCO was modeled using a hyperbolic tangent function $tanh(v)$. The simulations results are shown in Figure 1.24. The top plot illustrates the PSD for open-loop ΔΣ modulator architecture and the bottom plot corresponds to the PSD for the proposed closed-loop ΔΣ modulator architecture. The results reveal about 30 dB improvement in the SNDR with the proposed feedback approach. Experimental results have yet to confirm the validity of this approach and any unforeseen practical issues.

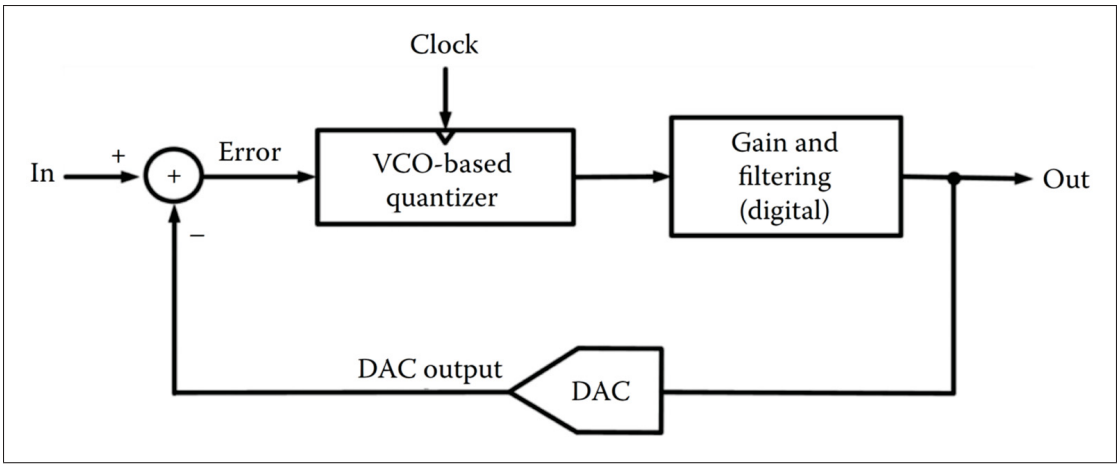
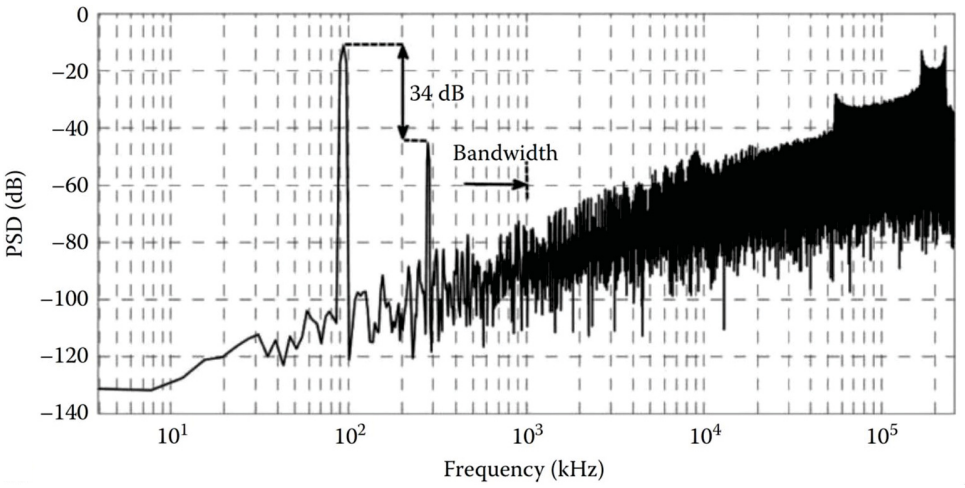


Figure 1.23 TM VCO-based ΔΣ with tracking-loop quantizer.

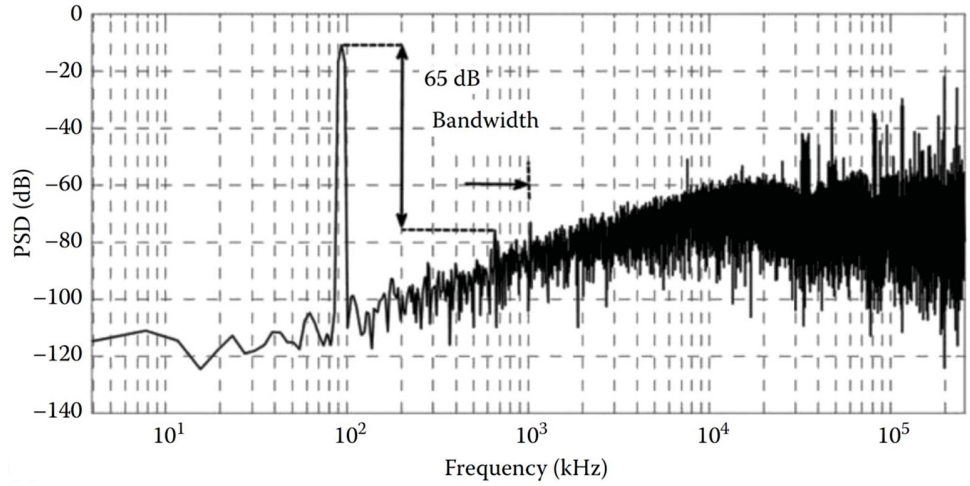
1.4.2 TM ΔΣADC Using DLL-Like Structure

A second-order TMΔΣ modulator with voltage input can be achieved by exploiting the structure of a DLL (Yoder *et al.*, 2011; Tousi *et al.*, 2011; Baker, 2011; Lin *et al.*, 2012). The general form of a DLL is shown in Figure 1.25(a). Here a VCDU is tuned such that the total delay through the VCDU is equal to the period of the incoming reference clock signal. By adding a voltage summing circuit between the charge-pump and loop-filter, an input voltage can be injected into the feedback loop. In addition, a one-bit quantizer (DFF) is added at the output of the phase detector to quantize its output. This output will be the output for the ADC. The VCDU is driven with a clock signal whose input–output phase difference will be proportional to the control voltage V_{ctrl}. In essence, this circuit acts as a voltage-to-phase converter. The resulting design is shown in Figure 1.25(b).

Collectively, the VCDU, phase detector, and DFF form a one-bit phase quantizer. The resulting single-loop configuration takes on the general form of Figure 1.22. Linearizing the system results in the equivalent z-domain block diagram shown in Figure 1.25(c). Here K_{VCDU} and K_{CP} are the gain of the VCDU and charge pump, respectively. Writing the output $D_{out}[n]$ in terms of the input $v[n]$ and phase quantization error $\phi_e[n]$, one can write in the frequency



a) Non-feedback VCO-based ΔΣ modulator.



b) VCO-based ΔΣ modulator with feedback.

Figure 1.24 PSD of the VCO-based ΔΣ modulator with a tracking-loop quantizer.

domain,

$$D_{out}(z) = STF(z)V_{in}(z) + NTF(z)\phi_e(z) \tag{1.53}$$

where

$$\begin{aligned} STF(z)V_{in}(z) &= \frac{K_{VCDU}H_{LP}(z)z^{-1}}{1+K_{VCDU}K_{CP}H_{LP}(z)z^{-1}} \\ NTF(z)V_{in}(z) &= \frac{1}{1+K_{VCDU}K_{CP}H_{LP}(z)z^{-1}} \end{aligned} \tag{1.54}$$

For a second-order loop filter of the general form,

$$H_{LP}(z) = \frac{1}{(1-z^{-1})^2} \tag{1.55}$$

the STF and NTF takes on the form

$$\begin{aligned} STF(z)V_{in}(z) &= -\frac{K_{VCDU}z^{-1}}{(1-z^{-1})^2 - K_{VCDU}K_{CP}z^{-1}} \\ NTF(z)V_{in}(z) &= \frac{(1-z^{-1})^2}{(1-z^{-1})^2 - K_{VCDU}K_{CP}z^{-1}} \end{aligned} \tag{1.56}$$

Simulink/MATLAB simulation reveals second-order noise shaping at the output of the time-mode ΔΣADC, confirming the aforementioned theory. This design achieved 8 bits of resolution over a 10 MHz signal bandwidth (Lin *et al.*, 2012). Experimental results have yet to confirm the validity of this approach and any unforeseen practical issues.

1.4.3 High-Order TM ΔΣADC Modulator With Voltage-Controlled GRO (VCGRO)

To achieve a high SNDR for wideband applications, the order of the ΔΣ modulator must be increased. In order to achieve this, two topologies have been presented in (Pavan *et al.*, 2017) that are suitable for this application, using a single-loop and a MASH architecture. A single-loop TMΔΣ modulator proposed in (Straayer *et al.*, 2008) utilizes the VCO as a quantizer to achieve third-order noise shaping. The main disadvantage of this design is that it uses voltage-domain components such as op-amp and DACs to realize the feedback structure around the quantizer. Therefore, large gain bandwidth (GBW) op-amps and extremely linear DACs are required to meet the aforementioned described system requirements.

A fully integrated time-domain high-order MASH ΔΣ modulator based on VCGRO has been presented in (*et al.*, 2013). Figure 1.26 displays a block diagram of this design. The basic idea behind this approach is that the VCO in the top block is used to convert the input voltage signal $v_{in}[n]$ to the phase domain and then applied to the bottom block that forms a VCGRO-based TDC to digitize the quantization noise from the first modulator and a sampled version of the

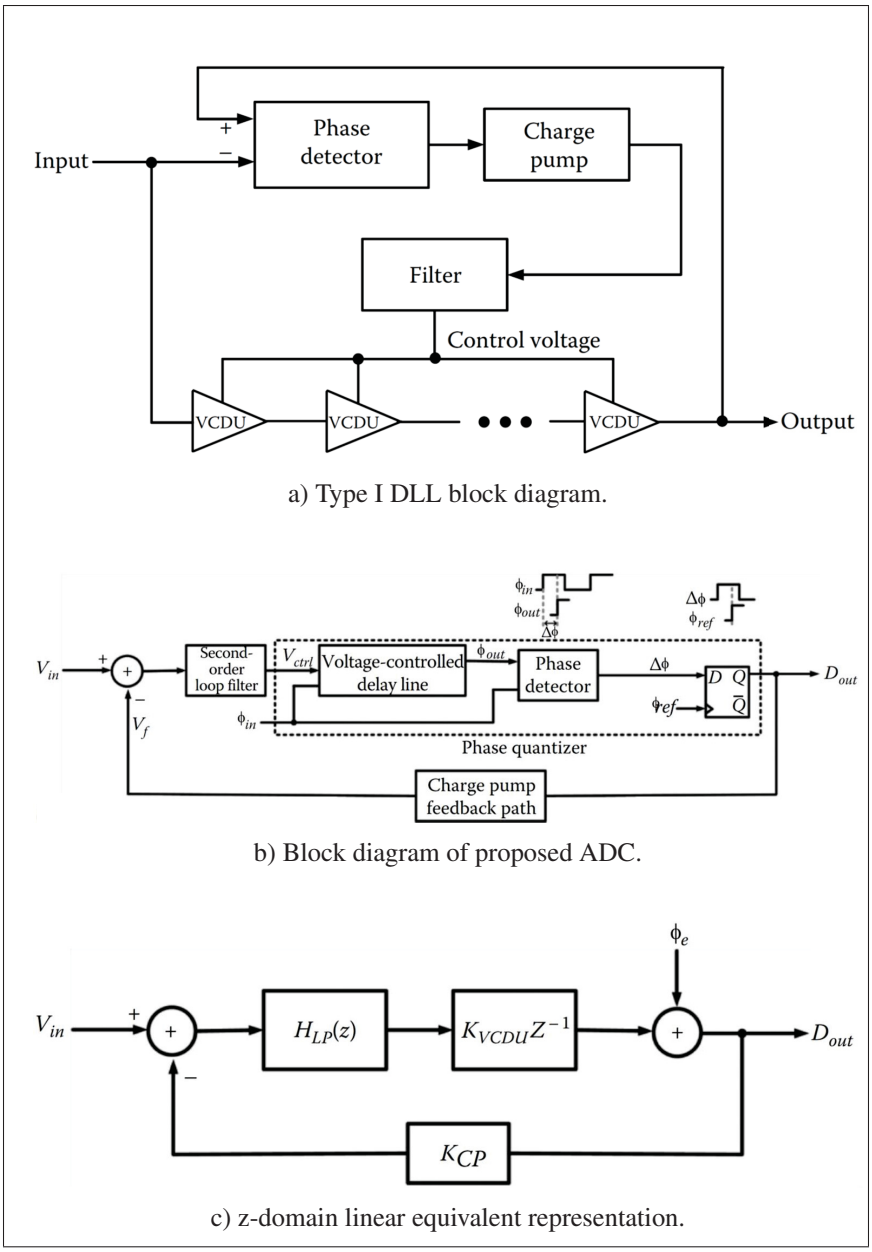


Figure 1.25 DLL-based ADC block diagram sharing the same mechanism as a conventional DLL.

input voltage, $v_{in}[n]$. A digitized version of this noise is passed to the digital cancellation logic block where the quantization noise from the first modulator is canceled. An attractive feature of this structure is that it can realize a high-order NTF with a cascade of two or more VCGRO quantizers.

Based on our previous analysis, the output code count $D_{VCO}[n]$ from the VCO can be written as

$$D_{VCO}[n] = \frac{1}{2\pi}\phi_{VCO}[n] - \frac{1}{2\pi}\left(\phi_{e,VCO}[n] - \phi_{e,VCO}[n-1]\right) \tag{1.57}$$

and output code count from the VCGRO as

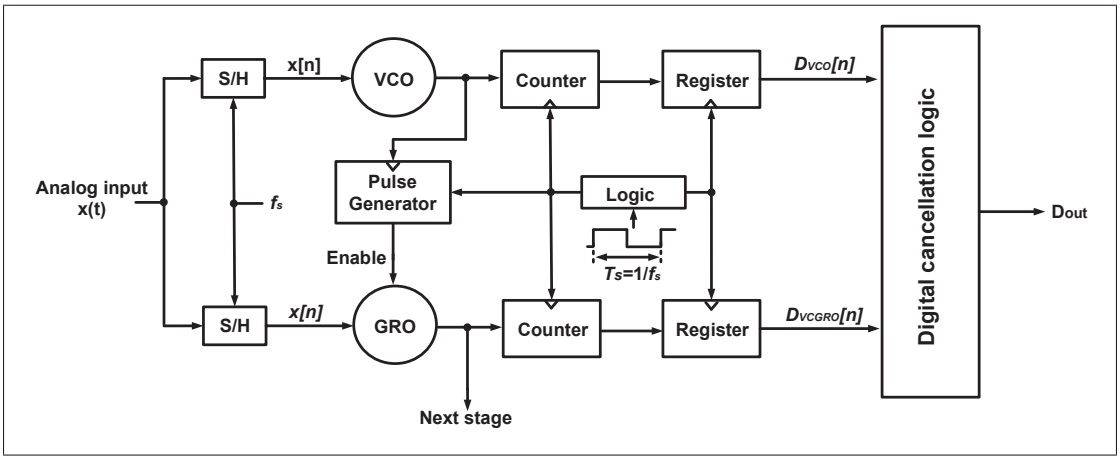


Figure 1.26 High-order TMΔΣ modulator with MASH structure using VCO and VCGRO.

$$D_{VCGRO}[n] = \frac{1}{2\pi}\phi_{VCGRO}[n] - \frac{1}{2\pi}\left(\phi_{e,VCGRO}[n] - \phi_{e,VCGRO}[n-1]\right) \tag{1.58}$$

where $\phi_{e,VCO}[n]$ and $\phi_{e,VCGRO}[n]$ are the corresponding quantization errors at the nth sampling instant from the VCO and VCGRO. In each case, first-order noise shaping of the quantization noise is present at the outputs of each VCO. The digital cancellation block combines the two output terms such that in the z-domain

$$D_{out}(z) = z^{-1}D_{VCO}(z) - (1-z^{-1})D_{VCGRO}(z) \tag{1.59}$$

Based on the mathematical analysis presented in (Yu *et al.*, 2013), together with a few approximations, the digital output $D_{out(}z)$ after cancellation can be written in terms of the input signal

$v_{in}[n]$ as

$$D_{out}(z) = K_{VCO}T_sV_{in}(z) - \frac{1}{2\pi}(1-z^{-1})^2\phi_{e,VCGRO}(z) \tag{1.60}$$

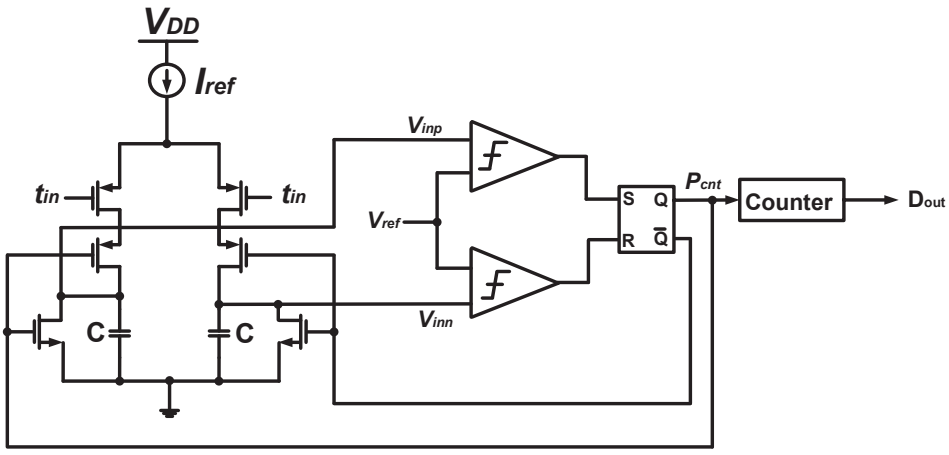
where $V_{in}(z)$ and $\phi_{e,VCGRO}(z)$ are the z-transforms of input signal $v_{in}[n]$ and quantization error signal generated by the VCRGO, that is, $\phi_{e,VCGRO}[n]$. This expression highlights the claim of second-order noise shaping provided by this architecture, as the second term of (1-79) contains the term $(1-z^{-1})^2$. Experimental validation is yet to be given for this new architecture.

1.4.4 High-Order TM ΔΣADC Modulator Using A Relaxation Oscillator Technique

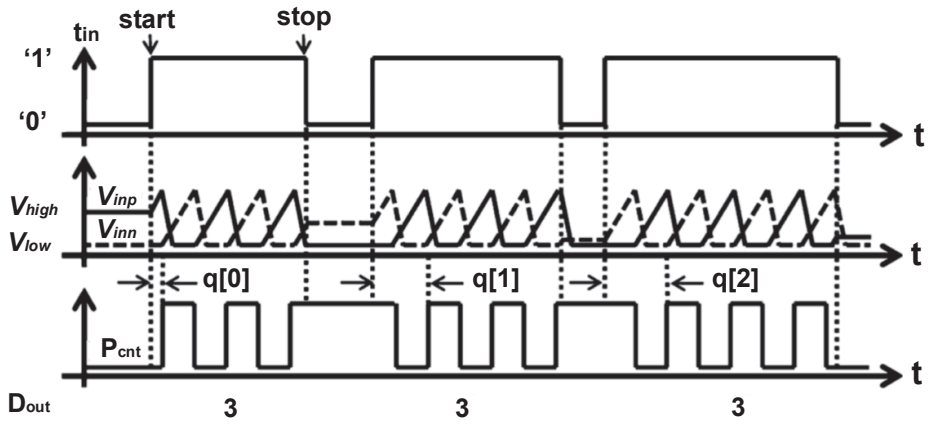
Another approach to achieve high-order noise shaping based on a MASH structure was presented in (Cao *et al.*, 2012) based on a relaxation oscillator technique. This design consists of three first-order TMΔΣTDCs with a structure of a cascade of three first-order sections denoted as a 1-1-1 MASH structure (see Figure **??**). The schematic of the first-order ΔΣ modulator is shown in Figure 1.27(a). It includes two comparators, SR flip-flop, counter, and a circuit to convert the input time-difference interval into a charge quantity on the capacitors C. Charging and discharging the capacitors will generate a clock pulse that enables the counter through the comparator and SR flip-flop combination. The width of this pulse is proportional to the voltage difference on the capacitors.

An interesting characteristic of the relaxation oscillator-based TMΔΣTDCs is that the quantization error is scrambled during successive quantization steps (Cao *et al.*, 2012) as depicted in Figure 1.27(b). Consequently, first-order noise shaping for one stage and third-order noise shaping for 1-1-1 MASH structure can be achieved.

A major performance limitation of this approach is the charge that leaks off the capacitors during their holding phase. Another issue relates to mismatches between stages.



a) Circuit schematic



b) Timing diagram

Figure 1.27 First-order ΔΣ modulator using a relaxation oscillator.

1.5 TMΔΣ Design Issues

The performance of TMΔΣ modulators is limited by four underlying factors: (1) nonlinearity of the basic delay element used in a delay line or in a ring oscillator, (2) mismatches between TM components, (3) clock jitter introduced noise, and (4) flip-flop metastability. In this section, these limitations will be described.

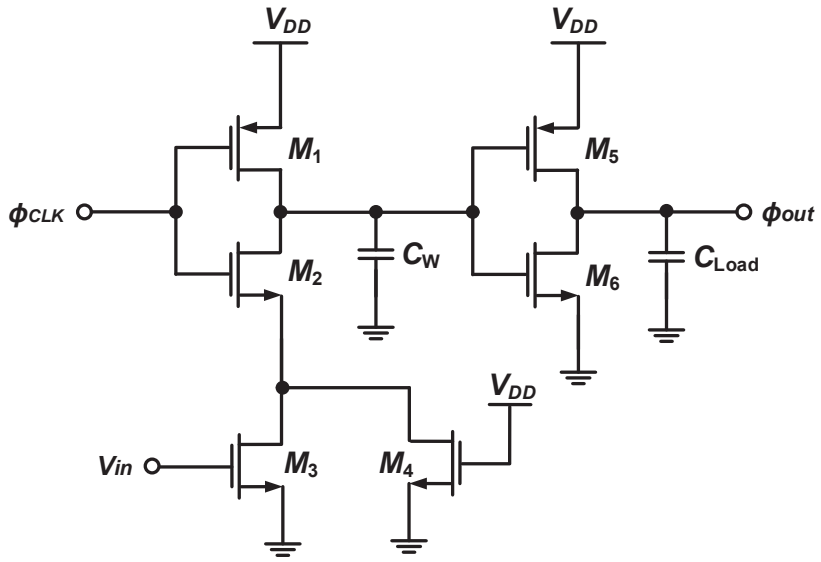
1.5.1 VCDU Nonlinearity

A VCDU is often used in TMSP to convert voltage-domain signals to a corresponding time-mode signal. The main drawback of this element is that it has a limited range of linear operation, thereby limiting its overall DR of operation.

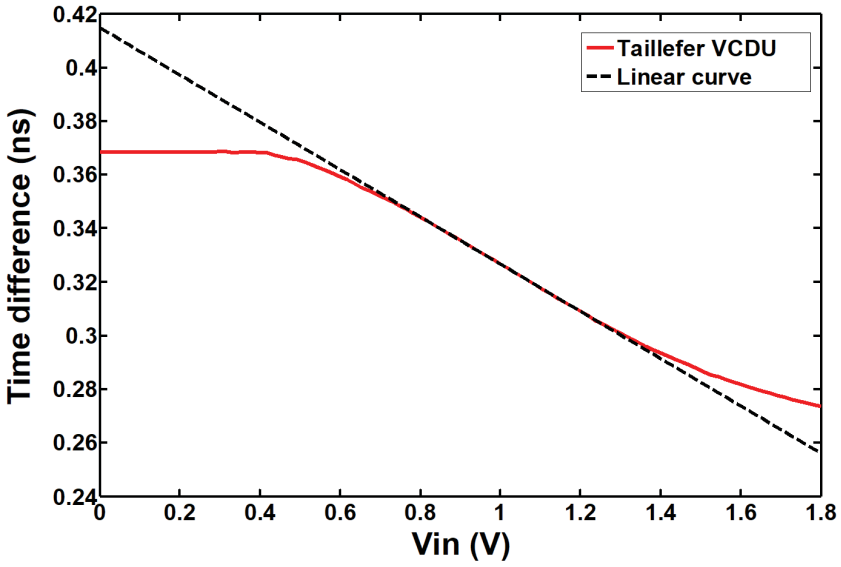
Figure 1.28(a) illustrates a CMOS implementation of a VCDU with a negative delay coefficient. The basic cell consists of essentially two capacitive loaded inverter circuits. The first inverter also includes two additional transistors M_3 and M_4. Both M_3 and M_4 operate in the triode region, thereby acting as voltage-controlled resistors. The gate of M_3 is connected to the input signal v_{in} so that its resistance value can change with this level and the gate of M_4 is simply connected to V_{DD} so that its value is constant. With a specific input voltage set at the gate of M_3 and the clock input set high, M_1 turns off and M_2 turns on, thereby discharging capacitor C_W and forcing the output node to a zero state. The subsequent inverter circuit then inverts this quantity and produces a logic 1 output. Conversely, when the clock input returns to a low level, M_1 turns on and M_2 turns off, thereby charging C_W back to V_{DD}. The following inverter then puts out a logic 0.

With a periodic clock input, the output is also periodic with the identical frequency but show a slight delay with respect to the input. The propagation delay is tunable with the control voltage v_{in}. The v_{in}-input versus VCDU propagation delay transfer characteristic is shown in Figure 1.28(b) for a 180 nm CMOS process. While the specific delay values are unimportant here, one can see the general shape of this transfer characteristic. It has a somewhat linear region between an input voltage of 0.8 V and 1.2 V, whereas for the input voltage less than 0.8 V or greater than 1.2 V, the VCDU behavior is visibly nonlinear.

This VCDU design is limited to a 0.4 V input voltage range, about 20% of the ideal headroom available from the power supply V_{DD}, which severely limits the performance of the TMΔΣ modulator. Indeed, it was shown in (Ziabakhsh *et al.*, 2015) that by improving the linearity of VCDUs with new circuit topologies, the DR of TMΔΣ modulators improves accordingly.



a) Circuit schematic.



b) Input-output transfer characteristic.

Figure 1.28 VCDU.

1.5.2 Component Mismatches

Mismatches between otherwise identical elements have a major impact on the linearity of TMΔΣ modulators. If the delays associated with individual inverters in a ring oscillator that is used to realize a multiphase generator are mismatched, then the relative output phases will contain systematic or offset phase errors. As a consequence, in-band noise level will increase, thereby limiting the effective resolution of the TMΔΣ modulator. An analysis of these effects was provided in Section 1.3.2 related to the GRO approach and how data-weighted averaging could minimize these effects by noise-shaping these errors out-of-band.

1.5.3 Jitter-Induced Noise

So far, we have covered issues related to nonlinearity in the transfer characteristic of a TM element such as a VCDU and mismatches between otherwise identical behaving devices. Another issue that one has to consider in the design of TM circuits is jitter-induced noise error that comes from the main reference clock. Noise associated with the clock reference generating circuit manifests itself into random variation in the placement of the clock edges as illustrated in Figure 1.29, clock jitter can be caused by electromagnetic interface (EMI), crosstalk, and wave reflections due to incorrectly terminating transmission lines, thermal noise, and/or poor power supply isolation.

Jitter is generally divided into two classifications: deterministic or random. Deterministic jitter (DJ) refers to jitter effects that are bounded in amplitude, periodic, or data dependent. Random jitter (RJ) is any jitter that does not fall into the DJ category and is fundamentally unbounded in value (M.P. Li, 2007). Jitter-induced noise effect is a fundamental limitation of ADCs and has been studied extensively (Luschas *et al.*, 2002; Lauritzen *et al.*, 2010). While clock jitter is expected to also be a fundamental limitation of TM circuits, the authors are not aware of any extensive study confirming that this is indeed the case.

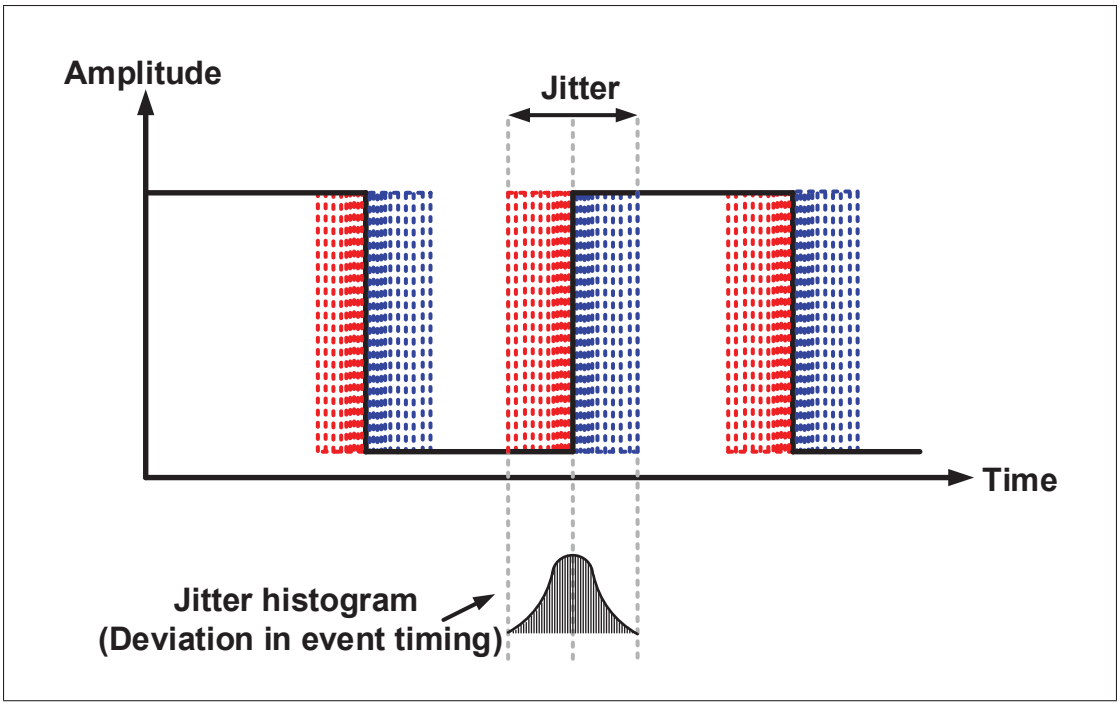


Figure 1.29 Jitter noise definition in TMΔΣ modulators.

1.5.4 DFF Design Challenges

A DFF is the most basic decision-making element of TM circuits. However, flip-flops experience a dead band effect whereby when the input timedifference signal is small in magnitude, such as when the time difference between a start and stop signal is small, the output of the flip-flop lies in an undetermined logic state, called the metastable state. Logic circuits that are reading this value cannot, as it is not a proper logic value, and instead misread the output value and can generate a logical bit error.

A classic method used to compensate for metastable behavior is to cascade multiple flips-flops or latches to give the front-end flip-flop more time to set its output value to the correct logic level (Deschamps *et al.*, 2012). Another method is to employ a time amplifier circuit to preamplify the small time difference prior to the decision-making flip-flop (Oulmane *et al.*, 2004; Chung *et al.*, 2010). This approach reduces the potential for metastable-related bit errors

and improves the resolution of TMΔΣ modulators; however, it consumes more power and die area.

1.6 Comparison of TM Versus VM ΔΣ Modulators

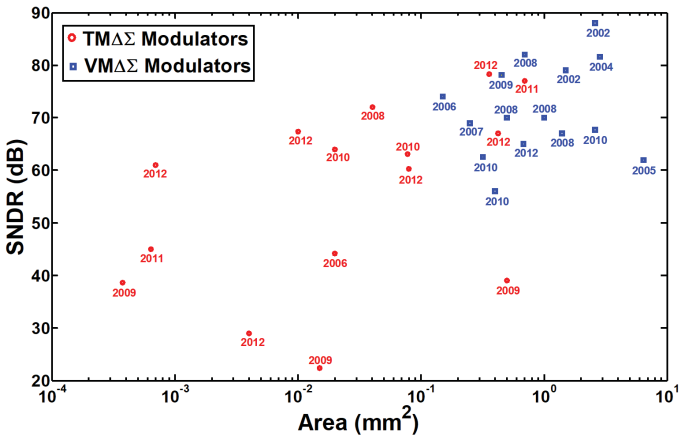
Over the last decade, many different VM and TM ΔΣ modulators have been implemented and their experimental results published. Of particular interest is how the SNDR performance of the reported ΔΣ modulators varies with silicon area, analog signal bandwidth, and power consumption. Scatter plots of the published works are shown in Figure 1.30.

It is interesting to compare the general behavior of a TM realization with a VM realization. One can see from these three scatter plots that the SNDR performance of a TM realization is generally less than those implemented using a VM approach; however, the power and silicon area requirements are generally orders of smaller magnitude. In contrast, the analog signal bandwidth is generally much higher for a VM realization than a TM realization.

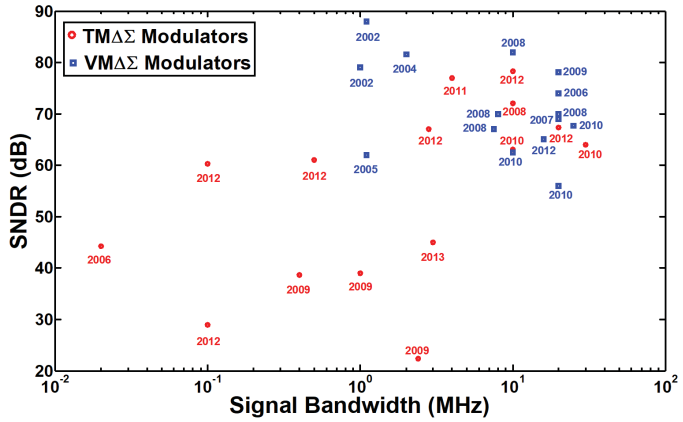
In the next chapter, we compare the peak SNR of both signal processing techniques (VM and TM) for a simple PMOS-NMOS transistor stack in the presence of technology scaling. It shows that below 90 nm CMOS process, TM circuits provide better SNR than VM circuits for the same bandwidth.

1.7 Summary

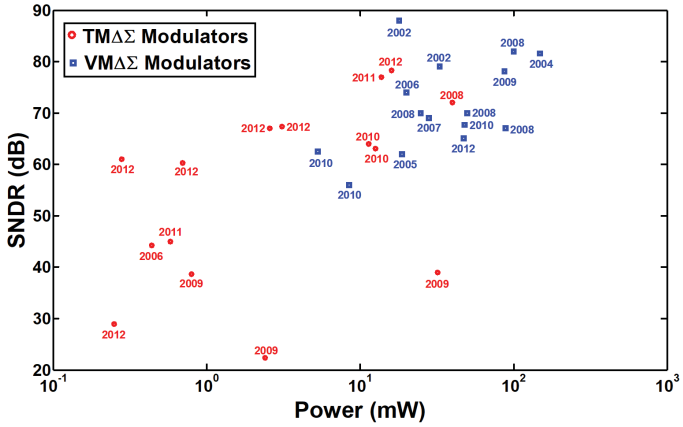
Voltage-domain ΔΣ modulators implemented in CMOS technologies are widely employed across the electronics industry as a main component of an ADC. However, as CMOS processes advance, MOS transistors must operate at lower voltage supply levels and this will cause major havoc on the operating characteristics of VMΔΣ modulators. TMΔΣ modulators make use of digital-like circuits that easily scale with advances in CMOS technologies and, hence, lend themselves as a potential solution to realize ADCs in fine-lined CMOS processes.



a) SNDR versus area.



b) SNDR versus signal bandwidth.



c) SNDR versus power.

Figure 1.30 Historical performance comparisons.

The primary objective of this chapter was to expose the principles of TM circuits for ΔΣ modulators more from a block diagram point-of-view rather than detail circuit perspective. While both perspectives are important, it is our belief that the block level perspective should be the priority of TM circuit designers before venturing down into the morass of transistor circuit design of ΔΣ modulators.

To date, numerous types of TMΔΣ modulators have been proposed, fabricated, and tested. This includes single-bit, multibit, first-order, and higher-order type modulators. Through the application of the noise-shaping principle, both the quantization error made by a TM decision-making circuit and the systematic phase offsets associated with the component mismatches in the various timing circuits can be significantly reduced, giving way to a new generation of TM circuits that do not require any form of off-line or on-line calibration.

Results are extremely encouraging, especially in light of the present day facts that TMΔΣ modulators offer low power operation and a small silicon area foot print. While the DR of TM circuits is not quite at the level of a VM circuit, it is the author's belief that this is just a matter of time before TM circuits reach performance levels equivalent to their voltage mode equivalents. One must recognize that the key principle of noise-shaping in TM circuits was only recently introduced and the number of people working in this area had been modest. It is our belief that this is soon to change.

CHAPTER 2

THE PEAK-SNR PERFORMANCES OF VOLTAGE-MODE VERSUS TIME-MODE CIRCUITS: THE PMOS-NMOS STACK USE CASE

2.1 Introduction

The objective of this chapter is to identify whether future TM circuits will achieve performance levels on par or higher than what is expected from future VM circuits operating at different bandwidth levels, i.e., rise/fall times, in the presence of transistor thermal and flicker noise components (Ziabakhsh, Gagnon and Roberts, 2018). To do so, the maximum achievable signal-to-noise ratio (SNR) of the most basic circuit element common to both designs: a PMOS-NMOS transistor stack, will be analyzed and used to predict the peak-SNR performance of VM and TM circuits over various technology nodes. In (Pathan *et al.*, 2016), a model for VM and TM noise analysis was proposed; however, the noise model only describes the effect of thermal noise on circuit operation, and therefore is limited in its performance prediction as it ignores the flicker noise component. In this chapter, the proposed analysis is applied to different CMOS technology nodes and compared to Spectre transient noise analysis. A silicon prototype was fabricated in the IBM 130-nm CMOS technology. The accuracy of our proposed analysis is validated by measurement results and transistor-level transient noise simulations.

2.2 PMOS-NMOS Transistor Stack: Performance Definitions

A core transistor circuit common to both VM and TM circuits is the PMOS-NMOS transistor stack shown in Figure 2.1. In VM circuit shown in Figure 2.1(a), the PMOS-NMOS stack is used as a voltage amplifier, whereas in a TM circuit, the transistor stack is used as a delay element.

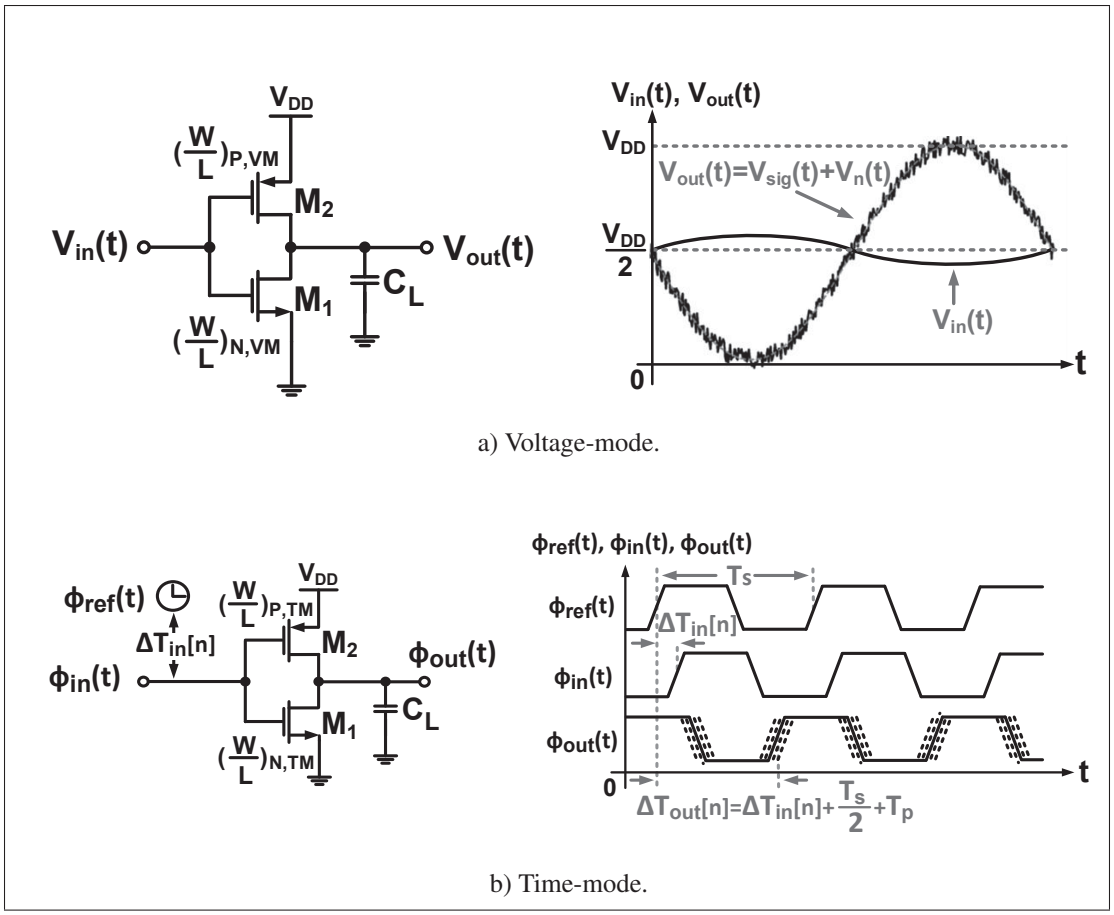


Figure 2.1 Basic primitive circuit element consisting of a PMOS-NMOS transistor stack in presence of noise.

2.2.1 Voltage-Mode Analysis

In the case of the amplifier, the output instantaneous voltage signal can be expressed in terms of the input voltage signal $v_{in}(t)$ as

$$v_{out}(t) = Gv_{in}(t) \tag{2.1}$$

where G represents the voltage gain of the amplifier. As the power supply level V_{DD} limits the maximum output signal, the maximum sinusoidal output signal will have an amplitude of $V_{DD}/2$ assuming the output quiescent operating point is set at $V_{DD}/2$. Correspondingly, the rms value of this output signal is $\left(V_{DD}/2\sqrt{2}\right)$. The noise generated by the PMOS-NMOS stack

limits the maximum SNR to:

$$SNR_{VM} = 10\log_{10}\left(\frac{V_{sig,rms}^2}{V_{n,rms}^2}\right) \tag{2.2}$$

where $V_{sig,rms}$ is the rms value of the output signal and $V_{n,rms}^2$ is total rms output noise signal over the bandwidth $f_H - f_L$ (where f_H and f_L are the upper and lower frequency bounds, respectively) that can be expressed as

$$V_{n,rms}^2 = \int_{f_L}^{f_H}\left(\sum_{i=1}^{M} S_{n,i}(f)|H_i(j2\pi f)|^2\right)df \tag{2.3}$$

Here $S_{n,i}(f)$ $(i = 0,1,2,...,n)$ represents the noise spectral densities (PSD) for each transistor which can include thermal and flicker noise components and $H_i(j2\pi f) = 1/\left(1+(2\pi R_o C_L f)^2\right)$ is the transfer function from each noise source to the output. To calculate the output-referred noise voltage, the input signal is shorted to the ground and the output noise voltages of M_1 and M_2 is calculated as:

$$\begin{aligned} &V_{n,rms}^2 = \\ &\int_{f_L}^{f_H}\left(\left(\left(g_{m,N}^2 S_{n,N}(f) + g_{m,P}^2 S_{n,P}(f)\right)R_o^2\right)|H_i(j\omega)|^2\right)df \end{aligned} \tag{2.4}$$

where

$$S_{n,N/P}(f) = 4kT\gamma\frac{1}{g_{m,N/P}} + \frac{K_{f,N/P}}{W_{N/P}L_{N/P}C_{ox}}\frac{1}{f} \tag{2.5}$$

and k is Boltzman's constant, T is the temperature, γ is a coefficient which depends on channel length (γ=1 for short-channel), $R_o = r_{oN} \parallel r_{oP}$ (r_{oN} and r_{oP} are output resistance of the NMOS and PMOS transistors, respectively), and $g_{m,N}$ and $g_{m,P}$ are the transconductance of NMOS and PMOS, respectively. The thermal and flicker noise of the transistors are modeled as uncorrelated voltage sources in series with their gates (B. Razavi, 2004). The second term on the right-hand side of (2.5), $K_{f,N/P}$ is a process-dependent constant, WL is the product of the transistor's dimensions, and C_{ox} represents the gate capacitance per area. In order to compute the total output noise power, the output PSD is integrated across the bandwidth of the amplifier

(from f_L to f_H). Subsequently, the expected SNR can be written as

$$SNR_{VM} = 10\log_{10}\left(\frac{\left(\frac{V_{DD}}{2\sqrt{2}}\right)^2}{\left(V^2_{n,rms,Thermal} + V^2_{n,rms,Flicker}\right)}\right) \tag{2.6}$$

where

$$V^2_{n,rms,Thermal} = 4KT\gamma R_o\left(g_{m,N} + g_{m,P}\right)\frac{tan^{-1}(f_H - f_L)}{2\pi C_L}$$

$$V^2_{n,rms,Flicker} =$$

$$\left(\frac{K_{f,N}g^2_{m,N}}{W_N L_N C_{ox}} + \frac{K_{f,P}g^2_{m,P}}{W_P L_P C_{ox}}\right)\left(\frac{R_o^2}{2}\right) \times \ln\left(\frac{(2\pi C_L R_o)^2 + \left(\frac{1}{f_H}\right)^2}{(2\pi C_L R_o)^2 + \left(\frac{1}{f_L}\right)^2}\right)$$

2.2.2 Time-Mode Analysis

In TM circuits, on the other hand, signals are represented as time differences between two time-varying signals, with one acting as the reference (or ground). For instance, the time-difference between the rising edge of an input signal $\phi_{sig}(t)$ and the rising edge of a periodic reference clock signal $\phi_{ref}(t)$ during the n-th clock cycle (rather than n-th time instant) defines a TM discrete-time signal as

$$\Delta T_{in}[n] = \phi_{in}(t) - \phi_{ref}(t), \quad \text{during n-th clock cycle} \tag{2.7}$$

For the PMOS-NMOS stack (Figure 2.1(b)), with input and output time-varying signals $\phi_{in}(t)$ and $\phi_{out}(t)$, and reference signal $\phi_{ref}(t)$, the output TM signal $\Delta T_{out}[n]$ can be expressed in terms of input TM signal as

$$\Delta T_{out}[n] = \Delta T_{in}[n] + \frac{T_s}{2} + T_p \tag{2.8}$$

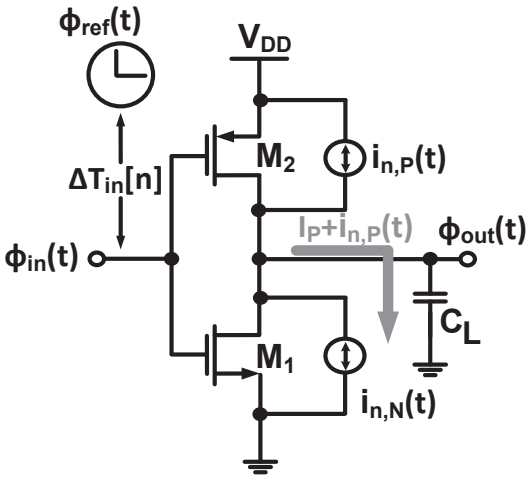
where T_s is the sampling period and T_p represents the propagation delay of the PMOS-NMOS stack.

In TM circuits, the signal amplitude is not limited by the power supply level and thus can be made to be arbitrarily large simply by using larger time-difference signals. However, TM signals are discrete by nature. Consequently, to satisfy the Nyquist sampling criterion, a tradeoff exists between the signal amplitude and its bandwidth. A large TM signal will inherently occupy a small bandwidth, or conversely, a small-signal can occupy a much larger bandwidth (Abdelfattah *et al.*, 2017). Unfortunately, small-signals are masked in various noise signals, such as jitter from the clock reference circuit, or jitter created by the thermal and flicker noise. As a result, the maximum achievable output SNR will be limited by both the desired bandwidth and output jitter.

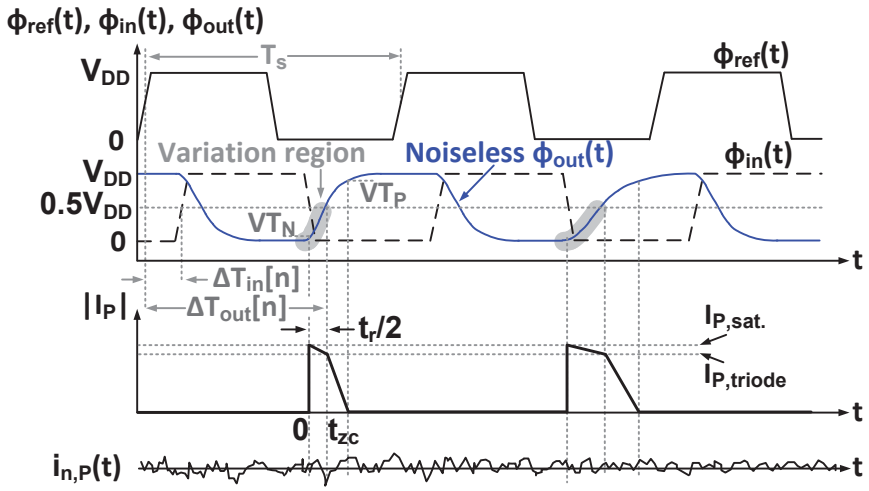
Let us assume that the maximum output signal level is bounded by the sampling period, T_s, with maximum output power $\left(T_s/2\sqrt{2}\right)^2$. The noise power is limited by the noise-induced jitter, denoted here by $\sigma_{t_{zc},rms}$. Consequently, the output SNR expressed in dB would be stated as

$$SNR_{TM} = 10\log_{10}\left(\frac{\left(\frac{T_s}{2\sqrt{2}}\right)^2}{\sigma^2_{t_{zc},rms}}\right) \tag{2.9}$$

An expression of the output timing jitter can be derived from an analysis of the time at which the output signal crosses the threshold level at $V_{DD}/2$ during low-to-high transition. An equivalent circuit with noise representation is shown in Figure 2.2(a). The timing diagram of the circuit under test is shown in Figure 2.2(b) with the top plot showing the ideal reference signal ($\phi_{ref}(t)$), the second plot showing the input and output voltage signals of the PMOS-NMOS stack, respectively. It should be noted that $\phi_{out}(t)$ is plotted with different rising times in order to show its impact on the output events. In this section, we describe a method to comprehend the dominant noise sources in TM circuits. While the timing jitter analysis has been described in previous publication (Pathan *et al.*, 2016), it was limited to a small-signal perspective; one that does not apply to TM, as they operate in a digital or large-signal manner. In the following analysis, the large-signal perspective of TM circuits is taken into account to calculate its jitter period. In addition, this analysis includes both thermal and flicker noises in contrast to the work of (Pathan *et al.*, 2016), which performed only a thermal noise analysis.



a) Equivalent circuit with noise representation.



b) Timing diagram with noise superimposed.

Figure 2.2 PMOS-NMOS stack jitter analysis.

We begin by assuming that PMOS transistor is turning on and the output signal, $\Phi_{out}(t)$, begins to rise. The charging current flowing into capacitor, C_L, during the initial low-to-high transition is essentially constant at a level of $I_{P,sat}$. While there are minor variations from this constant value, their effects are low enough to be ignored in our analysis. After the low-to-high transition crosses the threshold $V_{DD}/2$, the charging current rapidly decreases to zero. In addition, during this initial time, a noise component from the PMOS transistor ($i_{n,p}(t)$) also contributes to the

charge on C_L, resulting in timing jitter, as depicted in the fourth plot from the top. As this time is approximately one-half the rise time of the low-to-high transition, this time will be designated as t_{zc}; which, due to jitter, is a random variable. It is during this time interval that the noise affects the zero crossing. Any noise appearing after this time, has no effect, as the circuit has fully changed state. Here t_{zc} can be expressed in terms of the circuit parameters as follows

$$t_{zc} = \frac{t_r}{2} = \frac{V_{DD}/2}{SR} \tag{2.10}$$

where t_r is the rise time of $\Phi_{out}(t)$ and $SR = I_{P,sat}/C_L$ is the slew rate during the time interval $[0, V_{DD}/2]$. The PSD of t_{zc} can be expressed as in (A. A. Abidi, 2006)

$$S_{t_{zc}}(f) = \frac{(t_r/2)^2}{I_{P,sat}^2}\left(sinc^2(\pi f t_r/2) \times S_{i,n}(f)\right) \tag{2.11}$$

where $S_{i,n}(f)$ in units of A^2/Hz is the PSD of noise current across C_L in terms of both thermal and flicker noise that can be calculated:

$$S_{i,n}(f) = S_{thermal}(f) + S_{flicker}(f) = 4KT\gamma g_m + \frac{K_{f,P} g_m^2}{WLC_{ox} f} \tag{2.12}$$

The variance of the timing jitter can be found by integration of $S_{i,n}(f)$ from dc to infinite frequency (Abidi, 2006; Homayoun *et al.*, 2013) and can be derived as

$$\begin{aligned}\sigma_{t_{zc}}^2 = {} & \frac{4KT\gamma g_m (t_r/2)^2}{I_{P,sat}^2}\int_0^\infty \left|\frac{sin(\pi f t_r/2)}{\pi f t_r/2}\right| df \\ & + \frac{(t_r/2)^2 g_m^2 K_{f,P}}{I_{P,sat}^2 WLC_{ox}}\int_0^\infty \left(\frac{sin(\pi f t_r/2)}{\pi f t_r/2}\right)^2 \frac{1}{f} df\end{aligned} \tag{2.13}$$

The first and second terms in (2.13) indicate the jitter amount caused by thermal and flicker noise during low-to-high transition. Evaluating the integral for the first term, (A. A. Abidi,

2006) gives the thermal noise contribution

$$\sigma^2_{t_{zc},thermal} = \frac{2KT\gamma g_m t_r/2}{I^2_{P,sat}} \tag{2.14}$$

The solution to the second term integration due to transistor flicker noise contribution is slightly more complicated. However, an approximation can be found by moving the lower limit of dc to a non-zero frequency limit denoted as f_l. In practice, one typically selects an offset frequency of 10 Hz or less from the reference clock frequency, depending on phase noise requirements. Such an analysis was performed in (Liu *et al.*, 2004) resulting in the following closed-form solution,

$$\sigma^2_{t_{zc},flicker} = \frac{(t_r/2)^2 g^2_m K_{f,P}}{I^2_{P,sat} WLC_{ox}} \left(\frac{3}{2} - Ci(2\pi f_l t_r/2) \right) \tag{2.15}$$

where $Ci(x)$ is cosine integral function. Substituting (2.14) and (2.15) into (2.13) and using the expression given previously for t_{zc} in (2.10), the standard deviation of total jitter due to thermal and flicker noise can be written as follows

$$\sigma_{t_{zc}} = \sqrt{\left[\frac{2KT\gamma g_m V_{DD} C_L}{2I^3_{P,sat}} + \frac{V^2_{DD} C^2_L g^2_m K_{f,P}}{4I^4_{P,sat} WLC_{ox}} \left(\frac{3}{2} - Ci\left(2\pi f_l \frac{V_{DD} C_L}{2I_{P,sat}} \right) \right) \right]} \tag{2.16}$$

Although it is not directly evident, depending on the actual rise-time of the circuit, one of the two terms dominates the jitter expression. For instance, when the circuit rise time in a 180 nm CMOS process is greater than 65 ns, the flicker noise component will be two times larger than the thermal noise component. Conversely, when the rise time is less than 15 ns, the thermal noise will be two times larger than the flicker noise.

2.3 Simulation Results

In this section, we shall demonstrate the accuracy of the VM and TM noise and SNR expressions with a Spectre simulation using different CMOS technologies. To begin, our theoretical analysis will be based on device parameters extracted from a TSMC 180 nm CMOS process. These predictions will then be compared with the simulated Spectre results corresponding to VM and TM circuits constructed using TSMC 180 nm, IBM 130 nm, and TSMC 65nm CMOS technologies under the assumption of maximum output signal swing (zero voltage and time offsets). A convenient way to scale down the transistor device parameters is to make use of Dennard's scaling law (Weste *et al.*, 2011), whereby a scaling factor $1/S$ is used to reduce the device dimensions. Table 2.1 consists of two groups of transistor aspect ratios: the initial transistor aspect ratios and another that was optimized for maximum signal swing operation. The initial transistor sizes for the 180 nm process were selected through simulation. The sizes for other technologies were selected by scaling them downwards by using Dennard's scaling law. Using the physical parameters shown in Tables 2.1 and 2.2, the device parameters (i.e., I_D or $I_{P,sat}$, g_m and r_o) across to three technologies was calculated using a square-law transistor model and is shown in Table 2.3 under the columns denoted Theoretical. A second set of columns denoted Simulation is also listed. These are values computed by Spectre using the optimized transistor sizes in Table 2.1.

To show the effectiveness of the proposed analysis, VM output noise and TM jitter as a function of the technology node length is shown in Figure 2.3(a) and (b), respectively. Two or three sets of data are shown in each plot. In the case of Figure 2.3(a) the circuit-level simulated data in different transistor types (e.g., lvt, svt, hvt) together with the theoretical results produced by (2.6) are displayed. As is evident, the output noise power increases with decreasing node length. In the case of the plot shown in Figure 2.3(b) the total jitter versus technology node length is shown for three separate cases: two theoretical plots and one transistor level simulation. One of the theoretical plots is based on (2.16) where both thermal and flicker noise is included. The second theoretical plot is based on the theory by (A. Pathan *et al., 2016*) where only thermal noise is considered. The TM calculated noise values shown in (2.16) agree with

Table 2.1 Initial transistor sizes and optimized sizes for simulation.

			Initial Transistor Sizes			Optimized Transistor Sizes		
			TSMC 180 nm	Dennard's Scaling Rule Applied				
Mode	**Aspect Ratio**	**Unit**		**IBM 130 nm-svt**	**TSMC 65 nm-svt**	**TSMC 180 nm**	**IBM 130 nm-svt**	**TSMC 65 nm-svt**
VM	$(W/L)_{PMOS}$	$[\mu m/\mu m]$	8/0.54	5.79/0.39	2.88/0.19	8/0.54	4.2/0.36	1.8/0.24
	$(W/L)_{NMOS}$	$[\mu m/\mu m]$	1.8/0.54	1.30/0.39	0.65/0.19	1.8/0.54	1.0/0.36	0.6/0.24
TM	$(W/L)_{PMOS}$	$[\mu m/\mu m]$	2/0.18	1.44/0.13	0.72/0.065	2/0.18	1.5/0.12	0.72/0.065
	$(W/L)_{NMOS}$	$[\mu m/\mu m]$	1/0.18	0.72/0.13	0.36/0.065	1/0.18	0.55/0.12	0.6/0.065

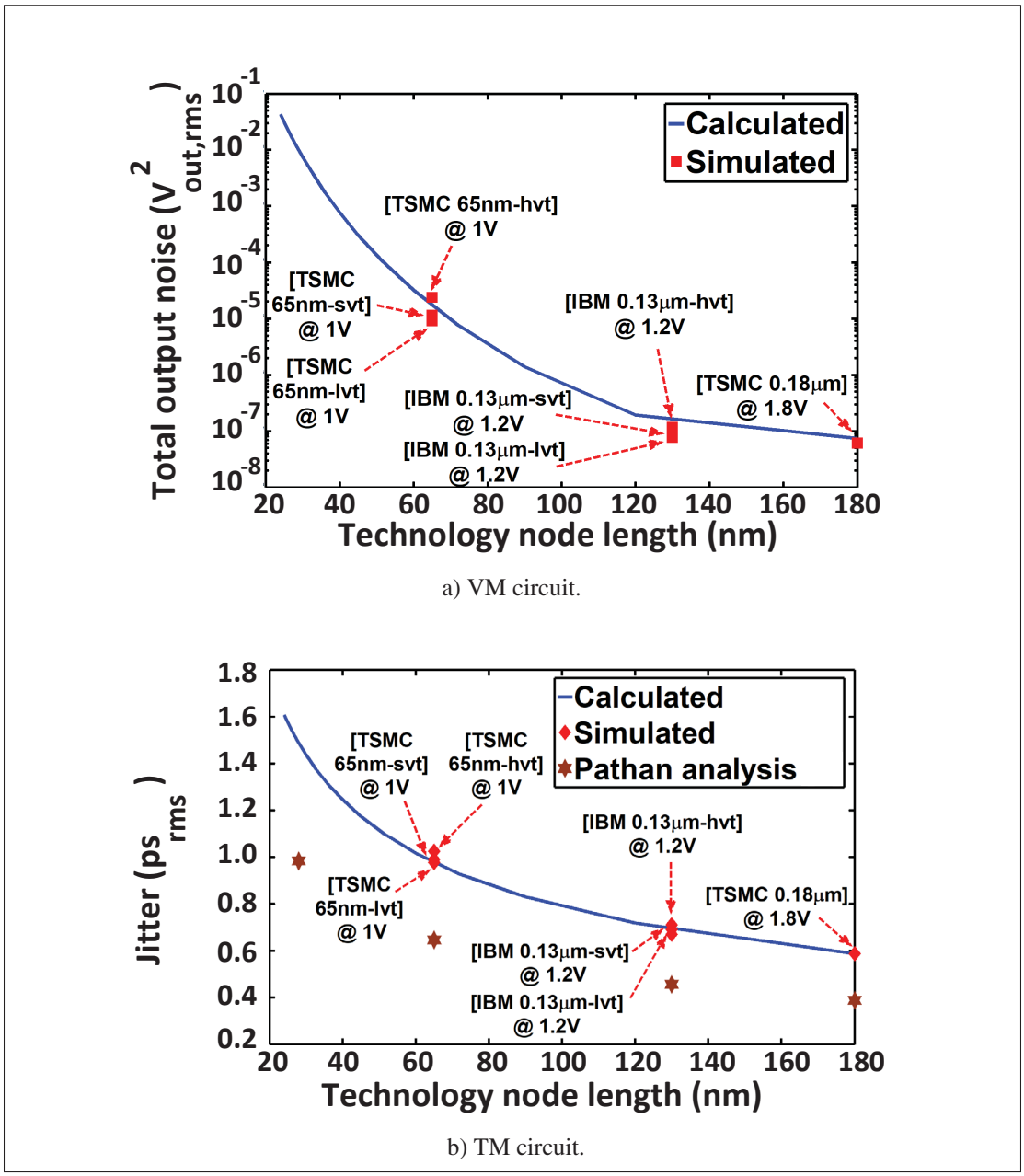
Table 2.2 Physical parameters of the CMOS transistors used in simulations.

Technology node	$\mathbf{V_{TH,P}}$ $[mV]$	$\mathbf{V_{TH,N}}$ $[mV]$	$\mathbf{K_{f,P}}$ $[V^2F]$	$\mathbf{K_{f,N}}$ $[V^2F]$	$\mu_\mathbf{P}\mathbf{C_{ox}}$ $[A/V^2]$	$\mu_\mathbf{N}\mathbf{C_{ox}}$ $[A/V^2]$	$\mathbf{T}$ $[^\circ K]$
TSMC 180 nm	463	489	1.6×10^{-25}	20×10^{-25}	97.48×10^{-6}	263×10^{-6}	300
IBM 130 nm	289	249	3.4×10^{-25}	22.4×10^{-25}	87.65×10^{-6}	249×10^{-6}	300
TSMC 65 nm	357	320	5.4×10^{-25}	24.6×10^{-25}	34.6×10^{-6}	113.4×10^{-6}	300

Table 2.3 Theoretical prediction and simulation results for the VM and TM device parameters.

Mode	**Parameter**	**Unit**	**TSMC 180 nm**		**IBM 130 nm-svt**		**TSMC 65 nm-svt**	
			Theoretical	**Simulation**	**Theoretical**	**Simulation**	**Theoretical**	**Simulation**
VM	I_D	$[\mu A]$	104.42	110.7	67.74	66.02	33.35	18.59
	$g_{m,N}$	$[\mu S]$	448.3	488.46	329.65	284.7	162.3	170.7
	r_{oP}	$[K\Omega]$	6.93	4.97	2.83	2.95	17.58	20.74
	r_{oN}	$[K\Omega]$	13.51	15.26	10.52	14.76	30.15	32.79
TM	$I_{P,sat}$	$[\mu A]$	128.8	132.6	93.02	104.8	46.51	48.8
Both	C_L	$[fF]$	150	150	108.33	105	54.16	50

the Spectre transient noise simulation results within a 5% error, but differs by as much as 35% from the analysis presented in (A. Pathan *et al., 2016*).



a) VM circuit.

b) TM circuit.

Figure 2.3 Output noise and jitter as a function of technology node length (lvt, std, and hvt are low, standard, and high threshold voltage, respectively).

Another result that supports the proposed analysis is by visualizing the TM jitter using (2.16) against the rise time t_r, as shown in Figure 2.4. This can be done by increasing C_L from the values shown in Table 2.3 for three technologies while other parameters are maintained constant. Figure 2.2.1 shows the comparison between transistor-level simulations (points marks either squares, triangles or stars) and theoretical predictions based on (2.16) (solid lines) and that predicted by the (A. Pathan *et al., 2016*) model (dashed lines). As can be seen from Figure 2.4, the rms jitter increases with increasing rise time t_r. The discrepancy between simulation results and the analysis in (A. Pathan *et al., 2016*) highlights the importance of including the effect of flicker noise as the rise time increases. The analysis is extrapolated to various technology nodes as shown in Figure 2.5 to provide insight as to whether TM circuits with different values of rise time, t_r, can surpass SNR performances of VM circuits. Here the reference rise-time $t_{r,ref}$ is set to 250 ps. Our analysis shows that the SNR performances of VM circuits decreases at a faster rate than TM circuits with technology scaling. This can be accounted for by the reduction in power supply level. This is confirmed by our simulation results. Below approximately 100-nm, TM circuits have the potential to provide a better dynamic range than VM circuits.

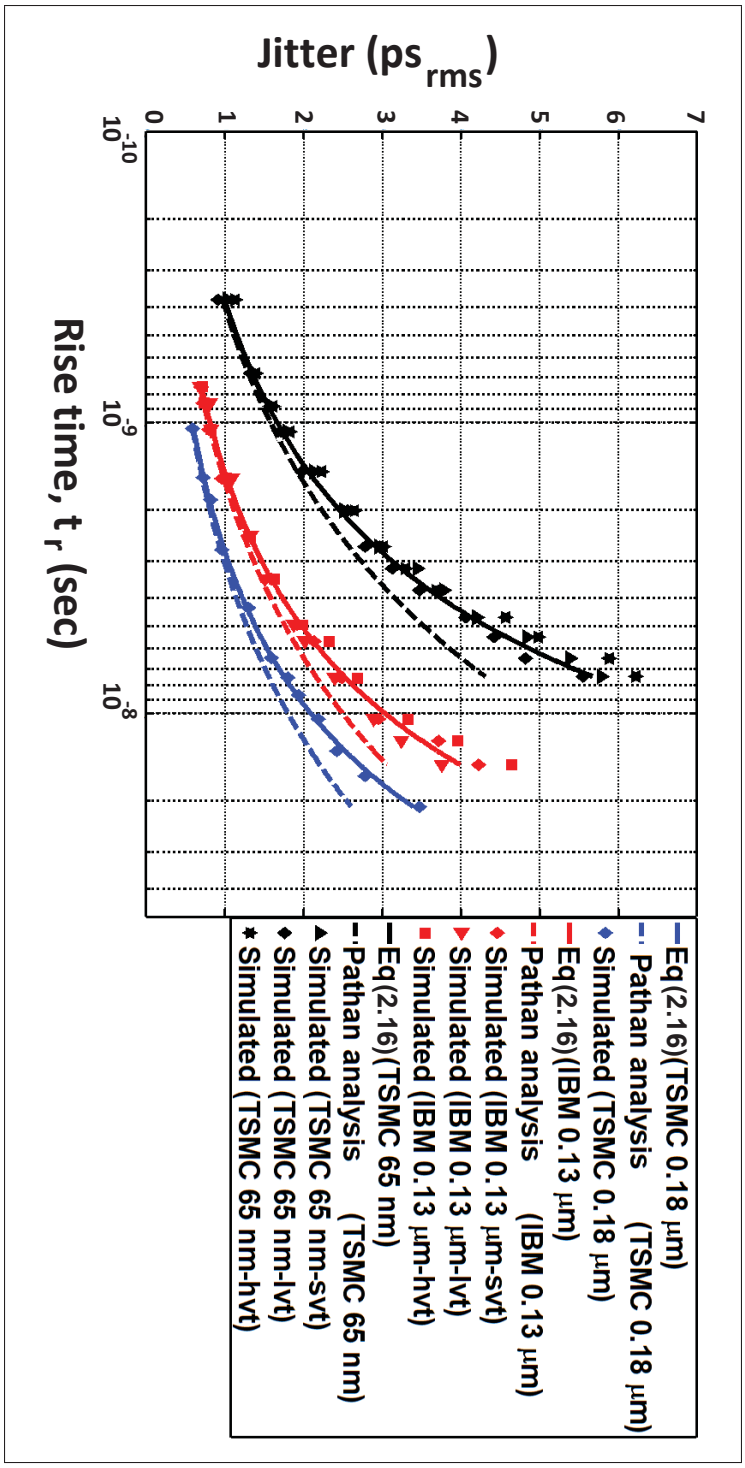


Figure 2.4 TM rms jitter versus rise time, t_r.

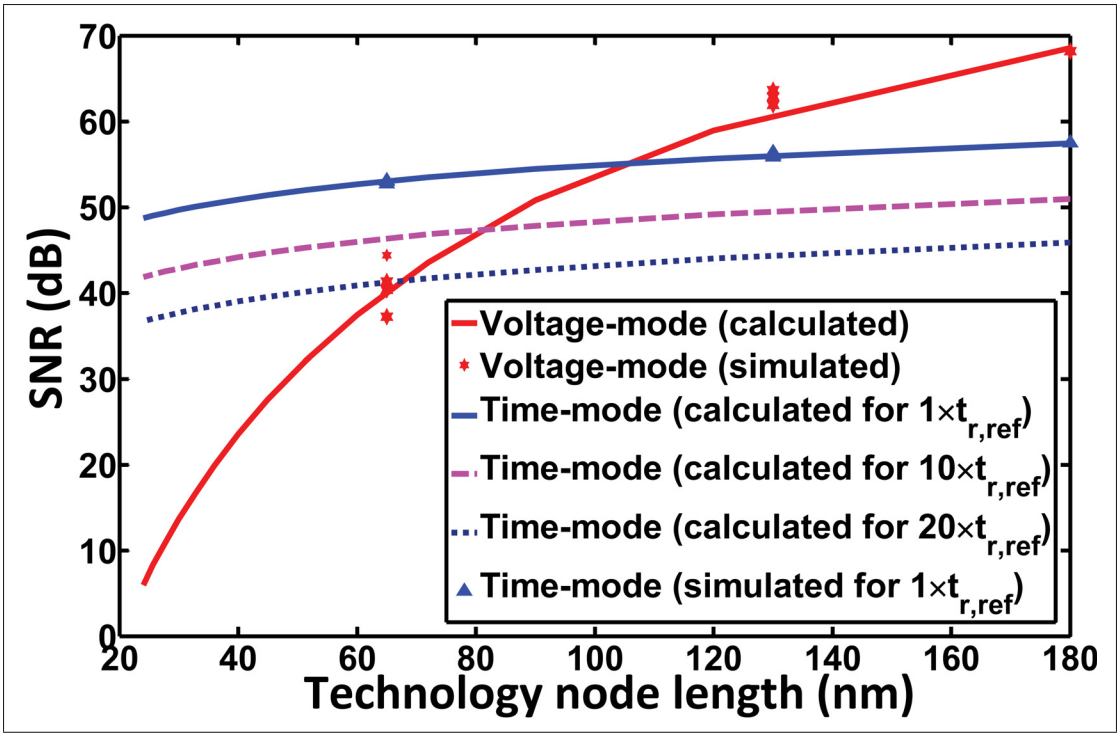


Figure 2.5 Peak-SNR performance for VM and TM PMOS-NMOS transistor stack versus technology node length ($t_{r,ref}$=250 ps).

2.4 Experimental Validation of Proposed Theory

In order to verify experimentally the jitter expression proposed in this paper, a VCDU has been designed based on (S. Ziabakhsh *et al., 2015*) and fabricated in a 130-nm IBM CMOS process. Figure 2.6 shows the schematic of the VCDU which is buffered by a series of inverters at its input and output. The design parameters for the VCDU and buffers are summarized in Table 2.4. From a noise perspective, the circuits of Figure 2.2(a) and Figure 2.6 are equivalent. As the effect of the noise at the output of the TM circuit occurs during the charging phase of the VCDU, only the top PMOS transistor contributes to the output noise. The NMOS transistors are essentially turned off during the charging phase. Figure 2.7 shows a die photograph of the VCDU. The fabricated VCDU occupies an area of 29.2 μm $\times$ 18.8 μm of silicon area (excluding the input and output buffers).

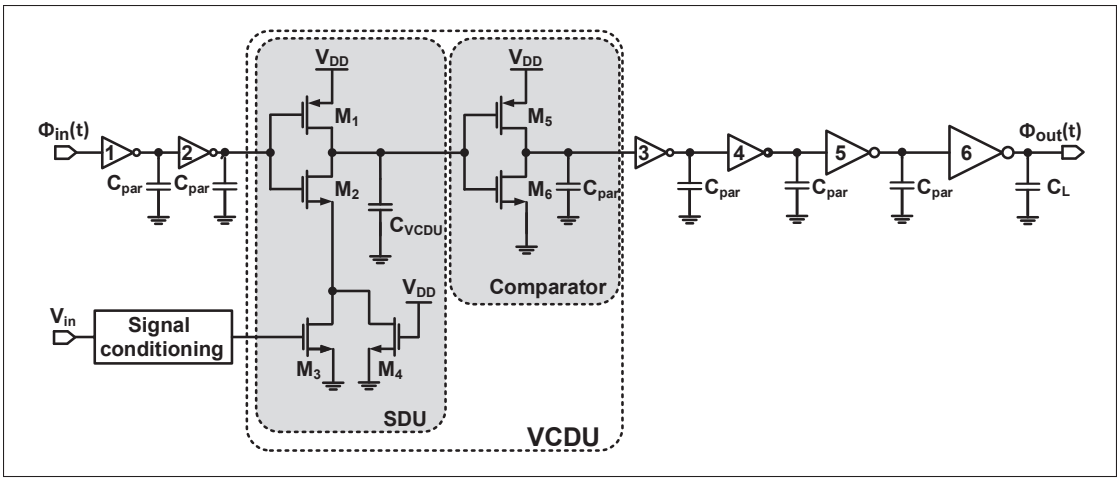


Figure 2.6 Schematic of the VCDU.

Table 2.4 Component values of the implemented VCDU.

$(W/L)_{M1}$	$(W/L)_{M2}$	$(W/L)_{M3}$
$5\mu m/0.36\mu m$	$2\mu m/0.12\mu m$	$1\mu m/4\mu m$
$(W/L)_{M4}$	$(W/L)_{M5}$	$(W/L)_{M6}$
$0.5\mu m/6\mu m$	$5\mu m/0.36\mu m$	$2\mu m/0.36\mu m$
$(W/L)_{PMOS,inv1}$	$(W/L)_{NMOS,inv1}$	$(W/L)_{PMOS,inv2}$
$20\mu m/0.12\mu m$	$10\mu m/0.12\mu m$	$20\mu m/0.12\mu m$
$(W/L)_{NMOS,inv2}$	$(W/L)_{PMOS,inv3}$	$(W/L)_{NMOS,inv3}$
$10\mu m/0.12\mu m$	$2\mu m/0.12\mu m$	$1\mu m/0.12\mu m$
$(W/L)_{PMOS,inv4}$	$(W/L)_{NMOS,inv4}$	$(W/L)_{PMOS,inv5}$
$4\mu m/0.12\mu m$	$2\mu m/0.12\mu m$	$8\mu m/0.12\mu m$
$(W/L)_{NMOS,inv5}$	$(W/L)_{PMOS,inv6}$	$(W/L)_{NMOS,inv6}$
$4\mu m/0.12\mu m$	$16\mu m/0.12\mu m$	$8\mu m/0.12\mu m$
C_L=10 pF	C_{VCDU}=50 fF	C_{par}=10 fF

Figure 2.8(a) shows the jitter histogram of the time difference between $\phi_{in}(t)$ and $\phi_{out}(t)$ of the fabricated VCDU using a real-time digital oscilloscope (Agilent DSA80000B). The measured mean and rms timing jitter are 4.58 ns and 8.99 ps, respectively, for 50,000 samples for V_{in}=0.7 V and 50 MHz clock frequency. Figure 2.8(b) presents the simulated jitter histogram of the VCDU, showing typical mean and rms jitter of 4.49 ns and 8.75 ps, respectively, at the same condition of experimental setup. Using (2.16) together with the jitter introduced by the

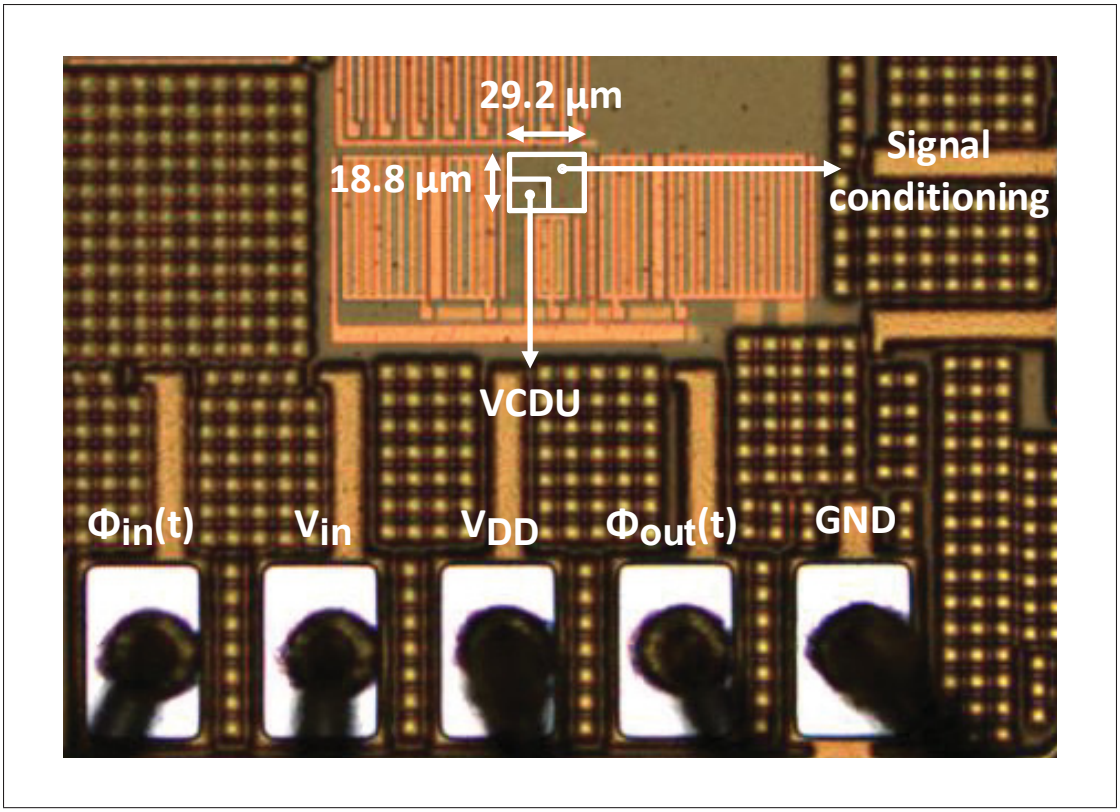
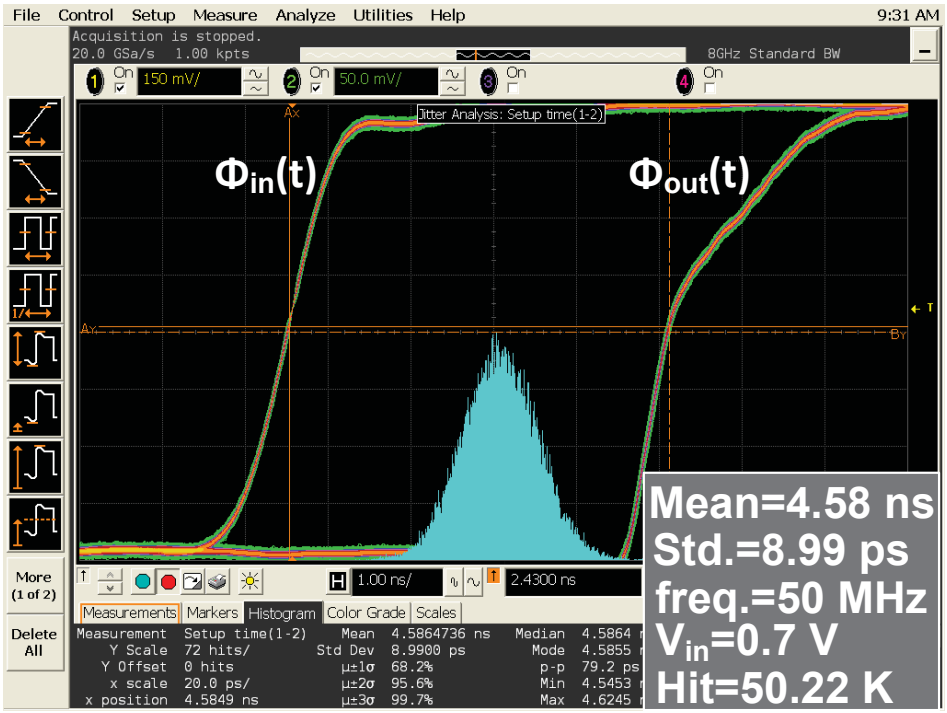


Figure 2.7 Die photograph.

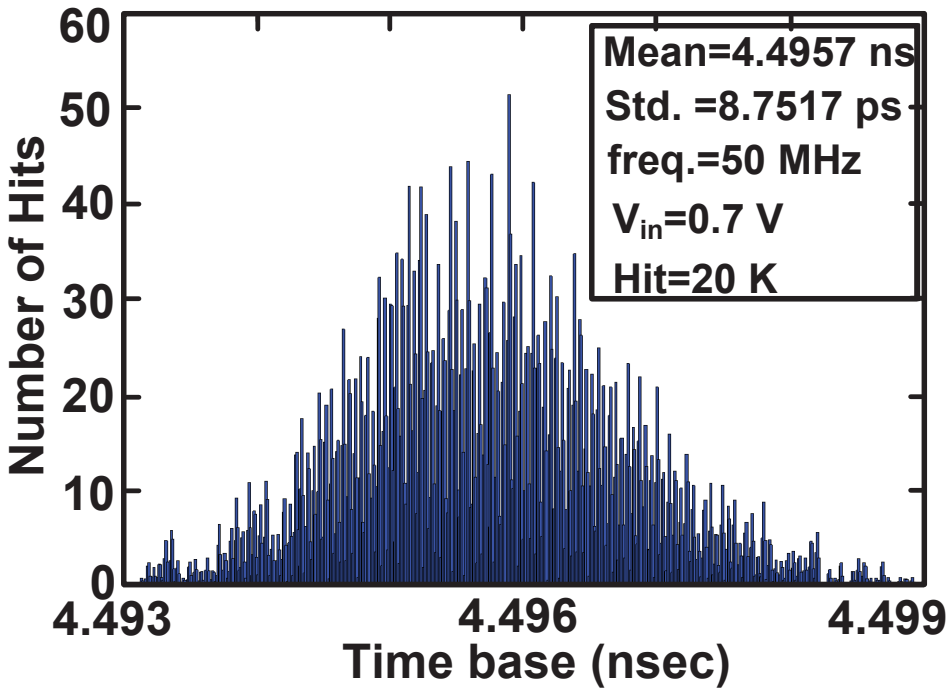
digital input and output drivers, the jitter for VCDU can be calculated as

$$\sigma^2_{t_{zc},total} = \sigma^2_{t_{zc},SDU} + \sigma^2_{t_{zc},Comparator} + \sum \sigma^2_{inv1-6} \tag{2.17}$$

One finds similar results for rms jitter: 8.73 ps, assuming Gaussian distributed noise. The results show a level of matching between our proposed analysis, simulation and experimental results. As a last test, we measured the rms jitter versus rise time for the VCDU circuit of Figure 2.6. These results, shown in Figure 2.9, again show the accuracy of the proposed analysis. The discrepancy being attributed to a statistical deviation.



a) Measurement.



b) Simulation.

Figure 2.8 Jitter histogram of the VCDU.

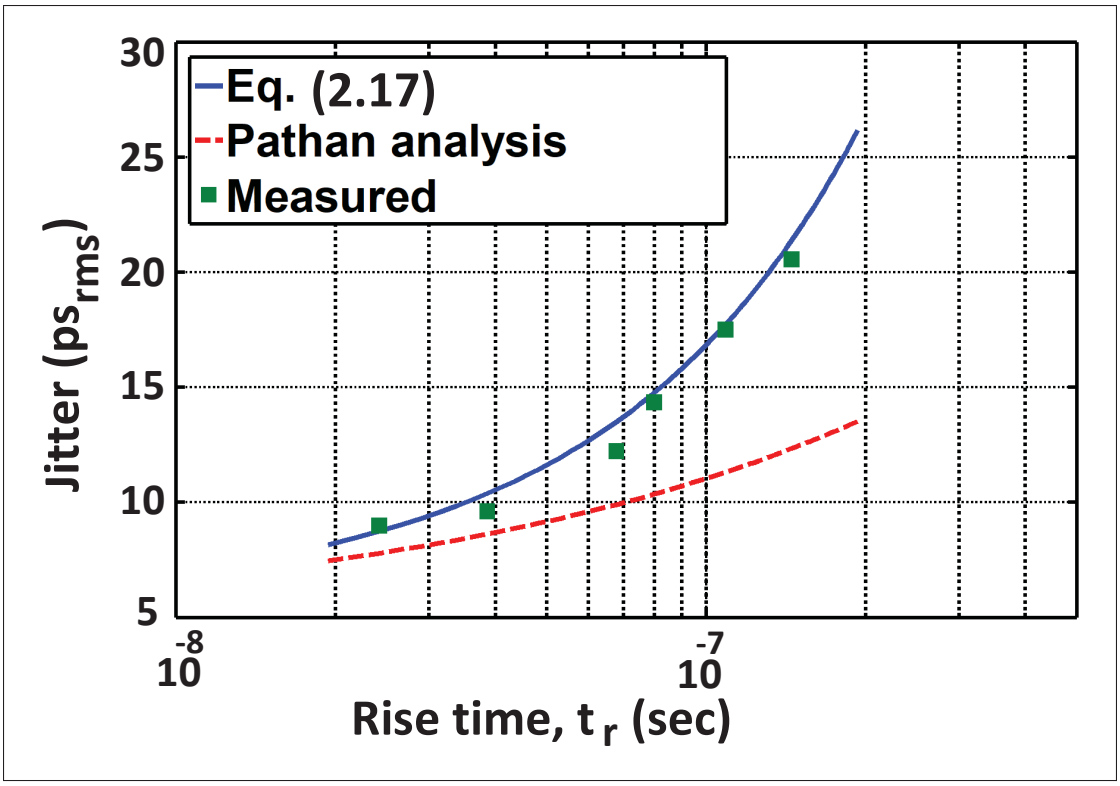


Figure 2.9 Comparison of jitter prediction with experimental results.

2.5 Summary

An analytical expression for the noise operation of both a VM and TM PMOS-NMOS transistor stack was derived, leading to the expression of the peak-SNR of both architectures. These results can easily be extended to more complicated TM circuits. This work extended the noise analysis of (A. Pathan *et al., 2016*) for TM circuits to include both thermal and flicker noise components, as well as the fact that the noise level will be influenced by the rise-time of the TM signals. The proposed noise theory was found to be consistent across different technology nodes through extensive transistor-level transient simulations and through noise experiments involving a custom chip in a 130 nm CMOS process. Our analysis shows that by around 90 nm feature size, TM circuits should provide better SNR than VM circuits for the same bandwidth. However, VM circuits having a longer history of design, they typically perform better than their TM counterparts. More research is therefore required to develop TM circuits that implement complex signal processing (mixing, conversion, filtering, etc.) with a high dynamic range.

CHAPTER 3

A SECOND-ORDER BANDPASS ΔΣ TIME-TO-DIGITAL CONVERTER WITH NEGATIVE TIME-MODE FEEDBACK

3.1 Introduction

One of the key building blocks in TMSP is the time-to-digital converters (TDCs), which are increasingly used in many applications, such as time-of-flight (ToF) (Vornicu *et al.*, 2017), jitter measurement (K. No *et al.*, 2006), medical imaging (Chen *et al.*, 2017), all-digital PLL (ADPLL) (Avivi *et al.*, 2017), and time-domain ADCs (Naraghi *et al.*, 2010; Daniels *et al.*, 2010). It is mainly because of this reason that TDCs seem to offer the means to get around many of the obstacles facing analog circuits as one moves to advanced CMOS technology nodes (40 nm or less) (see chapter 3). In addition, TDCs provide the opportunity to employ highly efficient digital circuits to realize very complex mixed-signal circuits (Kim, *et al.*, 2013). Consequently, it is expected that TDCs achieve high-performance (i.e., resolution, bandwidth, dynamic range, etc.) with the continued scaling the technology nodes.

Various implementations of TDCs have been proposed to process TM information in the range of sub-nanosecond or even sub-picosecond resolution. Some successful examples of TDCs are reported in literature (Jansson *et al.*, 2009; Chen *et al.*, 2000; Lu *et al.*, 2012; Vercesi *et al.*, 2010; Yu *et al.*, 2010; Roberts *et al.*, 2010; Yu *et al.*, 2010; Young *et al.*, 2010; Gande *et al.*, 2012; Straayer *et al.*, 2009; Yu *et al.*, 2015; Elshazly *et al.*, 2014). In all of the TDC implementations published thus far, the operation of these circuits is restricted to LP baseband operation.

In this work, we take a step further by proposing for the very first time a second-order BPΔΣTDC using digital-like TM arithmetic circuits suitable for bandpass data conversion. The BPΔΣTDC is designed to operate over a wide range of sampling frequencies, while taking advantage of the technology scaling. The closed-loop TDC is designed using a TM LDI-based resonator, TM subtractor, and an all-digital DTC in a feedback loop. Two different techniques with dig-

ital implementation are applied to adjust the timing variations from the main system clock, synchronization and TM phase alignment. In addition, a feed-forward topology is employed to improve the SNDR.

Most of the material from this chapter is adapted from:

S. Ziabakhsh, G. Gagnon, G. W. Roberts, "A Second-Order Bandpass ΔΣ Time-to-Digital Converter with Negative Time-Mode Feedback," *IEEE Transactions on Circuits and Systems I: Regular Papers*, Submitted April 19, 2018.

3.2 New TM Building Blocks And Extensions To Some Old Ones

3.2.1 Previous Work

The architecture of the proposed BPΔΣTDC is based on a TM memory cell (TLatch) that is able to store (or write) the input time-difference and latch it for further processing (i.e., addition, subtraction, multiplication, or division) (Ali-Bakhshian *et al.*, 2012). To realize this concept, an inverter-like structure called a switched-delay unit (SDU) is employed to provide the voltage-controlled delay cell with an on-off switch (SW) in the discharging path. The circuit schematic of the SDU is shown in Figure 3.1(a). PMOS transistor M_1 serves as a current source to charge capacitor C and $M_2 - M_4$ provides a discharging path for the capacitor. An additional digital inverter is employed to provide a suitable digital signal at the output when the voltage of the capacitor (V_{Cap}) crosses the threshold voltage of the inverter (V_{TH}). The time-difference between the rising edge of CLK to the rising edge of Φ_{out} is a fixed value and denoted as T_{SDU}. The timing diagram of the SDU is illustrated in Figure 3.1(b). The capacitor starts to discharge from V_{DD} to ground when CLK is set high. However, if SW is activated low with some pulse-width ΔT_{SW}, the discharge process will be stopped and the voltage across capacitor V_{Cap} will be kept constant. In essence, this action has delayed the discharge time by exactly ΔT_{SW} seconds, resulting in a low-to-high transition appearing at the output $T_{SDU} + \Delta T_{SW}$ seconds later.

Figure 3.1(c) displays the block diagram of the TLatch, which is composed of a pair of SDUs and some digital gates. During the write mode when $\overline{W}$=0 and $\overline{R_{ref}}$=$\overline{R_{sig}}$=1, the time-difference between the rising edges of $\Phi_{in,ref}$ and $\Phi_{in,sig}$, denoted as ΔT_{in}, is stored in the form of charge into the capacitors of the two SDUs and retrieved after the arrival of the two falling edges at the read ports, $\overline{R_{ref}}$ and $\overline{R_{sig}}$. In the read mode, the stored TM information with the same value of input (ΔT_{in}) can be detected at the output after some internal propagation delay (i.e., T_{SDU}) (Ali-Bakhshian *et al.*, 2012).

The timing diagram of the input/output ports as well as the internal connections of the TLatch are illustrated in Figure 3.1(d). The top two plots show the ideal reference ($\Phi_{in,ref}$) and signal clocks ($\Phi_{in,sig}$); the next plot below shows the write signal ($\overline{W}$). This signal is activated on the rising edge of the $\Phi_{in,ref}$ and deactivated on the rising edge of $\Phi_{in,sig}$. The reset signal as depicted in the fourth plot from the top is a global signal and initializes the digital gates of TLatch in each clock cycle. Read signals ($\overline{R_{ref}}$ and $\overline{R_{sig}}$) are set equal to $\Phi_{in,ref}$ so that the output can be read shortly after the arrival of the falling edge at $\Phi_{in,ref}$. Two internal signals, $Trig$ and $SW_{R,S}$, are plotted to illustrate the operation of each digital block. The bottom two plots show the two output signals with time-difference ΔT_{out}. Relative to the input TM signal, the output TM signal is set after a half-period delay of the reference clock $\Phi_{in,ref}$ having a 50% duty cycle. Mathematically, the output TM signals ΔT_{out} can be written as the addition/subtraction of a half-period delay of ΔT_{in} and the time-difference between the two input read signals $\overline{R_{ref}}$ and $\overline{R_{sig}}$ as follows

$$\Delta T_{out}[n] = \Delta T_{in}[n-\frac{1}{2}] \pm \Delta T_R[n] \tag{3.1}$$

where

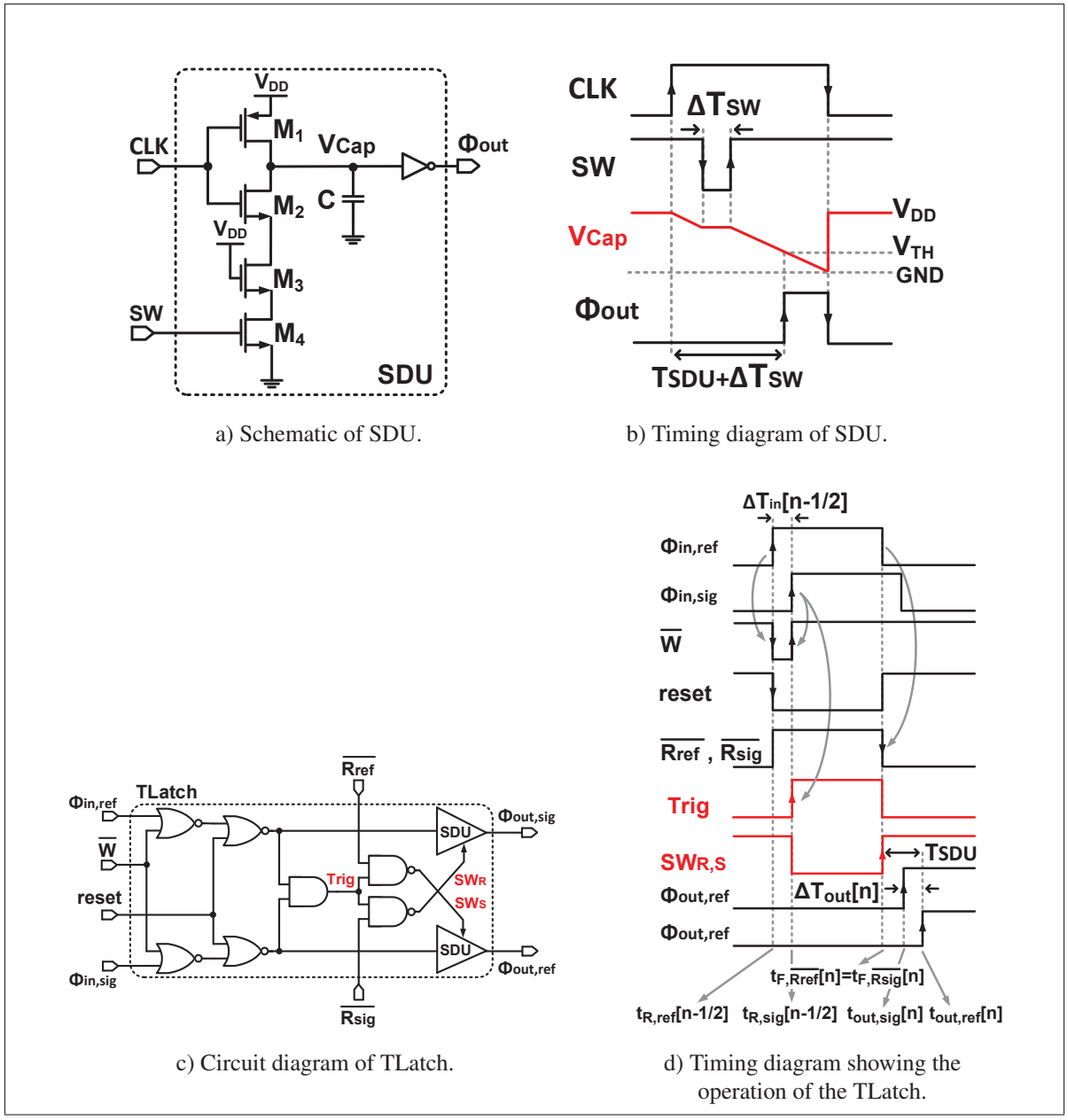
$$\Delta T_{in}[n-\frac{1}{2}] = t_{R,ref}[n-\frac{1}{2}] - t_{R,sig}[n-\frac{1}{2}] \tag{3.2}$$

and

$$\Delta T_R[n] = t_{F,\overline{R_{ref}}}[n] - t_{F,\overline{R_{sig}}}[n] \tag{3.3}$$

Here, t_R and t_F are denoted as the time instance of arrival of the rising and falling edges of input digital signals, respectively. In addition, to represent the half-period delay, we make use

of the time index (n-1/2) to represent the second half portion of the nth-cycle of the reference clock signal $\Phi_{in,ref}$. An equivalent z-domain model for the TLatch can then be described with the block diagram shown in Figure 3.2.



a) Schematic of SDU.

b) Timing diagram of SDU.

c) Circuit diagram of TLatch.

d) Timing diagram showing the operation of the TLatch.

Figure 3.1 SDU and VCDU.

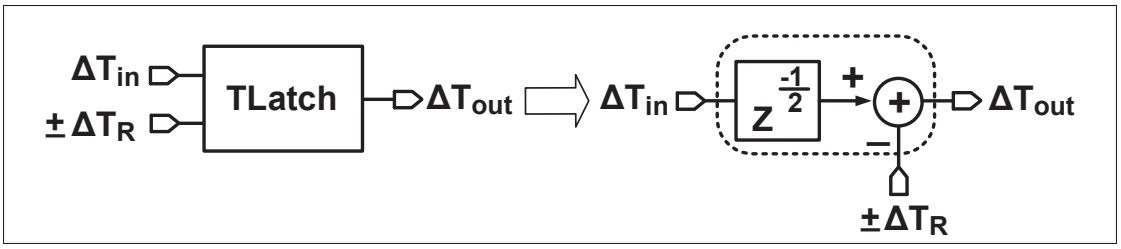


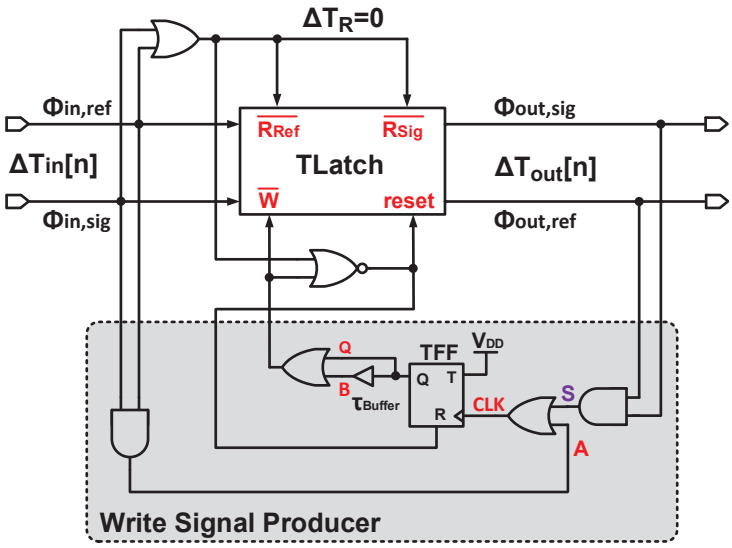
Figure 3.2 TLatch equivalent model in z-domain.

In the following subsections, we shall describe several the new TM building blocks used in this work: (B) the half-period delay unit, (C) cascading of two half-period delay units, (D) adaptive time offset correction, (E) a TM subtractor and (F) the half-period delay DTC. Ultimately, these will be combined to form the TM LDI-based resonator circuit - the core component of the BPΔΣTDC.

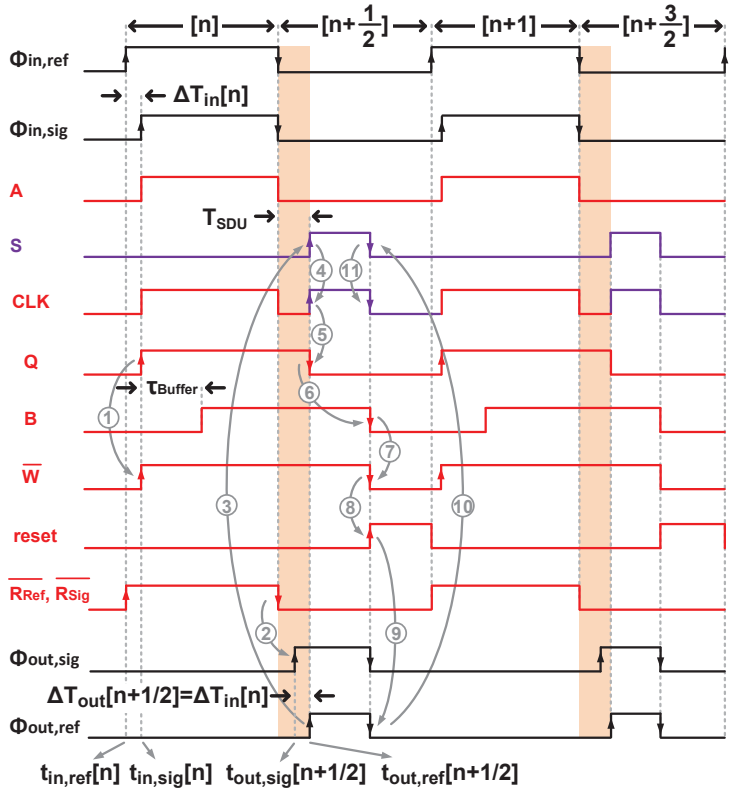
3.2.2 Half-Period Delay Unit

The circuit schematic of the half-period delay unit is shown in Figure 3.3(a). At its core is a TLatch with some random and sequential logic to control its read, write, and reset signals. These signals are generated by a block identified in the diagram as the Write Signal Producer. The operation of the overall circuit can be described with the aid of the timing diagram shown in Figure 3.3(b). Let us first consider two input signals, $\Phi_{in,ref}$ and $\Phi_{in,sig}$. Here $\Phi_{in,ref}$ is assumed to be a periodic signal with period T_s having a 50% duty cycle. To explain the operation of the circuit, we start from the initial condition when the $\overline{W}$="0", $\overline{R_{ref}}$=$\overline{R_{sig}}$="1", and the T-Flip-Flop (TFF) is reset to its logic low state (i.e., Q =0). In this situation, the TLatch captures the time-difference between two rising edges at $\Phi_{in,ref}$ and $\Phi_{in,sig}$. Upon the arrival of the rising edge at $\Phi_{in,sig}$, say at time $t_{in,sig}[n]$, the *CLK* input of the TFF will be set to "1" and this changes the output of TFF (Q) from "0" to "1". When Q=1, the write signal of the TLatch ($\overline{W}$) will be set to "1" and the TLatch will be placed into an idle state.

On the arrival of the falling edge at $\Phi_{in,ref}$, both $\overline{R_{ref}}$ and $\overline{R_{sig}}$ go logically low, the two SDUs inside the TLatch begin to discharge towards ground, and deliver the rising edges at the output



a) Circuit implementation of the TLatch with improved timing precision.



b) Operational timing diagram.

Figure 3.3 Half-Period Delay Unit.

of the TLatch. When the signal $\Phi_{out,ref}$ is set to a logic high, the digital AND gate connected to the output ports in the Write Signal Producer will set the signal S to "1" in order to reset the TFF to "0" and change the state of $\overline{W}$ to "0." There is a small intensional delay τ_{Buffer} created by a buffer between the output of TFF and the B input to the OR gate. This delay is used to set the pulse-width of the output signal $\Phi_{out,ref}$. After the output rising edges are read out completely (i.e., both TLatch outputs are set high), the TLatch and TFF will be reset by a NOR gate and ready to store the next TM sample value. Assuming this condition is met, the half-period delay cell will automatically store positive/negative TM signals, latch, deliver, and reset itself after each cycle. As a result, the output pair of the rising edges will appear at

$$t_{out,ref}[n+\frac{1}{2}] = \frac{T_s}{2} + T_{SDU} \tag{3.4}$$

and

$$t_{out,sig}[n+\frac{1}{2}] = \frac{T_s}{2} + T_{SDU} - \Delta T_{in}[n] \tag{3.5}$$

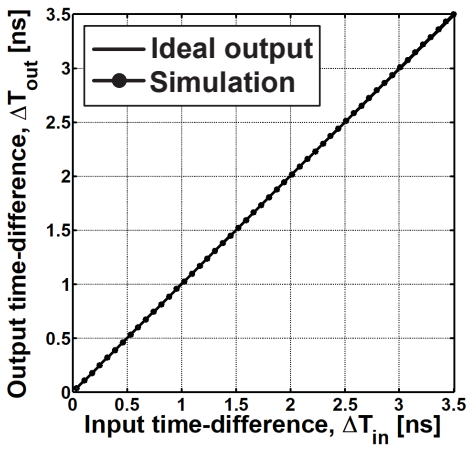
where T_{SDU} represents the propagation delay of SDUs inside the TLatch, and T_s is the period of the ideal reference clock. This propagation delay introduces a signal-independent time offset for both paths. Using (3.4) and (3.5), a difference equation representing the output from the TLatch ($\Delta T_{out}[n]$) can be written as

$$\begin{aligned} \Delta T_{out}[n+\frac{1}{2}] &= t_{out,ref}[n+\frac{1}{2}] - t_{out,sig}[n+\frac{1}{2}] \\ &= \Delta T_{in}[n] \end{aligned} \tag{3.6}$$

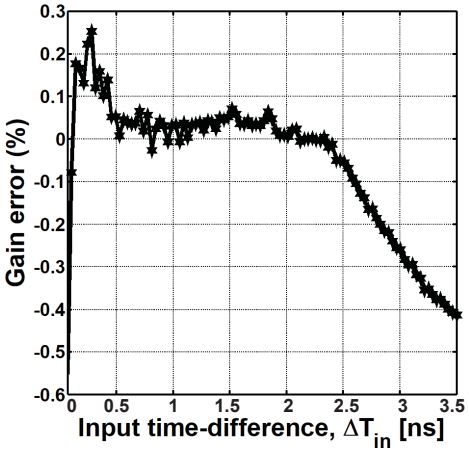
As seen from (3.6), $\Delta T_{out}[n+\frac{1}{2}]$ is not dependent on the time offset term $T_s/2 + T_{SDU}$.

The output time-difference, ΔT_{out}, for the half-period delay unit is simulated in a 1.2 V IBM 130 nm CMOS process for different input time-differences ranging from 0 to 3.5ns operating with a reference clock of f_s=42.8 MHz. The output response versus input time-differences is shown in Figure 3.4(a). As is evident, the simulated ΔT_{out} follows quite closely with a straight line behavior. The relative gain error transfer curve shown in Figure 3.4(b) was found to be less than 0.5% in magnitude across the input range from 0 to 3.5ns, which is approximately 15%

of the reference clock period. This range can be increased up to the full clock period T_s at the expense of a lower operating frequency, as larger SDU capacitors will be required to reduce charge leakage effects.



a) Input-output transfer characteristic.

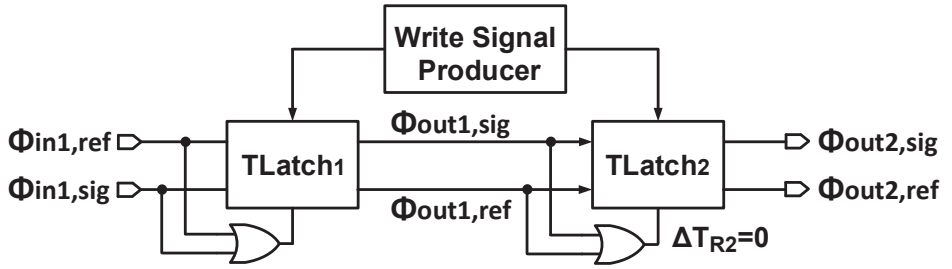


b) Gain error for the TLatch circuit shown in Figure 3.3(a) as found by Spectre simulation. Note that the time offset is zero for ΔT_{out}.

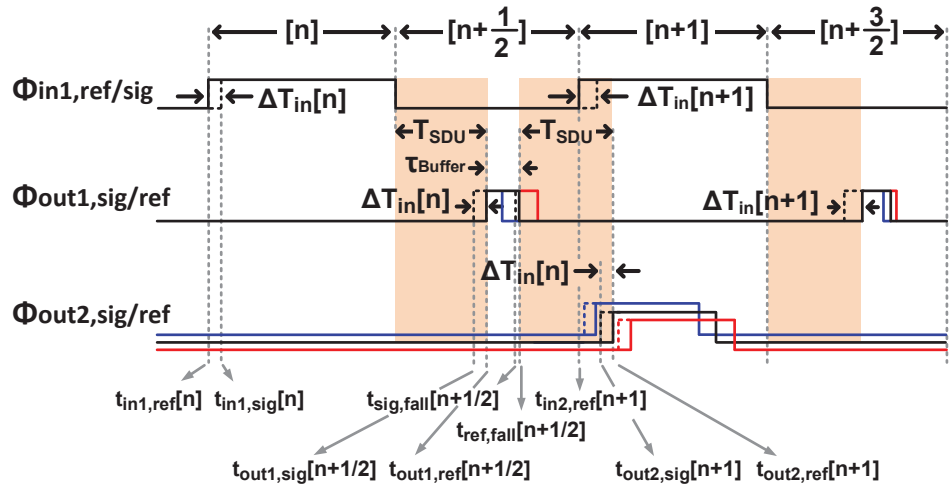
Figure 3.4 Simulation results.

3.2.3 Cascading Of Two Half-Period Delay Units

An essential feature of the half-period delay circuit shown in Figure 3.3(a) is its ability to be cascaded to create a larger delay. For instance, a one-period delay (z^{-1}) can be realized by cascading two half-period delay cells. To complete the circuit, the input and read ports of the second TLatch (TLatch_2) are connected directly to the output ports of the first TLatch (TLatch_1). This is shown in Figure 3.5(a). However, prototypes of the realization have been found to be sensitive to device mismatches among elements in the Write Signal Producer (i.e., digital buffer, digital gates) and the SDU elements of the TLatches leading to a nonlinear transfer characteristic. Figure 3.5(b) shows the timing diagram of a TLatch cascade. To simplify our presentation, the input and reference signals are superimposed on top of one another, thereby



a) Block diagram.



b) Timing diagram ($T_{SDU} = T_s/4$). $\Phi_{in1,ref/sig}$ represents the signals $\Phi_{in1,ref}$ and $\Phi_{in1,sig}$, respectively, and $\Phi_{out1-2,sig/ref}$ represents the signals $\Phi_{out1-2,sig}$ and $\Phi_{out1-2,ref}$, respectively.

Figure 3.5 Cascaded two half-period delays without TFFs.

highlighting the time-difference signal. This notation will be used extensively throughout this chapter.

The input TM signal is delayed by a half-period clock to generate the signals $\Phi_{out1,ref}$ (solid line) and $\Phi_{out1,sig}$ (dashed line). In this situation, the time difference between $\Phi_{out1,ref}$ and $\Phi_{out1,sig}$ is latched by the TLatch$_2$ and is kept until the falling edge of the sum of these two signals arrive to initiate the read out of this TLatch (using OR gate in Figure 3.5(a)). Unlike the time-to-time integrator in the TM biquadratic filter realization (Abdelfattah *et al.*, 2017),

where the output signals of TLatch_1 are propagated through the next TLatch and connected to the read signals of TLatch_2, in our case it is much more convenient to use the falling edges of $\Phi_{out1,ref}$ and $\Phi_{out1,sig}$ to read out the latched data at the output of the TLatch_2 at the proper time. However, the falling edges at the output of the TLatch_1, say at time $t_{ref,fall}[n+1/2]$ and $t_{sig,fall}[n+1/2]$, can occur at any time between the rising edge of $\Phi_{out1,ref}$ and the next rising edge of $\Phi_{in1,ref}$, where

$$t_{ref,fall}[n+\frac{1}{2}] = \frac{T_s}{2} + T_{SDU1} + \tau_{Buffer1} \tag{3.7}$$

and

$$t_{sig,fall}[n+\frac{1}{2}] = \frac{T_s}{2} + T_{SDU2} + \tau_{Buffer2} \tag{3.8}$$

Here T_{SDU1} and T_{SDU2} represent the propagation delay of SDU_1 and SDU_2, respectively, inside TLatch_1, and $\tau_{Buffer1}$ and $\tau_{Buffer2}$ represent the individual delay of each buffer in the two Write Signal Producer circuits. The rising edges at $\Phi_{out2,ref}$ and $\Phi_{out2,sig}$ as a function of the n-th cycle of the input reference clock, $\Phi_{in1,ref}$, occur at

$$t_{out2,ref}[n+1] = \frac{T_s}{2} + 2 \times T_{SDU1} + \tau_{Buffer1} \tag{3.9}$$

and

$$t_{out2,sig}[n+1] = \frac{T_s}{2} + 2 \times T_{SDU2} + \tau_{Buffer2} - \Delta T_{in}[n] \tag{3.10}$$

Equations (3.9) and (3.10) illustrate that the output pair of rising edges of TLatch_2 are dependent on T_{SDU1} and T_{SDU2} and the digital buffer delay of the Write Signal Producer block in TLatch_1, which is often difficult to set precisely. This issue becomes more serious in face of PVT variations. In addition, the T_{SDU} of each TLatch needs to be designed exactly equal to $T_s/4$ in order to realize the desired transfer function z^{-1}. Using (3.9) and (3.10), a recursive difference equation representing the output of the cascaded half-period delays can be written

as

$$\begin{aligned}\Delta T_{out}[n+1] &= t_{out2,ref}[n+1] - t_{out2,sig}[n+1] \\ &= \Delta T_{in}[n] + 2\times(T_{SDU1} - T_{SDU2}) \\ &\quad + \tau_{Buffer1} - \tau_{Buffer2}\end{aligned} \tag{3.11}$$

Clearly, the differences in the delays along each signal path introduces a unique time offset. To minimize this offset, two additional TFFs can be placed in cascade with the output of each TLatch as shown in Figure 3.6(a). The TFFs are synchronized with the falling edges of signals $\Phi_{TL-out1,ref}$ and $\Phi_{TL-out1,sig}$ together with the next rising/falling edge of $\Phi_{in1,ref}$. In the circuit of Figure 3.6(a), the outputs of each TLatch are connected to the clock ports of TFFs. Upon the arrival of a pair of rising edges at $\Phi_{TL-out1,ref}$ and $\Phi_{TL-out1,sig}$, the outputs of the TFFs will change their states to "1" and will be remained unchanged. On occurrence of the rising/falling edge of the reference clock $\Phi_{in1,ref}$ (rising edge for the first pair of TFFs and falling edge for the second pair of TFFs), the outputs of TFFs will be changed to "0" resulting in a synchronization of the falling edges of TLatches with the reference clock $\Phi_{in1,ref}$. Consequently a pulse of fixed width is produced at the TLatch output independent of any digital component mismatch. Subsequently, the output signals $\Phi_{out2,ref}$ and $\Phi_{out2,sig}$ are no longer dependent on any internal buffer delay, as a detail analysis reveals (see Figure 3.6(b)) that the rising edge transitions are located at the following time instances:

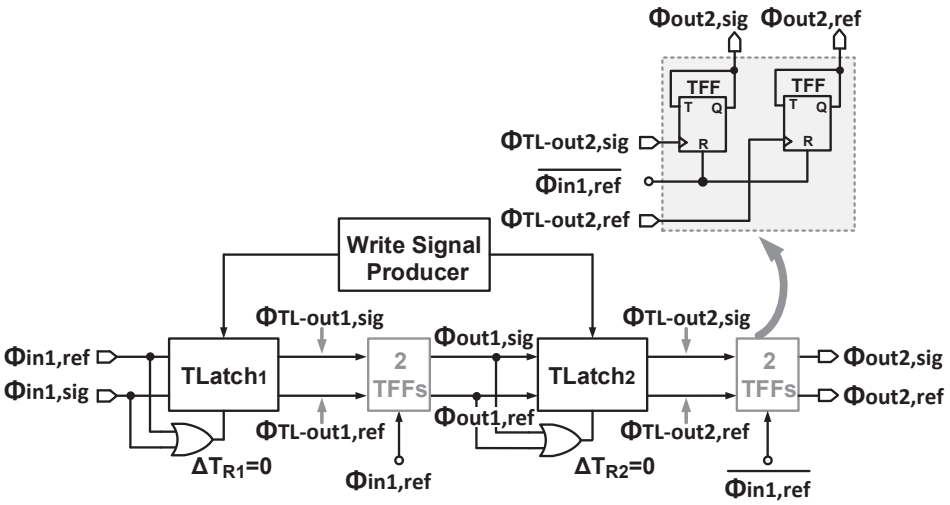
$$t_{out2,ref}[n+1] = T_s + T_{SDU1} \tag{3.12}$$

and

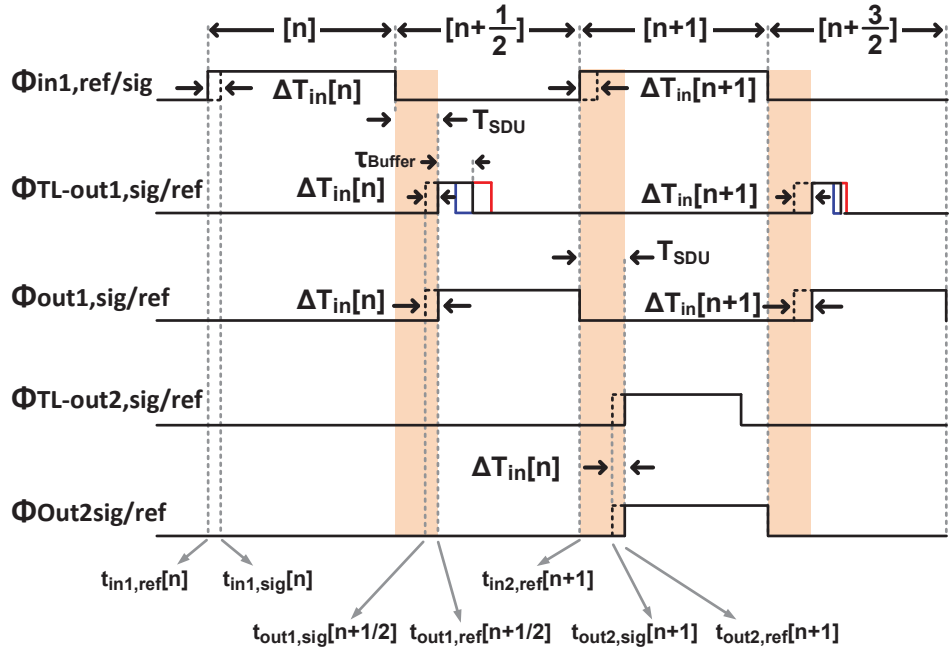
$$t_{out2,sig}[n+1] = T_s + T_{SDU2} - \Delta T_{in}[n] \tag{3.13}$$

Using (4.1) and (3.13), the recursive time-difference equation for the $(n+1)$-th time instance will be equal to $\Delta T_{out}[n+1] = \Delta T_{in}[n] + T_{SDU1} - T_{SDU2}$. As is evident, the addition of the TFFs eliminate the effect of the buffer mismatches on the Tlatch time offset.

To see the sensitivity of the rising edges of TLatch_2 with and without TFFs in the presence of transistor mismatches among the digital components in the Write Signal Producer and



a) Block diagram.

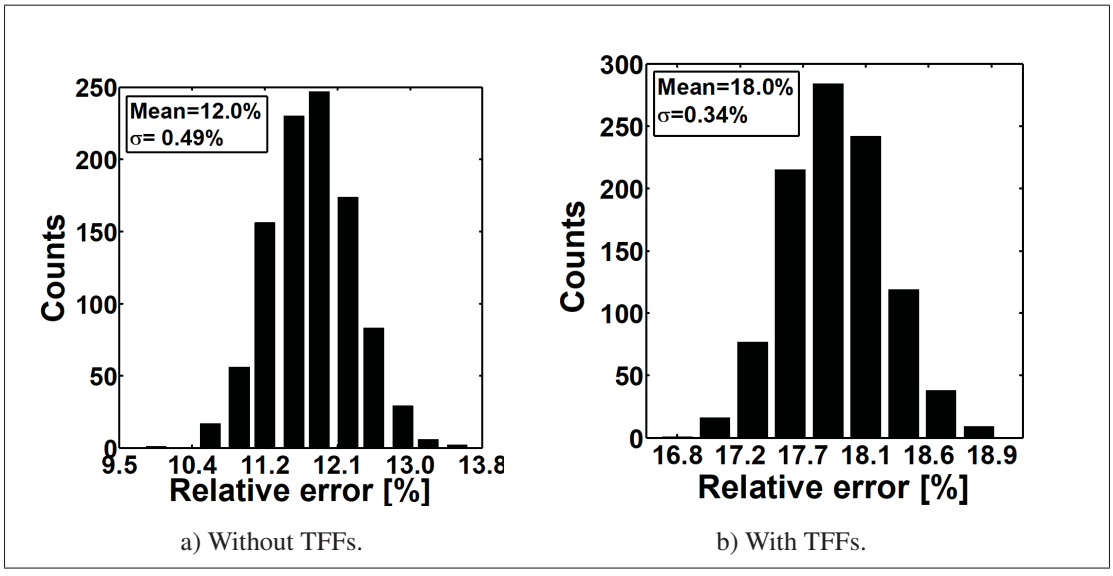


b) Timing diagram ($T_{SDU} < T_s/4$).

Figure 3.6 Cascaded two half-period delays with TFFs.

TLatches, the circuits shown in Figure 3.5(a) and Figure 3.6(a) were simulated at the transistor level using the Monte-Carlo analysis within Spectre. In this simulation, the widths of

individual transistors were assigned a random value drawn from a Normal distribution with a mean value set to its nominal value and a sigma equal to 10% of this value. Two digital square-wave signals at a frequency of 42.8 MHz with a time offset $\Delta T_{in}[n]$ set to 500ps was applied to the input of the unit delay cell (cascade of two half-delay cells). The time-difference between the input rising reference signal $\Phi_{in1,ref}$ and the corresponding output reference signal $\Phi_{out2,ref}$ was evaluated relative to the period of the reference clock T_s, i.e., $\frac{t_{out2,ref}[n+1]-t_{in1,ref}[n]}{T_s}$. Figure 3.7(a) shows the histogram of the input-output delay for the circuit shown in Figure 3.5(a). Here the input-output time delay exceeded the reference period with a mean value 12% larger than the ideal expected value. Moreover, the overall input-output delay experienced a standard deviation σ of 0.49%. In contrast, Figure 3.7(b) shows the histogram of the output delay when TFFs are used at the output of the TLatches. Here one sees that the input-output delay increased slightly to 18% but, more importantly, its σ reduced to 0.34%. While the latter circuit approach introduced a larger output-referred time offset, this offset can be further reduced with the introduction of an adaptive delay circuit.



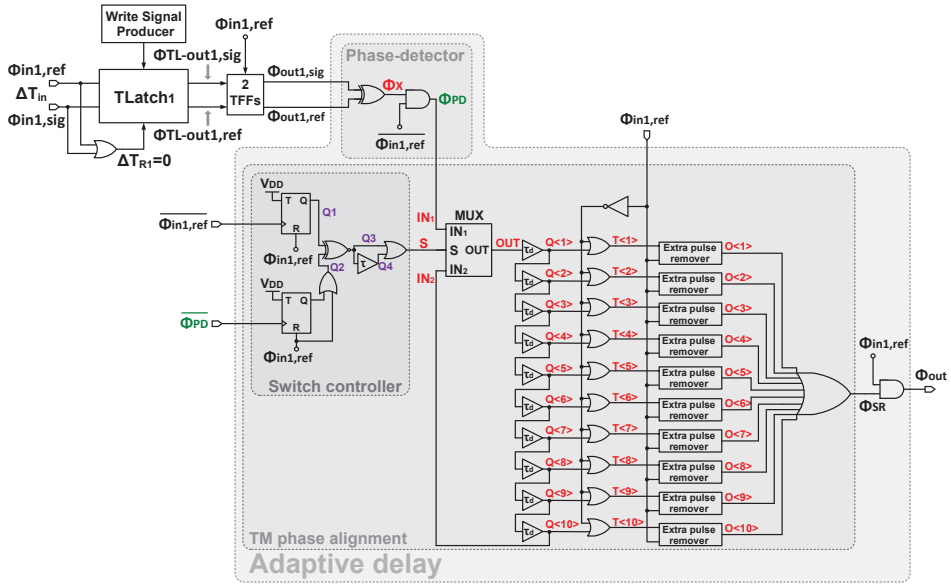
a) Without TFFs. b) With TFFs.

Figure 3.7 Monte-Carlo simulations ($N = 1000$ samples) of the cascaded half-period delays.

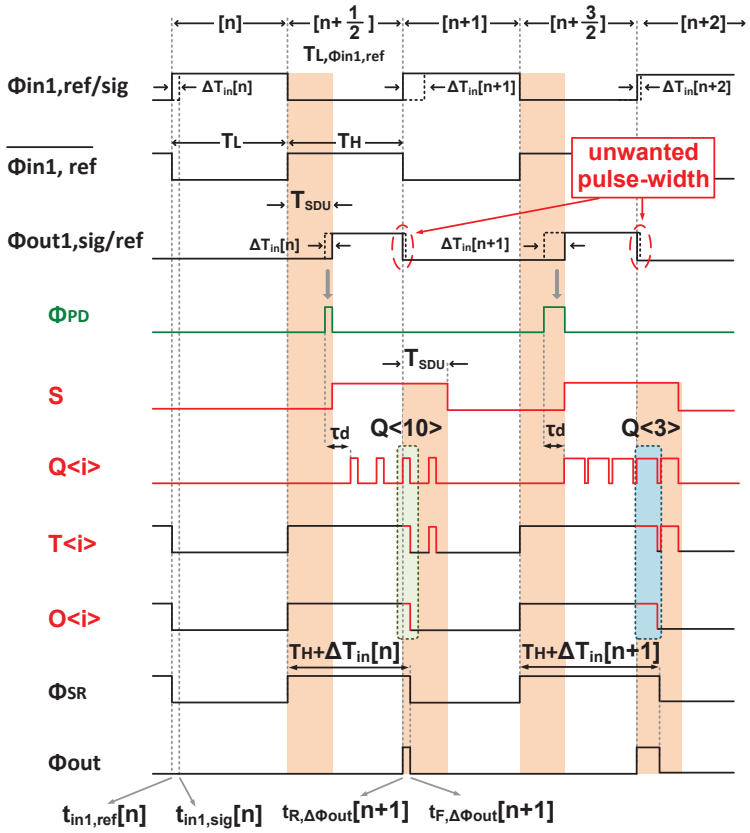
3.2.4 Adaptive Time Offset Correction

While the cascading of two half-period delay block described in the previous section (Figure 3.6(a)) offers full-period delay, its input-output delay contains a fairly large time offset. Fortunately, this problem can be reduced by designing an adaptive delay block, which is capable of producing a fractional-period delay to compensate for any time offset. The block diagram of the cascaded half-period delay with an adaptive delay along with its detailed timing diagram is shown in Figure 3.8. The adaptive delay block receives the output time-difference of TLatch_1 (time-difference between the rising edges of signals $\Phi_{out1,ref}$ and $\Phi_{out1,sig}$) and produces an output signal $\Delta\Phi_{out}$ that is aligned with the rising edge of the reference signal $\Phi_{in1,ref}$. It consists of two main components: a phase-detector and a TM phase alignment circuit. The phase detector provides a pulse-width signal that corresponds to the time-difference between the rising edges of $\Phi_{out1,sig}$ and $\Phi_{out1,ref}$. This can be realized by using a digital XOR gate at the output of TLatch_1. However, this time-difference extraction may contain significant nonlinear components related to the falling edges of $\Phi_{out1,ref}$ and $\Phi_{out1,sig}$. To remove these, the output node of the XOR gate labeled Φ_X is synchronized by the reference clock with an additional digital AND gate to eliminate the unwanted pulse-width signal that occurs after the falling edges of $\Phi_{out1,ref}$ and $\Phi_{out1,sig}$. The output of the phase-detector (signal Φ_{PD}) is directly connected to a TM phase alignment circuit for precise edge placement.

The TM phase alignment circuit is shown in Figure 3.8(a). It contains a switch controller block, a multiplexer, an inverter-based delay line, extra pulse remover blocks and a digital ten-input OR gate. The output of the switch controller block is initially low (S="0") and enables the Φ_{PD} pulse signal to arrive at the output port of the multiplexer (MUX). The MUX output then propagates through the inverter-based delay line to generate signals $Q<1>$ to $Q<10>$. After the arrival of the falling edge of signal Φ_{PD}, selection signal S is set to a logic "1" and stay at this level until a T_{SDU} delay after the next rising edge of the reference clock $\Phi_{in1,ref}$. The second input to the MUX labeled IN_2 is now connected to the MUX output (OUT). This, in turn, closes the loop around the delay line allowing the line to reset itself. Using this technique, there will always be one signal of $Q<i>$ (i=1 to 10) that is aligned with the reference clock.



a) Circuit diagram.



b) Timing diagram.

Figure 3.8 Cascaded half-period delay with an adaptive delay block.

The ten outputs from the delay line are compared to the low-portion of the reference clock (labeled as T_H) using a bank of two-input OR gates. Subsequently, only those pulses that overlap with the low-portion of the reference clock $\Phi_{in,ref}$ are passed (signals $T<i>$). In order to remove additional pulses that appear after the low activation of $T<i>$, some additional filtering is performed using the extra pulse removal circuits. The outputs of the circuits are then added together by a ten-input OR gate to produce Φ_{SR}. Consequently, Φ_{SR} will be set high for a duration equal to the duration of the low-portion of the reference clock and the duration of the Φ_{PD} signal. The time difference between the falling edge of Φ_{SR} and the rising edge of $\Phi_{in,ref}$ is used to generate an output signal Φ_{out} with a pulse-width equal to that established by Φ_{PD} using a two-input AND gate with no offset with respect to the rising edge $\Phi_{in,ref}$.

To illustrate this operation, a timing diagram is presented in Figure 3.8(b). During the n-th clock cycle, $Q<10>$ is aligned with the falling edge of $\overline{\Phi_{in,ref}}$ and during the next clock cycle, $Q<3>$ is aligned with the falling edge of $\overline{\Phi_{in,ref}}$. Here, the extra pulse remover block eliminates the extra shifted of the Φ_{PD} signal and generate signal Φ_{SR} whose pulse-width is $T_H+\Delta T_{in}$. Digitally multiplying the Φ_{SR} with $\overline{\Phi_{in1,ref}}$ results in a well-aligned output signal, Φ_{out}.

Figure 3.9 shows the circuit schematic and the timing diagram of the extra pulse remover circuit. The *valid controller logic* generates the signals $\overline{En}$ and reset (R) for the TFF with a delay of $\tau = T_{SDU}$ from the input reference clock $\Phi_{in1,ref}$. The signal $\overline{En}$ is digitally multiplied by the input signal $T<i>$ to produce the signal A which eliminates the most shifted signal of Φ_{PD}. Signal R sets the $\overline{Q}$ of TFF to level "1" and keeps its state until the falling edge of $T<i>$ has arrived. The $\overline{Q}$ and A are then multiplied together using a two-input AND gate to produce the output $O<i>$ signal without any additional pulses.

To verify the operation of the circuit shown in Figure 3.8(a), a Monte-Carlo simulation was performed to obtain the output delay from the rising edge of the reference clock, say at time $t_{in1,ref}[n]$, to the rising edge of Φ_{out} when subject to the same device mismatches described earlier. Figure 3.10 shows the relative error histogram for the cascaded half-period delay with

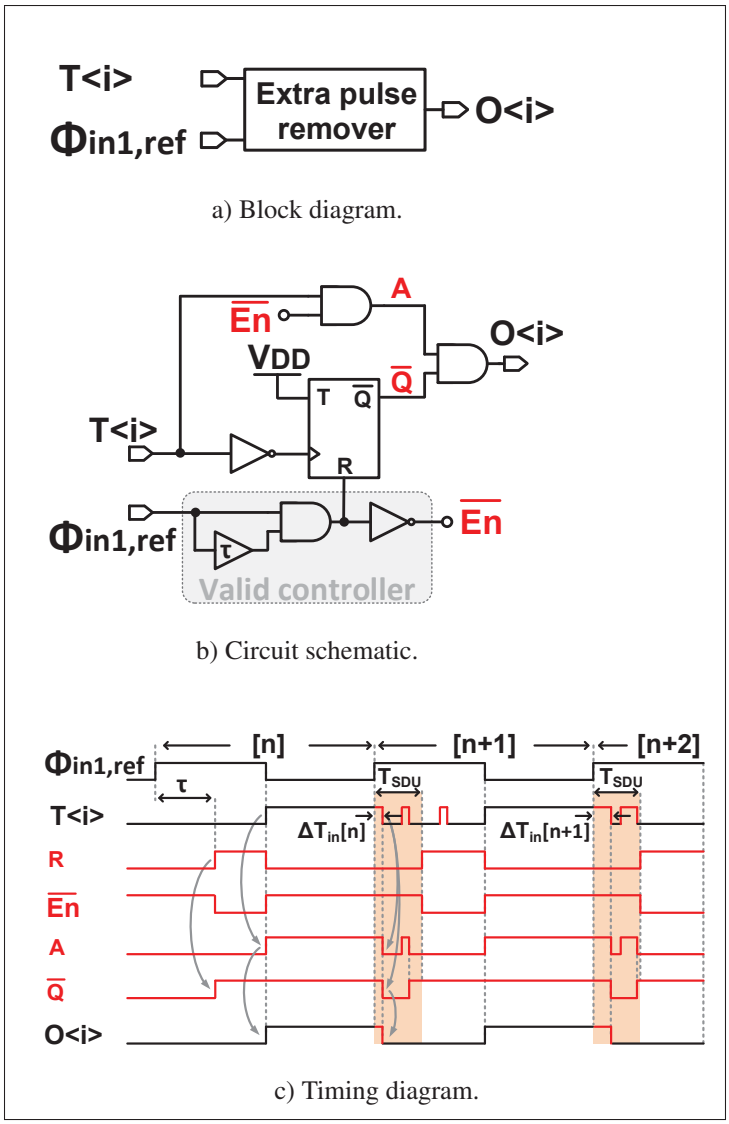


Figure 3.9 Extra pulse remover.

an adaptive delay circuit. The error histogram appears Gaussian with a mean and a standard deviation of 0.1% and 0.095%, respectively. As is evident, the offset has been greatly reduced without increased sensitivity to device mismatches.

Figure 3.11 depicts the simulated output time error (t_{error}) versus input time-difference $\Delta T_{in}[n]$ with different processes (FF, TT, and SS), supply voltage (1.2 V $\pm$ 0.12 V), and temperature (0°C - 80°C). For this simulation, t_{error} is calculated by the difference between ϕ_{out} and ϕ_{PD}. As shown, the t_{error} of the TM phase alignment remains below $\pm$30ps.

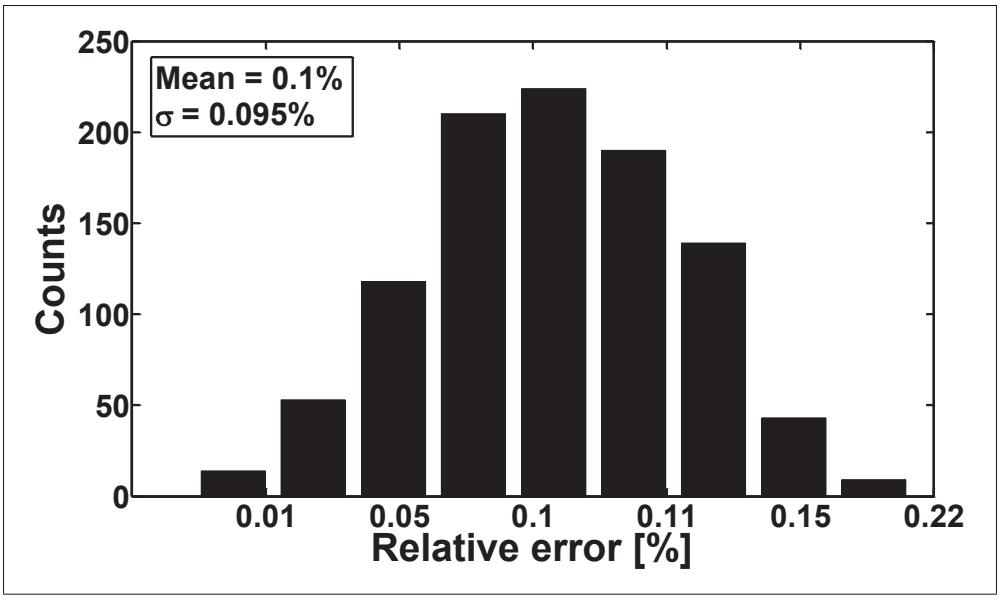


Figure 3.10 Monte-Carlo analysis (N = 1000 samples) for the transistor mismatches ($\Delta T_{in} = 500$ ps, $T_{SDU} = T_s/8$, and $f_s = 42.8$ MHz).

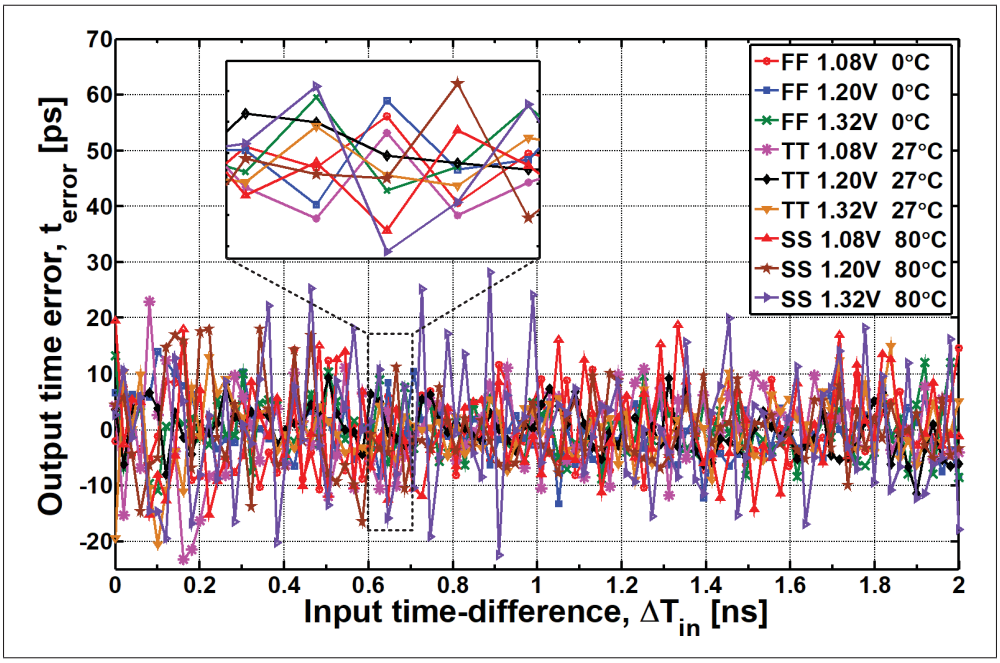


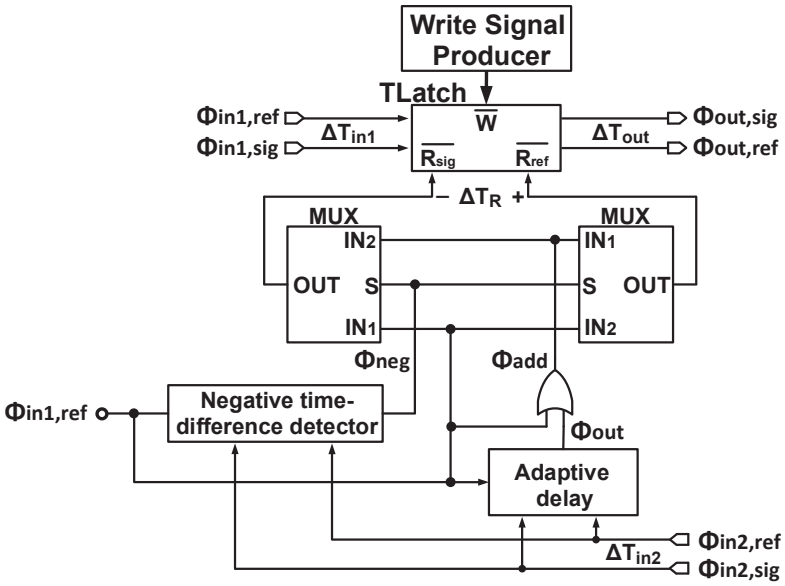
Figure 3.11 Simulation results of the adaptive delay with PVT variations.

3.2.5 TM Subtractor

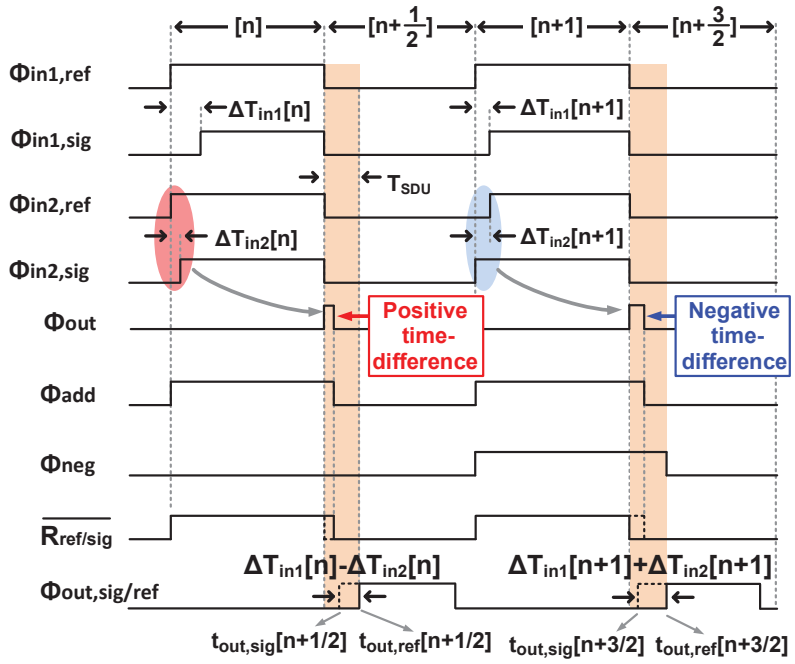
Figure 3.12(a) illustrates the circuit schematic of the TM subtractor, which is a modified form of the TM subtractor first described in (Ziabakhsh *et al.*, 2017). Here the subtractor circuit uses a TLatch in the feedforwad path, and an adaptive delay, a negative time-difference detector block as well as two MUXs in the read path. The TLatch is considered as the computational memory that stores the input time-differences, ΔT_{in1}, and performs basic arithmetic operations (i.e., addition or subtraction) from the second input signal, ΔT_{in2}. In this implementation, the time-difference of ΔT_{in2} is first extracted and aligned with the reference clock, $\Phi_{in1,ref}$. At the same time, the polarity of ΔT_{in2} (i.e., positive or negative) is detected at each sampling instant by the negative time-difference detector and flips the roles of $\overline{R_{ref}}$ and $\overline{R_{sig}}$ by changing the selector inputs of each MUX (S pin). To better understand the TM subtractor, the subtraction of two categories of signals will be illustrated in Figure 3.12(b): one involving a positive TM signal $\Delta T_{in2}[n]$, and another involving a negative TM value. Beginning with the positive TM signal case, during the n-th clock cycle, both TM input samples, $\Delta T_{in1}[n]$ and $\Delta T_{in2}[n]$, are positive and connected to the input and read ports, respectively, of the TLatch. As seen in Figure 3.12(b), the TLatch captures the $\Delta T_{in1}[n]$ at its input ports and waits for the $\Delta T_{in2}[n]$ to be aligned with the falling edge of the reference clock $\Phi_{in1,ref}$ then generates the signal Φ_{out}. The signal Φ_{out} is then added with $\Phi_{in1,ref}$ to produce signal Φ_{add}, which is connected to either $\overline{R_{ref}}$ or $\overline{R_{sig}}$, depending on the positive/negative sign of ΔT_{in2}. The edge alignment and time addition are performed by the adaptive delay line and a digital OR gate, respectively. At the arrival of an input pair of falling edges labeled with $\overline{R_{ref}}$ and $\overline{R_{sig}}$, the subtraction of two TM signals will be read out. As a result, the rising edges at the output of the TLatch occurs at

$$\begin{aligned} \Delta T_{out}[n+\frac{1}{2}] &= t_{out2,ref}[n+\frac{1}{2}] - t_{out2,sig}[n+\frac{1}{2}] \\ &= \Delta T_{in1}[n] - \Delta T_{in2}[n] \end{aligned} \tag{3.14}$$

During the $(n+1)$-th clock cycle, when $\Delta T_{in1}[n] > 0$ and $\Delta T_{in2}[n] < 0$, the negative time-difference detector will change Φ_{neg} to "1", thereby forcing the multiplexers to change the connection of



a) Block diagram.



b) Timing diagram.

Figure 3.12 Modified TM subtractor.

read signals. In this situation, $\Delta T_{in1}[n+1]$ stored in the TLatch will be added to the $\Delta T_{in2}[n+1]$. As shown in Figure 3.12(b), the time difference between the output rising edges for the $(n+1)$-th cycle of the reference clock can be written as

$$\begin{aligned}\Delta T_{out}[n+\frac{3}{2}] &= t_{out2,ref}[n+\frac{3}{2}] - t_{out2,sig}[n+\frac{3}{2}] \\ &= \Delta T_{in1}[n+1] + \Delta T_{in2}[n+1]\end{aligned} \tag{3.15}$$

The circuit schematic of the negative time-difference detector is shown in Figure 3.13. In this circuit, the negative time-difference at the input signals $\Phi_{in2,ref}$ and $\Phi_{in2,sig}$ is detected by an AND and a NOT digital gate to produce the CLK_1 signal. Upon the arrival of the rising edge at Φ_{neg}, $\overline{Q_1}$ is set to "0", which activates the TFF_2 to change its state when the rising edge of CLK_2 arrives. To synchronize the TFF_2 with the input reference clock of the TM subtractor, $\Phi_{in1,ref}$, a SDU with a propagation delay of T_{SDU} is utilized. The additional XOR gate at the output sets the Φ_{neg} to logic "1" whenever the rising edge occurs on either $\overline{Q_1}$ or $\overline{Q_2}$.

Figure **??** shows the Spectre simulation of the output time-difference versus ΔT_{in2} for the TM subtractor with and without digital circuits to control the read ports. As is evident, when the multiplexers and negative time-difference detector shown in Figure 3.12(a) are used in the read path, the TM subtractor circuit is able to distinguish between the positive or negative TM signals carried by ΔT_{in2} and subtract it from ΔT_{in1}. The output response (line with black circles) is compared with the ideal (solid line only) and the subtractor without digital control (dashed line only) responses. As can be seen from the simulation, there is a good agreement between the simulation of circuit shown in Figure 3.12(a) and the ideal subtractor.

3.2.6 Half-Period Delay DTC

A final building block necessary to realize a BP$\Delta\Sigma$ modulator is the digital-to-time converter (DTC). A detailed schematic of the DTC used in this work together with its timing diagram are shown in Figure 3.15. The circuit corresponding to this block will take as input a 1-bit digital signal on the rising edge of $\Phi_{in,ref}$ and produce a corresponding output TM signal ($\overline{R_{ref1}}$ and

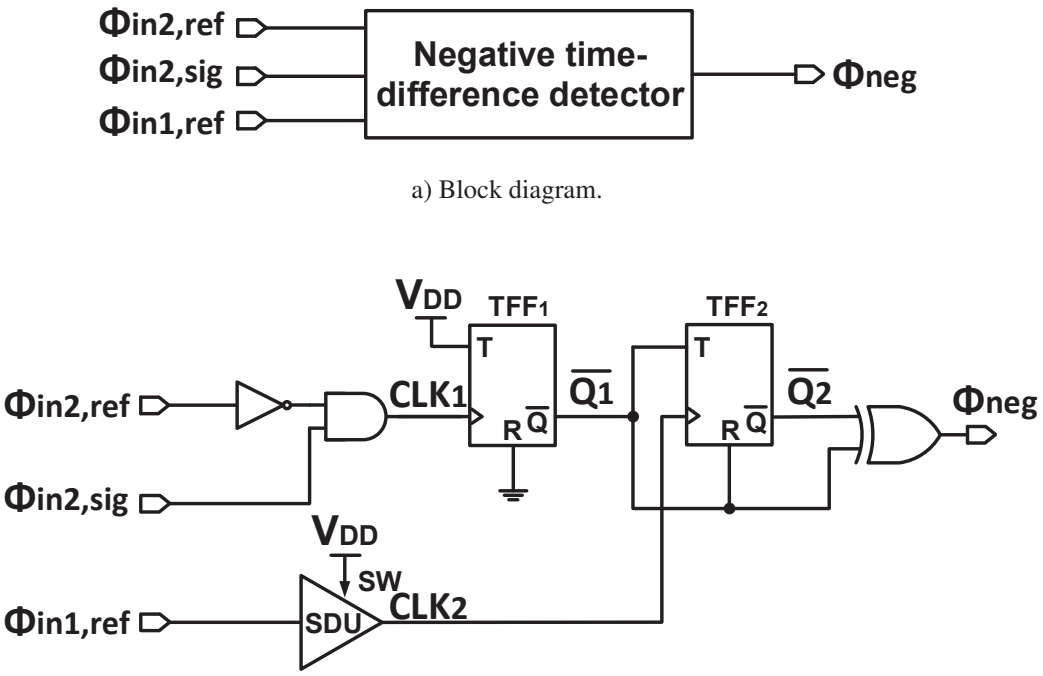
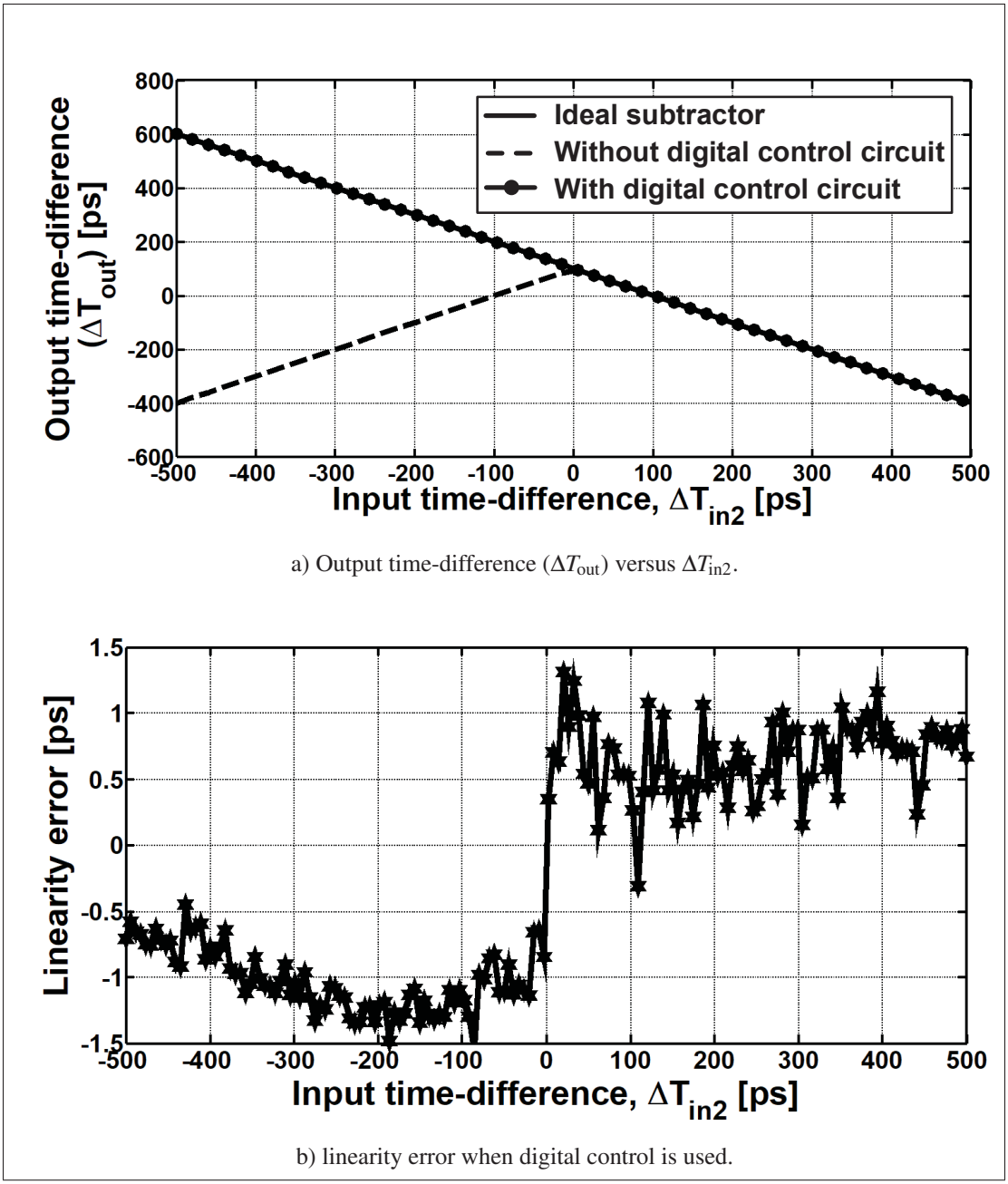


Figure 3.13 Negative time-difference detector.

$\overline{R_{sig1}}$) centered around the falling edge of the $\Phi_{in,ref}$. More specifically, for a digital input of logic "0" the DTC will produce an output TM signal $\overline{R_{sig1}}$ that lags the reference signal $\overline{R_{ref1}}$ by 1 ns. $\overline{R_{ref1}}$ will be activated on the falling edge of $\Phi_{in,ref}$. Conversely, for a input of logic "1" the output $\overline{R_{ref1}}$ will be made to lag behind the $\overline{R_{sig1}}$ by 1 ns, when $\overline{R_{sig1}}$ is activated on the falling edge of $\Phi_{in,ref}$. The magnitude of 1 ns pulse-widths were selected to ensure that the subtractor at the front-end of the modulator does not saturate. Numerous transistor-level simulations were performed using Spectre to identify this value. At the core of the DTC is a new type of delay element block which will be referred to as the double-edge VCDU. This block is an extension of previous proposed VCDUs (Taillefer *et al.*, 2009). Past VCDUs would delay the incoming rising edge of a digital signal by an amount determined by an input voltage level V_{in}. In this work, a signal conditioning block is used at the input control voltage port to increase the VCDU linear operating region. Readers can refer to chapter 5 for more details.



a) Output time-difference (ΔT_{out}) versus ΔT_{in2}.

b) linearity error when digital control is used.

Figure 3.14 Simulation results of the TM subtractor. ΔT_{in1}=100 ps at 42.8 MHz.

In the case of a double-edge VCDU, both the rising and falling edges of the incoming digital signal are delayed in equal portion with respect to the input control voltage V_{in}. In other words, a double-edge VCDU delays both transitions of the input reference signal $\Phi_{in,ref}$ by the exact same amount set by V_{in}. This provides an opportunity to run TM circuits at twice their normal

operating speed, or as demonstrated here, to provide a half-period delay DTC. Another key benefit of using the double-edge VCDU is that the output time-difference of the DTC, denoted by ΔT_{DTC}, can be easily controlled by V_{in} over a linear range, and thus no significant circuit-level design effort is required.

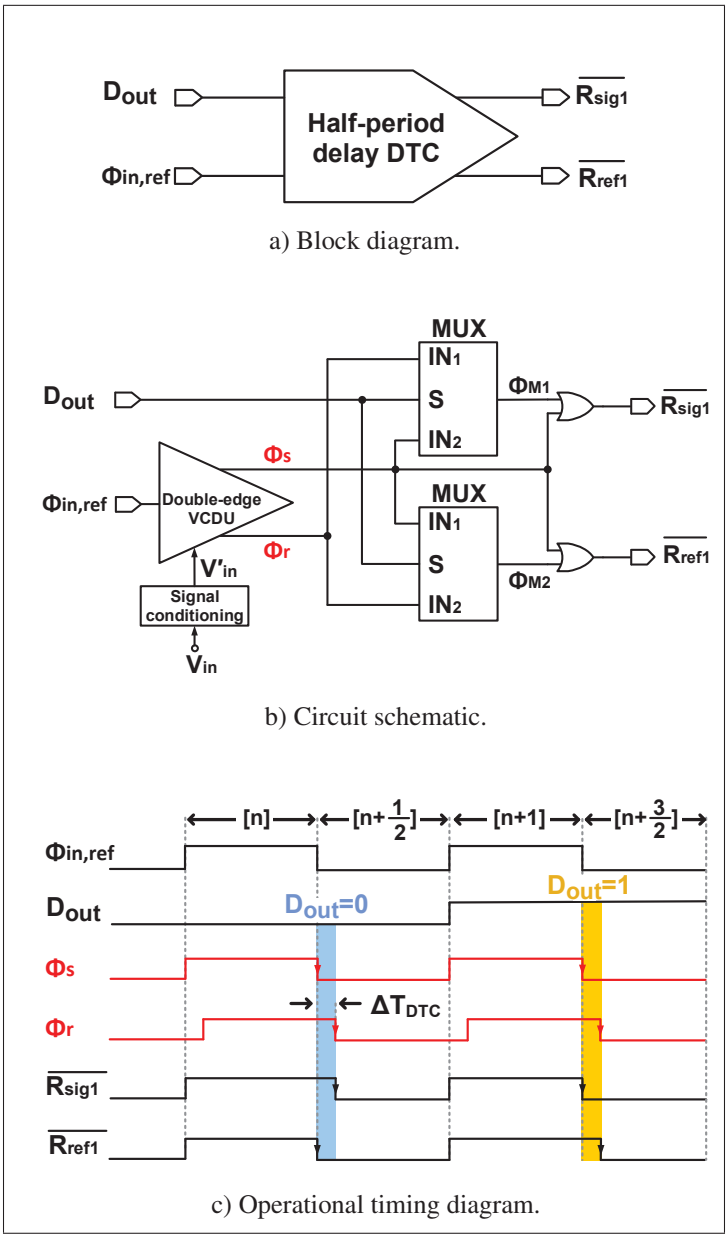
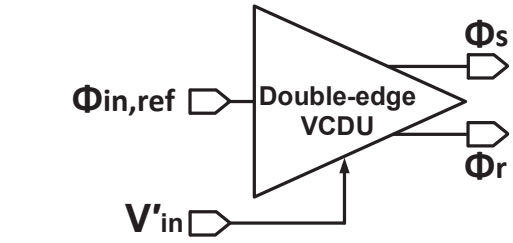
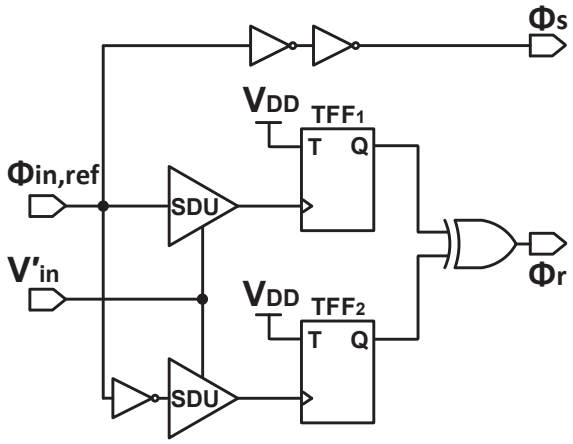


Figure 3.15 Half-period delay DTC.

The detailed implementation of the double-edge VCDU is shown in Figure 3.16. Two SDUs are clocked at the rising and falling edges of the reference signal, $\Phi_{in,ref}$, and produce two signals with propagation delay T_{SDU} relative to the rising and falling edges of $\Phi_{in,ref}$. These two signals are then used to toggle the two TFFs such that the XOR of their Q-outputs produce signal Φ_r with the same period of $\Phi_{in,ref}$. The signal Φ_s is equal to the input reference clock $\Phi_{in,ref}$ with the same propagation delay as those circuits that appear in the signal path defined from $\Phi_{in,ref}$ to Φ_r.



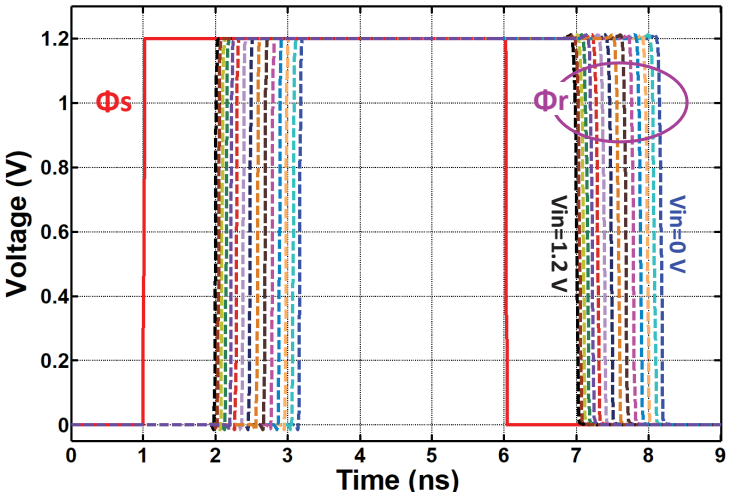
a) Block diagram.



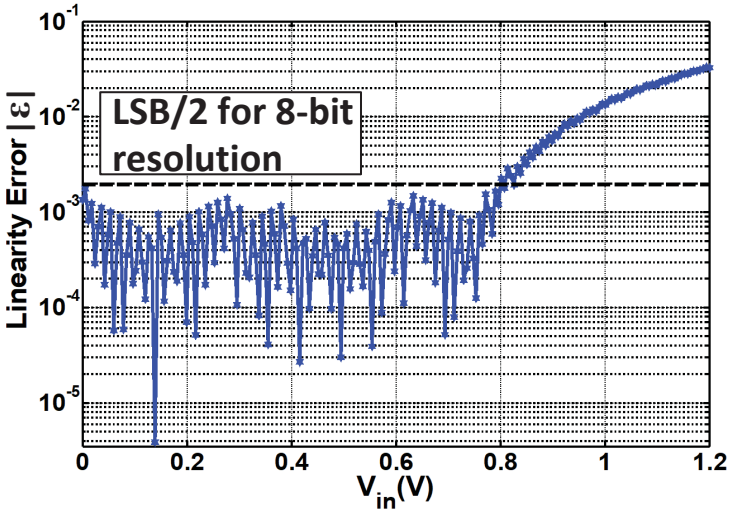
b) Circuit schematic.

Figure 3.16 Double-edge VCDU.

Figure 3.17(a) shows the transient response of the double-edge VCDU with input bias conditions (V_{in}) ranging across the voltage supply from 0 V to 1.2 V. As is evident, for the each input



a) Transient response at different voltage input voltages.



b) Linearity error. The relative linearity error is defined as the largest deviation from the ideal behavior over the full scale linear range of the input voltage. Note that $\Phi_s = \Phi_{in,ref}$.

Figure 3.17 Transistor-level simulation results of the double-edge VCDU.

voltage, V_{in}, the time-difference between the rising edges of the reference clock, $\Phi_{in,ref}$, and the output of the double-edge VCDU, Φ_s, is equal to the time-difference between the falling edges of $\Phi_{in,ref}$ and Φ_s. In order to verify the linearity of the propose double-edge VCDU, we performed a transistor-level Spectre simulation. The results sre shown in Figure 3.17(b),

where the linearity error is defined as the largest deviation from the linear behavior over the ideal response in percent. Simulation results indicate that the linear range for both rising and falling edges is below the 8-bit resolution for a full-scale range from 0 to 0.8 V.

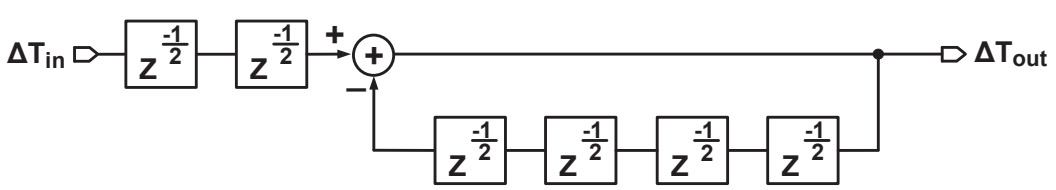
3.3 TM LDI-Based Resonator

To achieve a BPΔΣTDC with a narrow 3-dB bandwidth and deep notch frequency (equivalently, one with a high Q-factor), the second-order TM LDI-based resonator shown in Figure 3.18 will be used. Part (a) of this figure shows the z-domain block diagram of the proposed LDI-based resonator with input-output transfer function

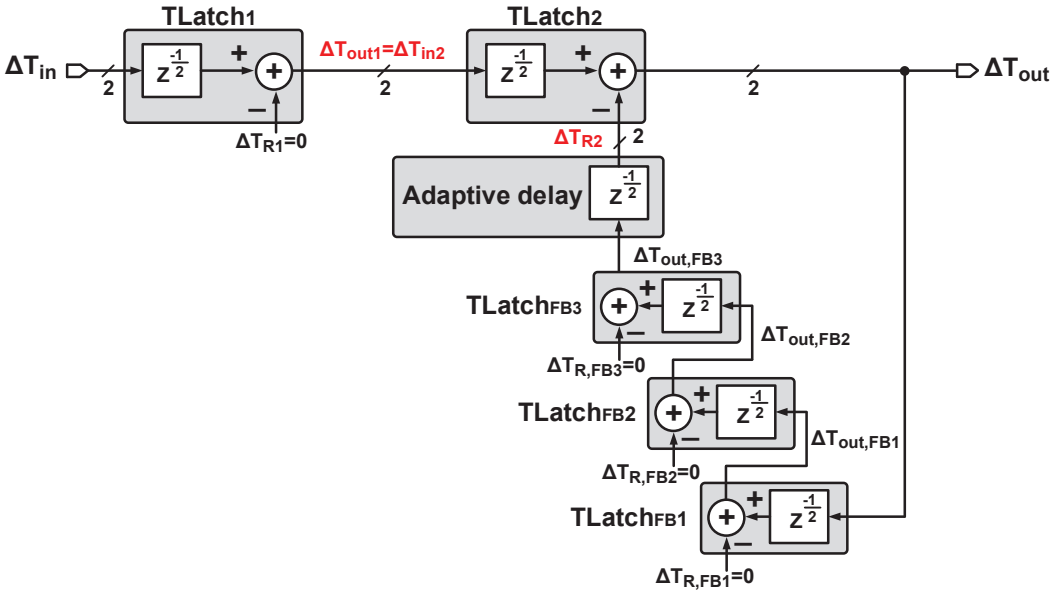
$$T(z) = \frac{z^{-1}}{1+z^{-2}} \tag{3.16}$$

and (b) illustrates the corresponding block diagram using TLatches. This particular arrangement was selected based on the half-period delay that can be realized by the TLatch. As is evident from Figure 3.18(a), six TLatches can be used to implement the resonator structure: two in the feedforward path and four in the feedback path. However, due to manufacturing processing errors, temperature and supply voltage variations, one of the half-period delay elements in the feedback loop will be replaced by the adaptive delay element. One additional advantage of using the adaptive delay element in the feedback path is that it is capable of handling a wide range of sampling clock frequencies. This is because the adaptive delay tracks the phase alignment between its input TM signal and the reference clock so that the total loop delay in the feedback path is nearly equal to two clock-period delays (i.e., z^{-2}). While process errors can also affect the delay in the feedforward path of the LDI resonator involving TLatch_1 and TLatch_2, this error will be accommodated by the DTC in the feedback loop of the BPΔΣTDC - more on this later in section 3.4. It is also important to note that TLatch_2 performs a subtraction role in addition to including a half-period unit delay in the feedforward signal path.

The circuit-level implementation of the proposed second-order TM LDI-based resonator is shown in Figure 3.19. The feed-forward path consists of a half-period delay unit and one input



a) z-domain representation consisting of two half-period delay elements in the feedforward path and four half-period delay elements in the feedback path.



b) Block diagram of the proposed TM LDI-based resonator constructed with multiple TLatches.

Figure 3.18 LDI-based resonator.

port to the TM subtractor to realize the numerator portion of the resonator transfer function (Eqn. (3.16)). The denominator term $(1+z^{-2})$ is achieved by the application of three half-period delay units and another port of the subtractor circuit of Figure 3.12 - which includes another TLatch and the adaptive delay element for another half-period delay.

The timing diagram of the proposed TM LDI-based resonator is illustrated in Figure 3.20. Starting from the first two cycles corresponding to the time index $[n-1]$ and $[n]$, the output is assumed to equal $\Delta T_{in}[n-1]$ and $\Delta T_{in}[n]$, respectively. During the $[n+1]$-th cycle, $\Delta T_{in}[n-1]$ appears at the output of (TLatch$_{FB3}$) in the feedback path. The time-difference between the

two rising edges of the output of TLatch$_{FB3}$ (i.e., $\Phi_{out,ref,FB3}$ and $\Phi_{out,sig,FB3}$) is then extracted by a phase-frequency detector (PFD) and aligned with the reference clock $\Phi_{in,ref}$. However, over one period of the reference clock $\Phi_{in,ref}$, the feedback signal produces a negative time-difference, meaning that the rising edge of $\Phi_{out,ref}$ leads the rising edge of $\Phi_{out,sig}$. This negative TM instance will appear at the output of TLatch$_{FB3}$ during the $[n+4]$-th time instance and sets the Φ_{neg} signal to "1" T_{SDU} seconds after the next rising edge of clock reference. This, in turn, flips the subtractor into its adder mode. As a result, the desired transfer function is achieved at the output of the TM LDI-based resonator (ΔT_{out}).

The circuit prototype of the TM LDI-based resonator was designed in a 130 nm IBM standard CMOS process with a 1.2 V supply voltage. The proposed resonator operates over a wide input range (ΔT_{in}) from 0 to 3.5ns under different sampling frequencies from 4 MHz to 43 MHz. The lower limit of the sampling frequency is set by the capacitor current leakage in the SDU of the TLatches during their holding phase. Conversely, the upper limit is due to the charging time constant established by the SDU capacitors. In this design, a compromise between the current leakage and bandwidth limitation lead to the SDU capacitors being set to 600 fF.

To verify the performance of the resonator, a step response with a constant input time-difference of 1 ns was applied to the input of the resonator (i.e., ΔT_{in}=1ns) and the corresponding output TM signal was captured and analyzed using an FFT. The results are shown in Figure 3.21 for both the transistor-level circuit implementation and the block-level system description shown in Figure 3.18(a).

As is clearly evident, the resonance peak of the TM LDI-based resonator and system-level simulation are very similar; occurring at the desired frequency of $f_s/4$. In addition, one sees that the 3-dB bandwidth of either response is quite small. Detail analysis reveals a Q-factor is seen to be greater than 10.

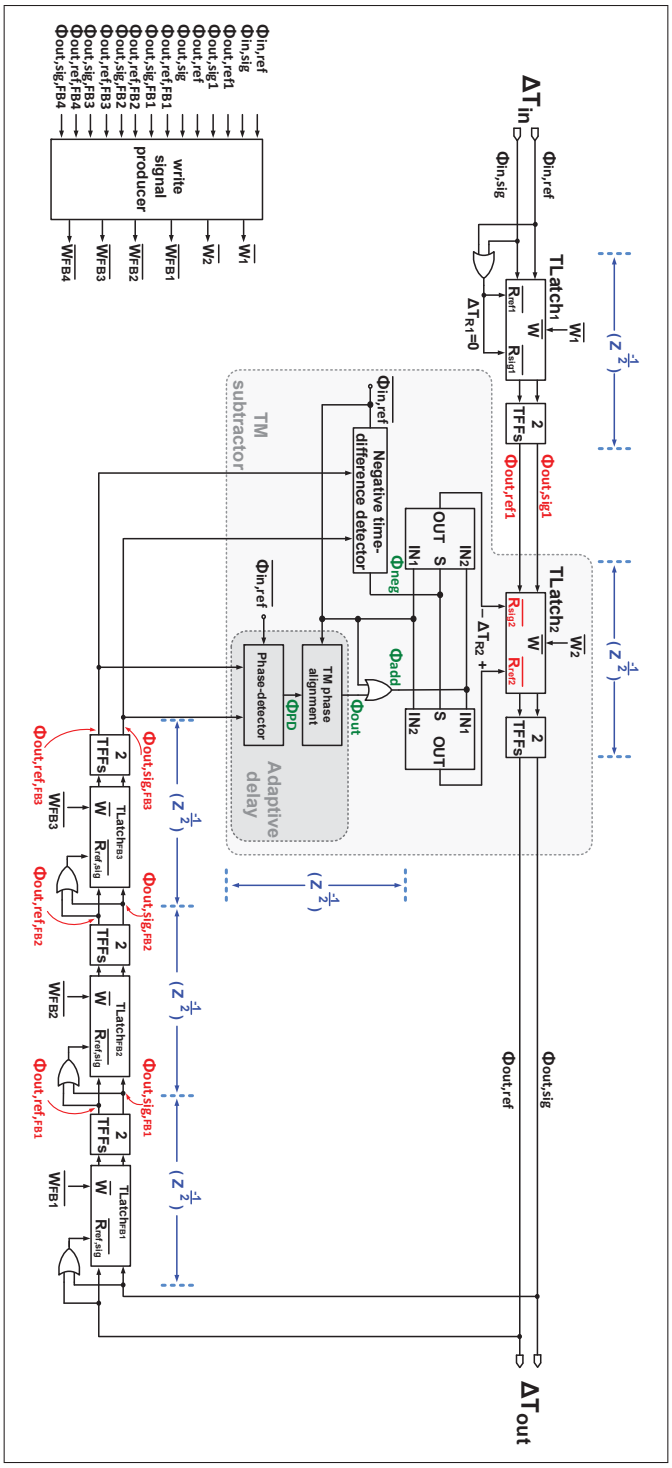


Figure 3.19 Circuit schematic of TM LDI-based resonator with negative TM signal detect circuitry.

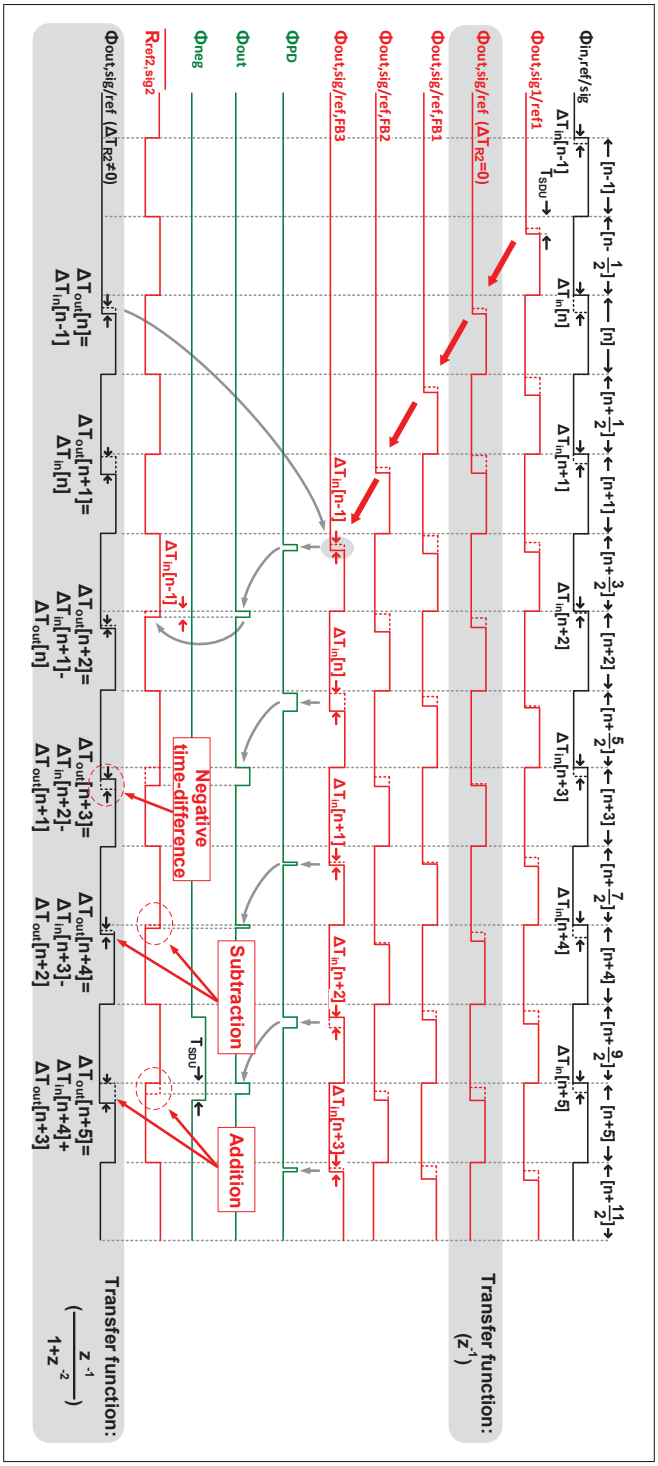


Figure 3.20 Timing diagram of TM LDI-based resonator. $\Phi_{out,sig/ref,FB1-3}$ in the timing diagram represents the signals $\Phi_{out,sig,FB1-3}$ and $\Phi_{out,ref,FB1-3}$, respectively.

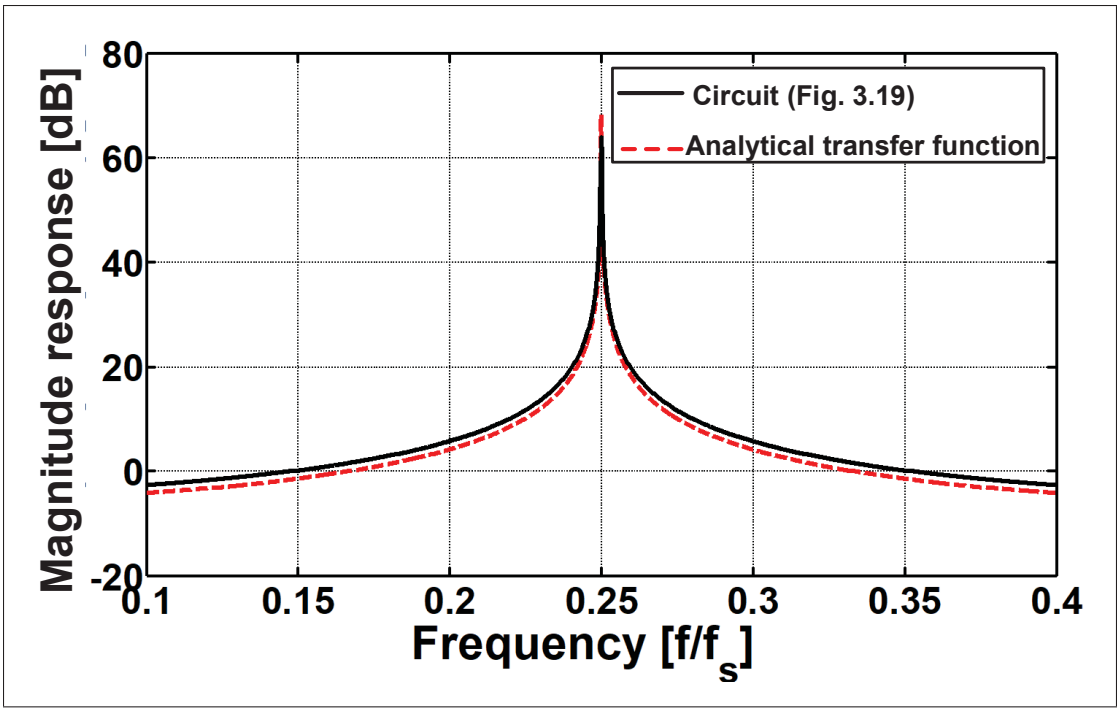


Figure 3.21 Simulation results of the step response of the circuit-level implementation in Figure 3.19.

3.4 Second-Order BPΔΣTDC Circuit Implementation And Simulation Details

Figure 3.22 shows a closed-loop architecture with feed-forward compensation of the proposed BPΔΣTDC. This TDC utilizes a TM LDI-based resonator with transfer function $\frac{z^{-1}}{1+z^{-2}}$ whose poles are located at $\pm f_s/4$. The TM signals at the output of the resonator is subtracted (subtractor #2) from the input TM samples and passed through a 1-bit quantizer to obtain the digital output. The quantized signal is then converted back to the TM signals by a one-bit DTC and fedback to the first subtractor (subtractor #1).

The overall design of the prototype second-order BPΔΣTDC circuit is shown in Figure 3.23. The feed-forward path of the TDC consists of a modified TM LDI-based resonator where a second input port of $TLatch_1$ (read ports) is provided to allow for the subtraction of a feedback TM signal, another TLatch acting as a second subtractor ($TLatch_3$) and a quantizer (DFF) clocked at f_s. The feedback path consists of a half-period delay DTC. In addition, control

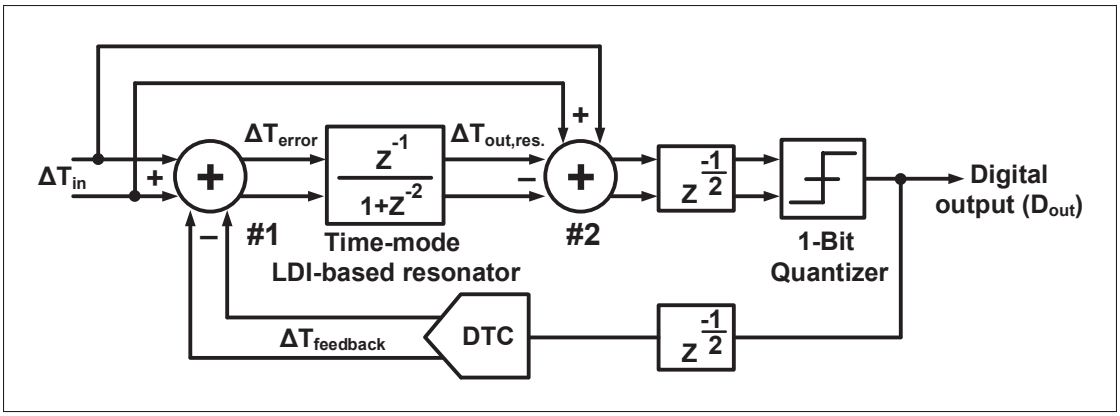


Figure 3.22 Block diagram of the essential components in the proposed BPΔΣTDC.

signals are generated by the Write Signal Producer block shown at the top of the diagram. This block provides the write signals for all TLatches in the appropriate time sequence.

In this work, several architecture and circuit techniques are employed to achieve the desired SNDR with minimum silicon area and power. Firstly, TLatch_1 used as a half-period delay unit inside the LDI resonator is modified to enable the LDI resonator to act on the time-difference between the input signal ΔT_{in} and the feedback TM signal $\Delta T_{feedback}$; thus, no extra TLatch is necessary at the front-end. Secondly, a direct feed-forward compensation path is incorporated to increase the SNDR of the modulator. By using this direct feed-forward path, the TM resonator's output swing can be reduced, as it only needs to process the quantization noise error and is free from the input TM signals (Haurie *et al.*, 1995; Lee *et al.*, 2015). To implement this technique in the time-domain, TLatch_3 is included at the output of the resonator to subtract the input TM signal, ΔT_{in}, from the output of the resonator, $\Delta T_{out,res}$. This TLatch uses the same circuit topology as that shown in Figure 3.3(a). Intentionally, ΔT_{in} and $\Delta T_{out,res}$ are connected to the read and input ports of TLatch_3, respectively. Thirdly, to maintain negative feedback around the loop involving the LDI resonator and the 1-bit quantizer (DFF), signals $\Phi_{out,sig,FF}$ and $\Phi_{out,ref,FF}$ are connected to the *CLK* and *D* inputs of the DFF, respectively. Fourthly, a DTC with a half-period delay is employed in the feedback path. This block converts the output 1-bit digital signal from the quantizer to a corresponding time-difference signal to be fedback

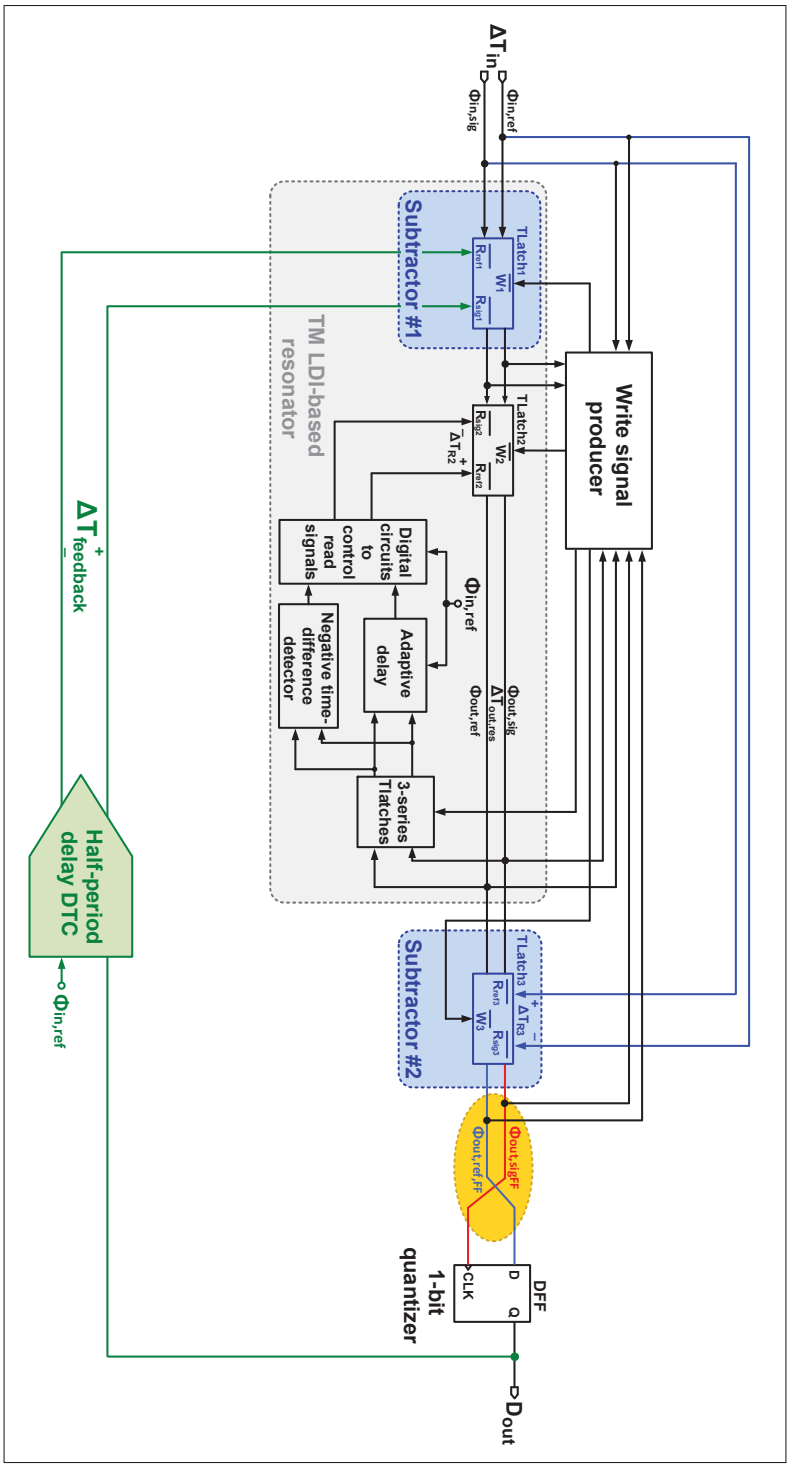


Figure 3.23 Top-level schematic of the proposed BP ΔΣ TDC. TFFs in the output of TLatch_1 and TLatch_2 are not shown for simplicity.

to input subtractor. The half period-delay is necessary to ensure that a full two-period delay is achieved around the loop as depicted in Figure 3.22.

Figure 3.24 shows the simulated PSD of the BPΔΣTDC and the ideal BPΔΣ modulator. The output spectrum in Figure 3.24 shows the desired second-order noise shaping at 10.73 MHz IF. The input TM signal is a 1 ns_{pp}, 10.73 MHZ sinusoidal tone, and the simulated SNDR, SNR, and SFDR are 45.4 dB, 45.8 dB, and 49.6 dBc, respectively, while operating with 1.2 V voltage supply.

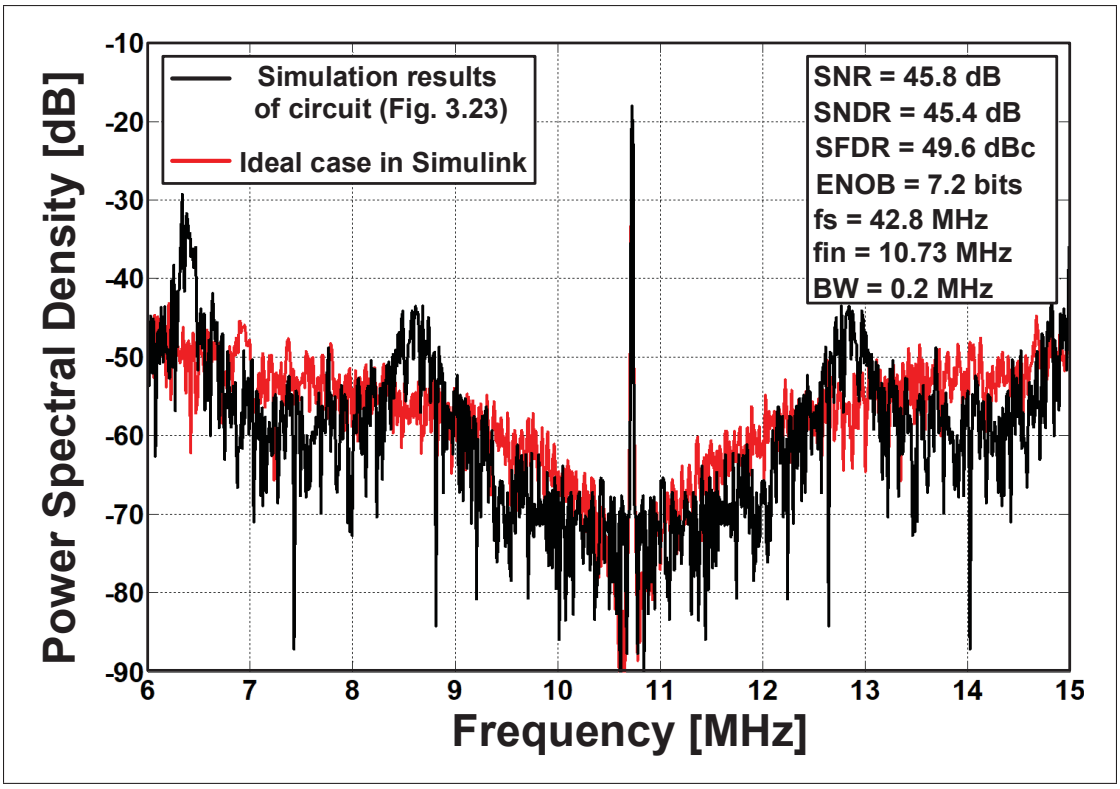
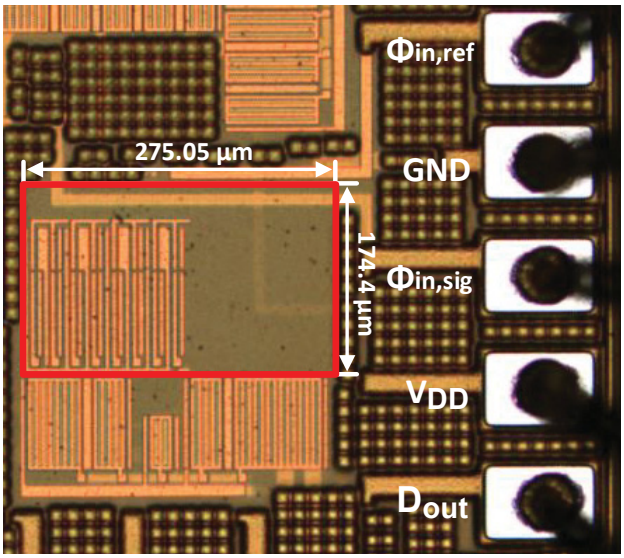


Figure 3.24 Simulated PSD of the transistor-level circuit of BPΔΣTDC and Simulink system-level BPΔΣ modulator.

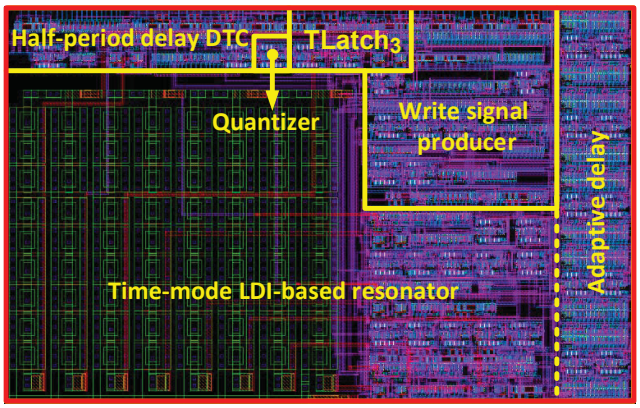
3.5 Experimental Setup

The proposed BPΔΣTDC shown in Figure 3.23 was fabricated in 130 nm IBM CMOS technology. Figure 3.25 shows the chip micrograph and layout of the proposed TDC, which occupies the core size of 0.048 mm^2 (275.1 μm × 174.4 μm). The prototype chip is assembled in a 44-pin CQFP and mounted on a custom ten-layer PCB as shown in Figure 3.26. Apart from the TDC chip marked with a white box, the test board included some features such as SMA connections to the input/output signals, non-inverting clock drivers (IDT ICS621) and a voltage regulator (Analog Devices ADP1706ARDZ-1.2). Bias voltages were derived from this reference voltage using resistor divider circuits, together with some 100 nF capacitors to suppressed any AC power-supply-related ripples. To reduce digital noise coupling into the power supplies network, the digital voltage supply lines were intentionally placed some distance away from the analog power lines. In addition, all power nets were decoupled with additional 100 nF capacitors. The other components seen on the PCB seen in Figure 3.26 are not related to this TDC test and are used for other purposes.

A block diagram of the measurement setup used to characterize the prototype BPΔΣTDC is depicted in Figure 3.27. The input TM signals ($\Phi_{in,ref}$ and $\Phi_{in,sig}$) were synthesized using an arbitrary waveform generator model Tektronix AWG5014B. The data loaded into the AWG5014B was created using Spectre by simulating an ideal VCDU with a conversion gain of 1 ns/V. The digital input to the VCDU was driven by a 1.2 V amplitude square wave operating at a frequency of 42.8 MHz. The voltage controlled input port was driven by a 1 V amplitude 10.73 MHz sine wave. The output phase-modulated voltage signal from the VCDU was then sampled at a rate of 42.8 Ms/s, then loaded into the AWG5014B to drive the PCB test setup. The digital output bit-stream, D_{out}, was captured by a logic analyzer (Tektronix TLA7012) and processed in MATLAB to extract the relevant parameters. In addition, digital oscilloscope (Agilent DSA80000B) was used to monitor the input signals of the TDC to ensure a stable constant sources (i.e., digital signals with variable time-differences and duty cycle of 50%). Through measurement, the DSA80000B was found to have a timing resolution as low as 150 ps with a rms jitter below 1 ps. A MATLAB/simulink simulation was performed at the sys-



a) Die photograph.



b) TDC core layout.

Figure 3.25 Experimental Prototype.

tem level where the instrument was modeled with a timing resolution ranging between 300 ps and 1 ns. The block diagram corresponding to this setup is shown in Figure 3.28(a). The corresponding PSD of the resulting measurement (simulated) is shown in Figure 3.28(b). As is evident from the plot, the timing resolution of the Agilent Infiniium DSA80000B digital sampling scope with its 150 ps timing resolution is sufficient to perform the required measurement.

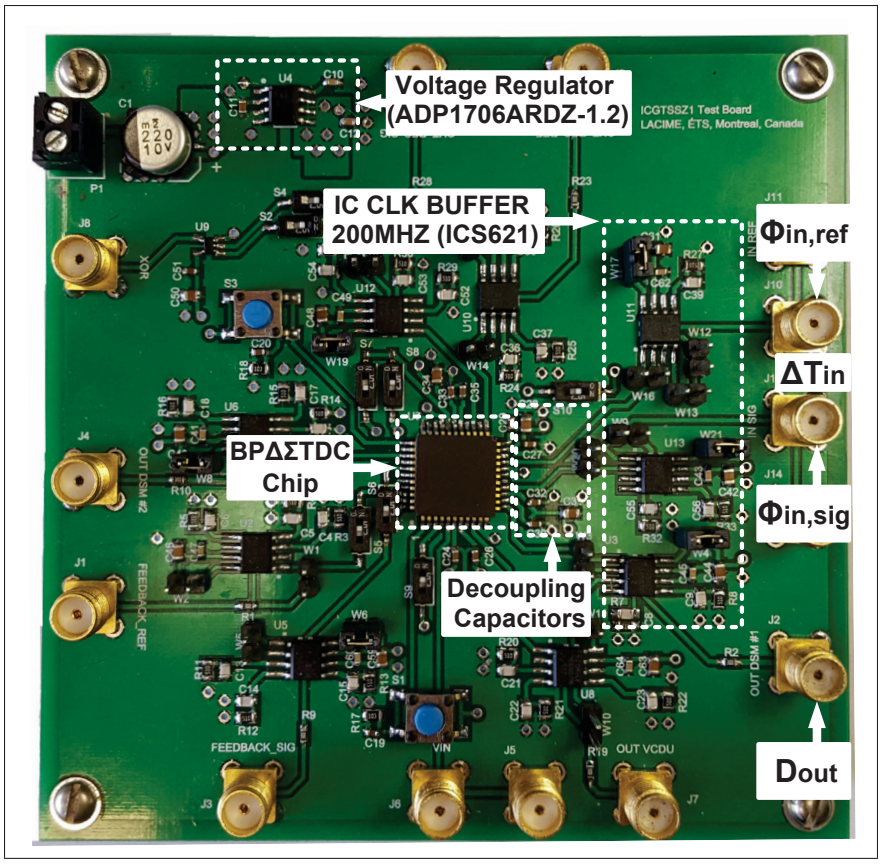


Figure 3.26 Photograph of the customized board to test the TDC circuit.

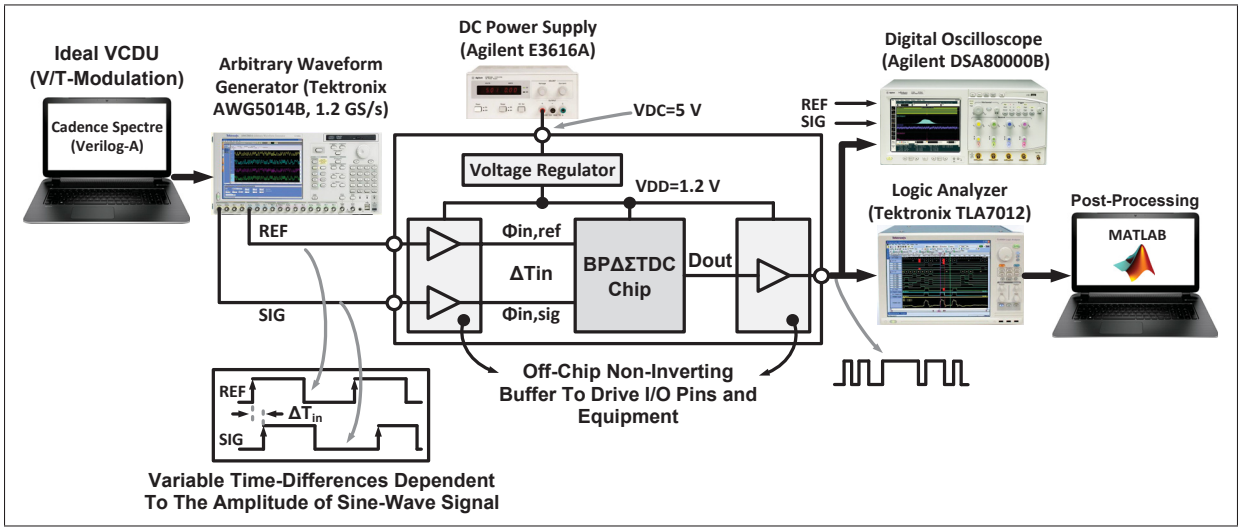


Figure 3.27 Block diagram of the measurement setup.

An instrument with a timing resolution as high as 400 ps should be capable of making this measurement. Figure 3.29 shows the jitter measurement of the time difference (ΔT_{in}) between the input reference and signal clocks, $\Phi_{in,ref}$ and $\Phi_{in,sig}$. The arbitrary waveform generator has been setup to generate ΔT_{in}=500 ps and then it was connected to the digital oscilloscope. The measurement results in a jitter with a mean of a 495.35 ps and a standard deviation of 7.52 ps.

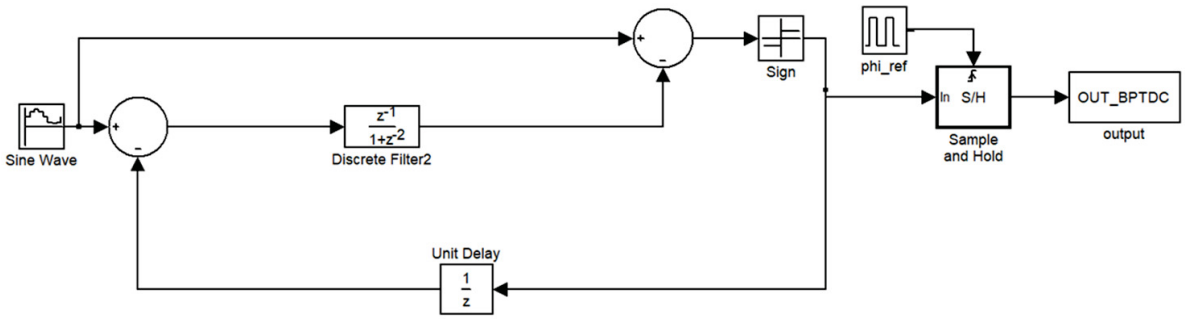
The step response measurement of the TM LDI-based resonator for ΔT_{in}=1 ns at f_s=42.8 MHz is illustrated in Figure 3.30. The measured results agree with theory.

3.5.1 Measurement Results

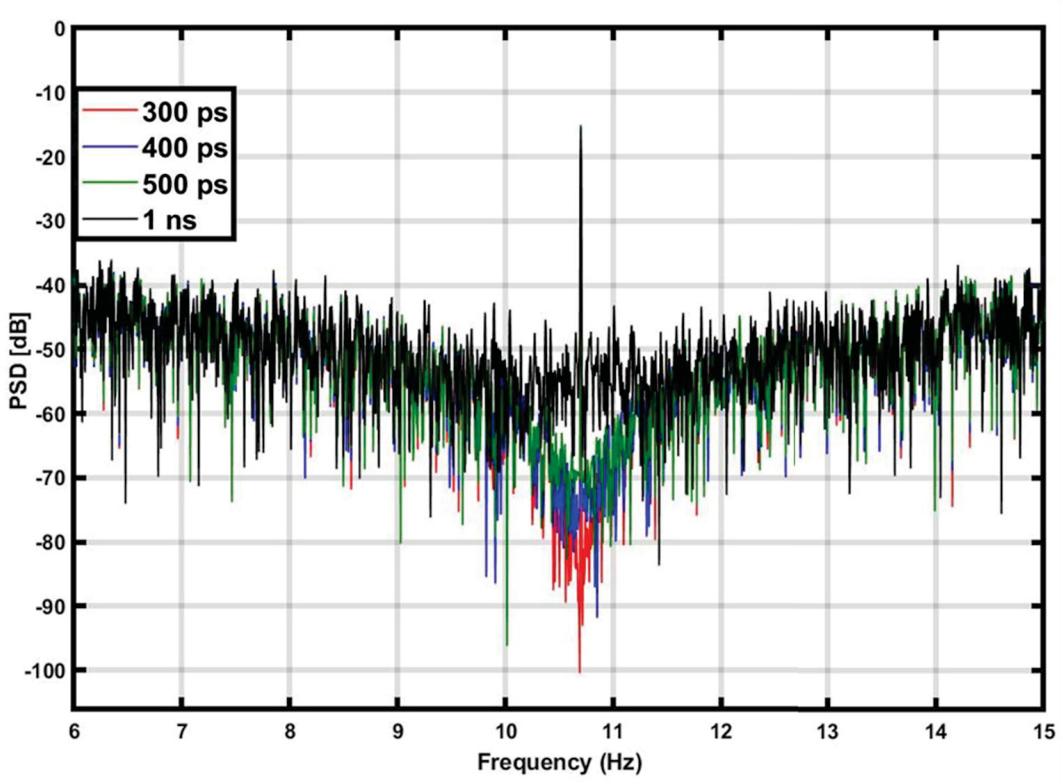
Figure 3.31 shows the testing environment consisting of an arbitrary waveform generator, digital oscilloscope, spectrum analyzer, and power supply.

Figure 3.32 shows a small portion of the input TM signals as seen on the scope, operating at 42.8 MHz frequency, as well as the output bit-stream of TDC. In the plot, the yellow and green traces are $\Phi_{in,ref}$ and $\Phi_{in,sig}$, respectively, and the output bit-stream signal D_{out} is displayed with a violet trace. As is evident, the input and output digital signals are operating at the expected data rate of 42.8 MHz with good rise and fall times.

Figure 3.33 shows the measured PSD processed obtained using a Hanning window and FFT. The output spectrum shows a 20 dB/dec bandpass noise shaping characteristic corresponding to the behavior of a second-order BPΔΣTDC. The TDC achieved an SNR of 39.9 dB and an SNDR of 39.5 dB over a 0.2 MHz signal BW, resulting in an effective number of bits (ENOB) of 6.3 bits. This ENOB value is in good agreement with 7-bit circuit-level simulation prediction that corresponds to a 42 dB peak-SNDR. Figure 3.34 shows the measured SNDR of the BPΔΣTDC versus the input signal level. Note that, the maximum input amplitude of the TDC is limited only by the SDU's capacitors when the input time-differences are close to full scale. The SDUs can be easily optimized to avoid any saturation of the TLatches.



a) Block diagram of the Simulink set up for evaluating the effects of the digital sampling scope timing resolution on the ΔΣTDC operation.



b) PSD results from simulation as a function of timing resolutions of 300 ps, 400 ps, 500 ps and 1 ns.

Figure 3.28 System-level model of Instrument.

Table 3.1 shows a comparison between the measured performance of the prototype BPΔΣTDC and system-level design in MATLAB/Simulink. As is evident, the bandwidth of the measured

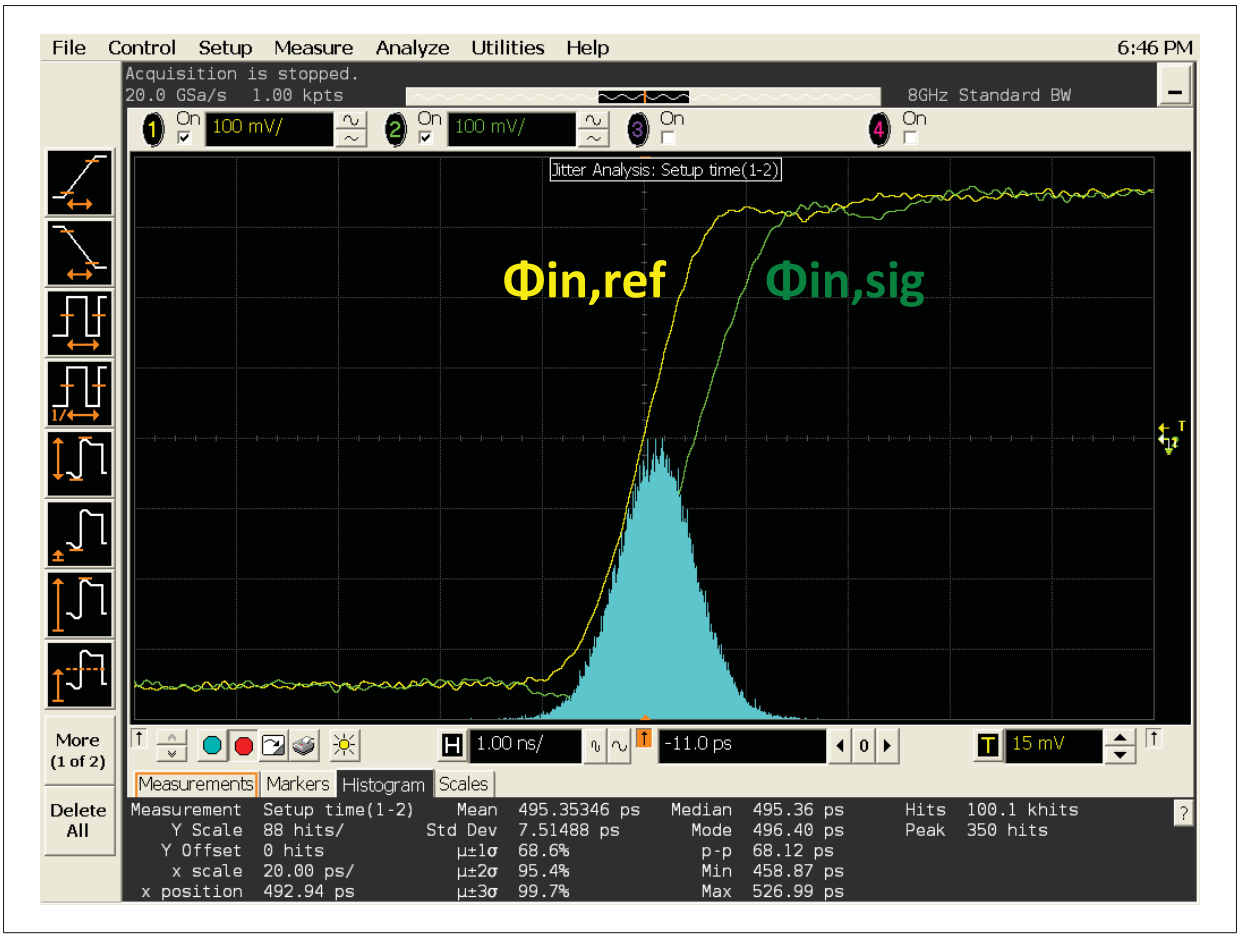


Figure 3.29 Measurement the time difference jitter (ΔT_{in}=500 ps).

prototype is the same as that predicted by simulation (in other words, the pole-zero positioning is correct). The measured signal-to-noise ratio performance metrics differ from the Simulink simulations results by about 10 dB. This we attribute to the additional noise sources related to the IC and PCB implementation which are not modeled in Simulink. The performance of the proposed BPΔΣTDC is summarized and compared with other recent state-of-the-art Nyquist-rate and ΔΣTDCs, as shown in Table 3.2. The proposed architecture performs band-pass noise shaping while achieving a reasonable resolution. The area of the BPΔΣTDC is efficient even for the 130-nm technology.

The TDC consumes a total power of 4.9 mW from the 1.2 V supply voltage at maximum sampling frequency of 42.8 MHz. Figure 3.35 shows the breakdown in power consumption. The

Table 3.1 Performance summary of the proposed BPΔΣTDC.

Specification	**Measurement**	**Simulation**	**MATLAB/Simulink**
Technology	130-nm IBM CMOS	130-nm IBM CMOS	-
Order	Second	Second	Second
Sampling frequency (f_s)	42.8 MHz	42.8 MHz	42.8 MHz
IF signal frequency (f_{in})	10.73 MHz	10.73 MHz	10.73 MHz
Signal bandwidth (f_{BW})	0.2 MHz	0.2 MHz	0.2 MHz
Input range (T_{range})	0-3.5 ns	0-3.5 ns	-
Peak SNDR	39.5 dB	45.4 dB	48.9 dB
Peak SNR	39.9 dB	45.8 dB	48.9 dB
SFDR	45.4 dBc	49.6 dB	61.5 dBc
ENOB	6.3 bits	7.2 bits	7.8 bits
Supply voltage (V_{DD})	1.2 V	1.2 V	1.2 V
Power consumption	4.9 mW	4.9 mW	-
BPΔΣTDC area	0.048 mm^2	-	-
Total chip area	1.0 mm $\times$ 1.0 mm	-	-

Table 3.2 Comparison of state-of-the-art TDCs with similar specifications.

	Kim, TCAS I'14	Yu, JSSC'15	Kim, JSSC'14	Yu, TCAS I'14	Cao, JSSC'12	**This work**
Technology (nm)	130	65	65	65	130	130
Supply voltage (V)	1.2	1	1	1	1.2	1.2
Technique	3D Vernier	1-3 MASH GRO	Pipeline TDC	1-1 MSH GSRO	1-1-1 MASH	TLatch-based
Sampling frequency (MHz)	25	150	250	200	10	42.8
Noise shaping	No	LP	No	LP	LP	BP
Input Range (T_{range}) (ns)	14	5.4	0.58	4	100	3.5
Resolution (ps)	6.98	2.64	1.12	1.58	6	1.87
Calibration required	No	No	No	No	Yes	No
Power (mW)	0.33	3.52	15.4	4.26	0.7	4.9
Core area (mm^2)	0.28	0.03	0.14	0.43	0.08	0.048

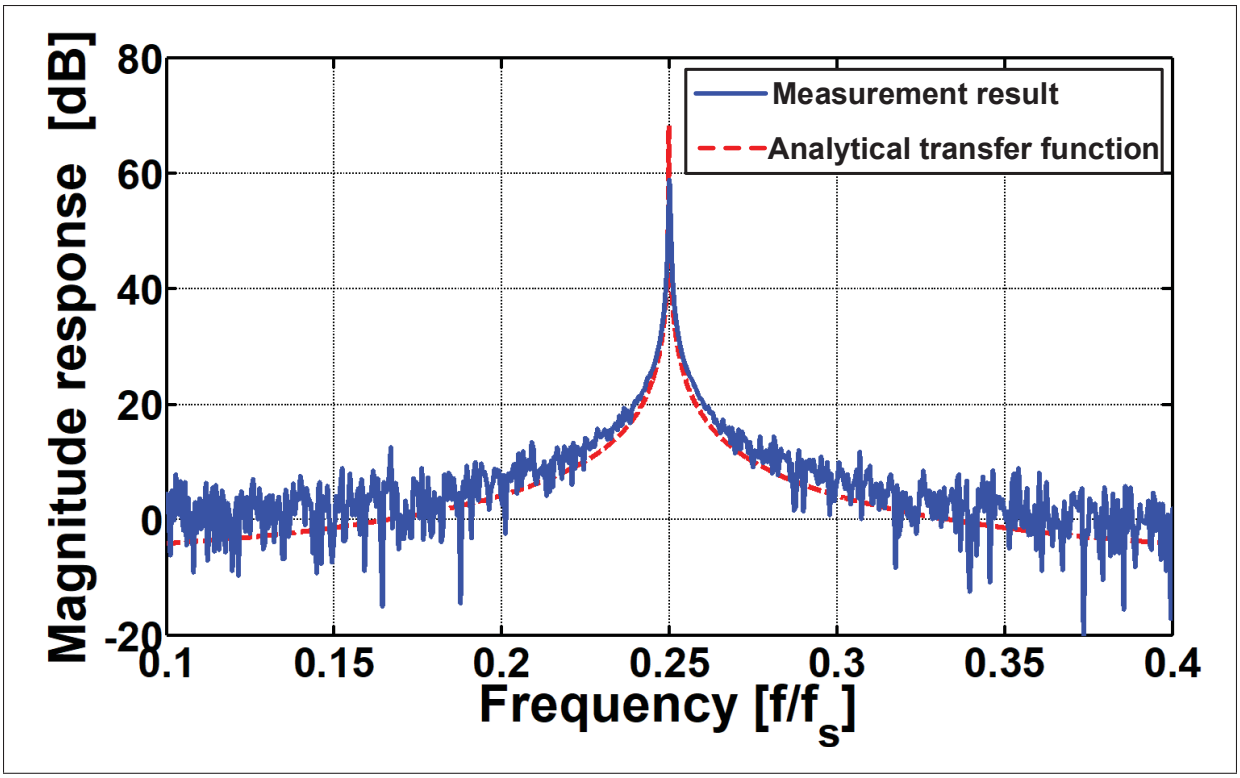


Figure 3.30 Measurement results of the step response of the TM LDI-based resonator.

first two series TLatches ($\text{TLatch}_{1,2}$) consumes 6% of total power which includes the core of the TLatch and digital circuits to produce their write signals. $\text{TLacth},_{FB1,2,3}$ and TLatch_3 as well as their Write Signal Producers consume 11% and 3%, respectively. The negative time-difference detector consumes 8%, and digital circuits shown in Figure 3.19 (two multiplexers and a digital OR gate) and phase detector consume power less than 1%. Due to complexity of TM phase alignment in time shifting of Φ_{PD} signal, this circuit consumes 69% of the total power. While the power consumption on the VCDU-based DTC and quantizer are only 2% and $<$1%, respectively. A power breakdown analysis was performed on the adaptive delay element as shown in Figure 3.36. However, this analysis revealed that the highest power consumption element is the extra pulse remover circuit at 74 %, the next highest element being the inverter-based delay line, which consumes 13 % of the power budget. With further care, the power consumption can be reduced by improving the power consumption of the individual digital gates by optimizing the transistor sizes and replacing the static TFFs with dynamic flip-

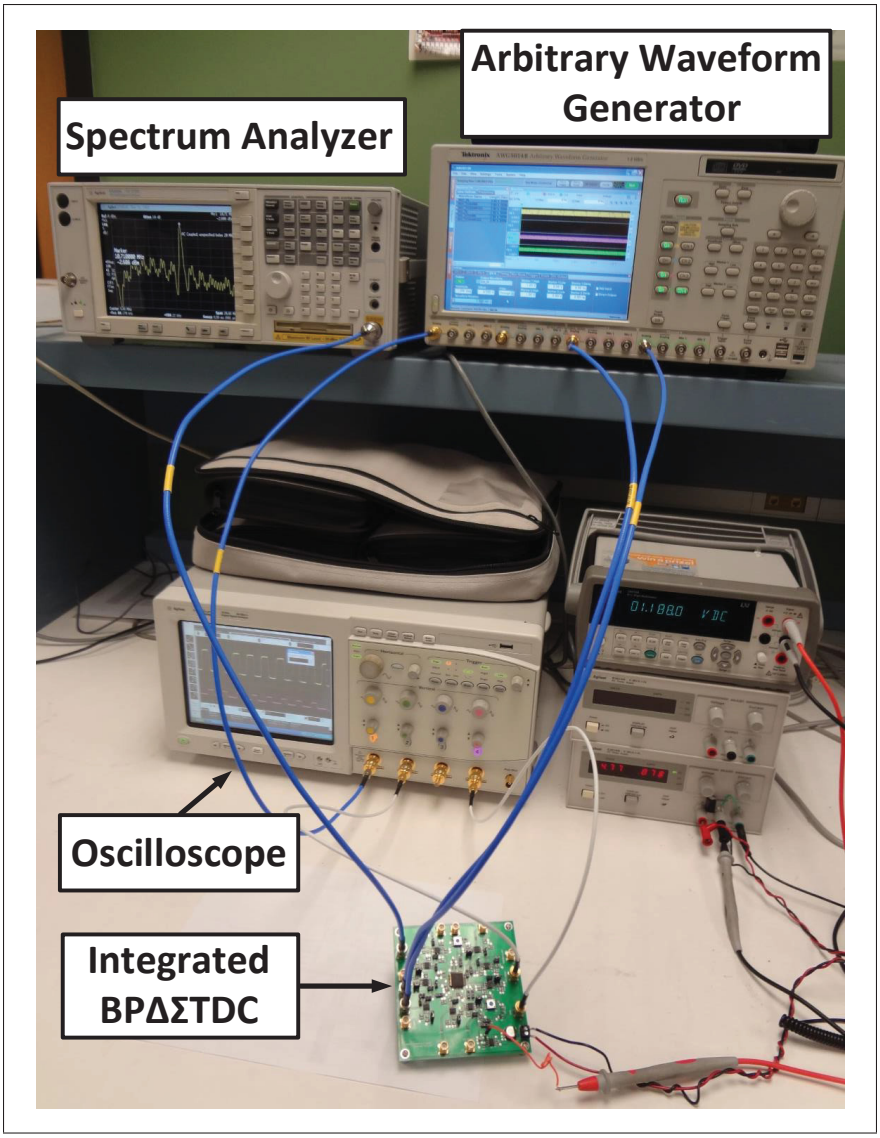


Figure 3.31 Experimental test bench setup.

flops. It should be noted that the power consumption of the BPΔΣTDC can be reduced further using innovative circuit design solutions now that the circuits proposed in this work have been validated. This is the subject of future work.

In order to verify the capability of the BPΔΣTDC over a wide range of reference clock frequencies, the above setup was utilized. The measured SNDR value versus the sampling frequency with a 0.2 MHz bandwidth and $f_{in} = f_s/4$ is shown in Figure 3.37. When the sampling frequency is greater than 36 MHz, the SNDR is still greater than 37 dB, thanks to TM phase

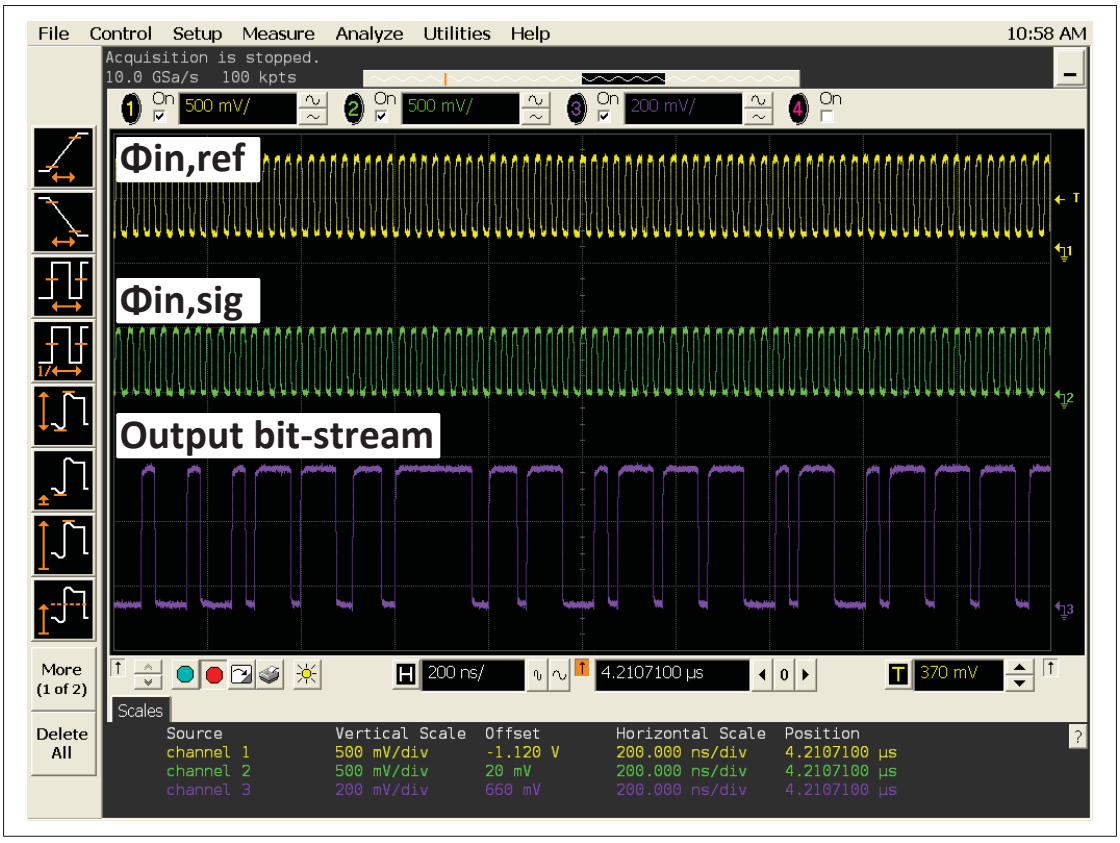


Figure 3.32 Experimental time-domain waveforms of the input signals ($\Phi_{in,ref}$ and $\Phi_{in,sig}$) at sampling frequency 42.8 MHz and output bit-stream (D_{out}).

alignment and synchronization technique. Further decreasing the sampling frequency degrades the SNDR due to reduced the OSR.

3.6 Summary

In this chapter, we presented new TM building blocks using digital circuits. The proposed TM blocks include the half-period delay unit, cascading of two half-period delay units, adaptive time offset correction, TM subtractor and the half-period delay DTC. In the next step of this work, we have successfully implemented the very first prototype of a BPΔΣTDC with second-order noise shaping. It achieves a peak SNDR of 45.4 dB over a 0.2 MHz bandwidth centered around 10.73 MHz. The key building blocks of the proposed TDC include a TM LDI-based resonator, an all-digital DTC, a TM subtractor circuit capable of subtracting negative time-

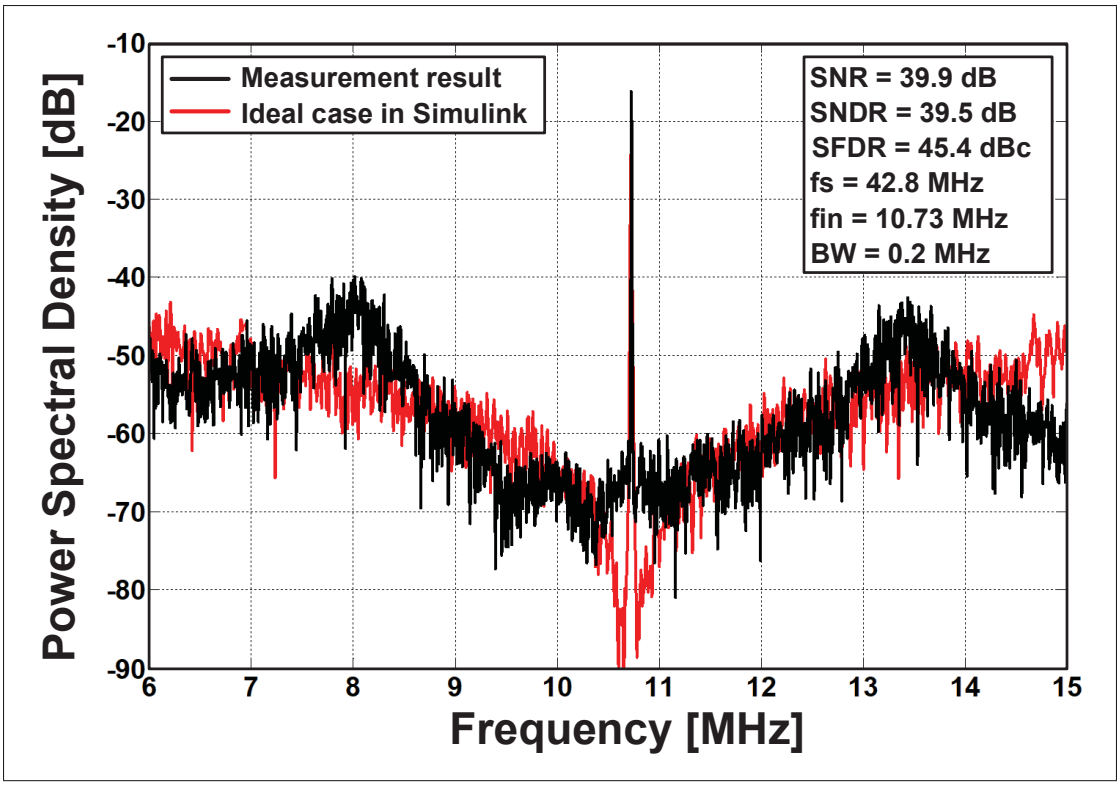


Figure 3.33 Measured output spectrum of the BPΔΣTDC with a 10.73 MHz input signal and 42.8 MHz sampling frequency. Each of the output spectrum are averaged to reduce the variance of the PSD.

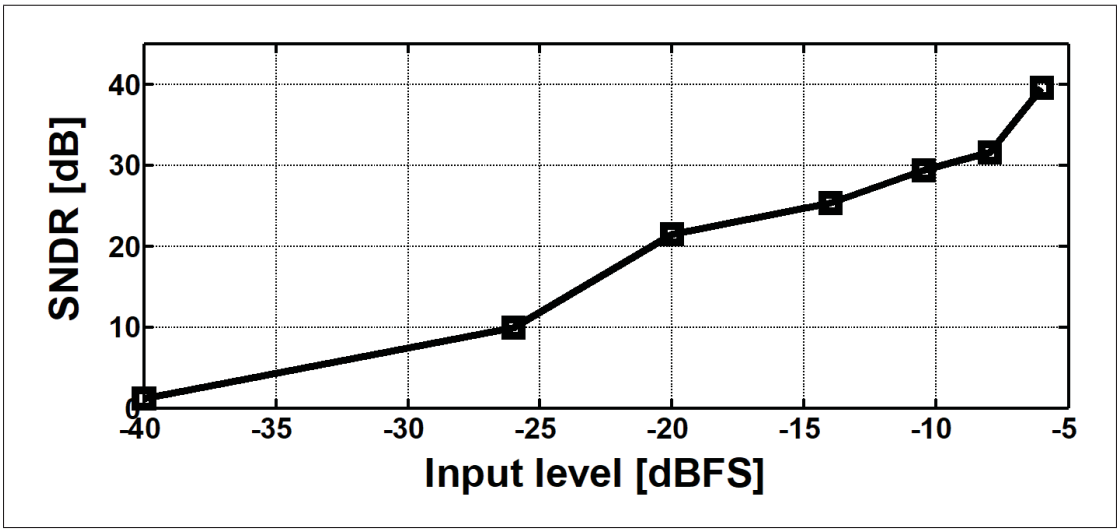


Figure 3.34 Measured SNDR versus input signal level.

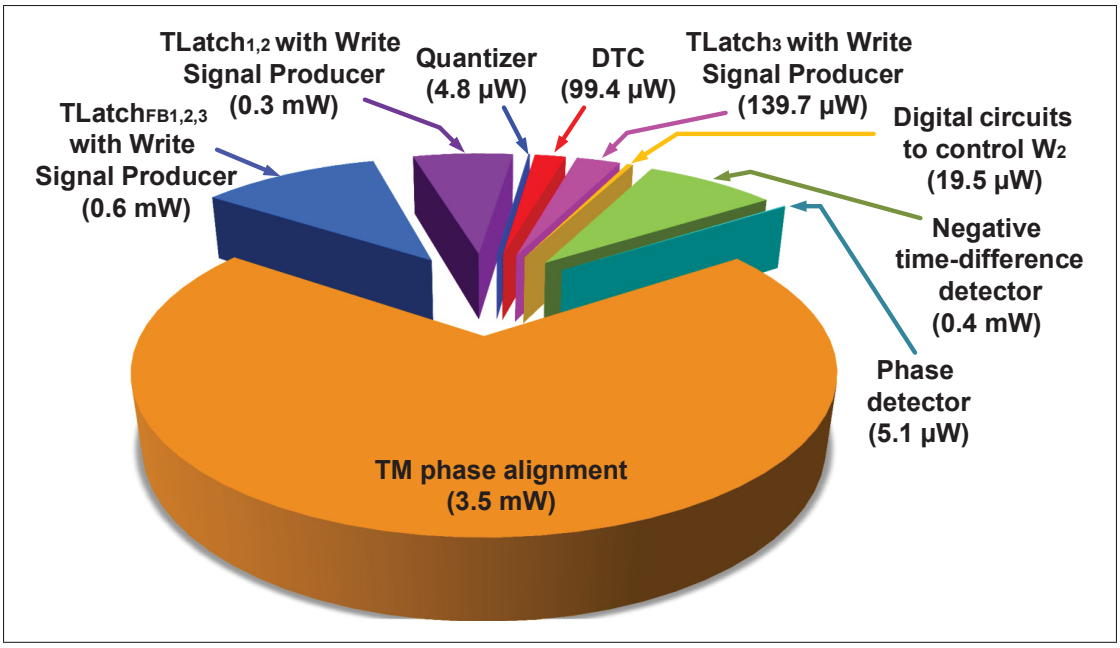


Figure 3.35 Power breakdown of the prototype TDC.

difference values and an adaptive delay circuit that can compensate for process variations. The adaptive delay circuit enabled the sampling frequency to be adjusted from 4 MHz to 42.8 MHz with a notch frequency equal to one-quater of the sampling clock. The performance of the BPΔΣTDC was best at the highest sampling rate of 42.8 MHz. To conclude, this chapter has demonstrate a BPΔΣTDC which is compact, efficient, and accurate that can be easily adopted into a new CMOS technologies under low supply voltage conditions. The prototype BPΔΣTDC achieves a 39.5 dB peak SNDR over a 0.2 MHz signal bandwidth at 42.8 MS/s while consuming less than 5 mW in a 1.2 V IBM 130 nm CMOS process. The proposed TDC is highly digital and occupies a core area of only 0.048 mm^2.

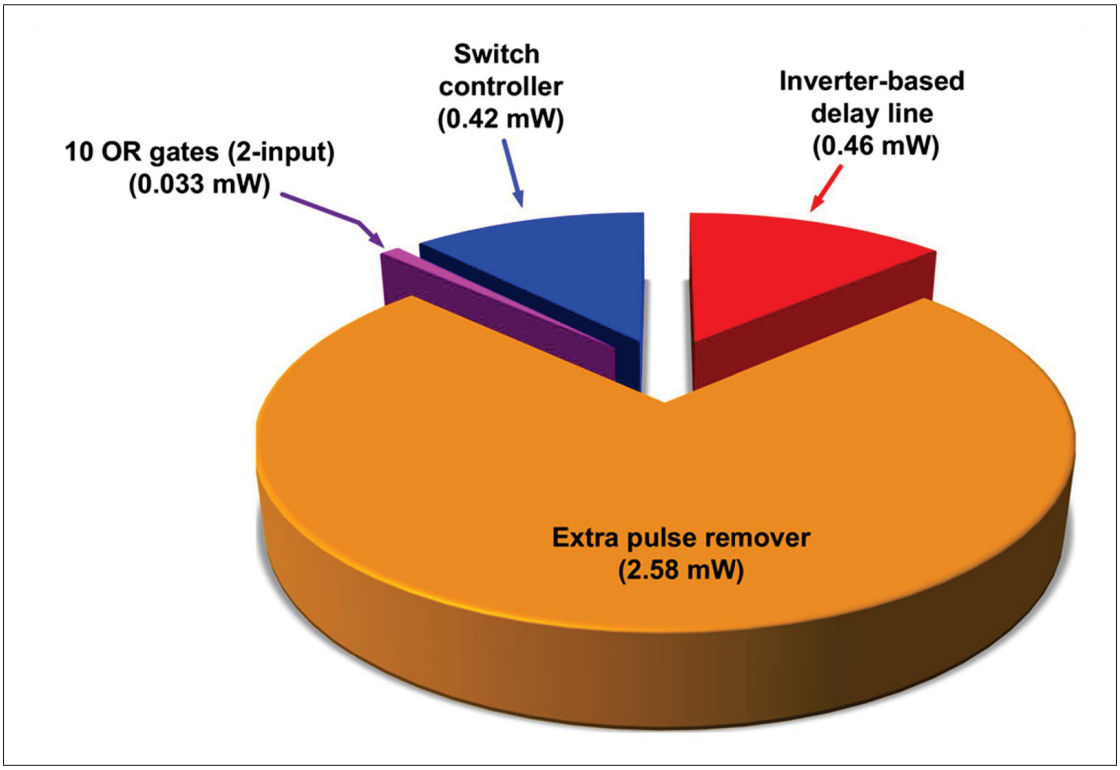


Figure 3.36 Power breakdown of the Adaptive Delay element.

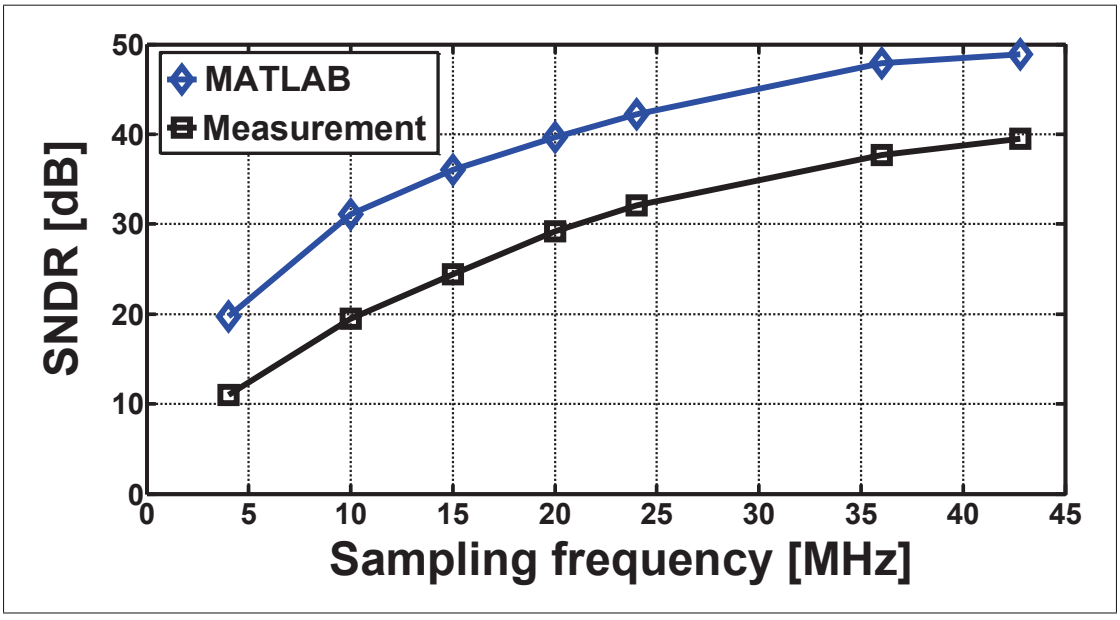


Figure 3.37 MATLAB and Measured SNDR for different sampling frequency ($f_{in} = f_s/4$) with BW=0.2 MHz.

CHAPTER 4

NEW IMPROVEMENT TECHNIQUES FOR VCDU AND TDA

4.1 Introduction

This chapter presents two novel approaches in time-domain to improve the performance parameters of voltage-controlled delay unit (VCDU) and time-difference amplifier (TDA). In the first section, a new design of VCDU with signal conditioning circuit will be presented which improves the linearity range compared to the state-of-the-art design. The behavior of the VCDU is then validated in an example application of $\Delta\Sigma$ modulation. The VCDU is designed and simulated in a 1.8 V TSMC 180 nm CMOS process. Circuit-level simulation results of the $\Delta\Sigma$ modulator show a peak SNDR of 58 dB when clocked at 140 MHz with a 400 kHz bandwidth.

In the second section, a novel programmable TDA with femtosecond resolution is presented. The TDA is simulated in a 1 V 65 nm TSMC CMOS process to validate the accuracy of the proposed architecture. The linearity of the proposed TDA is verified from 150 fs to 200 ps with a gain error of less than $\pm 4\%$, while consuming 519 μW with a 450 MHz clock frequency.

Most of the material from this chapter are adapted to the following papers:

S. Ziabakhsh, G. Gagnon, G. W. Roberts, "Wide linear range voltage-controlled delay unit for time-mode signal processing", *IEEE International Symposium on Circuits and Systems (ISCAS)*, Portugal, 2015.

S. Ziabakhsh, G. Gagnon, G. W. Roberts, "An All-Digital High-Resolution Programmable Time-Difference Amplifier Based on Time Latch", *IEEE International Symposium on Circuits and Systems (ISCAS)*, Italy, 2018.

4.2 Wide Linear Range VCDU

4.2.1 Basic Concepts

One of the basic component of TMSP circuits is a VCDU, which converts input voltage signals into proportionally-delayed versions of a reference clock signal (Taillefer *et al.*, 2009). Signal processing can then be performed on these time-mode signals using either a synchronous or asynchronous approach to implement analog or mixed-signal circuits.

The linearity of VCDUs is important because it defines the dynamic range of the TMSP circuits that follow. Previously published VCDU designs exhibit a linear input range of 200 mV (Macpherson, 2013) to 400 mV (Taillefer *et al.*, 2009). This section proposes a novel VCDU design which uses a signal conditioning circuit to extend the input voltage linear range. The proposed circuit works without any operational amplifier or comparator, which would increase chip area and power consumption.

4.2.2 Proposed VCDU Design

The proposed VCDU, which is based on the design in (Taillefer *et al.*, 2009), is shown in Figure 4.1. The circuit works by charging and discharging capacitor C_w, which is formed by the parasitic drain capacitors of M_1 and M_2 and the gate capacitors of M_5 and M_6. If the reference signal ϕ_{clk} is high, M_1 is turned off and the capacitor discharges from V_{DD} to zero through NMOS transistors M_{2-4}. During the discharging phase, when the voltage of capacitor C_w is less than the threshold of inverter transistors M_{5-6}, the output ϕ_{out} switches to high. The discharging of the capacitor C_W begins on the rising edge of the reference signal ϕ_{clk} through transistors M_{2-4}. The discharge rate of the capacitor is:

$$\frac{dV_{CW}}{dt} = \frac{-I_{D2}}{C_W} = \frac{-(I_{D3}+I_{D4})}{C_W} \tag{4.1}$$

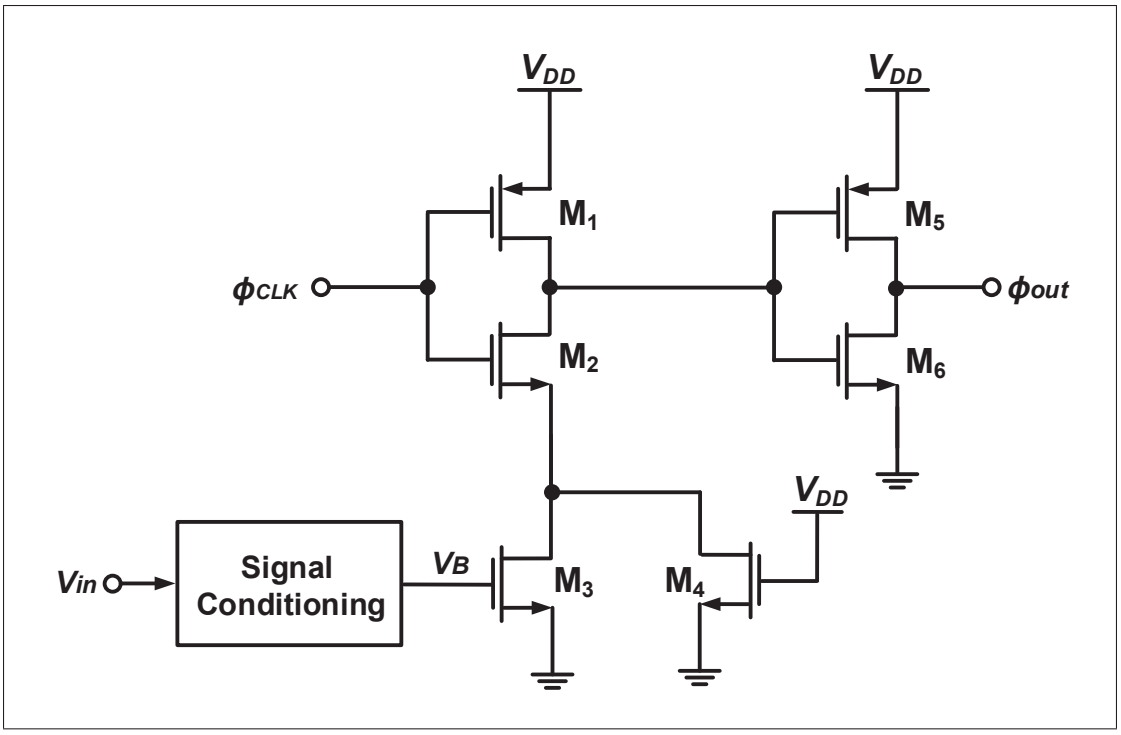


Figure 4.1 Schematic of the proposed VCDU with signal conditioning block.

where V_{CW} is the voltage across C_W, and I_{D3} and I_{D4} are the drain currents of M_3 and M_4, which are in triode in most of the input voltage range. When ϕ_{clk} is high, M_2 is ON and $V_{DS3} = V_{DS4} \simeq V_{CW}$. Therefore (D. A. Johns and K. Martin, 2008),

$$I_{D3} = \mu_n C_{ox} \frac{W_3}{L_3} \left(\left(V_B - V_{th,n} \right) V_{CW} - \frac{1}{2} V_{CW}^2 \right) \tag{4.2}$$

$$I_{D4} = \mu_n C_{ox} \frac{W_4}{L_4} \left(\left(V_{DD} - V_{th,n} \right) V_{CW} - \frac{1}{2} V_{CW}^2 \right) \tag{4.3}$$

where μ_n is the mobility of the carriers, C_{ox} is the gate oxide capacitance per unit area, W/L is the aspect ratio of the respective transistors and $V_{th,n}$ is the threshold voltage of NMOS transistors. Eqs. 4.2 and 4.3 indicate how the voltage V_B changes the time constant of the discharging path and thus controls the delay of the output signal.

The time-difference interval between rising edges of ϕ_{clk} and ϕ_{OUT} is a representation of the input signal in the time domain. This time-difference is controlled by capacitor C_W, control

voltage VB, and transistors in the discharging path. This design is linear for an input voltage between 0.8 V to 1.2 V (Taillefer *et al.*, 2009), the nonlinearity at lower input voltages being mainly caused by M_3 entering the subthreshold region.

In order to increase the linear input range of the VCDU, the signal conditioning circuit of Figure 4.2 is proposed. This circuit improves the linearity range by two mechanisms. A DC offset is applied to the input voltage while the circuit has an exponential response in the midrange (from 0.5 V to 1.2 V). This is achieved by combining two voltage sources through transistors M_{12} and M_{13}. The DC offset is realized with the voltage divider formed by R_1 and R_2 and two NMOS transistors, M_{7-8}. The input voltage is increased through the diode-connected transistor M_8 and the gate-source of M_7. This DC offset ensures that M_3 is in saturation at low input voltages. Finally, the combination of transistors M_{9-11} with the DC offset generates the desired exponential response in the midrange. Figure 4.3 shows the transient response of the input-output signals for various input voltages when signal conditioning block is used. As can be seen from this figure, with the increasing the input analog signal, V_{in}, the time-difference between ϕ_{out} and ϕ_{clk} is decreased linearity from 0 V to 1 V. The transfer characteristics of the signal conditioning block is shown in Figure 4.4, including the effect of a $\pm 1\%$ and $\pm 5\%$ mismatch on the value of R_1. To our knowledge, this circuit is the first structure that applies transformations to the input signal to improve the linearity of TMSP circuits without using any operational amplifier.

4.2.3 Simulation Results

The (Taillefer *et al.*, 2009) VCDU and the proposed VCDU were designed and simulated using Spectre in a TSMC 0.18 nm CMOS process with a 1.8 V supply voltage. Figure 4.5 shows that the linear range of the VCDU was effectively extended using the proposed signal conditioning circuit, and that the conversion gain was also improved. For both VCDUs, the output data was exported to MATLAB, and a linear regression was performed to evaluate the linearity error.

Since a typical application of TMSP circuits is analog-to-digital conversion, we define the linear range of the VCDU as the input range for which the linearity error is less than half

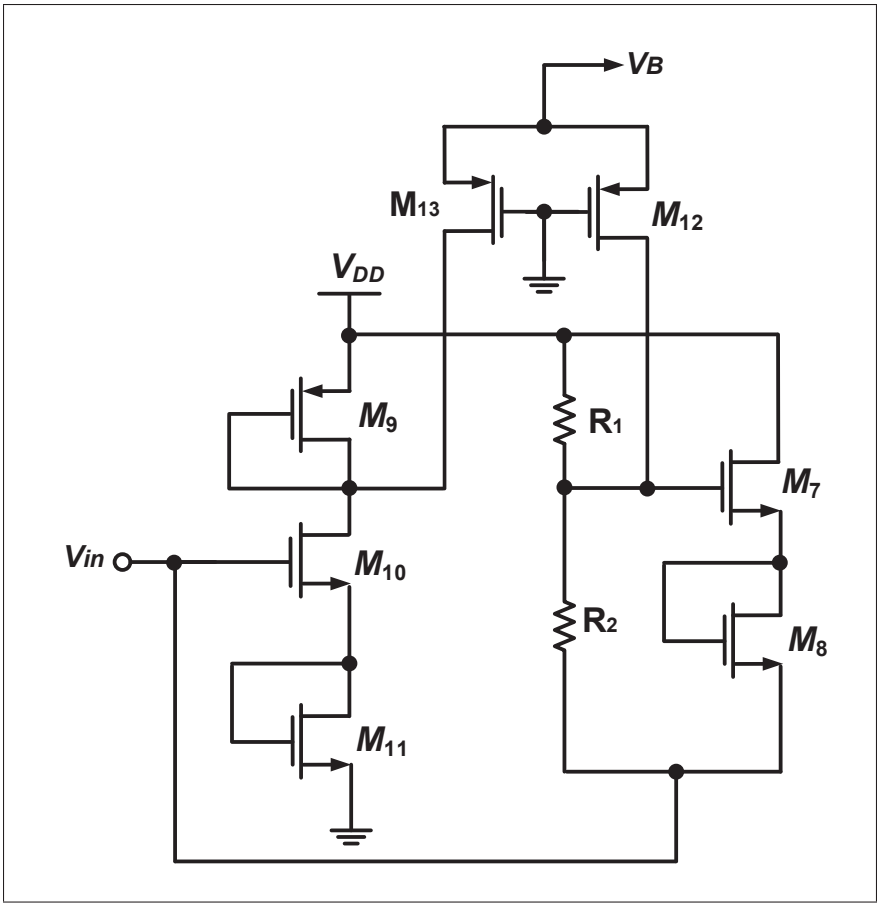


Figure 4.2 Circuit diagram of the proposed signal conditioning block.

the step of the LSB for an 8-bit ADC. For this purpose, the following relative linearity error calculation is used:

$$\varepsilon = \frac{E}{FS} \times 100 \tag{4.4}$$

where E is the largest deviation from the ideal (linear) behavior over the full scale linear range FS of input voltage. As shown in Figure 4.6, the linear range which provides 8-bit resolution ($\pm 2\%$) for the proposed VCDU is from 0.15 V to 1 V, which is suitable for low-voltage TMSP.

One of the anticipated issue with the proposed signal conditioning circuit is the sensitivity to the ratio of the values of resistors R_1 and R_2. To evaluate this sensitivity, simulations were performed by forcing a 1% error on the value of R_1. Figure 4.6 shows that the linearity error was not affected by this mismatch on R_1 and R_2, i.e. the linear range for 8-bit resolution is the

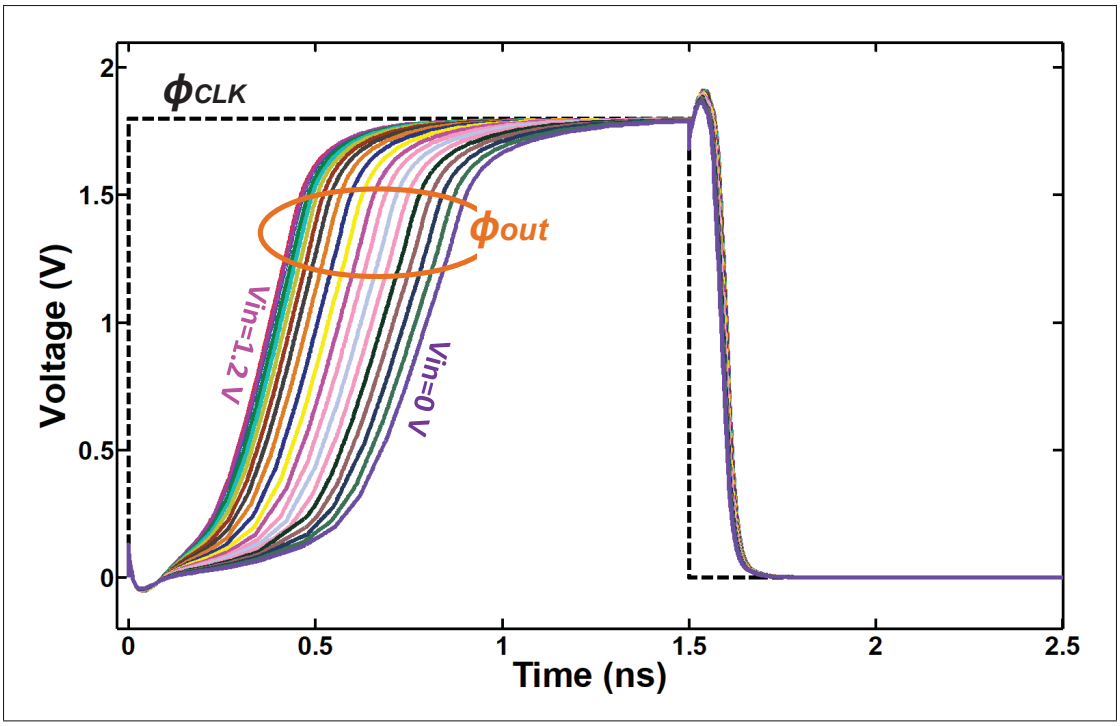


Figure 4.3 Transient response of the proposed VCDU for various input voltages (circuit-level simulation results).

same with the forced mismatch. Careful layout should ensure that the mismatch between R_1 and R_2 is kept below 1%.

The performances of the proposed architecture is summarized in Table 5.1 and compared with some reported VCDUs. In order to compare VCDU performances, we propose the following figure of merit (FOM):

$$FOM = \frac{P}{FS^2 \times f_s} \tag{4.5}$$

where P is power dissipation and f_s is the sampling frequency. The proposed FOM is in line with the commonly used FOM for ADCs (Le *et al.*, 2005). Using this metric, the proposed VCDU achieves a FOM of 0.86 pJ/V^2.

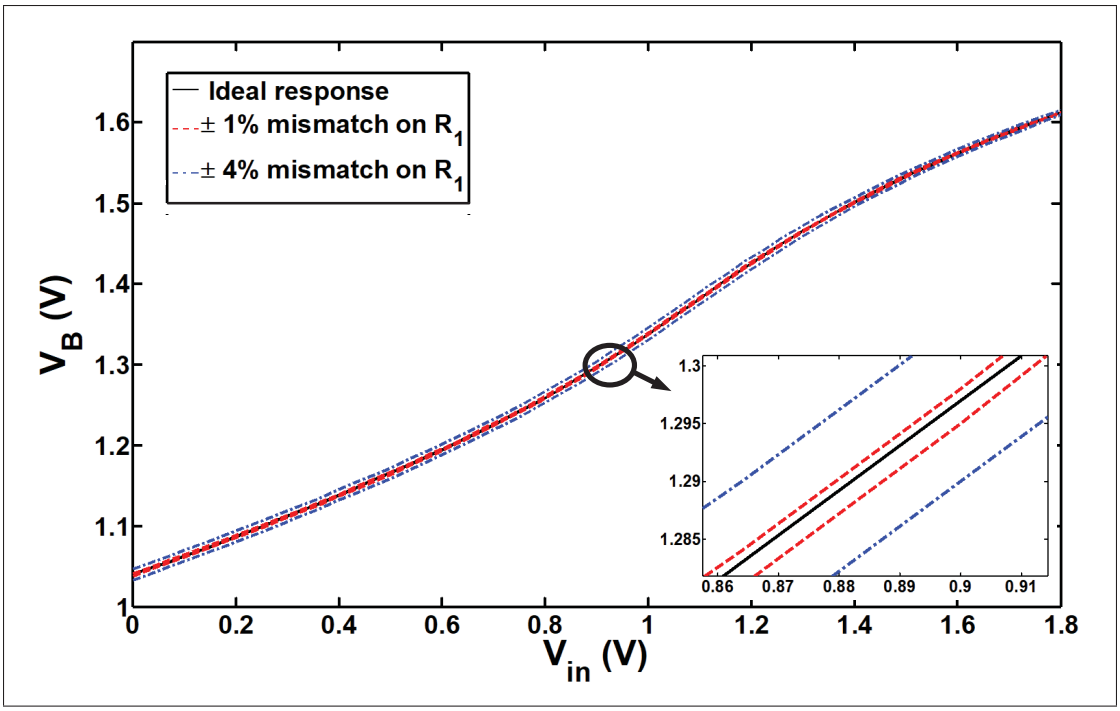


Figure 4.4 DC response of the signal conditioning block.

Table 4.1 Performance summary and comparison.

	Taillefer VCDU	**Macpherson VCDU**	**Proposed**
Conversion gain, G_ϕ	-92 ps/V	-250 ps/V	-311 ps/V
8-bit Linear range, FS	0.82 V - 1.2 V	-0.1 V - 0.1 V	0.15 V - 1 V
Max. sampling frequency, f_s	1 GHz	7.5 GHz	500 MHz
Power consumption, P	175 μW	4 mW	315 μW
FOM [pJ/V^2]	1.22	13.33	0.86

Simulation results are obtained at the Maximum sampling frequency.

4.2.4 Application To ΔΣ Modulation

Wide-range linear VCDUs have many applications in TMSP such as ΔΣ modulators, TDCs and digital phase-locked loops. In this section, the simulation of a time-mode ΔΣ modulator using the proposed VCDU is performed to evaluate its performance for this application.

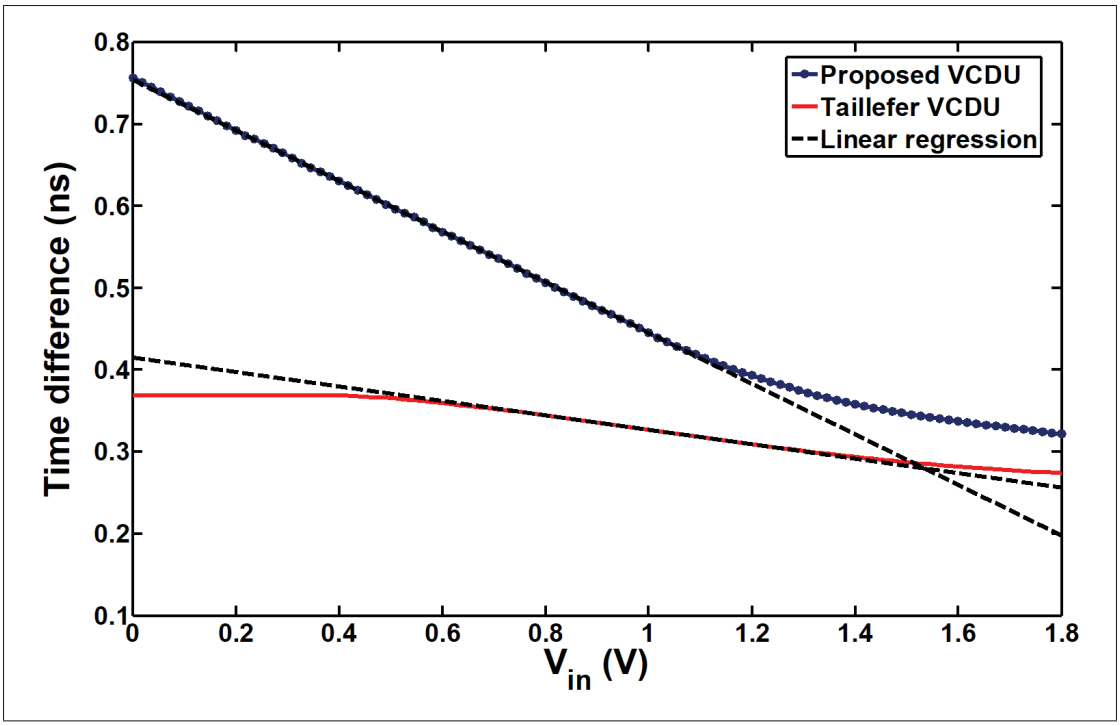


Figure 4.5 Transfer characteristic of Taillefer VCDU and proposed VCDU.

The modulator introduced in (Taillefer *et al.*, 2009) employs a VCDU in a time-mode ADC implementation with first-order noise shaping. The authors in (Taillefer *et al.*, 2009) suspected that the VCDU linearity might be the limiting factor for the SNDR performances.

The modulator is realized by two voltage-controlled ring oscillators, a DFF, and some digital inverters, as shown in Figure 4.7. The top ring oscillator converts the input signal to a time-difference information and adds it to the inverse of the digital output. The frequency of the bottom voltage-to-time integrator (reference oscillator) is controlled by the reference voltage V_{ref} to provide the sampling frequency. The DFF is a one-bit quantizer to convert the time difference between the input and the reference oscillators to a digital representation.

The differential equation between the output and input of this modulator is given by:

$$V_{out}[n] = V_{in}[n-1] + \frac{1}{G_\phi}\left(\Delta T_\varepsilon[n] - \Delta T_\varepsilon[n-1]\right) \tag{4.6}$$

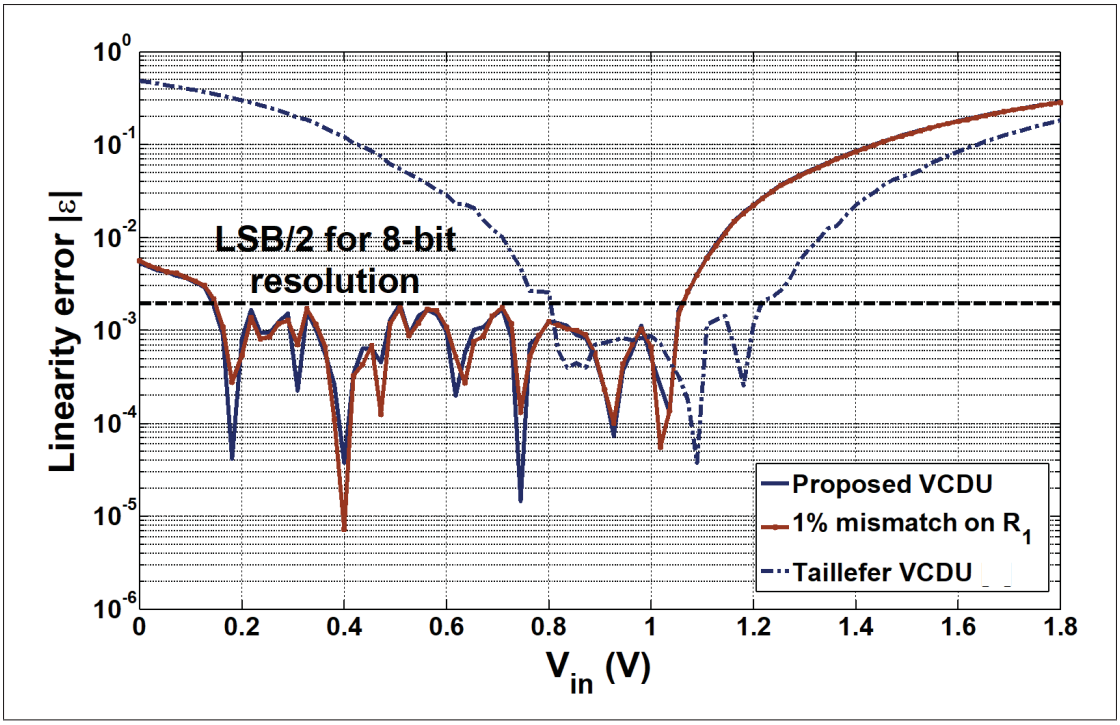


Figure 4.6 Linearity error of Taillefer VCDU and proposed VCDU.

where G_ϕ is the voltage-to-time conversion gain and $\Delta T_\varepsilon[n]$ is the quantization error made by the DFF.

This $\Delta\Sigma$ modulator was designed and simulated using Cadence Spectre in 0.18 μm CMOS technology using the proposed VCDU. The modulator operates over a range of input voltage from 0.15 V to 1 V. The signal ring oscillator is biased at a DC offset of 0.6 V with 400 mV peak-to-peak amplitude for a 111 kHz sinusoidal input signal. The reference voltage of the bottom voltage-to-time integrator V_{ref} is set to 1 V to provide a 140 MHz sampling frequency. The signal bandwidth is 400 kHz, yielding an oversampling ratio of 175.

Figure 4.8(a) plots the PSD of the modulator's output using the proposed VCDU, showing the 111 kHz input signal and first order noise shaping. The spur at 317 kHz is not an harmonic of the input signal caused by nonlinearity; it is caused by periodic quantization noise of the first order $\Delta\Sigma$ modulator. This spur, which could be removed by dithering, actually limits the SNDR of the modulator.

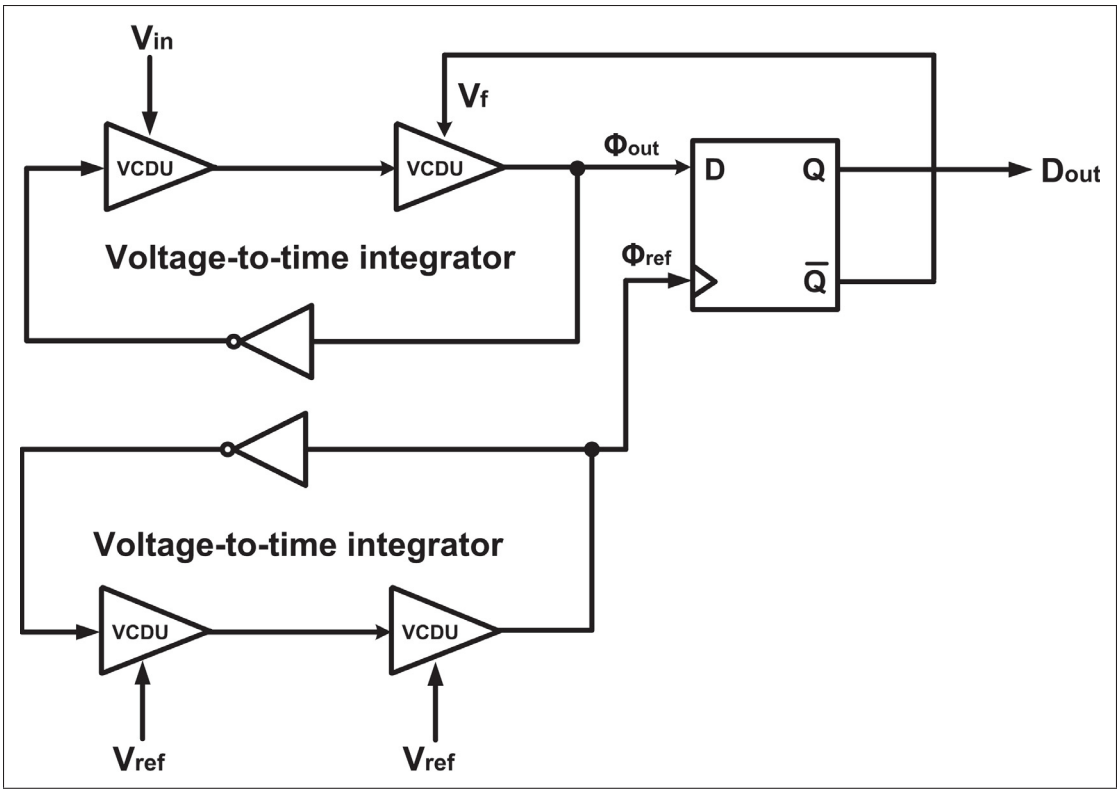
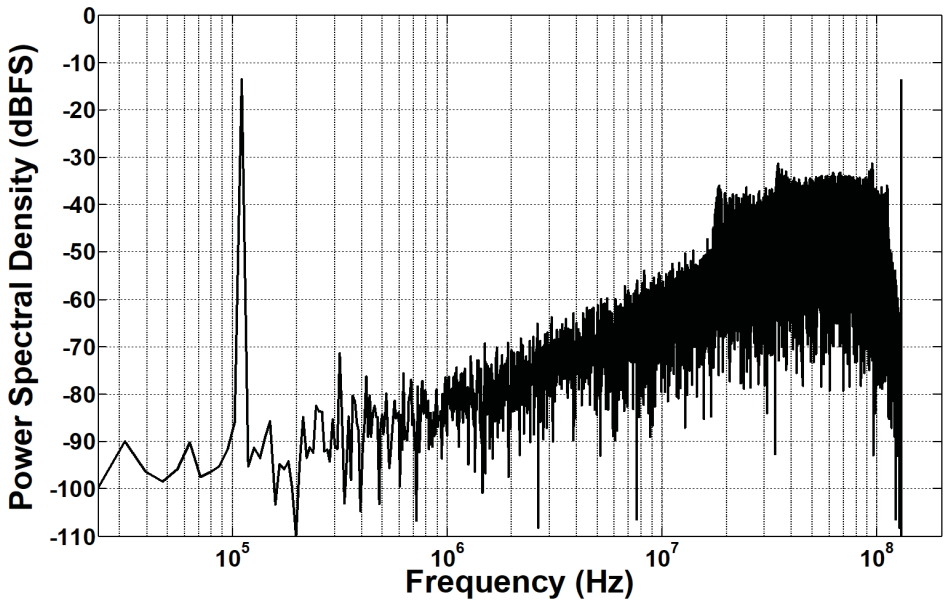
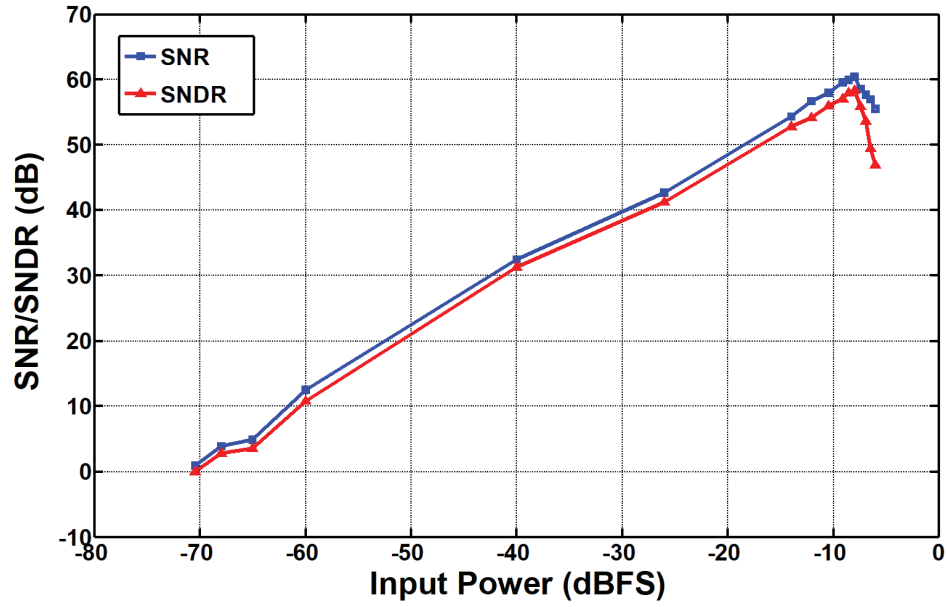


Figure 4.7 First-order single-bit time-mode ΔΣ modulator.

The SNR and SNDR versus input amplitude of the modulator are plotted in Figure 4.8(b). These simulation results show that the peak SNR is 60 dB and peak SNDR is 58 dB. In comparison, the single-ended modulator in (Taillefer *et al.*, 2009), also using 0.18 nm CMOS technology, the same bandwidth and sampling frequencies, achieves a peak SNDR of 42 dB, thereby confirming that by increasing the VCDU linearity, improved performances are obtained for the time-mode ΔΣ modulator.



a) PSD of the modulator output.



b) SNR/SNDR versus input power.

Figure 4.8 Simulation results of the first-order ΔΣ modulator using the proposed VCDU.

4.3 An All-Digital High-Resolution Programmable TDA Based on Time Latch

4.3.1 Basic Concepts

TDAs have been widely employed in the design of TMSP such as time-domain arithmetic (Heo *et al.*, 2014), ToF (Vornicu *et al.*, 2017), ADPLL (Lyu *et al.*, 2017), ADCs (Oulmane *et al.*, 2005; Hsu *et al.*, 2008; Naraghi *et al.*, 2010; Kim *et al.*, 2013), on-chip jitter measurement (Cao *et al.*, 2012), medical imaging (Chen *et al.*, 2017), and TDCs (i.e., two step, pipeline, cyclic) (Heo *et al.*, 2014). In these applications, it is crucial to have high time resolution with a wide dynamic range for accurate signal representation. With the development of CMOS processes and digital technologies, the resolution of time-mode circuits can be improved in the range of picoseconds (Oulmane *et al.*, 2004). However, this excellent resolution is limited to the CMOS inverter delay and requires more circuitry to achieve sub-gate resolution with suitable dynamic range (Chen *et al.*, 2014). Therefore, TDAs often require extra components such as calibration circuit (Lyu *et al.*, 2017) or analog component (Dehlaghi *et al.*, 2011; Kwon *et al.*, 2014) to effectively improve the resolution and dynamic range.

Previous TDA designs were built based on the time expansion in SR latches when operating in metastable region, which unfortunately limits the gain accuracy and predictability due to nonlinearity (Lyu *et al.*, 2017). Further developments of TDAs based on metastability of cross-coupled architectures were introduced (Oulmane *et al.*, 2005; Kim, *et al.*, 2013). These designs, however, mainly suffer from a limited dynamic range with a constant gain due to device mismatch. In (Heo *et al.*, 2014), regeneration time control with programmable transconductance in a SR latch-based TDA is employed, resulting in programmable gain. However, many time-mode circuit applications require an increased dynamic range and operational frequency. Although calibration using a DLL can be used to compensate the mismatch issue, efforts are required to improve linearity and keep the gain constant. Another method to amplify ΔT_{in} up to 120 with programmable gain is to use the slew-rate control method (Kwon *et al.*, 2014). The concept of this method is discharging two capacitors from V_{DD} to ground through current sources with different slew rates. The gain of TDA is controlled by the ratio of current sources.

The slew rate based TDA uses analog components in its architecture which are typically very sensitive to the supply noise and mismatch of current sources, which increases the gain error.

This section presents a new method to improve the resolution of TDAs in the range of femtoseconds using standard time latches (also knows as a time register) to achieve linear, reliable, and programmable gain for a wide input range. Our time latch-based TDA performs amplification by activating the read signals of the time latches with a proper timing to generate time gain. Performing time gain using digital gates takes advantage of process scaling and can thus operate at higher frequencies with improved time resolution, reduced area and sensitivity to mismatch.

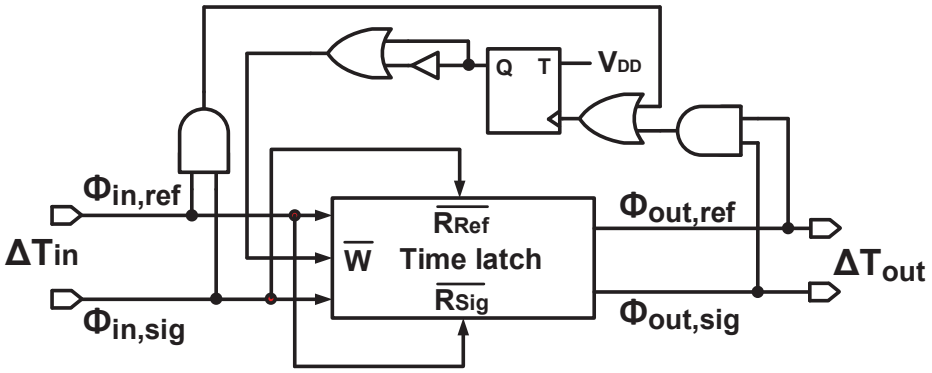
4.3.2 Proposed TDA

The proposed TDA uses the time addition and subtraction capabilities of the time latch, and a novel design using digital gates to control the various inputs of the time latch, thus manipulating the many pulse signals to obtain the desired time amplifier gain.

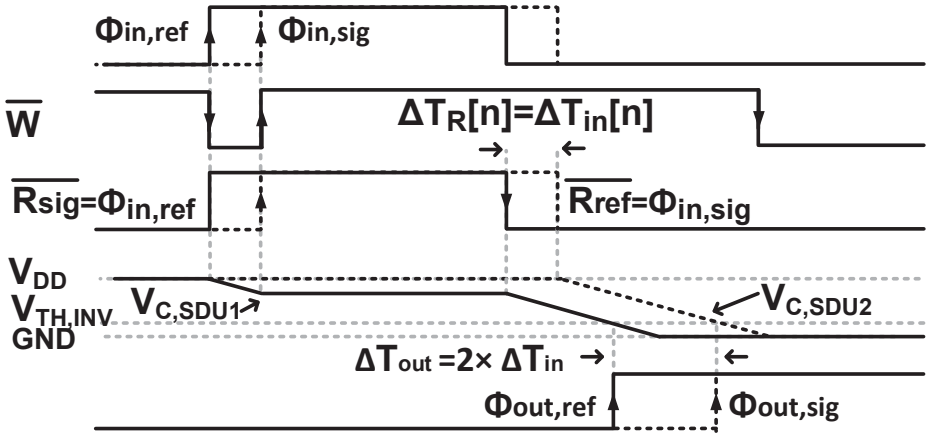
4.3.2.1 2×TDA Basic Operation

The first block to be described is a $2\times$ fixed-gain TDA, shown in Figure 4.9 with is timing diagram. To simplify the diagram, the propagation delay of gates, TFF, and internal delay of time latch have been ignored. At the rising edge of $\Phi_{in,Ref}$, $\overline{W}$ becomes low and captures the input time difference ΔT_{in}. At the rising edge of $\Phi_{in,Sig}$, $\overline{W}$ returns high and places the time latch in an idle state. By connecting $\overline{R_{Ref}}$ and $\overline{R_{Sig}}$ to signals $\Phi_{in,Sig}$ and $\Phi_{in,Ref}$, the read signal time difference is equal to the input time difference: $\Delta T_R = \Delta T_{in}$. Therefore C_{SDU1} starts to discharge earlier than C_{SDU2} by a time difference equal to ΔT_{in}. Combined with the discharging time difference during at the beginning of the cycle, which was also equal to ΔT_{in}, a time gain of two is obtained:

$$G = \frac{\Delta T_{out}}{\Delta T_{in}} = 2 \tag{4.7}$$



a) Circuit implementation.



b) Timing diagram.

Figure 4.9 Architecture of the 2×TDA block.

4.3.2.2 Digitally-Controlled TDA

The proposed TDA operates on the digital control signals of time latches to change the TDA's gain, without relying on analog components to extend the time difference. The proposed programmable gain TDA with an open-loop architecture is shown in Figure 4.10. The key concept that we exploit is that three cascaded time latches with different connections to the read signals can adequately control the gain digitally. Using this approach, the digital gain controller sets

the switches (SW_1 to SW_7) to determine which time difference ΔT from the input or output of time latches should go into to the read signals and thus control the gain.

Using the cascaded time latches, the proposed programmable TDA amplifies ΔT_{in} with a gain $G = \{2,3,4,5,6,8\}$[1]. To explain the operation of the proposed TDA, shown in Figure 4.10, Time latch$_1$ captures ΔT_{in} and amplifies it by two as explained in the previous section. The amplified time signal is then connected to the input of Time latch$_2$.

The signals $\overline{R_{Ref2}}$ and $\overline{R_{Sig2}}$ can produce a gain of $2\times$, $3\times$, and $4\times$ depending on configuration of the switches. These selection signals are generated when Time latch$_1$ delivers its output. As soon as $\phi_{out,ref1}$ and $\phi_{out,sig1}$ readout completely, $\overline{W}$ will be set to "0" and ready to latch the time information. For the $G = 4$, SW_3 should be on so as to add ΔT_{out1} with itself. However, for proper operation, the falling edges of signals $\overline{R_{Ref2}}$ and $\overline{R_{Sig2}}$ must be ready before the falling edges of ΔT_{out1}. To ensure such timing, digital buffers with fixed delay of $\tau_Q = T_s/2$ are added in Time latch$_2$. Time latch$_3$ follows the same approach and provides the the gain of $5\times$, $6\times$, and $8\times$ in combination with Time latch$_2$. The same buffer is also added in the read signals path of Time latch$_3$ to match the delay between ΔT_{out2} and signals connected to SW_6 and SW_7.

[1] G=7 can be realized at the cost of requiring extra time latch which consumes more power and area.

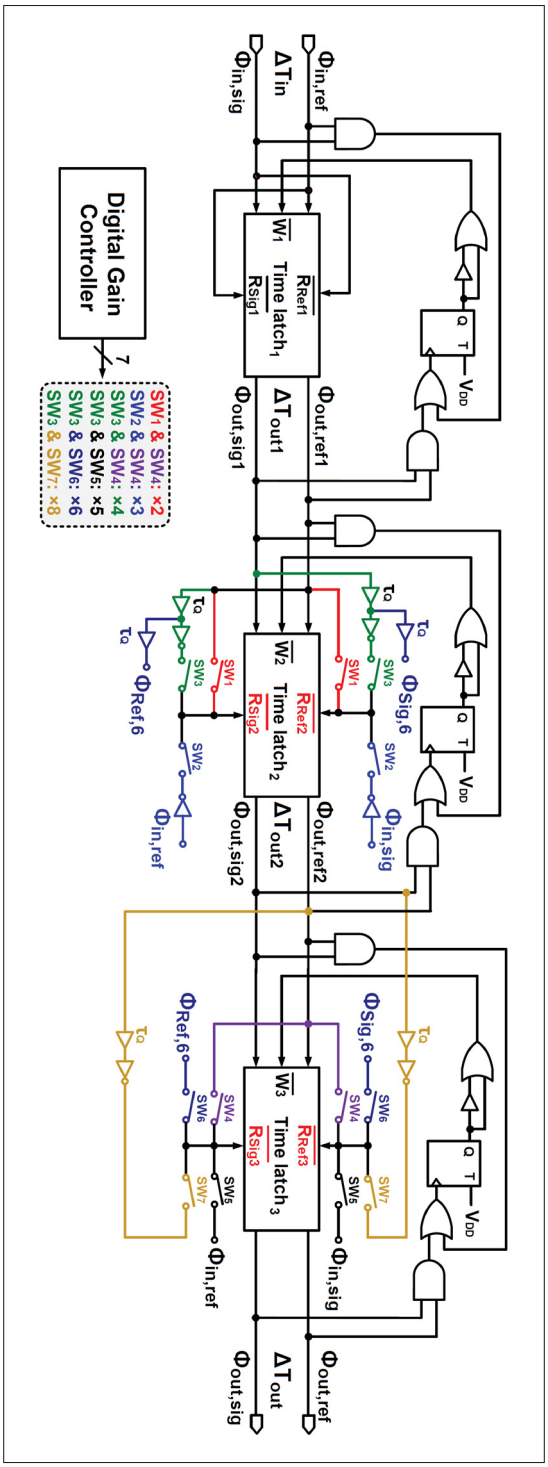


Figure 4.10 Circuit implementation of the programmable TDA.

4.3.3 Simulation results

To evaluate the performance of the proposed TDA, Spectre simulations in 65 nm TSMC CMOS process were carried out. The proposed TDA was designed to have a time resolution of 150 fs with a MIM capacitor C_{SDU} = 50 fF.

Figure 4.11(a) shows the simulated transfer curves of the proposed programmable TDA. The linear amplification range for $G = \{2,3,4,5\}$ is from 150 fs to 200 ps, but restricted to a maximum of 100 ps for $G = \{6,8\}$ due to output saturation when using higher gain values. The gain error is determined by $\frac{\|Gain_{actual} - Gain_{ideal}\|}{Gain_{ideal}} \times 100\%$ and is shown in Figure 4.11(b) for the different gain settings. The gain error remains below $\pm 4\%$ for all gains. The average power consumption for various time inputs is 518.8μW using a 450 MHz clock frequency and 1 V supply voltage. Note that these simulations were obtained without any calibration or tuning of any latch. To see the effect of process, voltage, and temperature (PVT) variations on the proposed TDA, Spectre simulations have been performed. Figure 4.12 shows the simulated gain error versus input time-differences on three process corners (FF, TT, and SS), and variations on supply voltage (1V$\pm$0.05V), and temperature (-10°C-80°C). This plot indicates that the gain error remains below $\pm 4\%$ under these PVT variations. Comparing these results to Figure 4.11, these variations do not introduce significant gain errors. To evaluate the sensitivity of the proposed TDA in the presence of transistor mismatches among the digital components, the circuit shown in Figure 4.10 was simulated using a Monte-Carlo analysis. Figure 4.13(a) shows the histogram of the TDA's gain for the 2$\times$ case. It results in a mean of 2.02 and a standard deviation (std) of 0.04. For the 8$\times$ amplifier case, as shown in Figure 4.13(b) the mean and the std are 7.96 and 0.137, respectively.

The performance of the proposed TDAs is summarized in Table 5.2 with previously reported TDAs. Compared with previous works, the proposed TDAs achieve fine time resolution and large operating frequency without any calibration.

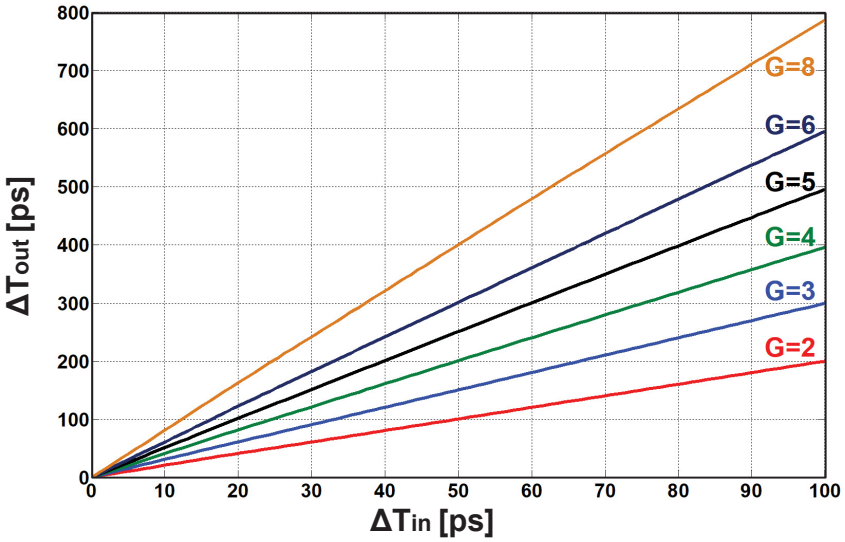
Table 4.2 Performance summary and comparison.

	(Y. Lyu, 2017)* **	**(K. Kim, 2013)**	**(S. K. Lee, 2010)*** **	**This work**
Gain	2	2-8	2	2-8*
Input range [ps]	$\pm$150	0-200	$\pm$100	0.15-200
Max. input frequency [MHz]	100	200	250	450
Process [nm]	65	65	180	65
Power [μW]	62	1200	-	518.8**

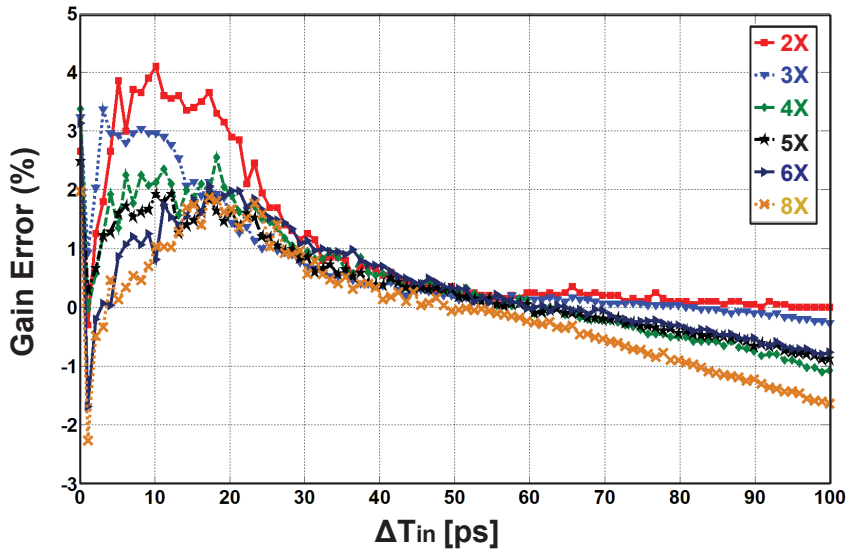
* G=7 is not included.

** Power consumption is obtained at the maximum sampling frequency. The power consumption is 336.48 μW for G=2.

*** Calibration is used.



a) Transfer curve.



b) Gain error.

Figure 4.11 Simulation results of the proposed TDA.

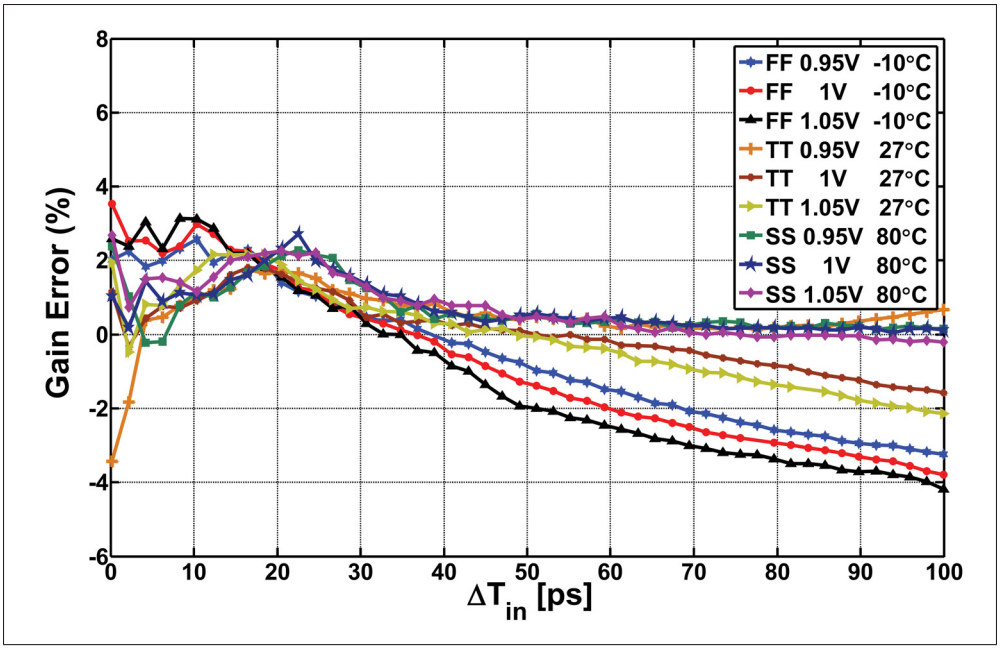
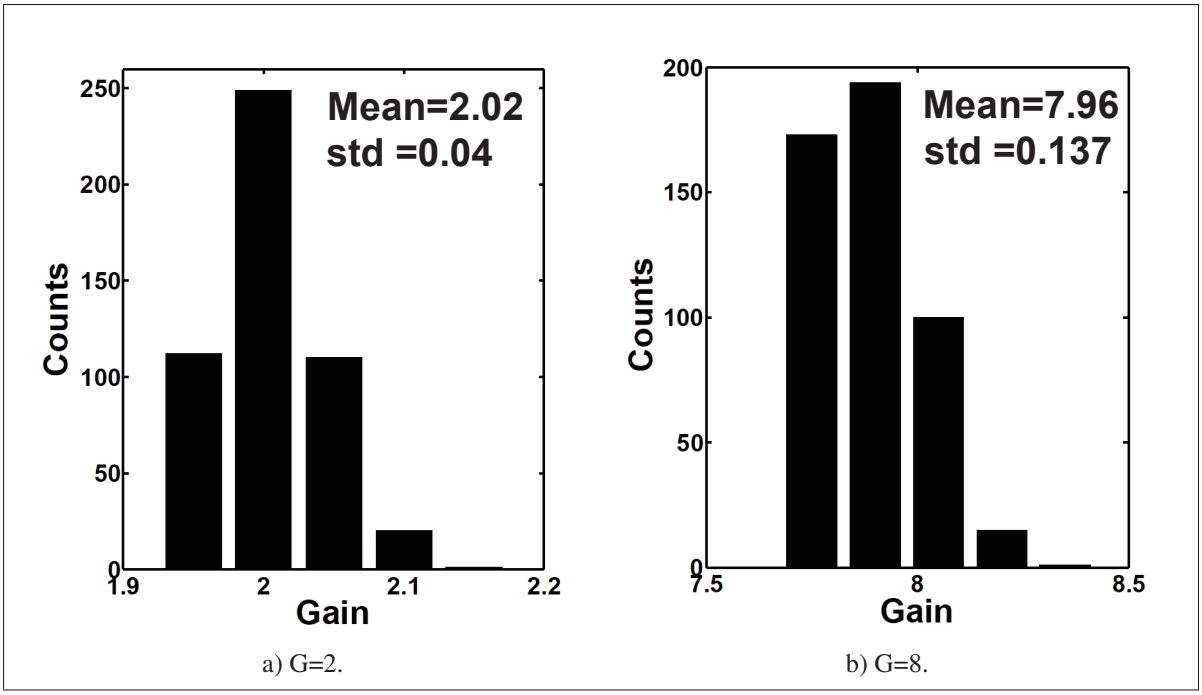


Figure 4.12 Simulation results of the programmable TDA for G=8× with PVT variations.

4.4 Conclusion

Two techniques for VCDU and TDA were described to improve the performance parameters. First, signal conditioning circuit was employed in the analog input port of the conventional design of VCDU to increase the linearity range. The circuit-level simulations confirm that the proposed architecture is linear from 0.15 V to 1 V with an equivalent 8-bit linearity error (±0.2%). The obtained voltage-to-time conversion gain is -311 ps/V and its power consumption is 315 μm being supplied by a 1.8 V source. Then, the new VCDU was used in the voltage-controlled ring oscillators of the first-order single-bit TM ΔΣ modulator and demonstrated promising SNDR in 140 KHz bandwidth.

Second, the design procedure of a novel programmable TDA with 150 fs resolution was explained. The first stage of the programmable TDA is a 2× gain stage built using one time latch and digital gates to control the read signals of the time latch which effectively re-adds the input time difference to the output signal. That 2×TDA can be used by itself in applications requiring a gain of two. The programmable TDA uses three time latches with digital switches to



a) G=2. b) G=8.

Figure 4.13 Monte-Carlo histograms of the programmable TDA (N=500). In this simulation, a constant input, $\Delta T_{in} = 500$ fs is applied to the TDA.

select the time amplification. The amplifier is simply controlled by changing digital switches. Simulation results confirm the operation of the proposed TDA. It produces a gain control from 2 to 8 (excluding G=7) with the gain error less than $\pm 4\%$. The simulated average of power consumption is 519 μW under 420 MHz clock frequency from a 1 V supply.

CONCLUSION AND RECOMMENDATIONS

This chapter concludes the research approaches used in this thesis to design highly efficient TM circuits. In the first section, the major achievements and contributions are introduced. In the second section, some possible future developments related to TM circuits are briefly discussed.

5.1 Thesis Summary

This thesis investigates the concept of TM circuits as an alternative approach to minimize the issues of performance degradation of analog circuits in advanced CMOS technology. In this approach, signal information in the analog domain is represented by a time-difference interval between two digital clocks. Consequently, shifting the signal processing from the voltage or current domains to the time domain enables the use of digital circuits instead of analog elements (capacitors, op-amps, etc.), which makes it very attractive for advanced CMOS process technologies.

One question that naturally arises is: can TM circuits provide higher operating performance than VM circuits? Today, all empirical data suggests that VM circuits outperform TM circuit realizations at similar power levels. In this thesis, the peak SNR of a PMOS-NMOS transistor stack used in both VM and TM circuits was evaluated. The analysis which includes both thermal and flicker noises was applied to different CMOS technology nodes and compared to Spectre transient noise analysis tools. In order to verify the validity of the proposed jitter analysis for TM circuits, a VCDU was designed and implemented. The silicon prototype was fabricated in the IBM 130-nm CMOS technology and the experimental results were presented.

New TM building blocks and extensions to some old ones were proposed, namely the the half-period delay unit, cascading of two half-period delay units, adaptive time offset correction, the TM subtractor, and the half-period delay DTC. At the core of all thesis blocks is a TLatch with some random and sequential logic to control its read, write, and reset signals. These signals

are generated by a block identified in the diagram as the Write Signal Producer to assert the write signal for each TLatch in the appropriate time sequence. As the timing of the read and write signals are referenced with respect to this signal, processing errors will decrease. All of the novel TM blocks were then combined to realize a novel TM LDI-based resonator to achieve high Q-factor. An important development with this work is the incorporation of a single negative feedback loop in a TM circuit. However,an important issue that arises with the use of a negative feedback loop in the resonator is the creation of a signal that falls outside the synchronization range. To accommodate negative TM signals, the sign of the TM quantity was recognized by Negative Time-Difference Detector and fed back to the read ports of a TLatch in the feed-forward path. In this implementation, the operation of the TLatch is changed from cycle-to-cycle and add or subtract the TM signals. The proposed resonator was designed to operate over a wide input range (ΔT_{in}) from 0 to 3.5ns under different sampling frequencies from 4 MHz to 43 MHz. Simulation results confirmed the accuracy of the proposed designs and techniques.

The above new TM building blocks as well as the resonator were used to implement a highly digital second-order BP$\Delta\Sigma$TDC. The proposed TDC achieves bandpass quantization noise shaping for a wide operating frequency range. TDC utilizes two on-chip techniques, synchronization and TM phase alignment, to compensate the timing errors from process variation and device mismatches. The prototype BP$\Delta\Sigma$TDC was fabricated in a IBM 130 nm CMOS process. It operates from 4 MHz to 42.8 MHz sampling frequency and achieves 39.5 dB SNDR, 39.9 dB SNR, and 45.4 dBc SFDR at 0.2 MHz bandwidth in a 42.8 MHz sampling frequency. It dissipates only 4.9 mW from a 1.2 V supply. The active area is 275.1 $\mu m \times 174.4\ \mu m$.

Finally, wide linear range VCDU and high-resolution programmable TDA were designed and simulated in TSMC 180 nm CMOS and TSMC 65 nm CMOS, respectively. The conventional design of VCDU generally suffer from voltage-to-time nonlinearity error and incurs tradeoffs

between range of operation, conversion gain, speed, and power consumption among others. Wide linear range VCDU was designed to eliminate voltage-to-time conversion errors by using a signal conditioning block. Circuit-level simulations show a linearity error of less than $\pm$ 0.2% for a 0.15 V to 1 V input range. The new VCDU consumes only 315 μW from a 1.8 V supply at its maximum sampling frequency of 500 MHz. The high-resolution programmable TDA described in this work demonstrated the potential for high resolution, high accurate, low power consumption, and silicon area usage. TDA with programmable gain was simulated in a 65 nm TSMC CMOS process to validate the proposed architecture. Simulation results show less than $\pm$4% gain error for 150 fs to 200 ps input time-difference range. The simulated average of power consumption is 519 μW from a 1 V supply at 450 MHz clock frequency.

5.2 Recommendation for Future Works

In this thesis, we propose for the very first time a second-order BP$\Delta\Sigma$TDC using digital-like TM arithmetic circuits suitable for BP data conversion. Pursuing this kind of research, recommendations and guidelines for further research works to advance and extend this work are:

(a) The analysis proposed in Chapter 2 only considered the SNR performance for a PMOS-NMOS transistor stack. In this analysis, the maximum output power was investigated. The developed modeling technique could be further extended and compares the speed, power consumption, chip area, and FOM for both VM and TM designs. Moreover, the performance of different designs of VM and TM circuits (i.e., voltage amplifier versus time amplifier, DAC versus DTC, flash ADC versus flash TDC, VM$\Delta\Sigma$ Modulator versus TM$\Delta\Sigma$ Modulator, etc.) can be compared.

(b) In this thesis, synchronization and TM phase alignment techniques were used to eliminate the timing error of the resonator and BP$\Delta\Sigma$TDC. However, TLatch as a key building block is very susceptible to the SDU's mismatches and PVT variations. An on-chip cal-

ibration circuit referenced to the main system clock to adjust for timing variations in the time-mode circuits can be used to enhance the manufacturability of TM circuits.

(c) At the circuit-level implementation, the noise shaping performance of the BPΔΣTDC could be further improved by decreasing the signal-dependent errors associated with every TLatch using DC offset cancellation technique. In addition, the TM phase alignment circuit was designed without calibration or DC offset cancellation in order to simply its implementation and tuning. The quality factor of the TM LDI-based resonator could be improved by reducing all the errors introduced by this block.

(d) The primary motivation for the BPΔΣTDC is that it directly and efficiently digitizes IF frequencies using a single-bit quantizer. Therefore, a natural extension to the research presented in this thesis is to implement BPΔΣTDC with a multi-bit quantizer to achieve higher resolutions. There would be a great research opportunities to develop the DTC circuit presented in Chapter 3 for TDCs with multi-bit quantizers.

(e) The input frequency of the BPΔΣTDC is centered exactly equal to $f_s/4$. In the literature, this parameter can be changed by a ratio of two capacitors in a SC architecture. The input frequency of the TDC could be changed using similar circuit techniques in the architecture of LDI-based resonator.

(f) Due to limitation of the SDU, the operating sampling frequency is limited to 43 MHz sampling frequency. The maximum clock frequency is mostly limited by charging time constant of the capacitor inside the SDUs. Hence, multiple capacitors with discrete tuning can be used in the SDUs to switch from low value to high value in different sampling frequencies. Therefore, it would be possible to digitize higher-frequency BP signals (i.e., f_s>100 MHz).

(g) It is believed this work (BPΔΣTDC) can be applied to the design of high-order BPΔΣTDC with a MASH structure.

(h) The measurement and verification of the BPΔΣTDC were achieved at the room temperature. It would be very important and worthwhile to consider this factor in the measurement. Since, some of the circuit parameters (i.e., V_{th}) can be affected by temperature. We predict minor issues related to temperature effect because of using adaptive delay circuits and synchronization.

(i) Throughout this thesis, we used a Verilog-A model for the VCDU in the input of the BPΔΣTDC. An on-chip VCDU with a rail-to-rail linearity range can be designed for this application.

(j) The wide linear range VCDU and high-resolution programmable TDA presented in chapter 5 were designed and simulated in Spectre. It would be interesting to have experimental results in characterizing of their performances.

APPENDIX I

CIRCUIT DESIGN PARAMETERS FOR ALL CIRCUITS

Appendix I offers the circuit design architecture, transistor dimensions (W/L), and component values required to reproduce the designs presented in chapter 3 and 5 of this dissertation.

1. Transistor Dimensions Of The BPΔΣ TDC

Section 1 describes the circuit diagram and all the transistor parameters needed for the implementation of the BPΔΣTDC in chapter 3. A prototype chip fabricated in the IBM 130 nm CMOS process. The supply voltage (V_{DD}) is 1.2 V.

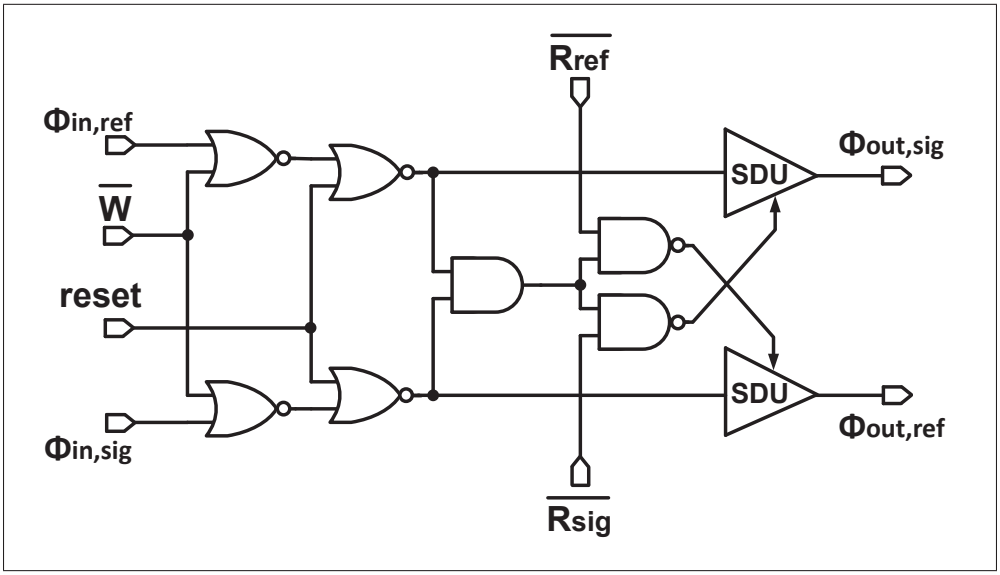


Figure-A I-1 Top-level schematic of the TLatch used in the implementation of BPΔΣ TDC.

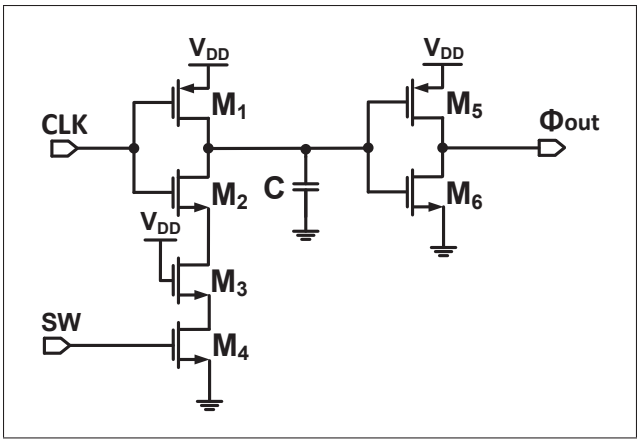


Figure-A I-2 The transistor schematic for the SDU block in Figure-A I-1.

Table-A I-1 The transistor dimensions (W/L) of the SDU.

M_1	M_2	M_3	M_4
7 μm/0.12 μm	2 μm/0.12 μm	0.54 μm/1.5 μm	1 μm/0.12 μm
M_5	M_6	C	
2 μm/0.12 μm	1 μm/0.12 μm	600 fF	

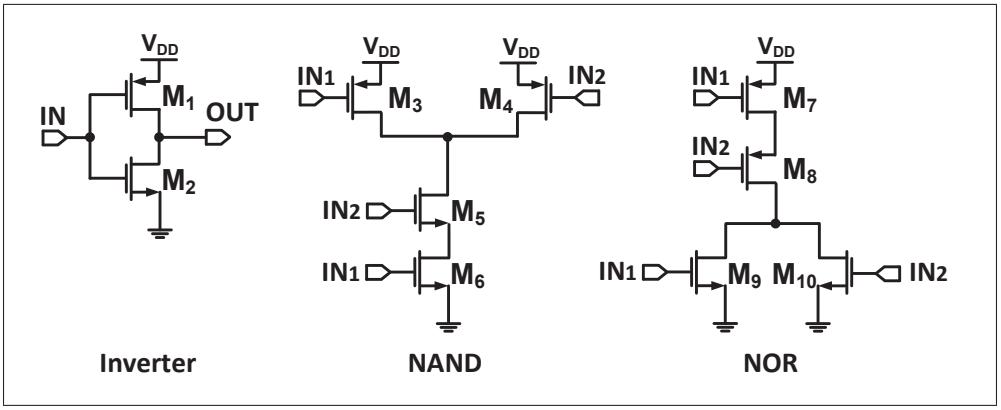


Figure-A I-3 The transistor schematic for the digital Inverter, NAND, and NOR gates.

Table-A I-2 The transistor dimensions (W/L) of the digital gates.

M_1, M_3, M_4, M_7, M_8	$M_2, M_5, M_6, M_9, M_{10}$
2 μm/0.12μm	1 μm/0.12 μm

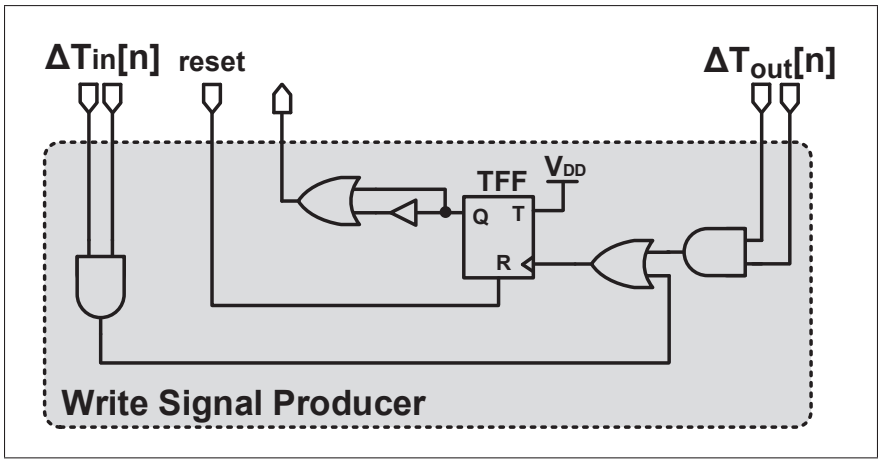


Figure-A I-4 The circuit diagram for the block Write Signal Producer.

Table-A I-3 The transistor dimensions in the schematic of Figure A- I-5

$M_1, M_3, M_7, M_9, M_{10}, M_{13}$	2 μm/0.12 μm
M_2, M_4, M_{11}, M_{12}	1 μm/0.12 μm
$M_5, M_6, M_8, M_{14}, M_{15}, M_{16}, M_{17}, M_{18}$	3 μm/0.12 μm
M_{19}, M_{21}, M_{23}	0.6 μm/0.12 μm
M_{20}, M_{22}, M_{24}	0.42 μm/0.12 μm

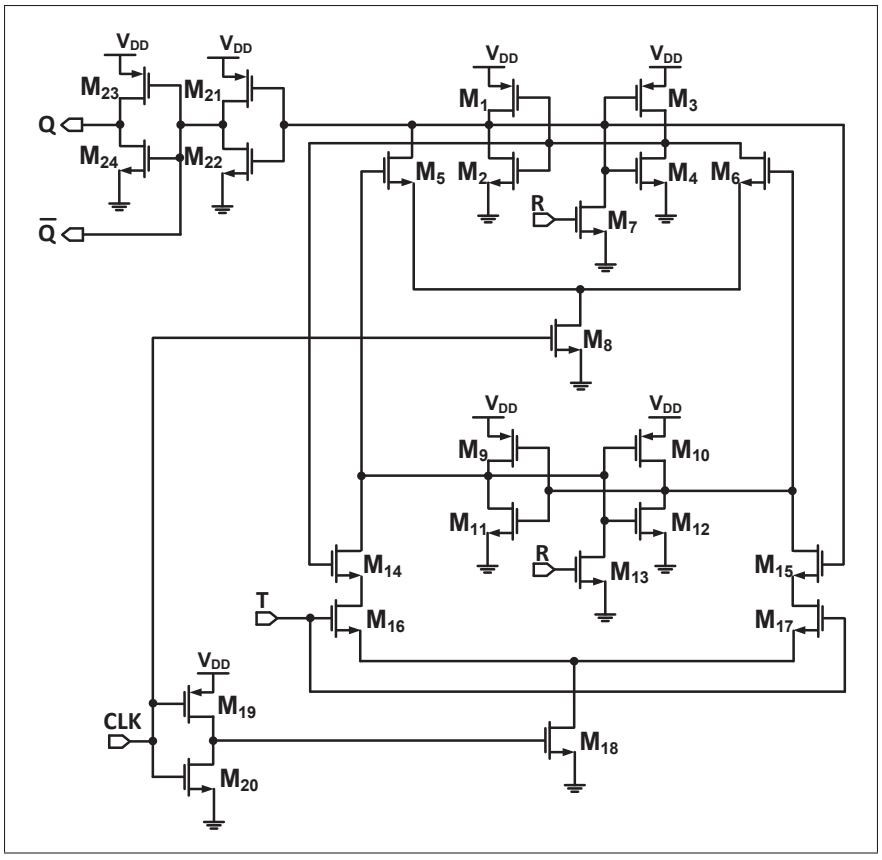


Figure-A I-5 The transistor schematic for the digital TFF used in Figure-A I-4.

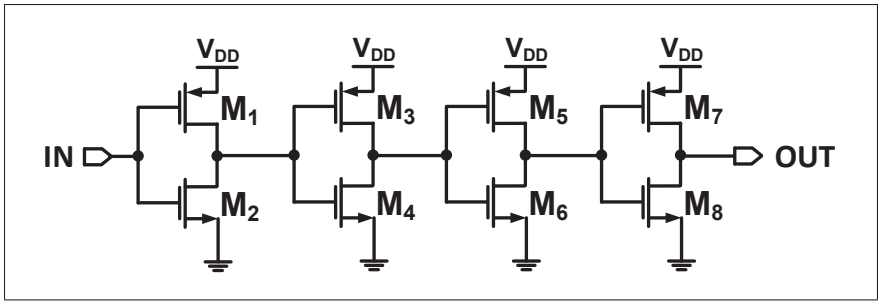


Figure-A I-6 The transistor schematic for the digital buffer used in Figure-A I-4.

Table-A I-4 The transistor dimensions in the schematic of Figure A- I-6

M_1, M_3	M_2, M_4	M_5
2 μm/1 μm	2 μm/1.62 μm	2 μm/4 μm
M_6	M_7	M_8
0.5 μm/2 μm	6 μm/0.12 μm	1 μm/0.12 μm

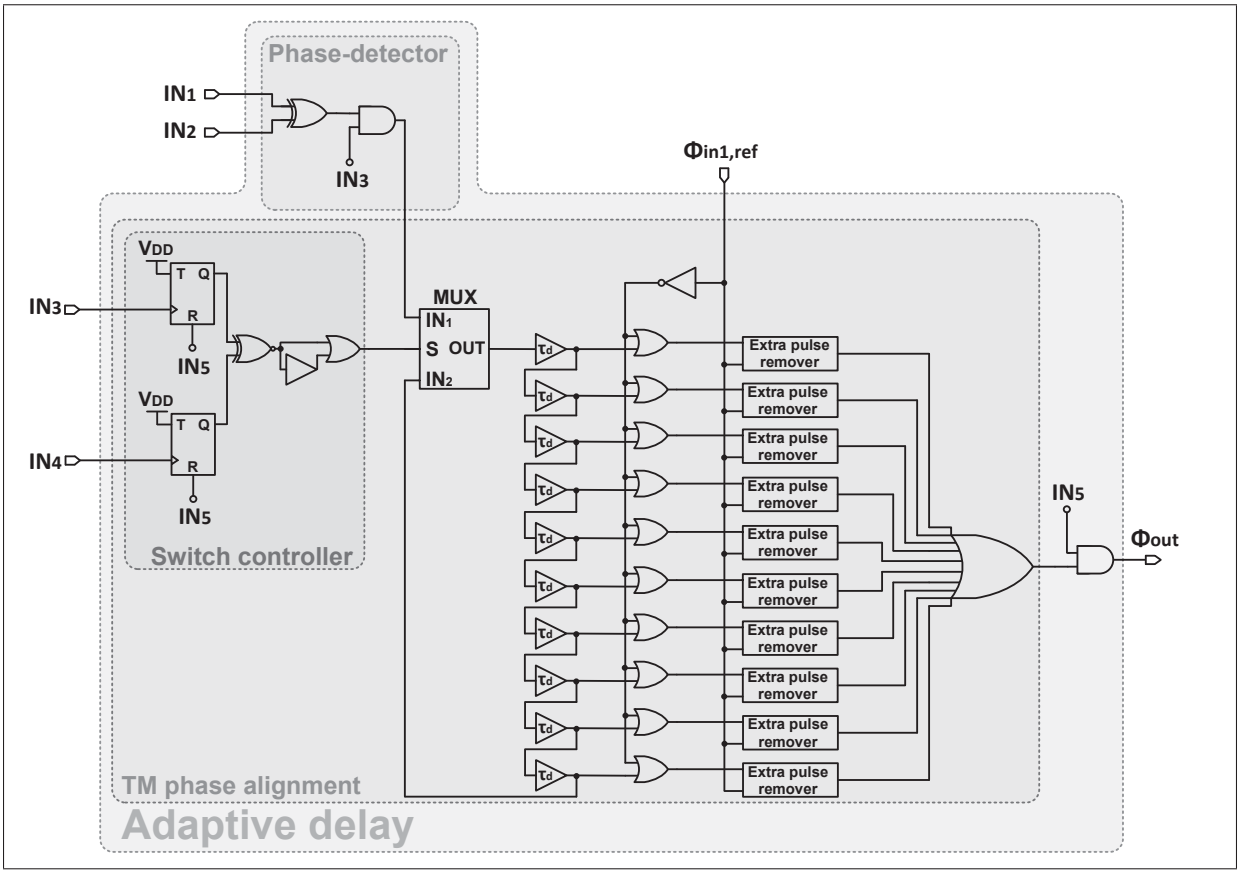


Figure-A I-7 Top-level schematic of the adaptive delay.

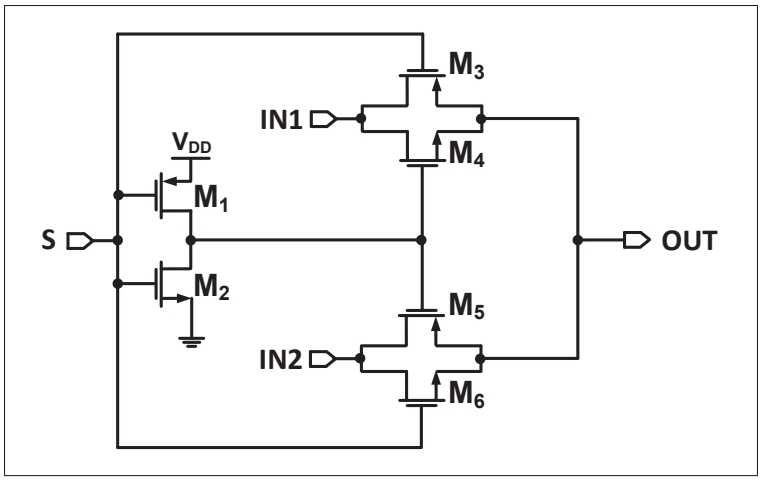


Figure-A I-8 The circuit diagram for the block MUX shown in Figure-A I-7.

Table-A I-5 The dimensions (W/L) of the transistors in the MUX.

M_1	M_2	M_3, M_5	M_4, M_6
0.6 μm/0.12 μm	0.42 μm/0.12 μm	2 μm/0.12 μm	1 μm/0.12 μm

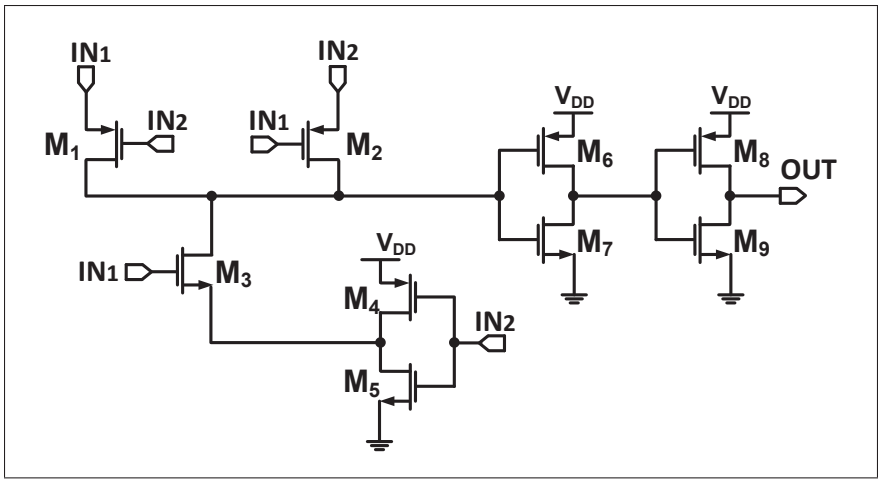


Figure-A I-9 The circuit diagram for the XOR shown in the phase-detector of Figure-A I-7.

Table-A I-6 The dimensions (W/L) of the transistors in the XOR block.

M_1 , M_2, M_4, M_6, M_8	M_3 , M_5, M_7, M_9
2 μm/0.12 μm	1 μm/0.12 μm

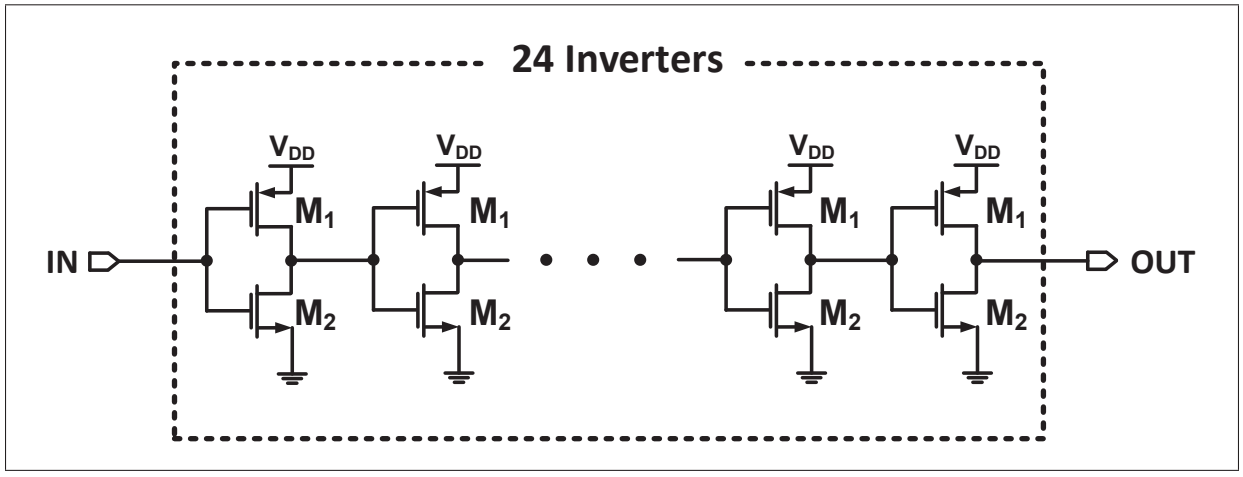


Figure-A I-10 The circuit diagram for the inverter chain shown in the TM phase alignment of Figure-A I-7.

Table-A I-7 The dimensions of the transistors in the schematic of Figure A- I-10

M_1	M_2
2.5 μm/0.12 μm	1.25 μm/0.12 μm

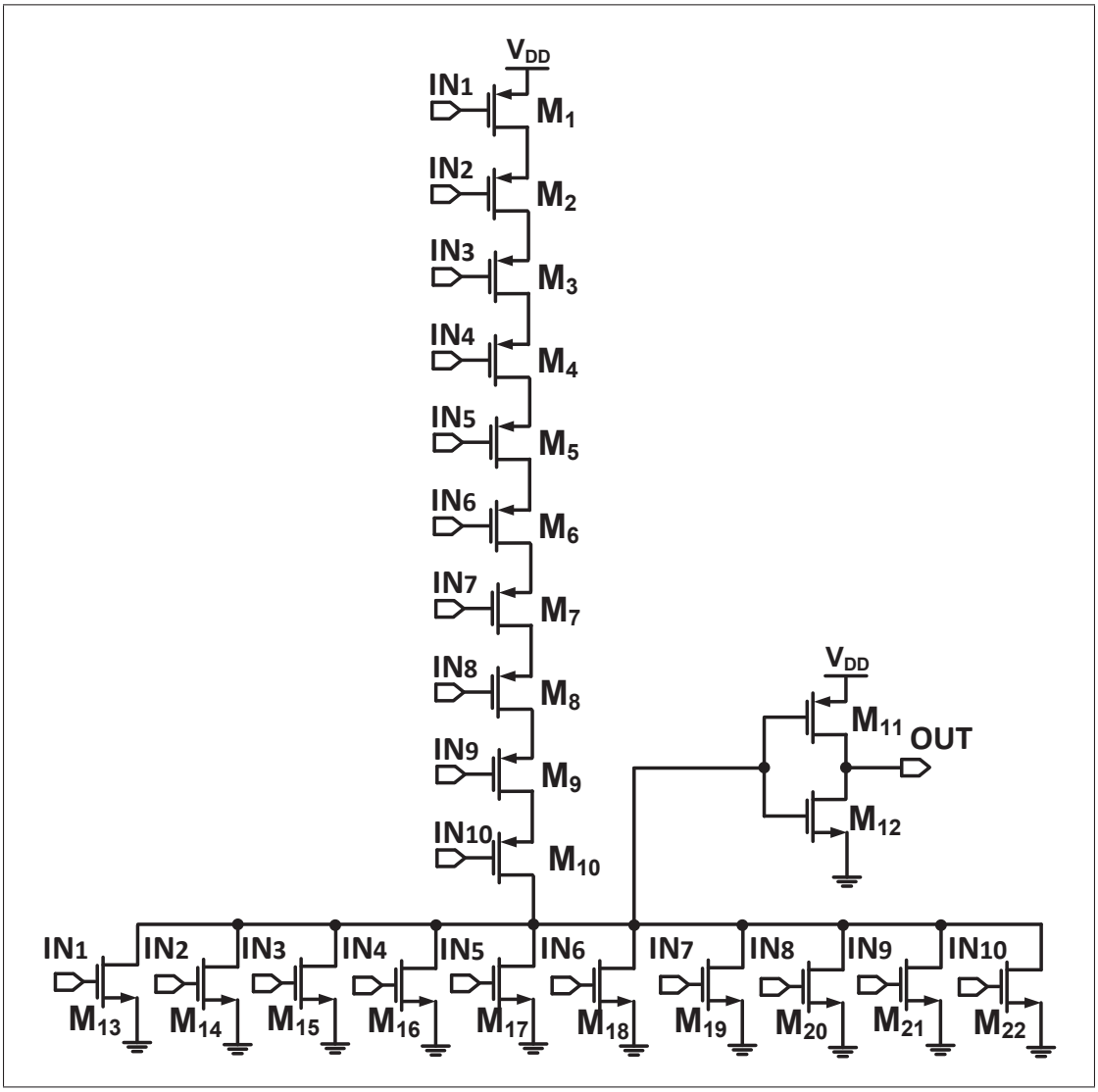


Figure-A I-11 The circuit diagram for the ten-input OR gate shown in the Figure-A I-7.

Table-A I-8 The dimensions (W/L) of the transistors in the schematic of ten-input OR gate.

$M_1 - M_{11}$	$M_{12} - M_{22}$
2 μm/0.12 μm	1 μm/0.12 μm

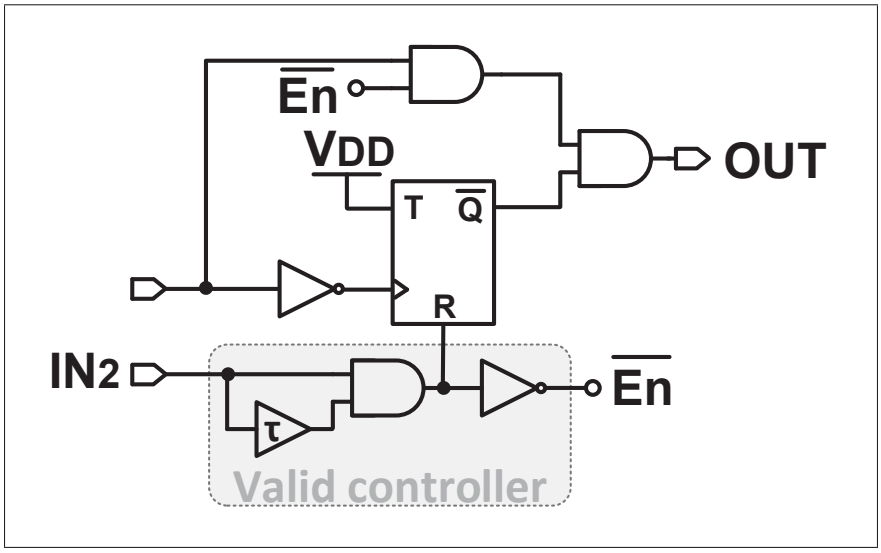


Figure-A I-12 The circuit diagram for the block Extra Pulse Remover shown in the Figure-A I-7.

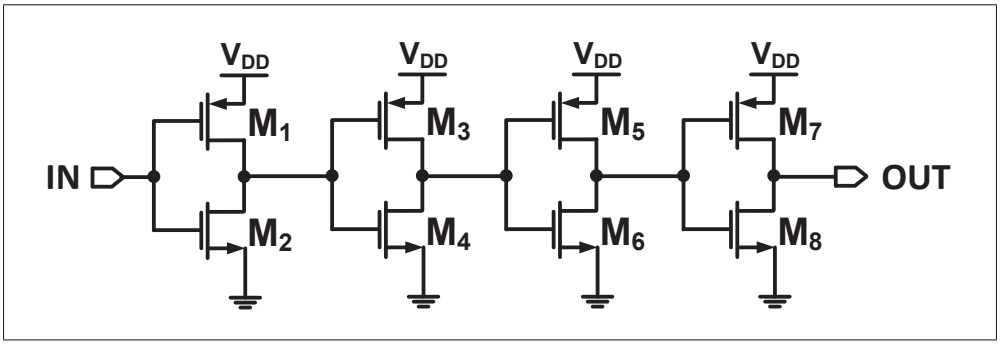


Figure-A I-13 The circuit diagram for the buffer in the Extra Pulse Remover (Figure-A I-12).

Table-A I-9 The dimensions (W/L) of the transistors in the schematic of buffer shown in Figure A- I-13

M_1, M_3, M_5	M_7
1.44 μm/0.48 μm	1.44 μm/0.36 μm
M_2, M_4, M_6	M_8
0.72 μm/0.72 μm	0.72 μm/0.36 μm

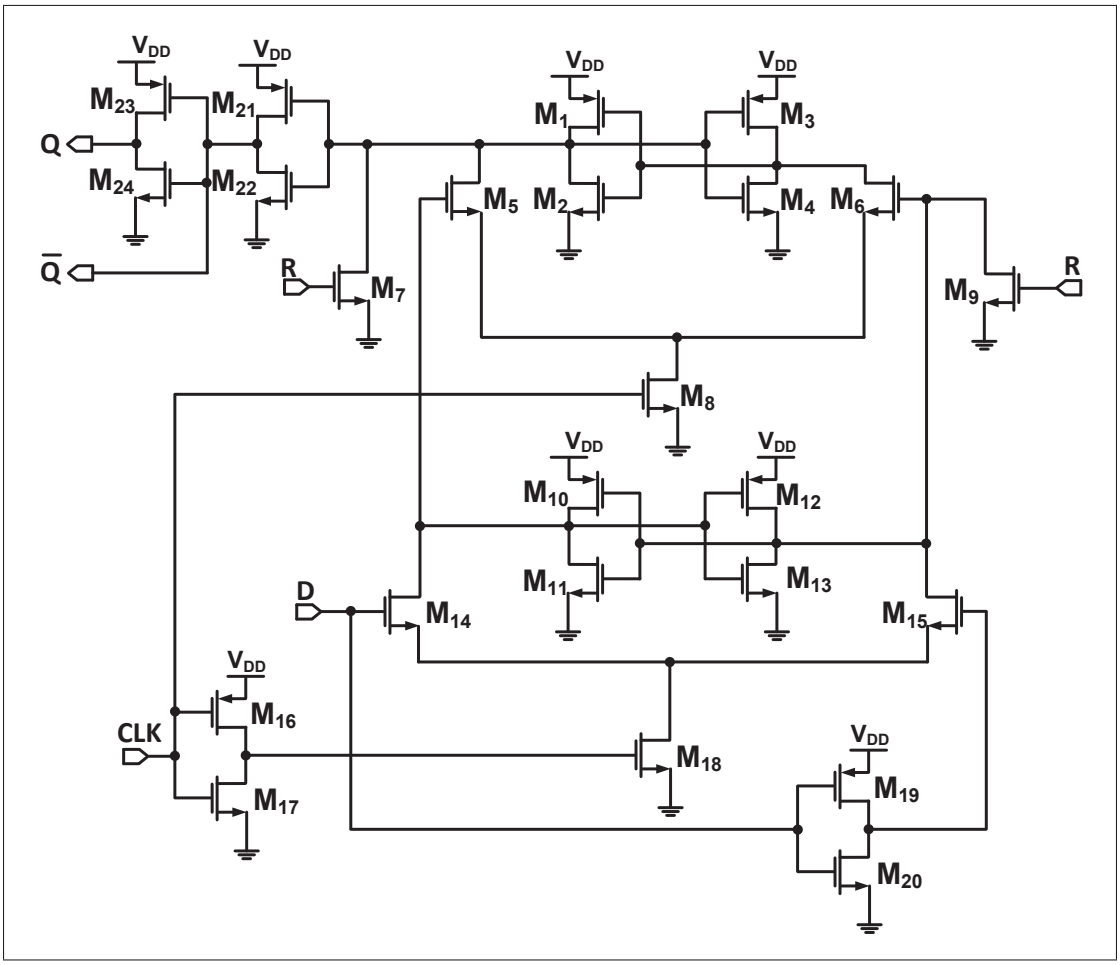


Figure-A I-14 The transistor schematic for the digital DFF used as an 1-bit quantizer in the BPΔΣTDC.

Table-A I-10 The transistor dimensions in the schematic of DFF.

$M_1, M_3, M_7, M_9, M_{10}, M_{12}$	2 μm/0.12 μm
M_2, M_4, M_{11}, M_{13}	1 μm/0.12 μm
$M_5, M_6, M_8, M_{14}, M_{15}, M_{18}$	3 μm/0.12 μm
M_{16}, M_{21}, M_{23}	0.6 μm/0.12 μm
M_{17}, M_{22}, M_{24}	0.42 μm/0.12 μm

Listing I.1: Verilog-A model of the VCDU used in Figure 3.31

```
1  `include "constants.vams"
2  `include "disciplines.vams"
3  module VCDU(OUT_REF, OUT_SIG, CLK, Vin);
4  output OUT_REF;
5  electrical OUT_REF;
6  output OUT_SIG;
7  electrical OUT_SIG;
8  input CLK;
9  electrical CLK;
10 input Vin;
11 electrical Vin;
12 parameter real gain = 1e-9;
13 parameter real period=1/(42.8e6);
14 parameter real frequency=42.8e6;
15 parameter real toff=0 from [0:inf);
16 parameter real td=0 from [0:inf);
17 real a;
18  analog begin
19      $bound_step (1/frequency);
20         @(timer(toff, period) or initial_step)
21             a = (V(Vin)) * (gain);
22             V(OUT_SIG) <+ absdelay (V(CLK) , abs(a) , period);
23             V(OUT_REF) <+ V(CLK);
24     $bound_step (1/frequency);
25           end
26 endmodule
```

Listing I.2: Verilog-A model of the TVC used in the simulation of BPΔΣTDC

```
1  `include "constants.vams"
2  `include "disciplines.vams"
3  module TVC(OUT_voltage, CLK_REF, CLK_SIG);
4  output OUT_voltage;
5  electrical OUT_voltage;
6  input CLK_REF;
7  electrical CLK_REF;
8  input CLK_SIG;
9  electrical CLK_SIG;
10 parameter real gain = 1/(1e-9);
11 parameter real thresh=0.9;
12 parameter real frequency=42.8e6;
13 parameter real td = 5e-9;
14 parameter integer dir = 1 from [-1:1] exclude 0;
15 integer armed;
16 real time_difference, t0, t1, out;
17 real b , s;
18 electrical c;
19           analog begin
20 $bound_step(1/frequency);
21         t0 = last_crossing (V(CLK_REF)-thresh, dir);
22         @(cross (V(CLK_REF)-thresh, dir))
23         armed = 1;
24         b = absdelay (V(CLK_SIG), td);
25         t1 = last_crossing (b-thresh, dir);
26         @(cross(b-thresh, dir)) begin
27           if (armed) begin
28           armed = 0;
29           time_difference = ((t1-td) - t0);
30           s = abs (time_difference);
31             if (s <= 0.3e-9) begin
32             time_difference = 0;
33                                end
34             out = ((time_difference * gain));
35                    end
36                                  end
37          V(OUT_voltage) <+ transition (out , 10f , 10f , 10f);
38          $bound_step (1/frequency);
39                   end
40 endmodule
```

2. Transistor Dimensions Of The Wide linear Range VCDU

This section presents the circuit diagram and all the transistor parameters of the wide linear range VCDU shown in chapter 5. The circuit is implemented in the TSMC 180 nm CMOS process. The supply voltage (V_{DD}) is 1.8 V.

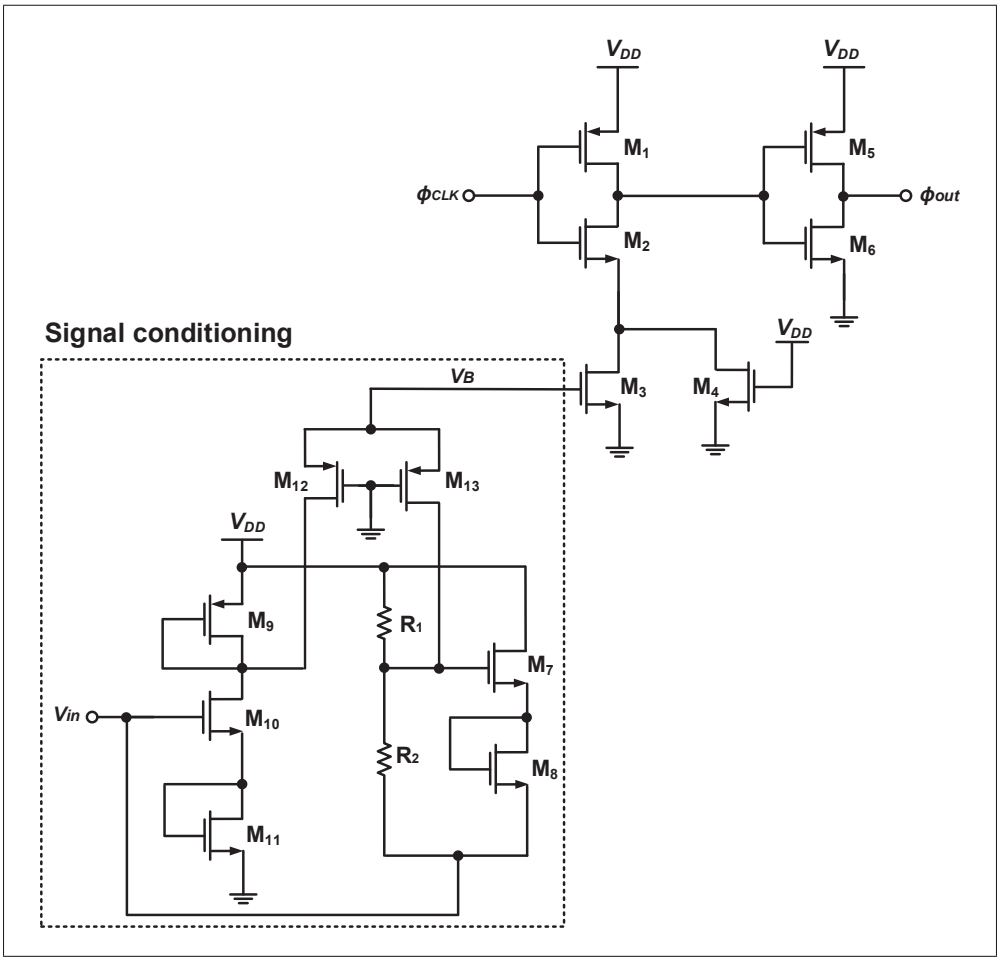


Figure-A I-15 The circuit diagram for the wide linear range VCDU with signal conditioning block.

Table-A I-11 The component values of the circuit shown in Figure-A I-15.

M_1, M_5	M_2, M_6	M_3	M_4
5 μm/0.36 μm	2 μm/0.36 μm	1 μm/4 μm	0.5 μm/6 μm
M_7, M_8	M_9	M_{10}, M_{11}	M_{12}, M_{13}
2 μm/0.36 μm	20 μm/0.36 μm	2 μm/0.36 μm	10 μm/0.36 μm
R_1	R_2		
5 K	3.5 K		

3. Transistor Dimensions Of The Programmable TDA

This section offers the transistor dimensions and component values of the all-digital high-resolution programmable TDA shown in chapter 5. The proposed TDA is simulated in a 65 nm TSMC CMOS process. The supply voltage (V_{DD}) is 1.0 V.

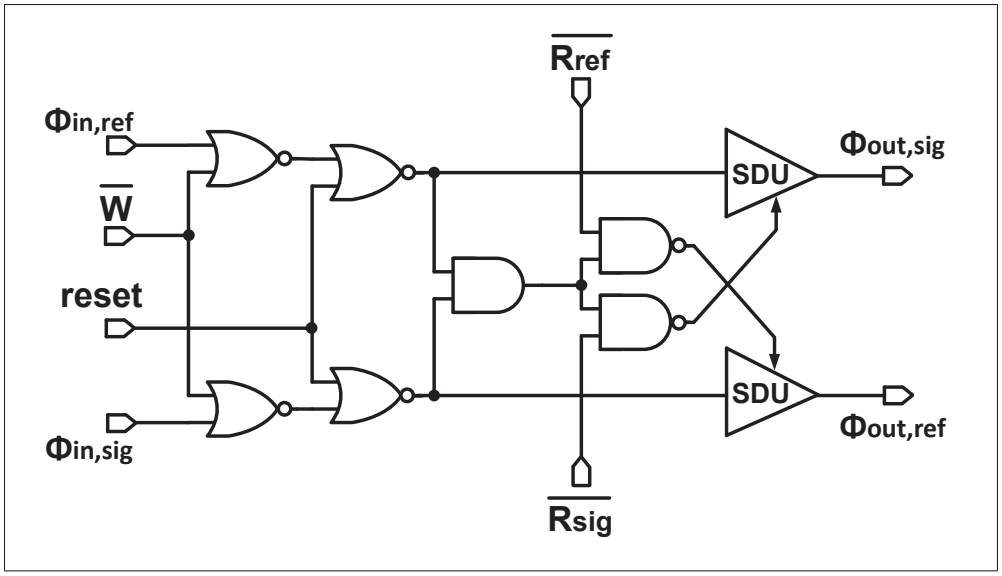


Figure-A I-16 Top-level schematic of the TLatch used in the design of all-Digital high-resolution programmable TDA.

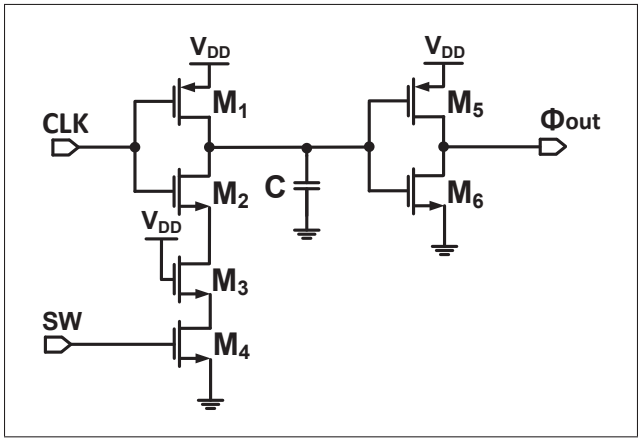


Figure-A I-17 The transistor schematic for the SDU block in Figure-A I-16.

Table-A I-12 The transistor dimensions (W/L) of the SDU.

M_1	M_2	M_3	M_4
3.5 μm/60 nm	0.6 μm/60 nm	0.27 μm/0.75 μm	0.5 μm/60 nm
M_5	M_6	C	
0.5 μm/60 nm	0.33 μm/60 nm	50 fF	

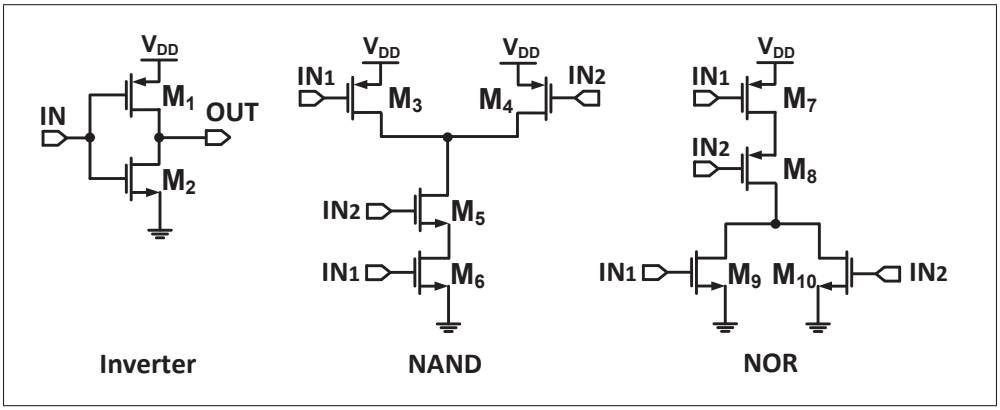


Figure-A I-18 The transistor schematic for the digital Inverter, NAND, and NOR gates used in the TLatch of Figure-A I-16.

Table-A I-13 The transistor dimensions (W/L) of the digital gates.

M_1, M_3, M_4, M_7, M_8	$M_2, M_5, M_6, M_9, M_{10}$
3.5 μm/60 nm	0.6 μm/60 nm

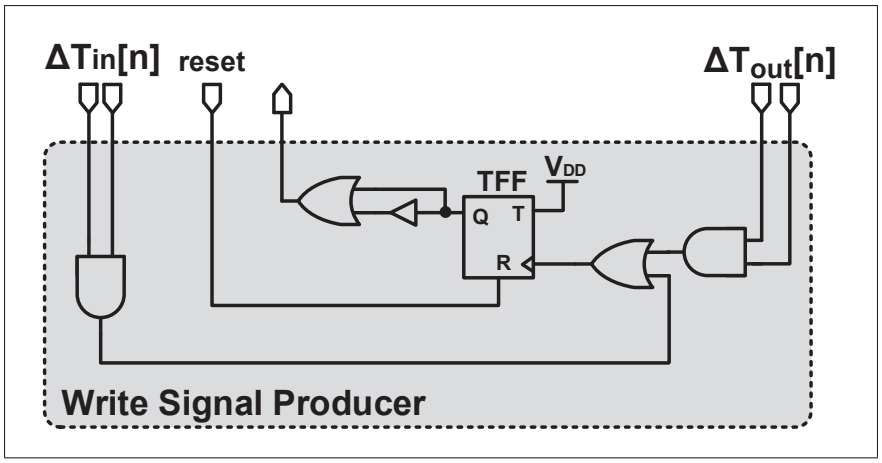


Figure-A I-19 The circuit diagram for the block Write Signal Producer.

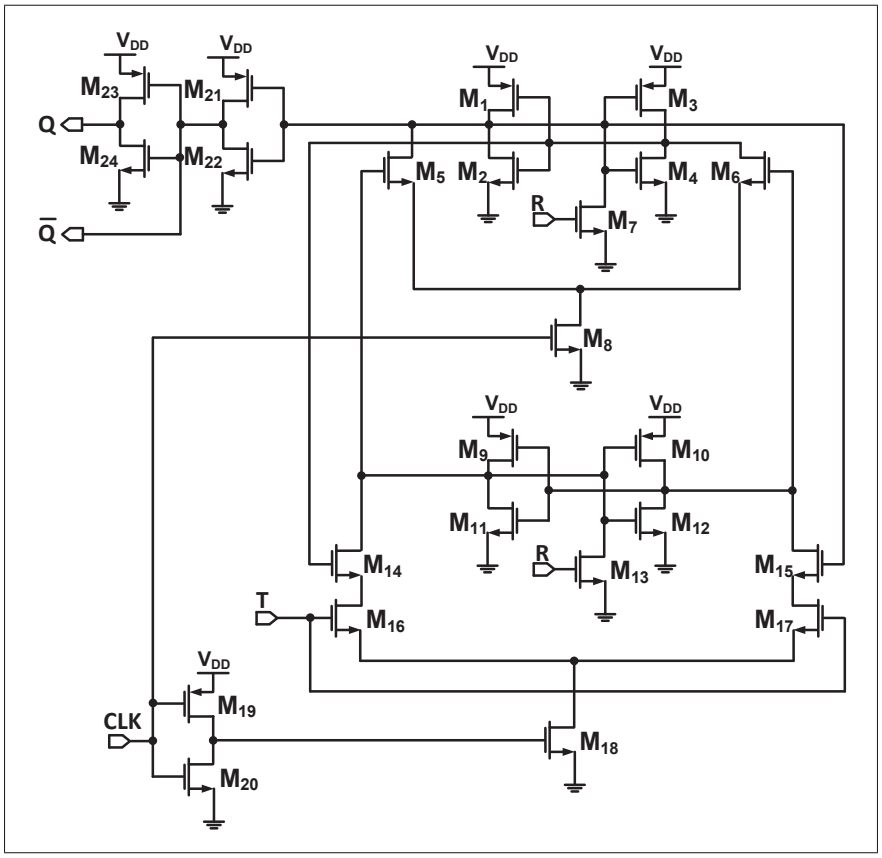


Figure-A I-20 The transistor schematic for the digital TFF used in Figure-A I-19.

Table-A I-14 The transistor dimensions in the schematic of Figure A- I-20

M_1, M_3, M_7, M_9, M_{10}, M_{13}	1 μm/60 nm
M_2, M_4, M_{11}, M_{12}	0.5 μm/60 nm
M_5, M_6, M_8, M_{14}, M_{15}, M_{16}, M_{17}, M_{18}	1.5 μm/60 nm
M_{19}, M_{21}, M_{23}	0.3 μm/60 nm
M_{20}, M_{22}, M_{24}	0.21 μm/60 nm

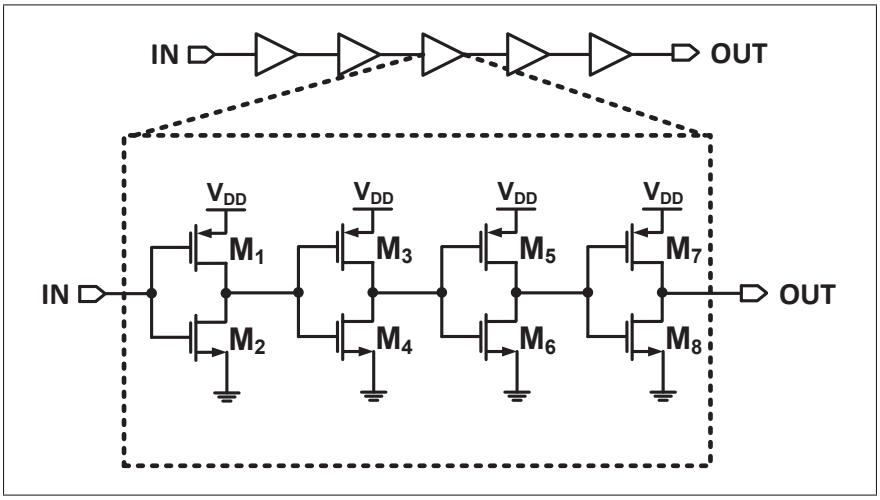


Figure-A I-21 The transistor schematic for the digital buffer used in Figure 4.10.

Table-A I-15 The transistor dimensions in the schematic of Figure A- I-21

M_1, M_3	M_2, M_4, M_6	M_5
1.44 μm/0.48 μm	0.72 μm/0.72 μm	1.44 μm/0.72 μm
M_7	M_8	
1.44 μm/0.36 μm	0.72 μm/0.36 μm	

BIBLIOGRAPHY

Abdelfattah M. and Roberts G. W. (2017). All-Digital Time-Mode Direct-Form All-Pole Biquadratic Filter Realization. *IEEE Transactions on Circuits and Systems II: Express Briefs*, 64(11), 1262-1266. doi: 10.1109/TCSII.2016.2636327.

Abidi, A. A. (2006). Phase Noise and Jitter in CMOS Ring Oscillators. *IEEE J. of Solid-State Circuits,*, 41(8), 1803-1816. doi: 10.1109/JSSC.2006.876206.

Ali-Bakhshian M. and Roberts G.W. (2012). A Digital Implementation of a Dual-Path Time-to-Time Integrator. *IEEE Trans. on Circuits and Syst. I: Regular Papers,*, 59(11), 2578-2591. doi: 10.1109/TCSI.2012.2190669.

Avivi R., Kerner M., Shumaker E., Puma G. L., Sela T., Sofer L., and Horovitz G. (2017). Adaptive Spur Cancellation Technique in All-Digital Phase-Locked Loops. *IEEE Trans. on Circuits and Syst. II: Express Briefs*, 64(11), 1292-1296. doi: 10.1109/TCSII.2017.2650782.

Baird R. T. and Fiez T. S. (1994). Stability analysis of high-order delta-sigma modulation for ADC's. *IEEE Transactions on Circuits and Systems II: Analog and Digital Signal Processing*, 41(1), 59-62. doi: 10.1109/82.275660.

Baker, R.J. (2011). *CMOS: Circuit Design, Layout, and Simulation*. Wiley. Consulted at https://books.google.ca/books?id=kxYhNrOKuJQC.

Cao Y. , De Cock W., Steyaert M. , and Leroux P. (2012). 1-1-1 MASH $\Delta\Sigma$ Time-to-Digital Converters With 6 ps Resolution and Third-Order Noise-Shaping. *IEEE J. of Solid-State Circuits*, 47(9), 2093-2106. doi: 10.1109/JSSC.2012.2199530.

Chan A. H. and Roberts G. W. (2002). A deep sub-micron timing measurement circuit using a single-stage Vernier delay line. *Proceedings of the IEEE 2002 Custom Integrated Circuits Conference*, pp. 77-80. doi: 10.1109/CICC.2002.1012770.

Chan A. H. and Roberts G. W. (2004). A jitter characterization system using a component-invariant Vernier delay line. *IEEE Transactions on Very Large Scale Integration (VLSI) Systems*, 12(1), 79-95. doi: 10.1109/TVLSI.2003.820531.

Chen C. C., Lin S. H., and Hwang C. S. (2014). An Area-Efficient CMOS Time-to-Digital Converter Based on a Pulse-Shrinking Scheme. *IEEE Transactions on Circuits and Systems II: Express Briefs*, 61(3), 163-167. doi: 10.1109/TCSII.2013.2296192.

Chen H., Zhang Y., and Li D. D. U. (2017). A Low Nonlinearity, Missing-Code Free Time-to-Digital Converter Based on 28-nm FPGAs With Embedded Bin-Width Calibrations. *IEEE Trans. on Instrumentation and Measurement*, 66(7), 1912-1921. doi: 10.1109/TIM.2017.2663498.

Chen P., Liu S., and Wu J. (2000). A CMOS Pulse-Shrinking Delay Element For Time Interval Measurement. *IEEE Trans. on Circuits and Syst. II: Analog and Digital Signal Processing*, 47(9), 954-958. doi: 10.1109/82.868466.

Chung S. H., Hwang K. D., Lee W. Y., and Kim L. S. (2010, May). A high resolution metastability-independent two-step gated ring oscillator TDC with enhanced noise shaping. *Proceedings of 2010 IEEE International Symposium on Circuits and Systems*, pp. 1300-1303. doi: 10.1109/ISCAS.2010.5537261.

Colodro F. and Torralba A. (2014). Linearity Enhancement of VCO-Based Quantizers for SD Modulators by Means of a Tracking Loop. *IEEE Transactions on Circuits and Systems II: Express Briefs*, 61(6), 383-387.

Daniels J. , Dehaene W., and Steyaert M. (2010, May). All-digital differential VCO-based A/D conversion. *Proceedings of 2010 IEEE International Symposium on Circuits and Systems*, pp. 1085-1088. doi: 10.1109/ISCAS.2010.5537342.

Daniels J., Dehaene W., Steyaert M. S. J., and Wiesbauer A. (2010). A/D Conversion Using Asynchronous Delta-Sigma Modulation and Time-to-Digital Conversion. *IEEE Trans. on Circuits and Syst. I: Regular Papers*, 57(9), 2404-2412. doi: 10.1109/TCSI.2010.2043169.

Dehlaghi B., Magierowski S., and Belostotski L. (2011). Highly-linear time-difference amplifier with low sensitivity to process variations. *Electronics Letters*, 47(13), 743-745. doi: 10.1049/el.2011.1279.

Deschamps J.P., Sutter G.D., and Canto E. (2012). *Guide to FPGA Implementation of Arithmetic Functions*. Springer Netherlands. Consulted at https://books.google.ca/books?id=IhDMoFtigvAC.

Elshazly A., Rao S., Young B., and Hanumolu P. K. (2014). A Noise-Shaping Time-to-Digital Converter Using Switched-Ring Oscillators-Analysis, Design, and Measurement Techniques. *IEEE J. of Solid-State Circuits*, 49(5), 1184-1197.

Figueiredo M. and Aguiar Rui L. (2012). A dynamic jitter model to evaluate uncertainty trends with technology scaling. *Integration, the VLSI Journal*, 45(2), 162 - 171. doi: https://doi.org/10.1016/j.vlsi.2011.11.002.

Gande M., Maghari N., Oh T., and Moon U. K. (2012, June). A 71dB Dynamic Range Third-Order ΔΣ TDC Using Charge-Pump. *2012 Symposium on VLSI Circuits (VLSIC)*, pp. 168-169.

Gerfers F. and Ortmanns M. (2006). *Continuous-Time Sigma-Delta A/D Conversion: Fundamentals, Performance Limits and Robust Implementations*. Springer Berlin Heidelberg. Consulted at https://books.google.ca/books?id=_M_gFcpH1eUC.

Guttman M. M. and Roberts G. W. (2009, May). Sampled-data IIR filtering using time-mode signal processing circuits. *IEEE International Symposium on Circuits and Systems*, pp. 2285-2288. doi: 10.1109/ISCAS.2009.5118255.

Haurie X. and Roberts G. W. (1995, Aug). A Multiplier-Free Structure for 1-Bit High-Order Digital Delta-Digma Modulators. *38th Midwest Symposium on Circuits and Systems. Proceedings*, 2, 889-892 vol.2. doi: 10.1109/MWSCAS.1995.510232.

Helal B. M., Straayer M. Z., Wei G. Y., and Perrott M. H. (2007, June). A Low Jitter 1.6 GHz Multiplying DLL Utilizing a Scrambling Time-to-Digital Converter and Digital Correlation. *2007 IEEE Symposium on VLSI Circuits*, pp. 166-167. doi: 10.1109/VLSIC.2007.4342700.

Heo M., Kwon v, and Lee M. (2014). Low-power programmable high-gain time difference amplifier with regeneration time control. *Electronics Letters*, 50(16), 1129-1131. doi: 10.1049/el.2014.1782.

Hesener M., Eicher T., Hanneberg A., Herbison D., Kuttner F., and Wenske H. (2007, 11-15 Feb). A 14b 40MS/s Redundant SAR ADC with 480MHz Clock in 0.13 μm CMOS. *2007 IEEE Int. Solid-State Circuits Conf. Digest of Technical Papers*, pp. 248-600. doi: 10.1109/ISSCC.2007.373387.

Homayoun A. and Razavi B. (2013). Analysis of Phase Noise in Phase/Frequency Detectors. *IEEE Trans. on Circuits and Syst. I: Regular Papers*, 60(3), 529-539. doi: 10.1109/TCSI.2012.2215792.

Hsu C. M., Straayer M. Z., and Perrott M. H. (2008). A Low-Noise Wide-BW 3.6-GHz Digital Delta-Sigma Fractional-N Frequency Synthesizer With a Noise-Shaping Time-to-Digital Converter and Quantization Noise Cancellation. *IEEE J. of Solid-State Circuits*, 43(12), 2776-2786.

Iwata A., Sakimura N., Nagata M., and Morie T. (1999). The architecture of delta sigma analog-to-digital converters using a voltage-controlled oscillator as a multibit quantizer. *IEEE Transactions on Circuits and Systems II: Analog and Digital Signal Processing*, 46(7), 941-945. doi: 10.1109/82.775391.

Jansson J. P., Mantyniemi A., and Kostamovaara J. (2009). Synchronization in a Multilevel CMOS Time-to-Digital Converter. *IEEE Trans. on Circuits and Syst. I: Regular Papers*, 56(8), 1622-1634. doi: 10.1109/TCSI.2008.2010111.

Johns D.A. and Martin K. (2008). *Analog Integrated Circuit Design*. Wiley India Pvt. Limited. Consulted at https://books.google.ca/books?id=6-8j7ycydtcC.

Kim J. and Cho S. (2006, May). A time-based analog-to-digital converter using a multi-phase voltage controlled oscillator. *2006 IEEE International Symposium on Circuits and Systems*, pp. 4 pp.-3937. doi: 10.1109/ISCAS.2006.1693489.

Kim J., Jang T., Yoon Y., and Cho S. (2010). Analysis and Design of Voltage-Controlled Oscillator Based Analog-to-Digital Converter. *IEEE Trans. on Circuits and Syst. I: Regular Papers,*, 57(1), 18-30. doi: 10.1109/TCSI.2009.2018928.

Kim K.,Kim Y. H., Y. W. & S., C. (2013). A 7 bit, 3.75 ps Resolution Two-Step Time-to-Digital Converter in 65 nm CMOS Using Pulse-Train Time Amplifier. *IEEE J. of Solid-State Circuits*, 48(4), 1009-1017. doi: 10.1109/JSSC.2013.2237996.

Kim Y. and Kim T. W. . (2014). An 11 b 7 ps Resolution Two-Step Time-to-Digital Converter With 3-D Vernier Space. *IEEE Transactions on Circuits and Systems I: Regular Papers*, 61(8), 2326-2336. doi: 10.1109/TCSI.2014.2304656.

Kozak M. and Kale I. (2007). *Oversampled Delta-Sigma Modulators: Analysis, Applications and Novel Topologies*. Springer US. Consulted at https://books.google.ca/books?id=lJQRBwAAQBAJ.

Kwon H. J., Lee J. S., Kim B., Sim J. Y., and Park H. J. (2014). Analysis of an Open-Loop Time Amplifier With a Time Gain Determined by the Ratio of Bias Current. *IEEE Transactions on Circuits and Systems II: Express Briefs*, 61(7), 481-485. doi: 10.1109/TCSII.2014.2328800.

Lauritzen K. C., Talisa S. H., and Peckerar M. (2010). Impact of Decorrelation Techniques on Sampling Noise in Radio-Frequency Applications. *IEEE Transactions on Instrumentation and Measurement*, 59(9), 2272-2279. doi: 10.1109/TIM.2009.2036344.

Le B., Rondeau T. W., Reed J. H., and Bostian C. W. (2005). Analog-to-digital converters. *IEEE Signal Processing Magazine*, 22(6), 69-77. doi: 10.1109/MSP.2005.1550190.

Lee, B. G. (2015). Power and Bandwidth Scalable 10-b 30-MS/s SAR ADC. *IEEE Trans. on Very Large Scale Integration (VLSI) Systems*, 23(6), 1103-1110. doi: 10.1109/TVLSI.2014.2331354.

Lee I., Han G., and Chae Y. (2015). A 2 mW, 50 dB DR, 10 MHz BW 5 *times* Interleaved Bandpass Delta-Sigma Modulator at 50 MHz IF. *IEEE Trans. on Circuits and Syst. I: Regular Papers*, 62(1), 80-89. doi: 10.1109/TCSI.2014.2347234.

Lee S. K., Seo Y. H., Suh Y., Park H. J., and Sim J. Y. (2010, Feb). A 1GHz ADPLL with a 1.25ps minimum-resolution sub-exponent TDC in 0.18 μm CMOS. *2010 IEEE International Solid-State Circuits Conference - (ISSCC)*, pp. 482-483. doi: 10.1109/ISSCC.2010.5433837.

Lee S., Kim B., and Lee K. (1997). A novel high-speed ring oscillator for multiphase clock generation using negative skewed delay scheme. *IEEE Journal of Solid-State Circuits*, 32(2), 289-291. doi: 10.1109/4.551926.

Li, M.P. (2007). *Jitter, Noise, and Signal Integrity at High-Speed*. Pearson Education. Consulted at https://books.google.ca/books?id=vmBJYOOFSwYC.

Lin Y. and Ismail M. (2012). Time-Based All-Digital Sigma-Delta Modulators For Nanometer Low Voltage CMOS Data Converters. *Analog Integrated Circuits and Signal Processing*, 73(3), 801-808. doi: 10.1007/s10470-012-9901-0.

Lindfors S., Lansirinne M., Lindeman T., and Halonen K. (1999, Jul). On the design of 2nd order multi-bit Delta-Sigma modulators. *Circuits and Systems, 1999. ISCAS '99. Proceedings of the 1999 IEEE International Symposium on*, 2, 13-16 vol.2. doi: 10.1109/ISCAS.1999.780474.

Liu C. and McNeill J. A. (2004, May). Jitter in oscillators with 1/f noise sources. *IEEE Int. Symp. on Circuits and Systems*, 1, I-773-6 Vol.1. doi: 10.1109/ISCAS.2004.1328309.

Lota J., Al-Janabi M., and Kale I. (2014). Nonlinear Stability Prediction of Multibit Delt-Sigma Modulators for Sinusoidal Inputs. *IEEE Transactions on Instrumentation and Measurement*, 63(1), 18-26. doi: 10.1109/TIM.2013.2273597.

Lu P., Liscidini A., and Andreani P. (2012). A 3.6 mW, 90 nm CMOS Gated-Vernier Time-to-Digital Converter With an Equivalent Resolution of 3.2 ps. *IEEE Journal of Solid-State Circuits*, 47(7), 1626-1635. doi: 10.1109/JSSC.2012.2191676.

Luschas S. and Lee H. S. (2002). High-speed Sigma; Delta; modulators with reduced timing jitter sensitivity. *IEEE Transactions on Circuits and Systems II: Analog and Digital Signal Processing*, 49(11), 712-720. doi: 10.1109/TCSII.2002.807575.

Lyu Y., Feng J., Ye H., and Yu D. (2017). All-digital synchronous 2 $\times$ time-difference amplifier based on time register. *Electronics Letters*, 53(16), 1102-1104. doi: 10.1049/el.2017.1771.

Macii D., Pianegiani F., Carbone P., and Petri D. (2006). A stability criterion for high-accuracy Delta-Sigma digital resonators. *IEEE Transactions on Instrumentation and Measurement*, 55(2), 577-583. doi: 10.1109/TIM.2006.870118.

Macpherson, A. R. (2013). *A Time-Based 5GS/s CMOS Analog-to-Digital Converter*. PhD thesis, University of Calgary. doi: http://dx.doi.org/10.5072/PRISM/25056.

Manganaro G. and Leenaerts D. (2013). *Advances in Analog and RF IC Design for Wireless Communication Systems*. Elsevier Science. Consulted at https://books.google.ca/books?id=Skl2DAAAQBAJ.

Matsumoto A., Sakiyama S., Tokunaga Y., Morie T., and Dosho S. (2008). A Design Method and Developments of a Low-Power and High-Resolution Multiphase Generation System. *IEEE Journal of Solid-State Circuits*, 43(4), 831-843. doi: 10.1109/JSSC.2008.917567.

Mohan S. S., Chan W. S., Colleran D. M., Greenwood S. F., Gamble J. E., and Kouznetsov I. G. (2005, Sept). Differential ring oscillators with multipath delay stages. *Proceedings of the IEEE 2005 Custom Integrated Circuits Conference, 2005*, pp. 503-506. doi: 10.1109/CICC.2005.1568716.

Naraghi S., Courcy M., and Flynn M. P. (2010). A 9-bit, 14 μW and 0.06 mm^2 Pulse Position Modulation ADC in 90 nm Digital CMOS. *IEEE J. of Solid-State Circuits*, 45(9), 1870-1880.

Ninh H. P., Miyahara M. , and Matsuzawa A. (2011, Nov). A 83-dB SFDR 10-MHz bandwidth continuous-time Delta-Sigma modulator employing a one-element-shifting dynamic element matching. *2011 IEEE International Symposium on Radio-Frequency Integration Technology*, pp. 109-112. doi: 10.1109/RFIT.2011.6141779.

Norsworthy S.R., Schreier R., and Temes G.C. (1997). *Delta-Sigma data converters: theory, design, and simulation*. IEEE Circuit and Systems Society. Consulted at https://books.google.ca/books?id=P2hTAAAAMAAJ.

Nose K., Kajita M., and Mizuno M. (2006). A 1-ps Resolution Jitter-Measurement Macro Using Interpolated Jitter Oversampling. *IEEE J. of Solid-State Circuits*, 41(12), 2911-2920.

Oulmane M. and Roberts G. W. (2004a, May). A CMOS time amplifier for Femtosecond resolution timing measurement. *2004 IEEE International Symposium on Circuits and Systems (IEEE Cat. No.04CH37512)*, 1, I-509-12 Vol.1. doi: 10.1109/ISCAS.2004.1328243.

Oulmane M. and Roberts G. W. (2004b, Oct). Digital domain time amplification in CMOS process. *Proceedings. 7th International Conference on Solid-State and Integrated Circuits Technology, 2004.*, 2, 1416-1420 vol.2. doi: 10.1109/ICSICT.2004.1436837.

Park H., Nam K., Su D. K., Vleugels K., and Wooley B. A. (2009). A 0.7-V 870-μ W Digital-Audio CMOS Sigma-Delta Modulator. *IEEE Journal of Solid-State Circuits*, 44(4), 1078-1088. doi: 10.1109/JSSC.2009.2014708.

Pathan A. and Liscidini A. (2016). Thermal noise limit for time-domain analogue signal processing in CMOS technologies. *Electronics Letters*, 52(18), 1567-1569. doi: 10.1049/el.2016.1908.

Pavan S., Schreier R., and Temes G.C. (2017). *Understanding Delta-Sigma Data Converters*. Wiley. Consulted at https://books.google.ca/books?id=JBauDQAAQBAJ.

Plassche, Rudy J. van de. (2013). *CMOS Integrated Analog-to-Digital and Digital-to-Analog Converters*. Springer US. Consulted at https://books.google.ca/books?id=F7PaBwAAQBAJ.

Razavi B. (2002). *Design of Analog CMOS Integrated Circuits*. Tata McGraw-Hill. Consulted at https://books.google.ca/books?id=ZdXvVEtGrhQC.

Razavi B. and Wooley B. A. (1992). Design techniques for high-speed, high-resolution comparators. *IEEE Journal of Solid-State Circuits*, 27(12), 1916-1926. doi: 10.1109/4.173122.

Reddy K., Rao S., Inti R., Young B., Elshazly A., Talegaonkar M., and Hanumolu P. K. (2012). A 16-mW 78-dB SNDR 10-MHz BW CT Delta-Sigma ADC Using Residue-Cancelling VCO-Based Quantizer. *IEEE Journal of Solid-State Circuits*, 47(12), 2916-2927. doi: 10.1109/JSSC.2012.2218062.

Roberts G. W. and Ali-Bakhshian M. (2010). A Brief Introduction to Time-to-Digital and Digital-to-Time Converters. *IEEE Trans. on Circuits and Syst. II: Express Briefs*, 57(3), 153-157.

Roberts G.W. and Chan A. (2005). Timing measurement device using a component-invariant vernier delay line. *US Patent 6,850,051, McGill University, Montreal, Quebec, Canada,*.

Rosa, Jose M. de la . (2011). Sigma-Delta Modulators: Tutorial Overview, Design Guide, and State-of-the-Art Survey. *IEEE Transactions on Circuits and Systems I: Regular Papers*, 58(1), 1-21. doi: 10.1109/TCSI.2010.2097652.

Salo T. O., Lindfors S. J., Hollman T. M., Jarvinen J. A. M., and Halonen K. A. I. (2003). 80-MHz bandpass Delta-Sigma modulators for multimode digital IF receivers. *IEEE Journal of Solid-State Circuits*, 38(3), 464-474. doi: 10.1109/JSSC.2002.808327.

Si v, Li F., and Zhang C. (2012, April). A 100MHz S/s, 7 bit VCO-based ADC which is used in time interleaved ADC architectures. *2012 2nd International Conference on Consumer Electronics, Communications and Networks (CECNet)*, pp. 4-7. doi: 10.1109/CECNet.2012.6202063.

Straayer M. Z. and Perrott M. H. (2008). A 12-Bit, 10-MHz Bandwidth, Continuous-Time Delta-Sigma ADC With a 5-Bit, 950-MS/s VCO-Based Quantizer. *IEEE Journal of Solid-State Circuits*, 43(4), 805-814. doi: 10.1109/JSSC.2008.917500.

Straayer M.Z. and Perrott M.H. (2009). A Multi-Path Gated Ring Oscillator TDC With First-Order Noise Shaping. *IEEE J. of Solid-State Circuits,*, 44(4), 1089-1098. doi: 10.1109/JSSC.2009.2014709.

Taillefer C.S. and Roberts G.W. (2009). Delta-Sigma A/D Conversion Via Time-Mode Signal Processing. *IEEE Trans. on Circuits and Syst. I: Regular Papers,*, 56(9), 1908-1920. doi: 10.1109/TCSI.2008.2010144.

Tao H., Toth L., and Khoury J. M. (1999). Analysis of timing jitter in bandpass sigma-delta modulators. *IEEE Transactions on Circuits and Systems II: Analog and Digital Signal Processing*, 46(8), 991-1001. doi: 10.1109/82.782040.

Tousi Y. M. and Afshari E. (2011). A Miniature 2 mW 4 bit 1.2 GS/s Delay-Line-Based ADC in 65 nm CMOS. *IEEE Journal of Solid-State Circuits*, 46(10), 2312-2325. doi: 10.1109/JSSC.2011.2162186.

Vercesi L., Liscidini A., and Castello R. (2010). Two-Dimensions Vernier Time-to-Digital Converter. *IEEE J. of Solid-State Circuits*, 45(8), 1504-1512.

Vornicu I., Carmona-Galan R., and Rodriguez-Vazquez A. (2017). Arrayable Voltage-Controlled Ring-Oscillator for Direct Time-of-Flight Image Sensors. *IEEE Trans. on Circuits and Systems I: Regular Papers*, 64(11), 2821-2834. doi: 10.1109/TCSI.2017.2706324.

Weste N. and Harris D. (2011). *CMOS VLSI Design: A Circuits and Systems Perspective*. Pearson Education.

Yoder S., Ismail M., and Khalil W. (2011). *VCO-Based Quantizers Using Frequency-to-Digital and Time-to-Digital Converters*. Springer New York. Consulted at https://books.google.ca/books?id=Z3k7rHhSq2oC.

Young B., Kwon S., Elshazly A., and Hanumolu P. K. (2010, Sept). A 2.4 ps Resolution 2.1 mW Second-Order Noise-Shaped Time-to-Digital Converter With 3.2 ns Range in 1MHz Bandwidth. *IEEE Custom Integrated Circuits Conf. 2010*, pp. 1-4.

Yu J. and Dai F. F. (2010, September). A 3-Dimensional Vernier Ring Time-to-Digital Converter in 0.13 μm CMOS. *IEEE Custom Integrated Circuits Conf. 2010*, pp. 1-4. doi: 10.1109/CICC.2010.5617431.

Yu W., K. K. & S., C. (2014). A 148 fs_{rms} Integrated Noise 4 MHz Bandwidth Second-Order Delta-Sigma Time-to-Digital Converter With Gated Switched-Ring Oscillator. *IEEE Trans. on Circuits and Syst. I: Regular Papers*, 61(8), 2281-2289. doi: 10.1109/TCSI.2014.2321195.

Yu W., Kim J., Kim K., and Cho S. (2013). A Time-Domain High-Order MASH Delta-Sigma ADC Using Voltage-Controlled Gated-Ring Oscillator. *IEEE Trans. on Circuits and Syst. I: Regular Papers,*, 60(4), 856-866. doi: 10.1109/TCSI.2012.2209298.

Yu W., Kim K., and Cho S. (2015). A 0.22 ps_{rms} Integrated Noise 15 MHz Bandwidth Fourth-Order Delta-Sigma Time-to-Digital Converter Using Time-Domain Error-Feedback Filter. *IEEE J. of Solid-State Circuits*, 50(5), 1251-1262.

Yuan, F. (2014). Design Techniques For Time-Mode Noise-Shaping Analog-to-Digital Converters: A State-Of-The-Art Review. *Analog Integrated Circuits and Signal Processing*, 79(2), 191-206. doi: 10.1007/s10470-014-0271-7.

Ziabakhsh S., Gagnon G., and Roberts G. W. (2017, Aug). A Time-Mode LDI-Based Resonator for a Band-Pass $\Delta\Sigma$ TDC. *2017 IEEE 60th Int. Midwest Symposium on Circuits and Systems (MWSCAS)*, pp. 1296-1299. doi: 10.1109/MWSCAS.2017.8053168.

Ziabakhsh S., Gagnon G., and Roberts G. W. (2018). The Peak-SNR Performances of Voltage-Mode versus Time-Mode Circuits: the PMOS-NMOS Stack Use Case. *IEEE Transactions on Circuits and Systems II: Express Briefs*, 1-5. doi: 10.1109/TCSII.2018.2817504.

Ziabakhsh S., Gagnon G., and Roberts G.W. (2015, May). Wide Linear Range Voltage-Controlled Delay Unit For Time-Mode Signal Processing. *IEEE Int. Symp. on Circuits and Systems (ISCAS)*, pp. 1826-1829. doi: 10.1109/ISCAS.2015.7169011.