Designing and developing nine-level Packed U-Cell (PUC9) inverter for high power applications

by

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Conception et développement d'un onduleur PUC9 (Packed U-Cell) à neuf niveaux pour les applications à forte puissance, THESIS M.SC.A.

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RÉSUMÉ

Il est indéniable que la consommation d'énergie a tendance à augmenter et que, pour des raisons économiques et environnementales, l'utilisation des énergies renouvelables tels : éolienne et solaire a augmenté considérablement. A cet effet, des onduleurs sont nécessaires pour convertir l'énergie produite en énergie utilisable par les consommateurs. Bien que les onduleurs existants fonctionnent correctement, les efforts pour réduire les pertes d'énergie dans ces étages de conversion avec une réduction des coûts des composants utilisés constituent un objectif en soi. Compte tenu de ce qui précède, l'onduleur PUC9 pourrait être un choix approprié en raison de sa simplicité, de sa fiabilité et de son efficacité en comparaison avec d'autres onduleurs.

Les objectifs de ce projet sont de réduire la complexité du système de contrôle du PUC9, ce qui permet de produire un convertisseur orienté vers l'industrie et capable d'équilibrer les niveaux des tensions des condensateurs selon les besoins de la charge, aussi d'accroître son efficacité, et finalement de concevoir l'expérimentation nécessaire pour valider ce nouveau concept avec sa commande.

Afin d'atteindre les objectifs de recherche susmentionnés; tout d'abord, je effectué une revue de la littérature sur différents types d'onduleurs, en particulier des onduleurs à source continue, et vérifier la complexité de chaque type d'onduleur étudié en termes de fréquence de commutation, du nombre de composantes utilisées, et le THD. (Distorsion harmonique totale). Ensuite, j'ai passé en revue certaines techniques d'équilibrage des condensateurs. Par après, l'onduleur PUC9 est théoriquement analysé et étudié. Après cela, j'ai appliqué la commande prédictive sur le PUC9. J'ai proposé une technique de modulation adaptée. À cette occasion, j'ai obtenu un modèle mathématique du PUC9, et effectué la simulation utilisant SimPowerSystem et Matlab Simulink. Un prototype expérimental a été développé et a servi pour la validation expérimentale.

Enfin, une nouvelle topologie a été proposée nommée onduleur UX-Cell à neuf niveaux sur laquelle j'ai appliqué un contrôle prédictif et une technique de contrôle sans capteur. Cette nouvelle topologie a été simulée avec Matlab Simulink, et a été validée de manière expérimentale pour ainsi déterminer ses avantages et inconvénients par rapport à l'onduleur PUC9. À cette fin, le travail au laboratoire a permis la conception des circuits imprimés des onduleurs PUC9 et UX-Cell avec le logiciel Altium Design et de tester les deux brevets de manière expérimentale en mode autonome et en mode connecté au réseau électrique.

Mots-clés: PUC9**,** UX-Cell, Onduleur compact à neuf cellules en U, technique de commande MPC, équilibrage des tensions des condensateurs, états de commutation, onduleur à plusieurs niveaux de tension.

Designing and developing nine-level Packed U-Cell (PUC9) inverter for high power applications, THESIS M.SC.A

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ABSTRACT

It is a fact that energy consumption has had an increasing trend, and due to economic reasons and environmental concerns, the usage of renewable energies like wind and solar is increasing drastically. Inverters are needed in order to change the produced energy into usable energy for consumers. Although the existing inverters work properly, factories and countries always tend to decrease energy loss and the cost of the components used in producing and transferring energy. Considering the aforementioned issues, PUC9 inverter could be a suitable choice due to its simplicity, reliability and efficiency and also needing low weight transformers in comparison with other inverters.

The main objectives of this project are reducing the complexity of PUC9 control system, as a result producing an industry-oriented converter, which balances the dc capacitor level as desired, increasing the efficiency of PUC9 inverter, and designing an inverter compatible with adding series inverter together to decrease complexity.

In order to achieve the above mentioned research objectives; first, I do literature review on different types of inverters, especially single dc sources inverters, and check out the design the complexity of each type of reviewed inverter in terms of switching state possibility, the number of their components, advantages and disadvantages, and THD (Total Harmonic Distortion). Afterward, I review some modulation and voltage balancing techniques. Then, PUC9 inverter is theoretically analyzed. After that, I apply model predictive control on PUC9; in addition, I propose one modulation technique on it. On that occasion, I obtain mathematical model of PUC9, simulate it with SimPowerSystem and Matlab Simulink, and validate them experimentally. Finally, I offer nine-level UX-Cell inverter, apply model predictive control and sensorless control technique, simulate it with Matlab Simulink, validate it experimentally, and consider its pros and cons in comparison with PUC9 inverter. For this purpose, I design the PCB of PUC9 and UX-Cell inverter with Altium Design software and test both patents experimentally in stand-alone and grid-connected modes.

Keywords: Nine-Level Packed U-Cell Inverter, MPC Technique, Capacitors Voltage Balancing, Switching States Possibility, Multilevel Inverters, Total Harmonic Distortion**,** Power Quality, Renewable Energy Conversion.

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LIST OF ABREVIATIONS

AC	Alternative Current
AF	Active filter
AH-MLI	Asymmetric hybrid multilevel inverters
AOD-LS-PWM	Alternate Opposition-Disposition Level-Shifted Pulse Width Modulation
APF	Active power filter
APOD	Alternative Phase Opposite Disposition
CHB	Cascaded H-Bridge
DC	Direct Current
EV	Electrical vehicle
FB	Full Bridge
FC	Flying Capacitor
HB	Half Bridge
IEEE	Institute of Electrical and Electronics Engineering
IGBT	Insulated gate bipolar transistor
KCL	Kirchhoff's Current Law
KVL	Kirchhoff's Voltage Law
LS-PWM	Level Shifted Pulse Width Modulation
MLI	Multi-Level Inverter
NPC	Neutral Point Clamped
OD-LS-PWM	Opposition-Disposition Level-Shifted Pulse Width Modulation
PCC	Point of common coupling
PD-LS-PWM	Phase Disposition Level Shifted Pulse Width Modulation
PF	Power Factor
PFC	Power Factor Correction
PI	Proportional Integral
PID	Proportional Integral derivative
PLL	Phase Locked Loop
PS-PWM	Phase shifted Pulse Width Modulation
PUC5	5-Level Packed U-Cell

PUC7	7-Level Packed U-Cell
PUC9	9-Level Packed U-Cell
PV	Photovoltaic
PWM	Pulse Width Modulation
RMS	Root Mean Square
SPS	SimPowerSystem
SVM	Space Vector Modulation
THD	Total Harmonic Distortion
UPS	Uninterruptable power supplies
VSC	Voltage source converter
VSI	Voltage source inverter

INTRODUCTION

Due to rising concerns about the emission of greenhouse gases resulting from burning fossil fuels, which are expensive, air pollutant, and non-renewable sources, the usage of renewable energy sources is increasing in the world. As a result, countries invest more in such energy sources such as solar, wind, and hydroelectric power, etc. For injecting the generated electricity from solar panels, and new generation of wind and hydro turbines, we need inverters; however, conventional inverters, which are normally 2 or 3-levels converters, generate and inject negative harmonics into the grid. These adverse harmonics have negative effect on voltage and current of distributed networks and electric machines. Consequently, researchers focused more on reducing such harmful harmonics, especially after imposing harmonic restriction standards such as EN61000-3-2 and IEC 1000-3-2 recommended by IEEE (2004) and IEC (2005) in order (Grégoire, Al-Haddad, & Ounejjar, 2009; Ounejjar & Al-Haddad, 2008, 2009; Ounejjar, Al-Haddad, & Gregoire, 2011). Firstly, researches paid attention to developing active and passive filters in order to decrease negative harmonics that inverters produce. These days, researchers focus more on designing multilevel inverters, particularly single dc source multilevel inverters for increasing the efficiency and decreasing the fabrication and installation costs. There are different multilevel topologies; each topology has its own pros and cons. Among these patents, Packed U-Cell (PUC), planned by Ounejjar and Al-Haddad in 2008, is a promising topology, known as a highly efficient and low-cost inverter with the least number of switches in comparison with other multilevel inverters. On the other hand, it has problems such as capacitors' voltage balancing, the current limitation drawn from the voltage source, requiring more DC sources in three-phase setup, etc. Reducing the complexity and weakness of high efficiency multilevel converters like PUC can convince industry to utilize them more. In this work, I tried to decrease the complexity of PUC9 and then prove these techniques with Matlab Simulink and validate them experimentally.

CHAPTER 1

MULTILEVEL CONVERTER LITERATURE REVIEW

1.1 Introduction

The single dc source multilevel inverter topologies are dominant technologies in home and industrial applications due to high efficiency, high-power quality, and minimum manufacturing cost. They require many calculations for generating switching signals and more sensors compared to conventional inverters. Nowadays, by increasing the speed of microcontrollers, and decreasing the cost of high-speed microcontrollers and voltage/current sensors, the control of multilevel inverters is cheaper and easier. In this chapter, different topologies of single DC source multilevel inverters are reviewed. Some different structures of existing single DC source multilevel inverters are investigated in terms of switching state possibility, the number of their components, advantages and disadvantages, and THD (Total Harmonic Distortion). To this end, the conventional multilevel inverter topologies including NPC, FC and CHB are taken into consideration because they are the fundamental multilevel structures. Afterward, some recently introduced single dc source multilevel inverters' topologies are deeply surveyed. Then, PUC topology is considered. After that, some modulation and voltage balancing technique are briefly reviewed.

1.2 Multi-level Cascaded Topologies

1.2.1 Half-Bridge Inverter

Figure 1.1 shows half-bridge voltage-source inverter circuit, which consists of two identical capacitors: one ground between these capacitors, and one DC source (Batarseh & Harb, 2018; Koshti & Rao, 2017). These capacitors act as two identical DC sources with the value of $\frac{V_{dc}}{2}$ to make the output positive and negative. Table 1.1 illustrates switching states' possibility of half-bridge voltage source inverter.

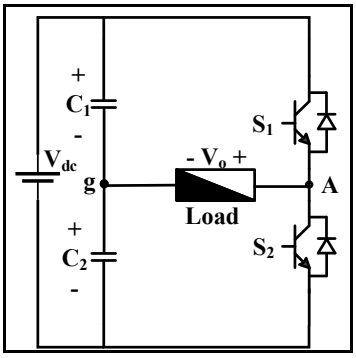


Figure 1.1 Half-bridge voltage source inverter

Table 1.1 Switching state possibility of half-bridge inverter

States	S_1	S_2	V_o
1	0	0	Open Circuit
2	0	1	$\frac{-V_{dc}}{2}$
3	1	0	$\frac{+V_{dc}}{2}$
4	1	1	Short Circuit

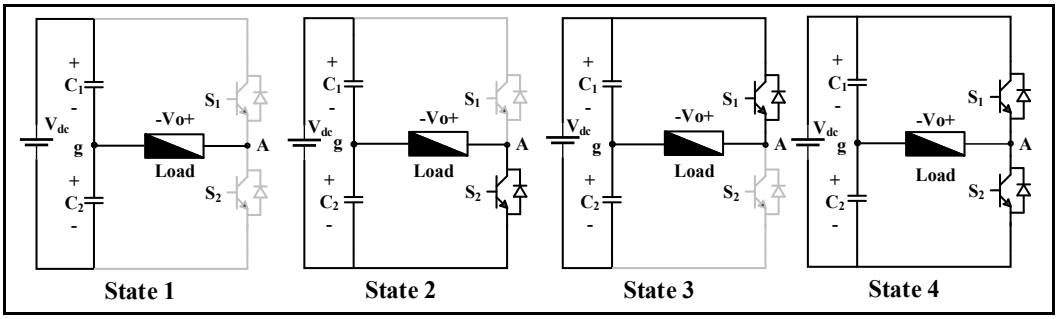


Figure 1.2 Equivalent circuit of half-bridge inverter in each switching state

Due to having two switches, there are four possible switching states as shown in Table.1.1 In the first state, both switches are OFF, as seen in Figure 1.2; this state is not suitable for the operation of inverter because the current should keep going through the load. In the second state, switch one is OFF and switch two is ON, with a simple KVL in the lower loop, it is

obtained that V_o is equal to$\frac{-V_{dc}}{2}$. In the third state, switch one is ON and switch two is OFF and with KVL in upper loop; it is obtained that V_o is equal to$\frac{+V_{dc}}{2}$. In the final state, both switches are ON, in this state, the current is shot through voltage source, and again no current passes through the load; therefore, it is not the appropriate state for the operation of the inverter. As a result, only two operational states for this inverter exist (states 2 and 3). It can be clearly seen that the output of half-bridge inverter has only two levels ($\frac{-V_{dc}}{2}$ and$\frac{+V_{dc}}{2}$); however, if the switches are controlled with PWM (Pulse Width Modulation), the output of the inverter looks like any voltages between $\frac{-V_{dc}}{2}$ and$\frac{+V_{dc}}{2}$.

1.2.2 Full-Bridge Inverter

Figure 1.3 shows full-bridge or H-bridge multilevel voltage-source inverter configuration (Batarseh & Harb, 2018; Koshti & Rao, 2017). Due to having four different switches in this topology, eight switching state possibilities exist, and yet in order to prevent KCL violation and shoot through, vertical switches are complimentary. It means that S_1 and S_4 cannot be ON or OFF at the same time; likewise, S_3 and S_2 cannot be ON or OFF at the same time, hence there are only four operational switching states, as shown in Table 1.2. Figure 1.4 indicates equivalent circuit for each state.

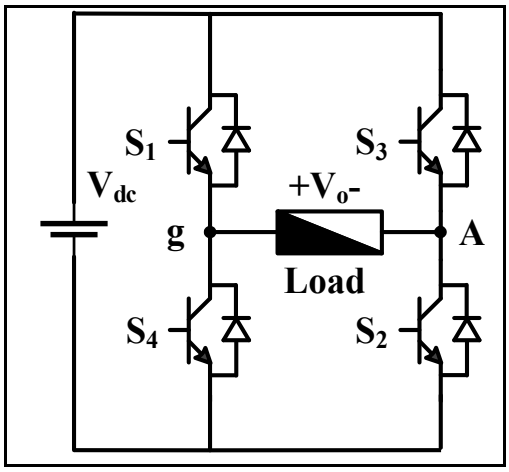


Figure 1.3 Full-bridge voltage source inverter

Table 1.2 Switching states of full-bridge inverter

States	S_1	S_2	S_3	S_4	V_o
1	1	1	0	0	V_{dc}
2	1	0	1	0	0
3	0	0	1	1	$-V_{dc}$
4	0	1	0	1	0

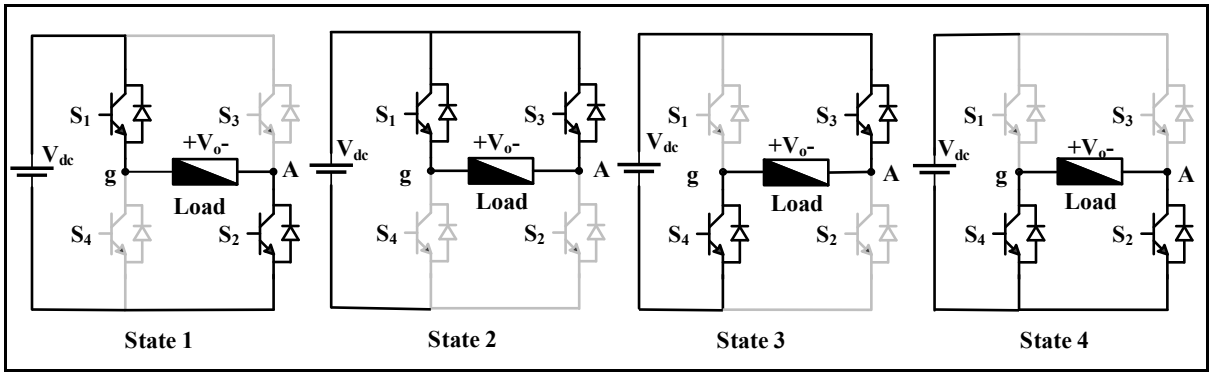


Figure 1.4 Equivalent circuit of H-bridge inverter in each switching state

1.2.3 Three-Phase Six Switches Voltage Source Inverter

Figure 1.5 shows three-phase full-bridge inverter with two capacitors as voltage sources and wye connected load (Batarseh & Harb, 2018; Koshti & Rao, 2017). As can be seen, this inverter is made by connecting three half-bridge inverters in parallel. The sequence of pulses summation at any time for S_1-S_6 should be zero in order to have balance line-to-line output voltage. In this regard, the conduction angle is equal to$\frac{\pi}{2}$.

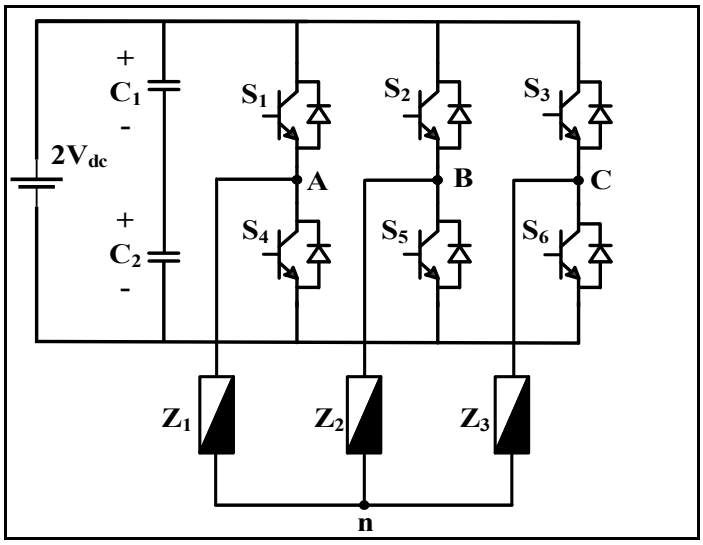


Figure 1.5 Three-phase full-bridge inverter

Table 1.3 illustrates switching states of S_1-S_6 for a three-phase full bridge inverter. It should be mentioned that in order to avoid short circuit in power supply, vertical switches are complimentary. It means that S1, S4 and S_3, S_6 and S_5, S_2 switches cannot be ON or OFF at the same time. It can be seen that this inverter produces three levels of voltage in each phase. Due to having balanced output voltages, the switches must switch in a way that the voltages V_a, V_b, V_c have $\frac{2\pi}{3}$phase difference.

Table 1.3 Switching states of three-phase full-bridge inverter

States	S_1	S_2	S_3	V_{an}	V_{bn}	V_{cn}	V_{ab}	V_{bc}	V_{ca}
1	0	0	0	$-V_{dc}$	$-V_{dc}$	$-V_{dc}$	0	0	0
2	0	0	1	$-V_{dc}$	$-V_{dc}$	$+V_{dc}$	0	$-2V_{dc}$	$+2V_{dc}$
3	0	1	0	$-V_{dc}$	$+V_{dc}$	$-V_{dc}$	$-2V_{dc}$	$+2V_{dc}$	0
4	0	1	1	$-V_{dc}$	$+V_{dc}$	$+V_{dc}$	$-2V_{dc}$	0	$+2V_{dc}$
5	1	0	0	$+V_{dc}$	$-V_{dc}$	$-V_{dc}$	$+2V_{dc}$	0	$-2V_{dc}$
6	1	0	1	$+V_{dc}$	$-V_{dc}$	$+V_{dc}$	$+2V_{dc}$	$-2V_{dc}$	0
7	1	1	0	$+V_{dc}$	$+V_{dc}$	$-V_{dc}$	0	$+2V_{dc}$	$-2V_{dc}$
8	1	1	1	$+V_{dc}$	$+V_{dc}$	$+V_{dc}$	0	0	0

1.2.4 Cascaded H-Bridge (CHB) Inverter

CHB is normally used for producing more than three levels of voltage at the inverter output (Gaikwad & Arbune, 2016; Koshti & Rao, 2017). This inverter, which is created by connecting a number of H-bridge inverters in series, is one of the popular inverters in industry due to its simplicity and basic technology. Each H-bridge has a separate DC source and produces two levels of voltage. Figure 1.6 shows the single phase five-level CHB MLI. The output voltage of this inverter is equal to the summation of output voltages of H-bridge cells together. Considering the 0-voltage, n number of H-bridge cells could produce (2n+1) levels of voltage at the output of this inverter and an n-level CHB inverter needs 2(n-1) switches.

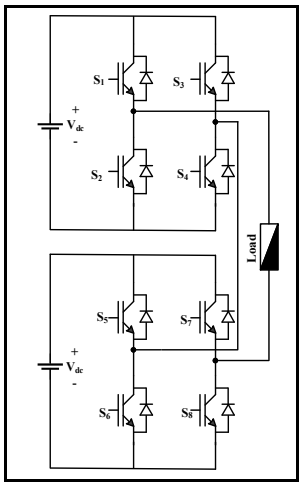


Figure 1.6 Single-phase five-level CHB MLI

Figure 1.7 (a) illustrates the main circuit and Table 1.4 shows the switching states of single phase five-level CHB inverter. As known form H-bridge topology, in each H-bridge cell, vertical switches are complimentary. Besides, the output of each H-bridge cell could be V_{dc}, 0, -V_{dc}. Furthermore, single phase five-level CHB MLI has two H-bridge Cells. Considering the given information, it can be said that five voltage levels at the output of this inverter are ($2V_{dc}$,V_{dc}, $0, -V_{dc}$, $-2V_{dc}$). As can be seen in Table 1.4, there are six switching states; in addition, for feeding switches, four signal pairs have to be generated for single phase five-level CHB inverter.

By connecting three single-phase CHB inverters in parallel, the three-phase CHB inverter would be produced. For generating three phases in this topology, 6-voltage sources and twelve pairs of switching signals for feeding 24 switches are needed. (See Figure 1.7 (b))

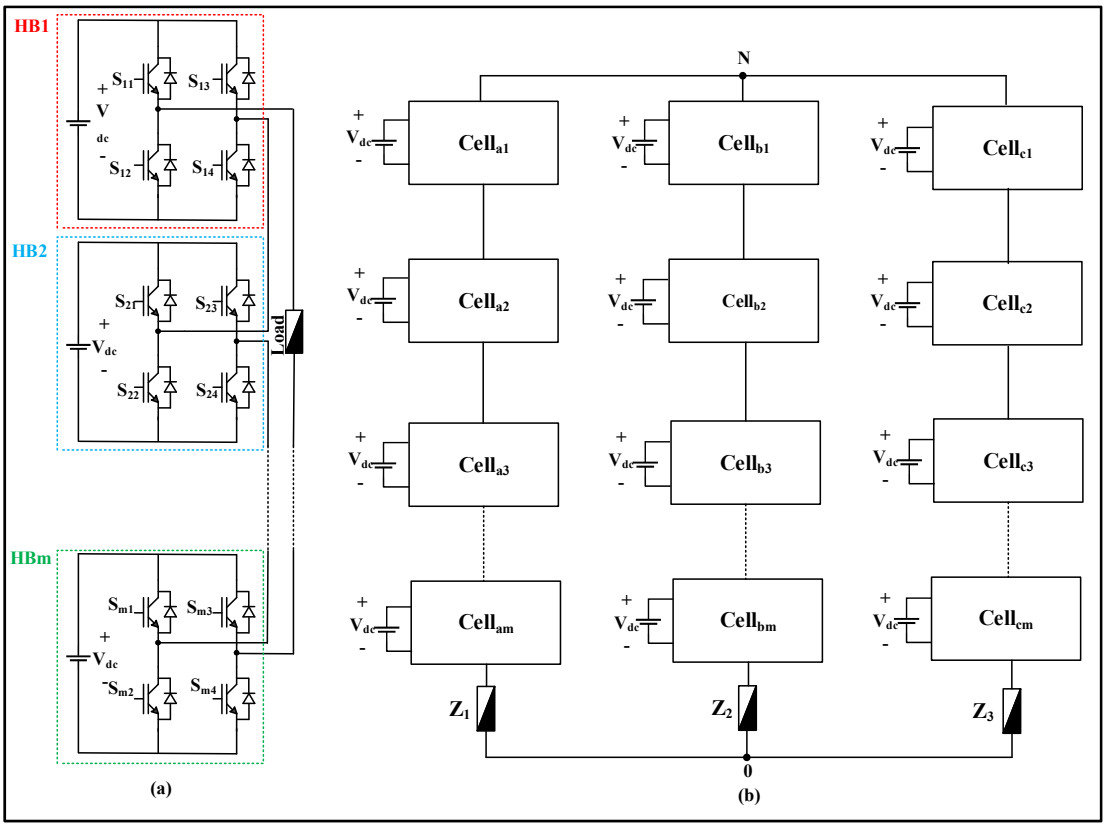


Figure 1.7 General Structure of CHB MLI (a) single-phase (b) three-phase

Table 1.4 Switching states of single-phase five-level CHB MLI

States	S_1	S_2	S_3	S_4	S_5	S_6	S_7	S_8	V_o
1	1	0	1	0	1	0	1	0	0
2	1	0	1	0	1	0	0	1	V_{dc}
3	1	0	0	1	1	0	0	1	$2V_{dc}$
4	0	1	0	1	0	1	1	0	$-V_{dc}$
5	0	1	0	1	0	1	0	1	0
6	0	1	1	0	0	1	1	0	$-2V_{dc}$

Advantages and disadvantages of five-level CHB Inverter are outlined as follows:

Advantages:

- It does not need any capacitor or diode for clamping.
- In comparison with NPC and FC inverter, it needs fewer components; therefore, its price is less than the two former types.
- By increasing the number of levels, its output is like sinusoidal waveform even without a filter.
- It is suitable for high-power, medium-power and low-power applications of renewable energies.

Disadvantages:

- It needs Isolated DC source for each stage.
- The number of PF levels is limited because of voltage unbalancing problems, packaging constraints and circuit layout.

1.2.5 Modular Multilevel Converter (MMC)

Lesnicar and Marquardt proposed Modular Multilevel Converter for HVDC applications in 2003 (Haridas, Khandelwal, & Das, 2016; Lesnicar & Marquardt, 2003). In this topology, a large number of identical submodules are connected in series for producing more voltage levels at the output of MMC MLI. Figure 1.8 (a) illustrates the main circuit of single phase MMC with half-bridge submodule and Figure 1.8 (b) indicates circuit of single phase MMC with full-bridge submodule. This topology consists of two arms and each arm consists of n submodules. Overall, one single phase MMC has 2n sub modules. In this topology, each submodule could be one of conventional voltage source inverters, such as half-bridge, full-bridge, etc. Half-bridge inverter can generate only $+V_c$ and 0 voltage level, so this topology with half-bridge submodules is appropriate for being connected to DC systems. Besides, full-bridge inverters generate $-V_c$, 0, and $+V_c$, hence this topology with full-bridge submodules is suitable for being connected to both DC and AC systems; however, it needs a high number of switches in

comparison with half-bridge submodules, which increases the cost of these inverters with full-bridge submodules. Figure 1.9 shows the general structure of three phase MMC.

Nowadays, this topology is used widely in industry and HVDC applications due to below pros.

Advantages:

- Different power and voltage levels are achieved.
- Developing is fast and easy.
- THD is decreased.
- Voltages are divided into power devices.
- Standard component are used.
- Approved devices are used.
- Failures are managed.
- It is modular.

Disadvantage:

- Capacitor voltage balancing is complicated.

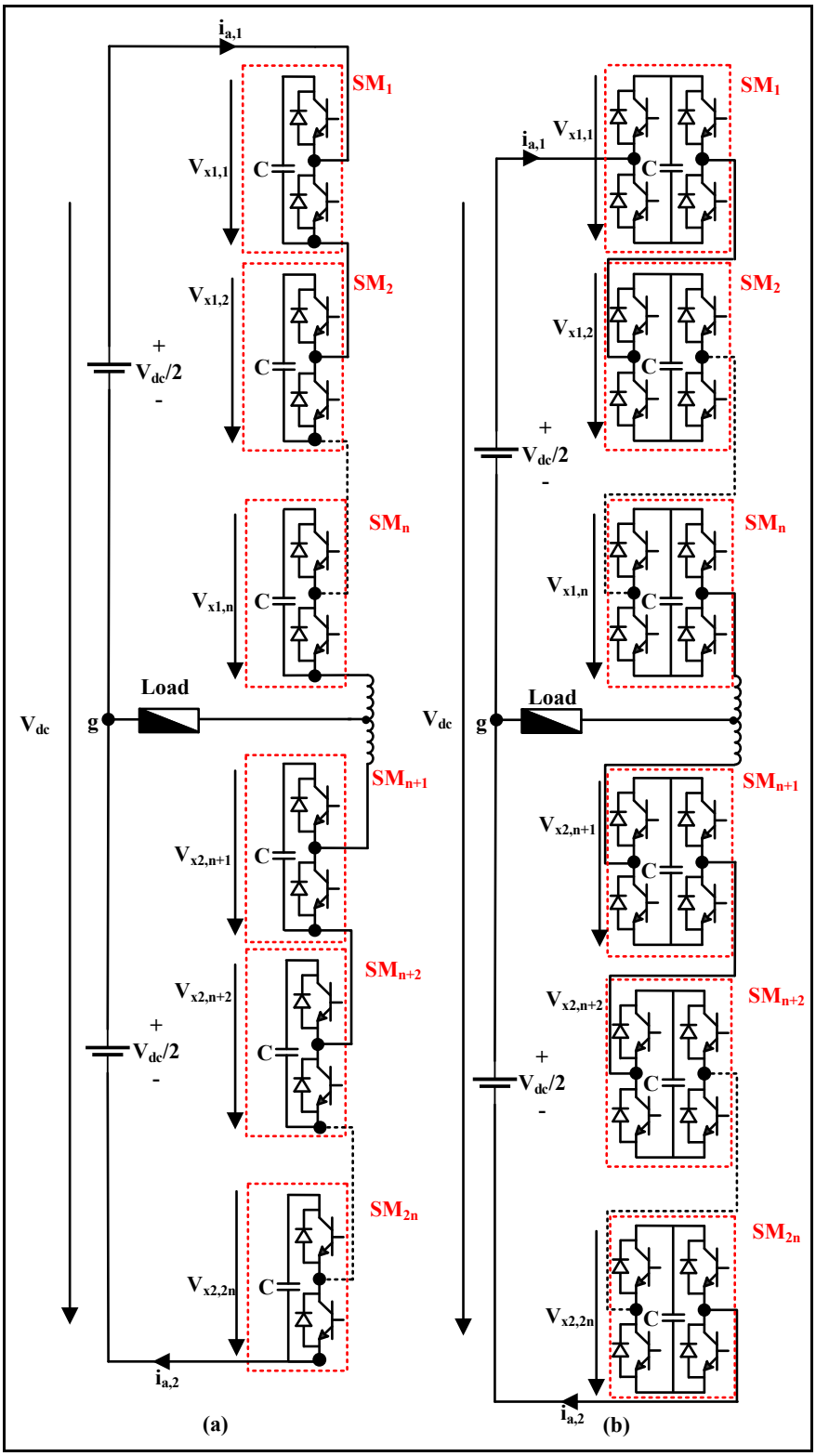


Figure 1.8 General structure of single-phase MMC (a) with half-bridge submodule (b) with full-bridge submodule

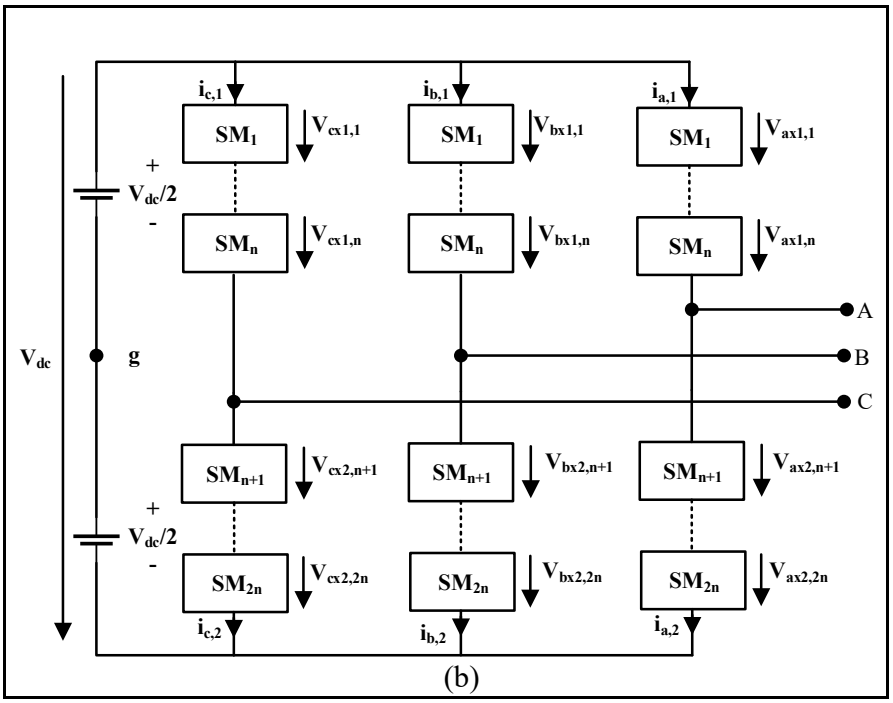


Figure 1.9 General structure of three-phase MMC

1.3 Multilevel Diode Clamped Inverter Topologies

1.3.1 Three-level Neutral Point Clamped (NPC) Inverter

Nabae, Takashi and Akagiin invented NPC inverter in 1981. NPC is also known as diode clamped multilevel inverter (Koshti & Rao, 2017; Rodriguez, Bernet, Steimer, & Lizama, 2010). In this topology, clamped diodes are used in order to limit voltage stress of electric devices. Figure 1.10 (a) illustrates the main circuit of single phase three-level NPC inverter. This topology is similar to half-bridge inverter but with two switches instead of each switch in half-bridge inverter plus two clamping diodes, one between switch S_1 and S_2 and the other one between S'_1 and S'_2 connected to the neutral point, and two bulky capacitors. S_1, S'_1 and S_2, S'_2 are complimentary. Each capacitor acts as a voltage source with value of $\frac{V_{dc}}{2}$ and the middle point of these capacitors is connected to the ground, thus three levels of voltage that the inverter produces in the output are ($\frac{+V_{dc}}{2}$, 0, $\frac{-V_{dc}}{2}$). By connecting three single-phase NPC inverters in parallel and managing the switching state in a way that each phase has 120-degree phase

difference with other phases, three-phase NPC inverter can be made, as seen in Figure 1.10 (b). Table 1.5 illustrates switching states of NPC three-level inverter and Figure 1.11 shows equivalent circuit of this topology in each state of Table 1.5.

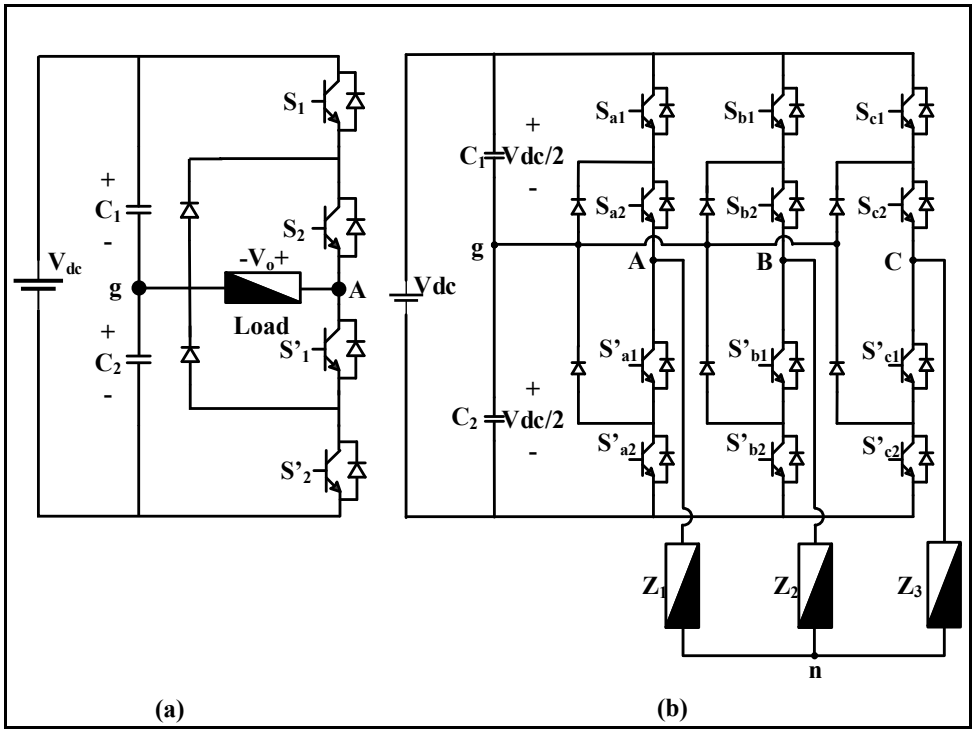


Figure 1.10 Three-level NPC inverter

Table 1.5 Switching states of three level NPC inverter

States	S_1	S_2	S'_1	S'_2	V_o
1	1	1	0	0	$\frac{+V_{dc}}{2}$
2	0	1	1	0	0
3	0	0	1	1	$\frac{-V_{dc}}{2}$

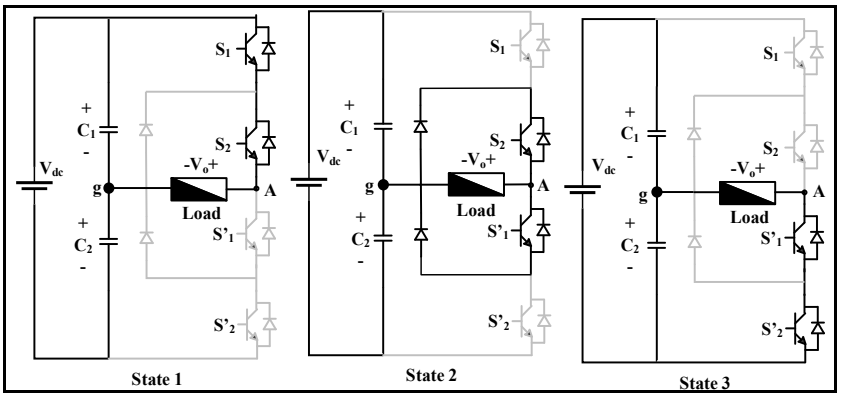


Figure 1.11 Equivalent circuit in each state of Table 1.5

1.3.2 Five-level Diode Clamped Inverter

Among the most important problems of the NPC topology, the imbalance of voltage among voltage diodes is a significant one. Indeed, as soon as three levels are exceeded, this problem appears, because the diode D_2 must support three times more voltage than diode D_1 (see Figure 1.12) (Koshti & Rao, 2017; Rodriguez et al., 2010).

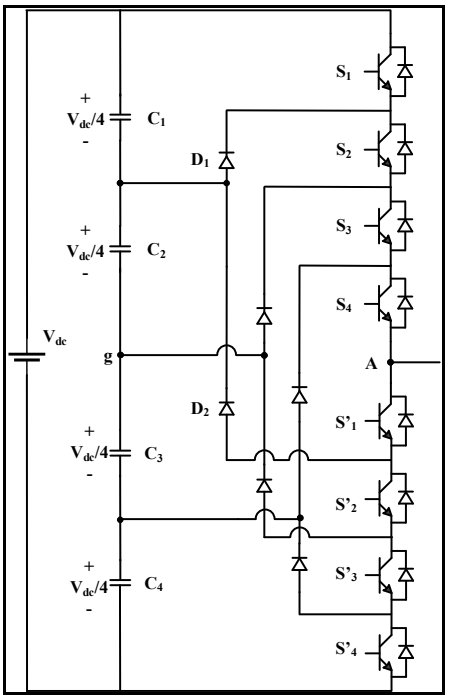


Figure 1.12 Five-level NPC inverter circuit

In general, the voltage that a diode must withstand depends on its position in the circuit, and is obtained by the following equation:

$$V_{diode} = \frac{N-1-k}{N-1} V_{dc}$$

Where:

N is the number of levels.

k is the position of the diode in the converter, which can take the values of 1 up to N-2.

V_{dc} is the voltage of the DC bus.

In order to overcome this problem, Lai and Peng (1996) suggested to use a topology similar to conventional NPC inverter, but with three series calibration diodes instead of one diode, which needs to support three times more voltage (instead of D_2) in order to divide this voltage between these diodes.

An N-level NPC inverter needs {2N-2} switches, {N-1} voltage source, and {(N-1) (N-2)} diodes and each capacitor acts like a DC source with the value of $\frac{V_{dc}}{(N-1)}$. Table 1.6 indicates the switching states of five-level NPC inverter. It should be noted that switches S_1, $S'_1$and $S_2, S'_2$and $S_3, S'_3$and S_4, S'_4 are complimentary.

Table 1.6 Switching states of five-level NPC inverter

States	**S_1**	**S_2**	**S_3**	**S_4**	**S'_1**	**S'_2**	**S'_3**	**S'_4**	**V_o**
1	1	1	1	1	0	0	0	0	$\frac{V_{dc}}{2}$
2	0	1	1	1	1	0	0	0	$\frac{V_{dc}}{4}$
3	0	0	1	1	1	1	0	0	0
4	0	0	0	1	1	1	1	0	$\frac{-V_{dc}}{4}$
5	0	0	0	0	1	1	1	1	$\frac{-V_{dc}}{2}$

Advantages:

- Switches have to tolerate half of DC voltage source.
- Voltage harmonics placed at the center double the switching frequency.
- Capacitors are pre-charged and they have low capacitance.
- Inverted are used back to back.
- It has high efficiency at fundamental frequency.

Disadvantages:

- By increasing a voltage level, the number of clamping diodes will increase.
- Precise monitoring and controlling of DC levels are needed.

Yuan and Barbi (1999, 2000) proposed a five-level converter characterized by diodes with the same voltage resistance $\frac{V_{dc}}{4}$ (Figure 1.13). Take the example where the point A is connected to the point O through the switches S_3, S_4, S'_1 and S'_2. In this case, the diodes D_3, D_4, D_7, D_8, D_9, D_{10}, D_{11} and D_{12} block zero volts, while D_2 and D5 diodes block $\frac{V_{dc}}{4}$. Since S_1 and S'_4 are blocked, D_1 and D_6 diodes will block zero volts; however, a big problem of this topology is the imbalance of output voltages. This drawback limits the use of this topology in the industry for the three-level inverter.

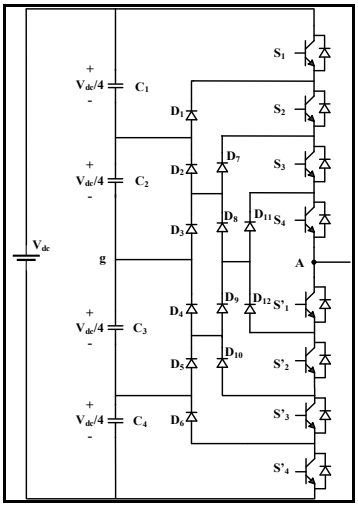


Figure 1.13 Five-level NPC inverter proposed by Yuan

1.4 Multilevel Flying Capacitor Topologies

1.4.1 Flying Capacitor (FC) Single-phase three-level inverter

The capacitor clamped inverter or flying capacitor was invented by Meynard and Foch in 1992 (Koshti & Rao, 2017; Taleb, Helaimi, Benyoucef, & Boudjema, 2016). FC inverter is alike NPC inverter, but instead of clamping diodes, capacitors are used. In this structure, each capacitor acts as a different voltage source. Figure 1.14 (a) shows the main circuit of single phase three-level FC MLI. By connecting three single-phase inverters in parallel, a three-phase FC MLI is made as shown in Figure 1.14 (b). In addition, managing the switching states of switches in the way that each phase has 120-degree phase difference with other phases is necessary.

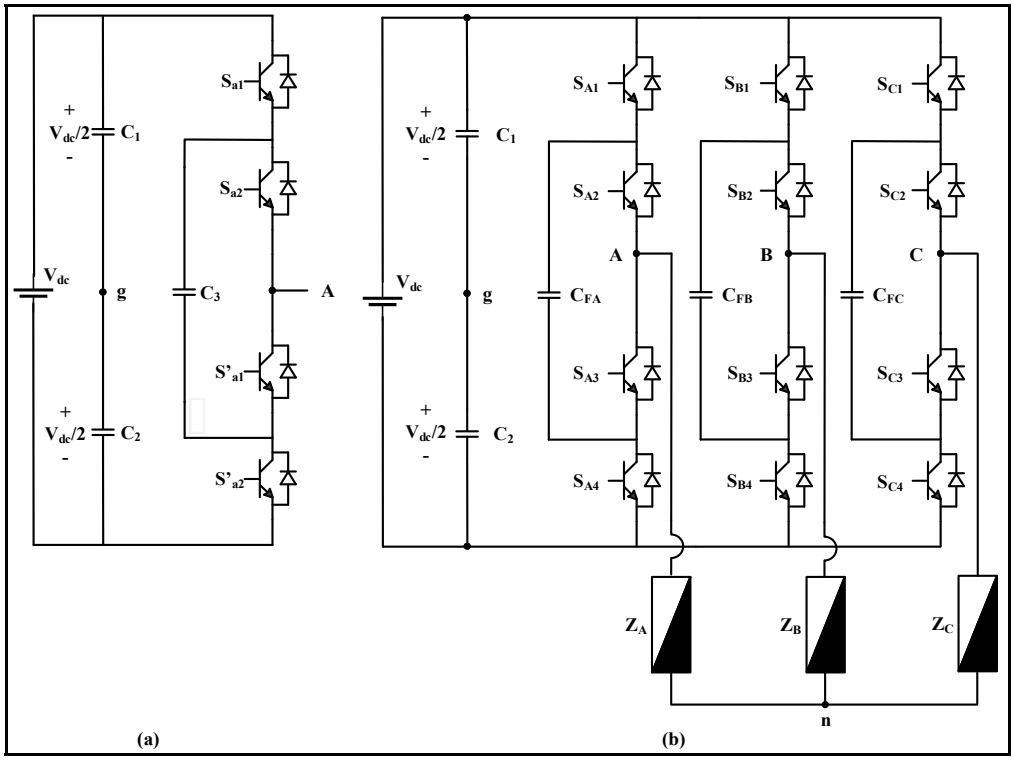


Figure 1.14 Circuit diagram of three level FC inverter

In the above-mentioned circuit, when S_{a1} and S_{a2} are ON, V_A is equal to$+V_{C1}$; when S'_{a1} and S'_{a2} are ON, V_A is equal to$-V_{C2}$; when S_{a1} and $S'_{a1}$are ON, C_3 is charged and V_A is equal to zero ; in addition, when S_{a2} and $S'_{a2}$are ON ,C_3 is discharged and also V_A is equal to zero(see Table 1.7 and Figure 1.15). An m-level FC inverter needs {2m-2} switches, {m-1} DC link capacitor, and $\left\{\frac{(m-1)(m-2)}{2}\right\}$auxiliary capacitor.

Table 1.7 Switching states of three-level FC inverter

States	S_{a1}	S_{a2}	S'_{a1}	S'_{a2}	V_o	Effect on capacitor(C_3)
1	1	1	0	0	$\frac{+V_{dc}}{2}$	No effect
2	0	0	1	1	$\frac{-V_{dc}}{2}$	No effect
3	1	0	1	0	0	Charging
4	0	1	0	1	0	Discharging

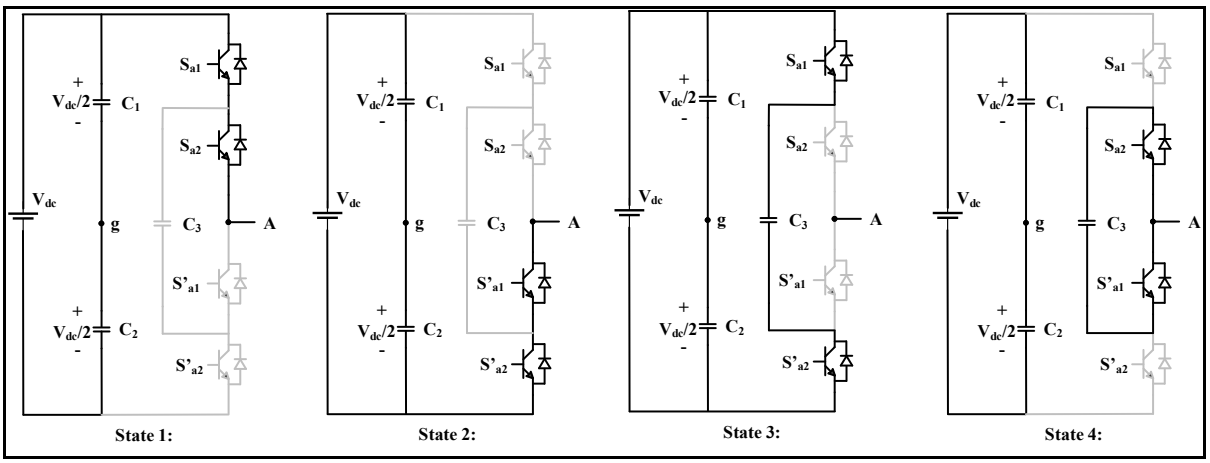


Figure 1.15 Equivalent circuit for each state in Table 1.7

1.4.2 Flying Capacitor (FC) Single-phase five-level inverter

Figure 1.16 shows the main circuit of FC single phase five-level inverter and Table 1.8 illustrates its switching states (Koshti & Rao, 2017; Taleb et al., 2016). In this topology, C_1,

C_2, C_3, and C_4 are charged to the value of $\frac{V_{dc}}{4}$, hence they can be considered as four identical DC sources with the value of $\frac{V_{dc}}{4}$.

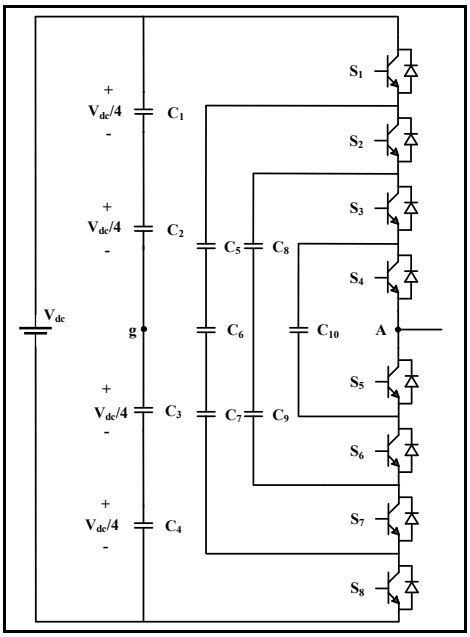


Figure 1.16 Circuit diagram of five level FC inverter

Table 1.8 Switching states of FC inverter

States	**S_1**	**S_2**	**S_3**	**S_4**	**S_5**	**S_6**	**S_7**	**S_8**	**V_o**
1	1	1	1	1	0	0	0	0	$\frac{+V_{dc}}{2}$
2	1	1	1	0	1	0	0	0	$\frac{+V_{dc}}{4}$
3	1	1	0	1	1	1	0	0	0
4	1	0	0	1	1	1	1	0	$\frac{-V_{dc}}{4}$
5	0	0	0	0	1	1	1	1	$\frac{-V_{dc}}{2}$

Advantages:

- No clamping diode is needed.
- One dc source is required.
- Without using transformer, the required number of voltage levels can be achieved.
- The capacitors are charged to different voltage levels instead of sharing the same voltage.
- Active and reactive power flow is controllable.
- Inverter can stay connected in short period outages and deep voltage sags.

Disadvantages:

- Complicated modulation process due to initial setup of capacitors.
- Controlling the voltage level of all capacitors is complicated.
- Pre-charging of all capacitors to the same voltage is complex.
- Switching utilization and efficiency for transmitting active power is poor.
- Design is complex when voltage across the capacitors has a large fraction of DC bus voltage.
- Capacitors are more expensive and bulky in comparison with diodes.
- Due to increasing the number of levels, packaging is more difficult.

1.5 Asymmetric hybrid multilevel inverters (AH-MLI)

With combination of two conventional inverters, Asymmetric hybrid MLI has been proposed. Figure 1.17 and Figure 1.18 show two popular Asymmetric hybrid multilevel inverters(Malinowski, Gopakumar, Rodriguez, & Perez, 2010). Normally, for decreasing the number of separate DC sources, CHB MLI is combined with other topologies. These inverters produce more voltage levels. As a result, they have a positive effect on the THD and power quality; however, these topologies are not considered in this paper owing to the fact that most of them are not single dc source inverters. Nevertheless, one of these topologies, which is popular in industry and is also single dc source, is taken into consideration.

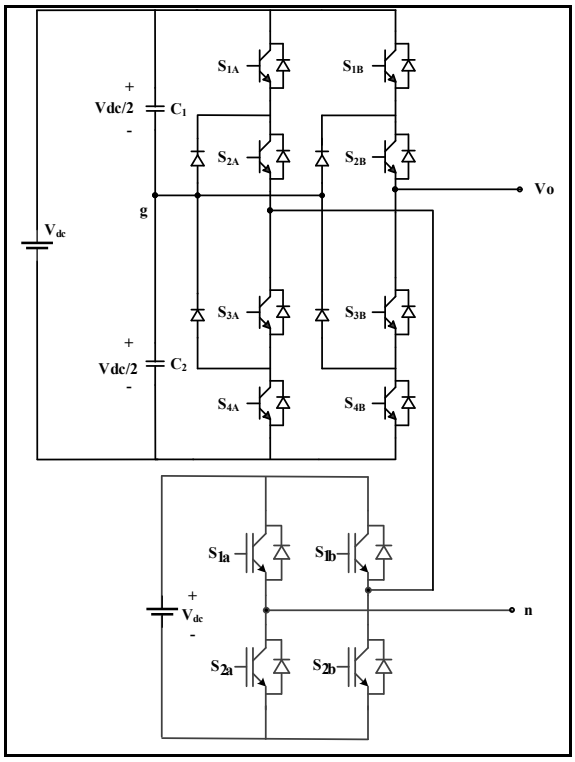


Figure 1.17 DC MLI and CHB MLI cascaded

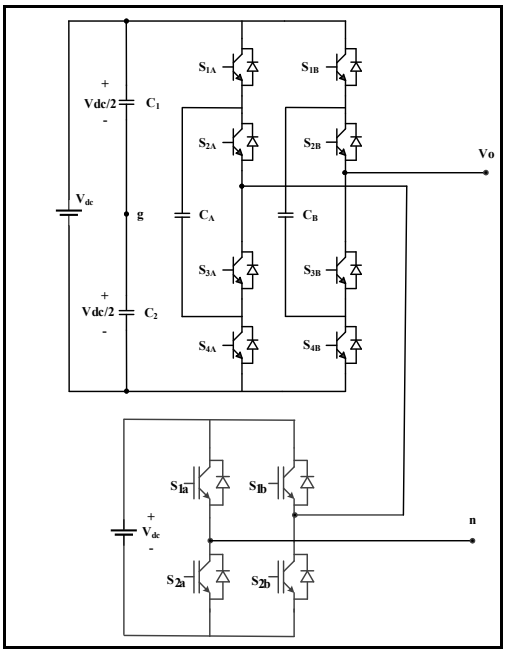


Figure 1.18 FC MLI and CHB MLI cascaded

1.6 Modulation Strategies to Control Switches of Inverters

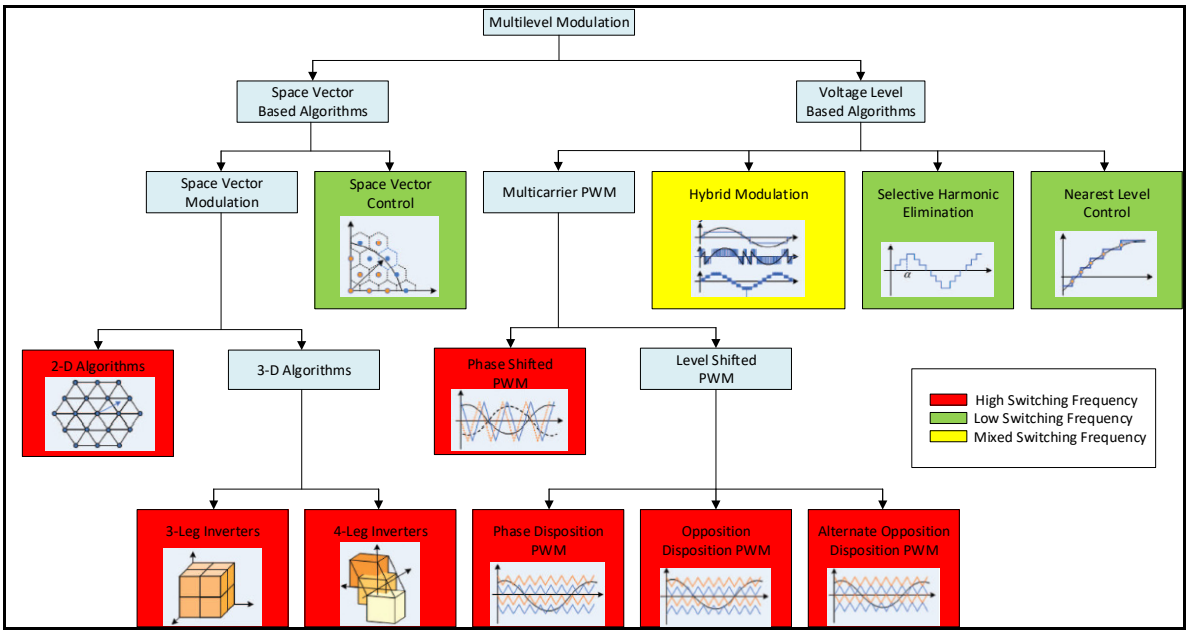


Figure 1.19 Conventional strategies for modulating the waveforms
Taken from Franquelo et al (2008)

Figure 1.19 illustrates most strategies for modulating the waveforms. The popular techniques in industry include phase shift pulse width modulation (PS-PWM), level shift pulse width modulation (LS-PWM), space vector modulation (SVM) and selective harmonic elimination. In this section, three methods of common modulation control strategies; PS-PWM, LS-PWM and SVM, highly used in industry, will be explained. Before describing these methods, to compare the two level inverter with multilevel one, bipolar PWM for half-bridge inverters will be discussed. In addition, it should be noted that the number of carrier signals for generating multilevel voltages depends on the counts of voltage levels. The following equation shows the relation between voltage levels and number of carriers.

$$N=L-1 \tag{1.1}$$

Where N is the number of carrier signals and L is the voltage levels. For instance, to generate 5 voltage levels, four carriers are needed.

1.6.1 Bipolar PWM

This modulation technique is called bipolar because in this method the output voltage of the inverter is varied between two values. Below equation shows the modulation index of bipolar PWM (Bin, 2006a, 2006b).

$$m = \frac{V_{ref}}{V_{cr}} \tag{1.2}$$

In this approach, generating bipolar voltage at the output needs one sinusoidal reference and one carrier signal. In this method, sinusoidal reference signal is compared to a carrier signal. When $\boldsymbol{V_{ref}} > \boldsymbol{V_{cr}}$ the value of switching signal will be one otherwise the switching signal value will be -1. (See Figure 1.20)

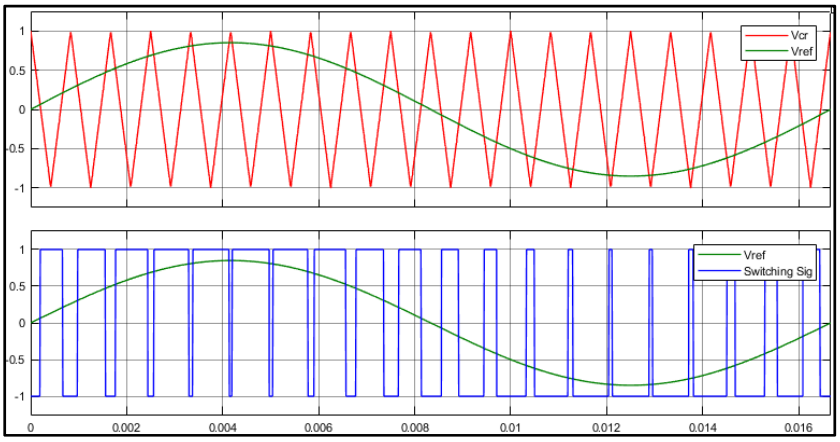


Figure 1.20 Bipolar PWM

1.6.2 Level Shifted Modulation

In this method, career signals are placed vertically between maximum and minimum value of sinusoidal reference signal(Bin, 2006a). In general, the sinusoidal reference signal is varied between 1 and -1. As a result, carriers are placed between 1 and -1. In this approach, an N level inverter needs N-1 carriers Equation (1.1). These carriers have the same frequency and peak-

to-peak amplitude. For example, for a nine level inverter like PUC9, eight carriers are needed. Assuming that sinusoidal reference signal fluctuates between 1 and -1, the amplitude of each carrier is equal to 0.25. In this method, triangular carriers' signals are compared to a sinusoidal reference signal. Equation (1.3) indicates the process of generating switching signal in this method and Figure 1.21 illustrates carriers' signals, sinusoidal reference signal and switching signal in this approach.

$$\begin{cases} \text{If } V_{ref} \geq Cr_1 & \rightarrow \text{Switching signal} = 8 \\ \text{If } Cr_2 \leq V_{ref} < Cr_1 & \rightarrow \text{Switching signal} = 7 \\ \text{If } Cr_3 \leq V_{ref} < Cr_2 & \rightarrow \text{Switching signal} = 6 \\ \text{If } Cr_4 \leq V_{ref} < Cr_3 & \rightarrow \text{Switching signal} = 5 \\ \text{If } Cr_5 \leq V_{ref} < Cr_4 & \rightarrow \text{Switching signal} = 4 \\ \text{If } Cr_6 \leq V_{ref} < Cr_5 & \rightarrow \text{Switching signal} = 3 \\ \text{If } Cr_7 \leq V_{ref} < Cr_6 & \rightarrow \text{Switching signal} = 2 \\ \text{If } Cr_8 \leq V_{ref} < Cr_7 & \rightarrow \text{Switching signal} = 1 \\ \text{If } Cr_8 > V_{ref} & \rightarrow \text{Switching signal} = 0 \end{cases} \quad (1.3)$$

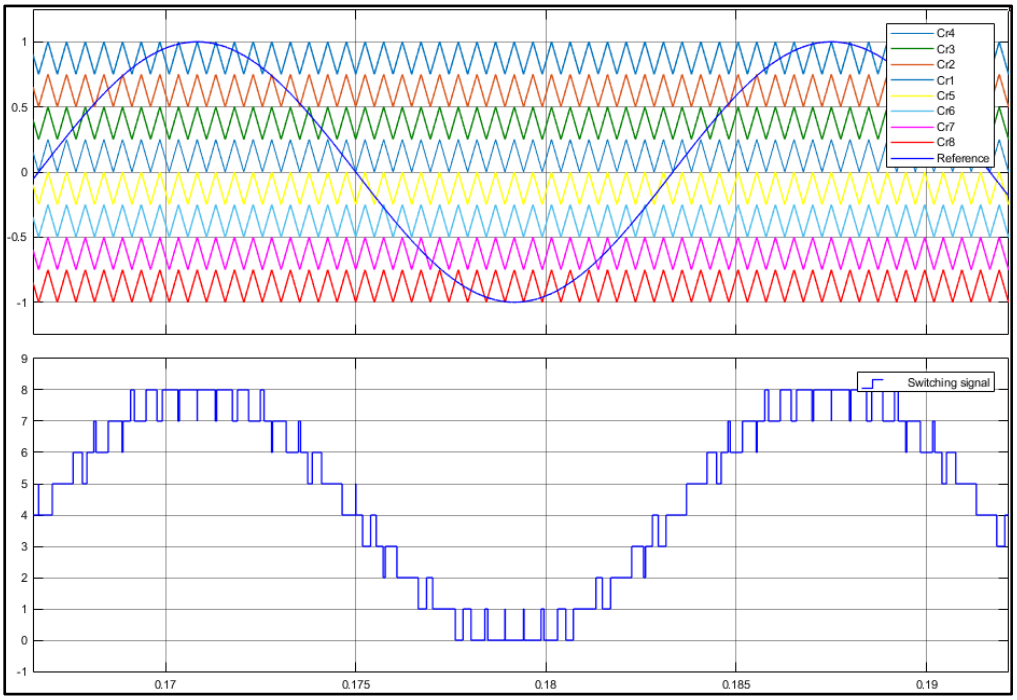


Figure 1.21 LS-PWM for nine-level inverters

1.6.3 Phase Shifted Modulation

In m voltage levels, MLI, m-1 carriers are required for PS-PWM(Bin, 2006a, 2006b). Equation (1.4) shows how by phase displacement these carriers should be placed between two adjacent carriers.

$$\Delta\emptyset = \frac{2\pi}{m-1} \tag{1.4}$$

For PS-PWM in five-level inverter, four triangular carriers are needed (see Figure 1.22) based on equation (1.4), $\Delta\emptyset = \frac{\pi}{2}$. It means that, Cr_1 with Cr_4 and Cr_2 with Cr_3 have 180° phase shift. Equation (1.5) shows Modulation index in PS-PWM.

$$m = \frac{V_{ref}}{Cr_i} \tag{1.5}$$

In this equation, Cr_i are the carrier waveforms and i=1,2, 3 ,… ,m. It should be mentioned that in this modulation technique all carriers have the same size, but the Cr_i in LS-PWM for m voltage level inverter must be multiplied by m-1 because of the amplitude of carriers that are divided to m-1.

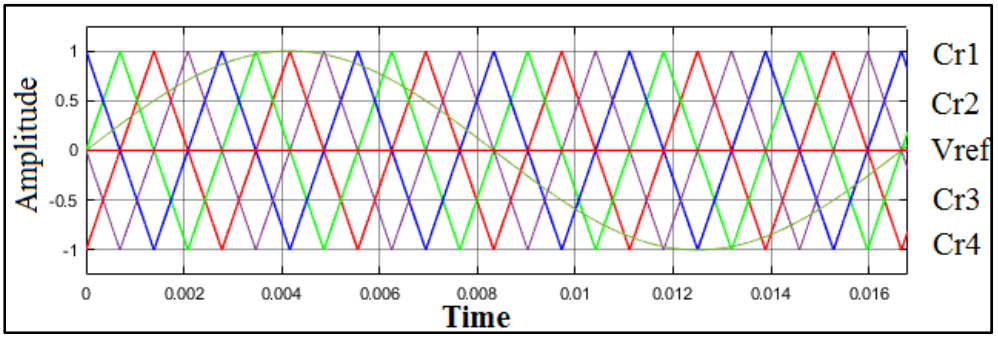


Figure 1.22 Phase shift PWM carrier wave forms

In order to shift the harmonic orders to next frequency, phase shift modulation technique is an industrial approach. Therefore, filters' size will be either low or neglected depending on the

switching frequency. Through PS-PWM, which is a modulation method, harmonic orders will be shifted to the multiples of (m-1) by switching frequency. The formula is as follows:

$$f_{sw-inverter} = (m-1)\ f_{cr} \quad (1.6)$$

If the modulation technique is PS-PWM, harmonic components are shifted due to the fact that carriers' frequency is multiplied by inverter's switching frequency. Inverter's frequency, however, is equal to carriers' frequency at level shift modulation.

Additionally, for modulating the reference voltage by the carrier signals, there is another technique, where two carrier signals are put at the phase shift of 180° and one reference voltage is compared to the signals. In this method, if $V_{ref} > V_{cr1}$ switch 1 gate is turned on. Also, the gate of another switch is turned on when $V_{ref} < V_{cr2}$. The modulation signals are shown in Figure 1.23.

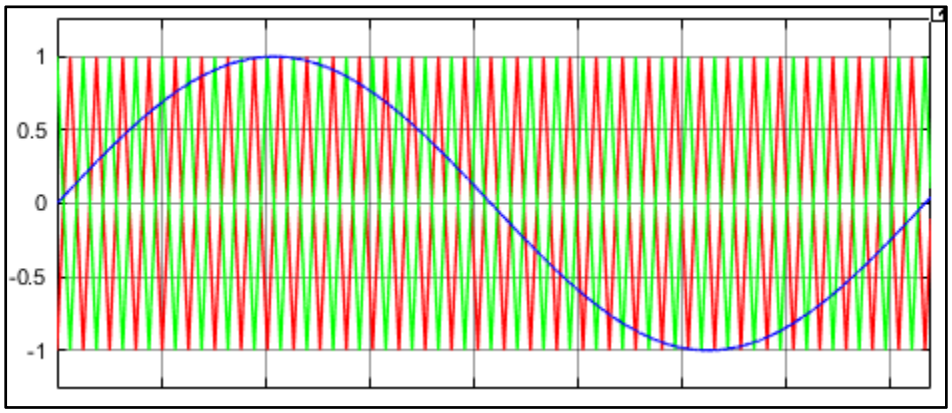


Figure 1.23 Unipolar modulation signal

1.6.4 Space Vector Modulation (SVM)

For generating pulses for switches, SVM is a method that uses vector concept, where the voltage vectors, which are produced by each switching state set, are calculated(Bin, 2006b). Next comes the instantaneous determining of magnitude and phase of the reference voltage vector. With respect to the location of reference voltage vector, the nearest voltage vectors'

combination is chosen and the corresponding switches for generating these voltage vectors are fired considering the time intervals which are specified. The calculation of the mentioned intervals is according to reference voltage vector. Figure 1.24 indicates the three-phase inverter H-bridge's concept of vectors. The equation mentioned below is used for modulation index if $\boldsymbol{V_d}$ is the DC voltage and $\boldsymbol{V_{ref}}$ is the reference voltage.

$$ma = \frac{\sqrt{3}V_{ref}}{V_d} \tag{1.7}$$

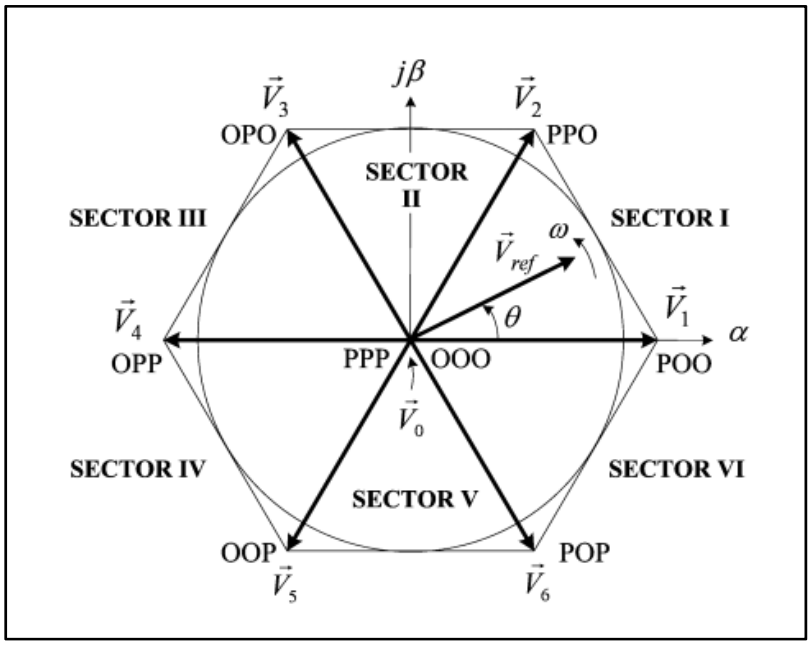


Figure 1.24 Space-vectors modulation to produce switching states of two level inverters Taken from Bin (2006b)

1.7 Single-DC Source Multilevel Inverter Topologies

1.7.1 Single-DC Source CHB Inverter

In the below five-level CHB inverter (Figure 1.6), if one of DC sources is replaced with one capacitor, it turns to single DC source CHB inverter as illustrated in Figure 1.25 (Vahedi, Sharifzadeh, Al-Haddad, & Wilamowski, 2015). It can be seen that the upper cell is connected

to voltage source and the lower cell is connected to the capacitor. Voltage source must charge the capacitor at the desired level, and for generating some voltage levels, capacitor is connected to the load. In this topology, for producing seven levels of voltage, capacitor must be controlled at $V_{dc}/2$. For clarification, we assume that the voltage source is equal to 2E; consequently, the voltage of the capacitor must be regulated at E. As a result, seven levels of output voltage are equal to +3E, +2E, +E, 0, -E,-2E,-3E. In this topology, in each cell (H-bridge cell), the switches which are in a vertical direction are complimentary; therefore, $S_2=\overline{S_1}$, $S_4=\overline{S_3}$, $S_6=\overline{S_5}$, and $S_8=\overline{S_7}$. To clarify, switch S_i =0 when the switch in off and S_i =1 when the switch is on and also $V_c=V_{dc}/2$.

Considering the above-mentioned information, it can be written that:

$$\begin{cases} V_1 = S_1 V_{dc} - S_3 V_{dc} \\ V_2 = S_5 V_{dc} - S_7 V_{dc} \end{cases} \Longrightarrow V_{an} = \left(S_1 - S_3 + \frac{S_5}{2} - \frac{S_7}{2} \right) \qquad (1.8)$$

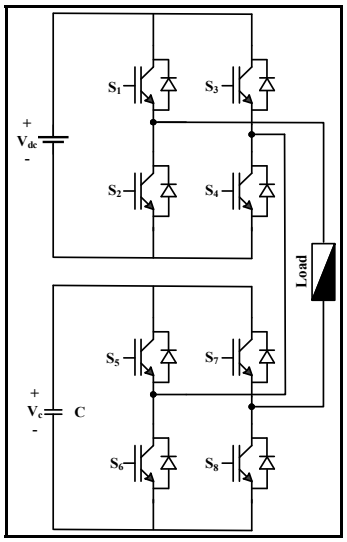


Figure 1.25 Single-phase Single DC source Cascade H-bridge (CHB) multilevel inverter

Table 1.9 illustrates the switching and capacitor state of CHB seven-level inverter. It can be seen that some redundant switching states exist in this table but these states are useful for balancing the capacitor voltage during charging and discharging. Figure 1.26 illustrates

equivalent of CHB seven-level inverter in each state, as shown in Table 1.9. It can be seen that states 2, 5, 8 do not affect capacitor since it is disconnected from voltage source and load. Moreover, States 3,4,6,7 play an important role for charging and discharging the capacitor. Furthermore, in States 1 and 9 the output is equal to the summation of V_c and V_{dc}. In these states, the capacitor is discharged firstly and then it is charged with reverse polarity, which is not desired. In this situation, larger capacitor is beneficial since it needs more time for discharging; as a result, it remains constant for a longer duration of time and in the next state, the capacitor will be charged again. In this topology, we can use PWM to manage these states easily.

Table 1.9 Switching states and Capacitor state of single-phase single-dc-source CHB cascaded 7-level inverter

States	**S_1**	**S_3**	**S_5**	**S_7**	**V_1**	**V_2**	**V_{an}**	**Effect on capacitor(C)**
1	1	0	1	0	$+V_{dc}$	$+V_c$	+3E	Discharging
2	1	0	1	1	$+V_{dc}$	0	+2E	No effect
3	1	0	0	1	$+V_{dc}$	$-V_c$	+E	Charging
4	1	1	1	0	0	$+V_c$	+E	Discharging
5	1	1	1	1	0	0	0	No effect
6	0	0	0	1	0	$-V_c$	-E	Discharging
7	0	1	1	0	$-V_{dc}$	$+V_c$	-E	Charging
8	0	1	0	0	$-V_{dc}$	0	-2E	No effect
9	0	1	0	1	$-V_{dc}$	$-V_c$	-3E	Discharging

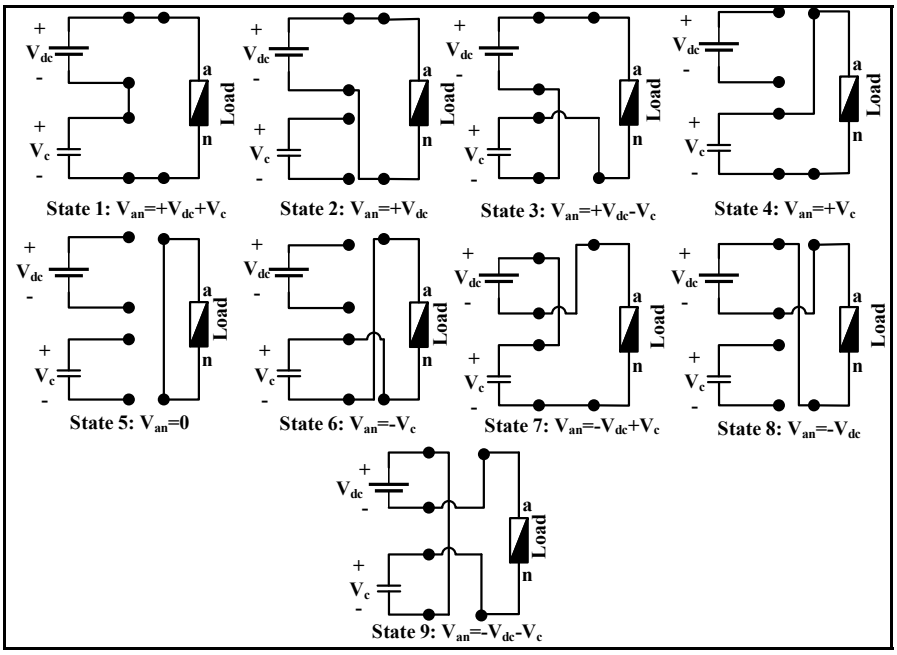


Figure 1.26 Equivalent circuit in each state shown in Table 1.9

1.7.2 Single Phase Seven Level Cascaded H-Bridge Multilevel Inverter

Improving the quality of MLI output while using fewer switches is the main objective of this topology (Shaikh & Rana, 2016). MLI design has a concerning issue, which is producing sinusoidal output waveform. In fundamental switching topology, a significant issue is determining the switching angles in a way that voltage with fundamental frequency is produced. Figure 1.27 illustrates general structure of this inverter.

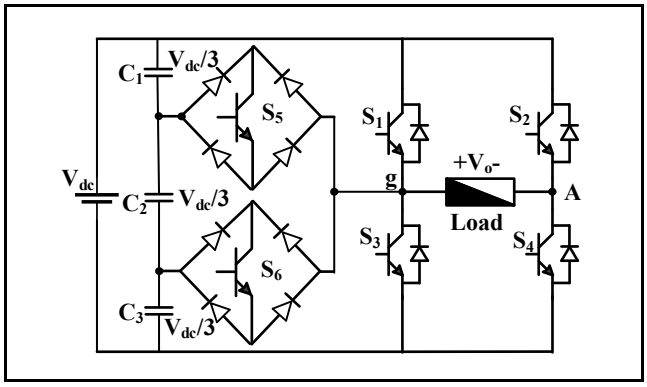


Figure 1.27 Single Phase Seven Level Cascaded H-Bridge MLI circuit

Table 1.10 and Figure 1.28 show the switching states and equivalent circuit in each state. This topology has three cycles as explained below. Firstly, when the current and the voltage output has the same polarity, positive half cycle happens. In this cycle, S_1 and S_4 are ON and S_5 and S_6 determine power supply voltage of H-bridge. The current path consists of S_1 and S_4 when the output voltage is equal to V_{dc} (State.1). When output voltage is $\frac{2V_{dc}}{3}$, the current path is via S_5 and S_4 (State.2) and $V_o = \frac{V_{dc}}{3}$ When switches S_6 and S_4 are ON. Secondly, zero cycles happens when S1 and S2 or S3 and S4 are ON. In this mode, the output voltage is zero (State.4, and State.5). Finally, negative half cycle happens when voltage output has opposite polarity. In this cycle, S_2 is ON, and S_5, S_6, and S_3 specify power supply of H-bridge. In negative half-cycle, when S_3 is on V_o is equal to $-V_{dc}$when S_6 is on V_o is equal to $\frac{-2V_{dc}}{3}$, and when S5 is on $V_o = \frac{-V_{dc}}{3}$.

Table 1.10 Switching states

States	**S_1**	**S_2**	**S_3**	**S_4**	**S_5**	**S_6**	**V_o**
1	1	0	0	1	0	0	V_{dc}
2	0	0	0	1	1	0	$\frac{2V_{dc}}{3}$
3	0	0	0	1	0	1	$\frac{V_{dc}}{3}$
4	0	0	1	1	0	0	0
5	1	1	0	0	0	0	0*
6	0	1	0	0	1	0	$\frac{-V_{dc}}{3}$
7	0	1	0	0	0	1	$\frac{-2V_{dc}}{3}$
8	0	1	1	0	0	0	$-V_{dc}$

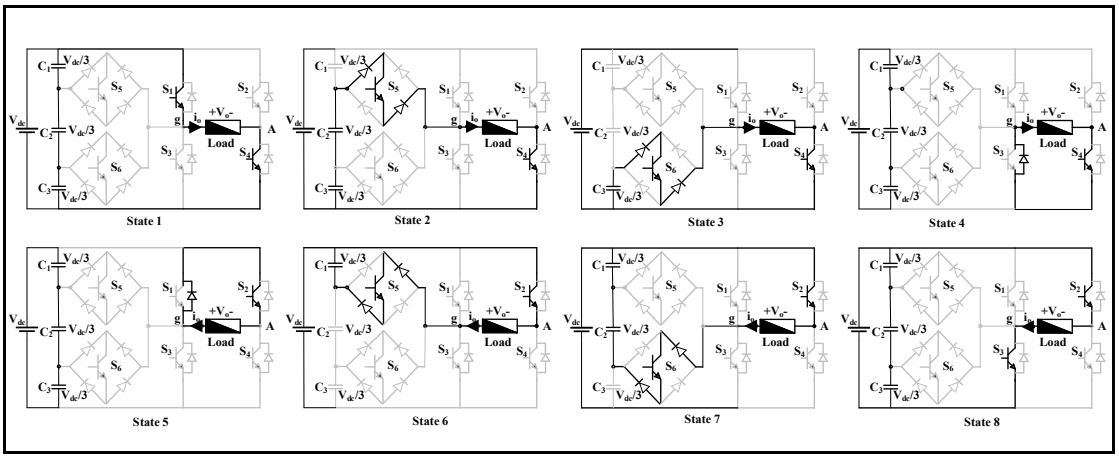


Figure 1.28 Current path in each switching state of Table 1.10

1.7.3 Step-Up Multilevel Inverter with a Single DC Source

There are plenty of famous topologies for inverters, most of which have deficits. For example, in NPC, and FC inverters, the combination of capacitors and switches is used so that input voltage is divided into smaller voltages; these voltages are then used for producing different levels of voltage in the output of inverter, but they face voltage unbalancing problem in capacitors. Handling this problem may need an additional circuit. CHB (H-bridge) inverter needs separate DC source, thus the magnitude and price of circuit is affected. Besides, in current applications, transformers are widely used in order to boost the low input voltages, which are bulky and expensive. Ye et al. proposed a SC inverter topology with voltage balancing and low number of switches, and yet it needs a lot of diodes, etc. Switching capacitor (SC) inverters is a new alternative for multilevel inverters so as to solve the above-mentioned problems in other inverters. These inverters are used mainly in high-power range and medium power range applications.

Circuit Topology:

Boosting the voltage, which is the most significant concept of this topology, is achieved by charging several capacitors in different stages (Taghvaie, Adabi, & Rezanejad, 2016). To charge a capacitor, a series of several capacitors are used. Arranging the switches in a special manner enables the capacitor's charging and discharging through creating paths.

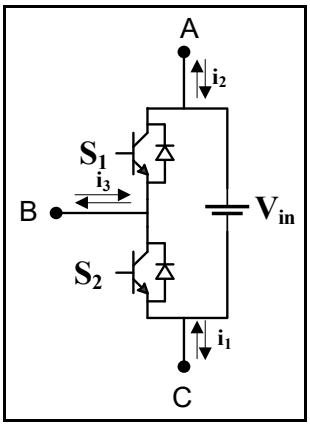


Figure 1.29 Half-bridge module

Building Block Modules:

A half-bridge module is shown in Figure 1.29. The combination of controlled switches, like IGBT, is indicated by *S*1 and *S*2, which enables bidirectional current flow. These switches can just block positive off-state voltage. Obviously, A, B, and C heads cannot control the current flow.

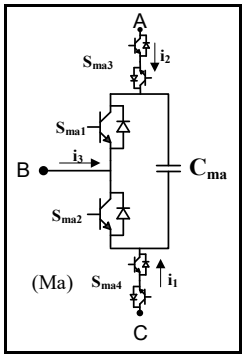


Figure 1.30 Add two bidirectional switches to half bridge inverter

The introduced building block enables creating bidirectional controllable current through the addition of two bidirectional switches (*S*3 and *S*4) providing four-quadrant performance to the half-bridge modules (see Figure 1.30). These bidirectional switches enable charging and discharging of the capacitor through paths from *A*, *B*, and *C*, which could be eliminated when the bidirectional current flow control from each side of this module is not needed anymore.

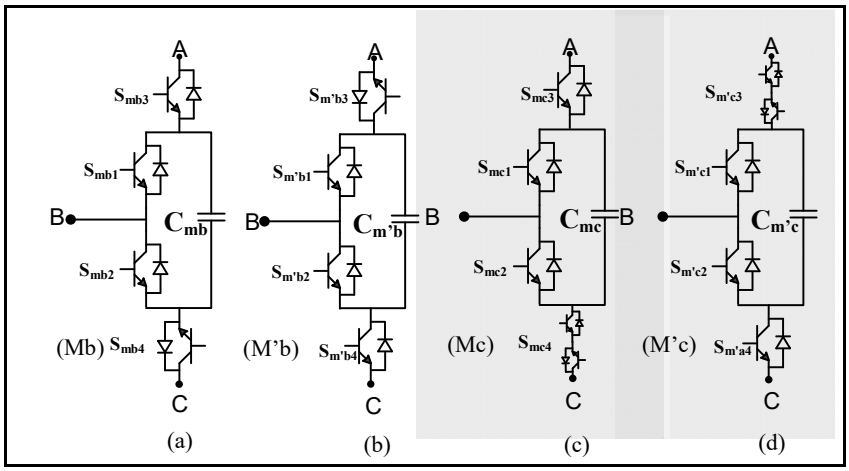


Figure 1.31 (a), (b) unidirectional current control in two sides,
(c), (d) unidirectional current control in one side and bidirectional in other side

In Figure 1.31 (a) and Figure 1.31 (b), current can be controlled only in one side, whereas in Figure 1.31 (c) and Figure 1.31 (d), bidirectional current control from one side and unidirectional current control from the other side of the module are enabled. Different switching states, the output voltage, and the direction of currents of this module are shown in Table 1.11. It should be noted that $i1$, $i2$, and $i3$ are considered positive for the considered directions at Figure 1.30.

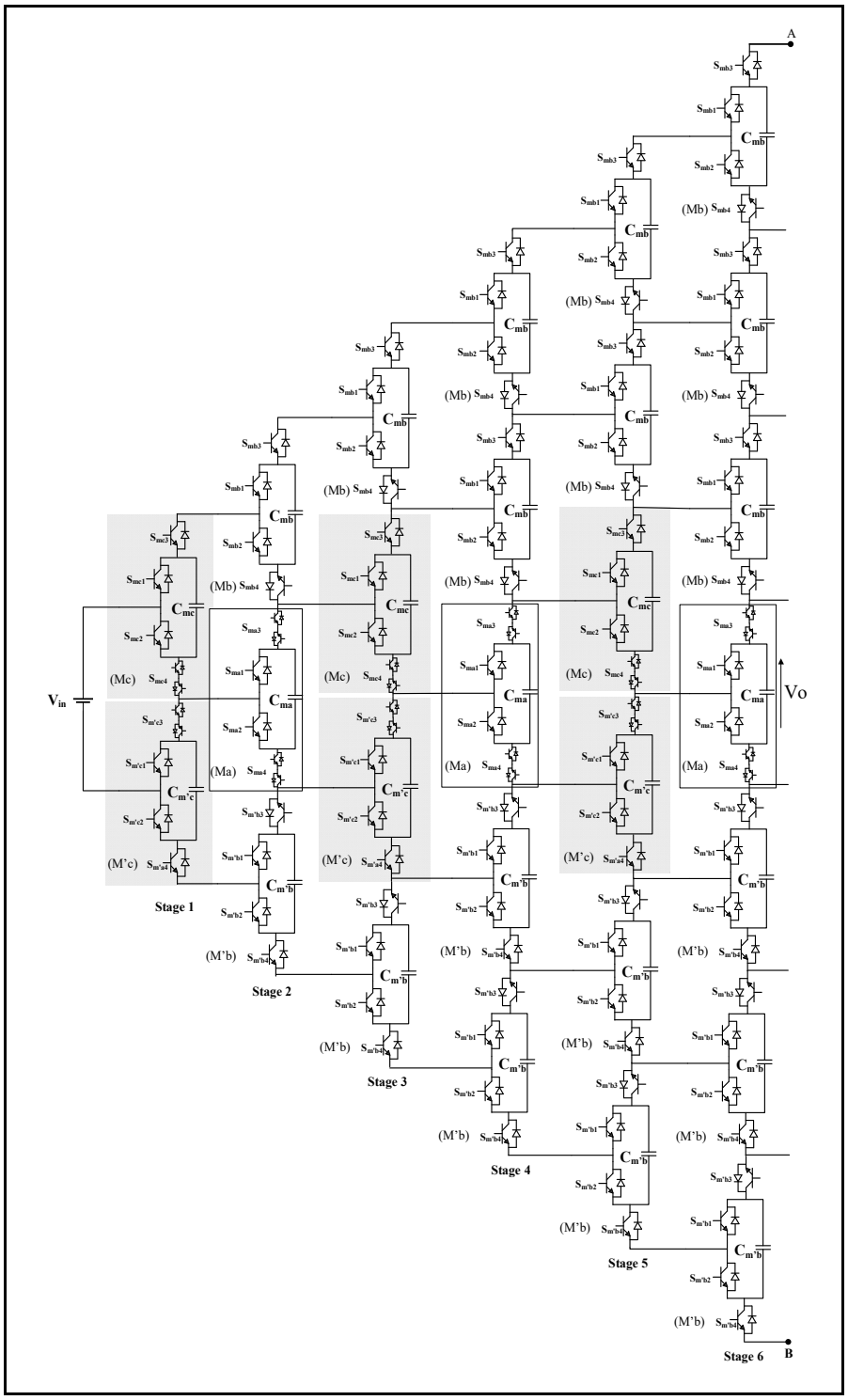


Figure 1.32 Circuit of step-up multilevel inverter with single dc source

Table 1.11 Switching states

States	S_1	S_2	S_3	S_4	Module Voltage	Current Direction
1	1	0	0	1	$V_{BC}= +V_C$	$i_1< 0$, $i_3< 0$
2	0	0	1	1	$V_{AC}= - V_C$	$i_1> 0$, $i_2< 0$
3	0	1	0	1	$V_{BC} = 0$	$i_3 > 0$, $i_1< 0$
4	0	1	1	0	$V_{AB}= +V_C$	$i_2< 0$, $i_3> 0$
5	1	0	1	0	$V_{AB}= 0$	$i_1< 0$, $i_3< 0$
6	1	0	0	1	$V_{BC}= +V_C$	$i_1> 0$, $i_3< 0$
7	0	0	1	1	$V_{AC}= - V_C$	$i_1< 0$, $i_2 > 0$
8	0	1	0	1	$V_{BC} = 0$	$i_3< 0$, $i_1> 0$
9	0	1	1	0	$V_{AB}= +V_C$	$i_2> 0$, $i_3< 0$
10	1	0	1	0	$V_{AB}= 0$	$i_2> 0$, $i_3< 0$
11	0	0	0	0	0	-

Structure:

A multi-structure inverter comprising different modules of Figure 1.33-35 is shown in Figure 1.32, in which modules with bidirectional current control capability are used in the middle of this triangular structure (*Mc, M_c*) for odd stages and (*Ma*) for even stages. Upper and lower sides of this structure are filled with *Mb* and *M_b* modules sequentially, being the unidirectional current-controlled ones. It is worth being mentioned again that the capacitors of the previous stage can charge the capacitors of each coming stage. Considering this case, the input dc sources charge the capacitors of the first stage to V_{in}. The second stage capacitors are charged to 3*V*in, increasing the capacitors' voltage of the third stage to 6*V*in. In general, where *n* = 2, 3, 4 . . ., the capacitors of *n*th stage are charged to $3 \times 2^{(n-2)} \times V$in.

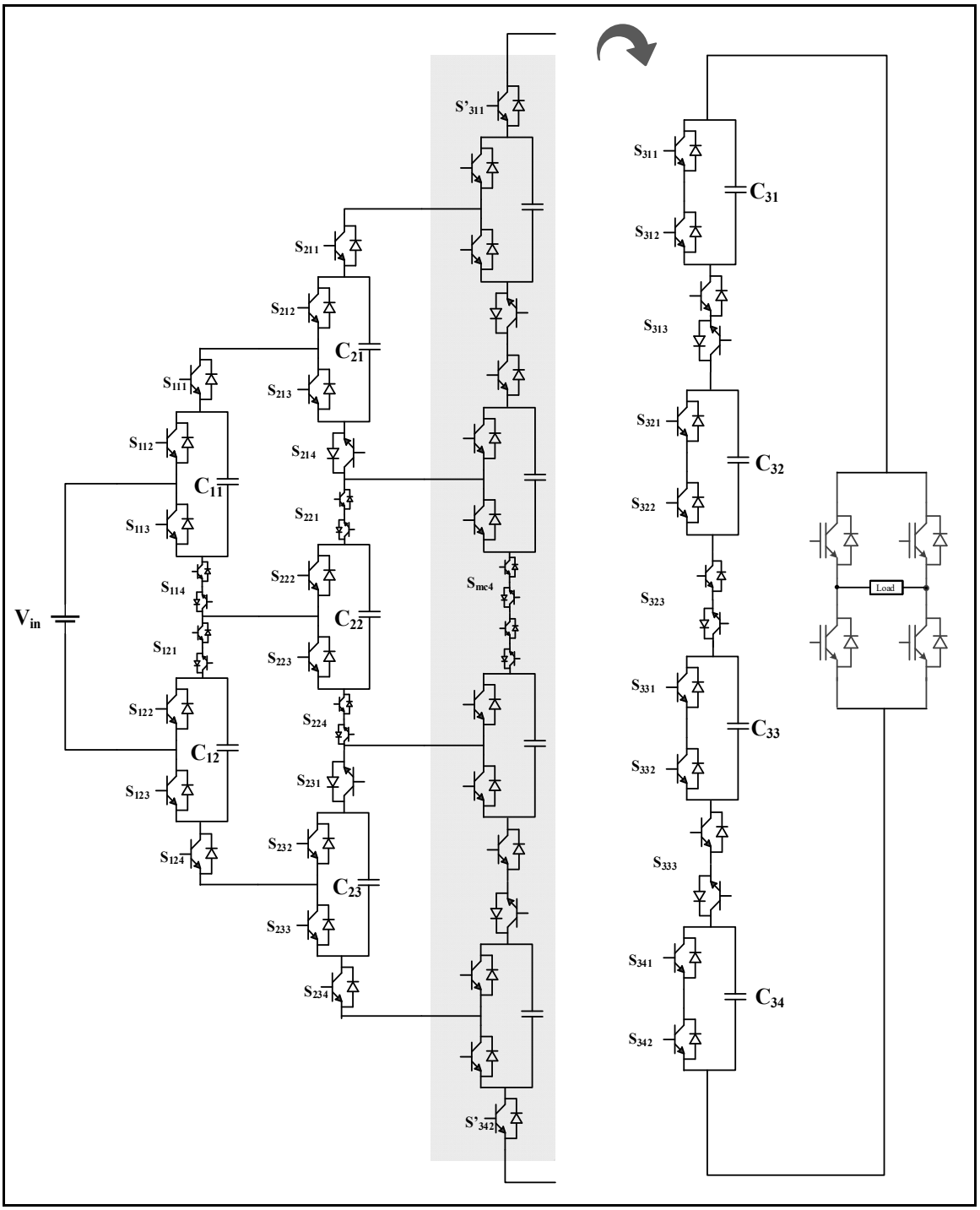


Figure 1.33 Three-stage step-up of this inverter

Operating principles:

Figure 1.33 illustrates the three-stage step-up of this inverter. It must be considered that in naming switches, which is in the format of S_{nij}, n is the stage of switch in the circuit, i is module number and j is switch number in that stage, likewise capacitor C_{nk} is the kth capacitor in nth stage. In the last stage, top and bottom switches and one of bidirectional switches must be eliminated. As can be seen in Figure 1.33, using 42 switches (38 switches for main circuit and 4 switches for full-bridge circuit) and 35 pulses for driving switches (31 pulses for main circuit and 4 pulses for h-bridge), maximum 49-level voltage at output of this inverter can be achieved.

In order to ease the switching state, hexadecimal system is used. Hexadecimal system is used to facilitate the illustration of switching states, where switching state of X is equal to a vector of 8 variables in shape of *X* = (*X*1, *X*2, *X*3, *X*4, *X*5, *X*6, *X*7, *X*8), each component has the following status:

*X*1 = (*S*111, *S*112, *S*113, *S*114)
*X*2 = (*S*121, *S*122, *S*123, *S*124)
*X*3 = (*S*211, *S*212, *S*213, *S*214)
*X*4 = (*S*221, *S*222, *S*223, *S*224)
*X*5 = (*S*231, *S*232, *S*233, *S*234)
*X*6 = (*S*311, *S*312, *S*313, *S*321)
*X*7 = (*S*322, *S*323, *S*331, *S*332)
*X*8 = (*S*333, *S*341, *S*342, 0)

Capacitor Charging:

First, using modules M_c , M'_c and DC $source$, capacitors of first stage (C_{11} and C_{12}) are charged to V_{in}, then capacitors of second stage ($C_{21}, C_{22} and\ C_{23}$) are charged to $3V_{in}$. Similarly, all capacitors of the third stage, except for upper and lower capacitors charged to $3V_{in}$, are charged $6V_{in}$(except $C_{311} and\ C_{342}$). In general, in the n-stage system, upper and lower capacitor in nth stage are charged to ($3 \times 2^{(n-3)} \times$ *V*in, *n* = 2, 3, 4, . . .), and other

capacitors are charged to ($3 \times 2^{(n-2)} \times V$in, n = 2, 3, 4, . . .). Table 1.12 indicates switching state of capacitor charging for different capacitors in this topology. Figure 1.34 shows the equivalent circuit for charging different capacitors.

Table 1.12 Switching status for capacitor charging

Capacitors	Switching state
c_{11}	5C000000
c_{12}	3A000000
c_{21}	A550C0E0
c_{22}	A539C000
c_{23}	A530A0E0
c_{34}& c_{31}	00909B1A
c_{32}	00990660, A5A0C660
c_{33}	000990C6, A53050CC

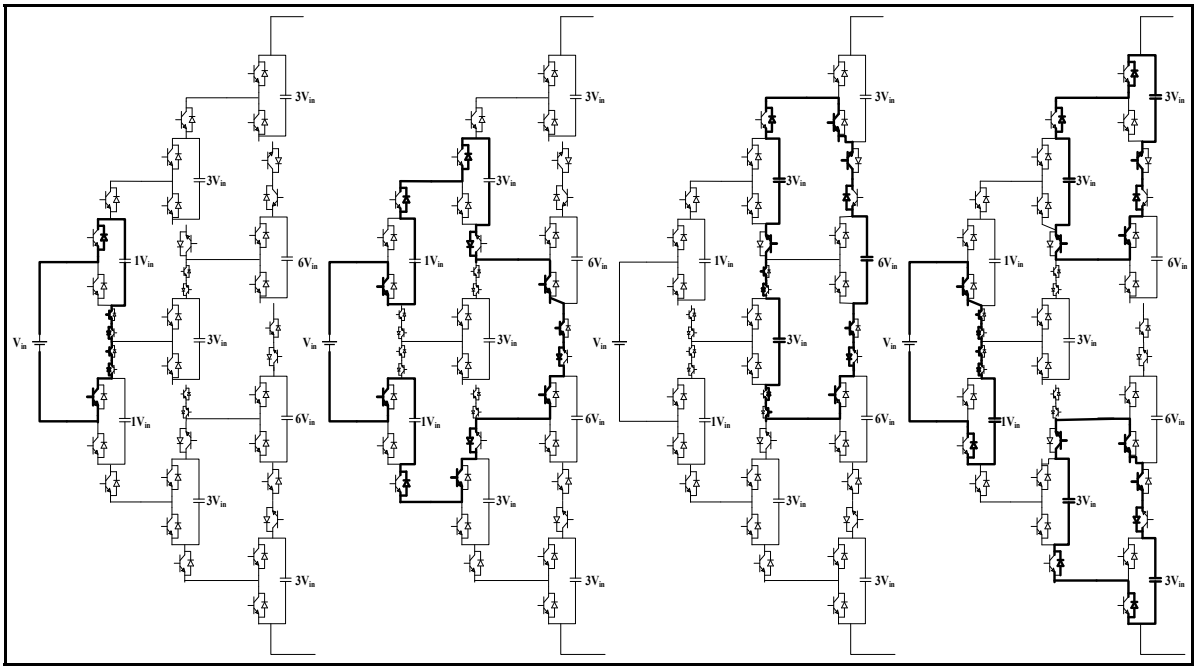


Figure 1.34 Charging different capacitors

Table 1.13 Switching states for discharging capacitors

Levels	Switching states
$1V_{in}$	C3503302- C3CO3802- C3C0A818- C350A318
$2V_{in}$	A3CO3802- C5CO3802- 99CO3802- A3503802- C550A318- A350A318- A3C0A818- C5503302- C5C0A18 1- 9950A318- 99503302- 99C0A181
$3V_{in}$	A5CO3102- A550A318- A5C0A818- A5503302- 530C3302- 530CA318- 539C3802- 539CA818- CAC39802- CA53A302- CAC30818- CA530318
$4V_{in}$	C3CO3402- C3C0A418- C3303302- C330A318- 330C3302- 330CA318- 090C3302- 090CA318- 550CA318- 550C3302- C3CO3804- C3503304- CCC30818- CC530318- C3C00818- C350C318- AAC30818- AA530318- 90C30818- 90530318- C3A03102- C3A0A8 18- 339C3802- 339CA818
$5V_{in}$	A3CO3402- A3C0A418- A3303302- A330A318- C5CO3402- C5C0A418- C5303302- C530A318- 350C3302- 350CA318- 99CO3402- 99C0A418- C5CO3804- C5503304- C5C00818- C550C318- A3CO3804- A3503304- ACC30818- AC530318- A3C00818- A350C318- 99CO3804- 99C00818- 99303302- A3A03802- A3A0A818- C5A03802- C5A0A818- AC539302
$6V_{in}$	A5CO3402- A5C0A418- A5303302- A530A318- A5CO3804- A5503304- A5C0081 8- A550C3 18- A5A03802- A5A0A818- A5CO5802- A5505302- 539C3402- 539CA418- CAC39804- CA539304- 530A3302- 530AA318- 53005302- 530C3304- 530CC318- 539C3804- 539C5802- 539CC818
$7V_{in}$	C3A03402- C3A0A418- 099C3402- 099CA418- 339C3402- 339CA418- 330A3302- 330AA318- 090A3302- 090AA318- C3503282- C350A298- 339A3802- 339AA818- C3CO5804- C3505304- 90C39804- 90539304- CCC39804- CC539304- CCC5081 8- CC550318- 90050818- 90550318
$8V_{in}$	A3A03402- A3A0A418- C5A03402- C5A0A418- 99A03402- 99A0A418- A3503282- A350A298- C5503282- C550A298- 99503282- 9950A298- 359C3402- 359CA418- 350A3302- 350AA318- 359A3802- 359AA818- C5CO5804- C5505304- A3CO5804- A3505304- 99CO5804- 99A03804
$9V_{in}$	A5A03402- A5A0A418- A5CO5804- A5505304- A5CO5402- A5305302- A5CO3404- A5C0C418- A5303304- A530C318- A5A05802- A5A03804- A5A00818- 009094E2- 009098E4- A5503282- A550A298- A5C0A828- A550A328- A5393262- A5C9C8C8- 00090318- CA350318- 00099302
$10V_{in}$	C3A03404- C3A0C418- CCA30418- 339C3404- 339CC418- 90A30418- 099C3404- 099CC418- AAA30418- 559C3404- 559CC418- C3CO5404- 33005304- C3305304- CCC39404- CC339304- 09005304- 90C39404- 90339304- 55005304- AAC39404- AA339304- C3A05804- 339C5804
$11V_{in}$	A3A03404- ACA30418- A3A0C41 8- C5A03404- 359C3404- C5A0C418- 359CC418- 99A03204- 99A0C418- A3A05402- ACA39402- C5A05402- 359C5402- 99A05402- C5CO5404- C5305304- 35005304- A3CO5404

Levels	Switching states
$12V_{in}$	A5A03404- A5A03418- A5A05402- A5CO5404- A5305304- A5503284- A5503298- A5505282- A5C0A428- A530A328- A5A0A828- A5303282- A530A298- A5C00828- A530C328- 00999804- 00990418- 00099304- 009094D4- 00009262- 009008C8- 00909962- 009098D2- 539CA428
$13V_{in}$	C3A05404- C3A39404- 339C5404- 90A39404- 099C5404- AAA39404- 559C5404- 330A5304- CCC59404- 090A5304- 550A5304- 339A5804- 099A5804- 559A5804- 339A3404- 339A3418- 559CA428- 099A5402- 099AC418- 099A3404- 339A5402- 339CA428- 559A5402- 90A59402
$14V_{in}$	A3A05404- C5A05404- 99A05404- A3505284- C5505284- 99505284- A3A0A428- C5A0A428- 99A0A428- 350A5304- 359A5804- ACA50418- ACA59402- A3303284- AC330298- A330C298- A3305282- AC339282- C5C0C428- C530C328- 350CC328- C5A00828- 359CC828- C5303284
$15V_{in}$	A5A05404- A5505284- A5A0A428- A5303284- A530C298- A5305282- A5C0C428- A530C328- A5A00828- A5395264- A5A9C4C8- A5393252- A5C9C948- 00999404- 00909562- 009004C8- 009098D4- 00009264
$16V_{in}$	C3305284- 33005284- CC339284- 90339284- 09005284-AA339284- 55005284- C3A0C428- 339CC428- CCA30428- 099CC428- 90A30428- 559CC428- AAA30428- 339A5404- 559A5404- 099A5404- CCA59404- 90A59404- AAA59404- 330A3284- 330AC298- 090A3284- 090AC298
$17V_{in}$	A3305284- C5305284- 35005284- 99305284- C5A0C428- A3A0C428- A3A03404- 99A0C428- 350A3284- 350AC298- 350A5282- ACC50428- 90050428- AAC50428- AC559284- 359AA428- AC5302A8- 350CA2A8- ACCC0948- 35033252- 35933564- ACCC94D4- 359A5404- ACA59404
$18V_{in}$	00000248-00909952-009094D4-00909564-00990428-00099284- A5AAC948- 00900948- A5A0C428- A5305284- A550C2A8- A5CA2A8- A5393254- A5395252- A5C9C548
$19V_{in}$	CCA50428- 90A50428- AAA50428- 330A5284- 090A5284- 550A5284- C330C2A8- 330CC2A8- CC33CO2A8- 903302A8- 090CC2A8- 090CC2A8- 550CC2A8- 903302A4- AA3302A4- AA3302A8- 550CC2A8- 339AC428- 099AC428- 559AC428- CC359284- 90359284- AA359284
$20V_{in}$	A330C2A8- AC3302A8- C530C2A8- 350CC2A8- AC3302A8- A330C2A8- 350CC2A8- C530C2A8- 350A5284- ACA50428- 359AC428- AC359284
$21V_{in}$	00900548- 000902A8- 00009254- A530C2A8
$22V_{in}$	CC3502A8- 903502A8- AA3502A8- 330AC2A8- 090AC2A8- 550AC2A8
$23V_{in}$	AC3502A8- 350AC2A8- 35933554
$24V_{in}$	00909554- CAAC9554- 53935554

Capacitor discharging:

As can be seen in table 1.13, the maximum voltage levels at the output of this inverter in stages 1, 2, and 3 are $3V_{in}, 9V_{in}\ and\ 18V_{in}$. As a result, it gives us output waveform with maximum value of $24V_{in}$. In Figure 1.35, we can see some selected discharging path of different capacitors. It can be seen that V_{out} in (a), (b), (c), and (d) are equivalent to$1V_{in}, 8V_{in}, 16V_{in}, and\ 24V_{in}$.

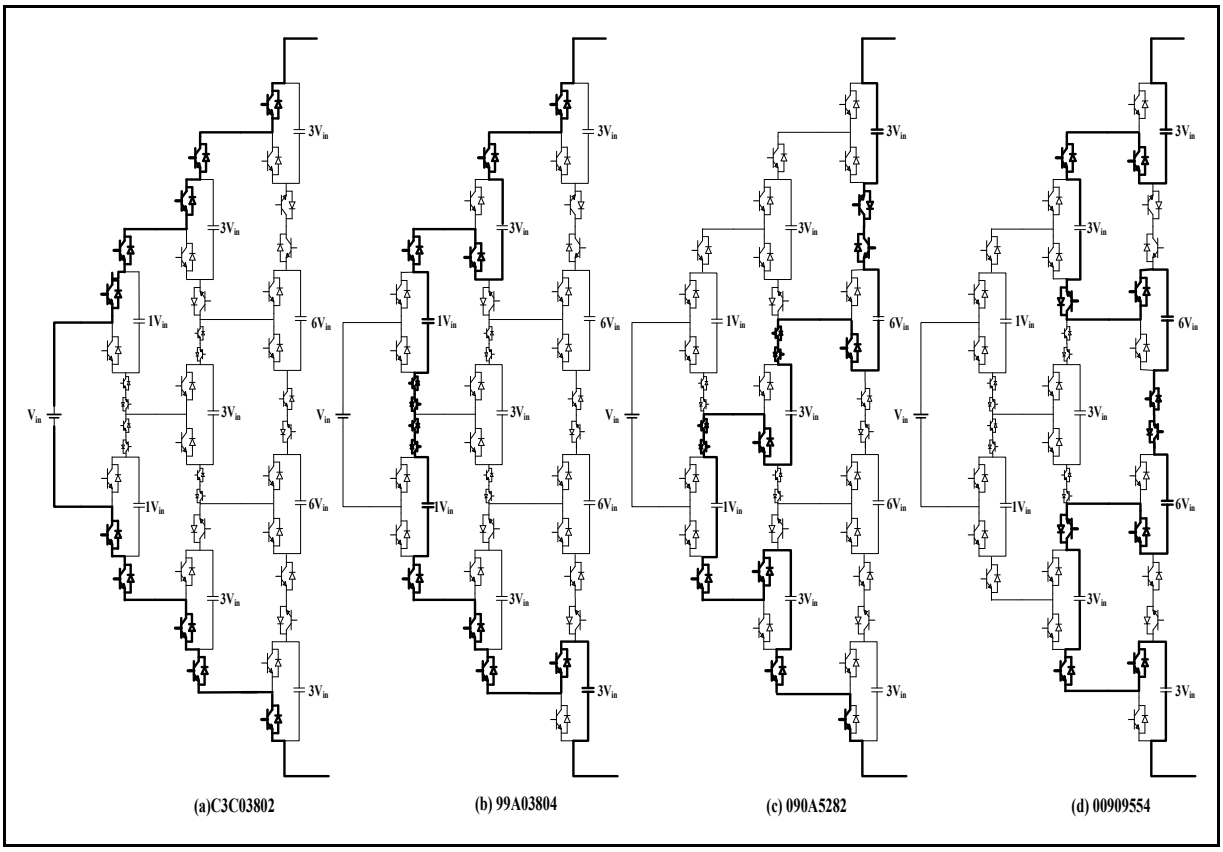


Figure 1.35 Some selected equivalent circuits for discharging capacitors

Table 1.14 Switching states for automatic charging and discharging
(charging ↑, discharging ↓, and no change -)

Levels	**Switching states($C_{11}, C_{12}, C_{21}, C_{22}, C_{23}, C_{31}, C_{32}, C_{33}, C_{34}$)**
$1V_{in}$	C3D03B02(--↓--↑---),C3C0B81A(----↓---↑),C3D0BB1A(--↓-↓↑--↑)
$2V_{in}$	DDC03802(↑↓-------),DDD0BB1A(↑↓↓-↓↑--↑),A3C0B81A(↓---↓---↑),DDD03B02(↑↓↓--↑---),BBD0BB1A(↓↑↓-↓↑--↑)
$3V_{in}$	A5C0B81A(↓↓--↓---↑),A5D03B02(↓↓↓--↑---),530C3302(↑----↓---),CAC39802(-↑--↓----),CAD30B18(-↑↓--↑--↓)
$4V_{in}$	C3C0B41A(----↓↓--↑),C3C9B8CC(---↓↓--↑↓),C9D05B02(--↓-↓↑---),AAC39802(↓↑--↓----),AAD30B1C(↓↑↓--↑--↓)
$5V_{in}$	C5C998CC(-↓-↓↓--↑-),A3D05B02(↓-↓-↓↑---),C5D03B04(-↓↓--↑--↓),C3A0B 81A(-↓↓-↓---↑),DDCOB41D(↑↓--↓↓--↑)
$6V_{in}$	A5B0B8E2(↓↓↓-↑----),A5D0D8E2(↓↓↑-↓----),A5C0B41A(↓↓--↓↓--↑),A5C9B8CC(↓↓-↓↓-↑↓),A5D05B02(↓↓↓-↓↑---)
$7V_{in}$	BAA30818(↓↑↓-----↓),5D9A3B02(↑↓↓↓-↑---),5D9AD81A(↑↓↓↓↓---↑),5D0AB31A(↑↓-↓↓↓--↑),C3A9B8CC(--↓↓↓--↑-)
$8V_{in}$	BBD05B04(↓↑↓-↓↑--↓),350AB31A(-↓-↓↓↓--↑),ACD59B1A(↓-↓↓↓↑--↑),BBC9B4CC(↓↑-↓↓↓-↑↓),DDA9B8CC(↑↓↓↓↓--↑↓)
$9V_{in}$	A539C318(↓↓-↑-↓--↓),A5D0D4E2(↓↓↑-↓↓---),A5B0B8E4(↓↓↓-↑---↓),A5A9B8CC(↓↓↓↓↓--↑↓),5C999B1A(↑-↓↓↓↑--↑)
$10V_{in}$	C3A9B4CC(--↓↓↓↓-↑↓),BAD59B04(↓↑↓↓↓↑--↓),5D9AB41A(↑↓↓↓↓↓--↑),BBD59B04(↓↑↓↓↓↑--↓),BAD30B28(↓↑↓--↑-↓↓)
$11V_{in}$	BBA9B4CC(↓↑↓↓↓↓-↑↓),ACD30B28(↓-↓--↑-↓↓),DD30B29A(↑↓--↓↓↓-↑),350CB29A(-↓--↓↓↓-↑),ACD59B04(↓-↓↓↓↑--↓)
$12V_{in}$	5C999662(↑-↓↓↓↓↑--),3A9998CC(-↑↓↓↓--↑↓),A5B9D662(↓↓↓↑↓↓↑--),A5B9D8CC(↓↓↓↑↓--↑↓),A5D0CB28(↓↓↓--↓-↓-),
$13V_{in}$	BAD50B28(↓↑↓↓-↑-↓↓),5D9A5B04(↑↓↓↓↓↑--↓),BAA5941A(↓↑↓↓↓↓--↑),5D0AB2AA(↑↓-↓↓↓↓-↑),BAD50B28(↓↑↓↓-↑-↓↓)
$14V_{in}$	ACD50B28(↓-↓↓-↑-↓↓),350AB29A(-↓-↓↓↓↓-↑),ACA5941A(↓-↓↓↓↓--↑),359A5B04(-↓↓↓↓↑--↓),DDB0CB28(↑↓↓--↑-↓↓)

Levels	Switching states($C_{11}, C_{12}, C_{21}, C_{22}, C_{23}, C_{31}, C_{32}, C_{33}, C_{34}$)
$15V_{in}$	A5B9D404(↓↓↓↑↓↓--↓),A5B9D664(↓↓↓↑↓↓↑-↓),A5B9D4CC(↓↓↓↑↓↓-↑↓),3A09929A(-↑-↓↓↓↓-↑),A5B9CB28(↓↓↓↑-↑-↓↓)
$16V_{in}$	5D9ACB28(↑-↓↓-↑-↓↓),BA35929A(↓↑-↓↓↓↓-↑),5D9A5404(↑↓↓↓↓↓--↓),BAA59404(↓↑↓↓↓↓--↓),5D933B52(↑↓↓--↑↓↓-)
$17V_{in}$	359ACB28(-↓↓↓-↑-↓↓),AC35929A(↓--↓↓↓↓-↑),35933B52(-↓↓--↑↓↓-),DDA0C428(↑↓↓--↓-↓↓),BB305284(↓↑--↓↓↓-↓)
$18V_{in}$	A539C248(↓↓-↑-↓↓↓↓),A550C2E8(↓↓↑--↓↓↓↓),A530A2E8(↓↓--↑↓↓↓↓),5C990668(↑-↓↓-↓↑↓↓),3A0992CC(-↑-↓↓↓↓↑↓)
$19V_{in}$	BA359284(↓↑-↓↓↓↓-↓),5D9AC428(↑↓↓↓-↓-↓↓),5D933B14(↑-↓--↑↓↓↓),BACC955A(-↑--↓↓↓↓↑)
$20V_{in}$	35933B54(-↓↓--↑↓↓↓),ACCC955A(↓---↓↓↓↓↑),DD30C2A8(↑↓---↓↓↓↓),BB30C2A8(↓↑---↓↓↓↓)
$21V_{in}$	3A900548(-↑↓--↓↓↓↓),5C900548(↑-↓--↓↓↓↓),5C90955A(↑-↓-↓↓↓↓↑),A539C2A8(↓↓-↑-↓↓↓↓),3A909B54(-↑↓-↓↑↓↓↓)
$22V_{in}$	5D933554(↑↓↓--↓↓↓↓),BACC9554(↓↑--↓↓↓↓↓),5D0AC2A8(↑↓-↓-↓↓↓↓)
$24V_{in}$	5C909554(↑-↓-↓↓↓↓↓),3A909554(-↑↓-↓↓↓↓↓)

Automatic charging and discharging of this model:

Table 1.14 indicates the switching state possibility of this topology. In this topology, while some capacitors are discharging, other capacitors are charging; therefore, it does not need any additional circuits for voltage balancing of capacitors. In this table, it can be seen that at least one capacitor is charging and the rest are discharging in each voltage level. Figure 1.36 illustrates some selected equivalent circuits for charging and discharging capacitors. Figure 1.37 indicates the output waveform and the reference waveform of this inverter.

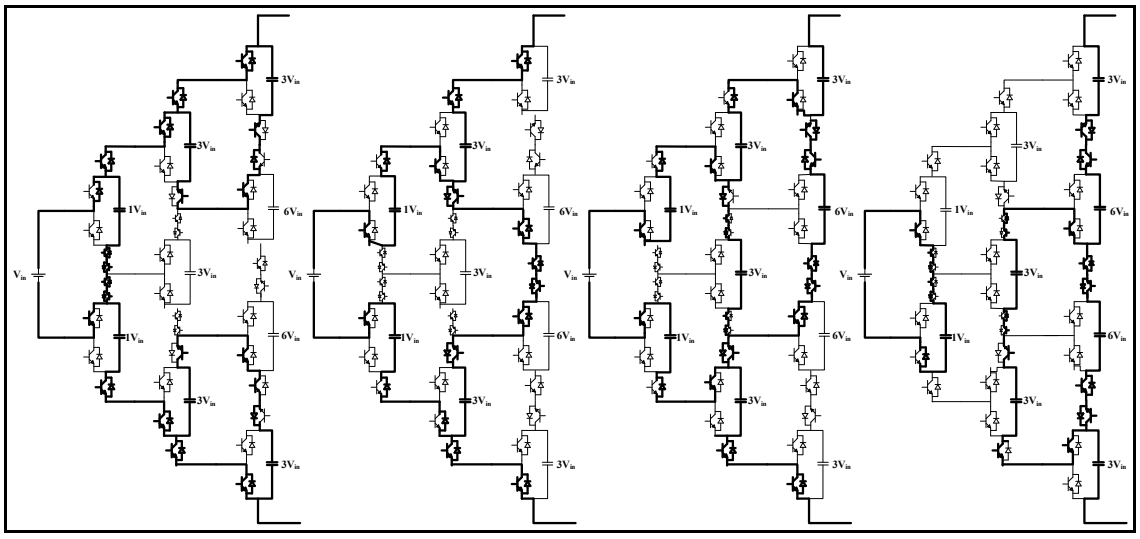


Figure 1.36 Some selected equivalent circuits for charging and discharging capacitors

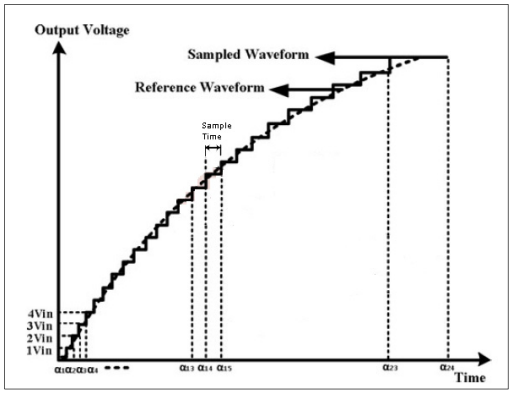


Figure 1.37 Output waveform
Taken from Taghvaie et al (2016)

Pros and Cons of this model are as per below:

Advantage:

- It has single dc source.
- It has self-balancing capacitors.
- Transformer and inductors are not bulky.
- Additional circuit in order to achieve voltage balancing of capacitors is not needed.
- It has a low number of components in comparison with other topologies.

Disadvantage

- The components' rating is kept in an acceptable commercial range.

1.7.4 Seven-Level PWM Inverter Employing Series-Connected Capacitors Paralleled to a Single DC Voltage Source

Increasing the usage of multilevel-inverter in high voltage and high-power applications in industry has made output quality of these inverters a big concern. As a result, many new topologies are proposed in order to solve the power quality problems. Although most of these inverters have Satisfactory THD, low-voltage stress and no bulky filters, they face some practical problems, such as having a lot of components that increase the cost of inverters, voltage balancing problem, complicated modules as well as modulation techniques, and bulky capacitors, etc. Figure 1.38 indicates the circuit of proposed inverter(Choi & Kang, 2015). It decreases the number of components; however, it raises the output voltage levels. It has one dc source, three capacitors, three switches, two diodes for synthesizing output level circuit and four switches for H-bridge circuit.

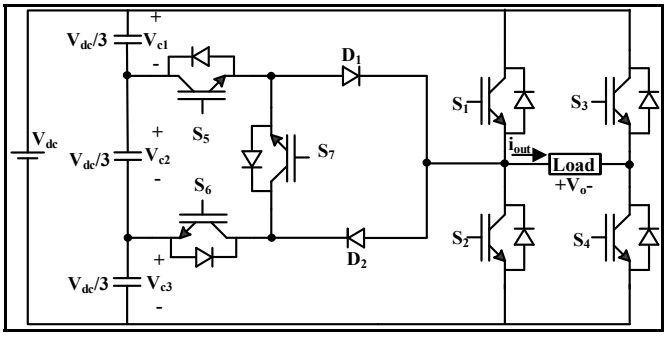


Figure 1.38 Main circuit

Circuit configuration:

Three identical capacitors are connected to each other in series and they are connected to a DC voltage source. Each capacitor is charged to $\frac{V_{DC}}{3}$. Firstly, for analysis purpose, it is assumed that all the components are ideal. This topology can generate seven levels of voltage, i.e.

V_{DC} , $\frac{2V_{DC}}{3}$, $\frac{V_{DC}}{3}$, 0, $\frac{-V_{DC}}{3}$, $\frac{-2V_{DC}}{3}$, $-V_{DC}$. Switches in H-bridge circuit (S1, S2, S3, S4) produce the highest and lowest voltage level, i.e. (V_{DC} , $-V_{DC}$), and other switches (S5, S6, S7) help to generate other voltage levels at output, i.e. $\frac{2V_{DC}}{3}$, $\frac{V_{DC}}{3}$, 0, $\frac{-V_{DC}}{3}$, $\frac{-2V_{DC}}{3}$.

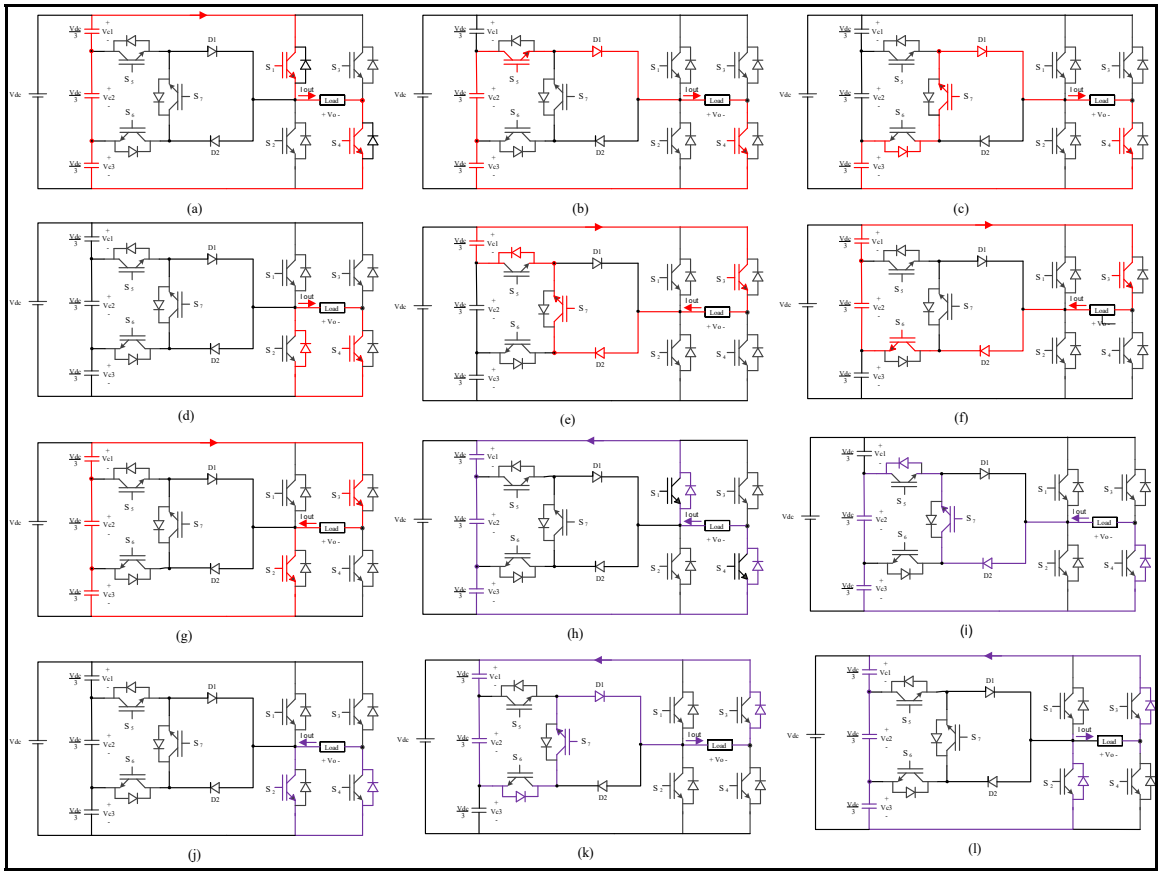


Figure 1.39 Equivalent circuit of each switching state for generating different output levels (a): $V_{out} = V_{DC}$,(b): $V_{out} = \frac{2V_{DC}}{3}$,(c): $V_{out} = \frac{V_{DC}}{3}$,(d)$V_{out} = 0$,(e)$V_{out} = \frac{-V_{DC}}{3}$, (f)$V_{out} = \frac{-2V_{DC}}{3}$, (g)$V_{out} = -V_{DC}$, (h)V_{out}= opposite current flow at V_{DC} , (i)V_{out}= opposite current flow at $\frac{2V_{DC}}{3}$, (j)V_{out}= opposite current flow at 0 , (k)V_{out}= opposite current flow at $\frac{2V_{DC}}{3}$, (l)V_{out}= opposite current flow at V_{DC}

Generation of output levels:

Figure 1.39 shows load current path and generating each voltage level. It should be considered that red represents direct current flow and purple represents opposite current flow.

1. As can be seen in Figure 1.39(a), flowing current through S1, S2 switches and C1, C2, C3 capacitors generates voltage level V_{DC} at the output; in addition , the capacitors are charged if the load current is opposite and also the load is inductive according to Figure 1.39(h).
2. For generating voltage level with the value of $\frac{2V_{DC}}{3}$ based on Figure 1.39 (b), two capacitors (C2, C3), connected in series, supply output voltage, flowing current through S4, S5, and D1. If the load current is opposite, capacitors are charged as shown in Figure 1.39 (h).
3. To generate $\frac{V_{DC}}{3}$ level, only C3 supplies the output voltage. In this step, current flows through D_{S6} , S7,D1, S4 to feed output load as given in Fig.39(c). In the opposite direction, current flows through D2, S7, D_{S5} , C2, C3, and D_{S4} as given in Figure 1.39(i).
4. In this topology, two methods exist for generating zero levels at the output of the inverter. First, by turning S2 and S4 on at the same time, the current flows through S4 and D_{S2} and generates zero level as given in Figure 1.39 (d). Secondly, by turning S1 and S3 on simultaneously, the current flows. The opposite direction is shown in Figure 1.39 (j).
5. As can be seen in Figure 1.39 (e), for producing level$\frac{V_{DC}}{3}$, capacitor C1 supplies the output voltage level by flowing current through D2, S7, D_{S5} and S3, the opposite current is shown in Figure 1.39 (k).
6. Figure 1.39 (f) indicates how this topology achieves $-\frac{2V_{DC}}{3}$ level at the output. Capacitors C1 and C2 provide this voltage level. Figure 1.39 (l) shows the reverse current flow in this situation.
7. Like step 1, C1, C2, C3 produce $-V_{DC}$ for load at the output as shown in Figure 1.39(g) and its opposite Figure 1.39(l).

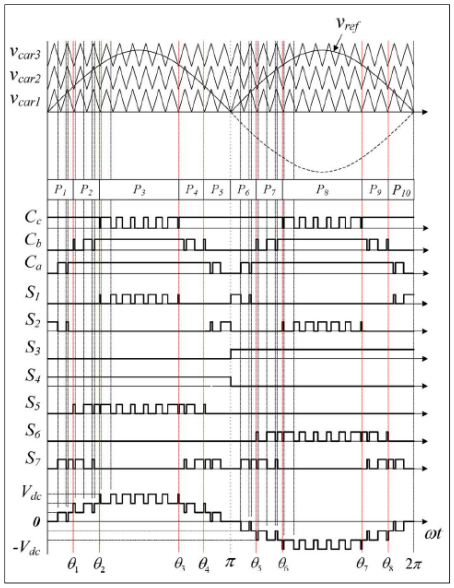


Figure 1.40 Switching pattern for generating 7-level PWM output voltage
Taken from Choi & Kang (2015)

Figure 1.40 and Table 1.15 ilustrate the switching pattern, switching states and output voltage shape for controling the proposed topology with PWM. Each cycle has been divided into 6 modes, which are written below. In these equations, P_n is the corresponding period for each mode.

Mode 1: P1 =0 < ωt < θ1 and P5 = θ4< ωt < π

Mode 2: P2 =θ1< ωt < θ2 and P4=θ3 < ωt < θ4

Mode 3: P3 =θ2 < ωt < θ3

Mode 4: P6 =π< ωt< θ5 and P10=θ8< ωt < 2π

Mode 5: P7 =θ5< ωt < θ6 and P9=θ7< ωt < θ8

Mode 6: P8 =θ6 < ωt < θ7.

By logical combination of *Ca*, *Cb*, *Cc*, and *Pn*,

$S1 = \overline{C_a} \cdot (P6 + P10) + \overline{C_c} \cdot P3$

$S2 = \overline{C_a} \cdot (P1 + P5) + \overline{C_c} \cdot P8$

$S3 = P6 + P7 + P8 + P9 + P10$

$S4 = P1 + P2 + P3 + P4 + P5$

$S5 = Cb \cdot (P2 + P4) + Cc \cdot P3$

$S6 = Cb \cdot (P7 + P9) + Cc \cdot P8$

$S7 = Ca \cdot (P1 + P5 + P6 + P10) + \overline{C_b} \cdot (P2 + P4 + P7 + P9)$.

Table 1.15 Switching states and output voltage levels

Comparison	Command			Switching Signal							Output
	C_a	C_b	C_c	S_1	S_2	S_3	S_4	S_5	S_6	S_7	V_{out}
$V_{car1} > V_{ref}$ $V_{car2} > V_{ref}$ $V_{car3} > V_{ref}$	0	0	1		1		1				0
$V_{car1} < V_{ref}$ $V_{car2} > V_{ref}$ $V_{car3} > V_{ref}$	1	0	1				1			1	$\frac{V_{DC}}{3}$
$V_{car1} < V_{ref}$ $V_{car2} < V_{ref}$ $V_{car3} > V_{ref}$	1	1	1				1	1			$\frac{2V_{DC}}{3}$
$V_{car1} < V_{ref}$ $V_{car2} < V_{ref}$ $V_{car3} < V_{ref}$	1	1	0		1		1				V_{DC}
$V_{car1} > V_{ref}$ $V_{car2} > V_{ref}$ $V_{car3} > V_{ref}$	0	0	1	1		1					0
$V_{car1} < V_{ref}$ $V_{car2} > V_{ref}$ $V_{car3} > V_{ref}$	1	0	1			1				1	$\frac{-V_{DC}}{3}$
$V_{car1} < V_{ref}$ $V_{car2} < V_{ref}$ $V_{car3} > V_{ref}$	1	1	1			1			1		$\frac{-2V_{DC}}{3}$
$V_{car1} < V_{ref}$ $V_{car2} < V_{ref}$ $V_{car3} < V_{ref}$	1	1	0		1	1					$-V_{DC}$

Table 1.16 shows the switching angle considering $M_a = \frac{A_m}{3A_c}$ and $V_{out} = M_a \sin \omega t$,

$$when \begin{cases} M_a < 0.33\,, & V_{out}\ has\ three\ levels \\ 0.33 \le M_a \le 0.66\,, & V_{out}\ has\ five\ levels \\ M_a > 0.66, & V_{out}\ has\ seven\ levels \end{cases} \quad (1.9)$$

Table 1.16 Switching angles

$\boldsymbol{\theta_n}$	$\boldsymbol{M_a < 0.33}$	$\boldsymbol{0.33 < M_a < 0.66}$	$\boldsymbol{M_a > 0.66}$
θ_1	$\frac{\pi}{2}$	$\sin^{-1}(\frac{A_c}{A_m})$	$\sin^{-1}(\frac{A_c}{A_m})$
θ_2	$\frac{\pi}{2}$	$\frac{\pi}{2}$	$\sin^{-1}(\frac{2A_c}{A_m})$
θ_3	$\frac{\pi}{2}$	$\frac{\pi}{2}$	$\pi - \theta_2$
θ_4	$\frac{\pi}{2}$	$\pi - \theta_1$	$\pi - \theta_1$
θ_5	$\frac{3\pi}{2}$	$\pi + \theta_1$	$\pi + \theta_1$
θ_6	$\frac{3\pi}{2}$	$\frac{3\pi}{2}$	$\pi + \theta_2$
θ_7	$\frac{3\pi}{2}$	$\frac{3\pi}{2}$	$2\pi - \theta_2$
θ_8	$\frac{3\pi}{2}$	$2\pi - \theta_1$	$2\pi - \theta_1$

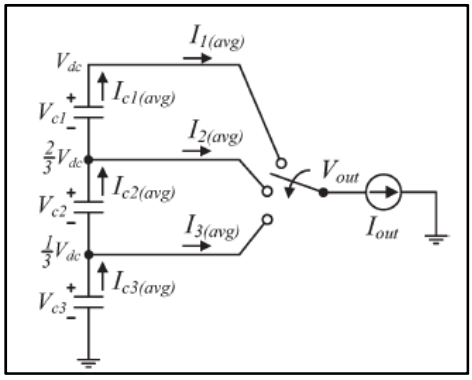


Figure 1.41 Equivalent circuit of the proposed mode
Taken from Choi & Kang (2015)

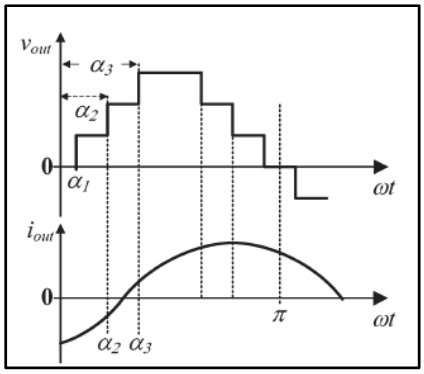


Figure 1.42 Output voltage and lagging load current
Taken from Choi & Kang (2015)

Figure 1.41 simplifies the circuit of proposed model for better understanding, and Figure 1.42 indicates operational waveform. In order to control voltage balancing, a new switching pattern has been introduced. The main objective of this switching pattern is controlling, discharging and charging of capacitor C_2 because it is located between C_1 and C_3, and the charging and discharging current of them should flow through capacitor C_2. Figure 1.43 shows this new control method for regulating C_2 through comparing V_{ref} and carrier wave V_{car2}. Figure 1.44 illustrates two carriers with different amplitudes. The following equation also shows the amplitude range.

$$\mathrm{v_{car1-max}} = \mathrm{v_{car2-min}} \leq \Delta \mathrm{v_{car2}} \leq \mathrm{v_{car2-max}} = \mathrm{v_{car3-max}} \qquad (1.10)$$

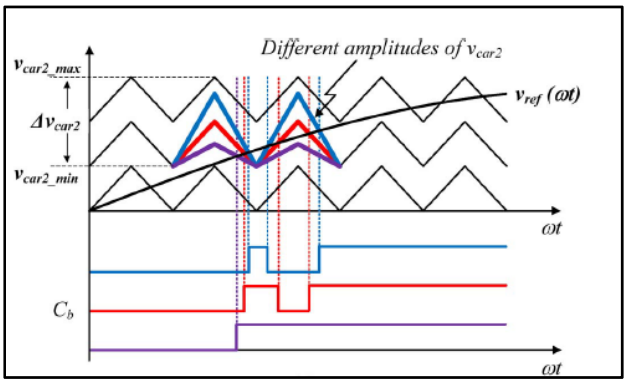


Figure 1.43 Modified control methods for regulating C_2
Taken from Choi & Kang (2015)

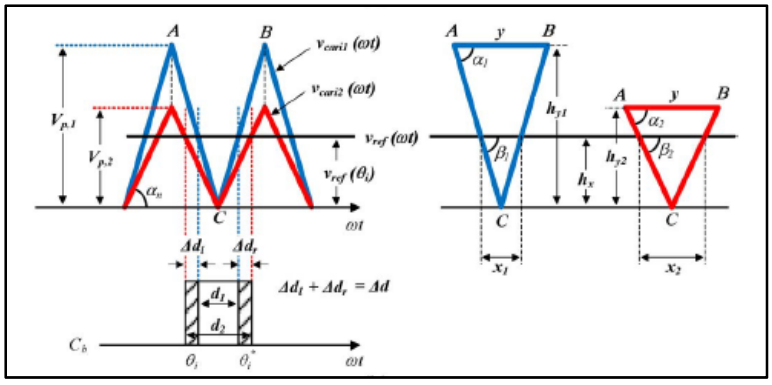


Figure 1.44 Relation between v_{car1}, v_{car2} and V_{ref}
Taken from Choi & Kang (2015)

Advantage:

- This topology is able to produce more voltage levels at the output with a low number of components.
- It works efficiently, hence
- It is a suitable substitution for conventional inverters.

Disadvantage:

- It has a complicated switching pattern

1.7.5 Multilevel inverter with combined T-type and cross-connected modules

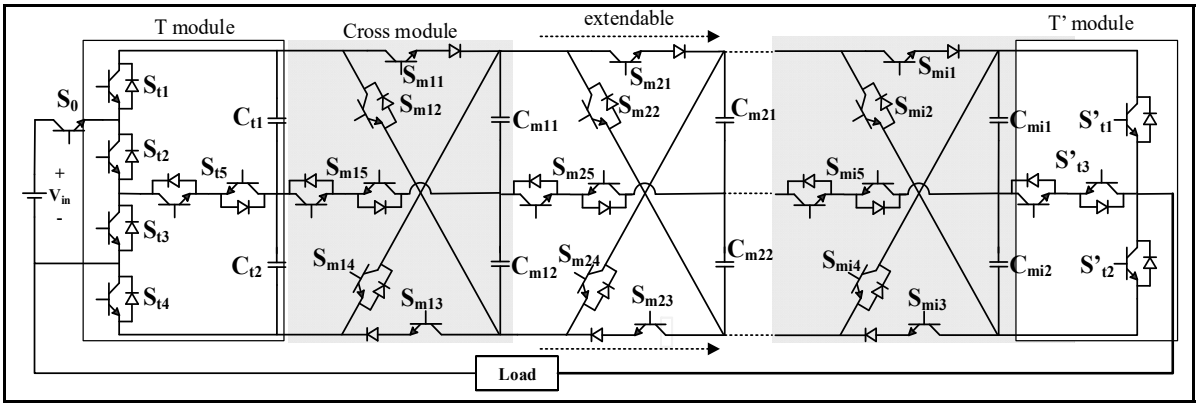


Figure 1.45 Circuit of combined T-type and cross-connected modules

Figure 1.45 shows the general structure of MLI with combined T-type and cross-connected modules (Khenar, Taghvaie, Adabi, & Rezanejad, 2018), in order to produce 2N+1-level voltages at the output, N capacitors, 3N+5 switches, and 2.5N+4 drivers are needed as blocking voltage. Firstly, in T-module, all switches are blocked at V_{in} except for S_{t4}, which is blocked at $2V_{in}$. Secondly, in T-module, all switches are blocked at $2V_{in}$ except for S'_{t3}, which is blocked at $2V_{in}$. Finally, for CM switches, S_{m1j}, S_{m3j},S_{m5j} are blocked at $2V_{in}$, and S_{m2j} as well as S_{m4j} are blocked at $4V_{in}$.This topology consists of three modules, two T-shape modules at both its end sides and there are some cross modules between these two. Naming the switches is in a way that in switch S_{mij}, i is module number and j is switches' number. Cross modules are used for boosting output AC voltage to the N time of input DC. As a result, $\left[\frac{N}{2}-1\right]$ cross module is needed.

Operating principal:

Figure 1.46 illustrates the structure of proposed thirteen-level inverter and Table 1.17 indicates its switching state.

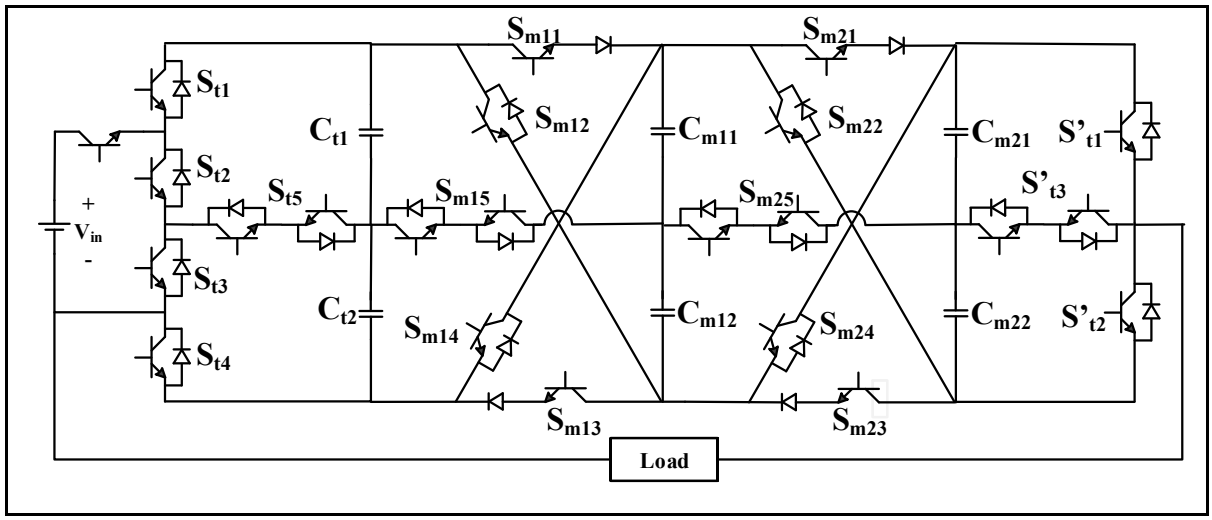


Figure 1.46 Equivalent circuit of thirteen-level proposed inverter

Table 1.17 Switching states of thirteen-level proposed inverter

	TM	CM_1	CM_2	TM'	
S_0	$S_{t1}S_{t2}S_{t3}S_{t4}S_{t5}$	$C_{m11}C_{m12}C_{m13}C_{m14}C_{m1}$	$C_{m21}C_{m22}C_{m23}C_{m24}C_{m2}$	$S'_{t1}S'_{t2}S'_{t3}$	V_{out}
1	10101	10001	10001	001	0
	01011	00101	00101	010	0
0	11100	00001	10001	001	$+V_{dc}$
				010	$+2V_{dc}$
			00010	100	$+2V_{dc}$
				001	$+3V_{dc}$
				010	$+4V_{dc}$
		01000	00010	001	$+V_{dc}$
				010	$+2V_{dc}$
			00001	001	$-V_{dc}$
				100	$-2V_{dc}$
			01000	010	$-2V_{dc}$
				001	$-3V_{dc}$
				100	$-4V_{dc}$
		00010	01000	010	$+2V_{dc}$
			00001	001	$+3V_{dc}$
			00010	100	$+4V_{dc}$
				001	$+5V_{dc}$
				010	$+6V_{dc}$
	00101	00010	01000	010	$+V_{dc}$
			00001	001	$+2V_{dc}$
				010	$+3V_{dc}$
			00010	100	$+3V_{dc}$
				001	$+4V_{dc}$
				010	$+5V_{dc}$
		00001	00010	100	$+V_{dc}$
				001	$+2V_{dc}$
				010	$+3V_{dc}$
			00001	010	$+V_{dc}$
				100	$-V_{dc}$
			01000	010	$-V_{dc}$
				001	$-2V_{dc}$
				100	$-3V_{dc}$
		01000	00010	100	$-V_{dc}$
			00001	001	$-2V_{dc}$
				100	$-3V_{dc}$
			01000	010	$-3V_{dc}$
				001	$-4V_{dc}$
				001	$-5V_{dc}$

	TM	CM_1	CM_2	TM'	
S_0	$S_{t1}S_{t2}S_{t3}S_{t4}S_{t5}$	$C_{m11}C_{m12}C_{m13}C_{m14}C_{m1}$	$C_{m21}C_{m22}C_{m23}C_{m24}C_{m2}$	$S'_{t1}S'_{t2}S'_{t3}$	V_{out}
0	00010	00010	00001	001	$+V_{dc}$
				010	$+2V_{dc}$
			00010	100	$+2V_{dc}$
				001	$+3V_{dc}$
				010	$+4V_{dc}$
			01000	001	$-V_{dc}$
				100	$-2V_{dc}$
		00001	00001	001	$-V_{dc}$
				100	$-2V_{dc}$
			01000	010	$-2V_{dc}$
				001	$-3V_{dc}$
				100	$-4V_{dc}$
		01000	00010	100	$-2V_{dc}$
			01000	010	$-4V_{dc}$
				001	$-5V_{dc}$
				100	$-6V_{dc}$

This topology has two operational modes: 1) Start-up mode 2) Discharging mode.

Start-up mode:

The start-up mode consists of two states. First, charging top capacitors in parallel with CD source (Figure 1.47). Second, charging bottom capacitors in parallel with DC source (Figure 1.48). In this mode, capacitors are charged to V_{in}; as a result, zero voltage in the output is achieved. Switches S_{mi1}, S_{mi3},$S_{mi5}$are on in this mode.

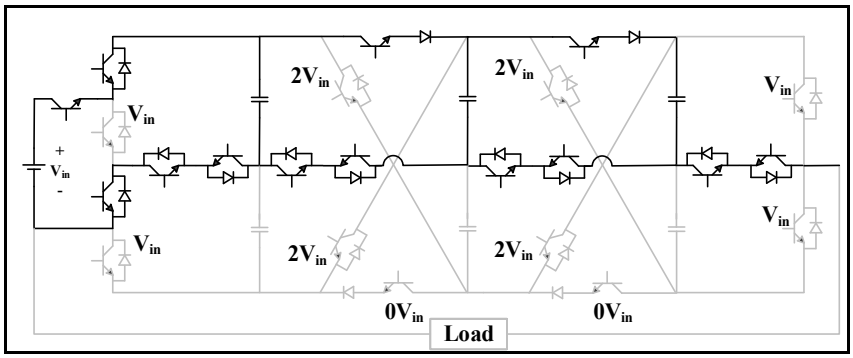


Figure 1.47 Charging of top capacitors

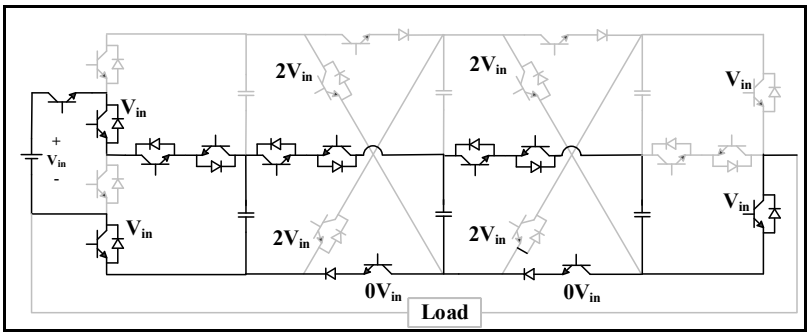


Figure 1.48 Charging of bottom capacitors

Discharge mode:

As can be seen in table 1.17 lots of redundant switching states exist in this topology, these switching states help to decrease the voltage stress of switches while the capacitors are discharging. Figure 1.49 shows one selected switching state for each voltage level.

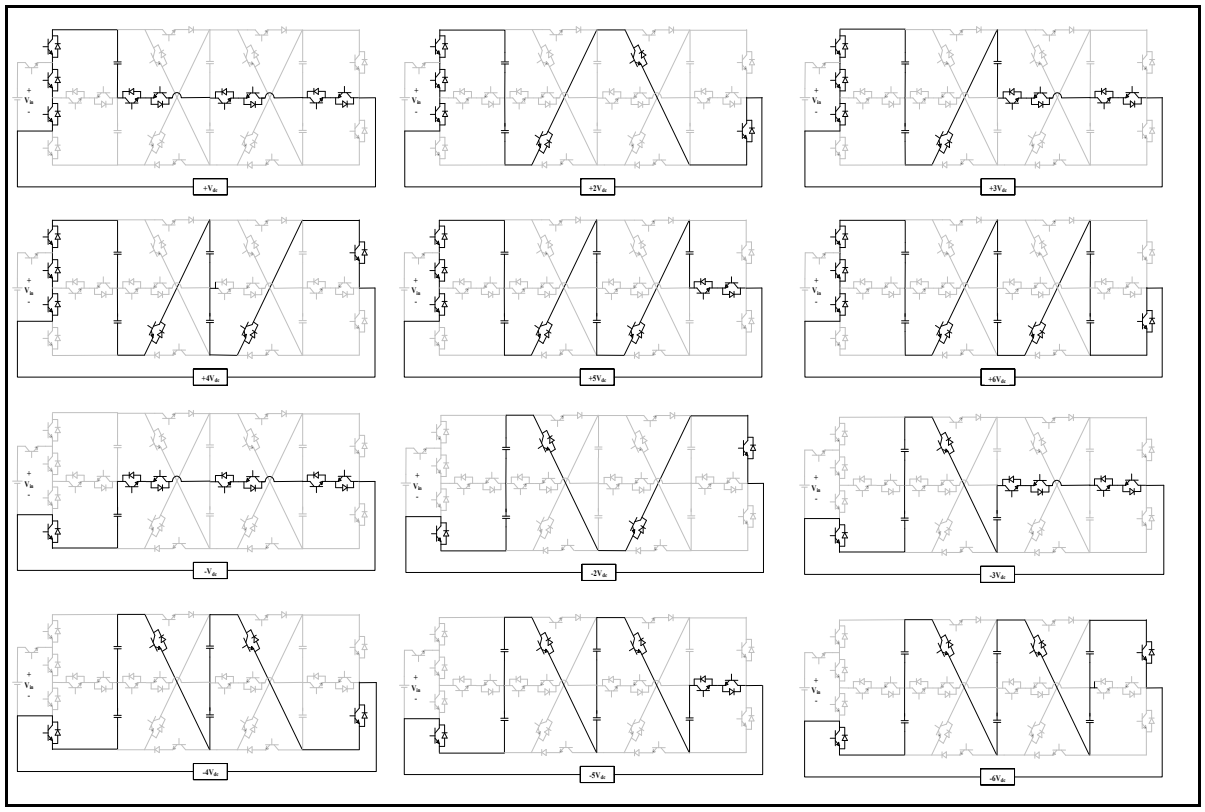


Figure 1.49 Equivalent circuit for discharging capacitors in some selected switching states

Control method:

Figure 1.50 shows multilevel staircase output waveform for one cycle. By selecting the number of inserted capacitors in this topology, 2N+1 levels of voltage are produced; furthermore, the selected harmonic order can be mitigated by changing switching angles ($\beta_1, \beta_2, \dots, \beta_n$) to the proper value.

In general, based on Fourier transformation, all periodic signals can be written as:

$$V(\omega t) = \alpha_0 + \sum_1^{\infty}(a_n \cos(n\omega t)) \tag{1.11}$$

In which ω is the output voltage angular frequency and n is harmonic orders. For odd function of Figure 1.50, $a_0 = a_n = 0$. Hence, this equation can be written as:

$$V(\omega t) = \sum_{n=1}^{\infty} b_n \sin(n\omega t) \tag{1.12}$$

As for a quarter-symmetric staircase voltage waveform with N switching angles, b_n can be defined as:

$$b_n = \begin{cases} 0 & n = even \\ \frac{4E}{n\pi}\sum_{k=1}^{N} P_K \cos(n\beta_k) & n = odd \end{cases} \tag{1.13}$$

SHM-pulse-width modulation (PWM) should be performed in a way that the selection of switching angles results in reducing harmonic orders up to a certain value (L_n). Thus, solving the following equation leads to achieving switching angles.

$$\begin{cases} H_1 = |b_1 - m_a| \le L_1 \\ H_n = \frac{1}{|b_1|}\frac{4}{n\pi}\sum_{k=1}^{N} \cos(n\beta_k) \le L_n \qquad \forall n = 3,5,7,9,\dots,49 \end{cases} \tag{1.14}$$

Where:

1. $m_a$is the modulation index.

2. To gain a waveform with N switching angles, harmonic orders of $n = 3, 5, 7, 9, 11, \ldots, 2N-1$ will be mitigated.

3. For switching angles constraint of $0 \leq \beta_1 \leq \beta_2 \leq \ldots \leq \beta_n$ is applied.

4. $E \cdot P_K = 1PU$, where P_K is voltage amplitude's coefficient.

5. E, which is the voltage of each level of staircase voltage waveform, is equal to input DC voltage (Vin) in the proposed circuit.

Solving the following objective function leads to calculating switching angles in order to achieve SHM-PWM objectives.

$$OF(\beta_1, \ldots, \beta_i) = {}_{n=1,5,7,\ldots,49}C_n(H_n)^2 \tag{1.15}$$

C_n coefficients show the significance of low harmonic orders reduction in objective function. As a result, it can be written:

$$C_1 > C_5 > \cdots > C_{49} \tag{1.16}$$

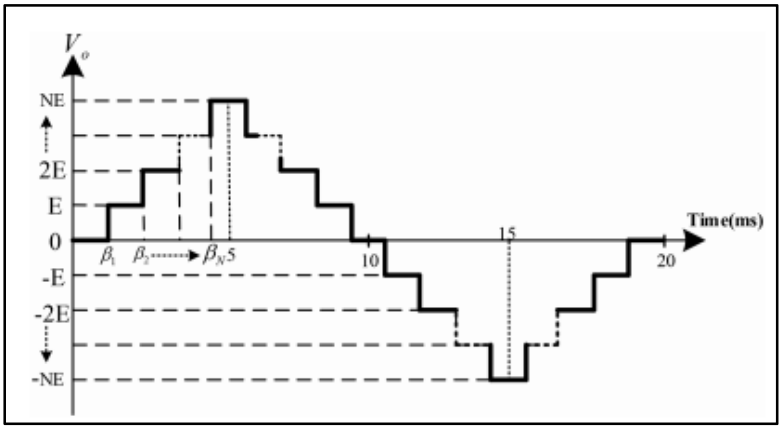


Figure 1.50 Multi-level output waveform
Taken from Khenar et al (2018)

On the basis of the mentioned analysis, for a 13-level inverter, six switching angles are offered by SHM-PWM so as to mitigate harmonic orders of 3, 5, 7, 9 and 11 as illustrated in Table 1.18.

Table 1.18 Six switching angles for proposed 13-level inverter

Angles	β_1=4.86	β_2=14.4	β_3=24.57	β_4=35.64	β_5=48.51	β_6 = 66.42

Capacitor calculation:

Figure 1.51 illustrates the charging time for each capacitor in this topology; in addition, Table 1.19 illustrates coefficients K1 and K2 in each voltage level.

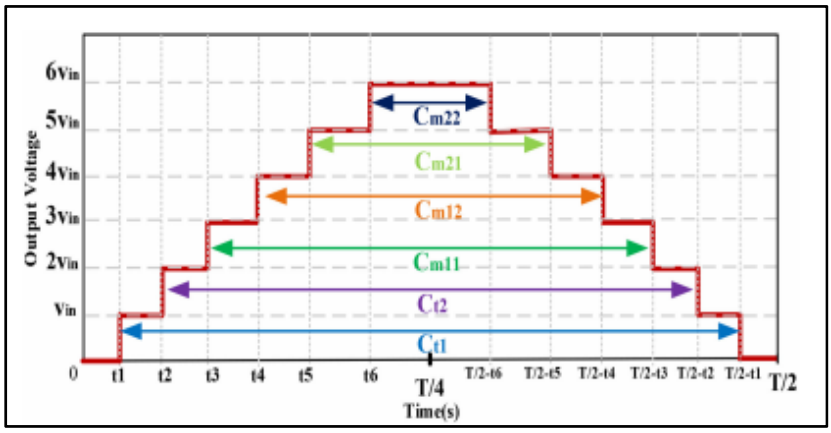


Figure 1.51 Discharging time of different capacitors
Taken from Khenar et al (2018)

Table 1.19 Coefficients K_1 and K_2 for each voltage level

Output voltage level, V_{in}	**K_1**	**K_2**
+1	2	4
+2	2	2
+3	2	3
+4	1	3
+5	1	5
+6	0	6
-1	3	2
-2	3	1
-3	3	3
-4	3	1
-5	4	1
-6	4	0

Advantages:

- It is expandable for generating high-voltage levels without increasing circuit component ratings.
- No bulky capacitor and transformer are needed.
- It produces bipolar output without using h-bridge inverter.
- It has self-balancing capacitors.
- It is single-DC-source.
- It is able to operate output HF.

Disadvantages:

- Keeping the rate of semiconductors and other components in commercial rate is difficult.

1.7.6 Single-Phase Single-Source 7-Level Inverter with Triple Voltage Boosting Gain

Circuit configuration of this topology is shown in Figure 1.52(Lee, 2018). This topology consists of connecting three H-bridge inverters together in series with bidirectional voltage blocking switches in between. $S_5$and $S_{10}$are bidirectional voltage blocking switches consisting of two series MOSFET. It should be mentioned that right-end and left-end H-bridge are connected to floating capacitor and the middle one to DC source. In order to produce voltage levels, each capacitor is charged to the value of V_{dc} when it is connected with V_{dc} in parallel and discharged when it is connected to V_{dc} in series.

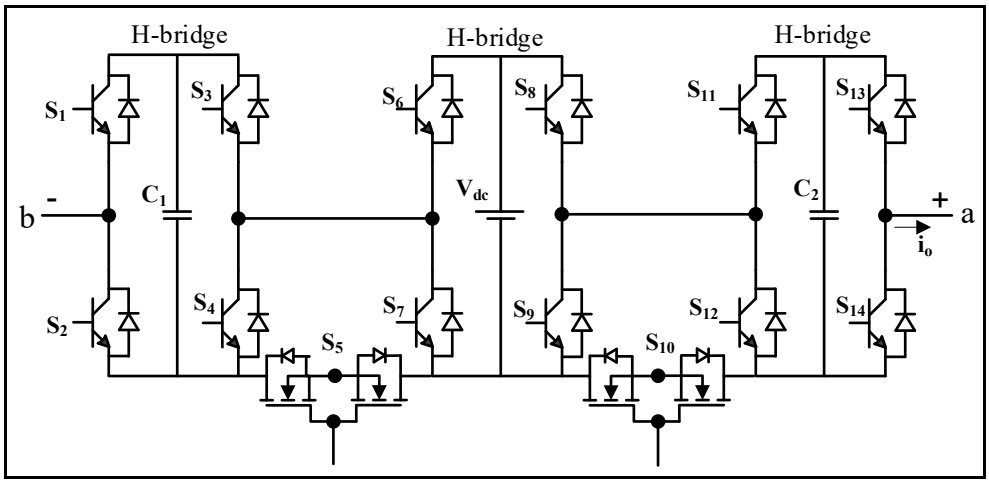


Figure 1.52 Single-Phase Single-Source 7-Level Inverter with Triple Voltage Boosting Gain

Table 1.20 illustrates the switching state possibility of this topology. In this topology, vertical switches are complimentary; therefore, only one switch from two complementary switches is shown in this table.

Table 1.20 Switching states possibility of this model

States	**S_1**	**S_3**	**S_5**	**S_6**	**S_8**	**S_{10}**	**S_{11}**	**S_{13}**	**Output Voltage**	**C1 Voltage**	**C2 Voltage**
1	0	1	1	1	1	1	1	1	0	Charging	Charging
2	0	1	1	1	1	1	1	0	$+V_{dc}$	Charging	Charging
3	0	1	1	1	1	0	0	0	$+2V_{dc}$	Charging	Discharging
4	0	1	0	0	1	0	0	0	$+3V_{dc}$	Discharging	Discharging
5	1	1	1	1	1	1	1	1	$-V_{dc}$	Charging	Charging
6	1	0	0	1	1	1	1	1	$-2V_{dc}$	Discharging	Charging
7	1	0	0	1	0	0	1	1	$-3V_{dc}$	Discharging	Discharging

Figure 1.53 indicates equivalent circuit of this topology in each state. Figure 1.54 shows output waveform of this topology. In this figure, φ is load angle, θ_1 is the angle of output voltage when output is equal to V_{dc}, θ_2 is the angle of output voltage when output is equal to $2V_{dc}$, and θ_3 is the angle of output voltage when output is equal to $3V_{dc}$. It can be seen in table 1.20 and Figure 1.54 that the capacitor C1 is charged for a longer period during positive half-cycle compared

with the negative half cycle; on the contrary, C2 is charged for a longer period during negative half-cycle compared with the positive half-cycle in negative half-cycle; consequently, during operation this topology will be automatically balanced.

By considering the discharging duration of capacitors i.e. from $(\pi + \theta_2)$ to $(2\pi - \theta_2)$ for C_1 and from θ_2 to $(\pi - \theta_2)$ for C_2, capacitor voltage ripple can be calculated with the following equation:

$$\Delta V_c = \frac{\sqrt{2}\, I_0 \cos\theta_2 (PF)}{\pi f_0 C} \tag{1.17}$$

Where:

I_0 is RMS of load current

f_0 is fundamental output frequency (50 or 60Hz)

PF= $\cos\varphi$

C=$C_1 = C_2$

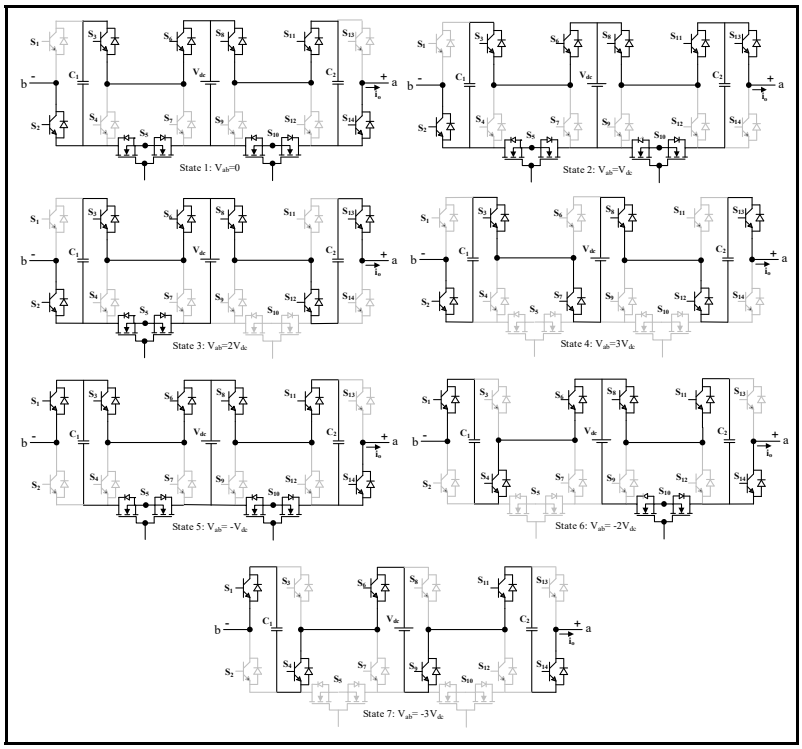


Figure 1.53 Equivalent circuit for each switching state

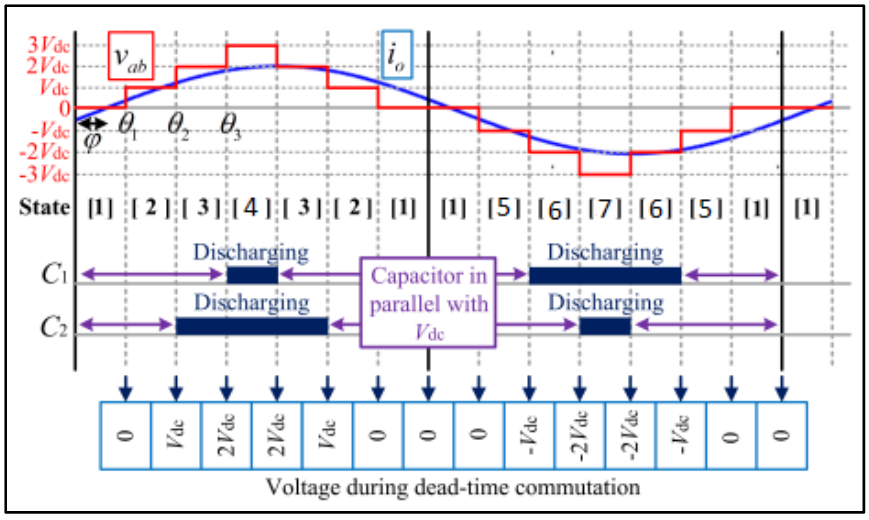


Figure 1.54 Output waveform
Taken from Lee (2018)

Advantage:

- It has single dc source.
- This inverter generates seven-level voltages.
- It has low-voltage stress on switches as V_{dc} in comparison with the other existing switched-capacitor MLI.
- Considering dead time, it has smooth communication with no voltage spike.
- It has high-voltage boosting gain.

Disadvantage:

- It needs 16 switches for generating seven-level voltage.

1.7.7 A Novel Step-Up Single Source Multilevel Inverter: Topology, Operating Principle and Modulation

Circuit configuration:

Figure 1.55 illustrates general Structure of this topology (Saeedian, Firouzjaee, Hosseini, Adabi, & Pouresmaeil, 2018). It can be seen that this topology consists of two half-bridge inverters on the right and left sides, marked with RHB and LHB in the figure plus m number

of switch capacitor cells in the middle, marked in the figure with SCC. Each SCC module consists of two unidirectional power switches (S_u, S_d), two capacitors (C_u, C_d), and two power diodes (D_u, D_d). One important advantage of this topology is voltage boosting to any desirable voltage at the output with single dc source and without using H-bridge at the output; therefore, this topology is suitable for medium and high-power applications.

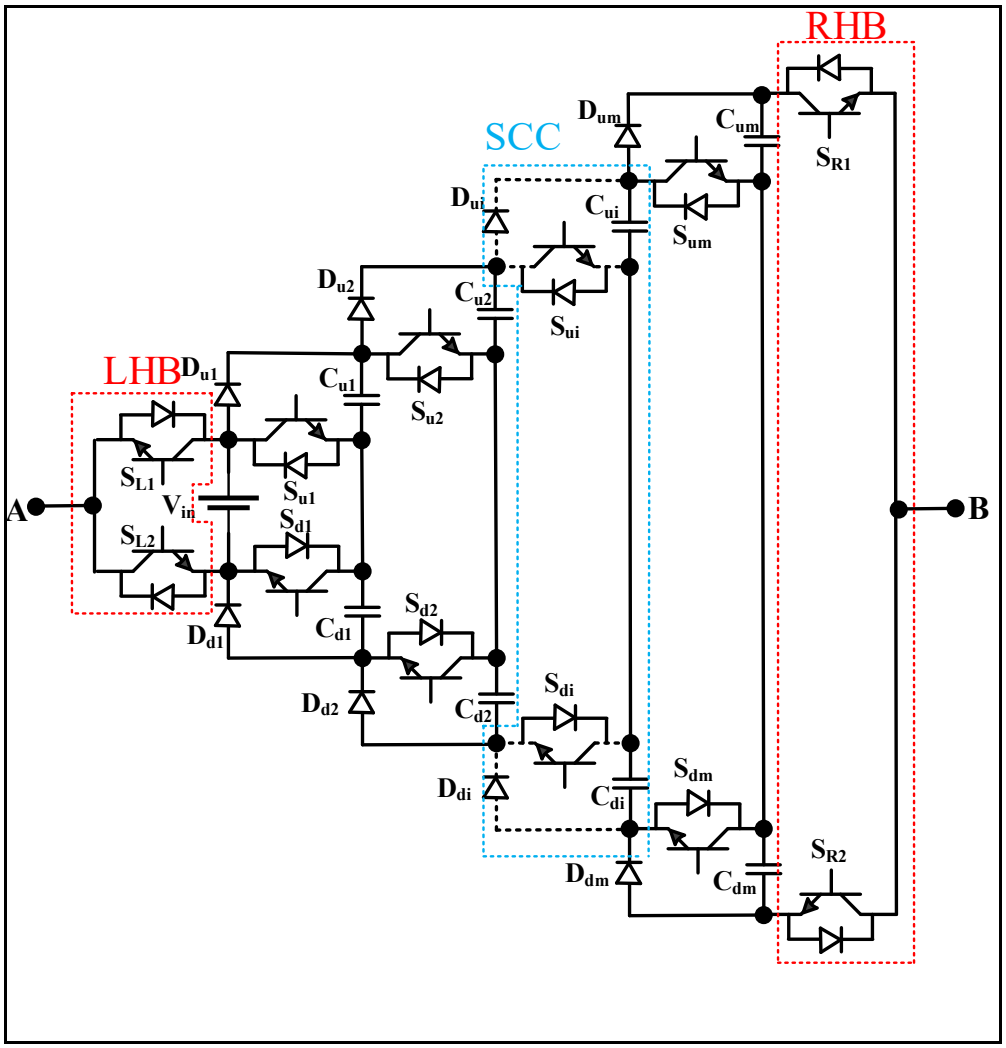


Figure 1.55 Circuit configuration of step-up single source MLI

Capacitors charging:

Red path in Figure 1.56 (a) illustrates charging path of C_{u1}. It can be seen that when S_{d1} is on, Vin charges C_{u1} via D_{u1} and S_{d1}.Similarly, blue dashed line box in Figure 1.56(b) indicates

charging path of C_{d1} by Vin via S_{u1} and D_{d1}. It must be mentioned that S_{u1} and S_{d1} are complimentary. In Figure 1.56 (b), red path shows charging route of C_{u2} and blue dashed line box presents charging path of C_{d2} in the second SCC. It can be seen that series mixture of first SCC capacitors charge C_{u2} and C_{d2}. To charge all capacitors, this process continues. Following equation can be used to calculate the voltage across each capacitor where m is the number of SCC:

$$V_{cui}=V_{cdi}=2^{m-1}*V_{in} \qquad i=1,2,\ldots,m$$

As demonstrated below, the capacitors are discharged across the load. In the proposed topology, closed loop controlling method or additional circuit balancer for voltage balancing of capacitor is not needed.

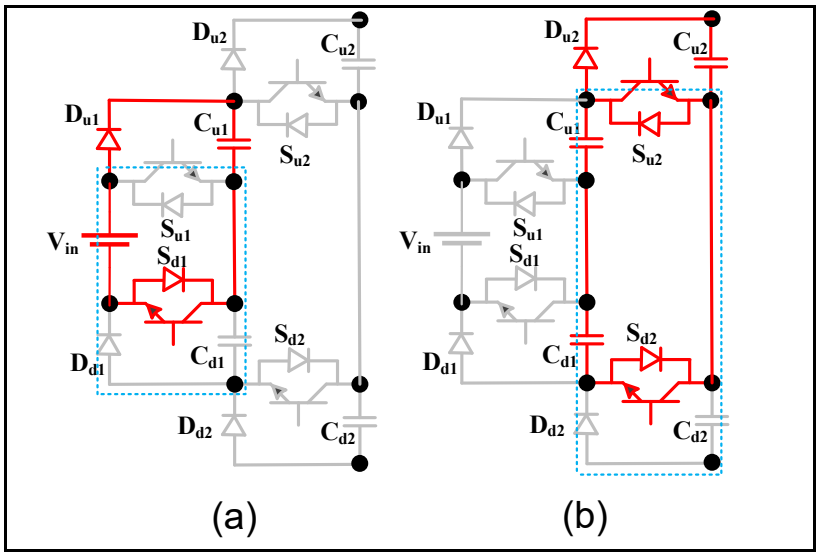


Figure 1.56 Charging paths of first SCC (b) charging path of second SCC

Operating Principles:

Switching model in Table 1.21 shows different voltage levels. It should be mentioned that 0 and 1 values represent OFF and ON states of the related semiconductors, in order. C, D, and - are indicative of charging, discharging and no changes modes, respectively. Possible current paths in the positive half cycle are shown in Figure 1.57.

Table 1.21 Switching states possibility of this model and Charging / Discharging

Voltage levels	Switches								Diodes				Capacitors			
	S_{L1}	S_{L2}	S_{u1}	S_{d1}	S_{u2}	S_{d2}	S_{R1}	S_{R2}	D_{u1}	D_{d1}	D_{u2}	D_{d2}	C_{u1}	C_{d1}	C_{u2}	C_{d2}
$+4V_{in}$	1	0	0	1	0	1	0	1	1	0	1	0	C	D	C	D
$+3V_{in}$	1	0	1	0	0	1	0	1	0	1	1	0	D	C	C	D
	0	1	0	1	0	1	0	1	1	0	1	0	C	D	C	D
$+2V_{in}$	1	0	0	1	1	0	0	1	1	0	0	1	C	D	-	C
	0	1	1	0	0	1	0	1	0	1	1	0	D	C	C	D
$+1V_{in}$	1	0	1	0	1	0	0	1	0	1	0	1	D	C	-	C
	0	1	0	1	1	0	0	1	1	0	0	1	C	D	-	C
0	0	1	1	0	1	0	0	1	0	1	0	1	D	C	-	C
	1	0	0	1	0	1	1	0	1	0	1	0	C	D	C	-
$-1V_{in}$	0	1	0	1	0	1	1	0	1	0	1	0	C	D	C	-
	1	0	1	0	0	1	1	0	0	1	1	0	D	C	C	-
$-2V_{in}$	0	1	1	0	0	1	1	0	0	1	1	0	D	C	C	-
	1	0	0	1	1	0	1	0	1	0	0	1	C	D	D	C
$-3V_{in}$	0	1	0	1	1	0	1	0	1	0	0	1	C	D	D	C
	1	0	1	0	1	0	1	0	0	1	0	1	D	C	D	C
$-4V_{in}$	0	1	1	0	1	0	1	0	0	1	0	1	D	C	D	C

Modulation Strategy:

In order to control semiconductor switches, a technique called phase disposition pulse width modulation is used. As shown in Figure 1.58, eight triangular carrier waves (V_{t1} to V_{t8}) are compared with a reference sinusoidal waveform (Vref) so as to produce switches' gate signal.

There is amplitude (A_t) and frequency (f_t) in carrier waves, and yet their offset voltages are different. The required switching pulses are generated by V_{t1} to V_{t4} (V_{t5} to V_{t8}) so as to form the positive (negative) half cycle.

Table 1.22 shows the algorithm determining on-state switches in each voltage level.

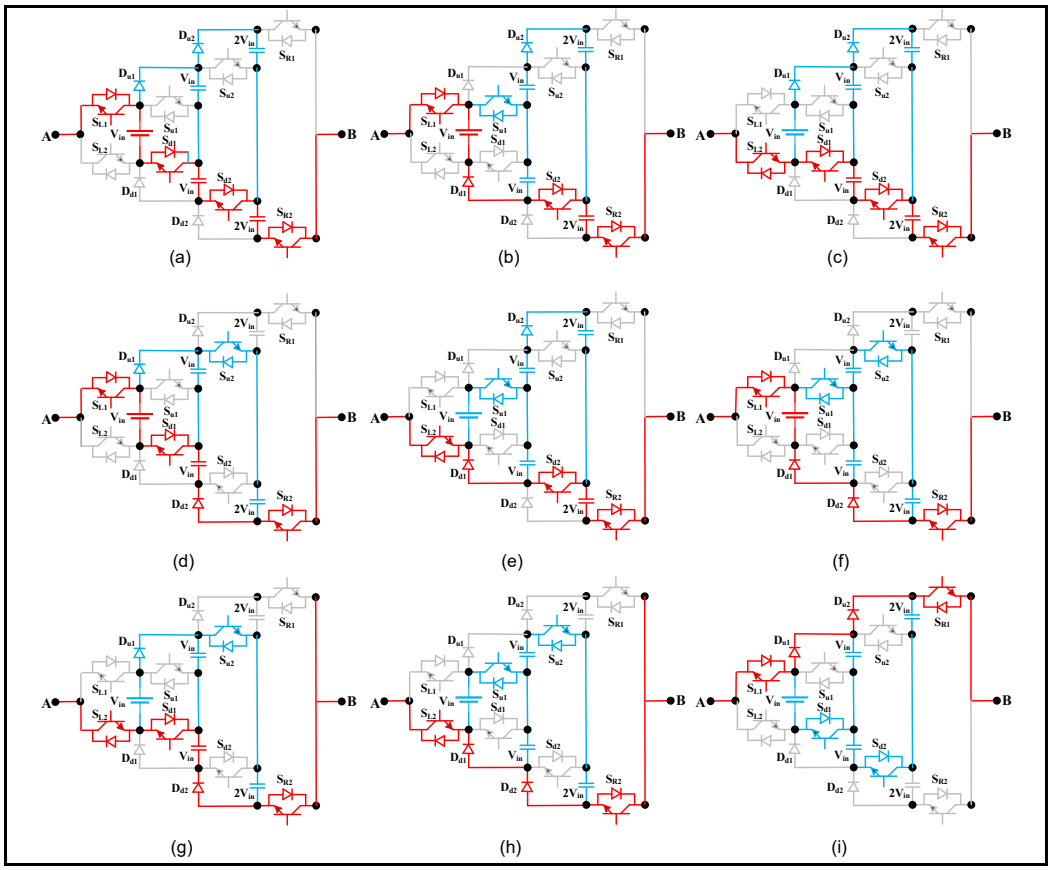


Figure 1.57 Current path of output voltage levels

Determination of capacitances:

Retaining the capacitors' voltage ripple in an acceptable level is necessary in switched-capacitor DC-AC converters. The range of fluctuation of capacitor voltage is inversely proportional to its capacitance, the period of discharging, and load value. The lower the ripple is, the lower the power loss and the higher the efficiency of the capacitor is. Table 1.21 shows two switching states for +3Vin(or -3Vin) leading to two different modes for C_{d1} and C_{u1}.When discharge time is maximum in the capacitance calculations, a worse case is considered. As for positive and negative half cycles, these intervals are t_4-t_3 and t_{10}-t_9 respectively, where C_{d1} and C_{u1} are discharged. Similarly, t_5-t_2 and t_{11}-t_8 are the maximum discharging intervals of C_{d2} and C_{u2}, respectively. As a result, each capacitor's maximum discharging value is as follows:

$$\Delta Q_c = \int_{t_a}^{t_b} I_{Loud} Sin(2\pi f_{ref}\, t)dt \qquad (1.18)$$

Where the discharging interval of each capacitor is$[t_a, t_b]$ and the maximum load current is I_{Loud}.

Calculations of t_2 to t_5 and t_8 to t_{10} are as follows:

$$t_2 = \frac{\sin^{-1}(2A_t/A_{ref})}{2\pi f_{ref}}, t_3 = \frac{\sin^{-1}(3A_t/A_{ref})}{2\pi f_{ref}}, t_4 = \frac{\pi - \sin^{-1}(3A_t/A_{ref})}{2\pi f_{ref}}, t_5 = \frac{\pi - \sin^{-1}(2A_t/A_{ref})}{2\pi f_{ref}} \quad (1.19)$$

$$t_8=\pi+t_2,\ t_9=\pi+t_3,\ t_{10}=\pi+t_4,\ t_8=\pi+t_2,\ t_{11}=\pi+t_5$$

in which f_{ref} and A_{ref} are the frequency and amplitude of reference waveform, in order. As a result, if K is the maximum ripple, which is acceptable, obtaining the capacitances is as follows:

$$C \geq \frac{\Delta Q_c}{kV_{IN}} \quad (1.20)$$

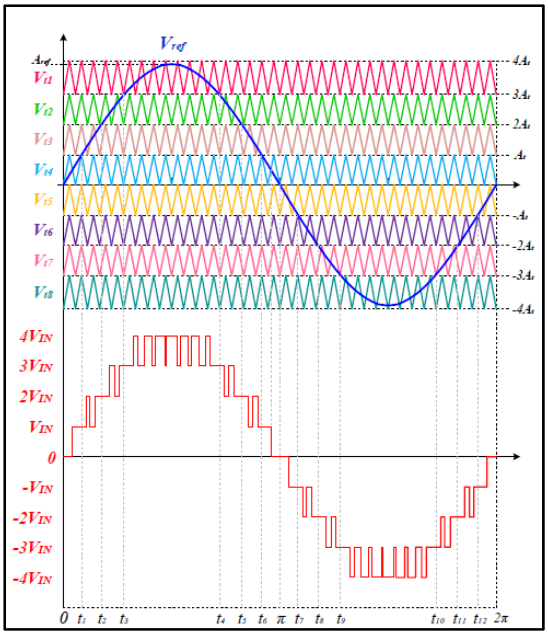


Figure 1.58 Modulation technique and output waveform of A Novel Step-Up Single Source MLI
Taken from Saeedian et al (2018)

Table 1.22 Switching states possibility of this model

Relationship between V_{ref} and V_{ti}	On state switches	Output Voltage
$V_{ref} > V_{t1}$	$S_{L1} - S_{d1} - S_{d2} - S_{R2}$	$+4V_{in}$
$V_{t2} < V_{ref} < V_{t1}$	$S_{L1} - S_{u1} - S_{d2} - S_{R2}$ $S_{L2} - S_{d1} - S_{d2} - S_{R2}$	$+3V_{in}$
$V_{t3} < V_{ref} < V_{t2}$	$S_{L1} - S_{d1} - S_{u2} - S_{R2}$ $S_{L2} - S_{u1} - S_{d2} - S_{R2}$	$+2V_{in}$
$V_{t4} < V_{ref} < V_{t3}$	$S_{L1} - S_{u1} - S_{u2} - S_{R2}$ $S_{L2} - S_{d1} - S_{u2} - S_{R2}$	$+1V_{in}$
$V_{t5} < V_{ref} < V_{t4}$	$S_{L2} - S_{u1} - S_{u2} - S_{R2}$ $S_{L1} - S_{d1} - S_{d2} - S_{R1}$	0
$V_{t6} < V_{ref} < V_{t5}$	$S_{L2} - S_{d1} - S_{d2} - S_{R1}$ $S_{L1} - S_{u1} - S_{d2} - S_{R1}$	$-1V_{in}$
$V_{t7} < V_{ref} < V_{t6}$	$S_{L2} - S_{u1} - S_{d2} - S_{R1}$ $S_{L1} - S_{d1} - S_{u2} - S_{R1}$	$-2V_{in}$
$V_{t8} < V_{ref} < V_{t7}$	$S_{L2} - S_{d1} - S_{u2} - S_{R1}$ $S_{L1} - S_{u1} - S_{u2} - S_{R1}$	$-3V_{in}$
$V_{ref} < V_{t8}$	$S_{L2} - S_{u1} - S_{u2} - S_{R1}$	$-4V_{in}$

1.7.8 Packed U-Cell (PUC) inverter

PUC inverter was invented in 2008 by Ounejjar and Al-Haddad as a seven-level inverter (Ounejjar & Al-Haddad, 2008), then they changed it in order to produce five-level (Vahedi, Labbé, & Al-Haddad, 2016), nine-level (Ounejjar & Al-Haddad, 2018), fifteen level (Ounejjar & Al-Haddad, 2010), etc. This topology is created by removing two switches from CHB and connecting two U-shaped cells together (Ounejjar et al., 2011). Figure 1.59 indicates one cell of PUC inverter. In comparison with other proposed inverters, PUC has the lowest number of switches while generating the highest number of voltage levels at the output; in addition, this topology is transformer less, it means that this inverter does not need transformers to generate and isolate the DC bus voltages. Indeed, in the multilevel inverters, DC sources must be isolated, which leads to the use of transformers. The PUC topology avoids this problem since these DC voltages can be interconnected; therefore, they can be regulated to the desired values. Figure 1.60 shows the single phase seven-level PUC inverter and Chart.7 indicates switching state of PUC inverter.

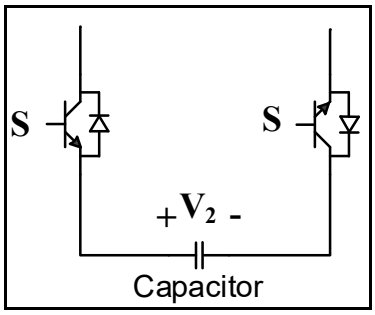


Figure 1.59 U-shaped cell

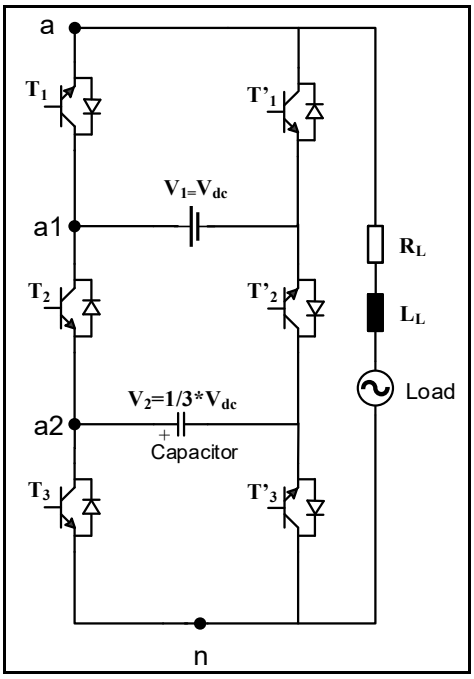


Figure 1.60 Single-phase PUC-7 inverter

The number of required power sources can be calculated with below equation where N_i is the number of voltage levels and Nc_i is the number of voltage sources and i is an integer:

$$N_i = 2^{Nc_i+1}\text{-}1 \tag{1.21}$$

Similarly, the number of required switches can be calculated with the following equation where Nsw_i is the number of switches:

$$N_i = 2^{\frac{Nsw_i}{2}}\text{-}1 \tag{1.22}$$

The PUC inverter topologies are classified according to the increase of produced voltage levels in Table 1.23. The voltage level to which each capacitor must be charged is given in this table. For example, the fifteen-level converter requires eight semi-conductors and three capacitors; furthermore, the voltage sources must be equal to V_{dc}, $V_{dc}\frac{3}{7}$ and $V_{dc}\frac{3}{7}$ respectively.

Figure 1.60 and Figure 1.61 illustrate single-phase and three-phase PUC-7 inverter and Figure 1.62 shows single phase thirty-one-level PUC inverter.

Table 1.23 DC voltages bus of the different converters of the PUC topology

Number of capacitors(Nc)	**Number of semi-conductors(Nsw)**	**Number of voltage levels (N)**	**V1**	**V2**	**V3**	**…**	**V(n-1)**	**Vn**
0	-	1	-	-	-	…	-	-
1	4	3	V_{dc}	-	-	…	-	
2	6	7	V_{dc}	$\frac{V_{dc}}{3}$	-	…	-	-
3	8	15	V_{dc}	$V_{dc}\frac{3}{7}$	$V_{dc}\frac{3}{7}$	…	-	-
. . .	. . .	. . .	. . .	. . .	. . .	… … …	. . .	. . .
$Nc_{(i-1)}$	$Nsw_{(i-1)}$	$N_{(i-1)}$	V_{dc}	$V_{dc}\frac{N_{(i-3)}}{N_{(i-2)}}$	$V_{dc}\frac{N_{(i-4)}}{N_{(i-2)}}$	…	$\frac{3Vdc}{N_{(i-2)}}$	$\frac{Vdc}{N_{(i-2)}}$
$Nc_i = Nc_{(i-1)}+1$	$Nsw_i = Nsw_{(i-1)} + 2$	$N_i = 2N_{i-1} + 1$	V_{dc}	$V_{dc}\frac{N_{(i-2)}}{N_{(i-1)}}$	$V_{dc}\frac{N_{(i-3)}}{N_{(i-1)}}$	…	$\frac{Vdc}{N_{(i-1)}}$	$\frac{3Vdc}{N_{(i-1)}}$

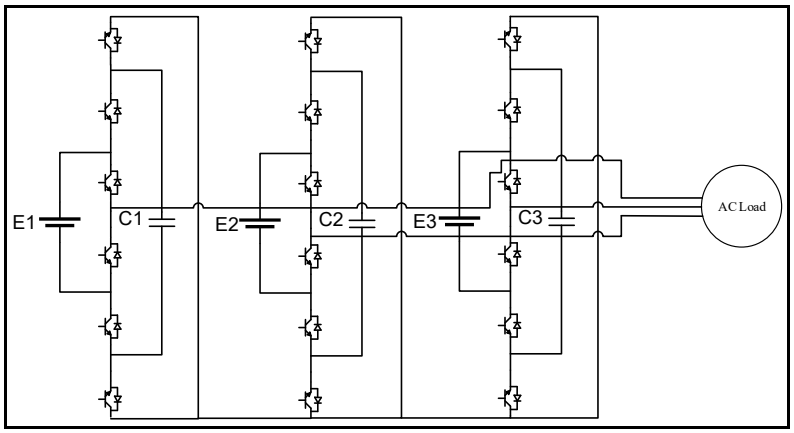


Figure 1.61 Three-phase PUC7 inverter

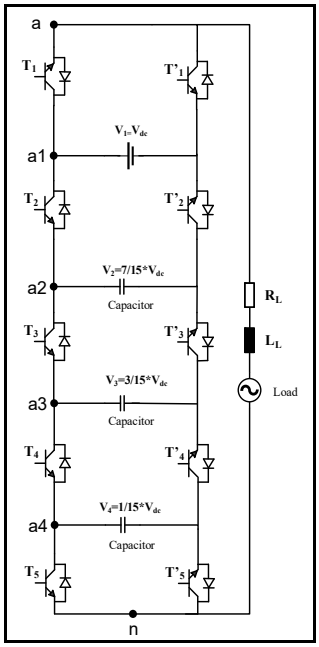


Figure 1.62 Thirty-one level transformerless PUC inverter

Operational mode:

The PUC7 inverter consists of six switches (see Figure 1.60). Each switch can only have two states, one state where it is blocked and another where it is saturated, which allows to reach (2^3) eight states including two redundant. Table 1.24 shows the five voltage levels produced according to the states of the switches. Figure 1.63 shows equivalent circuit of PUC inverter in each state of Table 1.24.

Table 1.24 Switching states of PUC5 MLI

States	S_1	S_2	S_3	Output Voltage	Vo	Capacitor Voltage
1	1	0	0	V_1	+2E	No effect
2	1	0	1	$V_1 - V_2$	+E	Charging
3	1	1	0	V_2	+E	Discharging
4	1	1	1	0	0	No effect
5	0	0	0	0	0	No effect
6	0	0	1	$-V_2$	-E	Discharging
7	0	1	0	$V_2 - V_1$	-E	Charging
8	0	1	1	$-V_1$	-2E	No effect

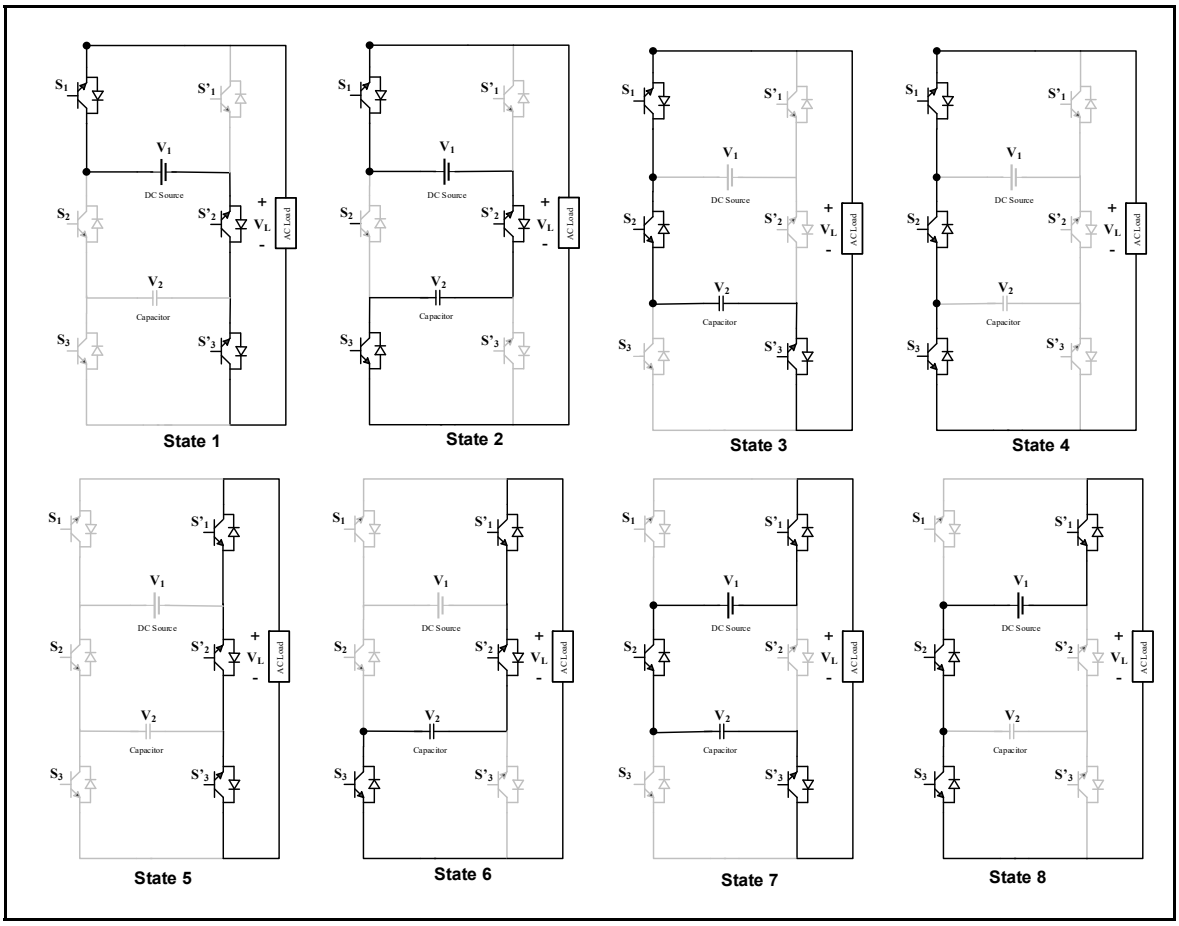


Figure 1.63 Equivalent circuit of each state in PUC7 or PUC5 inverter

Modulation:

By subdividing the desired sinusoid into six parts, three positive and three negative, and using the seven-level modulation, six signals can be generated. Some signals from the positive half cycle take the 1 or 2 values and the same for the negative alternation take the -1 or -2 values. The other signals will be 0 or 1 for the positive half and -1 or 0 for the negative half as shown in Figure 1.64. The sum of these signals results in a single signal, which will be noted with the letter S. This signal consists of eight levels corresponding to those desired for the output voltage. It should be said that there are two levels (2 and -2) that are redundant and refer to the zero voltage level (see Figure 1.65 and Table 1.25). The waveform of the signal S is given in Figure 1.66.

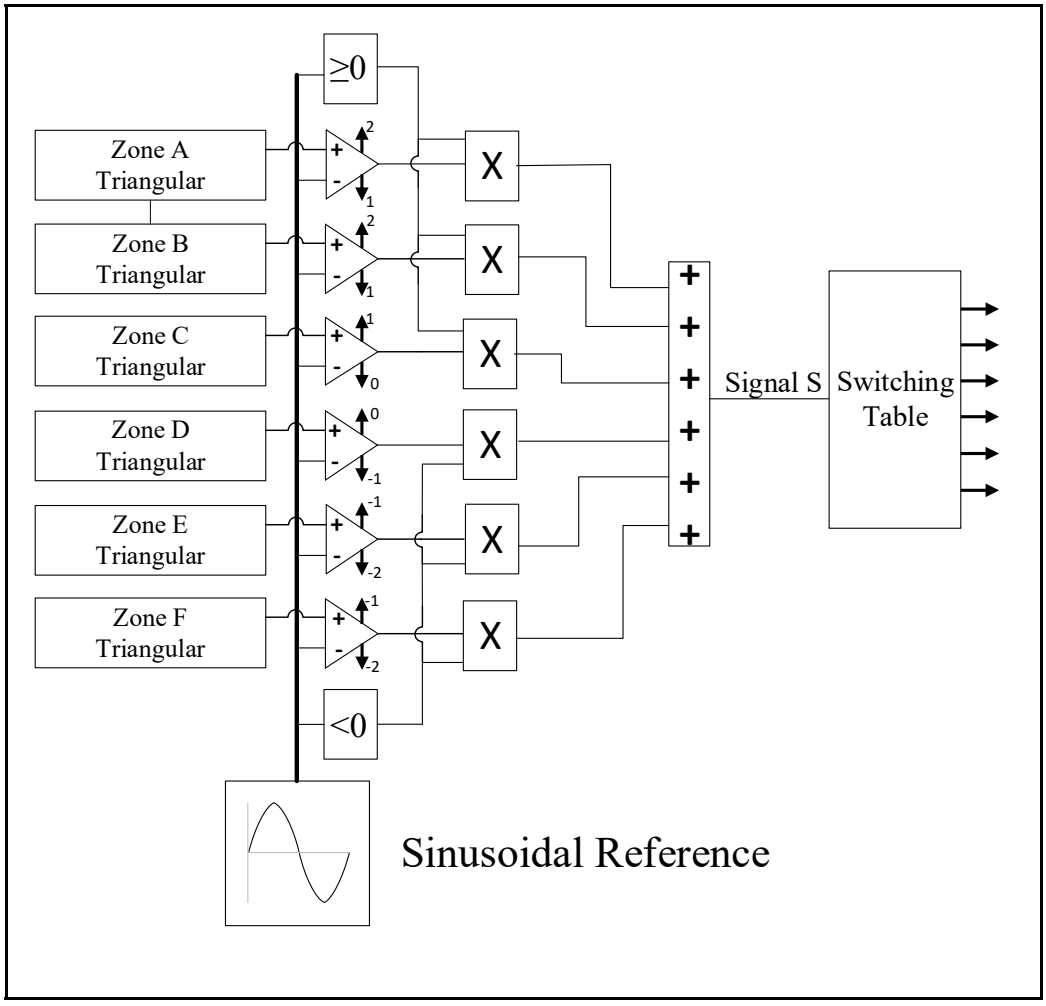


Figure 1.64 Modulation technique

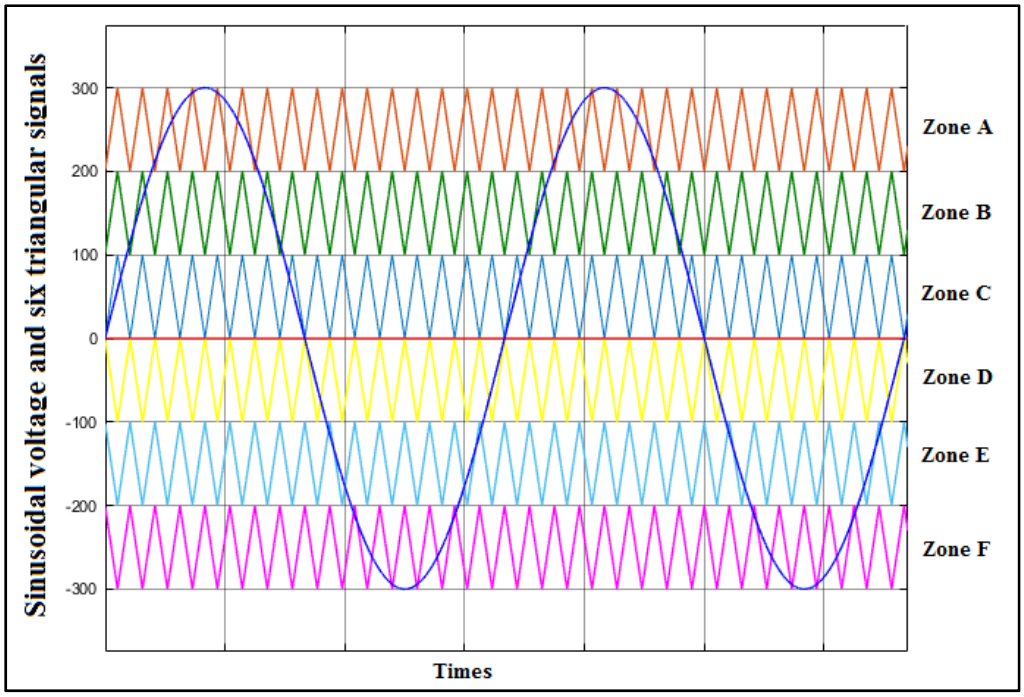


Figure 1.65 Seven-level sinusoidal PWM

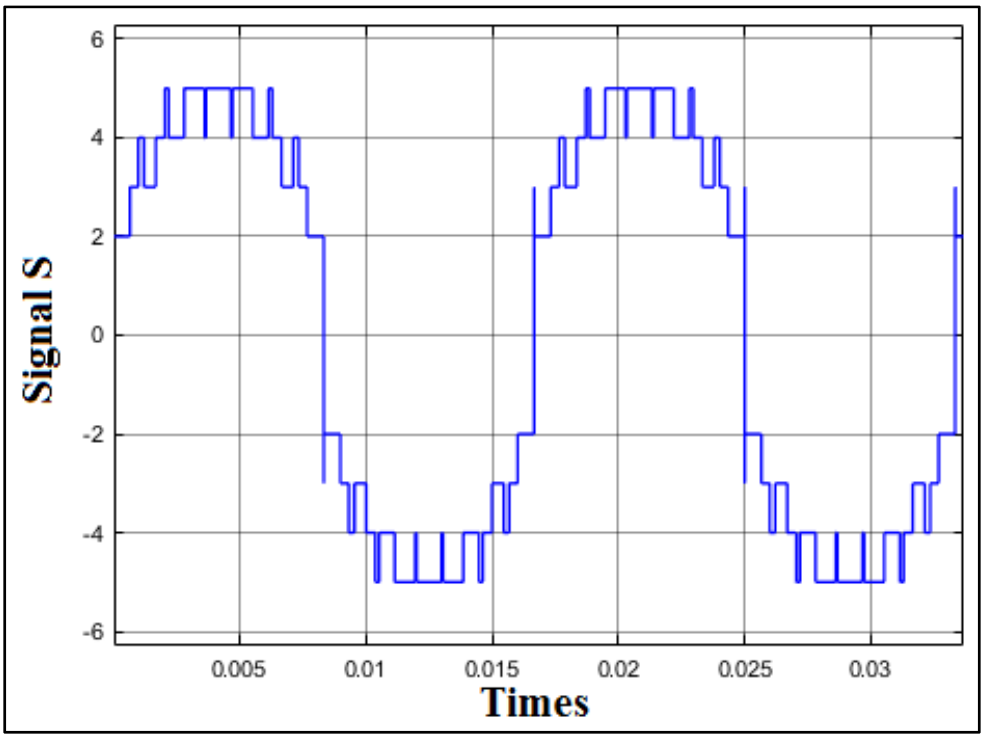


Figure 1.66 Waveform of signal S

Table 1.25 Correspondence table

State	Signal S	Produced voltage
1	5	V1
2	4	V1-V2
3	3	V2
4	2	0
4’	2-	0
5	3-	-V2
6	4-	V2-V1
7	5-	-V1

Advantage:

- Line current harmonic is reduced to less than 1%.
- Modulation frequency is very low, which increases the energy efficiency.
- There is a low number of components.
- Sizes of switches are reduced.
- Dynamic output voltages are very good, even under unbalanced loads.
- Very stable output voltages are generated.

Disadvantage:

- Design is complicated due to complex and high-switching frequency controllers to maintain the DC side capacitors at the desired level.
- Bulky capacitor is needed.

CHAPTER 2

CURRENT BASED MODEL PREDICTIVE CONTROL FOR DC CAPACITOR OPTIMIZATION IN GRID-CONNECTED AND STAND-ALONE NINE-LEVEL PACKED U-CELL INVERTER

2.1 Introduction

As is known among all MLIs, single DC source MLIs are more preferable in industry due to low cost of manufacturing. In first chapter, a few Single DC source inverters are reviewed. All of these MLIs have their own advantage and disadvantages. Among these topologies, PUC MLI makes it possible to avoid the excessive use of passive and active filters, which has a huge impact on reducing the cost as well as being energy-efficient. The PUC topology has a very good dynamic output voltage even with unbalanced loads. It is also very competitive since it uses a small number of components compared to the existing topologies, thereby avoids bulky installations. As a result, the PUC topology opens up a great future by offering the possibility of combination with other topologies, which have so far remained limited to three-level voltage inverters. In this chapter, the mathematical model of PUC9 is obtained, then model predictive control is applied on it. Finally, the applied control method is both validated with Matlab Simulink and experimentally.

2.2 Nine-level Packed U-Cell Inverter operation and modeling

Figure 2.1 illustrates PUC9 converter with two capacitors. This circuit is created by adding one U-shape cell to PUC7 topology (Ounejjar & Al-Haddad, 2010, 2018; Ounejjar et al., 2011). It is obvious that it consists of eight switches and two auxiliary capacitors, which work as DC sources. Each pair of horizontal switches must work complimentarily in order to prevent short circuit. Considering the fact that each switch has two operating status (saturated and blocked) and PUC9 has eight switches, there are 16 switching states. If we consider V_1=V_{dc}, V_2=$\frac{3V_{dc}}{7}$, and V_3= $\frac{V_{dc}}{7}$, this circuit is able to produce 15 output levels with only one redundant switching state. Besides, if we consider V_1=V_{dc}, V_2=$\frac{V_{dc}}{2}$, and V_3=$\frac{V_{dc}}{4}$, this circuit generates nine output

levels but with seven redundant states. These redundant switching states are used to balance the voltage of auxiliary capacitors in desired values. Table 2.1 indicates all possible switching states of this topology and Figure 2.2 depicts current path of PUC9 topology in each switching state of Table 2.1.

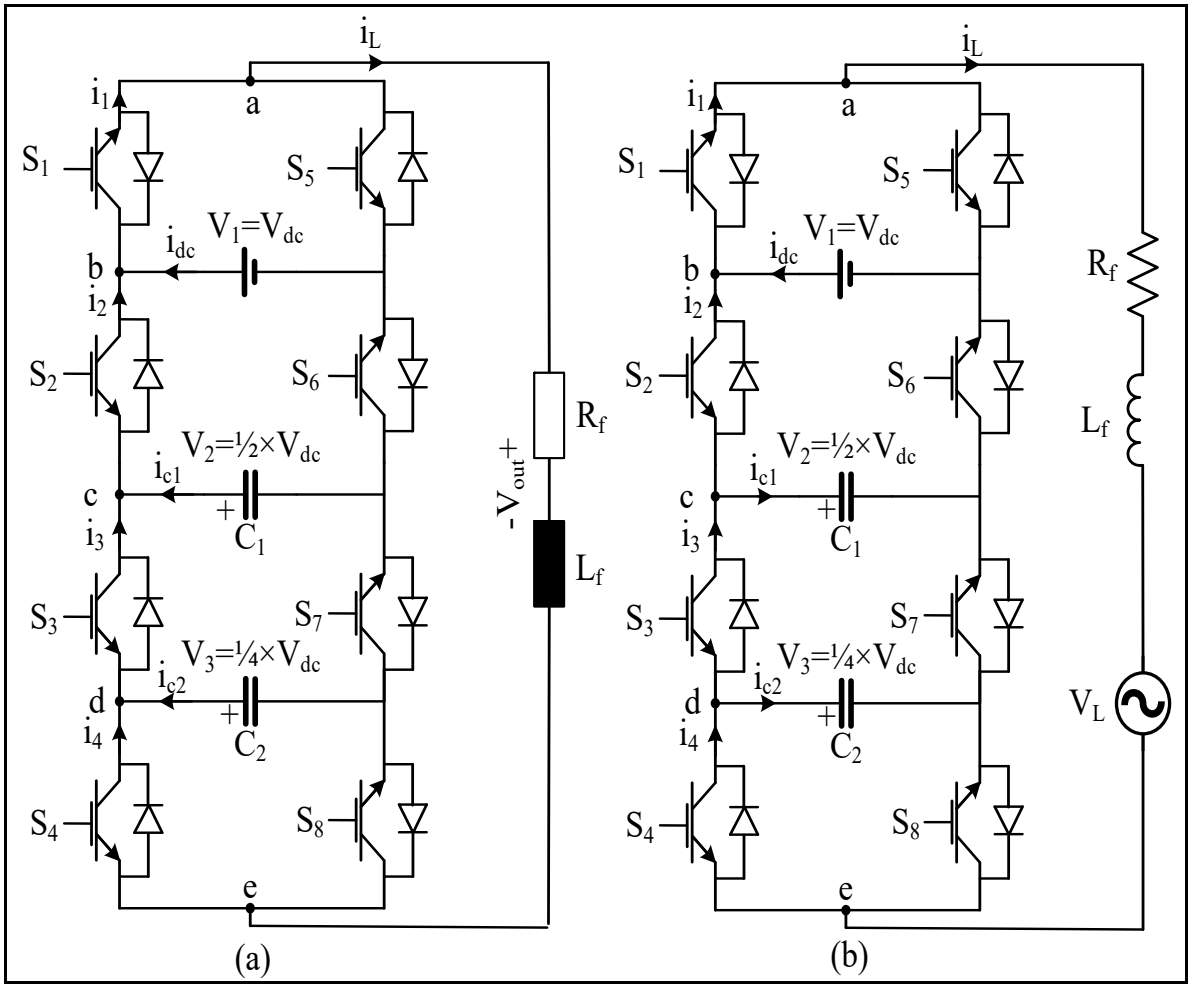


Figure 2.1 Main circuit of nine-level PUC (a) Stand-alone (b) Grid-connected

Table 2.1 Switching states of PUC9 MLI (↑=charging, ↓=discharging, - = no effect)

States	**S_1**	**S_2**	**S_3**	**S_4**	**Output Voltage**	**C_1**	**C_2**
1	1	0	0	0	$V_1=+V_{dc}$	-	-
2	1	0	1	0	$V_1-V_2+V_3=+\frac{3}{4}\times V_{dc}$	↑	↓
3	1	0	0	1	$V_1-V_3=+\frac{3}{4}\times V_{dc}$	-	↑
4	1	0	1	1	$V_1-V_2=+\frac{1}{2}\times V_{dc}$	↑	-
5	1	1	0	0	$V_2=+\frac{1}{2}\times V_{dc}$	↓	-
6	1	1	1	0	$V_3=+\frac{1}{4}\times V_{dc}$	-	↓
7	1	1	0	1	$V_2-V_3=+\frac{1}{4}\times V_{dc}$	↓	↑
8	1	1	1	1	0	-	-
9	0	0	0	0	0	-	-
10	0	0	1	0	$V_3-V_2=-\frac{1}{4}\times V_{dc}$	↓	↑
11	0	0	0	1	$-V_3=-\frac{1}{4}\times V_{dc}$	-	↓
12	0	0	1	1	$-V_2=-\frac{1}{2}\times V_{dc}$	↓	-
13	0	1	0	0	$V_2-V_1=-\frac{1}{2}\times V_{dc}$	↑	-
14	0	1	1	0	$V_3-V_1=-\frac{3}{4}\times V_{dc}$	-	↑
15	0	1	0	1	$V_2-V_3-V_1=-\frac{3}{4}\times V_{dc}$	↑	↓
16	0	1	1	1	$-V_1=-V_{dc}$	-	-

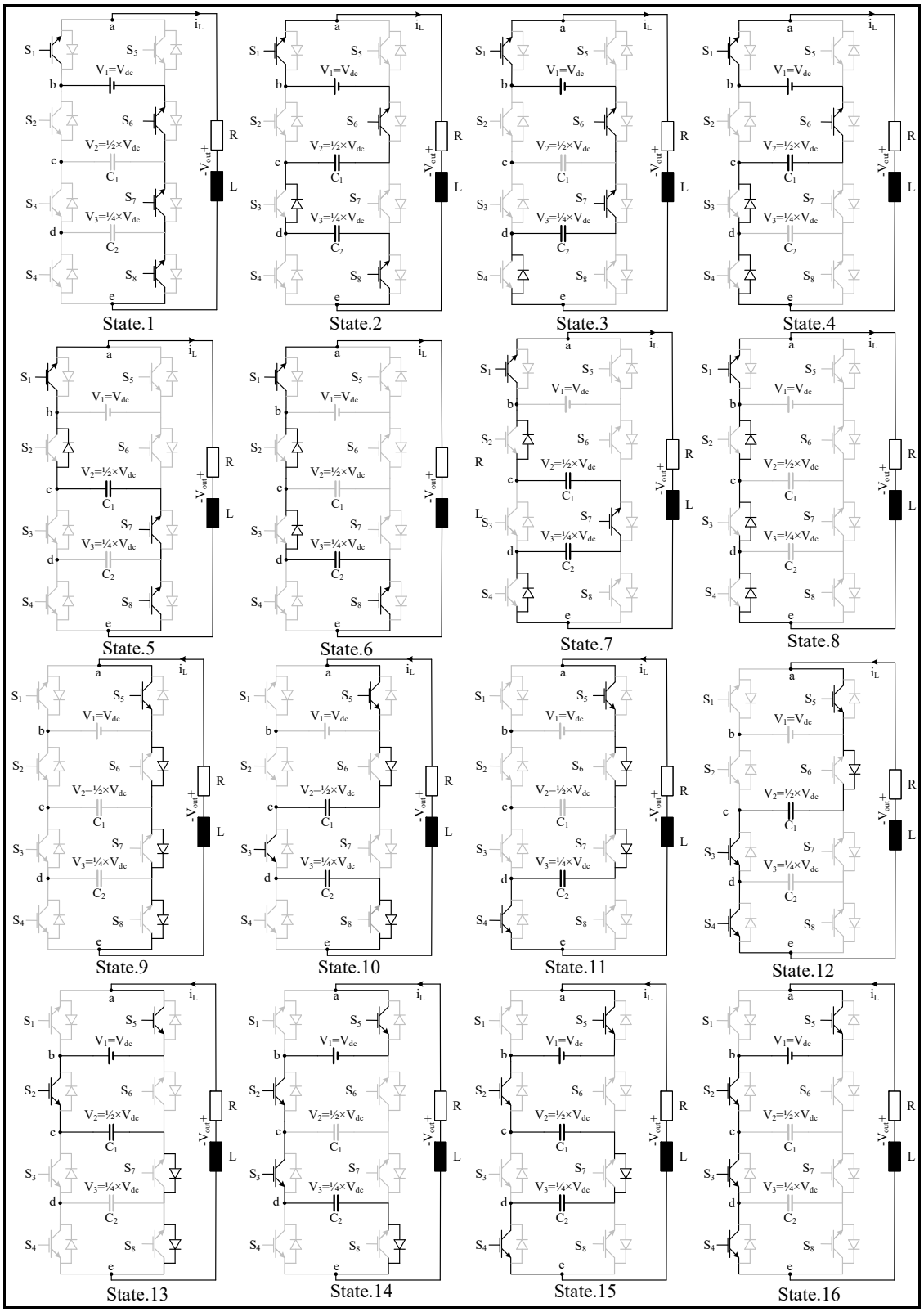


Figure 2.2 Equivalent circuits of PUC in each switching state according to Table 2.1

There are many control techniques like hysteresis control, PI control, and sensorless control, etc. Applying most of these control methods on PUC9 inverter has its own difficulties such as the time-consuming process of tuning, large number of calculations, needing bulky capacitors, working in only stand-alone mode, etc. MPC is a discrete dynamic model-based controller, which is a promising control technique among others for PUC inverter because of its efficiency and simplicity. By applying MPC on PUC9 inverter, the size of capacitors can be decreased drastically, besides it is fast transient and high-power quality.
For designing MPC, mathematical model of our system is needed. As a result, mathematical model of PUC9 will be obtained in the first step.

Each power switch has two operation modes, as shown in equation (2.1).

$$S_i = \begin{cases} 0 \text{ if } S_i \text{ is off (Blocked)} \\ 1 \text{ if } S_i \text{ is on (Saturated)} \end{cases} \tag{2.1}$$

Based on Kirchhoff's Voltage Law (KVL), it can be written that:

$$V_{ae} = V_{ab} + V_{bc} + V_{cd} + V_{de} \tag{2.2}$$

Considering Table.2.1 and Figure 2.2, it is clear that the voltage between two nodes is related to the status of power switch between those nodes and the magnitude of voltage sources that are connected to those notes. (See equation (2.3))

$$\begin{aligned} V_{ab} &= (S_1 - 1) \times V_{dc} \\ V_{bc} &= (1 - S_2) \times (V_{dc} - V_{c1}) \\ V_{cd} &= (1 - S_3) \times (V_{c1} - V_{c2}) \\ V_{de} &= (1 - S_4) \times V_{c2} \end{aligned} \tag{2.3}$$

where V_{dc} is the voltage of DC source, V_{C1} is voltage of C_1, and V_{C2} is voltage of C_2. Substituting equation (2.3) into equation (2.3), the V_{ae} can be obtained based on below equation:

$$V_{ae}(k) = (S_1 - S_2) \times V_{dc}(k) + (S_2 - S_3) \times V_{C1}(k) + (S_3 - S_4) \times V_{C2}(k) \quad (2.4)$$

Based on Table 2.1 and Figure 2.2, it can be written that the currents, which pass through each switch, are affected by line current and also switching operations (see equation (2.5)).

$$\begin{cases} i_1 = S_1 i_L \\ i_2 = S_2 i_L \\ i_3 = S_3 i_L \\ i_4 = S_4 i_L \end{cases} \quad (2.5)$$

By calculating based on KVL law via V_{ae} to V_g as grid voltage, the dynamic model of load current is also achieved as indicated in equation (2.6).

$$V_{ae} = V_g + i_L R_f + L_f \frac{di_L}{dt} \quad (2.6)$$

In the equation (2.6), i_L is the load current, V_L is grid voltage, R_L is load resistance, and L_f is load inductance. As shown in equation (2.7), the current model of capacitors for i_{C1} and i_{C2} are also gained. In the aforementioned equation, switching action controls the capacitors' current.

$$\begin{cases} i_{C1} = C_1 \frac{dV_{C1}}{dt} = (S_3 - S_2) \times i_L \\ i_{C2} = C_2 \frac{dV_{C2}}{dt} = (S_4 - S_3) \times i_L \end{cases} \quad (2.7)$$

2.3 Model predictive control on PUC9

Formulating the control objectives in a cost function and then evaluation of the whole possible switching vectors so as to find the one with minimum value in the cost function, which was previously defined, is the main idea of MPC (Abarzadeh & Al-Haddad, 2018; Falkowski & Sikorski, 2018; Kouro, Cortes, Vargas, Ammann, & Rodriguez, 2009; Sebaaly, Vahedi, Kanaan, & Al-Haddad, 2018; Trabelsi, Bayhan, Ghazi, Abu-Rub, & Ben-Brahim, 2016;

Venkata & Bin, 2017). As indicated in equation (2.8), the conventional form of MPC is as follows.

$$G_{MPC} = k_1 f(x_1) + k_2 f(x_2) + \cdots + k_n f(x_n) \tag{2.8}$$

if weighing factor of the cost function is k_n and a control objective's mathematical model, which is considered to be controlled, is $f(x_1)$. As it was previously stated, converting the mathematical models obtained from nine-level PUC to discrete models is essential due to the fact that MPC is a discrete controller. As regards Euler forward approximation shown in equation (2.9), the load current and voltage model of capacitors presented in equations (2.6) and (2.7) are defined again as discrete models, as indicated in equations (2.10) and (2.11) in turn.

$$\begin{cases} \dfrac{di_L}{dt} \approx \dfrac{i_L(k+1) - i_L(k)}{T_s} \\ \dfrac{dV_{C1,2}}{dt} \approx \dfrac{V_{C1,2}(k+1) - V_{C1,2}(k)}{T_s} \end{cases} \tag{2.9}$$

Where T_s is the MPC sampling time.

$$i_L(k+1) = \left(1 - \frac{R_f \times T_s}{L_f}\right) \times i_L(k) + \frac{T_s}{L_f} \times \left(V_{ae}(k) - V_g(k)\right) \tag{2.10}$$

$$\begin{cases} V_{C1}(k+1) = \dfrac{T_s(S_3 - S_2)}{C_1} i_L(k) + V_{C1}(k) \\ V_{C2}(k+1) = \dfrac{T_s(S_4 - S_3)}{C_2} i_L(k) + V_{C2}(k) \end{cases} \tag{2.11}$$

In the above-mentioned equations, $i_L(k+1)$, $V_{C1}(k+1)$ and $V_{C2}(k+1)$ are predicted models of load current and capacitors' voltage for the next sampling time in order. Based on equations (2.10) and (2.11), the definition of MPC cost function is as follows:

$$G = K_1(i_L(k+1) - i_L(K+1)^*)^2 + K_2 \times (V_{C1}(k+1) - V_{C1}(K+1)^*)^2 + K_3 \times (V_{C2}(k+1) - V_{C2}(K+1)^*)^2 \quad (2.12)$$

In cost function equation(2.12) $i^*_L(k+1)$, $V^*_{C1}(k+1)$ and $V^*_{C2}(k+1)$ are the desired values of the load current and capacitors' voltage in turn, and k_1, k_2 and k_3 are the weighting factors of the cost function, used for assigning the significance of each term in the control process. As the MPC performance is directly under the influence of cost function weighting factor, the weighting factors of cost function must be appropriately selected. In each sampling time, the cost function (G_{MPC}) for sixteen possible switching states of Table 2.2 is calculated. After that, the switching state, which has the minimum cost, is selected for the next sampling time. Figure 2.3 presents block diagram of MPC for nine-level PUC in grid-connected mode. However, for a stand-alone mode, the grid source will be removed in the control loop as indicated in Figure 2.3.

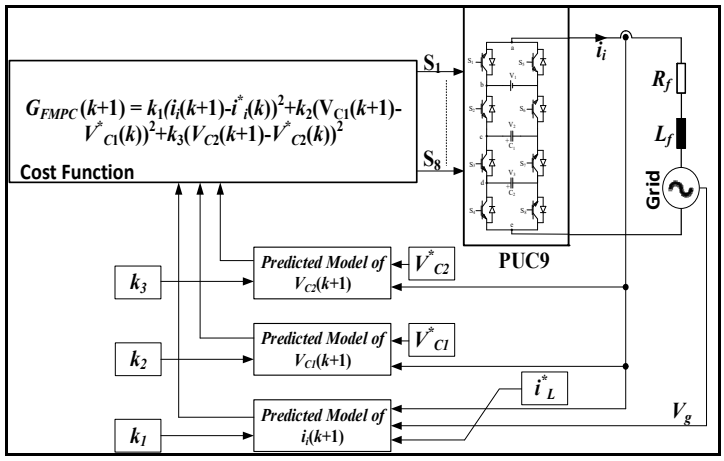


Figure 2.3 Block diagram of MPC for Grid-connected PUC9

2.4 Simulation Parameters

Simulation parameters used for simulating designed control method are shown in Table 2.2. As mentioned before, in dc topology, the voltage of capacitor one must balance at ½×V_{dc} and

the voltage of capacitor two must balance at ¼×V_{dc}. Figure 2.4 indicates Flowchart of MPC for Grid-connected PUC9.

Table 2.2 PUC9 simulation parameters for Grid-Connected and Stand-alone Modes

Parameters	**Value**
Grid Voltage	120 V (rms)
Grid Frequency	60 Hz
Grid Link Inductor (L_f) in grid connected mode	2.5 mH
Grid Link Inductor (L_f) in stand-alone mode	20 mH
DC Source Voltage (V_1)	180-240 V
Line resistance (R_f) in grid connected mode	0.1 Ω
Line resistance (R_f) in stand-alone mode	40-80 Ω
Sampling Time	10 µs
DC Capacitors	560 µF

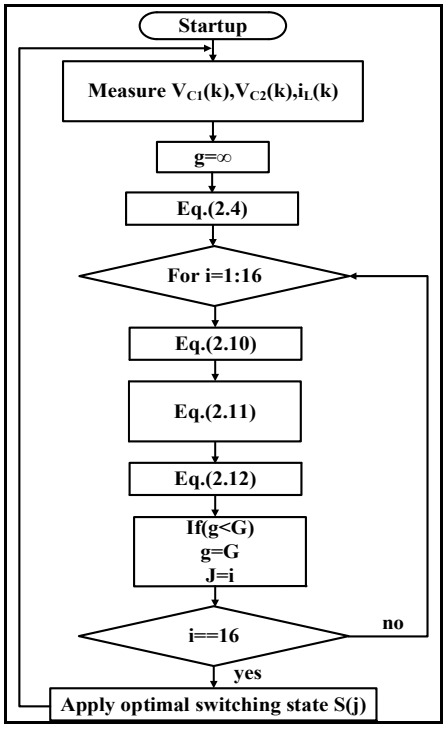


Figure 2.4 Flowchart of MPC for Grid-connected PUC9

2.5 Simulation results in stand-alone mode

In stand-alone mode, the synchronization of the load current and voltage is done automatically; therefore, a sinusoidal wave is the reference current. In the following section, the simulation of proposed control loop is done under unstable conditions if DC voltage source rises from 180 to 240. Figure 2.5 and Figure 2.6 show inverter voltage, load current, capacitors' voltage and THD analysis under unstable conditions. The high performance of the proposed control loop is proven in the stand-alone mode of operation by the presented results.

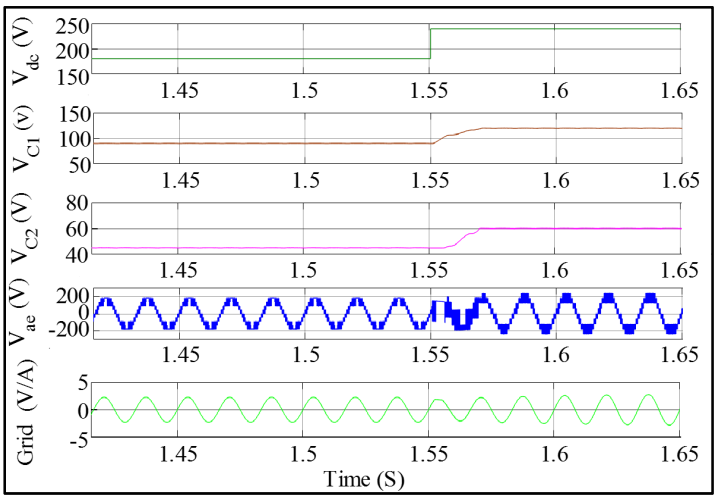


Figure 2.5 Simulation results of stand-alone mode in unstable conditions

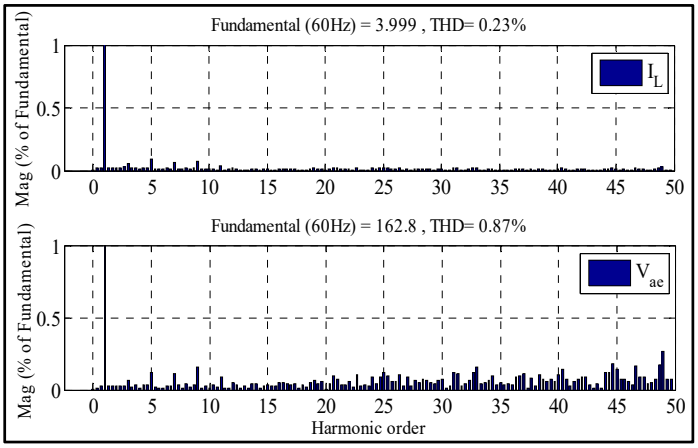


Figure 2.6 Harmonic content analysis for grid current and nine-level voltage in stand-alone mode

2.6 Simulation results in grid-connected mode

In grid-connected mode, for obtaining the unity power factor, the load current and grid voltage must be in the same phase. Therefore, for designing the current reference, a Phase-Locked Loop (PLL) is needed in the control loop. In Figure 2.7, capacitors' voltages, grid voltage, grid current and nine-level voltage are illustrated under stable conditions. As indicated in the mentioned figure, the exact synchronization of inverter current and grid voltage has been done, hence unity power factor has been obtained. Moreover, the voltage ripple of capacitors under 1% is obtained, when the size of capacitors is also properly decreased. Figure 2. 8 shows the analysis of harmonic current including THD for inverter output current and nine-level voltage. As is obvious, the THD is acceptable since it is also under 1%.

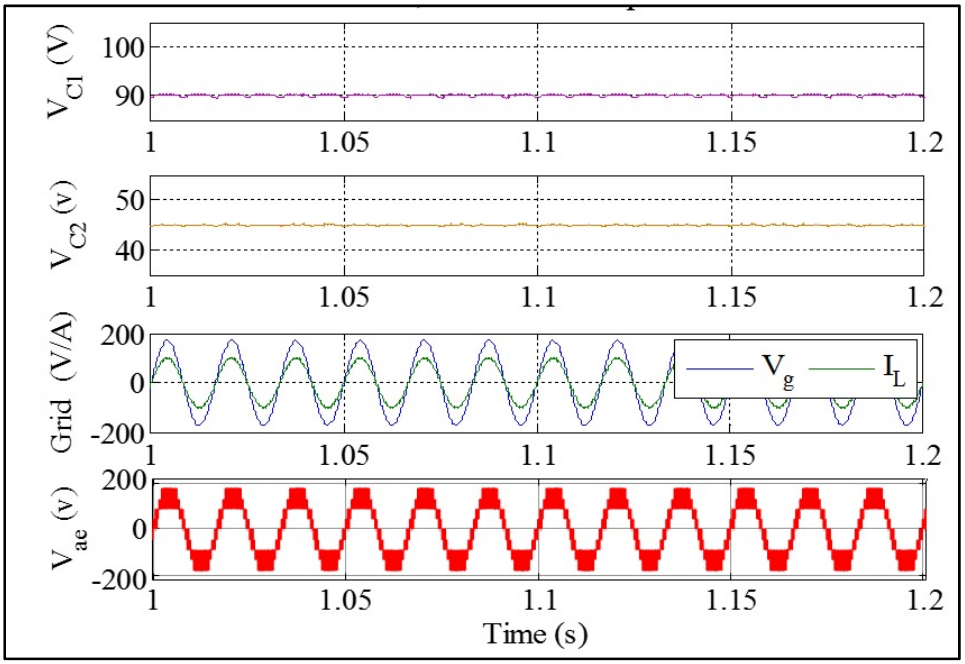


Figure 2.7 Simulation results of grid-connected mode in stable conditions

So as to test the proposed control loop under unsteady conditions, DC voltage source rises from 180 to 240 at first, and then the reference current reduces from 10A to 5A. Based on Figure 2.7-9, the simulation results indicate the fast transient response of MPC in order to track the desired reference if the DC source and current reference are changed rapidly.

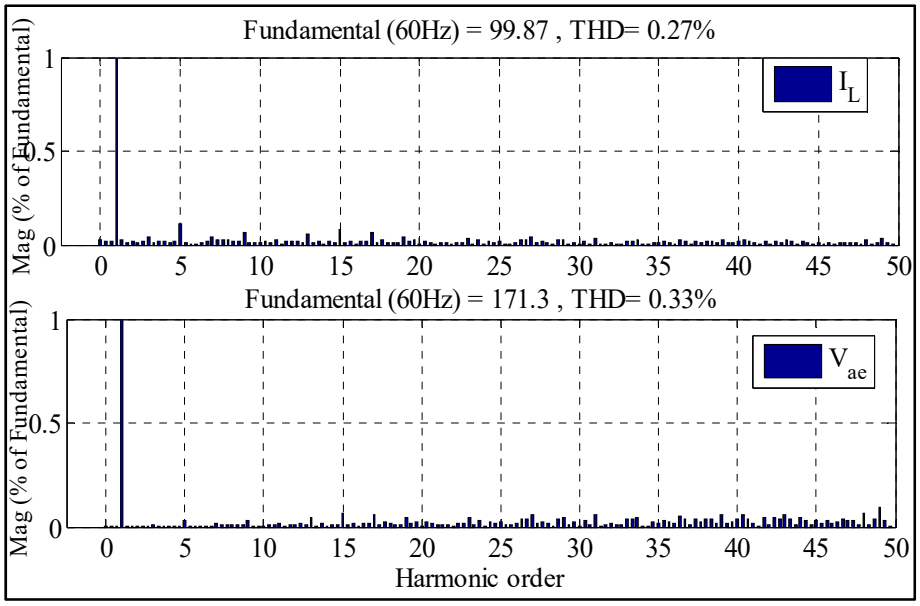


Figure 2.8 Harmonic content analysis for grid-current and nine-level voltage

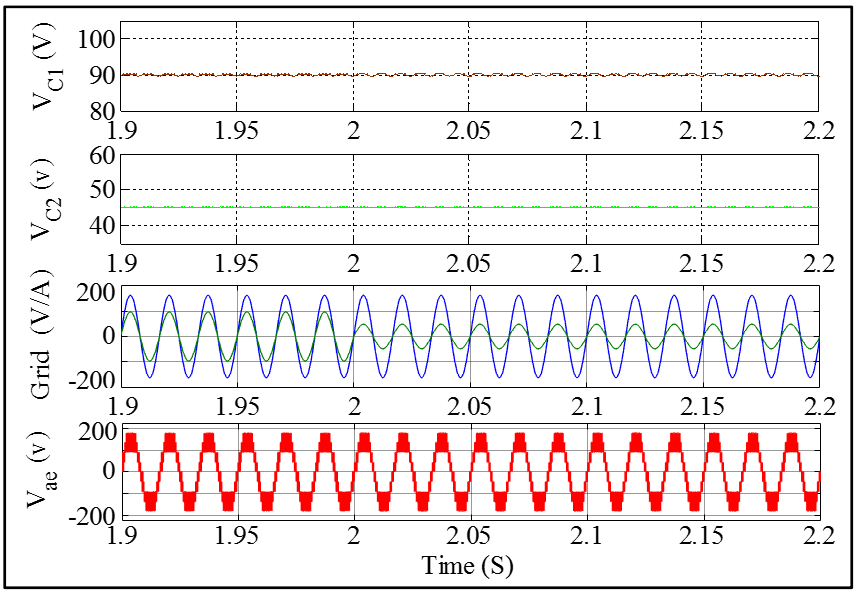


Figure 2.9 Simulation results of grid-connected mode in unstable conditions

2.7 Experimental results

For obtaining experimental result in this section, dSpace 1103 controller and Opal-RT voltage/current measurement is used. For design consideration of PUC9 MLI, please refer to

APENDIX I. Table 2.3 depicts the parameters used during these tests. In the experimental consideration of proposed control technique, first the system is considered in stable condition. Then, reference current is decreased from 4A to 2A. Finally, the voltage of DC source is risen from 50 to 60 to test the dynamic of proposed technique. The gained results were satisfactory and they showed the fast transient of this technique.

Table 2.3 PUC9 experimentation parameters

Parameters	**Value**
Grid Voltage	35 V (RMS)
Grid Frequency	60 Hz
Grid Link Inductor (L_f)	2.5 mH
DC Source Voltage (V_1)	50-60 V
Line resistance (R_f)	0.1 Ω
Sampling Time	46 µs
DC Capacitors	560 µF

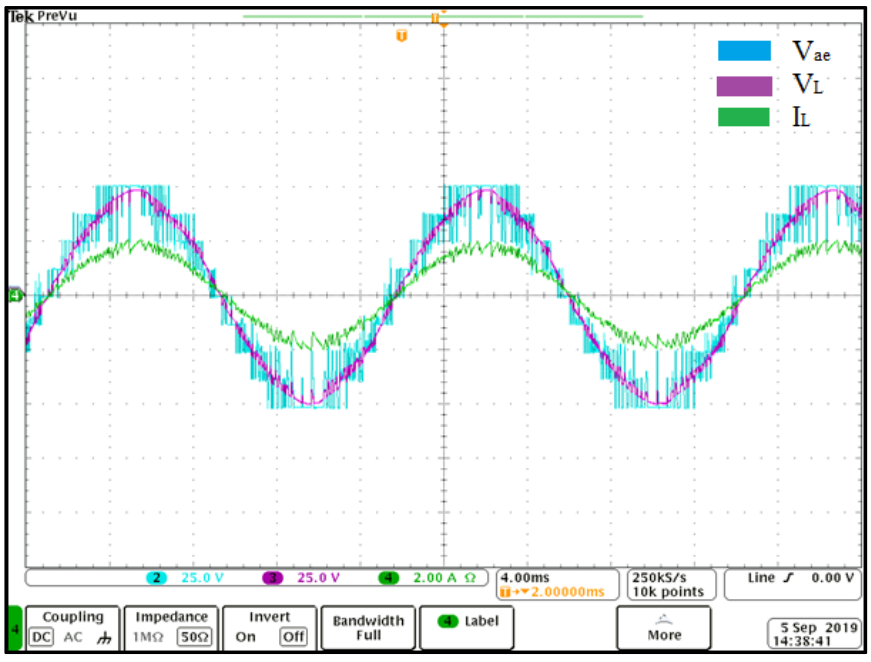


Figure 2.10 Stable condition reference current 2A

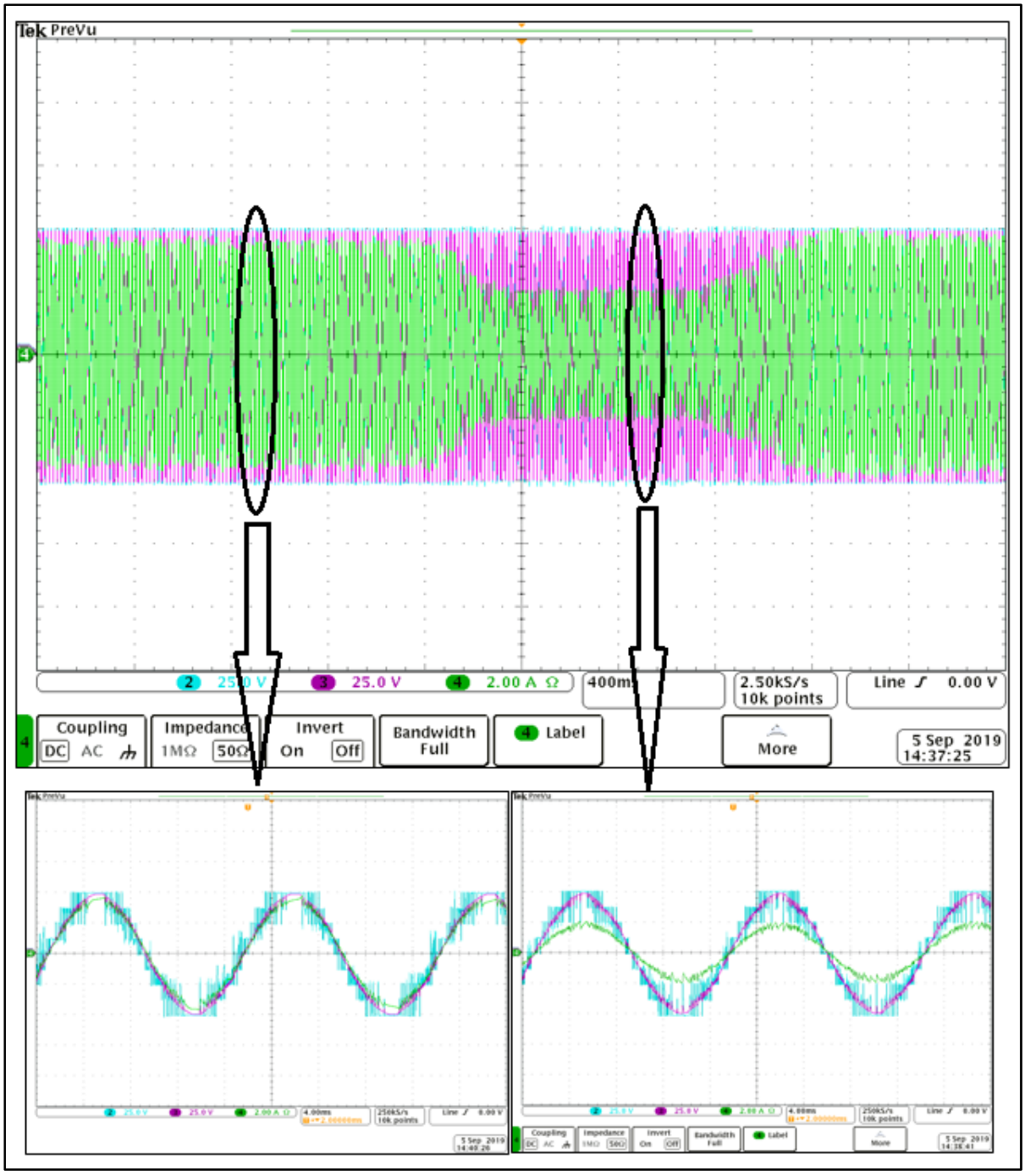


Figure 2.11 Reference currenct changed from 4A to 2A

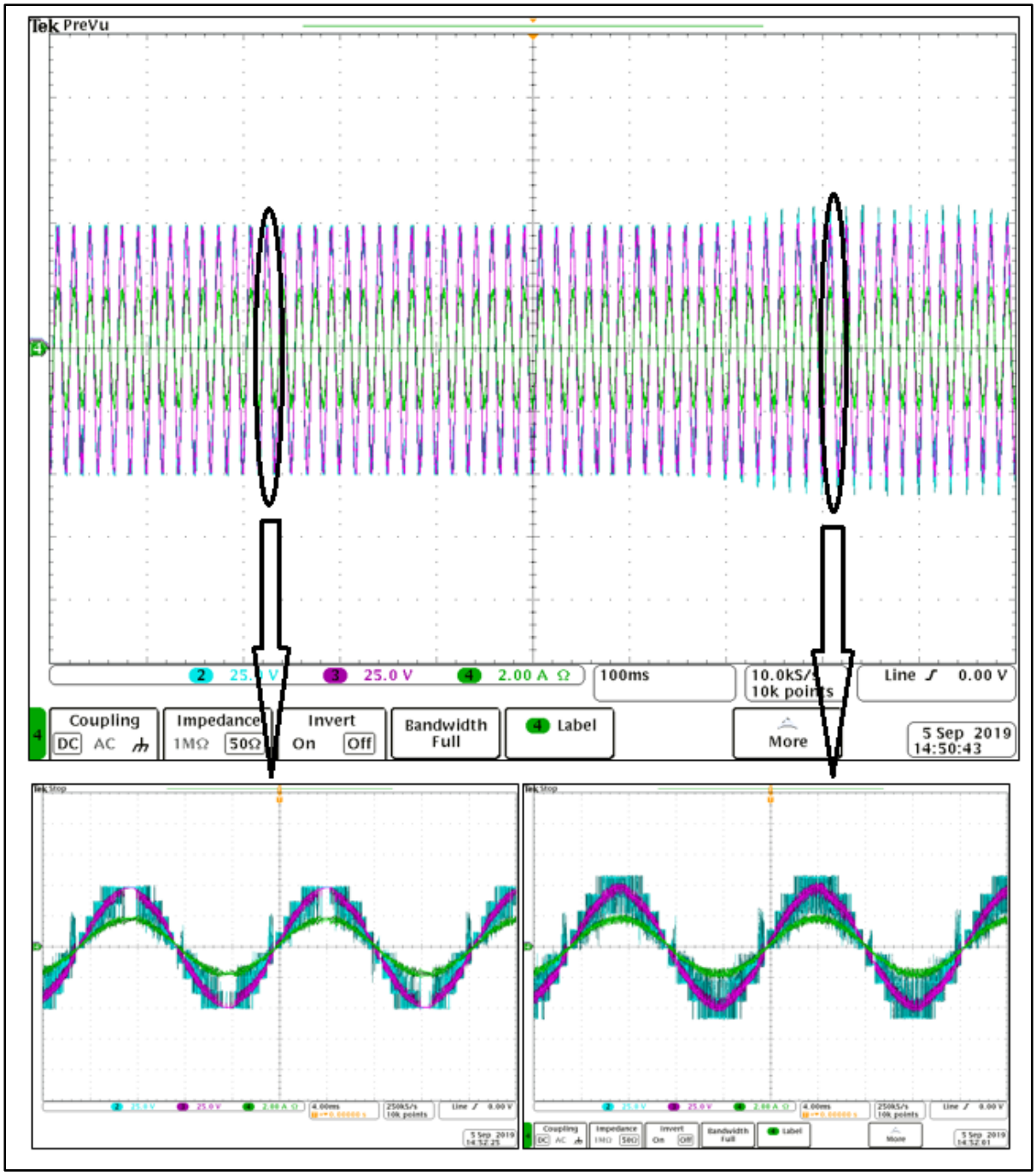


Figure 2.12 Vdc changed from 50V to 60V

2.8 Conclusion

PUC makes it possible to avoid the excessive use of passive and active filters, which has a huge impact on reducing cost as well as having an energy-efficient and reliable system. PUC topology is much more optimized to feed unbalanced loads while ensuring a very good dynamic of the output voltage. However, it has problems such as voltage balancing, current limitations drawn from the voltage source, and requiring three isolated DC sources in three-phase configurations. This chapter implemented an MPC to regulate the load current and balance capacitors' voltage of nine-level PUC topology in both grid-connected and stand-alone modes of operations. The proposed control loop has been simulated by MATLAB software in which results for stable and unstable supply and load conditions prove that capacitors size can noticeably be reduced, and current reference is tracked desirably while unity power factor operation is achieved. Minimum THD and least capacitors voltage ripples are also obtained as shown. The proposed nine-level PUC control loop proved PUC as an efficient low-cost high-performance multilevel inverter for various industrial applications; mainly grid-connected converters are used for renewable energy integration and battery chargers for high-power fast-charging electric cars.

CHAPTER 3

A NEW MULTICARRIER LS-PWM TECHNIQUE FOR VOLTAGE BALANCING OF NINE-LEVEL PACKED U-CELL INVERTER'S CAPACITORS

3.1 Introduction

PID controller and PWM technique are two popular methods in industrial applications of different converters due to their simplicity and efficiency; in other words, over 90% of industrial controllers are PID controllers. It means that the industry is not very interested in using new control methods. On the other hand, tuning PID controllers for generating reference voltage of PWM is a time-consuming and complicated task. The combination of these two known methods for voltage balancing and current control of nine-level Packed U-Cell inverter (PUC9), which is energy efficient converter without spending a lot of time for tuning with high efficiency, can be more convincing for the industry to utilize such high quality and low price inverters. Some voltage balancing and current controllers have been applied on PUC9 such as hysteresis control and sensorless control. Most of these methods need bulky capacitors or are not highly efficient, which are the most considerable disadvantages of them.

3.2 Conventional multicarrier level shifted pulse width modulation (LS-PWM)

The basic concept of this technique is comparing a sinusoidal reference voltage with triangular carriers. There is three conventional level-shifted PWMs (See Figure 3.1). In these methods, N voltage levels need N-1 carriers. These carriers will be placed vertically between peal-to-peak amplitude. As a result, the peak-to-peak amplitude should be divided by the number of carriers. For example, if peak-to-peak amplitude is equal to two (from -1 to 1), for having nine levels of voltage, eight triangular carrier waves with peak-to-peak amplitude of 0.25 are required. All carriers have the same frequency and the same peak-to-peak magnitude (Bin, 2006a, 2006b; Franquelo et al., 2008). Figure 3.2 depicts the conventional PD-LS-PWM technique (Ounejjar et al., 2011), Figure 3.3 indicates input waveforms of conventional PD-LS-PWM for nine-level inverters, and Figure 3.4 illustrates the output waveform of

conventional PD-LS-PWM when the carriers' frequency is 2 kHz and reference frequency is 60 Hz.

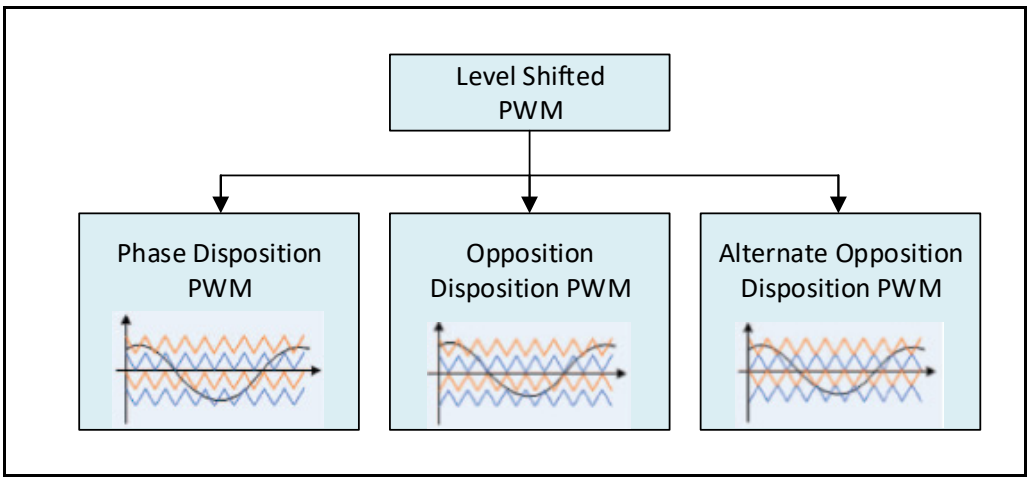


Figure 3.1 Three conventional LS-PWM

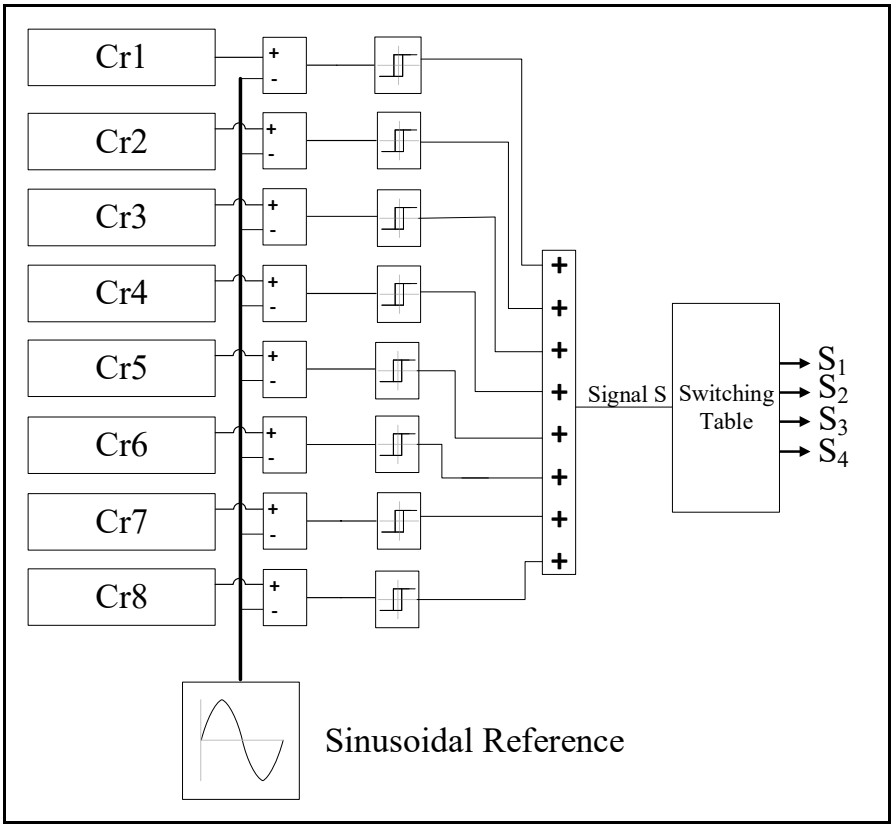


Figure 3.2 Conventional PD-LS-PWM technique

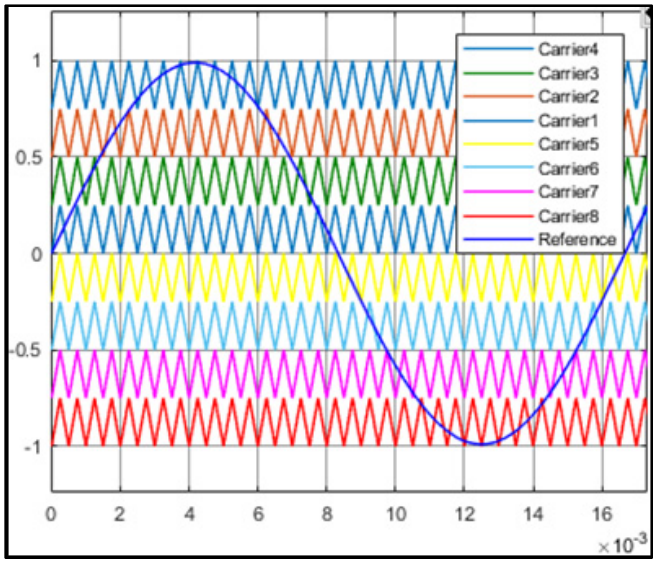


Figure 3.3 Input waveforms of conventional nine level PD-LS-PWM

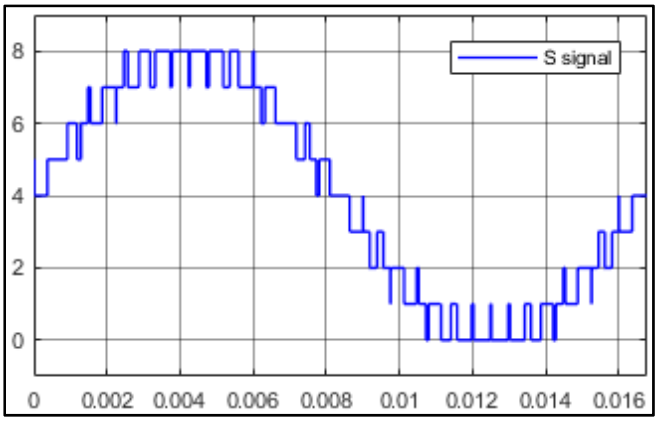


Figure 3.4 Output Waveform of conventional nine level PD-LS-PWM

3.3 Proposed voltage balancing technique

Some voltage balancing techniques have been applied on nine levels packed U Cell like hysteresis control and sensorless PWM, etc. Most of these methods need bulky capacitors. By applying the proposed voltage balancing technique, the size of capacitors could be decreased remarkably, which reduces the cost of manufacturing. As mentioned before, in conventional PD-LS-PWM in nine level inverters, eight triangular carriers with amplitude of 0.25 are needed (if peak-to-peak amplitude is considered equal to two). In this proposed method, these eight

carriers are considered as fixed carriers. There is one floating carrier between each two fixed carriers. As a result, six floating carriers are required for nine-level inverters. The role of these floating carries is to use redundant states to balance the voltage of capacitors without changing output waveform. In other words, these floating carriers increase or decrease the charging time of the capacitors in order to hold the capacitors' voltage in the desired level. In this technique, there are two PI blocks (one PI block for voltage balancing of each capacitor). The error of PI blocks is calculated by subtracting the desired voltage of C_1 and C_2 and their measured values. Then, the output of each PI block is added to the concerning floating carriers in order to specify the level of that carrier. It should be considered that floating carriers must not pass through the fixed carriers, thus the upper and lower saturation points of each PI block should be limited between upper fixed carrier level and lower fixed carrier level. Figure 3.5 illustrates the proposed modulation technique, Figures 3.6 and 3.7 depict input and output waveforms of this method in a single period.

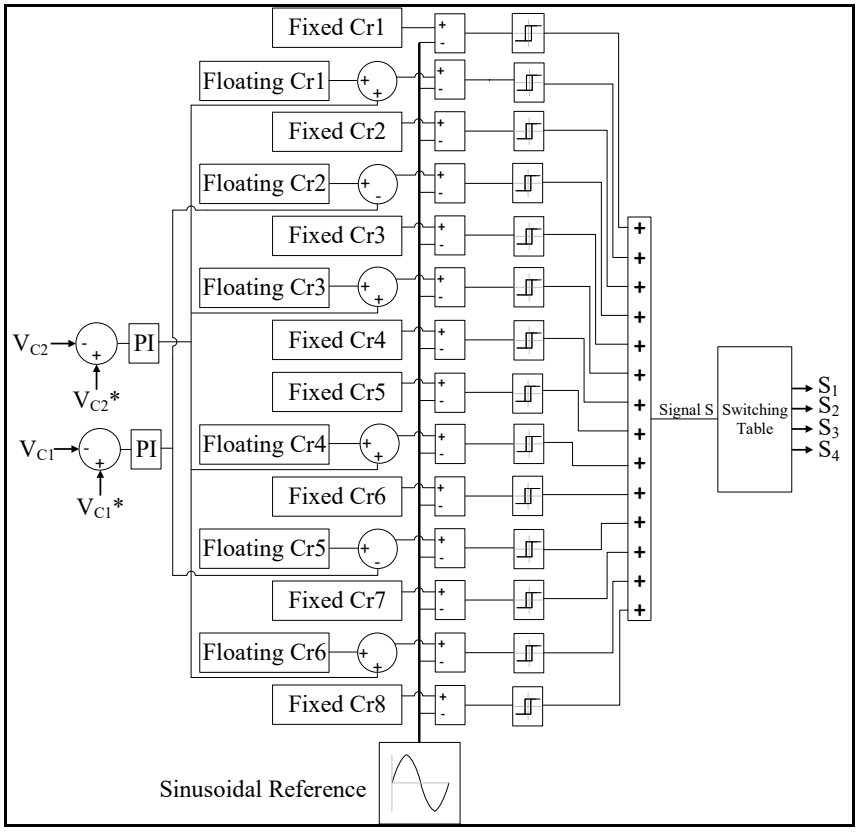


Figure 3.5 Proposed modulation technique

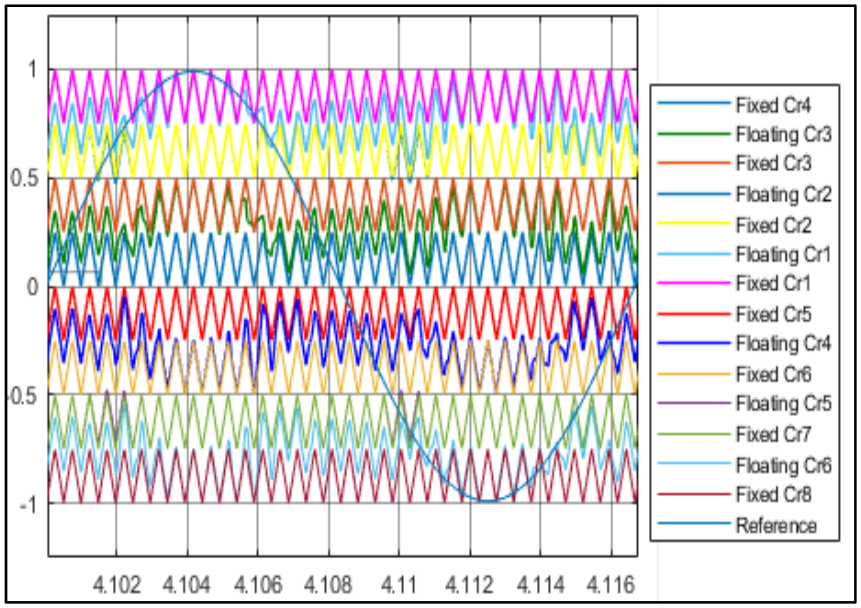


Figure 3.6 Input waveforms of proposed technique

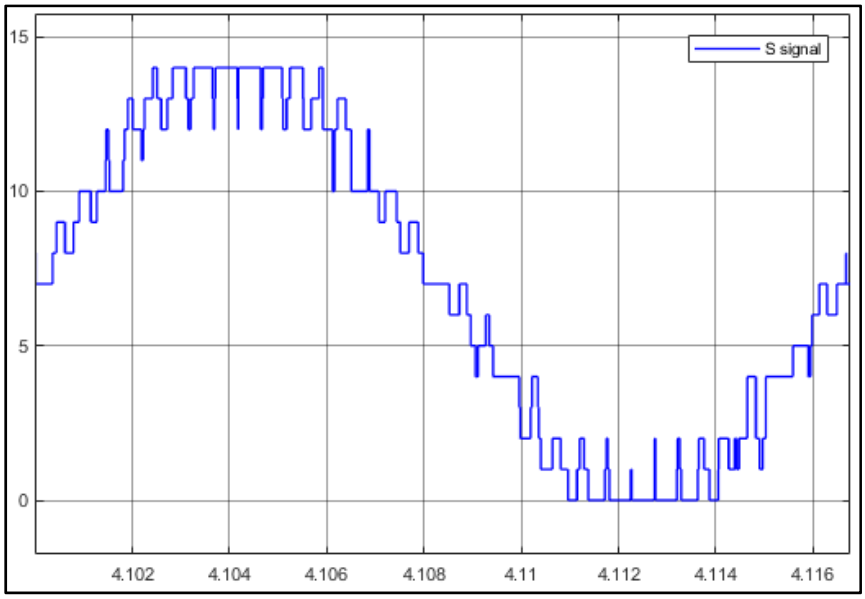


Figure 3.7 Output waveform of proposed modulation technique

3.4 Simulation Results

The parameters used during the simulation are shown in Table 3. Based on Table 3.1, if V_{DC}=400 V, voltages of V_{C1} and V_{C2} must be equal to ½×V_{dc}=200 and ¼×V_{dc}=50 in order. It

should be mentioned that S_1 must support all voltage V_{dc}, while S_2 must support V_{C1}, and switches S_3, S_4 must only support V_{C2}. Figure 3.8 shows the simulation result while the voltage of dc source has been raised from 300 V to 400 V. Figure 3. 9-13 illustrate dc link and capacitors' voltage, output voltage, THD of output voltage, output current, and THD of output current, respectively in stable conditions. It can be seen that the THD of output current is equal to 2.09% and the THD of output voltage is 14.16%.

Table 3.1 Main System Parameters

Parameters	**Value**
Sampling Time	10 µs
DC Voltage Source	400V & 300V
Capacitors(C_1,C_2)	100 µF,560 µF
Load inductance	20mH
Load resistance	40Ω
Switching Frequency	2 kHz

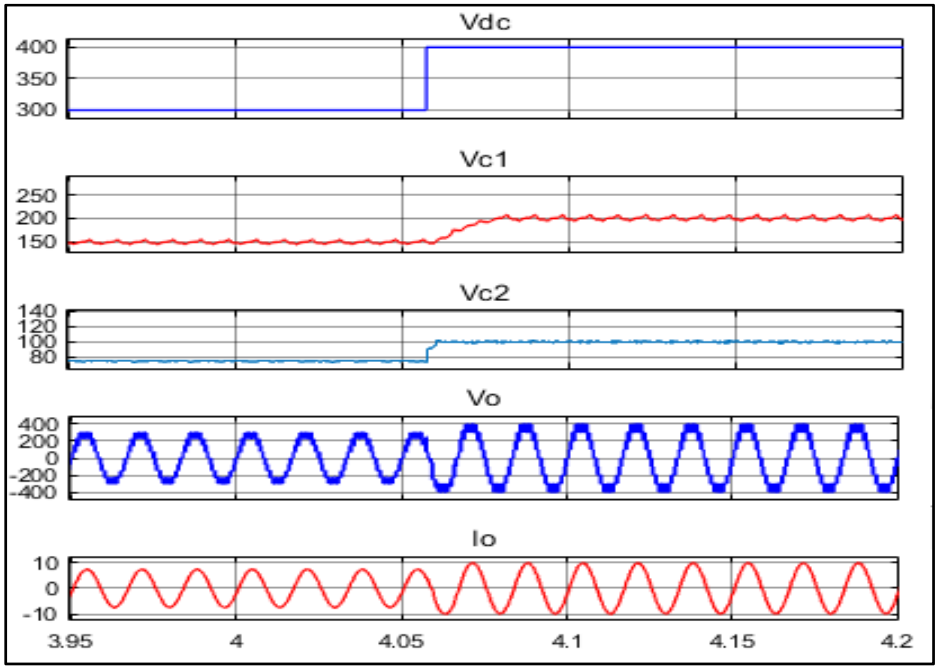


Figure 3.8 Simulation result in unstable condition

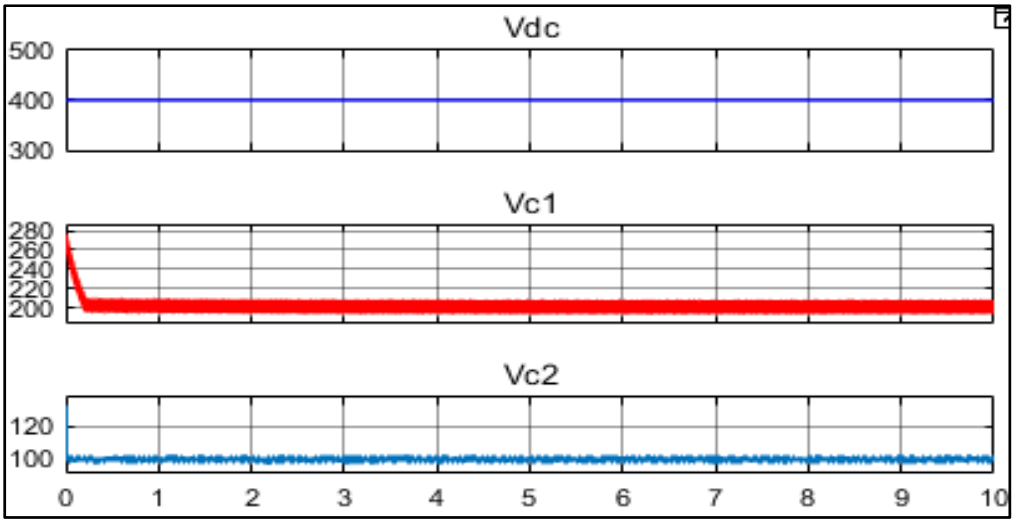


Figure 3.9 DC source and capacitors voltages in stable condition

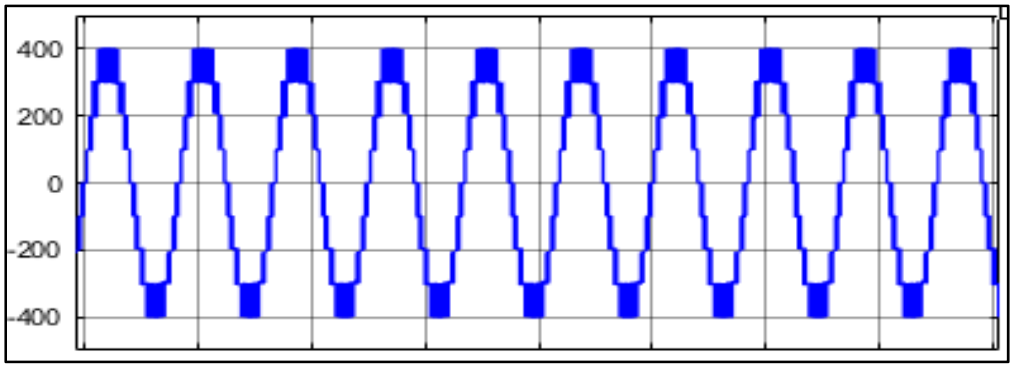


Figure 3.10 Output voltage in stable condition

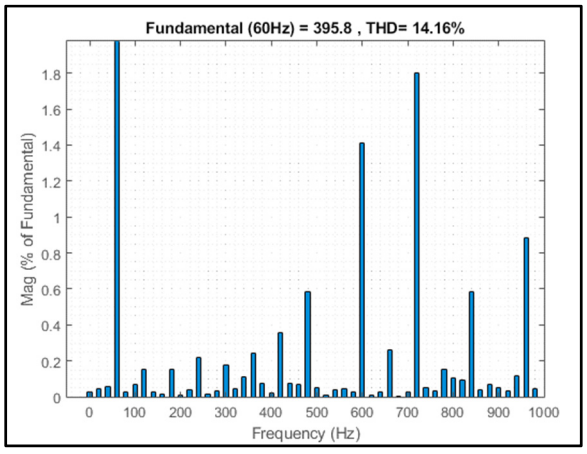


Figure 3.11 Output voltage THD in stable condition

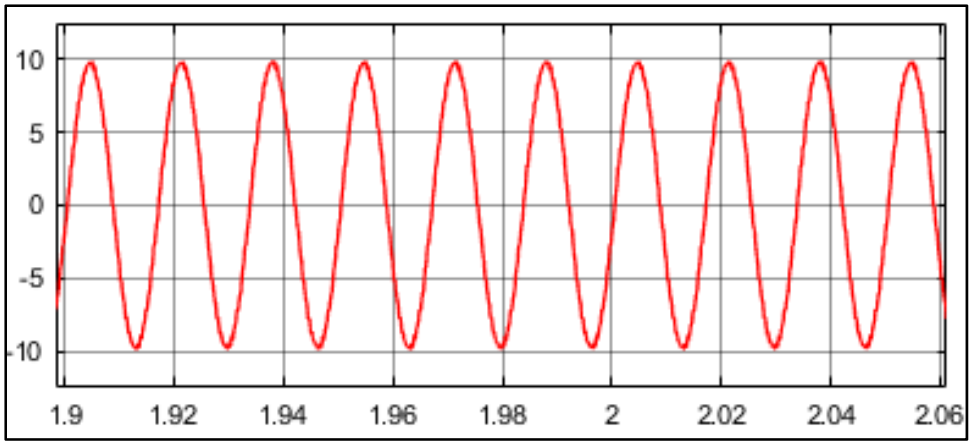


Figure 3.12 Output current in stable condition

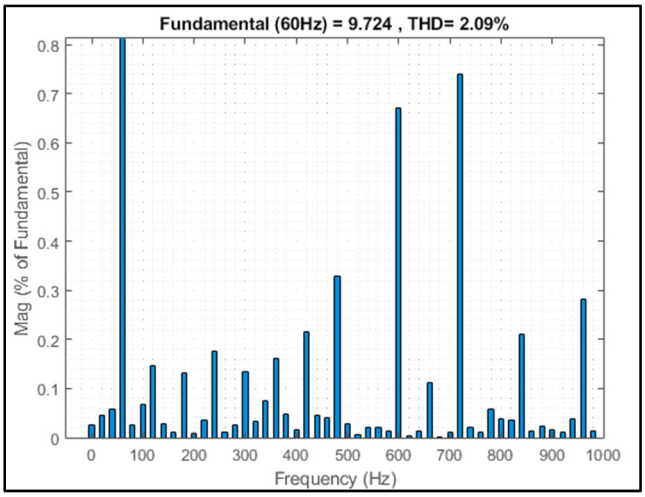


Figure 3.13 Output current THD in stable condition

3.5 Experimental Results

For experimental evaluation of the proposed modulation technique, first PCB of PUC9 was designed with altium designer software (see APENDIX I), then via using dSpace1103 and OPAL-RT voltage/current measurement, the proposed technique was implemented on it. Table 3.2 illustrates the parameters during the experimental test. Firstly, the proposed method was evaluated experimentally in stable conditions. Secondly, for testing the dynamic of proposed technique, dc source was increased from 150 V to 195 V and then returned to 150 V. Finally, the load changed from 80 to 40 and then returned to 80. Figure 3.1-3.4 illustrate the above-mentioned steps in order. As it is obvious, in this method the size of C2 is decreased drastically in comparison with other existing methods. Besides, this method provides fixed switching frequency, so the designing of snubber and controlling switching losses is an easy task. To sum up, the experimental results depict the capability of proposed control technique on PUC9.

Table 3.2 System Parameters

Parameters	**Value**
Sampling Time	46 µs
DC Voltage Source	153,170 & 195V
Capacitors(C_1,C_2)	560 µF,100 µF
Load inductance	20mH
Load resistance	40Ω, 80Ω
Switching Frequency	2 kHz

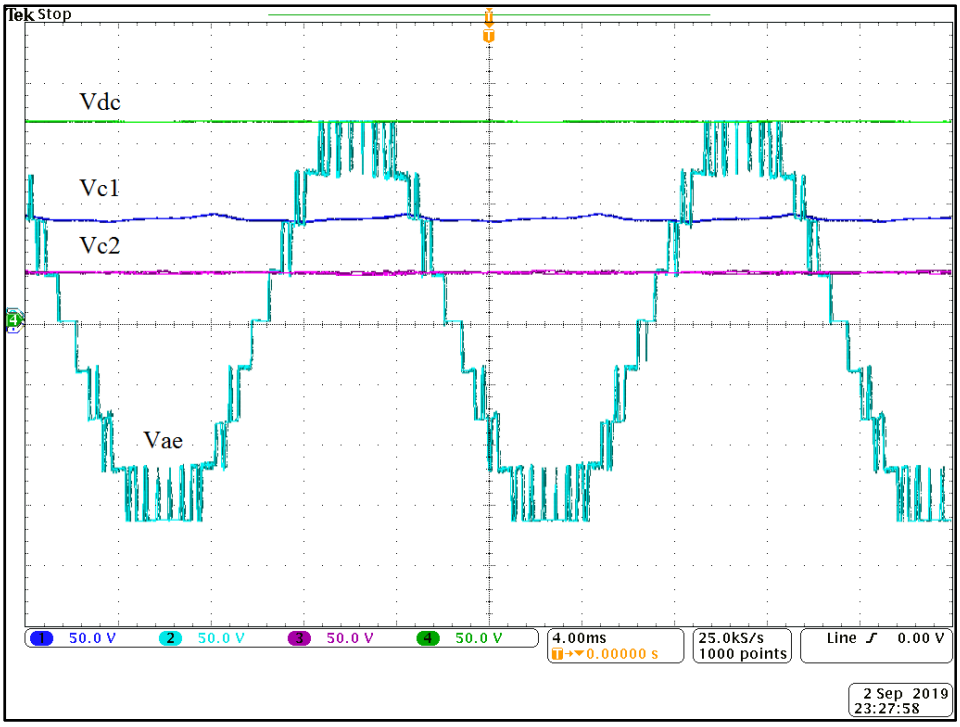


Figure 3.14 Voltages of V_{dc}, V_{c1}, V_{c2}, and V_{ae} in stable condition

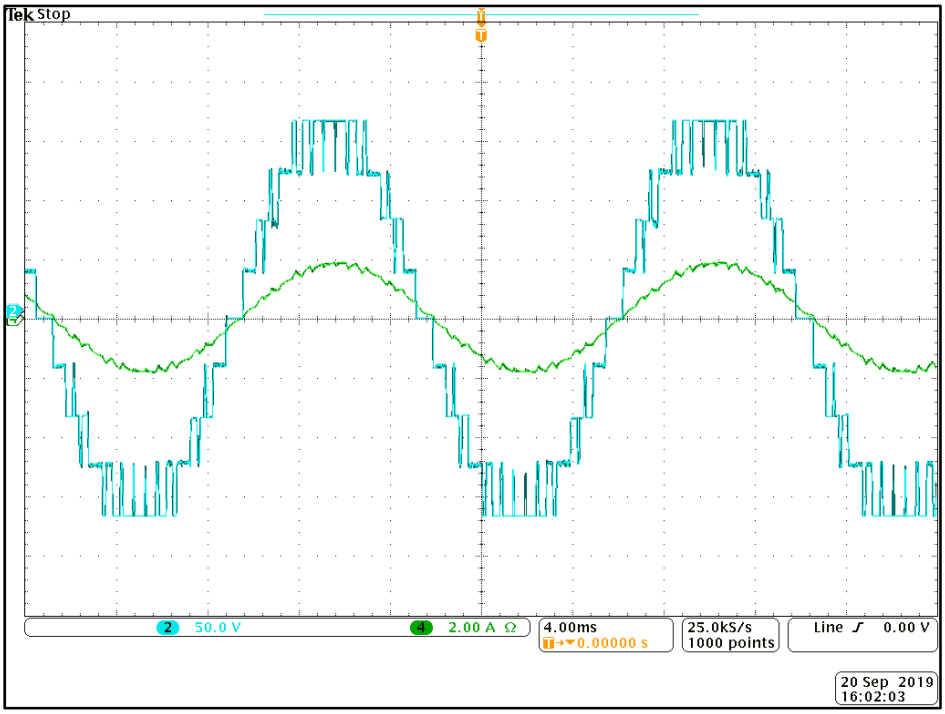


Figure 3.15 V_{ae} and I_o in stable condition R_L=80Ω

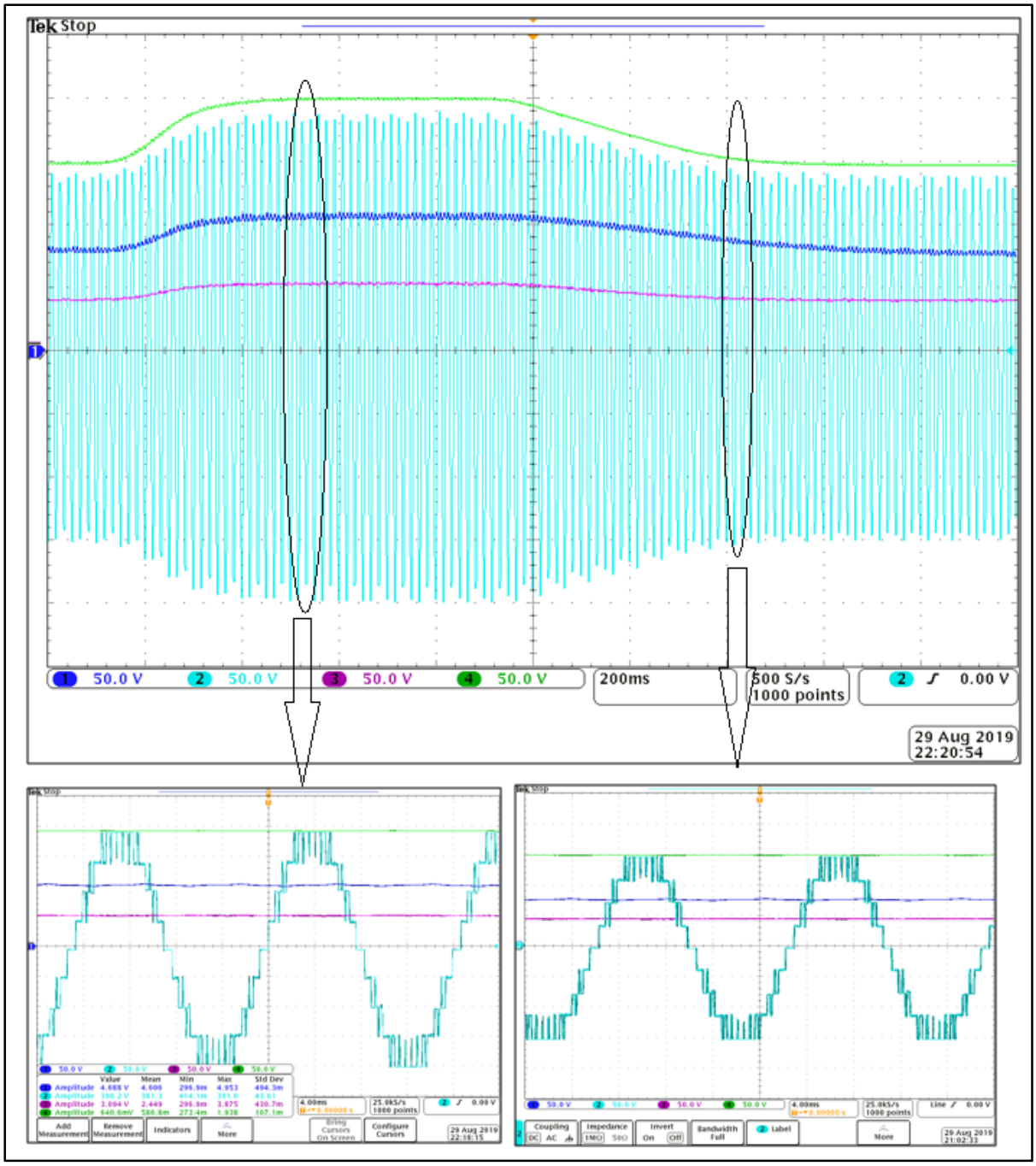


Figure 3.16 V_{dc} changes from 153V to 195V

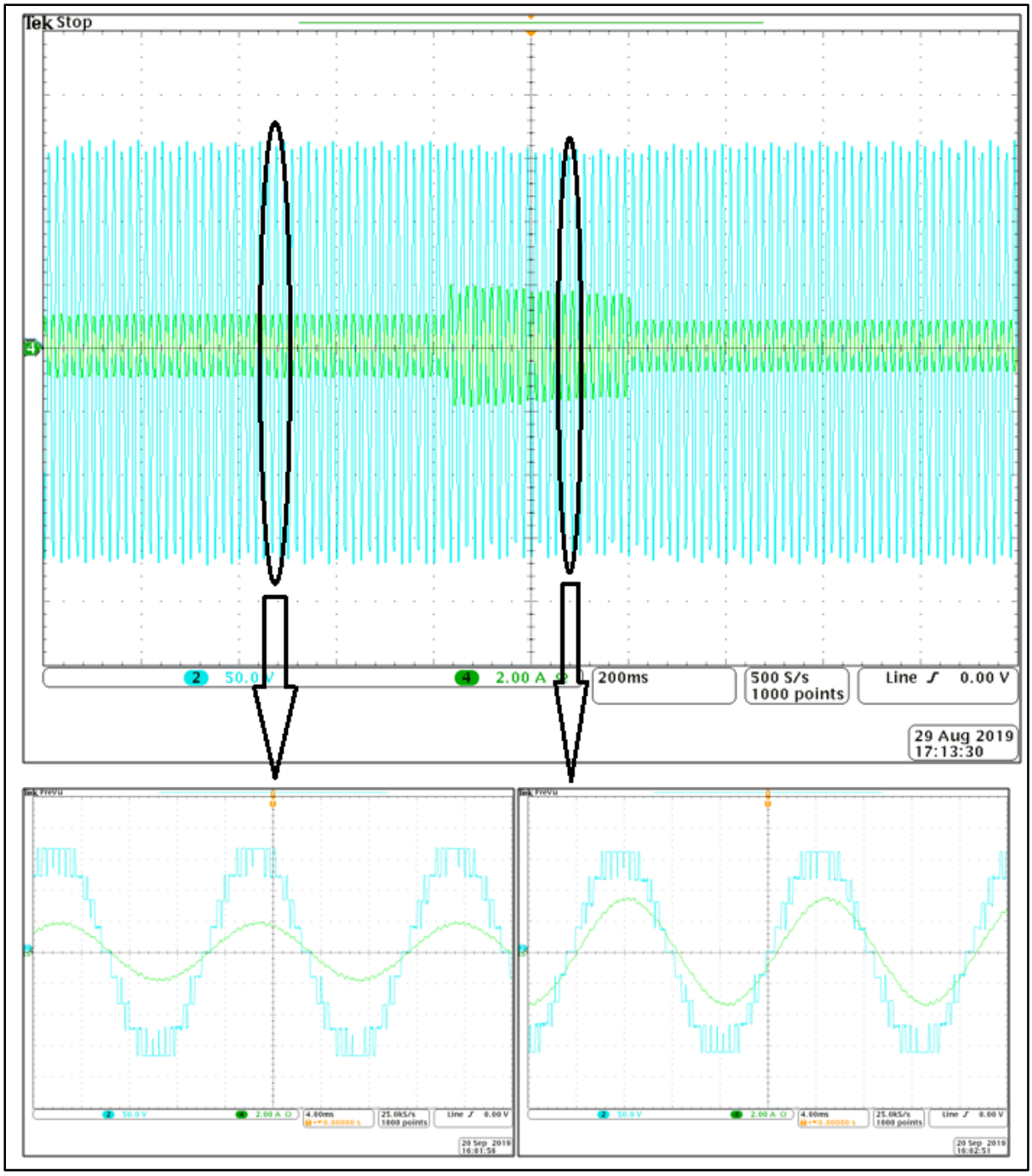


Figure 3.17 Step Load change from 80 Ω to 40Ω when Vdc= 170 V

3.6 Conclusion

PWM technique and PID controller are two popular methods in industry due to their efficiency and simplicity. Besides, many modules are available in the market for these methods. As a result, there is not much tendency to use other methods in the industry. PUC is a part of new generation multilevel inverters, which reduce the manufacturing cost and increase power quality. In this chapter, a new method for voltage balancing of capacitors in PUC9 was proposed. By this method, the size of capacitors is reduced remarkably, while it works efficiently. In addition, the tuning of proposed PID controller is not a complicated and time-consuming process because the coefficients of PI controller can be tuned for each capacitor separately. The simulation result approves the efficiency of this method. It should be mentioned that this method works and remains efficient even with a very simple P controller.

CHAPTER 4

NINE-LEVEL UX-CELL INVERTER TOPOLOGY: MODEL PREDICTIVE CONTROL

4.1 Introduction

After working on PUC9 topology for a couple of months and getting familiar with its advantages and disadvantages, when I was applying MPC on PUC7 MLI, I realized that if two crossover switches are added to PUC7, it is able to generate nine levels of voltage at its output like PUC9 with one less capacitor and the added value of achieving boosting ability. Additionally, it was necessary to change two side switches of PUC7 into bidirectional voltage blocking switches in order to prevent short circuit between positive and negative polarity of DC voltage source and auxiliary capacitor when proposed MLI is boosting the input voltage. In this chapter, the operation of UX-Cell MLI is explained, then its mathematical model is obtained. Afterward, based on the obtained model, MPC will be applied on the proposed MLI. Finally, the validity of designed control technique is proven with Sim-Power-System and Matlab Simulink software and it is also validated experimentally using dSpace 1103 and OPAL-RT voltage/current measurement.

4.2 Nine-Level UX-Cell Inverter operation and modeling

UX-Cell MLI is created by changing two side switches in the middle cell of PUC7 to bidirectional switches and adding two crossover switches to it. The function of these bidirectional switches is omitting the effect of internal diode of side switches in PUC topology when DC link voltage is added to capacitor voltage. Figure 4.1 depicts the main circuit of UX-Cell MLI. It has the minimum number of switches, while it generates maximum number of output voltage levels, besides it has boost operation. It means that the output peak amplitude of this inverter is 33% higher than the amplitude of its dc link voltage; in addition, this topology is transformer less. DC sources must be isolated in most multilevel inverters topologies, but this inverter topology does not need transformers to isolate the DC bus voltages. In UX-Cell

MLI, as DC voltages can be interconnected and consequently regulated to the desired values, there is no need to use transformers. UX-Cell MLI consists of eight switches (see Figure 4.1); switches have only two states. One state where it is off or blocked (S=0) and another one where it is on or saturated (S=1), which allows to reach (2^4) sixteen states with seven redundant. This circuit can produce nine levels of voltage at the output when V_1 is equal to V_{dc} and V_2 is equal to $\frac{1}{3} \times V_{dc}$. In Table 4.1, nine levels of voltage, produced based on the states of the switches, are shown. It should be noted that switches S_1, S_4 and S_3, S6 are complimentary, which means that when S_1 is blocked, S_4 must be saturated and vice versa. Moreover, among middle cell switches, the saturation of only one switch is needed at the same time so as to prevent short circuit between positive and negative terminals of dc voltage source and/or capacitors. In Table 4.1, ↑ shows the charging status, ↓ indicates discharging status, and – illustrates no affect status of the capacitor. Figure 4.2 shows the current paths of this topology in each switching state of Table 4.1.

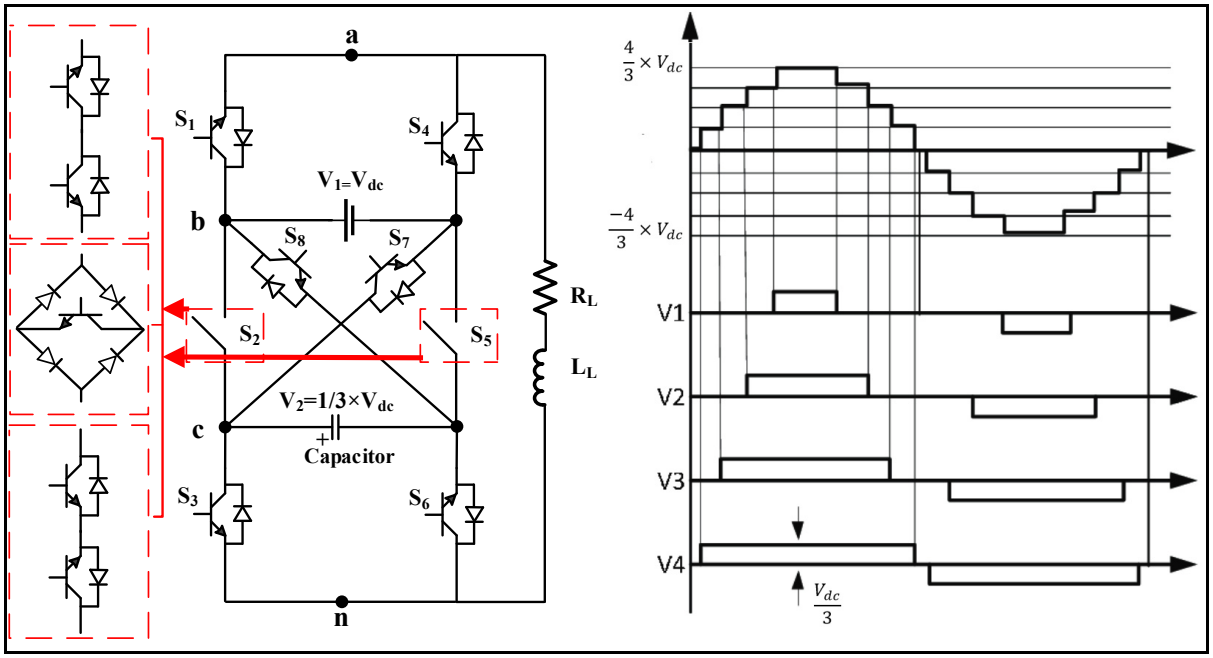


Figure 4.1 Nine-level UX-Cell inverter in stand-alone mode

Table 4.1 Switching states of UX-Cell MLI

States	S_1	S_2	S_3	S_4	S_5	S_6	S_7	S_8	Output Voltage	C
1	**1**	**0**	**0**	**0**	**0**	**1**	**1**	**0**	$\boldsymbol{V_1 + V_2 = \frac{4}{3} \times V_{dc}}$	↓
2	1	0	0	0	1	1	0	0	$V_1 = V_{dc}$	–
3	**1**	**0**	**1**	**0**	**0**	**0**	**1**	**0**	$\boldsymbol{V_1 = V_{dc}}$	–
4	**1**	**0**	**1**	**0**	**1**	**0**	**0**	**0**	$\boldsymbol{V_1 - V_2 = \frac{2}{3} \times V_{dc}}$	↑
5	**0**	**0**	**0**	**1**	**0**	**1**	**1**	**0**	$\boldsymbol{V_2 = \frac{1}{3} \times V_{dc}}$	↓
6	1	1	0	0	0	1	0	0	$V_2 = \frac{1}{3} \times V_{dc}$	↓
7	0	0	1	1	0	0	1	0	0	–
8	1	1	1	0	0	0	0	0	0	–
9	0	0	0	1	1	1	0	0	0	–
10	**1**	**0**	**0**	**0**	**0**	**1**	**0**	**1**	**0**	–
11	0	0	1	1	1	0	0	0	$-V_2 = \frac{-1}{3} \times V_{dc}$	↓
12	**1**	**0**	**1**	**0**	**0**	**0**	**0**	**1**	$\boldsymbol{-V_2 = \frac{-1}{3} \times V_{dc}}$	↓
13	**0**	**1**	**0**	**1**	**0**	**1**	**0**	**0**	$\boldsymbol{V_2 - V_1 = \frac{-2}{3} \times V_{dc}}$	↑
14	**0**	**0**	**0**	**1**	**0**	**1**	**0**	**1**	$\boldsymbol{-V_1 = -V_{dc}}$	–
15	0	1	1	1	0	0	0	0	$-V_1 = -V_{dc}$	–
16	**0**	**0**	**1**	**1**	**0**	**0**	**0**	**1**	$\boldsymbol{-V_1 - V_2 = \frac{-4}{3} \times V_{dc}}$	↓

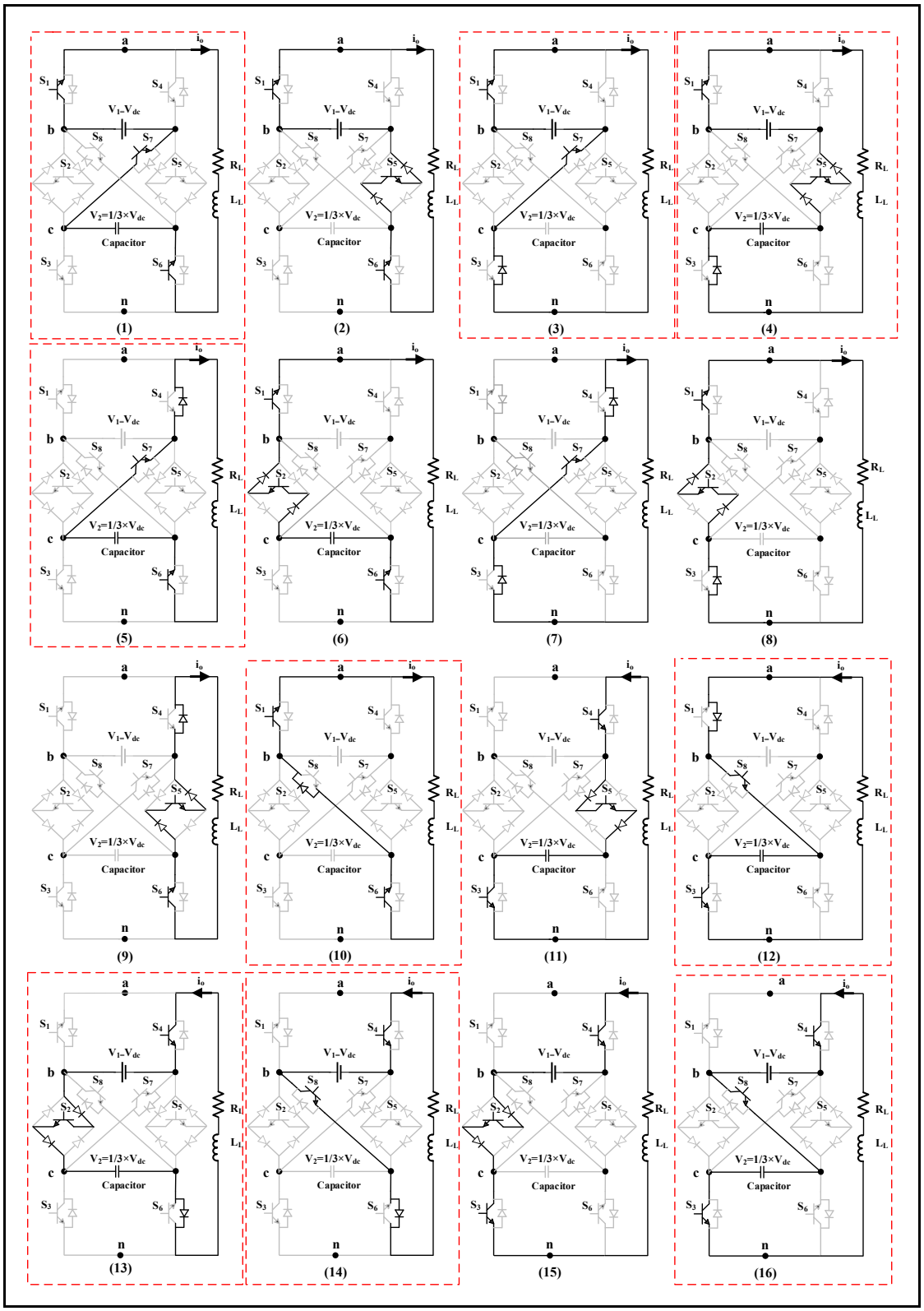


Figure 4.2 Current path in each switching state of Table 4.1

Due to decreasing the fabrication cost in experimental design, I did not want to use expensive Schottky diodes. As a result, I preferred to use ultra-fast standard diodes but I decreased the usage of these diodes as far as I could to reduce the losses in the circuit. Consequently, I used only highlighted switching states in table 4.1 and figure 4.2 in my application. In this situation, I figured out that only two unidirectional voltage-blocking switches are enough for this topology instead of bidirectional voltage blocking diodes. Figure 4.3 illustrates the power circuit connection of this topology and Table 4.2 compares some existing nine level topologies and the proposed topology.

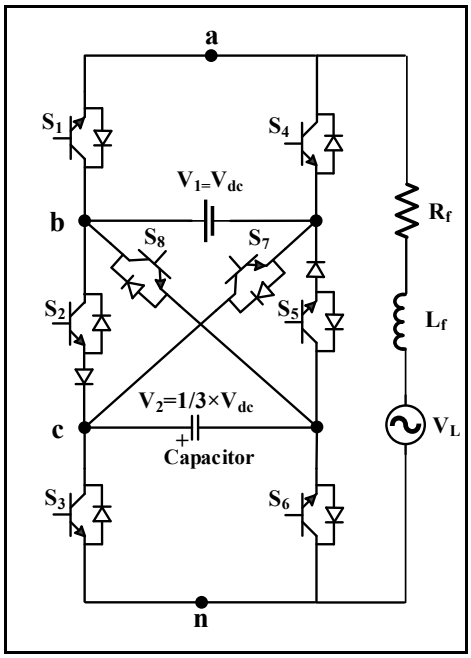


Figure 4.3 UX-Cell in grid-connected mode

Table 4.2 Comparison between other nine-level inverter topologies and UX-Cell

	NPC	**FC**	**Classic CHB**	**Hybrid CHB**	**PUC**	**PEC**	**UX-Cell**
No of Capacitors	8	8	3	2	2	2	1
No of Diodes	14	0	0	0	0	0	2
No of Switches	16	16	16	12	8	8	8
Boosting	0%	0%	0%	0%	0%	0%	33%

4.3 Model predictive control design

Most of the conventional control methods have their own disadvantages, for example a lot of calculations, working only in stand-alone mode or needing bulky capacitors, etc. Model predictive control, however, is rather simple and needs lower number of computations. In addition, it is appropriate for both grid-connect and stand-alone applications. Moreover, the size of capacitors can be decreased remarkably with MPC, which results in reduced cost of manufacturing. The concept of MPC is not complicated. Through measuring the present value of variables of our system, the future behavior of the system is predicted (Abarzadeh & Al-Haddad, 2018; Falkowski & Sikorski, 2018; Kouro et al., 2009; Sebaaly et al., 2018; Trabelsi et al., 2016; Venkata & Bin, 2017). The appropriate switching state is then applied based on these predictions.

Where i= (1, 2, 3, 4) the definition of $S_i$is as per below.

$$S_i = \begin{cases} 0 \; if \; S_i \; is \; off \\ 1 \; if \; S_i \; is \; off \end{cases} \tag{4.1}$$

Based on Figure 4.1, it can be said that

$$V_{ae} = V_{ab} + V_{bc} + V_{cn} \tag{4.2}$$

$$\begin{cases} V_{ab} = \; -(1 - S_1) \times V_{dc} \\ V_{bc} = \; (1 - S_2) \times [S_7 V_{dc} - S_8 V_c + S_5 (V_{dc} - V_c)] \\ V_{cn} = \; (1 - S_3) \times V_c \end{cases} \tag{4.3}$$

$$\begin{cases} i_1 = S_1 i_L \\ i_2 = S_2 i_L \\ i_3 = S_3 i_L \\ i_4 = S_4 i_L \end{cases} \tag{4.4}$$

$$V_{an} = V_L + (i_L \times R_f) + (L_f \times \frac{di_L}{dt}) \tag{4.5}$$

Where V_{an} is inverter output voltage vector, i_L is load current, $V_L$is active load voltage, R_f is load resistance, L_f is load inductance, V_{dc} is the voltage of DC voltage source, and $V_c$is capacitor voltage. According to Euler, forward approximation, $\frac{di_L}{dt}$ is defined as:

$$\frac{di_L}{dt} \approx \frac{i_L(k+1) - i_L(k)}{T_s} \tag{4.6}$$

From (4.5) and (4.6), it can be written that:

$$i_L(k+1) = \left(1 - \frac{R_f \times T_s}{L_f}\right) \times i_L(k) + \frac{T_s}{L_f} \times \left(V_{ae}(k) - \widehat{V_L(k)}\right) \tag{4.7}$$

Where $i_L(k+1)$ is the predicted load current, $\widehat{V_L(k)}$is the predicted load voltage. Regarding equations (4.5) and (4.3), $V_{ae}(k)$ is calculated as per below:

$$V_{ae}(k) = (S_1 - S_2 - S_8) \times V_{dc}(k) + (S_2 - S_3 + S_7) \times V_C(k) \tag{4.8}$$

Referring to the fact that the load voltage variation in comparison with sampling frequency is negligible, it can be written that $V_L(k-1) = \widehat{V_L(k)}$, thus $V_L(k)$ in equation (4.7) can be replaced by $V_L(k-1)$.

Employing Ohm's Law for capacitors,

$$i_c = C\frac{dV_C}{dt} = (S_3 - S_2 - S_7) \times i_L \tag{4.9}$$

Where i_c is instantaneous current through capacitor one, C is the capacitance of capacitor one, and $\frac{dV_C}{dt}$ is instantaneous rate of voltage change of capacitor one. It should be mentioned that capacitor current is approximated when internal resistance of capacitors is ignored. Applying Euler forward approximation, $\frac{dV_C}{dt}$ is obtained as

$$\frac{dV_C}{dt} \approx \frac{V_C(k+1) - V_C(k)}{T_s} \tag{4.10}$$

Replacing (4.10) in (4.11), (4.12) is obtained

$$V_C(k+1) = \frac{(S_3 - S_2 - S_7)}{C_1} \times i_L(k) \times T_s + V_C(k) \tag{4.11}$$

The cost function g is formulated as:

$$G = K_1 \times (i_L(k+1) - i_L(K+1)^*)^2 + K_2 \times (V_C(k+1) - V_C(K+1)^*)^2 \tag{4.12}$$

Where K_1, K_2 are weighting factors used to prevent different variables' coupling effects. The cost function g is calculated for nine possible switching states of Table 4.1 in each sampling time. Then, the switching state is selected that minimizes the cost function. Figure 4.4 shows the block diagram of MPC for UX-Cell MLI in grid-connected mode.

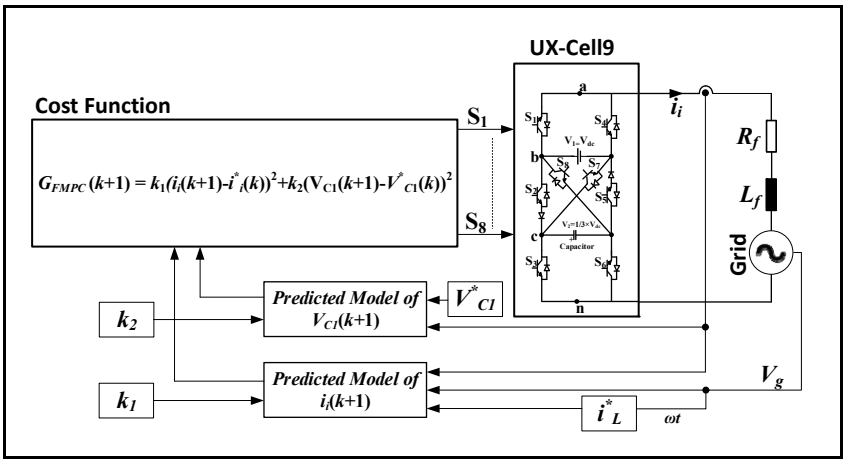


Figure 4.4 Block diagram of MPC for Grid-connected UX-Cell MLI

4.4 Simulation parameters

The parameters used during simulations are indicated in Table 4.3. According to Table 4.1, the V_C voltage must be equal to $1/3 \times V_{dc}=50$. It should be mentioned that S_7, S_8 must support

$4/3\times V_{dc}$, when the S_1, S_2, S_4, S_5, must support V_{dc}, and Switches S_3, S_6 must only support 1/3 V_{dc}. Figure 4.4 shows MPC flowchart for grid-connected UX-Cell MLI. Firstly, the reference current decreases from 10A to 5A and then returns to 10A again, while Vdc=153V, and AC Grid Voltage is equal to 120 V RMS. Figure 4.5 illustrates inverter voltage (V_{an}) and grid current (i_L) in the first step. Secondly, DC voltage source increases from 153 V to 195 V, while AC Grid Voltage is equal to 120 V RMS. Figure 4.6-7 indicates capacitors voltage (V_{dc}, V_c), inverter voltage (V_{an}), grid current (i_L), and grid voltage in point of common coupling (V_{PCC}) in the second step. Figure 4.8-13 shows total harmonic distortion (THD) of inverter voltage, grid current, and grid voltage in point of common coupling respectively, while DC voltage source is equal to 153 V, and 195 V when AC grid voltage is stable at 120 V RMS. It can be seen that the THD of grid voltage in point of common coupling is equal to 2.99% when Vdc=153 and it is equal to 5.29% when Vdc=195, which is satisfactory. Finally, DC voltage source is considered stable at 170 V and the grid voltage is reduced from 138 V RMS to 108 V RMS and THD of different points is obtained (See Figure 4.14-20). It should be mentioned that $\omega\tau$ of the gird voltage (utilizing PLL) is used to generate the reference current for MPC.

4.5 Simulation Results

The parameters used in the simulation have been shown in Table 4.3. Figure 4.5 illustrates the flow chart of proposed control technique. Figure 4.6 depicted inverter voltage (V_{an}) and Grid current (i_L) while the reference current is changed from 10A to 5A and is returned to its initial value. In the next step, the DC voltage source is changed from 153 V to 195 V. Figures 4.7-4.21 indicate the output parameters and THD analysis of our system before and after this change. It can be seen that the capacitor voltage is balanced to its desired value and it has very small and acceptable ripple; in addition, it is obvious that the system has fast transient and the output THD of the system is acceptable in different points. For example, the THD of output current is below 2.25%, which is acceptable; furthermore, the THD of inverter output voltage when dc voltage is equal to 153 V is 17.95%, which is proper for a nine-level inverter. It should be mentioned that when the grid voltage is 120 V RMS (170 V peak-to-peak) and V_{dc}=195V, the controller decreases two levels from inverter output voltage in order to adapt the output of

the inverter with the grid voltage. As a result, the THD of output voltage in this situation is equal to 31.71%.

Table 4.3 Main System Parameters

Parameters	Value
Sampling Time	10 μs
DC Voltage Source	153V & 195V
Capacitor(C)	560 μF
Line inductance	2.5 mH
Grid inductance	500 μH
AC Grid voltage	108,120V,138V RMS
Reference Current	10A & 5A

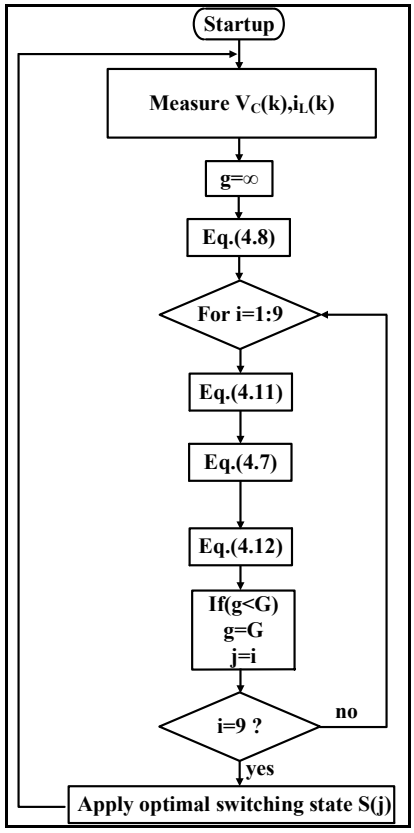


Figure 4.5 Flowchart of MPC for Grid-connected UX-Cell MLI

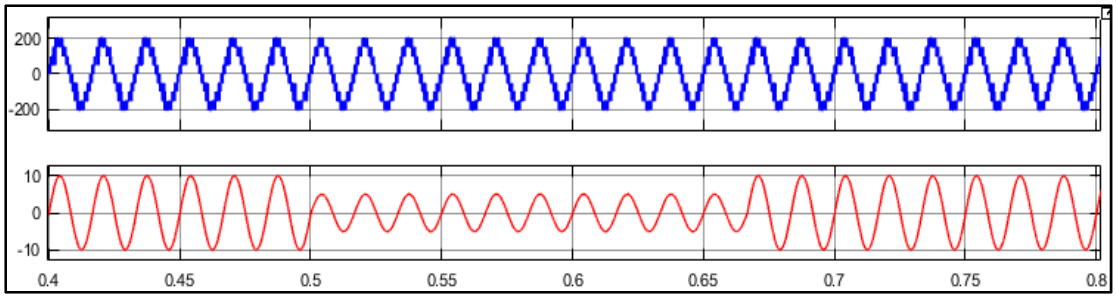


Figure 4.6 Inverter voltage (V_{an}) and Grid current (i_L)

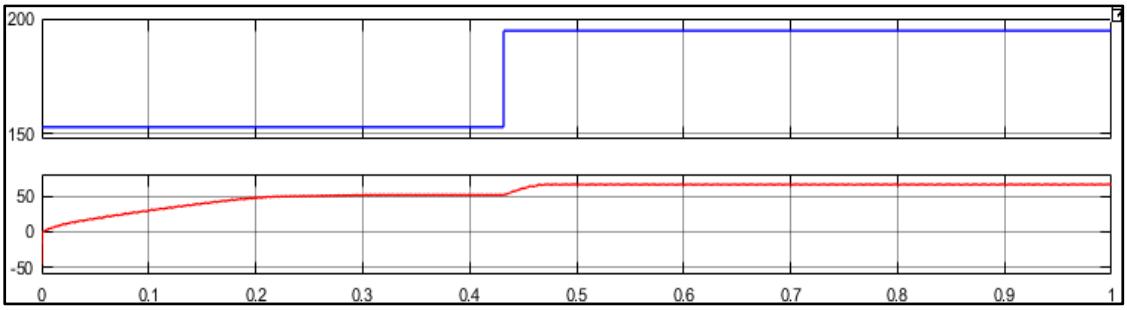


Figure 4.7 Capacitors voltage (V_{dc}, V_c)

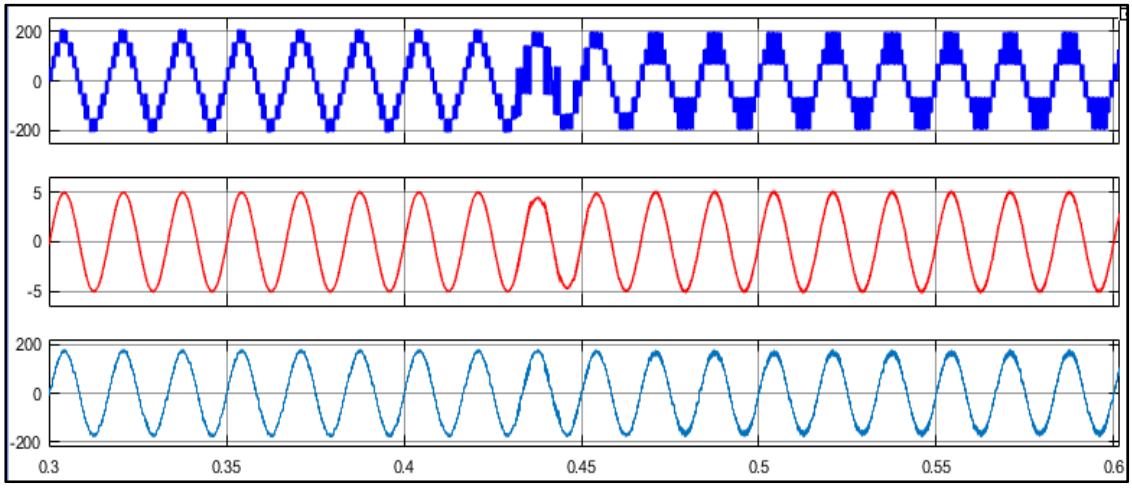


Figure 4.8 Inverter voltage (V_{ae}), Grid current (i_L), Grid Voltage in PCC (Vpcc)

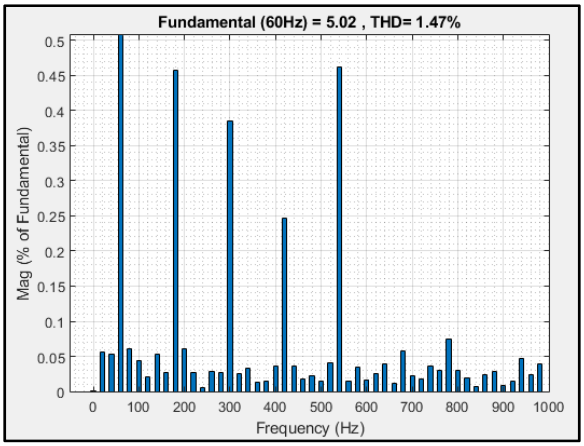


Figure 4.9 THD of grid current (i_L) while V_{DC}=153V and V_{GRID}=120V RMS

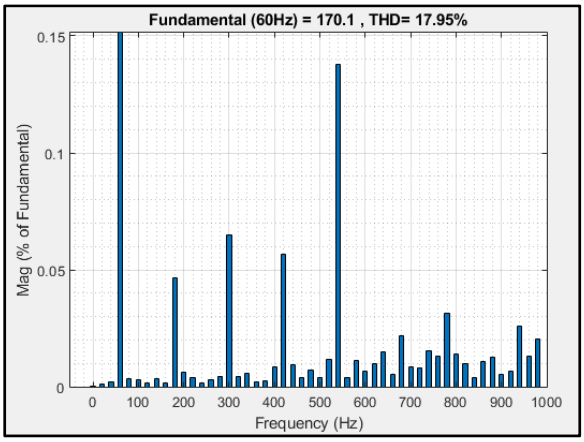


Figure 4.10 THD of inverter voltage (V_{ae}) while V_{DC}=153V and V_{GRID}=120V RMS

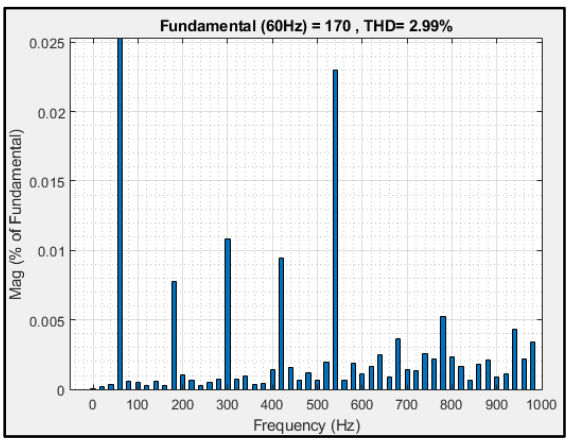


Figure 4.11 THD of Grid voltage in PCC (V_{PCC}) while V_{DC}=153V and V_{GRID}=120V RMS

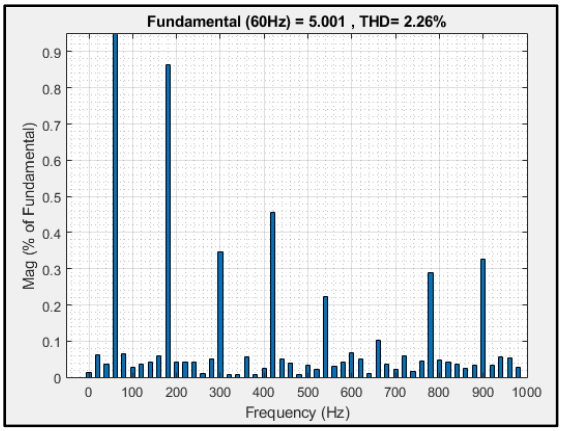


Figure 4.12 THD of grid current (i_L) while V_{DC}=195V and V_{GRID}=120V RMS

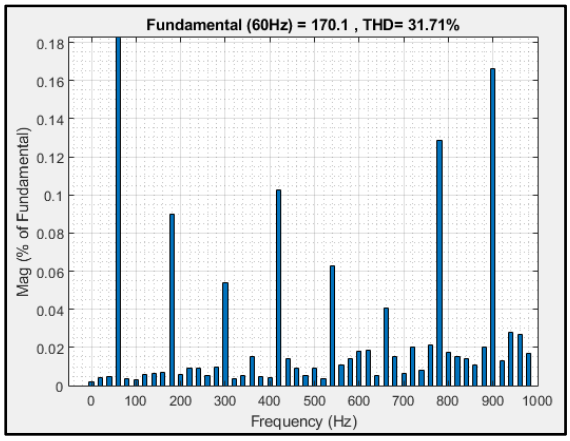


Figure 4.13 THD of inverter voltage (V_{ae}) while V_{DC}=195V and V_{GRID}=120V RMS

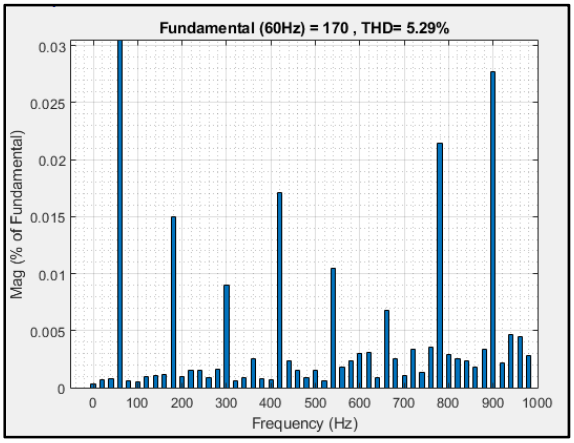


Figure 4.14 THD of Grid voltage in PCC (V_{PCC}) while V_{DC}=195V and V_{GRID}=120V RMS

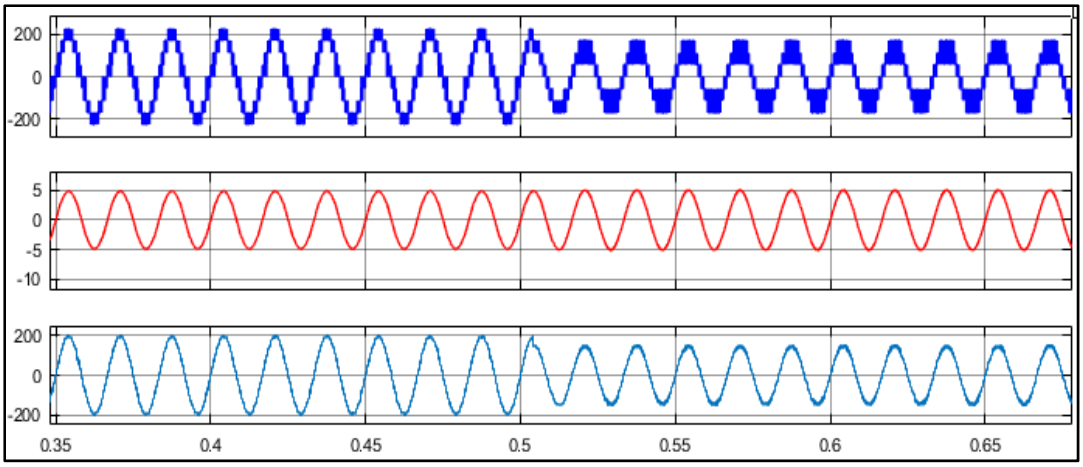


Figure 4.15 Inverter voltage (V_{ae}), Grid current (i_L), Grid Voltage in PCC (V_{pcc})

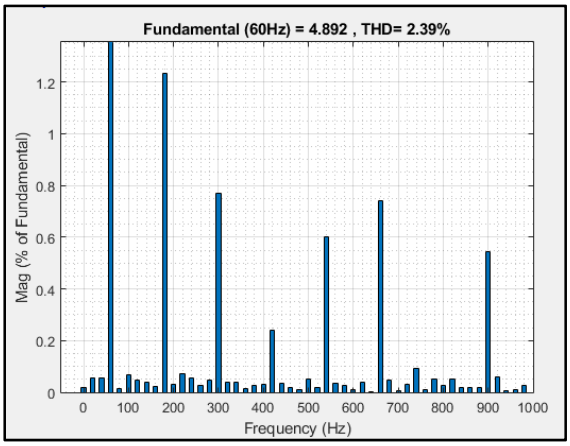


Figure 4.16 THD of grid current (i_L) while V_{DC}=170V and V_{GRID}=138V RMS

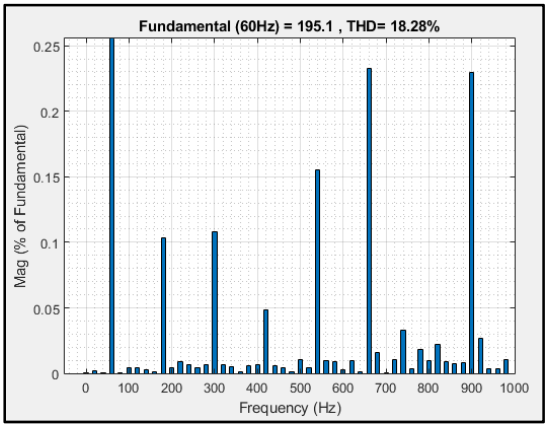


Figure 4.17 THD of inverter voltage (V_{ae}) while V_{DC}=170V and V_{GRID}=138V RMS

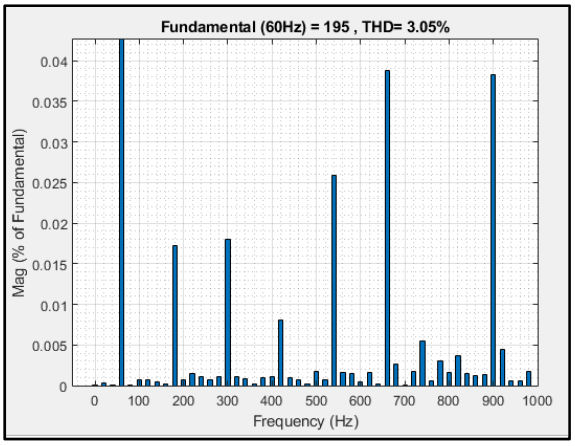


Figure 4.18 THD of Grid voltage in PCC (V_{PCC}) while V_{DC}=170V and V_{GRID}=138V RMS

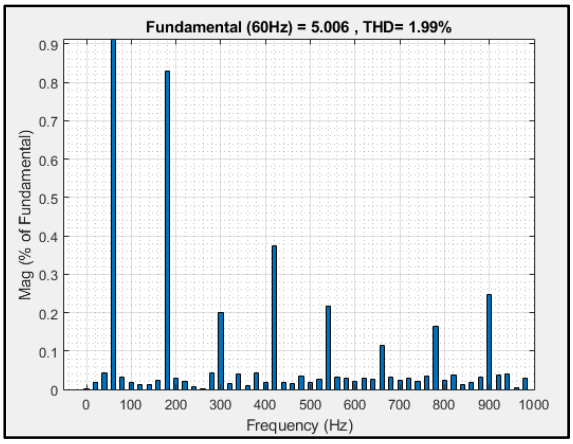


Figure 4.19 THD of grid current (i_L) while V_{DC}=170V and V_{GRID}=108V RMS

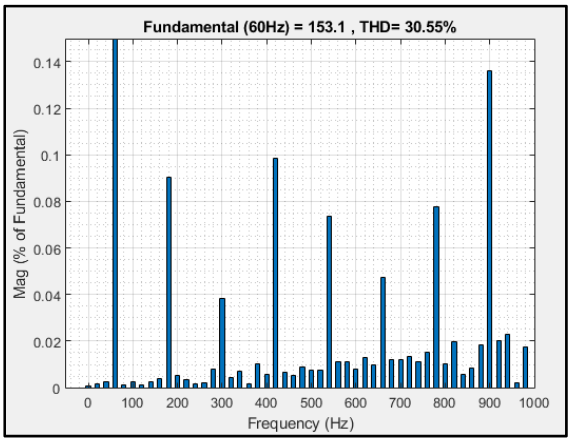


Figure 4.20 THD of inverter voltage (V_{ae}) while V_{DC}=170V and V_{GRID}=108V RMS

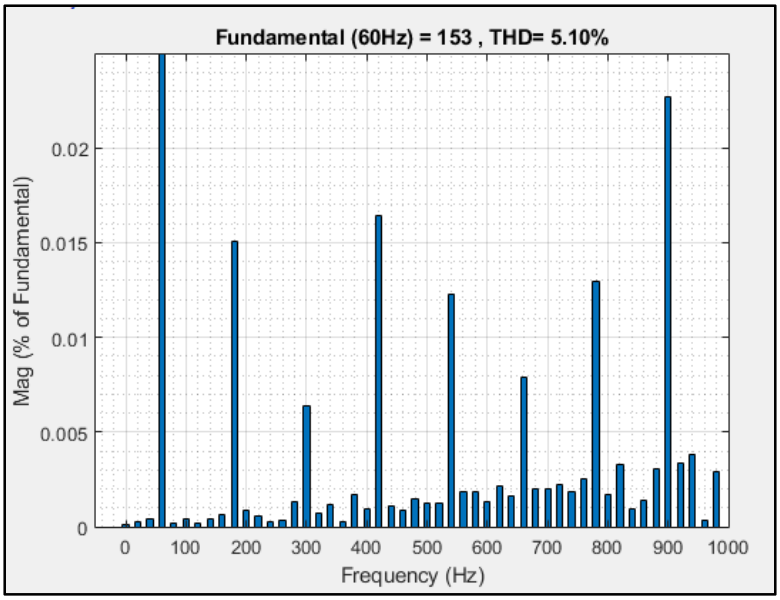


Figure 4.21 THD of Grid voltage in PCC (V_{PCC}) while V_{DC}=170V and V_{GRID}=108V RMS

4.6 Experimental Results

For obtaining experimental results; first, the PCB of UX-Cell inverter is designed with Altium designer software, then through using dSpace 1103 controller and OPAL-RT high current/high-voltage measurement, the proposed control technique is applied on this inverter topology. Figure 4.22 shows grid voltage, inverter output voltage, inverter output current, and V_{dc} in stable conditions for grid-connected modes of operation. Figures 4.23-4.24 illustrate above-mentioned parameters when reference current is raised from 2A to 4A, and DC voltage source is increased from 50 V to 60 V, in order.

Table 4.4 Main System Parameters

Parameters	Value
Sampling Time	46 µs
DC Voltage Source	50V & 60V
Capacitor(C)	560 µF
Line inductance	2.5 mH
AC Grid voltage	35V RMS
Reference Current	2A & 4A

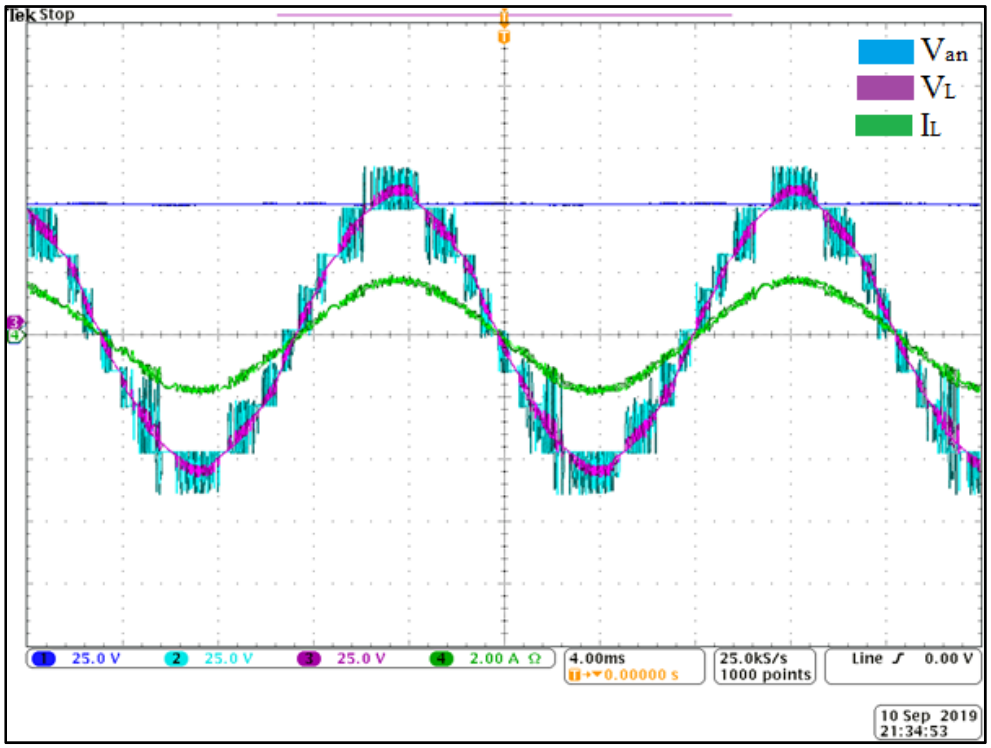


Figure 4.22 Grid voltage, output voltage, output current, and V_{dc} in grid-connected mode

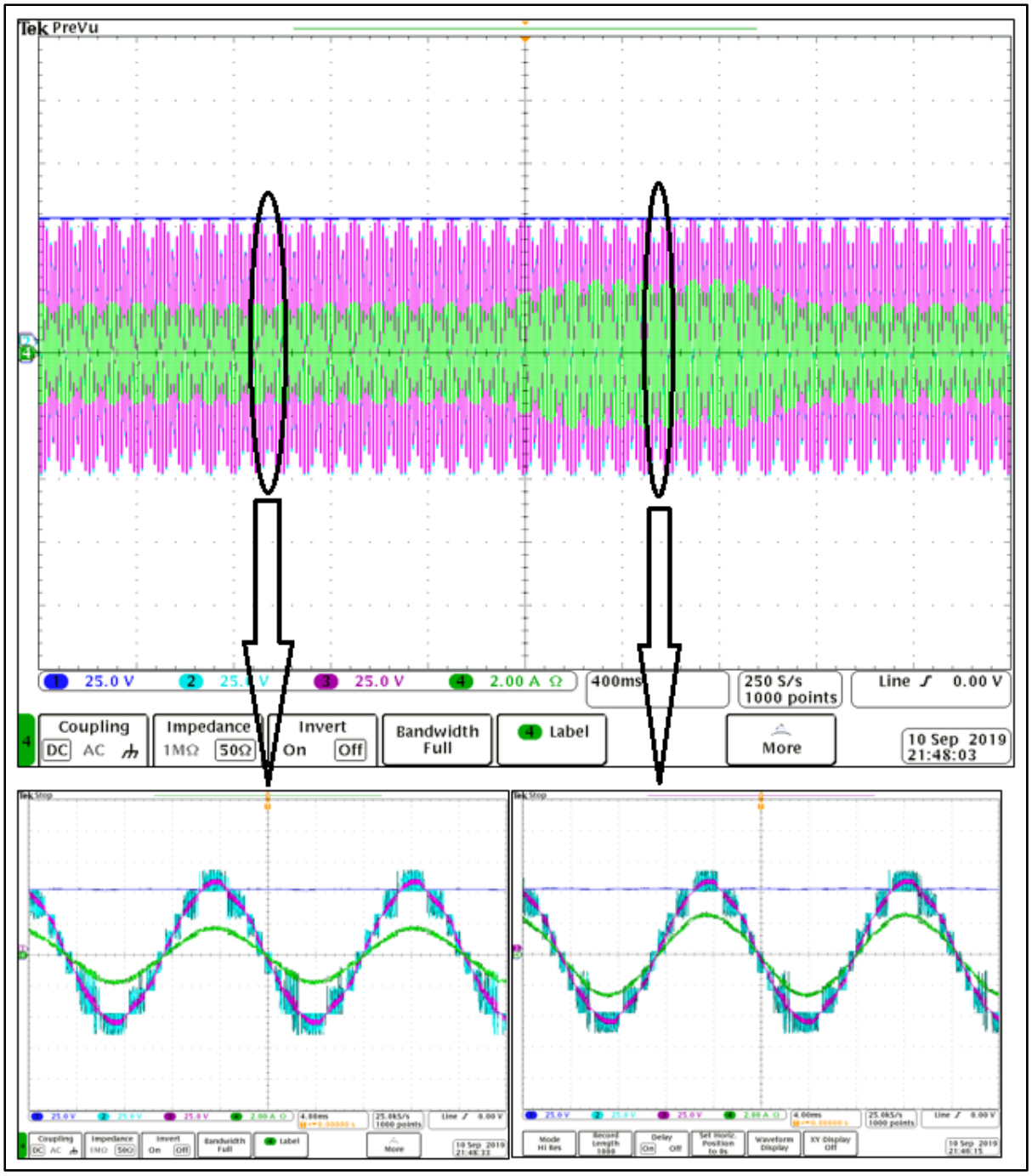


Figure 4.23 Reference current is changed from 2A to 4A

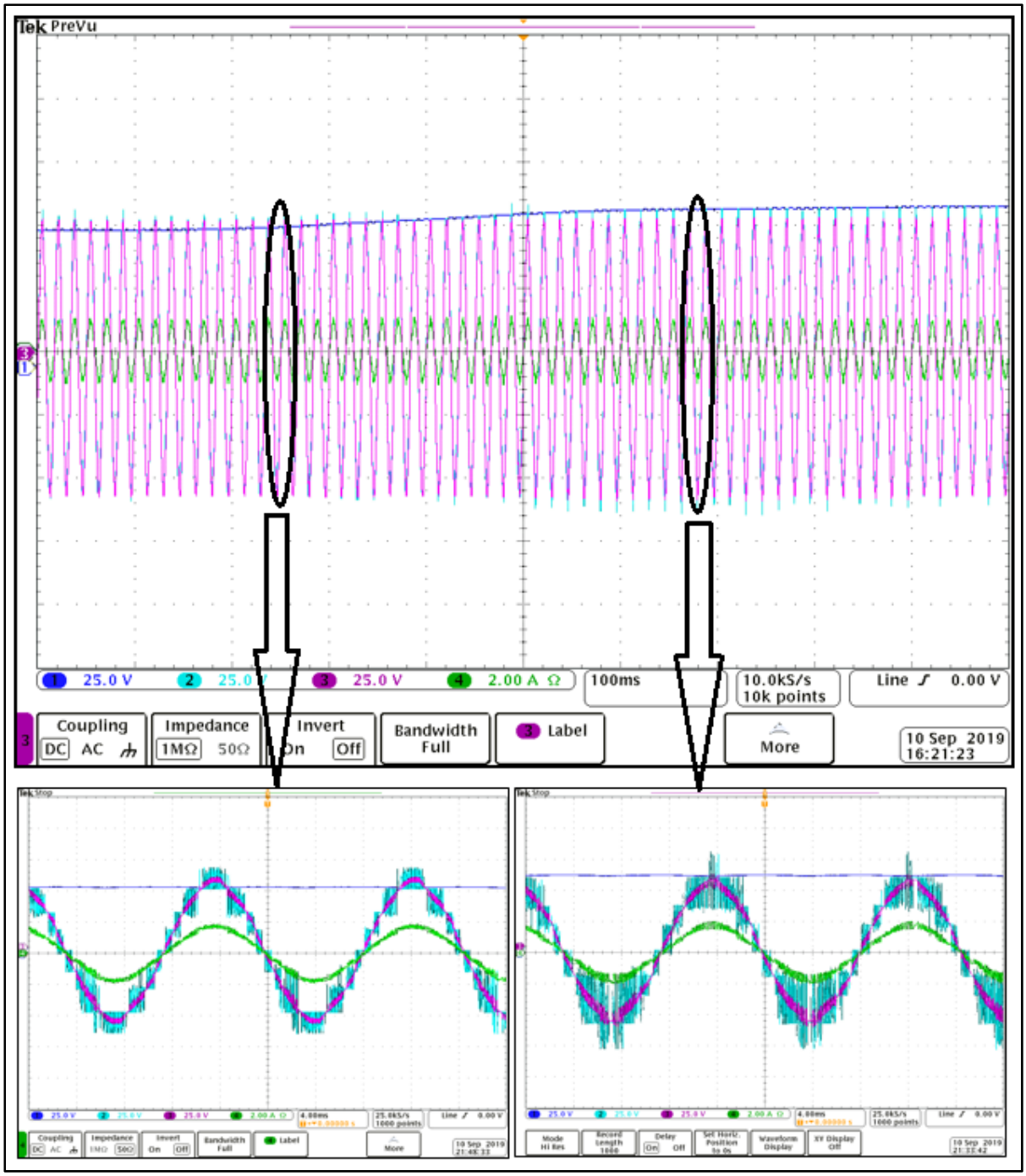


Figure 4.24 DC voltage source is changed from 50V to 60V

4.7 Conclusion

Nowadays, PUC topology is known as highly efficient and low manufacturing cost MLI in industry and also among power electronic researchers. The proposed UX-Cell topology in this chapter is created by adding two switches to PUC7 topology and it has all features of PUC MLI while it has one less capacitor and boosting ability, which make it interesting for photovoltaic power system applications. Besides, the main problem of asymmetric MLI is voltage balancing of the capacitors because the voltage of dc source and capacitors must be set in different values. There are plenty of control techniques for voltage balancing of capacitors and output current control like PWM control, and hysteresis control, etc. Most of these control techniques have disadvantages like time-consuming process of tuning PID controller, working in only stand-alone or grid-connected mode, needing long and complicated calculations, etc. In this chapter, model predictive control was applied on UX-Cell MLI. PMC is a highly efficient discrete control technique for regulation of load current and balance capacitors' voltage. It has none of above-mentioned disadvantages, but in MPC the switching frequency is not fixed. The proposed MPC was verified by simulation using Matlab Simulink and Sim power system and it was validated experimentally using Opal-RT voltage/current measurement and dSpace 1103. The simulation results as well as experimental results show the fast transient of MPC technique and negligible capacitor voltage ripple and the results are promising and satisfactory.

CHAPTER 5

SENSORLESS OPERATION OF NINE-LEVEL UX-CELL INVERTER TOPOLOGY

5.1 Introduction

Nowadays, researchers tend to pay special attention to Sensorless control technique because in this method there is no need to use expensive isolated measurement sensors for measuring voltages in converter topologies. Although with increasing the fabrication technology, the cost of these sensors has decreased remarkably, but high precision and the accurate sensors are still expensive. Applying sensorless control technique can reduce production cost of MLI; consequently, the usage of these inverters will rise, especially for utilizing them in renewable energy converters in homes and industrial applications and it will have positive effects on the environment.

5.2 PWM Sensorless control technique on nine-level UX-Cell MLI

The basic concept of sensorless technique is simple. When the energy that a capacitor C absorbs is equal to the energy that is delivered or supplied, the voltage level of that capacitor will always remain stable (Abarzadeh, Vahedi, & Al-Haddad, 2019; Ounejjar, Gadari, Abarzadeh, & Al-Haddad, 2018; Vahedi et al., 2016). Using sensors for capacitor voltage balancing in this topology needs at least two sensors for measuring capacitors voltages as well as dc supply voltage. Figure 4.3 illustrates power circuit of UX-Cell MLI. In this converter, although this topology has seven redundant switching states, these redundant switching states do not have any effects on charging or discharging the capacitor. As a result, the proposed method in chapter 3 is not applicable on this converter. The proposed sensorless control strategy contains only the LS-PWM switching technique. In the proposed balancing technique in open-loop controller, it means that for this voltage balancing technique there is no need for controller or state variable feedback. As a result, it has very simple implementation as well as fast dynamics. In this technique, there are eight sawtooth waveforms, which are placed vertically between +1 and -1. Given that UX-Cell MLI is a nine-level inverter and the carriers

must have the same frequency and peak-to-peak amplitude, the amplitude of each carrier must be equal to 0.25 (see figure 5.1). A sinusoidal reference waveform is compared to these sawtooth waveforms. Figure 5.2 and equation 5.1 show the process of this comparison and figure 5.3 depicts the output waveform of proposed technique (Ounejjar et al., 2011), which is S signal. Finally, S signal specifies the desired switching state among switching states that are highlighted in gray in table 4.1.

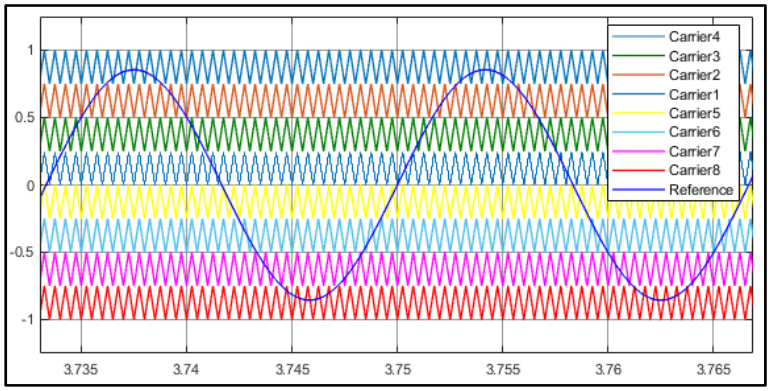


Figure 5.1 Carriers and sinusoidal reference waveforms in LS-PWM

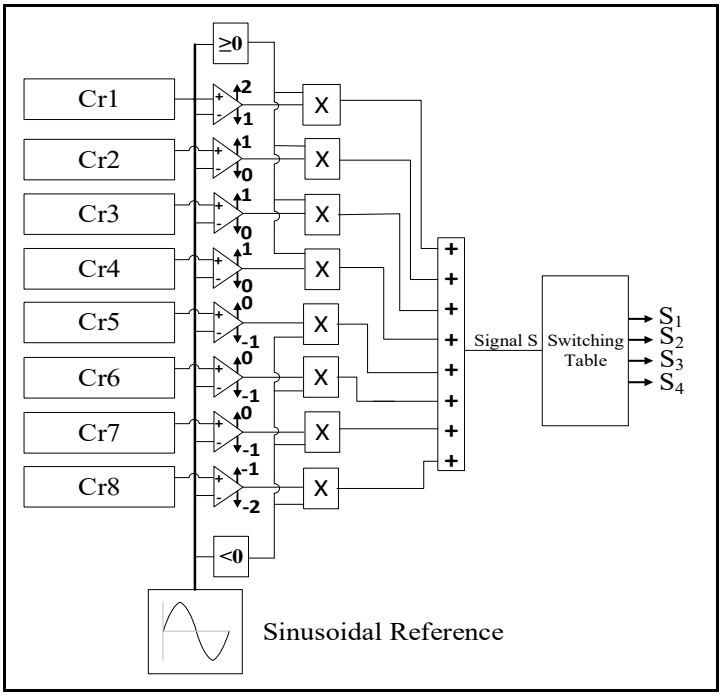


Figure 5.2 Proposed sensorless technique

$$\begin{cases} \text{If } V_{ref} \geq Cr_1 & \rightarrow \text{Switching signal} = +5 \\ \text{If } Cr_2 \leq V_{ref} < Cr_1 & \rightarrow \text{Switching signal} = +4 \\ \text{If } Cr_3 \leq V_{ref} < Cr_2 & \rightarrow \text{Switching signal} = +3 \\ \text{If } Cr_4 \leq V_{ref} < Cr_3 & \rightarrow \text{Switching signal} = +2 \\ \text{If } 0 \leq V_{ref} < Cr_4 & \rightarrow \text{Switching signal} = +1 \\ \text{If } Cr_5 \leq V_{ref} < 0 & \rightarrow \text{Switching signal} = -1 \\ \text{If } Cr_6 \leq V_{ref} < Cr_5 & \rightarrow \text{Switching signal} = -2 \\ \text{If } Cr_7 \leq V_{ref} < Cr_6 & \rightarrow \text{Switching signal} = -3 \\ \text{If } Cr_8 \leq V_{ref} < Cr_7 & \rightarrow \text{Switching signal} = -4 \\ \text{If } Cr_8 > V_{ref} & \rightarrow \text{Switching signal} = -5 \end{cases} \quad (5.1)$$

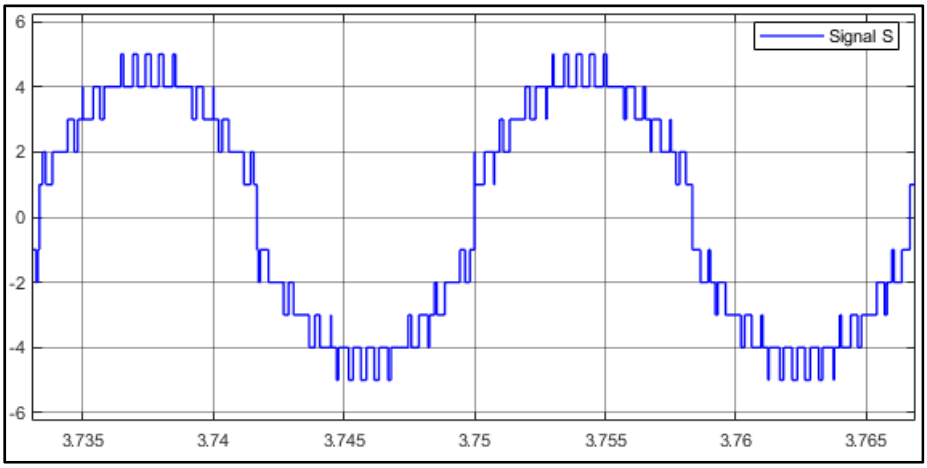


Figure 5.3 Signal S

5.3 Simulation results

Table 5.1 shows system parameters during simulation with Matlab Simulink and Sim power system. Figures 5.4-5.8 depict V_{dc}, V_c, V_{an}, THD of V_{an}, I_o, and THD of I_o respectively in stable condition when V_{dc}=300V and R_L =40Ω. In order to test the dynamic of proposed sensorless voltage balancing technique, first DC supply is decreased from 300 V to 150 V and is then returned to 300 V. After that, the load is changed from 40Ω to 20Ω (See Figures 5.9-5.12). It can be seen that when the voltage of dc supply is equal to 300 V, inverter output voltage is equal to $400V_{peak\text{-}to\text{-}peak}$. It means that UX-Cell topology has boosting ability, which is a remarkable advantage of it.

Table 5.1 Main System Parameters

Parameters	Value
Sampling Time	10 µs
DC Voltage Source	150V & 300V
Capacitor	560 µF
Load inductance	20mH
Load resistance	40Ω, 20Ω
Switching Frequency	2 kHz

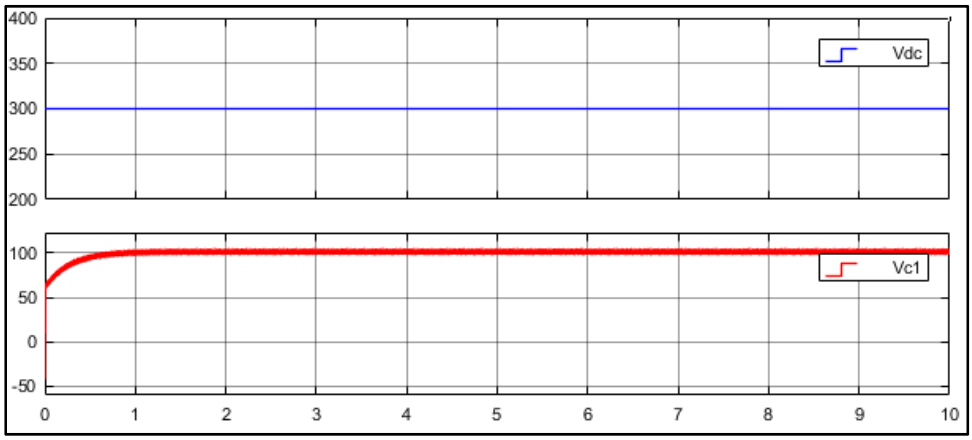


Figure 5.4 Capacitors voltage V_{dc}, V_c in stable condition

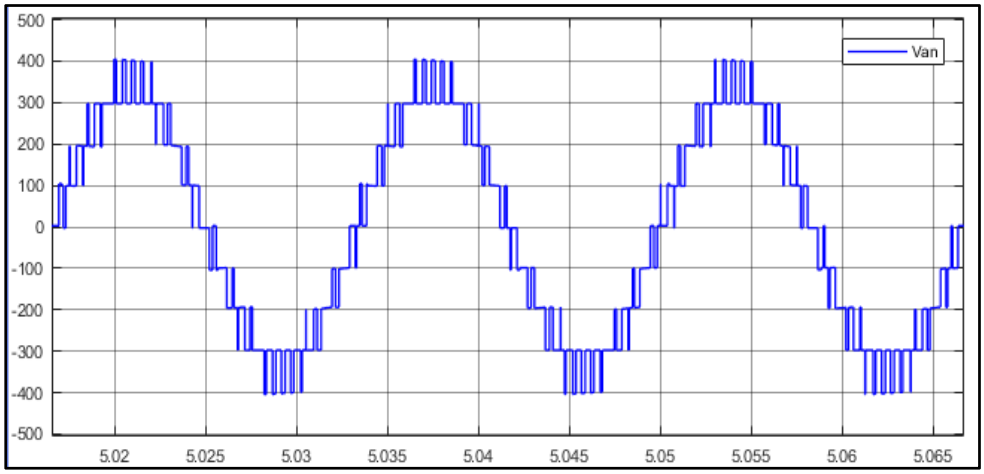


Figure 5.5 Inverter output voltage in stable condition when Vdc=300V

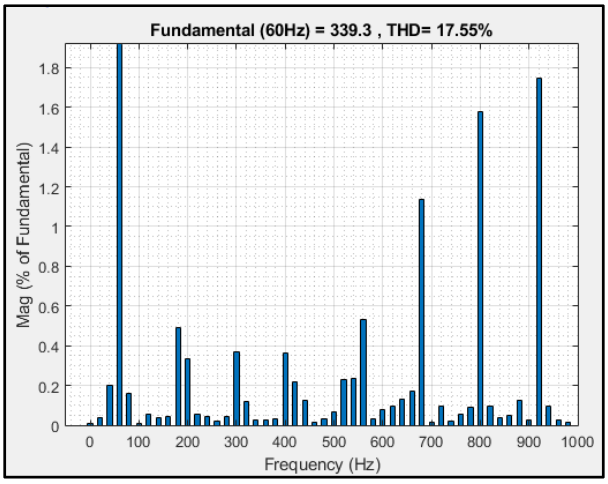


Figure 5.6 THD of inverter output voltage in stable condition when V_{dc}=300V

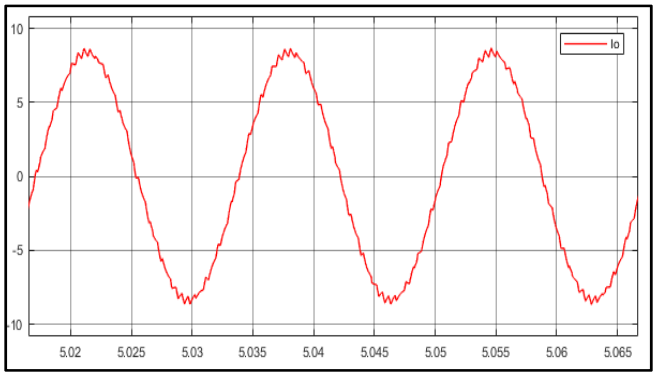


Figure 5.7 Output current when R_L=40Ω and V_{dc}=300V

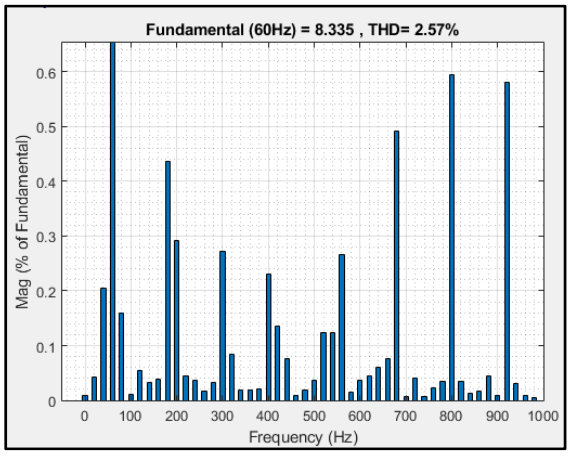


Figure 5.8 THD of output current when R_L=40Ω and V_{dc}=300V

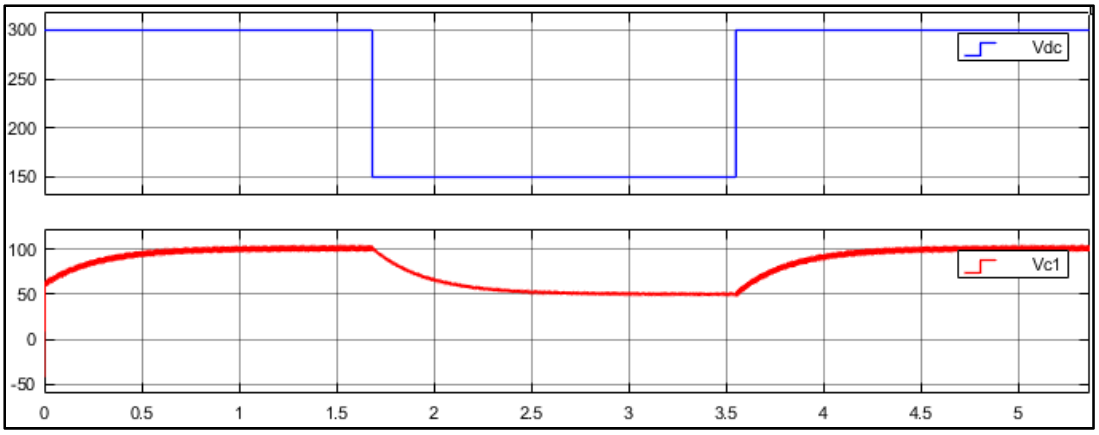


Figure 5.9 DC voltage source is changed from 300V to 150V

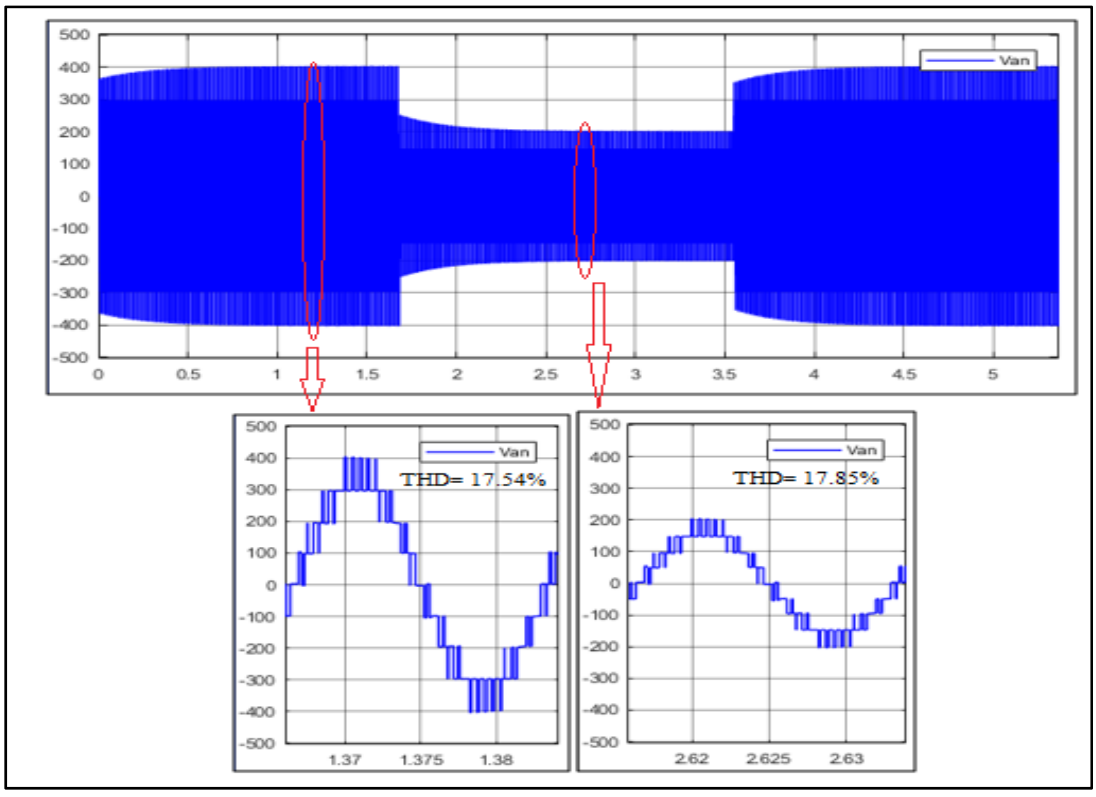


Figure 5.10 V_{an} when the voltage of DC supply is changed from 300V to 150V

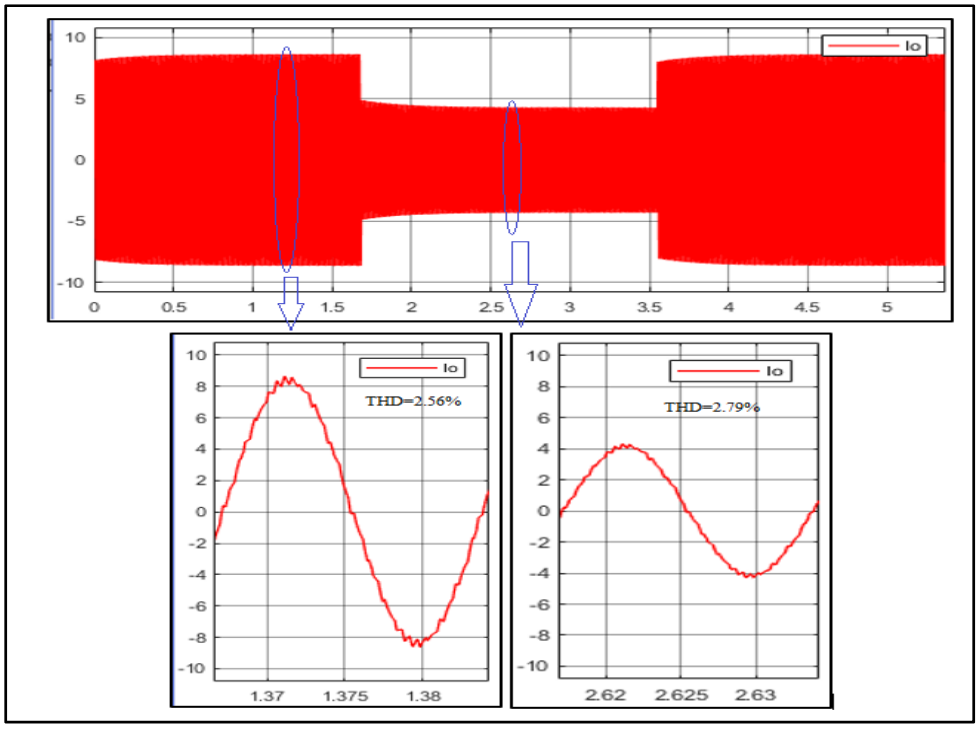


Figure 5.11 Output current when the voltage of DC supply is changed from 300V to 150V

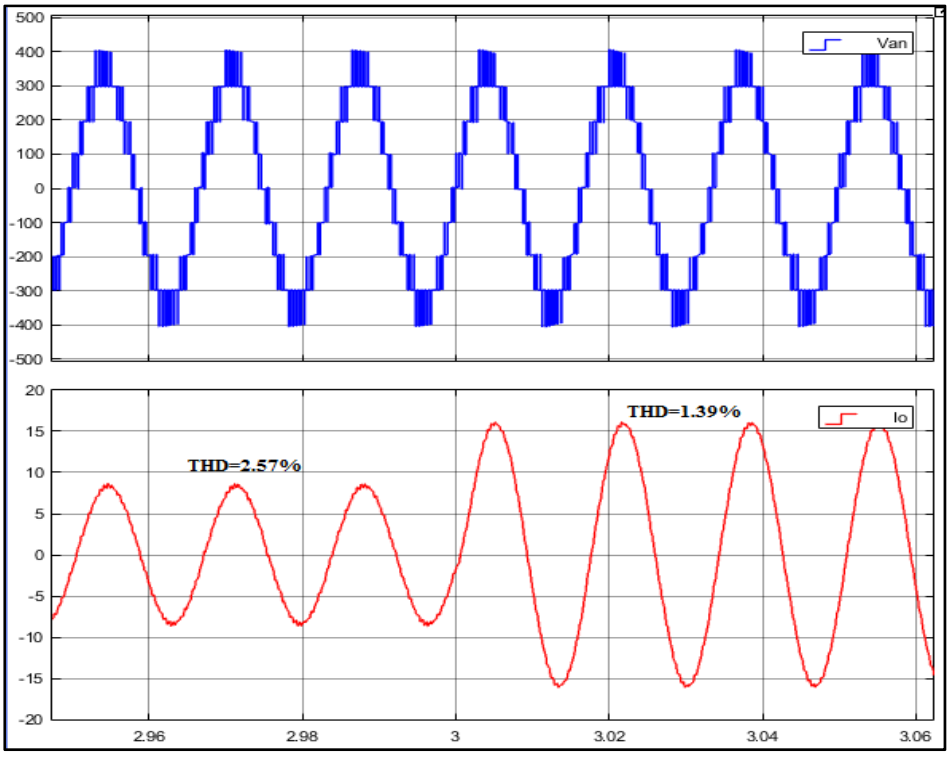


Figure 5.12 Output voltage and output current when the load is changed from 40Ω to 20Ω

5.4 Experimental results

In order to gain the experimental results, the PCB that was designed for the previous chapter by using the Altium designer software is used plus dSpace 1103 controller and OPAL-RT high current/high-voltage measurement like Chapter 4. Figures 5.13-5.15 indicate the output current, output voltage, the voltage of the capacitor and voltage of DC source in different conditions. First, it shows above-mentioned parameters in stable condition, when the load is changed from 80Ω to 160Ω and is returned to its initial value. Finally, dc source is increased from 120 V to 150 V. In experimental results as well as simulation results, it is obvious that the voltage of the capacitor is balanced in desired level and the proposed technique has fast transient.

Table 5.2 Main System Parameters

Parameters	Value
Sampling Time	46 µs
DC Voltage Source	120V & 150V
Capacitor	560 µF
Load inductance	20mH
Load resistance	80Ω, 160Ω
Switching Frequency	2 kHz

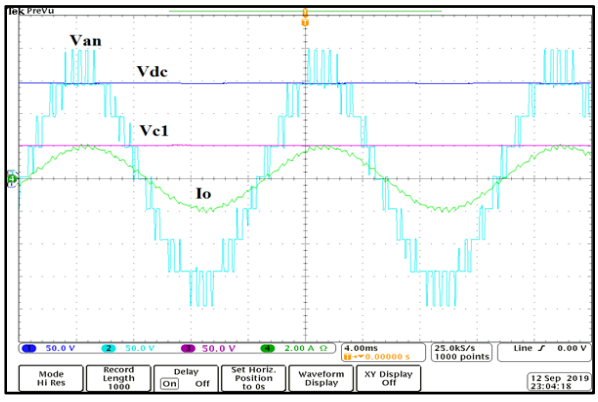


Figure 5.13 Stable condition (RL load 80Ω, 20mH, and Vdc=150)

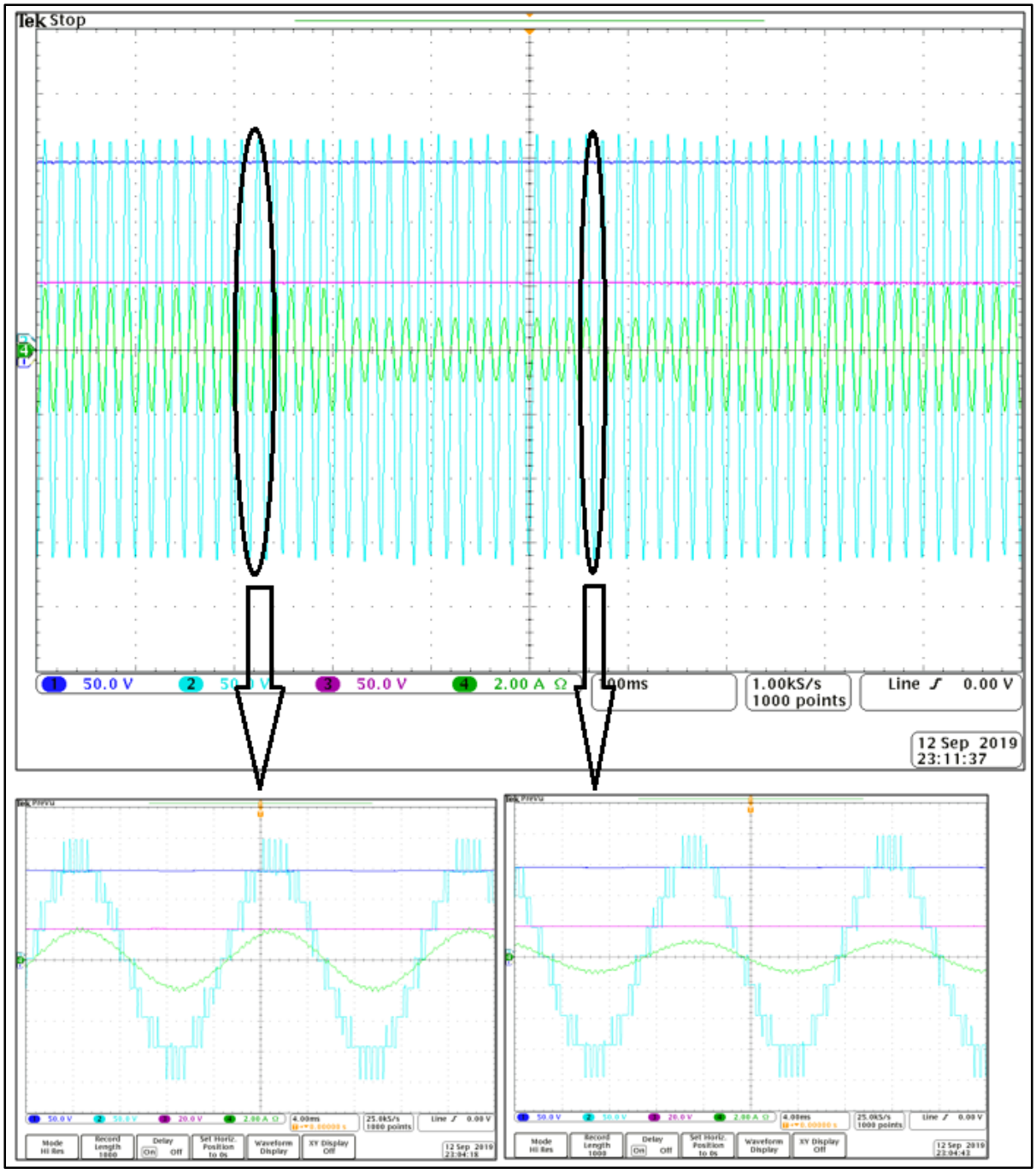


Figure 5.14 Step load change from 80Ω to 160Ω

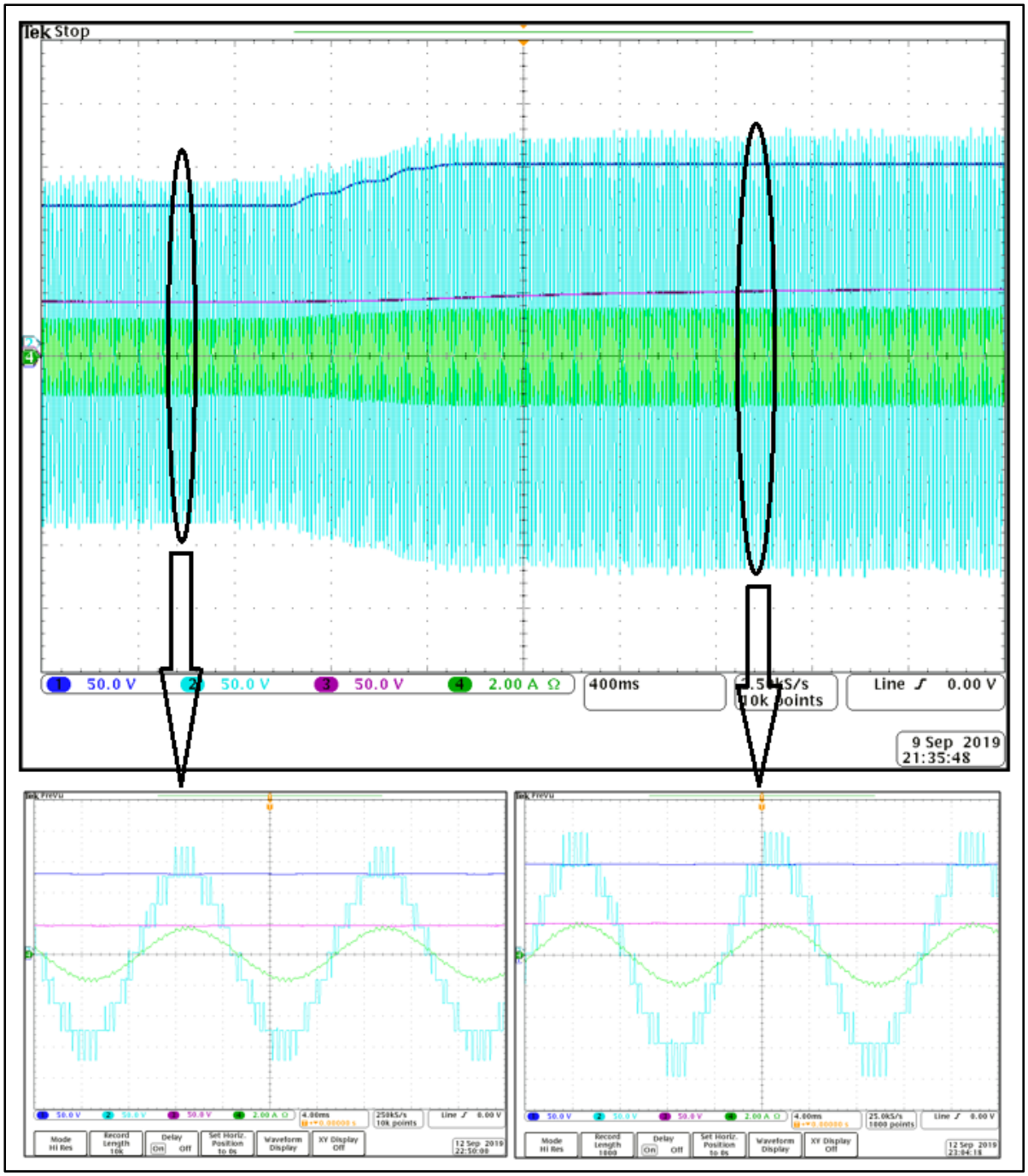


Figure 5.15 DC source change from 120V to 150V

5.5 Conclusion

For measuring the voltage of capacitors in close-loop operations, an additional circuit including a voltage sensor plus an isolated voltage source is needed. These voltage sensors are normally expensive; moreover, designing an isolated DC source is not an easy task and it has additional charge for fabrication. As a result, these days Sensor-less or self-balancing technique is an interesting method for industry and researchers because it decreases the fabrication cost with omitting additional circuit for measuring the voltage of capacitors. In this chapter, the proposed sensor-less method was verified by simulation results and also experimental results. It can be seen that the output voltage THD is equal to 17.57% and voltage ripple of capacitor is less than 5%, which is acceptable and satisfactory. On the other hand, it has disadvantages like needing bulky capacitors or slow transient in comparison with close-loop techniques.

CONCLUSION

To sum up, PUC MLI is a promising topology, which is able to generate maximum output level while using minimum number of switches in comparison with other topologies. PUC is known as an energy-efficient topology; however, it has a complicated switching pattern and it also needs bulky capacitors while using conventional control technique. Applying new voltage balancing techniques like MPC could decrease the complexity and capacitor size of this converter. Moreover, UX-Cell MLI is an enhanced MLI derived from PUC topology so it has all features of PUC7 or PUC5 converters plus three more advantages. First, it has boosting ability, which can decrease the application cost; secondly, it has one capacitor less than PUC topology while it has same number of switches in comparison with PUC9. Finally, this topology needs smaller capacitor because of its structure since it has two more paths in each half cycle.

FUTURE WORKS

- Designing a comprehensive PCB for PUC9 and UXC9 (including voltage/current measurements and gate drivers).
- Obtaining Experimental result in three-phase configuration of PUC9 and UXC9.
- Designing PCB of PUC17 and UXC19 for obtaining Experimental results in stand-alone and grid-connected mode.
- Designing a sensorless technique for PUC17 and UXC19.
- Applying the SVM and PS-PWM technique on PUC9, UXC9, PUC17 and UXC19.
- Applying the hysteresis control and PI control technique on PUC9, UXC9, PUC17 and UXC19.
- Using PUC9, UXC9, PUC17 and UXC19 as a submodule in MMC.
- Designing a MPC control for PUC9, UXC9, PUC17 and UXC19 inverters with fixed switching frequency.

APENDIX I

DESIGN CONSIDERATION OF PUC9 MLI

AI.1 Selecting switches

An important consideration in designing PCB of an inverter is choosing proper switches. In this regard, based on the power of the converter that we want to design and application voltage, the maximum current must be obtained. Considering the fact that the voltage in industrial application in Canada is normally 240 V RMS, to design a 3 kW inverter, it can be said that:

$$P_{conerter} = V_{peak-to-peak} * I_{Max\ output} = V_{rms} * \sqrt{2} * I_L \qquad \text{(A I-1)}$$

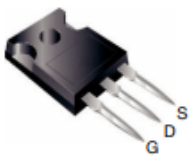
$$\rightarrow I_l = \frac{3000 * \sqrt{2}}{240} = 17.67\ A$$

Where I_l is maximum current that inverter can inject to the grid

Firstly, I_l may pass through each switch; as a result, the switches must be able to tolerate this current. Secondly, in PUC topology, DC source must be equal to or bigger than the peak of grid voltage, which is $240 * \sqrt{2} = 340V$; therefore, in this case, 400 V as DC source could be proper. Switches S_1 and S_5 must support all of dc source, S_2 and S_6 must support half of dc source voltage, and other switches must support one fourth of dc source voltage. Considering all switches the same, these switches must be able to support all voltage of dc voltage source. Consequently, due to decreasing fabrication cost, I selected IRFP460, which is an N-channel metal oxide Mosfet (Siliconix, 2012). Figure-A I-1 shows a summary from datasheet of this Mosfet.

IRFP460B

PRODUCT SUMMARY		
V_{DS} (V) at T_J max.	550	
$R_{DS(on)}$ max. at 25 °C (Ω)	V_{GS} = 10 V	0.25
Q_g max. (nC)	170	
Q_{gs} (nC)	14	
Q_{gd} (nC)	28	
Configuration	Single	



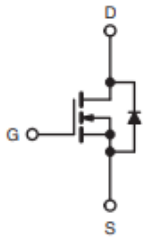


Figure-A I-1 IRFP460 summary
Taken from Siliconix (2012)

AI.2 Snubber circuit design

The role of snubber circuit is limiting $\frac{dv}{dt}$. In other words, it protects power switches during a turn-on/off situation. There are various kinds of snubber circuits, among which the RC has the most popularity. Figure-A I- 2 indicates RC snubber circuit(Semiconductor, 2014). One of affecting factors in capacitors and resistors' value in snubber circuit is leakage current in designed PCB. As a result, there are many equations for obtaining the values of snubber circuit in different books and also application notes. When the dissipation of power is critical, optimized RC snubber should be used. Most of the methods are not optimized methods because they estimate the values approximately. I found one optimized method, proposed by Fairchild Semiconductor and contributed by Digi-key electronics 2014. In this method, first, F_{ring} is measured at the MOSFET switch node. Then, a 100 pF film capacitor should be soldered across the MOSFET. After that, the capacitance should be increased until the rising frequency reaches half of the original measured value. The added capacitance plus the original parasitic capacitance of the switch is called the total output capacitance (C_p). Therefore, the value of externally added capacitor is three times more than the parasite capacitance.

$$F_{ring} = \frac{1}{2\pi\sqrt{L_p * C_p}} \quad \text{(A I-2)}$$

R_{snub} and C_{snub} can be calculated with following equations after figuring out the inductance L_p and parasitic capacitance C_p.

$$R_{snub} = \sqrt{\frac{L_p}{C_p}} \quad \text{(A I-3)}$$

$$\rightarrow R_{snub} = \sqrt{\frac{0.234\ \mu H}{0.48\ nF}} \approx 22\Omega$$

$$C_{snub} = \frac{1}{2\pi * R_{snub} * F_{ring}} \quad \text{(A I-4)}$$

$$\rightarrow C_{snub} = \frac{1}{2\pi * 22 * 15\ MH} \approx 480PF$$

$$P_{R_{snubb}} = C_{snub} * V_{dc}^2 * f_{sw} \quad \text{(A I-5)}$$

$$\rightarrow P_{R_{snubb}} = 480PF * 400^2 * 2kH \approx 0.15\ \text{W}$$

To be in the safe side a 22Ω ¼ Watt standard resistor was selected.

AI.3 Electrical conductor spacing

There are some standards for electrical conductor spacing in PCB designing. IPC-2221A is a popular standard in industry, so I use this standard for designing PUC9 PCB with altium-designer software. Table-A I-1 illustrates relationship of voltage between conductors and minimum spacing in IPC-2221A standard.

Table-A I-1 minimum spacing based on IPC-2221A standard
Taken from IPC-2221A Standard

Voltage Between Conductors (DC or AC Peaks)	**Minimum Spacing**						
	Bare Board				**Assembly**		
	B1	**B2**	**B3**	**B4**	**A5**	**A6**	**A7**
0-15	0.05 mm	0.1 mm	0.1 mm	0.05 mm	0.13 mm	0.13 mm	0.13 mm
16-30	0.05 mm	0.1 mm	0.1 mm	0.05 mm	0.13 mm	0.25 mm	0.13 mm
31-50	0.1 mm	0.6 mm	0.6 mm	0.13 mm	0.13 mm	0.4 mm	0.13 mm
51-100	0.1 mm	0.6 mm	1.5 mm	0.13 mm	0.13 mm	0.5 mm	0.13 mm
101-150	0.2 mm	0.6 mm	3.2 mm	0.4 mm	0.4 mm	0.8 mm	0.4 mm
151-170	0.2 mm	1.25 mm	3.2 mm	0.4 mm	0.4 mm	0.8 mm	0.4 mm
171-250	0.2 mm	1.25 mm	6.4 mm	0.4 mm	0.4 mm	0.8 mm	0.4 mm
251-300	0.2 mm	1.25 mm	12.5 mm	0.4 mm	0.4 mm	0.8 mm	0.8 mm
301-500	0.25 mm	2.5 mm	12.5 mm	0.8 mm	0.8 mm	1.5 mm	0.8 mm
>500	0.00250 mm/volt	0.00500 mm/volt	0.02500 mm/volt	0.00305 mm/volt	0.00305 mm/volt	0.00305 mm/volt	0.00305 mm/volt

B1: Internal conductors

B2: External conductors, uncoated, sea level to 3050m

B3: External conductors, uncoated, over 3050m

B4: External conductors, with permanent polymer coating (any elevation)

A5: External conductors, with conformal coating over assembly (any elevation)

A6: External component lead/termination, uncoated, sea level to 3050m

A7: External component lead/termination, with conformal coating (any elevation)

Considering that PCB is coated with permanent coating and V_{dc} is equal to 400 V, 10mm spacing is proper for this converter. Figure AI.2 shows role setting in altium designer software for minimum spacing.

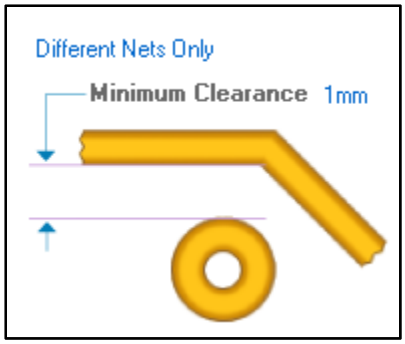


Figure-A I-2 minimum spacing setting in altium designer software

AI.4 Conductor thickness and width for internal and external layers

In order to determine the thickness and width of copper in internal and external layers of PCB, IPC-2221A standard is used. Figure AI.3 illustrates this standard based on temperature rise above ambient. Noted that this table shows the minimum width. To be sure, it is better to consider conductor width a little bigger than the value obtained from these line charts. Based on below charts, a copper track with 2 OZ thickness and 10 mm width is a suitable choice for PUC9 MLI. Figure AI.4 indicates conductor width setting in altium designer software for both internal and external layers.

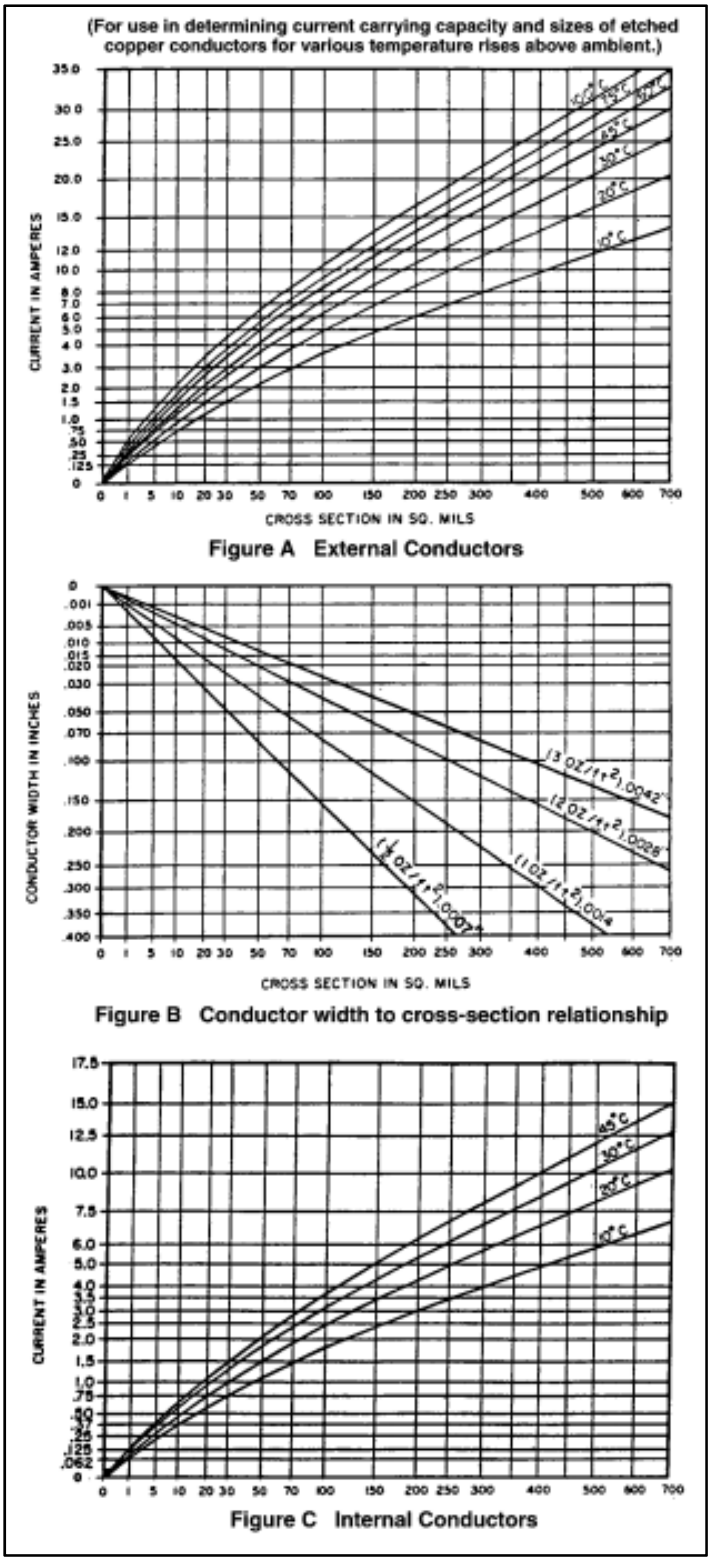


Figure-A I-3 IPC-2221A standard for tracks width
Taken from IPC-2221A standard

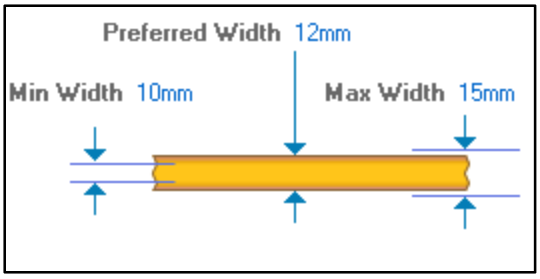


Figure-A I-4 conductor width setting in altium designer software for all layers with 2 OZ copper thickness

AI.5 Calculating output LC filter for PUC9 in grid-connected mode of operation:

In small grid's applications, selecting proper LC filter has a good effect on the performance of designed control method and the grid voltage. It should be mentioned that in large grid's applications because the output voltage of the inverter cannot have a big impact on the grid voltage, just a L filter is enough for connecting the output of inverter to the grid. The following equations indicates how to calculate the size of LC filter for PUC9 MLI (Abarzadeh & Al-Haddad, 2019; Abarzadeh, Javadi, & Al-Haddad, 2019; Abarzadeh, Vahedi, et al., 2019).

$$L = \frac{V_{dc}}{8*(n-1)*\Delta I_L*f_{1st\ sw\ Harmonic}} \tag{A I-6}$$

$$\rightarrow L = \frac{400}{8 * (9-1) * 17.67 * 0.05 * 2500} \approx 2.8\ mH$$

$$C = \frac{1}{(2\pi \times \frac{f_{1st\ sw\ Harmonic}}{10})^2 \times L} \tag{A I-7}$$

$$\rightarrow C = \frac{1}{(2\pi \times \frac{2500}{10})^2 \times 0.0028} \approx 144\ \mu F$$

AI.6 Selecting auxiliary capacitors:

In the PUC topology, auxiliary capacitors act as a DC voltage source. In an ideal situation, the voltage of auxiliary capacitors must be stable at desired levels but in reality, they have some ripple. As a result, the selection of auxiliary capacitors' size is very important because it

directly affects the voltage ripple of auxiliary capacitors. Besides, as per Voltage Source Inverter Design Guide, 2015, at most 5% voltage ripple is acceptable. Below equation shows how to calculate the size of auxiliary capacitors based on peak current, voltage ripple, and ripple frequency (Abarzadeh & Al-Haddad, 2018; Abarzadeh, Javadi, et al., 2019; Abarzadeh, Vahedi, et al., 2019).

$$C = \frac{I_{peak}}{V_{ripple} * f_{ripple}} \tag{A I-8}$$

$$\rightarrow C_1 = \frac{I_{peak\ C1}}{V_{ripple} * f_{ripple}} \rightarrow C_1 = \frac{6}{200 \times 0.05 \times 2500} = 240\ \mu F$$

$$\rightarrow C_2 = \frac{I_{peak\ C2}}{V_{ripple} * f_{ripple}} \rightarrow C_2 = \frac{7}{100 \times 0.05 \times 2500} = 560\ \mu F$$

Figures-A I-5 and A I-6 indicate the designed PCB of PUC9 with altium designer software in 3D and 2D modes in order.

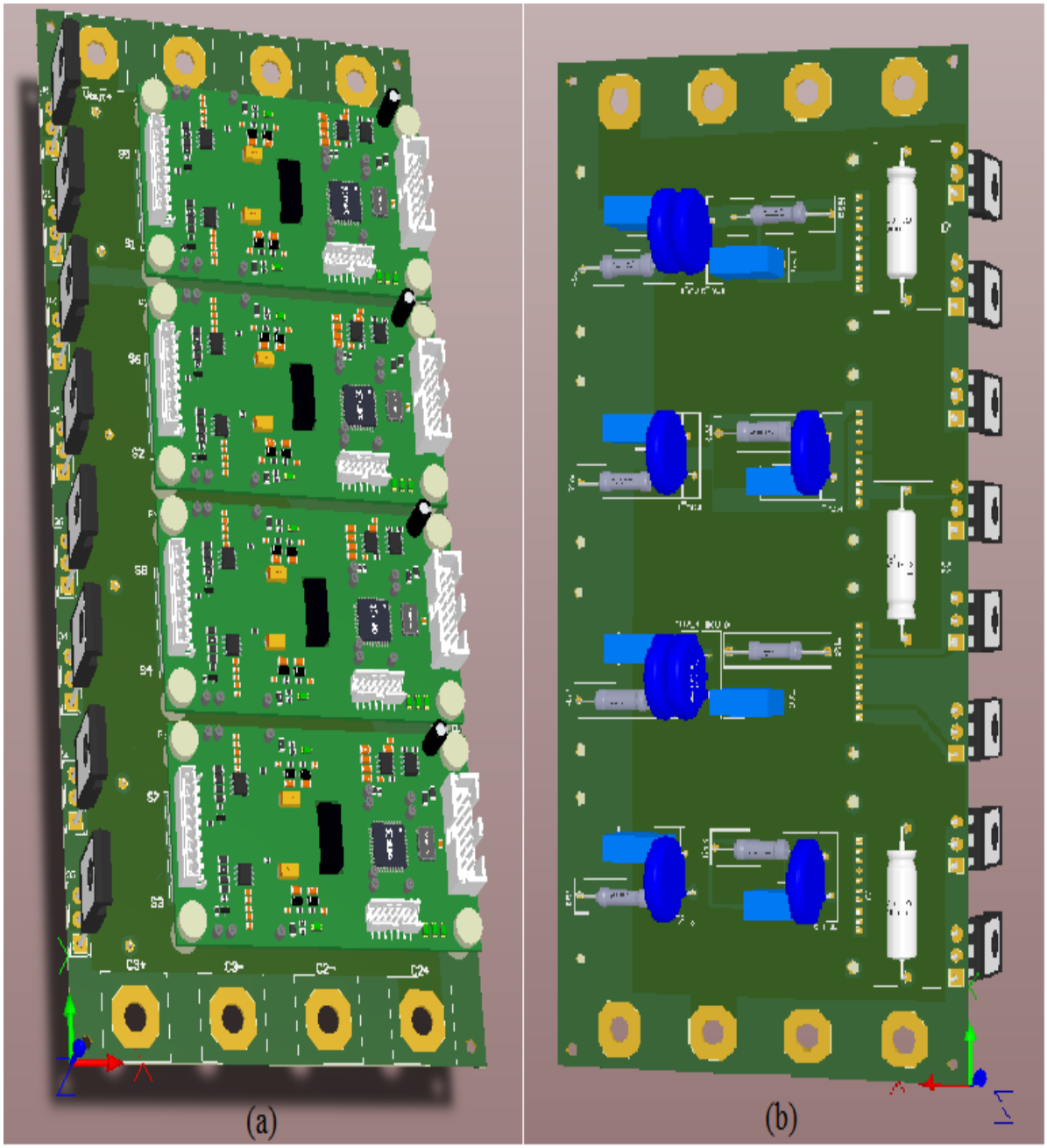


Figure-A I-5 PCB of PUC9 in 3D mode (a) top view, (b) bottom view

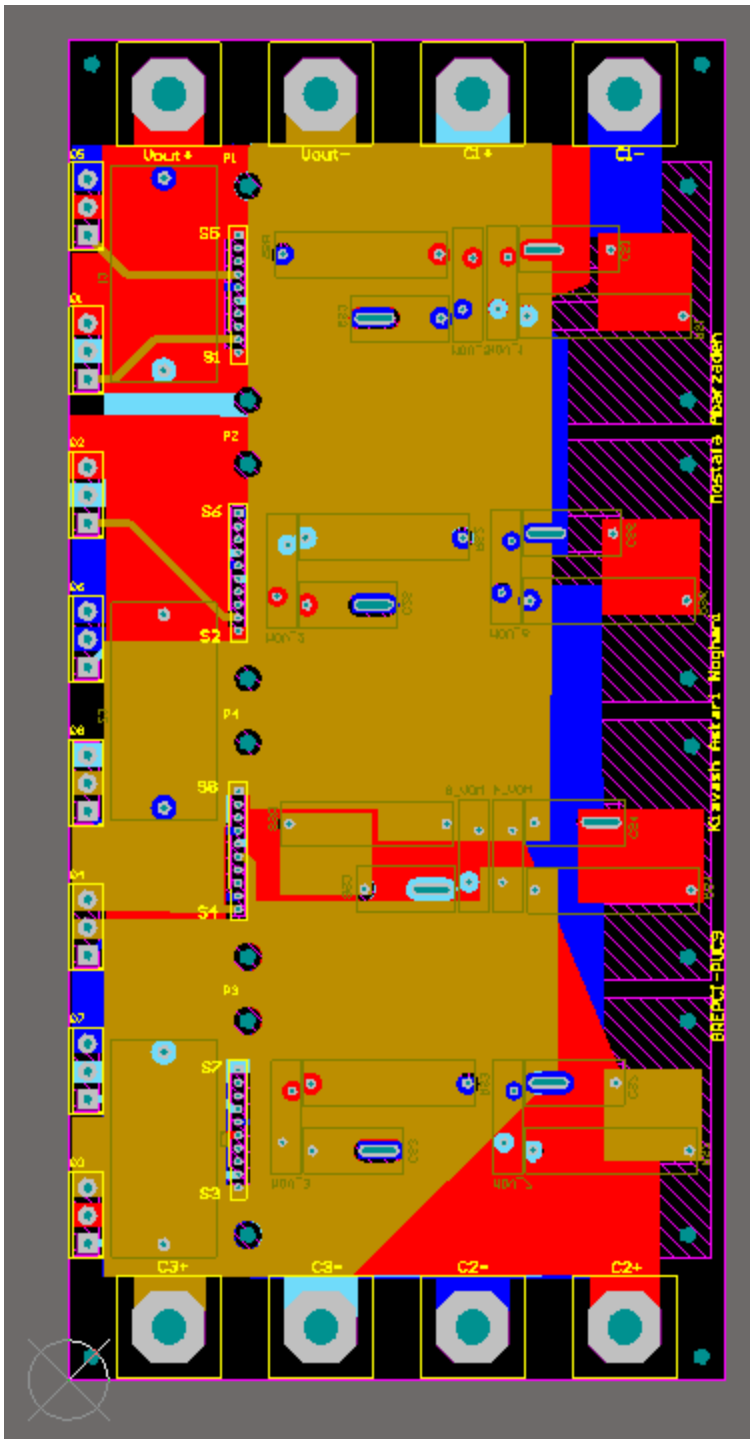


Figure-A I-6 PCB of PUC9 in 2D mode

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