Introducing Positive Envelope Feedback – A New Method for Linearity Improvement in Radio Frequency Integrated Circuit Power Amplifiers

by

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DEDICATION

To Ma and Ta, for everything.

FOREWORD

The work presented in this thesis presents my original research work that was carried out from 2012 to 2019 at École de technologie supérieure, Montreal as part of my master's-doctoral integrated-program studies under the supervision of Professor Nicolas Constantin and in collaboration with the Ottawa R&D division of Skyworks Solutions, Inc., a U.S.-based world leader in the area of radio frequency integrated circuits for wireless communication. The objective of this research work is to address the linearity-power efficiency trade-off in power amplifiers (PAs), a subject of extensive investigation and much scholarly treatment since the advent of vacuum tube power amplifiers in the early part of the twentieth century and yet never short on excitement in terms of new and innovative methods that continue to be proposed towards further improving power amplifier performances. My doctoral research work introduces and demonstrates one such innovation based on an original positive envelope feedback circuit technique in Radio Frequency Integrated Circuit (RFIC) PAs. Further, my doctoral research work introduces an analytical three-port power amplifier representation to aid the design and implementation of envelope-dependent PA biasing techniques, including positive envelope feedback PAs, in practical scenarios that benefit from the availability of closed-form equations for predicting PA performances and PA biasing requirements. One such scenario, shown for the first time through my doctoral research, demonstrates using the 3-port power amplifier representation for the embedded self-calibration of PAs within the mobile unit to compensate against part-to-part variation of RFIC PA performances. The results of my doctoral research work have been submitted to two journals (one published and one currently under revision), published in three patents (two granted and one under provisional application) and one conference paper (awarded "Best Student Paper"). Multiple additional journal manuscripts are currently under preparation for submission. Another journal, two conference papers (including one as a second author) as well as various posters have also been presented and highlight contributions directly or indirectly stemming from the research work conducted during my doctoral studies.

ACKNOWLEDGMENT

It would hardly be an overstatement to say that the research work presented in this thesis would have been impossible without the constant help, guidance and encouragement given by my thesis supervisor, Professor Nicolas Constantin. From working very late hours together to spending entire weekends (including during the holidays) trying to troubleshoot designs, reviewing test measurements and drafting technical documents – my years in academia during the last few years of graduate studies have truly been a learning experience, and in no small part because of Professor Constantin. Whatever little that I have learned regarding the nuances associated with conducting research is largely due to his excellent tutelage, and I am extremely grateful for it.

I would like to express my appreciation to the members of my thesis evaluation jury for accepting to review this document, and for taking time out to examine the research work presented here. I would also like to express my gratitude to the staff at Skyworks Solutions, Inc. for their assistance with various aspects of my work, as well as their insights into industry practices that I was exposed to during (as well as after) my time at the R&D Division of their Ottawa design center. My thanks are due to the staff at the Laboratoire de communication et d'intégration de la microélectronique (LACIME) and the staff at the Electrical Engineering Department of ÉTS, who have both always been forthcoming with their help. I would also like to acknowledge the support of ÉTS Excellence awards for international students – Master's-PhD Award, CMC Microsystems Canada, MITACS Canada and the Natural Science and Engineering Research Council (NSERC), Canada.

My life at ÉTS, and in Montreal, has been enriched by many individuals. While it is impossible to name every one of them here, I would like to thank David, Gabriel and Tân – all at LACIME – for making life at school as fun as it was. Our morning chats over coffee (supplemented with unhealthy levels of politics, cooking recipes and television show banter), afternoon swimming sessions at the neighbourhood pool and many Friday evenings at the pub – these, along with many other unforgettable experiences (as well as the academic

exchanges), have all been extremely memorable, and I would not have traded them for anything else. I would also like to acknowledge David's contribution to an essential aspect of my work – my diagrams. The basic structures of most of the figures found in my work are based on a template created by David and that he kindly shared with me at the beginning of my graduate studies, and this template has made my life – when it comes to drafting figures – so much easier. I would also like to acknowledge Tân's timely help with generating the references, in addition to all the moral support throughout – both inside and outside the university. Thanks are also due to my many friends back in India, and elsewhere, who have digitally kept in touch and helped me get through the trials and tribulations of life at graduate school. While the list is (again) too long, I am indebted to Dhiman for his constant mirth (as well as the countless entertaining conversations).

Despite the very long winters, Montreal is a terrific city to call home – and my hours outside school were made all the more fabulous thanks to a notorious circle of friends that has only grown over the years. I would like to mention the chief architects among them – Jean, and *especially* David M. and Jamie – for all the good (and constant) cheer. It is the people that you surround yourself with that *maketh* life, and I count myself fortunate to have been given the chance to surround myself with such special people. *Nothing would have been the same without them, and nothing will ever be*.

It would also hardly be an overstatement to say that my family's unwavering optimism, infinite patience and unfaltering faith have been my single biggest sources of motivation throughout. My parents have sacrificed a lot and consistently emphasized the value of education, and my brother could always be counted on when I needed him. *For this, and for everything else, I would forever be indebted and grateful*.

Présentation de la rétroaction positive de l'enveloppe - une nouvelle méthode d'amélioration de la linéarité dans les amplificateurs de puissance radiofréquences intégrés sur puces de semiconducteur

Smarjeet SHARMA

RÉSUMÉ

Dans la première partie de cette thèse de doctorat, l'auteur présente la technique de rétroaction positive de l'enveloppe dans les amplificateurs de puissance radiofréquences intégrés sur puces (acronyme en anglais: RFIC PAs). Il s'agit d'une nouvelle méthode introduite dans cette thèse, pour améliorer le compromis linéarité-efficacité énergétique d'un amplificateur et basé sur un cheminement du signal directement à partir de la sortie de l'amplificateur, à travers un seul détecteur d'enveloppe et vers son entrée de polarisation. La technique proposée nécessite une surface de circuit supplémentaire minimale, consomme un courant supplémentaire négligeable, ne présente pas de limitations sévères de la bande passante et ne dégrade pas les performances de bruit de l'amplificateur de puissance. La simplicité inhérente de la technique proposée permet son intégration dans les architectures d'amplificateur existantes avec un minimum de modifications dans la conception, ainsi que son utilisation conjointement avec d'autres techniques de circuit pour l'amélioration de la performance des amplificateurs. La théorie, la conception et l'implémentation de la technique proposée sont décrites en détail, tout en considérant les différentes conditions de conception à respecter pour améliorer les performances des amplificateurs utilisant cette technique. L'implémentation de la technique proposée est démontrée en utilisant plusieurs conceptions d'amplificateurs de puissance, à l'aide des résultats obtenus par simulation et aussi des expériences sur des conceptions d'amplificateurs qui ont été fabriquées. Les mesures sur une conception expérimentale d'un amplificateur de puissance en technologie CMOS SOI démontrent une augmentation de 1,7 dB de la puissance correspondant au point de compression de 1dB du gain (P_{1dB}) de l'amplificateur en utilisant la technique proposée ici, ainsi qu'une amélioration de la distorsion d'intermodulation de troisième ordre en sortie (IMD_3) allant jusqu'à environ 3,44 dB. Des simulations sur une version modifiée de cette conception montrent une amélioration IMD_3 allant jusqu'à 3,5 dB et une amélioration de la réjection de puissance aux canaux adjacents (ACPR) allant jusqu'à 6 dB pour les signaux à large bande passante, aux niveaux de puissance de sortie où l'amplificateur subit une compression de gain importante.

Dans la seconde partie de cette thèse, l'auteur développe les fondements analytiques d'une nouvelle représentation non-linéaire multi-ports pour amplificateurs radiofréquences. Elle est basée sur des ensembles distincts de polynômes complexes non-linéaires décrivant un combineur, un convertisseur non-linéaire de l'information en bande de base jusqu'aux radiofréquences, ainsi qu'une fonction d'amplification non-linéaire aux radiofréquences, pour le traitement d'un signal RF modulé à l'entrée de l'amplificateur et d'un signal de polarisation dynamique dépendant de l'enveloppe. La représentation proposée permet une

prédiction précise des composantes de distorsion en sortie de l'amplificateur, en fonction d'une excitation RF à tonalités multiples en entrée et d'un signal de polarisation dépendant de l'enveloppe et à tonalités multiples. Cette nouvelle représentation des effets non-linéaires d'un amplificateur rend possible des formulations analytiques pour décrire un système amplificateur non-linéaire à trois ports et permet de déterminer les ajustements nécessaires dans le signal de polarisation dynamique ainsi que dans les circuits pour l'amélioration de la linéarité de l'amplificateur en présence de signaux d'excitation à tonalités multiples et modulés. La nouvelle représentation proposée est destinée à un contexte qui, du mieux des connaissances de l'auteur, est introduit pour la première fois et qui est envisagé comme prometteur pour les équipements de communication mobile actuels et futurs – soit l'optimisation automatique des performances de linéarité d'un amplificateur utilisant une polarisation dynamique dépendante de l'enveloppe du signal modulé, à l'aide de fonctions d'auto-calibration intégrées à la tête-RF d'un émetteur à l'intérieur d'un équipement de communication mobile. La représentation proposée permet ainsi d'optimiser la polarisation dynamique dépendante de l'enveloppe dans un amplificateur pour l'amélioration de la linéarité dans la transmission de signaux modulés par chaque equipment de communication mobile individuellement. Une telle optimisation de chaque unité d'équipement de communication est donc possible grâce à ces fonctions d'auto-calibration intégrées qui ne requièrent, comme séquences d'entraînement, que des mesures quasi-statiques de la puissance d'entrée et celle de la sortie de l'amplificateur. Cela contraste avec les séquences d'entraînement beaucoup plus complexes qui sont nécessaires pour les représentations non-linéaires d'ordre élevés telles que les séries de Volterra, ou d'autres représentations proposées dans la litérature scientifique. L'applicabilité de la représentation proposée ici est illustrée par des simulations et des analyses comparées à des résultats expérimentaux, démontrant une caractérisation précise des performances d'amplificateurs conçus selon différentes techniques de polarisation dynamique et utilisant différentes technologies de semiconducteur. Dans une implémentation expérimentale utilisant un amplificateur en technologie d'Arséniure de Gallium (AsGa) et conçu dans un milieu industriel, la représentation proposée prédit avec précision les ajustements de polarisation dynamiques nécessaires pour obtenir une réduction de plus de 4 dB de la valeur IMD_3 à la sortie. Une réduction similaire de la puissance du canal adjacent (ACP) est démontrée avec un signal modulé. Dans une deuxième implémentation expérimentale, la représentation proposée permet, pour la première fois, d'utiliser une approche analytique pour prédire l'état de la stabilité d'un amplificateur utilisant la rétroaction d'enveloppe positive en boucle fermée, ainsi que de déterminer les performances optimales requises pour les composants du système en rétroaction.

Mots clés: polarisation dynamique, efficacité, auto-calibration intégrée, linéarité, signaux multi-tons, enveloppe de signaux modulés, rétroaction positive de l'enveloppe, amplificateurs de puissance radiofréquences, circuits intégrés radiofréquences, représentation non-linéaire à trois ports

Introducing Positive Envelope Feedback – A New Method for Linearity Improvement in Radio Frequency Integrated Circuit Power Amplifiers

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ABSTRACT

In the first part of this doctoral thesis, the author introduces Positive Envelope Feedback in Radio Frequency Integrated Circuit (RFIC) Power Amplifiers (PAs) - a new method for improving the PA's linearity-efficiency trade-off and based on a signal flow directly from the PA output, through a single envelope detector, to its bias input. The proposed technique requires minimum additional circuit area, consumes negligible additional current, does not suffer from bandwidth limitations and does not degrade PA noise performances. The inherent simplicity of positive envelope feedback enables its incorporation into existing PA architectures with minimum re-design, as well as its use in conjunction with other circuit techniques aimed at PA performance enhancement. The theory, design and implementation of positive envelope feedback are described in detail while underscoring the various design conditions that must be taken into consideration to ensure PA performance improvement through the proposed technique. Its implementation is highlighted with the help of multiple PA designs, using results obtained through simulation as well as experiments on fabricated designs. Measurements on one experimental Complementary Metal-Oxide-Semiconductor (CMOS) Silicon-on-Insulator (SOI) PA design using positive envelope feedback show an increase of 1.7dB in the PA's 1dB gain compression point (P_{1dB}) and an output third-order intermodulation distortion (IMD_3) improvement of up to ~3.44dB while requiring only an equivalent ~5% increase in chip area and 1.2% increase in quiescent current consumption. Simulations on a modified version of this PA design demonstrate an IMD_3 improvement of up to 3.5dB and Adjacent Channel Power Ratio (ACPR) improvement of up to 6dB thanks to the use of positive envelope feedback with larger signal bandwidths, and at output power levels where the open-loop PA is under significant gain compression.

In the second part of this thesis, the author develops the analytical foundations of a novel multi-port PA representation based on distinct sets of nonlinear complex polynomials that describe a combiner, a nonlinear baseband-to-RF converter and a nonlinear RF amplifying function, for the processing of the PA's input modulated RF signal and any envelope-dependent dynamic biasing signal. The proposed representation is shown to allow an accurate prediction of the PA's output distortion components as a function of an input RF multi-tone excitation and a multi-tone envelope-dependent biasing signal. This novel representation of a PA's nonlinearities renders possible closed-form analytical formulations to describe a three-port PA system, and allows determining the adjustments necessary in the dynamic biasing signal and circuitry for PA linearity improvement under multi-tone as well as modulated excitation signals. It is intended for a context introduced for the first time in the author's research work and envisioned as promising for current and future mobile communication equipment – the automatic optimization of linearity performance in RFIC

PAs that employ envelope-dependent dynamic biasing, through embedded self-calibration functions implemented within the transmitter front-ends of mobile equipment. The proposed representation allows the optimization of the PA's envelope-dependent dynamic biasing for linearity improvement from one mobile unit to another through embedded self-calibration, starting from quasi-static measurements alone of the PA's input and output power, in contrast to more complex training sequences that are required for high-order Volterra-based and other PA representations. The applicability of the proposed representation is highlighted through simulation and benchmarking against experimental results, demonstrating accurate characterization of PA performances under different dynamic biasing techniques, for multiple RFIC PA platforms and in different semiconductor technologies. In one experimental implementation using an industry-designed Gallium Arsenide (GaAs) PA, it accurately predicts the necessary dynamic biasing adjustments to achieve more than 4dB reduction in the output IMD_3. A similar reduction in Adjacent Channel Power (ACP) is demonstrated with a modulated signal. In a second experimental PA implementation, the proposed representation allows, for the first time, using an analytical approach for predicting the condition of system stability under closed-loop positive envelope feedback operation, as well as determining the optimum performance requirements for the feedback system components.

Keywords: dynamic biasing, power efficiency, embedded self-calibration, linearity, multi-tone signals, output envelope, positive envelope feedback, power amplifier, three-port representation

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LIST OF ABBREVIATIONS AND ACRONYMS

3GPP	Third Generation Partnership Project
5G-NR	Fifth Generation-New Radio
ACPR	Adjacent Channel Power Ratio
AM	Amplitude Modulation
BJT	Bipolar Junction Transistor
CAD	Computer-Aided Design
CCDF	Complementary Cumulative Distribution Function
CDMA	Code-Division Multiple Access
CG	Common Gate
CMOS	Complementary Metal-Oxide-Semiconductor
CS	Common Source
CW	Continuous Wave
DC	Direct Current
DPD	Digital Pre-Distortion
DSP	Digital Signal Processor
DUT	Device Under Test
EM	Electromagnetic
ET	Envelope Tracking
EVM	Error Vector Magnitude
FET	Field-Effect Transistor
FM	Frequency Modulation
GaAs	Gallium Arsenide

XXX

HBT	Heterojunction Bipolar Transistor
HB	Harmonic Balance
IMD	Intermodulation Distortion
InGaP	Indium Gallium Phosphide
LCD	Liquid Crystal Display
LNA	Low-Noise Amplifier
LTE	Long-Term Evolution
MCM	Multi-Chip Module
ME	Mobile Equipment
MMIC	Monolithic Microwave Integrated Circuit
MN	Matching Network
MOSFET	Metal-Oxide-Semiconductor Field-Effect Transistor
NMOS	Negative-Channel Metal-Oxide Semiconductor
PA	Power Amplifier
PAE	Power-Added Efficiency
PAPR	Peak-to-Average Power Ratio
PCB	Printed Circuit Board
PM	Phase Modulation
PMOS	Positive-Channel Metal-Oxide Semiconductor
PTO	Patent and Trademark Office
RF	Radio Frequency
RFIC	Radio Frequency Integrated Circuit
SMT	Surface-Mount Technology

SOI	Silicon-on-Insulator
STI	Shallow Trench Isolation
UL	Uplink
VGA	Variable Gain Amplifier
VSWR	Voltage Standing Wave Ratio
WCDMA	Wideband Code Division Multiple Access
WLAN	Wireless Local Area Network

LIST OF SYMBOLS

β	RF-to-analog linear conversion gain of the feedback path
λ	Wavelength
ω	Angular frequency (in radians per second)
A	Baseband-to-RF linear conversion gain of the PA's power-stage
C_{ggn}	Input capacitance looking into the gate of NMOS transistor
C_{ggp}	Input capacitance looking into the gate of PMOS transistor
C_{in}	Input capacitance (e.g. at the input of PA power-stage)
Env_{in}	Envelope of input RF signal
f_1	Frequency with index 1 (in hertz)
f_{rf}	RF frequency (in hertz)
I_D	Drain current
IMD_3	Third-order intermodulation distortion product
IMD_{3hi}	Upper third-order intermodulation distortion product
IMD_5	Fifth-order intermodulation distortion product
P_1	Port 1 (e.g. port 1 of a multi-port PA representation)
P_{DC}	DC power
P_{in}	Input power level (e.g. at the input of PA)
P_{out}	Output power level (e.g. at the output of PA)
P_{ref}	Reference power level (e.g. threshold power level for PA under positive envelope feedback)
Q	Quisceint operating point
Q_{dyn}	Instantaneous operating point

RF_{dr}	RF signal at the output of PA driver stage
RF_{in}	RF signal at the input of PA (e.g. at the input of PA driver-stage)
RF_{out}	RF signal at the output of PA (e.g. at the output of PA power-stage)
R_{opt}	Optimum value of PA output resistance
t_{del}	Absolute value of time delay (e.g. time delay through PA power-stage transistors)
T_{x1}	Transmit antenna with index 1
V_{bias}	Bias voltage of PA (e.g. DC bias applied to the gate of PA power-stage)
V_{dd}	Drain supply voltage (e.g. drain supply voltage of PA power-stage in ET PAs)
V_{DD}	DC value of drain supply voltage (e.g. DC bias applied to PA power-stage drain)
v_{ds}	Drain-source RF voltage signal (in time-domain)
V_{DS}	Drain-source DC voltage level
V_{dyn}	Dynamic-bias voltage signal (e.g. envelope-varying bias signal applied to PA power-stage gate under positive envelope feedback)
V_{GG}	Gate-bias voltage (e.g. of PA power-stage)
V_{GG0}	Quiescent value of gate-bias voltage (e.g. of PA power-stage)
v_{gs}	Gate-source RF voltage signal (in time-domain)
V_{GS}	Gate-source DC voltage level
v_{in}	Input voltage (e.g. frequency-domain multi-tone voltage signal at PA input)
$v_{in}(t)$	Input voltage in time-domain (e.g. time-domain modulated signal at PA input)
$V_{in}(\omega_c+i\omega_x)$	Value of V_{in} voltage-signal tone at frequency $\omega_c+i\omega_x$
v_o	Output voltage (e.g. frequency-domain multi-tone voltage signal at PA output)
Z	Impedance

INTRODUCTION

> "The mere formulation of a problem is far more often essential than its solution, which may be merely a matter of mathematical or experimental skill. To raise new questions, new possibilities, to regard old problems from a new angle requires creative imagination and marks real advances in science."
>
> Albert Einstein

In this chapter of the thesis, the reader is introduced to the underlying essence of the doctoral research work presented here. The research problems that the work presented in this thesis attempts to find an answer to, as well as the motivation behind trying to solve these problems, are described in Section 0.1. Having presented the research problems, the objectives aimed at through the work reported in this thesis are identified in Section 0.2. In Section 0.3, some of the key contributions that have resulted from this doctoral work are listed while outlining the major theme of each, before presenting their content in greater detail in the subsequent chapters of this thesis.

0.1 Problem statement and motivation

0.1.1 Motivation 1: PAs and the linearity-efficiency trade-off

The power amplifier is a vital component of the RF front-end in mobile units and has always been among the most critical hardware components of the entire RF transmitter, largely determining many of its system performance specifications. Figure 0.1 is a block diagram representation of a typical front-end in an RF transmitter of a mobile device and shows the relative position of the PA (or PAs) within this front-end. As may be observed, the PA inputs interface with the transceiver section (Tx, Rx and Tx-Rx) within the Radio Block (responsible for signal generation, modulation and demodulation) while the PA outputs interface with the transmit antennas (usually via one or more switches) for radio communication with cellular telephony networks or mobile connectivity networks such as Wi-Fi or Bluetooth. The RFIC PA component is therefore responsible for imparting power to

(i.e. amplifying) the RF frequency communication signal before being delivered to the antenna and transmitted over the air.

The design of this RFIC PA presents several challenges. Chief among these challenges are optimizing the PA's *efficiency* and its *linearity*, among other critical (and often interrelated) criteria such as bandwidth, gain, noise, silicon area, cost, etc. The PA's efficiency is commonly measured using the metric Power-Added Efficiency (or *PAE*) defined by (0.1) below.

$$PAE\ (\%) = \frac{P_{out} - P_{in}}{P_{DC}} \times 100 \tag{0.1}$$

where P_{out} is the PA's delivered output RF power, P_{in} is the PA's input RF power, and P_{DC} is the PA's DC power that it consumes (e.g. from the battery). As seen by this equation, ideally, the DC power consumed from the battery should be only a little more than the RF power imparted to the transmitted signal by the PA and delivered at its output, for this component to be highly efficient. The PA's *PAE* is, therefore, a good measure of its DC power consumption requirements, and a lower efficiency translates into a PA design that is consuming more battery (i.e. DC) power than it should be. The DC power consumed by the PA when it is not transmitting is commonly referred to as the PA's quiescent power consumption, and a high value of this quiescent power consumption translates into a PA that suffers from poor efficiency. Indeed, a high quiescent power consumption adversely affects the PA's efficiency not just at lower power levels, but over its entire range of transmitted power levels. The judicious consumption of battery power is critical in mobile devices, where a higher PA efficiency ensures a more extended time period for which the mobile device remains operational before the battery needs to be recharged. While not being the only contributor to the phenomenon, a lower PA efficiency also translates into higher heat production in the mobile device. Such heating issues are because the PA is consuming DC power disproportionate to its requirements, which in turn can negatively affect other PA performances (e.g. gain) as well as make the handheld device uncomfortable to hold.

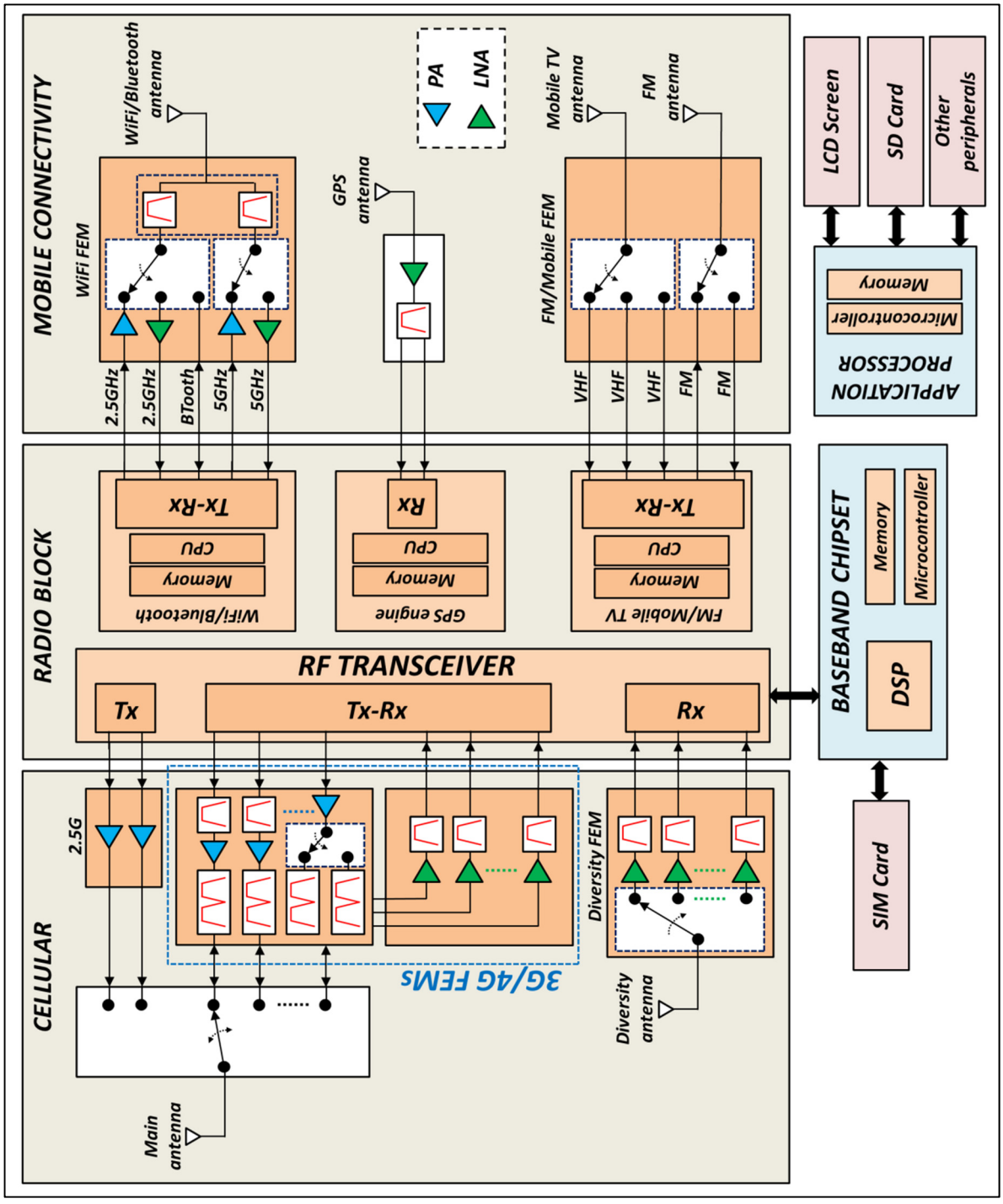

Figure 0.1 Example of typical transmitter architecture of a handheld mobile device showing the use of RFIC PAs. Notice the use of multiple PAs in the transmitter architecture. Each of these PAs have their unique specifications (frequency band of operation, output power, etc.) and are intended for the transmission of signals targeting different specific applications Adapted from Bailoo (June 2019) and Walsh (September 2010)

It is worthwhile to note here that the PA in the mobile device represents approximately 20% of the entire power consumption of a modern cellular device (such as a smartphone) under normal cellular usage conditions (Carroll & Heiser, 2010; Javed, Shahid, Sharif, & Yasmin, 2017). The remainder of the power is shared among other components such as the Liquid Crystal Display (LCD) screen, memory devices, multimedia applications, etc. While this share of the total power consumption by the PA is lower than in older generation cellular devices (since the display, multimedia applications, etc. consumed substantially lower power in these yesteryear devices), it still highlights the significance of the PA's efficiency in the context of the performance of the entire RF front-end in mobile devices used for cellular communication today.

Having explained the importance of the PA's efficiency, we now turn our attention to the aspect of the PA's linearity. The PA's linearity is a measure of the degree of signal distortion that the PA's input signal suffers from during amplification through the PA and which is reflected in its delivered output signal, due to the nonlinearities associated with the PA design. Amplification through a power amplifier in a mobile device is an inherently nonlinear process due to several factors intrinsic to semiconductor technology and circuit topology, and which are strongly dependent on the PA voltage supply and PA biasing conditions (i.e. the current intensity applied to the transistors within the PA). Besides linearity, PA biasing is also dictated by considerations regarding efficiency, and all these considerations will be further discussed in Section 1.1. Similar to the metric *PAE* used for measuring the PA's efficiency, a number of metrics exist to measure the PA's degree of nonlinearity, e.g. IMD_3, *EVM*, *ACPR*, etc. IMD_3 is a simple, popular and useful measurement to perform, and is calculated using a multi-tone (commonly 2-tone or 3-tone) excitation applied to the PA, and measuring the resulting spectrum levels at different frequencies in the PA's output. For a 2-tone input excitation, if the two input tones are at frequencies f_1 and $f_2=f_1+f_x$, the PA's output IMD_3 is defined by (0.2).

$$IMD_{3lo} = \frac{P_{out}\ @(f_1 - f_x)}{P_{out}\ @(f_1)} \text{ and } IMD_{3hi} = \frac{P_{out}\ @(f_2 + f_x)}{P_{out}\ @(f_2)} \tag{0.2}$$

where IMD_{3hi} and IMD_{3lo} are the upper and lower values of the PA's third-order intermodulation distortion ratio (IMD_3) respectively. P_{out} @f_1-f_x refers to the PA's output spectrum power level at frequency f_1-f_x; the other definitions of the terms in (0.2) follow likewise. IMD_3 values are commonly reported using the decibel scale, which is obtained by taking the ten-base logarithmic value, and then multiplied by 10, of the ratio given in (0.2). Higher-order intermodulation ratios may also be measured. For example, IMD_5 ratios are calculated by replacing the numerators in (0.2) with spectral power values at frequencies f_1-$2f_x$ and f_2+$2f_x$.

A higher value of IMD_3 arises from higher values of unwanted distortion products present at the PA output, which itself is a result of a higher degree of PA nonlinearity. These distortion products are present at frequencies other than those used in the excitation signal, i.e. at frequencies f_1-f_x, f_1-$2f_x$, … and f_2+f_x, f_2+$2f_x$ …, whereas the input tones are at frequencies f_1 and f_2 only. PA nonlinearities are undesirable since they result in a transmitted output signal that is a corrupted version of the intended message signal at the PA input and has a direct consequence on the quality of the transmitted signal by the mobile device. Besides, distortion products may fall outside the transmission frequency band and exceed the regulatory out-of-band emission specifications, which are intended to ensure the quality of other communication channels. It is worthwhile to note that PA nonlinearities become especially important at higher output power levels when large-signal effects such as signal clipping come into play.

An ideal PA is, therefore, one which is both efficient and linear over the entire range of power levels that it is transmitting, starting from very low power levels to its maximum rated power level. However, as will be shown in Section 1.1, efficiency and linearity in a PA come at the cost of each other. An extremely linear PA is usually one that suffers from poor efficiency and vice versa. The PA designer, therefore, has to make a choice - a *compromise* - between the efficiency and the linearity that is desired for any particular PA design, and based on PA specifications tailored to answer the needs of a particular application. This compromise is referred to as the power amplifier's linearity-efficiency *trade-off*. The trade-

off assumes more considerable significance in the light of modern communication signals, where the complex modulation schemes that are used translate into large peak-to-average power ratios (PAPR) of the signal. The PA transmitting such modulated signals is expected to be both linear and efficient over the entire range of power levels spanned by its average and peak power levels - a challenge that is not trivial to answer.

Improving this linearity-efficiency trade-off is a popular research problem in the field of power amplifiers, and continues to remain an area of active research. A review of popular design strategies that seek to improve this trade-off will also be given in Section 1.1 and highlights the constant evolution and innovation that is a trademark of this area of research. In this thesis also, the fundamental motivation is to improve this linearity-efficiency trade-off in RFIC PAs.

However, through the doctoral studies presented in this thesis, it is sought to answer this research problem while taking into account some additional constraints. These additional constraints stem from the need for *circuit simplicity* – and the advantages that any PA performance improvement technique offers when it is simple. The simpler a PA technique is, the more feasible it is to realize it as a standalone integrated RFIC PA solution or to incorporate it into (and operate in conjunction with) already existing PA architectures. The main characteristics of such simple techniques are: the requirement of minimum additional chip area, the consumption of minimum additional power and the necessity of minimum additional signal processing. Such attributes are especially attractive in the context of millimetre-wave PAs envisaged for 5G applications, where it is believed that given the large bandwidths, complex constellations and large PAPR of the signals that are envisioned for deployment, digital techniques alone cannot satisfy all the requirements to guarantee efficient and linear PA operation (P. M. Asbeck, Rostomyan, Özen, Rabet, & Jayamon, 2019). Both digital and analog techniques have to be used concurrently to meet all the needs of such PAs, and the simplicity of the analog technique will be critical in determining its feasibility for integrating into the RFIC front-end module of the transmitter.

Having explained the research motivation, which will be alluded to throughout the rest of this document and especially in Chapter 2 and Chapter 3, we may now state our first problem statement as given in Section 0.1.2.

0.1.2 Problem Statement 1

There is a need for power amplifier circuit techniques that improve the PA's linearity-power efficiency trade-off while remaining simple - i.e. requiring minimum additional chip area, minimum additional power and no external signal processing. A PA circuit technique that would meet these requirements facilitates its realization as an integrated RFIC PA solution, as well as contributes to its feasibility for incorporation into existing RFIC PA architectures.

0.1.3 Motivation 2: PAs and part-to-part variation

A second source of research motivation for the work presented in this thesis is related to the variation of PA performance from part-to-part in different mobile units, and a need for an automatic self-calibration method that allows achieving optimum PA performances across parts. This aspect is now explained in the succeeding paragraphs.

PA integrated circuits are designed with the help of Computer-Aided Design (CAD) software tools, using circuit models that reflect the *typical* performance parameters of various devices. For example, the MOSFET performance parameters (transconductance, noise, etc.) simulated by the PA designer during a CMOS SOI PA design process generally reflects its typical values. They are simulated under different circuit conditions (e.g. biasing, temperature, etc.) that can be varied within the CAD simulator. During a first design cycle, the designer optimizes a PA design based on these simulated typical values given by the circuit models.

In reality, however, device performances may vary considerably across parts in different mobile units due to many factors, e.g. semiconductor manufacturing process variations, inconsistencies in assembly, deviations in the encapsulation used, etc. Additionally, these

variations are also aggravated as the complexity of the PA design increases, e.g. PAs that use hardware reconfiguration, envelope-dependent control mechanisms, dynamic biasing, etc. In such cases, process variations of the required additional circuitry (e.g. switches in PAs that use hardware reconfiguration, envelope detectors in envelope-controlled PAs, biasing circuitry in dynamic-bias PAs, etc.) add to the already significant performance variations of the basic PA line-up. These are also further accentuated by differences in the biasing and other circuit conditions (e.g. temperature) from one mobile device to another.

As a result, the PA performances simulated using the typical circuit models do not reflect the measured performances that may be expected from the actual fabricated PA circuit. While modern simulators allow the designer to predict in advance (to a certain degree) what these variations will be, it is extremely difficult to design a PA that achieves its best possible performance across all these variations from part-to-part. Subsequent PA design cycles after the first rely on data gathered through extensive measurements in the laboratory over many different PA parts which are deliberately taken from different process corners of the wafer. These measured values are then correlated with the typical simulated values, to select the best value of different PA circuit parameters – *common for all the parts* of a particular PA design in a given production run – which ensures a satisfactory yield of PA parts that meet the *range of performance limits* fixed in the target specifications.

The common PA circuit parameter values that are ultimately selected through circuit adjustments at the prototyping stage for any given PA design, therefore, represent a *compromise*: they ensure that all the delivered PA parts meet the limits of performance variation fixed in the target specifications despite the deviation in their performance from one PA part to another, even though the common circuit parameter values do not allow all the PA parts to achieve their best possible *individual* performance in the mobile device. Such a compromise has implications for both the PA manufacturer as well as the Mobile Equipment (ME) manufacturer. The PA manufacturer is forced to relax the guaranteed limits related to the PA design's performance in the specifications datasheet, to account for all the part-to-part variations of performances compared to that of the typical PA part. Such a relaxation is

necessary to increase PA yield from any given fabrication run. The ME manufacturer faces a similar conundrum arising from PA performance variations due to inconsistencies in the PA assembly within the mobile unit. Such inconsistencies for the ME manufacturer may occur due to a number of factors – e.g. due to deviations from manufacturing tolerances in the PCBs that are used, variations in the bias voltage and supply voltage sources, irregularities in the wire-bonding, etc.

To better explain this, refer to Figure 0.2, which is a portion of the datasheet of a commercial RFIC PA design (SKY85402-11 [Datasheet], August 2018). As can be seen, most performance metrics are associated with a higher and a lower limiting value specified by the PA manufacturer. These limiting values reflect the extremities of the spread in performance that may be expected due to variation from one PA part to another. Such a spread, though undesired, is difficult to circumvent and is accounted for as part of the tolerable limits of performance deviation that is deemed acceptable for a given PA design.

In this context, an automatic self-calibration technique that enables PA performance optimization from one part to another during operation of the mobile equipment would be of interest to any stakeholder in the mobile industry associated with RFIC PAs, and significantly affect the design and operating strategies adopted by RFIC PA manufacturers and ME manufacturers for current and future mobile wireless equipment. The manufacturer may also perform a first calibration step during production/assembly; subsequent automatic self-calibration is performed in the field during operation of the mobile equipment.

Such a calibration technique would target enhancing PA performances within the mobile equipment by ensuring close-to-optimum performance across parts, by varying one or more key circuit parameters from part-to-part in different mobile units during operation. To allow embedding within the mobile equipment, the calibration should be performed with simple (and minimum) probing circuitry and require a simple calibration training sequence based on a minimal number of measurements. The aforementioned is what we refer to as *embedded self-calibration* in this thesis. Such a method would allow reducing the spread of

performance across PA parts and enable the PA manufacturer to guarantee more aggressive specifications by ensuring that a higher number of PA parts are operating at close to optimum performance. In turn, this will positively affect the time-to-market of the mobile equipment and potentially help in securing the edge over the competition. It will be further shown in Section 1.3 and Chapter 4 that the analytical PA representation for PA performance characterization proposed in this thesis may significantly contribute towards the realization of such an embedded self-calibration technique. An example where self-calibration would be useful is when the PA is subjected to dynamic biasing through the modulation of the gate bias as a function of the PA's envelope, to improve its linearity-efficiency trade-off. Embedded self-calibration would then allow performing the necessary adjustments on the dynamic bias applied to each PA part to reduce the spread in performance from one mobile unit to another, hence ensuring close-to-optimum PAE-linearity trade-off in every mobile unit.

Having explained this second research motivation, which will be reiterated in Chapter 4, we may now state our second problem statement as given in Section 0.1.4.

0.1.4 Problem Statement 2

There is a need for a method of power amplifier self-calibration that enables automatic optimization of PA performance across parts, from one mobile equipment to another. Such a method would allow each PA part in different mobile equipment to achieve close-to-optimum performance. To allow such a self-calibration method to be embedded within the mobile unit, it should use simple probing circuitry and require a simple training sequence based on only a minimum number of measurements.

0.2 Research objectives

With our research motivation clearly explained in Section 0.1, the objectives of the doctoral research work presented in this thesis are as follows:

Table 5. SKY85402-11 Electrical Specifications: General[1]
(VCC1 = VCC2 = VCC3 = 5.0 V, PA_EN = 3.3 V, T_{OP} = +25 °C, Unless Otherwise Noted)

Parameter	Symbol	Test Condition	Min	Typ	Max	Units
Frequency range	f		5.15		5.85	GHz
Output power	P_{OUT}	802.11ac, MCS9, -35 dB DEVM, HT80, 5 V	+20.5	+22		dBm
		802.11n, MCS7, -30 dB DEVM, HT40, 5 V	+23	+25		dBm
		MCS0, 5 V, HT20, mask compliant	+26	+27.5		dBm
1 dB output compression point	OP1dB	P_{IN} = CW	+28	+29		dBm
Small signal gain	|S21|		30	32	36	dB
Input return loss	|S11|		8	14		dB
Gain variation over band	Δ S21			±1.5		dB
2nd and 3rd harmonics	2fo, 3fo	P_{OUT} = +23 dBm		-50	-45	dBm/MHz
Rise and fall time	t_R, t_F			0.5		µs
Stability		P_{OUT} = +28 dBm, VSWR = 6:1, all phases	All non-harmonically related outputs < -50 dBm/MHz			-
Ruggedness	Ru	P_{IN} = +10 dBm, VSWR = 6:1, all phases	No damage			-

[1] Performance is guaranteed only under the conditions listed in this table.

Figure 0.2 Excerpt from a typical PA datasheet showing different specifications. The typical value, the upper limit and the lower limit of the guaranteed values of these different performance specifications are also shown
Taken from SKY85402-11 Datasheet (August 2018)

- To propose and demonstrate a new method of power amplifier design to improve the linearity-efficiency trade-off in RFIC PAs and which requires minimum additional overhead for implementation, i.e. minimum additional chip area, minimum additional power consumption and no external signal processing.

- To propose and demonstrate a multi-port analytical representation of PAs for the processing of the input modulated RF signal and any envelope-dependent dynamic biasing signal, and which facilitates accomplishing the research objective stated in the third bullet point below.

- To propose and demonstrate a method of self-calibration of PAs that is embedded within the mobile unit and based on the proposed multi-port analytical PA representation of the second bullet point above, for automatic performance optimization of open-loop and closed-loop PAs from one mobile unit to another.

0.3 Research contributions

The first investigations within the broader framework of my research work were started in Fall 2013, when I embarked on my Master's studies at ÉTS as part of an M.A.Sc.-Ph.D. integrated program, having been awarded the "ÉTS Excellence awards for international students – Master's-PhD Award." Besides completing the requisite courses, the research conducted during this period resulted in two publications. This work also formed the basis of some of the more theoretical aspects of my doctoral studies. The contributions are listed below, along with a brief description summarizing their content:

Sharma, S., & Constantin, N. G. (December 2013). Formulations for the Estimation of IMD Levels in an Envelope Feedback RFIC Amplifier: An Extension to Dynamic AM and PM Behavior. *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 32*(12), 2019-2023.

- The aforementioned paper extends Professor Constantin's previously published work for estimating PA IMD levels, by additionally accounting for PA nonlinearities arising from memory effects, with the help of novel formulations that describe a system of complex nonlinear equations. The intended application is for estimating the linearity requirements of circuit blocks typically found in the error signal paths of envelope feedback amplifiers, to facilitate the design and test of RFIC PAs within a computer-aided IMD test setup.

Sharma, S., & Constantin, N. (May 2014). *An Algorithm for IMD Computation in Automated Tests of RFIC Power Amplifiers.* Paper presented at the 2014 IEEE Canadian Conference on Electrical and Computer Engineering (CCECE).

- The above paper presents an algorithm for the computation of IMD levels in RFIC PAs. The algorithm is aimed at overcoming typically encountered convergence problems when solving systems of nonlinear equations associated with PA behavioural models. The algorithm is intended to facilitate the implementation of these behavioural models as part of a computer-aided IMD test setup.

Following this, I undertook a research internship at Skyworks Solutions, Inc., Ottawa. The focus of this internship was aligned along the axis of my first research problem stated in Section 0.1.2. As part of this work, I investigated, measured and performed design work on a complex industrial SOI CMOS PA platform. Various aspects of this work included examining techniques related to PA gate capacitance linearization, PA linearization, PA protection under Voltage Standing Wave Ratio (VSWR) mismatch, etc. Much of the original work stemming from the research started during this period, and then continued after, relate to **a novel concept that I have introduced during the course of my Ph.D. research: positive envelope feedback**, applied to RFIC PAs and that form the crux of the material presented in Chapter 2 and Chapter 3 of this thesis. The resulting research contributions are enumerated below:

Sharma, S., & Constantin, N. G. (January 2017). Amplifier architecture using positive envelope feedback. United States Patent Application nº 10,320,345 (Granted: June 2019).

- This patent application was filed on behalf of Skyworks Solutions Inc. after examination and approval by Skyworks' patent applications selection committee. It describes the design of PAs using positive feedback of the PA's instantaneous output envelope signal, for dynamic biasing aimed at improving PA performance.

Sharma, S., Soliman, Y., & Constantin, N. G. (April 2017). *Positive Envelope Feedback for Linearity Improvement in RFIC PAs.* Paper presented at the IEEE 2017 27th International Conference Radioelektronika.

- The aforementioned paper, awarded the ***Best Student Paper*** at the conference, introduces positive feedback of the instantaneous envelope signal at the PA's output for dynamic biasing of RFIC PAs. Results from the implementation of a 5.4GHz SOI CMOS PA are provided, demonstrating the improvement of the PA's linearity-efficiency trade-off through positive envelope feedback. The proposed technique requires minimum additional resources and does not endanger PA requirements related to stability and noise.

Sharma, S., & Constantin, N. G. (April 2017). Apparatus and methods for power amplifiers with positive envelope feedback. United States Patent Application nº 10,439,558 (Granted: October 2019).

- This patent application was filed on behalf of Skyworks Solutions Inc. after examination and approval by Skyworks' patent applications selection committee. It describes additional embodiments related to the design of PAs using positive envelope feedback, some of which are described in the Conclusion chapter of this thesis.

Another significant part of my doctoral research work, which aims at answering the second research problem stated in Section 0.1.4 and is covered extensively in Chapter 4 of this thesis, is related to the in-depth study, analysis and experimental evaluation of an equations-based behavioural model of PAs initially proposed by Professor Constantin. My theoretical and experimental investigations have allowed demonstrating the accuracy of the model, its benchmarking against other state-of-the-art models, as well as identifying various practical

implementation scenarios of its application for embedded self-calibration of PAs within the mobile unit. **To the best of the author's knowledge, a method specifically for embedded self-calibration of envelope-dependent dynamic biasing in a PA module within a mobile unit has not been reported.** The resulting research contributions are enumerated below:

Sharma, S., & Constantin, N. G. (September 2019). Power amplifier linearizing module and power amplifier system equipped therewith. United States Provisional Patent Application nº 62,972,179.

- This patent application was filed on behalf of ÉTS after examination by its research commercialization collaborator Aligo Innovation and describes a new analytical multi-port representation of PAs for use as a PA linearizing module. The representation is based on a multi-tone modulated input RF signal, a multi-tone modulated output RF signal and a multi-tone dynamic biasing signal. This multi-port representation facilitates the implementation of embedded self-calibration functions in the mobile unit to compensate for part-to-part variation of PA performances in different mobile equipment.

Sharma, S., & Constantin, N. G. (November 2019). Nonlinear Three-Port Representation of PAs for Embedded Self-Calibration of Envelope-dependent Dynamic Biasing Implementations. *IEEE Access, vol. 7,* 172796-172815.

- The above paper proposes a 3-port analytical PA representation based on distinct sets of nonlinear complex polynomials for the processing of the input modulated RF signal and any envelope-dependent dynamic biasing signal, for accurate prediction of distortion components at the PA's output as a function of the input and the dynamic biasing signals. The representation is intended for an application that enables automatic optimization of linearity performance in RFIC PAs with the help of embedded self-calibration functions within the transmitter front-end of mobile equipment. The applicability of the proposed representation is highlighted through simulation and benchmarking against experimental results, demonstrating accurate characterization of PA performances under different dynamic biasing techniques, for multiple RFIC PA platforms in different technologies.

Another contribution is related to a more detailed exploration of the positive envelope feedback technique associated with the first research problem. Within the same framework, the analytical PA representation associated with the second research problem is applied to facilitate the design methodology of positive envelope feedback PAs with the help of analytically derived formulations. This work resulted in the following research contribution:

Sharma, S., & Constantin, N. G. (December 2019). Positive Envelope Feedback for Linearity Improvement in RFIC PAs. *IEEE Access* (under revision).

- This paper gives a robust and more in-depth analysis of the design and implementation of positive envelope feedback in RFIC PAs. Additional implementation examples are provided compared to the first conference paper. An application is also shown to illustrate the use of the 3-port PA representation formulations to analytically determine the design requirements of the feedback components for ensuring stability and achieving optimum linearity of the closed-loop PA under positive envelope feedback.

Other contributions stemming directly or indirectly from my research conducted during my doctoral studies, some of them in the form of collaboration with colleagues, have resulted in other disseminations throughout the course of my studies. The more significant ones among these are listed below:

Sharma, S., Berthiaume, D., & Constantin, N. (2014). *Modèle estimant les niveaux de distorsion d'intermodulation d'un amplificateur de puissance sur puce à rétroaction d'enveloppe pour le comportement dynamique AM et PM.* Paper presented at the 2014 82e Congrès de l'Acfas.

Berthiaume, D., Sharma, S., & Constantin, N. (2016). *Low Current, 100MHz Bandwidth Envelope Detector for CMOS RFIC PAs.* Paper presented at the 2016 IEEE Canadian Conference on Electrical and Computer Engineering (CCECE).

Nobert, G., Sharma, S., & Constantin, N. (2017). *A Linearity and Predistorsion Characterization Bench for RF Power Amplifiers.* Poster presented at the STARaCOM Poster Session, Montreal.

The research contributions from my doctoral work are also listed in Table 0.1 for the reader's easy reference.

0.4 Organization of thesis

In the **current chapter**, the motivation for our research was presented, the research problems were identified, the research objectives were defined, and the resulting contributions from this doctoral work were highlighted. The remainder of the thesis is divided into four chapters. In **Chapter 1**, the state-of-the-art related to our research problems is reviewed. Existing techniques that target improving PA performances are described, as well as analytical representations that are used for characterizing PA behaviour. While listing the advantages of these existing techniques, we also focus on their insufficiencies which make them unsuitable in the framework of the research problems stated in Section 0.1.2 and Section 0.1.4. In **Chapter 2**, we introduce our proposed PA technique based on the novel concept of positive envelope feedback. The underlying theory is presented, and the design conditions that have to be necessarily respected to ensure successful implementation of positive envelope feedback in RFIC PAs are enumerated. Two different CMOS SOI PA implementations of positive envelope feedback are shown in **Chapter 3**, with a simulation example in Section 3.1 and an experimentally measured prototype in Section 3.2. Both implementations demonstrate the same trends and degree of linearity improvement under positive envelope feedback for the PA's higher range of operating power levels, and highlight the inherent simplicity of realizing positive envelope feedback in RFIC PAs. In **Chapter 4**, we introduce our novel multi-port analytical representation of PAs under dynamic biasing. The detailed formulations of this representation are derived, and the use of the representation for PA performance improvement under different scenarios are shown. We also introduce the idea of embedded self-calibration of PAs within the mobile unit in this chapter, and demonstrate the use of our proposed multi-port representation for the embedded self-calibration of various open-loop and closed-loop PA structures. In the **Conclusion chapter**, we summarize the work presented in this thesis as well as discuss its limitations, and identify topics stemming from my doctoral research work that solicit further investigation.

Table 0.1 Summary of main contributions from the research work presented in this doctoral thesis

Title	Authors	Details
Formulations for the Estimation of IMD Levels in an Envelope Feedback RFIC Amplifier: an Extension to Dynamic AM and PM Behavior	**Sharma, Smarjeet** and Constantin, Nicolas G.	*IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, vol. 32, no. 12, pp. 2019-2023, December 2013.
An Algorithm for IMD Computation in Automated Tests of RFIC Power Amplifiers	**Sharma, Smarjeet** and Constantin, Nicolas G.	*IEEE Canadian Conference on Electrical and Computer Engineering (CCECE)*, Toronto, May 2014, pp. 1-6.
Amplifier architecture using positive envelope feedback	**Sharma, Smarjeet** and Constantin, Nicolas G.	US Patent Application nº 10,320,345, January 2017. (Granted: June 2019)
Positive Envelope Feedback for Linearity Improvement in RFIC PAs	**Sharma, Smarjeet**, Soliman, Yasser and Constantin, Nicolas G.	*IEEE 2017 27th International Conference Radioelektronika*, Brno, April 2017, pp. 1-5. (***Best Student Paper***)
Apparatus and methods for power amplifiers with positive envelope feedback	**Sharma, Smarjeet** and Constantin, Nicolas G.	US Patent Application nº 10,439,558, April 2017. (Granted: October 2019)
Power amplifier linearizing module and power amplifier system equipped therewith	**Sharma, Smarjeet** and Constantin, Nicolas G.	US Provisional Patent Application nº 62,972,179, September 2019.
Nonlinear Three-Port Representation of PAs for Embedded Self-Calibration of Envelope-dependent Dynamic Biasing Implementations	**Sharma, Smarjeet** and Constantin, Nicolas G.	*IEEE Access*, vol. 7, pp. 172796-172815, November 2019.
Positive Envelope Feedback for Linearity Improvement in RFIC PAs	**Sharma, Smarjeet** and Constantin, Nicolas G.	*IEEE Access*, December 2019 (under revision).

Table 0.1 (continued)

Title	Authors	Details
Other selected contributions		
Modèle estimant les niveaux de distorsion d'intermodulation d'un amplificateur de puissance sur puce à rétroaction d'enveloppe pour le comportement dynamique AM et PM	**Sharma, Smarjeet**, Berthiaume, David and Constantin, Nicolas G.	*82e Congrès de l'Acfas*, Montreal, May 2014.
Low Current, 100MHz Bandwidth Envelope Detector for CMOS RFIC PAs	Berthiaume, David, **Sharma, Smarjeet** and Constantin, Nicolas G.	*IEEE Canadian Conference on Electrical and Computer Engineering (CCECE)*, Vancouver, May 2016, pp. 1-4.
A Linearity and Predistorsion Characterization Bench for RF Power Amplifiers	Nobert, Gabriel, **Sharma, Smarjeet** and Constantin, Nicolas G.	*STARaCOM Poster Session*, Montreal, December 2017.

CHAPTER 1

LITERATURE REVIEW

> "Bernard of Chartres used to say that we are like dwarves perched on the shoulders of giants, and thus we are able to see more and farther than the latter. And this is not at all because of the acuteness of our sight or the stature of our body, but because we are carried aloft and elevated by the magnitude of the giants."
>
> John of Salisbury

In the first part of this chapter (Section 1.1 and Section 1.2), the linearity-efficiency trade-off in RFIC PAs that was introduced previously in Section 0.1.1 is briefly described again, as well as the motivation to improve this trade-off in the context of PAs transmitting envelope-modulated signals. Some existing well-known techniques that are used for the improvement of RFIC PA performances are reviewed, and their various advantages as well as their disadvantages are analyzed. Particular attention is paid to envelope-dependent biasing techniques of PAs and to PA architectures based on negative feedback while emphasizing on the need for design methods that allow realizing a fully integrated standalone PA solution. In the second part of this chapter (Section 1.3 and Section 1.4), a review of the state-of-the-art analytical RFIC PA representations is presented. Representations that target characterizing the relationships among the input port, output port and control port signals in RFIC PAs are highlighted, with specific attention to a recently proposed approach based on a modified first-order Volterra series approximation. The features and deficiencies of these approaches are pointed out in the context of an analytical representation that is suitable for embedded self-calibration of the PA within the mobile unit, a concept introduced in Chapter 4 of this thesis.

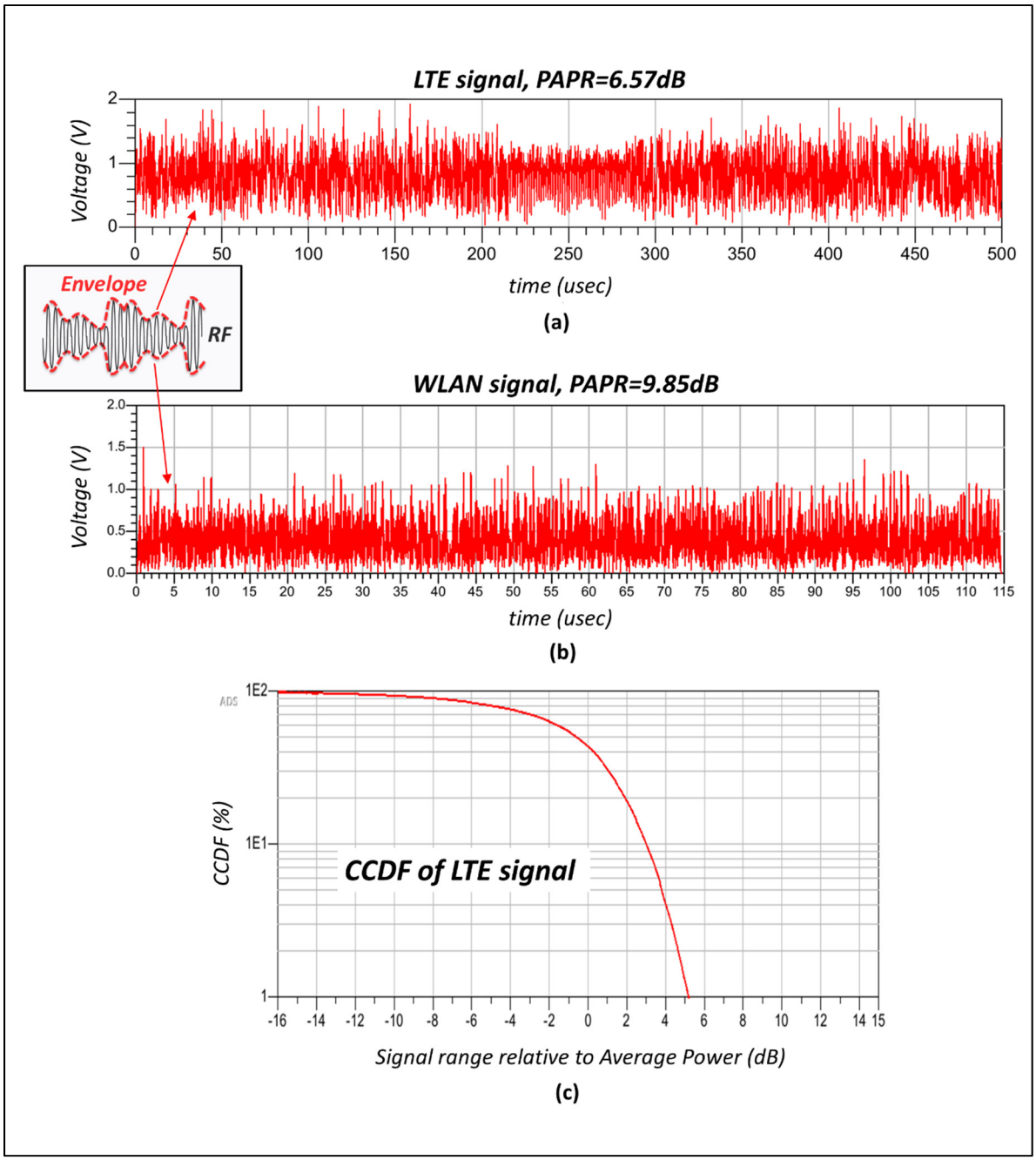

Figure 1.1 Simulated transient form of (a) an LTE signal (b) a WLAN signal, exhibiting PAPR values that are typical of modern communication signals. The signal is generated using examples in the default design libraries from Keysight ADS^{TM}. The CCDF plot of the LTE signal is also shown in (c), to illustrate the probability of the different excursions of the instantaneous signal power (envelope power) from its average power value

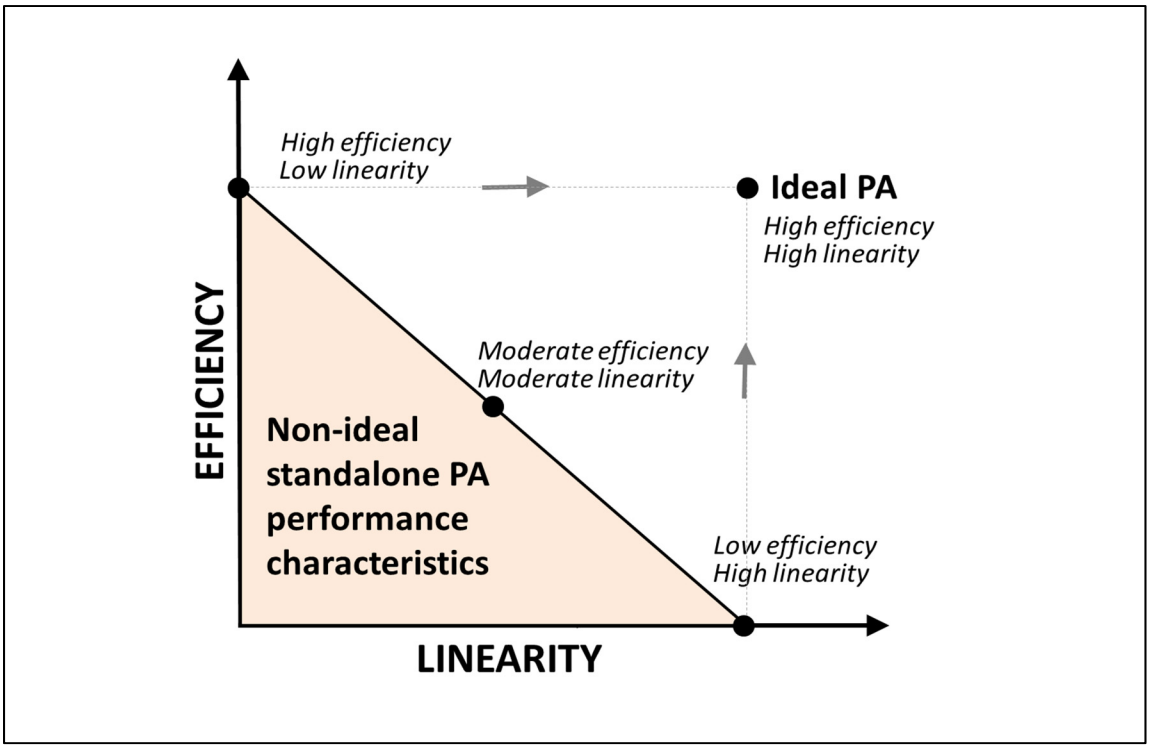

Figure 1.2 Illustration of linearity-efficiency trade-off in RFIC PAs. Improved PA linearity comes at the cost of increased current consumption resulting in poorer PA efficiency. Similarly, improving PA efficiency necessitates reducing the PA's current consumption that translates into poorer PA linearity

1.1 Improving the linearity-power efficiency trade-off in RFIC PAs – An overview

The design of RFIC PAs that simultaneously satisfy stringent efficiency and linearity requirements is a constant challenge. The challenge is more difficult for RFIC PAs transmitting envelope-modulated signals, such as those in Wideband Code-Division Multiple Access (WCDMA), Long-Term Evolution (LTE) and the 5G-New Radio (NR) standards, where the instantaneous output power may be several dB higher than its average output power (Pedro, Carvalho, Fager, & García, 2004; Lavrador, Cunha, Cabral, & Pedro, 2010). Examples of the transient form of a modulated LTE signal and a modulated Wireless Local Area Network (WLAN) signal, and the associated Complementary Cumulative Distribution Function (CCDF), are given in Figure 1.1, showing that the signal's instantaneous power

(referred to also as envelope power) may be more than 9.5dB higher than its average power (for some WLAN signals, this can even be greater than 12dB). Hence, the PA is required to be both linear and efficient not only at its rated average power level but over the extensive range of instantaneous power (envelope power) levels determined by the peak-to-average power ratio (PAPR) of the particular type of modulated signal that it is transmitting (J. C. Pedro, 2003). Additionally, for reasonable efficiency at considerable back-off power levels to enable extended battery life, the quiescent current consumption of the PA has to be low, while still ensuring that the PA satisfies stringent linearity/efficiency specifications at higher (rated) power levels (Park et al., 2016). The above gives rise to what is commonly referred to as the PA's linearity-efficiency trade-off and was discussed in Section 0.1, and is also illustrated conceptually in Figure 1.2 here. Such performance requirements make class-AB PAs a popular choice for RFIC PAs in mobile applications, where the linearity-efficiency trade-off of the power amplifier in the transmitter front-end is a critical design parameter (Park et al., 2016; Ali, Agarwal, Baylon, & Heo, 2017; Yu, Feng, & Zhao, 2018).

Class-AB PAs offer a performance compromise between class-B PAs (high efficiency, low linearity, low quiescent current) and class-A PAs (low efficiency, high linearity, high quiescent current) (Park et al., 2016). Class-A PAs are biased to have a conduction angle of 360°, i.e. the PA is amplifying for 100% of the transmitted signal's time period. While this ensures high linearity, it comes at the cost of high quiescent power consumption and consequently low power efficiency. On the other hand, class-B PAs are biased to have a conduction angle of 180°, i.e. the PA is amplifying for only 50% of the transmitted signal's time period. The lower quiescent current consumption results in higher power efficiency but also results in higher levels of output signal nonlinearity due to increased signal distortion. Class-AB PAs are biased to have a conduction angle between that of class-B PAs (180°) and class-A PAs (360°). For a small input signal, a PA biased for class-AB operation transmits the entire signal without clipping, i.e. the PA operation is similar to that in class-A. However, for larger values of input signal amplitude, part of the PA's output signal may be clipped. Such signal clipping occurs because for large values of the input signal amplitude, the class AB PA suffers from decreasing transconductance due to the MOS transistors being forced

into the triode region of operation, or the BJT devices being forced into the saturation region of operation. Signal clipping is described with greater detail in Section 2.1. The class-AB PA is nonetheless transmitting for more than 50% of the transmitted signal's time period, resulting in a performance compromise between the extremities of class-A and class-B PAs. A comparison of the transient form of the PA's drain/collector current (for an input signal excitation of adequately large amplitude) under these different classes of operation is shown in Figure 1.3.

However, class-AB PAs often require additional circuit techniques to meet linearity requirements that cannot always be achieved with the standalone PA by itself, particularly at higher output powers when large-signal effects become significant (Park et al., 2016; P. Asbeck & Popovic, 2016; Tam et al., 2015).

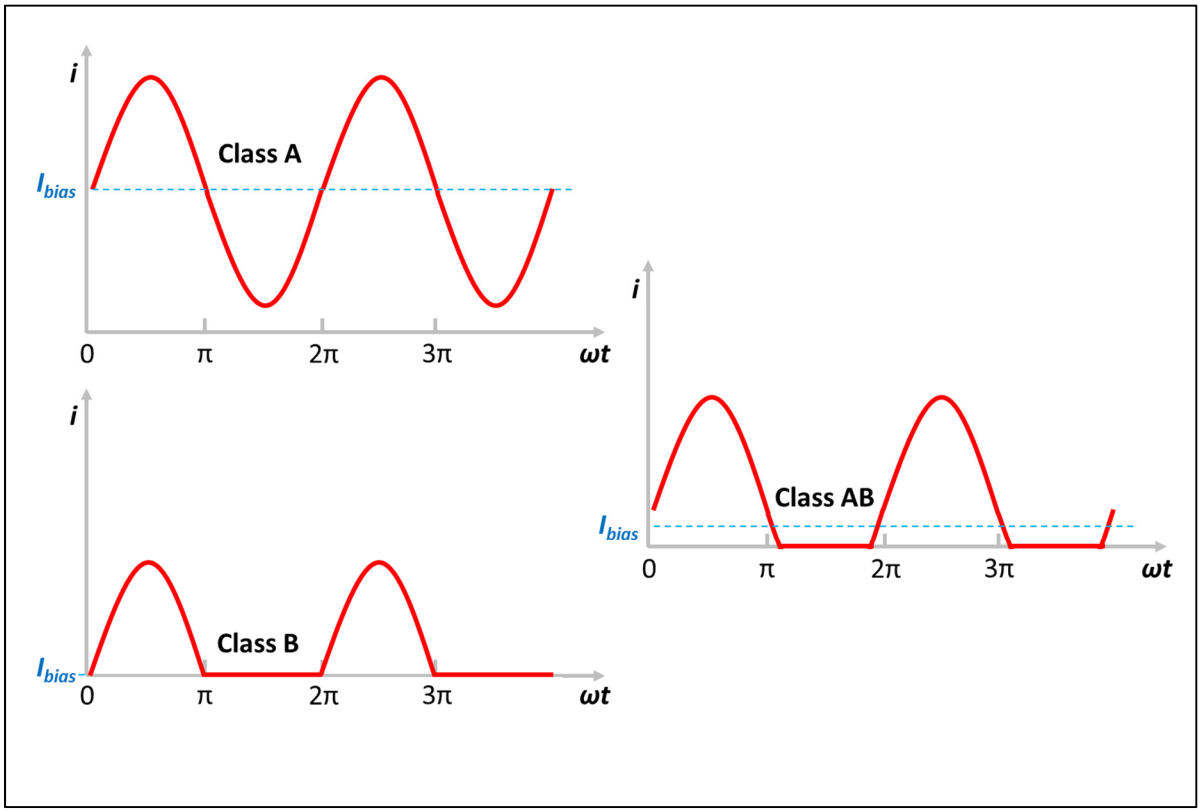

Figure 1.3 Comparison of transient form of the transistor's drain/collector current under Class A, Class B and Class AB PA operation

One possible solution to meet the linearity requirements at higher power levels is by increasing the PA transistor device size and operating the PA at adequate power back-offs. However, such an increase in the device size is accompanied with an increased quiescent current requirement that adversely affects PA efficiency at lower power levels or when the PA is not transmitting. Improving the PA's linearity at higher power levels while still ensuring efficient operation at back-off power levels constitutes a linearity-efficiency trade-off that is critical to any PA design, and which the technique introduced in Chapter 2-3 of this thesis aims to improve.

1.1.1 Some existing PA architectures for improving PA performance

In this section, some important current PA architectures that target improving the PA's linearity-efficiency trade-off are presented. The PA architectures described here are Envelope Tracking (ET) (Asbeck & Popovic, 2016), Doherty PAs (Onizuka, Ikeuchi, Saigusa, & Otaka, 2012), "ON/OFF" switching of transistor matrices (Joung, Ho, & Sun, 2013), tunable matching networks (Hedayati et al., 2012), and digitally-controlled PAs (Presti, Carrara, Scuderi, Asbeck, & Palmisano, 2009). While this list of PA architectures given here is by no means exhaustive, we have decided to focus on the more significant ones. Though effective at improving PA performances, the implementations of these techniques present their own set of challenges, especially in the context of circuit techniques that are simple enough to allow their realization as a fully integrated standalone PA solution on a single chip. Some of these issues described next highlight the need for circuit techniques that do not entail using extensive additional hardware or signal processing, or both.

1.1.1.1 Envelope Tracking (ET) PAs

Envelope Tracking is a popular design technique that allows improving the Power Added Efficiency (PAE) of PAs transmitting envelope-modulated signals with a large PAPR, such as those shown in Figure 1.1 and described extensively previously. An example of a possible ET PA implementation is shown in Figure 1.4.

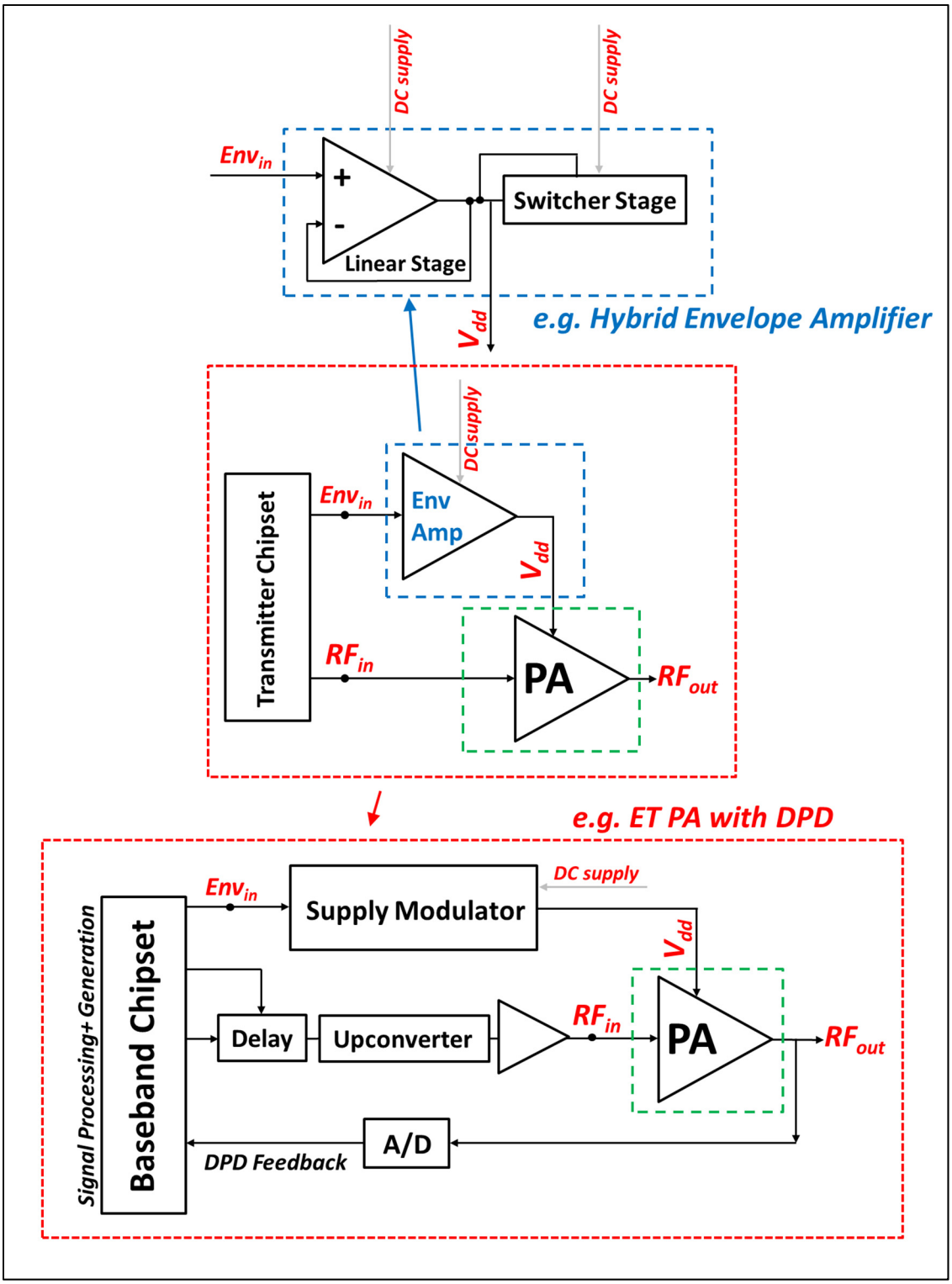

Figure 1.4 Implementation of Envelope Tracking PAs
Adapted from Asbeck & Popovic (2016)

The basic tenet of envelope tracking is to use a drain supply voltage (V_{dd} in Figure 1.4, at the output of the envelope amplifier *Env Amp*) that *tracks* the time-varying envelope Env_{in} of the PA's transmitted signal, instead of using a fixed DC voltage *DC supply*. The drain voltage is kept low for low values of the signal envelope; similarly, for higher values of the signal envelope, the drain voltage is kept higher. The PA is therefore constantly operated under compression and not just at the maximum power level, thereby theoretically ensuring close-to-maximum PA efficiency even at significant back-off power levels. The effect of Envelope Tracking on maximizing the PAE is also seen through equation (0.1), where the DC power (P_{DC}) is minimized by keeping the envelope-dependent time-varying supply at the lowest value possible without driving the transistor into saturation (BJT) or cut-off (MOSFET). Without delving into the details regarding the implementation of ET PAs, we focus instead on some of the challenges that are associated with ET PA architectures.

While calculating the overall system efficiency of the ET PA, besides the losses of the basic PA transistor line-up, a significant source of power loss that has to be taken into account is that of the envelope amplifier *Env Amp* shown in Figure 1.4, also alternatively referred to as the *Supply Modulator* in ET PAs. A simplified schematic of one possible envelope amplifier design that is currently used is shown within the blue dotted box at the top in Figure 1.4 and is composed of a linear stage and a switcher stage in cascade. The linear stage inherently suffers from poor efficiency, and such a poor efficiency necessarily affects the performance of the entire ET PA system negatively. Besides its efficiency, other design parameters of the *Env Amp* that are critical for the performance of the overall ET PA system are its accuracy, noise performance and its slew rate, the latter assuming increased relevance in light of the large bandwidth signals envisaged for future mobile communication systems. It has also been shown that the efficiency of the supply modulator (and therefore the ET PA system) drops substantially with increasing bandwidth (e.g. due to transistor parasitics in the *Env Amp* switcher). Such efficiency impairments encourage speculation that for future wideband applications, ET techniques alone cannot meet all the PA requirements and must be used in conjunction with other methods that are not bandwidth restricted (P. M. Asbeck, Rostomyan, Özen, Rabet, & Jayamon, 2019).

Such performance constraints of the envelope amplifier often force its design to be fabricated using a device technology different from that used for the basic PA itself. It, therefore, requires the implementation of the PA and the envelope amplifier using separate Monolithic Microwave Integrated Circuit (MMIC) modules and reduces the possibility of implementing ET PAs as a single-chip solution. While separate MMIC modules are easily realizable for base-station PA applications, single-chip integration can greatly enhance the likelihood of any PA architecture to be incorporated into handheld devices. In fact, most ET PA implementations in handheld devices are still based on average-power tracking (APT), which is less complex to implement, and therefore not based on a truly envelope-dependent supply voltage modulation (Asbeck & Popovic, 2016).

Additionally, ET PA designs can quickly become complex, as illustrated with the system shown within the red dotted box at the bottom in Figure 1.4. Here the linearity degradation of the efficient supply-modulated PA is corrected with the help of Digital Pre-Distortion (DPD) techniques that are implemented using Digital Signal Processors (DSPs) (Hekkala, January 2012). While theoretically feasible, the power consumption of the DSP and the additional space/resource requirements to implement DPD - and further aggravated by the stringent specifications for the supply modulator - makes the viability of implementing such complex ET PA architectures in handheld devices a more contentious topic, especially as the bandwidth becomes large.

1.1.1.2 Doherty PAs

Doherty PAs, first demonstrated by William H. Doherty of Bell Telephone Laboratories Inc. in 1936, has enjoyed a steady return to many commercial platforms since the advent of the transistor. Unsurprisingly, it also continues to be an active area of research. Figure 1.5 illustrates the basic structure of the Doherty PA, comprising a main (or carrier) PA and a peaking PA.

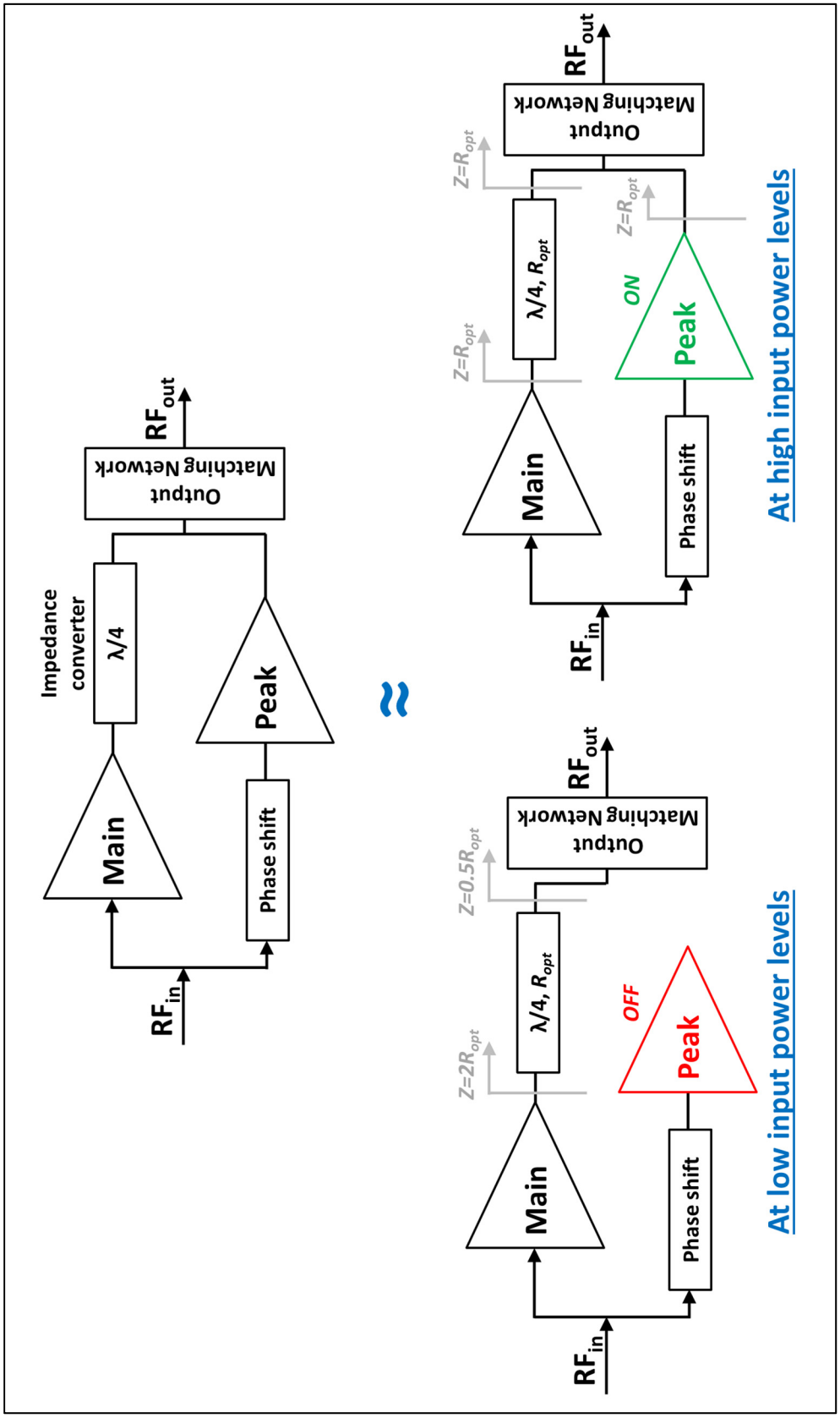

Figure 1.5 Implementation of Doherty PAs
Adapted from Zhao, Liu, Wu, & Kang (2017), Qi & He (2019) and T.Burns (2013)

The main PA is biased in Class AB or Class B region of operation, while the peaking PA is biased in Class C. For low and average envelope power levels, the peaking PA is OFF and only the main PA is conducting, while for high envelope power levels (i.e. for *peak* signal power levels), the main and the peaking PA operate simultaneously. As shown in Figure 1.5, the main PA operates on the $2\text{x}R_{opt}$ load-line in the low power mode. In the high power mode, both the main PA and the peaking PA operate on the R_{opt} load-line. The output matching network and the load-impedance (e.g. 50Ω) remain constant throughout. The load modulation necessary for the main PA to operate on the $2\text{x}R_{opt}$ load-line when the peaking PA is OFF is achieved using the quarter-wave transformer (of characteristic impedance R_{opt}), which performs the necessary conversion from $Z=0.5\text{x}R_{opt}$ (at its terminal towards the output matching network) to $Z=2\text{x}R_{opt}$ (at its terminal towards the main PA). The respective load-lines over different output envelope power levels ensure elevated PA efficiency values over a significant range of operating envelope power, and the near-flat high-efficiency curve characteristic to Doherty PAs over the span of envelope power levels when the peaking PA is ON, i.e. theoretically a 6dB range below the rated maximum output envelope power.

While Figure 1.5 illustrates the conventional Doherty architecture, there have been tremendous advances in this field, and varying flavours of the basic Doherty structure have been demonstrated to achieve good performances. While these structures are not explicitly given in this thesis, some of them are multi-way Doherty (Kang et al., 2017), Doherty outphasing (Jang et al., 2016), dual-in Doherty (Darraji, Mousavi, & Ghannouchi, 2016) and inversed Doherty (Ahn et al., 2007). These different architectures are synthesized using different flavours of the conventional architecture shown in Figure 1.5 – the type of input signal splitting, the number of branches, the ratio in size between the main PA and the peaking PA, etc. For example, asymmetric sizing of the main and the peaking PA has been proven to extend the power range over which efficiency is improved (Son, Kim, Moon, Lee, & Kim, 2011; Koo et al., 2018). Increasing the number of peaking PA branches has also been shown to have a similar effect (Wong, Watanabe, & A. Grebennikov, October 2017). Advanced designs may employ DSP to correct the Doherty PA's linearity (Yu, Iwamoto, Larson, & Asbeck, 2003), envelope-dependent dynamic biasing for the peaking PA to enable

further improvement of efficiency (Onizuka, Ikeuchi, Saigusa, & Otaka, 2012), ET operation during low-power operation to increase efficiency through supply modulation (Zhang & Xin, 2014; Moon et al., 2010), etc.

Despite the remarkable performances that have been demonstrated in the literature for Doherty PAs, its single biggest drawback arises from its implicit complexity that is difficult to circumvent. For example, even the conventional Doherty design of Figure 1.5 offers many difficulties during circuit realization – parasitics and matching circuits introduce unwanted phase offsets; the phase shifts have to be carefully designed for, tolerances on the characteristic impedances have to be accounted for while designing the quarter-wave transformers, etc. The desired efficiency improvement also has to be achieved over the signal bandwidth and dynamic power range of interest, both of which are a challenge in the context of the large PAPR, significant bandwidth signals that are characteristic of modern communication standards. Additionally, to begin with, the structure shown in Figure 1.5 is large, and the various modified Doherty architectures mentioned previously can quickly become unfeasibly complex, resource-hungry and space-hungry. Complex PA structures also invariably introduce heightened levels of variation from one PA unit to the other, resulting in lower manufacturing yield. All these factors justify the fact that, to date, no Doherty PA has been implemented as a single-chip IC, and these same factors suggest that this is simply not possible despite the excellent performances that are found in the literature.

1.1.1.3 Switching PAs

Figure 1.6 is an example of a switching mode PA, a type of PA architecture aimed at efficiency improvement through the switching ON or OFF of different arrays of transistors (Joung, Ho, & Sun, 2013). As shown, such a PA design consists of a PA bank comprising m different PA blocks (PA_1, PA_2, … PA_m) designed to deliver m different ranges of power levels to the load. In Figure 1.6, the PA load interfaces with the transmit antennas T_{x1} or T_{x2}, the choice itself of which is made via switch S_2.

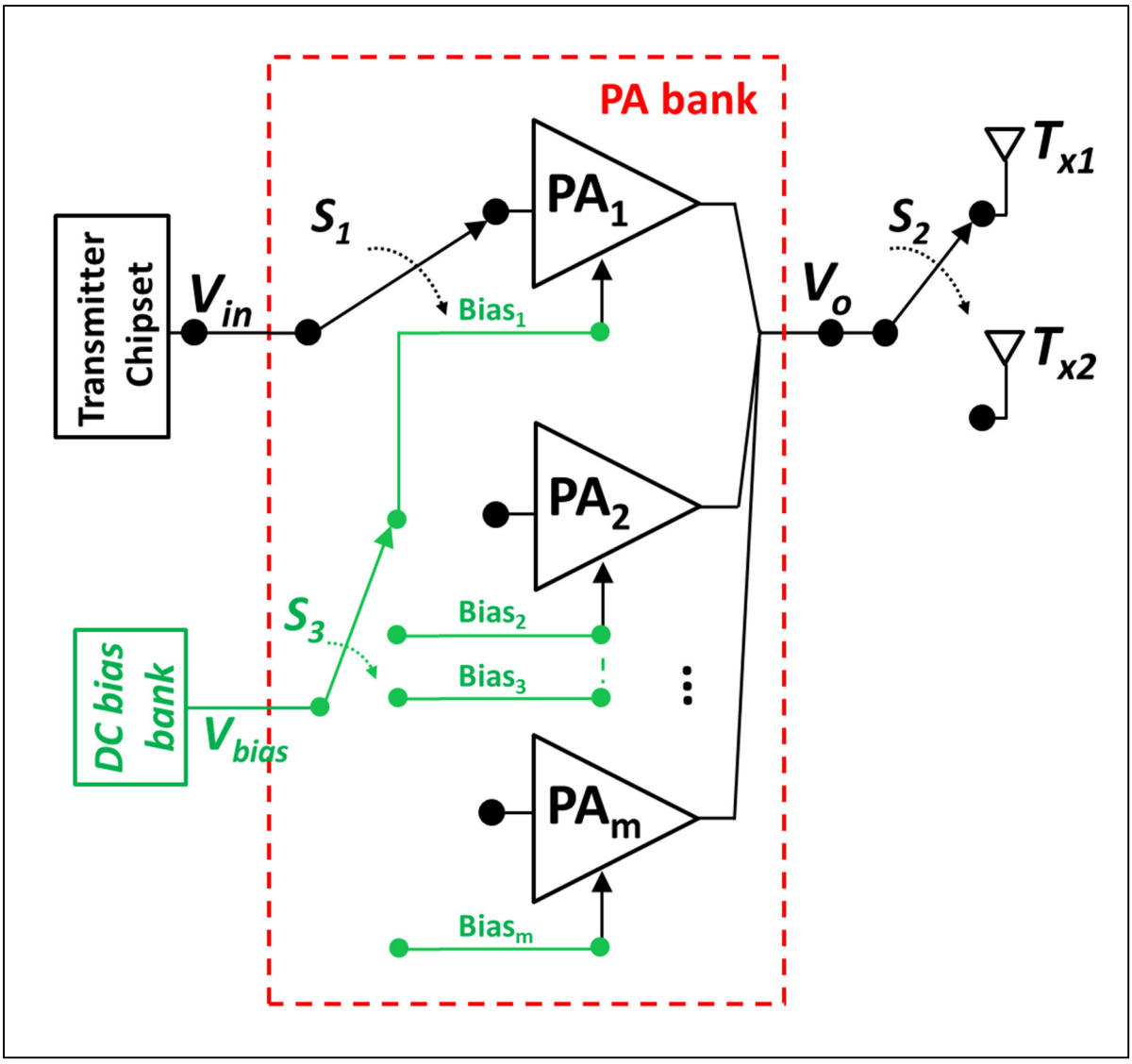

Figure 1.6 Implementation of switching PAs
Adapted from Joung, Ho, & Sun (2013)

Each PA block within the PA bank is designed to optimally deliver one particular range of power levels, and the choice of which PA block to use at any given power level is made using the control signal of switch S_1. The input and output matching networks may be common to all the PA blocks though they may also be designed and optimized for each PA block separately but at the cost of significantly added complexity and circuit area. In the implementation shown in Figure 1.6, independent control of the bias of each PA block is also

enabled to allow optimizing PA efficiency further. For any given power level that the PA is transmitting, only one PA block in the PA bank is ON and transmitting, while all other PA blocks are OFF.

However, the efficiency improvement from using the PA architecture shown in Figure 1.6 comes at the cost of linearity degradation at back-off power levels. This linearity degradation arises due to the use of multiple switching at discrete power levels, which inevitably introduces variations in PA gain when the switching is triggered. A convenient and popular workaround for such linearity degradation is the use of gain calibration algorithms to flatten the switching PA's gain and, therefore, its linearity. However, to implement such linearization algorithms requires the use of external processors that must be incorporated into the design. While switching PA architectures such as the one shown in Figure 1.6 are complex already, the requirement for additional signal processing (along with the associated power consumption, circuit area, cost, etc.) present added challenges which make it difficult for single-chip integration in a handheld device. The computation overhead of the processors used for implementing the gain control algorithms may also prove to be a limitation, especially in the context of the very fast-varying envelope signals planned for deployment in future mobile communication standards.

1.1.1.4 Other PA architectures

Other PA architectures of interest include PAs that employ tunable matching networks (Hedayati et al., 2012) and digitally controlled PAs (Presti, Carrara, Scuderi, Asbeck, & Palmisano, 2009). While digital signal processors are critical for the implementation of digitally controlled PAs, PAs that use tunable matching networks suffer from the same linearity degradation due to the use of switching schemes triggered at discrete power levels, as described earlier for ON-OFF PAs. This linearity degradation also necessitates the use of gain calibration algorithms that require external processors for their implementation (Hedayati et al., 2012; Presti, Carrara, Scuderi, Asbeck, & Palmisano, 2009). The use of such

external hardware for signal processing that is necessary for such techniques makes it difficult to implement as a single-chip solution.

In light of the deficiencies pointed out for the above-mentioned PA techniques, a circuit technique that enables PA performance improvement without the use of additional sophisticated hardware offers a more viable alternative towards realizing a fully integrated PA solution. When adequately simple, such a circuit technique affords the possibility of incorporating it as a functional block into existing PA architectures, as well as using it in conjunction with other PA performance improvement techniques. Simplicity of PA circuit techniques is especially important in the context of PAs targeting millimetre-wave 5G applications, where it is envisaged that digital techniques alone cannot fully answer all PA linearity requirements and must possibly be used in conjunction with analog techniques (P. M. Asbeck, Rostomyan, Özen, Rabet, & Jayamon, 2019; Fager et al., 2019).

1.1.2 Dynamic gate biasing of PAs

Another method to improve PA performances is through dynamic biasing of the PA transistor's gate/base. The earliest investigations of such dynamic biasing include evaluating the effect on PA performance by manually varying its DC bias (Miers & Hirsch, 1992; Ghannouchi, Cardinal, & Hajji, 1995). Implementations of changing the PA's bias as a function of its average power include PA architectures where the bias signal relies on an optimized external control signal (Nam & Kim, 2007), where different bias-signal values are triggered at distinct, discrete average input power levels using off-chip switches (Forestier et al., 2004), and where the bias signal is tuned externally (Lau, Xue, & Chan, 2007; Sahu & Rincon-Mora, 2007), all aimed at the PA's linearity/efficiency improvement. However, when transmitting modulated signals with significant PAPR, dynamic biasing that is dependent on *average* power levels can improve PA performances at large back-off power levels only, while PA performances at higher instantaneous envelope output powers (where the high currents severely degrade the PAE) are minimally affected in terms of improvement.

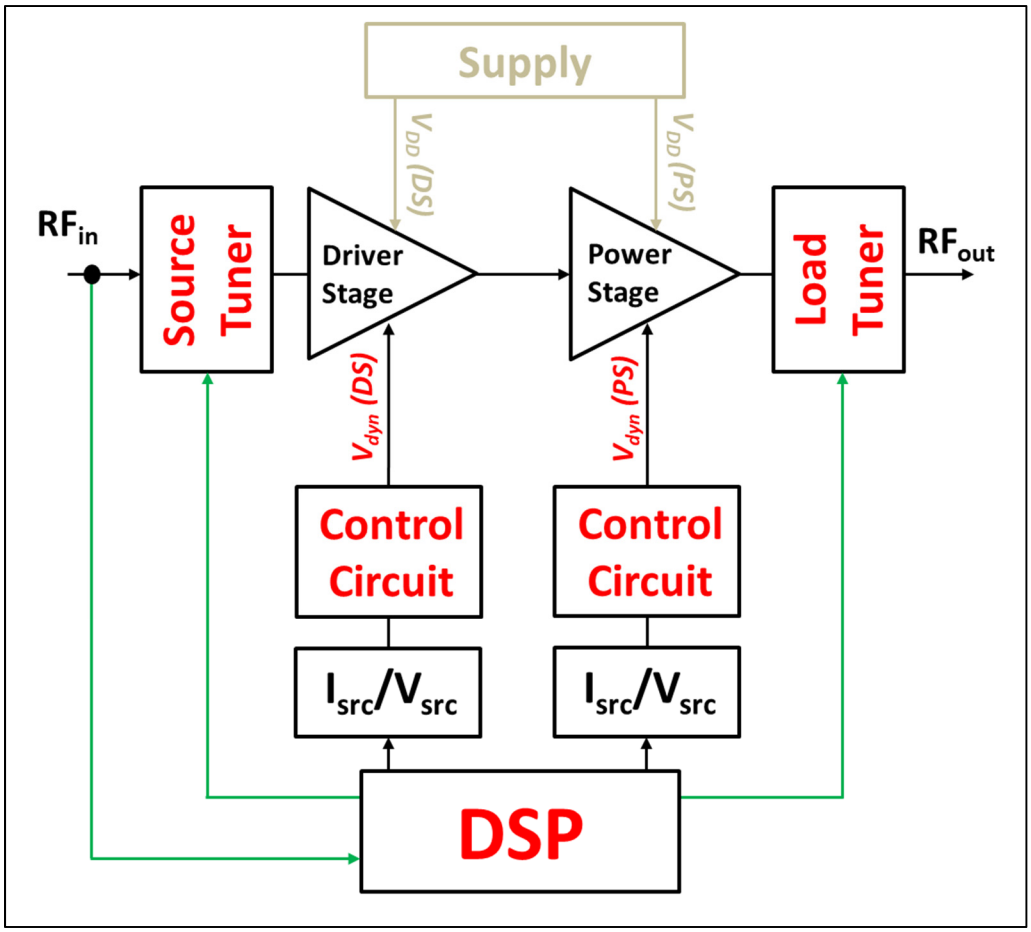

Figure 1.7 Implementation of dynamic biasing using extensive hardware
Adapted from Deltimple, Leyssenne, Kerhervé, Deval, & Belot (2010)

1.1.2.1 Envelope-dependent dynamic gate biasing of PAs

Implementations of dynamic biasing as a function of the PA's instantaneous envelope power levels have also been shown. The work of (Deltimple, Leyssenne, Kerhervé, Deval, & Belot, 2010) is based on a switched-cell PA design for improved efficiency, with discrete PA power cells that are switched ON or OFF based on the value of an input envelope power-dependent control signal. The linearity degradation arising from the switching scheme is corrected with the help of digital signal processing. (Medrel et al., 2013; Tafuri, Sira, Jensen, & Larsen, 2013) demonstrates dynamic biasing based on input envelope power detection, and relies exclusively on extensive external signal processing to extract the optimum bias signal

function for linearity/efficiency performance. However, the realization of these techniques described in (Deltimple, Leyssenne, Kerhervé, Deval, & Belot, 2010; Medrel et al., 2013; Tafuri, Sira, Jensen, & Larsen, 2013) as a single-chip solution is difficult due to the requirement for external hardware (including for signal processing), as shown in Figure 1.7.

On the other hand, on-chip envelope detection to improve PA performances is reported in (Onizuka, Ikeuchi, Saigusa, & Otaka, 2012; Po-Chih et al., 2008; Koo, Joo, Na, & Hong, 2012). In (Onizuka, Ikeuchi, Saigusa, & Otaka, 2012), a feed-forward architecture is used for PA efficiency improvement in a Doherty design, by using an envelope detector at the PA's input node to generate the dynamic bias for the sub-PA. In (Po-Chih et al., 2008; Koo, Joo, Na, & Hong, 2012), an envelope detector at the driver-stage output is used to modulate the succeeding power-stage bias in a feed-forward biasing scheme aimed at linearity improvement. A generic illustration of such feed-forward PA architectures is shown in Figure 1.8.

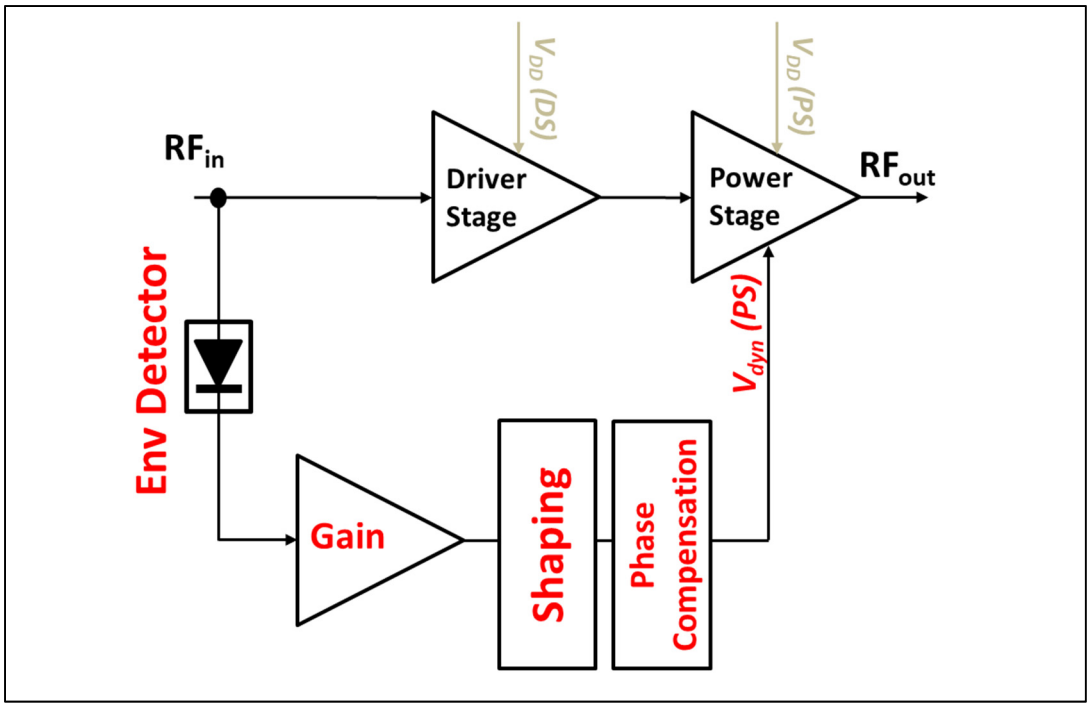

Figure 1.8 Implementation of feed-forward envelope-dependent dynamic biasing
Adapted from Po-Chih et al. (2008) and Koo, Joo, Na, & Hong (2012)

While on-chip envelope detection removes the problems regarding on-chip integration posed by the use of external signal processing elements, feed-forward dynamic biasing schemes based on input or driver-stage envelope detection to generate the PA's power-stage dynamic bias have their own drawbacks. For example, these implementations rely on input envelope power detection to approximate the PA's output envelope. While this approximation is generally valid, it fails to account for variations in the PA's power-stage bias, temperature, etc. that may critically affect its output signal envelope. Additionally, feed-forward dynamic biasing schemes based on input envelope detection require the implementation of shaping circuits and phase compensation circuits, which contribute to increased circuit complexity (Tafuri, Sira, Jensen, & Larsen, 2013; Koo, Joo, Na, & Hong, 2012). The amplitudes of the PA's input envelope signal are also relatively small compared to the amplitudes of the PA's output envelope signal, and the need for adequate envelope power resolution requires the input envelope detection to incorporate signal amplification in the feed-forward path (Koo, Joo, Na, & Hong, 2012). Such signal amplification may result in noise degradation at the PA output due to input noise amplification through the feed-forward path. As will be shown in the succeeding sections, the envelope-dependent dynamic biasing technique based on the positive envelope feedback concept introduced in this thesis does not suffer from these disadvantages.

1.1.3 PA architectures based on negative feedback

Before introducing PAs based on positive envelope feedback in Chapter 2 of this thesis, it is useful to distinguish the approach from PA architectures based on *negative* feedback, e.g. (Zargari, 2012; Katz, Wood, & Chokola, 2016; Kang, Baek, & Hong, 2017). Negative envelope feedback PA architectures are based on feeding back an inverted version of the PA's output envelope signal to its input to reduce distortion. Sometimes also referred to as indirect negative feedback technique, this technique is illustrated in Figure 1.9, where the PA's input and output envelopes are detected, compared (after appropriate amplitude scaling and phase alignment), and the resulting baseband error signal is used to control the gain and phase of a pre-amplifier block to optimize the linearity of the entire PA system. The principle

of negative envelope feedback relies on the loop dynamics working towards matching the scaled-down RF output envelope with the reference RF input envelope by adjusting the pre-amplifier's RF gain and phase, such that the error signal tends to zero.

Direct negative feedback, i.e. a feedback process that depends on the complete amplitude-modulated and phase-modulated RF signal (as opposed to an envelope-only signal), has also been proposed for PA linearization. A recent example is shown in (Kang, Baek, & Hong, 2017). Here, a cold-FET transistor (i.e. acting as a variable resistor, and not as an amplifier) in series with a capacitor-resistor network is added in a negative feedback loop to the power-stage transistor, and results in a desirable AM-to-AM or AM-to-Phase Modulation (PM) improvement (or both) effect at higher power levels. Input envelope-based control of this cold-FET transistor is used to linearize the PA performance further in (Kang, Sung, & Hong, 2018).

However, negative feedback techniques are associated with their own disadvantages. As shown in Figure 1.9, the use of two envelope detectors Det_{in} and Det_{out} that ideally must be perfectly matched (both in terms of frequency response and distortion characteristics) adds to the circuit's complexity, which is compounded by provisions of voltage scaling and high-order loop stability compensation circuits that are often found to be necessary (Zargari, 2012). Attention must also be paid to ensure that the delay of the error amplifier in Figure 1.9 does not limit the maximum signal bandwidth that can be supported when using negative feedback (Katz, Wood, & Chokola, 2016). The delay in the error signal path translates into the need for high-order phase compensation circuitry to ensure stability, and this can only be achieved over relatively narrow bandwidths, thereby prohibiting the applications of negative envelope feedback in modern transmitter designs. Negative feedback also commonly relies on a high loop gain, which demands careful design considerations to ensure that PA output noise performance is not adversely affected due to such a high gain being applied to the input or output noise (or both) and then being injected into the PA transmit chain. Because of the above limitations mainly, the implementation of negative envelope feedback is unsuitable as a viable linearity improvement technique in modern RFIC PA designs.

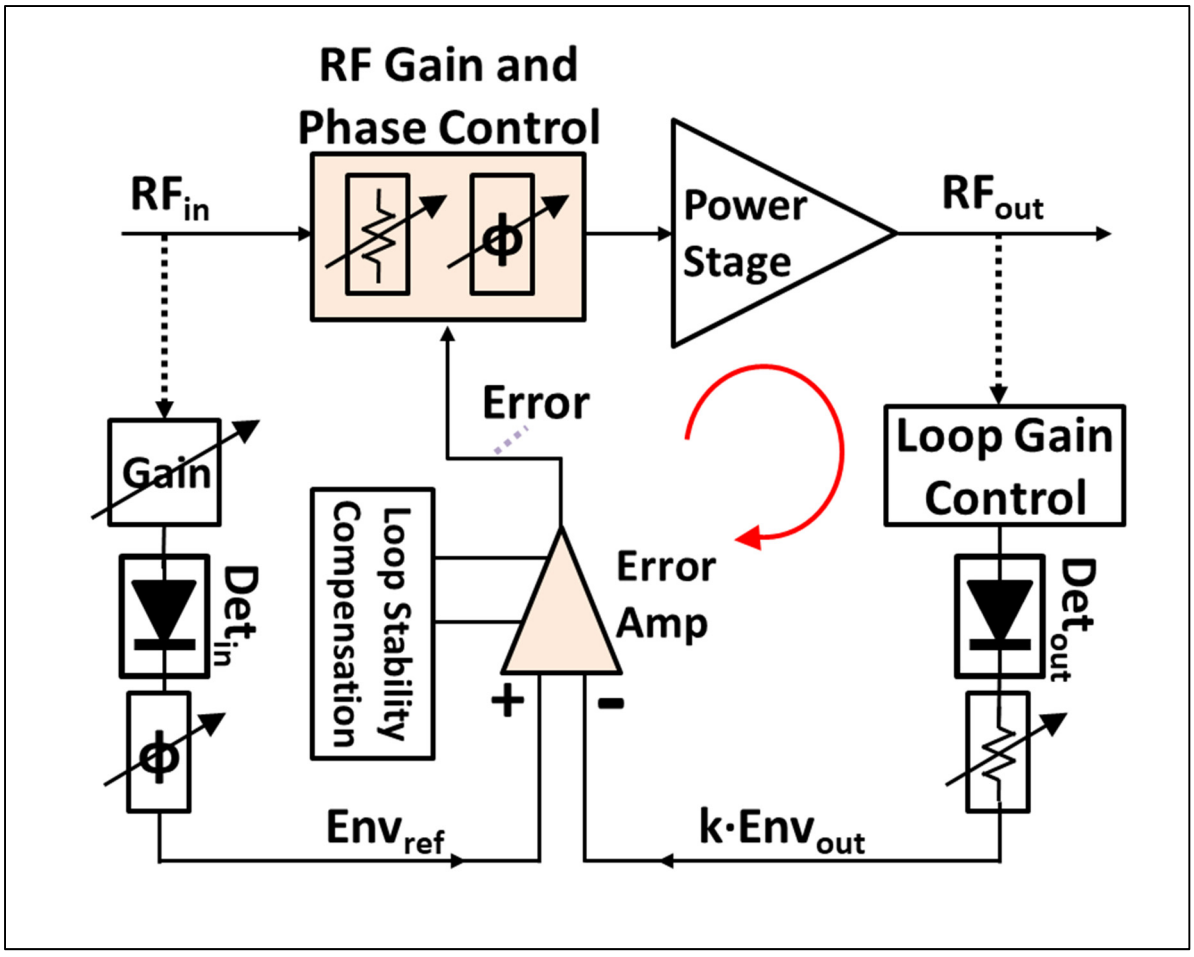

Figure 1.9 Schematic of state-of-the-art implementation of negative envelope feedback in RFIC PAs
Adapted from Zargari (2012) and Katz, Wood, & Chokola (2016)

1.2 Summary of existing techniques

Table 1.1 is a summary of the advantages and disadvantages of the various PA design techniques described in Section 1.1. As may be observed, several characteristics pertaining to the aforementioned PA techniques make them difficult to implement as a feasible single-chip standalone PA solution. Consequently, there is a need for a viable circuit technique that improves PA linearity-efficiency performances without the drawbacks mentioned in Table 1.1.

Table 1.1 Summary of advantages and disadvantages of various RFIC PA design techniques

Design Technique		Advantages	Disadvantages
ET PAs		ET ensures high PAE over a large range of the PA's envelope power levels, including at back-off power levels.	Performance requirements of the supply modulator (especially power efficiency) are difficult to achieve, and single-chip PA integration is difficult. ET PA designs are also complex, often requiring external signal processing for linearity correction.
Doherty PAs		Doherty PAs ensure elevated PAE over a significant range of envelope power levels.	Doherty PAs are inherently complex and difficult to realize as a single-chip solution suitable for production. Variations of the basic Doherty structure can quickly become resource and space hungry.
Switching PAs		Switching PAs allow power-efficient operation over a large range of the PA's envelope power levels.	Due to multiple switching triggered at discrete power levels, switching PAs suffer from linearity degradation at back-off power levels. The external signal processing required to correct such linearity impairments makes it difficult for single-chip integration in a handheld device.
Dynamic Biasing of PAs	Average power-dependent	Average-power dependent dynamic biasing improves PA performances for constant-envelope signals, and at large back-off power levels only for modulated signals with large PAPR.	It has minimal impact on PA performances at higher instantaneous envelope power levels when the PA is transmitting modulated signals with large PAPR.
	Feed-forward, envelope power-dependent	Feed-forward envelope-power dependent schemes improve PA performances over a significant range of envelope power levels.	They fail to account for various factors that can critically affect the PA's output signal envelope. The need for ancillary circuits, as well as the danger of noise degradation through the feed-forward path, further hinders its realization as a single-chip solution.
Negative feedback PAs		Negative feedback improves PA performances by relying on a baseband error signal to control the gain and phase of a pre-amplifier block, thereby enhancing the overall linearity of the PA system.	Negative feedback circuits are complex, may degrade noise performances and require high-order phase compensation circuits to ensure closed-loop PA stability, resulting in inherent bandwidth limitations.

We now turn our attention to positive envelope feedback, which is the first contribution of the research work presented in this thesis. In chapters 2 and 3, we introduce positive envelope feedback as a novel circuit technique for dynamic biasing of the PA, where the bias signal is a function of the PA's true output envelope power (Sharma, Constantin, & Soliman, 2017; Sharma & Constantin, January 2018; Sharma & Constantin, April 2018). The CMOS PA's gate (or BJT PA's base) bias is varied based on an actual signal flow from the PA's output node to its bias node. **To the best of the author's knowledge, positive envelope feedback has never been reported in any PA architecture, nor in any analog or RF signal processing function.** The proposed approach is simple, requires minimum additional chip area, consumes minimum additional current and does not require any external signal processing. All of the above greatly enhances its feasibility for full on-chip integration as well as facilitates its integration as a functional block into existing state-of-the-art PA architectures to further improve PA performance. The proposed approach does not suffer from excessive delays and the bandwidth limitation, as in the case of negative envelope feedback, and does not require additional circuits for loop stability compensation. It requires a single envelope detector and does not need a high loop gain, which ensures that the PA's output noise performances are not degraded. All these features contribute towards enhancing the feasibility of implementing positive envelope feedback in PAs as a single-chip stand-alone solution.

A second contribution of the research work presented in this thesis is towards the analytical representation of PAs under dynamic biasing and its application for the embedded self-calibration of PAs within the mobile equipment. **To the best of the author's knowledge, this is the first time in the literature that such a concept of embedded self-calibration has been proposed.** The prior art related to this aspect is now presented in Section 1.3.

1.3 Analytical representation of PAs – An overview

Analytical representation of PAs is a well-known and active area of research (J. C. Pedro & Maas, 2005; Draxler, 2013; Mkadem, 2014). Simply put, an analytical representation of a

circuit, as defined in this thesis, refers to a "black-box" representation of the circuit's *behaviour* by deriving the relationship between various signals in the circuit that are of interest. These relationships are derived based purely on measured data, which may either be experimental or based on simulation. Once these relationships are obtained, the analytical representation is said to have been *characterized* or *trained*. The characterized analytical representation can then be used without necessarily knowing the nuances of how the circuit characterized by the "black-box" actually works. Such an analytical representation can be used advantageously for a variety of applications, a few examples of which will be described in this section and with further detail in Chapter 4.

Such analytical representations of electrical circuits are especially useful when it comes to power amplifier (PA) circuits, and this is the primary topic of discussion in this section. The PA in telecommunication systems is an inherently nonlinear device and plays a crucial role in determining the quality of communication, besides affecting other critical performance parameters such as efficiency, noise, etc. While the performance of a PA design can be visualized with the help of various circuit simulation software – some of which are extremely advanced and offer a high degree of sophistication with regard to how the parameters associated with the PA circuit can be modified – there are many applications where the accuracy of circuit simulation software can be traded for with a PA representation that offers adequate accuracy but is significantly more straightforward to characterize and faster to simulate. One such application example is related to the PA design process and was described extensively in Section 0.1.3. In this previously discussed context, analytical PA representations derived from experimentally measured data can help the PA designer correlate initially expected circuit performances obtained via simulation, with actual experimental data from laboratory measurements of the fabricated design. By correlating the two and by relying on the experimentally derived analytical PA representation for subsequent design cycles, the time-to-market for a given PA product can potentially be significantly accelerated. A second application related to embedded self-calibration, to account for part-to-part variation of PA performances in different mobile units, will be discussed comprehensively in Chapter 4.

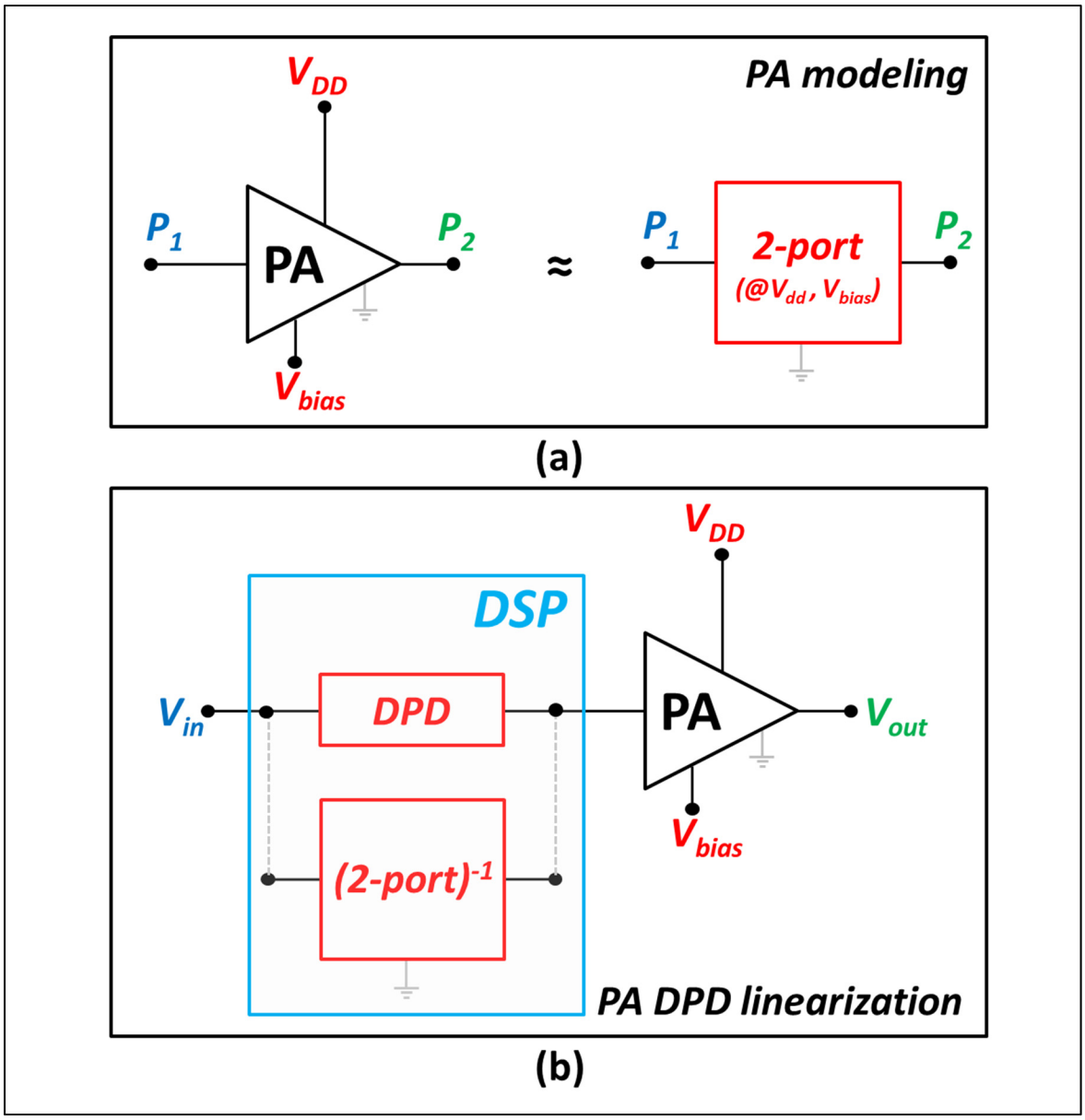

Figure 1.10 (a) Example of a PA design and its equivalent 2-port analytical representation. (b) One possible linearization application using the analytical representation is also shown

Figure 1.10 is an illustration of a 2-port analytical representation of a PA. The PA being characterized is shown on the left within the first box at the top, and P_1 and P_2 refer to the signals/nodes of the PA that are of interest. In this case, P_1 and P_2 refer to the input and the output nodes of the PA, respectively. The PA is being operated with its bias node held at the DC voltage value V_{bias} and its supply node held at the DC voltage value V_{DD}.

The equivalent 2-port analytical representation of this PA is also shown on the right side of the same figure and represents the relationship between the signals at nodes P_1 and P_2 of the PA on the left. This 2-port analytical representation is characterized under the specific conditions of the bias and the supply voltage that is shown on the left. Commonly, this relationship is derived with the help of a mathematical fitting tool for measured data of the PA circuit on the left, the measurements being based on exciting the PA with a set of known signal values at node P_1 and measuring the corresponding signal values at node P_2. Once characterized, the analytical 2-port representation describes how changes in the value of the PA's signal at node P_1 affects the value of the signal at node P_2, without knowing the intricacies of the actual PA's circuit operation. Depending on the specific type of model that is used for the analytical representation, the reverse relationship - i.e. how changes in the value of the PA's signal at node P_2 affects the value of the signal at node P_1 - may also be known using the same 2-port representation.

However, the relationship between P_1 and P_2, using the 2-port analytical representation, is *accurate* only when the PA's bias node is held at the DC voltage value V_{bias} and its supply node is held at the DC voltage value $V_{DD,}$ i.e. under the same circuit conditions that was used when the measurement data for characterization was collected. For accurately predicting PA behaviour when the PA is operated under a bias voltage or supply voltage (or both) different from the values used during characterization, a new set of analytical relationships have to be derived based on new measurement data collected with the PA's bias/supply node held at the changed value. In Chapter 4, we will introduce a new multi-port analytical representation that circumvents this requirement to re-characterize the PA representation for every change of the PA's operating conditions.

In Figure 1.10, we also show one possible application of the 2-port analytical representation when used for PA linearization through digital pre-distortion, or DPD (Keysight; Mkadem, 2014). The 2-port PA representation is used to synthesize the PA's *pre-distorted* input excitation signal. This pre-distorted input signal represents the *inverse* nonlinearity (symbolically represented by $(\text{2-port})^{-1}$ in the figure) of the PA's behaviour captured by the

2-port analytical representation. When such a pre-distorted signal is applied as input to the PA and subjected to the PA's inherent nonlinearity, it results in an output signal V_{out} that is linear and (ideally) distortion-free.

Many different approaches for representing PAs analytically are described in the literature (J. C. Pedro & Maas, 2005; Fager et al., 2019). As mentioned previously, such analytical representations are based on empirical observations and do not require knowledge of the PA's internal circuit composition (J. C. Pedro & Maas, 2005). Such analytical representations are in contrast to physical models, such as those used in circuit simulators, which rely on representing the PA's nonlinear behaviour using an equivalent circuit description of the nonlinear PA (admittedly, some of these equivalent circuit components are themselves purely analytical and based on detailed empirical measurements).

Without delving into details, we now mention a few different approaches for PA analytical modelling. From one perspective of classification, PA analytical representations may be viewed as those that use equivalent band-pass PA models and those that use equivalent low-pass PA models (J. C. Pedro & Maas, 2005). The former processes the complete RF signal at the carrier frequency, while the latter uses an equivalent low-pass model that handles only the envelope information. For low-pass PA models, the RF signal is considered as an equivalent *bias signal*. It is useful to note that our proposed 3-port analytical PA representation described in Chapter 4 offers more versatility in its use in that it is a hybrid of the aforementioned approaches and hence allows incorporating both band-pass and low-pass structures into the same representation.

All analytical PA representations may be further classified as those that are memoryless and those that capture memory effects (which are induced by energy-storing components in the circuits – inductors and capacitors). The PA's output signal envelope in memoryless representations reacts instantaneously to its input signal envelope (Fisher & Al-Sarawi, 2016). On the other hand, the PA's output signal envelope in representations that include memory reacts not only as a function of the instantaneous value of the signal envelope but

also its previous values (Draxler, 2013). The PA's output for representations that include memory is, therefore, a function of the amplitude as well as the frequency of the envelope signal, and such representations are commonly characterized using the PA's AM-AM and AM-PM response (Clark, Silva, Moulthrop, & Muha, 2002). Representations that include memory may either be linear or nonlinear (Draxler, 2013).

Common analytical representations of PAs rely on a 2-port approximation, such as that in Figure 1.10, where the PA's input-to-output relationship may be approximated by a variety of different approaches (J. C. Pedro & Maas, 2005). These approximations may be characterized using data measured under static conditions (i.e. constant DC bias and constant DC supply, e.g. (Hammi, Carichner, Vassilakis, & Ghannouchi, 2008)) or data measured under dynamic conditions (i.e. dynamic bias or dynamic supply, e.g. (Gibiino, Avolio, Schreurs, Santarelli, & Filicori, 2016)). A common approach for approximating the PA's input-to-output relationship is by using 2-D or 3-D look-up tables (Gilabert, Cesari, Montoro, Bertran, & Dilhac, 2008; Shen, Gajadharsing, & Tauritz, 2007). 2-D look-up tables relate the PA's input-to-output relationship for different values of the input (e.g. P_{out} vs P_{in}), while 3-D look-up tables relate the PA's input-to-output relationship as a function of an additional variable (e.g. P_{out} vs P_{in} as a function of the supply voltage). Higher-order look-up tables are also possible, but their implementation can quickly grow in complexity. Polynomial approximations are also popular (e.g. (Barradas, Cunha, Lavrador, & Pedro, 2014)), and the 3-port representation described in Chapter 4 is also based on a system of equations derived from distinct sets of complex nonlinear polynomials, but with the help of a never-before proposed signal flow. In Section 1.3.1, we describe in greater detail the frequently cited Volterra series that is used for analytical PA representations, and in particular, a recently proposed 3-port modified variant of this Volterra series (Gibiino, Avolio, Schreurs, Santarelli, & Filicori, 2016).

The accuracy of the analytical representation is critically determined by the adopted model structure and the characterization procedure, but a high accuracy can also adversely affect the simplicity of the necessary training sequence. A lot of research focus so far has been put into

determining the best possible model for a particular application. Expectedly, there is no one single approach that perfectly answers the requirements of every possible application. This facet is also commonly discernible by going through publications in this field of study, where papers are less commonly observed to compare themselves with previous work but instead focus on how their described approach allows meeting the needs of any relevant PA implementation (J. C. Pedro & Maas, 2005). Therefore, depending on the end-use use that is aimed at, careful considerations must be made while selecting the appropriate approach for analytically representing PA behaviour. To highlight one interesting example of such a context, attention may be drawn to the proposed transmitter architectures in the base-station for future 5G systems (Fager et al., 2019). Hundreds of branches, each with their own PA line-up, are envisaged for such transmitters – and it is impossible to perform circuit-level simulations for such large systems. Instead, a more feasible solution is to analyze the system at the system-level, with the PA blocks (as well as other constituent circuits) approximated by their equivalent analytical representations. The simplicity of the analytical PA representation that is used, in addition to its accuracy, is decisive for such an application.

We now focus on PA analytical models based on the well-known Volterra series, which deserve attention given its potential as a mathematically exact representation of weak nonlinearities. In Section 1.3.1, we lay particular emphasis on the recently proposed 3-port behavioural model (Gibiino, Avolio, Schreurs, Santarelli, & Filicori, 2016) based on modified Volterra formulations. The difficulties associated with this modified Volterra formulations approach (and by extension, with any Volterra-based approach) for application to embedded self-calibration of PAs under dynamic biasing within the mobile unit (a concept introduced in Chapter 4 of this thesis) are also described.

1.3.1 Volterra-based analytical representation of PAs

Among the nonlinear analytical PA representations found in the literature (Yang, Yi, Nam, & Kim, 2000; Gibiino, Avolio, Schreurs, Santarelli, & Filicori, 2016; J. C. Pedro & Maas, 2005; Tehrani et al., 2010), frequent references are drawn to the Volterra series given by the

multi-dimensional time-domain convolution in (1.1) below, as given in (Gibiino, Avolio, Schreurs, Santarelli, & Filicori, 2016). The full Volterra series, as in (1.1), is well known for its ability to model memory effects arising from weakly nonlinear mechanisms in PAs and represents an exact mathematical model in theory.

$$y(t) = \sum_{n=1}^{\infty} \int_{-\infty}^{+\infty} \dots \int_{-\infty}^{+\infty} h(\tau_1, \dots, \tau_n)\{x(t-\tau_1) \dots x(t-\tau_n)\}\, d\tau_1 \dots d\tau_n \tag{1.1}$$

$h(\tau_1, \dots, \tau_n)$ in (1.1) are known as the kernels of the Volterra series, and range from the first-order Volterra kernel $h(\tau_1)$ to the nth-order Volterra kernel $h(\tau_1, \dots, \tau_n)$. However, higher-order Volterra kernels $h(\tau_1, \dots, \tau_n)$ in (1.1), which are required to perfectly capture the PA's memory effects, present significant difficulties to extract due to the inherent complexity of the Volterra series (J. C. Pedro & Maas, 2005). Due to such problems in the extraction procedure, works based on using Volterra series for representing PAs often limit themselves to first-order Volterra kernels only, under the assumption that higher-order Volterra kernels can be ignored without sacrificing the necessary level of accuracy. For example, the first-order approximation of (1.1) is used for the *modified* Volterra series applied to a multi-tone excitation in (Gibiino, Avolio, Schreurs, Santarelli, & Filicori, 2016), as shown in (1.2).

$$y(t) = F[x(t)] + \int_{-\infty}^{+\infty} g_1(x(t), \tau_1)\{x(t-\tau_1) - x(t)\}\, d\tau_1 \tag{1.2}$$

where $F[x(t)]$ represents the PA's quasi-static nonlinearity only and $g_1(x(t), \tau_1)$ is a first-order Volterra kernel. Further details of this PA representation are discussed in Section 4.6 of this thesis.

In the context of many applications (such as that of embedded self-calibration within a mobile unit, introduced and described in detail in Chapter 4), the advantages of PA representations using first-order Volterra series over other equations-based representations is debatable. Such advantages are an especially relevant argument since, within the framework

of such applications, the need for simplicity in the calibration steps and the computation algorithms largely outweighs the requirement for mathematically exact formulations. The extraction of even first-order Volterra coefficients have been shown to present challenges (Gibiino, Santarelli, Schreurs, & Filicori, 2017), and the extraction of higher-order Volterra kernels can quickly become laboriously complex. For example, the use of higher-order Volterra-based PA representations for the analytical representation of PAs necessitates employing complex training sequences to calculate the kernels, starting from the low-order through to higher-order Volterra kernel extractions (Maas, 2003). The overhead in terms of complexity (and consequently, in terms of computational resources) can quickly become impracticable in the context of many applications such as that of embedded self-calibration, which requires re-tuning the analytical representation from one mobile unit to another during the operation of the mobile equipment in the field. Another key consideration is that the applicability of Volterra-based approach for closed-form analytical representation of closed-loop systems such as (Sharma, Constantin, & Soliman, 2017; Kang, Baek, & Hong, 2017; Thangarasu, Ma, & Yeo, 2017; El-Shennawy, Joram, & Ellinger, 2016), which rely on RF or envelope feedback signals (or both), has not been demonstrated.

1.4 Summary of deficiencies of existing approaches for analytical representation of PAs

Table 1.2 is a summary of some key features, or lack thereof, of various analytical representations of PAs found in the literature. As may be observed, there is no one single analytical representation that answers the requirements for all possible applications. The *Remarks* column in Table 1.2 highlights the deficiencies associated with the features mentioned in the first column of the same table, with a particular emphasis on the requirements necessary for an analytical representation that is suitable to be used for embedded self-calibration of PAs as described in Chapter 4 of this thesis.

Table 1.2 Summary of features and deficiencies of existing approaches for analytical representation of PAs

Feature/Deficiency	Remarks
Memoryless representations	Memoryless analytical representations fail to capture the critical effect on the PA's output due to previous values of the transmitted signal's envelope. The PA's output signal envelope in memoryless representations reacts instantaneously to its input signal envelope only. Memory effects are induced by energy-storing components in the circuits and are a function of the amplitude as well as the frequency of the envelope signal.
2-port representations	2-port analytical representations do not directly and distinctly account for contributions of the PA's bias/supply to the PA's output. For example, they do not capture the effect on the PA's output nonlinearity from varying the value of the bias that is applied. Their accuracy is also limited when they are used under circuit conditions (bias, supply, etc.) different from that under which the representations were characterized.
Representations characterized under static bias only	When characterized under static-bias conditions only, analytical PA representations fail to predict PA performance accurately under dynamic circuit conditions. Such dynamic circuit conditions are common in many PA architectures, e.g. dynamic supply voltage is used in ET PAs to improve its PAE. Hence, PAs characterized under static conditions only are severely limited in their scope of applicability.
PAs with complex characterization	Complex training sequences required for characterizing some representations, such as that for Volterra-based approaches, makes such representations unsuitable to be used for many applications (e.g. embedded self-calibration of PAs as described in Chapter 4). The simplicity of the training sequence, computational algorithms, storage requirements and the necessary probing circuitry can critically determine the feasibility of using an analytical representation for a given application.

Here again, to the best of the author's knowledge, a 3-port nonlinear PA representation that provides a viable alternative to the Volterra approach in the context of self-calibration of envelope-dependent dynamic biasing of a PA within a mobile unit during operation, while offering comparable accuracy and with the added advantage of allowing a closed-form analytical representation of the 3-port embedded PA system, has not been demonstrated. The nonlinear PA representation introduced in this thesis addresses these needs by demonstrating:

- a 3-port analytical PA representation based on two distinct sets of nonlinear complex polynomials that describe a combiner, a nonlinear baseband-to-RF converter and a nonlinear RF amplifying function. It accurately captures the effects of dynamic biasing (including memory effects) under multi-tone excitation and allows predicting linearity improvement in terms of IMD_3, as well as *ACP* reduction with a modulated signal.

- the simplification of the computational requirements for PA characterization under envelope-based dynamic biasing, in particular for high-order nonlinearity and with comparable accuracy to earlier proposed Volterra-based approaches.

- the simplification of the training sequence within the mobile unit for embedded self-calibration of the dynamic biasing mechanism.

- a method for embedded optimization of dynamic biasing performances from one mobile unit to another during operation.

- a closed-form analytical representation of open-loop and closed-loop envelope-based dynamic biasing, enabling the determination of closed-loop feedback parameters to ensure stability and optimal linearity.

The proposed 3-port PA representation is mathematically derived with the use of a multi-tone input excitation and a multi-tone dynamic biasing signal, with arbitrary amplitude and phase

for each tone, which allows taking into consideration high degree nonlinearities. It is well known that multi-tone representations may be strongly correlated to spectral regrowth under modulated excitations (Carvalho & Pedro, Dec. 1999; Hyunchul & Kenney, 2001; Park et al., 2016). This correlation is also shown later in Section 4.4.3. Additionally, though the proposed 3-port representation is demonstrated for the PA's dynamic gate biasing here (under open-loop and closed-loop conditions), it can be used to represent other PA nonlinear dynamic mechanisms (such as supply modulation (Gibiino, Avolio, Schreurs, Santarelli, & Filicori, 2016)). Details of this 3-port analytical PA representation are discussed in Chapter 4.

It is useful to mention that the formulations in Chapter 4 of this thesis are distinctly different from the formulations in (Sharma & Constantin, 2013) also proposed by the same authors. The formulations in (Sharma & Constantin, 2013) are based on a simple variable gain control, using only a *linear* processing of a multi-tone biasing signal and are applicable only for limited peak-to-average envelope power (~2.5dB). They are also intended only for *estimating* IMD levels in feedback amplifiers during the PA's engineering development phase. Hence, they do not suit embedded self-calibration during the operation of the mobile equipment. The 3-port PA representation proposed here is fundamentally different since it is based on the use of a combiner, a nonlinear baseband-to-RF converter and a nonlinear amplifying function, for the *nonlinear* processing of the dynamic-bias signal. This fundamentally different structure allows *accurate* prediction of PA performances under larger peak-to-average excitation, with a distinct representation of the nonlinear transfer function from the baseband dynamic-bias signal to the RF output signal, as required for embedded self-calibration.

CHAPTER 2

INTRODUCING POSITIVE ENVELOPE FEEDBACK: THEORY

> "Science is founded on uncertainty. Each time we learn something new and surprising, the astonishment comes with the realization that we were wrong before. The body of science is not, as it is sometimes thought, a huge coherent mass of facts, neatly arranged in sequence, each one attached to the next by a logical string. In truth, whenever we discover a new fact it involves the elimination of old ones."
>
> Lewis Thomas

In this chapter, the theory underlying the design of positive envelope feedback in RFIC PAs is described. In Section 2.1, the fundamentals of positive envelope feedback and the resulting PA performance improvement is explained from the perspective of the *dynamic* operating point. The design conditions that must be respected to ensure successful implementation of positive envelope feedback are discussed in Section 2.2. While highlighting the inherent simplicity of this technique, the salient attributes that make positive envelope feedback an excellent candidate for on-chip RFIC PA integration - low additional current consumption, low additional chip area and no external signal processing requirements - are identified.

2.1 Positive envelope feedback and the dynamic operating point

Figure 2.1 shows the general schematic of a multi-stage RFIC PA transmitting a modulated RF signal. As shown, the PA typically comprises a driver-stage followed by a power-stage, though more than one driver-stage may also be used. V_{GG}=V_{GG0} defines the quiescent (DC) gate/base-bias voltage of the power-stage transistor array. The RF_{in} and the RF_{out} ports are typically terminated with 50Ω impedances. For conciseness, other circuit details (such as matching networks, etc.) are not explicitly shown in Figure 2.1. The DC supply voltage of the driver-stage $V_{DD}(DS)$ and the DC supply voltage of the power-stage V_{DD} are shown as separate signal lines in Figure 2.1; however, they may also be implemented as a single supply signal V_{DD} in any given PA implementation.

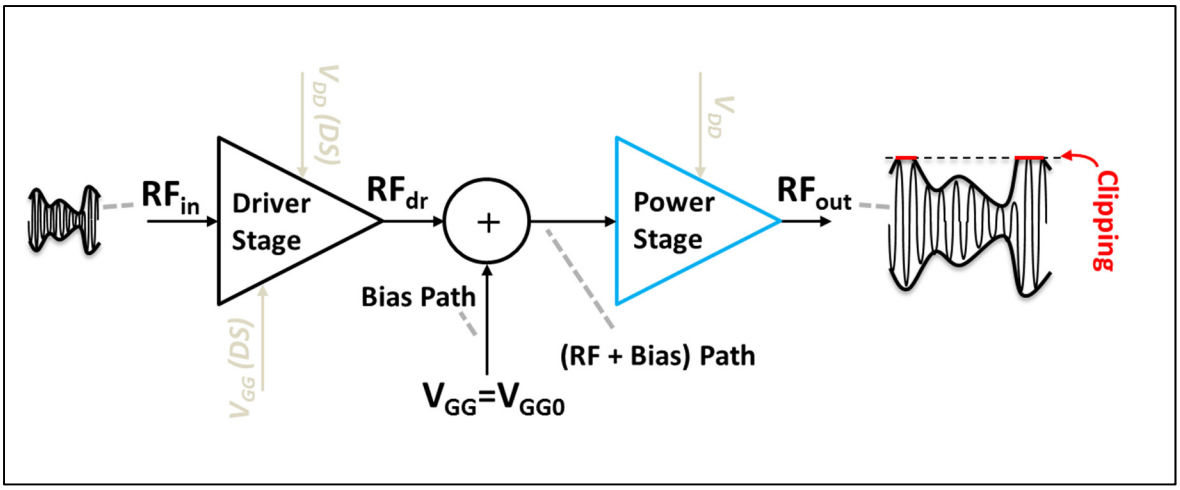

Figure 2.1 Schematic of state-of-the-art multi-stage RFIC PA transmitting an envelope modulated signal. V_{GG}=V_{GG0} refers to the quiescent (DC) gate bias applied to the power-stage transistor array. The PA's output voltage is clipped for high values of the signal envelope

For convenience, we will refer to the design in Figure 2.1 as a CMOS PA for the discussion that follows. However, the same discussion is also applicable to PAs using BJT devices after appropriately substituting references to the gate terminal of the CMOS device with the base terminal for the BJT device, etc.

The power-stage is commonly implemented as the well-known cascode structure, and V_{GG} refers to the gate-bias voltage for the common-source (CS) transistor in the cascode structure. The gate bias for the common-gate (CG) transistor is chosen to ensure optimized supply voltage division across the CS transistor and CG transistor components of the cascode structure. For simplicity of our analysis here and without any loss of generality, we can replace the CG transistor with a resistance R_x as shown in Figure 2.2 and focus on the voltage-current dynamics of the CS transistor, with the understanding that similar analyses apply to the CG transistor.

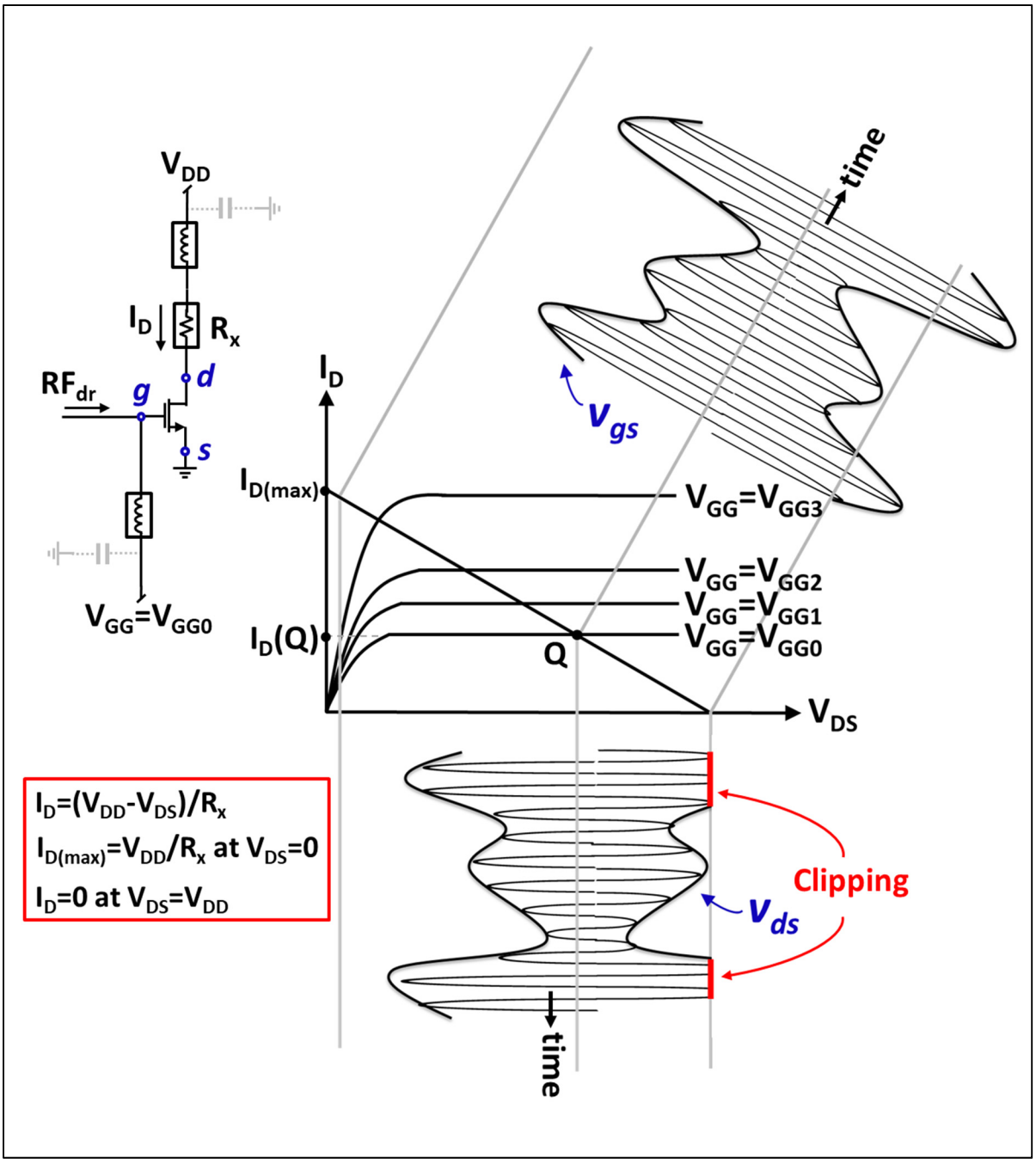

Figure 2.2 I_D vs. V_{DS} profile and the clipped v_{ds} waveform when the PA is excited with the envelope-modulated RF signal v_{gs}. The quiescent (DC) value of the transistor gate voltage is held at V_{GG0}. Q is the PA's quiescent operating point. v_{gs} and v_{ds} are drawn using two different voltage scales

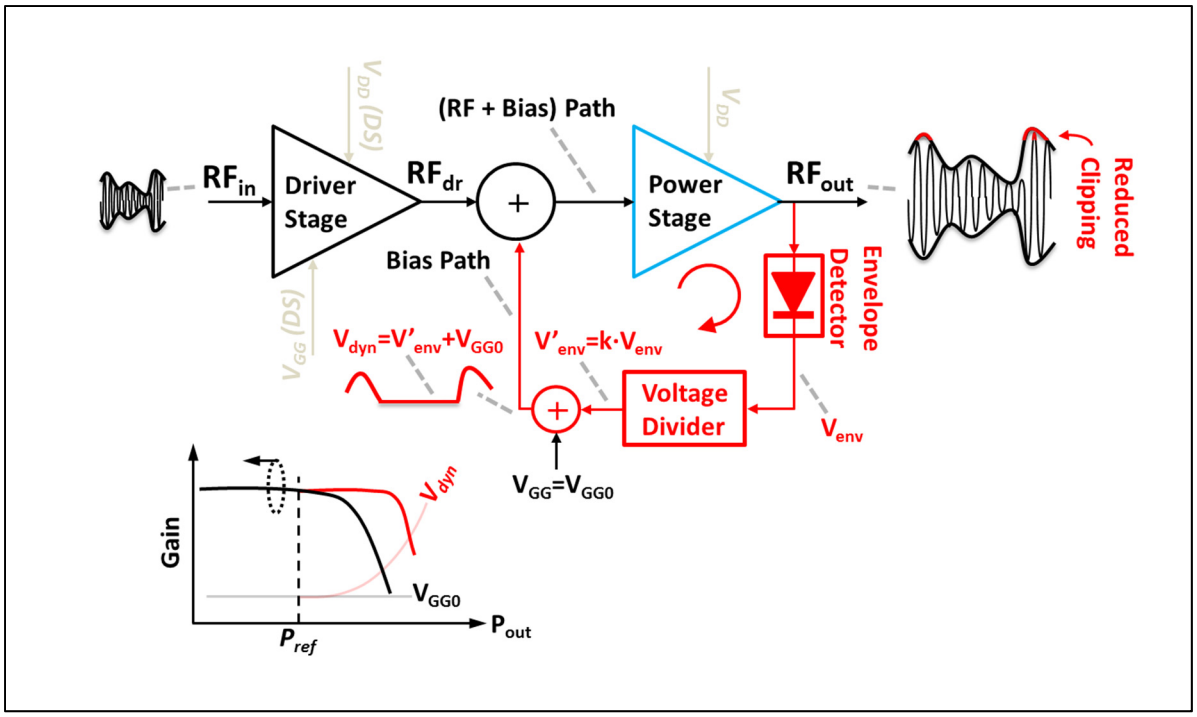

Figure 2.3 Schematic of proposed RFIC PA with positive envelope feedback. V_{dyn} is the dynamic-bias signal applied to the gate of the PA's power-stage transistors. The improvement of the PA's *Gain* vs. P_{out} profile under dynamic bias is also shown, along with the V_{dyn} vs. P_{out} profile necessary to achieve it

Figure 2.2, therefore, shows the profile of the drain current I_D vs. drain-source voltage V_{DS} of the CS transistor in the PA power-stage for various levels of DC gate-bias voltage V_{GG}. For a given PA load and with V_{GG} held at V_{GG0} for class-AB PA operation, the load-line is also shown. The PA's quiescent current consumption for this class-AB operation is given by $I_D(Q)$. As shown in Figure 2.2, the load-line is now used to trace the transient form of the output v_{ds} voltage signal when the input is excited with the v_{gs} voltage signal. Here, v_{gs} refers to the envelope-modulated input RF excitation across the gate-source terminals of the power-stage transistors, while v_{ds} refers to the output RF signal across the drain-source terminals of the CS transistor. While smaller values of the input envelope are transmitted without amplitude distortion, drain-current clipping as the input envelope gets larger is a major contributor to PA output nonlinearity at high PA power levels (Onizuka, Ikeuchi, Saigusa, & Otaka, 2012; Chengzhou, Vaidyanathan, & Larson, 2004; Po-Chih et al., 2008; Koo, Joo, Na,

& Hong, 2012; Kang, Baek, & Hong, 2017; Kang, Sung, & Hong, 2018). Such a clipped PA output voltage waveform is also illustrated in Figure 2.1 and Figure 2.2.

For reducing PA distortion due to clipping at higher envelope values without incurring an increase in the PA's quiescent current consumption $I_{D(Q)}$, the proposed positive envelope feedback architecture shown in Figure 2.3 is used. Its operation is described next. Compared to the PA schematic shown in Figure 2.1, the proposed technique introduces a positive feedback signal path (shown in red in Figure 2.3) from the PA output to its power-stage bias input. The new output envelope-dependent power-stage dynamic gate bias V_{dyn} is given by (2.1).

$$V_{dyn} = k \cdot V_{env} + V_{GG0} = V'_{env} + V_{GG0} \tag{2.1}$$

Here, V_{env} is the output voltage of the envelope detector and $V'_{env} = k \cdot V_{env}$ is the voltage at the output of the voltage divider that follows the envelope detector. The value of the constant k is determined by the voltage division ratio in the voltage divider. V_{GG0} is the quiescent DC bias applied to the PA's power-stage gate and is identical to the value utilized for the constant-bias case illustrated in Figure 2.1 and Figure 2.2.

For output power levels below a threshold value P_{ref}, the envelope detector in Figure 2.3 is designed to be OFF and $V'_{env}=k \cdot V_{env}$ is zero. Hence, V_{dyn} is held at the quiescent DC value V_{GG0} and the PA operation is identical to when it is biased using the constant biasing scheme in Figure 2.1 and Figure 2.2. However, for output power levels higher than P_{ref}, the envelope detector is ON, and as a result of the positive envelope feedback loop, V_{dyn} varies as a dynamic function of the PA's output envelope power. An increase (or decrease) in the PA's output envelope value leads to a corresponding increase (or decrease) of the power-stage gate bias V_{dyn}. We can therefore modify (2.1) to define V_{dyn} as given by (2.2).

$$\begin{aligned} V_{dyn} &= V_{GG0} && if\ RF_{out} < P_{ref} \\ V_{dyn} &= k \cdot V_{env} + V_{GG0} && if\ RF_{out} \geq P_{ref} \end{aligned} \tag{2.2}$$

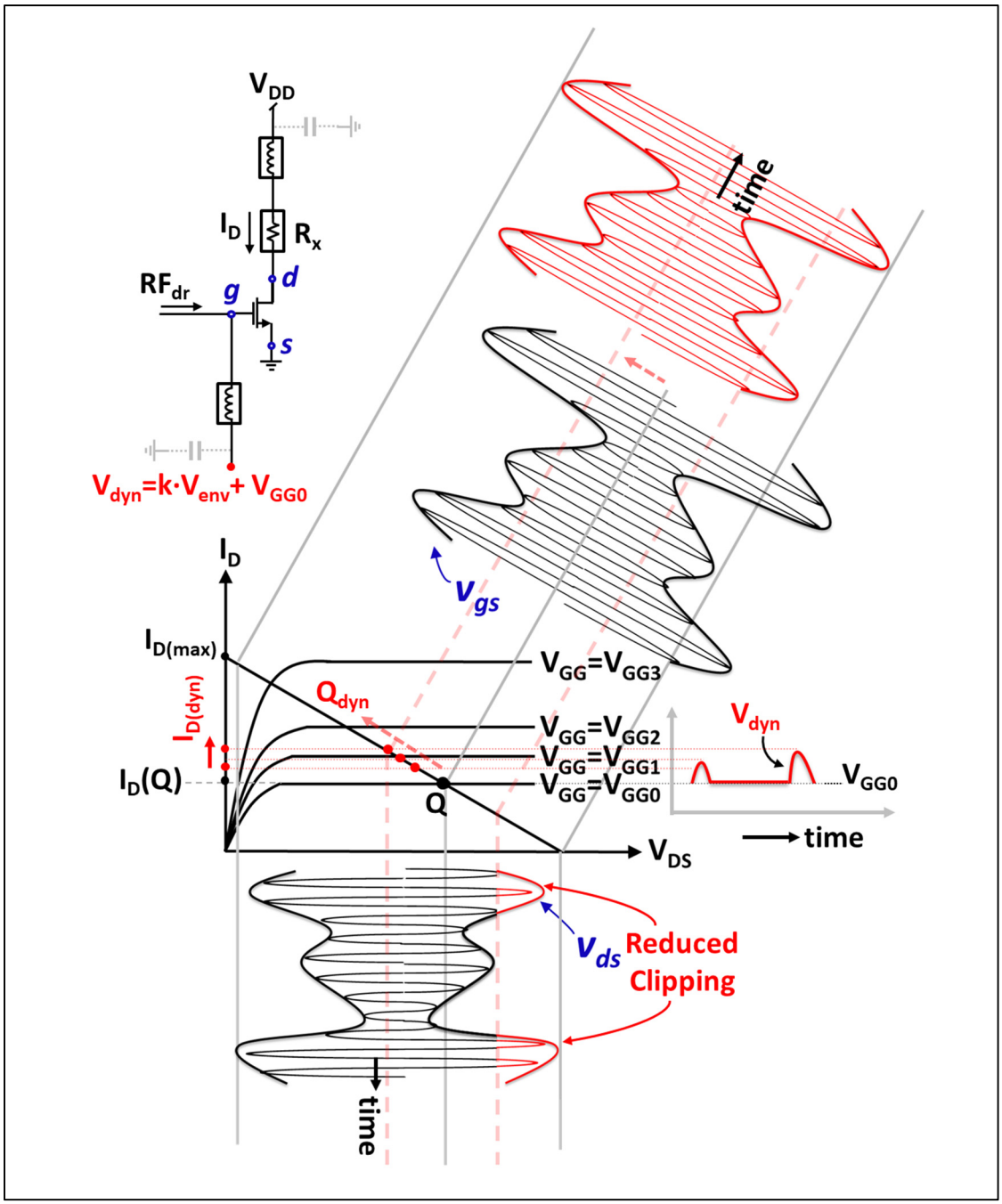

Figure 2.4 I_D vs. V_{DS} profile and the v_{ds} waveform for the proposed positive envelope feedback architecture of Figure 2.3, when the gate is excited with the envelope-modulated RF signal v_{gs}. Q is the PA's quiescent operating point (identical to the value in Figure 2.2), while Q_{dyn} is the PA's instantaneous operating point at high output envelope power levels. Note the reduced clipping of the v_{ds} signal compared to that in Figure 2.2. The v_{ds} waveform shown is drawn using Q_{dyn} due to the gate voltage value V_{dyn} corresponding to the maximum envelope level of v_{gs} (in red)

Figure 2.4 illustrates the corresponding I_D vs. drain-source voltage V_{DS} profile of the PA with positive envelope feedback. The associated v_{ds} transient voltage signal for the same RF input excitation v_{gs} used in Figure 2.2 is also shown. For low output envelope levels, the output v_{ds} waveform is obtained using the load-line determined by the quiescent bias V_{GGO} and the PA load, i.e. the same load-line as in Figure 2.2. However, for higher output envelope levels, an increase in the gate-bias voltage due to positive feedback translates into a movement of the PA's instantaneous operating point Q_{dyn} along the load-line, as shown in Figure 2.4. We refer to this as the PA's *dynamic operating point*. Such an instantaneously determined operating point for high output envelope levels allows the upper ranges of the PA's output signal v_{ds} to be transmitted without being clipped, leading to an improvement in the PA's linearity due to reduced amplitude distortion. P_{ref} in (2.2) is therefore selected to be equal to around the first PA output power level when drain-current clipping starts, and this is when the resulting distortion becomes a significant contributor to the PA's nonlinearity. By dynamically changing the PA's instantaneous operating point for $RF_{out} \geq P_{ref}$ through positive envelope feedback, the output-signal clipping is reduced, leading to an improvement of the PA's linearity.

An alternative way of analyzing the improvement of PA linearity due to positive envelope feedback is by looking at its *Gain* vs. P_{out} profile. As shown in Figure 2.3, P_{ref} is equivalently the first output power level when the PA's gain starts compressing (due to output-signal clipping) under constant bias. By using positive envelope feedback, the decrease in the value of the PA's gain at output power levels $RF_{out} \geq P_{ref}$ under constant bias is compensated for by an increase in the transistor's gate bias V_{dyn} under the action of positive envelope feedback, leading to an overall improvement in the PA's *Gain* vs. P_{out} profile and consequently its linearity.

As shown in Figure 2.4, such an increase in the gate-bias voltage for higher output envelope powers leads to an increase in the PA's drain current $I_{D(dyn)}$ at these power levels; however, the PA's quiescent current consumption $I_{D(Q)}$ and the current consumption at large back-off power levels remain identical to that for the constant-bias case in Figure 2.2. It is also

worthwhile to note that the voltage divider in Figure 2.3 is implemented with passive components (resistors), and the only additional current consumption in the schematic shown in Figure 2.3 compared to that in Figure 2.1 is due to the envelope detector. This quiescent current consumption of the envelope detector can be designed to be negligible compared to the total quiescent current consumption of the PA system, and ensures that the overall quiescent power consumption of the PA system in Figure 2.4 is negligibly affected due to implementation of the proposed positive envelope feedback technique.

Having introduced positive envelope feedback from the perspective of the basic load-line theory underlying it, we now turn our attention in Section 2.2 to the various circuit design conditions that must be respected to implement it successfully in RFIC PA designs.

2.2 Design conditions for implementing positive envelope feedback

As noted earlier, a number of design conditions have to be respected to ensure the successful implementation of positive envelope feedback in RFIC PAs. Meeting these requirements ensures that PA performances with respect to salient attributes such as stability, noise, distortion, etc. are not adversely affected due to positive envelope feedback. These prerequisites are highlighted in the following paragraphs, as well as described regarding how the proposed technique of positive envelope feedback allows meeting them comfortably.

2.2.1 Design condition regarding loop gain

A critical parameter to consider with any feedback system is loop stability, and the fear of PA instability is understandably a particular point of concern when considering the implementation of positive feedback in a PA system. Stability in linear analog circuits is commonly evaluated under small-signal conditions based on the well-known Barkhausen gain margin and phase margin stability criteria. While negative envelope feedback loops in PAs typically depend on a high loop gain to be effective (while maintaining safe values of phase margin), positive envelope feedback loops must satisfy a low loop gain condition to prevent PA instability. Such a requirement is because positive envelope feedback necessarily

introduces a ~360^0 phase shift across the PA's envelope information bandwidth, hence leaving no possibility of phase margin design.

For understanding this low loop gain requirement, a simplified small-signal representation is used next. An envelope feedback signal flow similar to (Constantin, Kwok, Shao, Cismaru, & Zampardi, 2012, Figure 4) is used but simplified to a single loop that represents only the signal flow within the envelope feedback path, through the envelope detector and the voltage divider. This simplification is sufficient for a small-signal stability analysis that does not require the modelling of distinct gain blocks representing the error signal processing and the gain control, as was required in (Constantin, Kwok, Shao, Cismaru, & Zampardi, 2012). Accordingly, the resulting simplified envelope signal flow representing a PA system with positive envelope feedback is shown in Figure 2.5. Moreover, as will be shown, the design of a positive envelope feedback system inherently includes a very low loop gain that translates into a significantly high gain margin that ensures operation far from any unstable condition. Hence, the Barkhausen gain and phase margin stability criteria may be applied to the envelope feedback path shown in Figure 2.5 as an approximate but sufficient stability analysis, only as a means of verifying stability with a comfortably high gain margin. Here, assuming a constant average power in the amplitude-modulated RF signal applied at the input of the PA, V_{in} represents the small-signal envelope of the input RF signal and A represents the linear conversion gain from the analog bias signal at the gate (or base) of the PA's power-stage to the envelope amplitude at its output. β represents the RF-to-Analog linear conversion gain of the feedback path through the envelope detector and the voltage divider, hence the ratio between the analog V_{dyn} signal and the output envelope signal. Based on the above small-signal approximation, the envelope transfer function of this closed-loop PA system is given by (2.3).

$$\frac{V_{out}}{V_{in}} = \frac{A}{1 - A \cdot \beta} \tag{2.3}$$

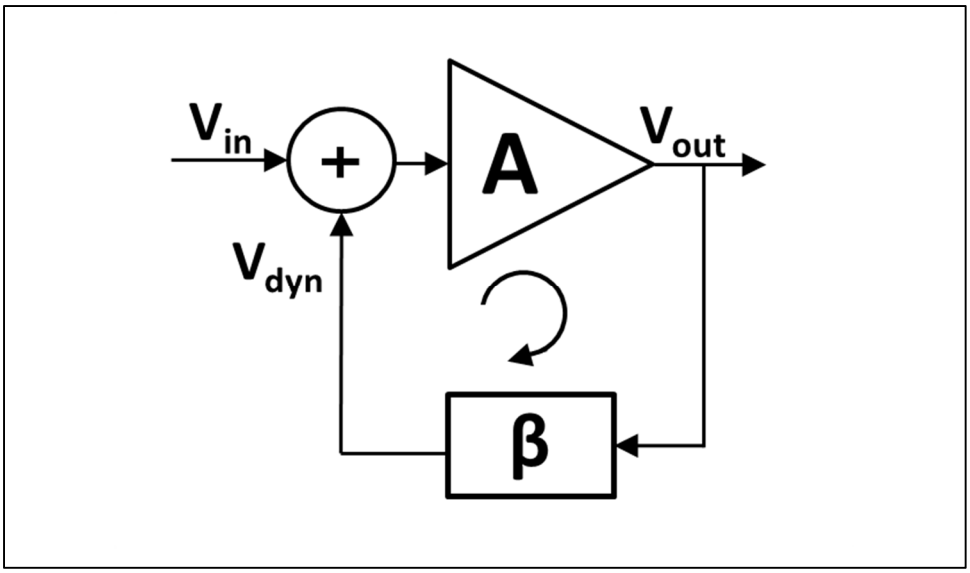

Figure 2.5 Block diagram of PA System with positive feedback loop showing envelope signal flow

From (2.3), it can be seen that the PA system in Figure 2.5 becomes unstable if $(1 - A \cdot \beta) \rightarrow 0$, i.e. if $|A \cdot \beta| \rightarrow 1$ and $\angle(A \cdot \beta) \rightarrow 360°$. As mentioned earlier, for a positive feedback system, the phase $\angle(A \cdot \beta)$ is ~360^0. Therefore, to maintain stability, it has to be ensured that the magnitude of the open-loop gain $|A \cdot \beta| < 1$, i.e. the open-loop envelope transfer function must be attenuative. In the case where the open-loop envelope transfer function is very small i.e. $|A \cdot \beta| \ll 1$, the closed-loop PA system's envelope transfer function given by (2.3) reduces to (2.4) below.

$$\frac{V_{out}}{V_{in}} = \frac{A}{1 - A \cdot \beta} \rightarrow \frac{A}{1 - 0} \approx A \tag{2.4}$$

The envelope transfer function of the closed-loop PA system in Figure 2.5 under positive feedback operation, therefore, approaches the gain A of the PA's power-stage as the open-loop gain $|A \cdot \beta|$ becomes smaller.

The low loop gain condition to ensure closed-loop PA stability under positive envelope feedback must be evaluated and verified for all envelope frequencies of the PA's transmitted

signal, and at different power levels ranging from small-signal operation to moderate gain compression. However, for frequencies that lie outside its maximum designed envelope bandwidth (i.e. outside the range of frequencies where PA gain A is intended) the PA design itself ensures that $|A| \ll 1 \Rightarrow |A \cdot \beta| \ll 1$, and closed-loop stability is therefore easily maintained. Additionally, the high values of gain compression when the PA is operating at significantly higher power levels ensure that $|A|$ (and consequently $|A \cdot \beta|$) becomes progressively smaller with increasing values of such higher output power. Hence, it is sufficient to evaluate the closed-loop PA's stability under positive envelope feedback at power levels ranging from small-signal operation to moderate gain compression only.

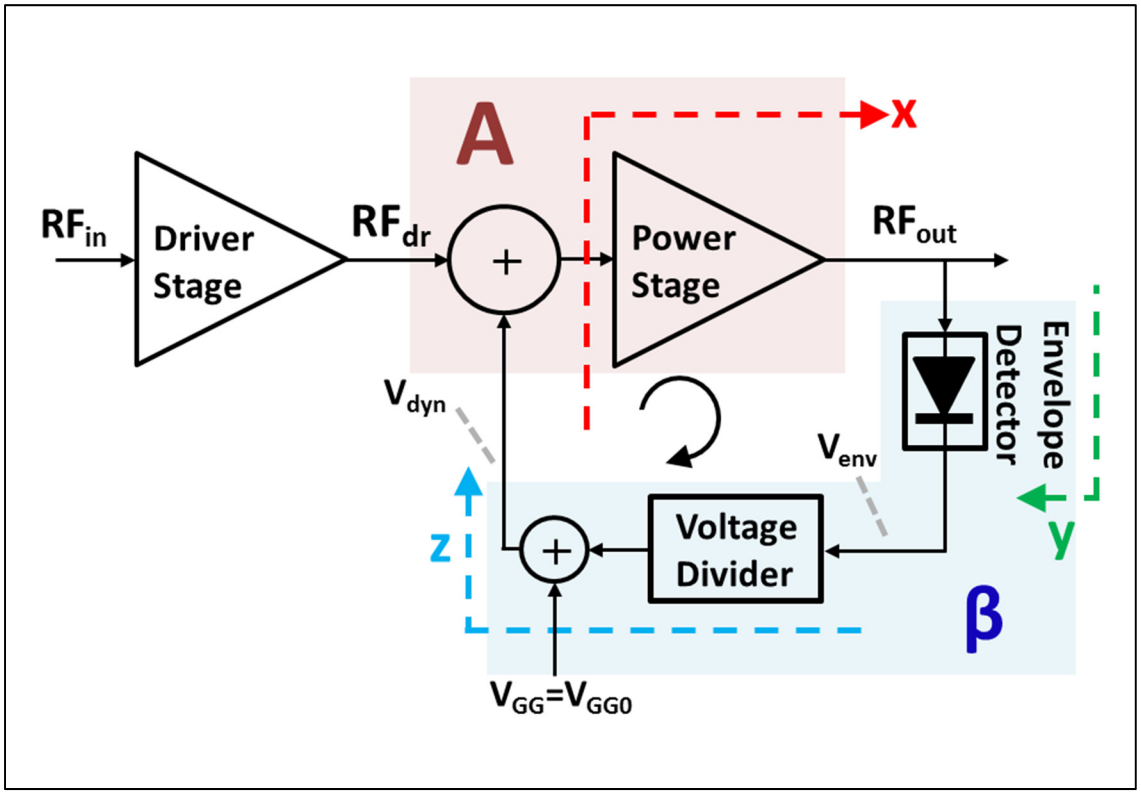

Figure 2.6 Illustration to trace the loop gain of the proposed positive envelope feedback PA architecture. x, y and z refer to the PA's power-stage conversion gain (voltage to voltage) from bias input to RF output, the RF-to-analog conversion gain (voltage to voltage) of the envelope detector and the voltage attenuation through the voltage divider respectively

We now further examine this stability condition for the specific case of the power amplifier structure using positive envelope feedback that was shown in Figure 2.3. When the envelope detector is OFF at low PA output power levels, the feedback loop is open, and there is no possibility of instability arising from positive envelope feedback. However, at higher power levels, when positive envelope feedback becomes operational, it needs to be verified if the condition of stability is respected. As illustrated in Figure 2.6, the loop gain is composed of the conversion gain *x* of the PA's power-stage from the analog bias signal to the envelope of the RF output node, the RF-to-analog conversion gain *y* of the envelope detector and the attenuation *z* through the resistive voltage divider network. The values of *x*, *y* and *z* discussed here are in terms of voltage ratios. For ensuring stability, the loop gain must satisfy the design condition given by (2.5) below.

$$\begin{aligned} &Loop\ Gain = x \cdot y \cdot z < 1 \\ &\text{or,} \quad 20 \cdot \log_{10}(x) + 20 \cdot \log_{10}(y) + 20 \cdot \log_{10}(z) < 0dB \end{aligned} \tag{2.5}$$

The baseband to RF up-conversion gain *x* (from the gate to the drain of the PA's power-stage transistors) is typically high since the power-stage is designed to deliver large RF output powers to the load. Therefore, to satisfy (2.5), $(y \cdot z)$ must be a high attenuation value so that the total loop gain is below 0dB. It will be shown through simulations and measurements in Chapter 3 of this thesis that the maximum voltage swing (i.e. maximum increase from the quiescent value V_{GGO}) typically required for the dynamic gate-bias signal V_{dyn} is in the order of ~0.1V. Such a relatively small value of the maximum dynamic gate-bias voltage swing (the swing itself being necessary only over the relatively small power range when the open-loop PA is under compression) can be achieved while still comfortably meeting the design condition specified by (2.5), i.e. with sufficiently high attenuation $(y \cdot z)$ through the feedback elements. This eliminates the necessity of loop compensation networks that are typically found in implementations of negative feedback in PAs to ensure stability (e.g. Figure 1.9), leading to an overall reduction in circuit complexity for implementing positive envelope feedback in RFIC PAs.

2.2.2 Design condition regarding loop bandwidth

To ensure that the implementation of positive envelope feedback does not result in output signal distortion, the value of the loop bandwidth must be sufficiently high. An adequately high loop bandwidth ensures that the dynamic-bias signal injected into the PA transmit chain through the feedback loop is not a distorted version of the PA's output envelope signal. Such a distortion may arise if the loop bandwidth is not adequately high, which may translate into significant amplitude/phase change associated with the higher envelope frequency components in the dynamic-bias signal relative to the lower envelope frequency components. It has been shown that a reasonable estimate of this loop bandwidth requirement is around four times the highest envelope frequency that the PA is transmitting (Onizuka, Ikeuchi, Saigusa, & Otaka, 2012; Katz, Wood, & Chokola, 2016).

In the implementation of positive envelope feedback shown in Figure 2.3, the loop bandwidth is primarily determined by the bandwidth of the envelope detector, and the impedance seen by the feedback circuit elements looking into the power-stage input. Implementations of envelope detectors with high bandwidth have been demonstrated in the literature (Katz, Wood, & Chokola, 2016; Berthiaume, Sharma, & Constantin, 2016; Xia & Boumaiza, 2015). It will be additionally shown in Chapter 3 of this thesis that through careful design considerations, the effect on the loop bandwidth due to the power-stage input impedance that is seen by the feedback circuit elements can be minimized.

Therefore, the proposed dynamic biasing technique based on positive envelope feedback is suitable for linearizing power amplifiers transmitting very large bandwidth signals in contrast to PA designs based on negative feedback. The latter suffers from the requirement of critical high-order loop stability compensation circuits that invariably introduce low-pass filter response effects, thereby severely limiting the effective PA signal bandwidth that can be linearized.

2.2.3 Design condition regarding delay

An important consideration while implementing any feedback circuit, including positive envelope feedback, is the delay t_{del} through the PA's transistor array. As illustrated in Figure 2.7 for a typical power-stage cascode implementation, t_{del} is defined here as the delay measured from the gate plane '*g*' to the drain plane '*d*' of the PA's power-stage transistors.

The value of t_{del} (along with the delay through the feedback elements) must be adequately small to ensure that the detected output envelope at the transistor's drain is not too delayed before being applied to its gate as part of the positive envelope feedback. In the context of signal fidelity and PA efficiency, it has been shown that delay values of more than 2% of the envelope time-period corresponding to the highest envelope frequency can adversely affect PA linearization when using techniques based on envelope-dependent biasing (P. Asbeck & Popovic, 2016).

Besides the absolute value of the gate-drain delay t_{del}, the group delay through the power-stage transistor is another vital parameter to consider while implementing envelope-dependent biasing schemes (Hekkala, January 2012). The group delay is a measure of the variation in the transit time t_{del} through the power-stage transistors over the frequency range of its bandwidth. It is commonly also expressed by the derivative of the phase with respect to frequency ($d\varphi/d\omega$) across the band-pass frequency range. The group delay ripple (Δ in Figure 2.7) across the channel bandwidth should be minimum, to ensure that the application of positive envelope feedback causes minimal distortion arising out of frequency-dependent lags in the dynamic-bias signal, due to varying values of t_{del} across this bandwidth.

It will be shown in Chapter 3 of this thesis that the proposed technique of positive envelope feedback can be successfully used to improve PA performance for values of delay t_{del} and group delay that are typically encountered in PA systems.

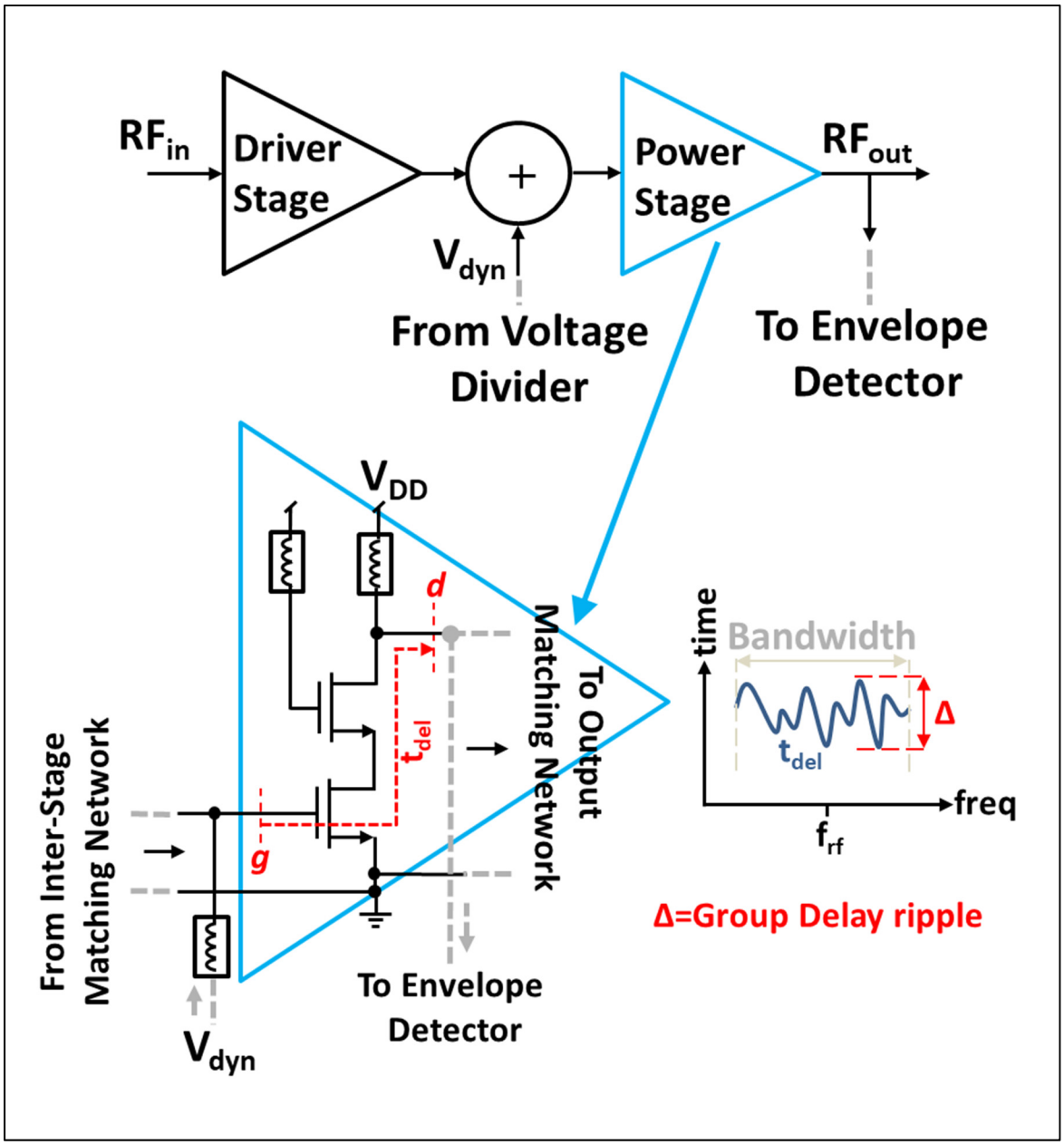

Figure 2.7 Typical PA power-stage schematic with the time delay t_{del} from the gate to the drain of the power-stage cascode transistors. The gate and drain planes are shown with the dotted lines *g* and *d* respectively. The group delay Δ ripple measured over the PA's signal bandwidth around its carrier frequency f_{rf} is also illustrated

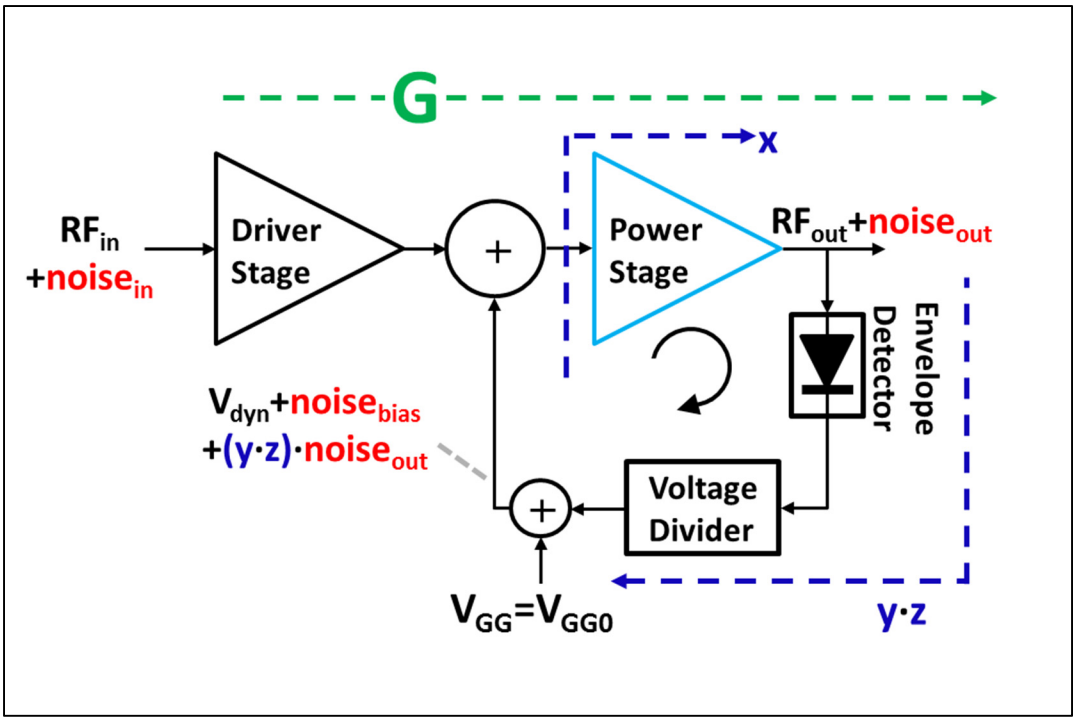

Figure 2.8 PA with positive envelope feedback showing noise levels at the various critical nodes

2.2.4 Considerations regarding noise

Using any kind of feedback, including positive envelope feedback, raises concerns regarding PA output noise degradation. As shown in Figure 2.8, the signal path available from the PA output to its bias input raises the possibility of its output noise (given by $noise_{out}$ in Figure 2.8) being amplified through the feedback circuit elements, and the resulting noise in the dynamic-bias signal being up-converted through the PA power-stage, leading to severe noise degradation at the PA output. It will now be shown that the proposed technique of positive envelope feedback does not lead to such an aggravated noise performance.

For low power levels (hence no positive envelope feedback since the envelope detector is OFF), the PA's output noise $noise_{out}$ is given by (2.6) below and is identical to that for open-loop PA operation.

$$noise_{out} = G \cdot noise_{in} + x \cdot noise_{bias} \tag{2.6}$$

Here, G is the total RF gain through the PA's transmit chain (i.e. driver-stage and power-stage) and parameter x refers to the baseband-to-RF conversion gain from the gate to the drain of the PA's power-stage transistors, as defined in Section 2.2.1, Figure 2.6. $noise_{in}$ is the noise present at the PA's input. $noise_{bias}$ refers to noise contributions from components in the PA's biasing circuit (such as due to the quiescent-bias source V_{GG0}) and is present in any PA design.

For higher power levels, i.e. when the envelope detector is ON and the PA is under closed-loop positive feedback operation, an additional noise contribution $(y \cdot z) \cdot noise_{out}$ is also present in the V_{dyn} signal, as illustrated in the block diagram shown in Figure 2.8. Here, parameters y and z are the RF-to-analog conversion gain of the envelope detector and the attenuation through the resistive voltage divider network respectively, as defined in Section 2.2.1, Figure 2.6.

The large attenuation $(y \cdot z)$ through the feedback elements (to maintain stability as described in Section 2.2.1) ensures at the same time that the output noise $noise_{out}$ is reduced to insignificant levels in V_{dyn}, compared to $noise_{bias}$ from components in the PA's biasing circuit. The primary contribution to noise in the bias signal V_{dyn}, therefore, comes from $noise_{bias}$, and is comparable to that in any typical PA biasing scheme. It is worthwhile to note that the noise contribution of these bias circuit elements are accounted for while designing any PA (with or without feedback) and does not represent a source of noise that is specific only to PAs using positive envelope feedback.

Any slight increase in the PA's output noise levels with positive feedback at higher output power is due to an increase in the PA's gate-bias voltage at these power levels when using the proposed technique of positive envelope feedback. The increase in gate bias results in an increase of the PA's overall RF gain G compared to the PA under constant bias. Consequently, a higher gain G is applied to the PA's input noise $noise_{in}$, as shown in (2.6).

Such a phenomenon of a slight increase in the PA's output noise will also be demonstrated through an example in Chapter 3 of this thesis. However, this does not represent any additional noise degradation that arises from the feedback of output noise through the bias into the PA's transmit chain due to the specific implementation of positive envelope feedback. In fact, such an increased output noise may be expected of any PA linearization scheme (e.g. (Kang, Baek, & Hong, 2017; Kang, Sung, & Hong, 2018)) that depends on improving its AM-AM through an increase of its RF gain.

2.3 Summary: Theory of positive envelope feedback

The theory underlying the proposed technique of positive envelope feedback is now complete. Table 2.1 is a summary of the various design conditions discussed in Section 2.2 that are necessary to implement positive envelope feedback successfully in RFIC PAs. These design conditions will be referred to again in Chapter 3, where the implementation of positive envelope feedback, via simulation as well as experimental measurements, is illustrated.

Table 2.1 Summary of design conditions necessary to successfully implement positive envelope feedback

Design condition	Brief description	Remarks
Loop gain	Loop Gain < 1 (or 0dB)	A loop gain lesser than unity is necessary to maintain PA stability under positive envelope feedback, since there is no scope for phase margin design. The typically high baseband-to-RF conversion gain from the gate to the drain of the PA's power-stage transistors must be compensated for by an adequately high value of attenuation through the envelope detector and the resistive voltage divider.
Loop bandwidth	Loop Bandwidth > 4 times maximum envelope frequency	An adequately large loop bandwidth is necessary to eliminate the possibility of PA output signal distortion due to significant frequency-dependent amplitude and phase changes associated with the envelope in the feedback bias signal.
Signal delay	Values of absolute delay and group delay through PA transistors must be small	Low values of absolute delay and group delay through the PA's power-stage transistors are necessary to ensure output signal fidelity and PA efficiency. High values of signal lags, and/or frequency dependent signal lags, in the feedback bias signal may lead to severe distortion effects in the PA's output signal.
Noise	Sufficient signal attenuation is necessary through feedback loop	An adequately large signal attenuation through the feedback elements of the positive envelope feedback loop ensures that the PA's output noise levels are reduced to insignificant levels in the bias signal before being injected back into the PA's transmit chain.

CHAPTER 3

POSITIVE ENVELOPE FEEDBACK: DESIGN AND IMPLEMENTATION

> "If the experiments, which I urge, be defective, it cannot be difficult to show the defects; but if valid, then by proving the theory, they must render all objections invalid."
>
> Isaac Newton

In this chapter, the design and implementation of positive envelope feedback in PAs is described. Extensive simulations of a first PA design in Section 3.1, as well as measurements of a second fabricated PA design in Section 3.2, are used. Both PAs are based on RF-SOI CMOS technologies from two different foundries. Results from both these platforms confirm the same levels and trends of linearity improvement that is possible by using positive envelope feedback, and highlight the efficacy yet inherent simplicity of the proposed technique.

3.1 Validation of positive envelope feedback using simulation

3.1.1 Schematic of SOI CMOS PA line-up

As a first test platform to validate the theory described in Chapter 2, simulations were carried out on the SOI CMOS PA system shown in Figure 3.1. The design was done using Cadence™, while the simulations were performed using ADS™ via the RFIC Dynamic Link™ feature. A description of the test-bench follows. For this exercise of validation via simulation, the SOI CMOS PA design is intentionally kept simple and does not use any elaborate linearization scheme, to facilitate understanding the direct advantages of using the proposed positive envelope feedback technique for improving PA linearity. A simple design also eliminates the possibility of the proposed technique interacting with other linearization schemes that would not allow distinguishing clearly the linearity improvement achieved with our method.

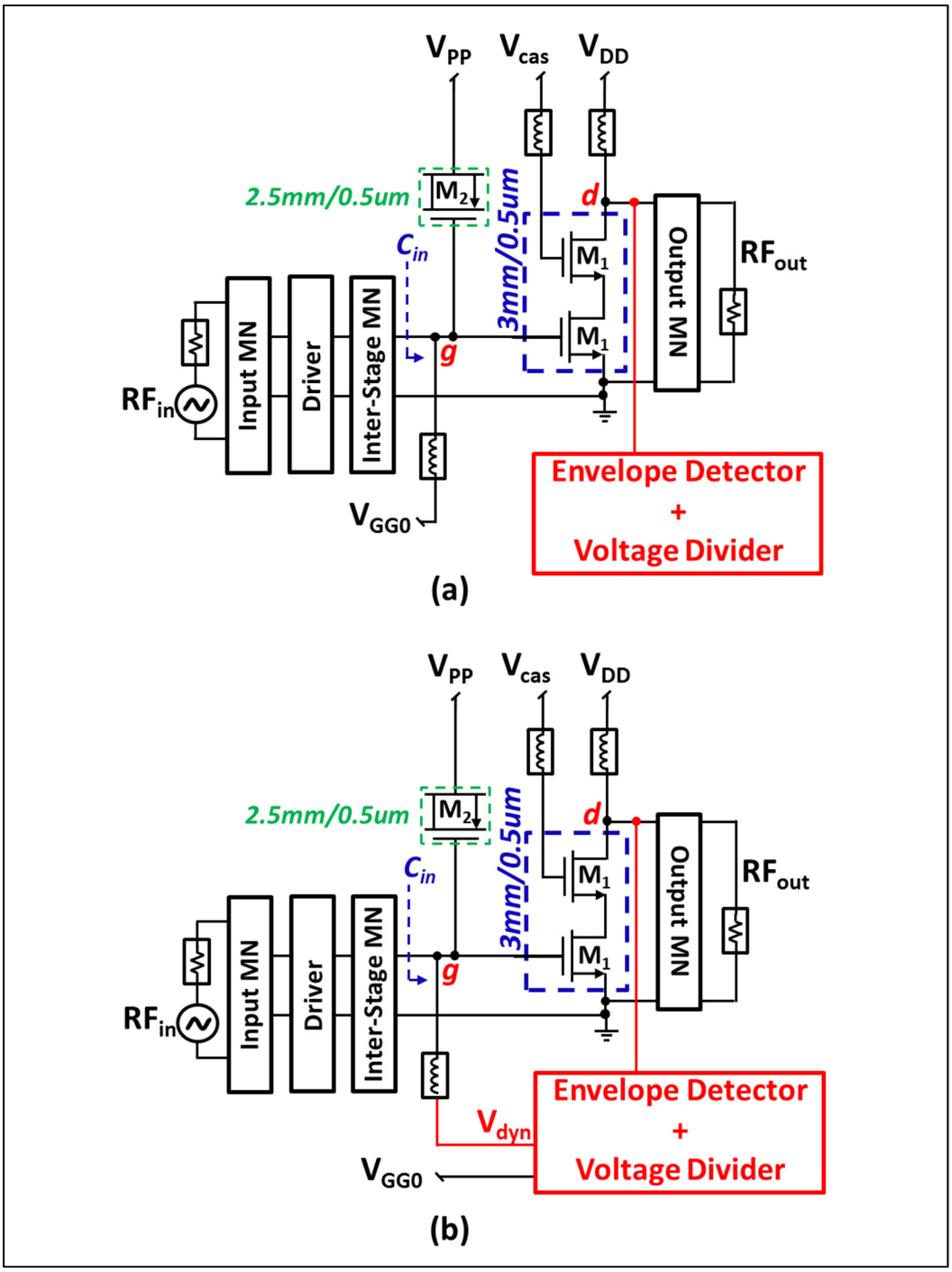

Figure 3.1 SOI CMOS PA line-up with (a) constant gate bias and (b) dynamic gate bias through positive envelope feedback. The feedback network is left connected to the output in both cases to avoid using two different output matching networks for (a) and (b) to ensure optimum PA performances

Figure 3.1(a) and 3.1(b) show the 1.9GHz RFIC SOI CMOS PA used for this validation exercise. The device technology used is IBM CMOS SOI7RF 0.18um technology. Refer to Appendix I for a description of a representative metal stack-up for this process. From private discussions with Skyworks Solutions, Inc., it has been confirmed that for the output power levels described here when the PA is under moderate gain compression, the foundry models for simulation provided with this technology are well correlated with actual measurement results in the laboratory. The size of the power-stage cascode transistors M_1 is 3mm/0.5um. The driver-stage transistors and the matching networks are not shown for conciseness. The PA input and output ports are terminated with 50Ω impedances. V_{DD}, V_{cas} and V_{GG0} refer to the DC drain supply voltage, DC cascode CG bias voltage and the DC gate-bias voltage respectively of the PA's power-stage. Figure 3.1(b) shows the same PA line-up as Figure 3.1(a), but with its gate bias varied dynamically through the proposed positive envelope feedback technique detailed in Chapter 2, in contrast to the constant DC bias V_{GG0} applied in Figure 3.1(a). In both cases (a) and (b), the feedback network (envelope detector and voltage divider) is left connected to the power-stage transistor drain to ensure that the optimized PA output impedance (and consequently the output matching network) is identical in both cases, and therefore allowing a fair comparison of the resulting PA performances from both.

Additionally, the power-stage gate, in both Figure 3.1(a) and 3.1(b), is connected to the gate of a drain-source shorted PMOS device M_2, the drain/source terminal of which is biased with the DC voltage V_{PP}. As described in (Chengzhou, Vaidyanathan, & Larson, 2004), such a drain-source shorted PMOS device enables an improvement of the CMOS PA's linearity by reducing the variation of the gate-source capacitance C_{gs} seen looking into the input of the power-stage-transistor. The cost of such an improved linearity (due to improved AM-PM) is a reduction in the PA's RF gain, due to an increased total capacitance (C_{in}=C_{ggn}+C_{ggp}, instead of C_{ggn} only) seen looking into the power-stage input. The value of V_{pp} and the size of M_2 in Figure 3.1 are optimized to achieve a maximally flat C_{in} vs. V_{GS} profile for the PA power-stage. Details of this PMOS compensation are further described in Section 3.1.6, and it will be shown that the linearity improvement achieved with positive envelope feedback is independent of the C_{gs} compensation effects.

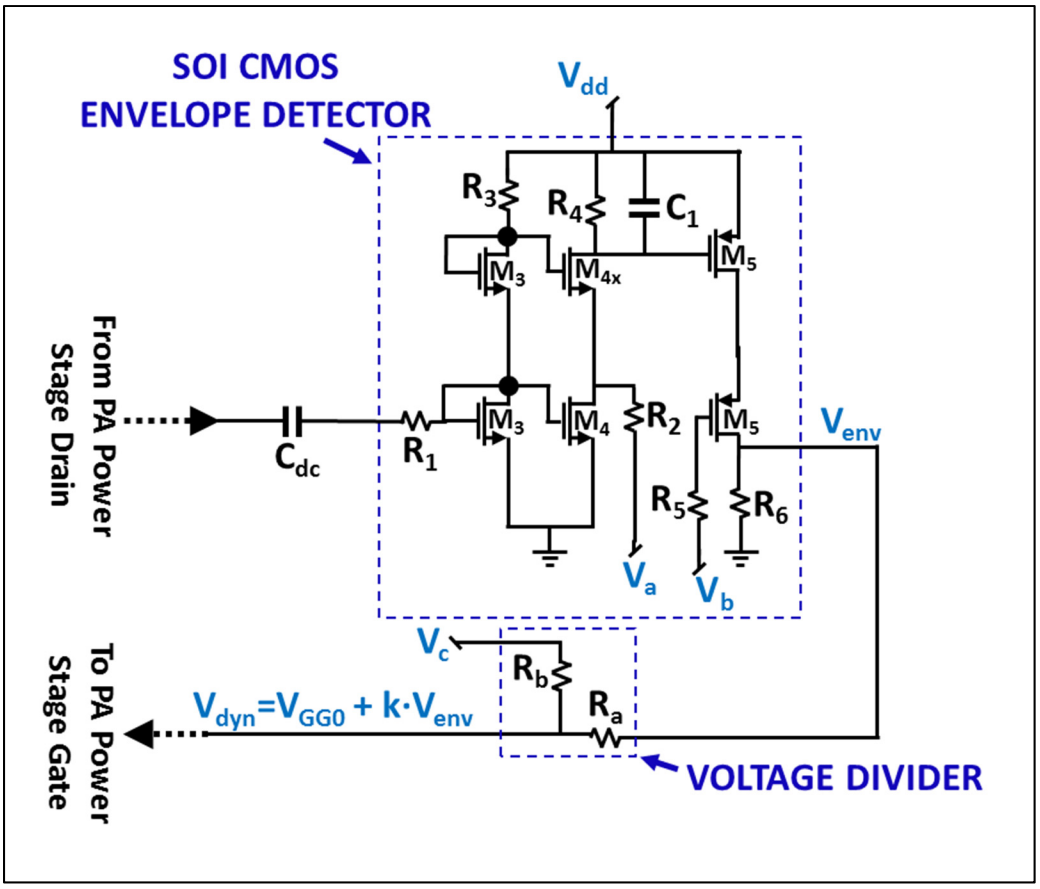

Figure 3.2 Schematic of Envelope Detector and Voltage Divider circuits

3.1.2 Design of envelope detector and voltage divider

A number of envelope detector architectures are discussed in the literature that allows achieving a large detector bandwidth while consuming very little DC power (Berthiaume, Sharma, & Constantin, 2016; Xia & Boumaiza, 2015). Figure 3.2 shows the schematic of the specific SOI CMOS envelope detector and voltage divider circuits used in Figure 3.1.

The structure of this envelope detector is based on that described in (Carrara, Presti, Scuderi, Santagati, & Palmisano, 2008). As shown in Figure 3.2, the drain of the power-stage transistor (*d* in Figure 3.1) is interfaced with the envelope detector input via a DC blocking capacitor C_{dc}. The high value of resistor R_1 results in a high input impedance of the envelope

detector and ensures that the RF signal at the drain of the RF transistor in the power-stage is minimally disturbed. Additionally, R_1 implements a voltage to current mode conversion at the drain node of transistor M_3. Transistor M_4 is sized so as to incorporate some current amplification going from M_3 to M_4. Transistor M_{4x} is configured to rectify the detector's input signal and extract its envelope via R_4-C_1 after the envelope crosses a specific threshold value, the threshold itself being controlled with the help of DC voltage V_a and resistor R_2. The PMOS cascode transistors M_5 incorporate further gain into the envelope detector structure, this gain being a function of the DC gate voltage V_b that is applied. Further details of the operating principle for this current-mode envelope detector may be found in (Carrara, Presti, Scuderi, Santagati, & Palmisano, 2008).

The voltage divider is implemented using a pair of resistors R_a and R_b, their resistance values being selected to achieve a voltage division ratio k. The output of the voltage divider is applied to the PA's power-stage gate. R_a and R_b are additionally so sized such that they minimally load the gate-source capacitance C_{gs} of the PA's power-stage transistors. The value of DC voltage V_c is chosen such that after division through the voltage divider, the quiescent value of the dynamic-bias signal V_{dyn} is V_{GG0}.

The output of the envelope detector is critically determined by the values of the two DC control voltages V_a and V_b in Figure 3.2. Varying V_a and V_b allow varying the detector's sensitivity (defined by the threshold power level P_{ref}) and the detector's gain conversion slope (defined by Θ) respectively. As illustrated in Figure 3.3, P_{ref} refers to the PA's output power level where the value of the dynamic gate bias starts increasing from its quiescent value V_{GG0}, while Θ refers to the rate of increase of the value of the dynamic bias vs. the detector's input power. P_{out} is the PA's output power and also the detector's input power.

Note that the quiescent current consumption of the envelope detector for the PA system in Figure 3.1 is only 1.7mA, compared to 45.0mA for the transistors in the PA lineup. 1.7mA represents only 3.6% of the total system quiescent power requirement when positive envelope feedback is implemented. At high output RF power, where the average current

drawn by the PA line-up is significantly higher than the quiescent value, the 1.7mA has an even smaller effect on the power efficiency of the PA system. It is also useful to point out that the envelope detector remains biased for all the measurements presented here in Section 3.1, irrespective of whether we are referring to results obtained from the structure in Figure 3.1(a) or Figure 3.1(b).

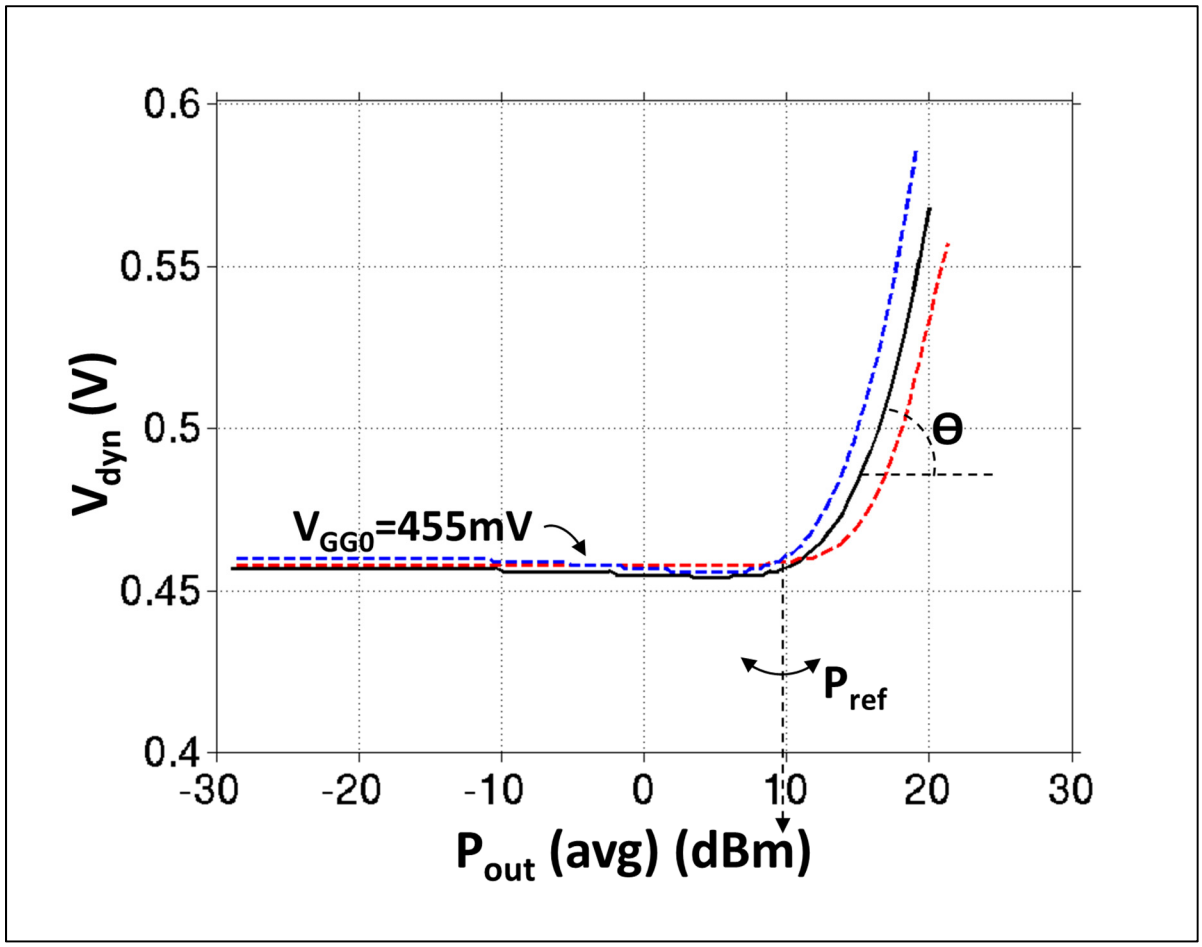

Figure 3.3 V_{dyn} as a function of the average power at the input of the envelope detector. The detector's sensitivity (P_{ref}) and the gain conversion slope (Θ) are indicated, as well as three different profiles of the detector's transfer function vs. P_{out} obtained by varying the control voltages V_a and V_b. The discontinuities in the plots at low P_{out} values are simulation artifacts from ADS™ simulation, due to the severe nonlinearities associated with the detector turn-on and the values of error tolerances used to ensure simulation convergence

Additionally, the maximum value of the up-conversion gain from the gate-bias input node (*g*) to the drain of the PA's power-stage (*d*) in Figure 3.1 is found to be 17dB. Therefore, to maintain PA stability under positive envelope feedback as per the loop gain condition of Section 2.2.1, the gain through the feedback elements (detector and divider) has to be less than -17dB, to ensure a total loop gain that is below 0dB. After designing the feedback circuit to achieve the voltage swing of the dynamic-bias signal necessary to linearize the PA system in this implementation, the gain through the envelope detector and the voltage divider is calculated to be -22dB, which results in a net loop gain of 17dB - 22dB = -5dB through the positive envelope feedback loop. It was verified through simulation that the net loop gain of the PA system is lower than -5dB for all operating PA power levels and envelope frequencies, consequently guaranteeing the unconditional stability of the PA system under positive envelope feedback. The loop bandwidth is simulated to be ~50MHz, which allows PA linearization for envelope bandwidths up to ~10MHz using positive envelope feedback (as per Section 2.2.2). As per Section 2.2.4, the -22dB attenuation through the loop feedback elements ensures that the PA's output noise does not degrade due to the implementation of positive envelope feedback.

It is worthwhile mentioning that the structure of the envelope detector and the voltage divider shown in Figure 3.2 benefits from the implementation of certain components off-chip in a first design cycle, to allow an experimental optimization of the transfer function from the PA's power-stage drain to the PA's power-stage gate bias input through the feedback circuit. For example, by implementing the voltage divider circuit in Figure 3.2 off-chip for a first design cycle allows a more convenient means to tune the voltage division ratio *k*. The optimization targets achieving the best output linearity (e.g. lowest IMD_3) for a given value of efficiency when the PA operating conditions are weakly nonlinear, and for output power levels where PA performance is sought to be improved through positive envelope feedback. Once the optimum values of R_a and R_b are determined, they can be easily integrated on-chip for subsequent design cycles. Similarly, off-chip facilities to modify R_2, R_6, etc. as well as the control voltages V_a and V_b are useful for a first PA design cycle.

3.1.3 PA performance under 1-tone RF excitation

Figure 3.4 shows the PA's *Gain* vs. P_{out} profile using a 1-tone RF excitation at 1.9GHz, with and without positive envelope feedback. The dynamic gate-bias signal V_{dyn} vs. P_{out} under positive envelope feedback is also shown. The profile of V_{dyn} is optimized using the tuning controls for P_{ref} and Θ, as discussed in Section 3.1.2. As shown, an increase of 75mV in the value of the dynamic gate-bias voltage V_{dyn} at P_{out}=18dBm (relative to its value of 455mV at low PA output power levels) is adequate to compensate for the gain compression at higher output powers and linearize the PA's AM-AM. Under the CW RF excitation used here, V_{dyn} is a DC signal; however, for an envelope varying RF excitation (such as a 2-tone signal in Section 3.1.4), V_{dyn} translates into a dynamic signal varying at the rate of the envelope frequency.

Note that the value of V_{dyn} at lower PA output powers (P_{out}<8dBm in Figure 3.4) is identical to its quiescent-bias value V_{GG0} under constant-gate bias. Therefore, the PA's quiescent power consumption is identical for both the constant gate-bias case and under positive envelope feedback.

3.1.4 PA performance under 2-tone RF excitation

Figure 3.5(a) shows the PA's *Gain* vs. P_{out} profile under a 2-tone RF excitation at 1.9GHz and a frequency spacing of 1MHz, with and without positive envelope feedback. The dynamic-bias signal V_{dyn} is identical to that in Figure 3.4 and is therefore not shown; however, V_{dyn} now varies at the rate of the envelope of the 2-tone excitation and is not merely a DC signal such as in Figure 3.4.

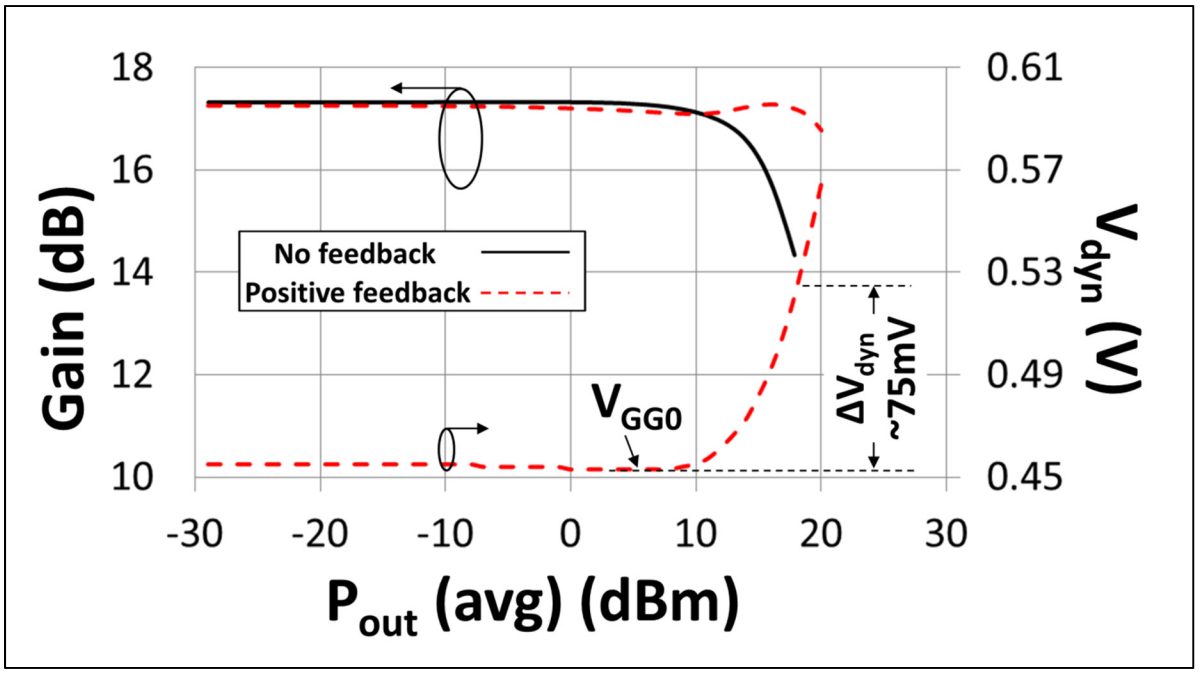

Figure 3.4 *Gain* vs. P_{out} for PA under 1-tone RF excitation, without and with positive feedback. The corresponding DC value V_{GGO} of the dynamic-bias signal V_{dyn} vs. P_{out} is also shown. An increase in the dynamic gate-bias voltage signal V_{dyn} at higher output powers linearizes the PA's *Gain* profile, while the value of the gate bias at back-off power levels is kept equal to V_{GG0}

The improvement in the PA's *Gain* profile at higher power levels due to a reduction in signal clipping under positive envelope feedback translates into an IMD_3 improvement of up to 2.5dB and 4.5dB for IMD_{3lo} and IMD_{3hi} respectively, as illustrated in Figure 3.5(b). For a similar 2-tone RF excitation but with a 10MHz spacing, Figure 3.6 shows the improvement in the IMD_3 values with positive envelope feedback, and confirms the same trend and level of linearity improvement as that in Figure 3.5(b). The transient simulation of the power-stage transistor's drain voltage at P_{out}=16dBm under two-tone RF excitation is shown in Figure 3.7, with and without positive envelope feedback. The reduced signal clipping due to positive envelope feedback translates into reduced output signal distortion and lower levels of intermodulation distortion products, resulting in improved PA linearity performances.

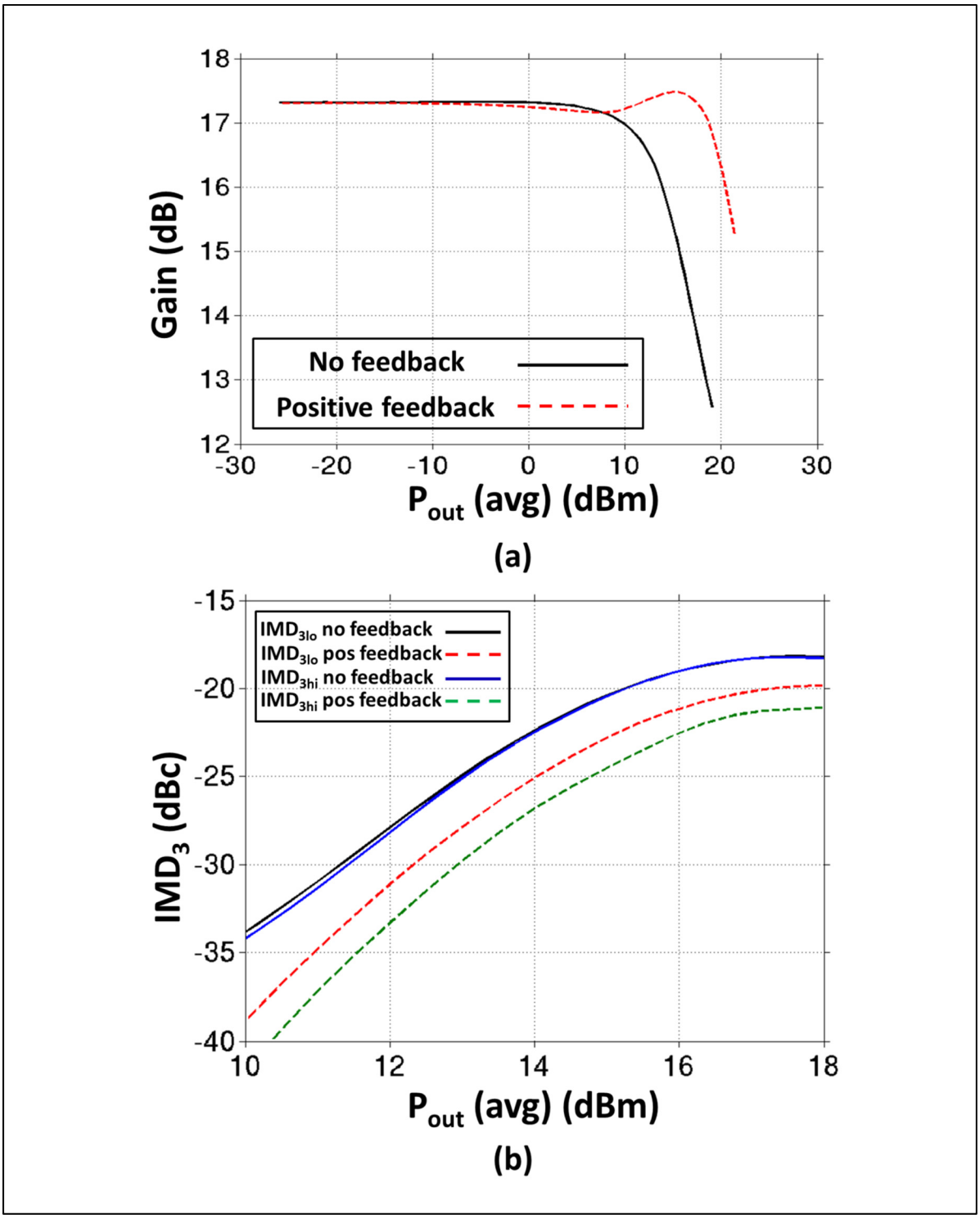

Figure 3.5 (a) *Gain* vs. P_{out} for PA under 2-tone RF excitation, without and with positive feedback. The frequency spacing used is 1MHz. (b) IMD_3 vs. P_{out} shows an improvement under positive feedback for P_{out}>10dBm. Note that the x-axis is the PA's average P_{out}

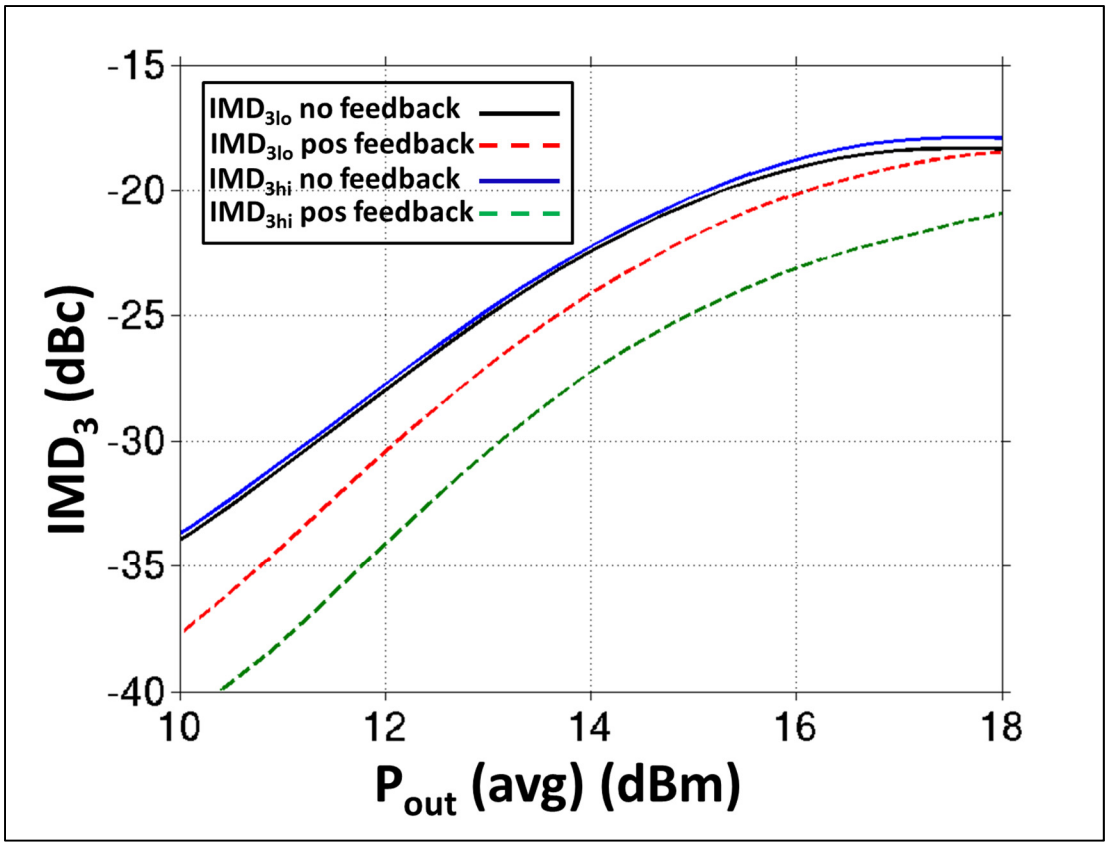

Figure 3.6 *IMD₃* vs. P_{out} for PA under 2-tone RF excitation, without and with positive feedback. The frequency spacing used is 10MHz

3.1.5 PA performance under modulated RF excitation

The RFIC PA is now excited with an envelope-modulated RF signal. The excitation used is an RF carrier modulated by a Forward Link CDMA signal with a signal bit-rate of 1.2288MHz, with 4 samples/bit and 256 total number of symbols. It is generated using the *PtRF_CDMA_IS95_FWD* component in the *Sources-Modulated* library in ADS™. Figure 3.8 shows the Adjacent Channel Power Ratio (*ACPR*) vs. P_{out} for the upper and lower adjacent channels, with and without positive envelope feedback. An improvement of up to 2.5dB in its *ACPR* value is observed for the PA's higher range of output power levels, and demonstrates the usefulness of the proposed approach for PA linearity improvement under modulated excitation.

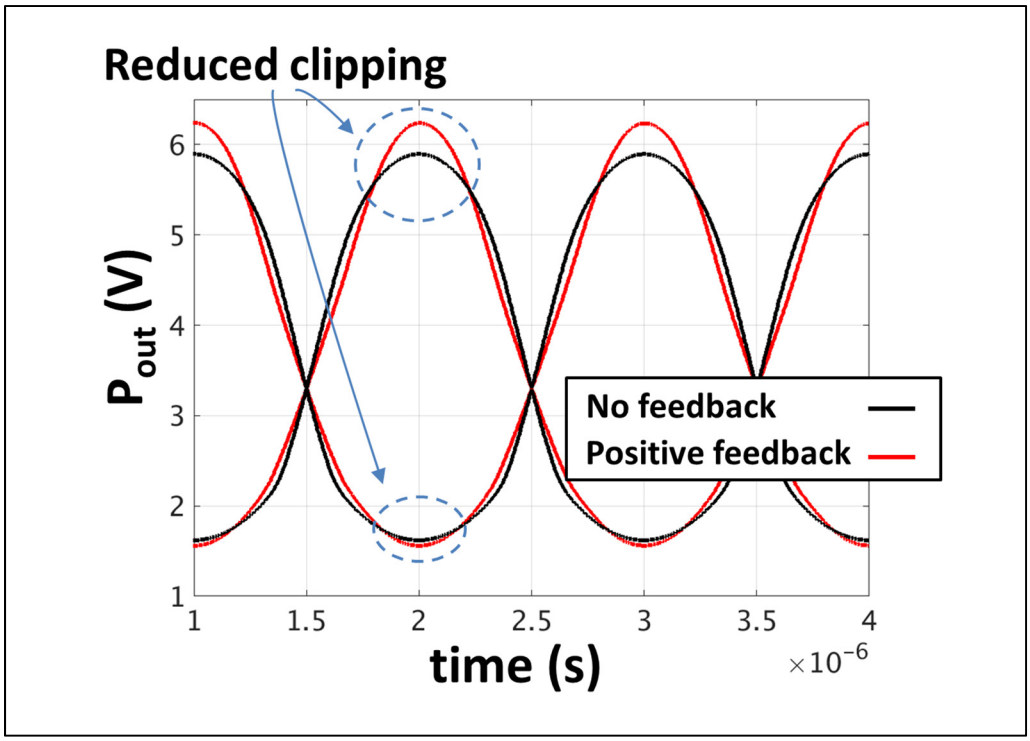

Figure 3.7 Transient simulation showing envelope of transistor drain voltage under two-tone RF excitation, without and with positive envelope feedback. Positive envelope feedback results in reduced clipping. The frequency spacing used is 1MHz and P_{out} is 16dBm

3.1.6 Comments regarding PA power-stage input impedance

As described in Section 3.1.1, the gate of a drain-source shorted PMOS transistor is connected to the gate of the power-stage NMOS CS transistors, to linearize the variation of the input capacitance seen looking into the PA's power-stage input (Chengzhou, Vaidyanathan, & Larson, 2004). Figure 3.9 shows this input capacitance C_{in} as a function of the gate-source voltage V_{GS} of the NMOS transistor M_1 in Figure 3.1. The capacitance values associated with the shorted PMOS and the power-stage NMOS (which together combine into C_{in}) were extracted separately with the help of the Cadence™ simulation tool, based on the RF voltage and current signals at their respective branches. Hence three different capacitor values are shown – of the NMOS transistor alone (C_{ggn}), of the PMOS transistor alone (C_{ggp}),

and of the PA power-stage with the gate of the NMOS transistor connected to the gate of the drain-source shorted PMOS transistor (C_{ggn}+C_{ggp}).

As shown in Figure 3.9, the inverse gate capacitance variation of the PMOS device (C_{ggp}) relative to that of the NMOS device (C_{ggn}) reduces the overall variation of the power-stage input capacitance C_{in}=C_{ggn}+C_{ggp} as the gate-source voltage V_{GS} varies. This reduced C_{in} variation results in a significantly improved AM-PM characteristic and contributes to the PA's improved linearity, as described in (Chengzhou, Vaidyanathan, & Larson, 2004). The capacitance compensation is optimized for minimum C_{in} variation by properly sizing the PMOS device and with appropriate choice of the voltage V_{PP} applied to the drain-source shorted PMOS terminal. The size of the PMOS device used for the PA system here is 2.5mm/0.5um, and the value of V_{PP} used is 0.8V. The trade-off associated with this compensation is the increased overall input capacitance C_{in} (~10.5pF here), which results in reduced RF gain for the PA system.

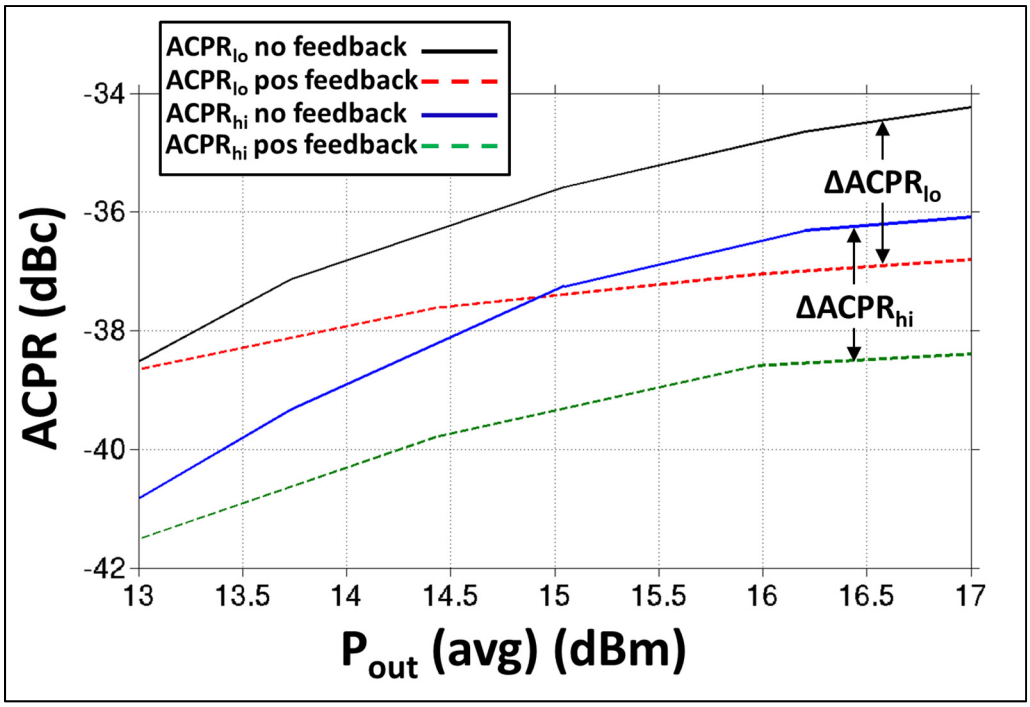

Figure 3.8 *ACPR* vs. P_{out} for PA under modulated RF excitation, without and with positive feedback. Note that the x-axis is the average P_{out}

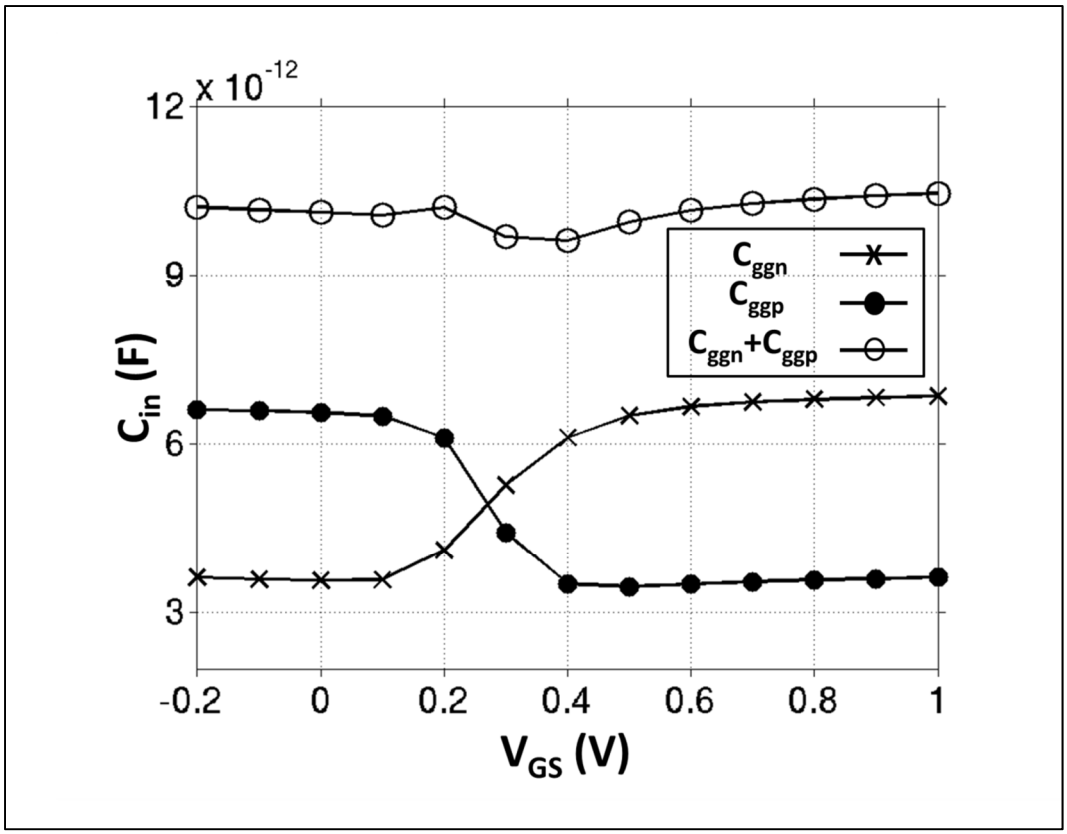

Figure 3.9 Input capacitance C_{in} seen looking into the PA's power-stage. C_{ggn} is the capacitance of the NMOS transistor alone, C_{ggp} is the capacitance of the drain-source shorted PMOS transistor alone and C_{ggn}+C_{ggp} is the total capacitance seen looking into the PA's power-stage when the NMOS transistor has the gate of the drain-source shorted PMOS transistor connected to its gate

Note, that the PMOS compensation proposed in (Chengzhou, Vaidyanathan, & Larson, 2004) and used here is useful to improve the PA's linearity over a wide range of *moderate* power levels only, i.e. well below the PA's P_{1dB} compression point as evidenced in (Chengzhou, Vaidyanathan, & Larson, 2004, Figure 4, Figure 5). The resulting improvement of the PA's AM-PM is not adequate for improving linearity at *higher* output powers when amplitude distortion due to drain-current clipping becomes the dominant source of PA nonlinearity (Chengzhou, Vaidyanathan, & Larson, 2004, Page 6).

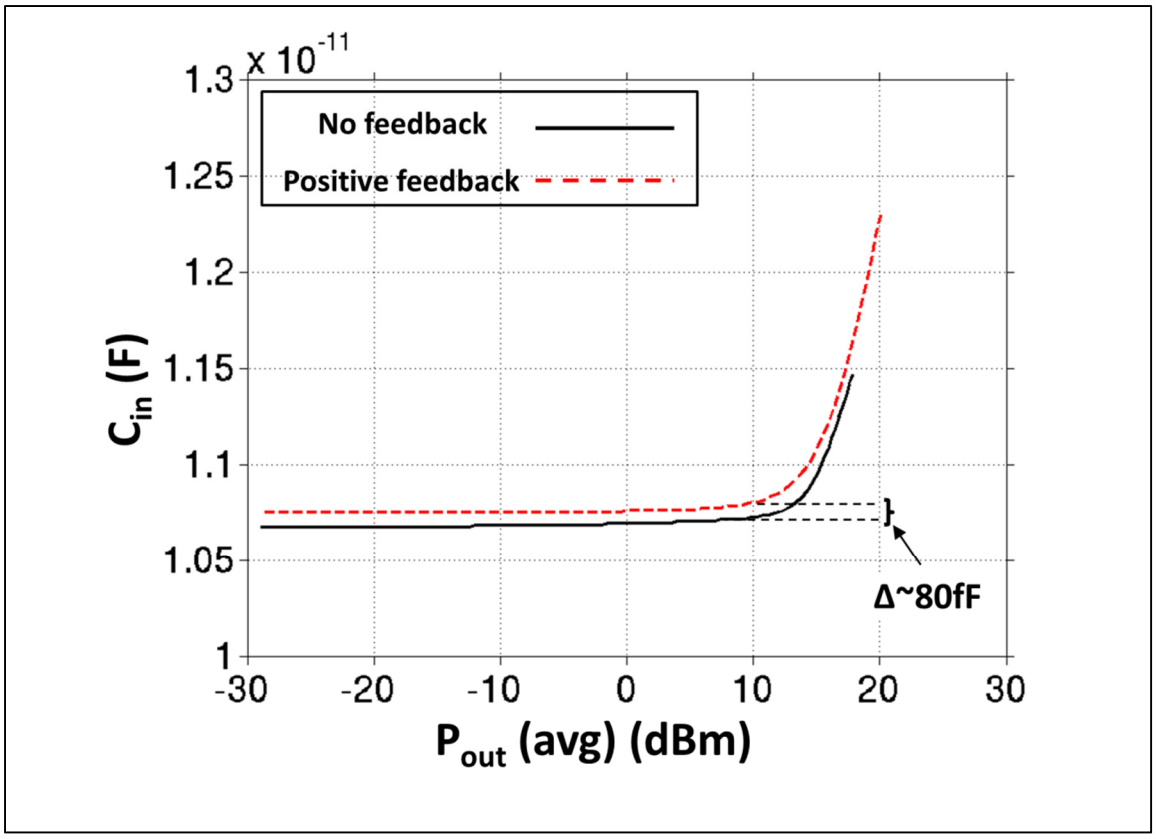

Figure 3.10 Capacitance seen looking into the PA power-stage input as a function of the PA's output power, with and without positive envelope feedback. The minimal difference in input capacitance (~80fF) at low output powers is due to the slight loading effect introduced when the feedback loop is connected

However, it is of interest to investigate if the PA's linearity improvement reported in this thesis (Section 3.1.3, 3.1.4 and 3.1.5) is also a result of the positive envelope feedback technique interacting with this PMOS compensation, and not only because of the decreased amplitude distortion (due to reduced signal clipping) as postulated earlier. For clarifying this aspect, the input capacitance of the PA's power-stage is simulated and plotted as a function of the PA's RF output power under CW excitation, both with and without the implementation of positive envelope feedback, i.e. we simulate C_{in} of the PA schematic in Figure 3.1(a) and Figure 3.1(b) respectively are simulated. As shown in Figure 3.10, there is no significant change in this input capacitance C_{in} when the positive envelope feedback loop is connected. The small 80fF difference is a result of a slight loading effect introduced when the feedback

loop is connected and is insignificant relative to the 10.5pF overall input capacitance. Figure 3.10 validates that the linearity improvement through positive envelope feedback demonstrated here is a separate and distinct linearity enhancement technique from the PMOS input capacitance compensation technique, and is not a result of the positive feedback loop interacting with the PMOS compensation in some indirect manner. For the upper range of PA power levels where the PA's gain starts compressing, positive envelope feedback effectively improves PA linearity by reducing amplitude distortion arising out of drain-current clipping.

3.1.7 Comments regarding delay

The simulated value of the delay t_{del} (defined in Figure 2.7) from the gate (g) to the drain (d) terminals of the PA's power-stage transistor in Figure 3.1 is found to be ~300ps. If we use the 2% metric suggested in (P. Asbeck & Popovic, 2016) to approximate the maximum allowable delay with respect to the time period of the maximum envelope bandwidth that can be successfully transmitted when the PA is being linearized using positive envelope feedback, it suggests a potential maximum envelope bandwidth of ~70MHz. However, the value of the power-stage input impedance seen by the feedback circuit, as well as practical delay values through the envelope detector in the feedback network, reduces the value of this maximum possible bandwidth. The group delay Δ for the implementation in Figure 3.1 is found by simulation to be 4% over a 20MHz bandwidth around the carrier frequency of 1.9GHz.

To further explore the possibility of using the proposed positive envelope feedback technique when the PA is transmitting very large bandwidth signals envisaged for millimetre-wave applications, the transistor gate-drain delay t_{del} is simulated for a Skyworks 28GHz PA designed using 45nm CMOS SOI technology. Without going into the PA design details, the delay t_{del} is found to be ~70ps and the group delay Δ is 4% over a 1GHz bandwidth. The approximate t_{del} delay criteria related to 2% of the inverse time-period of the maximum envelope frequency gives a potential maximum signal bandwidth of ~300MHz (expected to be slightly less in a real test-case, after accounting for practical delay values through the

envelope detector) that can be transmitted when the PA is being linearized using positive envelope feedback, and highlights the potential of using the proposed technique for millimetre-wave PAs aimed at 5G mobile applications, where it is speculated that the signal bandwidth of interest for handset applications is expected to be 200MHz (P. M. Asbeck, Rostomyan, Özen, Rabet, & Jayamon, 2019).

3.2 Validation of positive envelope feedback using experimental measurements

3.2.1 Description of Proof-of-Concept Device Under Test (DUT)

The proposed method of positive envelope feedback is now validated through implementation using a 5GHz SOI CMOS PA system (Sharma, Constantin, & Soliman, 2017). It is designed as a first proof-of-concept prototype unit in a hybrid form, i.e. in two separate IC's using 0.18um technology from TowerJazz as well as SMT components to facilitate investigations. The PA lineup IC is a differential 3-stage design (2 driver-stages + 1 power-stage) with a cascode structure (1 CS device + 2 CG devices) and designed for flip-chip assembly on a 6-layer multi-chip module (MCM), which is further assembled on a PCB. All DC lines have 100pF decoupling capacitors on the MCM, while the critical DC lines additionally have 1nF and 10nF decoupling capacitors on the PCB. Figure 3.11 shows the schematic of the PA's power-stage. Design details of the driver stages are not shown here for conciseness and also because their design details have minimal bearing on the improvement in PA performance from using positive envelope feedback that is demonstrated here. Additionally, this PA design is based on designs provided by our industrial partner (Skyworks Solutions, Inc.) and providing specific PA design details (regarding component values, transistor sizes, matching circuits, etc.) is restricted due to potential future commercialization of this design. Note that the exercise in this section focuses on the validation of the proposed positive envelope feedback concept, which itself is independent of the specific PA design that is used. The reader is encouraged to consult PA architectures discussed in (Niknejad, Chowdhury, & Chen, 2012) to extract typical values of PA design parameters that are also used for the PA design in Figure 3.11. As also shown in Figure 3.11, the output of the power-stage is connected via an SMT DC block capacitor C_{dc}=0.5pF to the

input of an envelope detector, whose architecture was shown in Figure 3.2 and described in Section 3.1.2. The detector's large input impedance ensures that the power loss at the PA's output is negligible. The envelope detector IC for this prototype dual-IC module is assembled on the PCB via wire-bonding and fabricated using the same 0.18um SOI CMOS technology from TowerJazz as the PA. The voltage divider is implemented using SMT resistors on the PCB to enable off-chip tuning for this first prototype design. The values of the envelope detector components are given in Figure 3.11.

A photograph of this prototype dual-IC module is shown in Figure 3.12. The PA chip size is 2.800mm x 1.275mm, and the wire-bond envelope detector chip size is 0.625mm x 0.625mm i.e. ~11% of the PA size. However, a single chip integration would avoid the need of wire-bonding pads for the envelope detector and would allow the envelope detector and the resistor divider to be implemented using a much smaller chip area, estimated at ~5%. Additionally, the total quiescent current of the system is 96mA, of which the detector consumption is only 1.1mA, i.e. 1.2% of the total quiescent current. As noted earlier in Section 3.1.2, when the PA is operating at higher power levels, the detector's share of the system's total current consumption is even lower. All of the above characteristics highlight the usefulness of the proposed method of positive envelope feedback in the context of simple circuit techniques that allow PA performance improvement while requiring only minimum overhead in terms of additional circuit area, power consumption and complexity. It is useful to point out that the envelope detector remains biased for all the measurements that are discussed in Section 3.2.2 and Section 3.2.4.

3.2.2 Experimental measurements

Figure 3.13 shows the PA's AM-AM under CW excitation at 5.4GHz in two states - with constant gate bias (R_a in Figure 3.11 open) and with positive envelope feedback (R_a in Figure 3.11 connected). The improved gain profile under positive envelope feedback leads to an improvement in the PA's P_{1dB} by 1.7dB.

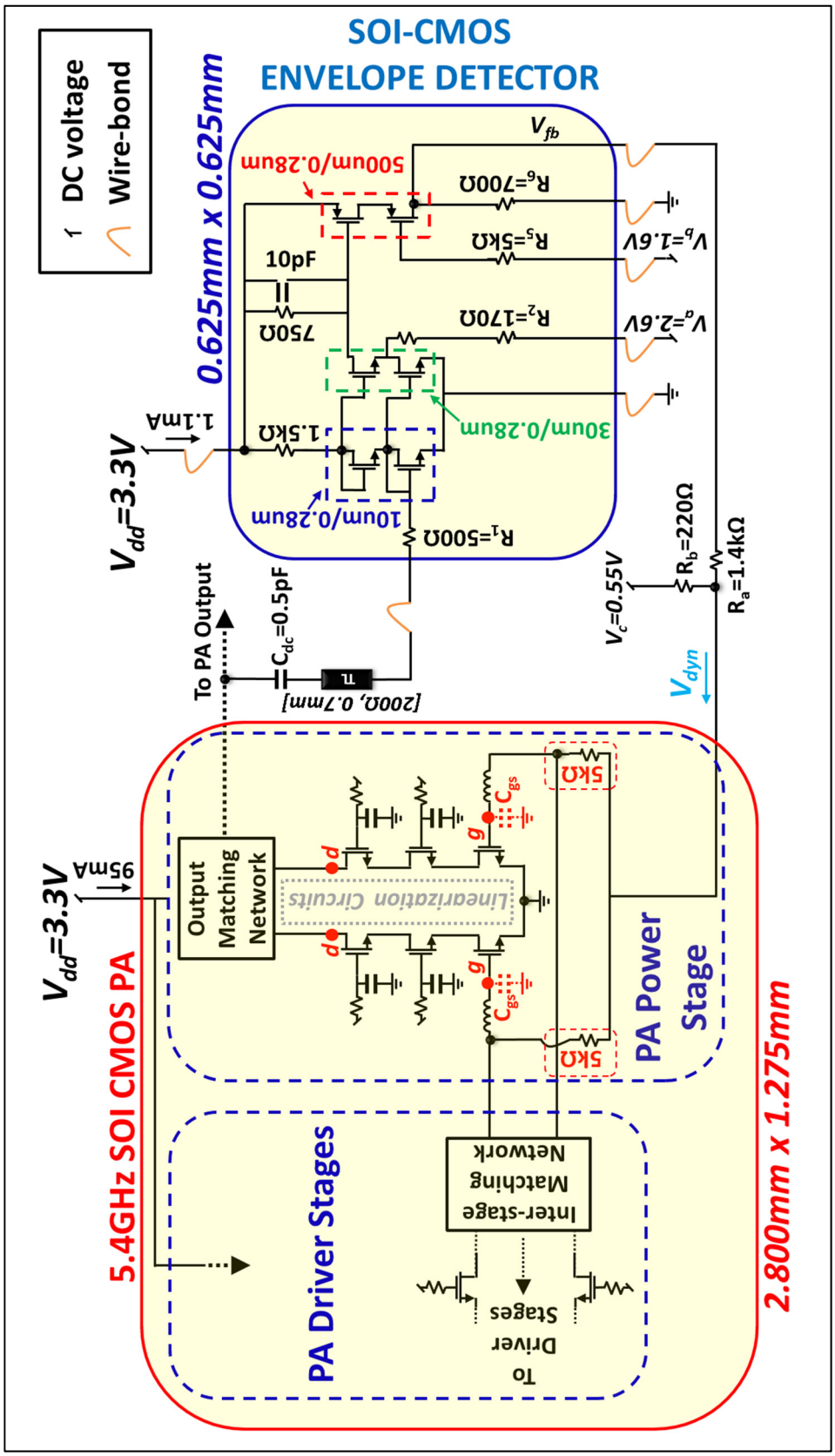

Figure 3.11 Simplified schematic showing PA differential power-stage, envelope detector and resistive voltage divider in positive envelope feedback implementation

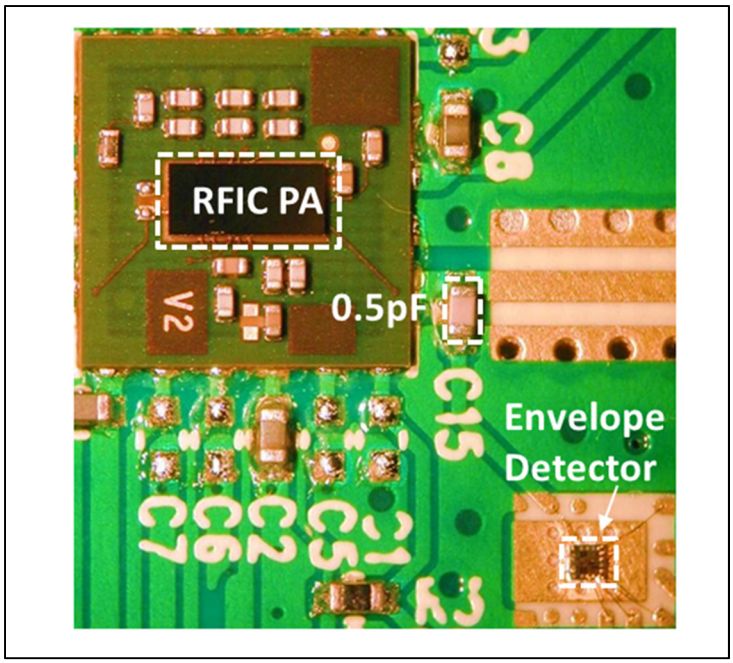

Figure 3.12 Photograph of prototype dual-IC module shown in Figure 3.11

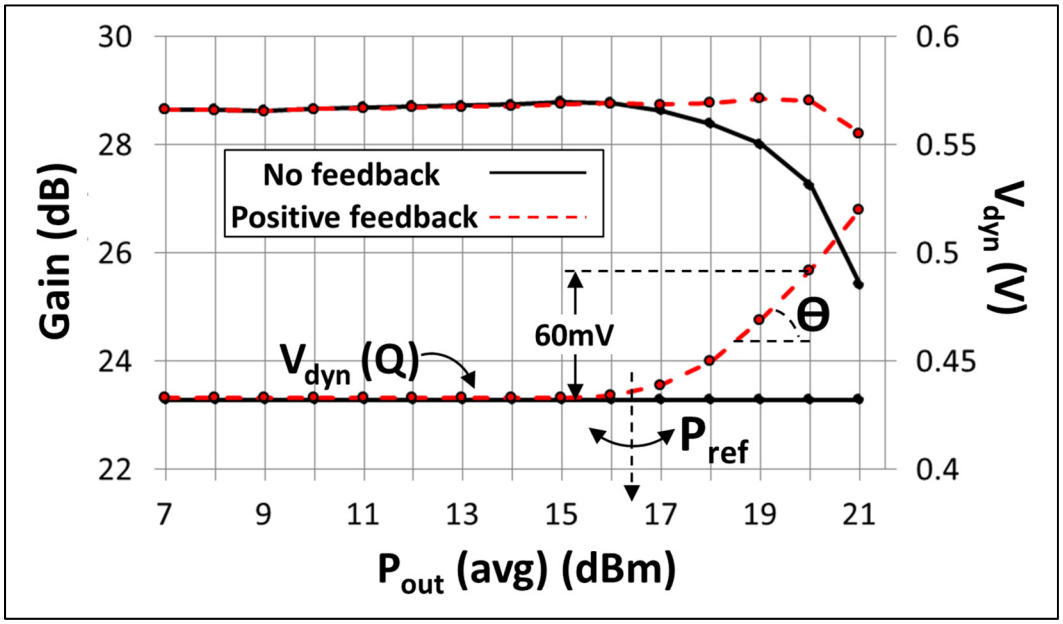

Figure 3.13 *Gain* vs. P_{out}, V_{dyn} vs. P_{out} under CW excitation. The quiescent value of the V_{dyn} signal $V_{dyn}(Q)$, the detector's sensitivity P_{ref} and the detector's gain conversion slope Θ are also indicated

As also shown in Figure 3.13, to achieve this improved AM-AM, only a 60mV increase of the gate-bias signal V_{dyn} at P_{out}=20dBm, from its quiescent value $V_{dyn}(Q)$ at low output powers, is adequate. It is worthwhile to note that such a small 60mV increase in the value of the gate bias is not significant enough to cause a drastic change in the class AB PA transistors' operation regime, such as a change from saturation to triode. The occurrence of such a drastic change in the PA transistors' operation would have also been captured as an excessive gain collapse/expansion in the PA's *Gain* vs. P_{out} plot shown in Figure 3.13. Figure 3.14 shows the PA's AM-AM under 2-tone excitation at 5.4GHz using a 100kHz frequency spacing, with and without positive envelope feedback. PA performance using two different V_{dyn} biasing profiles (1 and 2) through positive envelope feedback are shown, the two different profiles being set by adjusting the detector sensitivity P_{ref} and gain conversion slope Θ. The corresponding IMD_3 vs. P_{out} using V_{dyn} profile 1 under positive envelope feedback is given in Figure 3.15, and translates into an improvement of up to 3.44dB and 1.76dB for IMD_{3lo} and IMD_{3hi} respectively, for P_{out} levels from 17dBm to 20dBm. Although this IMD improvement is moderate for this prototype, it demonstrates that the technique improves the PA's overall linearity performance at its higher range of power levels while requiring only minimal additional circuitry and power consumption.

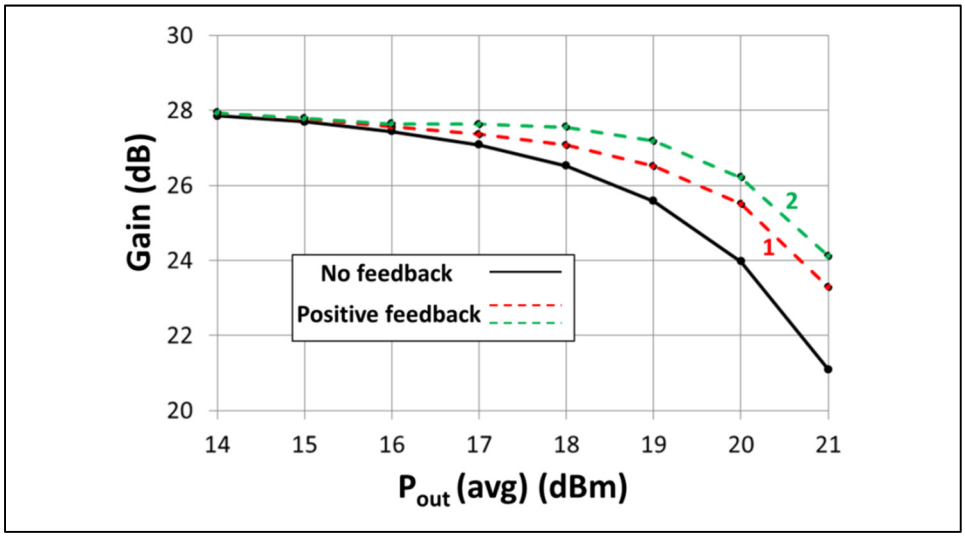

Figure 3.14 *Gain* vs. P_{out} under 2-tone excitation, with constant gate bias and two different V_{dyn} profiles (1 and 2) using positive envelope feedback

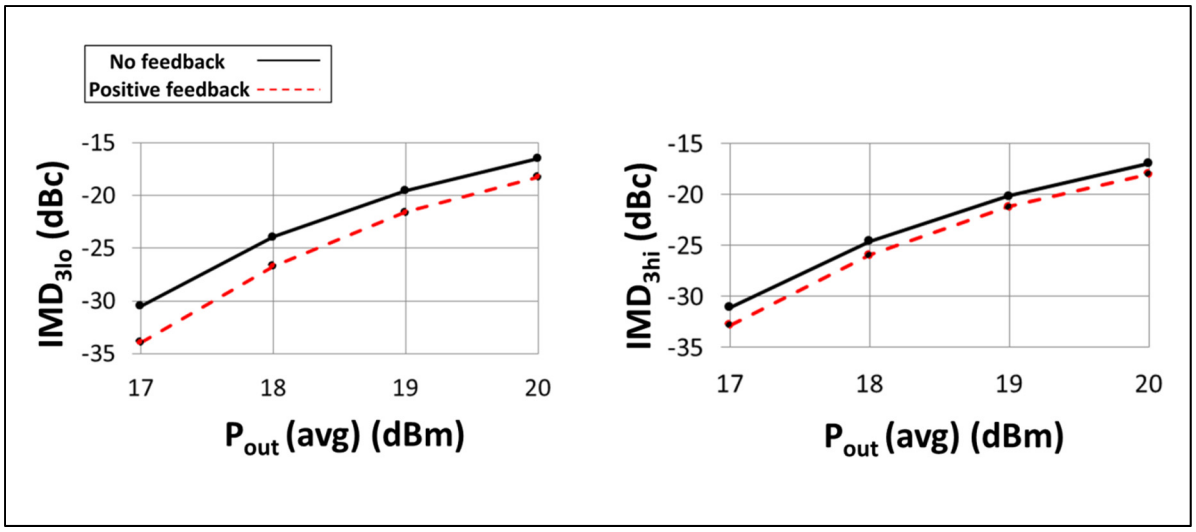

Figure 3.15 IMD_3 vs. P_{out} under 2-tone excitation, with constant gate bias and with positive envelope feedback corresponding to "1" in Figure 3.14

The corresponding *PAE* vs. P_{out} plot in Figure 3.16 shows that there is minimal effect on PA efficiency due to positive envelope feedback; in fact, a slight increase in the measured PAE may be observed. This improvement may be attributed to the following: the increasing excursions of the V_{dyn} signal for increasing envelope values of the PA's transmitted signal results in a slight increase in the average current of the PA's power-stage and therefore its gain. Consequently, for the same value of the PA's P_{out}, a lesser input drive is required for the PA's power-stage under positive envelope feedback, and the average current in the preceding driver-stage of the PA is therefore lower. The resulting lower P_{dc} and lower P_{in} values translate into a slightly higher PAE for the PA under positive envelope feedback, while delivering a certain level of average output power P_{out}.

Therefore, such an improvement in the PA's linearity for its higher range of power levels using positive envelope feedback, without any significant increase in its quiescent power consumption, leads to an overall enhancement of its linearity-efficiency trade-off.

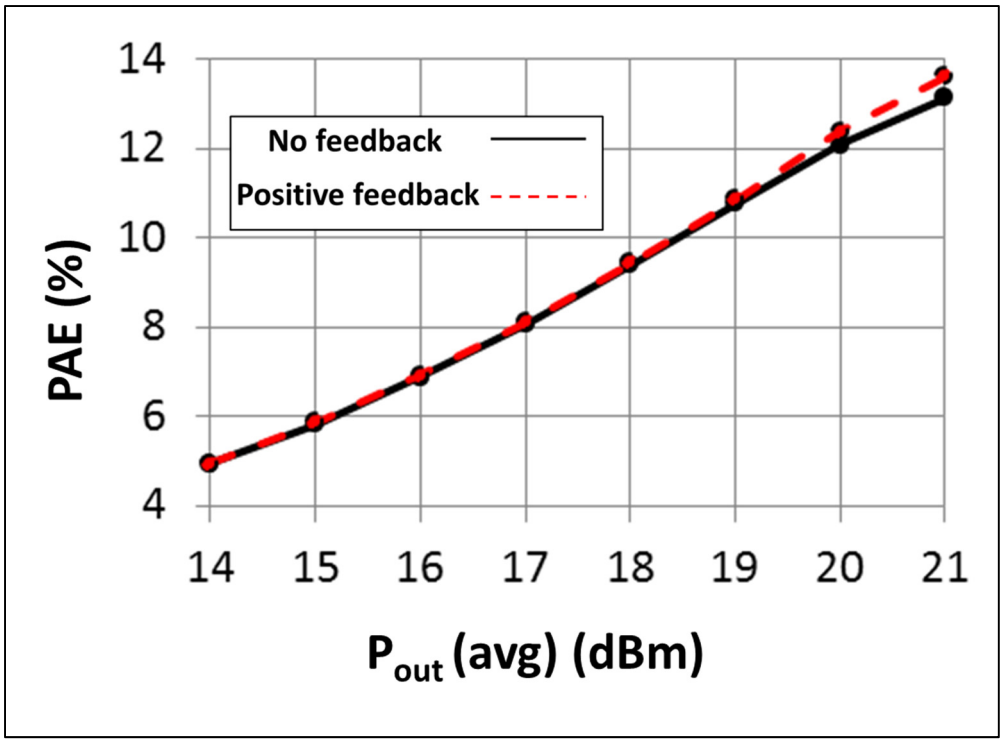

Figure 3.16 *PAE* vs. P_{out} under 2-tone excitation, with constant gate bias and with positive envelope feedback corresponding to "1" in Figure 3.14

3.2.3 Limitations of prototype DUT

In this proof-of-concept prototype, the large gate-source capacitance C_{gs} of the PA's power-stage transistor (Figure 3.11), compounded by 5kΩ on-chip gate resistance initially required for investigations on biasing, introduces unwanted AM-PM as a function of the dynamic-bias signal V_{dyn} under positive envelope feedback. Such AM-PM reduces the linearization effects of AM-AM compensation through the proposed technique of positive envelope feedback. This on-chip structure also dictated the 100kHz frequency spacing restriction of the 2-tone excitation in Figure 3.15 for this proof of concept, as a means to eliminate the AM-PM effects on linearity. Careful circuit design techniques allow overcoming these limitations, as evidenced by the results for a modified PA design presented in Section 3.2.4.

3.2.4 Simulations of modified design

Upon replacing the power-stage 5kΩ gate resistors in the design shown in Figure 3.11 with off-chip 15nH inductors, the *RC* time-constant overloading the dynamic biasing function V_{dyn} is removed. This replacement enables an improved AM-AM compensation over a much larger bandwidth, as demonstrated with the help of simulation results shown next.

The modified PA design that includes these 15nH inductors is now simulated using the harmonic balance (HB) simulator in ADS™ software. The simulation results with a 2-tone excitation at 5.4GHz and 10MHz frequency spacing are shown in Figure 3.17. The improved *Gain* vs. P_{out} profile (compared to the constant gate bias) in Figure 3.17(a) using positive envelope feedback translates into an IMD_3 improvement of up to 3.5dB for output power levels higher than 21dBm, as shown in Figure 3.17(b). As explained in (Chengzhou, Vaidyanathan, & Larson, 2004) and also in Section 3.1.6, the contribution to PA output nonlinearity from the PA's gain compression is predominant over nonlinear C_{gs} effects for this higher range of PA output power levels, and the reduced signal clipping from positive envelope feedback therefore results in the significant linearity improvement as shown. For conciseness, note that only IMD_{3lo} values are shown in Figure 3.17(b) since the simulated IMD_{3hi} profile closely follows the IMD_{3lo} profile.

Figure 3.18 and Figure 3.19 shows the PA's output linearity improvement using positive envelope feedback in terms of Adjacent Channel Power Reduction (*ACPR*) values, when the PA is excited using a modulated RF signal. The excitation used is an RF carrier modulated by a Forward Link CDMA signal with a signal bit-rate of 1.2288MHz, with 4 samples/bit and 256 total number of symbols. It is generated using the *PtRF_CDMA_IS95_FWD* component in the *Sources-Modulated* library in ADS™. *ACPR* improvement of up to ~6dB is achieved using positive envelope feedback for PA output power levels higher than 19dBm.

To further illustrate this improvement in PA linearity, the transient form of the V_{dyn} signal as well as the PA's output signal V_{out} that is delivered to the load is shown in Figure 3.20, at an

average output power level P_{out} =19dBm. The reduction in signal clipping of V_{out} under positive envelope feedback, compared to the PA under constant gate bias, for the upper range of envelope power levels translates into the improved PA linearity shown.

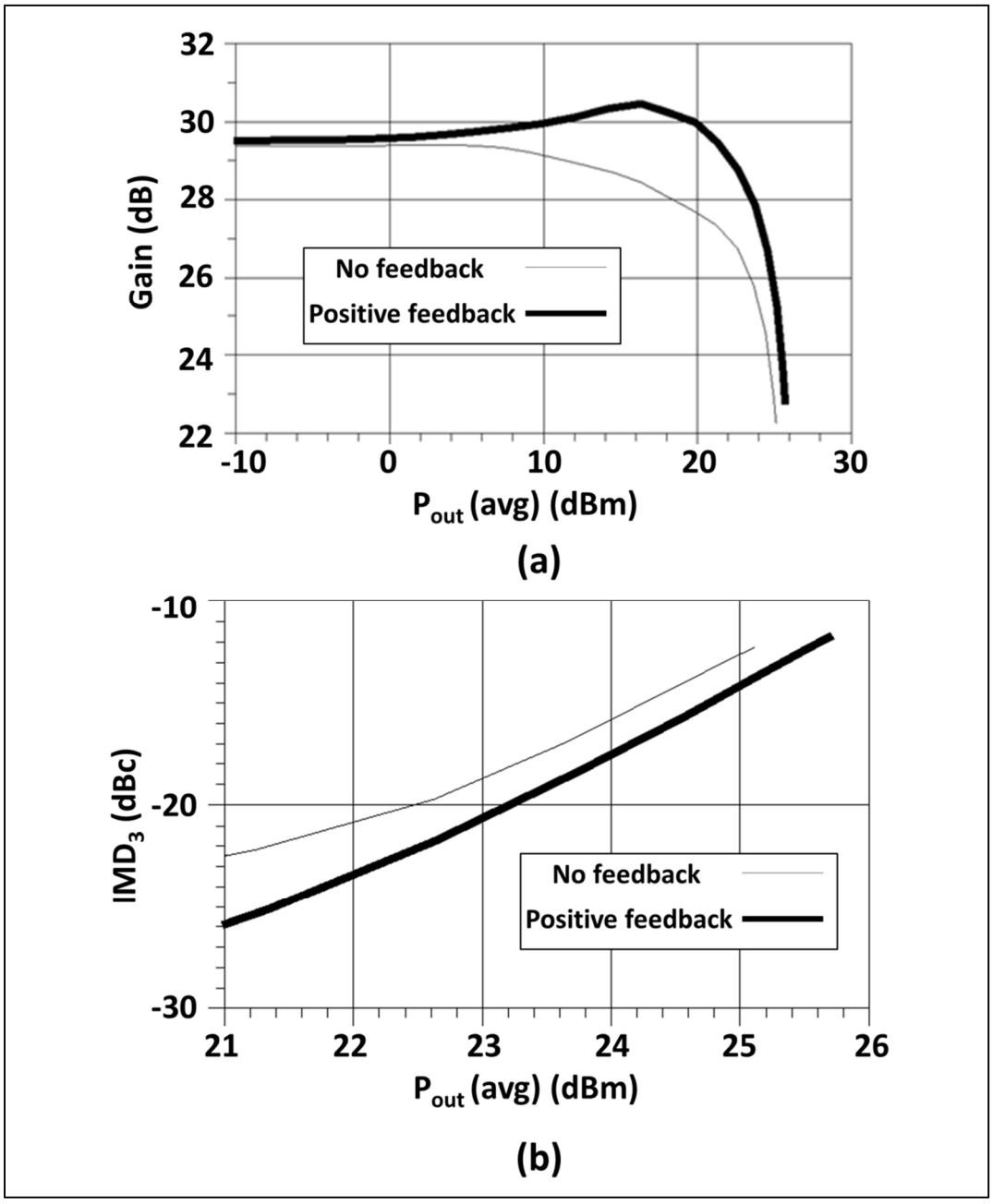

Figure 3.17 (a) Simulated *Gain* vs. P_{out} and (b) corresponding IMD_3 vs. P_{out} for 2-tone excitation at 5.4GHz, 10MHz spacing, with the modified design

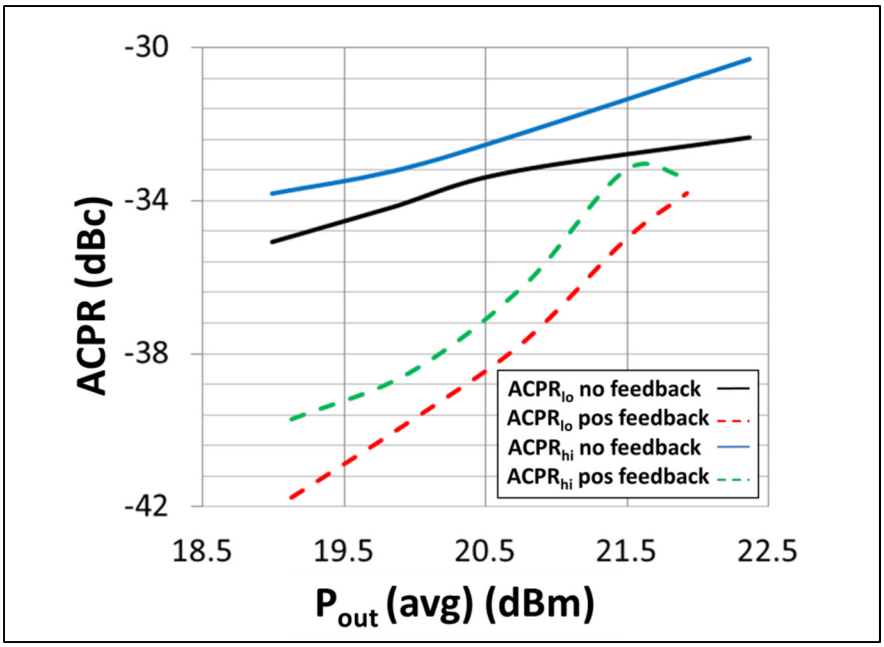

Figure 3.18 *ACPR* vs. P_{out} under modulated excitation, with constant gate bias and using positive envelope feedback

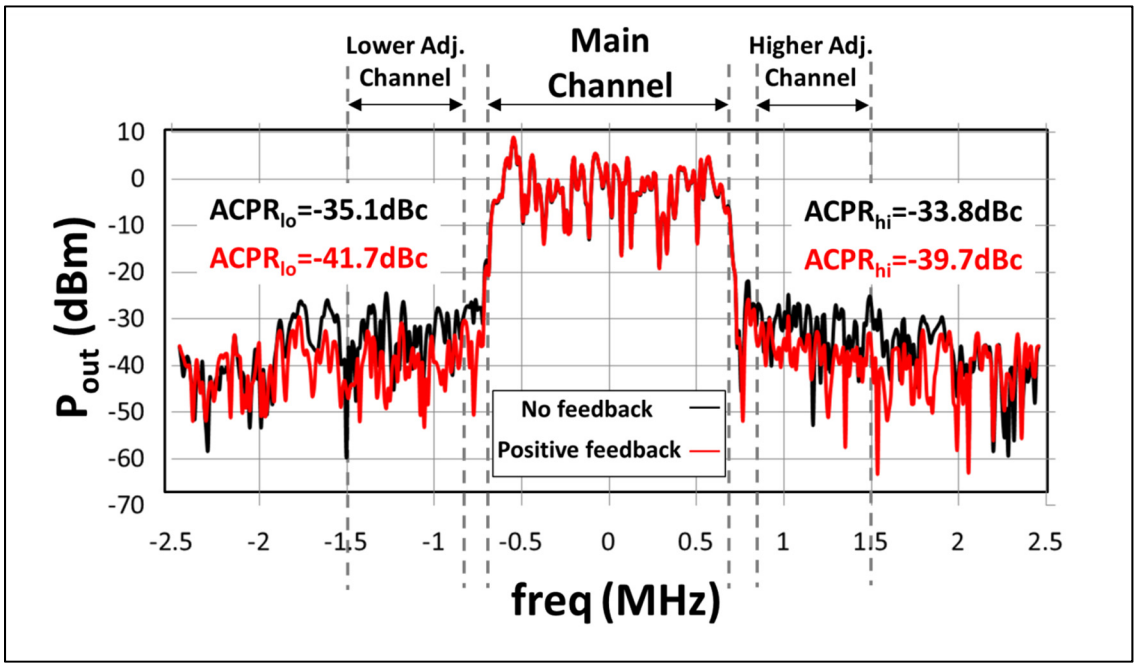

Figure 3.19 PA output frequency spectrum showing ACP levels under modulated excitation at P_{out}=19dBm, with and without positive envelope feedback

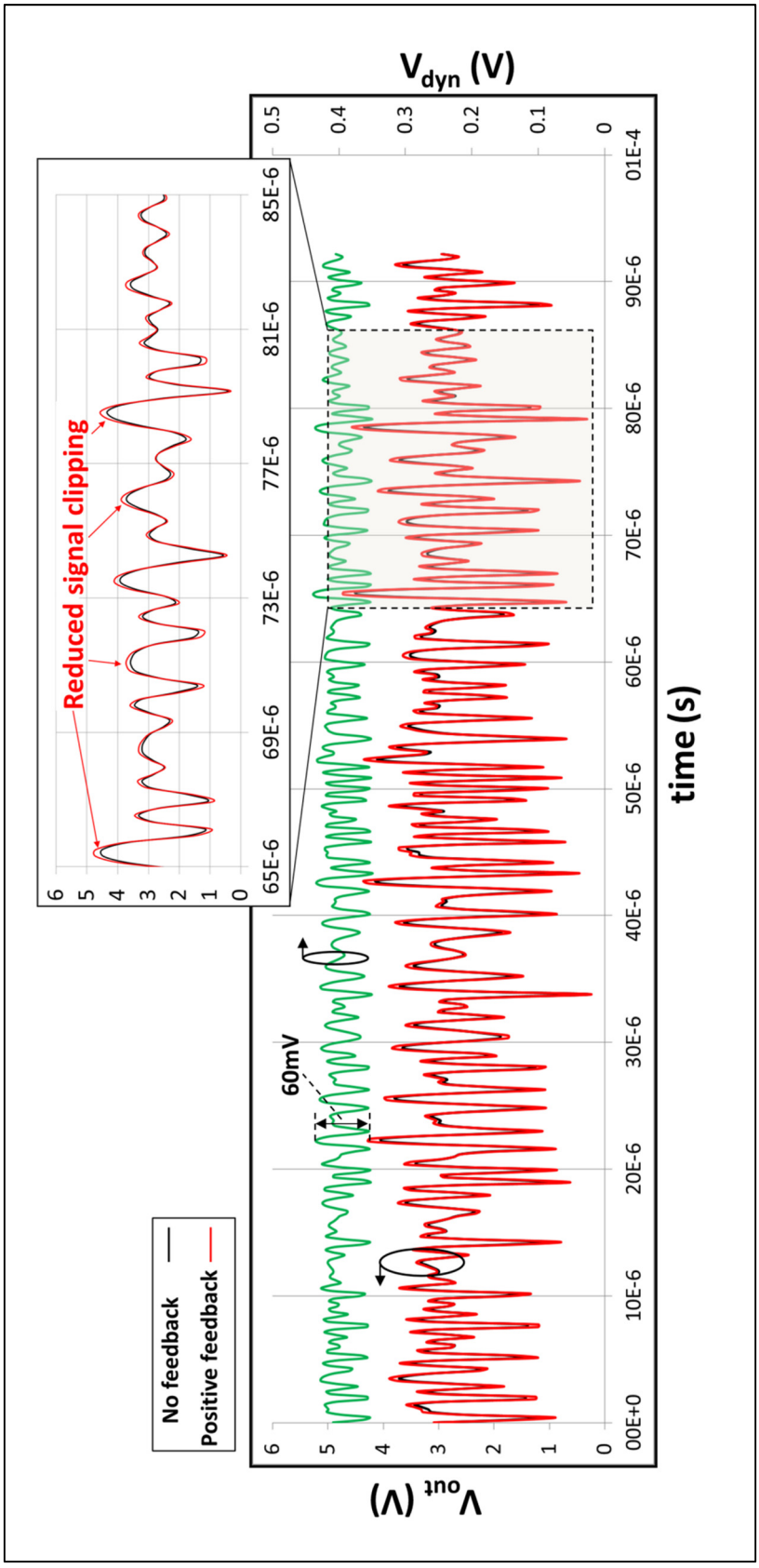

Figure 3.20 Transient V_{out} voltage signal, with and without positive envelope feedback, at $P_{out}(average)$=19dBm. The corresponding V_{dyn} signal under positive feedback is also shown, and has a maximum swing of ~60mV
Observe the reduced signal clipping of V_{out} under positive envelope feedback

Table 3.1 Simulated noise power for P_{out} =23dBm

	Noise Power (dBm) at ±Offset (Hz) from Carrier					
	-50MHz	*-30MHz*	*-20MHz*	*+20MHz*	*+30MHz*	*+50MHz*
Constant bias	-147.2	-146.4	-145.2	-144.7	-146.0	-146.8
Positive feedback	-146.2	-145.3	-143.8	-143.2	-144.8	-145.8
Δ (dB)	**1.00**	**1.10**	**1.40**	**1.50**	**1.20**	**1.00**

Noise simulation results of the PA design confirm that the proposed technique of positive envelope feedback does not significantly degrade PA output noise performance. Simulation results of noise performance on the same modified PA design, with and without positive envelope feedback, are shown in Table I. These performances are comparable to the requirements for a cellular Frequency division duplex (FDD) system, with the receiver (R_x) channel at ±20MHz to ±50MHz frequency offset from the transmitter (T_x) carrier. Such an FDD system represents a stringent test-case since the R_x offset frequencies lie within the PA's bandwidth where T_x gain is intended. As shown in Table 3.1, only a slight degradation in output noise power levels under positive envelope feedback is observed at the output power level of 23dBm, despite the positive envelope feedback loop being fully operational at this high power level. This slight degradation is a result of the increased bias level V_{dyn} and consequent increase of the PA's RF gain under positive envelope feedback as explained in Section 2.2.4, and may be expected of any PA technique that relies on improving the PA's AM-AM for linearity through dynamic biasing.

It is worthwhile to note that there is a discrepancy between the PA output power levels where positive envelope feedback improves linearity when comparing the experimental measurements in Figure 3.13-3.15 with the simulation results of the modified design in Figure 3.17-3.18. Such a discrepancy is because the simulation results obtained using the device models for the latter are slightly offset from actual experimental measurements in the lab. However, nearly identical trends with regard to linearity improvement using positive

envelope feedback are observed for both experimental measurements as well as from circuit simulations. Additionally, for the simulation results of the modified design, there is a shift of ~2.5dB in the range of output power levels where positive envelope feedback results in IMD_3 improvement in Figure 3.17(b) and *ACPR* improvement in Figure 3.18. This shift is due to the ~2.5dB difference in the peak-to-average power ratio (PAPR) between the case of two-tone and the case of modulated excitation, used for the IMD_3 and *ACPR* measurements respectively. The higher PAPR of the modulated excitation also results in higher PA output nonlinearity due to signal clipping compared to the 2-tone excitation, at the same value of the average output power. The reduced signal clipping with a modulated excitation translates into an increased effect in terms of signal waveform correction (Figure 3.20), therefore yielding a slightly higher linearity improvement (with respect to constant gate bias) under modulated excitation compared to the 2-tone excitation, as may be observed from Figure 3.17 and Figure 3.18. Such a beneficial effect in a weakly nonlinear system relates to the "sweet spot" phenomenon sometimes referred to in the literature (e.g. (Pedro, Carvalho, Fager, & García, 2004)).

It is also useful to point out that all PA performance improvement implementations demonstrated in this thesis use positive envelope feedback for dynamically biasing the power-stage transistors only. Further improvement may be expected by using positive envelope feedback for dynamically biasing the PA's driver-stage in addition to the power-stage as described in (Sharma & Constantin, April 2018) as well as Chapter 5 of this thesis, and requires more investigation.

3.3 Summary: Design and implementation of positive envelope feedback

Based on the simulation results presented in Section 3.1 and the experimental measurements given in Section 3.2, we can now make several observations and draw some useful conclusions regarding the design and implementation of positive envelope feedback. These are presented below. In the same summary, we also correlate the design conditions summarized previously in Table 2.1 with practical values obtained via simulation and experimental measurements in Chapter 3.

- **Observation**: Drain-source shorted PMOS device connected to PA NMOS gate is effective for PA linearization only at moderate power levels.

  This technique of PA linearization is based on linearizing the variation of the input capacitance C_{in} seen looking into the PA's power-stage input. Though extremely useful at moderate power levels, it is not adequate for improving linearity at higher output powers, when amplitude distortion due to drain-current clipping becomes the dominant source of PA nonlinearity and translates into gain compression at the PA output.

  A reduction in the PA's RF gain is also observed due to the increased value of the PA's input capacitance to $C_{in}=C_{ggn}+C_{ggp}$, instead of $C_{in}=C_{ggn}$ only without the PMOS compensation. For example, for the simulation example described in Section 3.1, the PA without PMOS compensation has a C_{in} varying from ~3.5pF to ~6.5pF as shown in Figure 3.9. On the other hand, the PA with PMOS compensation has an increased C_{in} of ~10.75pF, resulting in lower RF gain.

- **Observation**: Sensitivity and gain conversion slope of the envelope detector are critical parameters for ensuring PA stability and optimizing PA linearity through positive envelope feedback.

  In the PA designs shown in Chapter 3, facilities are made for explicit off-chip control signals (V_a and V_b) that allows tuning the detector profile (and hence the profile of the dynamic-bias signal generated through positive envelope feedback) for optimum PA linearity while maintaining PA stability. The values of the detector sensitivity and gain conversion slope that are used is illustrated in Figure 3.3 and Figure 3.13.

  A useful way of experimentally arriving at a first approximation of the values of V_a and V_b to be used for dynamic biasing through positive envelope feedback is by determining their values that allow flattening the PA's CW *Gain* vs. P_{out} profile. Once these values are known, the PA is excited with a 2-tone excitation and the values of control signals V_a and

V_b are manually adjusted till optimum linearity (in terms of IMD_3) at the desired output power level is reached.

In Chapter 4, a more methodical procedure to determine the values of V_a and V_b - based on formulations of a novel analytical PA representation - will be presented, eliminating the need to rely only on trial-and-error to arrive at these values.

- **Observation**: Quiescent current consumption of the PA system is negligibly affected by the implementation of positive envelope feedback.

  The quiescent current consumption of the PA system is minimally affected due to the implementation of positive envelope feedback. While the quiescent current consumption of the transistors in the PA line-up itself remains unchanged due to the use of identical DC quiescent-bias voltage V_{GG0} for both without and with positive envelope feedback, the envelope detector presents an additional source of current consumption for the latter. However, it is shown that this additional current consumption is negligible - for the PA systems in Section 3.1 and Section 3.2, the current consumption of this envelope detector is only 3.6% and 1.2% respectively of the total system current consumption. Note that the envelope detector's share of the total system current consumption reduces as the number of stages in cascade that constitute the RFIC PA increases, which itself is a function of the overall RF gain that is required of the RFIC PA. For example, the gain of the PAs in Section 3.1 and Section 3.2 are ~17.5dB (2-stage PA) and ~29dB (3-stage PA) respectively as shown in Figure 3.4 and Figure 3.13, while the respective shares of the envelope detector's current consumption are 3.6% and 1.2% as stated earlier.

  On the other hand, the improved linearity at higher power levels under positive envelope feedback and the equivalent DC power savings translates into an overall improved PA linearity-efficiency trade-off. In fact, as shown in Figure 3.16, the PAE may even be slightly improved under positive envelope feedback.

- **Observation**: The maximum voltage swing of the dynamic-bias signal that is required to linearize the PA through positive envelope feedback is in the order of ~100mV.

  The maximum voltage swing of the dynamic-bias signal to linearize the PA's gain (and avoid output-signal clipping) is relatively small – this swing required for the example in Section 3.1 is shown to ~75mV in Figure 3.4, while it is found to be ~60mV for the example in Section 3.2 as shown in Figure 3.13. It is possible to achieve such a dynamic voltage swing (over the 5dB to 6dB power range where the PA is under gain compression) with an adequately small loop gain, which ensures that the PA's stability and noise performances are not compromised under positive envelope feedback. Such a low bias voltage swing also ensures that the PA does not experience any drastic change in its class of operation which can result in unwanted signal distortion at the PA output.

- **Observation**: Linearity improvement in terms of IMD_3 under positive envelope feedback is in the order of 2.5dB to 4.5dB when the PA is under gain compression.

  The IMD_3 improvement under positive envelope feedback, compared to the PA under constant bias, is found to be in the order of 2.5dB to 4.5dB. This improvement is illustrated in Figure 3.5, Figure 3.6 and Figure 3.15. While such a demonstrated linearity improvement is moderate, it is essential to note that the circuit overhead required to implement positive envelope feedback – circuit complexity, additional power consumption and additional circuit area – is negligible.

  Also, the improvement in PA linearity under positive envelope feedback is more significant when the excitation signal used has a larger PAPR, such as the CDMA-modulated signal used for Figure 3.8 and Figure 3.18. This increased linearity improvement arises from the fact that at any particular value of the PA's average output power when it is under compression, a signal with a larger PAPR experiences greater signal clipping under constant bias and, therefore, the reduced signal clipping under positive envelope feedback translates into a higher degree of linearity improvement. As

may also be seen by comparing the linearity improvement shown in Section 3.1 and Section 3.2, the exact level of linearity improvement under positive envelope feedback depends on the intrinsic nonlinearities of the specific PA design; however, the same trends and degree of linearity improvement are identified.

- **Observation**: With a few careful design considerations, positive envelope feedback is suitable for linearizing PAs transmitting very large bandwidth signals.

  Careful design practices are essential to ensure that any low-pass filter structure does not inadvertently restrict the feedback loop. Such a limitation was encountered in the experimental prototype of Section 3.2; however, it was shown that by replacing the large 5kΩ DC gate-bias resistors with 15nH RF choke inductors as described in Section 3.2.4, the bandwidth limitation of the PA could be removed.

  Additionally, the simulated delay values listed in Section 3.1.7 for the 1.9GHz PA of Section 3.1, as well as for another 28GHz PA, illustrate the potential of using the proposed technique for PAs transmitting very large bandwidth signals, such as those envisaged for mm-wave PAs aimed at 5G mobile applications.

- **Observation**: PA output noise performance is minimally affected by the implementation of positive envelope feedback.

  Table 3.1 shows that PA noise performances are minimally affected by the implementation of positive envelope feedback. The slight degradation of the already extremely low values of the PA's output noise power levels is a result of an increased overall RF gain of the PA due to positive envelope feedback, and may be expected of any PA linearity improvement technique that relies on linearizing its AM-AM. There is no catastrophic noise degradation due to the PA's output noise being injected back into the PA transmit chain through its bias node, since the substantial attenuation through the envelope detector and the resistive voltage divider ensures that the PA's output noise is

reduced to insignificant levels in the dynamic-bias signal. These results also confirm the theory regarding PA noise performance under positive envelope feedback that was presented in Section 2.2.4.

CHAPTER 4

INTRODUCING EMBEDDED SELF-CALIBRATION OF PAS UNDER DYNAMIC BIAS USING NOVEL MULTI-PORT ANALYTICAL PA REPRESENTATION

> "Science, however, is never conducted as a popularity contest, but instead advances through testable, reproducible, and falsifiable theories."
>
> Michio Kaku

In Section 4.1 of this chapter, a method for embedded self-calibration of the PA within the mobile unit is introduced, for compensating the PA's dynamic bias against part-to-part variation. The proposed method for embedded self-calibration uses a novel multi-port analytical PA representation for nonlinear processing of the PA's input and dynamic-bias signals. This novel multi-port representation is presented in Section 4.2, and a more specific case of a 3-port analytical PA representation for representing a PA under dynamic gate bias is discussed in detail in Section 4.3. This novel 3-port representation is based on a distinct signal flow that uses a combiner, a nonlinear baseband-to-RF converter and a nonlinear amplifying function, for the nonlinear processing of the PA's dynamic-bias signal. In Section 4.4 and Section 4.5, some examples that highlight the application of the proposed analytical representation for embedded self-calibration of PAs during operation of the mobile equipment are discussed, and also for PA linearization under multi-tone as well as modulated input RF excitation. The proposed analytical PA representation also allows, for the first time to the best of the author's knowledge, describing closed-loop PA operation under feedback using closed-form formulations. These formulations enable determining the design requirements of the feedback system components to ensure the stability of the closed-loop PA system, without relying solely on trial-and-error to optimize the values of the loop elements. This aspect of the application of the presented analytical representation is treated in Section 4.7, and also discussed further in Section 4.8.

4.1 Introducing embedded self-calibration of PAs

The principle of dynamic biasing plays an essential role in the design of many RFIC PA architectures. As described in Section 1.1.2, typical implementations of dynamic biasing involves variation of the bias signal of the PA's RF transistors around its quiescent DC level as a function of a control signal, to improve the linearity-power efficiency trade-off. Such a control signal may be a function of the PA's average power level or its instantaneous power level. For example, dynamic biasing as a function of the average RF power level is used to improve the power-added efficiency (PAE) of RF amplifiers in (Lau, Xue, & Chan, 2007; Miers & Hirsch, 1992; Nam & Kim, 2007; Sahu & Rincon-Mora, 2007) and for PA gain regulation and efficiency optimization in (Forestier et al., 2004). Various open-loop and feed-forward implementations illustrated in (Constantin, May, 2010; Deltimple, Leyssenne, Kerhervé, Deval, & Belot, 2010; Medrel et al., 2013; Tafuri, Sira, Jensen, & Larsen, 2013; Po-Chih et al., 2008; Onizuka, Ikeuchi, Saigusa, & Otaka, 2012) use a dynamic-bias signal varying as a function of the PA's envelope power level to improve PA performances. The proposed positive envelope feedback technique described in Chapter 2 and Chapter 3 of this thesis demonstrates the use of instantaneous dynamic biasing in a closed-loop system to improve the linearity-efficiency trade-off of PAs. (Kang, Baek, & Hong, 2017) shows the use of active FET elements to provide dynamic feedback aimed at compensating the PA's gain compression at high power levels. Examples of closed-loop systems that use dynamic feedback are not limited to PAs. Designs in (Thangarasu, Ma, & Yeo, 2017; El-Shennawy, Joram, & Ellinger, 2016) are examples of variable gain amplifier (VGA) implementations that rely on closed-loop negative feedback for gain control.

The PA's response to an envelope varying RF signal in the above implementations is governed by complex nonlinear mechanisms, and dynamically changing the PA's bias as a function of the envelope adds further complexity to the PA's response. Moreover, the increasingly complex front-end PA modules in mobile transmitters may make use of different hardware states as part of a hardware reconfiguration scheme (e.g. (Joung, Ho, & Sun, 2013)). Such complex mechanisms inevitably introduce variations in the PA performances

from one mobile unit to another. In this context, a self-calibration technique embedded within the mobile unit that would allow optimizing the dynamic biasing after taking into account the performance variation from one unit to another would be of interest for current and future mobile wireless equipment.

An example where embedded self-calibration would be useful is when the PA is subjected to dynamic biasing through the modulation of the gate bias as a function of the PA's envelope (Sharma, Constantin, & Soliman, 2017; Kang, Baek, & Hong, 2017) to improve the PAE-linearity trade-off. Positive envelope feedback, as described in Chapter 2-3 of this thesis, is one such implementation. Embedded self-calibration within the mobile unit would then allow performing the necessary adjustments (e.g. in the case of positive envelope feedback, the value of the envelope detector's sensitivity and gain-conversion slope) on each PA to reduce the spread in performance from one mobile unit to another, hence ensuring the best PAE-linearity trade-off in every mobile unit.

To the best of the author's knowledge, a method specifically for embedded self-calibration of envelope-dependent dynamic biasing in a PA module within a mobile unit during operation has not been reported. Figure 4.1 shows the embedded RF front-end self-calibration application that is envisioned in this thesis. Here, the control signal V_{ctrl} determines the value of the PA's dynamic-bias signal to be used at a particular power level and its value is computed using a sufficiently accurate analytical PA representation (X in Figure 4.1). X (and hence the value of V_{ctrl}) is adjusted from one mobile unit to another starting from a minimum number of quasi-static power measurements over a narrow power range only, using simple interfacing circuits identified as *Input Probe* and *Output Probe* (the design of the probes themselves being not addressed in this thesis). Additionally, as shown in Figure 4.2, the *Input Probe* may not even be required in the case where the input envelope power information is derived directly from the baseband chipset within the mobile unit's baseband processor. In this and other contexts (discussed further in Section 4.8) that would require self-calibration, a simple analytical PA representation X which accounts for a sufficiently high order of PA nonlinearity, which is straightforward to extract and store and which is suitable for

embedding into mobile equipment for self-calibration (hence excluding commercially available tools/software) offers exciting possibilities.

Our novel multi-port analytical PA representation that is proposed to be used for embedded self-calibration is now introduced. As will be shown, unlike the analytical PA representations described in Section 1.3 and summarized in Table 1.2, this representation satisfactorily answers all the requirements necessary for the implementation of embedded self-calibration within the mobile unit.

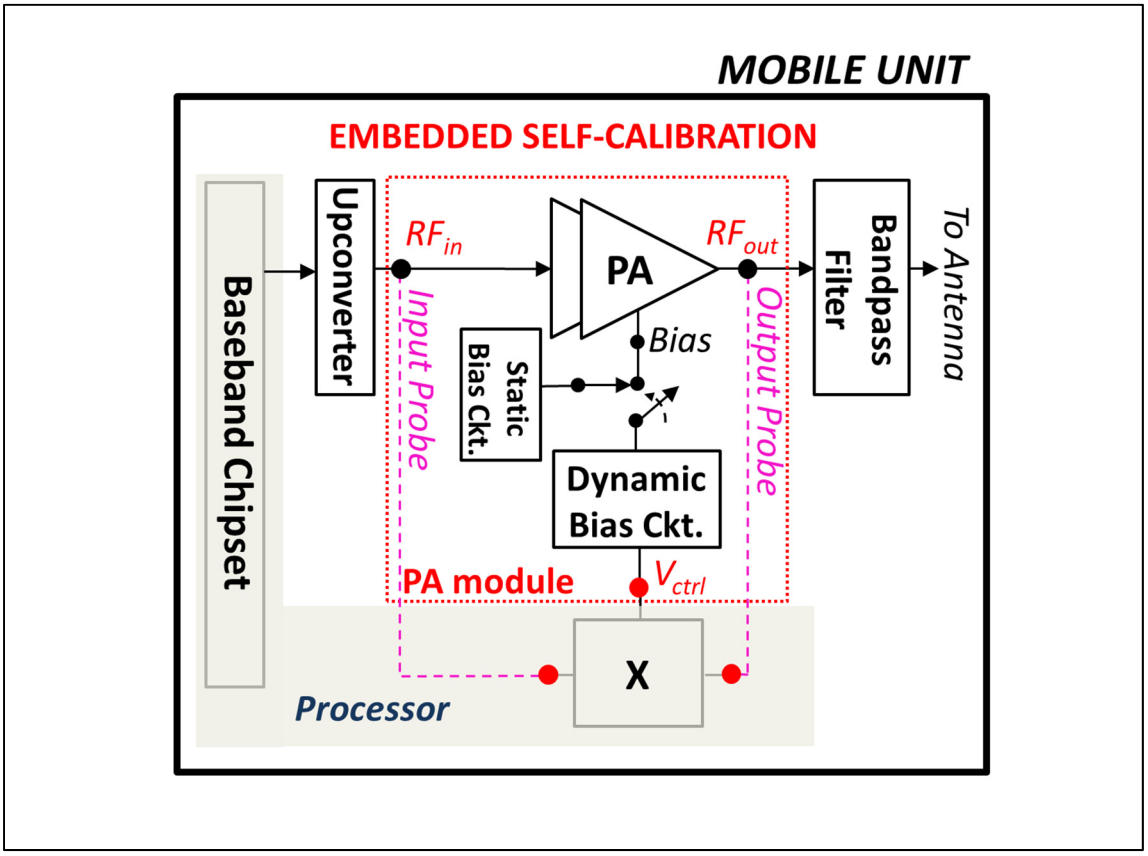

Figure 4.1 Proposed embedded self-calibration technique within the mobile unit in the RF front-end using the PA representation X. The control signal V_{ctrl} is synthesized using X and determines the value of the dynamic-bias signal at different power levels. The input and output probing for self-calibration from unit to unit need to only measure quasi-static input and output power over a narrow power range

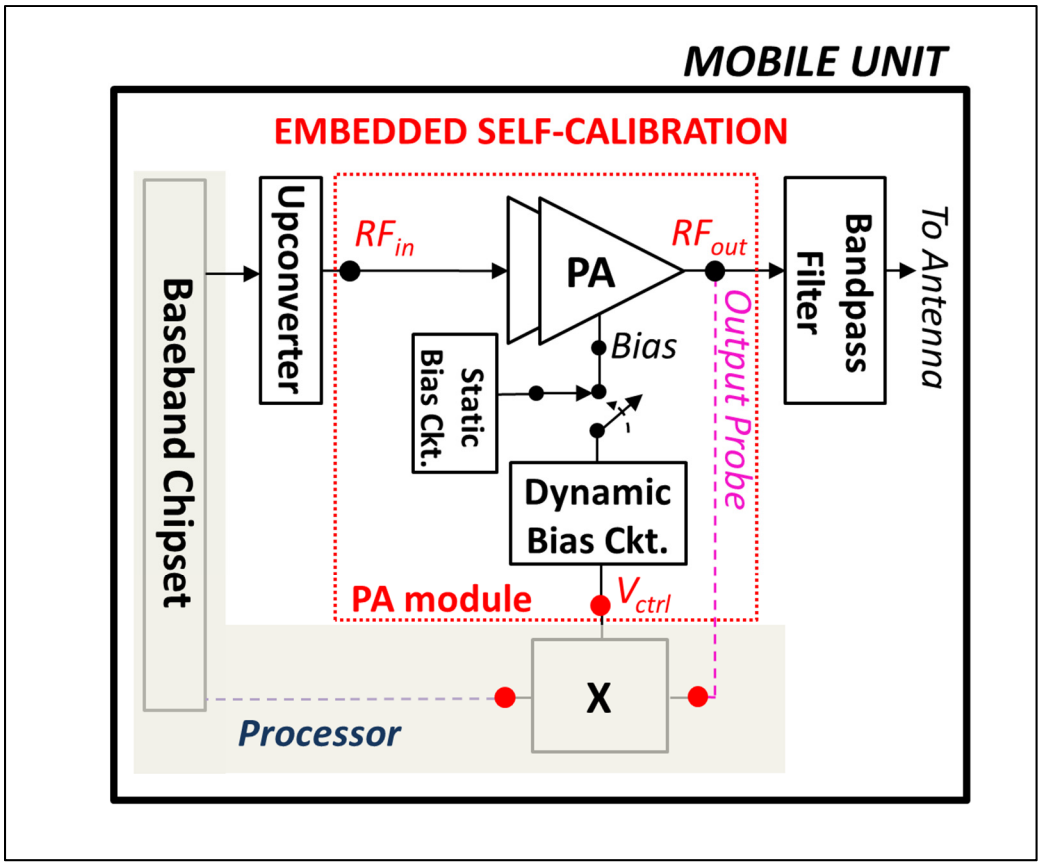

Figure 4.2 A second example of the proposed embedded self-calibration technique within the mobile unit shown in Figure 4.1. The input probe is not required in this implementation, and *X* instead relies on the baseband chipset within the mobile unit's processor to determine the input power to the PA

4.2 Multi-port analytical representation of PAs under dynamic bias

Figure 4.3(a) represents the multi-port analytical representation of PAs under dynamic bias that is proposed in this thesis. The representation comprises of n ports. Port 1 refers to the PA's input port that is excited by the input signal V_{in}. Port 2 refers to the PA's output port that delivers the output signal V_{out}. For example, V_{in} may refer to the PA's input modulated RF signal RF_{in} that is composed of an RF carrier modulated by a baseband signal, while V_{out} may refer to the PA's output modulated RF signal RF_{out}. As another example, V_{in} may refer

to the baseband signal BB_{in} from the transmitter's baseband chipset before being upconverted to RF and then injected into the PA transmit chain.

Besides the input and the output ports, the *n*-port analytical representation shown in Figure 4.3(a) consists of an additional (*n-2*) control ports. These are labelled *Port 3*, *Port 4* … *Port n-1*, *Port n* in Figure 4.3(a), and their respective signals are termed V_{ctrl3}, V_{ctrl4}, … $V_{ctrl(n-1)}$, $V_{ctrl(n)}$. Each of these (*n-2*) V_{ctrl} signals may be DC, baseband-dependent or RF-dependent signals. For example, in one such implementation, they may represent *n* different V_{ctrl} signals which correspond to *n* different envelope-dependent dynamic-bias signals applied to each of the gate/base terminals of an *n*-stage RFIC PA (the *n* stages being in cascade to each other). As another example, they may represent *n* different V_{ctrl} signals which correspond to *n* different envelope-dependent supply signals applied to each of the drain/collector terminals of an *n*-stage RFIC PA (the *n* stages being in cascade to each other). As yet another example, they may represent *n* different V_{ctrl} signals which correspond to *n* different envelope-dependent as well as DC signals that are applied to various gate/base terminals and drain/collector terminals of an *n*-stage RFIC PA (the *n* stages being in cascade to each other).

The *F* and *G* blocks in cascade, shown within the green dotted box in Figure 4.3(a), together capture the PA's input-to-output transfer function when all the supply and bias nodes of the PA are held at constant DC values, i.e. under quiescent supply and bias conditions. As will be shown in Section 4.3, *G* is a complex polynomial that accounts for the PA's nonlinear amplifying function under quiescent conditions. *F* may either be a constant value (scalar or complex), or a scalar-coefficient polynomial or a complex-coefficient polynomial. For example, in Section 4.3, it is sufficient to have *F* as a constant value. In the Conclusion chapter of this thesis, a case will be shown where *F* represents a complex-coefficient polynomial that performs a baseband-to-RF conversion and accounts for the signal conversion from the output of the baseband chipset to the input of the PA.

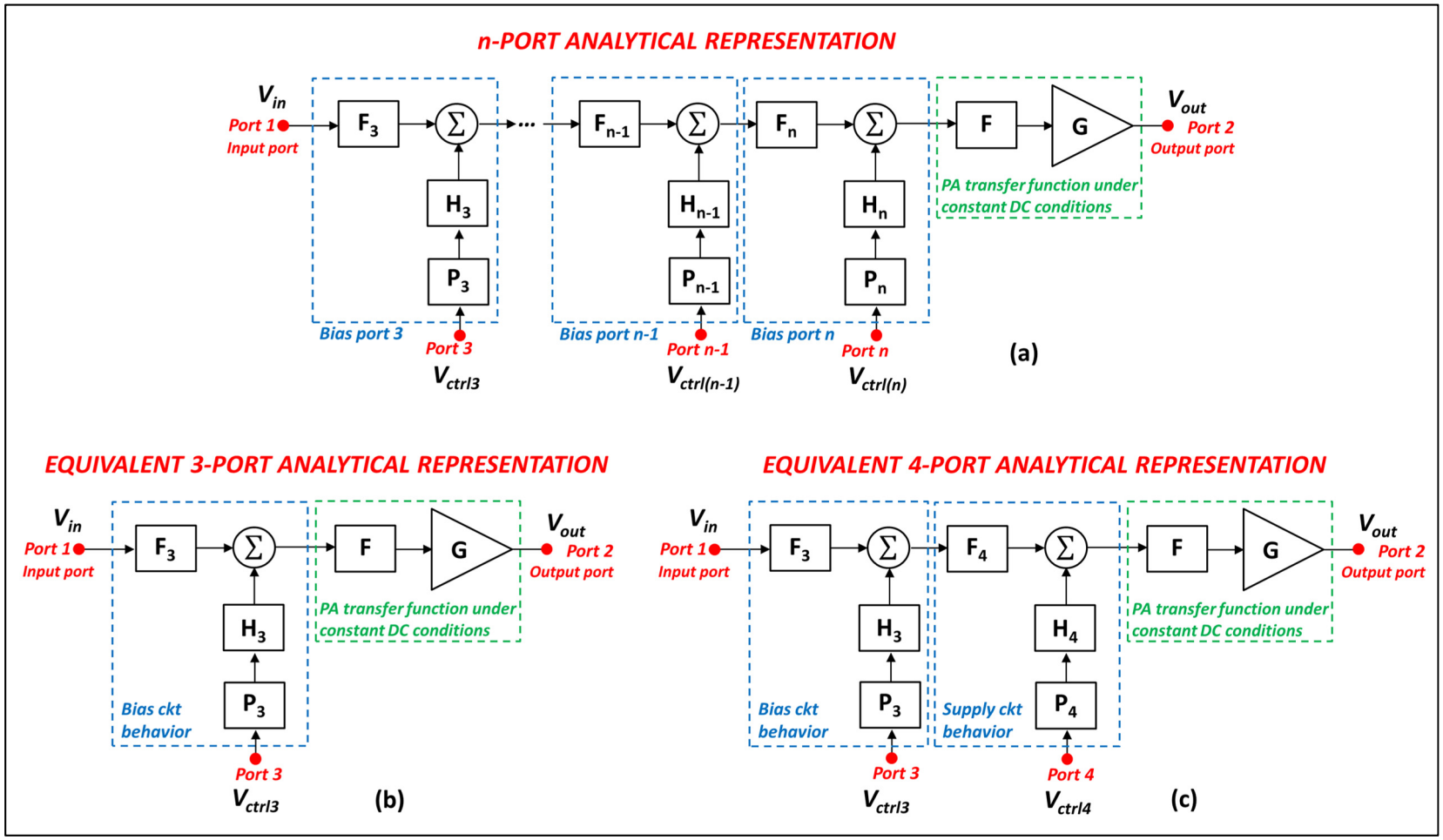

Figure 4.3 (a) Proposed multi-port analytical representation of PAs under dynamic bias (b) Equivalent 3-port representation (c) Equivalent 4-port representation

Shown within blue dotted boxes in Figure 4.3(a) are (*n-2*) sets of polynomials and combiners, where each set within a single blue dotted box is associated with one particular control port. The (*n-2*) sets are in cascade with one another. For instance, consider the control port 3. Associated with port 3 are three polynomials P_3, H_3 and F_3 in addition to a combiner. P_3, H_3 and F_3 are all polynomials that may either be linear or nonlinear, and with either scalar or complex coefficients. P_3 describes a polynomial function of signal V_{ctrl3}, the output of which is further processed by polynomial H_3. F_3 describes a polynomial function of the PA's input signal V_{in}. The combiner sums the signals at the output of the H_3 and F_3 polynomials, and the output of this combiner is itself provided as input to polynomial F_4 of the succeeding set of polynomials associated with control port 4.

For example, consider a multi-stage RFIC PA with a baseband dynamic-bias signal V_{ctrl3} applied to one of its gate/base terminals. For capturing the PA's performance under such dynamic biasing, the multi-port analytical representation shown in Figure 4.3(a) may be reduced to a 3-port representation (see Figure 4.3(b)), where port 3 is associated with the baseband dynamic-bias signal V_{ctrl3}. Port 1 and port 2 are associated with the PA's input signal V_{in} and output signal V_{out} respectively. P_3 is a complex polynomial describing a nonlinear baseband-to-RF conversion of the dynamic-bias signal V_{ctrl3}. H_3 and F_3 may either be complex polynomials or constants (e.g. a scalar value of 1 if H_3 and F_3 have no incidence). The outputs of H_3 and F_3 are summed using the combiner and directly applied as input to the cascaded polynomials F and G (within the green dotted box) to extract the PA's output signal V_{out} under dynamic biasing.

As another example, consider a multi-stage RFIC PA with a baseband dynamic-bias signal V_{ctrl3} applied to one of its gate/base terminals and a baseband supply modulation signal V_{ctrl4} applied to one of its drain/collector terminals. To capture the PA's performance under such dynamic biasing and supply modulation, the multi-port analytical representation shown in Figure 4.3 may be reduced to a 4-port representation (see Figure 4.3(c)), where port 3 and port 4 are associated with the baseband dynamic-bias signal V_{ctrl3} and the baseband supply modulation signal V_{ctrl4} respectively. Port 1 and port 2 are associated with the PA's input

signal V_{in} and output signal V_{out} respectively. Similar to the example described earlier, P_3 is a complex polynomial describing a nonlinear baseband-to-RF conversion of the dynamic-bias signal V_{ctrl3}. P_4 is a complex polynomial describing a nonlinear baseband-to-RF conversion of the supply modulation signal V_{ctrl4}. H_3, F_3, H_4, F_4 may either be complex polynomials or constants (e.g. a scalar value of 1 if they have no incidence). The outputs of H_3 and F_3 are summed using the combiner and applied as input to F_4. Now, the outputs of H_4 and F_4 are summed using the second combiner and directly applied as input to the cascaded polynomials F and G (within the green dotted box) to extract the PA's output signal V_{out} under dynamic biasing and supply modulation. An alternative representation would be to exchange the signals at port 3 and port 4 in Figure 4.3(c), such that the supply modulation signal V_{ctrl4} is applied at port 3 and the dynamic-bias signal V_{ctrl3} is applied at port 4. Depending on the nonlinear functions P_n, H_n and F_n, such exchange in the signals at port 3 and port 4, which leads to a different flow in the nonlinear processing of the dynamic biasing and the supply modulation signals, may be exploited through the solving of the resulting system of nonlinear equations, to capture the effects of the dynamic biasing and the effects of the supply modulation with different levels of accuracy.

The examples above may be similarly extended to an n-port analytical PA representation, to capture PA performances under envelope-dependent biasing signals applied to (n-2) different control ports. In Section 4.3, we take up the specific example of a PA under envelope-dependent dynamic biasing and the equivalent 3-port form of the proposed multi-port representation that is necessary to capture the performance of such a PA. A few other equivalent forms of the n-port analytical representation are also discussed in the Conclusion chapter of this thesis.

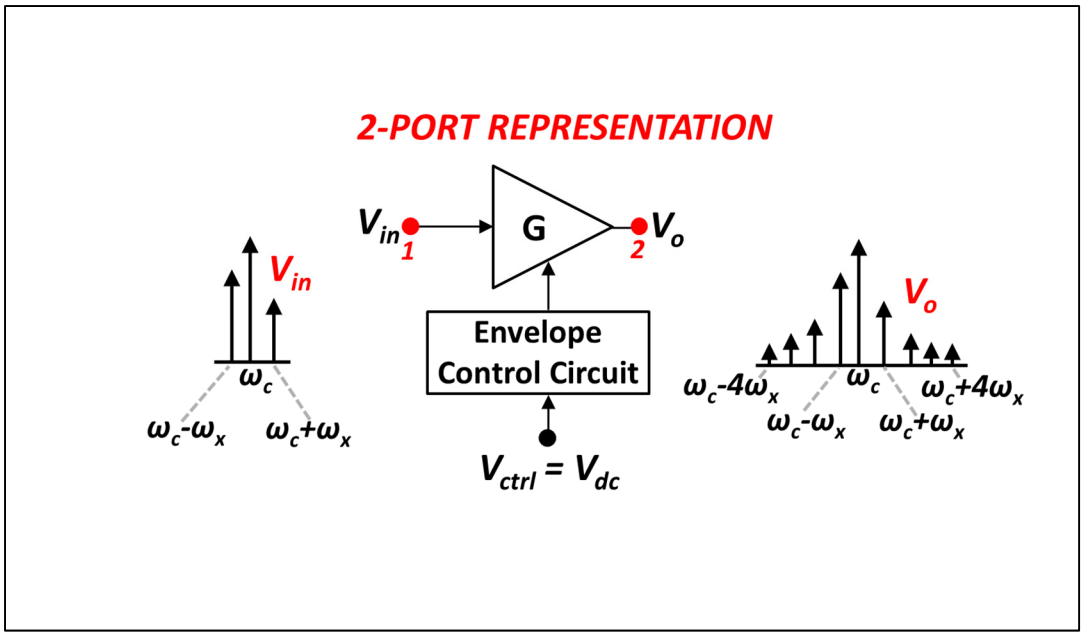

Figure 4.4 PA circuit under multi-tone excitation V_{in} and with V_{ctrl}=V_{dc} (under constant DC supply and biasing). V_o represents the PA's output multi-tone signal. G is characterized with V_{ctrl} held at V_{dc}. *1* and *2* are the input and output ports respectively of the 2-port PA representation

4.3 Three-port analytical representation of PAs under dynamic bias: Theory

The block diagram shown in Figure 4.4 represents a PA with its envelope-dependent control signal (e.g. supply modulation or dynamic biasing) held at $V_{ctrl} = V_{dc,}$ i.e. under constant DC supply and biasing. A complex nonlinear polynomial G represents the PA's RF transfer function, and the output multi-tone signal V_o can be derived from the input multi-tone signal V_{in} with the help of (4.1).

$$v_o(t) = a_1 v_{in}(t) + a_3 {v_{in}}^3(t) + a_5 {v_{in}}^5(t) + \cdots \tag{4.1}$$

There is an inherent assumption that the PA output has a band-pass filter to limit the RF output spectrum to the frequency range of interest around ω_c. Therefore, the odd-order terms only are needed in (4.1).

The complex coefficients a_1, a_3, a_5, etc. of polynomial G account for the PA's dynamic AM-AM and AM-PM behaviour under $V_{ctrl} = V_{dc}$. It is shown in (Clark, Silva, Moulthrop, & Muha, 2002) that the memory effects of a PA and its impact on the PA's IMD characteristics in response to a multi-tone input excitation can be accurately captured using its dynamic AM-AM and AM-PM responses. Such memory effects are dependent on the carrier frequency ω_c, on the envelope amplitude variations of the modulated RF signal, and on the envelope frequency set by the two-tone frequency spacing ω_x. The set-up shown in Figure 4.4 uses a three-tone excitation; hence the approximations detailed in (Clark, Silva, Moulthrop, & Muha, 2002) remain valid and the experimental set-up shown in (Clark, Silva, Moulthrop, & Muha, 2002, Figure 2) can be used for the extraction of the PA's dynamic AM-AM and AM-PM, which is then used for the extraction of the complex polynomial G in Figure 4.4.

The PA's RF transfer function G may be varied by modifying V_{ctrl}. Gain control by dynamically adjusting the PA's current through electronic control of its bias/supply circuit (e.g. using positive envelope feedback as detailed in Chapter 2-3 of this thesis) is one example of such a variation of G.

We now focus on dynamic biasing specifically, as an envelope-dependent mechanism. Figure 4.5 shows an implementation where a dynamic-bias signal V_e varying at the frequency of the input-excitation tone-spacing ω_x (as well as containing its higher-order harmonics) is applied to the PA. Such a dynamic-bias signal is encountered in techniques aimed at improving PA performances using envelope-dependent biasing schemes (Constantin, May, 2010; Deltimple, Leyssenne, Kerhervé, Deval, & Belot, 2010; Medrel et al., 2013; Tafuri, Sira, Jensen, & Larsen, 2013; Po-Chih et al., 2008; Onizuka, Ikeuchi, Saigusa, & Otaka, 2012, Sharma, Constantin, & Soliman, 2017; Kang, Baek, & Hong, 2017).

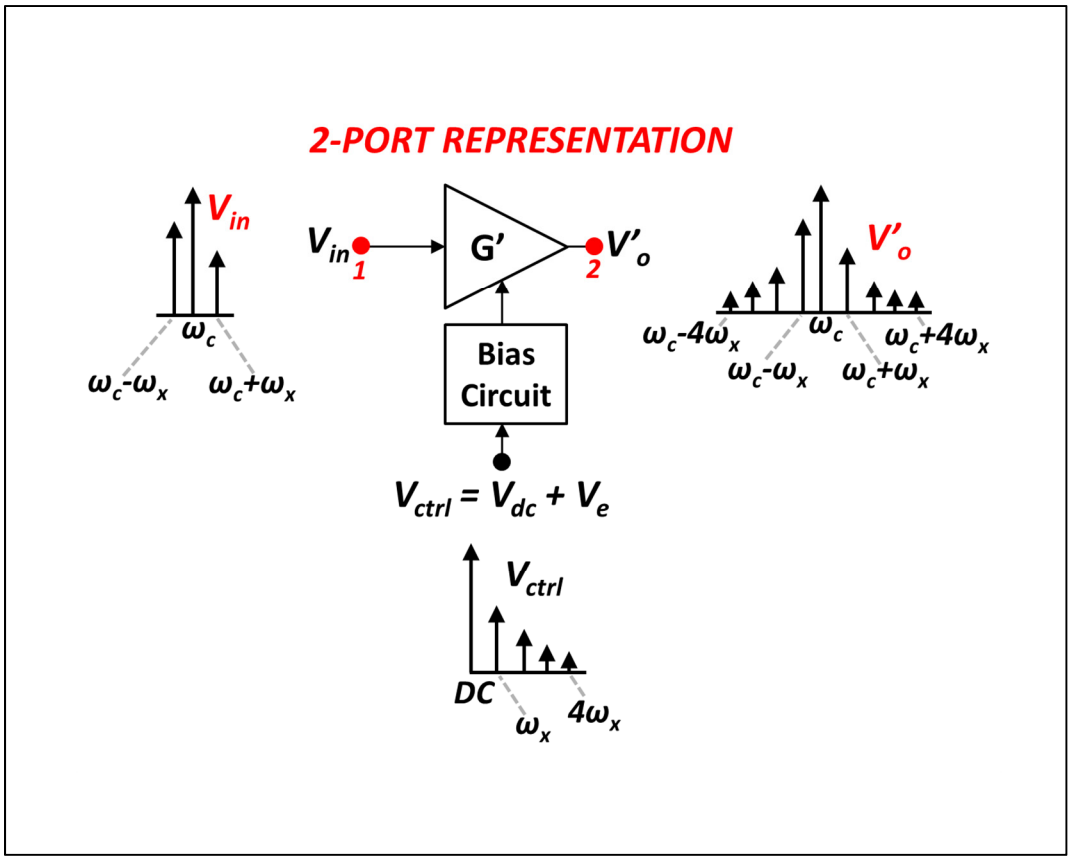

Figure 4.5 2-port PA representation of Figure 4.4 under dynamic bias. V_e is the dynamic multi-tone component of the bias signal and V'_o represents the PA's new multi-tone output signal. G' is the new complex polynomial characterized with the bias node excited by the dynamic-bias signal $V_{ctrl} = V_{dc} + V_e$

Let us consider this change in the bias signal from $V_{ctrl} = V_{dc}$ to $V_{ctrl} = V_{dc} + V_e$. The input excitation V_{in} remains unchanged, and the change in the output multi-tone from V_o to V_o' under dynamic bias is captured by the change in the PA polynomial from G to G' (Figure 4.5). G' therefore captures the PA's nonlinearities arising not only from an envelope-modulated input signal but also that due to a bias signal varying with the frequency of the PA's input/output envelope signal. However, any subsequent change in the PA's multi-tone bias signal V_{ctrl} would necessitate the characterization of another new polynomial G'', which reflects the PA's nonlinearities with this new bias control.

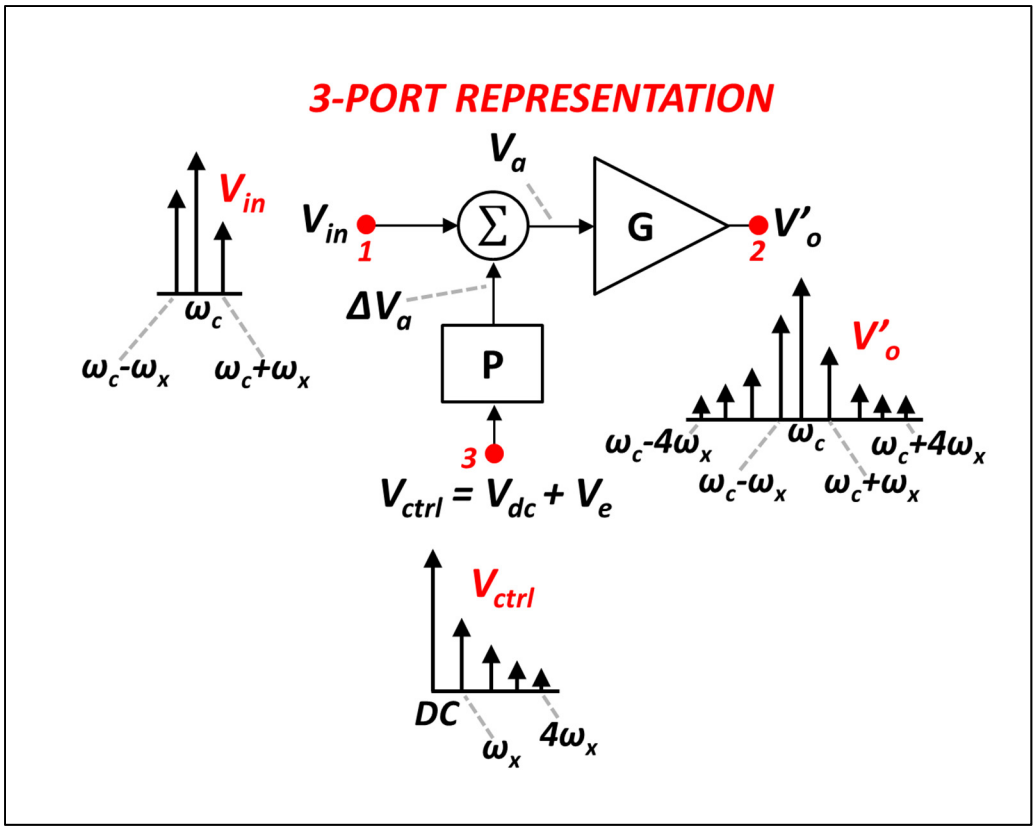

Figure 4.6 Proposed 3-port representation of PA under the dynamic biasing conditions shown in Figure 4.5. Port 3 represents the PA's bias port. *G* is the same complex polynomial in Figure 4.4 characterized with the PA's bias node held at $V_{ctrl} = V_{dc}$

In light of the above, a PA representation that accounts for the PA's nonlinearities arising out of a change in its bias signal without resorting to a polynomial extraction routine with every such change offers an attractive alternative to the two-port representation discussed so far, as well as an analytical means to understand the PA's nonlinearities as a function of its bias.

Figure 4.6 shows the proposed 3-port representation for the PA under the dynamic bias of Figure 4.5. The change in the polynomial from *G* to *G'* as described in Figure 4.5 (resulting in a change of the output IMD tones from V_o to V'_o) is equivalently accounted for in the proposed representation by an incremental change ΔV_a in the multi-tone input to the original polynomial *G*, where *G* is characterized with $V_{ctrl} = V_{dc}$, i.e. $V_e = 0$. ΔV_a is derived from the

dynamic biasing signal $V_{ctrl} = V_{dc} + V_e$ using a second nonlinear polynomial P (comprising a set of complex coefficients p, that define a multi-tone baseband to multi-tone RF conversion gain), and this ΔV_a signal, summed with V_{in} and applied to G, results in the new output signal V'_o. The summer and the node ΔV_a in Figure 4.6 are not physically present in a typical PA architecture but only represent an analytical equivalence.

It is worthwhile to note that PA tests and analysis based on multi-tone analysis are of significant help to designers (Yang, Yi, Nam, & Kim, 2000; Gibiino, Avolio, Schreurs, Santarelli, & Filicori, 2016; Hyunchul & Kenney, 2001; Carvalho & Pedro, Dec. 1999; Park et al., 2016). When limited to a few number of tones, such analyses offer intuitive insight and a relatively simple but accurate description of PA performances without dealing with the more complicated calculations involved when highly-complex modulated excitation signals are used. Measurement data of multi-tone tests additionally allow easy and fast benchmarking using widely accepted PA performance measurements (such as IMD_3). Besides, the correlation of multi-tone measurements such as IMD_3 with other measurements used for complex modulated excitation signals (such as *ACPR*, *EVM*) is also documented (Hyunchul & Kenney, 2001; Carvalho & Pedro, Dec. 1999).

Additionally, it is well known that a PA representation that accounts for higher-order nonlinear contributions enhances the representation's accuracy; however, the difficulty of extracting higher-order kernels when using Volterra series (and given the challenges associated with even extracting first-order Volterra coefficients (Gibiino, Santarelli, Schreurs, & Filicori, 2017)) makes it prohibitively complex to use in the context of embedded self-calibration. The 3-port PA representation proposed here overcomes this limitation by capturing higher-order contributions of the dynamic bias to the PA output with the help of lower-order polynomials that are easy to extract, thereby enhancing the accuracy of the PA representation.

To illustrate this, consider the proposed 3-port PA representation in Figure 4.6 limited to 3rd-order G (hence with coefficients a_1, a_3 only) and a 2nd-order P (hence with coefficients p_1, p_2)

polynomials. Additionally, to simplify our analysis and without any loss of generality, consider a 1-tone RF excitation V_{in} at RF frequency ω_c and a 1-tone dynamic-bias signal V_e (in addition to the quiescent DC value) at envelope frequency ω_x. As shown in Figure 4.6, the output of the polynomial P being itself applied as input to the polynomial G, allows capturing an overall sixth-order nonlinear dependence of the PA's output signal V_o' on the dynamic bias V_e. It can be shown through expansion of (4.1) and after simplification, that the value of the third-order output-tone $V_o'(\omega_c+2\omega_x)$ shows this sixth-order nonlinear dependence as given by expression (4.2).

$$V_o'(\omega_c + 2\omega_x) = k_2 {V_e}^2 + k_3 {V_e}^3 + k_4 {V_e}^4 + k_5 {V_e}^5 + k_6 {V_e}^6 \tag{4.2}$$

where complex constants k_2, k_3, k_4, k_5 and k_6 stem from the coefficients of P and G. For example, the dependence of k_6 on a_3 and p_2 is shown in (4.3).

$$k_6 = \frac{9}{4} \cdot a_3 \cdot {p_2}^3 \tag{4.3}$$

Therefore, solving for a_1, a_3 and p_1, p_2 simultaneously allows capturing up to a sixth-order dependence of the PA's output signal on V_e, despite P being limited to 2nd-order and G being limited to third order, as also illustrated in Figure 4.7. The presence of even-order terms in (4.2), although G contains odd-order terms only (as shown in (4.3)), is because P includes both even-order and odd-order baseband-to-RF contributions of the dynamic-bias signal V_e to ΔV_a. These contributions are summed with V_{in} and then processed by G, resulting in odd-order as well as even-order terms in (4.2) that contribute to $V_o'(\omega_c+2\omega_x)$ within the band-pass response of the PA.

On the other hand, extracting the same sixth-order nonlinear dependence on the dynamic-bias signal V_e when using Volterra-based PA representations would require increasing the order in equation (1.2), with the significant added complexity discussed before in Section 1.3.1.

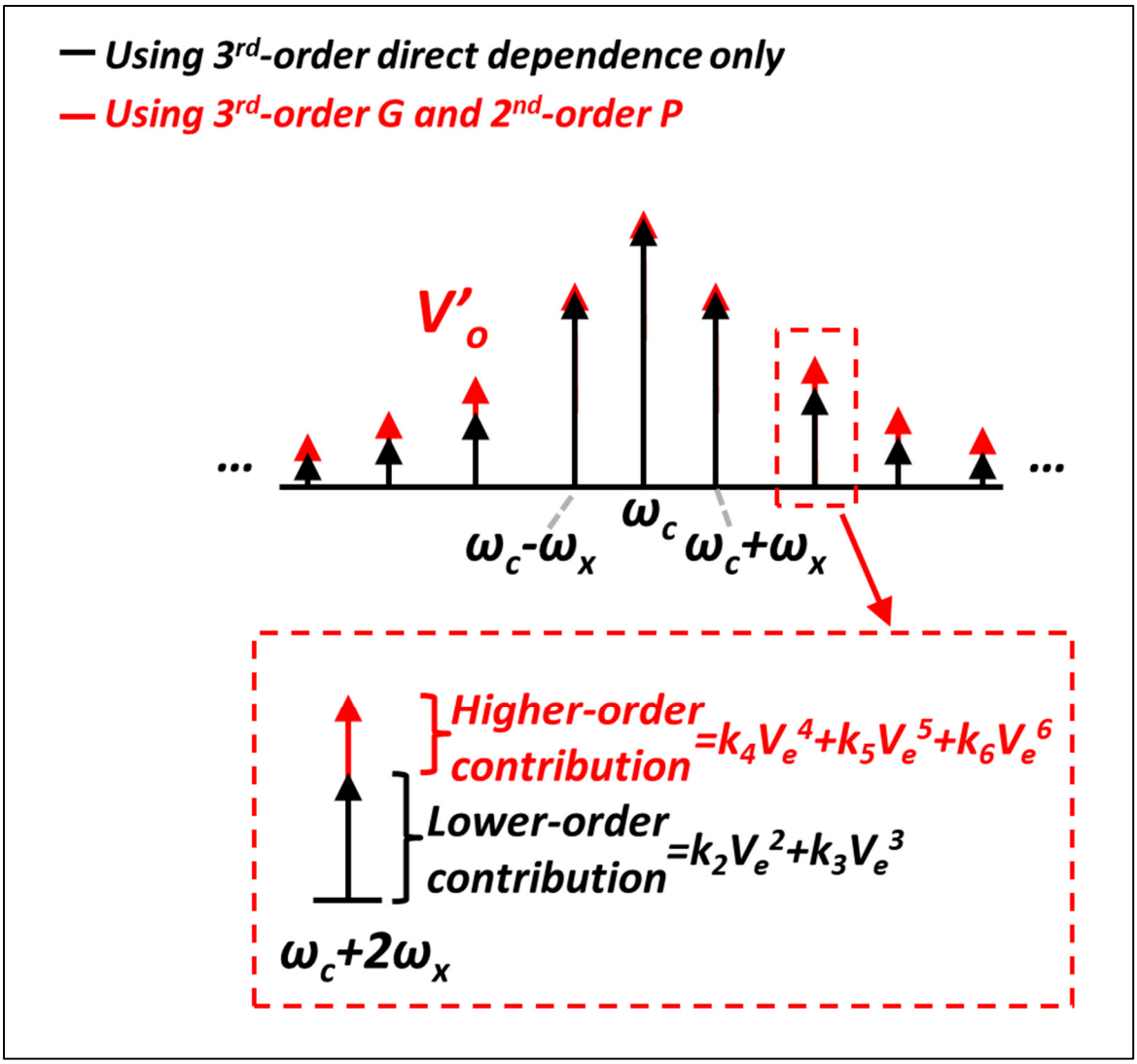

Figure 4.7 Illustration of the capture of contributions from higher-order PA nonlinearities using the proposed 3-port representation with the help of lower-order nonlinear polynomials

4.3.1 Three-port mathematical representation: Derivation of equations

The three-tone input signal $v_{in}(t)$ applied to the PA input, as shown in Figure 4.6, is represented by (4.4).

$$v_{in}(t) = \sum_{i=-1}^{1} V_{in}(\omega_c + i\omega_x) \cdot \cos\left((\omega_c + i\omega_x)t + \theta_{\omega_c + i\omega_x}\right) \tag{4.4}$$

where $V_{in}(\omega_c + i\omega_x)$ and $\theta_{\omega_c+i\omega_x}$ represent the magnitude and phase respectively for each tone of $v_{in}(t)$. The equivalent bilateral form of (4.4) is given by (4.5).

$$v_{in}(t) = \frac{1}{2} \sum_{\omega_r=\omega_c,-\omega_c} \left(\sum_{i=-1}^{1} V_{in}(\omega_r + i\omega_x) \cdot e^{j\theta_{\omega_r+i\omega_x}} \cdot e^{j(\omega_r+i\omega_x)t} \right) \tag{4.5}$$

Note that $V_{in}(-\omega_c - i\omega_x) = V_{in}(\omega_c + i\omega_x)$, $\theta_{-\omega_c-i\omega_x} = -\theta_{\omega_c+i\omega_x}$ and j is the complex imaginary unit.

The multi-tone dynamic-bias signal $v_e(t)$ applied to the PA bias terminal (and added to V_{dc}), as shown in Figure 4.6, is represented by (4.6).

$$v_e(t) = \sum_{i=1}^{m} V_e(i) \cdot cos(i\omega_x t + \Phi_i) \tag{4.6}$$

Here, m refers to the number of significant tones (excluding DC) present in the bias signal. For example, m equals 4 in Figure 4.6 since the number of tones is 4, ranging from ω_x *to* $4\omega_x$. $V_e(i)$ and Φ_i represent the magnitude and phase respectively for each tone of $v_e(t)$.

The nonlinear baseband-to-RF transformation of the dynamic-bias signal $v_e(t)$ through polynomial P (Figure 4.6) is now assumed to give the incremental RF signal $\Delta v_a(t)$ as expressed by (4.7).

$$\Delta v_a(t) = \sum_{i=-s}^{s} \Delta V_a(\omega_c + i\omega_x) \cdot \cos((\omega_c + i\omega_x)t + \gamma_{\omega_c+i\omega_x}) \tag{4.7}$$

where $\Delta V_a(\omega_c + i\omega_x)$ and $\gamma_{\omega_c+i\omega_x}$ represent the magnitude and phase respectively for each tone of $\Delta v_a(t)$. Here, s is related to the number of significant tones present in the $\Delta v_a(t)$ signal, e.g. s=4 indicates that there are 9 tones in the $\Delta v_a(t)$ signal, at frequencies ω_c-$4\omega_x$, ω_c-$3\omega_x$ *...0...* ω_c+$3\omega_x$, ω_c+$4\omega_x$. The bilateral form of (4.7) is given by (4.8).

$$\Delta v_a(t) = \frac{1}{2} \sum_{\omega_r = \omega_c, -\omega_c} \left(\sum_{i=-s}^{s} \Delta V_a(\omega_r + i\omega_x) \cdot e^{j\gamma_{\omega_r + i\omega_x}} \cdot e^{j(\omega_r + i\omega_x)t} \right) \tag{4.8}$$

Here, $\Delta V_a(-\omega_c - i\omega_x) = \Delta V_a(\omega_c + i\omega_x)$, $\gamma_{-\omega_c - i\omega_x} = -\gamma_{\omega_c + i\omega_x}$ and j is the complex imaginary unit. The tones $\Delta V_a(\omega_r + i\omega_x) \cdot e^{j\gamma_{\omega_r + i\omega_x}}$ present in (4.8) are now expanded in terms of amplitude and phase to clearly show the relationship of these tones to the multi-tone dynamic-bias signal $v_e(t)$. With the help of coefficients p_{iql} of the polynomial *P*, the value of the tones present in $\Delta v_a(t)$ is given by (4.9) below.

$$\{\Delta V_a(\omega_r + i\omega_x) e^{j\gamma_{\omega_r + i\omega_x}}\}|_{\omega_r = \omega_c} = \sum_{q=1}^{m} \sum_{l=1}^{n} p_{iql} \{V_e(q) \cdot cos(\phi_q)\}^l \tag{4.9}$$

Here, *n* refers to the order of the polynomial *P*. *i* varies from –*s* to +*s*, where *s* is as defined in (4.7). $V_e(q)$, ϕ_q and m are defined in (4.6). To understand the indexing of p_{iql} in (4.9), consider (for example) the coefficient p_{312}. Here, index 2 in p_{312} represents that it captures the 2nd-order contribution of the $V_e(1)$ tone at frequency $1 \cdot \omega_x$ in the bias signal (given by index 1 in p_{312}), to the 3rd side-tone $\Delta V_a(\omega_c + 3\omega_x)$ (given by index 3 in p_{312}). The extraction procedure of the polynomial coefficients p_{iql} is detailed in Section 4.3.2.

The incremental signal $\Delta v_a(t)$ is added to the input three-tone excitation $v_{in}(t)$ to obtain $v_a(t)$ as shown by (4.10)-(4.11).

$$v_a(t) = v_{in}(t) + \Delta v_a(t) \tag{4.10}$$

i.e.

$$\begin{aligned} v_a(t) = {} & \frac{1}{2} \sum_{\omega_r = \omega_c, -\omega_c} \left(\sum_{i=-1}^{1} V_{in}(\omega_r + i\omega_x) \cdot e^{j\theta_{\omega_r + i\omega_x}} \cdot e^{j(\omega_r + i\omega_x)t} \right) + \\ & \frac{1}{2} \sum_{\omega_r = \omega_c, -\omega_c} \left(\sum_{i=-s}^{s} \left(\sum_{q=1}^{m} \sum_{l=1}^{n} p_{iql} \{V_e(q) \cdot cos(\phi_q)\}^l \right) \cdot e^{j(\omega_r + i\omega_x)t} \right) \end{aligned} \tag{4.11}$$

The $v_a(t)$ signal given by (4.11) is now applied as input to the original complex polynomial *G* to obtain the output multi-tone signal $v'_o(t)$ under dynamic biasing.

$$v'_o(t) = a_1 v_a(t) + a_3 {v_a}^3(t) + a_5 {v_a}^5(t) \tag{4.12}$$

By replacing $v_a(t)$ in (4.12) with its value given by (4.11), expanding the resulting expression and then grouping the terms at each resulting frequency together provides closed-form expressions for the value of each tone present in the PA's output multi-tone signal, in terms of the parameters and signals listed in (4.11) and (4.12), i.e. in terms of the coefficients of *G* and *P*, and the signals $v_{in}(t)$ and $v_e(t)$. The number of terms as well as the explicit form of the expression $v'_o(t)$ in (4.12) resulting from such an expansion being large, they are not shown here for conciseness. The reader is encouraged to consult (Sharma & Constantin, 2014) for one possible algorithm that can be used to derive these terms. However, after regrouping the output terms at the same frequency as described before, a compact representation of the resulting $v'_o(t)$ output signal and its bilateral equivalent will have the form given by (4.13) and (4.14) respectively.

$$v'_o(t) = \sum_{i=-u}^{u} V'_o(\omega_c + i\omega_x) \cdot cos((\omega_c + i\omega_x)t + \beta_{\omega_c + i\omega_x}) \tag{4.13}$$

$$v'_o(t) = \frac{1}{2} \sum_{\omega_r = \omega_c, -\omega_c} \left(\sum_{i=-u}^{u} V'_o(\omega_r + i\omega_x) \cdot e^{j\beta_{\omega_r + i\omega_x}} \cdot e^{j(\omega_r + i\omega_x)t} \right) \tag{4.14}$$

where $V'_o(\omega_c + i\omega_x)$ and $\beta_{\omega_c + i\omega_x}$ represent the magnitude and phase respectively for each tone of $v'_o(t)$. Here again, $V'_o(-\omega_c - i\omega_x) = V'_o(\omega_c + i\omega_x)$, $\beta_{-\omega_c - i\omega_x} = -\beta_{\omega_c + i\omega_x}$ and j is the complex imaginary unit. *u* is related to the number of significant tones present in the PA's output RF signal $v'_o(t)$, e.g. *u*=4 in Figure 4.6 since the number of tones is 9, ranging from ω_c-$4\omega_x$, ω_c-$3\omega_x$ …0… ω_c+$3\omega_x$, ω_c+$4\omega_x$. (4.14) represents the system of equations that relates the PA's output IMD levels V'_o with the three-tone input RF signal V_{in} and the dynamic-bias signal V_e for the 3-port PA representation proposed here.

The mathematical formulations of the proposed 3-port PA representation are now complete.

4.3.2 Three-port mathematical representation: Steps for coefficient extraction

The following steps are followed to extract the coefficients of polynomials G and P. the RFIC PA manufacturer may use this sequence of steps at an advanced engineering phase of the development. The PA manufacturer may then provide the extracted coefficients to a mobile equipment manufacturer as parameters of the proposed PA representation (represented by X in Figure 4.1-4.2) that describe the typical behaviour of the PA and used for the proposed self-calibration embedded within the mobile unit.

Step 1: Using a three-tone V_{in} and with the PA's bias held at V_{dc}, the magnitude and phase of the output multi-tone signal V_o is measured. This measurement is repeated for a set of three-tone input signals that define the PA's input power range of interest. Using each of these V_o vs. V_{in} measurements in (4.1), a system of equations is now derived, the solution of which gives the coefficients a_1, a_3, a_5, etc. of the complex polynomial G.

Step 2: With the PA input excited with any one of the three-tone V_{in} values from the set used in Step 1, the PA's bias node is now excited with a multi-tone signal $V_{e,}$ i.e. its bias is now $V_{ctrl} = V_{dc} + V_e$. The magnitude of the power levels of the multi-tone signal V'_o at the PA's output is measured.

Step 3: Step 2 is now repeated for different values of the multi-tone dynamic-bias signal V_e. The values of V_e chosen define the range of interest for the PA's dynamic-bias signal. The PA's input three-tone signal V_{in} is held constant at the value used in Step 2. The corresponding PA output power levels for this set of varying V_e signal values are measured.

Step 4: With G already known from Step 1, the V'_o vs. V_e measurements of Step 2 and Step 3 are used in equations (4.10) to (4.14) to derive a new system of equations. The solution of this system of equations is the set of complex coefficients of the nonlinear polynomial P (p_{iql}

as defined in (4.9) and (4.11)) that relates V_e with ΔV_a, and which translates into the PA's output signal V'_o under dynamic biasing.

The extraction of the proposed PA representation is now complete.

Centring the range of the measurement values of Step 1, Step 2 and Step 3 significantly aids in solving the system of equations of Step 1 and Step 4. Centring is explained with greater detail in Appendix II, as well as ways to handle the asymmetry of the PA's upper and lower IMD_3 levels.

It is worthwhile to note here that the simplicity of the characterization procedure for extracting the coefficients of the novel 3-port PA representation makes it promising for adoption by the PA manufacturer at an advanced engineering phase of the PA development. The PA manufacturer may then provide the obtained coefficients to the mobile equipment manufacturer as a single set of parameters of our proposed representation that describe the typical behaviour of the PA product. Additionally, this single set of parameters may also be used by the PA manufacturer itself to increase the yield of the PA product, by optimizing against performance variation across PA parts.

On the other hand, it will be shown in Section 4.4.4 and in Section 4.8 that the simplicity of the probing circuitry and the training sequence required to adjust the typical PA parameters provided by the PA manufacturer, to account for part-to-part variation of PA performance across mobile equipment, incentivizes the self-calibration technique proposed in this thesis to be embedded within the mobile equipment by the ME manufacturer. Such a technique allows adjusting the biasing, etc. of each PA part to ensure its optimum performance during operation of the mobile equipment, the adjustment being based on a one-time embedded measurement for each mobile equipment and leading to an overall increase in the yield of the mobile equipment by the ME manufacturer.

4.3.3 Three-port mathematical representation: Comments on some signal forms

It is well known that nonlinearities in solid-state circuits are predominantly a function of voltage-amplitude excursions present at different nodes in the circuit. The time-domain waveform analysis in this sub-section is intended to illustrate better the flexibility of the proposed three-port representation in terms of capturing the voltage-amplitude dynamics at the three ports, even though the characterization process for parameter extraction is based on a multi-tone excitation at the input and the biasing ports. Figure 4.8 illustrates the proposed 3-port PA representation of Figure 4.6, with the equivalent time domain forms of the signals V_{in}, V'_o and V_{ctrl}. The input three-tone RF signal corresponds to an envelope-modulated RF signal with envelope amplitude Env_{in}, while the output multi-tone signal corresponds to a distorted RF signal with envelope amplitude Env_{out}. The severity of distortion in the PA's output signal is measured using the PA's output IMD distortion levels. For a three-tone input excitation with tones at frequencies ω_c-ω_x, ω_c, ω_c+ω_x, the output distortion products are present at ω_c-$2\omega_x$, ω_c-$3\omega_x$, ω_c-$4\omega_x$, etc. and ω_c+$2\omega_x$, ω_c+$3\omega_x$, ω_c+$4\omega_x$, etc.

Without any loss of generality for the time domain waveform analysis in this sub-section and the vector analysis in the following sub-section, and for the purpose of simplification, we can assume zero phase difference between the three-tones in the input signal $v_{in}(t)$ i.e. $\theta_{\omega_c+i\omega_x} = 0$ in (4.4)-(4.5). The above simply translates into the reasonable assumption that the three cosines at these three frequencies are each one centred as an even time-domain waveform on a common t=0 time reference, without limiting the scope of the following analyses. $v_{in}(t)$ is then expanded as shown in (4.15).

$$v_{in}(t) = \sum_{i=-1}^{1} V_{in}(\omega_c + i\omega_x) \cdot cos((\omega_c + i\omega_x)t) \tag{4.15}$$

i.e.

$$v_{in}(t) = \left(A \cdot cos(\omega_x t) + V_{in}(\omega_c)\right) \cdot cos(\omega_c t) - B \cdot sin(\omega_x t) \cdot sin(\omega_c t) \tag{4.16}$$

where

$$A = V_{in}(\omega_c + \omega_x) + V_{in}(\omega_c - \omega_x) \tag{4.17}$$

$$B = V_{in}(\omega_c + \omega_x) - V_{in}(\omega_c - \omega_x) \tag{4.18}$$

Therefore, by selecting the right input excitation levels of the different tones in the input signal $v_{in}(t)$, the PA can be excited by a variety of input waveforms with varying values of Env_{in}. For example, using a symmetric 3-tone excitation i.e. $V_{in}(\omega_c+\omega_x)=V_{in}(\omega_c-\omega_x)$, we obtain B=0 in (4.18) and $Env_{in}=A=2\cdot V_{in}(\omega_c+\omega_x)$ defines the input envelope amplitude centered around value $|V_{in}(\omega_c)|$.

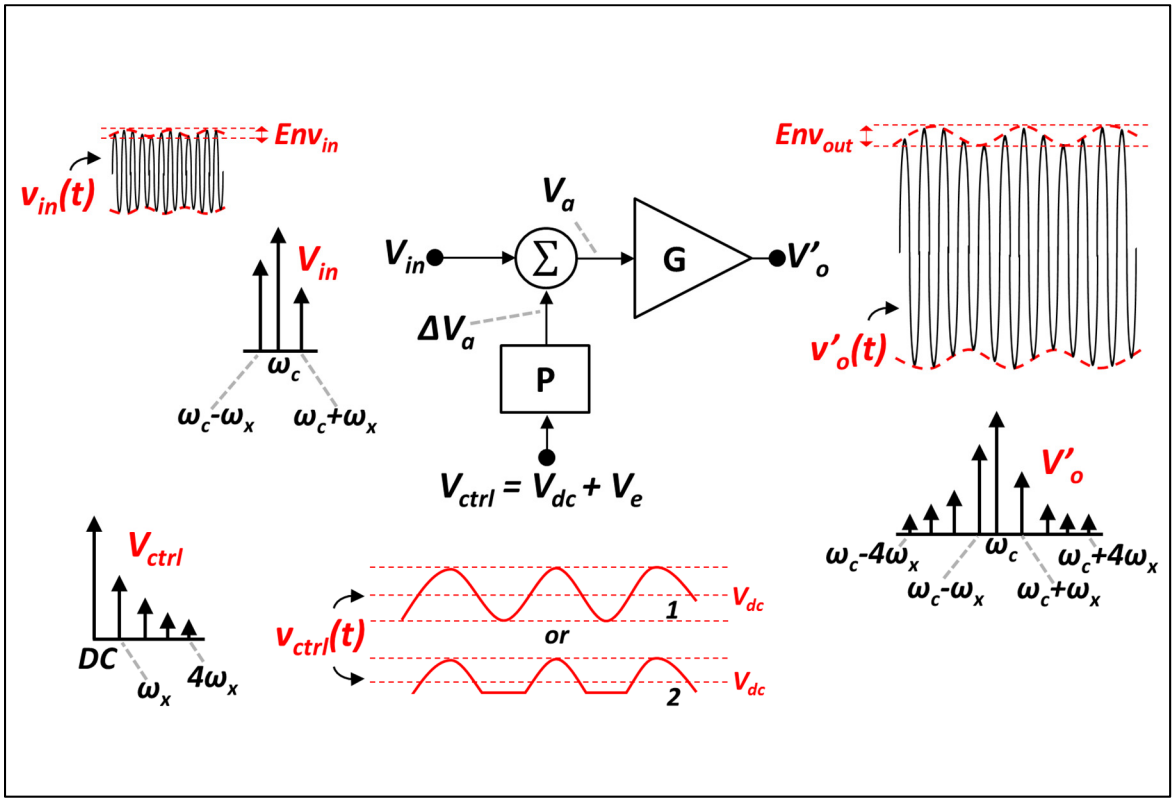

Figure 4.8 Illustrative time-domain form of signals at some critical nodes of the 3-port analytical PA representation

The complex polynomial G is extracted with the bias control V_{ctrl} held at the quiescent value V_{dc}. The accuracy of the PA's predicted output IMD levels using G is the highest for input envelope levels that lie in the proximity of the range of Env_{in} (or the equivalent range of Env_{out}) that is used to extract G. However, in the absence of strong nonlinearities, G is reasonably accurate for predicting PA output IMD levels for a broader range of input envelope levels than Env_{in}, as will be shown through various examples in Section 4.4.

A dynamic V_{ctrl} is now considered due to the addition of a multi-tone signal V_e to the DC level V_{dc}. Using the proposed 3-port PA representation, the effect of this dynamic biasing is captured using the complex polynomial P and the resulting incremental change in the input signal applied to G. The accuracy of prediction using this 3-port representation is the highest when the envelope of the dynamic biasing signal lies in the proximity of the envelope of the bias levels that were used while extracting the polynomial P. For bias conditions that lie outside this range and in the absence of strong PA nonlinearities arising out of such bias conditions, the representation still allows to estimate PA performances with reasonable accuracy.

The presence of multiple tones at different baseband frequencies in V_{ctrl} enables the representation of a variety of dynamic-bias signals. Two such forms 1 and 2 are shown in Figure 4.8. 1 represents a bias signal whose amplitude varies in linear proportion with Env_{in} (or Env_{out}). Such a signal can be synthesized by using the V_{ctrl} frequency component at ω_x alone, i.e. $V_{ctrl}(2\omega_x) = V_{ctrl}(3\omega_x) = \ldots = 0$. However, more complex biasing signals can also be used, such as the V_{ctrl} signal 2 shown in Figure 4.8. Here, the bias signal is held at a quiescent DC level for low values of Env_{in} (or Env_{out}), while it varies with an amplitude that is linearly proportional to Env_{in} (or Env_{out}) for higher envelope values. This case relates to the dynamic biasing signal V_{dyn} in the positive envelope feedback operation as discussed in Chapter 2, Figure 2.3. The equivalent frequency domain representation of such a bias signal contains components at frequencies $2\omega_x$, $3\omega_x$, $4\omega_x$, etc. In the proposed 3-port analytical PA representation, the complex polynomial P accounts for the contribution of all these frequency tones in the dynamic-bias signal to the PA's output IMD products.

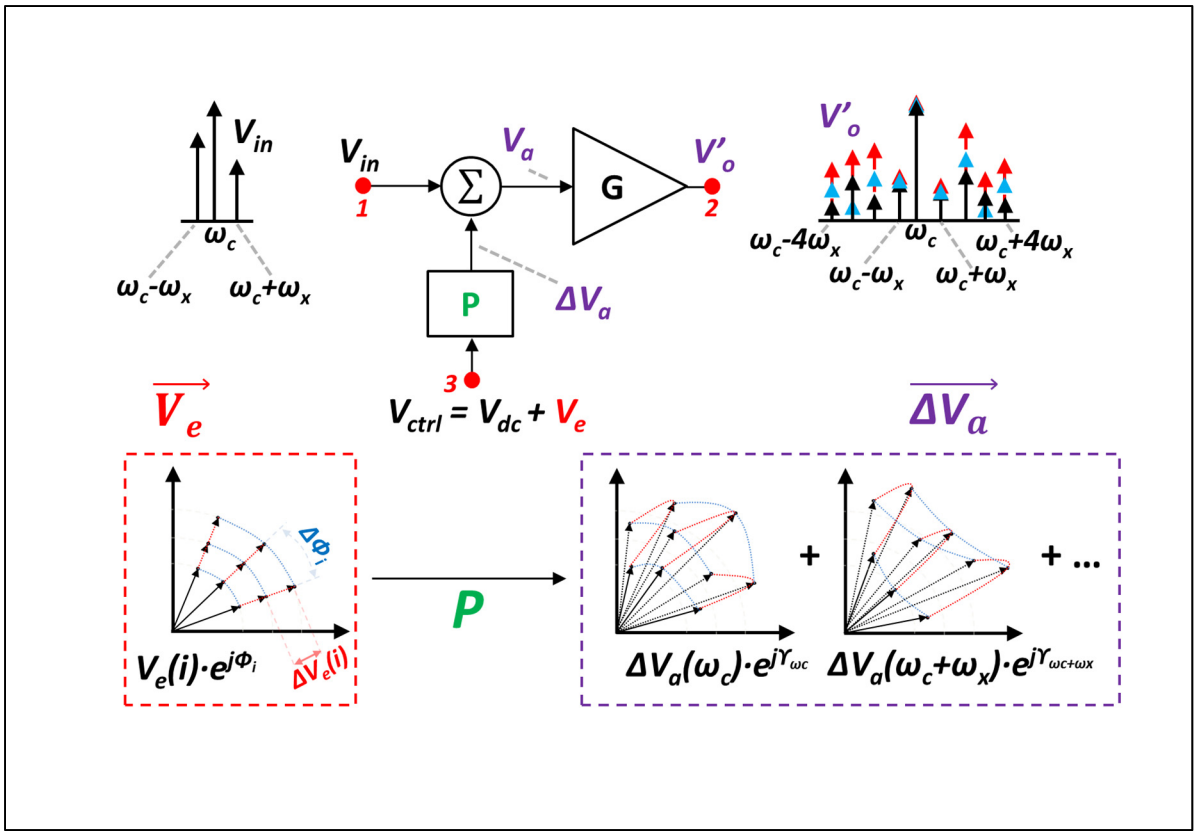

Figure 4.9 Equivalent vectorial illustration of signals in the 3-port analytical PA representation. The red dotted lines in V_e and ΔV_a reflect changes in their respective signal amplitudes, and the blue dotted lines reflect changes in their respective signal phases. The possible resulting variations in the PA's output IMD levels are also shown with coloured spectrum levels of V'_o

4.3.4 Three-port mathematical representation: Vector analysis

The proposed three-port PA representation is now analyzed with the help of the vector relationships that govern the magnitude and phase of the signals at the various PA nodes. Such an analysis is useful for understanding the effects of amplitude and phase excursions of the dynamic signal at the PA's bias port on the PA's output IMD products, which is captured with the help of our proposed three-port PA representation.

To understand the analytical PA representation from this vectorial perspective, refer to the illustration in Figure 4.9. Here, the dynamic-bias signal V_e represents a set of vectors with

magnitudes $V_e(1)$, $V_e(2)$, $V_e(3)$… and phases ϕ_1, ϕ_2, ϕ_3 … at frequencies ω_x, $2\omega_x$, $3\omega_x$… respectively. For the purpose of simplification of this discussion and without any loss of generality, only one tone $\overrightarrow{V_e}$ with magnitude $V_e(i)$ and phase ϕ_i at frequency ω_i is considered.

Figure 4.9 shows a possible variation $\Delta V_e(i)$ of the magnitude (shown with red dotted lines) and a possible variation $\Delta\phi_i$ of the phase (shown with blue dotted lines) of this bias vector $\overrightarrow{V_e}$ in the polar coordinate plane. Under the assumptions of the proposed PA representation, such variations of the bias vector translate into corresponding variations of the ΔV_a signal obtained through nonlinear transformation of V_e using the complex polynomial P. As shown in Figure 4.9, this ΔV_a signal may be represented as another set of vectors $[\Delta V_a(\omega_c)\cdot e^{j\gamma_{\omega_c}}, \Delta V_a(\omega_c+\omega_x)\cdot e^{j\gamma_{\omega_c+\omega_x}}, \Delta V_a(\omega_c+2\omega_x)\cdot e^{j\gamma_{\omega_c+2\omega_x}}$ … $\Delta V_a(\omega_c-\omega_x)\cdot e^{j\gamma_{\omega_c-\omega_x}}\ldots]$ defined at the frequencies ω_c, $\omega_c+\omega_x$, $\omega_c+2\omega_x$,… $\omega_c-\omega_x$ … respectively. An illustration of the possible resulting magnitude and phase variations of these $\overrightarrow{\Delta V_a}$ vectors is shown in Figure 4.9 with red and blue dotted lines.

The input three-tone signal V_{in} can also be viewed as a sum of three vectors $V_{in}(\omega_c-\omega_x)\cdot e^{j\theta_{\omega_c-\omega_x}}, V_{in}(\omega_c)\cdot e^{j\theta_{\omega_c}}$, $V_{in}(\omega_c+\omega_x)\cdot e^{j\theta_{\omega_c+\omega_x}}$ at frequencies ω_c-ω_x, ω_c, ω_c+ω_x respectively. Note that a variation of these V_{in} vectors will reflect a change in the PA's input power (envelope power or RF power, or both). In this section, we focus exclusively on the effect of the amplitude and phase variation of the $\overrightarrow{V_e}$ bias vector (shown within the red dotted box in Figure 4.9) on the PA's output signal V'_o, while considering a constant value of the input signal vector $\overrightarrow{V_{in}}$. By repeating the analysis that follows for a second case where the V_{in} signal at port 1 is a new signal V_{in}', the effect of the amplitude and phase variation of the $\overrightarrow{V_e}$ bias vector on the PA's output signal V'_o when there is a change in the PA's input power (envelope power or RF power, or both) may be calculated.

The vectors constituting ΔV_a are now summed with the vectors constituting V_{in} to give a new set of vectors constituting the signal V_a. When this V_a signal is applied as input to the complex polynomial G, the resulting set of vectors constituting the PA's output signal V'_o

reflects the changes in the PA's output IMD levels due to amplitude or phase variations (or both) of the frequency tone $V_e(i) \cdot e^{j\phi_i}$ in the bias signal. Two examples of possible resulting changes in the PA's output IMD levels are illustrated in Figure 4.9 with red and blue coloured spectrum levels of V'_o.

The preceding vector analysis can be extended to include the case when more than one tone is present in the dynamic-bias signal. In this case, the complex polynomial P captures the effect of all the tones present in the dynamic-bias signal on the vectors constituting the signal ΔV_a, and ultimately the impact of the dynamic-bias signal on the IMD levels at the PA's output. The aforementioned analysis highlights the ability of the proposed PA representation to predict a linearization process by pre-distortion for linearity improvement (i.e. reducing the output IMD products) with the use of the dynamic-bias signal at port V_e.

4.4 Validation of proposed 3-port representation through comparison with ADS™ simulation

4.4.1 Description of simulation test-bench

The formulations of the proposed representation are now validated through its bench-marking against an RFIC PA design within a simulation test-bench. The PA used is a 5GHz SOI CMOS PA in 0.18um technology from TowerJazz, and its design details were described in Section 3.2. These details are summarized here again to enable the reader to refer to them easily. The same PA will also be referred to again in Section 4.7. It is a 3-stage design with a cascode structure and designed for flip-chip assembly on a 6-layer multi-chip module (MCM), which is further assembled on a PCB. Decoupling capacitors are present on all DC lines. The simulation software used is ADS™ Dynamic Link™. All results shown for this design are performed using PEX™ extracted views (for active devices) and post-layout simulations using the electromagnetic (EM) extraction tool EMX™. As noted earlier, the PA schematic is provided again in Section 4.7, Figure 4.22, where the application of the analytical representation to closed-loop PAs under positive envelope feedback is discussed. For the open-loop operation described in the present section, resistance R_a in Figure 4.22 is

kept open and the quiescent value of the PA's third-stage gate bias is held at V_{dc}=0.355V. Dynamic biasing is performed by externally applying an envelope signal V_e directly to the gate of the NMOS in the third-stage (node *g* in Figure 4.22 (a)) via 15nH inductors, using a baseband signal generator component in the simulation test-bench. The input excitation V_{in} is a three-tone RF signal with the two side tones held 5dB lower than the center tone. The RF center frequency is f_c=5.4GHz and a spacing of f_x=50MHz is used.

4.4.2 PA linearization through dynamic gate bias

With the PA's gate bias held at V_{dc} = 0.355V and by varying V_{in} over the input power range of interest, the polynomial *G* given by (4.19) below is extracted. As shown in Figure 4.10, an excellent match between the PA's simulated and predicted output tones is observed (less than 0.12dB error for the f_c - $2f_x$ tone, which itself is ~26dB below the f_c tone, at the characterization power level of 14dBm). A 5th-order polynomial is sufficient for *G* and unlike other PA representations (e.g. (Gibiino, Avolio, Schreurs, Santarelli, & Filicori, 2016)), the coefficients remain unchanged over the PA's output power range of interest.

$$v_o(t) = (8.19 + j \cdot 1.48) \cdot v_{in}(t) + (-4.98 - j \cdot 1.56) \cdot {v_{in}}^3(t) + (3.40 + j \cdot 2.14) \cdot {v_{in}}^5(t) \quad (4.19)$$

The increase of the error at lower average output power levels does not affect the accuracy of the proposed representation at 14dBm since this error pertains to the *G* block only (not the *P* block). It will be shown in Section 4.4.3 that the full representation (i.e. including both *G* and *P* blocks) accurately captures the PA's IMD performance over a significant power range across the characterization power level.

With *G* extracted, a dynamic-bias tone V_e at frequency f_x is added to the DC bias of the PA. By varying the amplitude of V_e, noting the corresponding output multi-tone signals and solving the system of equations (4.11)-(4.14) for these measurements, the complex coefficients of the second-order polynomial *P* as represented in (4.9) are extracted. The resulting polynomial *P* is given by (4.20).

$$\Delta v_a(t) = \frac{1}{2}(1.27 - j \cdot 0.07) \cdot v_e(t) \cdot cos(\omega_c t)$$
$$+\frac{1}{2}(1.09 - j \cdot 0.31) \cdot v_e(t) \cdot cos\big((\omega_c + \omega_x)t\big)$$
$$+\left\{\frac{1}{2}(0.56 - j \cdot 0.31) \cdot v_e(t) + \frac{1}{4}(-1.85 + j \cdot 0.12) \cdot v_e(t)^2\right\} \cdot cos\big((\omega_c + 2 \cdot \omega_x)t\big) \quad (4.20)$$
$$+\frac{1}{2}(1.13 + j \cdot 0.12) \cdot v_e(t) \cdot cos\big((\omega_c - \omega_x)t\big)$$
$$+\left\{\frac{1}{2}(0.69 + j \cdot 0.15) \cdot v_e(t) + \frac{1}{4}(-1.16 - j \cdot 0.50) \cdot v_e(t)^2\right\} \cdot cos\big((\omega_c - 2 \cdot \omega_x)t\big)$$

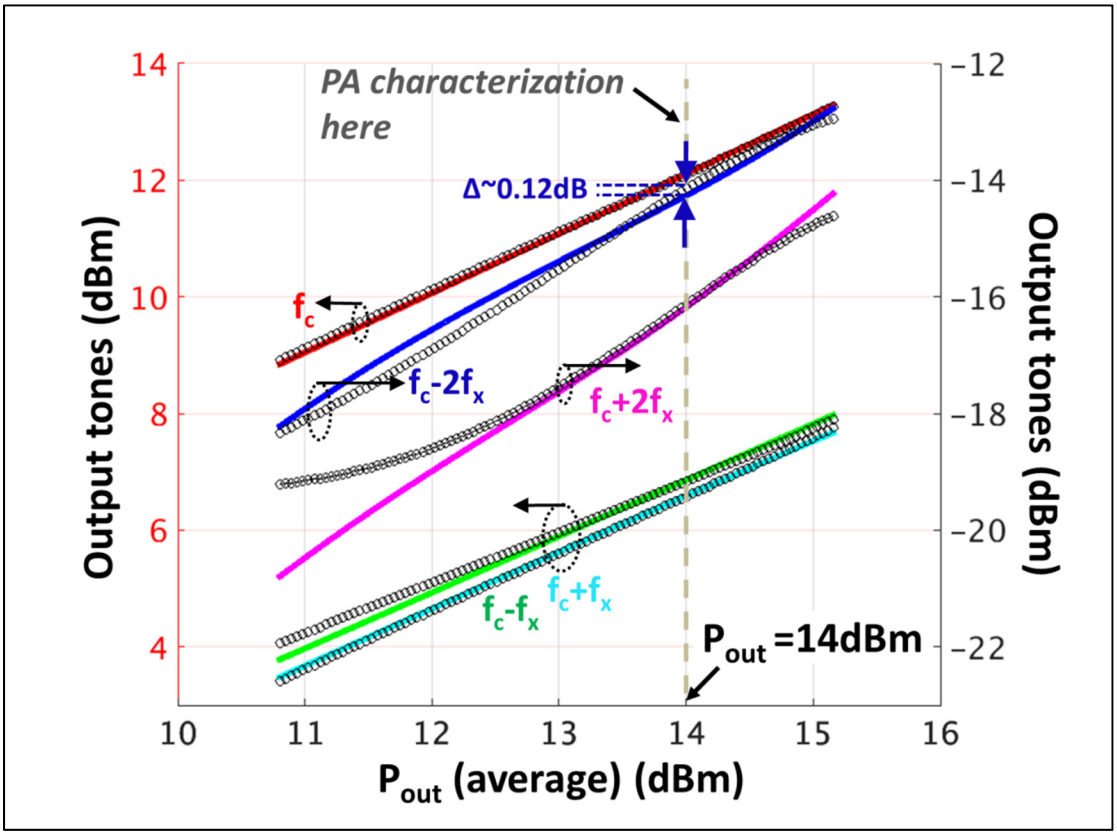

Figure 4.10 Simulated values (solid traces) and predicted values (circular marker traces) of the PA's output signal, including the output tones at f_c-$2f_x$ and f_c+$2f_x$ which are due to the PA's nonlinearity under quiescent bias.
The characterization power level is P_{out} (*average*) ~14dBm

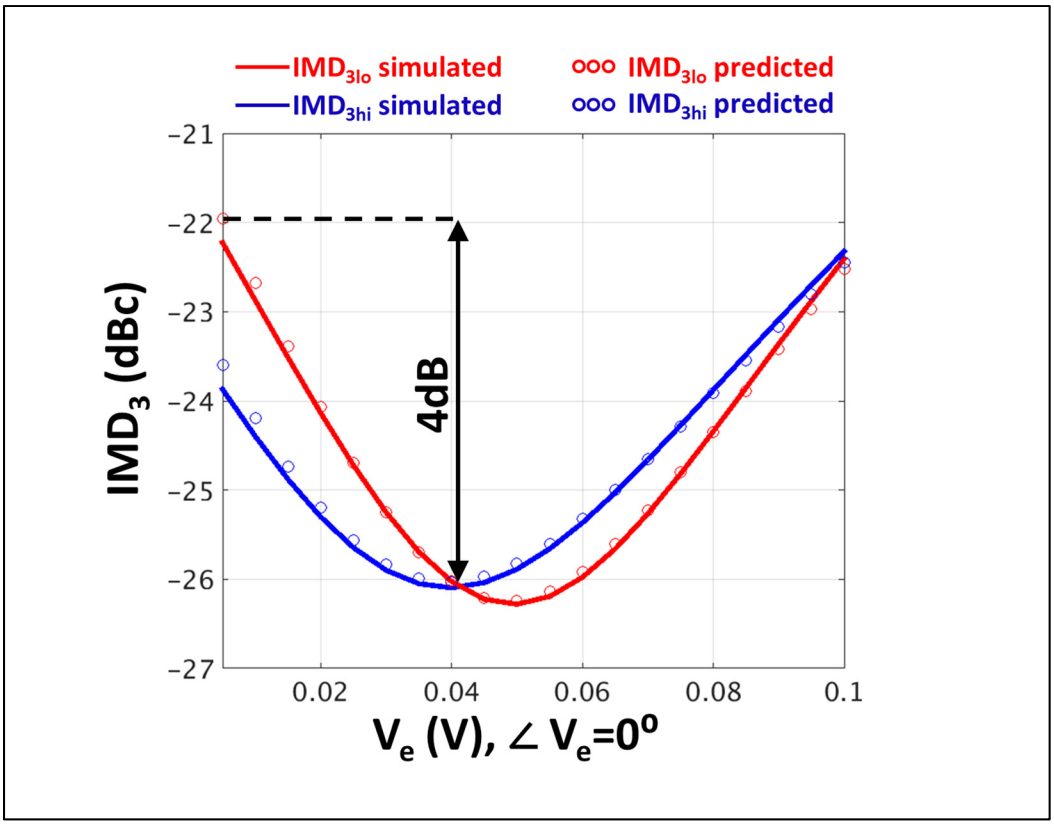

Figure 4.11 Simulated values (solid traces) and predicted values (circular marker traces) of the PA's output IMD_3 under dynamic bias, at P_{out} (*average*) ~14dBm

Figure 4.11 shows a comparison of the PA's simulated IMD_3 with that predicted using the proposed 3-port representation as a function of V_e at the PA's characterization power level P_{out} ~14dBm. The proposed representation predicts with negligible error that setting the dynamic biasing signal V_e to 40mV, $\angle 0^0$ yields a 4dB improvement in IMD_3. The 0^0 phase translates the fact that the delay through the driver stages and the bias interfacing (having minimal reactances) in this specific PA design (Figure 4.22) is negligible for baseband signals. It is sufficient to truncate P to 2^{nd}-order here, and the extracted P and G accurately captures the PA's performance over the range of interest of the PA's operating power and dynamic-bias levels. Note that experimental results shown in Section 4.5 will demonstrate a comparable IMD_3 improvement of ~4dB, based on computation using the proposed 3-port representation starting from purely experimental measurements.

A comparison of the simulated and predicted time-domain form of the PA's output envelope signal with V_e=40mV in Figure 4.12 further highlights the accuracy of the proposed 3-port PA representation. The coefficients of the quasi-static representation alone fail to account for the dynamic deviations of the PA's output signal envelope under dynamic bias, and the coefficients of both G and P polynomials are essential to account for them when using the analytical PA representation to capture the PA's nonlinearities arising from envelope-dependent dynamic biasing.

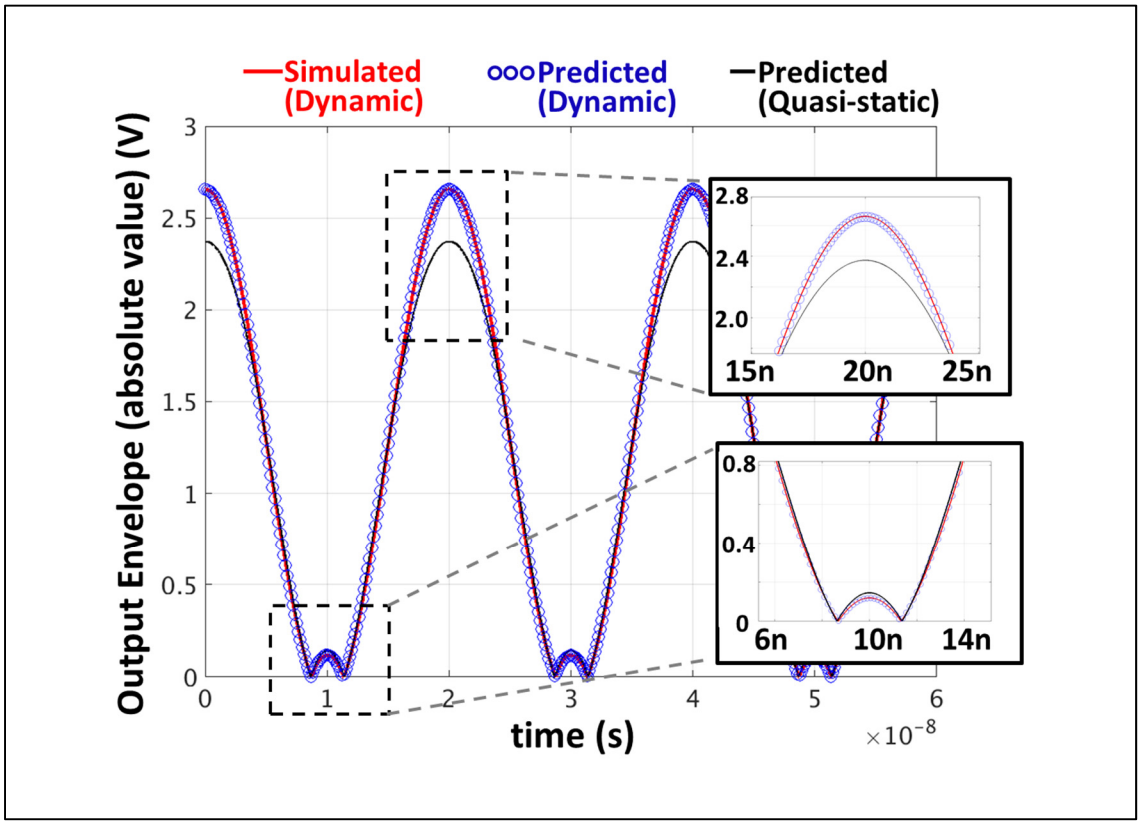

Figure 4.12 Simulated and predicted time-domain form of the PA's output envelope signal under dynamic bias with V_e=40mV and $P_{out}(avg)$ ~14dBm. The time-domain form predicted using only the quasi-static representation is also shown for comparison

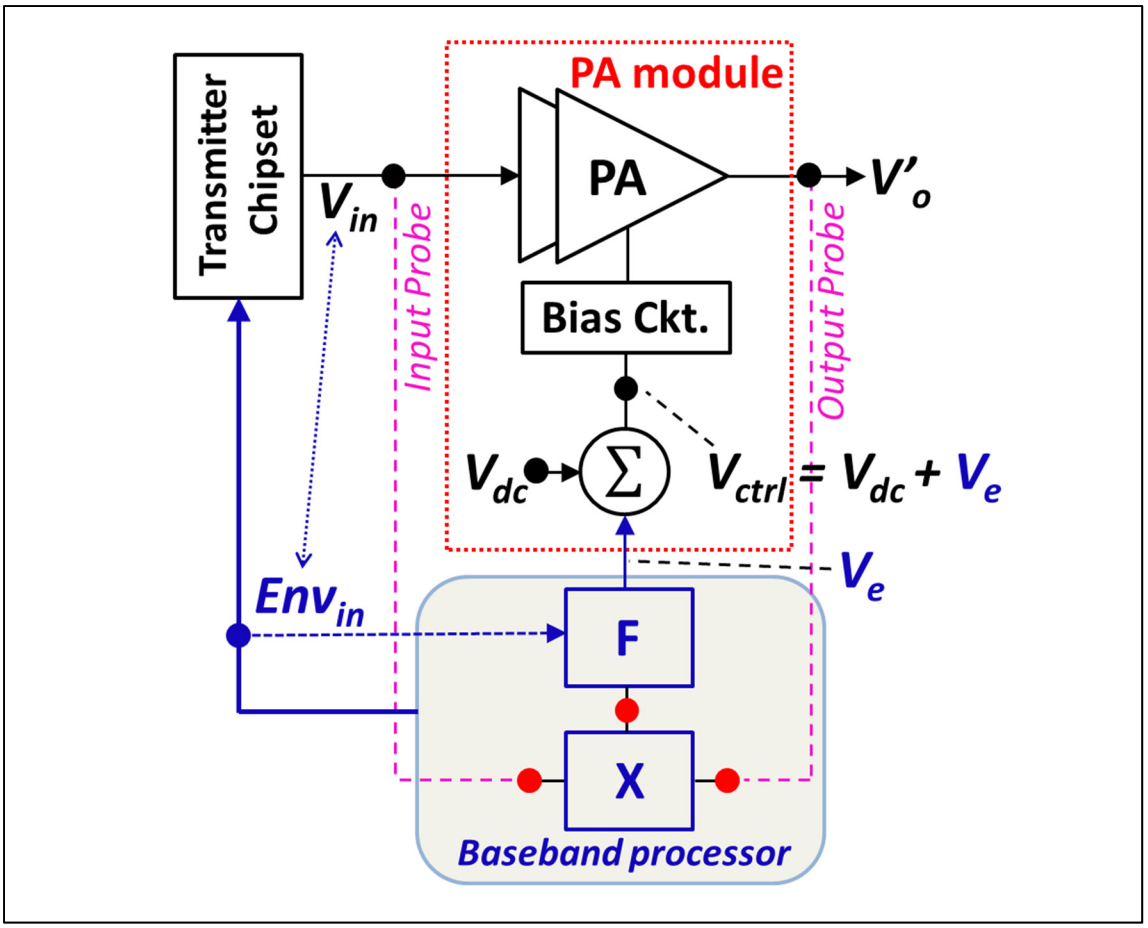

Figure 4.13 Implementation of feed-forward dynamic biasing embedded within the mobile unit for linearization of PA. *F* is extracted using our 3-port representation *X* of the PA module, and then applied to the PA module to optimize its output linearity via dynamic biasing

4.4.3 Application example 1: Feed-forward dynamic biasing for optimizing PA linearity

An application illustrated in Figure 4.13 is now demonstrated, where the $v_{in}(t)$-$v_o(t)$-$v_e(t)$ multi-tone relationships (4.19) and (4.20) of the extracted 3-port PA representation *X* is used to build a pre-distortion function *F* embedded as a signal processing element within the baseband chipset of a transmitter front-end. Note that the baseband processor also generates Env_{in}, which is the envelope signal related to the PA's input modulated signal V_{in}. The parameters of *X* (extracted as per Section 4.3.2) may be provided by the PA manufacturer in

a real implementation. This function F is aimed at performing the necessary embedded adjustment (performed within the mobile unit) on V_e to minimize the PA's output IMD_3 through feed-forward dynamic biasing. F, therefore, gives the relationship between the PA's input envelope Env_{in} and its bias signal V_e that allows achieving optimum PA output linearity. In this example, F is determined using MATLAB™ starting from the same 3-port representation X used for Figure 4.11, and that was characterized at P_{out} ~14dBm.

Note that though F is extracted using the proposed 3-port representation X, the PA's improved performance using the F block that is shown next is evaluated by applying F (implemented using the frequency-domain defined device *FDD* functional block in ADS™) to the 5GHz SOI CMOS PA design itself (represented by 'PA module' in Figure 4.13) within the ADS™ circuit simulation environment, and not by merely applying F to the extracted 3-port representation X of this PA module.

Figure 4.14 shows the PA's output IMD_3 vs P_{out} without and with the feed-forward dynamic biasing (using the F processing block) applied to the PA schematic within ADS™. The value of the IMD_3 at the characterization power level P_{out} =14dBm in Figure 4.14 is -26dBc, which is identical to the optimum improved IMD_3 value given in Figure 4.11 (also simulated at P_{out} =14dBm) and which was obtained by externally applying a dynamic biasing signal V_e. The exact match of the improved IMD_3 value in Figure 4.11 and Figure 4.14 at the characterization power level of the 3-port PA representation clearly validates the accuracy and usefulness of the proposed 3-port representation for implementing the embedded feed-forward dynamic biasing aimed at PA linearization as shown in Figure 4.13.

The PA's P_{out} values for which the feed-forward dynamic biasing using F achieves significant IMD_3 improvement (2dB to 8dB improvement) ranges from its maximum output power (~20dBm) and up to 8dB back-off (~12dBm). It may be observed that this 8dB power range for which significant IMD_3 improvement is achieved using F is shifted slightly towards the higher range of PA output power levels with respect to P_{out} =14dBm, the characterization power level of the 3-port representation X. A similar shift is also observed in the power range

where PA linearity is improved when it is excited with a modulated signal (as shown in Figure 4.15) and will be discussed and explained in the succeeding paragraphs.

The same PA schematic is now excited using a modulated signal in ADS™ and its output linearity, calculated using ACP Reduction, i.e. *ACPR* values, is measured without and with the *F* block applied to it. The excitation used is an RF carrier modulated by a Forward Link CDMA signal with a signal bit-rate of 1.2288MHz, with 4 samples/bit and 256 total number of symbols. It is generated using the *PtRF_CDMA_IS95_FWD* component in the *Sources-Modulated* library in ADS™. The *F* block itself remains unchanged from the preceding discussion and is not determined using a modulated signal; as described earlier, *F* is determined using the proposed 3-port PA representation *X* derived using multi-tone signals and characterized at P_{out} ~14dBm. The PA's input modulated signal is processed by this computed *F* block.

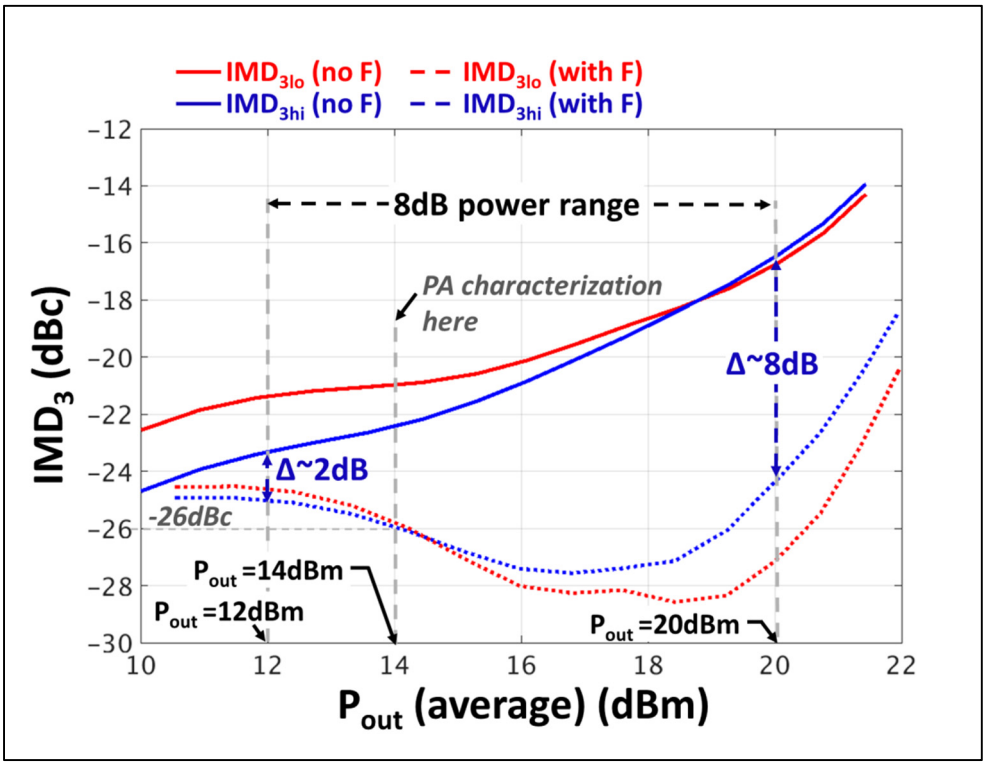

Figure 4.14 PA's simulated output IMD_3 vs. P_{out} without and with the *F* block for dynamic biasing of the PA module

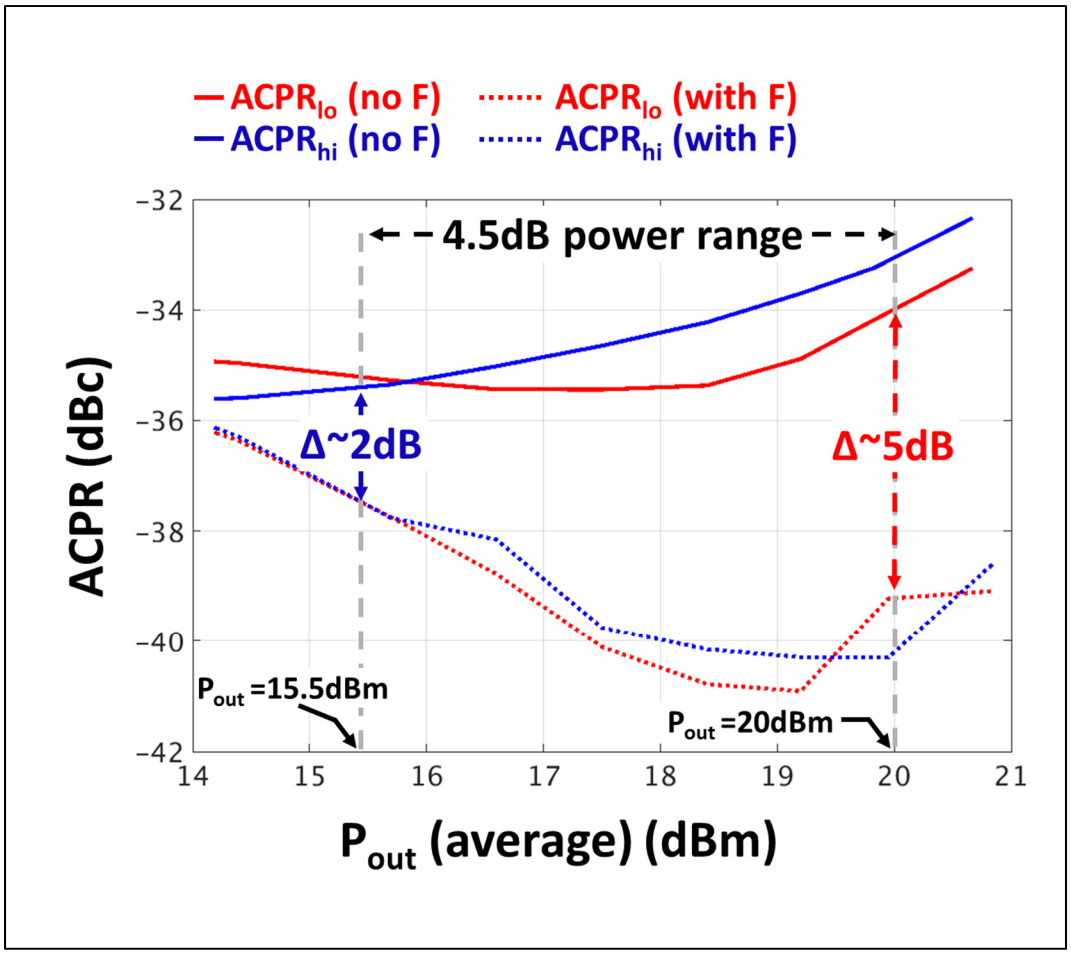

Figure 4.15 PA's simulated output *ACPR* vs. P_{out} without and with the *F* block for dynamic biasing of the PA module

As shown in Figure 4.15, an *ACPR* improvement of ~2dB to ~5dB is achieved for output power levels ranging from its maximum output power (P_{out} ~20dBm) to P_{out} ~15.5dBm. The modulated output signal centred at the RF carrier frequency for $P_{out(average)}$ =18.3dBm is also shown in Figure 4.16, and demonstrates the linearization that is achieved using the *F* block.

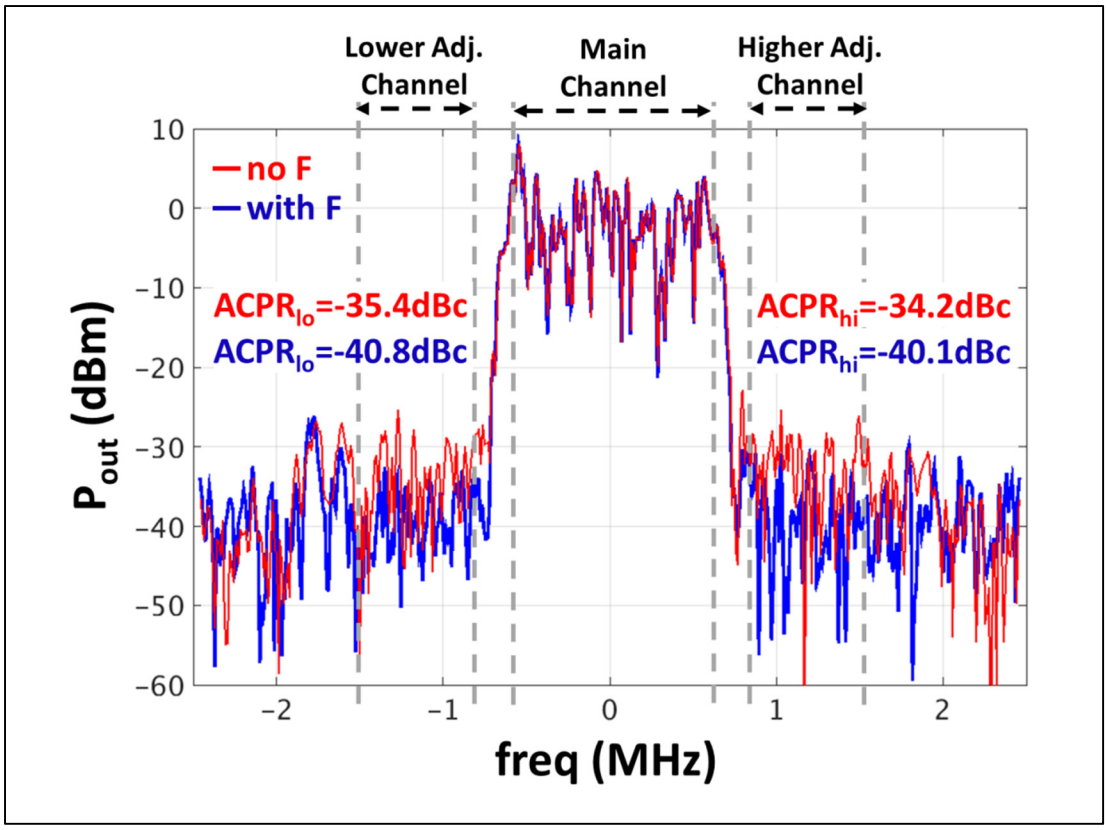

Figure 4.16 PA's simulated output signal (centred at carrier frequency) under modulated excitation at $P_{out}(avg)$~18.3dBm, without and with the *F* block for dynamic biasing of the PA module

The significant improvement in the PA's linearity at higher output power levels compared to the improvement at the PA characterization power P_{out}=14dBm, as observed in Figure 4.14 and Figure 4.15, is specific to this PA design and its nonlinear characteristics. The increased level of nonlinearity at these higher power levels for this particular PA design causes a heightened linearizing effect, dependent also on the specific pre-distortion function *F* implemented, as per Figure 4.13. Such a linearizing effect results in the observed IMD_3 and *ACPR* improvement for the higher range of output power levels. Such an improved linearity may be attributed to the phenomenon of sweet spots (J. Pedro, Carvalho, Fager, & García, 2004; Fager et al., 2004) that is well known among PA designers, and which the proposed pre-distortion in Figure 4.13 facilitates achieving for this specific PA design at power levels close to its maximum power. It is also worthwhile to note that there is a ~3.5dB shift in the

output power levels where significant ACPR improvement is achieved with a modulated signal (starting at P_{out} ~15.5dBm) when compared to the power levels where significant IMD_3 improvement is achieved with a multi-tone signal (starting at P_{out} ~12dBm). This shift stems from the difference between the PA's nonlinear behaviour that is captured during characterization with a 3-tone (sine wave) ~6dB peak-to-average envelope variation, and the PA's resulting nonlinear behaviour due to the CDMA envelope pattern (of the modulated signal) with a ~7.5dB peak-to-average envelope variation. Such a shift, however, may be compensated for by computing F based on the proposed 3-port PA representation X characterized at different output power levels, and which allows ensuring optimum PA linearity in the power range of interest where $ACPR$ improvement is sought, when it is excited using a modulated signal.

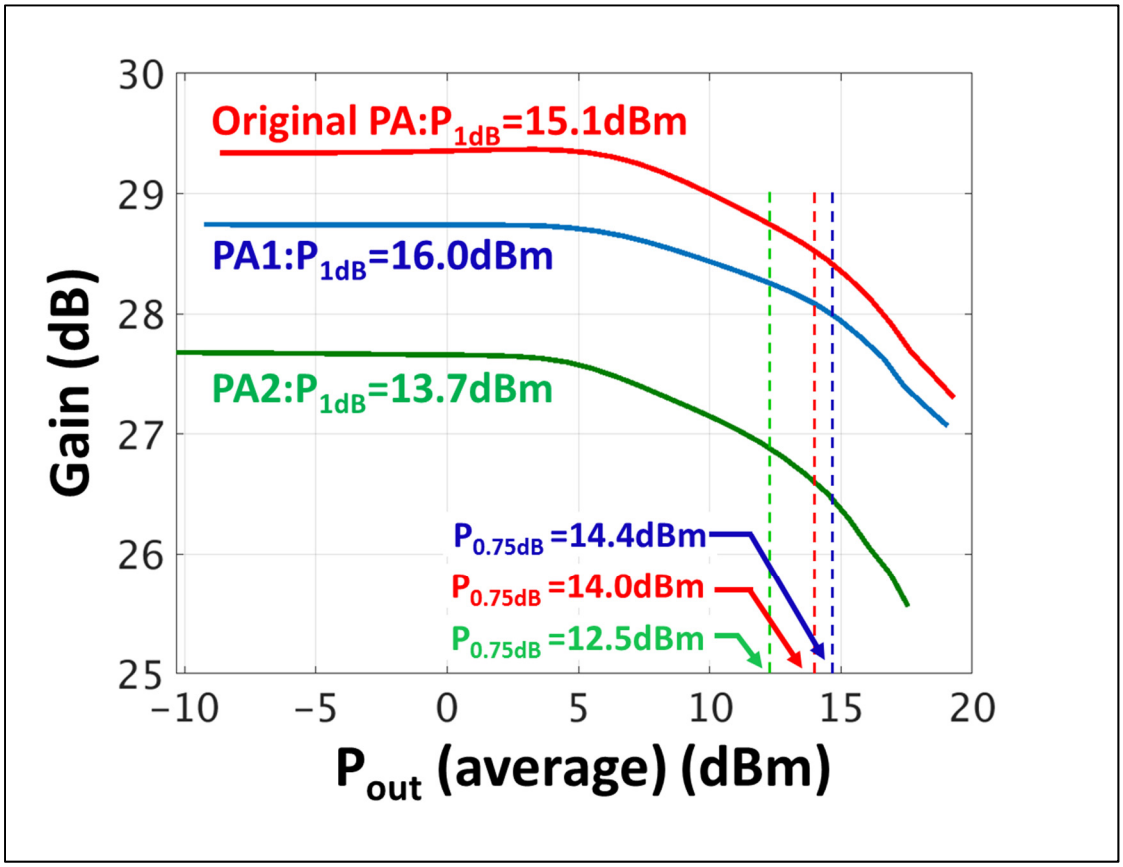

Figure 4.17 Comparison of *Gain* vs. P_{out} profile for the original PA and the new PA examples of Table 4.1 and Table 4.2

Therefore, the above results demonstrate the pertinence and usefulness of the proposed PA representation derived from a 3-tone characterization in the context of embedded adjustment of the applied dynamic biasing within the mobile unit, for linearity improvement under modulated excitation.

4.4.4 Application example 2: Use of proposed PA representation for performance compensation within embedded self-calibration against part-to-part variations

A second application example is now presented where the proposed 3-port PA representation X extracted in Section 4.4.2 is used to predict the embedded pre-distortion F (as in Figure 4.13) necessary for linearity optimization of a new PA. This new PA exhibits some level of performance variation with respect to the original PA that was characterized and linearized in Section 4.4.2 and Section 4.4.3, and the degree of this performance variation shown here may be typically expected from one PA part to another within different mobile equipment due to part-to-part deviations. It is demonstrated that by using an adjusted version of the original 3-port PA representation X, to compute an adjusted value of the pre-distortion F in Figure 4.13 that is then applied to the new PA as part of the embedded optimization within the mobile unit shown in Figure 4.13, enables a significant improvement of the new PA's linearity. This adjustment, performed using quasi-static measurements alone of the new PA's input and output power, accounts for the performance variation of the new PA with respect to the original PA, and the simple probing circuitry shown in Figure 4.13 that is necessary for these measurements makes it suitable for implementation in embedded self-calibration applications within the mobile communication equipment (Figure 4.1 and Figure 4.2).

As noted in Section 4.4.3, the parameters of the 3-port representation X that describe the original PA may be extracted by the PA manufacturer during an advanced engineering phase, and provided to the mobile equipment manufacturer. The automatic embedded adjustment (within the mobile equipment) of these original X parameters, to account for part-to-part PA performance variation, is what is referred to as our proposed embedded self-calibration.

For the demonstration here, the performance variation in the new PA is introduced by changing the bias condition of the original PA to force a change of 0.9dB in the output referred P_{1dB} (PA1 in Figure 4.17). In an actual implementation, a measurement of the *ratio* between the outputs of the same simple probing circuitry at the PA's input and output (Figure 4.13) should allow detecting such part-to-part variations in the PA's compression with respect to an original PA specification.

Table 4.1 shows PA1's IMD_{3hi} values under constant DC bias obtained using simulation of the PA1 schematic in ADS^{TM} for an output power range of 0.8dB around P_{out} ~14.4dBm. IMD_{3lo} values are not shown to keep Table 4.1 concise. The power level of 14.4dBm is chosen for our analysis since it is the output power level where the gain of PA1 has compressed by ~0.75dB (hereafter referred to as $P_{0.75dB}$), and the proposed 3-port representation X for the original PA was extracted at P_{out} ~14.0dBm in Section 4.4.2, which is also the $P_{0.75dB}$ for the original PA. This $P_{0.75dB}$ point is expected to be in the lower range of power levels where linearization through pre-distortion using F is useful, as observed in Figure 4.14.

We now proceed with adjusting the original 3-port PA representation X, to account for the performance variation of PA1 compared to the original PA, to be used for predicting the adjusted pre-distortion F necessary to optimize PA1's linearity. For this, it is only required to adjust the coefficients of polynomial G (i.e. a_1, a_3 and a_5 within X in Figure 4.13) starting from their original values provided by the PA manufacturer, by measurement of the amplitudes only of PA1's input three tones and the output three tones (i.e. at frequencies f_c-f_x, f_c and f_c+f_x) and only at the power level of interest (i.e. at P_{out}=14.4dBm). In an actual implementation, this would be done through the input-output probes in Figure 4.13, over the narrow power range of envelope variation of the 3-tone signal, hence requiring only simple envelope detector circuitry. Such simplicity holds promise for its use in embedded self-calibration applications that are based on incorporating the calibration set-up within the mobile equipment, since the adjustment requires only a minimum number of relatively simple measurements.

The optimum dynamic-bias values predicted by pre-distortion through the adjusted F computed using this adjusted 3-port PA representation are also shown in Table 4.1 (in blue). As demonstrated, IMD_3 improvement Δ of 2.02dB to 3.30dB over the constant-bias case is possible for the targeted power range when using these predicted dynamic-bias values, and represents a significant improvement in PA1's linearity. This IMD_3 improvement clearly demonstrates the effectiveness of the proposed embedded self-calibration to be used for pre-distortion of the new PA, using the set-up embedded within the mobile unit shown in Figure 4.13.

The difference in the IMD_3 improvement at its $P_{0.75dB}$ output power level between the original PA (~4dB at P_{out}=14dBm, Figure 4.14) and PA1 (2.65dB at P_{out}=14.4dBm, Table 4.1) may be explained as a result of the two PAs operating with different bias conditions, which translates into the applied pre-distortion having a different degree of linearizing effect.

Table 4.1 Simulated vs. predicted values of optimum dynamic bias for PA1

P_{out} (average) of PA1 (dBm)		**14.0**	**14.2**	**14.4**	**14.6**	**14.8**
Values under constant (DC) bias						
IMD_{3hi} (dBc)		-22.84	-22.75	-22.70	-22.58	-22.50
Values from pre-distortion predicted using Adjusted 3-port PA Representation (*G* only)						
Dynamic Bias	**Value (mV)**	37.6	38.5	39.8	40.5	42.0
IMD_{3hi}	**Value (dBc)**	-24.86	-25.10	-25.35	-25.60	-25.80
	Δ (dB)	**2.02**	**2.35**	**2.65**	**3.02**	**3.30**

Table 4.2 Simulated vs. predicted values of optimum dynamic bias for PA2

P_{out} (average) of PA2 (dBm)		**12.1**	**12.3**	**12.5**	**12.7**	**12.9**
Values under constant (DC) bias						
IMD_{3hi} (dBc)		-23.25	-23.15	-23.00	-22.90	-22.75
Values from pre-distortion predicted using Adjusted 3-port PA Representation (*G* only)						
Dynamic Bias	**Value (mV)**	30.8	31.7	32.5	33.4	34.2
IMD_{3hi}	**Value (dBc)**	-27.75	-28.00	-28.25	-28.50	-28.80
	Δ (dB)	**4.50**	**4.85**	**5.25**	**5.60**	**6.05**

A more drastic change in the PA's performance is now considered by forcing a change of 1.4dB in the PA's output referred P_{1dB} (PA2 in Figure 4.17). This time, both the bias and the output matching network are changed. The comparison of IMD_3 levels of PA2 with or without pre-distortion through F is again made at the $P_{0.75dB}$ output power level (12.5dBm for PA2) and is shown in Table 4.2. It can be seen that the IMD_3 levels are significantly improved (by more than 5dB) compared to the constant-bias case, by pre-distortion using the adjusted 3-port representation that accounts for the performance variation of PA2 compared to the original PA. The higher levels of IMD_3 improvement for PA2 in Table 4.2 compared to PA1 in Table 4.1 may be attributed to PA2 operating under stronger nonlinearities, given the change in both the bias and the output matching network for PA2. The same heightened linearization effect due to the sweet-spot phenomenon discussed in Section 4.4.3 is thus introduced.

Note that the resulting improvement in IMD_3 through pre-distortion is function of the assumption in the examples shown in Table 4.1 and Table 4.2 of updating the G coefficients only, and using very simple probe circuitry. Our analysis in this thesis is restricted to the use

of such simple probes only, within an embedded self-calibration set-up in the mobile unit. However, simulations show that by adjusting the coefficients of P in X, in addition to the coefficients of G as described earlier, allows even further improvement of the IMD_3 levels.

This suggests an interesting possibility of using the proposed PA representation to optimize PA linearity further while accounting for part-to-part variation. It would require a one-time measurement followed by adjustment, based on computation using the proposed 3-port representation. A potential approach to accomplish this is to use more precise envelope detectors in the probing circuitry, but over a narrow power range only, for the measurement of two additional output tones (at intermodulation frequencies f_c-$2f_x$ and f_c+$2f_x$) for the new PA, therefore allowing an adjustment of the coefficients of the P polynomial. The G coefficients may be left to the values obtained through the 3-tone quasi-static measurements for the adjusted 3-port representation in Table 4.1 and Table 4.2. This measurement of the two additional output tones, for the adjustment of the coefficients of the P polynomial, is performed with a 1-tone dynamic-bias signal at frequency f_x applied to the bias node of the PA. It can be performed from one mobile equipment to another, and it is sufficient to perform the measurement at the PA's rated power level only. We discuss such a possible application again with greater detail in Section 4.8 towards the end of the current chapter.

4.5 Experimental validation of proposed three-port representation

4.5.1 Power amplifier and device technology

For experimental validation of the proposed 3-port PA representation, the SE5003 WiFi PA from Skyworks Solutions, Inc. is used, but modified by Skyworks to allow access to the internal biasing circuitry specifically for the tests described here. This modification enables the application of an envelope-dependent dynamic-bias signal to the second or the third PA stages (or to both). The PA is fabricated using Indium Gallium Phosphide (InGaP) Heterojunction Bipolar Transistor (HBT) technology. It is capable of better than 3% EVM at 25dBm output power (802.11a signals) from 5.15GHz to 5.9GHz, has a P_{1dB} of about 32dBm and a gain of about 32dB (Skyworks Solutions, October 2013).

4.5.2 Test set-up

Figure 4.18 shows the schematic of the test set-up for the PA dynamic biasing experiment discussed in this section. The RF and Baseband Generator is used to synthesize the RF (at node *A*) and the baseband (at node *B*) signals which are applied to the input node (port 1) and bias node (port 3) respectively of the PA. The spectral content at nodes 1, 2 and 3 (node 2 being the PA's output node) are measured with spectrum analyzers, while power measurements at nodes 1 and 2 are done using a power meter.

An essential requirement for the testbench in Figure 4.18 is that the phase of the baseband multi-tone signal at port 3 is precisely known, calibrated and controlled to extract *phase-coherent* relationships between the signals at ports 1, 2 and 3, in addition to allowing the precise control of their amplitude. While the measurement, calibration and control of the amplitude is easily achieved, phase control must be achieved such that at any instant of time, the phase at nodes 1, 2 and 3 are calibrated with respect to a single time reference. For instance, refer to the time-domain illustration of the envelope-varying signals at ports 1, 2 and 3 in Figure 4.18. At any instant of measurement t, the phase of the signals at ports 1, 2 and 3 must be measured/controlled, which *requires* knowing that $t=0$ at port 1 corresponds (in this illustrated example) to $t=t_1$ at port 3 and $t=t_2$ at port 2. The phase measurements would then be *phase-coherent*. Such a phase-coherence may be achieved by using the oscilloscope in Figure 4.18 to perform an initial calibration of the phase measurements at these ports, i.e. a calibration to calculate t_1 and t_2 in Figure 4.18, such that all subsequent phase measurements for the set-up use a single time scale referenced to t=0 at port 1.

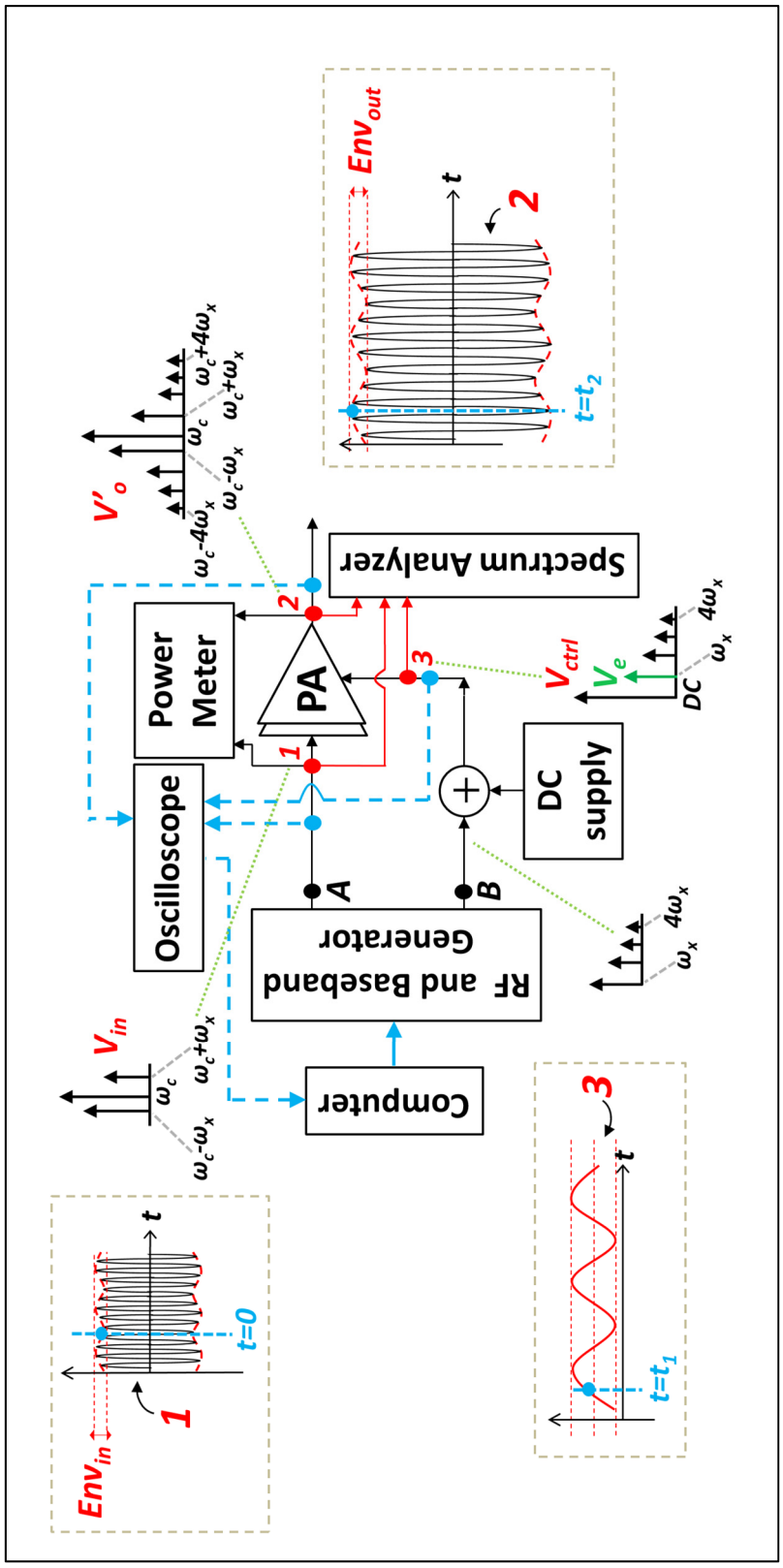

Figure 4.18 Test set-up for experimental validation of proposed 3-port PA representation

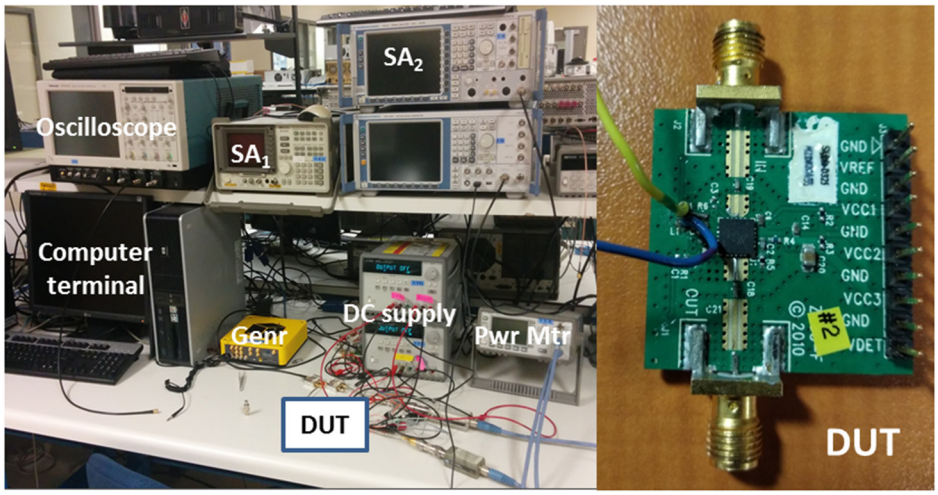

Figure 4.19 Photograph of experimental test set-up shown in Figure 4.18.
A photograph of the SE5003 PA test-board (DUT) is also shown

In other words, the RF and Baseband Generator accomplishes this using the oscilloscope measurements of the signals at ports 1, 2 and 3 (shown by blue dotted arrows in Figure 4.8) together with MATLAB^{TM}-based algorithms running on the computer that controls the equipment, to adjust the phase at nodes 1, 2 and 3 with respect to one single time reference. If phase measurements of the signals at these ports are done with independent time references for each, such a phase-coherence would be lost and the consistency in the phase measurements required for the formulations presented in Section 4.3.1 will be impossible to achieve.

A photograph of the laboratory test set-up is given in Figure 4.19.

4.5.3 Measurements and validation

The procedure to extract the proposed 3-port PA representation as detailed in Section 4.3.2 is now applied to the SE5003 GaAs HBT WiFi PA using a three-tone RF signal with a frequency spacing of 1.5MHz (i.e. a total signal bandwidth of 3MHz) and for P_{out}

(*average*)=29.2dBm. The PA is, therefore, being operated in the vicinity of its maximum rated linear output power (P_{1dB}~32dBm). The proposed 3-port representation is characterized with the multi-tone dynamic-bias signal V_{ctrl} (with tones at frequencies ω_x, $2\omega_x$, …$4\omega_x$) applied to the HBT base in the PA's third stage, since it is observed to have a significantly higher effect on the PA's linearity than applying it to the PA's second stage. The extracted representation is similar in form to (4.19)-(4.20) but with different coefficients, and is not shown here for conciseness.

Note, however, that a third-order *P* polynomial is found to be necessary to accurately capture the PA's nonlinearity under dynamic biasing for the experimental validation discussed here. This increase in the order of *P* is required to account for the more significant nonlinearities associated with the particular HBT PA design used here compared to the CMOS PA discussed in Section 4.4.

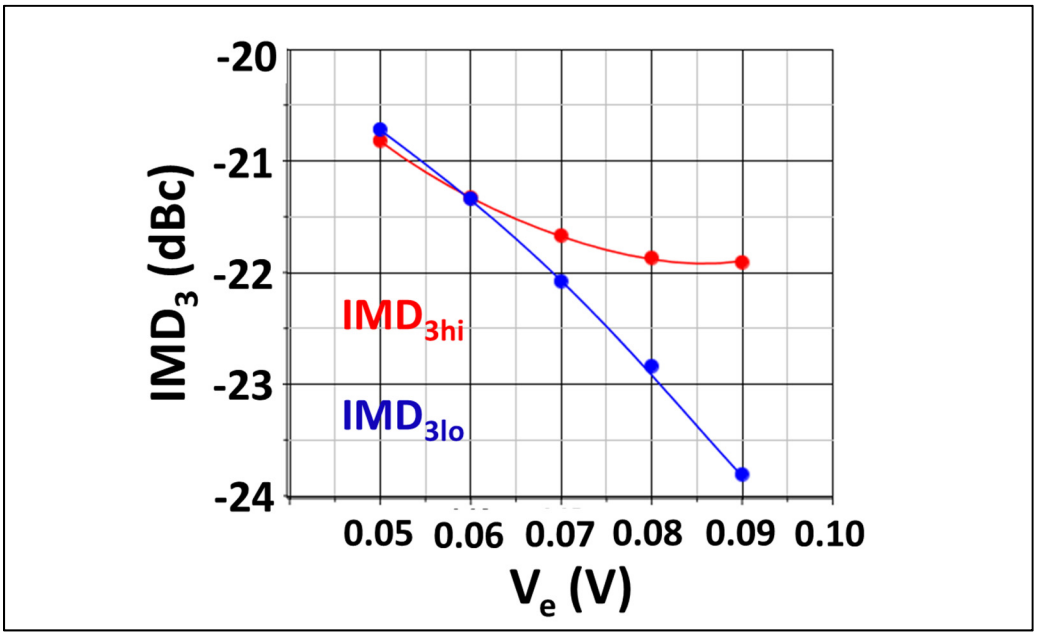

Figure 4.20 Measured values (dotted markers) and predicted values (solid traces) of the PA's *IMD3* under dynamic-bias tone V_e. V_e is the V_{ctrl} tone at ω_x with the phase kept constant at 80^0. Other tones are present in V_{ctrl} but are not varied. The PA's P_{out} (*average*) is 29.2dBm

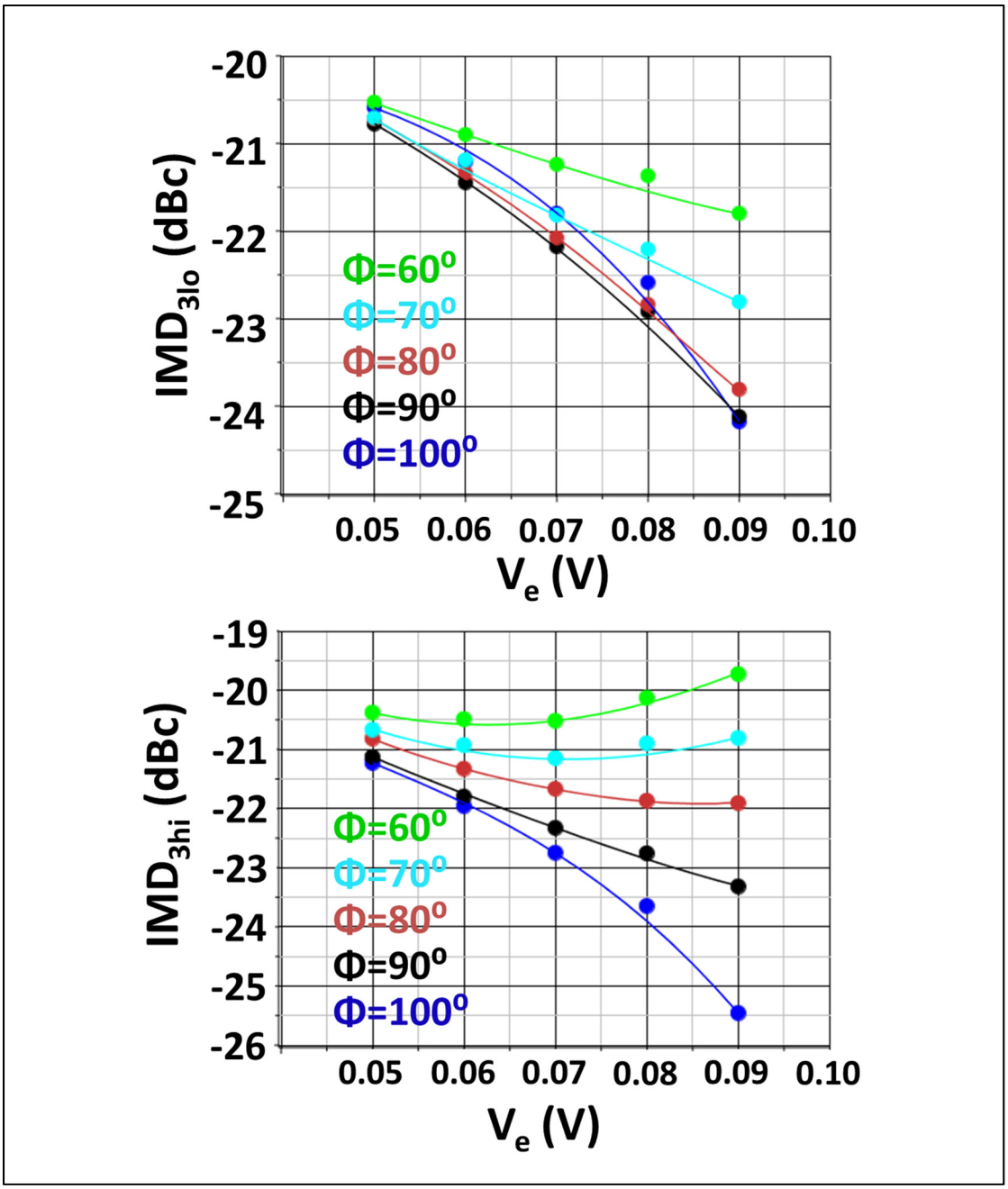

Figure 4.21 Measured values (dotted markers) and predicted values (solid traces) of the PA's *IMD3* under phase variation, in addition to amplitude variation, of its dynamic bias. The PA's P_{out} (*average*) is 29.2dBm

With the extraction of the proposed 3-port PA representation complete, it is now used to predict the necessary pre-distortion through dynamic bias, i.e. the required V_{ctrl} signal at port

3 in Figure 4.18, in order to linearize the DUT at the characterized power level. Because the variation of the tone V_e in the bias signal V_{ctrl} at frequency ω_x is found to have the greatest impact on PA linearity, the plots in the discussion that follows shows the variation of the PA's output IMD_3 with the magnitude and phase of this V_e tone only, even though higher frequency tones (at $2\omega_x$, $3\omega_x$, $4\omega_x$) are present in the bias signal during both PA characterization and in the pre-distortion test-cases that are described next.

As shown in Figure 4.20, the proposed 3-port PA representation allows predicting with negligible error the pre-distortion through the dynamic-bias tone V_e required to improve the PA's output IMD_3 by up to 3dB, using amplitude control only of the V_e tone. Further IMD_3 improvement is also possible by varying the phase of the V_e tone in addition to its amplitude. As shown in Figure 4.21, the proposed 3-port PA representation also allows accurately predicting the amplitude and phase (0.09V, $\angle 100^0$) of this V_e tone that is necessary to achieve more than 4dB of IMD_3 linearization.

4.6 Comparison with modified Volterra series

Of the recent advances in analytical PA representations, (Gibiino, Avolio, Schreurs, Santarelli, & Filicori, 2016) describes a 3-port Volterra-based representation for supply-modulated RF PAs and derived with a 2-tone excitation. Because of its apparent similarity to the proposed 3-port representation, it is useful to discuss the significant differences between the two approaches in terms of their intended application, the advantages and the disadvantages.

(Gibiino, Avolio, Schreurs, Santarelli, & Filicori, 2016) uses a first-order truncation of the full Volterra series to reduce the complexity of extracting the higher-order kernels. The first-order kernel values in (Gibiino, Avolio, Schreurs, Santarelli, & Filicori, 2016) are shown to vary as a function of three variables - the RF Input Power, the DC supply and the modulation signal bandwidth (Gibiino, Avolio, Schreurs, Santarelli, & Filicori, 2016, Figure 5, Figure 6, Figure 7). Since the kernels are derived for a large range of these three variables, they

remove the necessity for real-time coefficient updates that may be associated with tuned PA representations (Gibiino, Avolio, Schreurs, Santarelli, & Filicori, 2016, Page 9, Paragraph 1], tuned PA representations according to (Gibiino, Avolio, Schreurs, Santarelli, & Filicori, 2016) being those that are valid only when used under identical operating conditions as that during characterization. This is an interesting feature of the PA representation in (Gibiino, Avolio, Schreurs, Santarelli, & Filicori, 2016). On the other hand, such a large number of kernel values require being stored in some form (for example, as look-up tables) which allows them to be structured as nonlinear filters which nonlinearly change versus time (Gibiino, Avolio, Schreurs, Santarelli, & Filicori, 2016, Page 6]. Dynamically addressing and updating lookup tables which are functions of three separate variables (the RF Input Power, the DC supply and the modulation signal bandwidth), as part of a training sequence, makes it too complex for use in the proposed context of embedded self-calibration within mobile equipment to account for part-to-part variations (Figure 4.1, Figure 4.2). This is because of the complexity of the probing interfacing and training sequence that would be required to implement a dynamic updating of the look-up table as a function of these three separate variables. In contrast, it was shown in Section 4.4 that with the proposed 3-port representation, a relatively small number of coefficients (of G and P) require being stored. These are extracted (and adjusted) using a simple training sequence based on a minimum number of relatively simple measurements performed using a low-complexity probing circuitry, and successfully answers the requirements of embedded self-calibration application within mobile equipment.

It was also shown in Figure 4.11 that the proposed 3-port PA representation allows predicting with negligible error an improved IMD_3 of -26dBc via pre-distortion for the SOI CMOS PA in Section 4.4. Similarly, the experimental values in Figure 4.21 shows that the proposed 3-port PA representation accurately captures the nonlinearities and allows the prediction of the pre-distortion necessary to achieve an improved IMD_3 of less than -25dBc for an industry-designed GaAs PA. The error in prediction of the IMD_3 for this GaAs PA using the proposed representation is negligible (< 0.1dB, Figure 4.21) when the PA is tested at power levels in the vicinity of its P_{1dB} output power (i.e. when PA nonlinearity is significant). These error

values are comparable to those associated with using the Volterra-based PA representation in (Gibiino, Avolio, Schreurs, Santarelli, & Filicori, 2016) for predicting output IMD_3 levels, while operating the PA under similar degrees of nonlinearity and comparable IMD_3 under dynamic conditions (IMD_3~-25dBc in (Gibiino, Avolio, Schreurs, Santarelli, & Filicori, 2016, Figure 9(a))). Therefore, the proposed 3-port PA representation in this thesis allows accurately capturing PA nonlinear behaviour that is of the same degree as that discussed in (Gibiino, Avolio, Schreurs, Santarelli, & Filicori, 2016), but without the significantly more complex training sequences associated with extracting Volterra kernels.

Additionally, it has been shown in Section 4.5 that it was necessary to increase the order of P from two to three to capture with minimal error (<0.1dB) the effect of the dynamic biasing signal on a GaAs HBT PA's nonlinearity, when the PA is operating in a significantly nonlinear region (P_{out} ~29.2dBm). Increasing to the third-order the kernels in Chapter 1, equation (1.2) for the Volterra-based representation in (Gibiino, Avolio, Schreurs, Santarelli, & Filicori, 2016) has not been demonstrated, nor the accompanying complexity that would ensue for such higher-order Volterra characterization, given the considerable challenges associated even with the extraction of first-order Volterra kernels (Gibiino, Santarelli, Schreurs, & Filicori, 2017).

4.7 Application of proposed three-port representation to closed-loop PA

Closed-loop PA architectures relying on feedback have been widely demonstrated to improve PA performances. For example, (Kang, Baek, & Hong, 2017) improves PA linearity by using negative feedback through active elements for gain compensation at high power levels when the PA's compression is significant. (Thangarasu, Ma, & Yeo, 2017; El-Shennawy, Joram, & Ellinger, 2016) uses negative feedback in VGA architecture to regulate the system's overall gain. The proposed 3-port PA representation is useful for both PAs and VGAs under closed-loop operation, using either negative or positive feedback.

In this section, its usefulness is highlighted by applying it to the proposed positive envelope feedback linearization scheme described in details in Chapter 2 and Chapter 3, where the PA's output envelope signal is applied in positive feedback to the bias node (Sharma, Constantin, & Soliman, 2017; Sharma & Constantin, January 2018; Sharma & Constantin, April 2018). To the best of the author's knowledge, for the first time, an analytical approach using a 3-port representation is used to predict the conditions for closed-loop stability in an envelope feedback system as well as the design requirements of the feedback elements for optimum linearity, without relying solely on trial-and-error to optimize the value of the loop elements.

While this is demonstrated here in the context of positive envelope feedback PA design through sections 4.7.1 to 4.7.5, the proposed PA representation may also be used for other closed-loop PAs within an embedded self-calibration set-up in the mobile unit (such as the set-up in Figure 4.1, Figure 4.2) to verify PA stability as well as optimize PA linearity. This aspect is discussed in Section 4.8.

4.7.1 Description of Device Under Test

The device under test (DUT) is shown in Figure 4.22 and is identical to the PA design in Section 3.2. This PA design schematic is again shown here for the reader's easy reference.

Both simulation results of the PA schematic (Figure 4.22(a)) and experimental measurements on the prototype (Figure 4.22(b)) are referred to here and indicated appropriately. As described in detail in Section 3.2, the 5.4GHz PA and the envelope detector are fabricated using SOI-CMOS 0.18um technology from TowerJazz. The three-stage flip-chip PA is interfaced to the PCB via a 6-layer MCM. The reader may refer to Section 3.2 for further details regarding this PA design, and to Chapter 2 and Chapter 3 for the design of PAs using positive envelope feedback.

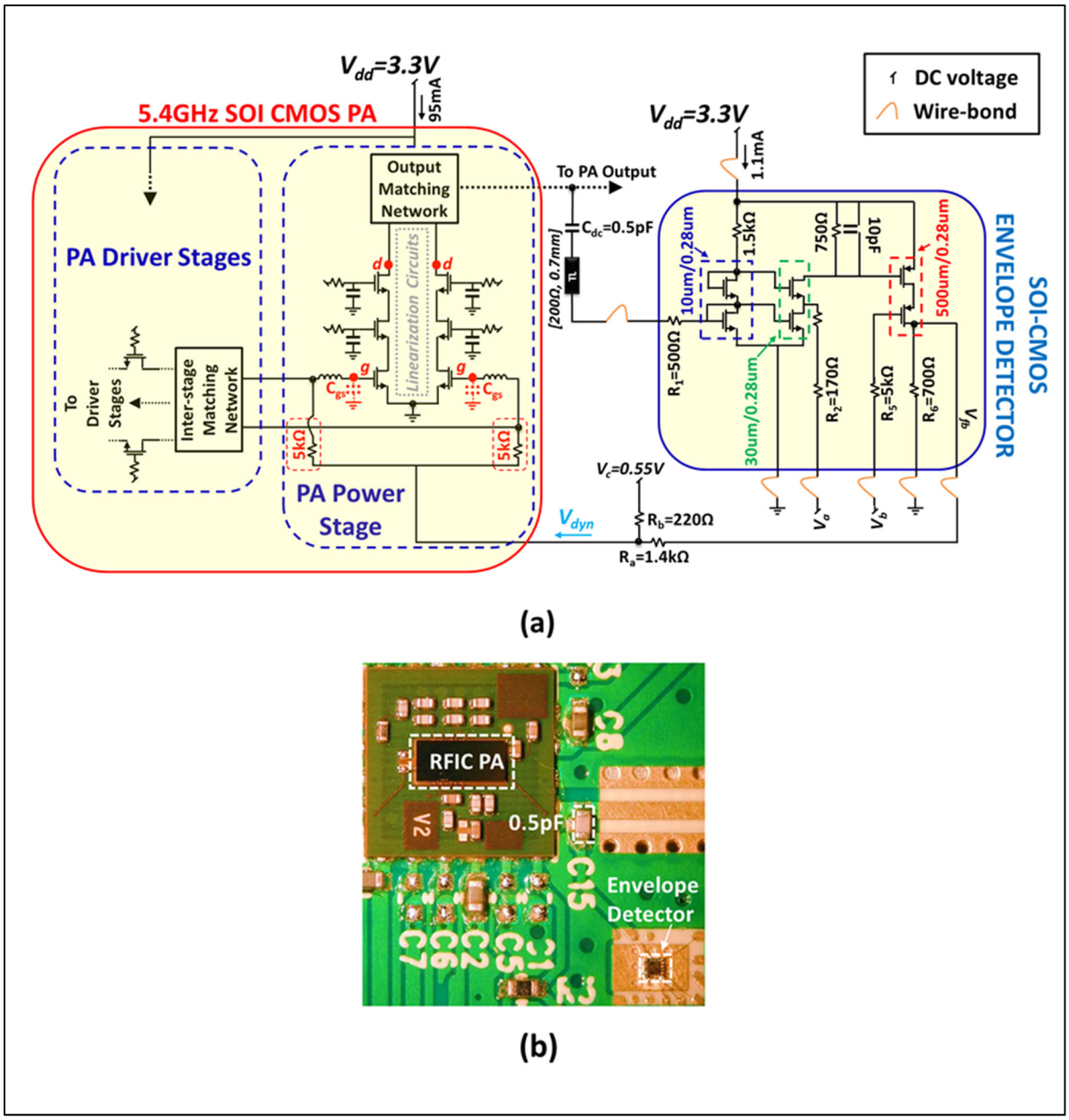

Figure 4.22 (a) Simplified schematic showing closed-loop PA using positive envelope feedback (b) Prototype system with PA and Envelope Detector

Figure 4.23 gives a schematic representation of the closed-loop PA using positive envelope feedback on the left and converts it into an open-loop system using the proposed 3-port PA representation in this thesis (indicated by *X*) on the right. The feedback circuit in Figure 4.23 is the high input impedance system composed of an envelope detector and a voltage shifter,

as shown in Figure 4.22 and detailed in Chapter 2 and Chapter 3. As also described in the preceding chapters, two parameters critical to the implementation shown in Figure 4.22 are the threshold and the gain conversion slope of the detector used in the feedback circuit. Their underlying circuit operation and characteristics are described in Section 3.1.2 and Section 3.2.2, and the values of these two parameters are voltage-controlled. In the schematic of Figure 4.23, these two voltage controls are represented by signals A and B. Signal A corresponds to signal V_a in Figure 4.22(a), which sets a threshold at the source of an NMOS comparator. Signal B corresponds to signal V_b in Figure 4.22(a), which controls the gain of an output PMOS stage.

X is first extracted using the procedure given in Section 4.3.2. At the end of this extraction procedure, the coefficients of complex polynomials G and P that constitute X in Figure 4.23 are known for power levels where the PA is under gain compression, and where the application of positive envelope feedback is effective at improving PA performance. The extracted representation is similar in form to (4.19) and (4.20) and is not shown here for conciseness.

4.7.2 Expression for conversion gain

For determining the expression of loop stability, the PA's conversion gain (C) from the dynamic-bias signal at node V_{ctrl} to the output envelope signal at node V_o in Figure 4.23 is first calculated. For this, the 3-port PA representation (X in Figure 4.23) is excited using a single small-signal baseband tone V_e (at frequency ω_x) at the bias node, a single RF tone V_i at the input node and measuring the resulting output multi-tone signal V_o. The value of V_i is chosen such that the PA is operating under gain compression. For V_o, the measurement of amplitudes alone and limited to that of the three primary tones (i.e. at frequencies ω_c-ω_x, ω_c and ω_c+ωx) is sufficient, given that the IMD_3 tones (and other higher-order tones) have a negligible contribution to the conversion gain. Using the formulations in Section 4.3.1 for the 3-port PA representation, the expression of the PA's conversion gain (C) is now calculated when the input excitation is V_i and the bias tone is V_e.

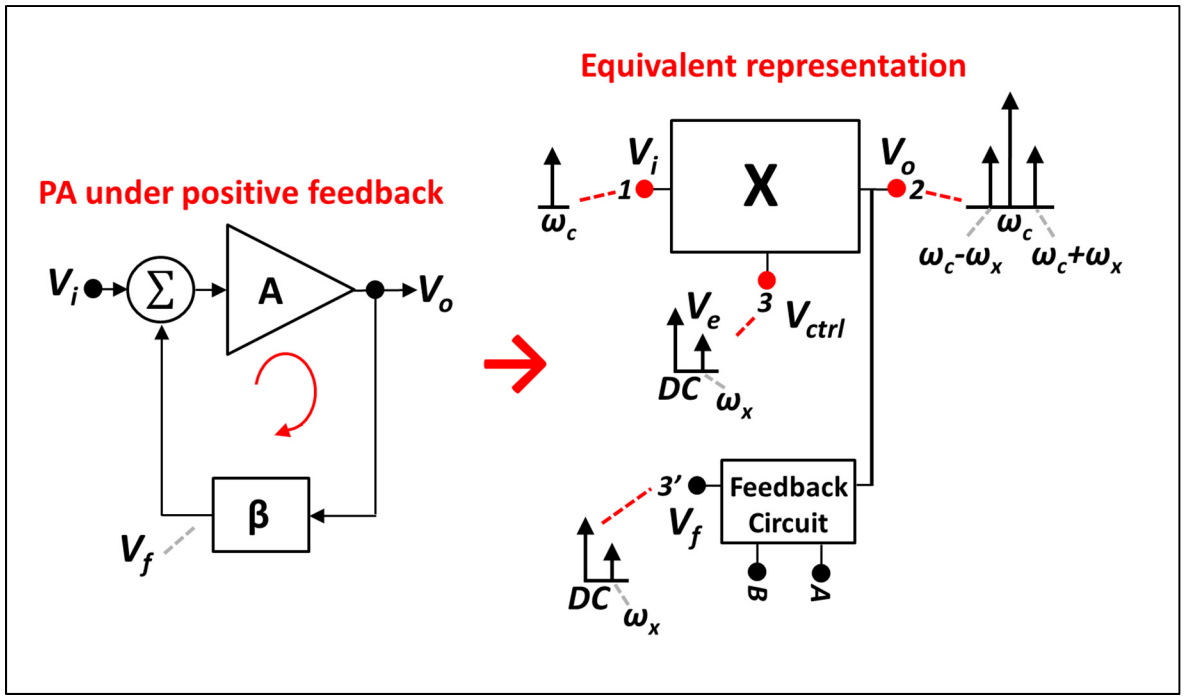

Figure 4.23 Closed-loop PA under positive feedback, and equivalent open-loop form using our proposed 3-port PA representation

For determining this conversion gain, note that the value of the amplitudes only of the baseband bias signal and the PA's output envelope (both at frequency ω_x) is necessary, and there is no requirement to measure the absolute phase value of the signals at the nodes V_i, V_o and V_{ctrl}, i.e. their phase with respect to a single time reference as described in Section 4.5.2.

Therefore, these absolute values of the phase of the signals are ignored without any loss of generality for the formulations derived here, and the amplitudes only of V_i, V_o and V_e are considered. (4.4) and (4.6) therefore reduce to equations (4.21) and (4.22).

$$v_i(t) = V_i(\omega_c) \cdot cos(\omega_c t) \tag{4.21}$$

$$v_e(t) = V_e \cdot cos(\omega_x t) \tag{4.22}$$

Assuming a second-order polynomial for P gives expression (4.23)-(4.25) for ΔV_a, where the number of tones are restricted to the three primary tones at frequencies ω_c, $\omega_c+\omega_x$ and $\omega_c-\omega_x$.

$$\Delta V_a(\omega_c) = p_{011} \cdot V_e + p_{012} \cdot {V_e}^2 \tag{4.23}$$

$$\Delta V_a(\omega_c + \omega_x) = p_{111} \cdot V_e + p_{112} \cdot {V_e}^2 \tag{4.24}$$

$$\Delta V_a(\omega_c - \omega_x) = p_{-111} \cdot V_e + p_{-112} \cdot {V_e}^2 \tag{4.25}$$

Here, p_{011}, p_{012}, p_{111}, etc. refer to the coefficients of polynomial P. For example, consider the coefficient p_{-112}. Here the third index 2 represents that it captures the contribution of the 2nd-order term V_e^2 to the 1st side-tone $\Delta V_a(\omega_c-\omega_x)$ (given by index -1), V_e being the value of the $1\cdot\omega_x$ frequency tone in the bias signal (given by index 1).

Using (4.23), (4.24) and (4.25) gives the following unilateral expression for $v_a(t)$.

$$\begin{aligned} v_a(t) = {} & V_i(\omega_c) \cdot cos(\omega_c t) + \left(p_{011} \cdot V_e + p_{012} \cdot {V_e}^2\right) \cdot cos(\omega_c t) \\ & + \left(p_{111} \cdot V_e + p_{112} \cdot {V_e}^2\right) \cdot cos((\omega_c + \omega_x)t) \\ & + \left(p_{-111} \cdot V_e + p_{-112} \cdot {V_e}^2\right) \cdot cos((\omega_c - \omega_x)t) \end{aligned} \tag{4.26}$$

i.e.

$$v_a(t) = p_0 \cdot cos(\omega_c t) + p_1 \cdot cos((\omega_c + \omega_x)t) + p_{-1} \cdot cos((\omega_c - \omega_x)t) \tag{4.27}$$

where

$$p_0 = V_i(\omega_c) + V_e \cdot (p_{011} + p_{012} \cdot V_e) \tag{4.28}$$

$$p_1 = V_e \cdot (p_{111} + p_{112} \cdot V_e) \tag{4.29}$$

$$p_{-1} = V_e \cdot (p_{-111} + p_{-112} \cdot V_e) \tag{4.30}$$

Applying (4.27) as input to the 5th-order polynomial G and considering only the resulting amplitudes at the three primary frequency tones shown in Figure 4.23 gives the following value of the output signal V_o.

$$v_o(t) = r_0 \cdot cos(\omega_c t) + r_1 \cdot cos((\omega_c + \omega_x)t) + r_{-1} \cdot cos((\omega_c - \omega_x)t) \tag{4.31}$$

where

$$\begin{aligned} r_0 = a_1 \cdot p_0 + a_3 \cdot \left\{ \frac{3}{4} {p_0}^3 + \frac{3}{2} p_0 {p_1}^2 + \frac{3}{2} p_0 {p_{-1}}^2 + \frac{3}{2} p_0 p_1 p_{-1} \right\} + a_5 \\ \cdot \left\{ \frac{5}{8} {p_0}^5 + \frac{15}{8} p_0 {p_1}^4 + \frac{15}{8} p_0 {p_{-1}}^4 + \frac{15}{4} {p_0}^3 {p_1}^2 + \frac{15}{4} {p_0}^3 {p_{-1}}^2 \right. \\ \left. + \frac{15}{4} p_0 {p_1}^3 p_{-1} + \frac{15}{4} p_0 p_1 {p_{-1}}^3 + \frac{15}{2} p_0 {p_1}^2 {p_{-1}}^2 + 5 {p_0}^3 p_1 p_{-1} \right\} \end{aligned} \tag{4.32}$$

$$\begin{aligned} r_1 = a_1 \cdot p_1 + a_3 \cdot \left\{ \frac{3}{4} {p_1}^3 + \frac{3}{2} p_1 {p_0}^2 + \frac{3}{4} p_{-1} {p_0}^2 + \frac{3}{2} p_1 {p_{-1}}^2 \right\} + a_5 \\ \cdot \left\{ \frac{5}{8} {p_1}^5 + \frac{15}{4} {p_0}^2 {p_1}^3 + \frac{15}{8} {p_0}^2 {p_{-1}}^3 + \frac{15}{4} {p_1}^3 {p_{-1}}^2 + \frac{15}{8} p_1 {p_0}^4 \right. \\ \left. + \frac{15}{8} p_1 {p_{-1}}^4 + \frac{15}{2} {p_0}^2 p_1 {p_{-1}}^2 + \frac{5}{4} {p_0}^4 p_{-1} + \frac{45}{8} {p_0}^2 {p_1}^2 p_{-1} \right\} \end{aligned} \tag{4.33}$$

$$\begin{aligned} r_{-1} = a_1 \cdot p_{-1} + a_3 \cdot \left\{ \frac{3}{4} {p_{-1}}^3 + \frac{3}{2} p_{-1} {p_0}^2 + \frac{3}{4} p_1 {p_0}^2 + \frac{3}{2} p_{-1} {p_1}^2 \right\} + a_5 \\ \cdot \left\{ \frac{5}{8} {p_{-1}}^5 + \frac{15}{4} {p_0}^2 {p_{-1}}^3 + \frac{15}{8} {p_0}^2 {p_1}^3 + \frac{15}{4} {p_{-1}}^3 {p_1}^2 + \frac{15}{8} p_{-1} {p_0}^4 \right. \\ \left. + \frac{15}{8} p_{-1} {p_1}^4 + \frac{15}{2} {p_0}^2 p_{-1} {p_1}^2 + \frac{5}{4} {p_0}^4 p_1 + \frac{45}{8} {p_0}^2 {p_{-1}}^2 p_1 \right\} \end{aligned} \tag{4.34}$$

The small asymmetry due to the higher-order terms in the two output side-tones of amplitude r_1 and r_{-1}, as shown in their expansions given by (4.33) and (4.34), has a negligible effect on the output envelope amplitude, whose value is then given by (4.35).

$$Env(V_o) \approx 2r_1 \approx 2r_{-1} \tag{4.35}$$

The PA's conversion gain (C) from the bias node to the output node is now given by (4.36).

$$C(V_i, V_e) = \frac{Env(V_o)}{V_e} \approx \frac{2r_1}{V_e} \tag{4.36}$$

A better understanding of the contribution of V_i and V_e to the conversion gain given by (4.36) can be obtained by simplifying (4.36) after its expansion. For this purpose, coefficient a_5 is set to zero and only the first few significant terms are considered. The resulting simplified expression is given by (4.37), and its compact representation by (4.38).

$$\begin{aligned} C(V_i, V_e) = {} & a_1 \cdot (p_{111} + p_{112} \cdot V_e) + \tfrac{3}{2} \cdot a_3 \cdot {V_i}^2 \cdot \left(p_{111} + \tfrac{1}{2} p_{-111}\right) + 3 \cdot a_3 \cdot V_i \cdot \\ & V_e \cdot p_{011} \cdot \left(p_{111} + \tfrac{1}{2} p_{-111}\right) + \tfrac{3}{2} \cdot a_3 \cdot {V_i}^2 \cdot V_e \cdot \left(p_{112} + \tfrac{1}{2} p_{-112}\right) + 3 \cdot a_3 \cdot V_i \cdot \\ & {V_e}^2 \cdot \left(p_{011} \cdot p_{112} + \tfrac{1}{2} p_{011} \cdot p_{-112} + p_{012} \cdot p_{111} + \tfrac{1}{2} p_{012} \cdot p_{-111}\right) + \tfrac{3}{2} \cdot a_3 \cdot {V_e}^2 \cdot \\ & \left({p_{011}}^2 \cdot p_{111} + \tfrac{1}{2} {p_{011}}^2 \cdot p_{-111} + {p_{-111}}^2 \cdot p_{111} + \tfrac{1}{2} {p_{111}}^3\right) + \ldots \end{aligned} \tag{4.37}$$

i.e.

$$C(V_i, V_e) = a_1 \cdot p_{111} + a_1 \cdot p_{112} \cdot V_e + a_3 \cdot f_1(V_i) + a_3 \cdot f_2(V_e) + a_3 \cdot f_3(V_i, V_e) \tag{4.38}$$

where $f_1(V_i)$, $f_2(V_e)$, $f_3(V_i,V_e)$ are nonlinear functions. $C(V_i,V_e)$ therefore consists of a constant term composed of the product of the 1st-order G coefficient a_1 and the 1st-order P coefficient p_{111}, along with other higher-order functions of V_i alone, of V_e alone, and of both V_i and V_e. (4.38) hence gives the expression of the PA's conversion gain (C) using the formulations of the proposed 3-port PA representation, when the PA's input excitation is V_i and bias tone is V_e.

4.7.3 Feedback circuit transfer function

A mapping of the feedback circuit's transfer function (from RF input V_o to baseband output V_f) as a function of A and B is now performed. For this mapping, the input of the feedback block is excited with the same multi-tone signal V_o as in Section 4.7.2. Leaving the feedback circuit connected to the PA output, as shown in Figure 4.23, ensures that the feedback circuit's transfer function is evaluated with the right input conditions, while also ensuring the

correct load conditions at the PA's output. For a particular value of A and B, the output signal V_f is measured, and the transfer function of the feedback block is given by (4.39).

$$\frac{V_f(\omega_x)}{Env(V_o)} = f(A,B) \tag{4.39}$$

where $V_f(\omega_x)$ is the amplitude value of V_f at the frequency ω_x and $Env(V_o)$, also at frequency ω_x, refers to the envelope of the PA's modulated output RF signal V_o. By repeating the measurement given by (4.39) for various values of A and B, the mapping of the feedback circuit's transfer function is generated and stored as a look-up table.

4.7.4 Conditions for loop stability

The requirements for stability of the closed-loop system in Figure 4.23 is based on the well-known Barkhausen gain margin and phase margin stability criteria. However, as described earlier in Section 2.2.1, only the gain margin is considered since the positive feedback necessarily introduces a ~360^0 phase shift across the PA bandwidth; hence, it leaves no possibility of phase margin design. Accordingly, the condition for stability is given by (4.40).

$$C(V_i, V_e) \cdot f(A,B) < 1 \tag{4.40}$$

By substituting (4.37) in (4.40), we get (4.41).

$$f(A,B) < \frac{1}{a_1 \cdot p_{111} + a_1 \cdot p_{112} \cdot V_e + a_3 \cdot f_1(V_i) + \cdots} \tag{4.41}$$

(4.41) is the condition for stability of the closed-loop circuit using positive envelope feedback at the input power level corresponding to V_i and bias tone corresponding to V_e. By calculating $C(V_i,V_e)$ for a few more V_i levels that define the PA's power levels where positive envelope feedback is of interest, the condition to maintain closed-loop stability at these power levels is also determined. For each such calculation, V_i is kept constant while V_e is

considered as a small-signal input, and the conversion gain $C(V_i,V_e)$ as given by (4.38) is the value of the PA's output envelope over V_e. The look-up table of Section 4.7.3 is used to determine the values of A and B that satisfy (4.41). The conditions to ensure closed-loop stability are therefore known. If G is considered as a 3rd-order polynomial, i.e. coefficient a_5 is set to zero, we can use (4.38) and (4.40) to obtain the following simplified expression of $f(A,B)$.

$$f(A,B) < \frac{1}{a_1 \cdot p_{111} + a_1 \cdot p_{112} \cdot V_e + a_3 \cdot f_1(V_i) + a_3 \cdot f_2(V_e) + a_3 \cdot f_3(V_i,V_e)} \tag{4.42}$$

We now substitute the parameter values of the 3-port representation X, extracted for the DUT described in Section 4.7.1, in (4.38). The resulting expression, given by (4.43), gives the value of the PA's power-stage conversion gain $C(V_i,V_e)$ as a function of the input voltage V_i and the bias tone V_e.

$$\begin{aligned} C(V_i,V_e) &= (4.693 - j\cdot 0.463) - V_i^2 \cdot (376.55 - j\cdot 189.85) \\ &+ V_i^4 \cdot (20123.0 - j\cdot 20871.0) - V_e^2 \cdot (4.65 + 0.094i) \\ &+ V_e^4 \cdot (7.60 + 1.20i) - V_e \cdot V_i \cdot (65.36 - 14.05i) \\ &+ V_e^3 \cdot V_i \cdot (189.01 - 14.99i) + V_e^2 \cdot V_i^2 \cdot (1827.3 - 603.08i) \\ &+ V_e \cdot V_i^3 \cdot (7844.2 - 4792.0i) \end{aligned} \tag{4.43}$$

Using (4.43), the PA's power-stage conversion gain $C(V_i,V_e)$ is plotted as a function of the output power in Figure 4.24, and also compared against the values obtained from circuit-level simulation. As shown, there is an error of 0.5dB between the simulated and predicted values at P_{out}=14dBm, which is the power level at which the 3-port representation was characterized. This error arises due to the approximation based on using a 1-tone RF input signal V_i applied to the formulations of the 3-port PA representation to derive the expression of $C(V_i,V_e)$ given by (4.38), while the coefficients a_1, a_3, a_5 and p_{111}, p_{112}, etc. of the 3-port representation itself were extracted under a 3-tone RF input signal V_i and aimed at accurately predicting the PA's nonlinearities under multi-tone input and dynamic-bias excitation.

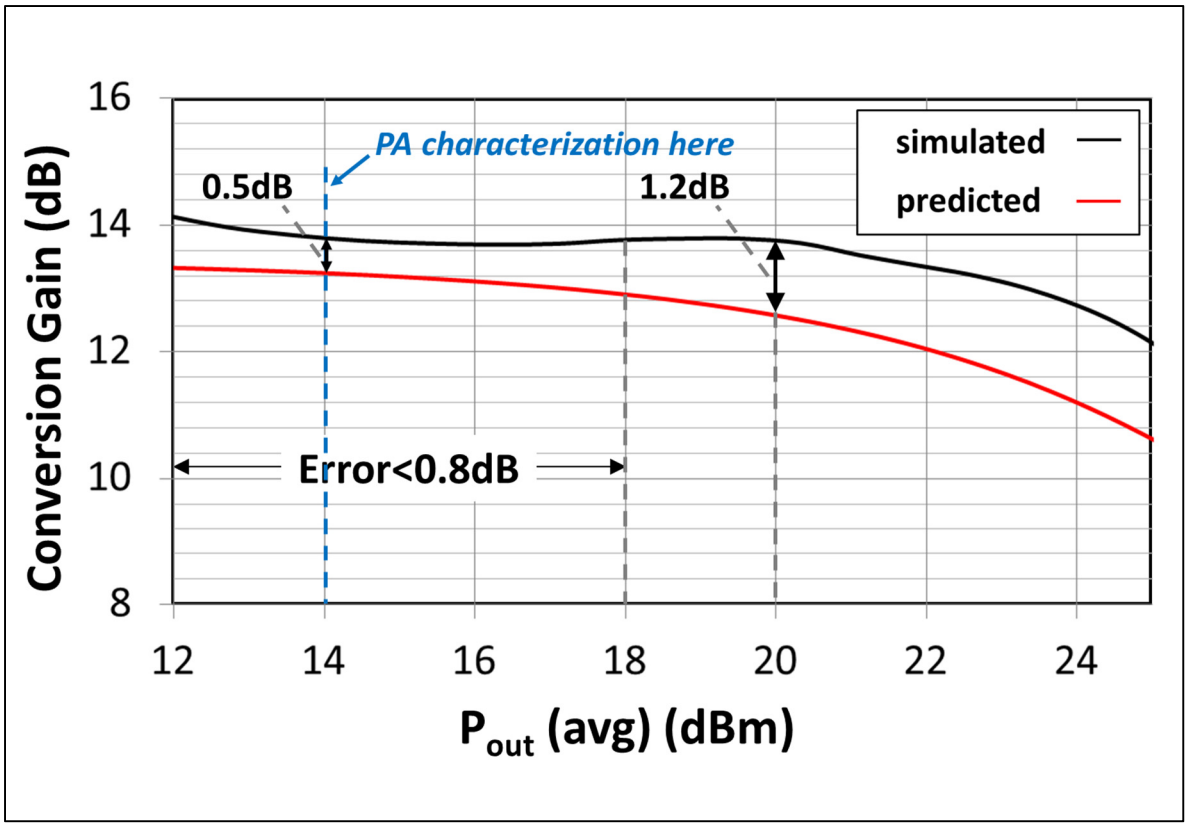

Figure 4.24 Values of the DUT's power-stage conversion gain simulated in ADS^{TM} (black trace) and predicted using the 3-port representation of (red trace)

As can be seen in Figure 4.24, the predicted and simulated values match well over a significant range of power levels where positive envelope feedback is useful (error of less than 0.8dB up to P_{out}=18dBm). This error increases as the power level increases, the increasing error being a result of the 3-port representation being most accurate around the power level of its characterization (P_{out}=14dBm), and becoming less accurate at power levels away from it.

Note that the characterization power level P_{out}=14dBm for the 3-port representation X was so chosen such that it is the most accurate at power levels close to the threshold power level P_{ref} ~14dBm, since it represents a critical power level for the implementation of positive envelope feedback. For predicting the conversion gain using (4.38) with better accuracy at higher P_{out}, the 3-port representation should be re-characterized at these desired levels of

higher power and the newly extracted parameter values substituted in (4.38). Also, since the PA's gain drops for power levels higher than P_{out}=14dBm (and consequently its conversion gain from the bias node V_{ctrl} to the RF node V_o also drops), the value of $C(V_i,V_e)$ at P_{out}=14dBm represents a critical limiting value, and the value of $f(A,B)$ calculated at P_{out}=14dBm *must* be satisfied to ensure closed-loop stability. For higher power levels, the value of $f(A,B)$ may be slightly higher than that at P_{out}=14dBm without compromising the closed-loop PA's stability.

With the power-stage conversion gain now known, control signals A and B are so adjusted such that together with the attenuation through the feedback components in Figure 4.23, the total gain through the positive envelope feedback loop remains less than 0dB for the range of output power levels of interest and where positive envelope feedback is useful. These limits on the control signals A and B are given by (4.44) below. Their actual values are set with an adequate safety margin to guarantee stable behaviour of the PA with positive envelope feedback.

Control signal for detector threshold: A> ~2.0V
Control signal for detector slope: B> ~1.1V (4.44)

4.7.5 Adjustment of detector profile for linearity improvement of PA

With the 3-port representation parameters and the limiting values of A and B that ensures the PA's stability under closed-loop feedback known, the following steps are followed to determine the values of A_{opt} and B_{opt} within this range that optimizes the PA's linearity using positive envelope feedback:

Step 1: The 3-port PA representation is used to determine the values of the dynamic-bias tone V_e at frequency ω_x required to optimize the open-loop PA's IMD_3 under a 3-tone RF excitation V_i, for values of output power P_{out} that lie in the range where positive envelope feedback is useful, i.e. at the power levels where the PA gain is under compression.

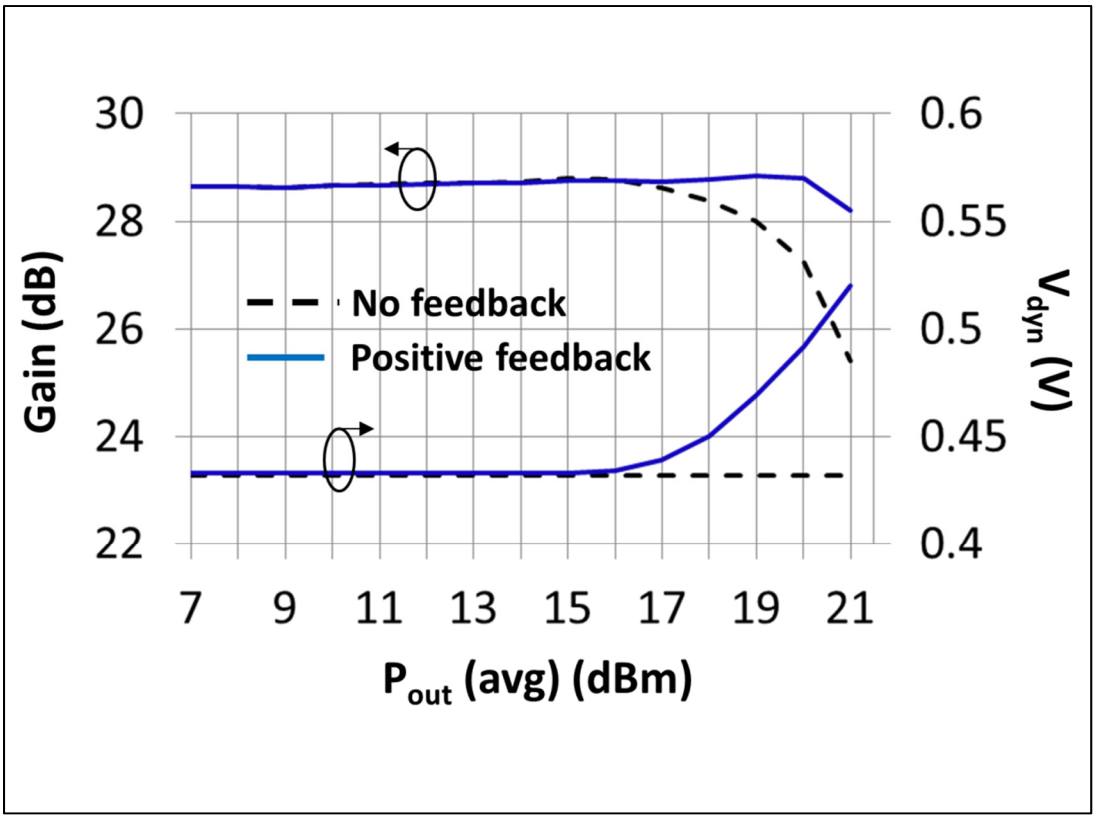

Figure 4.25 Measured *Gain* vs P_{out} , V_{dyn} vs P_{out} with and without positive envelope feedback

Step 2: The look-up table obtained in Section 4.7.3 is used to determine a single combination of the values of A and B, called A_{opt} and B_{opt}, which satisfy the following. First, A_{opt} and B_{opt} must satisfy the stability condition derived in Section 4.7.4. Second, A and B are adjusted to A_{opt} and B_{opt} such that it allows matching the output of the feedback circuit V_f (at frequency ω_x) to the already computed optimum bias values V_e (also at frequency ω_x) of Step 1, at the corresponding values of the PA's output power P_{out}.

With A_{opt} and B_{opt} set accordingly, the loop is now closed. The resulting closed-loop PA with positive envelope feedback has an improved gain profile, which translates into linearity performances close to optimum values while ensuring PA stability.

By applying Step 1 and Step 2 to the PA design of Section 4.7.1, the optimum values of A_{opt} and B_{opt} were found to be 2.6V and 1.6V respectively. Closing the positive envelope feedback loop with A and B set to these values, the measured values of the closed-loop PA's adjusted CW gain is shown in Figure 4.25. The corresponding values of the dynamic-bias signal V_{dyn}, which is the output of the feedback circuit, is also shown. The resulting gain flatness over the output power range from 16dBm to 21dBm, as illustrated in Figure 4.25, is achieved while simultaneously guaranteeing closed-loop PA stability, and translates into a linearity improvement as shown in Section 3.2.2.

4.8 Summary and discussion: Use of proposed three-port representation for embedded self-calibration

This section discusses the use of the proposed 3-port PA representation for implementing embedded self-calibration functions introduced for the first time in this thesis and intended for use within the mobile unit. One such application was extensively described in Section 4.4.4, which allowed adjusting, via embedded self-calibration, the analog pre-distortion applied to an open-loop PA to compensate against part-to-part variation of PA behaviour. The open-loop case is briefly highlighted again in this section, while an embedded self-calibration application for a closed-loop PA is discussed in greater detail.

4.8.1 Embedded self-calibration of open-loop PA

As discussed earlier, the sequence comprising Steps 1-4 of Section 4.3.2 to extract the coefficients of polynomials G and P of the proposed 3-port representation (X in Figure 4.1, Figure 4.2, Figure 4.13), lends itself favourably for adoption by the RFIC PA manufacturer at an advanced engineering phase of the development. A single set of extracted coefficients, which describe the PA's typical behaviour, may then be provided to a mobile equipment manufacturer as parameters of the proposed PA representation, for use in embedded self-calibration functions within the mobile unit that enables accounting for PA part-to-part variation in different mobile units.

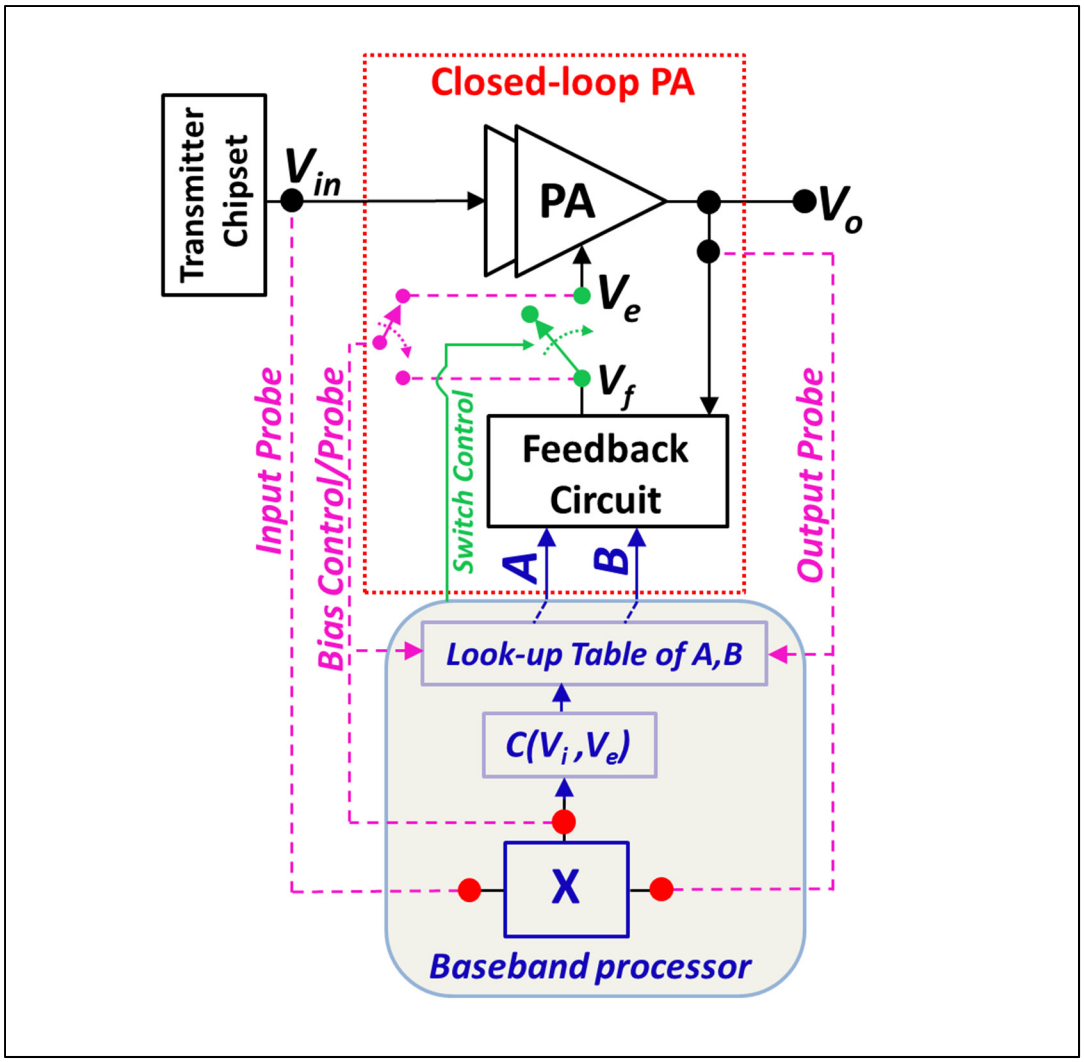

Figure 4.26 Application of proposed 3-port representation for self-calibration embedded within the mobile unit applied to closed-loop PA under positive envelope feedback

In Section 4.4.3, the use of these parameters for extracting a pre-distortion function *F* aimed at PA linearization is shown. Further, in Section 4.4.4, a method of self-calibrating this pre-distortion function *F*, to account for PA performance deviation from its typical behaviour, is demonstrated, using the set-up within the mobile unit shown in Figure 4.13. Only two probes, for a minimum number of quasi-static power measurements and over a narrow power range, are required for this embedded self-calibration in the mobile equipment. The resulting adjustments of the 3-port representation *X*, and consequently *F*, enable the PA linearity

improvements summarized in Table 4.1 and Table 4.2. It was also noted that including a more precise output probe and an additional probe to measure the bias signal (such as the *Bias Control/Probe* in Figure 4.26 as described in Section 4.8.2) allowed further PA linearity improvement.

The example above describes one possible self-calibration function that can be implemented and targets the open-loop PA's linearity. The application of the proposed 3-port representation for embedded self-calibration of closed-loop PAs, for the specific case of the closed-loop PA with positive envelope feedback, is now discussed.

4.8.2 Embedded self-calibration of closed-loop PA

Figure 4.26 shows the set-up within the mobile unit for embedded self-calibration of the closed-loop PA using positive envelope feedback. X refers to the proposed 3-port representation, the parameters of which gives the relationship between the signals at the nodes V_{in}, V_o and V_e for the typical open-loop PA. Along with this single set of parameters, the PA manufacturer may also provide to the mobile equipment manufacturer a single look-up table representing the typical transfer function of the feedback circuit (as shown in Figure 4.26), extracted through the steps described in Section 4.7.3. Knowing this single set of data, that represents parameter values associated to one given PA product, allows determining the value of A_{opt} (for optimum value of detector threshold) and B_{opt} (for optimum value of detector slope) that should be used for the typical closed-loop PA under positive envelope feedback (through the steps described in Section 4.7.4 and Section 4.7.5).

For a different PA under closed-loop operation within a different mobile equipment, suitable adjustments in the values of A_{opt} and B_{opt} may be carried out if necessary to optimize linearity while ensuring stability. To perform this, we describe here an embedded adjustment of the parameters of X and the look-up table stored in the baseband processor within the mobile unit in Figure 4.26, to account for a performance deviation of the new PA compared to its typical behaviour. The steps for this embedded adjustment are as follows:

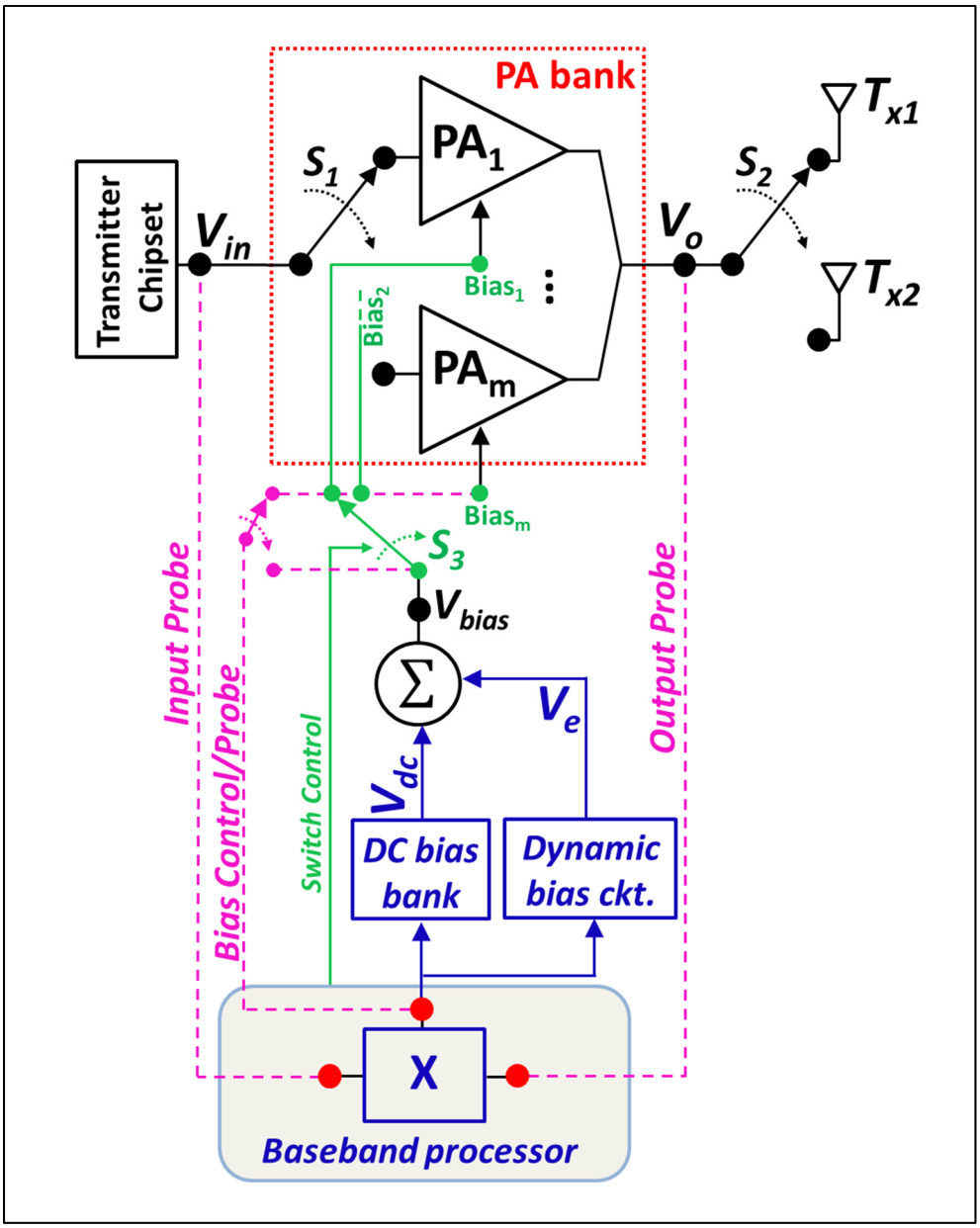

Figure 4.27 Application of proposed 3-port representation for gain regulation in PAs that employ ON/OFF transistor matrices

Updating the 3-port representation *X*: The *Input Probe*, *Output Probe* and *Bias Control/Probe* in Figure 4.26 are used to update the parameters of the open-loop PA representation *X* for the new PA, through the steps described in Section 4.4.4.

Calculating the updated expression of conversion gain: The updated parameters of X are used to update the conversion gain parameter $C(V_i, Ve)$ defined by (4.38) for this new PA. Consequently, the new limit value on the feedback circuit's transfer function computed with (4.42) and that must be respected to ensure its stability is known.

Calculating the updated look-up table values of the feedback circuit's transfer function: The *Output Probe* and the *Bias Control/Probe* are used to measure the RF signal V_o and the baseband signal V_f respectively, to determine the adjusted values of the feedback circuit's transfer function $f(A,B)$ (4.39), as shown in Figure 4.26. This allows accounting for part-to-part variation of the feedback circuit itself, and the look-up table of A, B is suitably updated.

Calculating the updated values of A_{opt} and B_{opt}: The updated value of the parameters in X, the new limit value of $f(A,B)$ and the updated look-up table are now used to adjust the values of A_{opt} and B_{opt} for improved linearity of the new PA while guaranteeing its closed-loop stability, through the steps described in Section 4.7.5.

Once the adjusted A_{opt} and B_{opt} are set, the electronic switch control in Figure 4.26 is used to close the positive envelope feedback loop for the new PA. The resulting closed-loop PA with positive envelope feedback is expected to have a gain profile that results in improved, close-to-optimum linearity performances while ensuring PA stability.

4.8.3 Other applications

Besides the open-loop and closed-loop applications discussed above, the proposed 3-port PA representation for embedded self-calibration may be used to optimize other PA performances. An example of one such application is for gain regulation in PAs that employ the switching ON or OFF of transistor arrays for efficiency improvement (Joung, Ho, & Sun, 2013). As shown in Figure 4.27, such PAs may consist of a PA bank comprising m different PA blocks (PA_1, PA_2, … PA_m) designed to deliver m different ranges of power levels to the load (e.g. to transmit antennas T_{x1} or T_{x2} via switch S_2). Each PA block is designed to

optimally deliver one particular range of power levels, and the choice of which PA block to use at any given power level is made using switch S_1. In the implementation shown in Figure 4.27, independent control of the bias of each PA block is also enabled. Among many important performance parameters of such a PA design is the gain from the input node V_{in} to the output node V_o, and the choice of the DC bias applied to each PA block within the PA bank is generally optimized to ensure minimal variation of the PA's gain.

However, when the transmit path is changed from one PA block to another (e.g. from PA_1 to PA_m) for such switching architectures, undesirable gain variations may indeed occur from one mobile unit to another in different mobile units. Such undesirable gain variations are because of the variation in the performance of structures on the PA (e.g. the transistor, passives, etc.) from one particular part of the PA bank to another in different mobile units. As a result of this variation, the value of the DC bias that is applied to each PA block (within the PA bank) in different mobile units is not optimized for minimum gain variation when switching between PA blocks occurs at predetermined power levels. In this context, an embedded self-calibration technique that reduces such PA gain variations in switching PA implementations from one mobile unit to another in different mobile units is useful for ensuring PA linearity across parts. Figure 4.27 illustrates an example of one such self-calibration set-up embedded within the mobile unit that is possible. Here, X is the 3-port analytical representation proposed in this thesis and implemented within the baseband processor of the mobile unit, and comprising parameters that represent the performance of the typical PA bank (shown within the red dotted box in Figure 4.27).

Using the simple probing circuitry shown in Figure 4.27 to measure the ratio between the input and output signals, any gain deviation of the PA due to switching between PA blocks is detected, and the control signal from X within the baseband processor is used to cancel this gain deviation through adjustment of the DC bias V_{dc} from the *DC bias bank*. The control signals for S_3 (to select the correct bias path) as well as the control signal for selecting the correct DC bias value from the *DC bias bank* (using X) are computed using the processing power of the baseband processor itself, and presents minimum overhead with regard to the

additional processing power that is required due to the proposed embedded self-calibration. Afterwards, the procedure described in Section 4.4.3 and Section 4.8.1 is followed, i.e. the typical values of X are adjusted for the new PA (with the help of measurements using the *Input Probe*, *Output Probe* and *Bias/Control Probe*) to calculate the adjusted value of the dynamic bias V_e that should be applied for optimum linearity of the PA bank.

Therefore, using the self-calibration set-up embedded within the mobile unit shown in Figure 4.27 and by following the steps detailed in this section allows us to reduce gain variation and ensure close to optimum linearity in PAs based on switching ON and OFF of transistor arrays, from one PA part to another.

CONCLUSION AND FUTURE WORK

> "N'oublions pas non plus qu'il ne saurait exister pour la science des vérités acquises."
>
> Claude Lévi-Strauss

5.1 Summary of thesis

This thesis may be broadly divided into two different (but interrelated) parts – the first part constituted by Chapter 2-3 that described a newly introduced technique of positive envelope feedback for improving the linearity-efficiency trade-off in RFIC PAs, and the second part constituted by Chapter 4 that described a recently introduced multi-port analytical representation of RFIC PAs, and its use for the embedded self-calibration of PAs within the mobile unit to account for part-to-part performance variation.

The literature review for both these aspects were covered in Chapter 1, where we identified the various insufficiencies of existing approaches in the state-of-the-art that make them unsuitable for answering the research problems stated in Section 0.1.2 and Section 0.1.4. In Chapter 2 of this thesis, we explained the theory behind positive envelope feedback, looking at its fundamental effect from the perspective of the dynamic quiescent operating point and the PA's load-line, and the resulting linearity enhancement due to a reduction in signal clipping for high values of the input signal's envelope. The design conditions that must be respected to implement positive envelope feedback in PAs were explained in detail, and it was theoretically confirmed that respecting these design conditions ensures that the PA's stability and noise performance are not compromised due to positive feedback. For validating the theory of Chapter 2, detailed simulations on a first CMOS SOI PA design and experimental measurements on a second proof-of-concept prototype CMOS SOI PA design were presented in Chapter 3, which highlighted the efficacy of the proposed technique to improve PA performances while requiring very little in terms of additional circuit area and additional power consumption. Simulations on a modified version of this prototype were also presented in Chapter 3 to demonstrate further the design and implementation of PAs with positive envelope feedback.

Chapter 4 of this thesis presented a multi-port analytical representation of RFIC PAs under envelope-dependent dynamic biasing. A more detailed analysis was given of a simplified 3-port version of this multi-port representation, and which is based on complex polynomials that describe a combiner, a nonlinear baseband-to-RF converter and a nonlinear RF amplifying function. This proposed representation, extracted using multi-tone signals, allows predicting the dynamic biasing necessary to linearize the PA under multi-tone as well as modulated RF excitation signals. The chapter also introduced a novel embedded self-calibration technique for use within the transmitter front-end of the mobile unit, which accounts for part-to-part variation of PA performance in different mobile units. This self-calibration technique, using the proposed 3-port representation, enables the adjustment of the PA parameters from one mobile unit to another to ensure close-to-optimum PA performance across parts. For example, when implementing envelope-dependent dynamic biasing of RFIC PAs in mobile devices, the embedded self-calibration technique allows modifying the applied dynamic biasing from one mobile device to another, to ensure close-to-optimum linearity-efficiency performance for each PA part in different mobile units. The various tests that were presented in Chapter 4, based on both simulation and experimental implementations, highlighted the relative simplicity yet good accuracy of the proposed 3-port representation's characterization process compared to other PA representations and its use for the embedded self-calibration of different open-loop and closed-loop PA architectures. One especially interesting example that was presented involved using the formulations of the 3-port PA representation to analytically derive the expression of the PA's conversion gain from the dynamic biasing port to the output port. This expression was then used to determine the value of the conversion gain for a range of PA power levels where positive envelope feedback is useful, to analytically identify the feedback circuit conditions that ensure closed-loop PA stability under positive envelope feedback.

Table 5.1 is a summary of the work presented in this thesis in tabular form, to allow easy reference for the reader.

Table 5.1 Summary of the various chapters in this thesis

Chapter	Summary
Chapter 0	This chapter presented the motivation behind, and the problem statements of, the research work presented in this thesis. The research objectives were clearly defined, and the resulting contributions were listed.
Chapter 1	This chapter reviewed the state-of-the-art - existing PA architectures for improving PA performance were described, and current approaches for analytically representing PA behavior were detailed. The insufficiencies of these existing techniques and approaches for answering the research problems stated in Chapter 0 were also enumerated.
Chapter 2	This chapter introduced the theory behind positive envelope feedback and the resulting improvement in PA linearity due to reduced output signal clipping. The design conditions for successfully implementing positive envelope feedback were also described.
Chapter 3	The design and implementation of positive envelope feedback in RFIC PAs was shown, with the help of both simulations and experimental measurements. Linearity improvement under both multi-tone and modulated RF excitation was demonstrated, while requiring minimum additional circuit area and minimum additional DC power consumption.
Chapter 4	This chapter introduced the novel multi-port analytical representation of PAs under envelope-dependent dynamic biasing. The formulations for a 3-port simplified version were derived, and its application to different PA linearization schemes were shown. Chapter 4 also introduced the use of this multi-port representation for the embedded self-calibration of PAs within the mobile unit to compensate against part-to-part variation of PA performances.

5.2 Limitations and discussion

Throughout the thesis, we referred to any limitations that were encountered as and when they arose, as well as provided recommendations on potential ways to overcome them. These are listed again in the next few paragraphs, along with a discussion on their cause and (if possible) how to eliminate them.

- There is a limitation on the signal bandwidth for which linearization using positive envelope feedback is demonstrated using the experimental prototype in Section 3.2. For example, the choice of the 2-tone spacing used for the IMD_3 plots shown in Figure 3.15 is only 100kHz. This choice was necessary due to AM/PM effects for larger 2-tone spacings, resulting in diminished linearity improvement. This bandwidth limitation also indicated the possible presence of a low-pass filter structure somewhere along the feedback loop. As explained in Section 3.2.4, such a structure was traced to the sizeable gate-source capacitance C_{gs} of the PA's power-stage transistor (Figure 3.11) compounded by a 5kΩ on-chip gate resistance initially required for investigations on biasing. This structure indeed introduced undesired AM-PM effects as a function of the dynamic-bias signal V_{dyn} under positive envelope feedback, which reduced the linearization effects of the AM-AM compensation through positive envelope feedback. As shown in Section 3.2.4, replacing the 5kΩ gate resistors with off-chip 15nH inductors (RF chokes) removes the RC time-constant associated with the positive feedback loop and enables PA linearization over the much larger signal bandwidth shown in Figure 3.17-3.19. Any remaining source of bandwidth limitation arises primarily from the frequency response of the envelope detector that is used, a topic that will be touched upon in Section 5.3.

- The experimental prototype demonstrated in Section 3.2 is a dual-IC module, with the flip-chip power amplifier IC and the wire-bond envelope detector IC fabricated separately and then assembled on the same multi-chip module (MCM) and PCB. The resistor divider is implemented using discrete SMT components on the PCB. It was mentioned in Section 3.2.1 that for a single-chip integration of the PA, the envelope

detector and the resistor-divider would require a much smaller overall chip area - the additional chip area requirements compared to the PA without positive envelope feedback was estimated at ~5%. Such a flip-chip IC was indeed designed and fabricated for assembly as a single-IC module. However, due to multiple issues over several attempts at assembly, efforts for measurement of this fabricated IC had to be abandoned. That being said, it is worthwhile to mention that the results from simulation of this single-module IC follow closely that of the modified prototype in Section 3.2.4.

- In Section 4.4.2, Figure 4.10, it was shown that the accuracy of predicting the values of the PA's output tones under constant DC bias using only the *G* polynomial of the proposed analytical PA representation is the highest at the characterization power level of P_{out} =14dBm. As the PA's output power deviates from this characterization power level, the error between the simulated and the predicted tones also increases. While this may come across as a limitation of the proposed analytical representation, it is actually a consequence of restricting *G* to a 5th-order polynomial here. By extending *G* to a higher-order polynomial, a process that is easily accomplished and requires minimum increase in complexity as explained in Section 4.6, the accuracy of prediction can be extended over a larger range of PA output power levels.

  Additionally, the increase of the error at lower average output power levels under constant DC bias does not affect the accuracy of the proposed 3-port representation for predicting PA performances under dynamic biasing conditions at P_{out} =14dBm, since this error pertains to the *G* block only (not the *P* block). It was also shown in Figure 4.11 and Figure 4.21 that the full 3-port representation (i.e. including both *G* and *P* blocks) accurately captures the PA's IMD performance over a significant range of amplitude as well as phase values of the dynamic-bias signal, at the PA's characterization power level.

- As shown in Figure 4.24, the simulated value of the PA's power-stage conversion gain and that predicted using expression (4.43) (derived from the formulations of our proposed 3-port analytical representation) show an error of 0.5dB at P_{out} =14dBm, which is the

power level at which the 3-port representation was characterized. This error, which is, in fact, relatively small with respect to the ~14dB conversion gain, may still be viewed as a limitation of our approach. It arises from the approximation of using a 1-tone RF input signal V_i applied to the formulations of the 3-port PA representation to derive the expression of $C(V_i,V_e)$ given by (4.38), while the coefficients a_1, a_3 and a_5 of the 3-port representation were extracted using a 3-tone RF input signal V_i and aimed at accurately predicting the PA's nonlinearities under multi-tone input and dynamic-bias excitations.

By re-deriving the coefficients of the 3-port analytical representation using a 1-tone RF input signal V_i would allow reducing this 0.5dB value of the error. However, the idea behind using a single set of coefficients for predicting both PA linearity under multi-tone excitation as well as its conversion gain was to evaluate and demonstrate that despite such an error (which can be removed through a one-time calibration step), the trends of the PA's conversion gain as a function of output power P_{out} can still be predicted satisfactorily using our proposed formulations, as evidenced in Figure 4.24. As can also be seen in Figure 4.24, the predicted and simulated values match well over a significant range of power levels where positive envelope feedback is useful (error of less than 0.8dB up to P_{out}=18dBm). The increasing value of error as the power level increases is a result of the 3-port representation being most accurate around the power level of its characterization (P_{out}=14dBm), and becoming less accurate at power levels away from it. For predicting the conversion gain using (4.38) with better accuracy at higher P_{out}, the 3-port representation should be re-characterized at these desired levels of higher power and the newly extracted parameter values substituted in (4.38).

- Figure 4.14 and Figure 4.15 in Section 4.4.3 demonstrates the use of our proposed 3-port representation for linearity improvement of an open-loop PA via feed-forward dynamic biasing. While the degree of linearity improvement through feed-forward dynamic biasing that can be achieved at different values of the power levels is partly due to the intrinsic nonlinearity of the PA structure as well as the PAPR of the multi-tone/modulated excitation that is used, it is reasonable to question if this improvement in

linearity at different power levels is limited by the specific value of the pre-distortion function F in Figure 4.13 that is used, since its value was derived based on the values of the coefficients of the 3-port analytical PA representation extracted only at P_{out} =14dBm. Indeed, it can be demonstrated that by computing F based on the proposed 3-port PA representation characterized at different output power levels allows achieving higher levels of PA linearity across this power range, compared to what is achievable with a 3-port representation characterized at a single power level. However, this is not a limitation of the approach described in Section 4.4.3, since the idea behind the linearization demonstrated here was to evaluate the range of power levels for which the proposed analytical representation X is useful to implement feed-forward linearization as shown in Figure 4.13, with the help of the value of X that was characterized at a single value of the PA's average output power. This same linearization exercise can be easily extrapolated to include the case where the pre-distortion function F is calculated using the 3-port representation X extracted at different power levels of interest.

- Similar to the example described in the previous two paragraphs, it is reasonable to question if the improvement in PA linearity through embedded self-calibration that is listed in Section 4.4.4, Table 4.1 and Table 4.2 is limited by the approach used – i.e. due to using only a minimum number of quasi-static measurements to adjust the coefficients of only the G polynomial in the 3-port representation. Indeed, as also explained in Section 4.4.4, the resulting degree of improvement in IMD_3 through pre-distortion is a function of the assumption that only the G coefficients are updated, such an updating procedure requiring the use of only a very simple probing circuitry. By additionally adjusting the coefficients of the P polynomial, even higher levels of linearity improvement may be achieved. However, this is not a limitation of the approach detailed in Section 4.4.4, since the idea behind the linearization demonstrated here was to evaluate the degree of linearity improvement that is possible through embedded self-calibration that is based on using the simplest possible probing circuitry to perform a small number of measurements necessary to minimally adjust only a few coefficients of X for the set-up

shown in Figure 4.13. By including more complex probing circuitry, higher PA performance improvement may be achieved, as discussed in Section 4.4.4.

5.3 Recommendations for future investigation

A number of ancillary research topics deemed promising for future investigation, and stemming from the research conducted through the course of the work described in this thesis, are recommended next and presented in the following paragraphs.

- The design architecture of the envelope detector used for positive envelope feedback requires further investigation. The detector design currently used for the implementation examples in Chapter 3 was not optimized for use in positive envelope feedback but borrowed from an existing work (Carrara, Presti, Scuderi, Santagati, & Palmisano, 2008) aimed at an entirely different application with its own unique requirements. An ideal candidate of our envelope detector would have substantially larger bandwidth (the detector design in Figure 3.2 is limited by several RC low pass filter structures at multiple nodes), consume minimum DC current, require minimum chip area and be tailored to be ON only for the 6-8dB range of PA operating power levels where the PA is under gain compression, hence where positive envelope feedback is useful. The high bandwidth requirement is especially important in the context of the large bandwidth communication signals envisaged for use in 5G millimetre-wave applications. All the above criteria may require a completely new detector architecture based on completely different operating principles from the one shown in Figure 3.2 and is a topic that requires further examination.

- The linearity improvement reported from positive envelope feedback in this thesis is a result of the technique applied to the power-stage transistors only. Further linearity improvement is potentially possible by applying positive envelope feedback to the driver-stage transistors in addition to the power-stage transistors. Another implementation that requires further investigation is to implement positive envelope feedback for supply

modulation, in addition to the dynamic biasing described in this thesis. The envelope detector necessary for any one stage of a multi-stage PA could potentially be shared between the dynamic biasing and supply modulation circuits, to ensure minimum requirements with respect to additional current consumption and additional circuit area. These aspects are covered by our second patent application with the US PTO (Sharma & Constantin, April 2018). The output of the same envelope detector used for positive envelope feedback can also be further utilized for PA transistor protection circuits against dangerous voltage swings arising from Voltage Standing Wave Ratio (VSWR) mismatch conditions. One possible illustration of such a holistic PA design is shown in Figure 5.1, the design itself of which is not addressed in this thesis and requires further investigation.

- In this thesis, we primarily discuss the 3-port simplification (Figure 4.6) of the multi-port analytical PA representation (Figure 4.3(a)) presented in Section 4.2, and its use for various applications related to PA performance optimization and embedded self-calibration. However, various other simplifications of the general multi-port representation in Figure 4.3(a) are possible, some of which may be better suited than the 3-port structure of Figure 4.6 to capture the PA's nonlinearity under specific conditions related to the PA architecture, type of biasing used, etc. For example, Figure 5.2 is a possible simplification of the analytical representation initially shown in Figure 4.3(c), and is intended to capture the PA's nonlinearities when it is under dynamic biasing and supply modulation simultaneously. Yet another possible implementation is shown in Figure 5.3 and aims at capturing the PA's nonlinearities under envelope tracking. Various other forms are also possible, and there is a need to study about optimizing the type, the order and the signal flow of the various polynomials in the proposed analytical representation to best capture different sources of PA nonlinearities under different conditions. All this merits further investigation.

- In this thesis, the design of the probing circuitry used for the different embedded self-calibration examples of Figure 4.1, Figure 4.2, Figure 4.13, Figure 4.26, Figure 4.25 is not discussed. For embedding within the mobile unit, these probes have to be adequately

simple but without compromising on the level of measurement accuracy necessary for self-calibration, by capturing the difference in performance from one PA part to another. The design of such probing circuitry, tailored to optimize their effectiveness for embedded self-calibration applications as described in this thesis, is also a subject that requires further examination.

5.4 Concluding remarks

In this thesis, we introduced a new method of improving the linearity-efficiency trade-off in RFIC PAs. Positive envelope feedback offers several advantages that make it an attractive option for use in power amplifier designs for current and future wireless mobile equipment. Any simple PA design technique that allows performance improvement without drastically requiring additional resources offers the possibility of integrating the technique into existing PA designs, as well as its use in conjunction with other PA performance improvement techniques. As a simple analog technique without fundamentally restrictive bandwidth limitations and that is suitable for single-chip integration, positive envelope feedback holds special significance in the light of the modulated signal waveforms envisaged for 5G applications. It is a widely held consensus that digital techniques alone *cannot suffice* for performance improvement in millimetre-wave PAs for 5G applications, and they must be concurrently used with analog techniques to guarantee meeting PA linearity requirements (P. M. Asbeck, Rostomyan, Özen, Rabet, & Jayamon, 2019). This notion is in contrast to the 1980s, when the rapid emergence of digital technology encouraged speculation that all analog techniques would ultimately be replaced by their digital counterparts. The ultimate goal would be to have positive envelope feedback included as an essential design technique in every RFIC PA due to its inherent simplicity, but there is *a ways to go* (and additional research) before this is achieved.

We also introduced in this thesis a technique for embedded self-calibration of the PA within the mobile unit, using a novel multi-port analytical PA representation and based on a minimum number of embedded measurements using simple probing circuitry. The technique

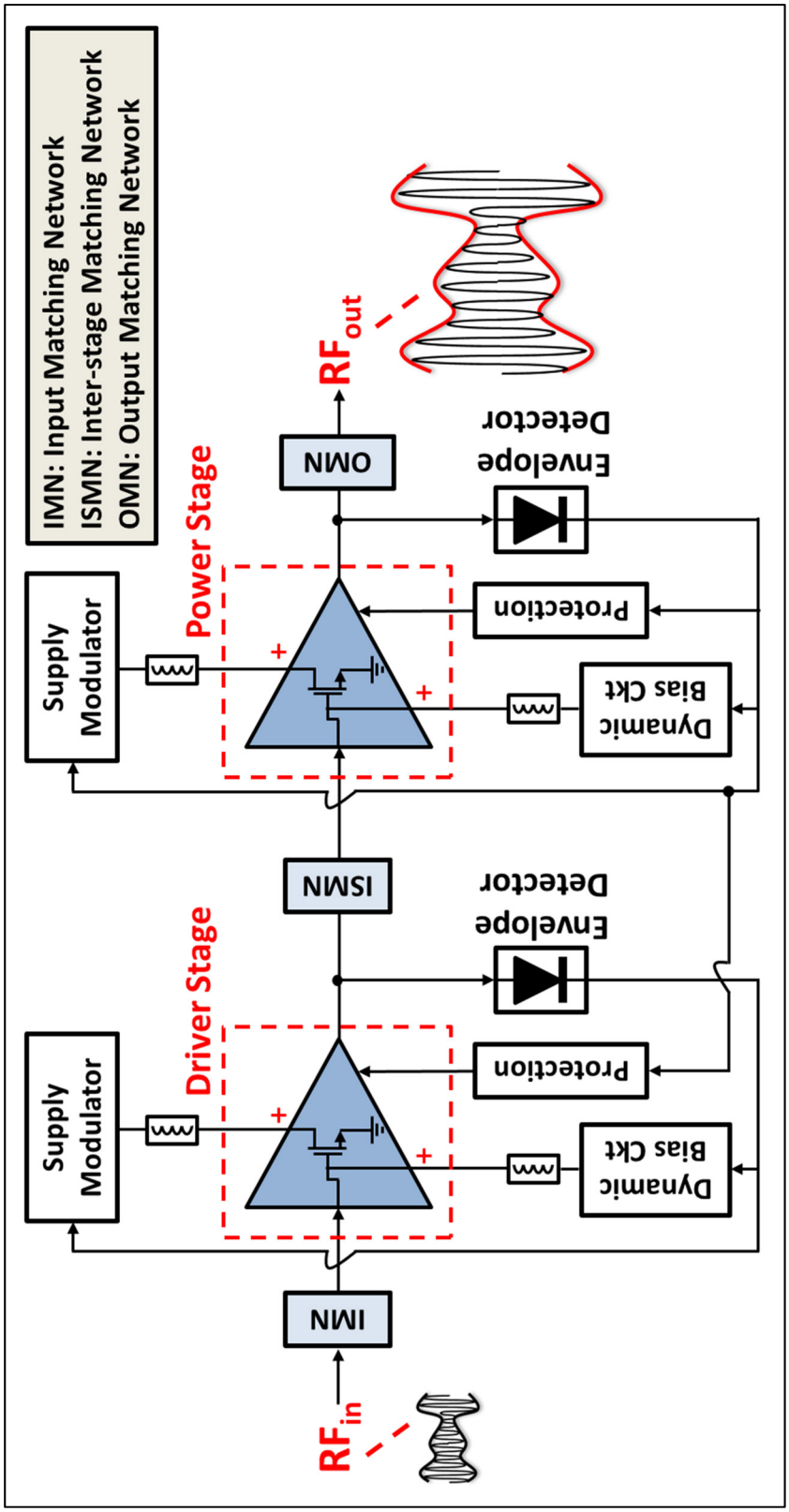

Figure 5.1 Illustration of multi-stage PA design using positive envelope feedback for dynamic biasing as well as supply modulation, for both the driver-stage and the power-stage transistors. The output of the envelope detector used for positive feedback is also concurrently used for protecting the PA transistors against very large voltage swings arising from VSWR mismatch conditions

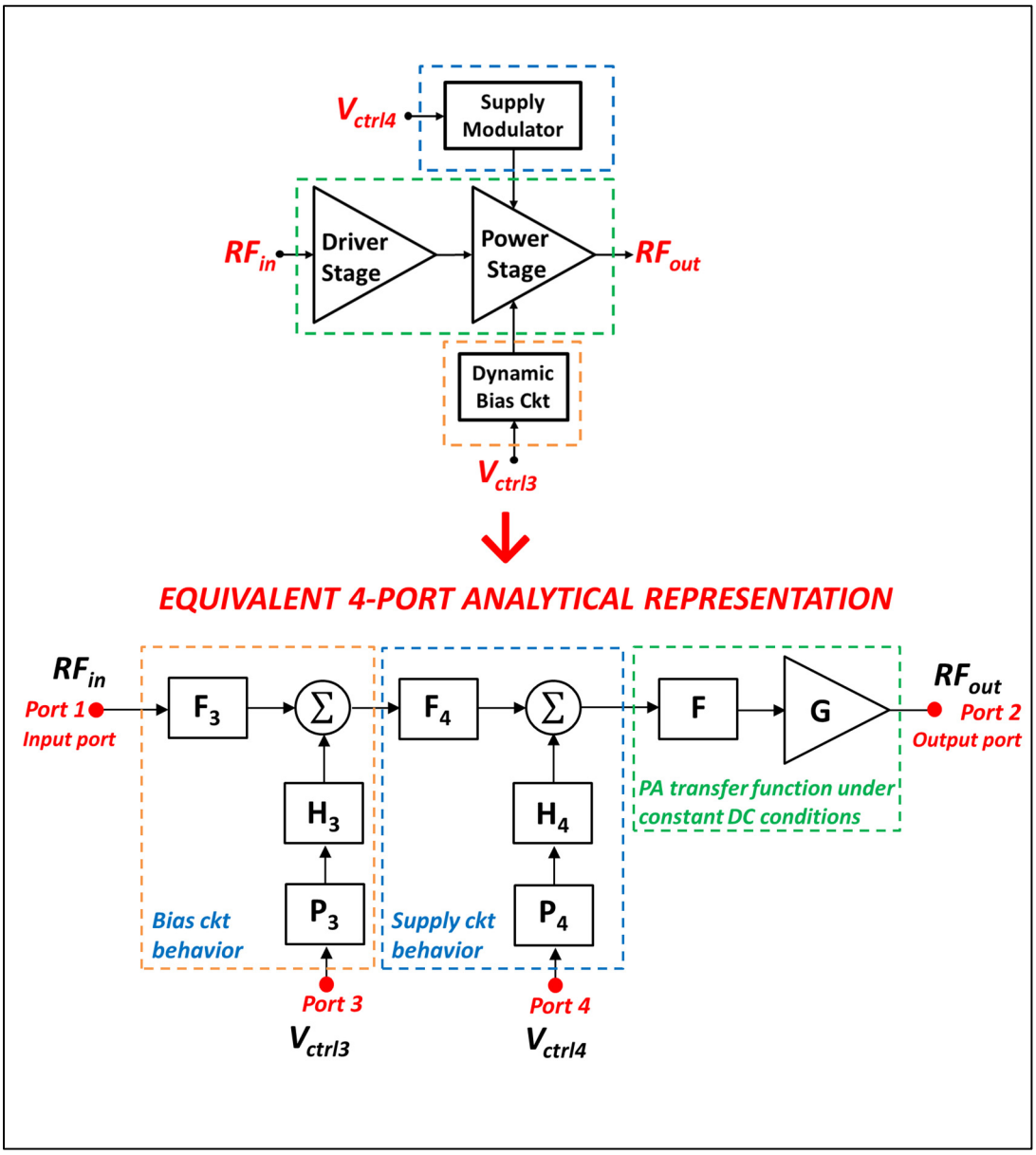

Figure 5.2 Illustration of a possible variant of proposed analytical PA representation to capture PA nonlinearities under simultaneous dynamic biasing and supply modulation

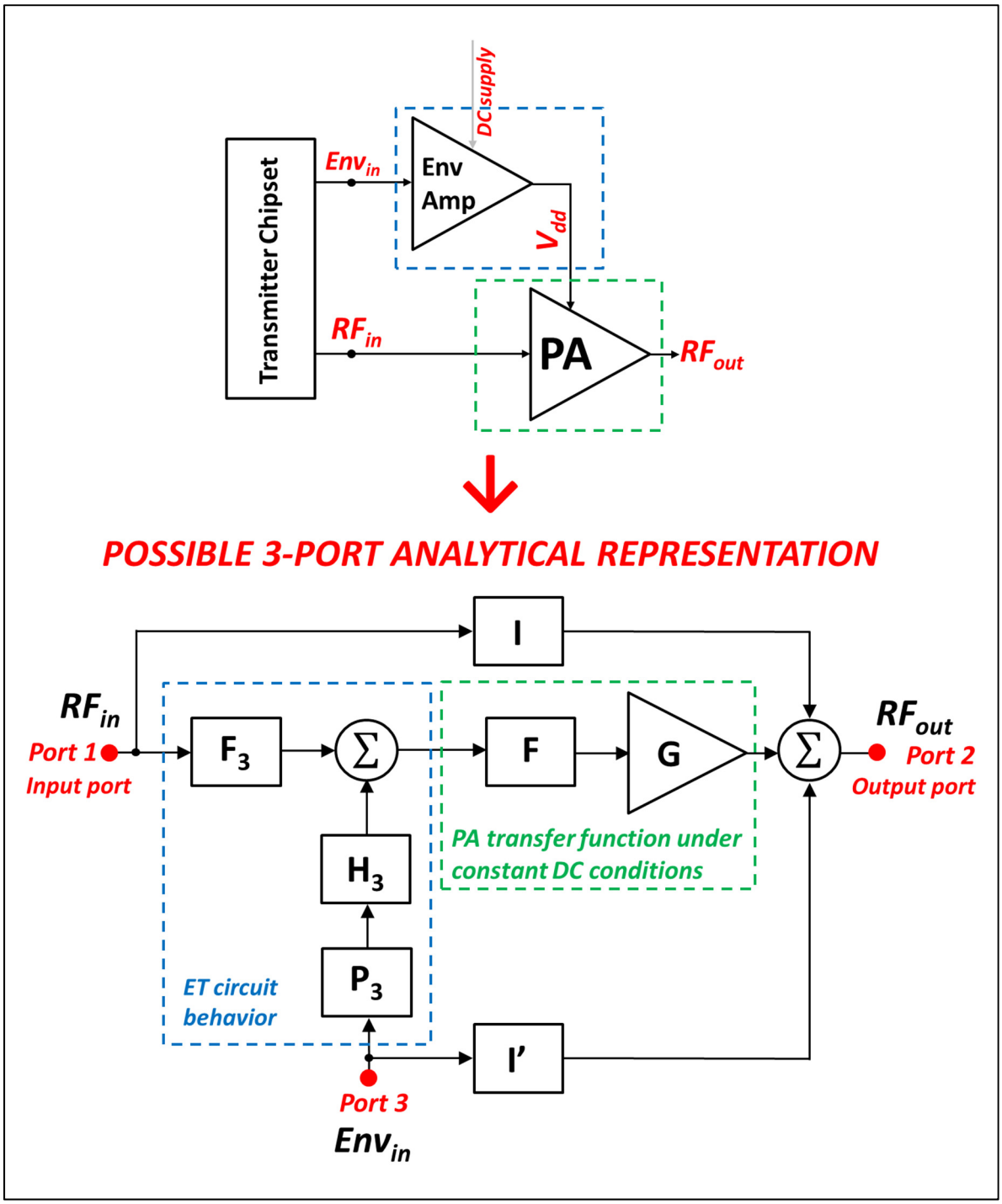

Figure 5.3 Illustration of a possible variant of proposed analytical PA representation to capture PA nonlinearities under envelope tracking. *I* and *I'* may capture linear dependencies of the output on the RF_{in} and Env_{in} signals respectively

allows PA performance optimization from one mobile unit to another in different mobile units, and offers the possibility of a significant increase in the yield for both the PA manufacturer and the ME manufacturer. The technique would allow the PA manufacturer to guarantee more aggressive performance specifications, as well as positively affect the *time to market* for both the PA and ME manufacturer. In the intensely competitive and continually evolving world of power amplifier design, any technique that allows even the slightest improvement of PA performance while requiring minimum increase in complexity can help in securing the edge over its rivals and capture the market. There is significant work still to be done before such a technique makes its way into every mobile device, but we have definitively established through the work presented in this thesis – for *the first time* in the literature – the possibility and the benefits of such an embedded self-calibration technique.

APPENDIX I

METAL STACK-UP OF USED CMOS SOI TECHNOLOGIES

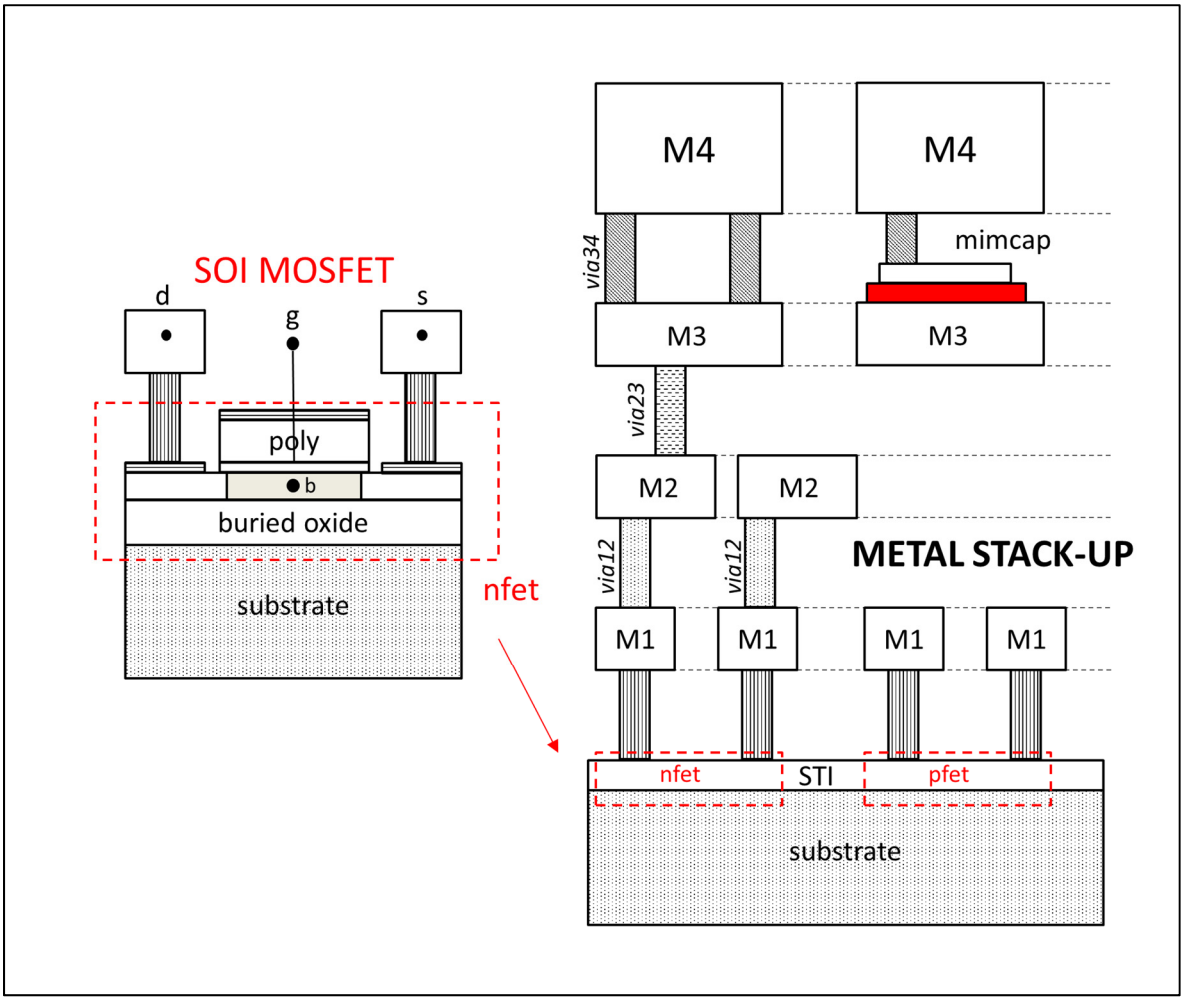

Figure-A I-1 Representative metal stack-up of used CMOS SOI technologies for PA designs discussed in this thesis. Further proprietary details may be obtained on request from the foundry

APPENDIX II

MULTI-TONE MEASUREMENTS FOR THREE-PORT REPRESENTATION: CENTRING DATA AND HANDLING IMD_3 ASYMMETRY

Centring the multi-tone measurements aids significantly in solving the system of equations in Step 1 and Step 4 of Section 4.3.2. Mathematically, this translates into a minor modification of (4.13) as it is presented earlier into the form in (A II-1), where the additional term $k(\omega_c+i\omega_x)$ refers to a constant complex number that accounts for centring the voltage measurements at the frequency tone $\omega_c+i\omega_x$.

$$v'_o(t) = \sum_{i=-u}^{u} (\boldsymbol{k_{\omega_c+i\omega_x}} + V'_o(\omega_c + i\omega_x)) \cdot cos((\omega_c + i\omega_x)t + \beta_{\omega_c+i\omega_x}) \qquad \text{(A II-1)}$$

These additional $k(\omega_c+i\omega_x)$ constants do not affect the extraction procedure of the coefficients a_1, a_3, a_5, etc. of polynomial G, which is described in Section 4.3.2. This is because a_1, a_3, a_5, etc. capture the nonlinear dependence of the PA's output signal on its input signal over the power range of interest, while $k(\omega_c+i\omega_x)$ merely represents a constant offset value.

An example of the values of $k(\omega_c+i\omega_x)$ are given by (A II-2), which are the values for the test-case described in Section 4.4.

$$\begin{aligned} k_{\omega_c} &= -0.03 - j \cdot 0.04 \\ k_{\omega_c+\omega_x} &= -0.03 + j \cdot 0.12 \\ k_{\omega_c+2\omega_x} &= 0.03 + j \cdot 0.03 \\ k_{\omega_c-\omega_x} &= 0.06 - j \cdot 0.13 \\ k_{\omega_c-2\omega_x} &= -0.02 + j \cdot 0.02 \end{aligned} \qquad \text{(A II-2)}$$

Additionally, frequency domain asymmetry of the PA's IMD_3 at high power levels is handled through a minor modification of the input signal V_a to the polynomial G, as shown in (A II-3). The coefficient $b(\omega_c+i\omega_x)$ is one when there is no IMD_3 asymmetry, but is a complex

constant (part of a complex matrix) for power levels when *IMD₃* asymmetry becomes significant.

$$v_a(t) = \left(\sum_{i=-1}^{1} \boldsymbol{b_{\omega_c+i\omega_x}} \cdot V_{in}(\omega_c + i\omega_x) \cdot cos\left((\omega_c + i\omega_x)t + \theta_{\omega_c+i\omega_x}\right)\right. \\ \left. + \sum_{i=-s}^{s} \left(\sum_{q=1}^{m} \sum_{l=1}^{n} p_{iql} \{V_e(q) \cdot cos(\phi_q)\}^l\right) \cdot e^{j(\omega_c+i\omega_x)t}\right. \tag{A II-3}$$

For example, the values of $b(\omega_c+i\omega_x)$ for the test-case described in Section 4.4 are given by (A II-4).

$$\begin{aligned} b_{\omega_c} &= 7.64 - j \cdot 2.45 \\ b_{\omega_c+\omega_x} &= 6.47 - j \cdot 5.10 \\ b_{\omega_c-\omega_x} &= 7.87 + j \cdot 0.79 \end{aligned} \tag{A II-4}$$

It is useful to point out that the modifications given in Appendix II do not affect the order or the complexity of the proposed formulations presented in Section 4.3.

BIBLIOGRAPHY

Ahn, G., Kim, M., Park, H., Jung, S., Van, J., Cho, H., Sung-wook, K., Jong-hyuk, J., Kyung-hoon, L., Kim, J. Y., Song, S.C., Cheon-seok, Park, Yang, Y. (2007). Design of a High-Efficiency and High-Power Inverted Doherty Amplifier. *IEEE Transactions on Microwave Theory and Techniques, 55*(6), 1105-1111. doi:10.1109/TMTT.2007.896807

Ali, S. N., Agarwal, P., Baylon, J., & Heo, D. (2017, 4-9 June 2017). *Reconfigurable high efficiency power amplifier with tunable coupling coefficient based transformer for 5G applications.* Paper presented at the 2017 IEEE MTT-S International Microwave Symposium (IMS).

Asbeck, P. M., Rostomyan, N., Özen, M., Rabet, B., & Jayamon, J. A. (2019). Power Amplifiers for mm-Wave 5G Applications: Technology Comparisons and CMOS-SOI Demonstration Circuits. *IEEE Transactions on Microwave Theory and Techniques, 67*(7), 3099-3109. doi:10.1109/TMTT.2019.2896047

Asbeck, P., & Popovic, Z. (2016). ET Comes of Age: Envelope Tracking for Higher-Efficiency Power Amplifiers. *IEEE Microwave Magazine, 17*(3), 16-25. doi:10.1109/MMM.2015.2505699

Bailoo, A. S. (24th Jun 2019). A Quick Introduction to Smartphone Architecture. Retrieved from https://www.evelta.com/blog/a-quick-introduction-to-smartphone-architecture/

Barradas, F. M., Cunha, T. R., Lavrador, P. M., & Pedro, J. C. (2014). Polynomials and LUTs in PA Behavioral Modeling: A Fair Theoretical Comparison. *IEEE Transactions on Microwave Theory and Techniques, 62*(12), 3274-3285. doi:10.1109/TMTT.2014.2365188

Berthiaume, D., Sharma, S., & Constantin, N. (2016, 15-18 May 2016). *Low current, 100MHz bandwidth envelope detector for CMOS RFIC PAs.* Paper presented at the 2016 IEEE Canadian Conference on Electrical and Computer Engineering (CCECE).

Carrara, F., Presti, C. D., Scuderi, A., Santagati, C., & Palmisano, G. (2008). A Methodology for Fast VSWR Protection Implemented in a Monolithic 3-W 55% PAE RF CMOS Power Amplifier. *IEEE Journal of Solid-State Circuits, 43*(9), 2057-2066. doi:10.1109/JSSC.2008.2001894

Carroll, A., & Heiser, G. (2010). *An analysis of power consumption in a smartphone*. Paper presented at the Proceedings of the 2010 USENIX conference on USENIX annual technical conference, Boston, MA.

Carvalho, N. B. D., & Pedro, J. (Dec. 1999). Compact Formulas to Relate ACPR and NPR to Two-tone IMR and IP3. *Microwave Journal*.

Chengzhou, W., Vaidyanathan, M., & Larson, L. E. (2004). A capacitance-compensation technique for improved linearity in CMOS class-AB power amplifiers. *IEEE Journal of Solid-State Circuits, 39*(11), 1927-1937. doi:10.1109/JSSC.2004.835834

Clark, C. J., Silva, C. P., Moulthrop, A. A., & Muha, M. S. (2002). Power-amplifier characterization using a two-tone measurement technique. *IEEE Transactions on Microwave Theory and Techniques, 50*(6), 1590-1602. doi:10.1109/TMTT.2002.1006421

Constantin, N. (May 18, 2010). U.S. Patent 7 719 354 B2.

Constantin, N. G., Kwok, K. H., Shao, H., Cismaru, C., & Zampardi, P. J. (2012). Formulations and a Computer-Aided Test Method for the Estimation of IMD Levels in an Envelope Feedback RFIC Power Amplifier. *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 31*(12), 1881-1893. doi:10.1109/TCAD.2012.2207954

Darraji, R., Mousavi, P., & Ghannouchi, F. M. (2016). Doherty Goes Digital: Digitally Enhanced Doherty Power Amplifiers. *IEEE Microwave Magazine, 17*(8), 41-51. doi:10.1109/MMM.2016.2561478

Deltimple, N., Leyssenne, L., Kerhervé, E., Deval, Y., & Belot, D. (2010, 2-4 June 2010). *Dynamic biasing techniques for RF power amplifier linearity and efficiency improvement.* Paper presented at the 2010 IEEE International Conference on Integrated Circuit Design and Technology.

Deltimple, N., Leyssenne, L., Kerhervé, E., Deval, Y., & Belot, D. (2010, 2-4 June 2010). *Dynamic biasing techniques for RF power amplifier linearity and efficiency improvement.* Paper presented at the 2010 IEEE International Conference on Integrated Circuit Design and Technology.

Draxler, P. J. (2013). *Behavioral Modeling of Nonlinearities and Memory Effects in Power Amplifiers.* (Doctoral thesis), University of California, San Diego, US, Retrieved from https://escholarship.org/uc/item/1fz1h8m3

El-Shennawy, M., Joram, N., & Ellinger, F. (2016, 27-30 June 2016). *A 55 dB range gain interpolating variable gain amplifier with improved offset cancellation.* Paper presented at the 2016 12th Conference on Ph.D. Research in Microelectronics and Electronics (PRIME).

Fager, C., Eriksson, T., Barradas, F., Hausmair, K., Cunha, T., & Pedro, J. C. (2019). Linearity and Efficiency in 5G Transmitters: New Techniques for Analyzing Efficiency, Linearity, and Linearization in a 5G Active Antenna Transmitter Context. *IEEE Microwave Magazine, 20*(5), 35-49. doi:10.1109/MMM.2019.2898020

Fager, C., Pedro, J. C., Carvalho, N. B. d., Zirath, H., Fortes, F., & Rosario, M. J. (2004). A comprehensive analysis of IMD behavior in RF CMOS power amplifiers. *IEEE Journal of Solid-State Circuits, 39*(1), 24-34. doi:10.1109/JSSC.2003.820860

Fisher, P. O., & Al-Sarawi, S. F. (2016, 5-6 Dec. 2016). *Memoryless AM/AM Behavioral Model for RF Power Amplifiers.* Paper presented at the 2016 3rd Asia-Pacific World Congress on Computer Science and Engineering (APWC on CSE).

Forestier, S., Bouysse, P., Quere, R., Mallet, A., Nebus, J., & Lapierre, L. (2004). Joint optimization of the power-added efficiency and the error-vector measurement of 20-GHz pHEMT amplifier through a new dynamic bias-control method. *IEEE Transactions on Microwave Theory and Techniques, 52*(4), 1132-1141. doi:10.1109/TMTT.2004.825745

Ghannouchi, F. M., Cardinal, J., & Hajji, R. (1995, 24-27 July 1995). *An adaptive linearizer using feedback and dynamic biasing techniques for SSPAs.* Paper presented at the Proceedings of 1995 SBMO/IEEE MTT-S International Microwave and Optoelectronics Conference.

Gibiino, G. P., Avolio, G., Schreurs, D. M. M., Santarelli, A., & Filicori, F. (2016). A Three-Port Nonlinear Dynamic Behavioral Model for Supply-Modulated RF PAs. *IEEE Transactions on Microwave Theory and Techniques, 64*(1), 133-147. doi:10.1109/TMTT.2015.2504467

Gibiino, G. P., Santarelli, A., Schreurs, D., & Filicori, F. (2017). Two-Input Nonlinear Dynamic Model Inversion for the Linearization of Envelope-Tracking RF PAs. *IEEE Microwave and Wireless Components Letters, 27*(1), 79-81. doi:10.1109/LMWC.2016.2630005

Gilabert, P. L., Cesari, A., Montoro, G., Bertran, E., & Dilhac, J. (2008). Multi-Lookup Table FPGA Implementation of an Adaptive Digital Predistorter for Linearizing RF Power Amplifiers with Memory Effects. *IEEE Transactions on Microwave Theory and Techniques, 56*(2), 372-384. doi:10.1109/TMTT.2007.913369

Hammi, O., Carichner, S., Vassilakis, B., & Ghannouchi, F. M. (2008, 15-20 June 2008). *Novel approach for static nonlinear behavior identification in RF power amplifiers*

exhibiting memory effects. Paper presented at the 2008 IEEE MTT-S International Microwave Symposium Digest.

Hedayati, H., Mobarak, M., Varin, G., Meunier, P., Gamand, P., Sanchez-Sinencio, E., & Entesari, K. (2012). A 2-GHz Highly Linear Efficient Dual-Mode BiCMOS Power Amplifier Using a Reconfigurable Matching Network. *IEEE Journal of Solid-State Circuits, 47*(10), 2385-2404. doi:10.1109/JSSC.2012.2203460

Hekkala, A., Kotelba, A., Lasanen, M. et al. (January 2012). *Novel Digital Compensation Approaches for Envelope Tracking Amplifiers* (Vol. 62): Springer US.

Hyunchul, K., & Kenney, J. S. (2001, 20-24 May 2001). *Estimation of error vector magnitude using two-tone intermodulation distortion measurements [power amplifier]*. Paper presented at the 2001 IEEE MTT-S International Microwave Symposium Digest (Cat. No.01CH37157).

J. C. Pedro, N. B. C. (2003). *Intermodulation Distortion in Microwave and Wireless Circuits*. Norwood, MA: Artech House.

Jang, H., Wilson, R., Canning, T., Seebacher, D., Schuberth, C., Arigong, B., Trang, F., Ward, S. (2016). RF-Input Self-Outphasing Doherty–Chireix Combined Amplifier. *IEEE Transactions on Microwave Theory and Techniques, 64*(12), 4518-4534. doi:10.1109/TMTT.2016.2618922

Javed, A., Shahid, M. A., Sharif, M., & Yasmin, M. (2017). Energy Consumption in Mobile Phones. Retrieved from https://pdfs.semanticscholar.org/3a95/fb408c04e7fff2edbc59abced45283b0b849.pdf

Joung, J., Ho, C. K., & Sun, S. (2013). Power Amplifier Switching (PAS) for Energy Efficient Systems. *IEEE Wireless Communications Letters, 2*(1), 14-17. doi:10.1109/WCL.2012.092612.120620

Kang, H., Lee, H., Oh, H., Lee, W., Park, C. S., Hwang, K. C., Lee, K.Y., Yang, Y. (2017). Symmetric Three-Way Doherty Power Amplifier for High Efficiency and Linearity. *IEEE Transactions on Circuits and Systems II: Express Briefs, 64*(8), 862-866. doi:10.1109/TCSII.2016.2609460

Kang, S., Baek, D., & Hong, S. (2017). A 5-GHz WLAN RF CMOS Power Amplifier with a Parallel-Cascoded Configuration and an Active Feedback Linearizer. *IEEE Transactions on Microwave Theory and Techniques, 65*(9), 3230-3244. doi:10.1109/TMTT.2017.2691766

Kang, S., Sung, E., & Hong, S. (2018). Dynamic Feedback Linearizer of RF CMOS Power Amplifier. *IEEE Microwave and Wireless Components Letters, 28*(10), 915-917. doi:10.1109/LMWC.2018.2861881

Katz, A., Wood, J., & Chokola, D. (2016). The Evolution of PA Linearization: From Classic Feedforward and Feedback Through Analog and Digital Predistortion. *IEEE Microwave Magazine, 17*(2), 32-40. doi:10.1109/MMM.2015.2498079

Keysight. Digital Pre-Distortion (DPD) Concept. http://rfmw.em.keysight.com/wireless/helpfiles/n7614/Content/Main/Digital%20Pre-Distortion%20(DPD)%20Concept.htm

Koo, B., Joo, T., Na, Y., & Hong, S. (2012, 19-23 Feb. 2012). *A fully integrated dual-mode CMOS power amplifier for WCDMA applications.* Paper presented at the 2012 IEEE International Solid-State Circuits Conference.

Koo, H., Kang, H., Lee, W., Lee, H., Lee, K., Hwang, K. C., & Yang, Y. (2018). GaN-HEMT asymmetric three-way Doherty power amplifier using GPD. *IET Microwaves, Antennas & Propagation, 12*(13), 2115-2121. doi:10.1049/iet-map.2018.5464

Lau, K. W., Xue, Q., & Chan, C. H. (2007, 11-14 Dec. 2007). *A Novel Biasing Technique for Low Adjacent Channel Power in Microwave Power Amplifiers.* Paper presented at the 2007 Asia-Pacific Microwave Conference.

Lavrador, P. M., Cunha, T. R., Cabral, P. M., & Pedro, J. C. (2010). The Linearity-Efficiency Compromise. *IEEE Microwave Magazine, 11*(5), 44-58. doi:10.1109/MMM.2010.937100

Maas, S. A. (2003). *Nonlinear Microwave and RF Circuits*. Norwood, MA, USA: Artechhouse.

Medrel, P., Reveyrand, T., Martin, A., Bouysse, P., Nébus, J., & Sombrin, J. (2013, 7-9 April 2013). *Time domain envelope characterization of power amplifiers for linear and high efficiency design solutions.* Paper presented at the WAMICON 2013.

Miers, T. H., & Hirsch, V. A. (1992, 1-5 June 1992). *A thorough investigation of dynamic bias on linear GaAs FET power amplifier performance.* Paper presented at the 1992 IEEE MTT-S Microwave Symposium Digest.

Mkadem, F. (2014). *Behavioral Modeling and Digital Predistortion of Wide- and Multi-Band Transmitter Systems.* (Doctoral thesis), University of Waterloo, Ontario, Canada, Retrieved from http://hdl.handle.net/10012/8815

Moon, J., Son, J., Kim, J., Kim, I., Jee, S., Woo, Y. Y., & Kim, B. (2010, 23-28 May 2010). *Doherty amplifier with envelope tracking for high efficiency.* Paper presented at the 2010 IEEE MTT-S International Microwave Symposium.

Nam, J., & Kim, B. (2007). The Doherty Power Amplifier with On-Chip Dynamic Bias Control Circuit for Handset Application. *IEEE Transactions on Microwave Theory and Techniques, 55*(4), 633-642. doi:10.1109/TMTT.2007.892800

Niknejad, A. M., Chowdhury, D., & Chen, J. (2012). Design of CMOS Power Amplifiers. *IEEE Transactions on Microwave Theory and Techniques, 60*(6), 1784-1796. doi:10.1109/TMTT.2012.2193898

Onizuka, K., Ikeuchi, K., Saigusa, S., & Otaka, S. (2012, 12-14 Nov. 2012). *A 2.4 GHz CMOS Doherty power amplifier with dynamic biasing scheme.* Paper presented at the 2012 IEEE Asian Solid State Circuits Conference (A-SSCC).

Park, B., Jin, S., Jeong, D., Kim, J., Cho, Y., Moon, K., & Kim, B. (2016). Highly Linear mm-Wave CMOS Power Amplifier. *IEEE Transactions on Microwave Theory and Techniques, 64*(12), 4535-4544. doi:10.1109/TMTT.2016.2623706

Pedro, J. C., & Maas, S. A. (2005). A comparative overview of microwave and wireless power-amplifier behavioral modeling approaches. *IEEE Transactions on Microwave Theory and Techniques, 53*(4), 1150-1163. doi:10.1109/TMTT.2005.845723

Pedro, J., Carvalho, N., Fager, C., & García, J. (2004). Linearity versus efficiency in mobile handset power amplifiers: A battle without a loser. 19-26.

Po-Chih, W., Kai-Yi, H., Yu-Fu, K., Ming-Chong, H., Chao-Hua, L., Tzung-Ming, C., Chia-Jun, C., Ka-Un, C., Ta-Hsun, Y., Wen-Shan, W., Ying-Hsi, L., Chao-Cheng, L. (2008, 15-19 Sept. 2008). *A 2.4-GHz +25dBm P-1dB linear power amplifier with dynamic bias control in a 65-nm CMOS process.* Paper presented at the ESSCIRC 2008 - 34th European Solid-State Circuits Conference.

Presti, C. D., Carrara, F., Scuderi, A., Asbeck, P. M., & Palmisano, G. (2009). A 25 dBm Digitally Modulated CMOS Power Amplifier for WCDMA/EDGE/OFDM with Adaptive Digital Predistortion and Efficient Power Control. *IEEE Journal of Solid-State Circuits, 44*(7), 1883-1896. doi:10.1109/JSSC.2009.2020226

Qi, T., & He, S. (2019). Power Up Potential Power Amplifier Technologies for 5G Applications. *IEEE Microwave Magazine, 20*(6), 89-101. doi:10.1109/MMM.2019.2904409

Sahu, B., & Rincon-Mora, G. A. (2007). A High Efficiency WCDMA RF Power Amplifier with Adaptive, Dual-Mode Buck-Boost Supply and Bias-Current Control. *IEEE Microwave and Wireless Components Letters, 17*(3), 238-240. doi:10.1109/LMWC.2006.890505

Sharma, S., & Constantin, N. G. (2013). Formulations for the Estimation of IMD Levels in an Envelope Feedback RFIC Amplifier: An Extension to Dynamic AM and PM Behavior. *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 32*(12), 2019-2023. doi:10.1109/TCAD.2013.2270284

Sharma, S., & Constantin, N. G. (2019). Nonlinear Three-Port Representation of PAs for Embedded Self-Calibration of Envelope-dependent Dynamic Biasing Implementations. *IEEE Access, vol. 7,* 172796-172815. doi:10.1109/ACCESS.2019.2956721

Sharma, S., & Constantin, N. G. (2014, 4-7 May 2014). *An algorithm for IMD computation in automated tests of RFIC power amplifiers.* Paper presented at the 2014 27th IEEE Canadian Conference on Electrical and Computer Engineering (CCECE).

Sharma, S., & Constantin, N. G. (Apr. 2018). United States Patent No. US 2018/0316312 A1.

Sharma, S., & Constantin, N. G. (Jan. 2018). United States Patent No. US 10 ,320 ,345 B2

Sharma, S., Constantin, N. G., & Soliman, Y. (2017, 19-20 April 2017). *Positive envelope feedback for linearity improvement in RFIC PAs.* Paper presented at the 2017 27th International Conference Radioelektronika (RADIOELEKTRONIKA).

Shen, Y., Gajadharsing, J., & Tauritz, J. (2007, 11-14 Dec. 2007). *Behavioral Modeling of Microwave Power Amplifiers Using a Look Up Table Method.* Paper presented at the 2007 Asia-Pacific Microwave Conference.

SKY85402-11: High-Power (+22 dBm) 802.11ac WLAN PA with Integrated Power Detector [Data sheet]. (August 21, 2018). http://www.skyworksinc.com/uploads/documents/SKY85402_11_202120L.pdf

Skyworks Solutions, I. (Oct.2013). *SE5003L1-R: High-Power (+19 dBm) 802.11ac WLAN Power Amplifier with Integrated Power Detector*.

Son, J., Kim, I., Moon, J., Lee, J., & Kim, B. (2011, 7-9 Nov. 2011). *A highly efficient asymmetric Doherty Power Amplifier with a new output combining circuit.* Paper presented at the 2011 IEEE International Conference on Microwaves, Communications, Antennas and Electronic Systems (COMCAS 2011).

T.Burns, C. (2013). GaN on SiC: RFMD High Power Doherty Design, Modeling and Measurement [PowerPoint slides]. Retrieved from https://www.keysight.com/upload/cmc_upload/All/7March2013Webcast.pdf

Tafuri, F. F., Sira, D., Jensen, O. K., & Larsen, T. (2013, 6-10 Oct. 2013). *Efficiency enhancement of an envelope tracking power amplifier combining supply shaping and dynamic biasing.* Paper presented at the 2013 European Microwave Conference.

Tam, S., Lu, Y., Nick, M., Zhao, Y., Wong, A., Winoto, R., & Lin, L. (2015, 17-19 May 2015). *A dual band (2G/5G) IEEE 802.11b/g/n/ac 80MHz bandwidth AMAM envelope feedback power amplifier with digital pre-distortion.* Paper presented at the 2015 IEEE Radio Frequency Integrated Circuits Symposium (RFIC).

Tehrani, A. S., Cao, H., Afsardoost, S., Eriksson, T., Isaksson, M., & Fager, C. (2010). A Comparative Analysis of the Complexity/Accuracy Tradeoff in Power Amplifier Behavioral Models. *IEEE Transactions on Microwave Theory and Techniques, 58*(6), 1510-1520. doi:10.1109/TMTT.2010.2047920

Thangarasu, B. K., Ma, K., & Yeo, K. S. (2017, 4-9 June 2017). *A 0.029 mm^2 8 Gbit/s current-mode AGC amplifier with reconfigurable closed-loop control in 65 nm CMOS.* Paper presented at the 2017 IEEE MTT-S International Microwave Symposium (IMS).

Walsh, K. (September 2010). RF Switches Guide Signals in Smart Phones. Retrieved from http://www.skyworksinc.com/downloads/press_room/published_articles/Microwave_RF_092010.pdf

Wong, J., Watanabe, N., & A. Grebennikov. (Oct 07, 2017). Doherty Amplifier Combines High Power and Efficiency. Retrieved from https://www.mwrf.com/materials/doherty-amplifier-combines-high-power-and-efficiency#close-olyticsmodal

Xia, J., & Boumaiza, S. (2015). A Novel Broadband Linear-in-Magnitude RF Envelope Detector with Enhanced Detection Speed and Accuracy. *IEEE Microwave and Wireless Components Letters, 25*(5), 325-327. doi:10.1109/LMWC.2015.2409796

Yang, Y., Yi, J., Nam, J., & Kim, B. (2000). Behavioral modeling of high power amplifiers based on measured two-tone transfer characteristics. *Microwave Journal, 43*(12), 90-104.

Yu, C., Feng, J., & Zhao, D. (2018, 3-6 Sept. 2018). *A 28-GHz CMOS Broadband Single-Path Power Amplifier with 17.4-dBm P1dB for 5G Phased-Array.* Paper presented at

the ESSCIRC 2018 - IEEE 44th European Solid State Circuits Conference (ESSCIRC).

Yu, Z., Iwamoto, M., Larson, L. E., & Asbeck, P. M. (2003, 8-13 June 2003). *Doherty amplifier with DSP control to improve performance in CDMA operation.* Paper presented at the IEEE MTT-S International Microwave Symposium Digest, 2003.

Zargari, M. (2012, 17-19 June 2012). *The path towards Gb/s wireless LANs.* Paper presented at the 2012 IEEE Radio Frequency Integrated Circuits Symposium.

Zhang, Z., & Xin, Z. (2014, 12-15 Aug. 2014). *A LTE Doherty power amplifier using Envelope tracking technique.* Paper presented at the 2014 15th International Conference on Electronic Packaging Technology.

Zhao, C., Liu, H., Wu, Y., & Kang, K. (2017). Analysis and Design of CMOS Doherty Power Amplifier Based on Voltage Combining Method. *IEEE Access, 5*, 5001-5012. doi:10.1109/ACCESS.2017.2678678