A High-Voltage Multi-purpose On-the-fly Reconfigurable Half-bridge Gate Driver for GaN HEMTs in 0.18-μm HV SOI CMOS Technology

by

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Pilote de Grille pour Dispositifs GaN à Demi-pont Reconfigurable à Usages Multiples de Haute Tension en Technologie SOI CMOS HT 0.18-μm

Nam LY

RÉSUMÉ

En raison de vitesses de commutation plus élevées, de faible résistance à l'état passant et de taille miniaturisée en comparaison avec des contreparties en silicium, l'utilisation de transistors de puissance à base de nitrure de gallium (GaN) est de plus en plus courante dans les circuits de puissances modernes. Avec des figures de mérite supérieures, les convertisseurs de puissance utilisant des dispositifs GaN peuvent fonctionner à des fréquences de commutation élevées. Cela se traduit par des dimensions plus petites, une efficacité supérieure et une réduction du coût du système. La redondance et la reconfigurabilité sont souhaitables dans les applications critiques pour la sécurité telles que les systèmes automobiles et aérospatiaux. Ces derniers fonctionnent dans des conditions difficiles nécessitant un niveau élevé de flexibilité et une grande fiabilité. Ce mémoire présente un circuit de pilotage de grille pour un tel système d'alimentation reconfigurable.

Destiné à être au coeur d'un système d'alimentation haute tension (HT) programmable et flexible, le pilote de grille présenté dans ce travail est capable de commander une large gamme de dispositifs GaN de différentes tailles. Cela est accompli en ayant un mécanisme configurable de vitesse de mis-à-on et mis-à-off. Cette fonctionnalité élimine le besoin de résistances de grille discrètes. Elle permet donc des conceptions de circuits plus denses, telles que l'intégration de système dans un boîtier (SiP - system-in-package). Dans un tel système les pilotes de grille, les dispositifs GaN et d'autres circuits intégrés de commande sont placés sur le même interposeur. La vitesse configurable de mis-à-on et de mis-à-off reconfigurable permet également de réduire les interférences électromagnétiques (EMI). Cela est important dans les applications critiques pour la sécurité. Une structure uniforme d'unités de commutation en demi-pont est proposée. Cette dernière permet une reconfigurabilité du fonctionnement du système avec une variété de topologies possibles à l'aide d'un grand nombre de cellules de commutation. Le pilote de grille exige un circuit de décalage de niveau de 200 V intégré. Ce circuit utilise une technique d'annulation de bruit en mode commun, ayant fait l'objet d'une étude approfondie. En utilisant cette technique dans une technologie HT SOI (silicium sur isolant), une immunité à une variation de bruit (CMTI) de 80 V/ns est obtenue. Le pilote de grille a un temps mort configurable allant de 5 ns à 60 ns. Ce temps mort configurable minimise les pertes dues à la conduction par mécanisme de «diode de corps» des transistors GaN pendant la période de conduction en roue libre pour différents profils de charge. Toutes les configurations sont programmées à travers un registre à décalage.

Le circuit de pilotage de grille a été fabriqué avec le procédé SOI de 200-V 0,18-μm (XFAB XT018). Les résultats expérimentaux montrent que la puce peut piloter les transistors GaN ciblés de la plus petite à la plus grande taille aux vitesses de mis-à-on et mis-à-off souhaitées. Une vitesse de 1,46 / 1,18 ns de temps de montée / descente est atteinte. Le temps mort mesuré est de

4,5 ns à 58 ns avec une tension d'entrée jusqu'à 86 V. Ces paramètres peuvent être reconfigurés à-chaud (on-the-fly) pendant que le circuit est en train de commuter à une fréquence jusqu'à 20 MHz. Ce travail contribue à l'avancement de la conception de pilotes de grille universels, en particulier pour les transistors GaN, et aux systèmes de puissance reconfigurables.

Mots-clés: Aérospatiale, CMOS, décalage de niveau, demi-pont, GaN, pilote de grille, reconfigurable

A High-Voltage Multi-purpose On-the-fly Reconfigurable Half-bridge Gate Driver for GaN HEMTs in 0.18-μm HV SOI CMOS Technology

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ABSTRACT

Nowadays, the use of Gallium Nitride (GaN) power transistors in power electronics is common, due to higher switching speeds, lower on-resistance and smaller size compared to silicon counterparts. With superior figures of merit, power converters utilizing GaN devices can operate at high switching frequencies, which translates into smaller size, higher efficiency and lower system cost. Redundancy and reconfigurability are highly desirable for safety-critical applications such as automotive and aerospace systems that operate under harsh conditions and require a high degree of flexibility together with high reliability. This thesis presents a gate driver for such a reconfigurable power system.

Intended to be the core design of a programmable and flexible high-voltage (HV) power system, the gate driver in this work is capable of driving a wide range of GaN devices with different sizes by having independently configurable turn-on and turn-off resistance paths. This feature eliminates the need for discrete gate resistors and allows for higher density designs, such as System-in-Package integration (SiP) where the gate drivers, GaN devices and other control integrated circuits are placed on the same interposer. Reconfigurable driving strength also allows for electromagnetic interference (EMI) reduction, which is important in safety-critical applications. A uniform structure of half-bridge switching units is proposed, enabling reconfigurability in the operation of the system with a variety of possible topologies, out of a large array of switching cells. The gate driver requires a built-in 200-V level shifter, with common-mode noise cancellation technique, thoroughly investigated and migrated to HV SOI technology, which is immune against a 80-V/ns slew rate of fast switching GaN devices despite excessive parasitics in the process and the packaging technique employed. The gate driver has a configurable dead-time ranging from 5 ns to 60 ns that minimizes loss due to so-called "body diode" conduction of the GaN FETs during freewheeling for different load profiles. All the configurations are set via shift registers.

The gate driver has been fabricated in a 200-V 0.18-μm silicon-on-insulator (SOI) process (XFAB XT018). Measurement results show that the chip can drive targeted GaN HEMTs from smallest to largest size at the desired turn-on and turn-off speeds, as fast as 1.46/1.18 ns of rise/fall-time. The measured dead-time is from 4.5 ns to 58 ns with an input voltage up to 86 V. The parameters can be reconfigured on-the-fly at a pulse width modulation switching frequency up to 20 MHz. This work contributes to the advancement of universal gate driver design, especially for GaN transistors, and toward reconfigurable power systems.

Keywords: Aerospace, CMOS, GaN, gate driver, half-bridge, level shifter, reconfigurable

TABLE OF CONTENTS

Page

LIST OF TABLES

LIST OF FIGURES

LIST OF ABBREVIATIONS

BJT	Bipolar Junction Transistor
CMOS	Complementary Metal Oxide Semiconductor
CMTI	Common-mode Transient Immunity
CPIOS	Configurable integrated Power Input/Output System
CPU	Central Processing Unit
DT	Dead-time
ÉTS	École de Technologie Supérieure
FET	Field Effect Transistor
FPGA	Field-Programmable Gate Array
GaN	Gallium Nitride
HEMTs	High Electron Mobility Transistors
HS	High-side
HW	Hardware
IC	Integrated circuit
IGBT	Insulated Gate Bipolar Transistor
LS	Low-side
MCU	Microcontroller Unit
nMOS	N-channel Metal Oxide Semiconductor
PCB	Printed Circuit Board

PD	Pull-down
PMIC	Power Management Integrated Circuit
pMOS	P-channel Metal Oxide Semiconductor
PU	Pull-up
PVT	Process Voltage Temperature
SiC	Silicon Carbide
SW	Switching
WBG	Wide Bandgap

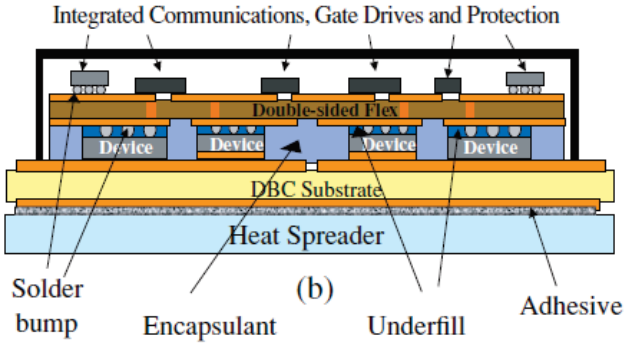
LIST OF SYMBOLS AND UNITS OF MEASUREMENTS

A	ampère
mA	mili-ampère
μA	micro-ampère
nA	nano-ampère
V	volt
mV	mili-volt
μV	micro-volt
nV	nano-volt
W	watt
mW	mili-watt
μW	micro-watt
nW	nano-watt
s	second
ms	mili-second
μs	micro-second
ns	nano-second

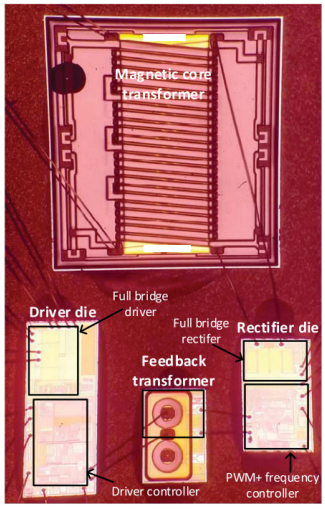
INTRODUCTION

Motivation

In 72 years since the first transistor came to life (Riordan, 2004) and more than 60 years of integrated circuit (IC) history (Moore, 2006), the computer has transformed from house form-factor into palm size. That has been a fantastic time where all aspects of society have been impacted with the modernization thanks to these two moments in history. Processing and communication systems have become more and more sophisticated, especially in aerospace and automotive applications. In safety-critical applications, such as fly-by-wire and actuator control in aircraft, some parts are duplicated, triplicated or even quadrupled according to desired fault probability (Patton, 1991). The redundancy obviously increases system cost, size and weight. More functionalities and features implemented demand higher integration to diminish or at least retain system size.



a) Power SiP (Lee *et al.*, 2002)



b) Isolated power transfer SiP (Lee *et al.*, 2002)

Figure 0.1 Power SiP in the literature

Power electronic circuits, occupying a large portion of the volume of a power supply, have been partially shrunk by introducing power semiconductor modules (Lee *et al.*, 2002). Other integrated components such as inductors, transformers, capacitors and control circuits require each a dedicated technology (Thomas *et al.*, 2018; Zhuo *et al.*, 2019; Jia & Gu, 2018; Wang *et al.*, 2018). The sub-system integration thus leads to a heterogeneous system or system-in-package (SiP) as illustrated in Figure 0.1.

Nowadays, wide bandgap (WBG) transistors are commonly used in power electronics due to superior figures of merit (FOM) which exceed the electrical boundary of silicon counterparts (Millán *et al.*, 2014). Furthermore, the reliability of silicon carbide (SiC) and gallium nitride (GaN) devices, the two mature WBG technologies, has been significantly improved over the last few years (Bindra, 2015b). GaN-based devices are suitable for 600-V range while SiC transistors are the candidates for kV range applications (Bindra, 2015a). These reasons make GaN high electron mobility transistor (HEMT) the best candidate as the power switch for a <200-V configurable power input/output system (CPIOS) (Figure 0.2b) for, but not limited to, aerospace applications. This CPIOS aims at shrinking overall system volume by replacing bulky power electronic parts with multiple configurable power SiPs (Figure 0.2c). Smaller system size relaxes the physical constraints associated with redundancy.

Towards the Reconfigurable Power System

As an important part of the CPIO-SiP, the gate driver in this work is designed to be universal, i.e. capable of driving a range of commercial bare-die GaN devices of different sizes (Figure 0.2d) without the need of hardware change or external gate resistor. Thus, it can be used with appropriate GaN devices per output electrical specification for the optimum SiP size and efficiency. The gate driver only needs to be placed close to the GaN transistors that it drives and the settings are handled by the configuration/status handler (CSH). The gate driver can drive a single GaN device or two of them in half-bridge topology with a configurable dead-time (DT).

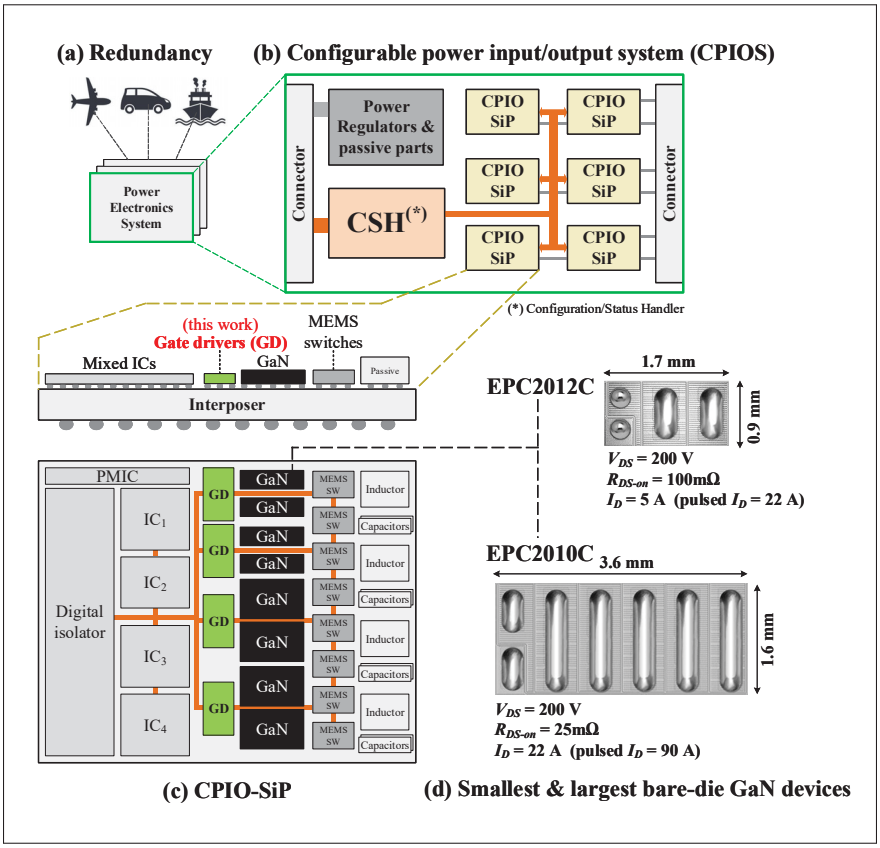


Figure 0.2 Redundancy in automotive applications, GaN devices are from EPC

In half-bridge configuration, the gate driver is robust against the high dV/dt slew rate of the switching (SW) node.

Contributions to Research

- The design, tape-out and testing of a versatile gate driver for GaN half-bridge (1–5.3 nC gate charge) with configurable speeds and dead-time with 226 V/ns CMTI.
- IEEE Publication:

N. Ly, N. Aimaier, A. H. Alameh, Y. Blaquière, G. Cowan and N. G. Constantin (2020). *A High Voltage Multi-Purpose On-the-fly Reconfigurable Half-Bridge Gate Driver for GaN HEMTs in 0.18-µm HV SOI CMOS Technology*. 2020 18th IEEE International New Circuits and Systems Conference (NEWCAS). **(ACCEPTED)**

Overview of This Thesis

This thesis consists of four chapters. Chapter 1 is an overview of gate driver concept, wide bandgap semiconductors and challenges of driving GaN transistors. A literature review of gate driver for GaN devices is discussed in Chapter 2. The design and simulation of the gate driver is outlined in Chapter 3 and its performance is examined and reported in Chapter 4.

CHAPTER 1

BACKGROUND

1.1 Introduction

Before discussing the main topic, the gate driver design, it is important to have a relevant background. This chapter gives an overview of the concept of DC/DC converter, gate driver, wide bandgap semiconductors and the challenges of driving GaN transistors.

1.2 Fundamentals of DC/DC converter

DC to DC converters are ubiquitous, from consumer electronics to electric vehicles. Such electronic devices often have multiple sub-circuits with their own supply level requirements different from the main input power which is either a built-in battery or an external supply. The supply of each sub-circuit can be either lower or higher than the main supply rail. Therefore, there are a lot of different types and topologies of DC/DC converter. They can be categorized into two main types: isolated and non-isolated.

Table 1.1 Non-isolated DC/DC converter topologies comparison

Category	**Topology**	**Property**
Step-down	Buck	$\|V_{out}\| < \|V_{in}\|$, same polarity
Step-up	Boost	$\|V_{out}\| > \|V_{in}\|$, same polarity
Step-up/down ($\|V_{out}\|$ can be higher or lower than $\|V_{in}\|$)	Buck-Boost	$V_{out} < 0$, simple structure & control
	Ćuk	$V_{out} < 0$, low input current ripple
	SEPIC	$V_{out} > 0$, low input current ripple
	Zeta	$V_{out} > 0$, high input current ripple
	Four-switch buck-Boost	$V_{out} > 0$, simple structure, complex control

The isolated ones, as the name suggests, have their output isolated from the input with transformers. The benefits of this type are safety, noise isolation and floating output which are useful in some applications. However, the drawbacks of isolated DC/DC converters are big size, high cost and low efficiency. In the context of CPIO-SiP project, non-isolated type is preferable thanks to

its higher efficiency, lower cost due to low number of components, and especially smaller size that favours high density designs. Table 1.1 details the typical non-isolated DC/DC converter topologies which are depicted in Figure 1.1.

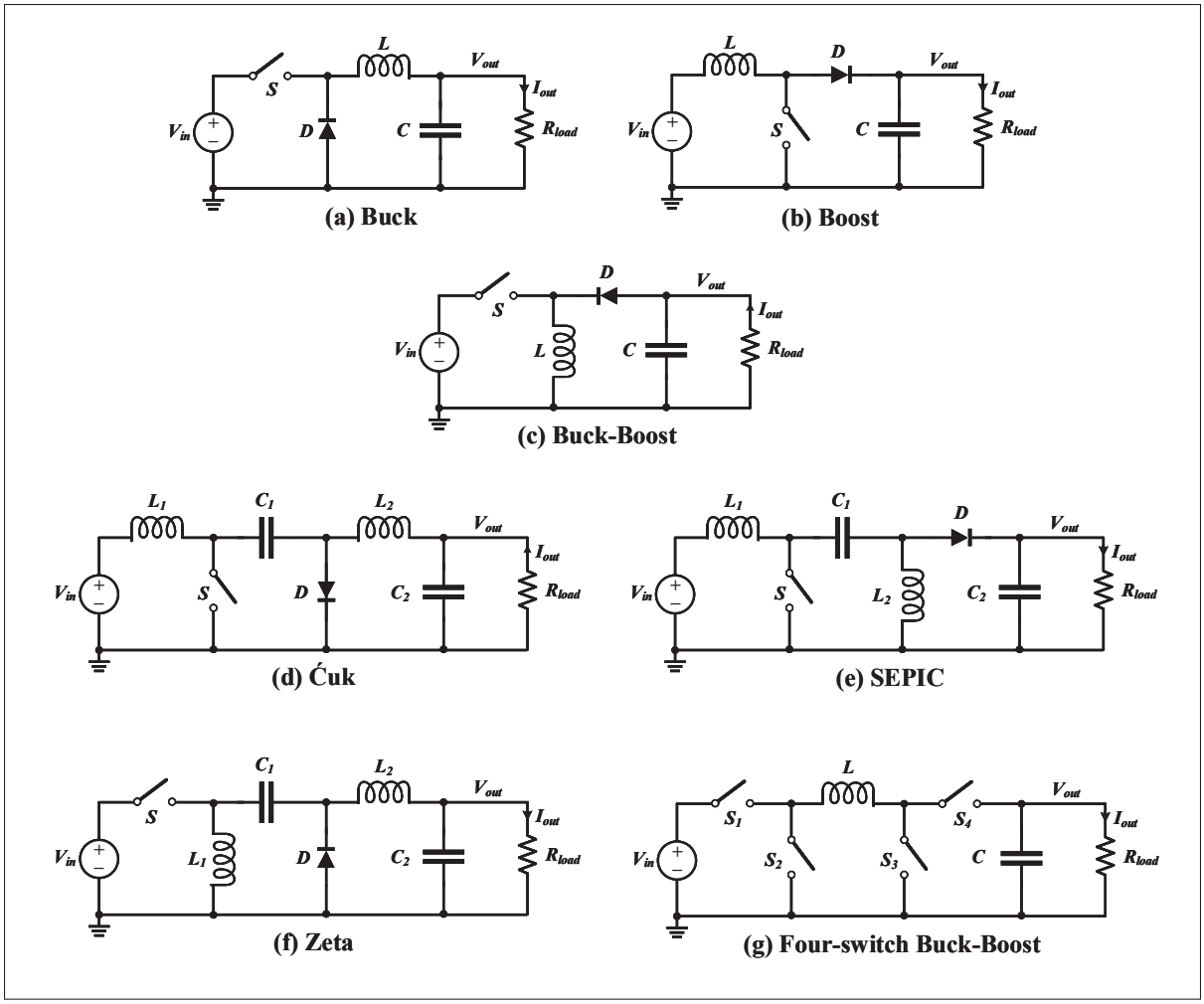


Figure 1.1 Typical non-isolated DC/DC converter topologies

In order to support the topology reconfigurability in CPIO-SiP, the half-bridge structure is chosen as the switching unit (SU). One SU can operate as either synchronous buck or synchronous boost typology. Two SUs can be combined to form a four-switch buck-boost as outlined in Figure 1.2. The power router can be realized using MEMS (Micro Electro-Mechanical System) switches. These MEMS switches do not need to switch fast but they must support high current in on-state and high voltage in off-state.

This solution has below advantages:

1. Uniform structure,
2. Scalable,
3. Covering both step-down and step-up with buck, boost and buck-boost topology.

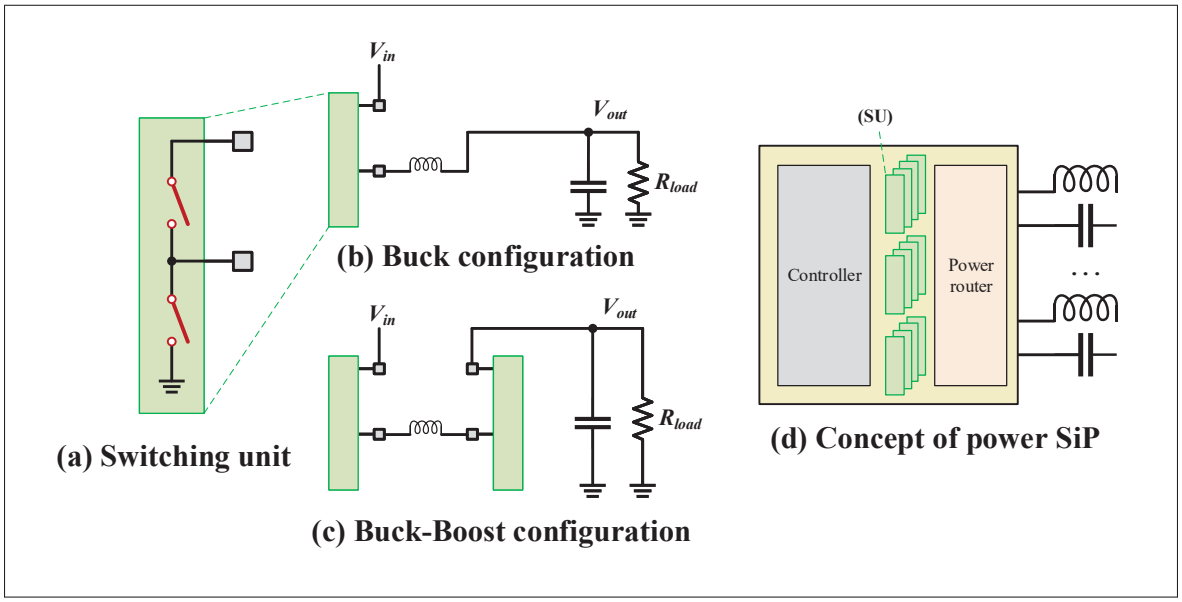


Figure 1.2 Switching unit and power SiP concept

In half-bridge operation, if high-side (HS) and low-side (LS) transistors turn on at the same time, they will form a low impedance path which shorts out power rail to ground. This is called shoot-through or cross-conduction catastrophe which causes the power devices over heat resulting in reliability degradation or even permanent damage. Therefore, this incident must be avoided. To prevent this, there should be time margin from the moment one transistor is off to the moment the other transistor is ON. This time margin is called dead-time (DT) and described in Figure 1.3. Depending on applications and electrical specifications, DT can range from nanoseconds to milliseconds.

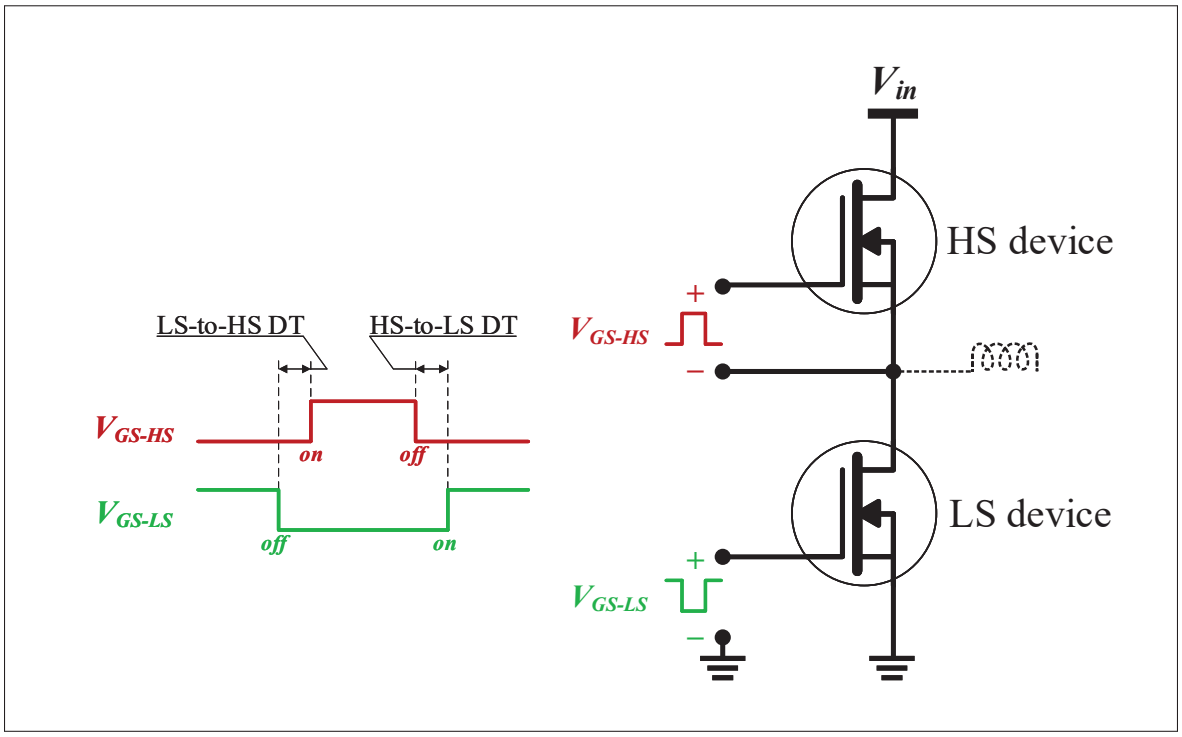


Figure 1.3 Dead-time in half-bridge operation

1.3 Why Gate Driver?

Before the 1980s, the world of solid-state circuits witnessed the golden era of bipolar transistors (BJT) after they had replaced the vacuum tubes in radio and television. The power BJTs were robust but had a low current gain (beta) of <10 (White, 2018). Thus, a 10-A on-state requires at least 1-A continuous base current. Furthermore, the turn-off of BJTs demands a negative base current to remove all base-emitter charge. The fast turn-off hence needs a large negative current. There had been works addressing this issue such as Baker clamp and other feedback techniques.

Since the 1980s, the MOSFETs had become more mature to replace the BTJs in power supplies as they have fast switching speed and required voltage drive instead of "base drive" current. In contrast to BJTs, MOSFETs do not require power input to maintain an ON or OFF-state. The gate capacitor, formed by the gate terminal, oxide layer and the active region, must be charged or discharged to switch the MOSFETs. The gate capacitor has to be charged to a certain required voltage, so-called threshold voltage (V_{th}), for the MOSFET to be ON. Similarly, this charge

must be depleted to turn the transistor off. When switching, MOSFETs do not instantly transit between the non-conducting and the conducting state. In fact, the transition time is inversely proportional to the charge and discharge speed of the gate capacitor, the typical range is from nanoseconds to milliseconds depending on power ratings and applications.

Let's examine an n-channel MOSFET driving a resistor in Figure 1.4. For simplicity, let's consider this an ideal MOSFET with zero on-state resistance. The applied voltage V_G to the gate rises from 0 V to surpass V_{th} to turn it ON. At t_1, when V_G equals V_{th}, the transistor starts to conduct and the drain current I_D starts to rise from 0 A while V_D starts to fall from V_{in}. At t_2, when V_D reaches 0 V, I_D reaches it max value. The period $[t_1, t_2]$ is called turn-on time of the MOSFET. During this time interval, the MOSFET consumes an energy ($E_{turn-on}$) as calculated in Equation 1.1. Since V_{in} and R are constant in the equation, the turn-on energy increases with t_{on}. Therefore, faster turn-on results in lower switching loss. During turn-off transition, the MOSFET also exhibits a similar switching loss that depends on t_{off}.

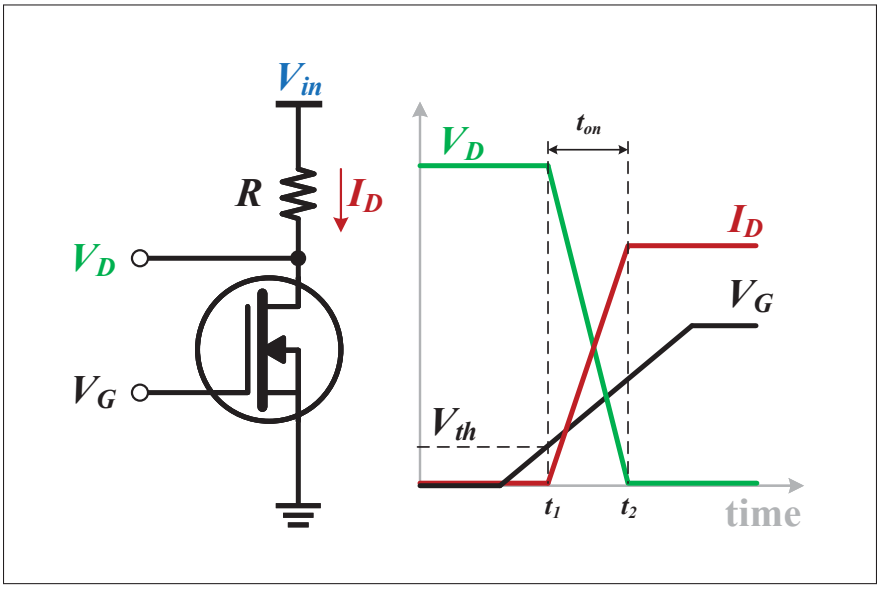


Figure 1.4 The turn-on of a MOSFET driving a resistor

$$
\begin{aligned}
E_{turn-on} &= \int_{t_1}^{t_2} V_d(t) \cdot I_d(t) \cdot dt \\
&= \frac{1}{6} \cdot V_{d(max)} \cdot I_{d(max)} \cdot (t_2 - t_1) \\
&= \frac{1}{6} \cdot \frac{V_{in}^2}{R} \cdot t_{on}
\end{aligned}
\tag{1.1}
$$

In order to control the ON and OFF interval of MOSFETs, a new class of circuit was born: Gate driver. A gate driver usually refers to a power amplifier that gets a signal from a controller (e.g. MCU or FPGA) and accordingly drives the gate of a power MOSFET, IGBT, SiC or GaN transistor.

1.4 Wide Bandgap Semiconductor

For over thirty years, innovations in power MOSFET technology and circuit topology have contributed to the improvement of power management efficiency and cost along with the increasing need for electrical power in human life. In the 21st century, the rate of improvement has slowed since the Si power MOSFET approaches its theoretical bounds. Hence, WBG power semiconductors have become gradually popular thanks to their superior characteristics versus Si counterparts.

Table 1.2 identifies the key electrical properties of three major semiconductor materials of the power electronics market.

Table 1.2 Comparison of material properties
Taken from Lidow *et al.* (2015)

Parameter		**Si**	**GaN**	**SiC**
Bandgap (E_g)	eV	1.12	3.39	3.26
Critical Field (E_{crit})	MV/cm	0.23	3.3	2.2
Electron Mobility (μ_n)	cm^2/V.s	1400	1500	950
Permittivity (ϵ_r)		11.8	9	9.7
Thermal Conductivity (λ)	W/cm.K	1.5	1.3	3.8

There are five key characteristics of a power device utilized in commercial power converters: conduction efficiency, switching efficiency, breakdown voltage, size and cost. The following sections will discuss the material characteristics and their relationship to the fore-mentioned power device characteristics in greater detail.

1.4.1 Bandgap (E_g)

The semiconductor bandgap refers to the chemical bonds strength between the atoms in the lattice. It is more difficult for an electron to jump from an energy level to another in wider bandgap materials. Therefore, higher bandgap devices exhibit lower leakage currents, higher operating temperatures.

1.4.2 Critical field (E_{crit})

Critical electric field is defined as the maximum field in one-sided junction at the onset of avalanche breakdown and is proportional to chemical bonds strength. Wider bandgap results in higher critical field and higher breakdown voltage (V_{BD}).

1.4.3 On-resistance (R_{on})

The theoretical area-specific R_{on} of a field-effect transistor can be calculated as follow (Lidow *et al.*, 2015):

$$R_{on} = \frac{4 \cdot V_{BD}^2}{\mu_n \cdot \epsilon_0 \cdot \epsilon_r \cdot E_{crit}^3} \quad [\Omega \cdot mm^2] \tag{1.2}$$

Where ϵ_0 is the permittivity of a vacuum measured in farads per meter ($8.854 \cdot 10^{-12}$ F/m). Equation 1.2 can be plotted for the ideal semiconductor materials in Figure 1.5 for Si, SiC and GaN. GaN appears to yield the lowest R_{on} which translates into lowest conduction loss in power converters.

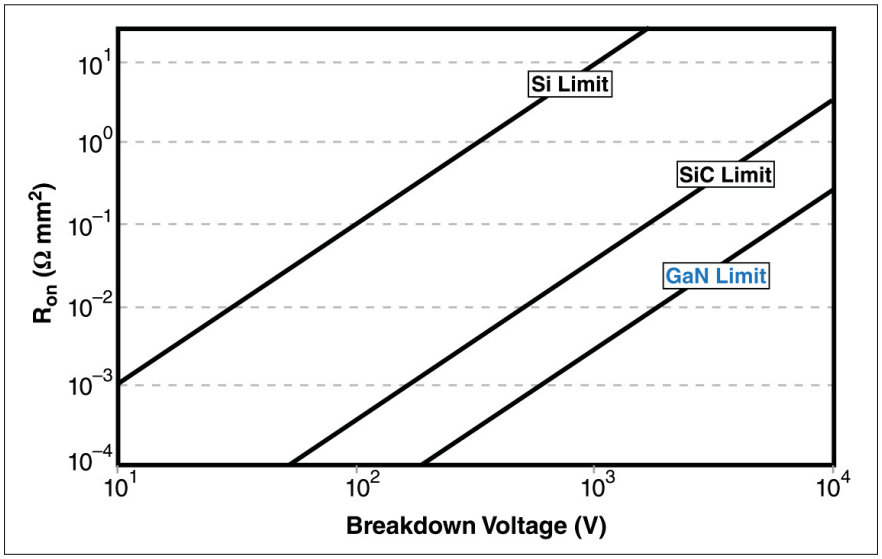


Figure 1.5 Theoretical R_{on} vs. V_{BD}
Taken from Lidow *et al.* (2015)

Real devices do not have ideal structures, so they lie on the top part of their material limit line. It took more than thirty years in case of Si MOSFETs for the development, improvement and diminution of the gap from their theoretical limit (Lidow *et al.*, 2015).

1.4.4 Commercial GaN HEMTs

There are two types of GaN HEMT: depletion-mode (d-mode) and enhancement-mode (e-mode). D-mode is normal-on and requires a negative V_{GS} to turn off. This requirement makes it ill-suited to DC/DC converters with the obvious risk of shoot-through current in half-bridges upon power up. In contrast, e-mode type is normally-off and has the same behaviour as n-channel MOSFETs, so this type is widely adopted. For this reason, e-mode GaN is in the scope of this thesis.

At the time this thesis is being written, there are many semiconductor companies showing their interest in GaN discrete components. Some of them have their products available on the market. The most emerging vendors are EPC, GaN systems, Infineon, Panasonic and VisIC. there are also various manufacturers doing research on GaN discrete device, such as HRL, Navitas, Exagan, Powdec, Sanken, etc.

Table 1.3 Commercial typical e-mode GaN discrete devices

Vendor	Part #	V_{DS-max}	I_{D-max}	R_{on-max}	Q_{G-typ}	$Q_{OSS-typ}$	Size mm
EPC	EPC2036	100 V	1.7 A	73 $m\Omega$	0.7 nC	3.9 nC	0.9×0.9
	EPC2052	100 V	8.2 A	13.5 $m\Omega$	3.6 nC	13 nC	1.5×1.5
	EPC2016C	100 V	18 A	16 $m\Omega$	3.4 nC	16 nC	2.1×1.6
	EPC2012C	200 V	5.0 A	100 $m\Omega$	1.0 nC	10 nC	1.7×0.9
	EPC2019	200 V	8.5 A	50 $m\Omega$	1.8 nC	18 nC	2.77×0.95
	EPC2010C	200 V	22 A	25 $m\Omega$	3.7 nC	40 nC	3.6×1.6
GaN systems	GS-065-004	650 V	3.5 A	500 $m\Omega$	0.7 nC	7.3 nC	5.0×6.0
	GS-065-011	650 V	11 A	150 $m\Omega$	2.0 nC	20 nC	5.0×6.0
Pana sonic	PGA26E34H	600 V	9.4 A	340 $m\Omega$	1.0 nC	8.5 nC	4.0×6.0
	PGA26E17B	600 V	15 A	175 $m\Omega$	2.0 nC	17 nC	8.0×8.0
Infineon	IGLD60R190	600 V	10 A	190 $m\Omega$	3.2 nC	16 nC	8.0×8.0
VisIC	V22N65A	650 V	80 A	22 $m\Omega$	41 nC	171 nC	18.6×15.6

Table 1.3 lists some GaN HEMTs that are available on the market. While most of the vendors make devices with the conventional package, Dual Flat No-lead (DFN), EPC and VisIC have their own unique footprint. VisIC parts support very high power whereas EPC ones favour lower power with higher density designs. Table 1.4 shows typical footprint options that are available on the market.

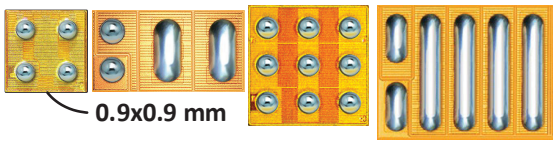
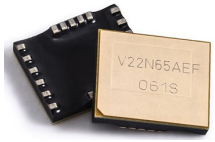
1.5 GaN Transistors - Attributes & Challenges

Although e-mode GaN HEMTs have characteristics similar to n-channel MOSFETs, there are unique features of GaN HEMTs that circuit designers should understand to best control these fast switching transistors. The characteristics and associated challenges are discussed in the this section, focusing on the half-bridge topology which is the most commonly used topology in power electronics.

1.5.1 Gate charge

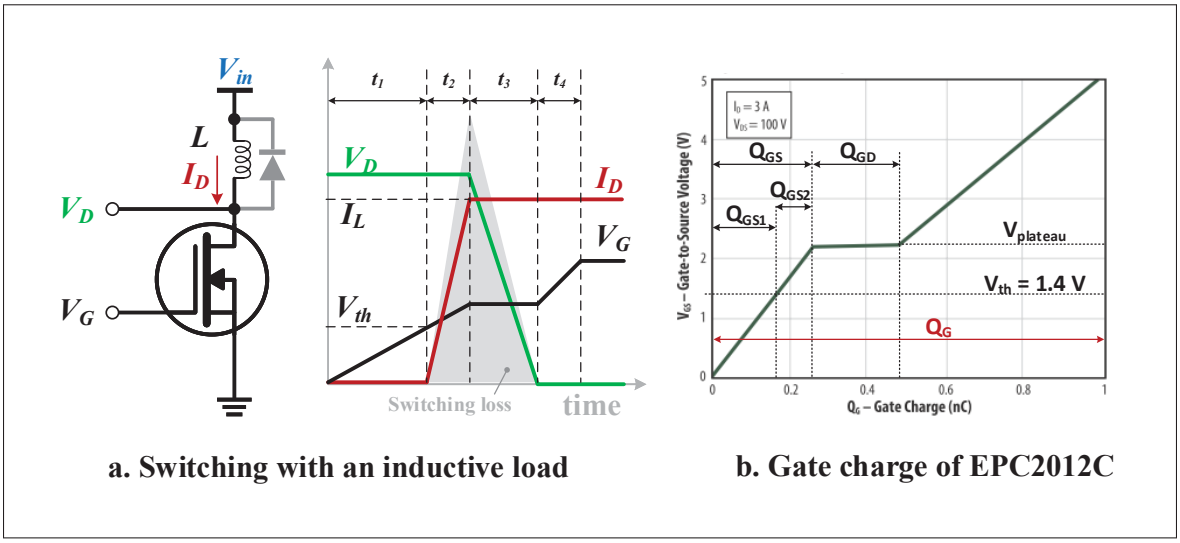
Like nMOS, the e-mode GaN HEMTs are controlled by injecting or removing a required amount of charge from the gate. Figure 1.6a demonstrates a turn-on switching of a GaN transistor with an inductive load. This turn-on process consists of four intervals: (t_1) the charge needed to raise

Table 1.4 Commercial typical e-mode GaN footprints

Vendor	Footprint	Figure
EPC	Bare-die	
GaN systems	DFN	 5.0x6.0 mm
Panasonic	DFN	 8.0x8.0 mm
Infineon	DFN	 8.0x8.0 mm
VisIC	Custom	 18.6x15.6 mm

the gate to V_{th}, (t_2) the charge required to complete the current rise time and for the gate to reach $V_{plateau}$, (t_3) the charge required to complete the voltage fall time, and (t_4) the charge required to bring the gate to the desired steady-state voltage. Figure 1.6b depicts EPC2012C gate charge curve with various components that are defined in Table 1.5. These gate charge components correspond to above four time intervals (t_1, t_2, t_3 and t_4).

With the same gate driving circuit, a FET with smaller gate charge should have faster switching time compared to the one with higher gate charge, which means lower switching loss.



a. Switching with an inductive load **b. Gate charge of EPC2012C**

Figure 1.6 An e-mode GaN FET driving an inductive load and different gate charge components of EPC2012C

Table 1.5 Gate charge components

Gate charge component	**Definition**
Q_{GS1}	Charge required to increase gate voltage from zero to V_{th} of the device.
Q_{GS2}	Charge required to commute the device current.
Q_{GS}	$Q_{GS1} + Q_{GS2}$
Q_{GD}	Charge required to commute the device voltage, at which point the device enters the linear region
Q_G	Total gate charge ($Q_G = Q_{GS} + Q_{GD}$).

One of the FOMs commonly used to compare MOSFETs is the product $R_{on}\times Q_G$, smaller being better. This FOM can also be used to compare Si and GaN technologies, as plotted in Figure 1.7. First-generation GaN devices have at least 3x better FOM for the same V_{DS} rating, which makes them switch much faster. This, however can translate into severe ringings at switching nodes with parasitics. Therefore, higher level (PCB or SiP) design should have optimized parasitics.

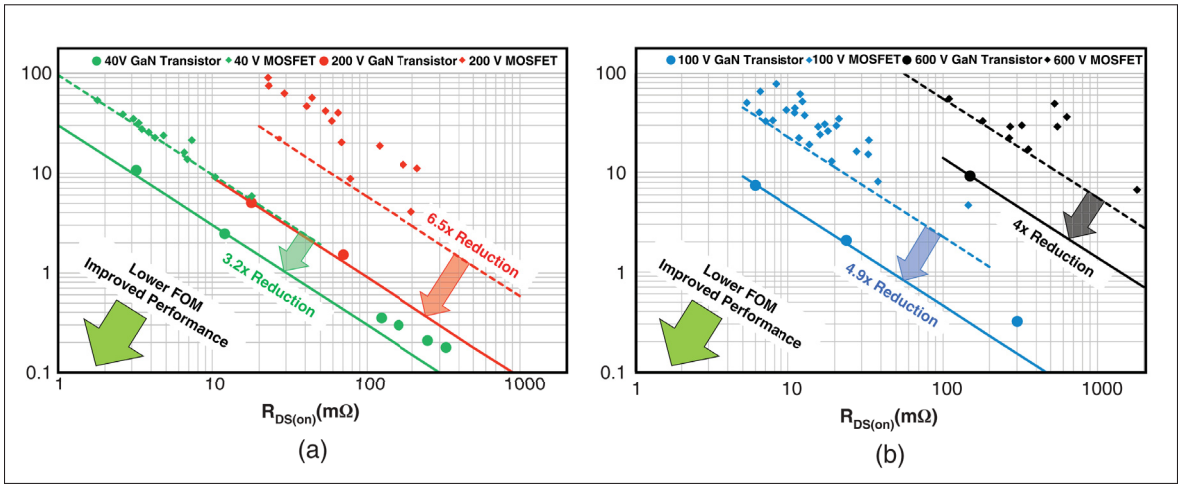


Figure 1.7 On-state resistance vs. total gate charge comparison for Si and GaN power devices showing (a) 40 V and 200 V, and (b) 100 V and 600 V devices
Taken from Lidow *et al.* (2015)

1.5.2 Gate drive voltage

Different technologies and different manufacturers have different maximum ratings. For e-mode GaN, such as the EPC2012C, the maximum V_{GS} is +6 V/-4 V. Exceeding this limit should be avoided, or the device will be damaged. For EPC2012C, the device R_{on} is specified in the datasheet at a recommended 5 V V_{GS} , which is 1 V below the absolute maximum rating. With very fast switching speed, care must be taken to prevent overshoot that may periodically bring V_{GS} above 6 V.

Figure 1.8 plots EPC2012C R_{on} across its V_{GS} at 3 A of drain current for the two temperature points: 25°C and 125°C. The rectangular dotted box in the figure marks the safe driving voltage range without significantly increasing its on-state resistance. This voltage range can be as low as 4 V. EPC also recommends keeping V_{GS-on} below 5.25 V to ensure a safe margin from 6 V. This requirement makes the gate driver design for GaN challenging due to tight V_{GS} tolerance in comparison with 6-10 V V_{GS-on} and ±20 V V_{GS-max} of Si power transistors.

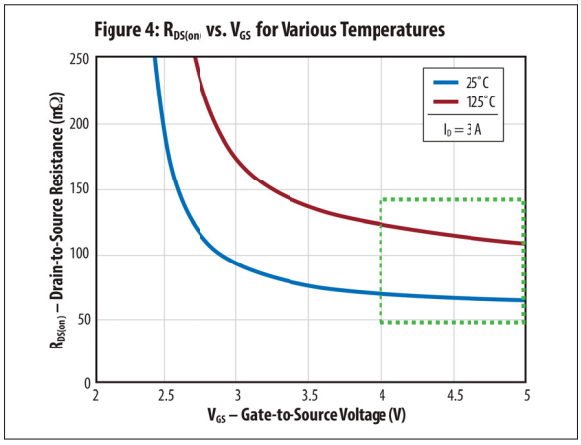


Figure 1.8 R_{on} vs. V_{GS} of EPC2012C taken from its datasheet

1.5.3 Reverse conduction

In a transistor's physical structure, its body diode provides a path whenever reverse current is needed. However, in a HEMT's physical structure, there is no such p-n junction. The mechanism of reverse conduction is completely different. The drain and source are symmetrical as depicted in Figure 1.9. When the GaN device is in off-state (shorted gate-source as shown in Figure 1.9b), if the gate-drain voltage is higher than V_{th}, it will conduct current from source (virtual drain) to drain (virtual source) in a diode-connected fashion. The reverse voltage, V_{SD}, in this situation is higher than V_{th}, ranging from 1 to 2 V. This value is about double the one of MOSFET body diode.

1.5.4 High-side driver supply

With half-bridge topology, the HS gate driver requires a floating supply. The simplest solution for this is using a bootstrap capacitor and a diode with a high reverse blocking voltage as illustrated in Figure 1.10. Decoupling capacitor C_{boot}, the bootstrap capacitor, acts as the energy storage for the HS logic circuitry supply.

At power-up, C_{boot} needs to be charged to V_{DD} value for the HS buffer to operate properly. This can only be done by turning on the LS GaN device to ground V_{SW}. The supply V_{DD} then charges

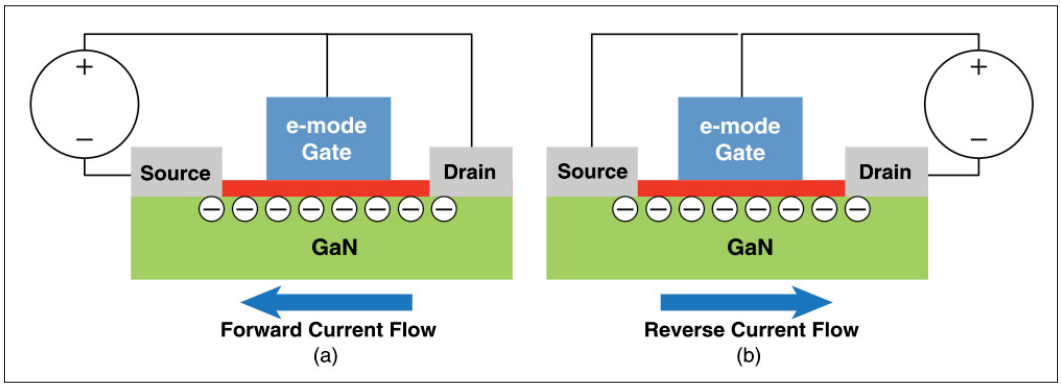


Figure 1.9 GaN reverse conduction
Taken from Lidow *et al.* (2015)

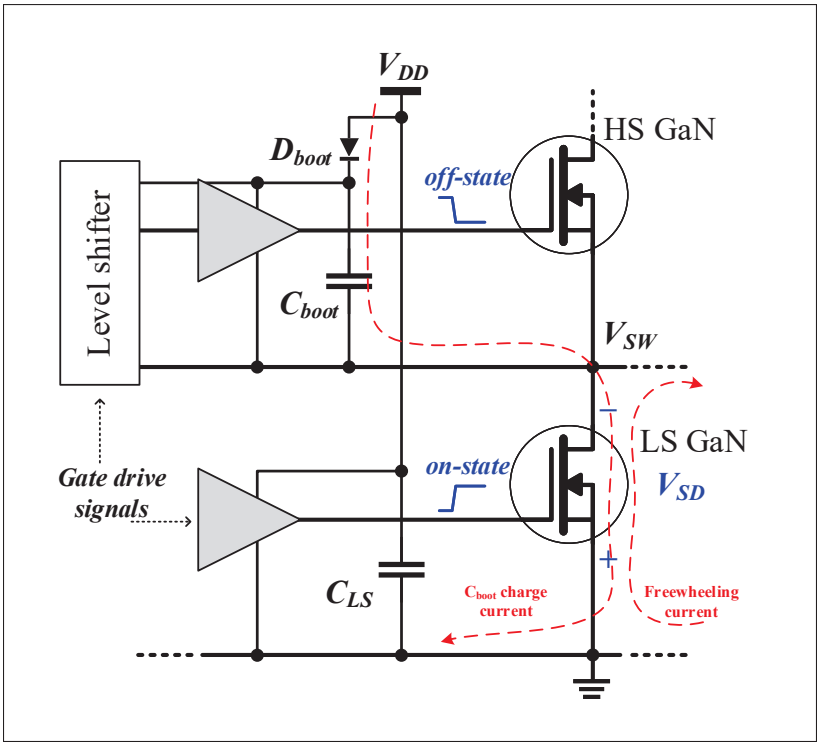


Figure 1.10 Bootstrap circuit in half-bridge gate driver

C_{boot} via D_{boot}. When HS buffer is turned on, C_{boot} is isolated from V_{DD} by D_{boot} and acts as the floating supply for the HS circuit.

Practically, C_{boot} is charged to V_{DD} minus the voltage drop across D_{boot}. This value is apparently lower than V_{DD}. However, when the half-bridge operates with a certain load current at the output, V_{SW} can swing negative during freewheeling current condition. The C_{boot}, in this situation, is charged up to V_{DD} minus forward voltage of D_{boot} and plus V_{SD}, the reverse conduction voltage of LS GaN device discussed in the previous section, which altogether could exceed 6 V. This overcharge issue can be avoided using the following common solutions:

1. Reduce dead-time resulting minimizing diode conduction time to nanoseconds range.
2. Reduce V_{SD} by adding an external Schottly diode across the LS GaN device.
3. Add a regulator (e.g. LDO) or a clamping circuit (e.g. Zener diode) after D_{boot}.
4. Replace bootstrap circuit with a charge pump, allowing the HS device to stay ON for a long time.

1.5.5 dV/dt immunity

A high voltage slew rate (dV/dt) on the drain of an off-state GaN device is a phenomenon worth investigating. Let's examine the circuit depicted in Figure 1.11 where the LS GaN is in off-state and the HS GaN starts to turn on. The high switching speed of the HS GaN results in a high dV/dt on the drain of LS GaN. This high voltage slew rate charges up all parasitics seen by this node to ground including C_{DS}, C_{GD} in series with a parallel circuit composed of C_{GS} and the turn-off path (R_G + L_{loop} + R_{pd}). The charge current though C_{GS} will result in a positive V_{GS} transient. If not well addressed, this induced V_{GS} could exceed V_{th} and accidentally turn on the LS GaN HEMT. This is known as the Miller turn-on effect and, if the duration is long enough, it may cause a catastrophic failure of the transistor and therefore must be prevented. The next chapter will discuss more about this as a criteria of the design.

1.5.6 Ground bounce

Ground bounce is a well-known phenomenon in power electronics, where parasitics inductance resonates with high dI/dt. As depicted in Figure 1.12a, L_S exhibits a high dI/dt switching and generates voltage spikes. The gate drive signal is then perturbed and could accidentally turn on

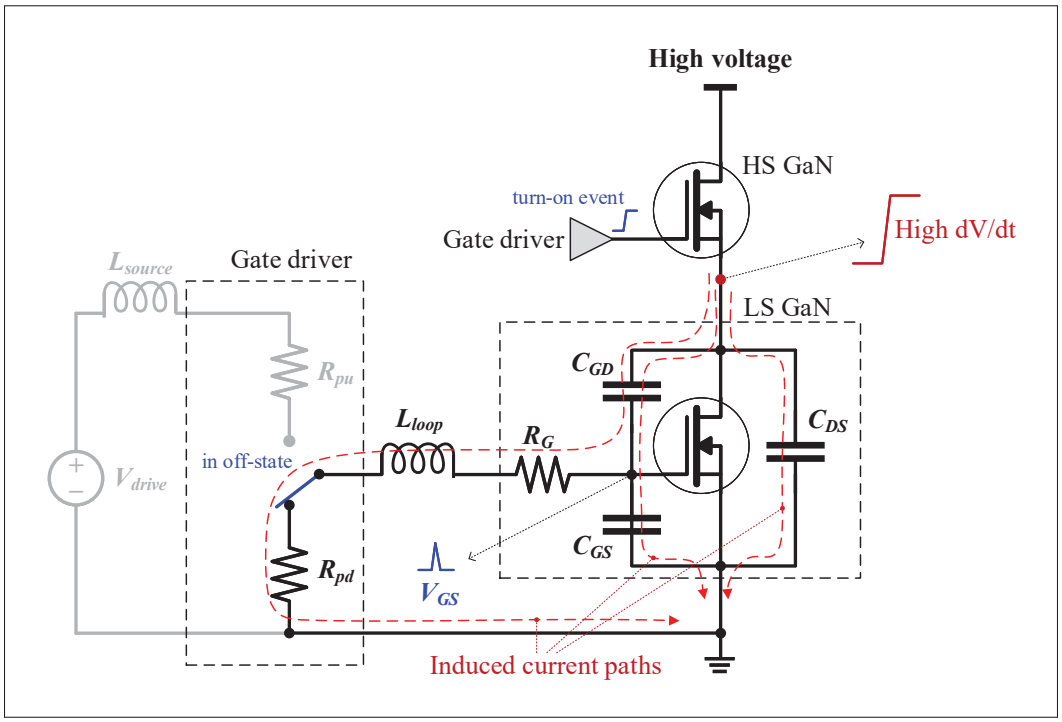


Figure 1.11 Miller turn-on effect of dV/dt on a low-side transistor in off-state

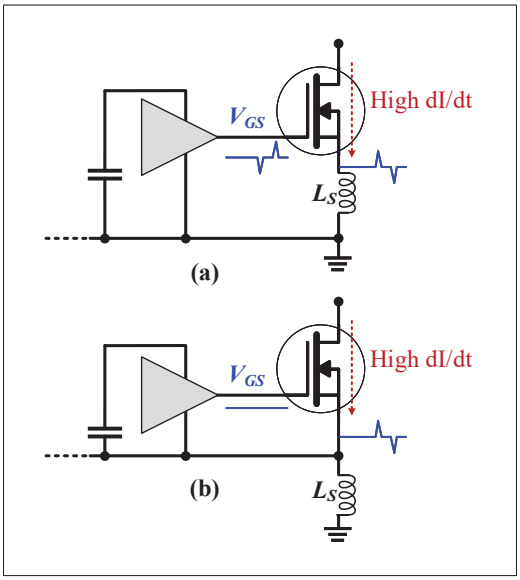


Figure 1.12 Common source inductance causing ground bounce.
(a) Gate drive impact and (b) simple solution for gate driver

or off the GaN device. One simple solution to this issue is to minimize the inductance within the loop comprising the Gate-Source terminals of the GaN device and the associated logic as in Figure 1.12b.

1.6 Conclusion

In this CPIO-SiP project, the power interface has to drive a load up to 1.25 A and withstand 84 V transients for hundreds of milliseconds. It must also survive under 150 V transients induced by lightning strikes (the voltage after being filtered) during its off-state. Therefore the GaN device candidates should have the following characteristics:

1. Favourable to high density integration in the context of SiP.
2. I_D > 1.25 A.
3. V_{DS} > 150 V.

The above requirements lead to the choice of EPC devices as the candidates of power switches used in CPIO-SiP. The SiP power stage is also scalable with the uniform SU of half-bridge. A light & low-voltage load can be driven by a buck converter with small GaN half-bridge while a current-controlled load with complex voltage profile can be supplied with a buck-boost stage. For this reason, a range of GaN device sizes are considered in this project.

With the background on the concept of gate driver, wide bandgap semiconductors and the challenges of driving GaN transistors, a review of state-of-the-art gate drivers will be given in the next chapter before entering into the detail of the proposed gate driver design.

CHAPTER 2

GATE DRIVER FOR GAN - STATE-OF-THE-ART

2.1 Introduction

This chapter presents a literature review of commercial and state-of-the-art gate drivers for GaN devices, especially in half-bridge topology. This review helps converge towards a versatile and reconfigurable architecture in the proposed gate driver.

2.2 Commercial Gate Driver for GaN

One of the key aspects of GaN power transistors is the capability of fast switching speed which copes with a minimum amount of parasitics. The ideal solution for power modules with GaN devices is monolithic integration of GaN switches, gate drivers and control ciruits on the same die. EPC and Navitas have commercialized e-mode GaN devices with built-in gate driver as detailed in Figure 2.1. However, these are with single power device or common source pair.

In the industry there are also commercial gate drivers for GaN device in half-bridge. Table 2.1 lists some of the typical parts.

Table 2.1 Typical commercial gate driver for GaN device in half-bridge

Vendor	Part Number	Description
Texas Instruments	LM5113	1.2/5 A, 100 V driver
Texas Instruments	LMG1210	1.5/3 A, 200 V driver with adjustable dead-time
Texas Instruments	LMG5200	80 V GaN half-bridge power stage
On Semi	NCP51820	-3.5 to +650 V, adjustable dead time, dual LDOs
uPI Semiconductor	uP1966A	0.4/0.7Ω pull-down/pull-up driver
Peregrine	PE29101	2/4 A, 80 V driver

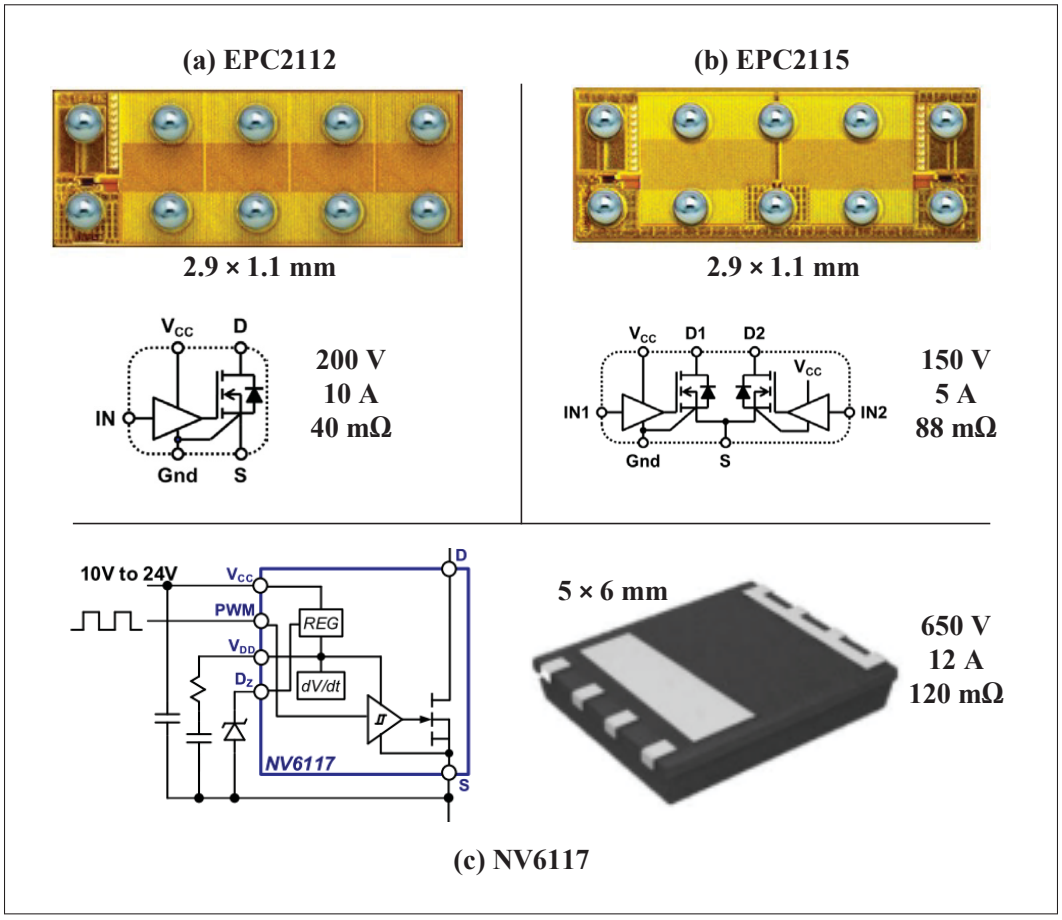


Figure 2.1 Integrated GaN device with gate driver from EPC and Navitas Semiconductor

2.3 Gate Driver for GaN in literature

To highlight the key elements in GaN gate drivers, Figure 2.2 shows the main building blocks in a gate driver for half-bridge topology, the most popular and commonly used converter topology (Delaine *et al.*, 2012; Song *et al.*, 2015).

As depicted, there are two output stages controlling the two GaN devices, high-side (HS) and low-side (LS). Each of them has an independent power supply. The ground of HS logic is tied to V_{SW}. To prevent large shoot-through current, a dead-time (DT) is usually inserted between the conduction time of HS and LS devices. The level shifter serves as the interface between LS logic and HS power domains.

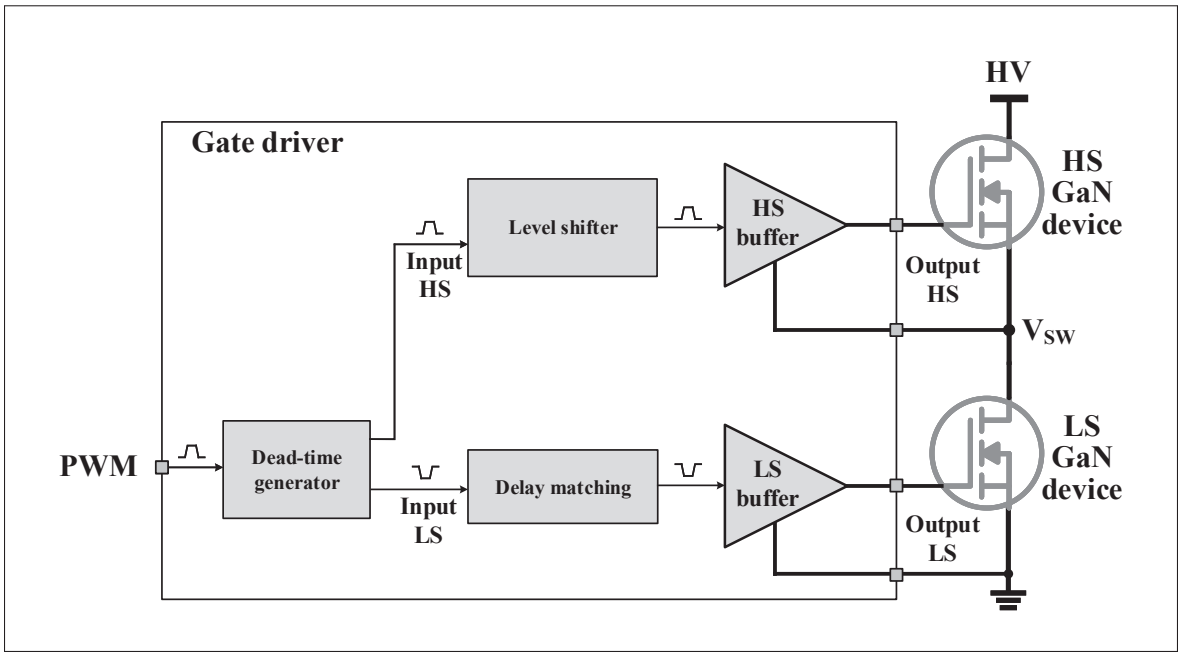


Figure 2.2 Half-bridge gate driver building blocks

In the literature, the majority of GaN power modules in half-bridge still opt for system-in-package, which integrates GaN power device with silicon gate driver on a surface-mount package (Luo *et al.*, 2014) or even PCB-level approaches. There are also works with discrete GaN devices in form of bare-die.

As power converter circuits are downsized, switching frequency increases to cope with miniature inductors and capacitors. At high f_{PWM}, timing mismatch between HS and LS becomes critical. Therefore, the performance bottleneck of high-speed gate drivers is the propagation delays of the level shifter and the DT generator. Such delays can be reduced with circuit techniques which leads to the classic power-speed compromise.

Conventional HV gate drivers often carry tens of ns of propagation delays in the level shifter, which becomes a critical problem as the f_{PWM} reaches the 10 MHz range. In (Kawai *et al.*, 2019), large delay of the level shifter and long DT in the driver limit its f_{PWM} to 1 MHz. To reduce the total delay, which is dominated by the HV level shifter, a sub-ns delay bootstrapped

gate driver with dynamic level shifter was reported (Song *et al.*, 2015). The speed gained at the cost of high power consumption that limits the peak power efficiency.

In a converter using half-bridge topology, the falling edge slope of V_{SW} is proportional to the output current (Roschatt *et al.*, 2016). A light load with a small DT leads to non-zero-switching of the GaN FETs whereas a heavy load with high DT results in reverse conduction in the GaN devices. Figure 2.3 illustrates the scenarios of optimal DT and two extremes. To overcome these challenges, digital control technique with generated adaptive DT is proposed. However, a high circuit complexity is involved (Wittmann *et al.*, 2016). A near-optimal DT control is reported (Lee *et al.*, 2011), however the long delay in sensing loop limits its use to low f_{PWM} applications. In (Ke *et al.*, 2016), a V_{SW} dual-edge DT modulator was designed, which senses load current and supply voltage and then generates modulated delays for V_{SW} rising and falling edges to adjust the instant DT, realizing zero-voltage switching for the GaN power switches. However, this method is too complicated for the CPIOS context of this project and the power consumption of the sub-ns comparator is high, leading to significant power loss.

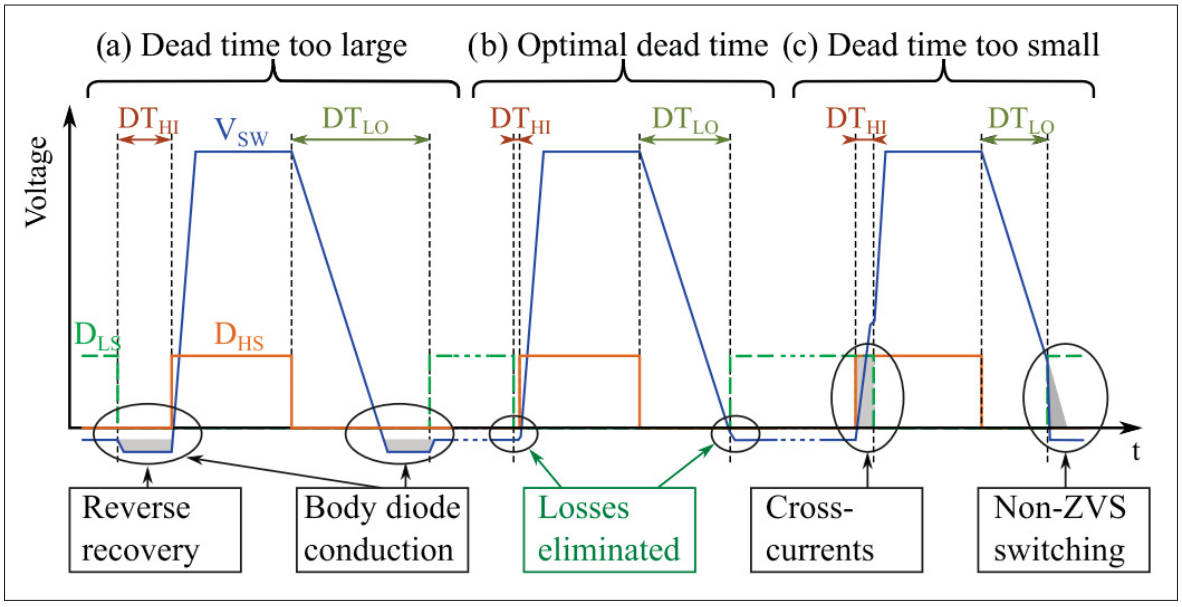


Figure 2.3 V_{SW} and dead-time
Taken from Wittmann *et al.* (2016)

Concerning the reliability, there have been some works addressing the bootstrap capacitor overcharge issue discussed in chapter 1. A Zener diode clamping technique was used to protect the bootstrap rail by sinking excessive charge to ground (Kawai *et al.*, 2019; Song *et al.*, 2015). However, this technique limits f_{PWM} as the power loss is proportional to the switching frequency. In (Ke *et al.*, 2016), an adaptive charging scheme called adaptive bootstrap balancing was proposed. To avoid overcharge, the charging time is initialized until the V_{SW} zero-crossing sensor determines that the charge voltage has enter the safe zone. This technique involves a high degree of circuit complexity. Another reliability issue is current collapse in the GaN devices. This phenomenon is due to hot electron injection and charge trapping, having been widely considered as one of the major causes of GaN device aging and premature failure (Bahl *et al.*, 2016). It degrades channel conductivity and increases R_{on} leading to higher junction temperature (T_J). As a consequence, the mean time to failure (MTTF) decreases exponentially (Paine *et al.*, 2019). To monitor the device aging, R_{on} drift is highly desirable as the early warning, because its change is directly related to current collapse effect. A similar approach was reported in (Smet *et al.*, 2011) using V_{CE} as the precursor for IGBTs. However, the monitoring can only be done when the system is off. An on-the-fly monitoring approach was reported (Dusmez *et al.*, 2016) by using pole variation in loop gain for power MOSFETs which correlates to the R_{on} variation. However, this technique is limited in continuous conduction mode (CCM) and the implementation of pole location is very sophisticated. Another indirect R_{on} measurement technique is realized through an I_{GSS}-inspired T_J sensor, based on the fact that gate-leakage I_{GSS} of a GaN device is both T_J-sensitive and aging-independent (Chen & Ma, 2019a). With sensed T_J, the in-situ condition monitor removes the impact of T_J on R_{on} through the T_J dependence remover effectively. This technique allows to take more proactive measures to slow down the aging process whenever possible (Chen & Ma, 2019a).

Electro-magnetic inteference (EMI) is one of the critical problems in highly reliable electronic devices, such as aircrafts. When power switches operate at high switching frequency, short switching cycles lead to high dI/dt and dV/dt rates that favours EMI emission. An LC filter can reduce EMI at the cost of size. Several techniques are reported to mitigate EMI. One of

them is frequency hopping using discrete frequencies in (Tao & Fayed, 2011), but this technique cannot spread the frequency spectrum evenly to lower the peak EMI. Another approach is with a series resistor, which is typically added at the gate of the GaN FET to damp the transitions (Song *et al.*, 2015; Ke *et al.*, 2016). However, the drawback is high switching loss. To overcome this, adjustable driving strength is proposed in (Rose *et al.*, 2010). Unfortunately, the sensing and driver delays are complicated and limit its use to low switching frequency applications.

Currently, spread-spectrum modulation (SSM) techniques are regarded as the most effective methods for EMI suppression (Amin & Choi, 2019). Periodic SSM (PSSM) is straightforward and easy to implement (Tse *et al.*, 2002). However, its EMI suppression is the least effective . Randomized SSM (RSSM) can outperform PSSM, with lower peak EMI and near-uniform noise spreading, but its performance highly relies on the random clock design. In (Yang *et al.*, 2018), an N-bit digital random clock was reported to achieve discrete RSSM (D-RSSM). However, the bit number N has to be large in order to achieve satisfying EMI attenuation, significantly increasing circuit complexity, chip area and power consumption. (Chen & Ma, 2019b) proposed a Markov chain based random clock to achieve analog f_{SW} modulation. It conducts SSM continuously and spreads spurious noise at f_{SW0} and its harmonics uniformly, achieving the desirable C-RSSM.

Closed-Loop EMI regulation is another promising approach. To best compromise between EMI and switching loss, it is important to accurately identify the Miller Plateau (MP) start point of V_{GS}. In (Chen *et al.*, 2017), a closed-loop adaptive MP sensing technique is presented. The technique utilizes the reverse conduction behavior of low-side switch to identify the MP starting point of the high-side device. This relaxes the design stress on the closed-loop propagation delay. Once the MP starting point is detected, the driving strength is modulated with an adaptive closed-loop control to achieve low dI/dt before the MP (for low EMI generation) and high dI/dt after the MP (to reduce the switching noise), leading to an optimum between noise and efficiency.

2.4 Conclusion

Driving GaN FETs is quite challenging. Multiple aspects have been studied and addressed in the literature: driving for performance, for reliability and for EMI reduction. Every approach was elaborate and aimed at a specific improvement. There has been no universal and versatile gate driver. The universal and configurable gate driver for GaN half-bridges in the context of SiP is proposed in this work. It can control a range of GaN devices (1–5.3 nC gate charge) with configurable speeds and DT without extra components. The adjustable parameters make local efficiency optimization possible. This gate driver, as a standalone chip, can also serve as a platform for other works that need on-the-fly configuration of drive strength and DT.

CHAPTER 3

DESIGN OF THE GATE DRIVER

3.1 Introduction

This chapter outlines the gate driver design, starting with system requirements and the choice of technology. The internal blocks will then be discussed and simulated. Some blocks require special layout techniques which will also be detailed. Various post-layout simulations are performed to ensure the functionality of the chip.

3.2 System Requirements

Intended to be the core design of the CPIOS for aerospace applications, the gate driver in this work is capable of driving GaN devices of various sizes, in half-bridge configuration, with configurable driving strength and dead-time. The half-bridges, so-called switching unit, can be configured to operate in buck, boost or buck-boost topology. Figure 3.1 summarizes the context of this work.

An SiP design, as shown in Figure 3.1c, has some basic requirements. First, the constrained space demands a limited number of discrete parts and imposes the use of proper GaN devices size per output specification. A large transistor driving a light load is a waste of space. Second, the overall cost increases with the number of custom designed ICs used in the SiP. A gate driver variant per GaN size is a burden for both design and cost. Hence, a single universal gate driver is desired, as depicted in Figure 3.2, without the need for external resistors. Third, a flexible and digitally configurable design is required in safety-critical transportation applications. Such a gate driver can be used in multiple versions of the SiP, each having different specifications in terms of protection thresholds (e.g. over-temperature threshold). Last, the gate driver supports not only configuration writing, but also status reading that is essential for self-calibration and trimming at system level. There are also sensors integrated in the gate driver: temperature sensors for thermal shutdown (TSD) circuits, voltage sensors and comparators for under-voltage

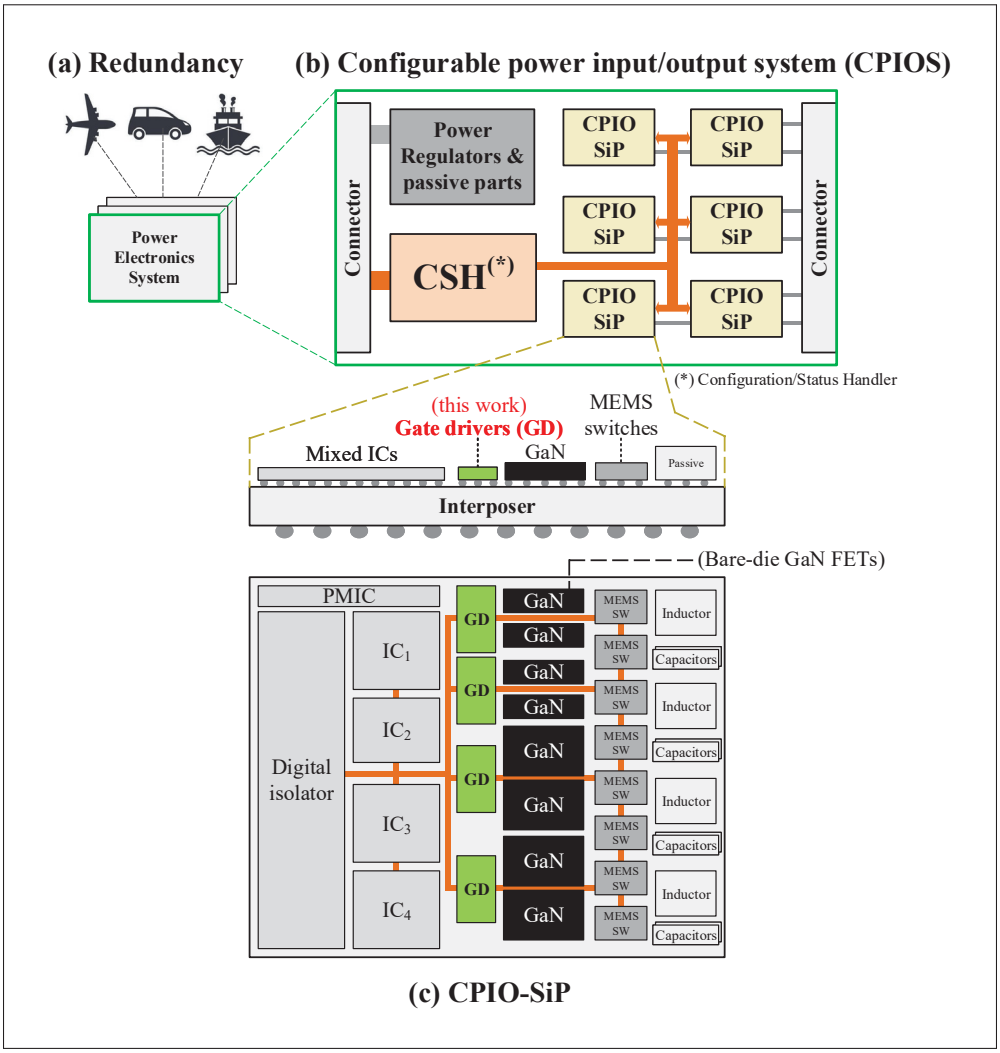


Figure 3.1 CPIOS context of the gate driver

lock-out (UVLO) blocks, and current sensors for a variety of protection blocks. These sensors compare their sensed electrical or physical record to a threshold, to let the system make an appropriate decision (e.g. when the chip temperature exceeds 100°C, shutting down the outputs). Depending on the level of criticality, the decision can be either direct hardware interception or via software from the top-level processor unit. In automotive applications, different circuits located at different places of the vehicle usually have different thresholds. The devices near the main engine or turbine operate at higher temperature than those placed in other locations. For this reason, a configurable threshold is a key point to make the gate driver universal.

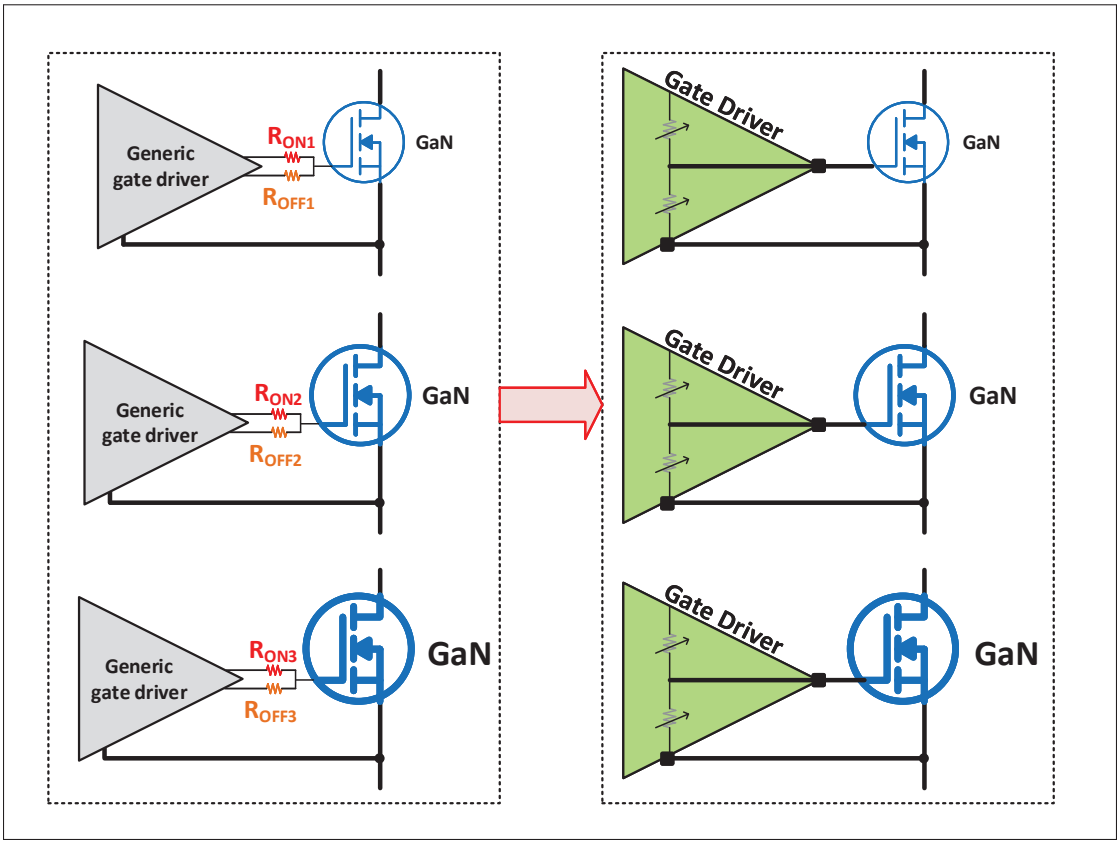


Figure 3.2 Configurable gate driver compatible with different GaN FET sizes

The stability and parameter drift over time of electronic components, such as sensors, which are used in critical sub-systems in aerospace applications and operate in harsh environments has been intensively studied (Marin *et al.*, 2018). In addition, any integrated circuit is subject to manufacturing process variation that makes its performance different from simulation results. The possibility of performance trimming after fabrication, and calibration before each operation or even in-flight (Capobianco *et al.*, 2019) is thus of great interest in aerospace applications.

Table 3.1 summarizes the electrical specs of the power interfaces of the CPIO-SiP.

Table 3.1 CPIO-SiP power interfaces electrical specifications

V_{in}	V_{out}	I_{out}
14 - 84 V	$\leq$ 32 V	50 mA - 1.25 A

V_{out} of some interface types can reach 150 V in off-state upon lightning strike. The interface types vary from as simple as a 24 V on/off logic circuits to as sophisticated as a buck-boost converter. The GaN device size will be chosen based on the output current rating per interface. The targeted GaN FETs are listed in Table 3.2. To be universal, the gate driver is chosen to be capable of driving half-bridge topology.

Table 3.2 Targeted GaN FETs driven by the gate driver

Part no.	I_{D-dc}	V_{DS}	R_{on}	Q_G	Q_{GS}	Q_{GD}	Q_{OSS}	**Size [mm]**
EPC2012C	5 A	200 V	100 mΩ	1 nC	0.3 nC	0.2 nC	10 nC	1.7×0.9
EPC2007C	6 A	100 V	30 mΩ	1.6 nC	0.6 nC	0.3 nC	8.3 nC	1.7×1.1
EPC2052	8.2 A	100 V	13.5 mΩ	3.6 nC	1.5 nC	0.5 nC	13 nC	1.5×1.5
EPC2019	8.5 A	200 V	50 mΩ	1.8 nC	0.6 nC	0.35 nC	18 nC	2.77×0.95
EPC2016C	18 A	100 V	16 mΩ	3.4 nC	1.1 nC	0.55 nC	16 nC	2.1×1.6
EPC2010C	22 A	200 V	25 mΩ	3.7 nC	1.3 nC	0.7 nC	40 nC	3.6×1.6

Figure 3.3 and Table 3.3 summarize the specifications of the the proposed gate driver. The typical driving voltage is 5 V which is ideal for the chosen GaN FETs. The two buffers, with adjustable drive strength, are able to control the GaN FETs with desired speeds. The dead-time is also configurable. The design in detail will be discussed in the following sections.

Table 3.3 Proposed Gate driver specifications

Parameter	**Min**	**Typ**	**Max**	**Unit**	**Note**
IC supply voltage	4.75	5	5.25	V	
V_{SW} to GND	-3		200	V	
Drive strength (source)	100		1,500	mA	Configurable, step 100
Drive strength (sink)	200		3,000	mA	Configurable, step 200
Dead-time	5		80	ns	Configurable, step 5
dV_{SW}/dt immunity			100	V/ns	

3.3 Technology Options

One of the critical specifications that narrows down the choice of technology is system survival at 150 V in off-state. Table 3.4 summarizes the key >150V technologies available. GlobalFoundries does not offer multi-wafer project to universities at the time of the project being planned whilst

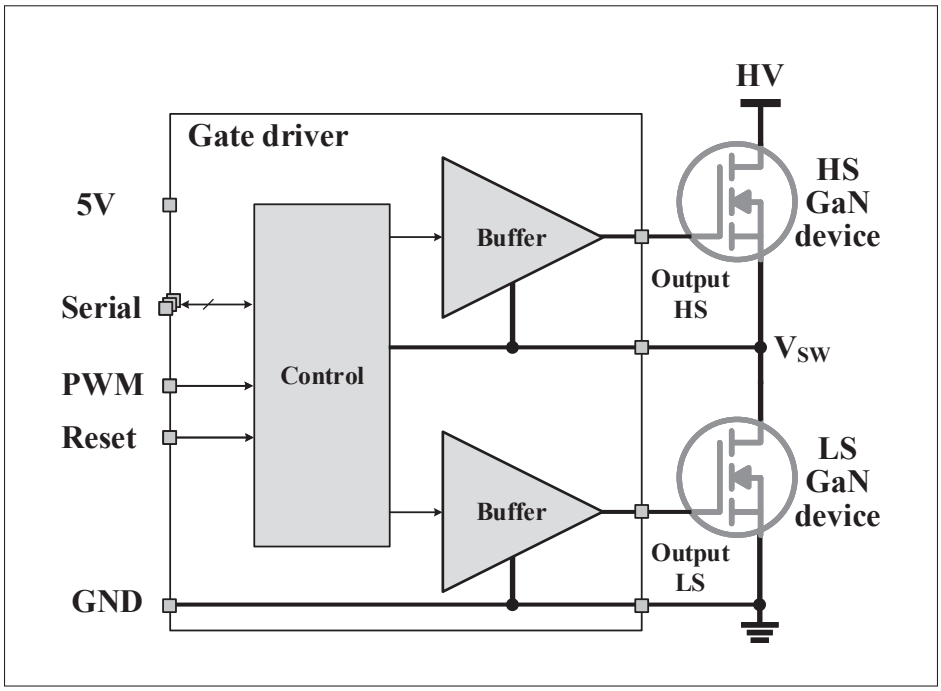


Figure 3.3 Proposed gate driver

XFAB does. XU035 is not SOI, which means multiple power domain monolithic design is not feasible. The two left options are SOI: 0.18μm and 1.0μm. The digital circuits in XDH10 1.0μm are not as fast as the much smaller node, XT018 0.18μm. For these reasons, XT018 is selected to realize the gate driver.

Table 3.4 High voltage technologies

Foundry	Tech name	Max voltage	Temperature
XFAB	XT018 0.18μm SOI-CMOS	200 V	-40 ~ 175°C
XFAB	XU035 0.35μm CMOS	700 V	-40 ~ 125°C
XFAB	XDH10 1.0μm SOI-CMOS	650 V	(not specified)
GlobalFoundries	180UHV 0.18μm SOI-CMOS	700 V	-40 ~ 150°C

3.4 Block Circuit Design

Ideally, the configurable gate driver should consist of the blocks listed below, which are also illustrated in Figure 3.4:

1. Dead-time (DT) generator.
2. Level-shifter for high-side (HS).
3. Delay matching for low-side (LS).
4. Output buffer stage.
5. Configuration handler.
6. 5V floating supply for HS.
7. Power-on reset (POR).
8. Under-voltage lockout (UVLO).
9. Thermal shutdown (TSD).

To simplify the verification of the reconfigurability pf the very first chip in CPIOS project, the floating supply, POR/UVLO and TSD are not included in the design presented in this work.

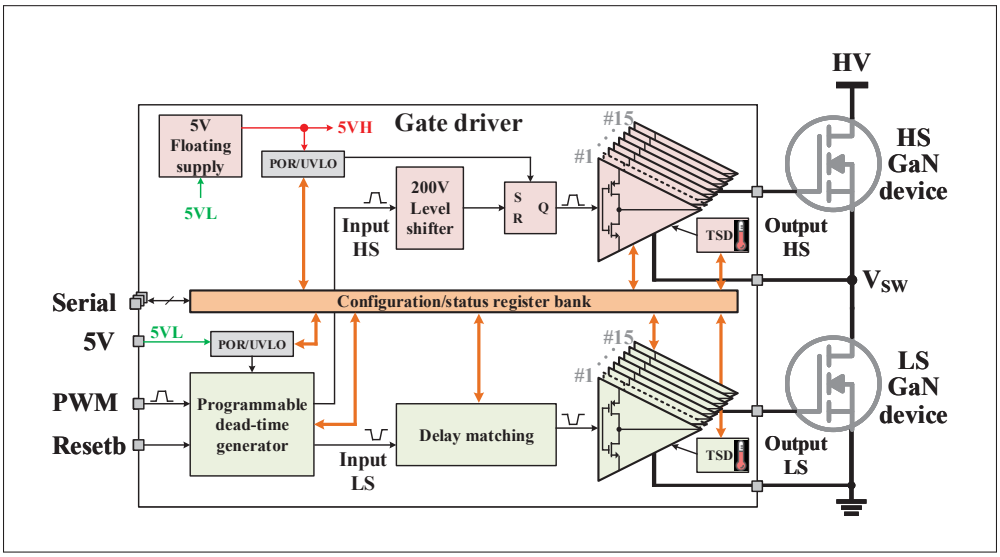


Figure 3.4 Half-bridge GaN gate driver block diagram

The following sections will discuss the design in greater detail.

3.4.1 Output Driver Stage

The output buffers are designed to have independent turn-on and turn-off speed. The speeds are digitally configurable.

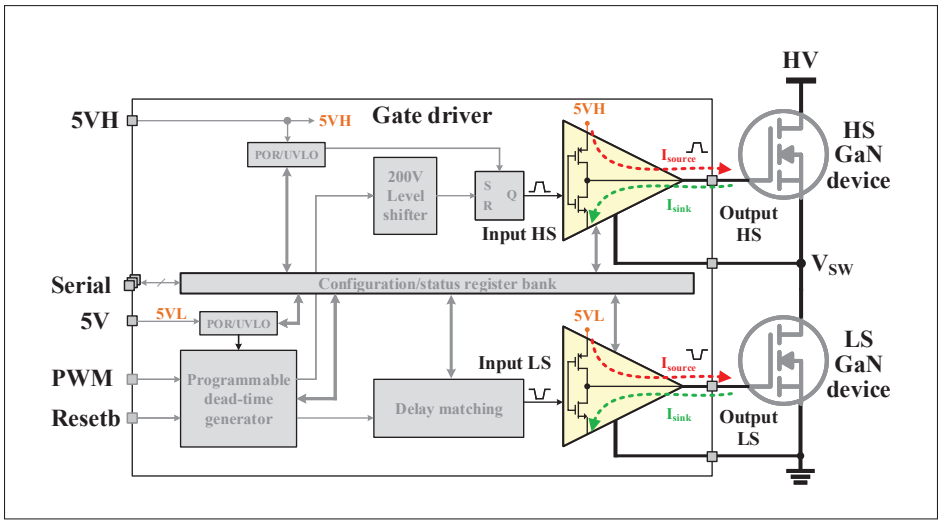


Figure 3.5 Output driver stage of the gate driver

Before going into the design, let's examine a simple gate driving circuit in Figure 3.6.

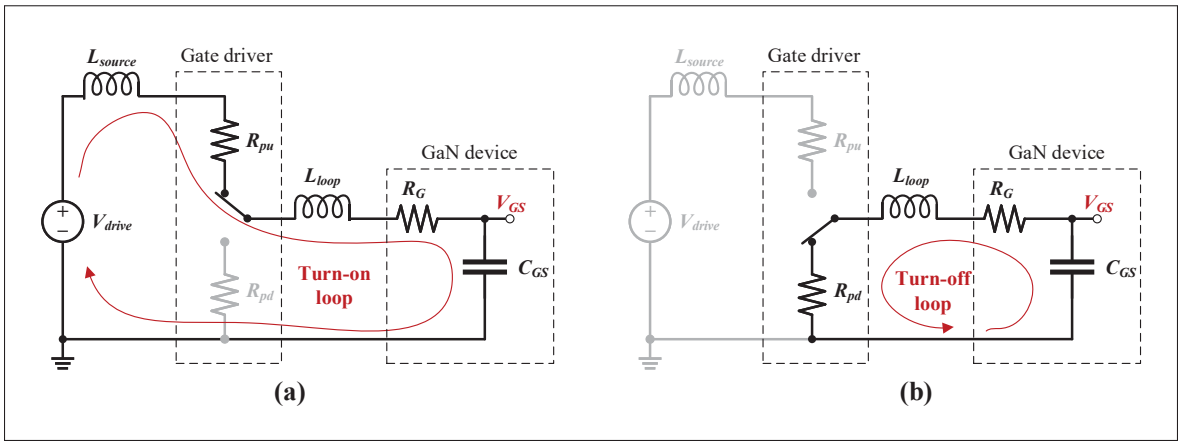


Figure 3.6 Gate drive circuit with independent (a) turn-on and (b) turn-off path

The gate driver has an equivalent pull-up resistor R_{pu} and pull-down one R_{pd}. L_{source} represents the stray inductance of power distribution network to the gate driver. L_{loop} is the equivalent

inductance in the gate driving loop from the driver to the GaN device. It is noticed that L_{source} is present only in the turn-on path and not in the turn-off one. R_G is the parasitic resistance from the GaN package pin to its intrinsic gate and C_{GS} represents its gate-source capacitance. In both turn-on and -off scenarios, the equivalent circuit is an RLC-series resonant tank with the equivalent components specified in Table 3.5. With EPC GaN devies, R_G is very small (around 0.4 Ω) and is negligible since the totality of other resistance components is in the order of Ohms.

Table 3.5 Equivalent components of RLC tank for turn-on and turn-off path

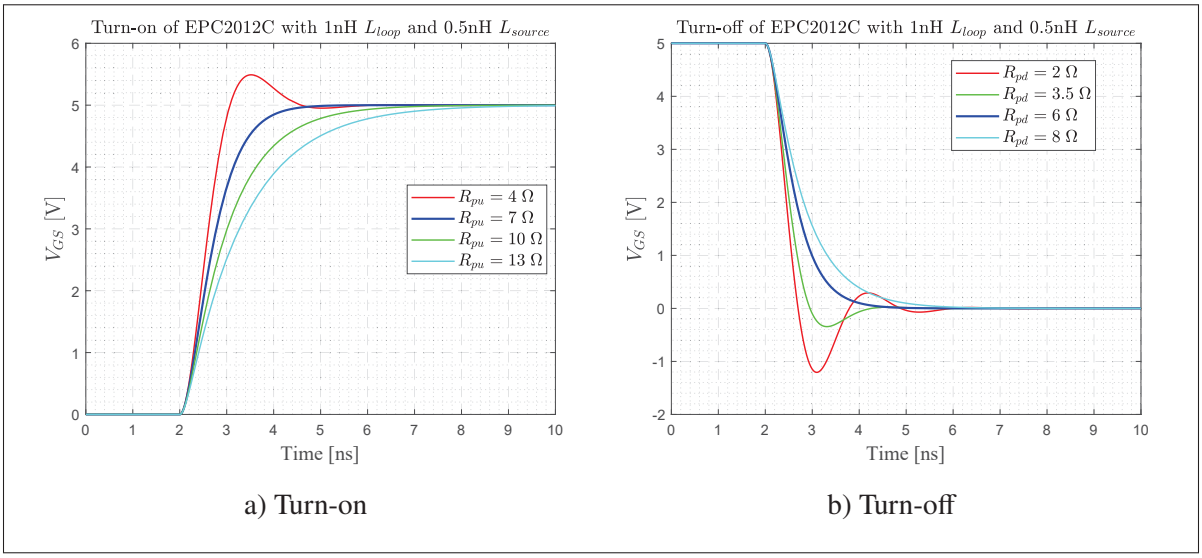
RLC component	**Turn-on path**	**Turn-off path**
R_{eq}	$R_{pu} + R_G \approx R_{pu}$	$R_{pd} + R_G \approx R_{pd}$
L_{eq}	$L_{source} + L_{loop}$	L_{loop}
C_{eq}	C_{GS}	C_{GS}

If R_{eq} is too small, the circuit is underdamped and exhibits overshoot/undershoot. In contrast, if R_{eq} is too large, the tank is overdamped and V_{GS} has slow rise- and fall-time. Therefore, the R_{eq} should be chosen so that both scenarios have near-critical damping factors. In an RLC-series resonant circuit, R_{eq} needed for the critical damp can be calculated as in Equation 3.1 and will be simulated later.

$$R_{eq(crit)} = 2 \cdot \sqrt{\frac{L_{eq}}{C_{eq}}} = \begin{cases} \frac{L_{source}+L_{loop}}{C_{GS}} \approx R_{pu(crit)} & \text{for turn-on path,} \\ \\ \frac{L_{loop}}{C_{GS}} \approx R_{pd(crit)} & \text{for turn-off path.} \end{cases} \tag{3.1}$$

From Equation 3.1, the chosen value for $R_{pu(crit)}$ is larger than $R_{pd(crit)}$ value because of the presence of L_{source}. In other words, drive strength of the turn-on path should be weaker than that of the turn-off path in general. Figure 3.7 shows the simulation results of turn-on and turn-off waveform of EPC2012C ($C_{GS} = 100pF$) at 1 nH and 0.5 nH of L_{loop} and L_{source} respectively, with different R_{pu} and R_{pd} values.

The critical damp occurs at $R_{pu} = 7\ \Omega$ and $R_{pd} = 6\ \Omega$. However, in reality the R_{pd} is chosen to be smaller than its critical damp value to further mitigate the false turn-on of Miller effect as



a) Turn-on b) Turn-off

Figure 3.7 Switching EPC2012C at (a) turn-on and (b) turn-off

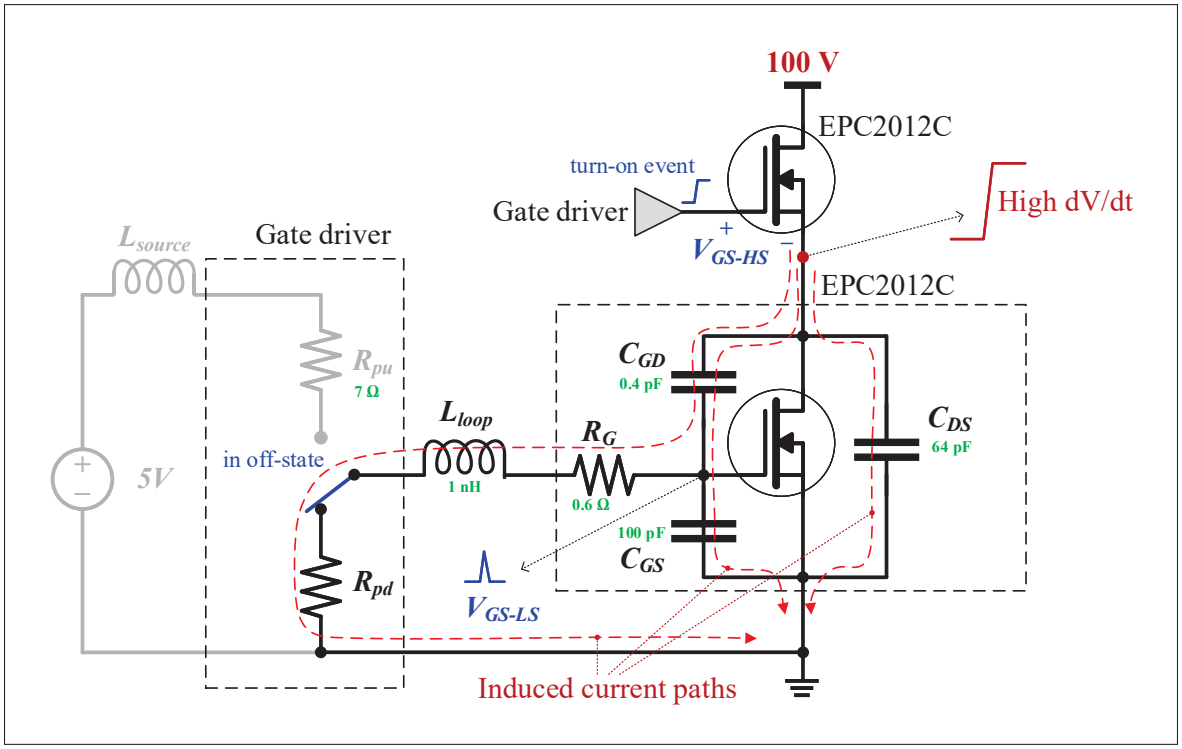


Figure 3.8 Miller effect on low-side GaN during off-state

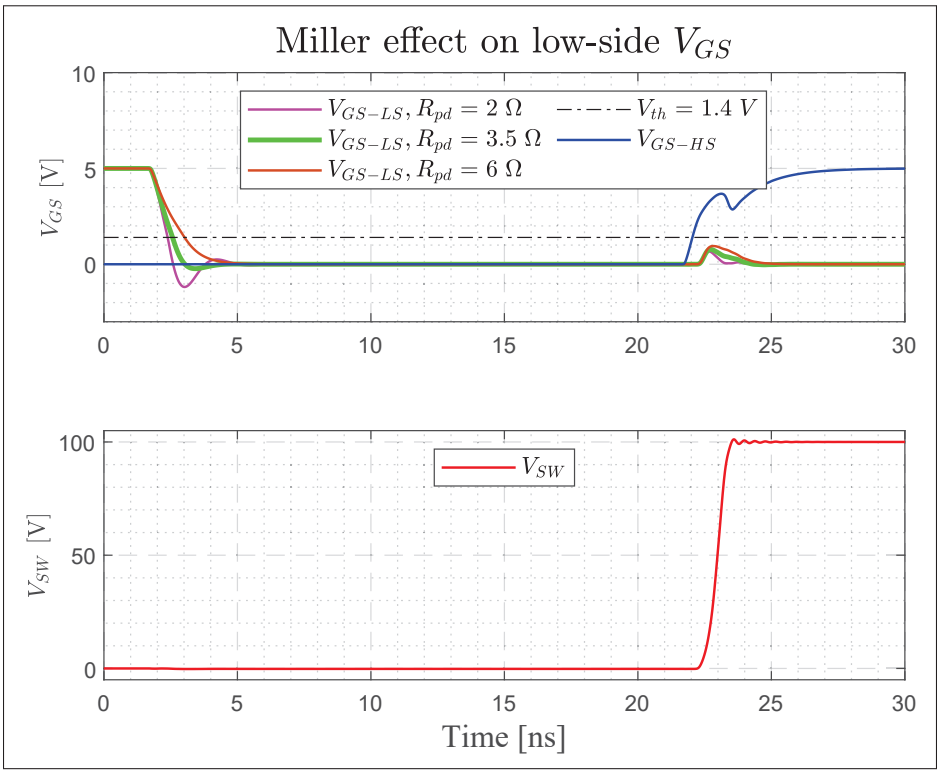
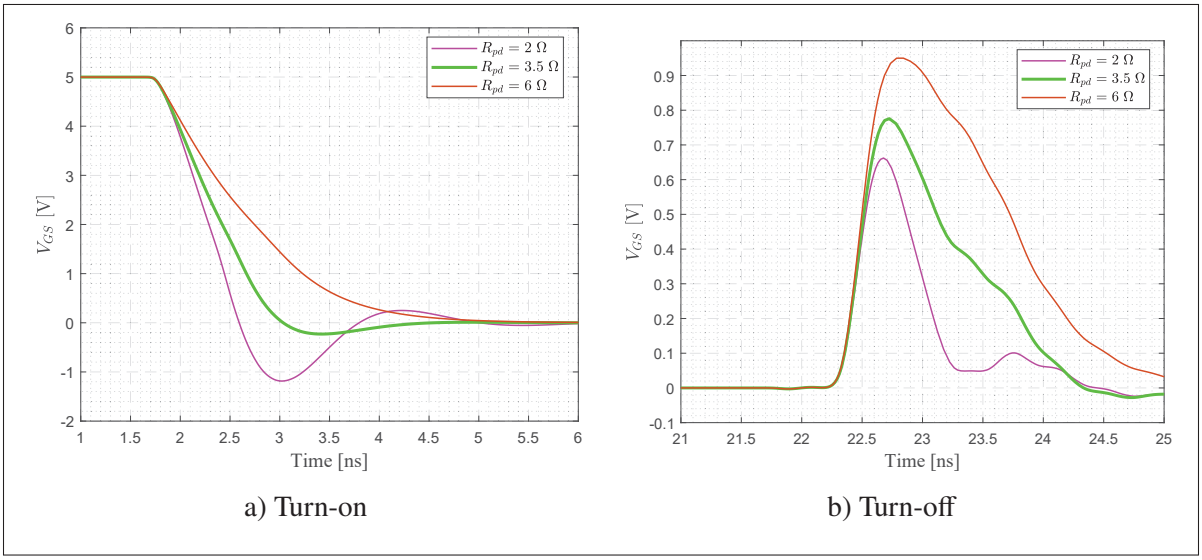


Figure 3.9 Simulated waveforms under Miller effect



a) Turn-on b) Turn-off

Figure 3.10 Zoomed waveforms of V_{GS-LS} in Figure 3.9

discussed in section 1.3. With smaller R_{pd} (e.g. 3.5 Ω), some amount of undershoot is present for the turn-off (-0.4 V) but the margin from its -4 V limit is safe enough. There is always a compromise between the margin from negative V_{GS} breakdown and the degree of Miller turn-on effect. A simulation of this compromise (demonstrated in Figure 3.8) is shown in Figures 3.9 and 3.10. One can see that 3.5 Ω R_{pd} gives the best compromise between the undershoot and the Miller turn-on effect, i.e. half of the R_{pu} (7 Ω). In other words, the pull-down drive strength is twice as strong as the pull-up one in general.

The output stage is realized with pMOS and nMOS as pull-up and pull-down networks. To size the integrated MOS transistors of this output stage, gate charge (Q_G) of the GaN FETs and the desired rise and fall times are taken into account. The initial criteria is that the rise time of V_{GS} of the targeted GaN devices should be less than 10 ns. This rise time (t_r) requirement helps determine source current (I_{source}) capability of the pMOS network. Equation 3.2 shows the relationship between Q_G, I_{source} and t_r with the first order model of gate charge illustrated in Figure 3.11.

$$I_{source} = \frac{Q_G}{t_{charge}} = 0.8 \cdot \frac{Q_G}{t_r} \tag{3.2}$$

Table 3.6 gives an overview of source current needed for various rise time values across the range of GaN FETs. The I_{source} range is chosen to be 0.1 A to 1.5 A with the step of 0.1 A. This range will ensure the switching speed of small GaN devices as fast as 1 ns and larger FETs up to 2 ns. The current sink capability is chosen to be twice the source one.

Table 3.6 Source current requirement across rise times and GaN FETs

Part no.	Q_G	$I_{t_r=1ns}$	$I_{t_r=2ns}$	$I_{t_r=3ns}$	$I_{t_r=4ns}$	$I_{t_r=10ns}$
EPC2012C	1 nC	0.8 A	0.4 A	0.27 A	0.2 A	0.08 A
EPC2007C	1.6 nC	1.28 A	0.64 A	0.43 A	0.32 A	0.13 A
EPC2019	1.8 nC	1.44 A	0.72 A	0.48 A	0.32 A	0.14 A
EPC2016C	3.4 nC	2.72 A	1.36 A	0.91 A	0.68 A	0.27 A
EPC2052	3.6 nC	2.88 A	1.44 A	0.96 A	0.72 A	0.29 A
EPC2010C	3.7 nC	2.96 A	1.48 A	0.99 A	0.74 A	0.3 A

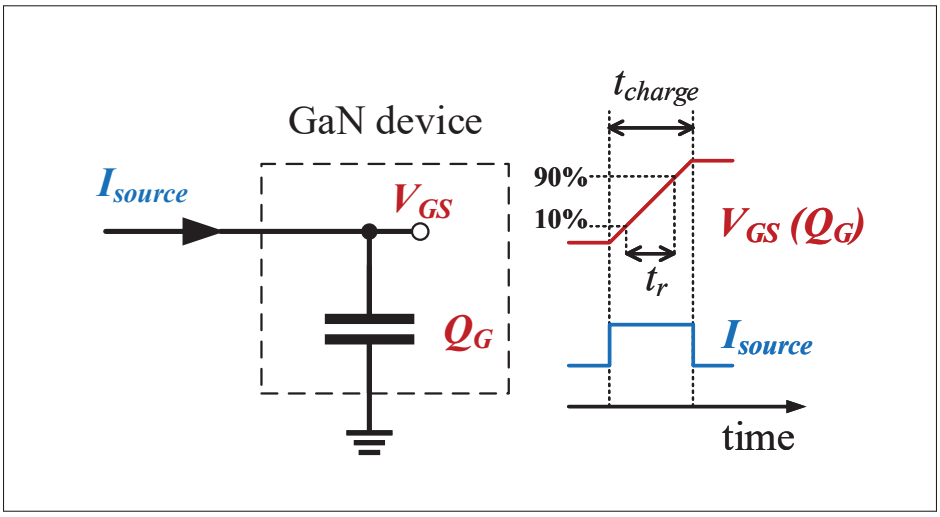


Figure 3.11 Gate charge, rise time and source current relationship

Figure 3.12 depicts the design of the output buffer. There are 15 parallel instances of 100/200 mA of source/sink cell. The source (pull-up) and sink (pull-down) networks are implemented using pMOS (MP1) and nMOS (MN1). All instances are in parallel and independently activated. The source and sink networks within each instance are also independent enabled/disabled via EN_PU[i] and EN_PD[i] bits. A built-in non-overlapping logic control per instance is meant to avoid simultaneous turn-on of MP1 and MN1.

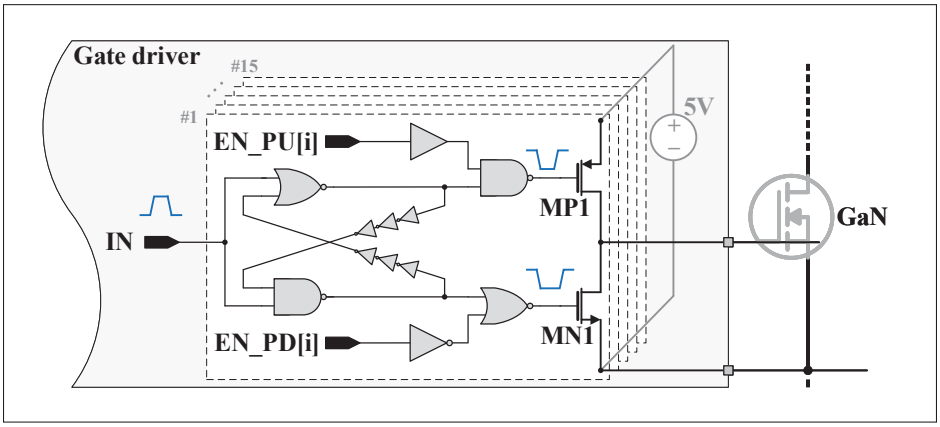


Figure 3.12 Output stage of the gate driver

The primitive devices in XFAB XT018 in use for MP1 and MN1 are pe5 and ne5 whose DC characteristics curves are shown in Figure 3.13 with the width of 10 μm and the minimum length of 0.5 μm. To support the source and sink capability of 100/200 mA, the pe5 and ne5 are upsized accordingly. Table 3.7 shows the chosen sizes of ne5 and pe5 with the desired current values of 100/200 mA.

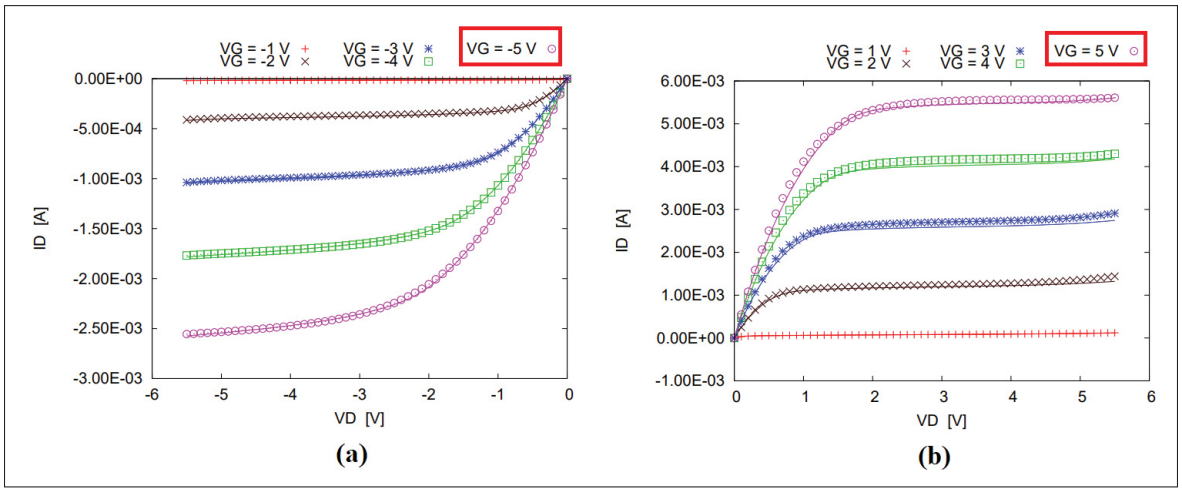


Figure 3.13 Characteristics curves of (a) pe5 and (b) ne5 at W/L = 10/0.5 um in XFAB XT018

Table 3.7 Chosen MP1 and MN1 sizes

pe5		**ne5**	
W/L [μm]	**Isource [mA]**	**W/L [μm]**	**Isink [mA]**
10/0.5	2.75	10/0.5	5.3
363.6/0.5	100	377.4/0.5	200

Table 3.8 shows the truth table of the drive strength control (PullUp and PullDown buses) and the output source/sink current. The source and sink parameter configurations are independent.

Figure 3.14 shows the simulation result of the buffer stage driving EPC2012C with all 15 different drive strength levels.

Table 3.8 Drive strength configuration data

PullUp[3:0] bin	Source current [A]	PullDown[3:0] bin	Sink current [A]
0000	Off	0000	Off
0001	0.1	0001	0.2
0010	0.2	0010	0.4
0011	0.3	0011	0.6
0100	0.4	0100	0.8
0101	0.5	0101	1.0
0110	0.6	0110	1.2
0111	0.7	0111	1.4
1000	0.8	1000	1.6
1001	0.9	1001	1.8
1010	1.0	1010	2.0
1011	1.1	1011	2.2
1100	1.2	1100	2.4
1101	1.3	1101	2.6
1110	1.4	1110	2.8
1111	1.5	1111	3.0

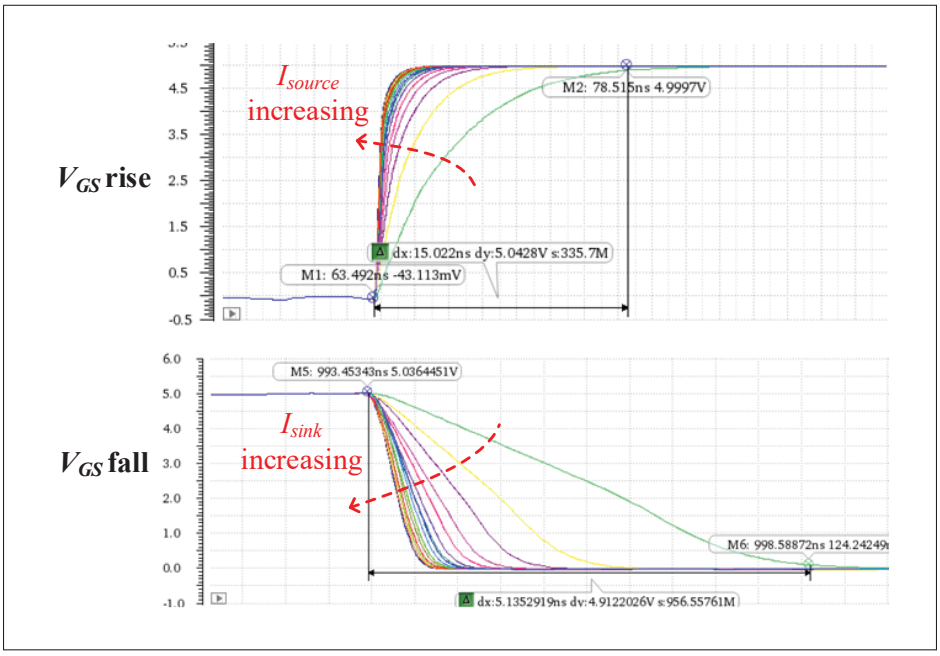


Figure 3.14 Post-layout simulation of the buffer driving EPC2012C with 15 drive strength levels

3.4.2 Dead-time Controller

Dead-time (DT) generator is a digital block with 6 input (PWM, Resetb and DT[3:0]) and 2 outputs (HS, LS). The DT[3:0] is a 4-bit configuration data which determines the DT value in use. Table 3.9 gives the relationship between DT[3:0] and the actual DT in ns. Table 3.10 shows the truth table of the input/output signals. To simplify the design, LS-to-HS and HS-to-LS share the same configuration data.

Table 3.9 Dead-time configuration data

DT[3:0] bin	DT value [ns]
0000	5
0001	10
0010	15
0011	20
0100	25
0101	30
0110	35
0111	40
1000	45
1001	50
1010	55
1011	60
1100	65
1101	70
1110	75
1111	80

Table 3.10 Truth table of DT block

Resetb	PWM	HS	LS
0	X	0	0
1	0	0	1
1	1	1	0

Figure 3.16 depicts the DT generator in detail. This is a non-overlapping logic with adjustable delay. The delay block consists of 16 of 5-ns delay blocks and a 16-to-1 multiplexer. DT[3:0] bus is tied to the input select signals of the multiplexer. The simulation of DT generator behaviour at

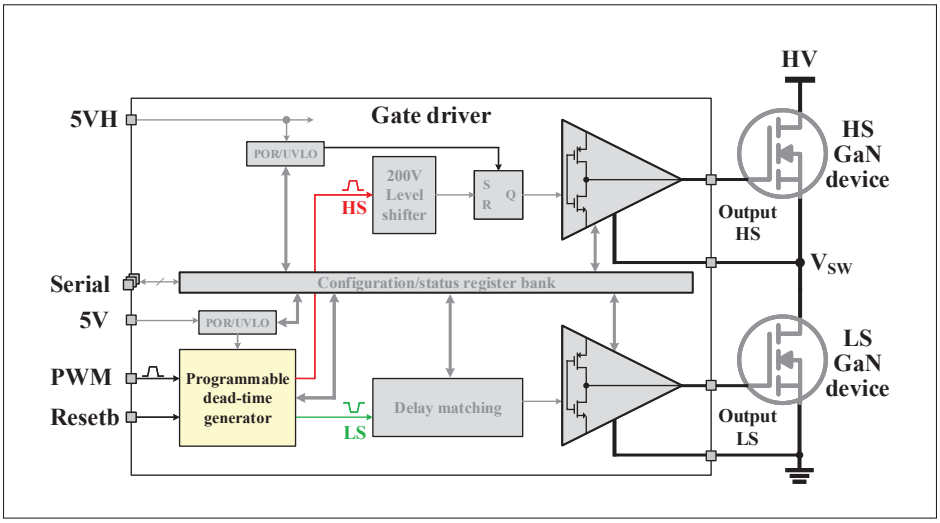


Figure 3.15 Dead-time generator of the gate driver

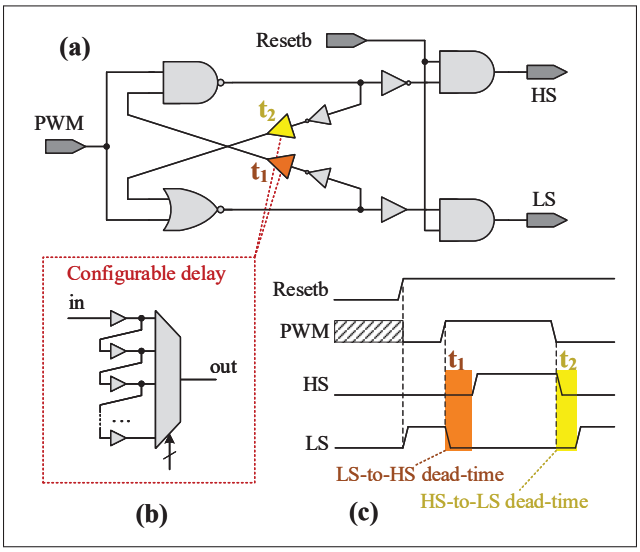


Figure 3.16 Dead-time generator design

DT = 10 ns is shown in Figure 3.17. The post-layout simulation of DT outputs across corners is given in Figure 3.18. The variation of the output is significant because the design is based on the standard buffer delay.

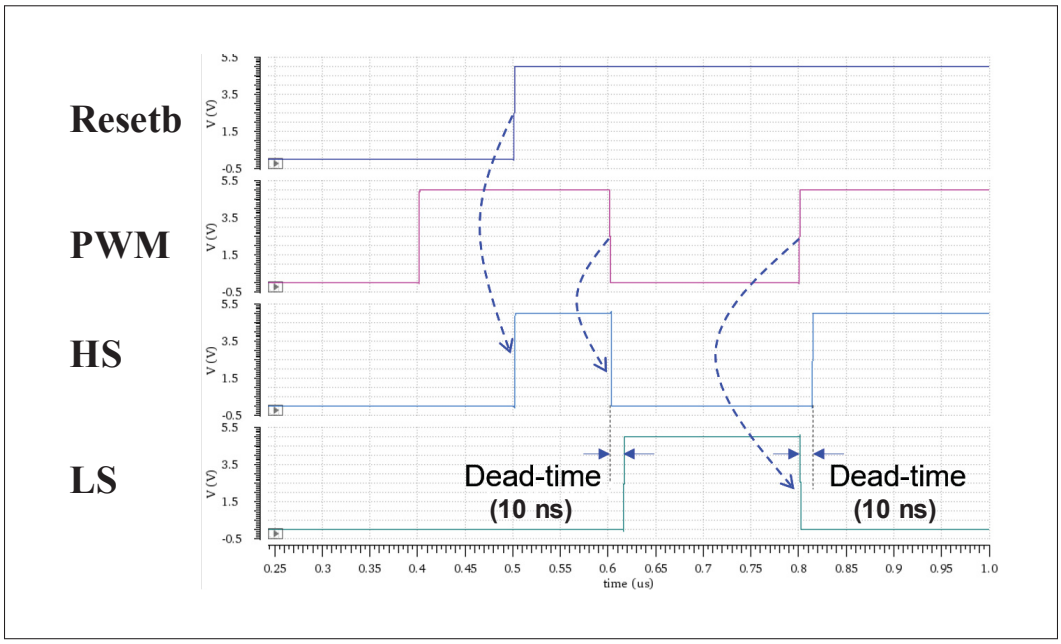


Figure 3.17 Dead-time behaviour simulation at DT = 10 ns

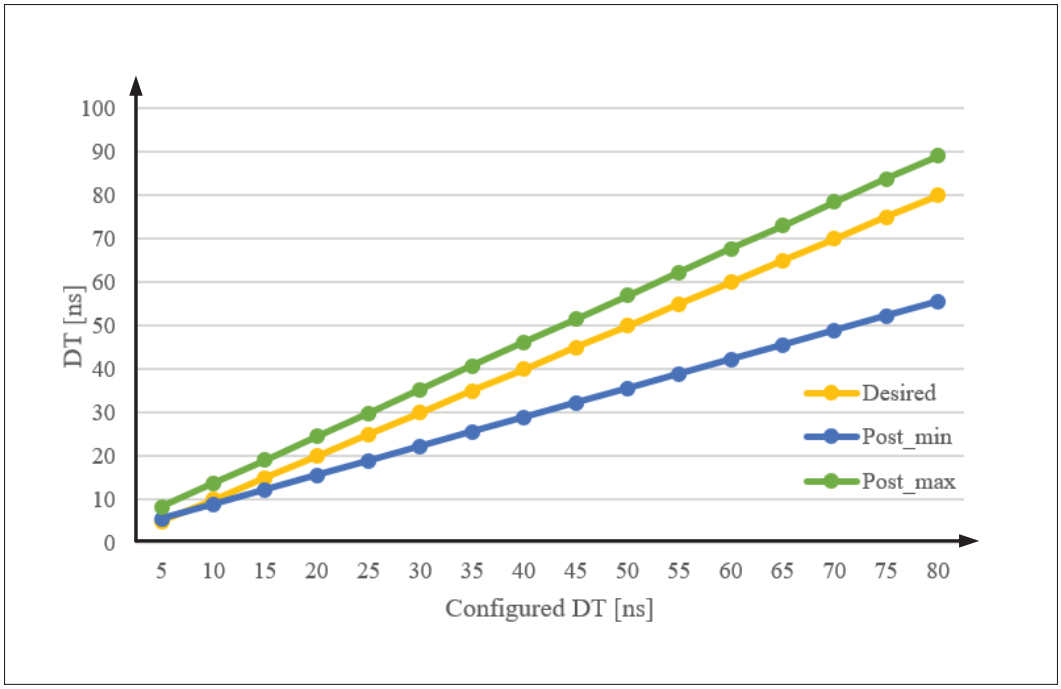


Figure 3.18 Dead-time - Post layout corners simulation (-40−85°C, 4.75−5.25 V)

3.4.3 Level-shifter

The CPIOS requires 84 V as the maximum input voltage of GaN half-bridges. Thus, a robust level-shifter block, as identified in Figure 3.19, with constant delay for the whole input voltage range is mandatory for the high-side. The level-shifter design is adapted from Liu *et al.* (2016).

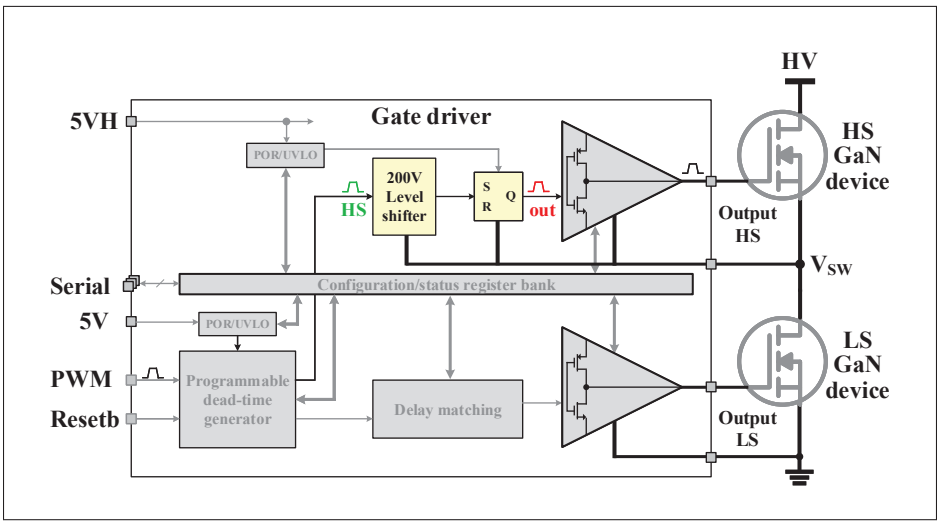


Figure 3.19 Level-shifter of the gate driver

Practically, the level-shifter is triggered at two moments: during DT when the LS GaN is freewheeling with V_{SW} (i.e. GNDH) at –1.5 V to –3 V for the turn-on of HS GaN, and when V_{SW} is high (i.e. 84 V) for the turn-off of HS GaN. In order to ensure the robustness and constant delay of the level-shifter for the voltage range from –3 V to 84 V of V_{SW}, first, a pair of HV transistors (HNM1a/b) are used. Second, they have to generate the same drain current ($I_{d-rise/fall}$) to trigger the latch, which requires them to operate in saturation with a headroom voltage as low as 2 V when V_{SW} is at –3 V, as calculated in Equation 3.3.

$$V_{headroom} = V_{5VH} = 5 + V_{GNDH} = 5 + V_{SW} = 2\ |_{V_{SW}\,=\,-3\ [V]}\ \ [V] \tag{3.3}$$

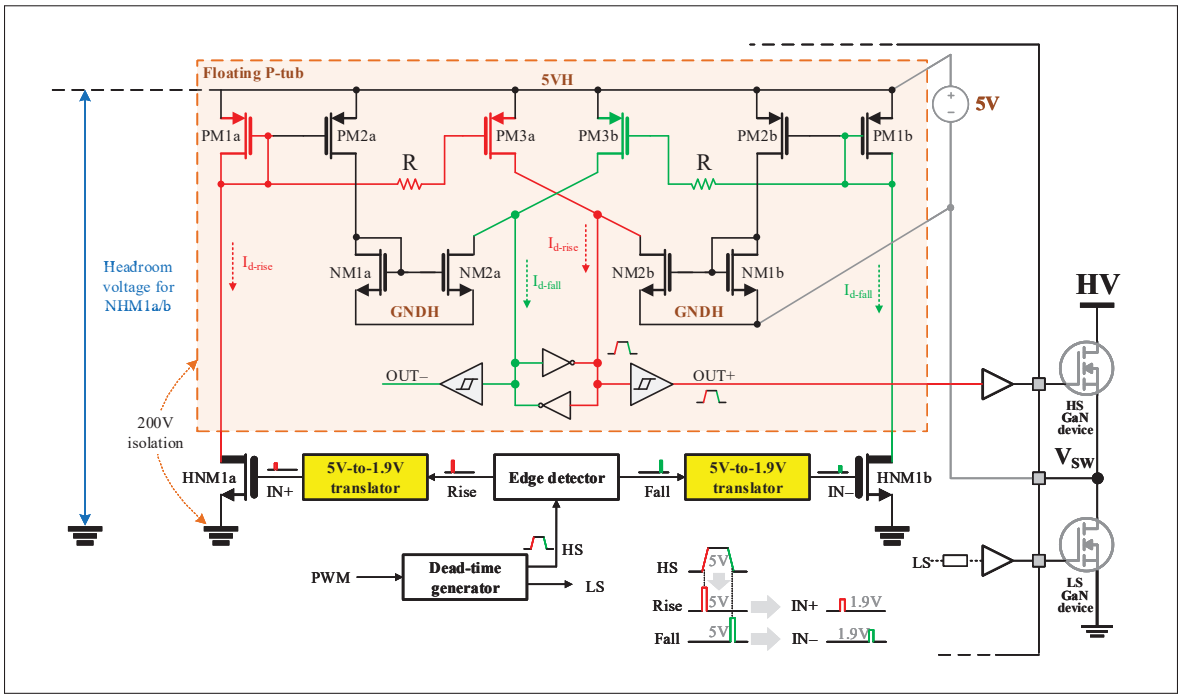


Figure 3.20 Level-shifter design

A 5-to-1.9V translator, converting 5 V-logic to 1.9 V-logic, helps reduce over-drive voltage (Vgs – Vth) of HNM1a/b. Thus, their saturation operation under lower headroom voltage is achieved. Major design steps will be analyzed in the following sections.

The ultimate goal of the level-shifter is to transmit digital from LS power domain to HS power domain. To save power consumption, the data is transmitted at the time it changes (i.e. edge sensitive) rather than keeping the link active all the time (i.e. level sensitive). Therefore, the level-shifter output should have a memory cell to store the transmitted value. The simplest structure for this is a back-to-back inverter pair latch as depicted in Figure 3.21. The latch is overridden with a pair of opposite phase current sources, so-called differential mode (Figure 3.21a), and is perturbed with a pair of current source of the same phase in common mode (Figure 3.21b). The differential-mode represents the normal operation in which the data is desired to be transmitted from LS to HS while the common-mode emulates the noise generated by common dV/dt of the floating ground (tied to V_{SW}).

To identify the inverters' size, the minimum differential-mode current needed to toggle the latch (I_{diff}) and the minimum common-mode current able to perturb the latch (I_{com}) are determined across all inverter sizes in the technology library. Table 3.11 shows the simulation results of I_{diff} and I_{com}.

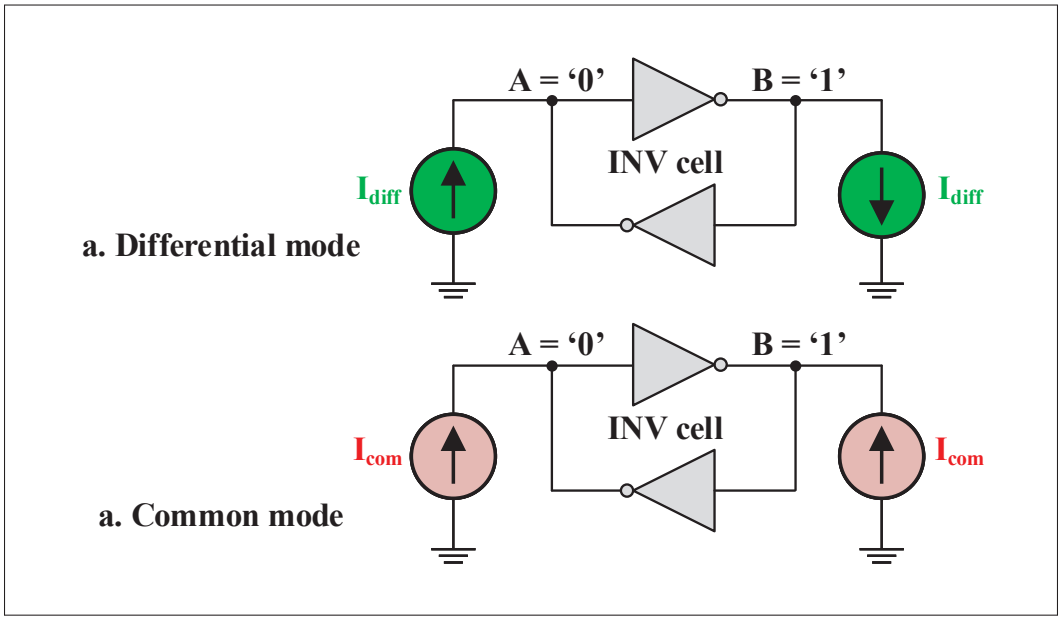


Figure 3.21 Back-to-back inverter pair latch triggered with current sources

Table 3.11 I_{diff} and I_{com} of latch with different sizes

Current [mA]	X0	X1	X2	X3	X4	X6	X8
I_{diff}	0.12	0.15	0.36	0.54	0.73	1.1	1.5
I_{com}	0.3	0.34	0.9	1.4	1.8	2.7	3.6

It is noticed that the current values increase with the latch size, and I_{com} is approximately 2.5x I_{diff}. In other words, the larger latch is, the more robust it is against common mode noise, but it requires higher current to trigger in normal mode. This is a power-robustness trade-off. The INV_X1 is chosen for the first design iteration. Figure 3.22 and 3.23 illustrate the common-mode and differential-mode current mechanism.

The common-mode current is induced by C_{DS} of the high-voltage nMOS HNM1a/b. To minimize this common-mode current, HNM1a/b should have minimum size (25/1μm with 2 fingers).

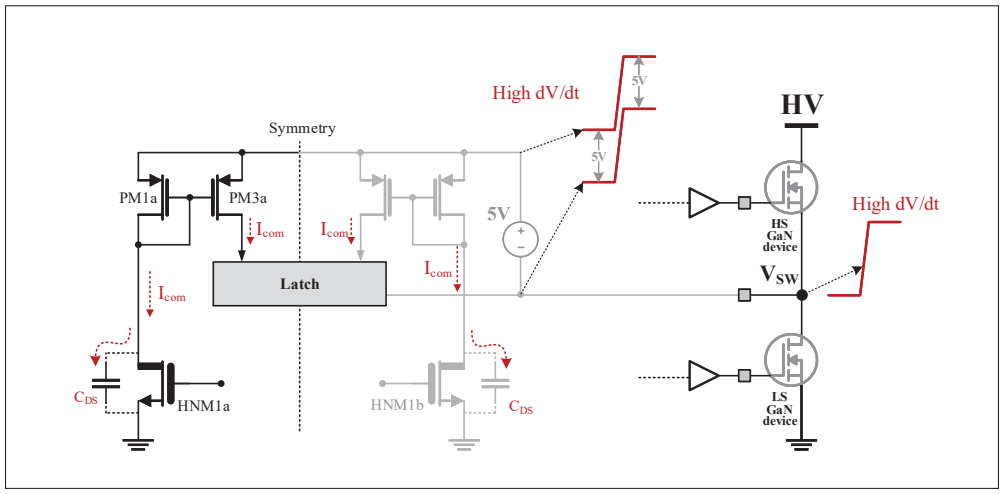


Figure 3.22 Mechanism of common-mode current

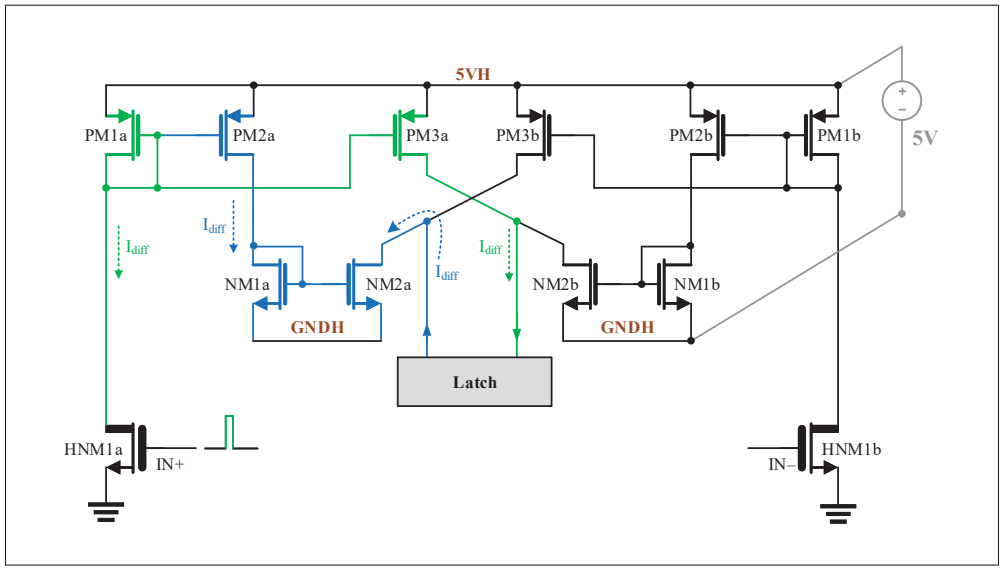


Figure 3.23 Mechanism of differential-mode current

Next, the pMOS PM1a is sized such that it does not require too high voltage drop when ON to support low head-room of the HV nMOS, as illustrated in Figure 3.24. Low head-room is made possible by reducing the triggering value of V_{GS} for the HV nMOS. Figure 3.25 plots I/V characteristics of the HV nMOS with different V_{GS}. The lower V_{GS}, the lower the head-room at the cost of lower drain current. The reasonable range of V_{GS} is from 1.8 to 1.9 V with the

allowed voltage drop across the PM1a of 1 to 1.5 V, at the drain current range of 0.3 to 0.7 mA. This current range is sufficient to trigger the latch of INV_X1.

The size of PM1a is then determined, as simulated in Figure 3.26. With W/L of 80/0.5 μm, its voltage drop and current are within the specified range.

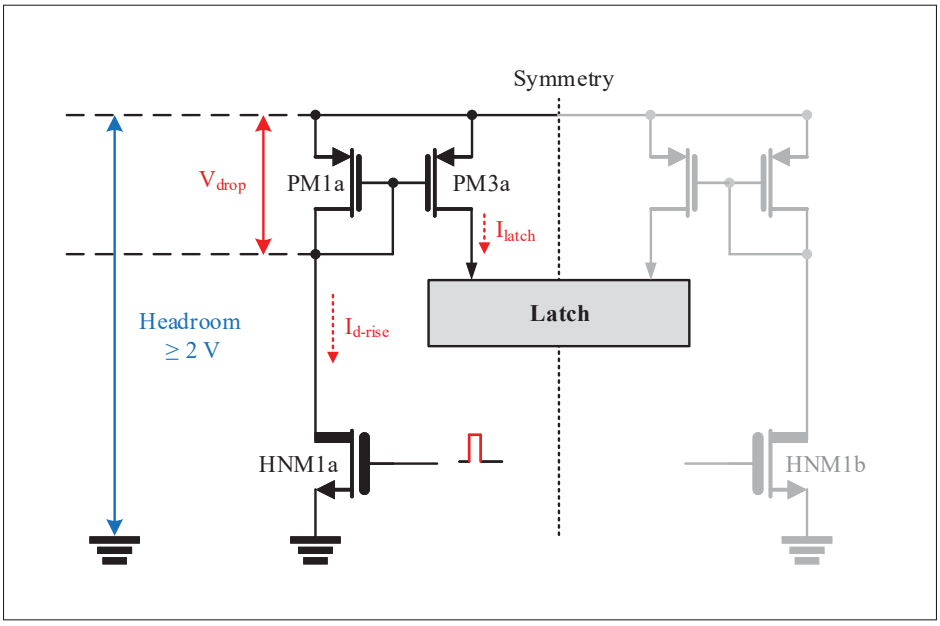


Figure 3.24 Sizing diode-connected pMOS

The overall operation of the level-shifter will be demonstrated in the post-layout simulation of the entire chip, along with a pair of GaN devices in half-bridge topology. An immunity against >200 V/ns will be shown.

3.4.4 Configuration registers

Figure 3.27 highlights the configuration block, one of the key elements of the gate driver. This block contains the configuration data for the entire chip. In order to reduce the I/O pin count, the serial-in-parallel-out type shift registers are utilized. With serial interface, the pin count is not scaled up with the number of bits in use.

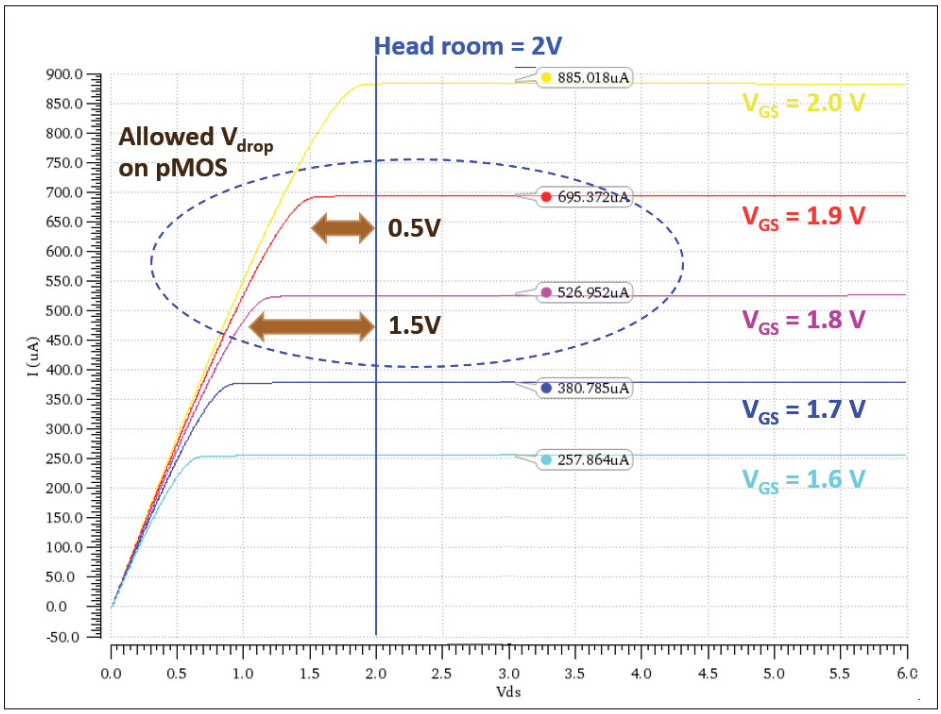


Figure 3.25 I/V characteristics of HV nMOS (50μm/1μm) is plotted with different V_{GS}

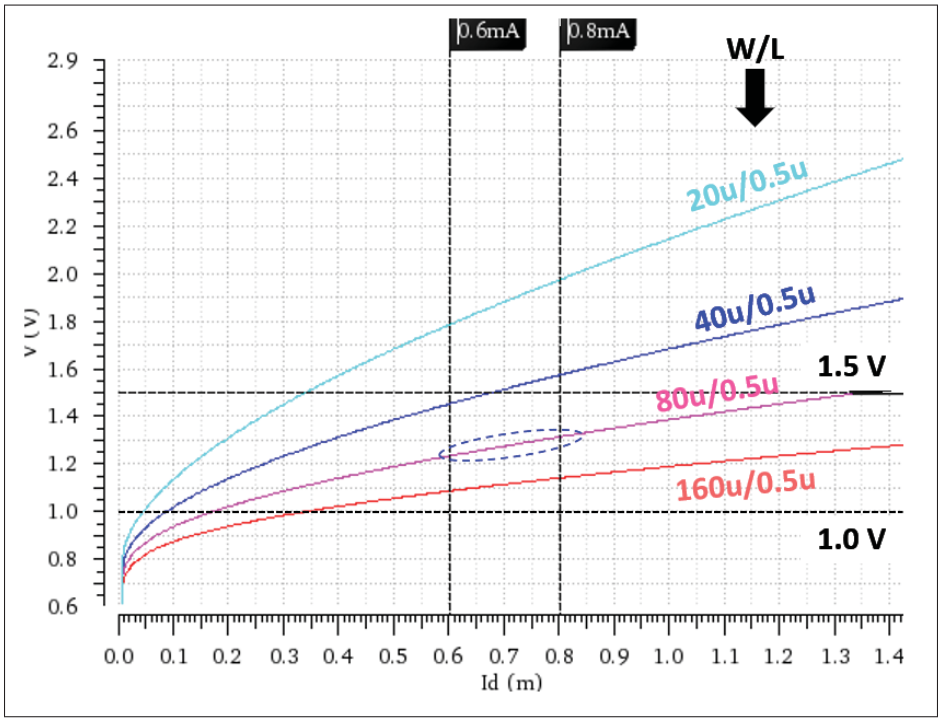


Figure 3.26 I/V of the diode-connected pMOS is plotted with different sizes

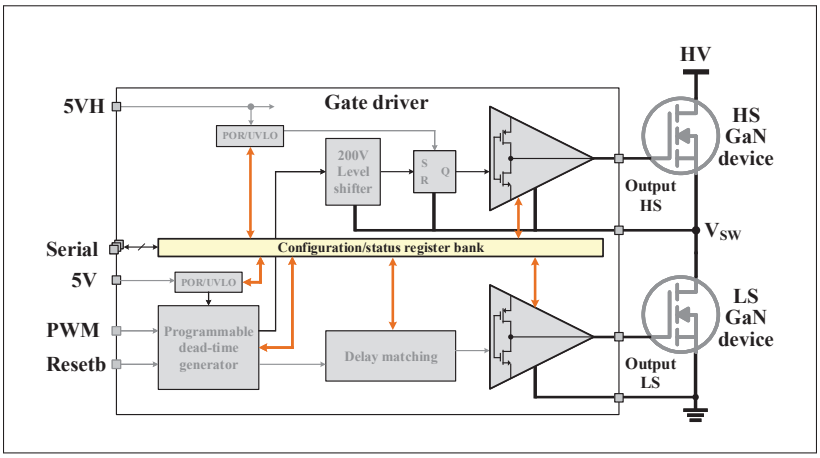


Figure 3.27 Configuration registers of the gate driver

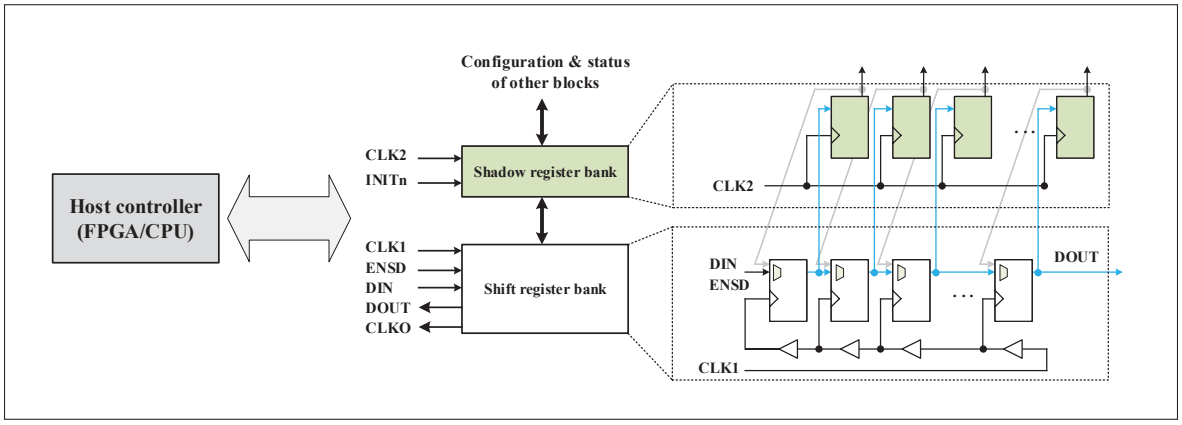


Figure 3.28 A configuration register set including a shift register and a shadow register

There are two sets of shift registers: one for HS and one for LS since they are under different power domains, as illustrated in Figure 3.29. Each one consists of two register banks, namely shift and shadow. The shadow registers hold the configuration bits while the shift registers are to receive and transmit the configuration bits from and to the host controller. The shadow registers are realized with D flip-flops (FF) while the shift registers consist of scan FFs (Figure 3.28). Table 3.12 describes the serial interface signals.

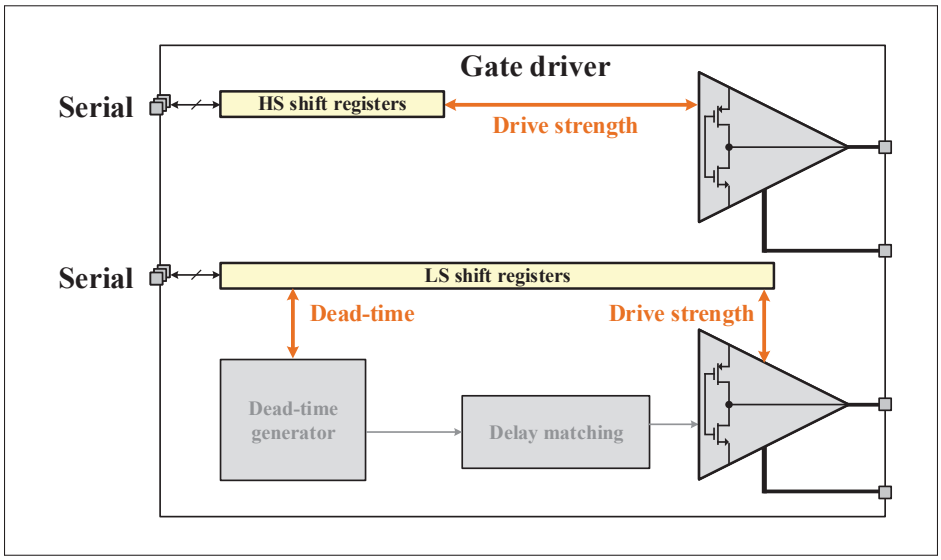


Figure 3.29 Configuration registers distribution of the gate driver

Table 3.12 Pin description of serial interface of the shift registers

Pin name	Description
CLK2	Clock of shadow register
INITn	Active-low reset of shift register
CLK1	Clock of shift register
ENSD	Active-high shift enable of shift register
DIN	Input data of shift register
DOUT	Output data of shift register
CLKO	Output clock of shift register

Table 3.13 shows the data bit assignment of both shift register sets. The reset values are 0x66 and 0x666 for the 8-bit register and 12-bit register respectively.

Table 3.13 Data bit assignment of the shift registers

HS 8-bit	Description	LS 12-bit	Description
		D[11:8]	DT_SEL[3:0] dead-time
D[7:4]	HS_PU[3:0] strength	D[7:4]	LS_PU[3:0] strength
D[3:0]	HS_PD[3:0] strength	D[3:0]	LS_PD[3:0] strength

If the system has multiple gate drivers, which is the case in this CPIOS project, then the shift registers of all gate drivers can be daisy-chained. As a result, the host controller can access any bit of the chain with a single serial interface. However, this chain connection requires careful consideration because of the different power domains. The interface between power domains are made possible using digital isolators as depicted in Figure 3.30.

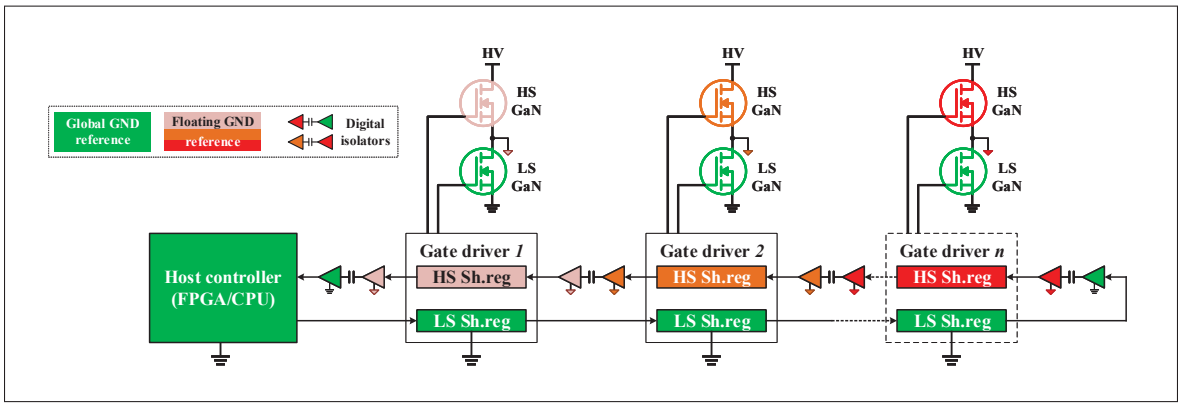


Figure 3.30 Daisy-chain of multiple shift registers in a system

As both shift/shadow register sets have similar timing performance results, the 8-bit register will be analyzed through simulation. Figure 3.31 shows the post-layout simulation of the 8-bit shift/shadow register set with a 200 MHz clock. There are four main operations: shift-data-in, write-shadow, read-shadow and shift-data-out. The clear-data operation is optional to make sure the shift register value is different from the shadow one before copying data from the latter. Each one of these operations will be analyzed in detail.

Figure 3.32 illustrates the first two operations: shift-data-in an write-shadow. At system start-up, the shadow register is reset with the active-low INITn input. The shift-data-in operation starts by feeding a serial data input sequence synchronized with CLK1 while enSD is held high. After eight CLK1 cycles, the entire shift register holds the new data. Now CLK1 should be stopped in order to start the second operation, write-shadow. It takes one CLK2 cycle to copy the shift register value into the shadow one. From this moment, the configuration data takes effect.

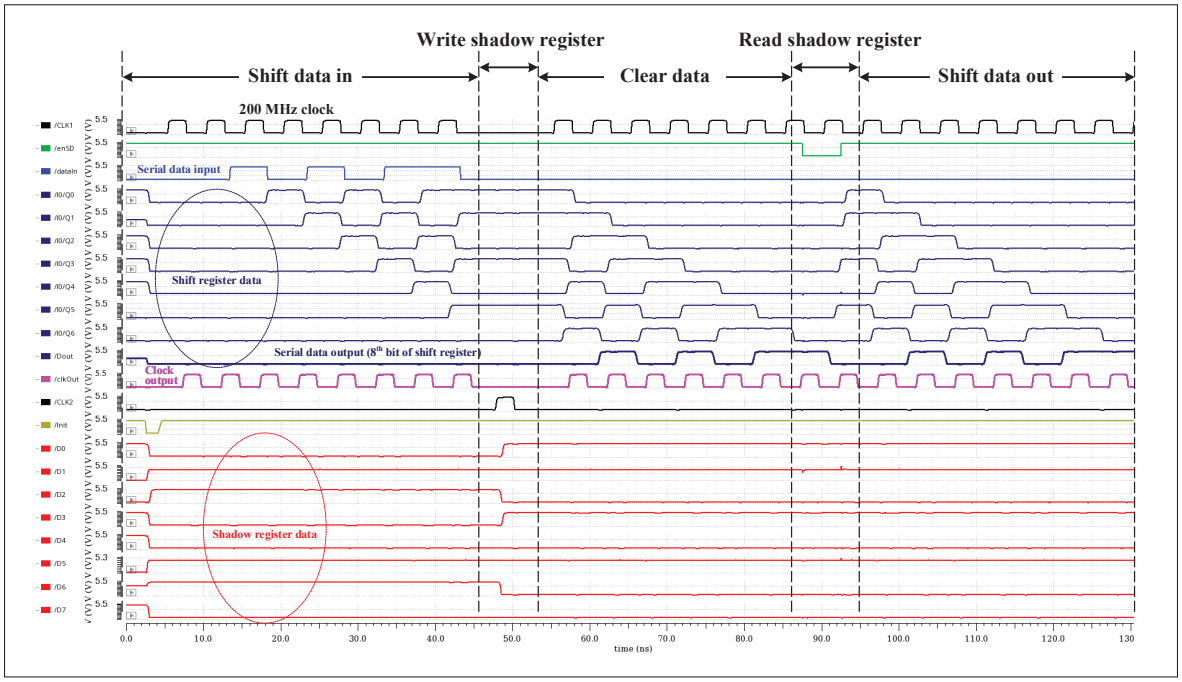


Figure 3.31 Four main operations of a shift/shadow register set

At some point, if the configuration data, held by the shadow register needs to be verified, it can be read back and shifted out for validation as illustrated in Figure 3.33. To copy shadow register back to the shift register for the read-shadow operation, only one CLK1 cycle is needed while enSD is held low. Once done, data can be shifted out.

The shift registers can operate up to 300 MHz clock as simulated in Figure 3.34. However, they should be operated at 200 MHz maximum to have a good timing margin.

3.5 Chip layout & simulation

XFAB XT018 supports two form factors of electrostatic discharge (ESD) cell with bonding pad: pad-limited and core-limited. Pad-limited ESD cells are long and narrow (60x243 μm), used in designs whose sizes are imposed by the number of IO pads. In contrast, in designs with complex core structure and few IO pads, the short and wide core-limited ESD cells (84x160 μm) are used. Both types support 4-kV human body model (HBM) target ESD robustness.

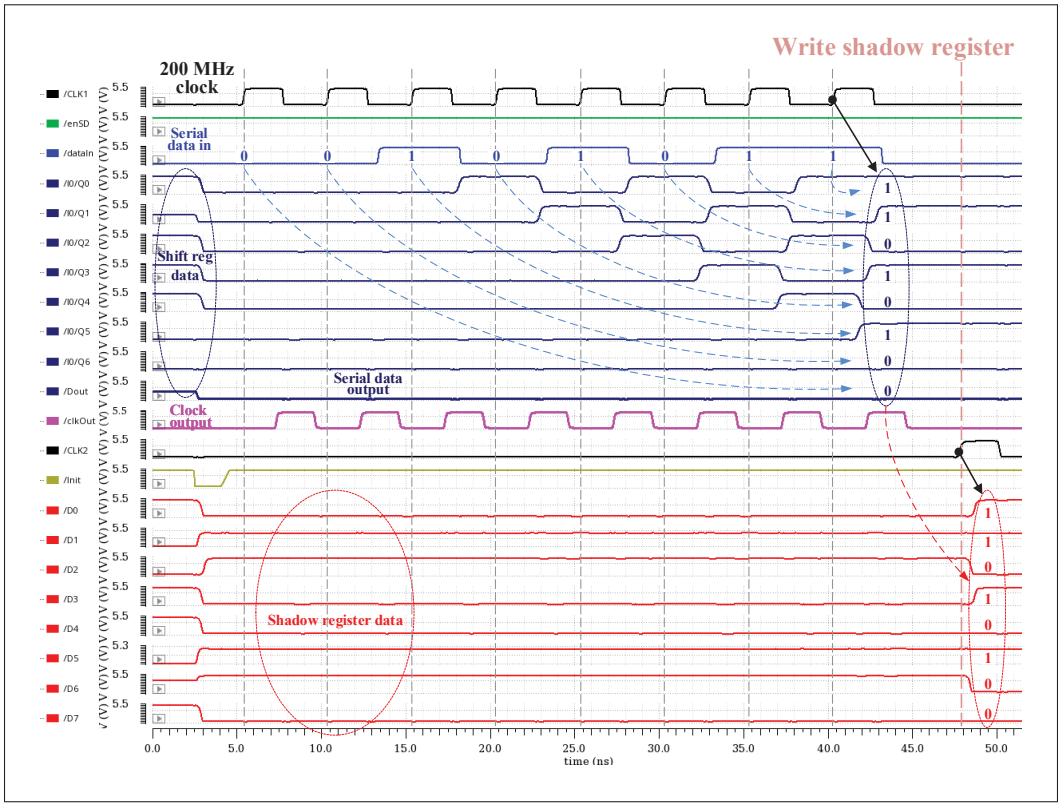


Figure 3.32 Shift-data-in and write-shadow

Figure 3.35 shows the ESD pad cell form factors and the general chip floorplan. The pad cells are placed around the chip core with the bonding pad oriented towards the outside. There are many pad cell types that can be categorized in the following:

1. Power cell.
2. GND cell.
3. Input signal cell.
4. Output signal cell.
5. Bidirectional signal cell.

3.5.1 Gate driver layout

Figure 3.36 shows the layout and micrograph of the gate driver. There are 38 bonding pads with the pin assignment given in Table 3.14. This is a pad-limited design in which the overall size is

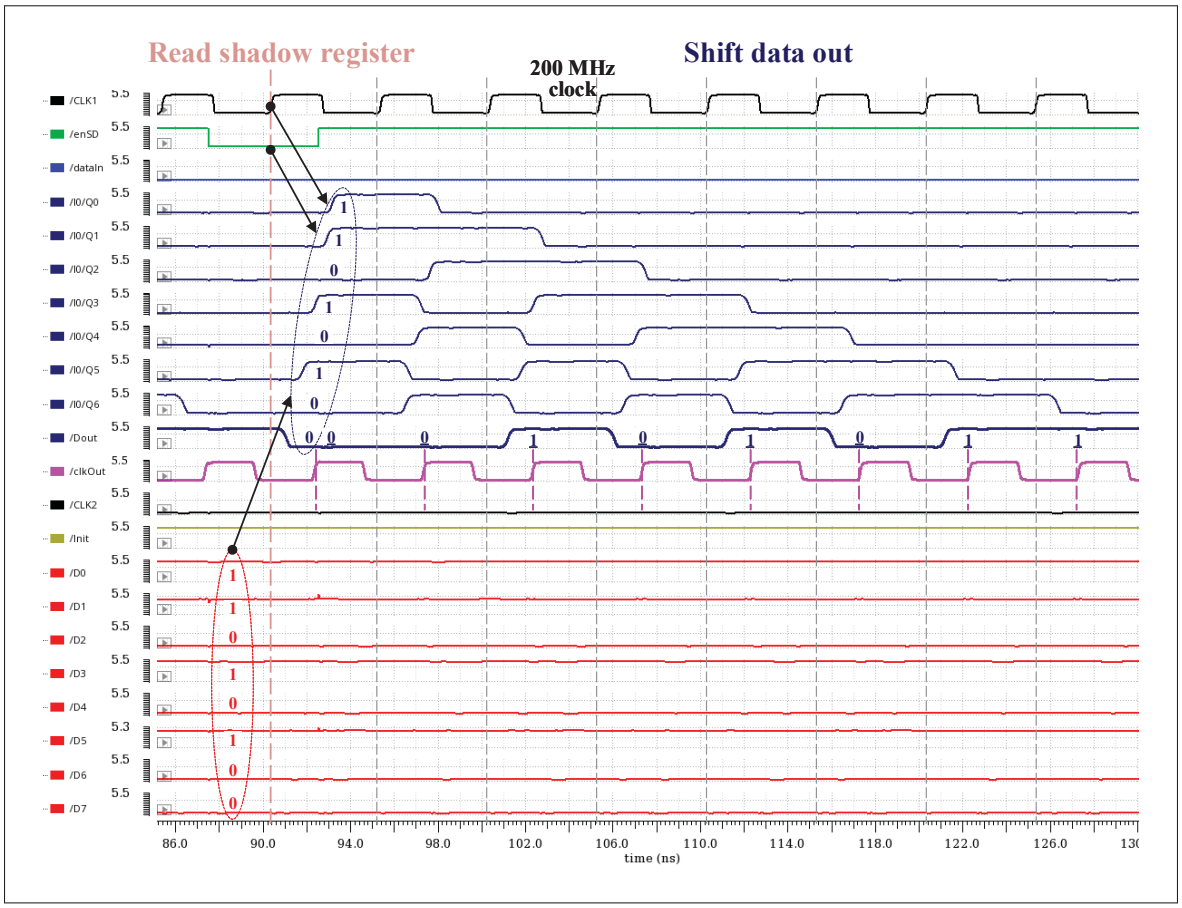


Figure 3.33 Read-shadow and shift-data-out

imposed by the number of pads. The default bonding pad of ESD cells is 60x67 μm which is good enough for automated bonders but way too small for semi-automated or manual machines. For a practical reason, in this first version of the chip, the 100x100 μm bonding pads are added for the ease of bonding. The active area of the chip is 0.5 mm^2.

Figure 3.37 shows the layout of the dead-time generator block. This block is purely digital with standard cells (and, or, nand, nor, not, buffer) and filler and cap cells. The overall size of this block is 113x55 μm.

Figure 3.38a is the layout of the output driver stage. There are 15 slices of buffer whose current source/sink is 100/200 mA. This driver stage occupies 680x175 μm of die size. Figure 3.38b and c show one buffer slice placement and routing respectively.

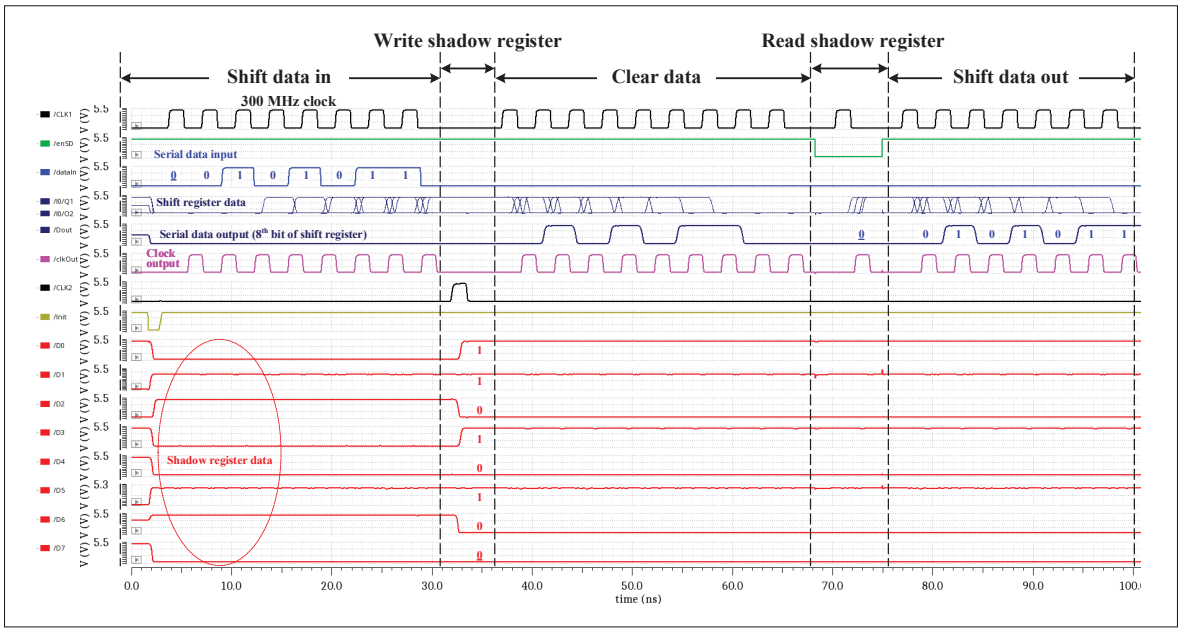


Figure 3.34 Post-layout simulation of 8-bit shift/shadow register at 300 MHz clock

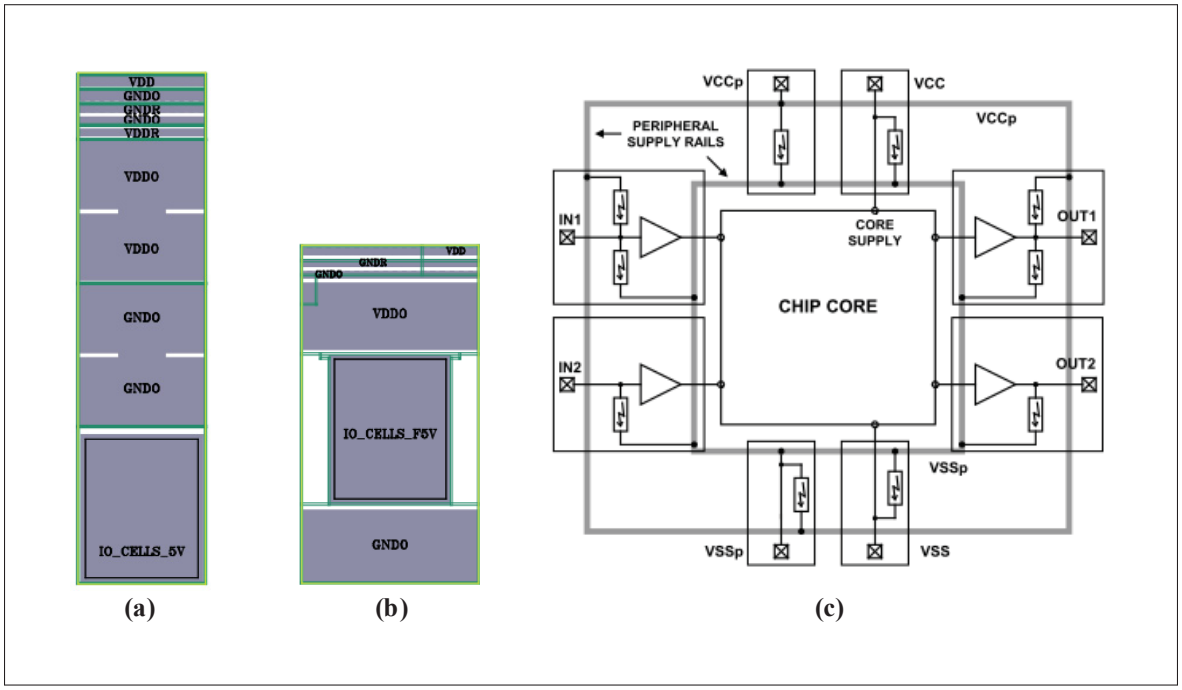


Figure 3.35 ESD pad cell for (a) pad-limited and (b) core-limited chip
(c) General chip floorplan with ESD pad cells

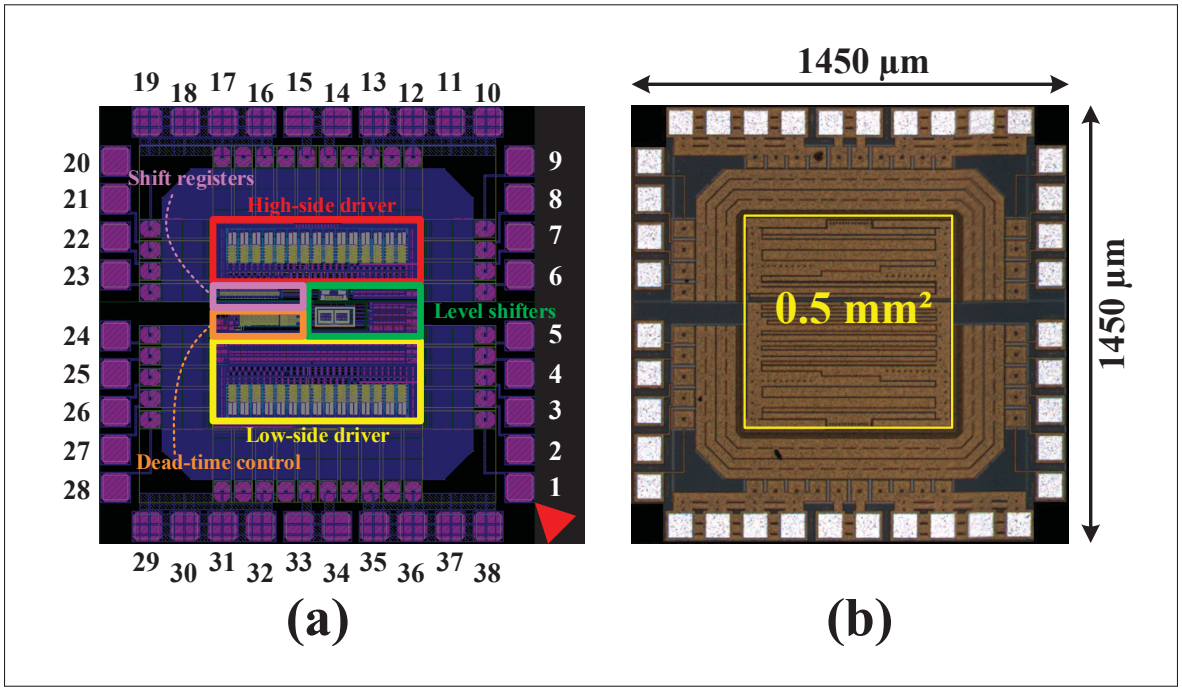


Figure 3.36 The gate driver (a) layout and (b) micrograph

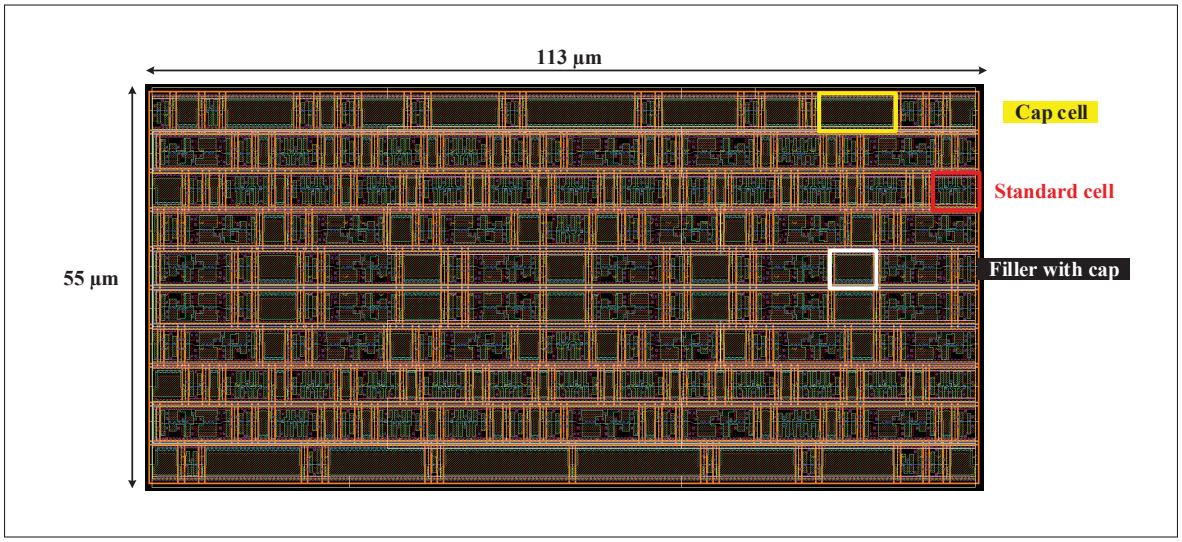


Figure 3.37 The layout of dead-time generator

Figure 3.39 shows the layout of level-shifter group, including the 5V-to-1.9V translator, 200 V level-shifter and output latch with reset logic. The latch along with the HS part of the level-shifter are supplied with floating 5 V which has a high common-mode voltage with respected to global

Table 3.14 Pin description of the gate driver

Pin no.	Pin name	Description
1	RESETn	Active-low reset of entire chip
2	DISABLEn	Active-low disable of entire chip (AND'ed with RESETn)
3	LSR_CLKO	Output clock of LS shift register
4	LSR_DOUT	Output data of LS shift register
5	PMW_IN	PWM input
6	HSR_ENSD	Active-high shift enable of HS shift register
7	HSR_DOUT	Output data of HS shift register
8	HSR_CLKO	Output clock of HS shift register
9	RESETnH	Active-low reset of the latch (after level-shifter)
10,11,12,13	GNDH	HS ground (floating ground, connect to V_{SW})
14,15	HSG	Output connect to HS GaN device
16,17,18,19	VDD5H	5V supply (vs. GNDH)
20	HSR_INITn	Active-low force initial value of HS shift register
21	HSR_CLK1	Clock of HS shift register
22	HSR_CLK2	Clock of HS shadow register
23	HSR_DIN	Input shift data of HS shift register
24	LSR_DIN	Input shift data of LS shift register
25	LSR_CLK2	Clock of LS shadow register
26	LSR_CLK1	Clock of LS shift register
27	LSR_INITn	Active-low force initial value of LS shift register
28	LSR_ENSD	Active-high shift enable of LS shift register
29,30,31,32	VDD5L	5V supply (vs. GNDL)
33,34	LSG	Output connect to LS GaN device
35,36,37,38	GNDL	LS ground (connect to global ground)

ground. Hence the entire HS logic circuit is placed in a floating p-tub which is isolated from the main substrate with a double DTI (Deep trench insulation) layer. This double DTI support 200-V isolation.

Figure 3.40 shows the layout of the configuration registers: 8-bit for HS and 12-bit for LS. Each set of registers has one instance of shift-register and one instance of shadow-register of the same length.

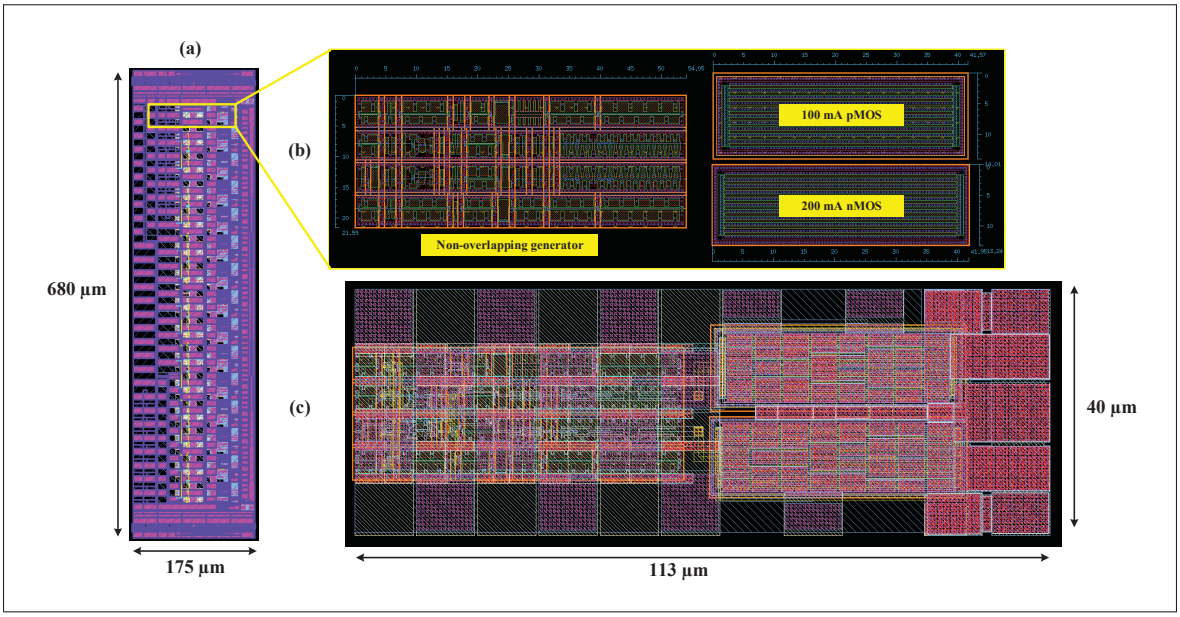


Figure 3.38 The layout of (a) output driver.
One buffer slice (b) placement and (c) routing

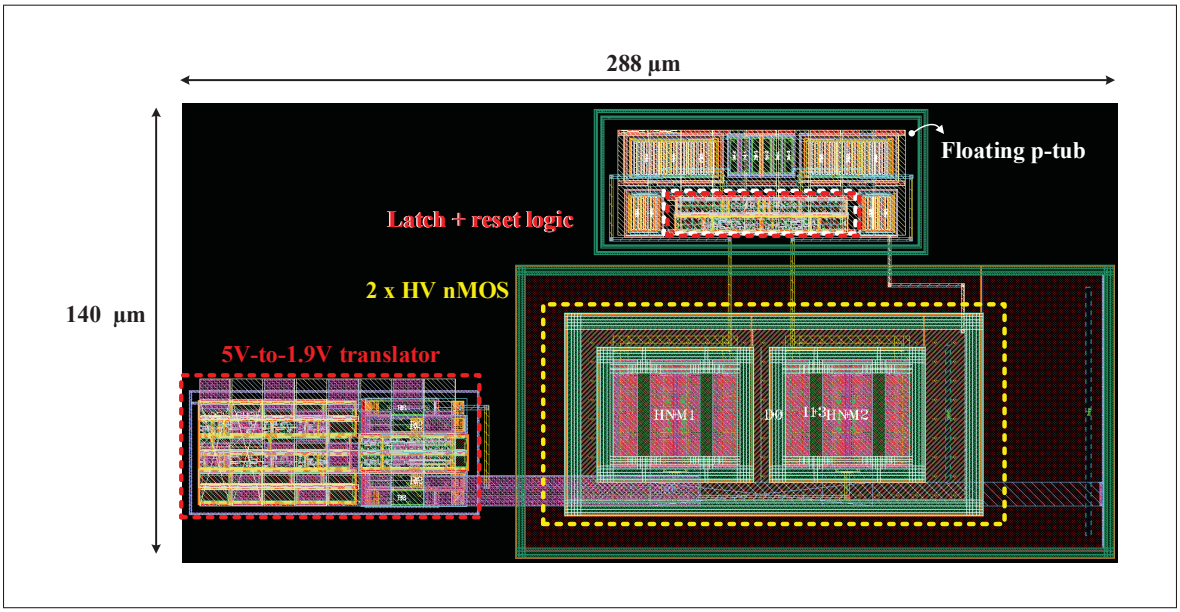


Figure 3.39 The layout of level-shifter group

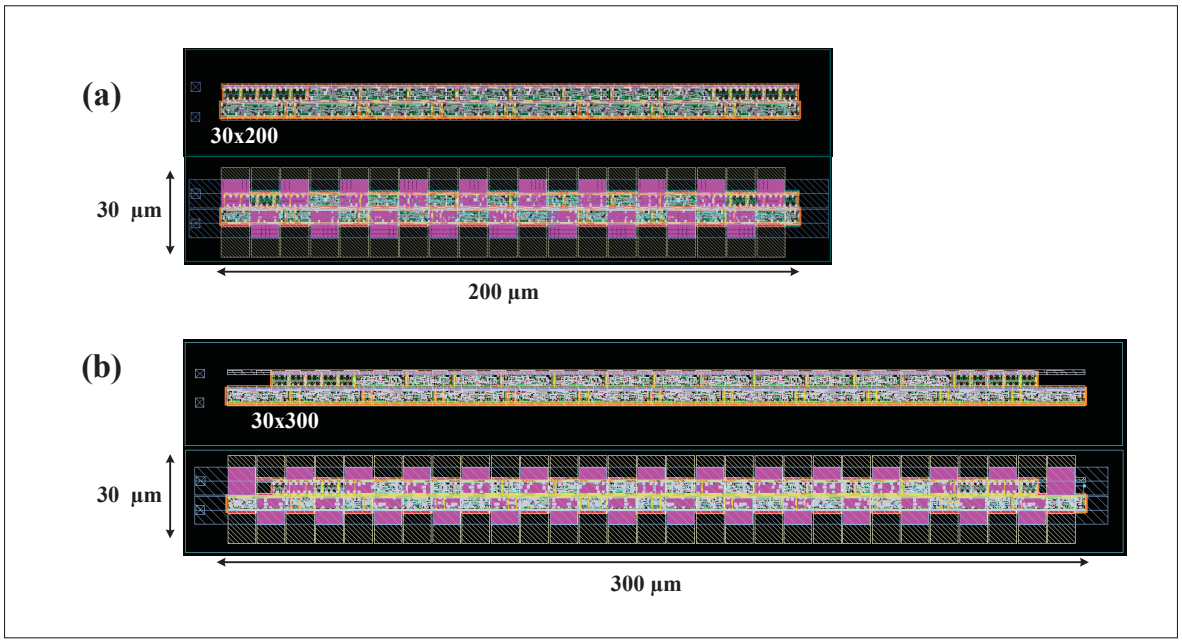


Figure 3.40 The layout of configuration registers (a) 8-bit for HS and (b) 12-bit for LS

3.5.2 Post-layout simulation of the gate driver

To evaluate the operation of the gate driver, an open-loop buck converter is utilized as the test bench as depicted in Figure 3.41. The supply voltage is 48 V with PWM duty cycle of 50% and 50 ns DT. Load current varies from 0.1 A to 1.25 A. Figure 3.42 shows the waveforms of V_{SW} node. During DT, the LS GaN device conducts reversely which results in negative V_{SW} and high loss. As expected, the rising edge of V_{SW} is independent of load current while the falling edge slope is proportional to I_{load}. Figure 3.43 shows the zoomed falling edge of V_{SW}.

The next simulation is performed with different DT values at 1 A load current, shown in Figure 3.44. Figure 3.45 shows the zoomed falling edge of V_{SW}. It is concluded that DT configuration takes effect on the output as expected.

Figure 3.46 shows the post-layout simulation of the circuit at 200-V at V_{in}, the zoomed rising edge of V_{SW} in Figure 3.47 shows a dV/dt of 226 V/ns.

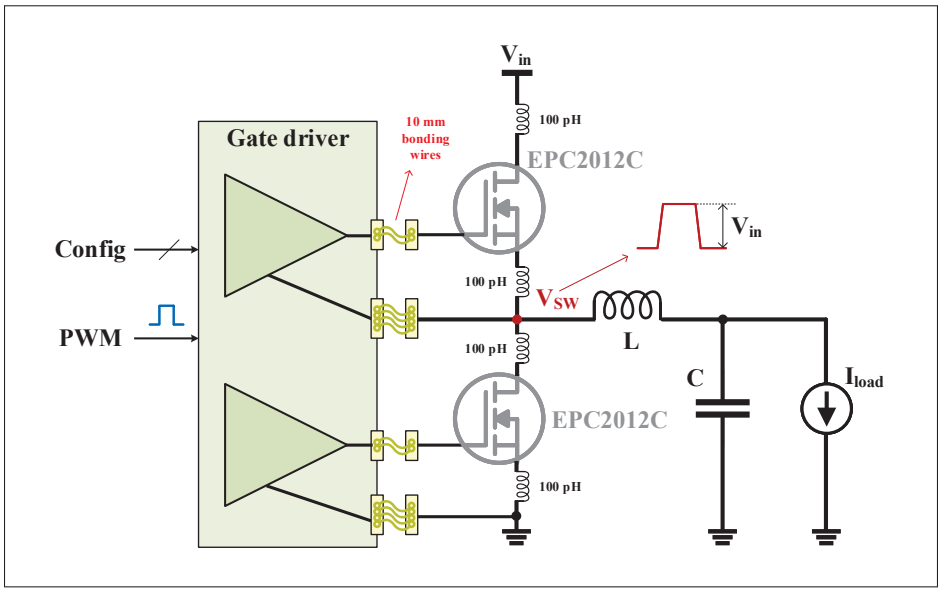


Figure 3.41 The test bench schematic of the gate driver

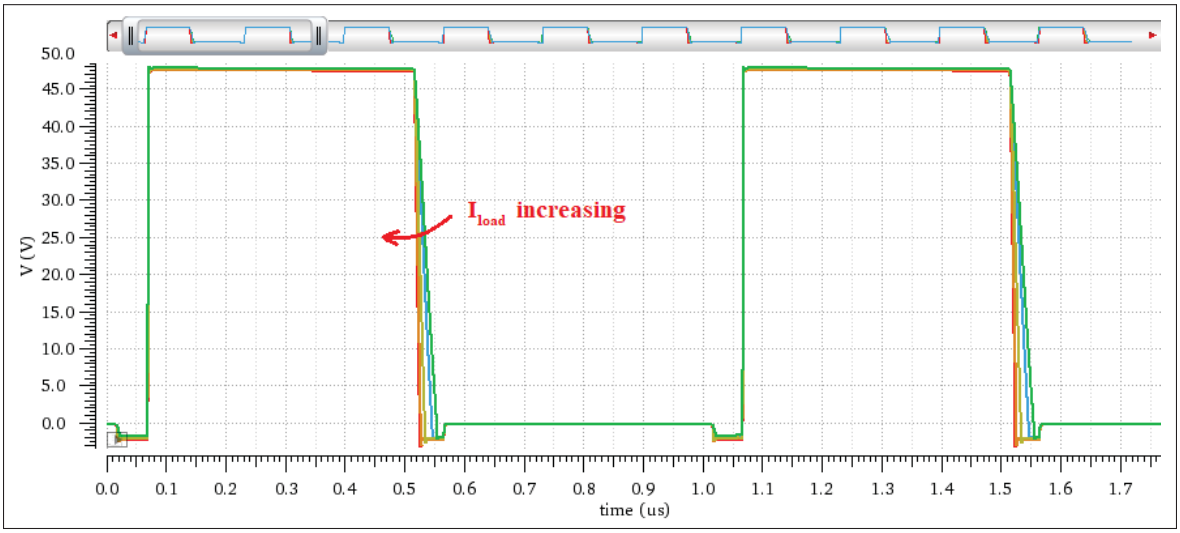


Figure 3.42 V_{SW} waveforms at 48-V V_{in} with fixed 50-ns DT and different load current values

3.6 Conclusion

The design, layout and simulation of the proposed gate driver is discussed in this chapter. The design approach is chosen to be conventional but robust. The level shifter is immune

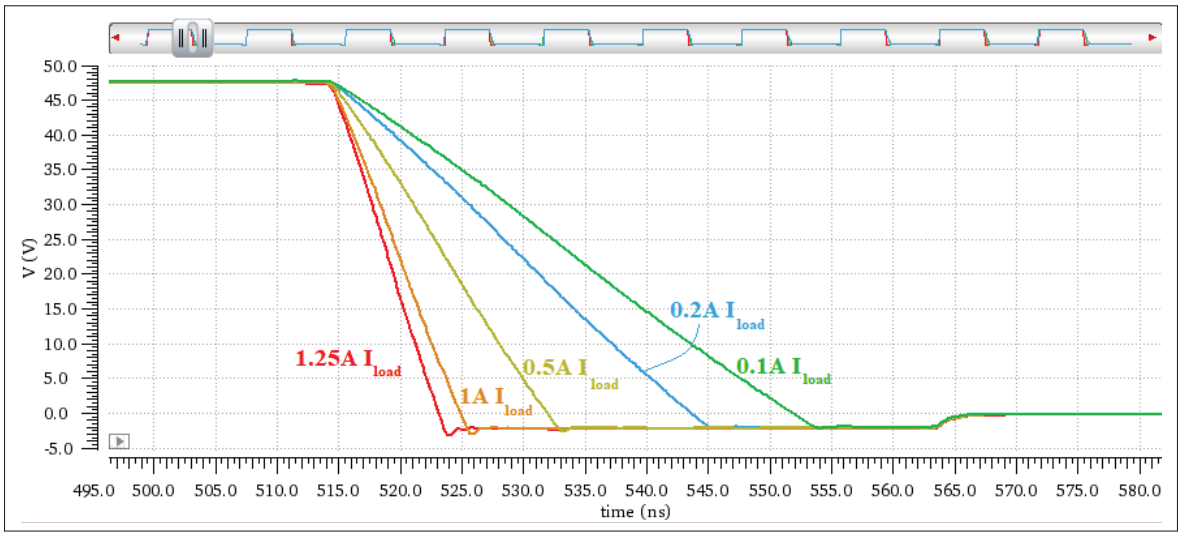


Figure 3.43 Zoomed falling edge of V_{SW} in Figure 3.42

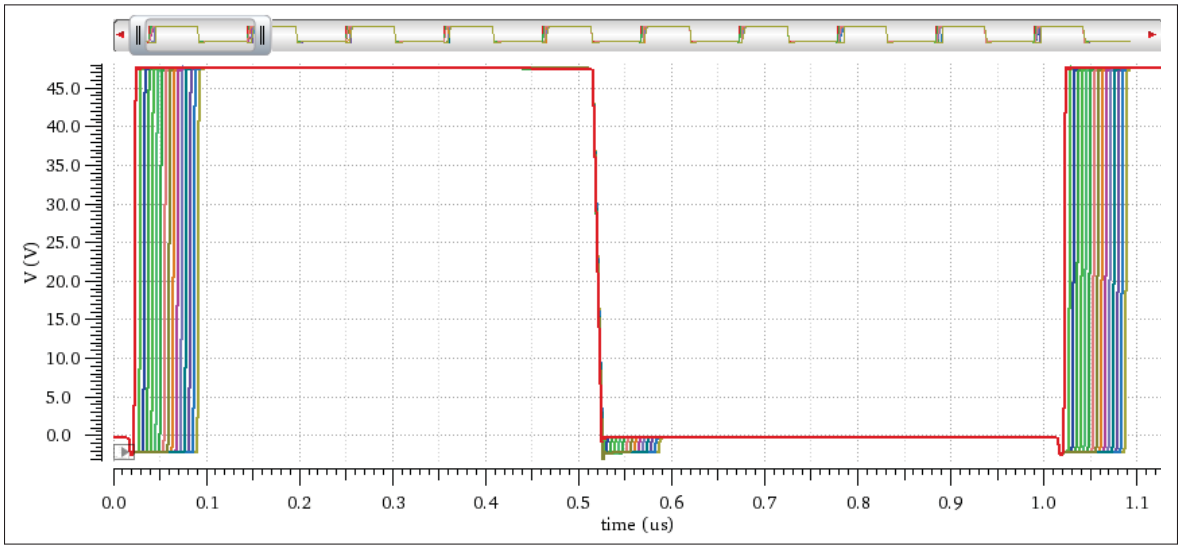


Figure 3.44 V_{SW} waveforms at 48-V V_{in} with fixed 1-A load and different DT values

against >200 V/ns of V_{SW} (floating ground). The shift registers can operate up to 300 MHz in post-layout simulation. The dead-time generator and output buffers are configurable with expected parameters. The next chapter will discuss about the test system and measurement results.

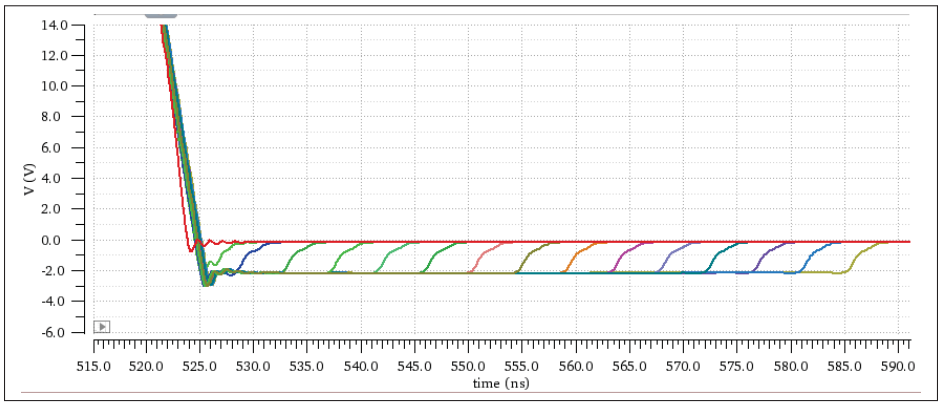


Figure 3.45 Zoomed falling edge of V_{SW} in Figure 3.44

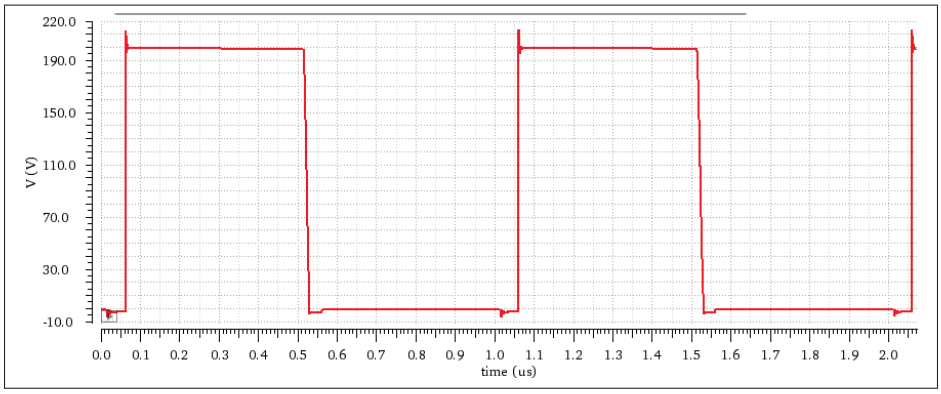


Figure 3.46 V_{SW} waveforms at 200-V V_{in} with 1-A load and 50-ns DT

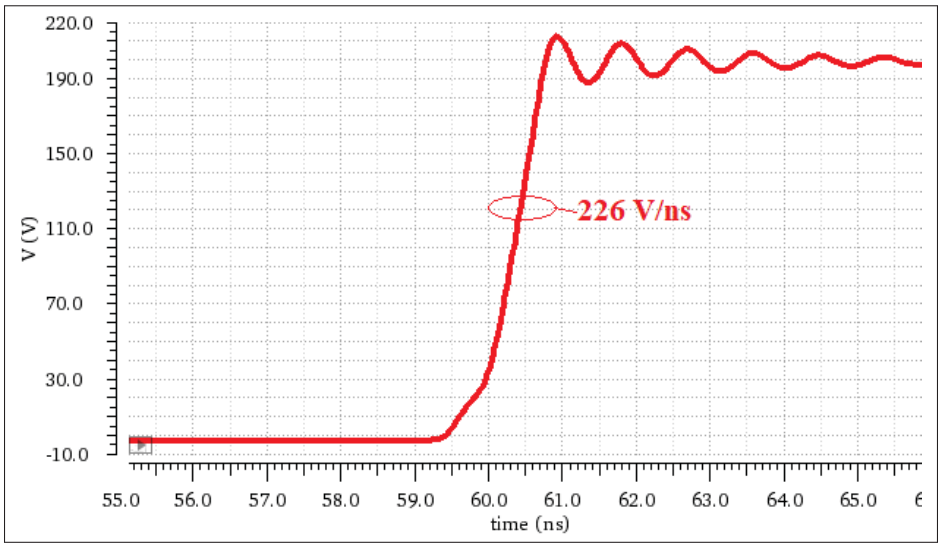


Figure 3.47 Zoomed rising edge of V_{SW} in Figure 3.46

CHAPTER 4

CIRCUIT MEASUREMENTS

4.1 Introduction

This chapter describes the test system for the gate driver, including PCB, FPGA and PC software designs. The measurement results will be shown and discussed.

4.2 Test System Description

Two experimental test-benches are used: one with the gate driver alone for its characterization and another with an open-loop buck converter with a GaN half-bridge driven by the gate driver. Both units under test are controlled with an FPGA kit via a software developed specifically for this gate driver testing.

Figure 4.1 shows the overall test diagram. The software GUI is developed under MATLAB to control the gate driver, as shown in Figure 4.2.

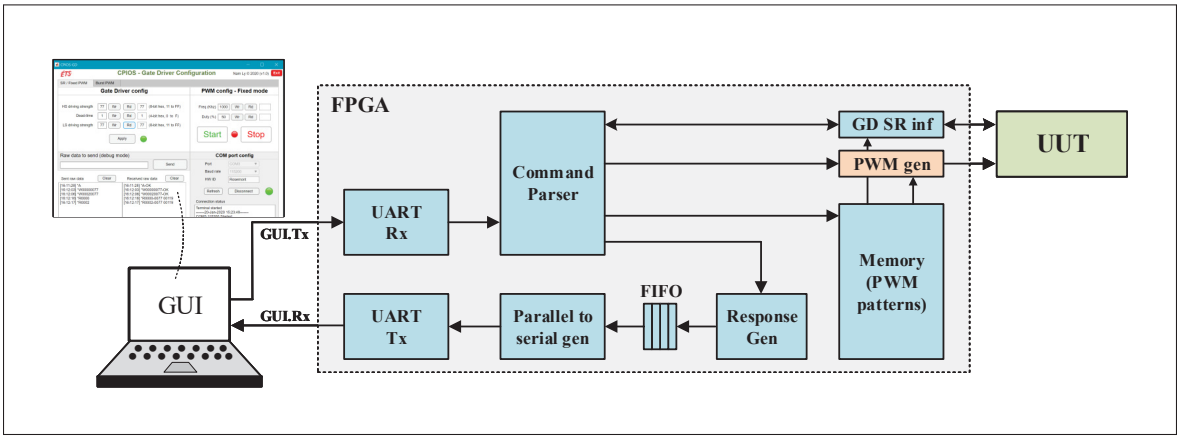


Figure 4.1 Test-bench diagram

Figure 4.3 shows the test setup of the open-loop buck converter operating with input voltage up to 86 V at 1 MHz PWM.

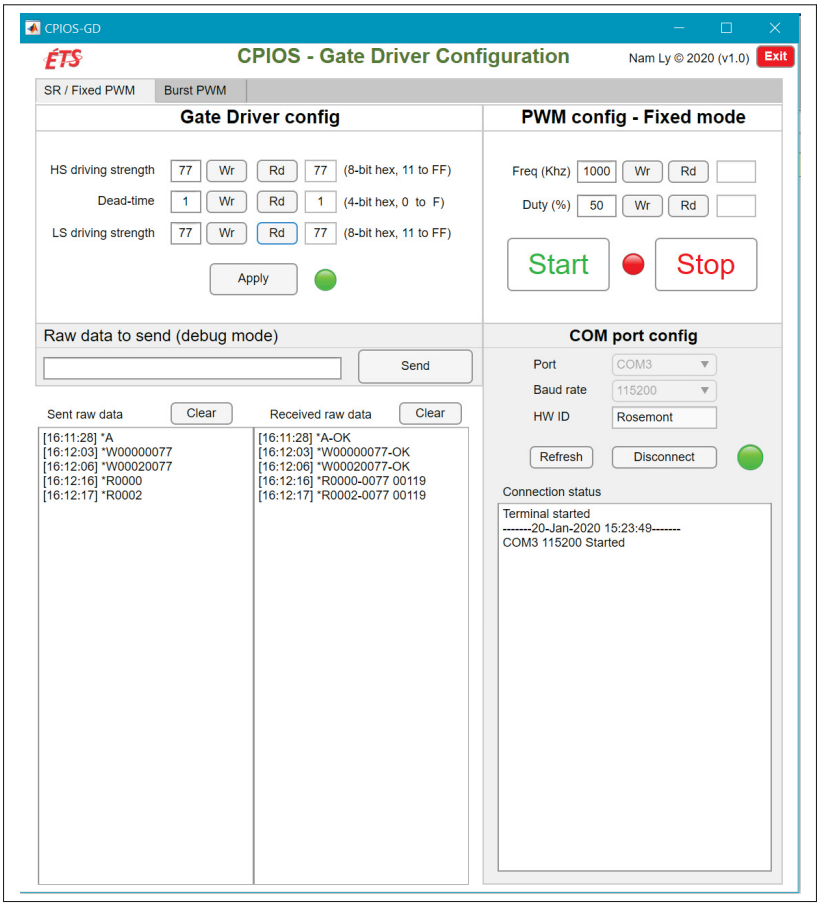


Figure 4.2 Matlab GUI of gate driver configuration and fixed PWM mode

4.3 Test results

The following table summarizes the test results and comparison with simulation results and some of commercial gate drivers.

Figure 4.4 demonstrates the dead-time optimization with a specific load condition, which helps minimize reverse conduction of the LS GaN HEMT.

Figure 4.5 shows the measurement of the open-loop buck converter with 86 V input voltage switching at 1 MHz PWM. The dV/dt in this scenario is 85 V/ns.

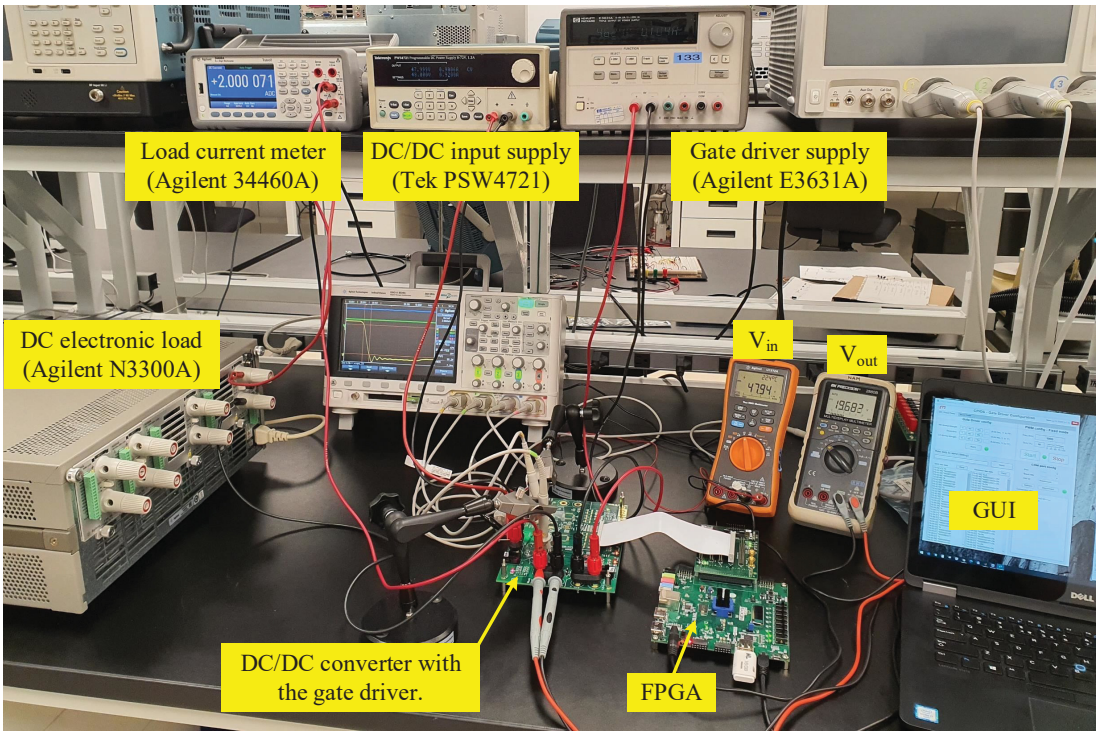


Figure 4.3 Test-bench of open-loop buck converter built with the gate driver

Figure 4.6 demonstrates the capability of on-the-fly configuration while PWM is running. This feature can be used for EMI optimization.

4.4 Conclusion

The universal and configurable gate driver for GaN half-bridges in the context of SiP is verified by measurement in this chapter. It can control a range of GaN devices (1–5.3 nC gate charge) with configurable speeds and DT without extra components. The adjustable parameters make local efficiency optimization possible. This gate driver, as a standalone chip, can also serve as a platform for other works that need on-the-fly configuration of driving strength and DT.

Table 4.1 Gate driver performance summary

Performance summary			
Specification		**Simulation**	**Measurement**
Dead-time (min/step/max)		6.5/4.76/80	4.5/4.46/58
Rise-time [ns]	with EPC2012C	1.41 - 9.90	1.46 - 10.81
Fall-time [ns]		1.24 - 4.17	1.18 - 4.5
Rise-time [ns]	with EPC2010C	2.89 - 27.78	3.7 - 27.83
Fall-time [ns]		2.82 - 11.57	2.39 - 10.8
Performance comparison with commercial gate drivers			
Parameter	This work	TI LM5113	TI LMG1210
Peak source/sink current [A]	Adjustable 1.5/3.0	Fixed 1.2 / 5.0	Fixed 1.5 / 3.0
Dead-time [ns]	Digitally configurable 4.5 - 58	N/A	Configurable with external resistor
Operating voltage [V]	Simulated / Measured 200 / 86	100	200

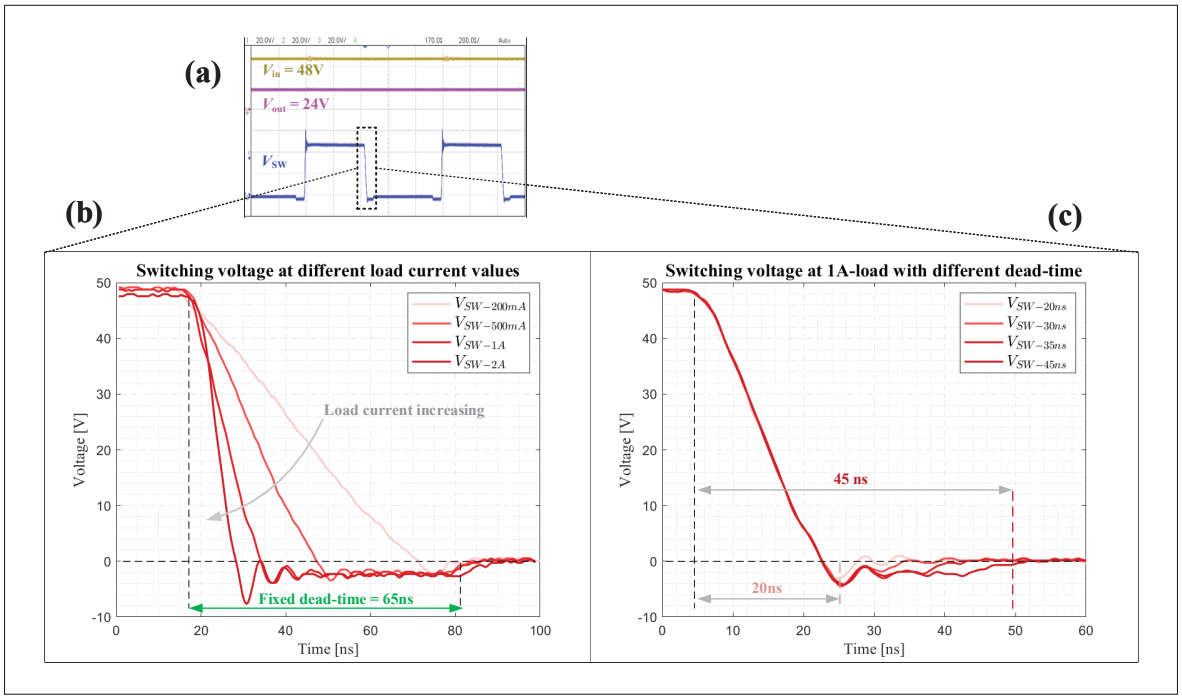


Figure 4.4 Switching node waveform with different dead-time values

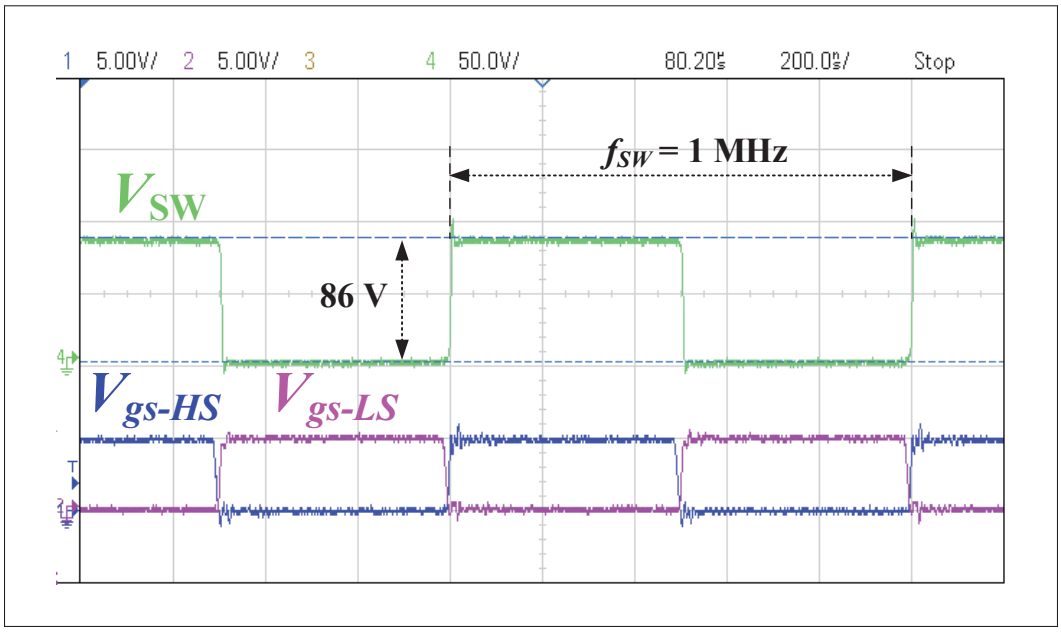


Figure 4.5 Switching at 1 MHz and 86 V input

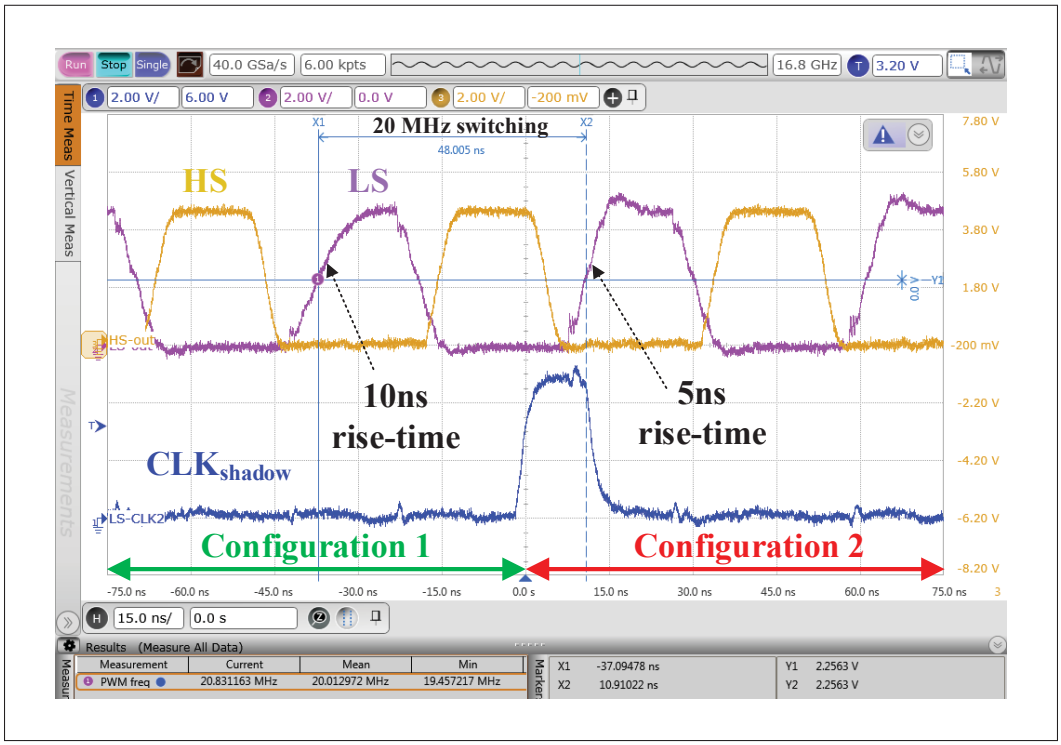


Figure 4.6 On-the-fly configuration of drive strength

CONCLUSION AND RECOMMENDATIONS

A universal and configurable gate driver for GaN half-bridges in the context of SiP is designed and demonstrated in this work. It can control a range of GaN devices (1–5.3 nC gate charge) with configurable speeds and DT without extra components. The adjustable parameters make local efficiency optimization possible. This gate driver, as a standalone chip, can also serve as a platform for other works that need on-the-fly configuration of driving strength and DT. The achieved CMTI is 226 V/ns in simulation.

Since this is the very first tape-out of XFAB XT018 technology at ÉTS, some design aspects might be overlooked. This chip can be improved as the following:

1. Optimize DT range for ultra fast GaN devices, such as min/step/max of 1/1/10 ns,
2. Make DT less sensitive to PVT,
3. Save die size with inherited bonding pad of ESD cells (requires automatic bonder),
4. Add protection blocks (UVLO, TSD, current sense).

APPENDIX I

PCB DESIGN

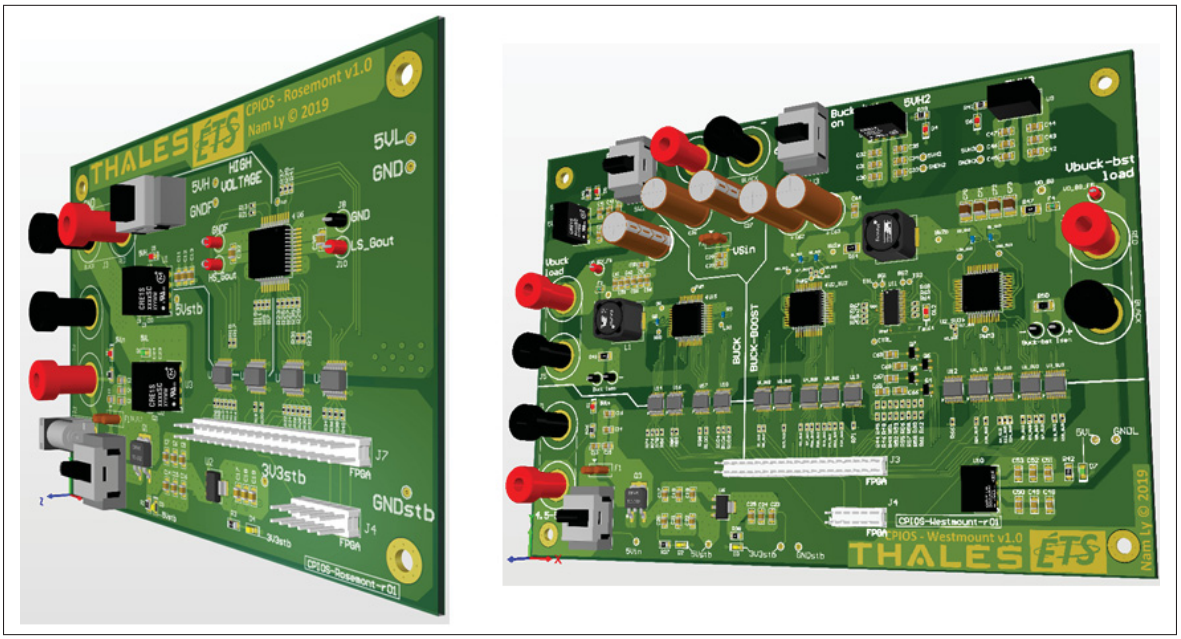


Figure-A I-1 3D view of the PCBs

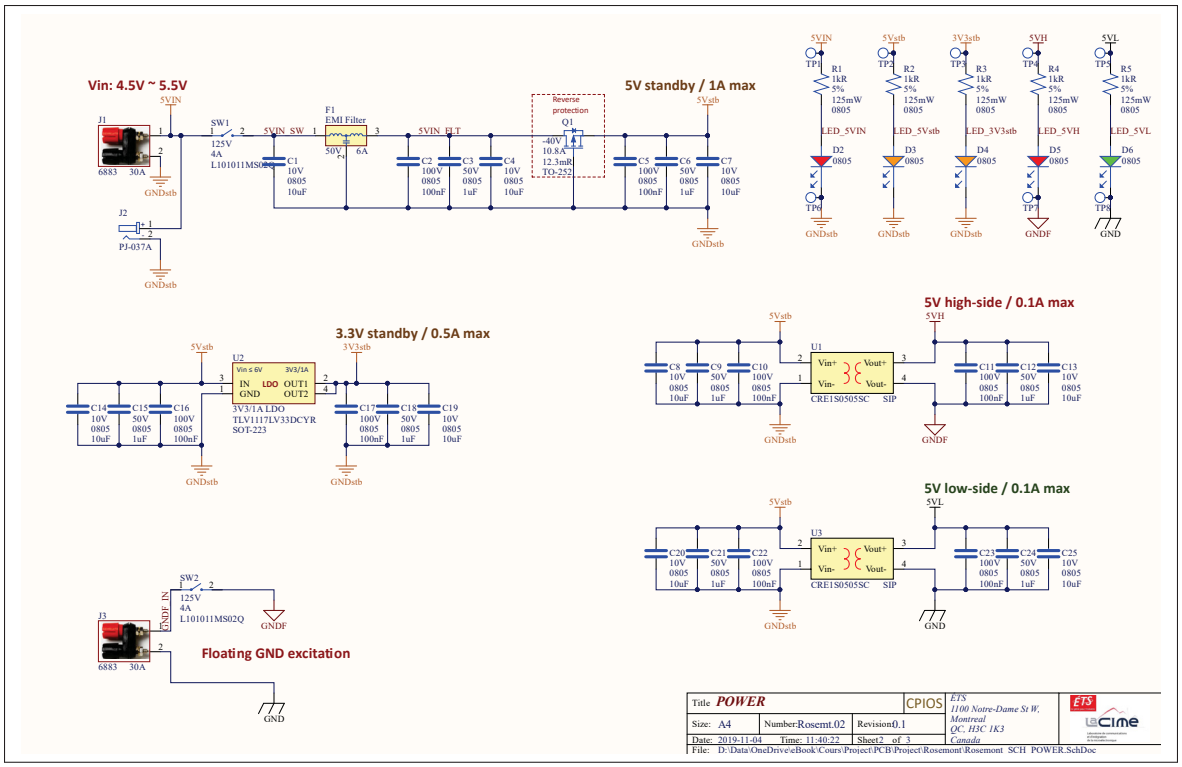


Figure-A I-2 Rosemont PCB - Schematic page 1 of 2

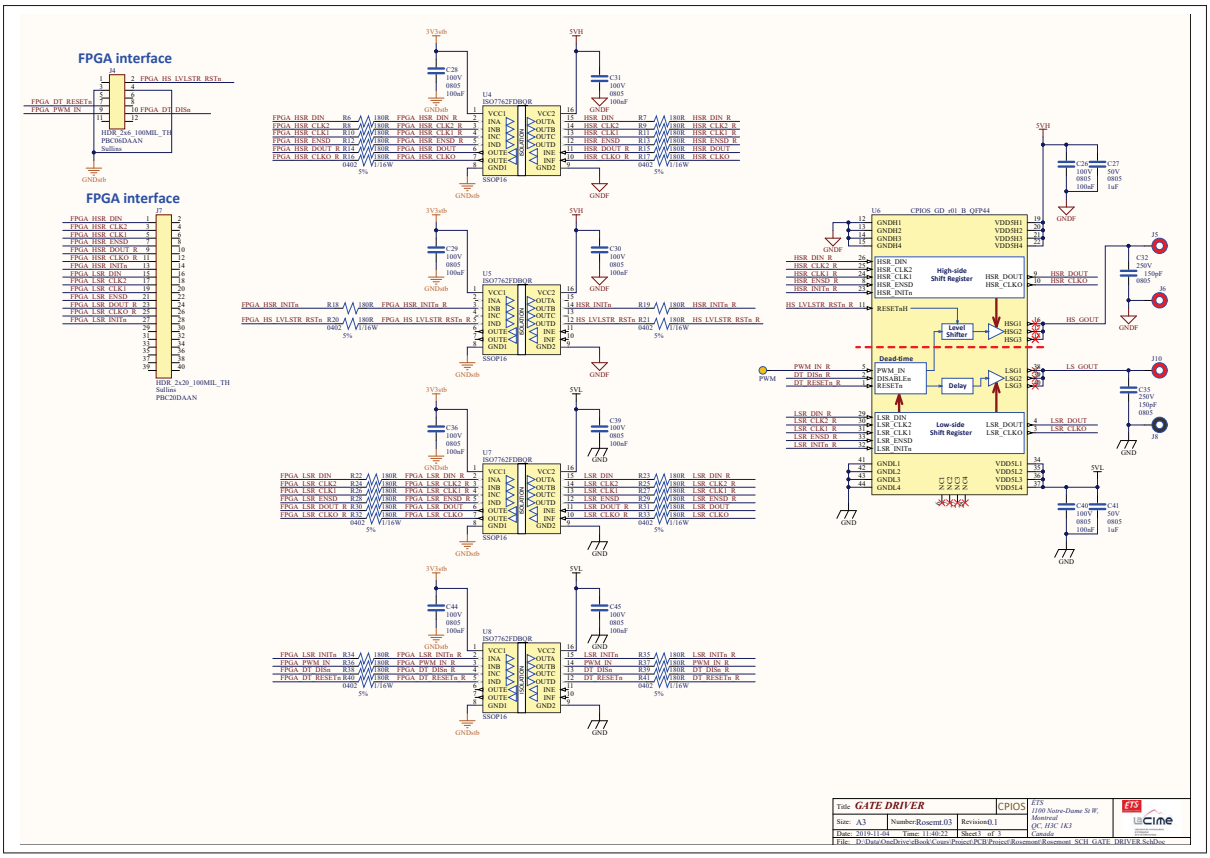


Figure-A I-3 Rosemont PCB - Schematic page 2 of 2

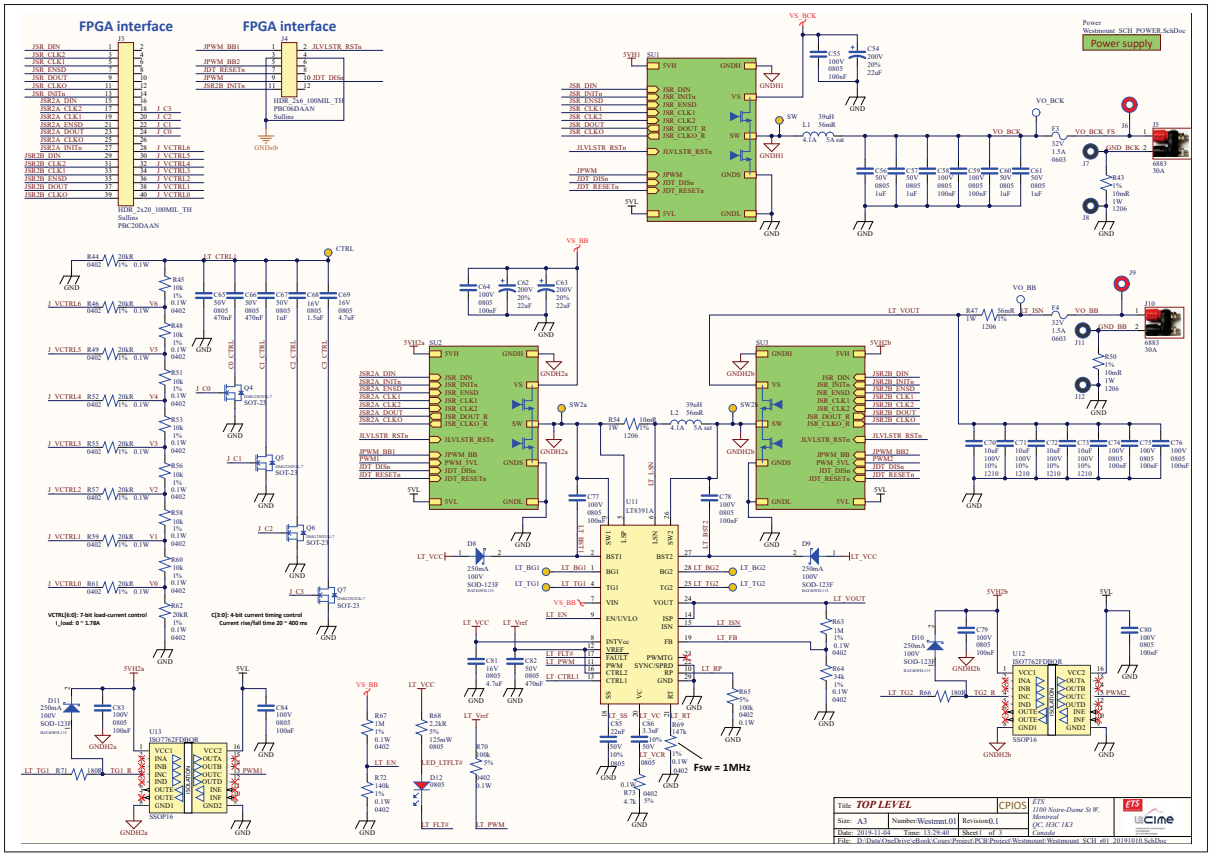


Figure-A I-4 Westmount PCB - Schematic page 1 of 5

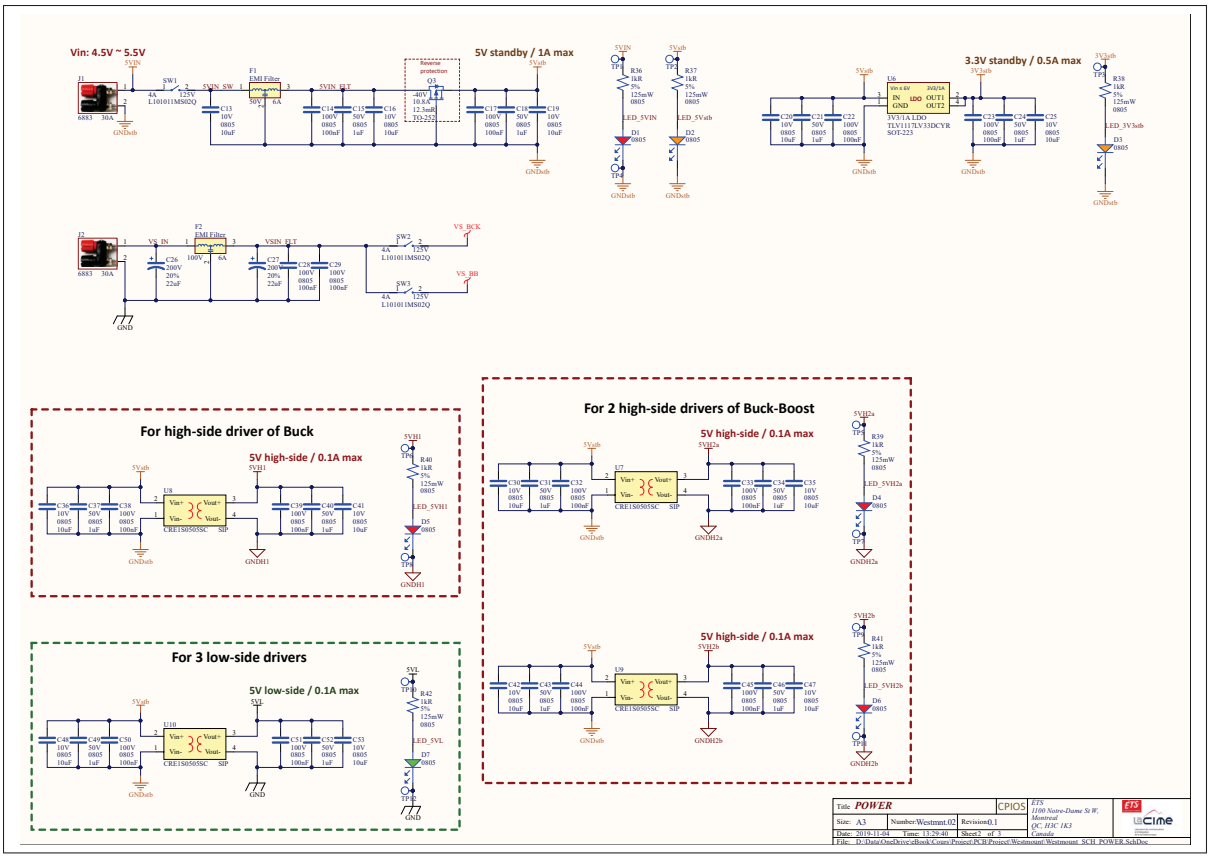


Figure-A I-5 Westmount PCB - Schematic page 2 of 5

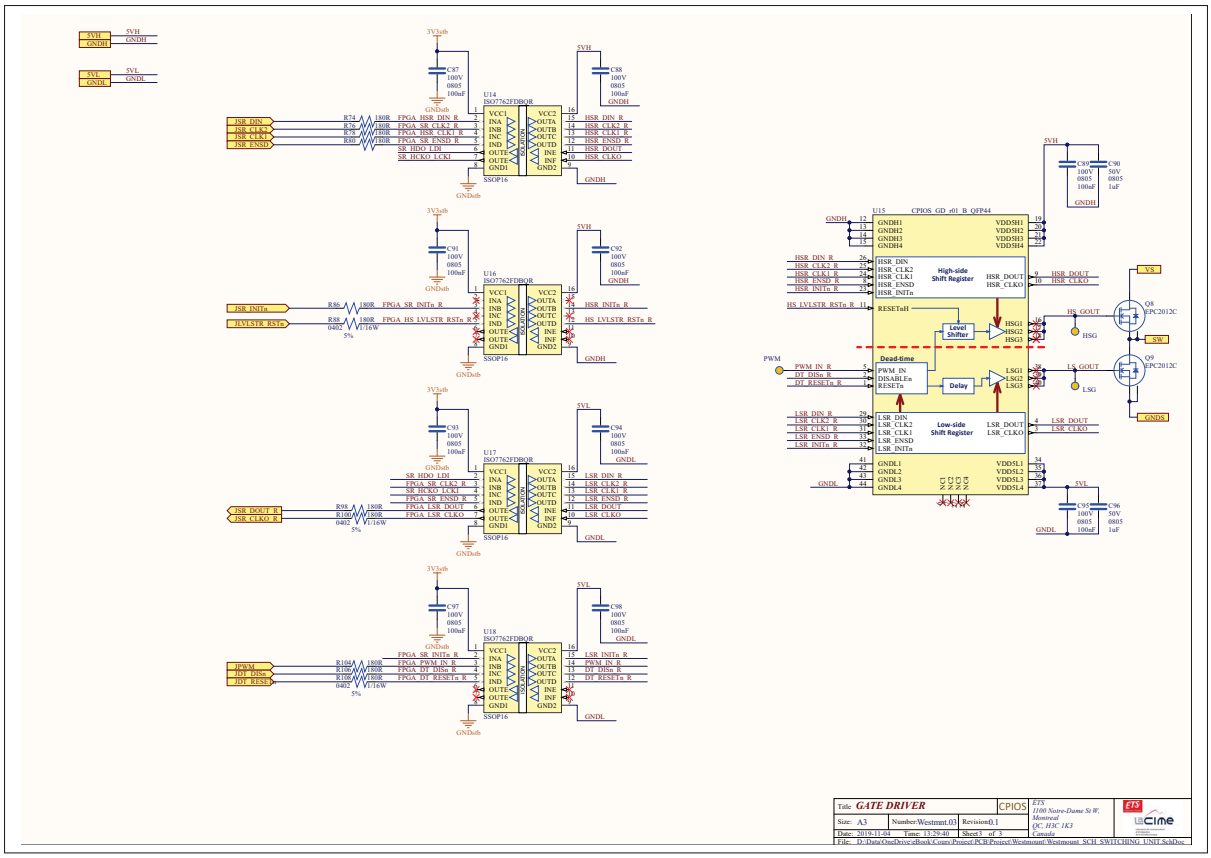


Figure-A I-6 Westmount PCB - Schematic page 3 of 5

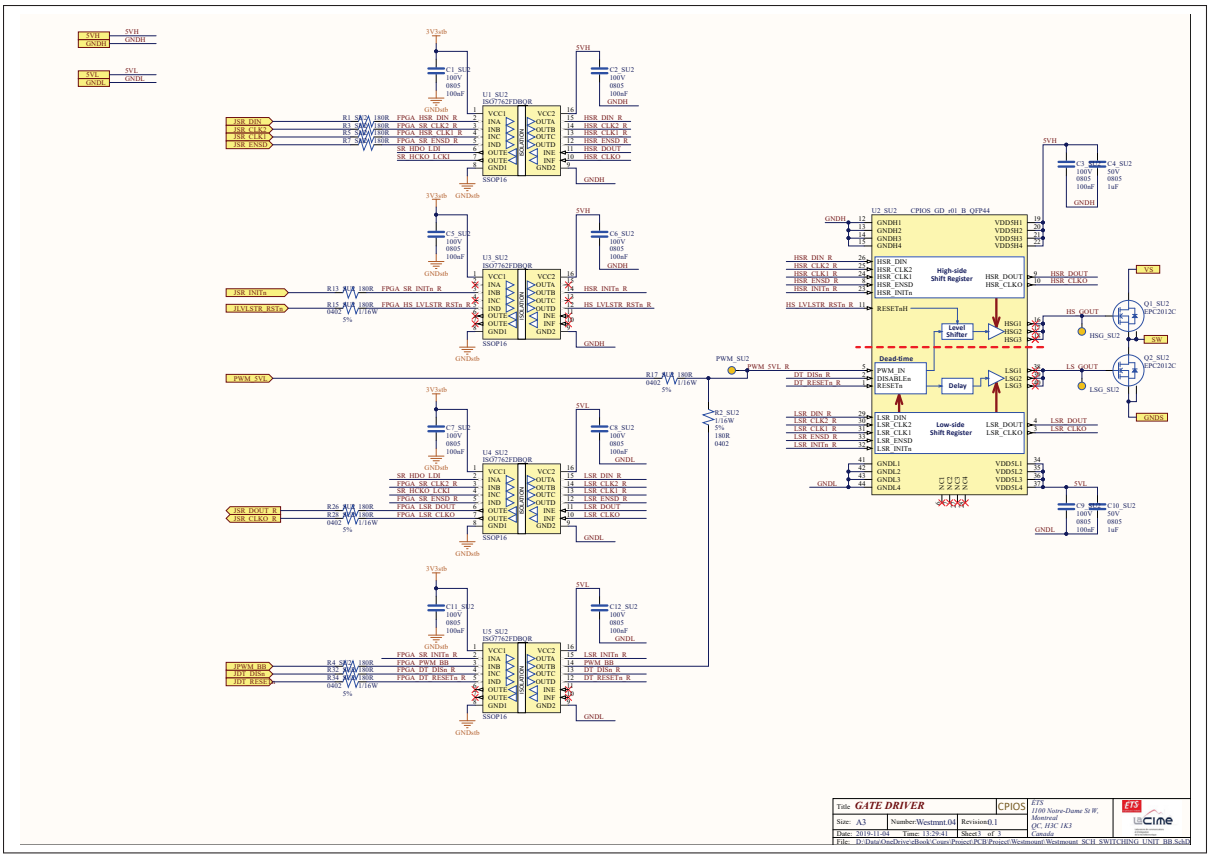


Figure-A I-7 Westmount PCB - Schematic page 4 of 5

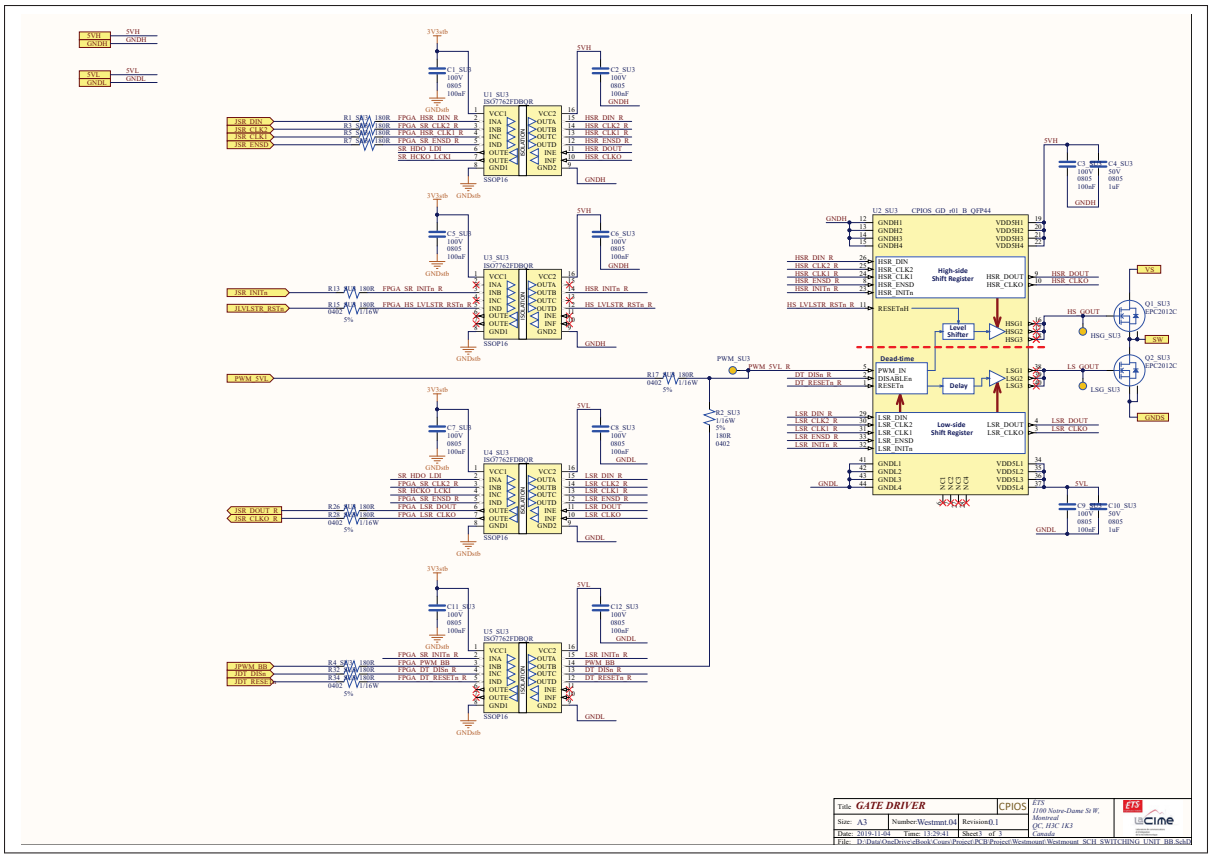


Figure-A I-8 Westmount PCB - Schematic page 5 of 5

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