Contribution to the Design of the Closed-Loop Control of a Real-Time Power Simulator

by

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FOREWORD AND ACKNOWLEDGEMENTSS

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To undertake a Ph.D. at 34 after building a family with three beautiful sons is a family decision, not just a personal one. Therefore, I thank the love of my life, Valérie, who not only gave me her support, but also encouraged me to take on this challenge. To my sons, Xavier, Alexis and Raphaël, who sometimes asked themselves why I was still going to school, I hope to have shown you the importance of finding a profession that you love. To my friends, in-laws and especially my parents, thank you for all the joy and happiness you have given me. Without you, my life would not be as balanced as it is!

Contribution à la conception de la commande en boucle fermée d'un simulateur de puissance en temps réel

OLIVIER TREMBLAY

RÉSUMÉ

Le contexte de la transition énergétique amène l'Institut de recherche d'Hydro-Québec (IREQ) à se doter d'un simulateur de puissance de 7.5 MVA afin d'y raccorder des équipements de puissance à divers réseaux électriques simulés en temps réel sur Hypersim. Ce genre de système, appelé « *power hardware-in-the-loop* (PHIL) », est une technologie émergente dans le domaine des réseaux électriques et représente encore aujourd'hui un défi de réalisation de taille. Ce défi se situe au niveau de la maîrise des signaux échangés au point d'interface entre le simulateur et l'amplificateur, ce qui constitue la principale problématique à solutionner. En effet, des délais apparaissent au point d'interface et ces derniers peuvent compromettre la stabilité de fonctionnement et/ou détériorer les performances dynamiques du système.

Dans un premier temps, une nouvelle base est établie pour comprendre la stabilité des systèmes PHIL compte tenu de leur nature hybride (analogique / numérique). En effet, la méthode conventionnelle de détermination du critère de stabilité, qui considère le système PHIL comme un modèle continu, n'est pas appropriée. Une nouvelle méthode d'évaluation de la stabilité basée sur des réponses en fréquence de l'impédance discrète est ainsi présentée.

Dans un deuxième temps, cette thèse présente une implémentation stable, robuste et précise d'une interface pour un simulateur PHIL basée sur le modèle de ligne de transmission Bergeron (BTLM). Deux limites de cette interface sont identifiées et des stratégies correctives sont formulées afin de garantir sa compatibilité avec l'application PHIL. Des analyses de stabilité, de passivité et de précision sont ensuite réalisées pour vérifier ses performances. L'interface proposée est par la suite implantée dans un banc d'essai PHIL expérimentale de 3 kVA, conçu et réalisé à l'IREQ. Plusieurs tests sont effectués afin de démontrer la stabilité et la précision du système en boucle fermée dans un large éventail de conditions de fonctionnement et avec divers équipements testés.

Troisièmement, le banc d'essai PHIL est exploité pour caractériser des onduleurs photovoltaïques résidentiels connectés à un réseau de distribution typique. Une méthode d'agrégation est d'ailleurs développée pour obtenir des paramètres d'essais réalistes. Les essais en boucle fermée ont permis de révéler des anomalies de fonctionnement lorsque ces onduleurs sont connectés à des réseaux ayant certaines caractéristiques.

Mots-clés: Algorithme d'interface numérique, analyse de stabilité, conversion de l'énergie, FPGA, modélisation, modèle de ligne de transmission de Bergeron, simulateur de puissance, simulation numérique, simulation avec matériel de puissance dans la boucle, simulation en temps réel, systèmes discrets.

Contribution to the design of the closed-loop control of a real-time power simulator

OLIVIER TREMBLAY

ABSTRACT

The energy transition has spurred Hydro-Québec's research institute (IREQ) to acquire a 7.5-MVA power simulator that will allow for the connection of power equipment to various power systems simulated in real time on Hypersim. This kind of "power-hardware-in-the-loop" (PHIL) system is an emerging power grid technology whose implementation is still very challenging. The main challenge revolves around the control of the signals exchanged by the simulator and the amplifier at their point of interface. More specifically, delays that occur at the interface may compromise the operating stability or dynamic performance of the system.

First, a new basis has been established to understand the stability of PHIL systems in light of their hybrid (digital-analog) nature. The conventional method for determining stability criteria is not appropriate as it assumes a continuous model of PHIL systems. A new stability analysis method based on the discrete impedance frequency response is thus presented.

Second, this dissertation presents a stable, robust and accurate interface for PHIL simulator based on the Bergeron transmission line model (BTLM). Two limitations of this interface are identified, and corrective strategies are formulated to ensure its compatibility with the PHIL application. Stability, passivity and accuracy analyses are then performed to verify its performance. The proposed interface has been implemented in a 3-kVA experimental PHIL test bench designed and built at IREQ. Several tests have been performed to demonstrate the stability and accuracy of the closed-loop system for various pieces of equipment under a wide range of operating conditions.

Third, the PHIL test bench was used to identify the characteristics of residential photovoltaic inverters connected to a typical distribution system. An aggregation method was developed to develop realistic testing parameters. Close-loop testing revealed operating anomalies that occur when such inverters are connected to certain types of power systems.

Keywords: Bergeron transmission line model, digital simulation, discrete-time systems, energy conversion, FPGA, interface algorithm, modeling, power hardware-in-the-loop simulation, power simulator, real-time systems, stability analysis.

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LIST OF ABBREVIATIONS

AC	Alternating current
ADC	Analog-digital converter
BTLM	Bergeron transmission line model
CEPRI	China Electric Power Research Institute
CPU	Central processing unit
CHIL	Control hardware-in-the-loop
DAC	Digital-analog converter
DC	Direct current
DER	Distributed energy resources
DIA	Digital interface algorithm
DIM	Damping impedance method
DT	Dead time
DUT	Device under test
EGRID	Duke Energy Electrical Grid Research Innovation and Development
EMT	Electromagnetic transient
FOH	First-order hold
FPGA	Field programmable gate array
FRT	Frequency ride through
FSU-CAPS	Florida State University Center for Advanced Power Systems
HIL	Hardware in the loop
HVRT	High voltage ride through
IREQ	Institut de Recherche d'Hydro-Québec
ITM	Ideal transformer method
LVRT	Low voltage ride through
NREL	National Renewable Energy Laboratory
OFCIE	Output filter characteristic impedance emulator
PA	Power amplifier

PCD	Partial circuit duplication
PHIL	Power hardware in the loop
PLL	Phase-locked loop
POC	Point of connection
PV	Photovoltaic
PWM	Pulse-width modulation
RMS	Root mean square
ROS	Rest of system
RTE	“Réseau de transport d’électricité” (power transmission system)
RTS	Real-time simulator
SCC	Short-circuit capacity
SCR	Short circuit ratio
TFA	Time-variant first-order approximation
TLM	Transmission line model
VSC	Voltage source converter
ZOH	Zero-order hold

LIST OF SYMBOLS AND UNITS

UNITS USED

A	Ampere
C	Coulomb
°	Degree
dB	Decibel
F	Farad
H	Henry
Hz	Hertz
kA	Kiloampere
kV	Kilovolt
kW	Kilowatt
MW	Megawatt
MVA	Megavolt-voltampere (apparent power)
Ω	Ohm
rad	Radian
s	Second
V	Volt
VA	Voltampere (apparent power)
W	Watt

SYMBOLS USED

C	Transmission line capacitance
C_f	Output filter capacitance
F_{sw}	Switching frequency
F_{swe}	Effective switching frequency
G	Transmission line conductance
I_1	Current left of separation point
I_2	Current right of separation point

i_{PA}	Power amplifier output current
i_s	Current on the emitting side of the transmission line
i_r	Current on the receiving side of the transmission line
K_{at}	Wave attenuation factor
l	Length
L	Transmission line inductance
L1	Power system side inductance
L2	Equipment side inductance
L_f	Output filter inductance
L_{EQ}	Equivalent inductance of test bench
L_{HQ}	Equivalent inductance of Hydro-Québec laboratory electrical outlet
R	Transmission line resistance
R1	Power system side resistance
R2	Equipment side resistance
R_f	Output filter resistance
R_{EQ}	Equivalent resistance of test bench
R_{HQ}	Equivalent resistance of Hydro-Québec laboratory electrical outlet
s	Laplace variable
V_1	Voltage left of separation point
V_2	Voltage right of separation point
V_f	Voltage drop due to amplifier internal resistance
V_{LL}	Line-to-line RMS voltage
V_s	Equivalent power system voltage
v_d	Equipment (DUT) side voltage
v_s	Transmission line emitter side voltage
v_r	Transmission line receiver side voltage
τ	Time constant
t	time
T	Sampling period
Ts	RTS sampling period

u_s	Forward wave
u_r	Backward wave
w_s	Backward wave (sending end)
w_r	Forward wave (receiver end)
x	Distance
Y_{DUT}	ROS side admittance
z	Discrete Laplace variable
Z_C	Characteristic impedance
Z_{EQ}	Equivalent impedance of test bench
Z_{DUT}	DUT side impedance
Z_{ROS}	ROS side impedance
Z1	Power system side equivalent impedance
Z2	Equipment side equivalent impedance

INTRODUCTION

Renewable energy integration, energy storage, emerging smart grids and ground transportation electrification are bringing new equipment onto power systems and new ways of operating it. Most of the new equipment includes power electronic converters and sophisticated control systems. Large-scale deployment of such new technologies on the transmission and distribution systems is presently limited by the ability of public utilities to validate their compliance with grid connection requirements, resilience, stability, compatibility and interoperability with other grid equipment.

To ensure a smooth integration of these new technologies and new future-grid operating modes, it no longer is sufficient to use the conventional approach, which consists in testing equipment and/or operating modes individually. A comprehensive approach is required whereby the system can be tested as a whole. The entire system means the actual physical equipment (e.g. microgrids, distributed generation equipment and storage), control systems (e.g., microgrid controllers), protection systems and the main power system. New means of testing must be developed, including cutting-edge simulation and testing techniques such as power hardware-in-the-loop (PHIL) and control hardware-in-the-loop (CHIL) (de Jong et al., 2012). Whereas CHIL simulation methods are well known and have been tested for a number of years, PHIL simulation techniques are the focus of ongoing research due to closed-loop operating stability issues.

Drivers

Hydro-Québec's research center (IREQ) already owns, continuously develops and operates a 25-kV (overhead and underground) distribution test line that includes energy storage, a diesel generator, various loads and a microgrid controller (Abbey, Brissette, Ouellet, & Zavoda, 2010; Awan, Abbey, Brissette, & Joós, 2014; Kleimaier, Brissette, Abbey, & Joós, 2013). IREQ also owns, develops and operates the Hypersim real-time power system simulator (Do, McCallum, Giroux, & De Kelper, 2001; Do et al., 1999; Paré, Turmel, Soumagne, & Casoria,

2003), marketed by Opal-RT Technologies Inc. The simulator is currently being used for CHIL testing (Sybille et al., 2010). The experimental test line and the Hypersim simulator are two separate facilities that are currently operated independently. Leveraging both of these large-scale facilities, Hydro-Québec is currently building a new PHIL/CHIL research and testing facility that will allow for the modeling of experimental transmission and distribution (T&D) systems. The new facility created by connecting the test line to the Hypersim simulator will greatly enhance IREQ's testing capacity. It will for example be used to develop and validate future grid technologies.

To create this new facility, it will be necessary to design a dedicated power amplifier and develop an algorithm to interface this amplifier with the Hypersim simulator. This dissertation focuses on this last point, i.e. the development of a high-performance control interface between the simulator and the power amplifier that fully leverages the capacities of both components.

Operating principle of IREQ's PHIL facility

To help readers, a simplified illustration of the new IREQ facility is shown in Figure 0.1. The new facility comprises the 25-kV distribution test line located on IREQ's campus, the Hypersim simulator and a 7.5-MVA amplifier with no output transformer. The interface between the test line and the simulator will be provided by the power amplifier, based on a multicellular converter, as well as the closed-loop control algorithm, which is the main topic of this dissertation. The closed-loop system comprised of the Hypersim simulator and the power amplifier is called a "power simulator" ("SimP"), whose operating principle is described below.

The simulator calculates in real time the instantaneous voltage (Vsim) to be applied to the line. The amplifier boosts the voltage to the desired value and applies it to the line. At the same time, the line current is measured (Imes) and injected into the simulator thus achieving closed-loop operation. In this operating mode, the test line is virtually connected to the simulated power grid.

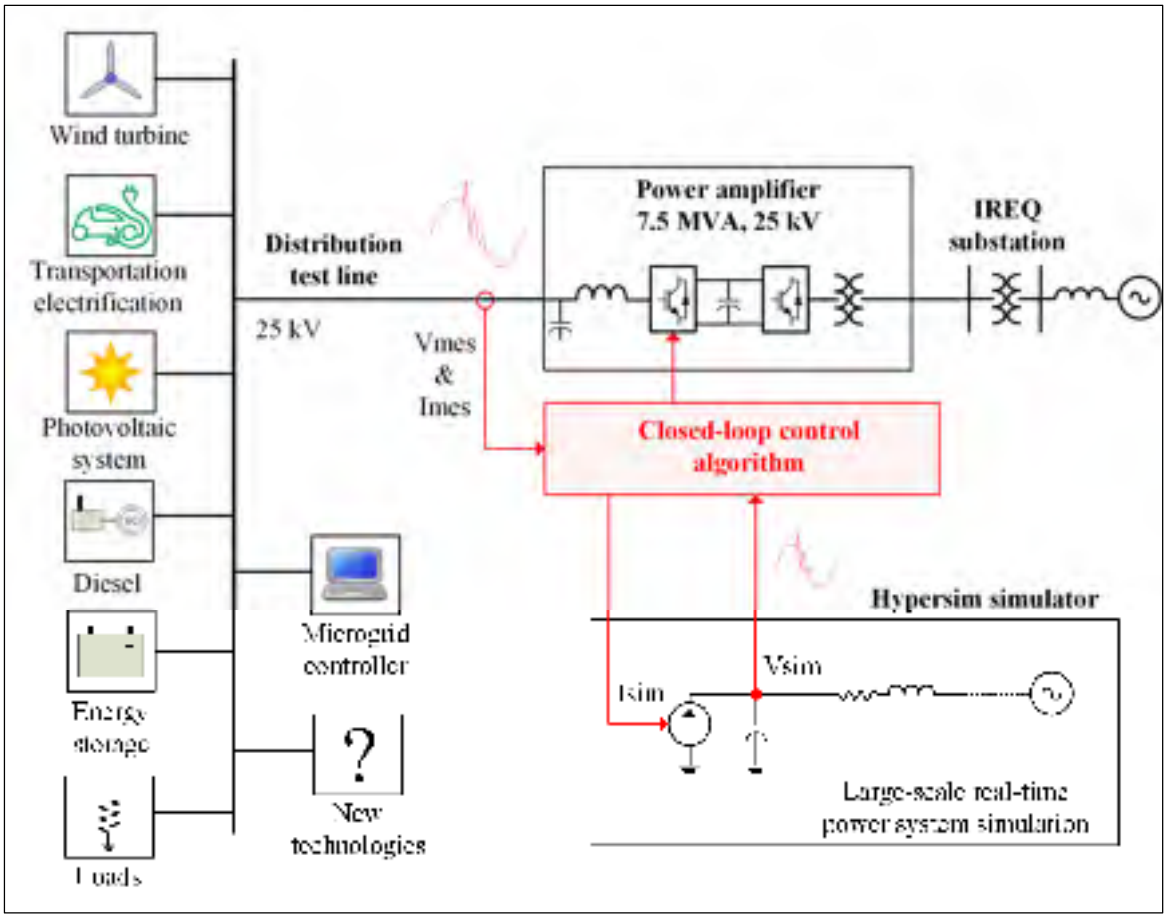

Figure 0.1 Illustration of the SimP research and testing facility

Using SimP will greatly enhance the line's test capabilities. The use of a simulated power system rather than an actual one will allow for the simulation of a variety of system conditions. It will be possible, for instance, to produce voltage dips and surges, generate realistic grid transient voltages at frequencies ranging from 0 Hz (DC) to a several kHz, study the impact of the grid on equipment connected to the line and study the impact of that equipment on the simulated grid. Using SimP will also make it possible to connect the test line to any grid by implementing the grid's simulation model in Hypersim. For example, the test line with its distributed generation equipment could be connected to any power system in the world. Manufacturers will, for instance, be able to use the new facility to develop and test the operation of various devices through a virtual connection to this simulated grid. Lastly, the proposed world-class research/testing facility will be unique in Canada. It will support

unprecedented tests that will help develop and validate future grid technologies, thus promoting the integration of renewable energy sources into power systems and enhancing research into the decarbonization of power generation.

Problem to be addressed (CHIL vs. PHIL)

Real-time hardware-in-the-loop (HIL) simulation consists in interfacing the actual equipment with a power system simulation model. Delays occur when signals are exchanged by the systems, mainly due to the real-time simulator (RTS) and the conversion between the digital (simulator) and analog (actual equipment) worlds. HIL systems can be divided into two broad categories. First, there are CHIL (or controller HIL) systems, where the actual equipment is a control system. The delays applied to the CHIL system do not create any special problem as the two systems are naturally decoupled. The equations used to simulate the electrical system are not instantaneously coupled with the control system, thus facilitating the decoupling. In the case of PHIL (power HIL) systems, the physical system under study is divided in two parts: an actual, physical part and a simulated part. It is this division that gives rise to the delays that break the simultaneity needed for the system to operate properly since the simulated equations cannot be solved instantaneously based on the electrical measurements made on the equipment. This is the fundamental problem with PHIL systems.

To illustrate the effect of these delays, consider the simplified electric circuit shown in Figure 0.2, comprising a source and two impedances. In this circuit, the current through impedance Z2 is the same as the current through impedance Z1.

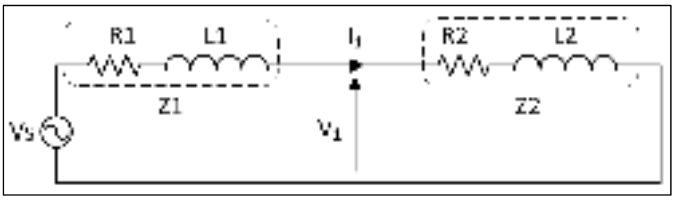

Figure 0.2 Original simplified electric circuit

In a PHIL system, this electric circuit is deliberately divided in two: one part of the circuit (called “rest of system” or ROS) is modeled by a real-time simulator, while the other part of the circuit is the actual power equipment being tested (called “device under test” or DUT). One intuitive method for implementing this circuit separation is called the ideal transformer method; it consists in measuring the voltage and current on both sides of the separation point, then injecting these signals using controlled sources, as shown in Figure 0.3. If the signals were exchanged instantaneously, I_1 would be strictly equal to I_2, and the same thing would hold for V_1 and V_2. The PHIL circuit would then behave exactly like the original circuit (prior to separation).

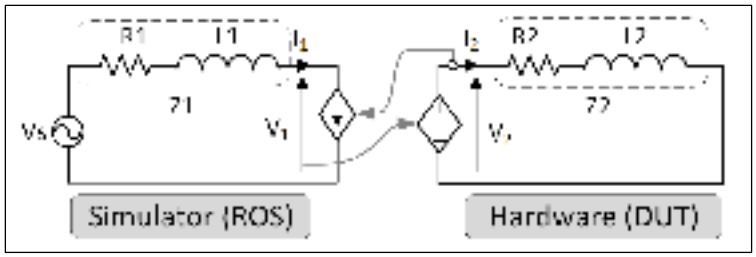

Figure 0.3 Simplified PHIL system electric circuit

However, in practice, the exchange of signals between the two parts of the circuit cannot take place instantaneously, mainly due to communication, conversion and simulation delays as shown in Figure 0.4. These delays make it impossible for the currents and voltages on either side of the separation point to be equal, thus decoupling the system (which should normally remain coupled).

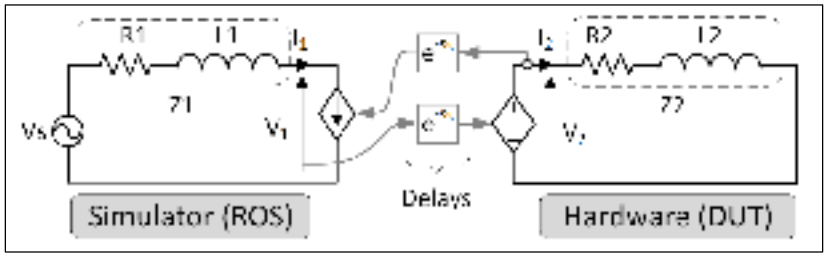

Figure 0.4 Practical implementation of a PHIL system

These delays alter currents and voltages, thus degrading the accuracy of results. They can also lead to system instability. Such instability could permanently damage the equipment under test and the power amplifier. To study the stability problem, it is possible to use the closed-loop block diagram in the Laplace domain, shown in Figure 0.5.

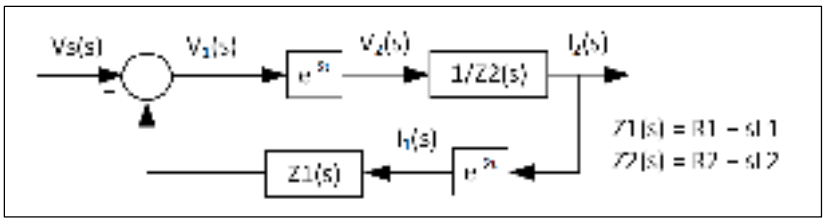

Figure 0.5 Closed-loop block diagram of PHIL system

An analysis of the stability of systems that include delays has demonstrated that this system becomes unstable for any delay (τ) greater than 0 when the magnitude of Z1(s) is greater than the magnitude of Z2(s) (M. H. Hong, S. Miura, Y. et al., 2009).

This potential instability due to interface delays is the main issue for PHIL systems as it considerably limits the operating range of such systems. For example, it is impossible to simulate power systems with low short-circuit capacities, islanded power systems or systems that contain supply disconnect switches. Furthermore, generating equipment under test generally includes an impedance that may be relatively low compared to the power system impedance. The development of higher performance digital interface algorithms (DIAs) is therefore necessary to achieve this high level of flexibility.

In the past, several DIAs were developed to mitigate the problems associated with the interface between the simulator and the power hardware. However, as the literature review will show, the range of validity of these digital interface algorithms is too limited to allow for the accurate modeling of complex and varied equipment as is the case for the SimP simulator.

Goal of thesis

The main goal of this thesis is to design a PHIL interface that is stable and accurate over a wide range of applications, independently of the equipment or power systems being simulated. The new digital interface algorithm (DIA) will need to be compatible with a 7.5-MVA @ 25-kV amplifier (i.e. high power electronics), with a large scale real-time simulation (based on the CPU technology) and with the connection of complex equipment. This DIA will also need to be implemented and validated experimentally on a reduced scale test bench.

The sub-goals of this thesis are:

1. Develop a new stability analysis method for PHIL systems that incorporates the notion of a hybrid system (analog-digital).
2. Design and build a reduced scale experimental test bench (3 kVA, 208 V_{LL}) to replicate the behavior of the full-scale system (7.5 MVA @ 25 kV).

Contributions and spinoffs

The main contribution of this thesis is the full overall design of a PHIL system, including all constraints up to and including its implementation using industrial hardware and its use in power system studies. This includes the development of a method to better understand the mechanisms that lead to PHIL system instability and mitigation measures, the development of a DIA adapted to the typical, rigorous uses of such systems at IREQ, and the development and validation of an experimental PHIL test bench.

This work has been published in two peer-reviewed journals. Published in *IET Generation, Transmission and Distribution,* the first article deals with the analysis of the stability of PHIL systems (Tremblay, Fortin-Blanchette, Gagnon, & Brissette, 2017). Published in *IEEE Transactions on Energy Conversion*, the second article describes the development and experimental validation of a new method for interfacing PHIL systems (Tremblay, Rimorov, Gagnon, & Fortin-Blanchette, 2020). In addition, this work has been presented three times at

international conferences on PHIL systems (Tremblay, Gagnon, Giroux, & Slimani, 2015; Tremblay et al., 2018; Tremblay, Slimani, et al., 2017).

Finally, given the availability of the test bench developed through this work and the performance of the new DIA, the PHIL test bench was used to carry out a study on the transient response of residential photovoltaic inverters. This spinoff is a practical application of the method developed (Rimorov et al., 2020).

Methodology

The methodology used to complete this thesis work can be divided in four main stages:

1. Modeling and simulation: A simulation environment capable of modeling complex systems is essential to properly understand the phenomena under study and develop new DIAs. Therefore, the environment provided by *MATLAB/Simscape Electrical Specialized Power Systems (SPS)* has been used to model and simulate the PHIL electric circuits and digital interface algorithms (DIAs) presented in this thesis.
2. Digital interface algorithm (DIA) development: The PHIL system stability analysis methods and the new DIAs can then be developed and improved in the simulation environment described in the first point.
3. Development and characterization of experimental test bench: Developing a test bench and mastering its operation are essential steps of the experimental validation process. It is therefore necessary to characterize the whole system, including its power amplifier, output filter, simulator, inputs-outputs, and field-programmable gate array (FPGA). This allows for the proper implementation of the DIA on the FPGA while taking into consideration all the system constraints.
4. Experimental validation: Experimental results (including tests on simple DUTs, such as passive loads, or more complex ones, such as a power system connected to photovoltaic inverters) will be compared with simulated cases to ensure the system is operating properly.

Thesis structure

To achieve the goals described above, this thesis is divided into seven chapters. The first chapter describes the typical environment in which a PHIL system is used, then reviews currently available DIAs. A new stability analysis method for PHIL systems that incorporates the notion of a hybrid system is then described in detail. The third chapter describes the exploratory attempts to develop a more performing DIA. Chapter four covers the development and validation of a new DIA suited to the IREQ environment. Chapter five describes in detail the experimental test bench specifically developed to implement a proof-of-concept version of the new DIA. Chapter six presents the experimental validation results obtained using the test bench and compares them with reference models. The seventh and last chapter describes how the PHIL system developed for this thesis was used by Hydro-Québec to study the transient response of residential photovoltaic inverters. Finally, concluding remarks and recommendations for future work are presented.

CHAPTER 1

BACKGROUND AND LITERATURE REVIEW

PHIL type simulations are increasingly being used in power system research due to the increased availability of real-time simulators and the growing capacity of amplifiers, on one hand, and the need to test increasingly complex equipment prior to their installation on the grid, on the other hand. The scientific community has yet to offer a general solution to the stability and accuracy problem that arises at the simulator-amplifier interface. It is therefore unsurprising to note the literature contains many articles on various interface methods and how they have been adapted to specific conditions. This chapter starts by defining the testing capabilities that a PHIL simulator should possess and assessing the ability of the main DIAs currently described in the literature to perform these tests. This chapter then reviews the technologies used by the main actors in the field of high-power PHIL systems (i.e. MW-order systems).

1.1 Real-time simulator and CHIL/PHIL applications

HIL (hardware-in-the-loop) simulation is widely used to validate the operation of hardware in a realistic simulated environment. Using this method, hardware can be tested under various scenarios that are generally not available under normal operating conditions. In power system research, HIL simulation allows for the testing of equipment under various grid contingencies. This enables the testing of equipment to ensure it operates properly prior to its commissioning, its testing under extreme operating conditions, the development of new functionalities, the training of future system operators and many more applications. There are two major families of HIL systems: those that only use the control module (controller HIL or “CHIL”) and those that use a control system integrated with their electrical power system (power HIL or “PHIL”).

The Hypersim simulator is mainly used to carry out CHIL type tests where the actual power equipment control system is connected to a simulated power system, as shown in Figure 1.1. The simulated model then includes the power circuitry of the equipment as well as the power

system to which the equipment is normally connected. This operating mode makes it possible to study the closed-loop dynamic performance of the actual control system of the equipment connected to its grid.

Typical applications include studies to validate the performance of protection relays, static VAR compensators and synchronous condensers control systems, as well as HVDC interconnections.

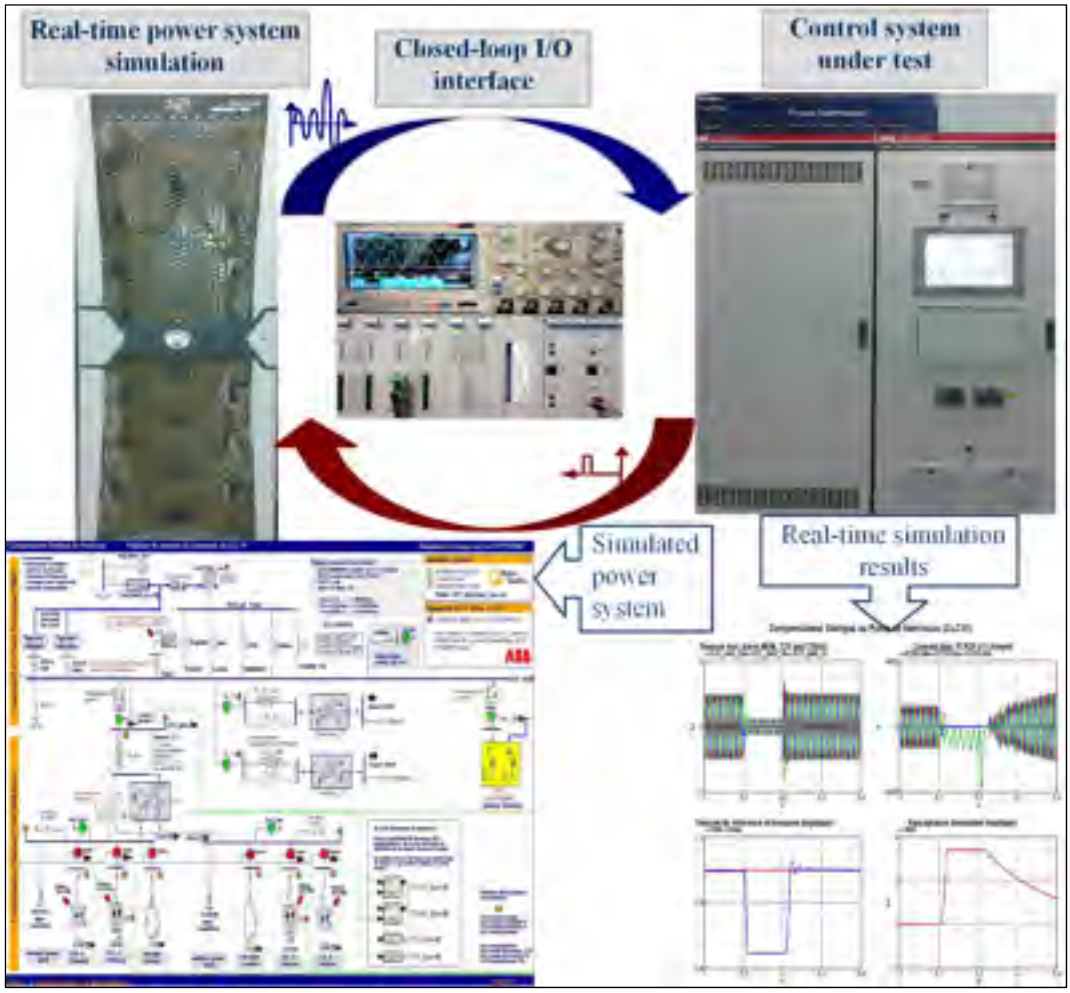

Figure 1.1 Sample simulation using controller hardware-in-the-loop (CHIL) system

The emergence of distributed energy resources (DERs) has changed the way equipment is tested. In these systems, electrical energy is generated using wind turbines and photovoltaic

panels, connected to energy storage systems, through power electric converters driven by advanced control systems. These converters can also provide ancillary services to the power grid, thus contributing to voltage and frequency regulation. In this kind of equipment, it is very difficult to dissociate the control system from its power circuitry, thus making CHIL testing especially difficult. In addition, it is sometimes impossible to develop the model required for CHIL testing as manufacturers (who often act as component assemblers) may not have detailed knowledge of the power circuitry.

To ensure the proper operation of these complex systems, it is necessary to carry out tests that consist in connecting the power equipment directly to a simulated grid in what is known as a PHIL system. The PHIL approach thus has the benefit of enabling the testing of equipment as a whole and not only its control system.

1.2 Typical uses of a PHIL system

Before developing or adapting a DIA for PHIL testing, it is necessary to define its typical uses, i.e. the types of tests that are to be performed and the hardware that may be tested. The DUT may be any electrical equipment, ranging from a simple passive load (e.g. resistive, inductive, capacitive or any combination of the three) to a more complex component (e.g. wind turbine, photovoltaic system or energy storage system, based on voltage-source converters). Furthermore, the DUT may consist in a combination of various interconnected components that form a complex distribution network.

The types of tests to be performed include tests that focus on the DUT's response to grid events, including low voltage ride through (LVRT), high voltage ride through (HVRT) and frequency ride through (FRT). These tests can be performed using any programmable voltage source, in an open-loop configuration where only the programmed voltage is applied to the equipment. However, under this kind of scenario, the interaction between the DUT and the power grid cannot be modeled, thus making it impossible to study phenomena such as voltage/VAR compensation or the effect of equipment inertial response on the grid frequency. Therefore, to

carry out more comprehensive studies, it is necessary to simulate a representative power grid and the DUT's response must be injected into the simulation through a closed-loop configuration. Examples of cases where closed-loop testing is required are provided below:

- DUT connected to a power grid with a low short-circuit ratio (SCR less than 10) [1].
- Testing in islanded mode, where the DUT only supplies power to local loads.
- Control tests of interactions between the DUT and the power grid to which it is connected.
- Ancillary service testing.

A digital interface algorithm (DIA) capable of handling all these tests is therefore essential. In addition, the selected DIA will need to ensure system stability without affecting the accuracy of results for all test cases.

1.3 Literature review and assessment of existing digital interface algorithms

This section provides an overview of the digital interface algorithms (DIAs) currently found in the literature. Each algorithm is assessed with respect to its ability to perform the tests listed in the previous section.

1.3.1 Ideal transformer method (ITM)

The ideal transformer method (ITM) described in the introduction is the most direct approach and the simplest one to implement (Brandl, 2017). On the other hand, two major constraints make its use difficult (M. Hong, Horie, Miura, Ise, & Dufour, 2009):

1. As mentioned above, to maintain stability, the equipment side inductance (L2) must always be greater than the sum of the simulator side series inductances, regardless of the interface delay.

[1] The short-circuit ratio (SCR) is defined as the ratio between the short-circuit capacity of the power system at the connection point and the rated capacity of the DUT.

2. A small delay (~1µs) promotes stability, while a large delay (~1ms) creates additional constraints on system impedance.

These constraints are incompatible with the PHIL approach since this DIA can become unstable, for example when an active DUT (i.e. one that supplies power) is connected to a power system that is islanded from the main system due to a switching operation. In this example, since the ROS impedance is greater than the DUT impedance, the system is unstable.

1.3.2 Partial circuit duplication (PCD)

Since the power grid is in general connected to the DUT through an impedance (Zab), it may be interesting to duplicate this impedance on both sides of the interface, as shown in Figure 1.2 (Paran, 2013). In this method, called partial circuit duplication (PCD), the voltages at each end of the impedance are exchanged with a delay of one simulator calculation step.

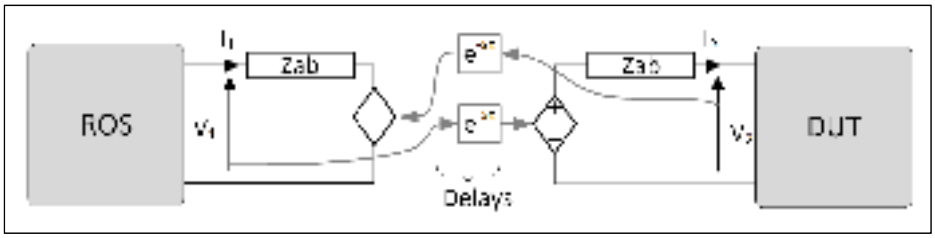

Figure 1.2 Partial circuit duplication

This technique has been used for over 30 years to decouple large calculation tasks in digital simulators. Off-line simulators, such as SPICE (Newton & Sangiovanni-Vincentelli, 1983), rely on this technique, which is based on relaxation, to separate the matrix of a large electrical system into several decoupled subsystems. Together with an iterative method, the solution obtained approaches the undecoupled system response (Dmitriev-Zdorov, 1996). For real-time simulators, it is very hard to achieve a sufficient accuracy due to the difficulty involved in iterating over calculation tasks (Kuffel et al., 1995). For PHIL systems, there are three problems:

1. If impedance Zab is located on the hardware side, it must be measured accurately to duplicate it on the simulator side. If impedance Zab is located on the simulator side, it must be physically inserted on the equipment side.
2. An error will be introduced since it is impossible to iterate between the two systems.

Although this DIA is stable for a wide range of operating conditions, the value of impedance Zab must be relatively large to ensure accurate results (Wei Ren, 2007), something that is not realistic for typical DUTs. In fact, the power grid is often connected to the DUT through a low impedance Zab, which is too limiting for our typical use cases.

1.3.3 Damping impedance method (DIM)

The damping impedance method (DIM) is a combination of the ideal transformer method (ITM) and the partial circuit duplication (PCD) method, with the addition of impedance Z*, as shown in Figure 1.3 (Paran, 2013).

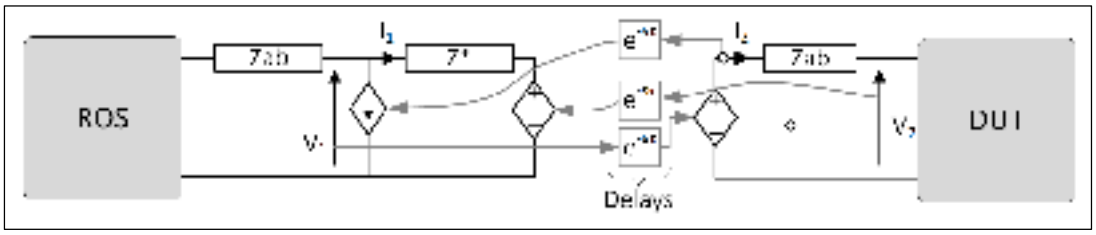

Figure 1.3 Damping impedance

For this configuration, it can be shown that if Z* is strictly equal to the DUT impedance (Z_{DUT}), the system will be absolutely stable, i.e. the error obtained at any given instant will not be cumulative (Wei Ren, 2007). In reality, measuring and "tracking" the value of Z_{DUT} can prove extremely difficult (Siegers & Santi, 2014). Although there are several methods for estimating the DUT impedance, they are difficult to use if the device is active, non-linear and/or complex (e.g. power converter).

1.3.4 Time variant first-order approximation (TFA)

The time variant first-order approximation (TFA) method is based on the principle that the actual hardware can be modeled using a first-order linear system, i.e. a RL or RC circuit (Wu, Lentijo, & Monti, 2004). By estimating the DUT parameters and using a trapezoidal approximation, it is possible to obtain the values for a, b and R_{eq} that are needed to implement the impedance in nodal form. This method is illustrated in Figure 1.4.

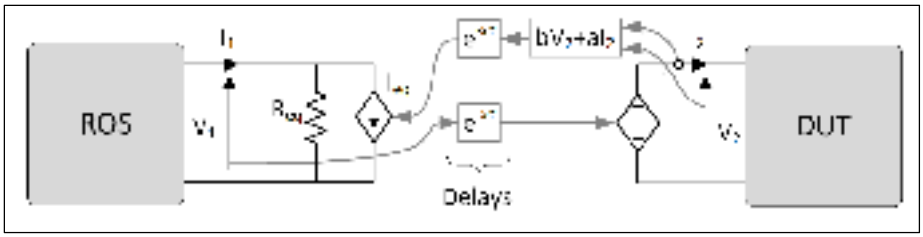

Figure 1.4 First-order approximation

Although this method is interesting since it represents the equipment using simple RL model, it is subject to several constraints (Wei, Steurer, & Baldwin, 2008) that make its use difficult in our typical use case:

1. **Accuracy**: To achieve the desired accuracy, it is necessary to measure the R and L values of the equipment to estimate the values of R_{eq}, b and a. This can be done through an on-line estimation using the recursive least-squares method, but the accuracy achieved will depend on the algorithm and the estimation noise.
2. **Instability**: The method is vulnerable to instabilities due to the inherently predictive nature of this method and the estimation algorithm. For example, an active DUT will be appear as a negative resistance, which could lead to instability.
3. **Load type (RL or RC)**: The same approach can be used for a RC load. This will result in a voltage source on the simulator side and a current source on the equipment side. This will create an implementation problem since the power amplifier is in general a voltage source.

1.3.5 Transmission-line model (TLM)

The transmission-line model (TLM) is widely used in real-time power grid simulators to decouple calculation tasks since, by using the natural line propagation delay, it is possible to parallelize the calculations for both ends of the line without introducing any error provided the delay is greater than the simulator calculation step (Do et al., 1999; Gagnon et al., 2010).

For power simulators, it is possible to use a transmission line whose propagation delay is strictly equal to the delay between the simulator and the amplifier. The TLM equivalent circuit is shown in Figure 1.5 as it appears in (Yoo, 2013).

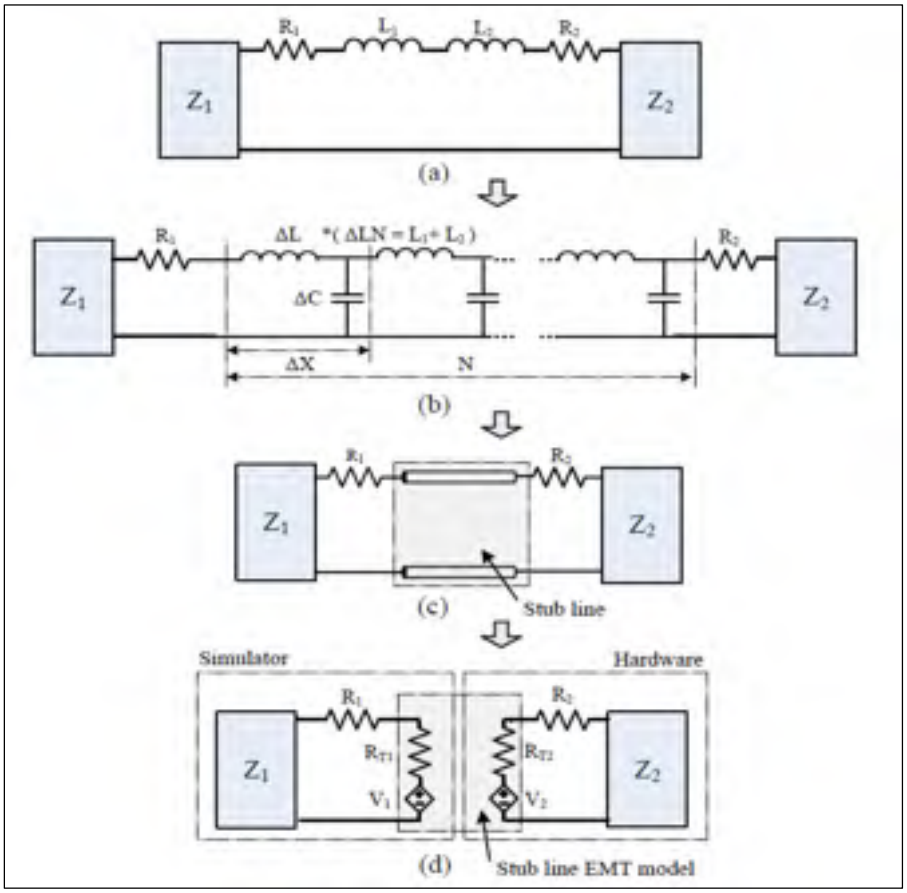

Figure 1.5 Short transmission line (stub line) model
Taken from Yoo (2013)

This method has the benefit of always being numerically stable. However, it has several drawbacks that impede its use with PHIL systems:

1. Although necessary to model the characteristic impedance of the line, the addition of R_{T2} on the equipment side causes Joule losses that may be significant. These losses should be compensated by oversizing the amplifier with respect to both power and voltage. To give the reader an order-of-magnitude estimate of the values involved, the SimP project amplifier has a rated capacity of 7.5 MVA at 25 kV, for a rated current of 173 A_{RMS}. A current of this magnitude flowing through a typical 300 Ω, resistor would generate losses of 27 MW and a voltage drop of 52 kV, which is completely disproportionate relative to the amplifier ratings. In addition, the cooling system required for such a resistor would be disproportionately large compared with the rest of the system.
2. This method calls for the introduction of a shunt capacitor, whose capacitance is calculated to obtain the required propagation delay. Such a shunt capacitor may not exist, and its effect must be considered.
3. For a 50-µs calculation step, this would entail assuming the amplifier is connected to the simulator through a 15-km line. A realistic parametrization is therefore required to factor in this distance.

1.3.6 Park transform based method (DQ)

The Park transform can be used to model, through a change in reference frame, an alternating three-phase system as a two-phase system. When the three-phase system is balanced and has a negligible harmonic content, the two-phase system magnitudes are constant, thus greatly simplifying voltage-source inverter control algorithms. This technique is attractive for PHIL systems since it allows for the easy compensation of delays through rotating reference phase angle lead-lag adjustments (Langston et al., 2012). As shown in Figure 1.6, the amplitude of the simulator voltage ($V_{abc\text{-}sim}$) becomes the reference signal for a voltage regulator whose output is the direct-axis voltage ($V_{d\text{-}r}$). The DQ-ABC transform is then applied to allow the amplifier to generate the voltages. The equipment current I_{abc} is then measured and converted into its rotating reference frame (ABC-DQ). This current is then injected into the simulation

using an inverse transform (DQ-ABC). Delays may then be compensated by adjusting the rotating reference frame phase-locked loop (PLL) lead-lag angle.

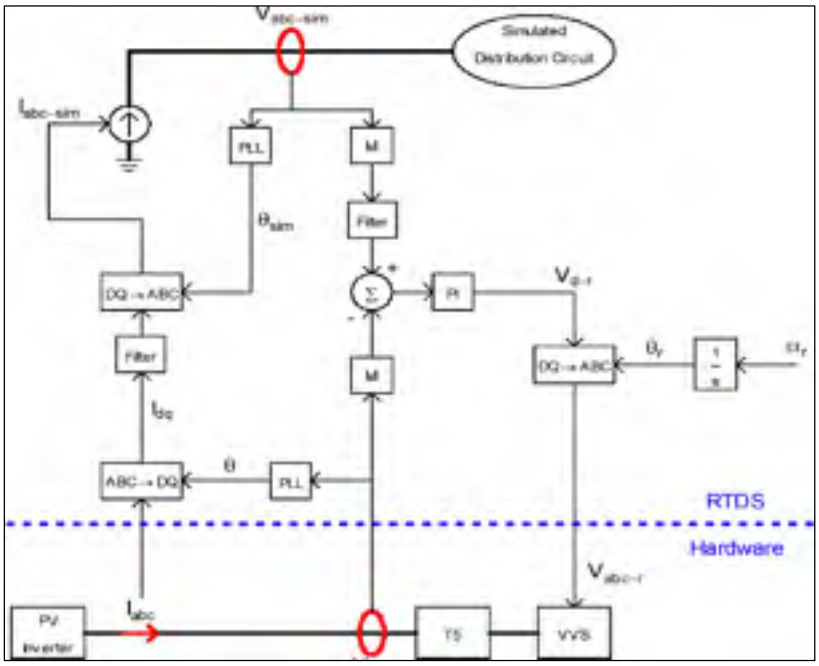

Figure 1.6 Park transform based interface
Taken from Langston (2012)

The main drawback of this approach is its small bandwidth as voltage and current values are transmitted as phasors, i.e. the magnitude and angle at the fundamental system frequency (50/60 Hz), which makes it ill-suited to transient electromagnetic testing. For example, this method cannot model harmonic interactions between the simulated power grid and the DUT although these are common in power grid studies.

1.3.7 Explicit discretization of series inductor or shunt capacitor

The partitioning of subnetworks through the discretization of a series inductor or a shunt capacitor is described in (Noda, 2003) and shown in Figure 1.7. This method consists mainly in using an explicit numerical integration method to discretize the differential equation (where

the inductor is modeled as a historical current source while the capacitor becomes a historical voltage source).

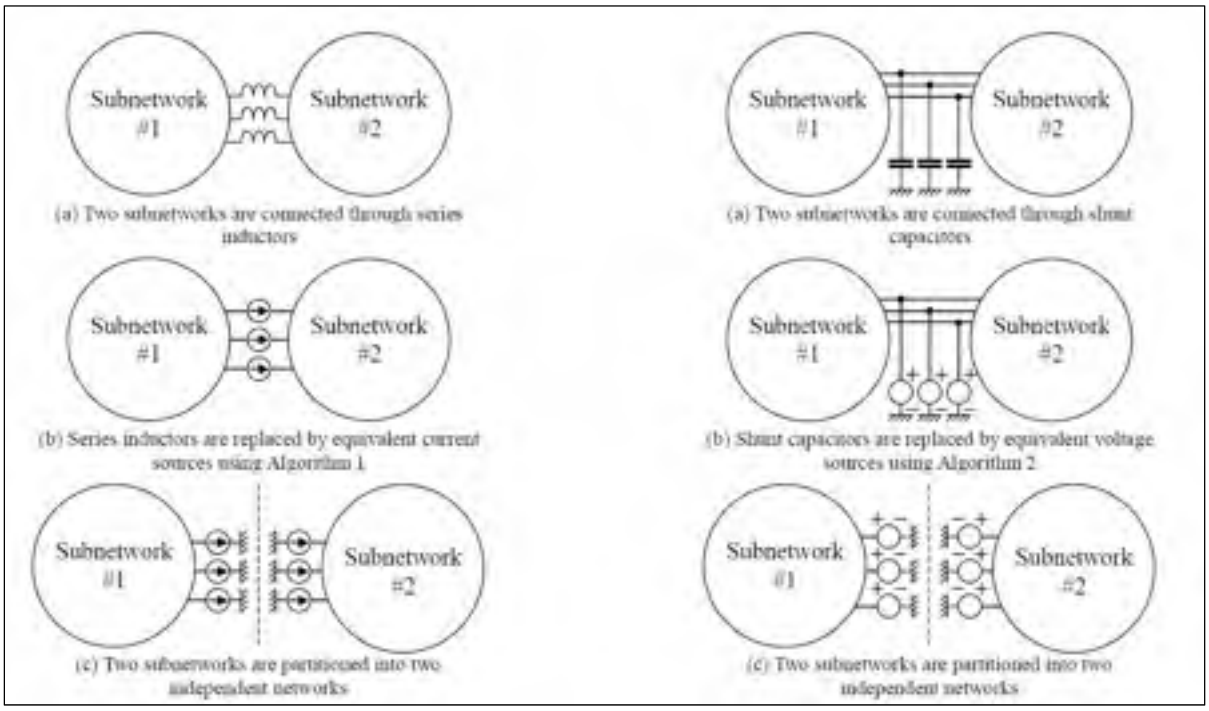

Figure 1.7 Partitioning using an explicit integration method
Taken from Noda (2003)

In general, inductor discretization is achieved using the trapezoidal method:

$$v_1(t) - v_2(t) = L\frac{d}{dt}i(t) \Rightarrow \frac{2(1-z^{-1})}{T(1+z^{-1})}I(z) = \frac{1}{L}\cdot(V_1(z) - V_2(z)) \tag{1.1}$$

$$i(k) = i(k-1) + \frac{T}{2L}\left(v_1(k) - v_2(k) + v_1(k-1) - v_2(k-1)\right) \tag{1.2}$$

Implicit since i depends on v_{12} at same instant.

This method has the advantage of being A-stable, thus ensuring the stability of the system regardless of the calculation step used by the simulator. However, this absolute stability has a significant drawback: the method is implicit since current *i(k)* is instantaneously dependent on voltages $v_1(k)$ and $v_2(k)$, as shown by equation (1.2). It is therefore to solve the equations for the whole system simultaneously. Hence, this method cannot be used for a PHIL system since the voltage at one of the two ends is in fact obtained with a delay of one calculation step.

To overcome this problem, (Noda, 2003) suggests using a linear extrapolation for the voltage that is not instantaneously available. This amounts to replacing the trapezoidal integrator with a two-step explicit linear method (second-order Adam-Basforth method):

$$v_1(t) - v_2(t) = L\frac{d}{dt}i(t) \;\Rightarrow\; \frac{2(1-z^{-1})}{T(3-z^{-1})}I(z) = \frac{1}{L}\cdot(V_1(z) - V_2(z)) \tag{1.3}$$

$$i(k) = i(k-1) + \frac{T}{2L}\left(3v_1(k-1) - 3v_2(k-1) - v_1(k-2) + v_2(k-2)\right) \tag{1.4}$$

Although its reliance on an explicit model allows for the exact expression of the inductor current, this method has some drawbacks that hinder its use with PHIL systems:

1. The second-order Adam-Basforth (AB) method is not A-stable (Ashourloo, Mirzahosseini, & Iravani, 2018), i.e. it may become unstable depending on system poles.
2. It is necessary to inject current on the amplifier side, but this amplifier is generally a voltage-source inverter.
3. The voltage extrapolation at both ends quickly becomes inaccurate during discontinuities or transient phenomena with a significant harmonic content, which is generally the case when transient events occur on the power grid.

1.4 Review of technologies used by major PHIL actors

Emerging at the start of the 2000s (Ayasun et al., 2003; Woodruff, Steurer, & Sloderbeck, 2004; Wu et al., 2004), the field of PHIL simulation has evolved steadily. Several major actors

currently operate MW-scale PHIL systems, including Florida State University Center for Advanced Power Systems (FSU-CAPS), Duke Energy Electrical Grid Research Innovation and Development (eGRID) (Clemson University, North Charleston, SC, USA) and National Renewable Energy Laboratory (NREL) Flatirons Campus (Boulder, CO, USA).

The FSU-CAPS system—commonly referred to as the "Advanced Prototype Power Test Bed"—consists of a set of AC and DC amplifiers connected to a digital simulator (Schoder, Langston, & Steurer, 2013). The bandwidth of these amplifiers is about 1 kHz; a transformer raises the output AC voltage from 416 V to 4.16 kV. At the simulator-amplifier interface, the ideal transformer method (ITM) (Steurer, Edrington, Sloderbeck, Ren, & Langston, 2010) and the damping impedance method (DIM) (Langston et al., 2015) have been used with several limitations with regards to their accuracy and stability. In fact, delays of the order of 350 μs have been observed between the reference and measured voltages (Steurer et al., 2010). Stability issues are avoided by using a more conservative DIA, based only on the fundamental frequency (Langston et al., 2012).

The Clemson University system—called "15-MW Grid Simulator"—consists in an amplifier designed by TECO-Westinghouse Motor Company (Ledezma et al., 2013) connected to a digital simulator. This amplifier has a 800-Hz bandwidth; a transformer raises the output AC voltage from 4.16 kV to 23.9 kV (Fox & Gislason, 2014). The ideal transformer method (ITM) is used; open-loop delays of 83 μs have been observed (McKinney, Fox, Collins, Bulgakov, & Salem, 2016).

Finally the NREL *Controllable Grid Interface* (GCI) is based on ABB's ACS6000 drive (converter) (Koralewicz, Gevorgian, Wallen, Merwe, & Jörg, 2016). The output voltage of the 7-MVA amplifier is obtained through magnetic addition using a transformer expressly designed for this application. The amplifier receives reference voltage magnitude and angle setpoints (at the fundamental frequency); a method is used to compensate for delays, which can be of the order of 2 ms (Koralewicz, Gevorgian, & Wallen, 2017). Although the system is

designed to operate at frequencies near 60 Hz, the amplifier has a 1-kHz bandwidth. The use of an interface method based on the fundamental frequency helps avoid stability issues.

Several lessons can be drawn from the experiences of these pioneers in the field of high-power PHIL simulation. First, it is worth noting that the results obtained by them are generally acceptable for tests the focus exclusively on DUT behavior. To assure DIA stability, low-impedance systems are used, which is tantamount to performing open-loop tests since the DUT has little or no impact on the simulated grid.

Second, the presence of a transformer at the output of the amplifier is a major drawback since it can easily saturate under the conditions below:

- Subsynchronous voltage oscillations (e.g. during an event on a series-compensated grid).
- Voltage with DC component.
- Voltage recovery after fault.

Saturation will decrease and distort the output voltage. In addition, the amplifier must be oversized since it must supply the saturation current. The fault could be cleared at a specific time to avoid saturating the transformer, but this would not be realistic since the exact fault clearance time is not usually known. Another solution would be to design a transformer with an appropriately sized magnetic circuit, but such a device would be extremely large and expensive.

Third, the observed delays between the simulator and the amplifier must be minimized to reduce uncertainty and stability issues. Finally, the selected DIA must be capable of replicating complex phenomena for any DUT connected to any ROS, including low short-circuit capacity power grids.

1.5 Summary

In short, existing digital interface algorithms (DIAs) found in the literature do not allow for the implementation of a general PHIL system, i.e. one that remains stable and accurate regardless

of its operating conditions. The methods developed until now perform in general well, but only for special cases, thus making them ill-suited to our application.
Although major laboratories currently operate high power PHIL systems similar to the system under development at IREQ, their performance does not meet our specifications. Commercially available products are unfortunately not designed for this type of application and do not have the required performance.

To efficiently integrate its various components, a comprehensive approach is being taken to design IREQ's PHIL system. This comprehensive approach considers all the components of the system: power amplifier, digital simulator and interface methods. Since stability is the main issue to be addressed for PHIL systems, the next chapter will describe a new stability analysis method that takes into consideration their technological particularities.

CHAPTER 2

NEW PHIL SYSTEM STABILITY ANALYSIS METHOD

2.1 Introduction

The simplified circuit shown in Figure 0.4 (reproduced below for the reader's convenience) is often used to investigate the stability of PHIL systems.

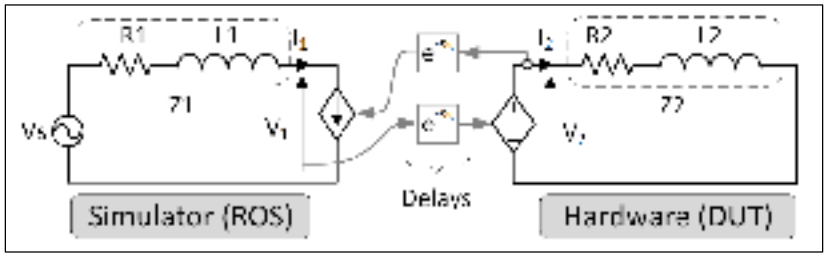

Figure 2.1 Intuitive implementation of PHIL circuit separation[2]

As demonstrated repeatedly (Guillo-Sansano, Roscoe, Jones, & Burt, 2014; M. H. Hong, S. Miura, Y. et al., 2009; Kotsampopoulos, Lehfuss, Lauss, Bletterie, & Hatziargyriou, 2015; G. Lauss, Lehfuss, Viehweider, & Strasser, 2011; G. F. Lauss et al., 2016; W. Ren et al., 2011; Alexander Viehweider, Lauss, & Felix, 2011; A. Viehweider, Lehfuss, & Lauss, 2012; Wei et al., 2008), the closed-loop stability of such systems can be maintained if the value of the ROS impedance (Z1) is less than the value of the DUT impedance (Z2) at all frequencies. This stability relation is valid if both the ROS and the DUT are analog (i.e. continuous) systems. However, in an actual PHIL system such the system shown in Figure 2.2, the ROS is a discrete system since the governing equations are solved using the simulator's numerical integration method and the DUT is a continuous system since the behavior of the power equipment is driven by the laws of physics. The system is therefore hybrid (discrete-continuous) and the

[2] A large resistor, not shown in this figure, is inserted in parallel with the current source to avoid a series connection with inductor L1. The effect of this resistor is neglected.

interface is implemented using a sampler (unit delay 1/z), which models the analog-digital conversion (ADC), and a zero-order hold (ZOH) block, which models the digital-analog conversion (DAC).

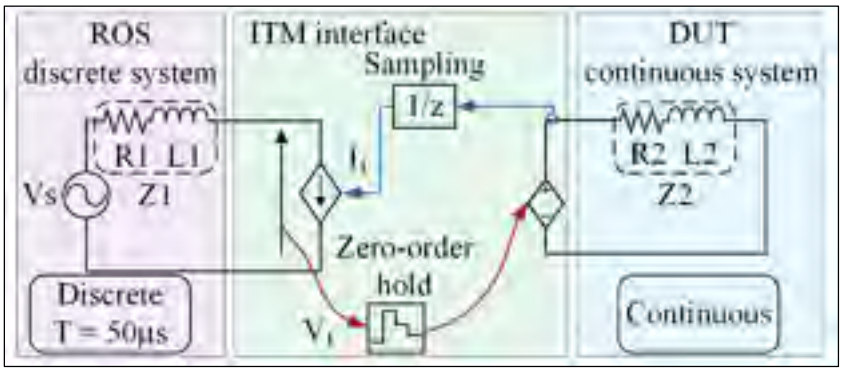

Figure 2.2 Hybrid model of a PHIL system

This system was simulated in the MATLAB/SPS environment, which can be used to model continuous systems (simulated using variable step algorithms) and discrete ones in the same simulation environment. The system is discretized using a 50-µs sampling period (T), which is a typical value for power grid simulations (Gagnon et al., 2010). Two sets of parameters were used for this simulation (see Table 2.1). In both cases, the ROS has a short-circuit capacity (SCC) of 150 MVA, with a X/R[3] ratio of 30 and a rated voltage of 14.4 kV, which are typical single-phase values at the output of a 47-MVA distribution substation transformer.

Table 2.1 Sets of parameters

Parameter	**Case 1 (Z1/Z2 = 0.1)**	**Case 2 (Z1/Z2 = 0.67)**
R1, L1 → Z1	0.0460 Ω, 0.0036 H → SCC = 150 MVA	0.0460 Ω, 0.0036 H → SCC = 150 MVA
R2, L2 → Z2	0.4600 Ω, 0.0360 H → SCC = 15 MVA	0.0690 Ω, 0.0054 H → SCC = 100 MVA

[3] The X/R ratio is the ratio between the inductive and resistive components of the impedance at the fundamental frequency.

Let us start with Case No. 1, where impedance Z1 is a tenth of impedance Z2. The simulation results presented in Figure 2.3 (a) show the current and voltage at the interface point, on the simulator side, relative to an undecoupled reference system (such as the system shown in Figure 0.4). The PHIL system simulation results are stable and properly match the reference case. Case 2 should also be stable since impedance Z1 is 1.5 times less than impedance Z2 (|Z1| / |Z2 | = 0.67). However, the simulation results shown in Figure 2.3(b) indicate that the PHIL system is in fact unstable, with an oscillation frequency of 6,667 Hz.

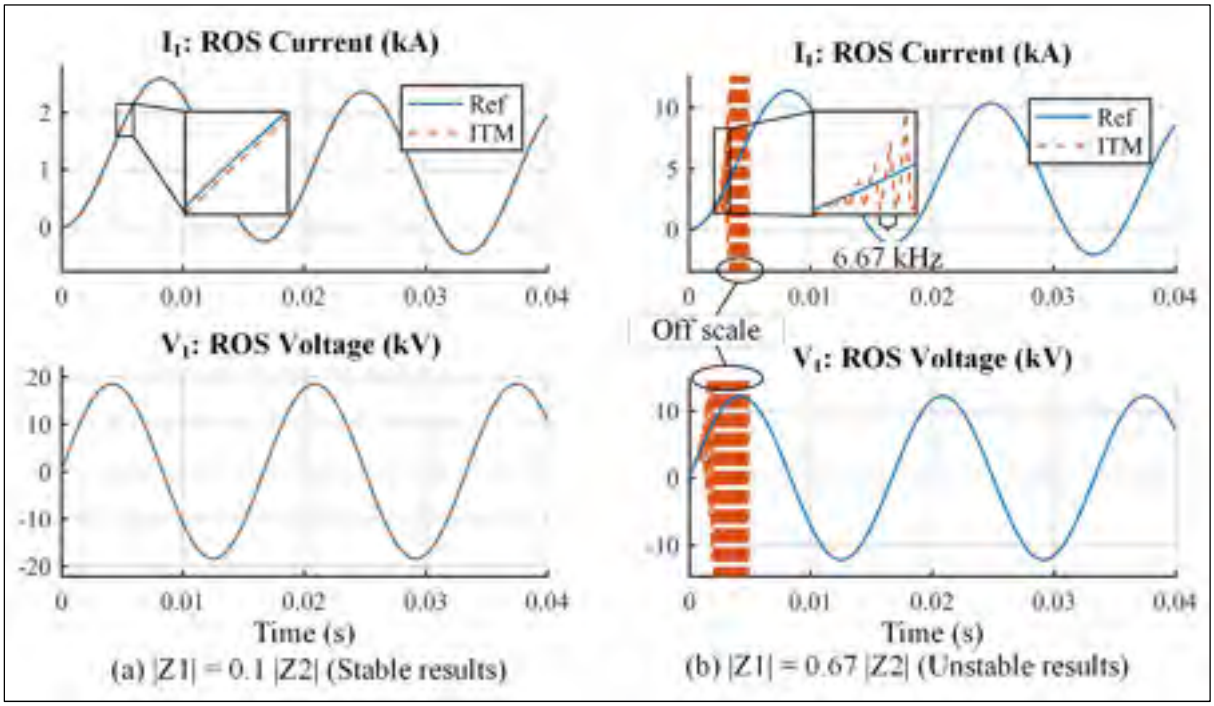

Figure 2.3 Simulation results for hybrid PHIL system

Unexpected according to existing analysis methods, this behavior will be analyzed in detail in this chapter using a new stability analysis method designed for closed-loop hybrid systems (Tremblay, Fortin-Blanchette, et al., 2017). It has been found that the development of a stability analysis method must take into consideration sampling effects at the analog-digital interface. In addition, the development of a method that allows for the independent analysis of both systems (ROS and DUT) will simplify the development of instability mitigation techniques.

2.2 Decomposition of system into two equivalent impedances

Used to assess the stability of continuous closed-loop systems, the Nyquist diagram is in general the approach used by researchers to study the stability of PHIL systems (G. Lauss et al., 2011; Lentijo, D'Arco, & Monti, 2010; A. Viehweider et al., 2012). However, as mentioned above, stability analysis cannot assume a fully continuous system since several significant aspects of system implementation would otherwise be ignored, including sampling and numerical integration effects. In addition, it is difficult to assess the impact of the various factors that affect the stability of PHIL systems using Nyquist diagrams since the ROS and the DUT are treated as a whole system. To overcome this challenge, a new stability analysis method is proposed to take into consideration the discrete modeling of the impedance on both sides of the separation point (by factoring in DUT sampler-hold block effects and the approximate numerical integration used for the ROS). By independently obtaining the frequency response of the two discrete systems, it will be possible the evaluation the stability of the system and identify proper mitigation measures to ensure closed-loop stability.

To achieve this decomposition, an impedance measurement “Z” is added at the simulator interface point, as shown in Figure 2.4. The left-side impedance ($Z_{ROS}(z)$) can then be determined while taking into consideration the numerical integration method while the right-side admittance ($Y_{DUT}(z)$) can be deduced based on the equipment impedance associated with the digital-analog conversion. By using these impedances in the discrete domain, it is possible to obtain a closed-loop block diagram for stability analysis purposes. It is well known that this system will be stable if “the open-loop transfer function magnitude is less than one at the frequency where the phase angle is equal to 180° (or, equivalently, -180°)” (Nise, 2000). The next sections will present in detail the method that can be used to obtain the impedances on both sides of the separation point. It is important to underscore that this method can be applied to other digital interface algorithms (since the discrete impedance at the interface point is known) and can be used for any ROS or DUT (assuming the system is linear).

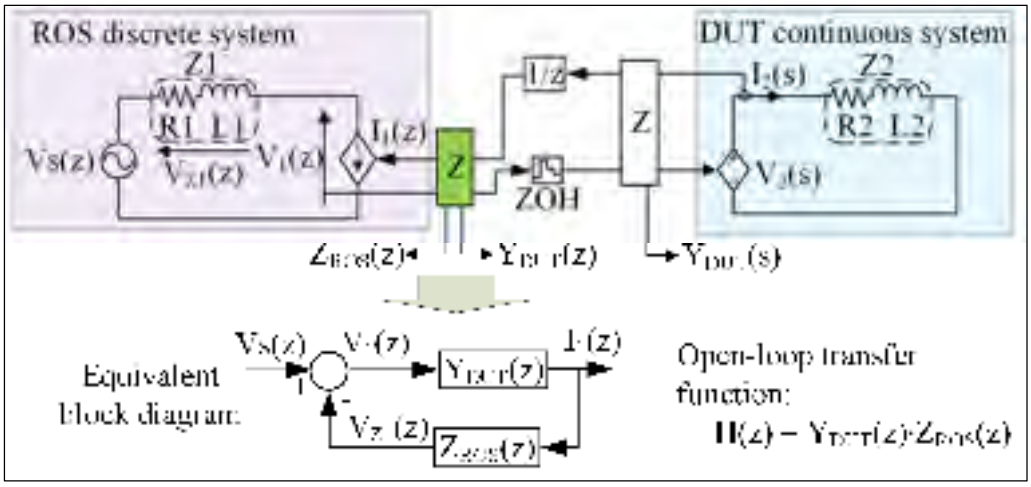

Figure 2.4 Impedance measurement for hybrid PHIL system

2.2.1 DUT impedance: effect of ZOH and sampling

First, the effect of the sampler-hold block on the DUT shown in Figure 2.4 will be studied. The voltage measured on the ROS side (discrete signal $V_1(z)$) is applied on the DUT side (continuous signal $V_2(s)$) through a ZOH with the transfer function below:

$$\mathrm{ZOH(s)} = \frac{V_2(s)}{V_1(z)} = \frac{1 - e^{-sT}}{s} \tag{2.1}$$

The continuous admittance of the DUT ($I_2(s)$ as a function of $V_2(s)$) is given by:

$$\mathrm{Y_{DUT}(s)} = \frac{I_2(s)}{V_2(s)} = \frac{1}{R2 + s \cdot L2} \tag{2.2}$$

ROS current (discrete signal $I_1(z)$) provided through the sampling, modeled as a unit delay, of the DUT current (continuous signal $I_2(s)$):

$$\frac{I_1(z)}{I_2(s)} = \frac{1}{z} \tag{2.3}$$

Using (2.1)–(2.3) and the discrete Laplace transform ($\mathcal{Z}$-transform), the discrete admittance of the DUT can be obtained:

$$\mathrm{Y_{DUT}(z)}=\frac{I_1(z)}{V_1(z)} = \mathcal{Z}(\mathrm{Y_{DUT}(s)\ ZOH(s)}) \cdot \frac{1}{z} = \frac{1 - e^{-T \cdot \frac{R2}{L2}}}{z \cdot R2 \cdot \left(z - e^{-T \cdot \frac{R2}{L2}}\right)} \tag{2.4}$$

The impedance cannot be modeled in each domain (continuous (2.5) and discrete (2.6)):

$$\mathrm{Z_{DUT}(s)} = \frac{1}{\mathrm{Y_{DUT}(s)}} = R2 + s \cdot L2 \tag{2.5}$$

$$\mathrm{Z_{DUT}(z)} = \frac{1}{\mathrm{Y_{DUT}(z)}} = \frac{z \cdot R2 \cdot \left(z - e^{-T \cdot \frac{R2}{L2}}\right)}{1 - e^{-T \cdot \frac{R2}{L2}}} \tag{2.6}$$

2.2.2 ROS impedance: effect of numerical integration method

Since the ROS is modeled using a digital simulator, the integration method used to discretize the system must be considered given that it changes the effective impedance value. Like most large-scale power grid simulators, Hypersim relies on a numerical integration method based on trapezoidal approximations to simulate dynamic elements (Do et al., 1999). This implicit numerical method has the advantage of always being stable, regardless of the sampling period or the dynamic characteristics of the elements being simulated. This is what is called an associative numerical integration method (Tom T. Hartley, 1994), where each "s" of the continuous transfer function can be replaced by:

$$s \Leftrightarrow \frac{2(z-1)}{T(z+1)} \tag{2.7}$$

The impedance can now be modeled in each domain (continuous Figure 2.4 and discrete) as shown below:

$$\mathrm{Z_{ROS}(s)}=\frac{V_{Z1}(s)}{I_1(s)} = R1 + s \cdot L1 \tag{2.8}$$

$$\mathrm{Z_{ROS}(z)}=\frac{V_{Z1}(z)}{I_1(z)} = R1 + \frac{2(z-1)}{T(z+1)} \cdot L1 \tag{2.9}$$

2.3 Algorithm to determine closed-loop system stability

To analyze system stability, impedances Z_{ROS} and Z_{DUT}—obtained in the continuous and discrete domains—are traced as a function of the frequency (F), from 0 Hz up to the Nyquist frequency (Fs = 1/T/2 Hz) using the relations below:

$$s = j2\pi \cdot F \tag{2.10}$$

$$z = e^{sT} = e^{j2\pi \cdot F \cdot T} \tag{2.11}$$

Using the set of parameters for Case 2 (Table 2.1, with |Z1|/|Z2| = 0.67), which give unstable results, the DUT and ROS frequency responses are obtained and presented in the sections below.

2.3.1 DUT frequency response

The magnitude and phase of $Z_{DUT}(s)$ and $Z_{DUT}(z)$, are obtained using (2.5), (2.6), (2.10) and (2.11). They are shown in Figure 2.5 as a function of frequency. Since the DUT is mainly inductive (X/R = 30), it is normal for the magnitude of the continuous impedance $|Z_{DUT}(s)|$ to increase linearly with the frequency and for its phase angle $\angle Z_{DUT}(s)$ increase rapidly up to 90°. However, when the system is sampled (in this case, T = 50 μs is equivalent to a 20-kHz sampling frequency), it is observed that:

- The impedance magnitude $|Z_{DUT}(z)|$ no longer matches the continuous impedance starting approximately at 2 kHz (one tenth of the sampling frequency). Therefore, the ZOH has the

effect of artificially decreasing the apparent magnitude of the DUT impedance, which is detrimental to closed-loop stability.

- The discrete impedance phase angle $\angle Z_{DUT}(z)$ increases linearly due to the ZOH and the sampling delay. Consequently, although the DUT is a passive RL element, the sampling mechanisms changes the nature of the system as the frequency increases. For Case 2, the discrete DUT impedance becomes a negative resistance at 3.33 kHz (since the impedance phase angle is 180°) and a negative inductance at 6.66 kHz (since the impedance phase angle is 270°). In addition to impacting the capacity balance, the changing nature of the impedance has an adverse effect on the closed-loop stability, as will be explained in section 2.3.3.

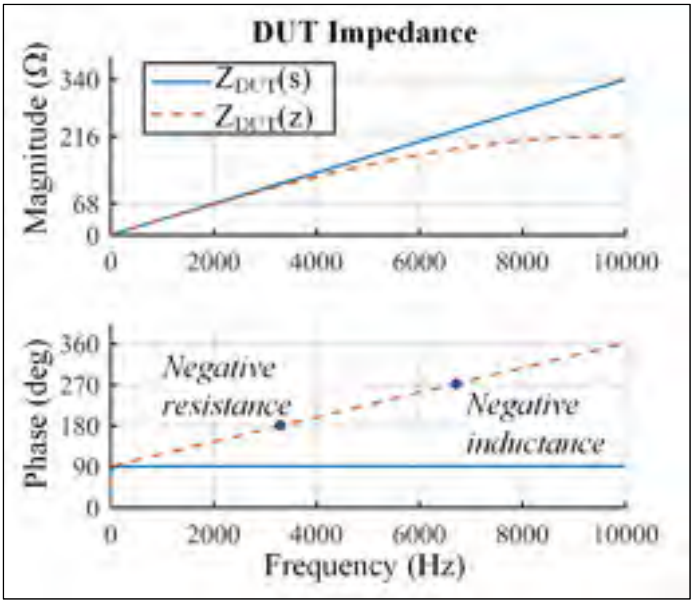

Figure 2.5 Hybrid DUT frequency response

2.3.2 ROS frequency response

Similarly, using (2.8), (2.9), (2.10) and (2.11), it is also possible to obtain the magnitude and phase angle of $Z_{ROS}(s)$ and $Z_{ROS}(z)$ as a function of time, as shown in Figure 2.6. Since the ROS is also mainly inductive (X/R = 30), it is normal for the magnitude of the continuous impedance magnitude $|Z_{ROS}(s)|$ to increase linearly with the frequency and for its phase angle

$\angle Z_{ROS}(s)$ to increase rapidly up to 90°. On the other hand, when the system is discretized using the trapezoidal method using T = 50 μs, it is noted that:

- The impedance magnitude $|Z_{ROS}(z)|$ no longer matches the continuous impedance starting approximately at 2 kHz (one tenth of the sampling frequency). The magnitude increases thereafter until it goes to infinity at the Nyquist frequency (10 kHz). This singularity is due to a division by zero that occurs in equation (2.9) at z = -1. The increased impedance magnitude adversely impacts closed-loop stability as discussed in section 2.2.
- The discrete impedance phase angle $\angle Z_{ROS}(z)$ matches well the behavior of $\angle Z_{ROS}(s)$, thus having have no adverse effect on closed-loop stability.

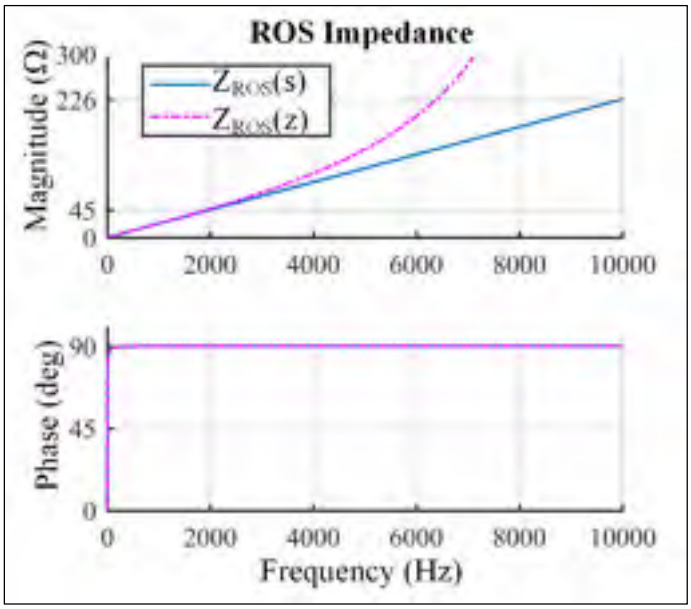

Figure 2.6 Hybrid ROS frequency response

The increase in the impedance magnitude is due to a tangential discrete ROS impedance relation. Given that, using (2.9) and (2.11), it is possible to see that the inductive impedance depends on a tangential function:

$$Z_{ROS}(z) = R1 + j\frac{2tan(\pi \cdot F \cdot T)}{T}L1 \tag{2.12}$$

This relation shows that, when the Nyquist frequency is reached, the impedance magnitude tends towards infinity, as shown above in Figure 2.6.

2.3.3 Closed-loop system stability

When a closed-loop connection is established between the DUT and ROS, stability is preserved if there is no positive feedback between the two open-loop systems. The main implication of this is that the phase difference between the two systems must be other than 180° at all frequencies from 0 Hz to the Nyquist frequency. If the phase angle between the two systems is equal to 180°, the closed-loop system will not necessarily be unstable since instability will only occur if the ROS impedance is greater than the DUT impedance (open-loop gain > 1), as shown in Table 2.2.

Table 2.2 Stability truth table

$\lvert\angle Z_{DUT}(z) - \angle Z_{ROS}(z)\rvert$	$\lvert Z_{ROS}(z)\rvert / \lvert Z_{DUT}(z)\rvert$	**Stable?**
=180°	< 1	Yes
=180°	> 1	No
≠ 180°	< 1	Yes
≠ 180°	> 1	Yes

The superimposed graphs of the ROS and DUT discrete impedance magnitudes and the phase angle difference between the two discrete impedances are shown in Figure 2.7. The main point of note in this figure occurs at 6,667 Hz. At this frequency, the phase angle difference between the two systems is equal to 180° and the open-loop gain ($|Z_{ROS}(z)| / |Z_{DUT}(z)|$) is greater than unity. This will result in instability when the two systems are connected in a closed-loop configuration, as seen in the simulation results presented in Figure 2.3 (b). On this figure, the oscillation frequency in the box is exactly 6,667 Hz, which matches the positive feedback frequency.

Using this analysis method, it is therefore possible to verify whether the closed-loop system will be stable prior to connecting the two systems. Furthermore, it is possible to visualize which of the impedances (ROS or DUT) will have the greatest impact on system gain margins.

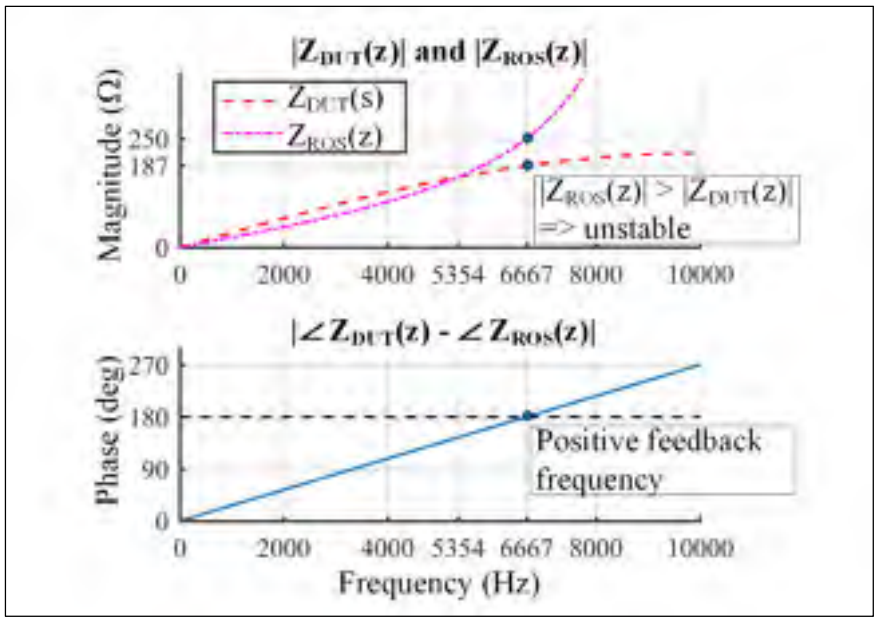

Figure 2.7 DUT and ROS impedance frequency response

2.3.4 Marginal stability case

To determine the minimum DUT impedance required to ensure system stability, the DUT impedance at 6,667 Hz is increased to 250 Ω (from 187 Ω) using the relation shown below, based on equations (2.6) and (2.11):

$$|Z_{DUT}(z)| = 250 = \left| \frac{z \cdot k \cdot R2 \cdot \left(z - e^{-T \cdot \frac{R2}{L2}}\right)}{1 - e^{-T \cdot \frac{R2}{L2}}} \right| \quad where \quad \begin{matrix} z = e^{j2\pi/3} \\ R2 = 0.069\ \Omega \\ L2 = 0.0054\ H \\ T = 50\ \mu s \end{matrix} \tag{2.13}$$

Factor "k"—which is the factor by which impedance Z2 must be multiplied to ensure the system is stable— may therefore be calculated by solving equation (2.13), thus giving a value of k = 1.3364. Thus, for the system to be stable, it is necessary that R2 = 0.092 Ω and L2 = .0072 H, i.e. exactly the double of impedances R1 and L1.

Hence, the so-called rule commonly used to check whether the basic inductive circuit of a PHIL system is stable (|Z1| < |Z2|) is only valid for continuous system models. When actual

PHIL implementation effects are considered, i.e. sampling and numerical integration, this rule is halved and becomes |Z1| < 0.5 |Z2|. The frequency response for the new DUT impedance is shown in Figure 2.8. It can be noted that at the positive feedback frequency (6,667 Hz), the open-loop gain is now unity, i.e. the corresponding closed-loop system will be marginally stable.

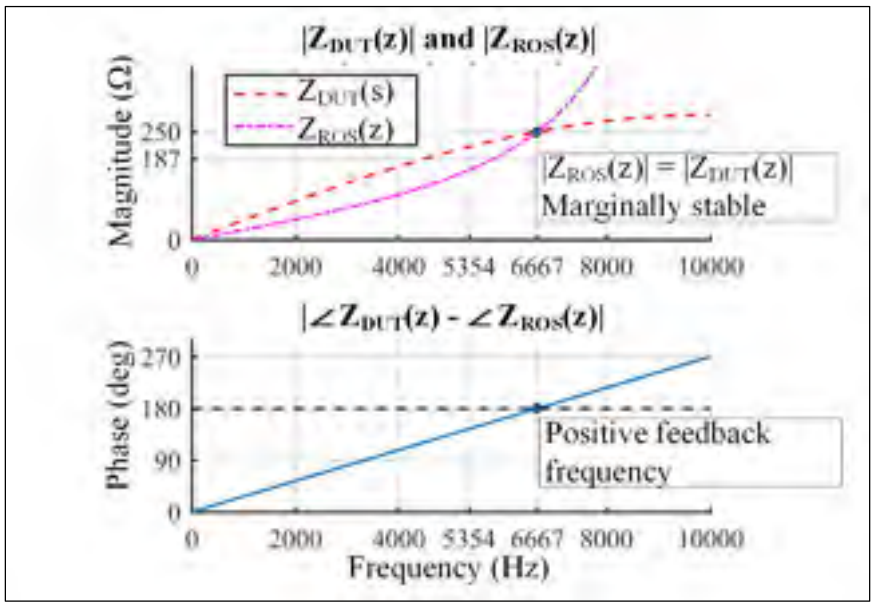

Figure 2.8 Frequency response for marginally stable case

A hybrid system simulation for the set of parameters to the left and the right of the marginal stability point is shown in Figure 2.9. Note that when |Z1| = 0.49 |Z2| (Figure 2.9(a)), simulation results are stable since the oscillation amplitude at the positive feedback frequency is damped. However, when |Z1| = 0.51 |Z2| (Figure 2.9 (b)), the system is unstable since the oscillation amplitude grows. These results agree perfectly with the frequency response-based stability analysis presented above.

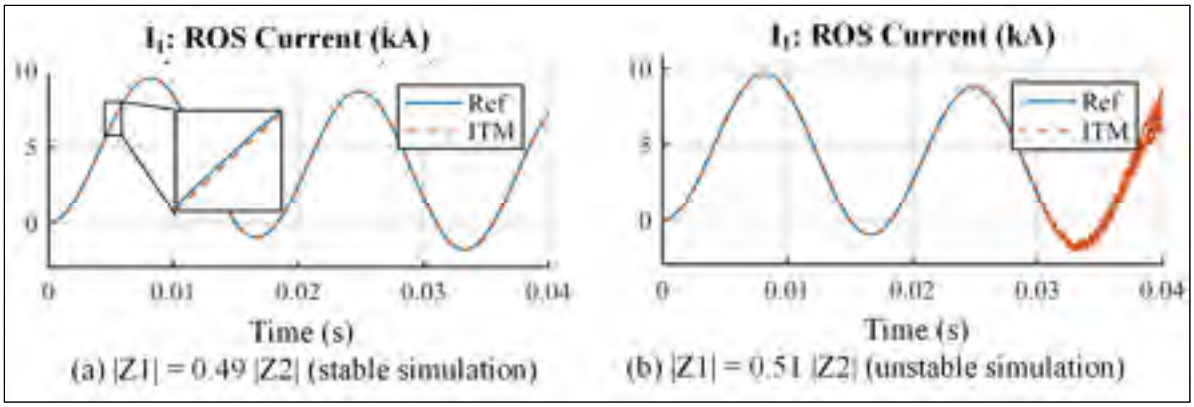

Figure 2.9 Simulation results around stability critical point

2.4 Conclusions

In this chapter, it has been demonstrated that the analysis of the stability of a PHIL system cannot be based on an entirely continuous model. Rather, the system must be treated as a hybrid (analog-digital) one. As a contribution, a new method for assessing the stability of decoupled electrical systems, such as PHIL simulators, has therefore been developed in detail. Based on the frequency response of the open-loop discrete impedances, the new method can be used to determine whether a system is stable without requiring the calculation of the closed-loop transfer function. This method helps understand the impact of the numerical integration method on stability and assess the various factors that influence it. For example, using the method together with the ideal transformer model digital interface algorithm (ITM-DIA), it was possible to observe that:

1. The zero-order hold (ZOH) and the sampler used to interface the DUT with the ROS result in an impedance attenuation and a high-frequency phase shift that adversely impact stability. This phase shift (responsible for the positive feedback) is the primary cause of the instability and the attenuation may be responsible for the open-loop gain being greater than one when the system phase angle crosses the 180° point.
2. The trapezoidal numerical integration method used to simulate the ROS increases the impedance magnitude at high frequencies, which also has an adverse impact on stability.

   The combined effect of these two points greatly enhances the risk of instability.

Furthermore, the development of this analysis method has also made it possible to observe empirically that the modeling of continuous impedances using discrete impedances is only accurate at frequencies lower than one tenth of the sampling frequency. This is a major observation since it limits the range of validity of simulation results at higher frequencies.

In short, considering the ideal transformer method (ITM) issues and limitations that have been identified in this section, other avenues must be explored to solve the PHIL system stability problem. This will be covered in the next chapter.

CHAPTER 3

EXPLORING NEW INTERFACE METHODS

3.1 Introduction

This chapter gives an overview of various preliminary approaches developed to solve the PHIL system stability problem. These exploratory efforts are presented in this dissertation to provide a relevant basis for better understanding the path leading to the development of a new digital interface algorithm (DIA).

3.2 Mitigation methods for ITM-DIA

As shown in Chapter 2, ITM stability depends on the ratio of the ROS and DUT impedances at the positive feedback frequency. Although it is impossible to eliminate this positive feedback since it is caused by the sampling delay and the sampling-hold block, it is interesting to explore how the impedance ratio could be modified artificially at this critical frequency. The stability analysis method developed in Chapter 2 (where the ROS and the DUT are treated independently) is thus leveraged in this section to develop a mitigation method.

3.2.1 Interface signal filtering

An intuitive approach to modifying the system's impedance is to add a filter in the feedback loop, as shown in Figure 3.1. For example, the addition of a low-pass filter with a 3-kHz cutoff frequency will increase the high-frequency DUT impedance, thus enhancing the closed-loop system stability.

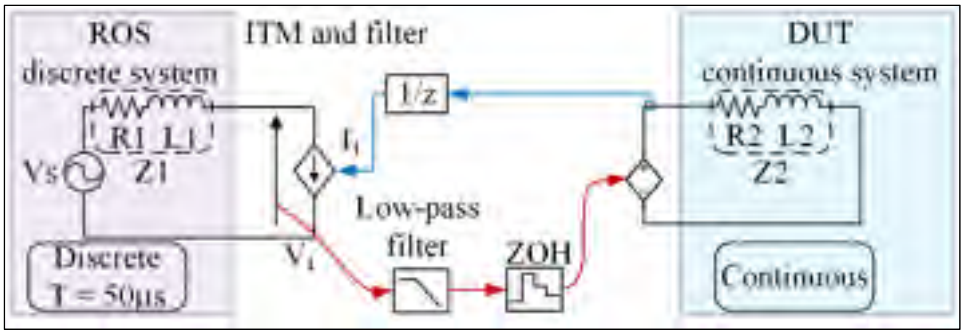

Figure 3.1 Block diagram for ITM with low-pass filter

The choice of filter discretization method is also important since it affects the system frequency response. The trapezoidal method has been selected to increase the high-frequency DUT impedance, as shown by the equation below:

$$\mathrm{Z_{DUT}(z)} = \frac{z \cdot R2 \cdot \left(z - e^{-T \cdot \frac{R2}{L2}}\right)}{1 - e^{-T \cdot \frac{R2}{L2}}} \cdot \left(\frac{2(z-1)}{T(z+1)} \cdot \tau + 1\right) \tag{3.1}$$

Where τ represents the filter time constant ($\tau = 1/(3000 \cdot 2\pi)$).

The DUT and ROS frequency responses—obtained using equations (2.9) and (3.1), and the set of parameters for Case 2 in Table 2.1—are presented in Figure 3.2(a). This figure shows that the system will be stable in its closed-loop configuration. This is confirmed by the simulation results shown in Figure 3.2(b).

Therefore, filtering seems to be an interesting method for stabilizing PHIL systems. However, for this method, stability remains dependent on the ROS and DUT impedances, thus making it too limiting for our intended range of applications. For example, it is impossible to model:

- Islanding as the DUT impedance is in general lower than the ROS impedance.
- Low short-circuit capacity power systems (typically used for DER testing).
- Power systems including breakers that may trip during the simulation.

This method also requires a priori knowledge of the DUT impedance to design the filter. This is in general impossible given the complexity of power equipment (e.g. power switch, control system, non-linearities).

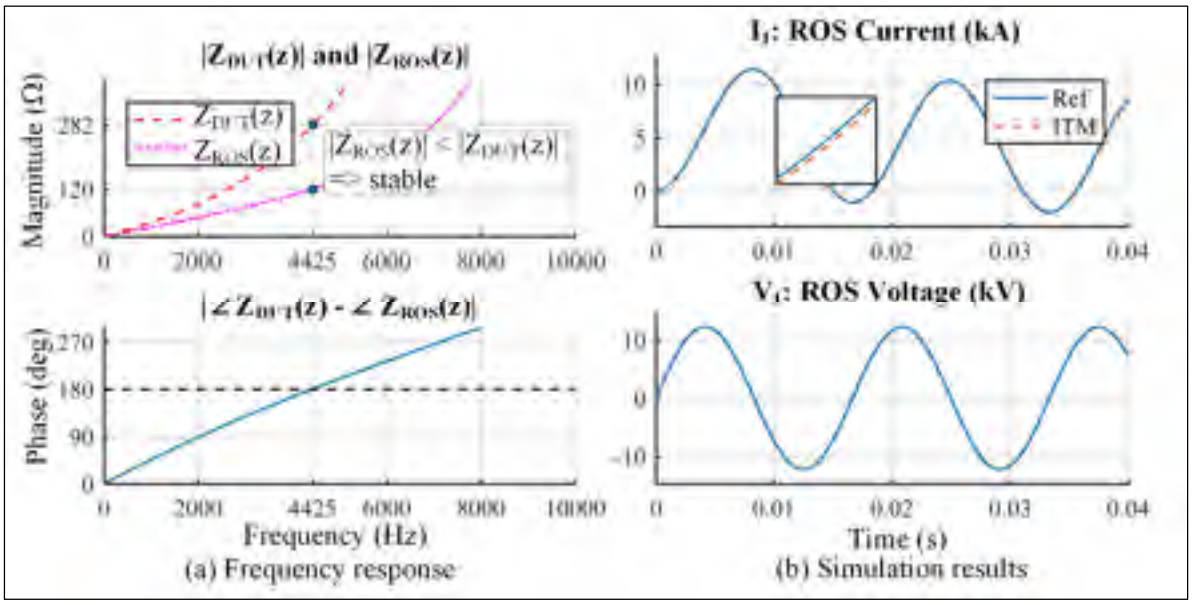

Figure 3.2 Results – ITM with low-pass filter

3.2.2 Numerical methods

Another way of modifying the equivalent system impedances consists in changing the numerical method used for the ROS and the DUT.

3.2.2.1 Numerical integration used for ROS

It is possible to use numerical methods other than the trapezoidal method to model the system on the simulator side. However, due to system stability considerations, the method must be absolutely stable (A-stable) and may only use one step in the calculation history. This constraint stems mainly from the real-time implementation of the system, but it is also required to efficiently manage the discontinuities created by non-linear elements. For this reason, the implicit Euler method has been selected:

$$s \Leftrightarrow \frac{(z-1)}{Tz} \tag{3.2}$$

The discrete ROS impedance then becomes:

$$\mathrm{Z_{ROS}(z)} = R1 + \frac{(z-1)}{Tz} \cdot L1 \tag{3.3}$$

The DUT and ROS frequency responses—obtained using equations (2.6) and (3.3), and the set of parameters for Case 2 in Table 2.1—are presented in Figure 3.3(a). This figure shows that the system will be stable in its closed-loop configuration since the discrete impedance no longer tends to infinity at the Nyquist frequency given that the implicit Euler method entails no division by zero. The stability of this system is confirmed by the simulation results shown in Figure 3.3(b).

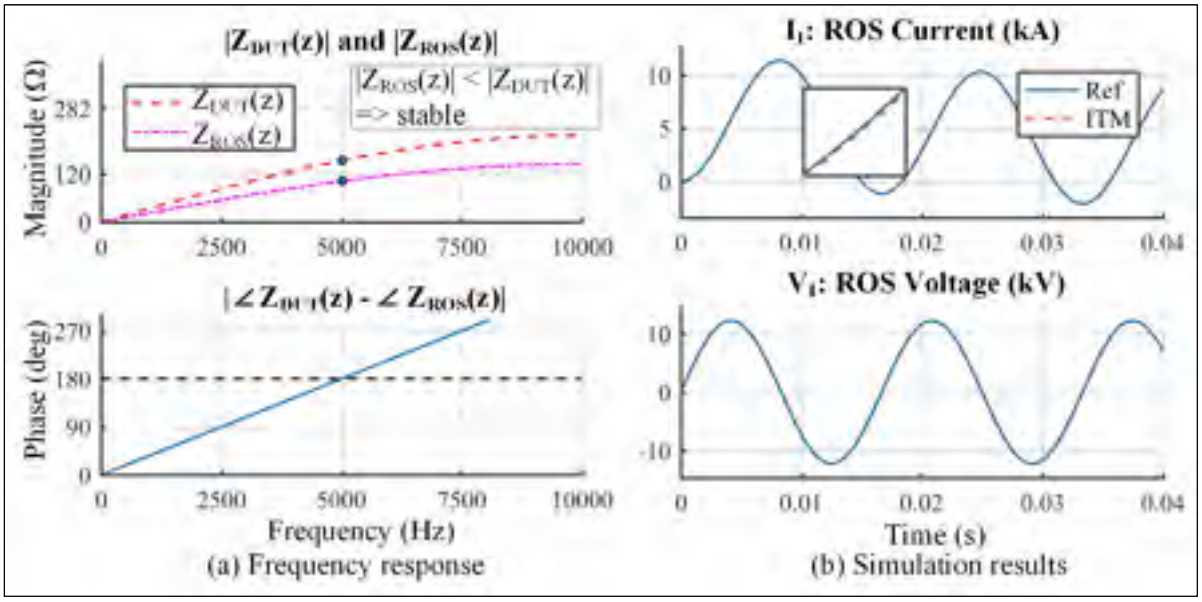

Figure 3.3 Results – ITM with implicit Euler method

Therefore, the implicit Euler method seems to be an interesting method for stabilizing PHIL systems. However, its use will be subject to the same constraints as those discussed in relation

to filtering (see section 3.2.1), i.e. the impossibility to model islanding, low short-circuit capacity power systems and those that contain series breakers.

3.2.2.2 Sampler-hold for DUT

Another technique that may be used to increase the DUT-side impedance is to use another type of hold block. For example, the triangular hold is a first-order hold (FOH) whose behavior closely resembles that of the trapezoidal method. In this technique, the DUT impedance is calculated as shown below:

$$\mathrm{Y_{DUT}(z)} = \mathcal{Z}(\mathrm{Y_{DUT}(s)\cdot FOH\ (s)}) \cdot \frac{1}{z} = \mathcal{Z}\left(\frac{1}{R2 + sL2} \cdot \frac{e^{sT}}{T}\left(\frac{1 - e^{-sT}}{s}\right)^2\right) \tag{3.4}$$

$$\mathrm{Z_{DUT}(z)} = \frac{1}{\mathrm{Y_{DUT}(z)}} = \frac{z\left(\left(\frac{R2}{L2} - 1 + e^{-T\cdot\frac{R2}{L2}}\right)z + \left(1 - e^{-T\cdot\frac{R2}{L2}} - T\cdot\frac{R2}{L2}\cdot e^{-T\cdot\frac{R2}{L2}}\right)\right)}{\frac{R2}{L2}\cdot\left(z - e^{-T\cdot\frac{R2}{L2}}\right)} \tag{3.5}$$

The DUT and ROS frequency responses—obtained using equations (2.9) and (3.5), and the set of parameters for Case 2 in Table 2.1—are presented in Figure 3.4(a). They show that the system will not be stable in its closed-loop configuration. This is to be expected since the impedance ratio rule is not respected at the positive feedback frequency. In fact, simulation results presented in Figure 3.4(b) validate this hypothesis, confirming the existence of an instability with a 10-kHz oscillation frequency.

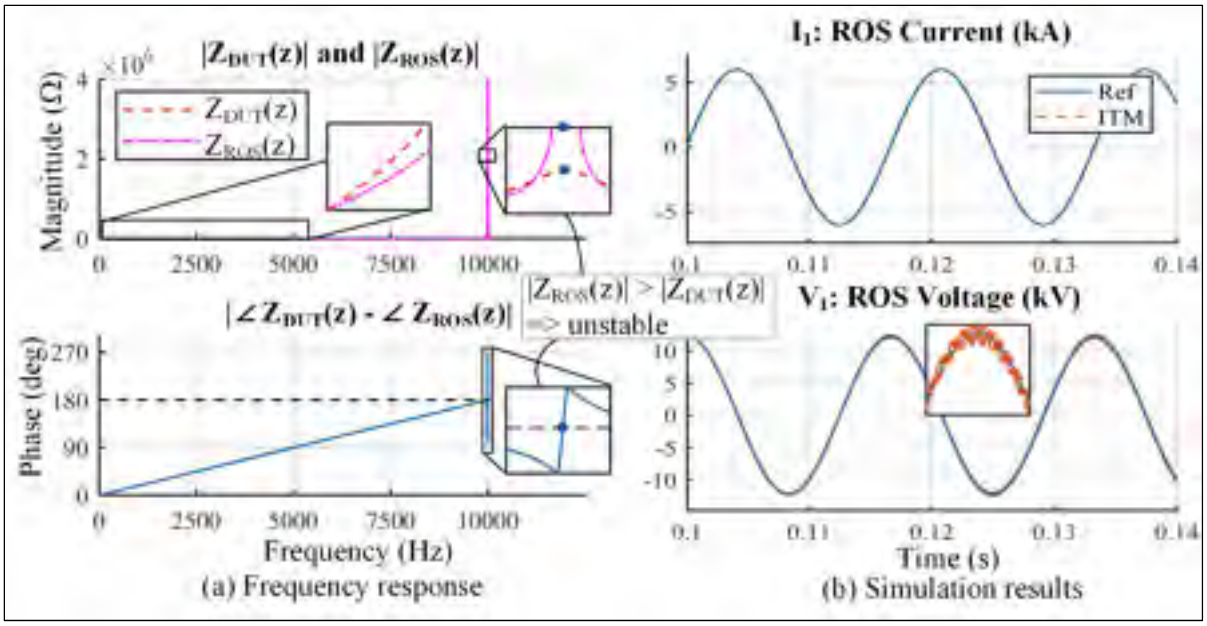

Figure 3.4 Results – ITM with first-order hold (FOH)

3.3 Predictive control

This section presents work carried out as part of a study focused on the control of time-delayed systems. This approach has been applied to PHIL systems since the latter can be modeled as time-delayed systems, controlled either by the ROS or the DUT.

First, the theory of time-delayed systems is presented. Their application to PHIL systems is then developed in detail, considering that the full system may be modeled as a continuous system. Finally, the applicability of this method to hybrid systems is discussed.

3.3.1 Theory

The predictive control approach used in this project (Fridman, 2014) is based on a linear, dynamic, time-invariant system with a constant input delay:

$$\dot{x}(t) = Ax(t) + Bu(t - \tau) \tag{3.6}$$

The delay τ and the system matrices A and B are deemed to be known. To stabilize this system, it is proposed to use state-feedback control based on a variable substitution that turns the system delayless:

$$u(t) = Kz(t) \tag{3.7}$$

where $z(t)$ is the predicted state at time $(t + \tau)$, obtained using the general solution of the differential equation below:

$$z(t) = x(t + \tau) = e^{A\tau}x(t) + \int_{t}^{t+\tau} e^{A(t+\tau-\rho)}Bu(\rho - \tau)\, d\rho \tag{3.8}$$

Substituting the integral variable with $\xi = \rho - \tau$ yields the state-space equation below:

$$z(t) = e^{A\tau}x(t) + \int_{t-\tau}^{t} e^{A(t-\xi)}Bu(\xi)\, d\xi \tag{3.9}$$

The state-space equation for $z(t)$ may then be written as:

$$\begin{aligned} \dot{z}(t) = {} & e^{A\tau}\big(Ax(t) + Bu(t - \tau)\big) \\ & + \left[Bu(t) - e^{A\tau}Bu(t - \tau) + A\int_{t-\tau}^{t} e^{A(t-\xi)}Bu(\xi)\, d\xi\right] \end{aligned} \tag{3.10}$$

Or in the form of a linear, delayless state-space equation:

$$\dot{z}(t) = Az(t) + Bu(t) \tag{3.11}$$

This formulation has the advantage of allowing for the use of the so-called “classical” state-feedback control approach. When implementing the predictive control algorithm described by equation (3.9), it is preferable to perform the variable substitution $\gamma = \xi - t$:

$$z(t) = e^{A\tau}x(t) + \int_{-\tau}^{0} e^{-A\gamma}Bu(t+\gamma)\,d\gamma \tag{3.12}$$

then apply the Laplace transform:

$$Z(s) = e^{A\tau}X(s) + \int_{-\tau}^{0} e^{-A\gamma}Be^{sI\gamma}U(s)\,d\gamma \tag{3.13}$$

and finally carry out the variable substitution $\theta = -\gamma$:

$$Z(s) = e^{A\tau}X(s) + \left(\int_{0}^{\tau} e^{-(sI-A)\theta}B\,d\theta\right)U(s) \tag{3.14}$$

The detailed block diagram of the predictive control system is presented in Figure 3.5 (a), while the simplified model of the equations that result from the variable substitutions is presented in Figure 3.5 (b).

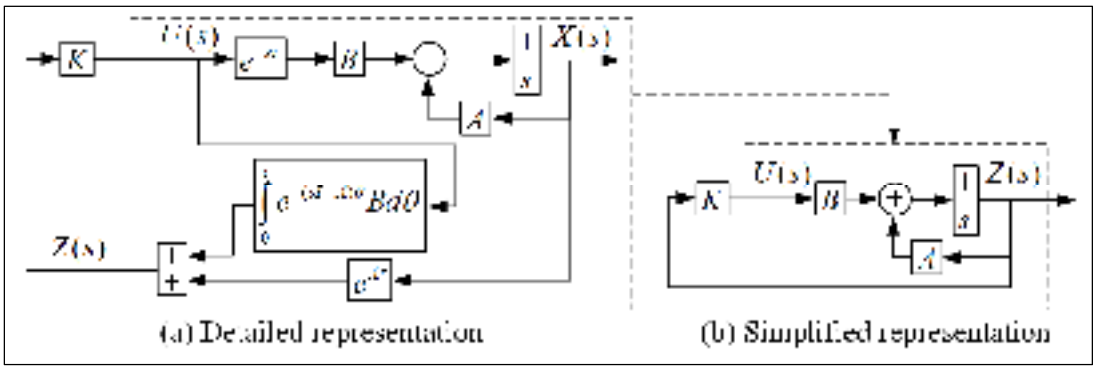

Figure 3.5 Predictive control block diagram

3.3.2 Application to PHIL system: predictive control of ROS

The system used to develop the predictive control system (shown in Figure 3.6) is based on the circuit shown in Figure 0.4, to which three changes have been made. The first change is the addition of a parallel resistor Rp (Rp = $1x10^6$ Ω) to obtain the state-space representation of the circuit. The second change involves applying a delay to Vs(t). This change is due to a limitation required for predictive control, based on the assumption that all inputs are applied with the same time delay. Finally, the time delay τ represents the total (round-trip) delay experienced by the signal between the ROS and DUT.

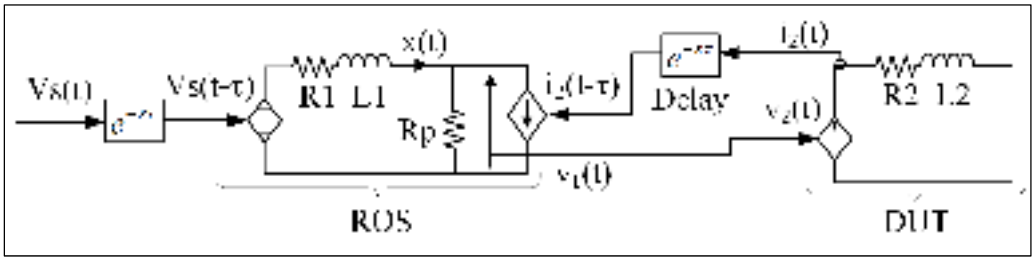

Figure 3.6 Electrical circuit used to achieve predictive control

Since the ROS is known in practice, the predictor will be located on the DUT side, using the predicted ROS values. The ROS state-space representation is given by:

$$\dot{x}(t) = \underbrace{\frac{-(R1+Rp)}{L1}}_{A} x(t) + \underbrace{\begin{bmatrix} \frac{Rp}{L1} & \frac{1}{L1} \end{bmatrix}}_{B} \underbrace{\begin{bmatrix} i_2(t-\tau) \\ Vs(t-\tau) \end{bmatrix}}_{U(t-\tau)} \tag{3.15}$$

$$v_1(t) = Rp(x(t) - i_2(t-\tau))$$

where x represents the current through inductor L1.

The goal here is to predict state variable x at time $t + \tau$, thus allowing for the calculation of the prediction to be applied to signal $v_2(t)$. Using equation (3.14), it is possible to obtain:

$$Z(s) = \underbrace{e^{\frac{-(R1+Rp)}{L1}\tau}}_{A_\tau} X(s) + \left(\frac{L1\left(1-e^{\frac{-(R1+Rp)}{L1}\tau}\cdot e^{-s\tau}\right)}{R1+Rp+L1\cdot s} \right) \cdot \begin{bmatrix} \frac{Rp}{L1} & \frac{1}{L1} \end{bmatrix} \begin{bmatrix} I_2(s) \\ Vs(s) \end{bmatrix} \tag{3.16}$$

$$V_2(s) = Rp(Z(s) - I_2(s))$$

The closed-loop predictive control block diagram is shown in Figure 3.7. Note that, in this system, the "controller" is the DUT (rather than a state-feedback control system) and the "process" is the ROS.

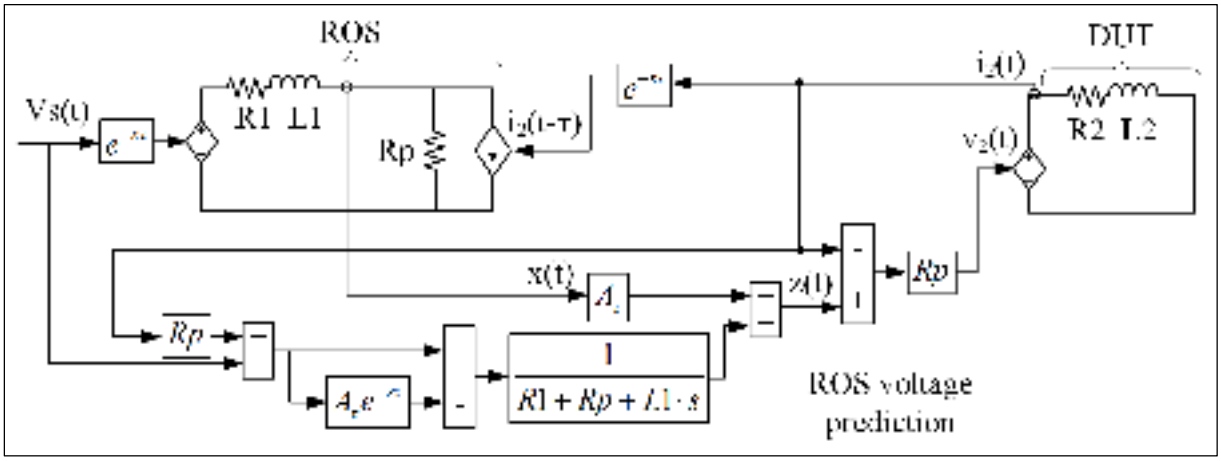

Figure 3.7 Predictive control of ROS

Simulation results for the set of parameters for Case 2 in Table 2.1 (shown in Figure 3.8) reveal a perfect match between the predictive model and the undecoupled reference model.

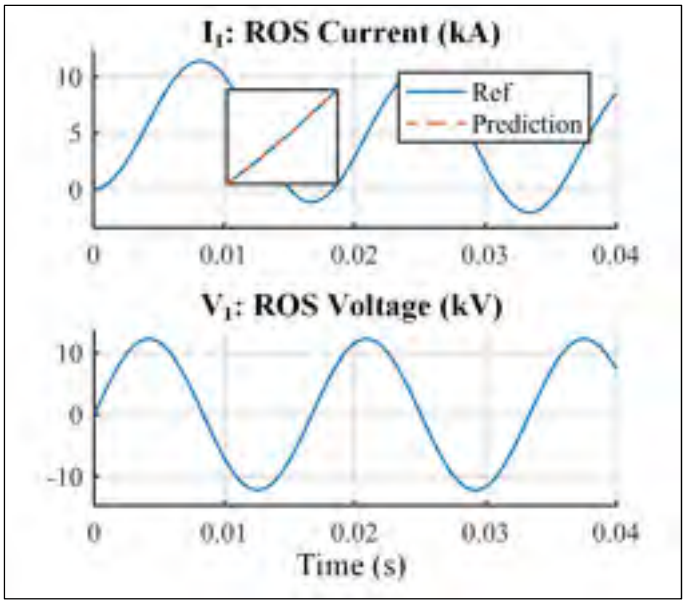

Figure 3.8 Results – Predictive control

3.3.3 Discussion

An analysis of the stability of this closed-loop system—based on the direct method (Fridman, 2014)—has shown it to be stable, regardless of time delay τ. Hence, if the ROS and the DUT are naturally stable, the closed-loop predictive control system will also be stable. Although this method seems promising and has yielded excellent results, it cannot be applied to an actual PHIL system for the following reasons:

- $x(t)$ and $i_2(t)$ must be available at the same time, which is not the case since there is a communication delay between the two systems (due to the ADC and DAC blocks).
- The use of measurement $i_2(t)$ to calculate $v_2(t)$ must be instantaneous (i.e. no delay between the two signals). This is impossible since the predictive control system will be implemented using a digital system (FPGA or microcontroller) that will add a delay in the loop.
- Predictive control assumes that the whole system is continuous. In practice, both the ROS and the implementation of the control system will be discrete.
- A delay must be added to voltage source $Vs(t)$, which is unacceptable.
- The exponent of matrix A may be difficult or impossible to calculate for a complex, non-linear and time-variable system.

For all these reasons, this avenue has not been pursued. However, it would be worthwhile to address some of its limitations in future work.

3.4 Comparison of digital interface algorithms for PHIL applications

Table 3.1 presents a comparison of all the digital interface algorithms (DIAs) discussed so far, i.e. those that have been presented in the literature review and those that have been explored in this chapter. For each algorithm, a qualitative assessment is provided in regard to their stability, the feasibility of their implementation with PHIL systems and their ease of use. The last column indicates why the DIA is not suitable to our typical uses.

Table 3.1 Digital interface algorithm (DIA) comparison table

DIA	Stability	PHIL implementation	Ease of use	Comments
Ideal transformer	**	*****	***	Very easy to use, but stability is too dependent on DUT and ROS
Partial duplication	***	***	***	Very stable, but requires a large coupling impedance, which is unrealistic
Damping impedance	$***^{1/2}$	**	**	Very stable, but requires real-time measurement of DUT impedance
First-order approximation	***	**	**	Requires real-time measurement of DUT impedance and assumes linear and passive DUT
Transmission line	*****	*	****	Always stable, but the addition of a large resistor on the DUT side turns this method unusable in its current state
DQ transform	****	****	****	Only models phenomena around 60 Hz

DIA	Stability	PHIL implementation	Ease of use	Comments
Explicit discretization	**	****	***	Stability is too dependent on DUT and ROS
ITM–filtering	***	****	**	Too specific to the filter frequency and DUT/ROS
ITM–implicit Euler	***	****	**	Stability is too dependent on DUT and ROS
ITM–FOH	*	****	**	Unstable
Predictive control	***	*	*	Too specific to ROS parameters; control application delay makes system unstable

3.5 Conclusions

In this chapter, various methods have been explored in search of a method to interface two decoupled electrical circuits. Although this research work has not yielded a new DIA applicable to PHIL systems, it has underscored the challenge faced when attempting to develop an algorithm that is stable, accurate, flexible and generally applicable. This difficult stems in fact from the fact that all DIAs (except for the transmission line method) violate energy conservation laws, which makes them susceptible to instabilities.

On the other hand, the transmission line decoupling method is always stable, accurate and flexible since it is based on the laws of physics. Unfortunately, in its current state, it is not suitable for PHIL systems due to the resistor that must be added at the amplifier output, which proves extremely limiting for the reasons set out in section 1.3.5. What is therefore suggested is to make major changes to this method to allow for its efficient, flexible and generalized implementation in PHIL systems. These changes will be discussed in detail in the next chapter.

CHAPTER 4

DEVELOPMENT OF A NEW TRANSMISSION LINE-BASED INTERFACE METHOD

4.1 Introduction

Transmission lines are a key component of long-distance power transmission systems or their interconnections. Their modeling and simulation have been well understood and tested since the end of the 1960s, when a transmission line model was implemented for the first time in electromagnetic transient (EMT) simulation software (Dommel, 1969).

As mentioned in section 1.3.5, the propagation delay associated with the physical behavior of transmission lines can also be used to separate calculation tasks, thus allowing for the real-time simulation of large-scale power systems (Do et al., 1999; Gagnon et al., 2010). In the case of PHIL systems, the transmission line model (TLM) could be used to subsume (or absorb) any delays between the ROS and the DUT within the line propagation delay, which would make possible an energy-conserving (hence physically stable) decoupling of the two systems. Unfortunately, the need to add a series resistor (used to represent the characteristics impedance of the line) at the output of the power amplifier has made this method impossible to implement until now.

This chapter sets out in detail a new TLM implementation based on the Bergeron model, which does not require the addition of any physical resistor (Tremblay et al., 2020). First, the transmission line model is reviewed, along with the implementation proposed by Bergeron. Major modifications to its implementation are then proposed to allow for its use as a PHIL system interface. Finally, work to validate the new implementation and an analysis of its stability are presented.

4.2 Transmission line model

A transmission line can be modeled using the telegraph equations (Marti, Marti, & Dommel, 1993), which treat the line as a sum of infinitesimal constant RLC components uniformly distributed along the line, as shown in Figure 4.1. The two ends of the line (the sending and the receiving ends) are separated by a distance *l*, which is subdivided into Δx elements that contain a series branch (resistor R and inductor L) and a parallel branch (capacitor C and conductor G).

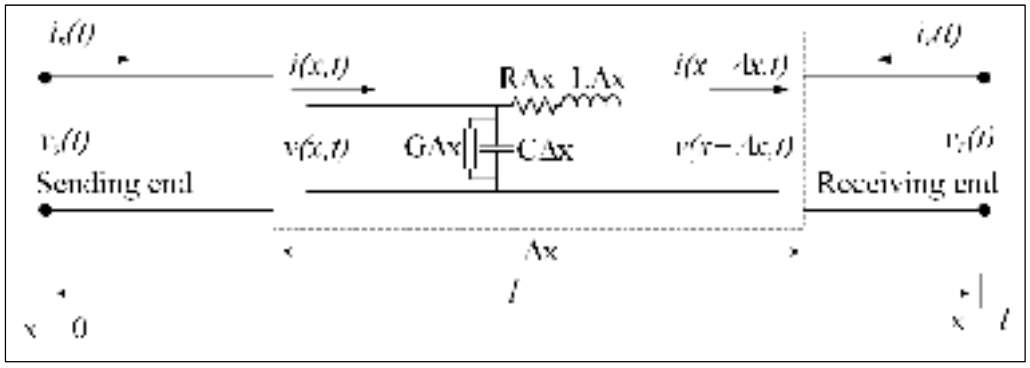

Figure 4.1 Distributed-parameter transmission line model

At every point of the line, the current and the voltage can be defined using the following partial differential equations in the Laplace domain:

$$\frac{\partial V(x,s)}{\partial x} = -(R + sL)I(x,s) \tag{4.1}$$

$$\frac{\partial I(x,s)}{\partial x} = -(G + sC)V(x,s) \tag{4.2}$$

Differentiating equations (4.1) and (4.2) with respect to x yields the equations below:

$$\frac{\partial^2 V(x,s)}{\partial x^2} = -(R + sL)\frac{\partial I(x,s)}{\partial x} \tag{4.3}$$

$$\frac{\partial^2 I(x,s)}{\partial x^2} = -(G + sC)\frac{\partial V(x,s)}{\partial x} \tag{4.4}$$

The substitution of equation (4.2) in (4.3) and equation (4.1) in (4.4) results in partial differential equations that have the same form as the wave equation:

$$\frac{\partial^2 V(x,s)}{\partial x^2} = \gamma(s)^2 V(x,s) \tag{4.5}$$

$$\frac{\partial^2 I(x,s)}{\partial x^2} = \gamma(s)^2 I(x,s) \tag{4.6}$$

Where $\gamma(s)$ is the line propagation constant as a function of frequency:

$$\gamma(s) = \sqrt{(R + sL)(G + sC)} = \alpha(\omega) + j\beta(\omega) \tag{4.7}$$

Where α is the damping constant and β is the phase constant. The d'Alembert solutions for the voltage wave V(x) and the current wave I(x) in the Laplace domain are given below:

$$V(x,s) = V^+(s)e^{-x\gamma} + V^-(s)e^{x\gamma} \tag{4.8}$$

$$I(x,s) = I^+(s)e^{-x\gamma} + I^-(s)e^{x\gamma} \tag{4.9}$$

Where V^+ and I^+ are the forward waves, and V^- and I^- are the backward waves. From equation (4.2), we know that:

$$\frac{\partial}{\partial x}(I^+(s)e^{-x\gamma} + I^-(s)e^{x\gamma}) = -(G + sC)(V^+(s)e^{-x\gamma} + V^-(s)e^{x\gamma}) \tag{4.10}$$

$$\gamma(-I^+(s)e^{-x\gamma} + I^-(s)e^{x\gamma}) = -(G + sC)(V^+(s)e^{-x\gamma} + V^-(s)e^{x\gamma}) \tag{4.11}$$

Through the identification of the $e^{-x\gamma}$ and $e^{x\gamma}$ terms in equation (4.11), it is possible to make the deduction below:

$$-\gamma I^{+}(s) = -(G + sC)V^{+}(s) \xrightarrow{thus} V^{+}(s) = Z_c I^{+}(s) \tag{4.12}$$

$$\gamma I^{-}(s) = -(G + sC)V^{-}(s) \xrightarrow{thus} V^{-}(s) = -Z_c I^{-}(s) \tag{4.13}$$

where $Z_c = \sqrt{\frac{R+sL}{G+sC}}$

Equations (4.8) and (4.9) can then be written as:

$$V(x,s) = Z_c(I^{+}(s)e^{-x\gamma} - I^{-}(s)e^{x\gamma}) \tag{4.14}$$

$$I(x,s) = I^{+}(s)e^{-x\gamma} + I^{-}(s)e^{x\gamma} \tag{4.15}$$

The general solution of these equations—which contain the expression $e^{k\sqrt{s}}$ (stemming from the γ term)—falls under the theory associated with the diffusion equation. There is no analytic solution to this equation—used to study heat transfer among other things—since the damping constant α is a function of frequency (Martí, 1980).

4.2.1 Solution for lossless line

If line losses are neglected, i.e. setting R = 0 Ω and G = 0 Ω^{-1}, the propagation constant (where the attenuation factor α is nil) and the characteristic impedance (which is now strictly real) become:

$$\gamma = \sqrt{(R + sL)(G + sC)} = s\sqrt{LC} = j\beta \tag{4.16}$$

$$Z_c = \sqrt{\frac{R + sL}{G + sC}} = \sqrt{\frac{L}{C}} \tag{4.17}$$

Substituting (4.16) and (4.17) in (4.14) and (4.15) yields:

$$V(x,s) = Z_c\left(I^+(s)e^{-xs\sqrt{LC}} - I^-(s)e^{xs\sqrt{LC}}\right) \tag{4.18}$$

$$I(x,s) = I^+(s)e^{-xs\sqrt{LC}} + I^-(s)e^{xs\sqrt{LC}} \tag{4.19}$$

Using the time delay property of the inverse Laplace transform, it is possible to obtain a time-domain solution for the voltage and current at any point along the line:

$$v(x,t) = Z_c\left(i^+\left(t - x\sqrt{LC}\right) - i^-\left(t + x\sqrt{LC}\right)\right) \tag{4.20}$$

$$i(x,t) = i^+\left(t - x\sqrt{LC}\right) + i^-\left(t + x\sqrt{LC}\right) \tag{4.21}$$

4.2.2 Special lossy line case: distortionless line

In practice, transmission line losses must be considered to properly model the damping that is in general observed over the line. A simple way of modeling this damping consists in using the Heaviside condition (Hartree & Porter, 1938). Named for Olivier Heaviside, this condition must be satisfied by a transmission line if there is to be no distortion of the transmitted signal. To eliminate distortion, the damping constant α in equation (4.7) must not depend on frequency. To achieve this, the following condition must be satisfied:

$$\frac{L}{R} = \frac{C}{G} \tag{4.22}$$

Applying this condition, equation (4.7) then becomes:

$$\gamma = \sqrt{R(1+s\frac{L}{R})G(1+s\frac{C}{G})} = \underbrace{\sqrt{RG}}_{\alpha} + \underbrace{s\sqrt{LC}}_{j\beta} \tag{4.23}$$

The damping constant α is then real and no longer a function of frequency. Hence, equations (4.14) and (4.15) become:

$$V(x,s) = Z_c\left(I^+(s)e^{-x\sqrt{RG}}e^{-xs\sqrt{LC}} - I^-(s)e^{x\sqrt{RG}}e^{xs\sqrt{LC}}\right) \tag{4.24}$$

$$I(x,s) = I^+(s)e^{-x\sqrt{RG}}e^{-xs\sqrt{LC}} + I^-(s)e^{x\sqrt{RG}}e^{xs\sqrt{LC}} \tag{4.25}$$

The forward I^+ and backward I^- waves are then attenuated by the coefficient $e^{\pm x\sqrt{RG}}$. The time-domain equations become:

$$v(x,t) = Z_c\left(e^{-x\sqrt{RG}}i^+\left(t - x\sqrt{LC}\right) - e^{x\sqrt{RG}}i^-\left(t + x\sqrt{LC}\right)\right) \tag{4.26}$$

$$i(x,t) = e^{-x\sqrt{RG}}i^+\left(t - x\sqrt{LC}\right) + e^{x\sqrt{RG}}i^-\left(t + x\sqrt{LC}\right) \tag{4.27}$$

These equations will be used to derive an electrical model of the time-domain behavior of line voltages and current.

4.3 Bergeron model

Louis Bergeron has developed a model (Bergeron, 1950), called “Bergeron transmission-line model” (BTLM), which models wave propagation over a line using a simple electrical interface at both ends. Although the literature contains a detailed description of the use of this method (Dommel, 1969) to model a lossless line (R = 0 Ω and G = 0 Ω^{-1}), this section will deal with the case of a lossy but distortionless line. Before going any further, it is important to note that the variables used in this section refer to Figure 4.1.

4.3.1 Forward wave

The line voltage depends on the forward i^+ and backward i^- current waves. To eliminate the dependence on i^-, the term $Z_c i(x,t)$ is added to equation (4.26) and the substitution $tt = t$ yields:

$$v(x,tt) + Z_c i(x,tt) = 2Z_c e^{-x\sqrt{RG}} i^+\left(tt - x\sqrt{LC}\right) \tag{4.28}$$

An observer traveling at the same speed (v = $1/\sqrt{LC}$) and in the same direction as i^+ would observe a constant forward wave as shown in Figure 4.2. The position of this observer is then given by $x(t) = v \cdot (tt - t + \tau)$.

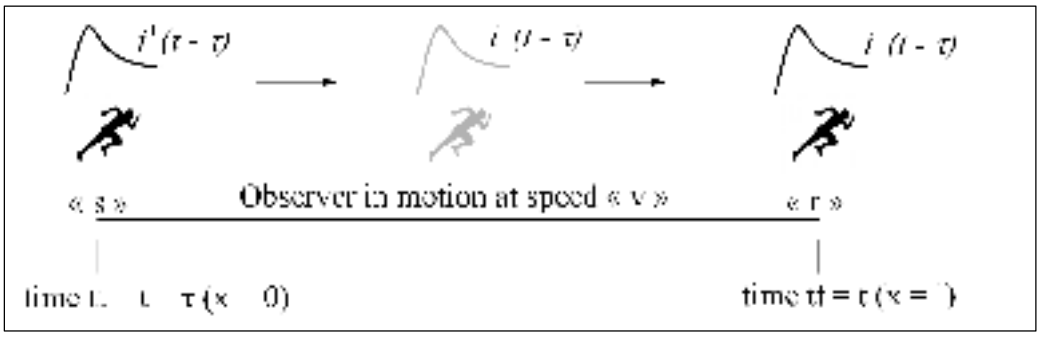

Figure 4.2 Forward wave observer

Hence, the observer would take τ second ($\tau = l/v = l\sqrt{LC}$) to reach the other end of the line:

1. When the observer is at the "s" end (i.e. $x = 0$) at time $tt = t - \tau$:

$$v_s(t-\tau) + Z_c i_s(t-\tau) = 2Z_c i^+(t-\tau) \tag{4.29}$$

2. When the observer is at the "r" end (i.e. $x = $ l) at time $tt = t$:

$$v_r(t) - Z_c i_r(t) = 2Z_c e^{-l\sqrt{RG}} i^+\left(t - \underbrace{l\sqrt{LC}}_{\tau}\right) \tag{4.30}$$

Please note that the forward wave is the same in both cases ($i^+(t-\tau)$). Combining equations (4.29) and (4.30) then yields:

$$v_r(t) - Z_c i_r(t) = \underbrace{e^{-l\sqrt{RG}}}_{K_{at}} (v_s(t-\tau) + Z_c i_s(t-\tau)) \tag{4.31}$$

The attenuation factor K_{at} thus reduces the magnitude of the forward wave exponentially. If R = 0 Ω and G = 0 Ω^{-1}, the original form of the Bergeron equation is recovered since K_{at} = 1.

4.3.2 Backward wave

Let's now subtract $Z_c i(x,t)$ from equation (4.26) to eliminate the dependence on i^+, and substitute $tt = t$:

$$v(x,tt) - Z_c i(x,tt) = -2Z_c e^{x\sqrt{RG}} i^-\left(tt + x\sqrt{LC}\right) \tag{4.32}$$

In this case, an observer traveling at the same speed and in the same direction as i^- would observe a constant backward wave as shown in Figure 4.3. The position of this observer is then given by $x(t) = v \cdot (-tt + t - \tau) + l$.

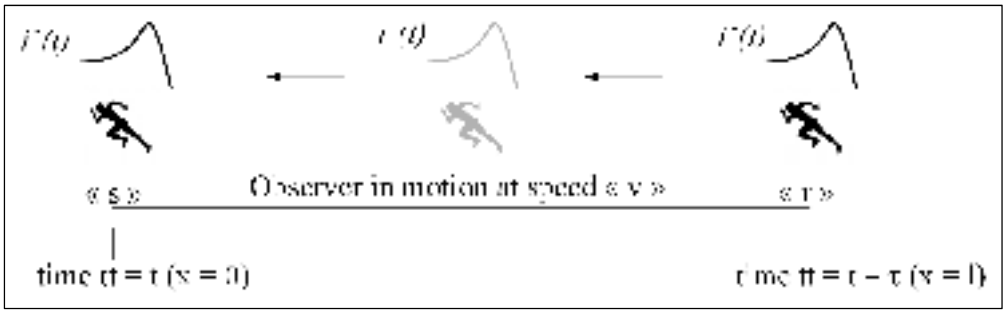

Figure 4.3 Backward wave observer

Hence, the observer would also take τ second to reach the other end of the line:

1. When the observer is at the "r" end (i.e. $x = l$) at time $tt = t - \tau$:

$$v_r(t-\tau) + Z_c i_r(t-\tau) = -2Z_c e^{l\sqrt{RG}} i^-\left(t \underbrace{-\tau + l\sqrt{LC}}_{0}\right) \tag{4.33}$$

2. When the observer is at the "s" end (i.e. $x = 0$) at time $tt = t$:

$$v_s(t) - Z_c i_s(t) = -2Z_c i^-\left(t + \underbrace{l\sqrt{LC}}_{0}\right) \tag{4.34}$$

Please note that the backward wave is the same in both cases ($i^-(t)$). Combining equations (4.33) and (4.34) then yields:

$$v_r(t-\tau) + Z_c i_r(t-\tau) = e^{l\sqrt{RG}}(v_s(t) - Z_c i_s(t)) \tag{4.35}$$

$$\Longrightarrow v_s(t) - Z_c i_s(t) = \underbrace{e^{-l\sqrt{RG}}}_{K_{at}} (v_r(t-\tau) + Z_c i_r(t-\tau)) \tag{4.36}$$

Equation (4.36) includes the same attenuation factor K_{at} as equation (4.31).

4.3.3 Electrical model

In a nodal method-based simulator, such as Hypersim, it is preferable to implement the Bergeron model using a current wave rather than a voltage wave. To do so, equations (4.31) and (4.36) are divided by Z_c:

$$\frac{v_s(t)}{Z_c} - i_s(t) = \underbrace{K_{at}\left(\frac{v_r(t-\tau)}{Z_c} + i_r(t-\tau)\right)}_{w_s(t),\, u_r(t-\tau)} \tag{4.37}$$

$$\frac{v_r(t)}{Z_c} - i_r(t) = \underbrace{K_{at}\left(\frac{v_s(t-\tau)}{Z_c} + i_s(t-\tau)\right)}_{w_r(t),\, u_s(t-\tau)} \tag{4.38}$$

Signals $w_s(t)$ and $u_r(t-\tau)$ represent the backward current wave on the sending-end of the line while $w_r(t)$ and $u_s(t-\tau)$ represent the forward current wave on the receiving-end of the line. The electrical diagram corresponding to these equations is presented in Figure 4.4. Both ends of the line are illustrated (i.e. The sending-end and the receiving-end).

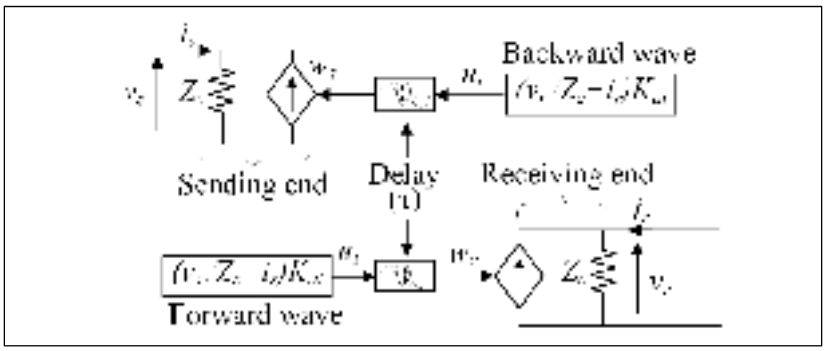

Figure 4.4 Electrical diagram of Bergeron model for lossy line

Although this implementation—with current sources at both ends of the line—is suitable for modeling a line on a digital simulator, it cannot be used directly to interface a PHIL system. However, it provides a starting point that can be adapted to PHIL applications as will be shown in the next section.

4.3.4 Intuitive implementation approach for PHIL systems

Intuitively, the Bergeron model could be implemented in a PHIL system by dividing the system in two parts (DUT and ROS) as shown in Figure 4.5. The sending-end of the line would be implemented in the real-time simulator (RTS)—using equation (4.37)— and would be connected to the ROS simulation model. The receiving-end of the line would be a physical system comprising a power amplifier (PA) series connected to a resistor Z_c used to supply power to the DUT. For MVA-scale PHIL systems, this voltage source would not be a linear amplifier; instead, it would be a pulse-width modulation (PWM) based voltage source converter (VSC). This type of converter—relying on electronic switching—would also require an output filter to smooth the voltage applied to the DUT.

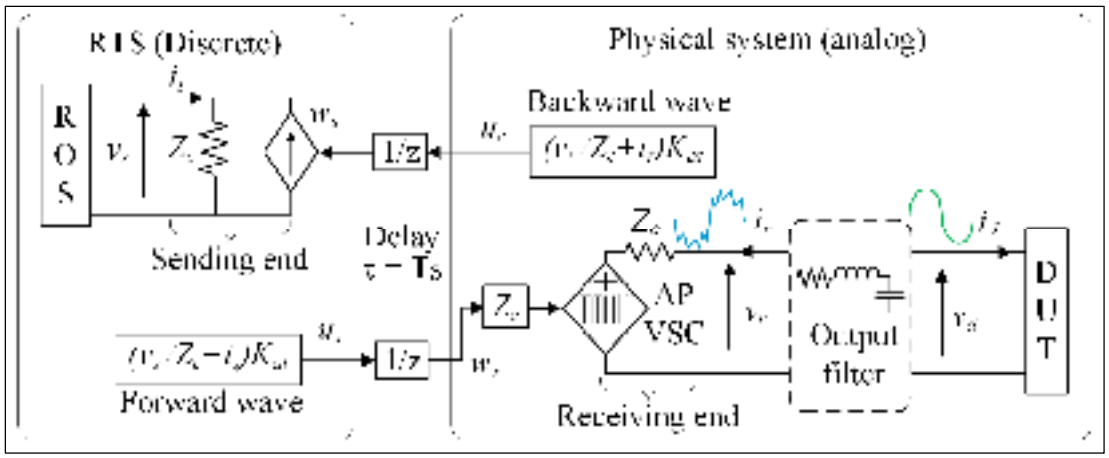

Figure 4.5 Electrical diagram of Bergeron model with losses (PHIL)

In an actual implementation, signals are exchanged between the RTS and the physical system synchronously at the RTS sampling rate (Ts). Therefore, there will be a time delay equal to one calculation step (Ts) for the forward wave, corresponding to the RTS execution time, and an identical time delay for the backward wave, corresponding to the sampling effect. The existence of this time delay provides an additional justification relying on the BTLM to interface a PHIL system since it can be understood to represent the delay associated with the round-trip propagation of waves over a distributed parameter transmission line. The parameters per unit of transmission line length can be calculated from τ and Z_c using the equations below:

$$\begin{aligned} Z_c &= \sqrt{L/C} \\ \tau &= Ts = \sqrt{LC} \end{aligned} \longrightarrow \begin{aligned} L &= Z_c \cdot Ts \\ C &= Ts^2/L \end{aligned} \tag{4.39}$$

At this stage, two major limitations still stand in the way of a practical implementation of a BTLM interface for a PHIL system:

- As indicated in section 1.3.5, the addition of an actual resistor on the receiving-end of the line entails the oversizing of the power amplifier power and voltage ratings by 350% for our use case. There are additional design constraints linked to the cooling of this resistor, the amplifier volume and voltage insulation.

- Another issue is the generation of high-frequency harmonics in current i_r (shown in blue in Figure 4.5) due to the power amplifier voltage source converter (PA-VSC) switching frequency. This harmonic current must not be injected in the backward wave since it is an artifact that would not be present if an ideal power amplifier were used.

A major contribution of this dissertation is therefore a new implementation of the BTLM interface designed to overcome these limitations. This new implementation is described in detail in the next sections.

4.4 New implementation of Bergeron model for PHIL systems

To allow for the use of the BTLM as an interface for PHIL applications, it is proposed to add a fast control loop between the sending-end and the receiving-end of the line, as shown in Figure 4.6. The purpose of this control system is to emulate the behavior of resistor Z_c, eliminate PWM harmonics from current i_r and compensate for the internal resistance of the power amplifier. This additional control loop also includes algorithms designed to handle the sampling rate transition between the CPU and the FPGA, especially for the forward wave. This new digital interface algorithm (DIA)—named BTLM-PHIL—allows for the use of the Bergeron model in a hybrid application without adding a physical resistor on the receiver-end.

One of the key factors that enable the implementation of the BTLM-PHIL system is the FPGA, which is closely connected and synchronized with the real-time simulator. This FPGA is in fact already being used to provide the PA-VSC PWM generator and to manage inputs and outputs (digital-analog converters or DACs and analog-digital converters or ADCs). Thus, these interfaces do not introduce additional time delays.

Each element of the BTLM-PHIL digital interface algorithm is described in detail in the subsections below: (1) Output filter and characteristic impedance emulator (OFCIE); (2) R_f internal resistance compensator; (3) forward wave resampling; and (4) backward wave calculation.

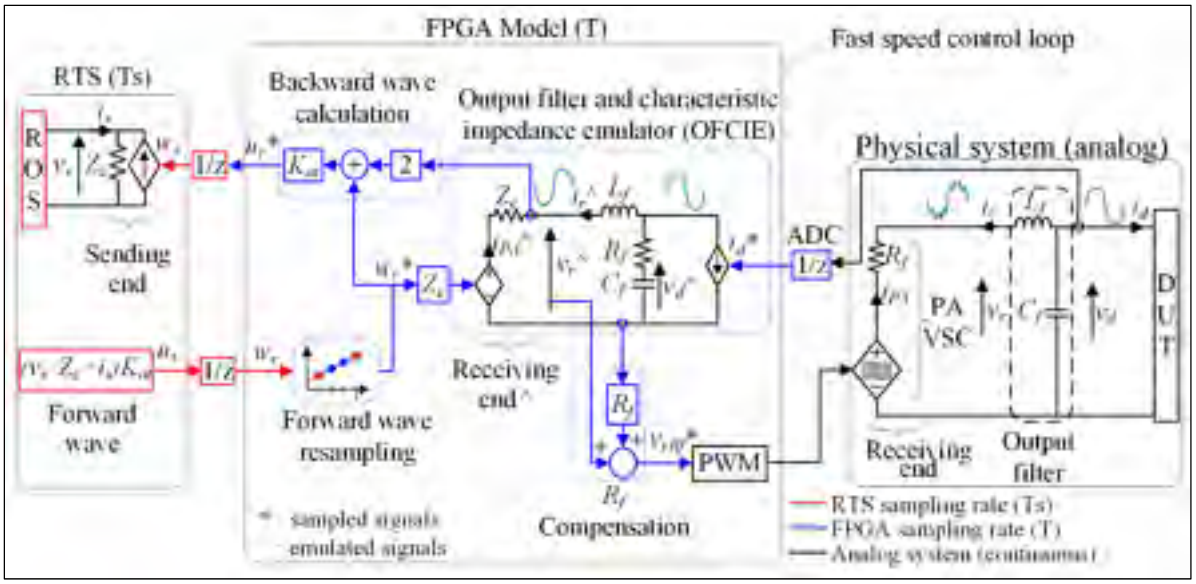

Figure 4.6 Implementation of the new BTLM-PHIL interface

4.4.1 Output filter characteristic impedance emulator (OFCIE)

The main technique proposed to emulate the behavior of resistor Z_c and obtain measurement signals that are free of switching harmonics consists in duplicating the output filter in the FPGA while adding to it resistance Z_c and damping resistance R_f in series with the capacitor (this resistance is discussed in section 4.4.2). By using an ideal voltage source (for the forward voltage wave) and measuring DUT current i_d*, it is possible to eliminate PWM harmonics almost completely from current i_r (required to calculate the backward wave) and reference voltage v_r (required by the PWM generator). In this way, the effect of resistance Z_c is now simulated within the FPGA emulator instead of adding it physically at the amplifier output, thus solving the problems raised in section 1.3.5.

The state-space representation of the proposed emulator—which replicates the LC filter used at the PA-VSC output and contains resistances Z_c and R_f–is presented in equation (4.40). There are two inputs: w_r*, which represents the forward wave originating from the sending-end; and i_d*, which represents the sampled DUT current. There are also two outputs: the desired receiving-end voltage v_r^ (used as a reference for the PWM generator) and current i_r^, required

for the backward wave calculation. The state variables are v_d^ (voltage at the terminals of capacitor C_f) and i_r^ (current through inductor L_f).

$$\underbrace{\begin{bmatrix} \dot{i}_r^{\wedge} \\ \dot{v}_d^{\wedge} \end{bmatrix}}_{\dot{X}} = \underbrace{\begin{bmatrix} \frac{-Z_c - R_f}{L_f} & \frac{1}{L_f} \\ \frac{-1}{C_f} & 0 \end{bmatrix}}_{A} \underbrace{\begin{bmatrix} i_r^{\wedge} \\ v_d^{\wedge} \end{bmatrix}}_{X} + \underbrace{\begin{bmatrix} \frac{-Z_c}{L_f} & \frac{-R_f}{L_f} \\ 0 & \frac{-1}{C_f} \end{bmatrix}}_{B} \underbrace{\begin{bmatrix} w_r^{*} \\ i_d^{*} \end{bmatrix}}_{U} \tag{4.40}$$

$$\underbrace{\begin{bmatrix} v_r^{\wedge} \\ i_r^{\wedge} \end{bmatrix}}_{Y} = \underbrace{\begin{bmatrix} Z_c & 0 \\ 1 & 0 \end{bmatrix}}_{C} \underbrace{\begin{bmatrix} i_r^{\wedge} \\ v_d^{\wedge} \end{bmatrix}}_{X} + \underbrace{\begin{bmatrix} Z_c & 0 \\ 0 & 0 \end{bmatrix}}_{D} \underbrace{\begin{bmatrix} w_r^{*} \\ i_d^{*} \end{bmatrix}}_{U}$$

This state-space representation is discretized using the trapezoidal method, according to equation (4.41), to be eventually implemented in the FPGA. Please note that the sampling period (T) is set by the FPGA ADC to 2.5 µs.

$$X_k = \underbrace{(I - \tfrac{1}{2}AT)^{-1} \cdot \left(I + \tfrac{1}{2}AT\right)}_{Ad} \cdot X_{k-1} + \underbrace{(I - \tfrac{1}{2}AT)^{-1} \cdot (\tfrac{1}{2}BT)}_{Bd} \cdot (U_k + U_{k-1}) \tag{4.41}$$

$$Y_k = C \cdot X_k + D \cdot U_k$$

4.4.2 PA-VSC internal resistance compensator

In practice the PA-VSC is a voltage source with a series internal resistance, represented using resistor R_f shown in the general block diagram in Figure 4.6. The presence of this resistor in the inductive branch of the output filter can lead to a significant drop in the voltage applied to the DUT. To mitigate this problem, it is proposed to compensate the voltage drop by increasing the reference voltage applied to the PWM generator:

$$v_{rRf}{}^{\wedge} = v_r{}^{\wedge} + R_f i_{AP}{}^{\wedge} \tag{4.42}$$

If it is assumed that the filter emulator has the same behavior as the output filter (i.e. $i_{AP} = i_{AP}\hat{}$ and $v_d = v_d\hat{}$), this compensation will be exact and will virtually eliminate resistor R_f from the PA-VSC[4]. The filter damping will then be replicated virtually by the filter emulator, which in fact includes resistor R_f in series with its capacitor to maintain the same no-load damping factor while avoiding any voltage drop in the inductive branch.

4.4.3 Forward wave resampling

The output filter characteristic impedance emulator (OFCIE) must receive all its input signals at the same sampling frequency to avoid generating uncharacteristic harmonics due to different sampling periods. In addition, the sampling rate of this emulator must be considerably faster than the real-time simulator (RTS) to allow for the rapid calculation of the reverence voltage v_r^ between RTS samples. This means that a resampling algorithm—such as the function shown in Figure 4.7—is required to process the forward wave w_r.

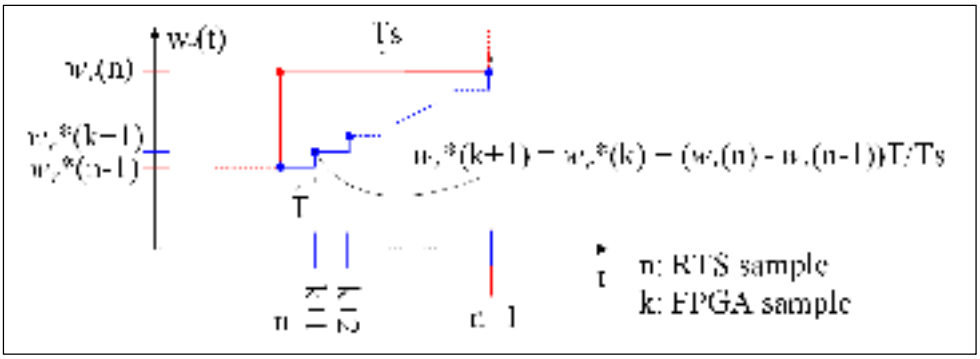

Figure 4.7 Resampling of forward wave originating from the RTS

This linear interpolation-based resampling function is also used to provide a sampling rate transition for the backward wave calculation. Finally, section 4.6.2 will demonstrate how this

[4] In practice, this compensation is applied with a 2.5-µs time delay; it is also filtered to eliminate PWM-related harmonics. This results in a frequency-dependent damping factor, as explained in section 6.5.2.

resampling function is also critical to maintain the passivity (and hence the stability) of the BTLM-PHIL system.

Lastly, it should be noted that this function does not add any additional delay to the BTLM since the backward wave u_r* (calculated using the forward wave) is sampled at the end of the RTS calculation step.

4.4.4 Backward wave calculation

Another BTLM modification required to implement it with a PHIL system involves the calculation of the backward wave. In general, the BTLM requires that voltage v_r be measured at the receiving-end of the line. This voltage cannot be used directly since it contains PA-VSC switching harmonics (this measurement is made upstream of the output filter). This problem can be solved by extracting signal v_r from equation (4.38):

$$v_r(t) = i_r(t)Z_c + w_r(t)Z_c \tag{4.43}$$

Signal u_r from equation (4.37) is then used:

$$u_r(t) = K_{at}\left(\frac{v_r(t)}{Z_c} + i_r(t)\right) = K_{at}\big(w_r(t) + 2i_r(t)\big) \tag{4.44}$$

This approach also avoids the line short-circuit problem that occurs when the PHIL system is started (before the amplifier is activated) since voltage v_r is equal to zero at this moment.

4.5 Validation of new BTLM-PHIL interface

This section aims to validate the performance of the BTLM-PHIL system using reference simulations performed in the *MATLAB/Simulink/SPS* environment. The BTLM-PHIL algorithm diagram presented above in Figure 4.6 has therefore been implemented in this

environment while taking into consideration the various sampling periods involved. As shown in Figure 4.8, the BTLM-PHIL system has been used to interface a RL-type DUT to the ROS. For this validation exercise, the parameters for a single-phase 2.5-MVA 14.4-kV PA-VSC have been used (see Table 4.1). The ROS impedances have been selected to model a very weak power system (SCR = 1) with a mainly resistive load.

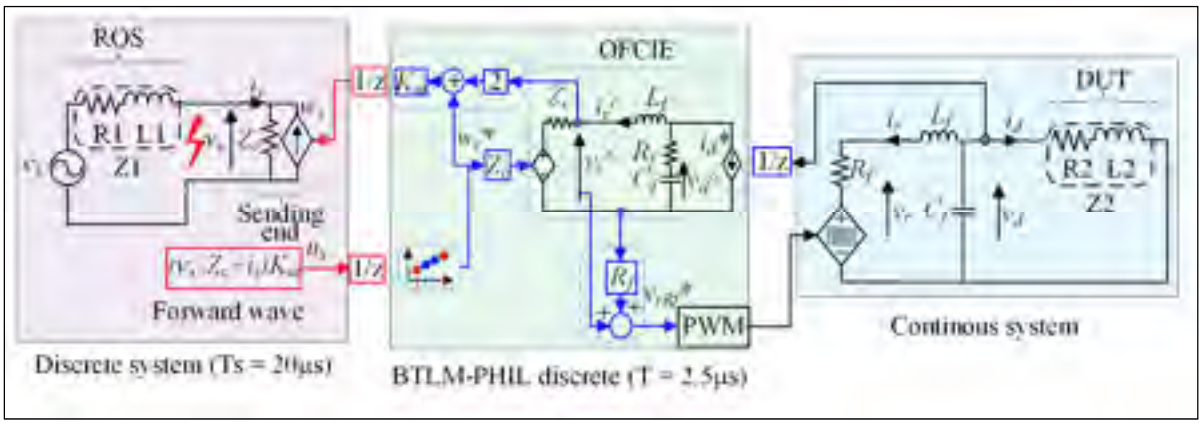

Figure 4.8 BTLM-PHIL simulation model

Table 4.1 Set of parameters used for BTLM-PHIL validation

Parameters	Values
Nominal voltage (line-to-neutral)	v_1 = 14.4 kV
Nominal power (single phase)	2.5 MVA
Characteristic impedance	Z_c = 230 Ω
Output filter (Fc = 7.1 kHz)	L_f = 576 μH, C_f = 869 nF
Damping resistance	R_f = 9.2 Ω
Effective switching frequency[5]	F_{swe} = 30 kHz
Calculation step: (RTS and OFCIE)	Ts = 20 μs, T = 2.5 μs
ROS impedances (Z1) (SCC = 2.43 MVA, X/R = 4)	R1 = 20.74 Ω, L1 = 220 mH
DUT impedances (Z2) (SCC = 2.5 MVA, X/R = 0.05)	R2 = 83 Ω, L2 = 11 mH

[5] The power amplifier comprises 15 cascaded H-bridges. Each H-bridge operates at 1-kHz switching frequency; each carrier phase is offset equidistantly. The total (effective) switching frequency is thus: 15x2x1 kHz = 30 kHz

4.5.1 OFCIE validation

The proposed emulator validation method consists in comparing the output filter signals (i_r and v_d) with the emulated filter signals ($\hat{i_r}$ and $\hat{v_d}$) under normal operating conditions and when a fault is applied on the sending-end of the line. The comparative results (see Figure 4.9) show that the emulated filter signals behave strictly like those of the output filter while eliminating, as expected, the high-frequencies due to the PA-VSC.

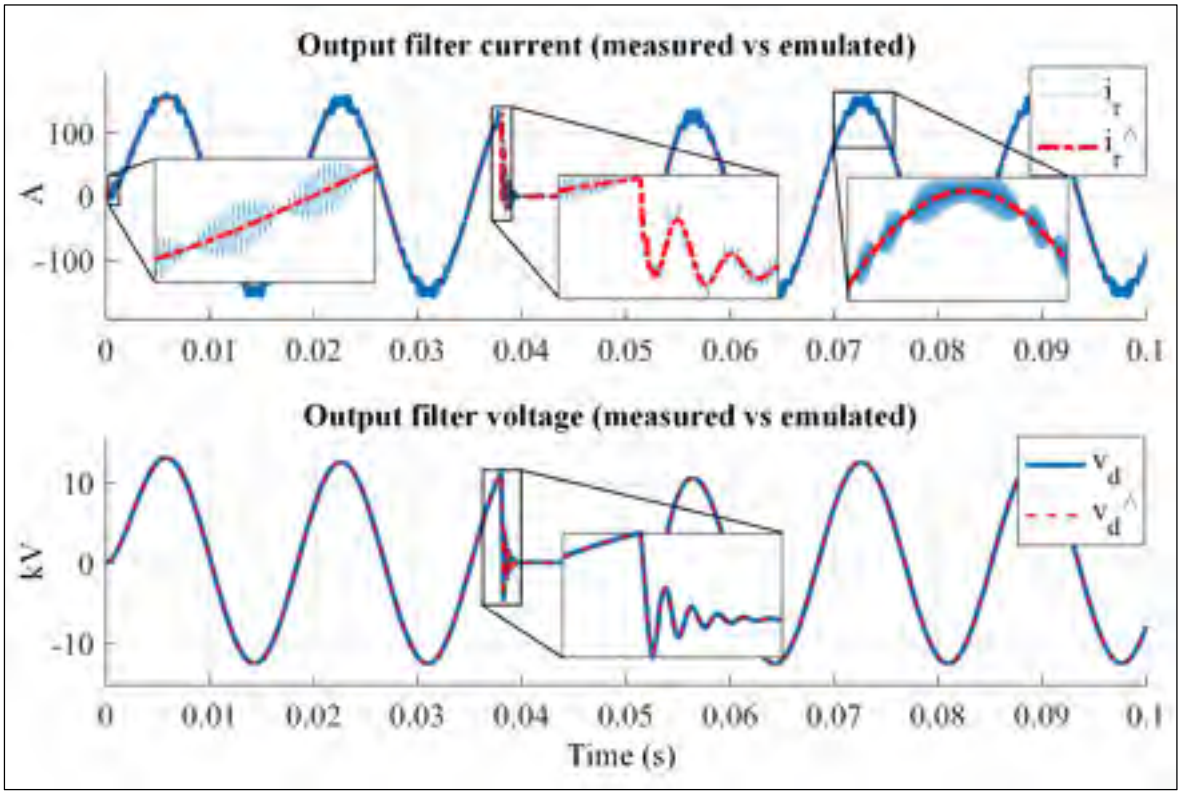

Figure 4.9 OFCIE comparative results

4.5.2 Comparison with reference simulation

To validate the dynamic operation of the BTLM-PHIL interface, simulation results are compared with those obtained for a reference case, as shown in Figure 4.10. The reference case involves the same set of parameters for the ROS, DUT, filter (with capacitive branch damping impedance) and characteristic impedance as those presented in Table 4.1 .

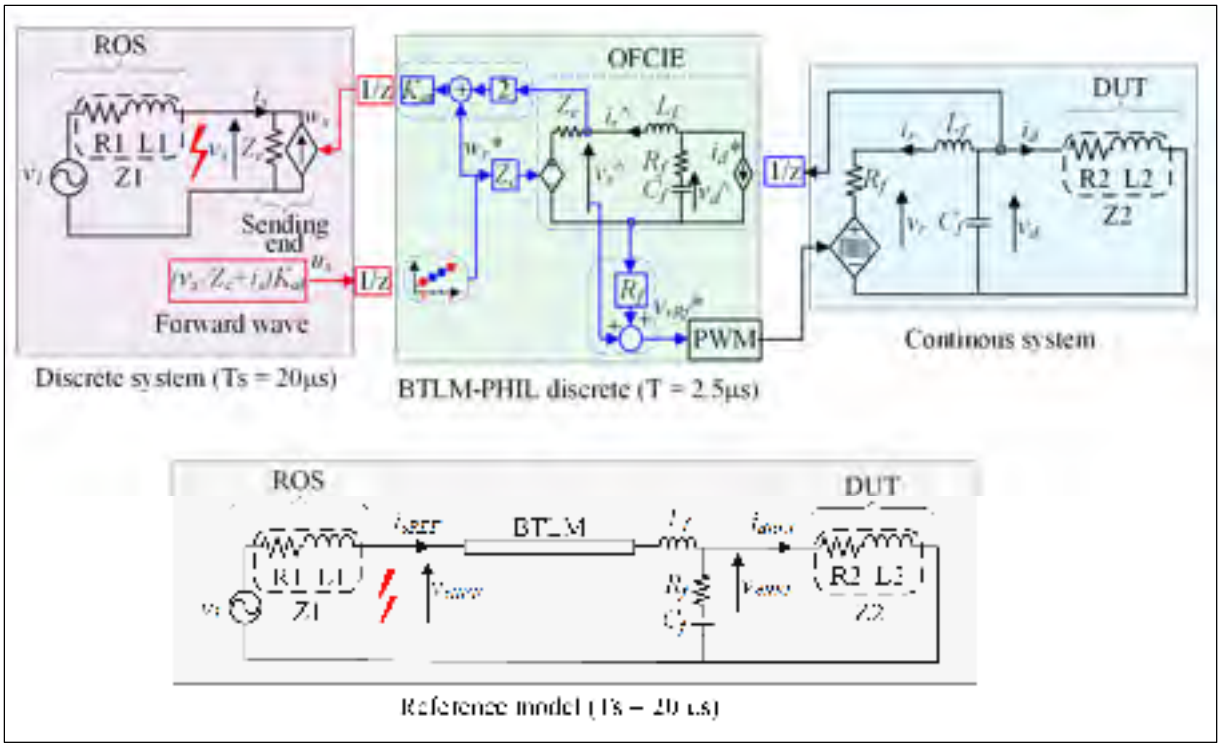

Figure 4.10 Reference case simulation model

The simulation results are shown in Figure 4.11 (new BTLM-PHIL implementation and reference case) for the DUT current (i_d and i_{dREF}) and the ROS voltage (v_s and v_{sREF}). There is a very good match between the two sets of results under steady-state conditions and when a fault is applied at t = 0.038 s. A relative error of less than 0.1% can be noted under steady-state conditions. A simulation has shown that this error is caused by the difference in numerical accuracy (continuous versus discrete DUT) and the R_f resistance compensation delay present in the BTLM-PHIL model.

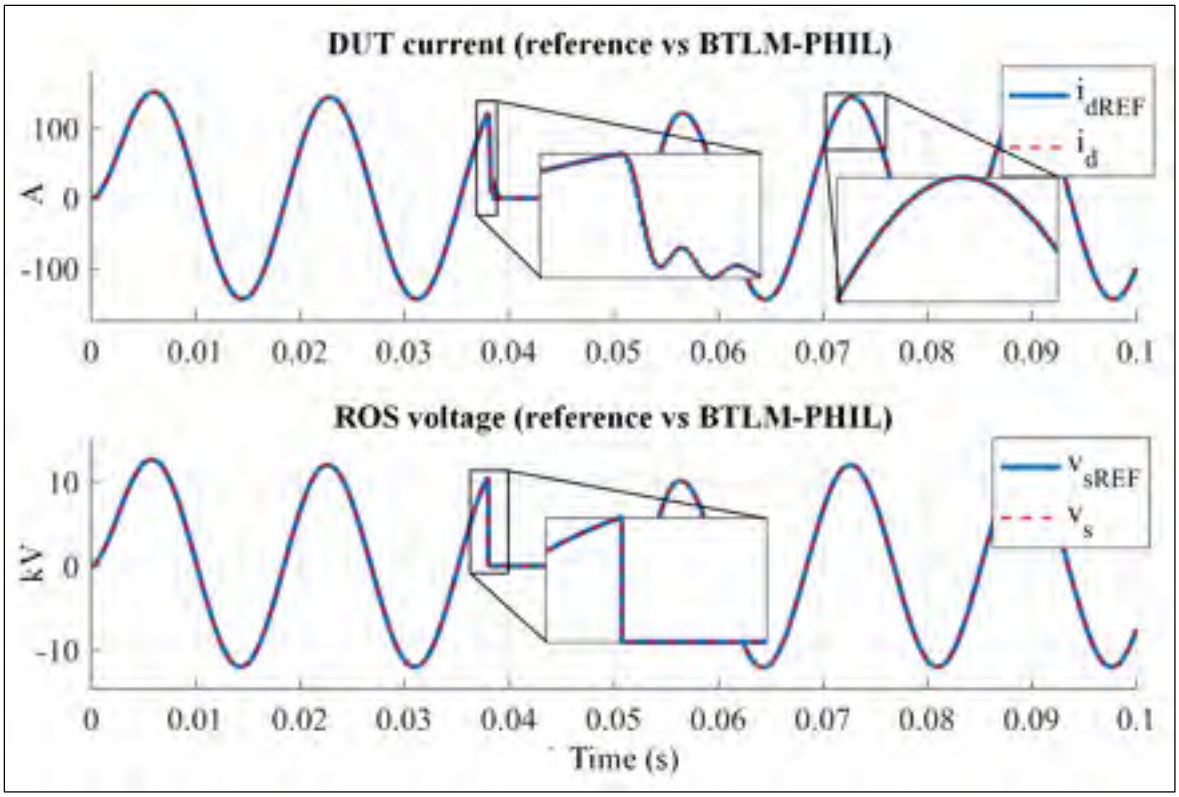

Figure 4.11 Comparative results for BTLM-PHIL method

4.6 Stability analysis of new BTLM-PHIL interface

The complex stability analysis issues associated with non-linear systems such as the interface of a PHIL system may be mitigated to some degree by introducing the notion of passivity (Wyatt, Chua, Gannett, Goknar, & Green, 1981). Defined as systems that do not generate any energy, passive systems are always stable. Meeting passivity requirements is a sufficient but not necessary condition for a system to be stable (i.e. all passive systems are stable, but non-passive systems are not necessarily unstable) and may lead to a conservative interface design. However, a passive interface is always stable, regardless of the ROS-DUT impedance ratio and the complexity of the interconnected systems.

The passivity of time-delayed systems is not always guaranteed; it depends on the exchange of signals between the sending-end and receiving-end of the interface. For instance, the ITM interface method is never passive and it is known to be unstable under certain operating

conditions (Anderson & Spong, 1989; Tremblay, Fortin-Blanchette, et al., 2017; Wei et al., 2008). On the other hand, interfaces based on the transmission line method (TLM) are inspired by the physical behavior of a naturally time-delayed passive element, thus ensuring their passivity (and hence their stability) regardless of the dynamics at the sending and receiving ends (Anderson & Spong, 1989).

In the case of the proposed BTLM-PHIL interface implementation, the stability analysis for the closed-loop system as a whole is a complex undertaking. However, it can be split into two: (1) OFCIE stability; and (2) passivity of the multiple rate BTLM. Performing a separate and independent stability analysis can be justified on the basis that the OFCIE sampling rate is almost ten times greater than that of the RTS.

4.6.1 OFCIE stability

As shown in Figure 4.6, the OFCIE and the PA-VSC connect through an ITM interface (voltage on PA-VSC side and current on emulator side), which is therefore subject to instability. Neglecting PWM- and PA-VSC-related effects, it is possible to derive the linear model shown in Figure 4.12. The left side (current source interface) includes the OFCIE and the R_f resistance compensator. The reference voltage v_{rRF}* is calculated as a function of the measured DUT current (i_d*) and the forward wave w_r^*. On the right side (which comprises the PA-VSC voltage source, output filter and DUT), current i_d is a function of the voltage v_{rRF} and the DUT impedance (Z_d). According to (Tremblay, Fortin-Blanchette, et al., 2017), the stability of this type of interface depends on the ratio of the impedances on both sides of it, considering the hybrid nature (i.e. both discrete and continuous) of the system.

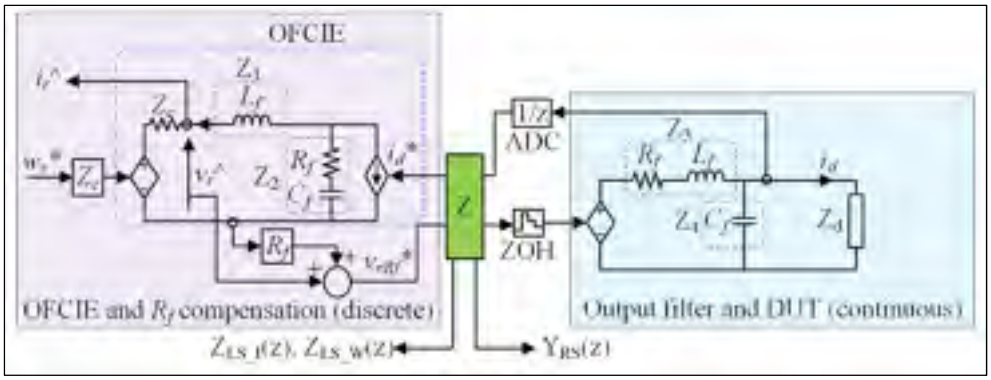

Figure 4.12 Linear model of ITM interface (filter and emulator)

The closed-loop block diagram of this linear model is shown in Figure 4.13. This system uses the sampling period provided by the real-time simulator ADC, i.e. 2.5 µs.

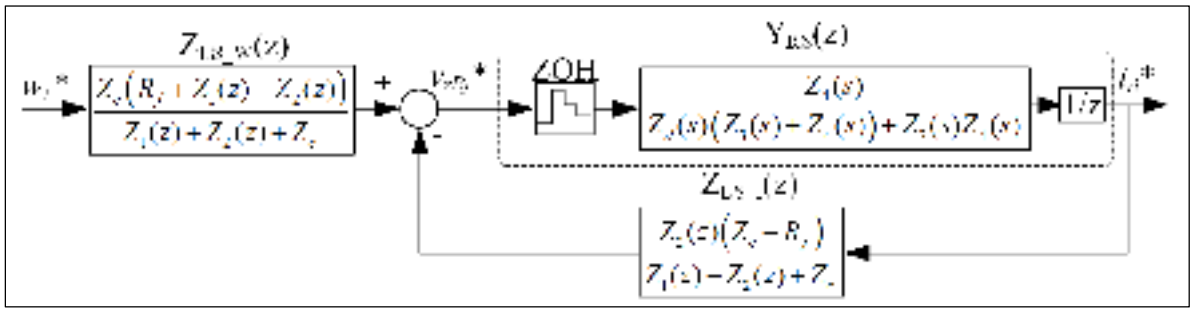

Figure 4.13 Block diagram of linear model of OFCIE-ITM interface

To derive the discrete impedance on the right side of the separation point, the DUT is modeled as a series linear impedance according to equation (4.45):

$$Z_d(s) = x + y(s) \tag{4.45}$$

Where x is the real (resistive) component of the impedance and $y(s)$ is either inductive ($y(s) = s|y(s)|$) or capacitive ($y(s) = 1/(s|y(s)|)$).

The discrete admittance $Y_{RS}(z)$ is then derived using the $\mathcal{Z}$-transform, together with the equation below:

$$Y_{RS}(z) = \frac{i_d^*(z)}{v_{rRF}^*(z)} = \mathcal{Z}\left(\frac{Z_4(s)(1-e^{-sT})/s}{Z_d(s)(Z_3(s)+Z_4(s))+Z_3(s)Z_4(s)}\right)\frac{1}{z} \quad (4.46)$$

The discrete impedance on the left side of the separation point is split in two: a transfer function ($Z_{LS\_I}(z)$) whose input is current i_d* and another transfer function ($Z_{LS\_W}(z)$) whose input is w_r*. These two transfer functions are derived by replacing the continuous impedances with a trapezoidal approximation:

$$Z_{LS\_I}(z) = \frac{Z_2(s)(Z_c - R_f)}{Z_1(s)+Z_2(s)+Z_c}\Big|s = \frac{2(z-1)}{T(z+1)} \quad (4.47)$$

$$Z_{LS\_W}(z) = \frac{Z_c(R_f + Z_1(s)+Z_2(s))}{Z_1(s)+Z_2(s)+Z_c}\Big|s = \frac{2(z-1)}{T(z+1)} \quad (4.48)$$

The closed-loop transfer function (G_{BF}) is given by:

$$G_{BF}(z) = \frac{i_d^*(z)}{w_r^*(z)} = \frac{Z_{LS\_W}(z)Y_{RS}(z)}{1+Z_{LS\_I}(z)Y_{RS}(z)} \quad (4.49)$$

The system is stable if the roots of polynomial $1 + Z_{LS\_I}(z)Y_{RS}(z)$ fall within the unit circle. Since the DUT is an unknown system (parameters $Z_d(s)$ are undefined), what is proposed is to extract the instability regions from $G_{BF}(z)$ for various values of x and y, as a function of: (1) various filter damping factors (represented by resistance R_f) and (2) various values of the characteristic impedance (Z_c)).

The instability regions are shown in Figure 4.14 (where they are represented by different shades of gray) as a function of x and y for a system that has the set of parameters presented in Table 4.1 . Please note the large instability region in Figure 4.14(a) where R_f is equal to 1 Ω. When the value of this resistance is doubled to 2 Ω, the instability region shrinks significantly, although it persists for all capacitive impedances, when the resistive component of $Z_d(s)$ is less than 5 Ω. Finally, when R_f is equal to 3 Ω, the instability region is almost inexistent, and

only persists for unlikely values[6] of the impedance $Z_d(s)$. Resistance Z_c (which is typically equal to 300 Ω) is also a parameter that may vary due to the use of the model. Therefore, Figure 4.14(b) shows the instability regions as a function of the decreasing values of Z_c, for a resistance R_f of 3 Ω. When Z_c is very large (500 Ω), the instability region grows, but it remains within an area of DUT parameters that are unlikely to be used. The lower Z_c is, the more the instability region shrinks. For example, if $Z_c = 175\,\Omega$, the instability region is almost inexistent.

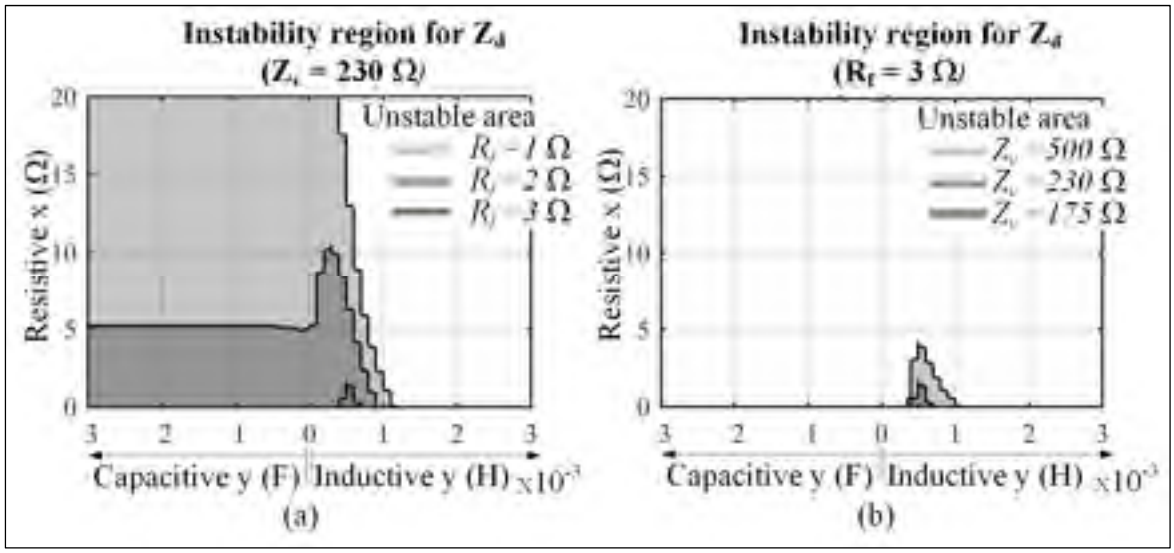

Figure 4.14 Instability regions for various values of $Z_d(s)$ and (a) R_f and (b) Z_c

4.6.2 Passivity of multirate BTLM

The passivity of the Bergeron model can be demonstrated by verifying that the energy entering on the sending end is greater than the energy existing on the receiving end:

[6] If the DUT short-circuit capacity is equal to 100 MVA (i.e. 40 times the rated capacity of the PA-VSC), its inductance is equal to 5.5 mH ((14.3E3)^2/100E6/377 = 0.0055). It is unlikely that any equipment would have an impedance lower than this value.

$$\int_{\tau}^{t} v_s(\xi) i_s(t)\, d\xi \geq \int_{\tau}^{t} -v_r(\xi) i_r(t)\, d\xi \tag{4.50}$$

Note: Since line voltages and currents are separated by a delay τ, energy calculations are performed starting at this moment (rather than using nil initial conditions).

For the line to be passive, the total dissipated energy $E(t)$ must be greater than or equal to 0:

$$\Rightarrow E(t) = \int_{\tau}^{t} \big(v_s(\xi) i_s(\xi) + v_r(\xi) i_r(\xi)\big)\, d\xi \geq 0 \tag{4.51}$$

Using equations (4.37) and (4.38), it is possible to replace equations $v_{s,r}(t)$ and $i_{s,r}(t)$ by:

$$v_{s,r}(t) = \frac{Z_c}{2}\Big(u_{s,r}(t) + w_{s,r}(t)\Big) \tag{4.52}$$

$$i_{s,r}(t) = \frac{1}{2}\Big(u_{s,r}(t) - w_{s,r}(t)\Big) \tag{4.53}$$

Equation (4.51) may then be rewritten as:

$$\begin{aligned} E(t) &= \frac{Z_c}{4}\int_{\tau}^{t} \big(u_s^2(\xi) - w_s^2(\xi) + u_r^2(\xi) - w_r^2(\xi)\big)\, d\xi \\ E(t) &= \frac{Z_c}{4}\int_{\tau}^{t} \big(u_s^2(\xi) - u_s^2(\xi-\tau) + u_r^2(\xi) - u_r^2(\xi-\tau)\big)\, d\xi \\ E(t) &= \frac{Z_c}{4}\int_{t-\tau}^{t} \big(u_s^2(\xi)\big)\, d\xi + \frac{Z_c}{4}\int_{t-\tau}^{t} \big(u_r^2(\xi)\big)\, d\xi \geq 0 \end{aligned} \tag{4.54}$$

The dissipated energy $E(t)$ is always positive, thus confirming the passivity of the BTLM interface. This passivity is guaranteed for a continuous system and for discrete systems with the same sampling period on both sides of the line. However, in the case of hybrid (continuous-

discrete) systems or systems with multiple sampling rates, passivity is no longer guaranteed, which could entail system instabilities.

Although the theoretical explanation of this phenomenon will be the focus of future research, it can be illustrated using Figure 4.15. Intuitively, the passivity rule violation results from the effect of the ZOH on the forward wave w_r, when it enters the emulator side since the signal goes from a slow sampling period (Ts) to a fast sampling period (T), as shown in Figure 4.15 (a). This change in sampling rate is seen as a Heaviside (step) function on the side of the interface where the sampling rate is faster. Depending on the nature of the circuit on the receiving end of the line (i.e. its transfer function), this step function may generate a significant transient in the backward wave u_r. Depending on the moment at which the backward wave is sampled (during the transition from a fast sampling rate to a slower one), the energy stored in the slow wave $u_{rsample}$ (shaded area) may exceed the energy stored in its continuous counterpart (hatched area) since the transients have not yet ended. One way to eliminate this unwanted phenomenon would consist in using the forward wave resampler presented in section 4.4.3 and shown in Figure 4.15 (b). This would result in less pronounced steps that generate less transients on the backward wave, thus reducing the sampling moment dependence.

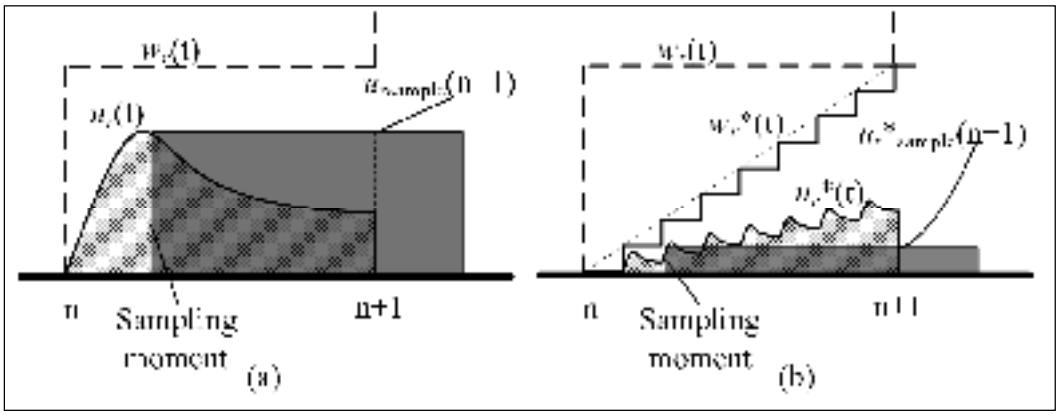

Figure 4.15 Illustration of ZOH effect on BTLM-PHIL passivity:
(a) without resampling (b) with resampling

4.7 Conclusions

This chapter has presented a new PHIL system interfacing method that is stable and accurate. This method is based on the Bergeron transmission line model (BTLM), used for more than 20 years to decouple systems separated by time delays. The major contribution of this dissertation to PHIL system design lies in the new BTLM implementation, which requires no physical resistor to represent the characteristic impedance Z_c on the receiving end of the line. In addition, the BTLM-PHIL implementation eliminates switching-related artifacts in the backward current wave and compensates for the PA-VSC internal resistance while maintaining the same damping factor.

The comparison of BTLM-PHIL simulation results with those for a classical BTLM implementation have shown excellent agreement, thus validating the proposed approach. Furthermore, the closed-loop stability analysis of the OFCIE (interfaced with the DUT using the ITM interface) reveals that the system will always be stable for R_f = 3 Ω, Z_c < 500 Ω and realistic DUT parameters ($|Z_d(s)| > 2\ \Omega$). Finally, the passivity of the system has been validated through an analysis of the energy emerging from the ends of the BTLM-PHIL interface, combined with the use of a forward wave resampling function.

The next chapter will cover the development of the experimental test bench that will be used to validate the operation of the full PHIL system with an actual DUT.

CHAPTER 5

EXPERIMENTAL PHIL TEST BENCH

5.1 Introduction

The purpose of the experimental PHIL test bench is to replicate as faithfully as possible the operation of the full-scale three-phase 25-kV/7.5-MVA power amplifier to validate the design of all the elements of the system, including the new BTLM-PHIL algorithm. To do so, a reduced-scale power amplifier (208 V/3 kVA) designed and built at IREQ has been used to develop and validate the new BTLM-PHIL method in an environment similar to the environment in which the 7.5-MVA system will operate.

Shown in Figure 5.1, the reduced-scale system includes: a power amplifier (six cells per phase, each cell comprising a DC source and a H-bridge); a real-time simulator, including inputs and outputs; an output filter, including the high-precision measurement system; and finally control systems implemented on a FPGA. All these elements will be covered in this chapter.

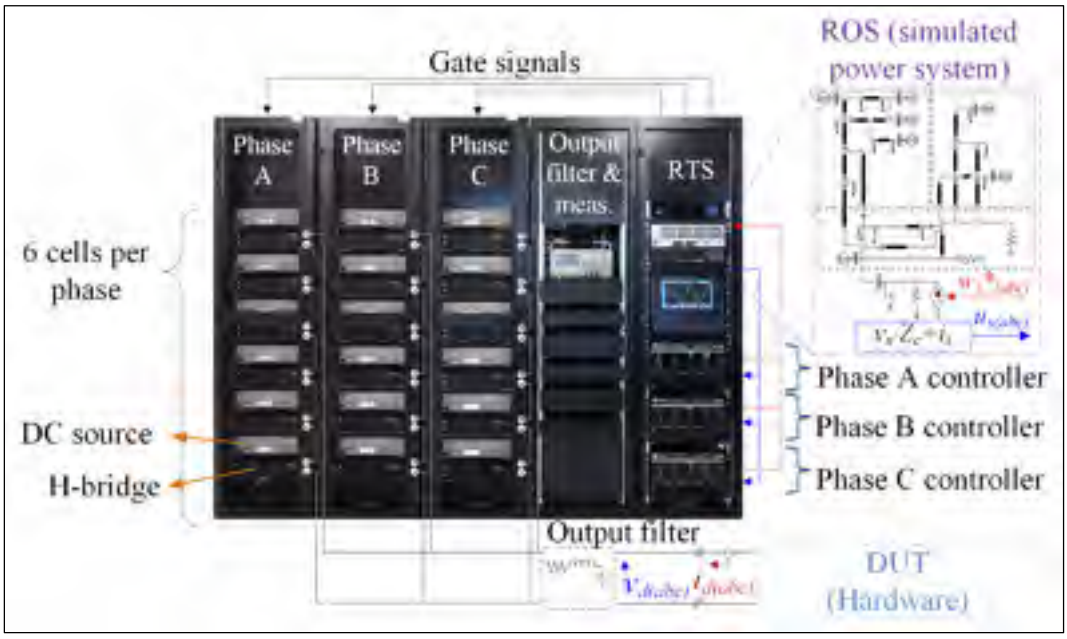

Figure 5.1 Experimental PHIL test bench

5.2 Power amplifier

As mentioned above, the power amplifier used in the test bench is a reduced-scale amplifier based on the same topology as the full-scale PHIL system (25 kVA/7.5 MVA). This system has been designed to offer performances similar to those of the full-scale system to develop the control and protection strategies required for closed-loop operation. The amplifier topology (shown in Figure 5.2) is based on a set of six cascaded H-bridges connected in series and driven directly by the triggering signals provided by the FPGA-based control system. Each H-bridge is powered by a 50-V_{DC} isolated bidirectional voltage source. With this topology, an output transformer is not needed, thus allowing for an increased bandwidth and supporting the modeling of very low frequency phenomena (starting at 0 Hz). This 208-V_{AC} three-phase amplifier has a rated capacity of 3 kVA and an effective switching frequency of up to 57.6 kHz[7] (4.8 kHz per cell). Its theoretical overvoltage capacity (neglecting losses) is 1.75 pu and its steady-state current overload capacity is 3 pu (8.5 pu during 1 ms).

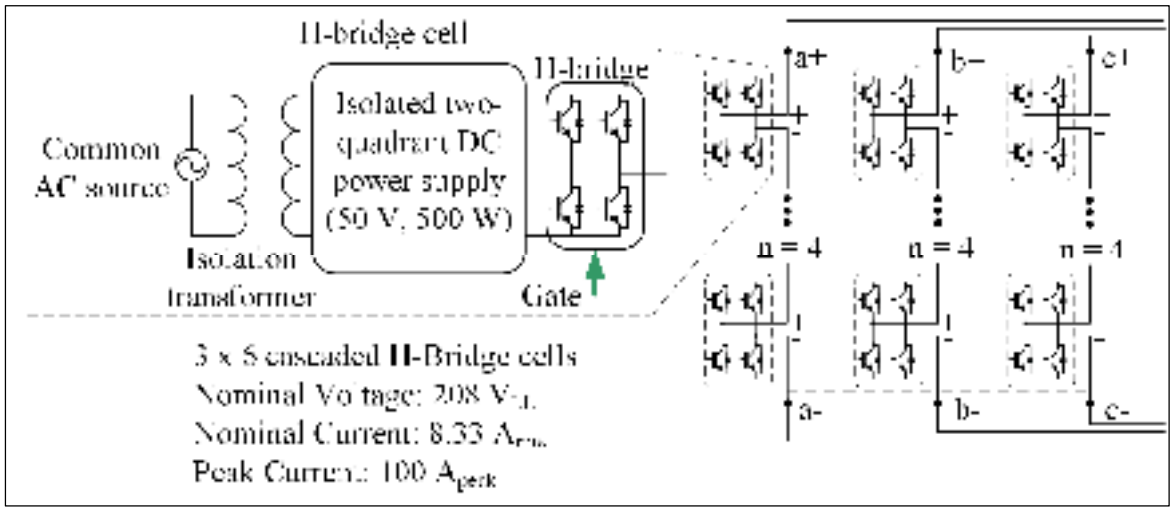

Figure 5.2 Experimental power amplifier topology

[7] Since the reduced-scale amplifier has less modules than the full-scale one (6 modules versus 15), the switching frequency is increased to achieve an effective frequency of the same order.

With this topology, it is possible to generate a sinusoidal wave with at most 13 – 50 V levels as shown in Figure 5.3. Since the equivalent switching frequency is high, a low-impedance output filter is used to eliminate switching harmonics. The design of this filter will be covered in section 5.4.1.

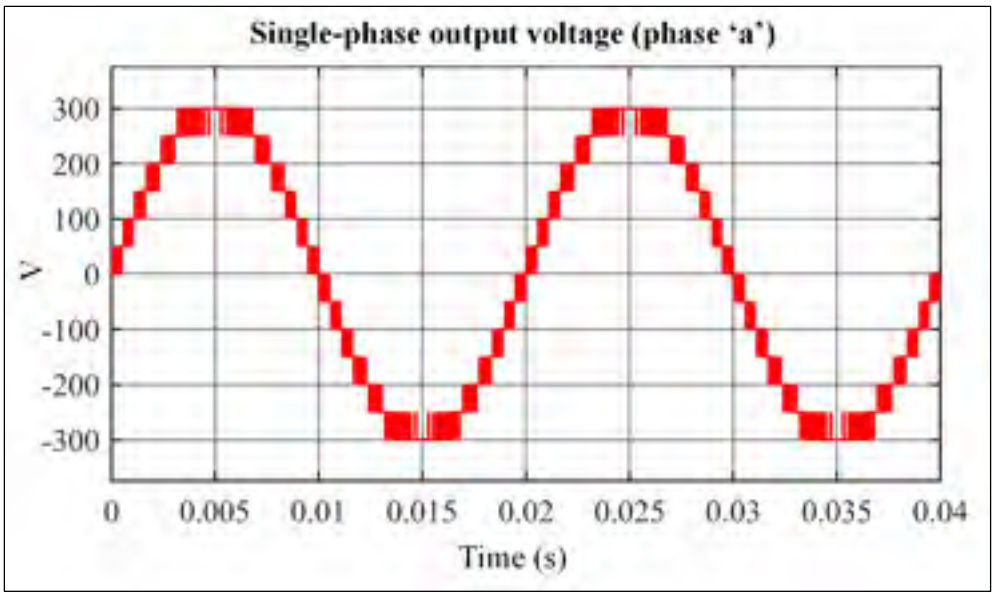

Figure 5.3 Theoretical amplifier output wave form

5.3 Real-time simulator and inputs/outputs

The Hypersim real-time simulation software runs on the Opal-RT OP5700 hardware platform, shown in Figure 5.4. This simulator—which includes 16 - 3.2 GHz calculation cores—is connected to three OP700 I/O expansion boxes comprising a Virtex-6 FPGA and analog/digital channels.

The full-scale system will rely on the same configuration, i.e. a simulator controlling one I/O expansion box for each phase. The triggering signals—provided by a PWM generator—are calculated based on voltage/current measurements and sent directly to the H-bridges through optical digital channels.

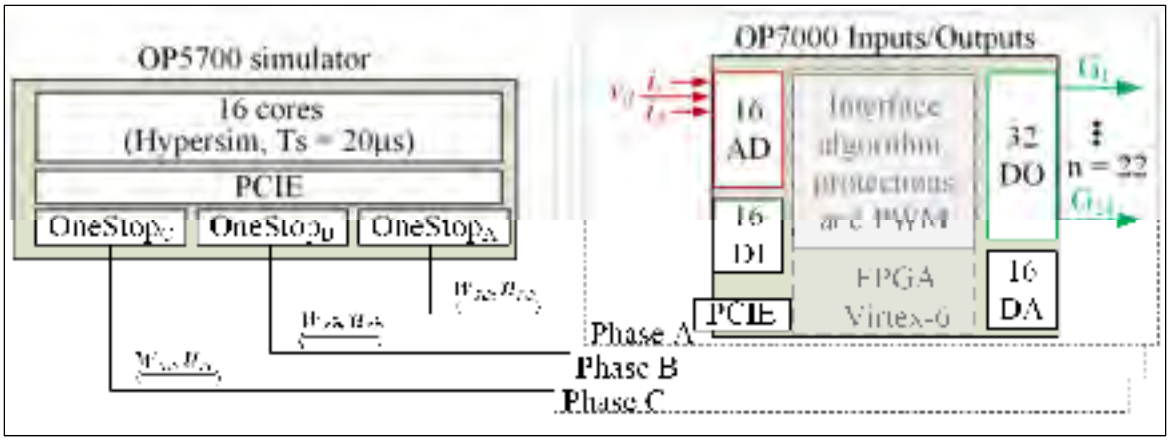

Figure 5.4 Simulator and I/O configuration

5.4 Output filter and measurement system

The power amplifier output voltage is shown in Figure 5.3. An output filter is required to improve the quality of the PA-VSC output voltage waveform. Shown in Figure 5.5, this filter is instrumented to ensure it is fully isolated and provides the voltage and currents necessary to ensure the proper operation of the interface algorithm and amplifier with the required accuracy and speed.

Figure 5.5 Experimental output filter configuration

5.4.1 Output filter design

The purpose of this filter is to eliminate the high-frequency components generated by the switching power amplifier while maintaining a wide dynamic range, hence a low output impedance. A 10-kHz cutoff frequency has been selected to provide a high attenuation at the characteristic harmonic frequency, i.e. at frequencies greater than 30 kHz. A LC topology was selected to allow for a simple and practical implementation. The diagram of this filter is shown in Figure 5.6 for phase "a"; phases "b" and "c" are identical.

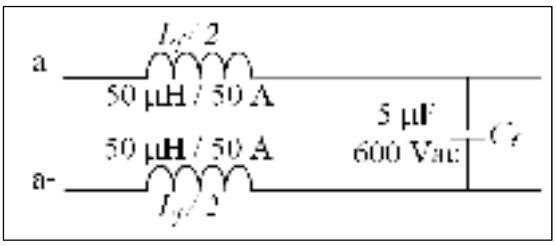

Figure 5.6 Output filter

The filter component values (L_f and C_f) were selected to limit the capacitive effect and reduce the inductive impedance while maintaining an acceptable current ripple. Selecting L_f = 100 µH and C_f = 5 µF yields the values below:

- Natural frequency (f_n) = 7.1 kHz.
- Cutoff frequency (f_c) = 10.7 kHz.
- Output impedance (@ 60 Hz) = 37 mΩ.
- Nominal single-phase reactive power = 27 VA.
- Maximum no-load harmonic ripple current (i_{ripple}) = 2.17 A peak-to-peak. For an effective switching frequency (F_{swe}) = 57.6 kHz, a voltage V_{dc} = 50 V and a duty cycle (d) of 0.5, the ripple current is given below:

$$i_{ripple} = \frac{V_{dc}(1-d)}{L_f} \cdot \frac{d}{F_{swe}} \tag{5.1}$$

- Maximum current change rate = 6 A/µs.

The no-load frequency response of this filter is shown in Figure 5.7. The residual switching harmonic voltage magnitude then becomes 1.6% (-36.2 dB) at 57.6 kHz. Please note that the filter's damping is provided by an equivalent resistance, stemming from the internal impedance of the amplifier [8], estimated at 1.86 Ω.

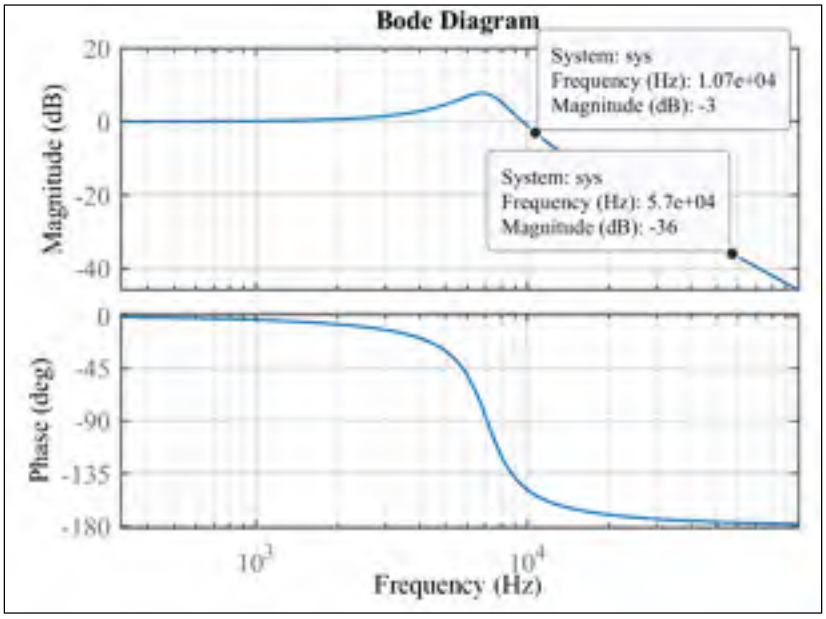

Figure 5.7 No-load frequency response of output filter

5.4.2 Measuring system

An accurate measurement system is required to achieve high transient-state performances. Shown in Figure 5.8, this system includes sensors designed to measure filter currents (input and output) and its output voltage for each of the three phases. The figure shown the circuit diagram for phase "a"; phases "b" and "c" are identical.

The current sensor is based on a non-inductive shunt resistance, thus allowing for DC and AC measurements (without calibration) in addition to providing immunity against large current

[8] More detailed information on this resistance and mitigation methods are provided in section 6.4.

variations (due to its very low inductance). The value of this resistance must also be very low (0.01 Ω) to minimize the voltage drop at its terminals, thus requiring the addition of an amplifier to maintain the signal within an acceptable range to maximize its resolution. It is also necessary to optically isolate the filter measurement system and the OP7000 inputs/outputs to avoid common-mode currents. The voltage sensors are based on a high-performance isolated differential probe that allows for a direct connection to the analog OP7000 inputs.

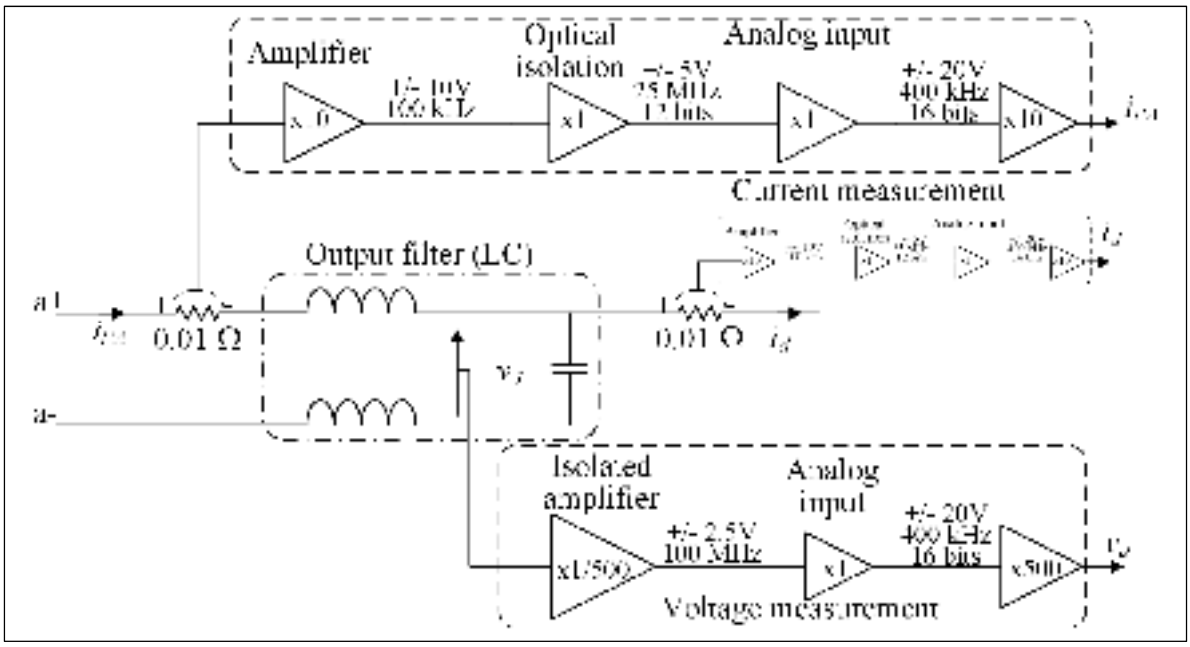

Figure 5.8 Phase “a” measurement system

The specifications of the measurement chain—including all the conversion and amplification components—are presented in Table 5.1. For current measurements, the minimum value and resolution are based on a 12-bit 10 V voltage range and a 10-A/V multiplication factor. For voltage measurements, the minimum value stems from an analog input noise value of 1.95 mV and a multiplication factor of 500.

Table 5.1 Measurement system specifications

Parameters	Current	Voltage
Minimum	+/- 24.4 mA	+/- 0.97 V
Maximum	+/- 50 A	+/- 1250 V
Resolution	24.4 mA	0.3 V
Bandwidth	100 kHz	200 kHz

5.5 Implementation of control system on FPGA

As mentioned in section 5.3, each amplifier phase is controlled by an OP7000 box which contains a Virtex-6 FPGA (XC6VLX240T) running at 100 MHz. This FPGA includes the functions required to handle external inputs/outputs (digital and analog) and simulator inputs/outputs. During the SimP project, it was decided to use this FPGA to develop amplifier-specific control algorithms, thus ensuring the synchronization of all elements and minimizing delays.

Figure 5.9 shows the various functions developed in the Xilinx System Generator environment: resampling, OFCIE, R_f compensator, PWM generator and backward wave calculator. For each function presented in the sections below, special care has been taken to make dynamic parameter changes possible. Thus, it is possible to adjust various parameters without having to regenerate the bitstream file (something that could take several hours). In addition, a 32-bit floating number representation has been used, thus maximizing the accuracy of calculations.

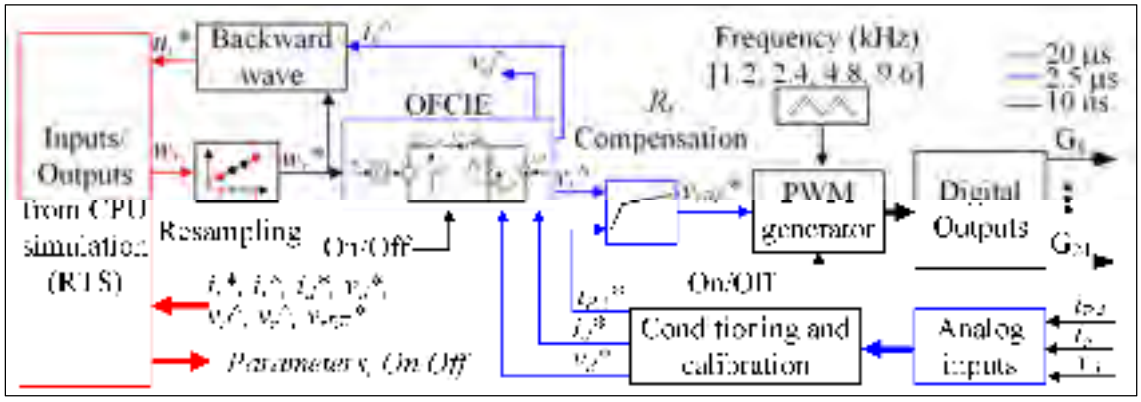

Figure 5.9 Implementation of control system on FPGA

Although mathematical operations are executed every 10 ns, some functions use a calculation step of 2.5 µs, which corresponds to the analog input sampling period.

5.5.1 Synchronization of FPGA with RTS

The synchronization of the simulator and the FPGA is critical to assuring quality results. The execution sequence of both systems is shown in Figure 5.10. At the start of a simulation step (instant n), the backward wave w_s originating from the FPGA is read and used to calculate the voltages at the power grid nodes ($V = Y^{-1}I$) and the corresponding forward wave u_s. The result of this forward wave calculation is immediately sent to the FPGA, although it is only taken into account at the start of the next calculation step (instant n+1). The backward wave calculation is then performed in the FPGA, which sends the results to the simulation at the next step (instant n+2), so that two calculation steps are required for the round-trip.

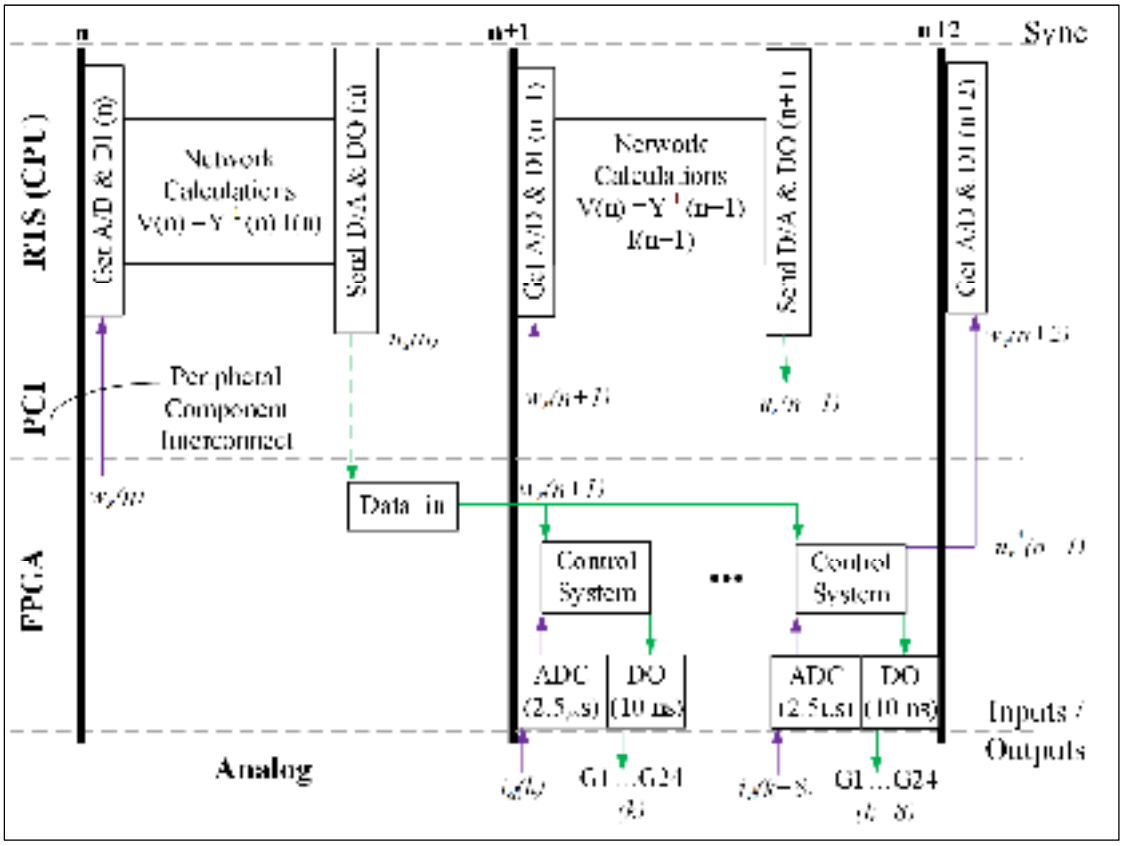

Figure 5.10 Input/output synchronization

5.5.2 Forward wave resampling

This block implements the equation presented in Figure 4.7. Specifically, whenever two RTS samples differ (the detection occurs every 10 ns), the most recent value is used, and a counter is decremented from 1 to 0 in 20 µs (RTS calculation step – unmodifiable without reprogramming the FPGA):

$$w_r^*(t) = w_r^*(n) - (w_r^*(n) - w_r^*(n-1))f(t) \tag{5.2}$$

$$f(t) = -\frac{t}{0.00002} + 1$$

5.5.3 Backward wave calculation

The backward wave calculation is performed using equation (4.44) while adding the attenuation factor on the RTS side.

5.5.4 Analog inputs and signal conditioning

The analog measurements originating from the ADCs (16 bits, ± 20 V, 2.5 µs) are scaled using multiplying factors as discussed in section 5.4.2. In the case of the shunt resistors used for current measurement, this factor depends on the actual resistance value, which is supplied by the manufacturer. An automatic calibration system—which must be enabled at system startup—can be used to adjust the DC component of each input to ensure the signal is centered around zero.

5.5.5 Output filter characteristic impedance emulator

The output filter characteristic impedance emulator (OFCIE) is implemented using equations (4.40) and (4.41). Matrices A, B, C and D are calculated based on the output filter parameters and the desired characteristic impedance, then dynamically discretized to obtain the real-time

Ad and Bd on the RTS side. Among other things, this is essential to enable modifying the characteristic impedance during a simulation without reprogramming the FPGA.

Since input w_r* is updated every 10 ns, the OFCIE equations can be solved using the same calculation step as the ADC, i.e. 2.5 µs, without any concern for data synchronization.

Another functionality implemented in this block is the replication of the high-impedance mode, required when the system in not enabled. To achieve this, current i_r^ is forced to 0, while the capacitance voltage is maintained at the measured value (v_d^ = v_d*). This allows for the proper initialization of the filter, for example when the DUT is a voltage source and the power amplifier has not yet been enabled. Finally, if so desired, the OFCIE can be bypassed to model the open-loop operation of the system.

5.5.6 Internal resistance compensation

As briefly stated in section 4.4.2, the practical implementation of the power amplifier involves a non-negligible internal resistance in the case of the test bench. Although the source of this resistance will be discussed in greater detail in section 6.4, it must be noted here that the voltage drop associated with this resistance is of such magnitude (approximately 10% at the nominal current) that the test bench is practically unusable. Special care has therefore been paid on compensating this resistance to minimize its adverse effect.

For the time being, let us assume that this resistance can be approximated using a two-segment non-linear resistance. Figure 5.11 shows the difference between the reference and measured voltages (neglecting the effect of inductance L_f) as a function of the amplifier output current i_{PA}.

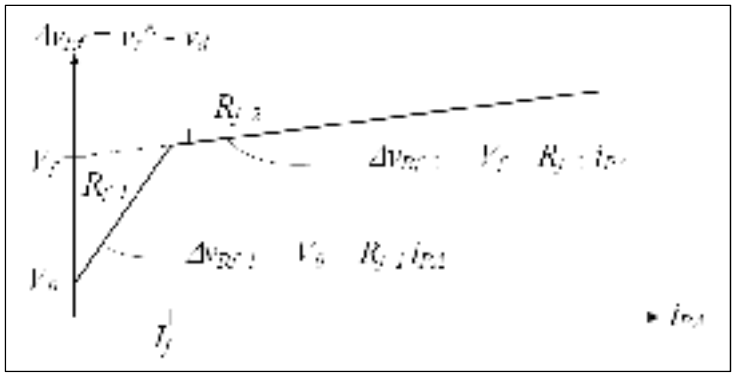

Figure 5.11 Non-linear amplifier resistance

To attenuate this voltage drop, it is proposed to add a function designed to compensate the reference voltage provided to the PWM generator (see section 4.4.2):

$$v_{rRf}{}^{*} = v_r{}^{\wedge} + \Delta v_{Rf} \tag{5.3}$$

In practice, current i_{PA}—which is the inverse of current i_r—contains harmonics due to switching, as discussed in sections 4.3.4 and 4.4. These variations (of the order of ± 1.1 A at the switching frequency) will instantaneously affect the compensation signal Δv_{Rf}, thus injecting undesirable noise in the reference signal $v_{rRf}{}^{*}$. To mitigate this problem, a filter based on the moving average of the switching period is used. The decision to place this filter at the output rather than the input stems from the non-linearity of the resistance and the ripples present in current i_{PA}.

The moving-average filter is described by the equation below:

$$\overline{\Delta v_{Rf}}(t) = \frac{1}{T}\int_{t-T}^{t} \Delta v_{Rf}(\tau)d\tau \tag{5.4}$$

where T is the period of the moving window. In discrete form, it is possible to write the equation as:

$$\overline{\Delta v_{Rf}}(k) = \frac{1}{n_e} \underbrace{\sum_{i=k-n_e+1}^{k} \Delta v_{Rf}(i)}_{Y(k)} \tag{5.5}$$

where n_e is the number of samples in the moving window. Since this window can be large, the sum can become somewhat unwieldy. Hence, signal Y(k) has been reformulated as a recursive equation, to cumulate each new value while removing the oldest one (which falls outside the interval of interest).

$$Y(k) = Y(k-1) + \Delta v_{Rf}(k) - \Delta v_{Rf}(k-n_e) \tag{5.6}$$

If the window period is not a whole number, a linear interpolation is performed.

$$Yint(k) = \Big(\big(\Delta v_{Rf}(k-n_e+1) - \Delta v_{Rf}(k-n_e)\big)(1-d) + \Delta v_{Rf}(k-n_e)\Big)\, d \tag{5.7}$$

where d is the difference between the whole number (n_e) and the decimal number (n). The block diagram of the moving average calculation based on equations (5.6) and (5.7) is shown in Figure 5.13.

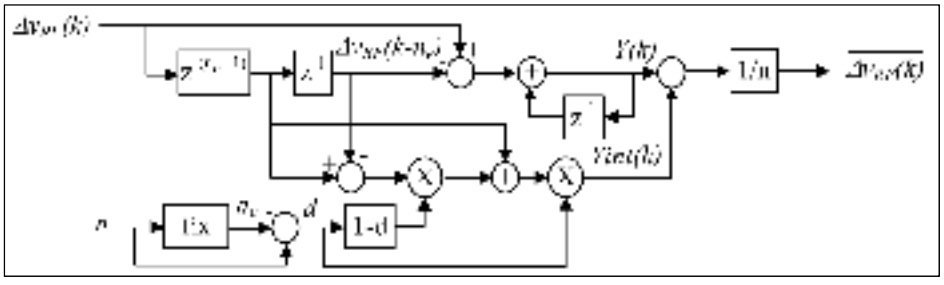

Figure 5.12 Moving average function with interpolation

The FPGA implementation of this moving average function allows for the on-the-fly modification of the number of samples n during a simulation (from 2 to 1024 samples of 2.5 µs). When required, a complex logic system can be used to reset the accumulator to zero

and reinitialize it during the *n* next sampling intervals (during this transition, the simulation result is erroneous).

As for the compensation function, it is possible to change in real time the equations for the first and second segments (Δv_{Rf_1} and Δv_{Rf_2}). Finally, the compensation function assumes that positive and negative currents are symmetric.

5.5.7 Phase-shifted PWM generator

The cascaded H-bridges are controlled using a modulation technique based on the equidistant shifting of carriers (triangular waveforms) over a full switching period. The triangular waveforms are generated using a counter with a 10-ns resolution. The switching frequency (F_{sw}) of each cell can be modified from 1.2 kHz to 4.8 kHz in multiples of two. Since the test bench has six cells, 12 carriers with a 30-degree phase shift between each (modifiable in real time) are generated as shown in Figure 5.13. The reference voltage v_{rRF}^* and each triangular waveform are continuously compared (naturally), thus minimizing the reaction time, especially during voltage steps (which typically occur during short-circuits).

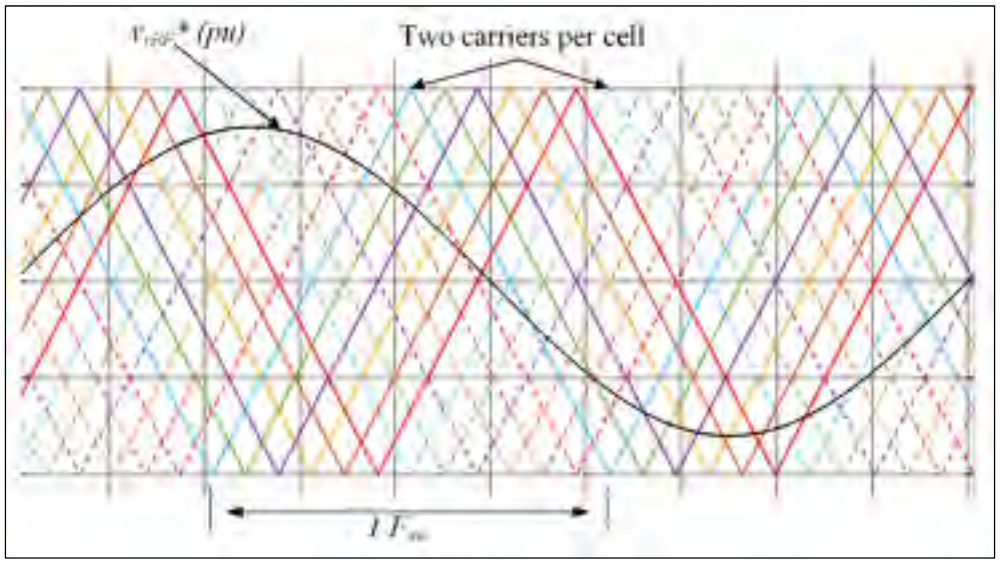

Figure 5.13 Phase-shifted PWM generator

Finally, a functionality allows for the addition of dead time, key to the proper operation of H-bridges, at the PWM generator output. As shown in Figure 5.14, this block delays the activation of the triggering signal to avoid simultaneously switching two switches in the same branch, which would short circuit the DC power source.

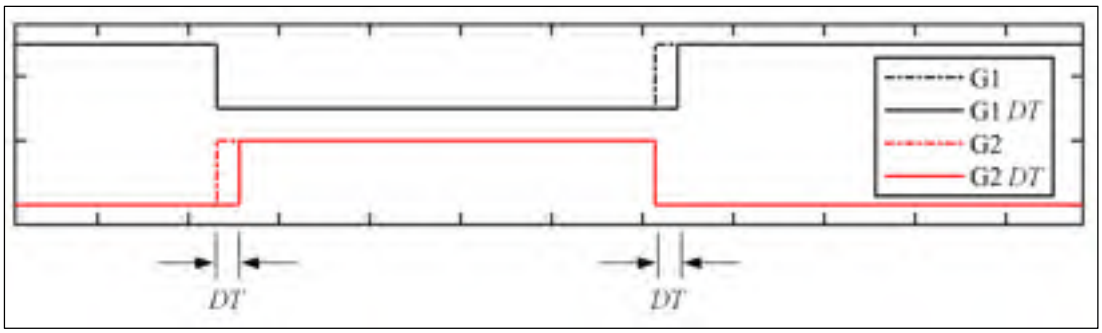

Figure 5.14 Waveform with dead time

5.5.8 FPGA control function summary

The FPGA control function implementation performance data are shown in Table 5.2. Latency is taken to be the signal propagation delay between the input and the output of each function, while the calculation step is taken to be the output signal refresh rate.

From this data and Figure 5.9, it is possible to identify the following signal latencies:

- Between input w_r and pulses (G1 -> G24) = 1.22 µs.
- Between input w_r and output u_r^* = 0.54 µs.
- Between analog inputs and pulses (G1 -> G24) = 1.14 µs.
- Between analog inputs and output u_r^* = 0.46 µs.

Table 5.2 FPGA control system performance summary

Functions	Latency	Calculation step	Dynamic parameters	Static parameters
Forward wave resampling	200 ns	10 ns	–	Ts = 20 µs
Backward wave calculation	N/A (included in OFCIE latency)	2.5 µs	N/A	N/A
OFCIE	340 ns	2.5 µs	Z_c, R_f, L_f, C_f	–
R_f resistance compensator	490 ns	2.5 µs	V_0, R_{f_1}, I_f V_f, R_{f_2}, n	–
Phase-shifted PWM generator	190 ns	10 ns	F_{sw}, TM	Phase shift = 30°
Analog inputs and conditioning	120 ns	2.5 µs	Scaling factor	–

The results of the control system implementation on a Virtex-6 FPGA (XC6VLX240T) are presented in Table 5.3. It should be noted that the FPGA is only lightly loaded and that many of its resources are still available.

Table 5.3 FPGA implementation results

Metrics	Used	Available	Use
Number of registers	22951	301440	7%
Number de LUTs	39868	150720	26%
Number of DSP48	163	768	21%
Number of RAM blocks	120	416	28%

5.6 Conclusions

The success of the SimP project rests on the extreme care taken during the design and implementation phases. The design and implementation of a 7.5-MVA 25-kV power amplifier involves several key steps: theoretical design, modeling/simulation, experimental PHIL test bench, and full-scale implementation. The test bench is therefore a critical milestone of the project. It precedes the full-scale implementation of the system. This test bench could have

been reduced to simple commercial linear power amplifier that would have allowed for the rapid development and validation of the interface method described in Chapter 4. However, using this approach, it would not have been possible to study of the role of the output filter (including the damping factor), the switching effects (including the dead time) and the non-linearities inherent to the topology. It would have been risky to go ahead with the full-scale implementation without a proper understanding of these phenomena.

The project team chose rather to develop a reduced-scale power amplifier based on the same topology as the full-scale amplifier. Except for the voltage and power involved, the only difference between the two systems is the number of levels and the switching frequency (the switching frequency of the test bench is higher since it has less levels). Because of the use of this reduced-scale system, the transition to the full-scale system will not require any change to the control system, except for the output filter and PWM generator parameters.

In this chapter, each element of the SimP experimental PHIL test bench have been presented: the reduced-scale power amplifier; the real-time simulator; the output filter, including the measurement system; and the control system implemented on a FPGA. This chapter makes the following contributions to the project:

- The design and implementation of the output filter, intrinsically tied to the stability of the closed-loop system.
- The development of a method to compensate the internal resistance of the PA, thus permitting the use of the amplifier to carry out realistic tests.
- The rigorous implementation of various functions on the FPGA, thus allowing for the synchronous operation of the simulator and the power amplifier.

In regard to the implementation of functions on the FPGA, great care was taken to ensure most parameters are modifiable in real-time. The whole system can thus be calibrated without having to regenerate the FPGA bitstream file at each change. In addition, to ensure a greater accuracy, a 32-bit floating number representation was selected. Finally, the results for each

individual function were validated using *MATLAB/Simulink/SPS* [9] to ensure their accuracy and latency.

The next chapter will cover the experimental validation of the digital interface algorithm (DIA) BTLM-PHIL, whose development is covered in Chapter 4 and implementation is covered in Chapter 5.

[9] Although these results are not presented in this dissertation, the experimental validation presented in Chapter 6 will demonstrate the overall accuracy of the implementation.

CHAPTER 6

EXPERIMENTAL VALIDATION OF NEW BTLM-PHIL METHOD

6.1 Introduction

The goal of this chapter is to validate the proper operation of the new BTLM-PHIL interface algorithm developed and implemented on the experimental PHIL test bench. The first section discusses the parameters used and describes how the effective line delays were validated. This is followed by the characterization of nonlinearities that will allow for the adjustment of the internal resistance compensation system so as to minimize it. Finally, several reference use cases will be developed to test the various possible system configurations (i.e. grid and the impedance emulator configurations). For each use case, a comparison with a simulation model will be used to assess the accuracy of the test bench experimental results.

6.2 BTLM-PHIL parameterization and impact

In this chapter, the experimental PHIL test bench parameters used are discussed and presented in Table 6.1. The characteristic line impedance value (Z_c = 20 Ω) was first selected to limit the low-frequency impact of the line (below 1 kHz). This value corresponds to a 400-µH series inductance and a 1-µF shunt capacitance. When combined with the output filter, the total series impedance corresponds to 1.3% of the base impedance[10], while the reactive power generated is 3.2% of the rated capacity of the amplifier.

The combined effect of the BTLM-PHIL system and the output filter can therefore be explained by the fact that rather than being connected directly to the ROS (ideal decoupling scenario), the DUT is connected to it through a line and a filter. The starting assumption is therefore that the line and the filter really do have an effect on the power system that is to be

[10] The base impedance is calculated using the rated phase power and voltage: Zbase = 120^2 / 1000 = 14.4 Ω

simulated and that this effect is taken into consideration by the BTLM-PHIL system. Section 7.3.2 will in fact present the set of test bench parameters used to model a distribution feeder to which several DUTs are connected. For the time being, when the selected parameters are used, the low-frequency effect of the line and the filter is considered negligible.

Table 6.1 Testing parameters

Parameters	Values
Nominal voltage (line-to-neutral)	120 V_{ac}
Nominal power (per phase)	1 kVA
Characteristic impedance of line	Z_c = 20 Ω Equivalent to: L = 400 µH and C = 1 µF
Line attenuation factor	K_{at} = 1
Output filter	L_f = 100 µH and C_f = 5 µF
Nominal damping resistance	R_f = 1.86 Ω
Effective switching frequency	F_{swe} = 57.6 kHz
Dead time	DT = 0.5 µs
Calculation step: (RTS and OFCIE)	Ts = 20 µs, T = 2.5 µs

6.3 Validation of delays – line short-circuit on receiving end

As mentioned in sections 4.3.4 and 4.4, the implementation of the Bergeron model for a PHIL system assumes a delay equal to one RTS calculation step (i.e. Ts = 20 µs). To validate the exact value of this time delay and ensure that the latency associated with the FPGA implementation of the BTLM-PHIL system does not create additional delays, a short-circuit test was performed on the line receiving end. To avoid short-circuiting the line at the power amplifier output, and thus tripping protections and/or damaging the amplifier, the short-circuit is created within the OFCIE. As shown in Figure 6.1, a resistance R_{cc} of 0.001 Ω has been inserted after Z_c.

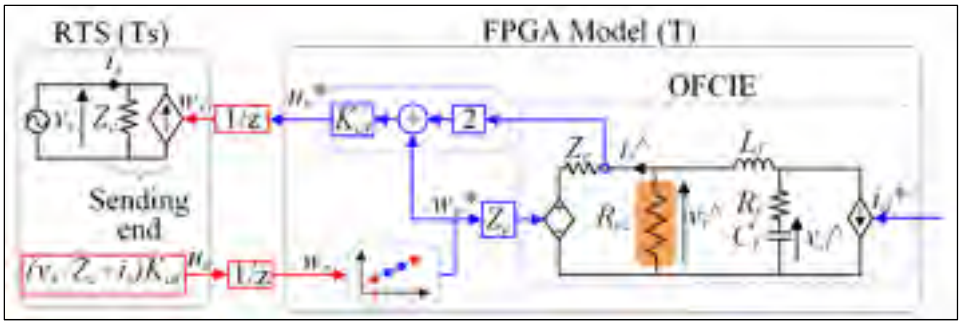

Figure 6.1 Short-circuit on receiving-end side of the line

For this short-circuit test, a characteristic impedance Z_c = 20 Ω has been used; it corresponds to an equivalent line inductance (L) of 400 µH and an equivalent line capacitance (C) of 1 µF. Neglecting the capacitive current (a realistic assumption during a short-circuit since one end of the line is at null potential and the inductive current is dominant), the theoretical current on the sending end of the line is given by the equation below:

$$i_s = \frac{v_s}{2\pi f L} = 795.775\ Arms \tag{6.1}$$

Where v_s = 120 Vrms, f = 60 Hz, L = 400 µH and Ts = 20 µs

Figure 6.2 shows that the measured RMS current is 795.768 A_{RMS} (with a 99.999% accuracy), thus proving that the line model implementation indeed has an effective delay of 20 µs.

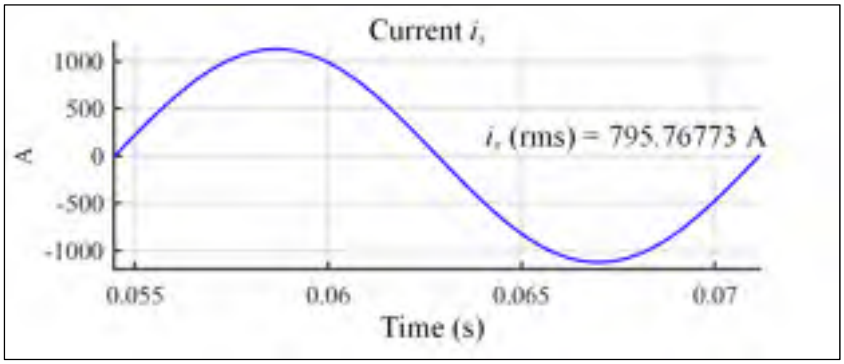

Figure 6.2 Short-circuit current test results

6.4 Nonlinearity characterization and compensation

As mentioned above, the power amplifier used in the reduced-scale test bench PHIL system is a power electronics-based converter that has significant resistive losses. In the test bench, these resistive losses cause a detectable voltage drop. To understand the source of these losses, recall that each H-bridge comprises four power switches, as shown in Figure 6.3. Each switch consists in a MOSFET with an intrinsic antiparallel diode. Although the latter provides a path for the freewheeling current that appears when an inductive load is connected, it does not allow the desired switching characteristics to be achieved. An external diode (D1) with the required switching characteristics has therefore been added in parallel and a series diode (D2) has also been added to block the activation of the internal diode.

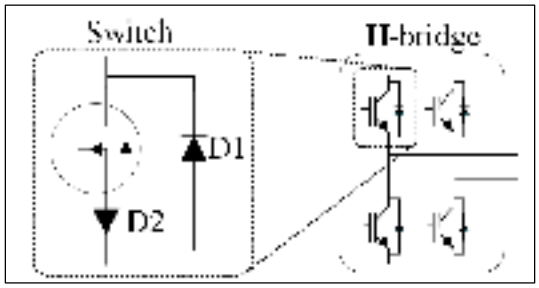

Figure 6.3 Power switch

The characteristics of a diode (applicable to both D1 and D2) can be represented by the curve shown in Figure 6.4. The voltage at the diode terminals increases rapidly at low current values, up to approximately 0.7 V. After this point, the voltage increases slightly with the current.

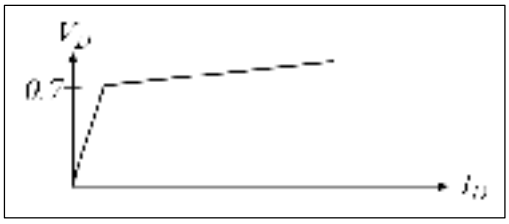

Figure 6.4 Diode characteristics

This voltage drop (0.7 V) is significant in the case of a test bench since the cells operate at a low DC voltage (50 V)[11]. Assuming that the effect of dead time can be neglected, 12 power switches are always in a conductive state (6 H-bridges and two switches conducting simultaneously). Hence, the total voltage drop represents the sum of the voltage drops in the 12 diodes, wires, connectors and printed circuit board traces.

To characterize the total resistance, i.e. the above-mentioned resistance plus the resistive losses in the measurement inductances and resistances, it is proposed to treat the amplifier and the filter as shown in the diagram shown in Figure 6.5. In this system, the equivalent voltage source is assumed to be ideal and equal to the reference voltage v_r^.

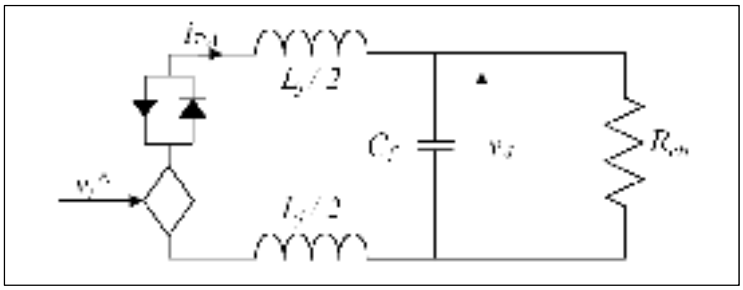

Figure 6.5 Nonlinearity characterization diagram

By measuring the difference between v_r^ and the voltage applied to the load v_d, it is possible to graph the voltage drop (Δv_{Rf}) as a function of the current i_{PA}. Figure 6.6 shows the experimental results obtained for phase "a" (red curve) with a low reference voltage variation rate (required to make the effect of inductance L_f negligible). The blue and black curves represent the best linear approximations of the curve; they clearly show that the voltage drop behaves as expected, i.e. with two linear segments. The green curve represents the nominal equivalent resistance (R_f) of the system, obtained at the nominal current. Phases "b" and "c" are characterized in the same manner.

[11] In the full-scale system, this voltage drop will be negligible (less than 0.5% of the DC voltage) since each cell will operate at 2000 V.

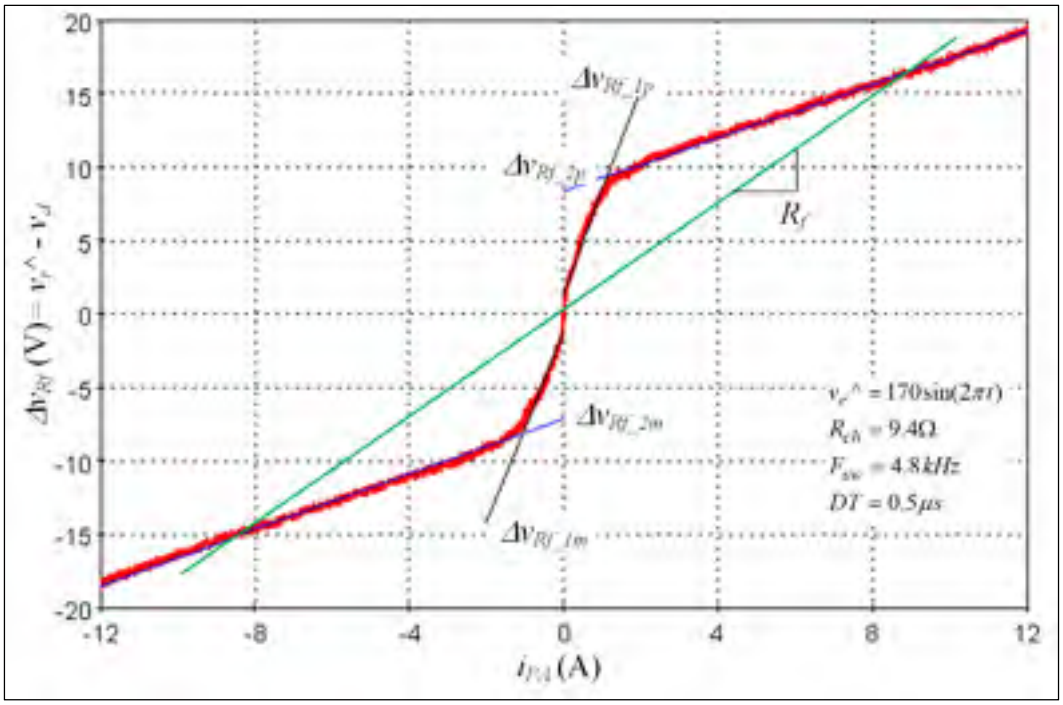

Figure 6.6 Voltage drop in amplifier phase "a"

The tests have given the parameters presented in Table 6.2. Since the compensation function described in section 5.5.6 assumes the system is symmetric, the average of the absolute values of the curves has been calculated. In addition, the nominal equivalent resistance (R_f) value—calculated based on the nominal current—will be used in the OFCIE.

Table 6.2 Voltage drop parameters

Parameters	$\|\Delta v_{Rf\_1}\| = V_0 + R_{f\_1}\, i_{PA}$	$\|\Delta v_{Rf\_2}\| = V_f + R_{f\_2} i_{PA}$	**Nominal R_f (i_{PA} = 8.33 A)**
Phase "a"	Δv_{Rf_1p} = 1.3 + 7.0 i_{PA} Δv_{Rf_1m} = -1.2 + 6.5 i_{PA} Average of absolute values: $\|\Delta v_{Rf\_1}\|$ = ($\|\Delta v_{Rf\_1p}\|$ + $\|\Delta v_{Rf\_1m}\|$) / 2 $\|\Delta v_{Rf\_1}\|$ = **1.25 + 6.75 $\|i_{PA}\|$**	Δv_{Rf_2p} = 8.3 + 0.91 i_{PA} Δv_{Rf_2m} = -7.2 + 0.94 i_{PA} Average of absolute values: $\|\Delta v_{Rf\_2}\|$ = ($\|\Delta v_{Rf\_2p}\|$ + $\|\Delta v_{Rf\_2m}\|$) / 2 $\|\Delta v_{Rf\_2}\|$ = **7.75 + 0.93 $\|i_{PA}\|$**	R_f = 1.86 Ω

Applying this set of parameters to the R_f compensation system described in section 5.5.6[12] yields the graph shown in Figure 6.7. This figure shows the voltage drop (Δv_{Rf}) as a function of current i_{PA} when the compensation system is enabled. The voltage drop is then drastically reduced to less than 1 V over most of the current range, and to less than 2 V when the current crosses zero. The latter can be explained by the fact that the actual diode characteristics are neither fully linear nor symmetric although the compensation system assumes both.

The average voltage drop—which corresponds to less than 0.5% of the nominal voltage—ensures the test bench amplifier can be treated as a very low-impedance amplifier (within the nominal current range).

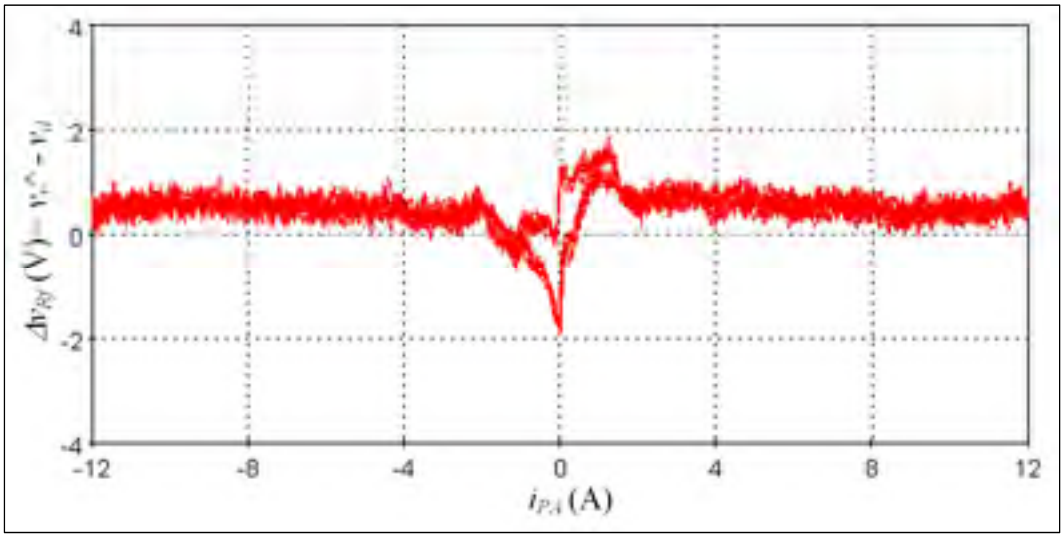

Figure 6.7 Voltage drop after compensation

6.5 Validation of power grid emulation operating mode

The purpose of this comparative test is to check whether the new BTLM-PHIL interface algorithm (in which the characteristic impedance Z_c is represented in the OFCIE) does not

[12] Testing has shown that the compensation system performs well with a moving average window of 34.72 µs, which corresponds to half of the effective switching frequency (F_{swe} = 57.6 kHz).

modify the theoretical behavior of the BTLM. To do so, results for the PHIL system—comprising an equivalent grid as the ROS, the experimental test bench and an actual resistor (with a rated capacity of 770 W at 120 V) as the DUT—are compared with those for a reference simulation model, as shown in Figure 6.8. The reference simulation model is an exact copy of the experimental system, except for the BTLM, which is the theoretical model described in section 4.3.3. The two systems share the same set of parameters and use the same equivalent network: SCC = 5 kVA (at 120 V) and X/R = 4. Since this grid impedance is considered to be weak[13] relative to the capacity of the load, it will therefore cause a noticeable voltage drop across the load.

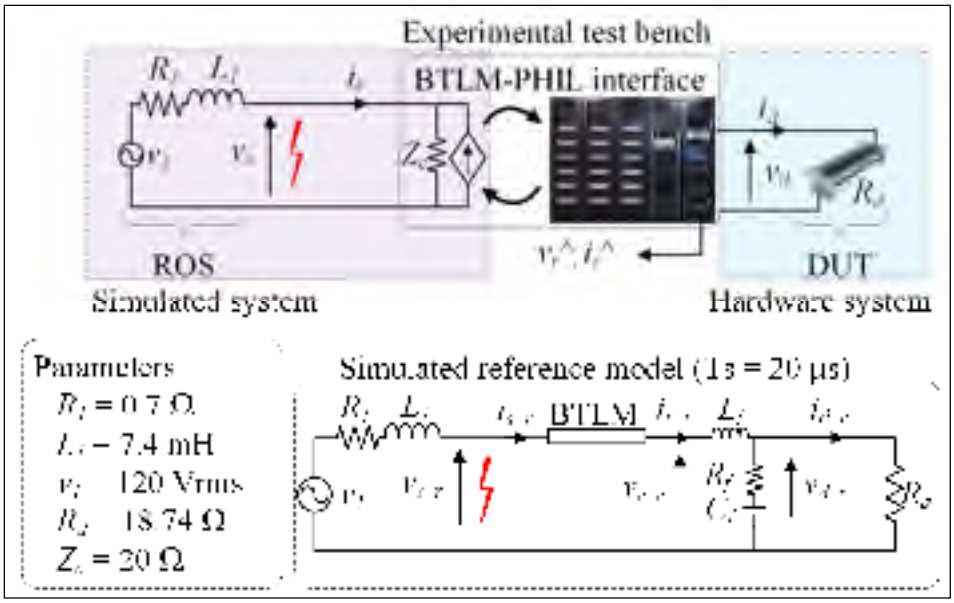

Figure 6.8 Resistive load tests (grid emulation mode)

Note: This configuration—with an inductive ROS with a low SCC and a resistive DUT—is very difficult to simulate using the PHIL system. For example, according to the stability analysis method developed in (Tremblay, Fortin-Blanchette, et al., 2017), the ITM interface method would yield unstable results since the impedance ratio is equal to 27 at the critical

[13] In this case, the grid impedance is only 6.5 times lower than that of the DUT. Any ratio below 10 is generally considered weak.

frequency. To stabilize the system with this method, the SCC should be increased to about 135 kVA, which would be tantamount to performing open-loop tests.

6.5.1 Transient response during fault

This test involves applying a line-to-ground impedance fault over two cycles on the ROS side and observing the voltage across the DUT (v_d) and the ROS-side current (i_s). When the fault is cleared, voltage source v_1 adds 3rd, 5th, 7th, 11th and 13th order voltage harmonics to represent the oscillation modes that may occur on the simulated transmission system. The amplitude of these harmonics is 10% of the nominal voltage of source v_1. Figure 6.9 shows that the PHIL simulation is stable, on one hand, and that the results overlap perfectly, on the other hand. The voltage measure before the fault is 115 V, which illustrates well the effect of the closed-loop behavior of the system with a low SCC power system. This 5-V voltage drop would not have been observed during an open-loop simulation.

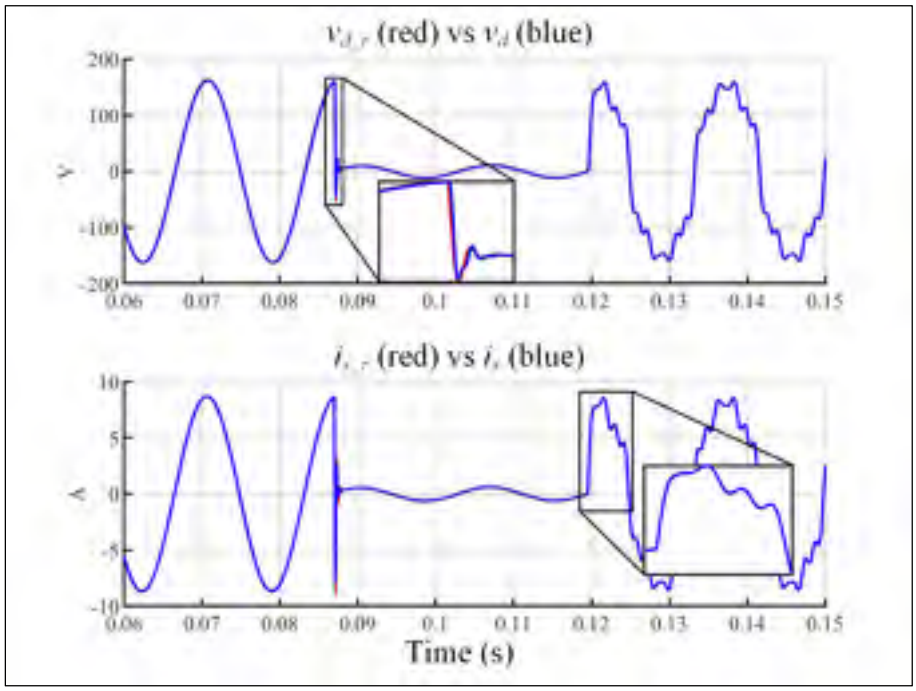

Figure 6.9 Transient results (grid emulator)

A zoomed-in view showing the current and voltage at the moments when the fault is applied and when it is cleared confirms that the BTLM-PHIL method operates transparently and preserves the dynamic BTLM behavior. In addition, these results show that the R_f resistance compensation system is able to dynamically cancel the negative effects of amplifier nonlinearities.

The performance of the OFCIE can also be verified by comparing the voltages and currents that come from the receiving end of the line (v_r^ and i_r^) with those that come from the reference simulation model (v_{r_r} et i_{r_r}). Figure 6.10 shows that the results agree perfectly, thus proving that the OFCIE is operating properly and hence so is the BTLM-PHIL system.

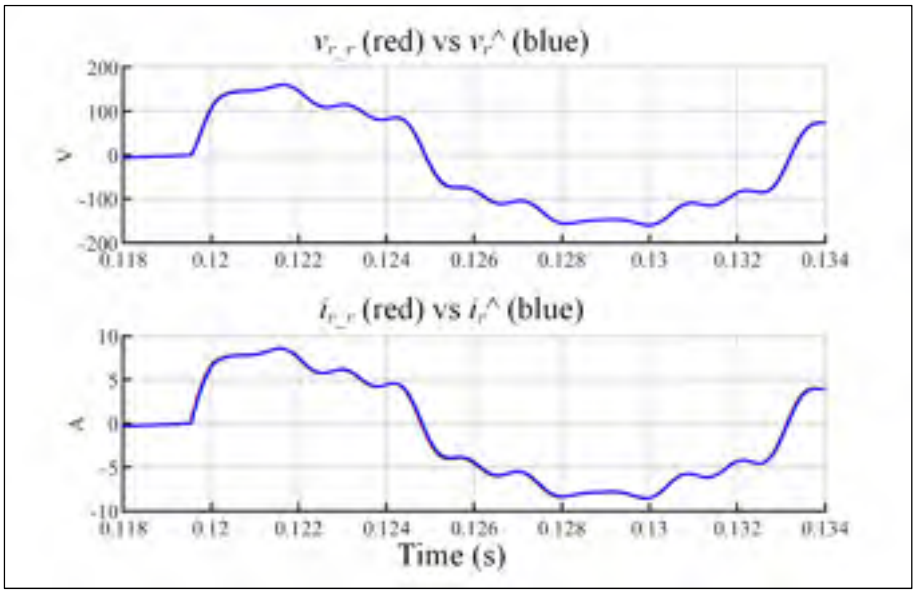

Figure 6.10 Experimental OFCIE validation

6.5.2 Frequency response as seen by the grid emulator

Another way of validating the transient performance of the PHIL system (BTLM-PHIL method and R_f compensation) consists in obtaining a frequency response. To do so, an ideal voltage source is connected to the sending-side of the line (voltage v_s is then fixed), and a harmonic voltage source (with an amplitude equivalent to 3% of the nominal voltage) is superimposed

on it, as shown in Figure 6.11. The impedance (Z_s) seen by this source is then calculated by applying the Fourier transform to voltage v_s and current i_s for the frequency band of interest.

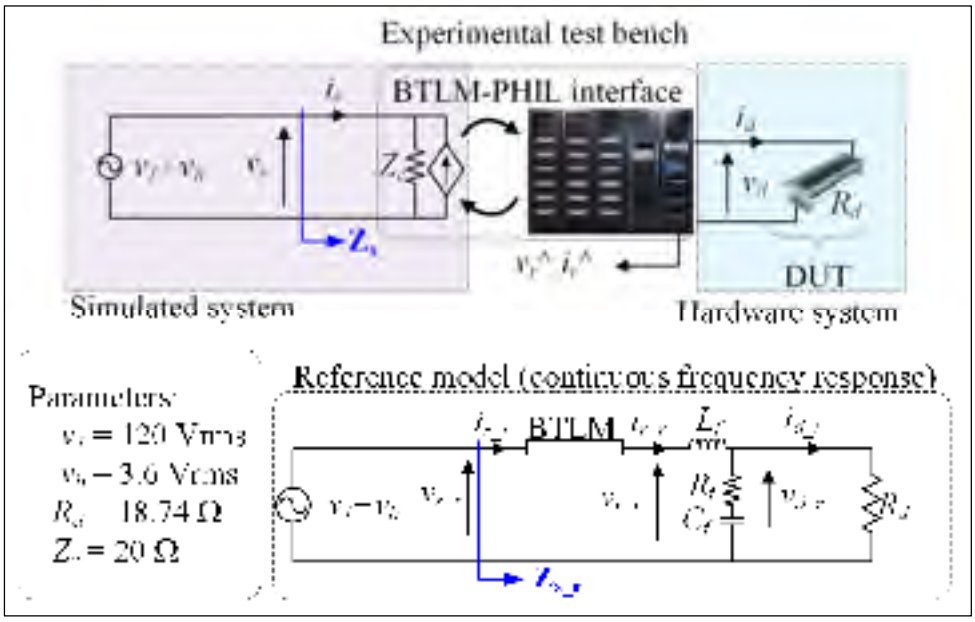

Figure 6.11 Resistive load tests (frequency response)

Figure 6.12 shows the results obtained (magnitude and phase) with the test bench (Z_s) in comparison with a reference case generated using a continuous frequency response (Z_{s_r}). There is an excellent agreement for frequencies from 0 to 8 kHz. For frequencies over 8 kHz, significant differences are noted, especially with respect to damping at the 10.8-kHz pole. In addition, a 21-kHz zero is present in the reference case while it is found at 19 kHz in the experimental measurements. As discussed in detail in (Tremblay, Fortin-Blanchette, et al., 2017), these differences are believed to be mainly due to the discretization of the system, which changes the system impedance at frequencies over 10% of the sampling frequency (0.1/Ts = 5 kHz), and the forward wave resampling effect. It must however be said that the higher frequencies fall outside the validity range of the grid simulation models. At frequencies that fall within the range of interest, i.e. below 5 kHz, the agreement between the two systems is completely acceptable.

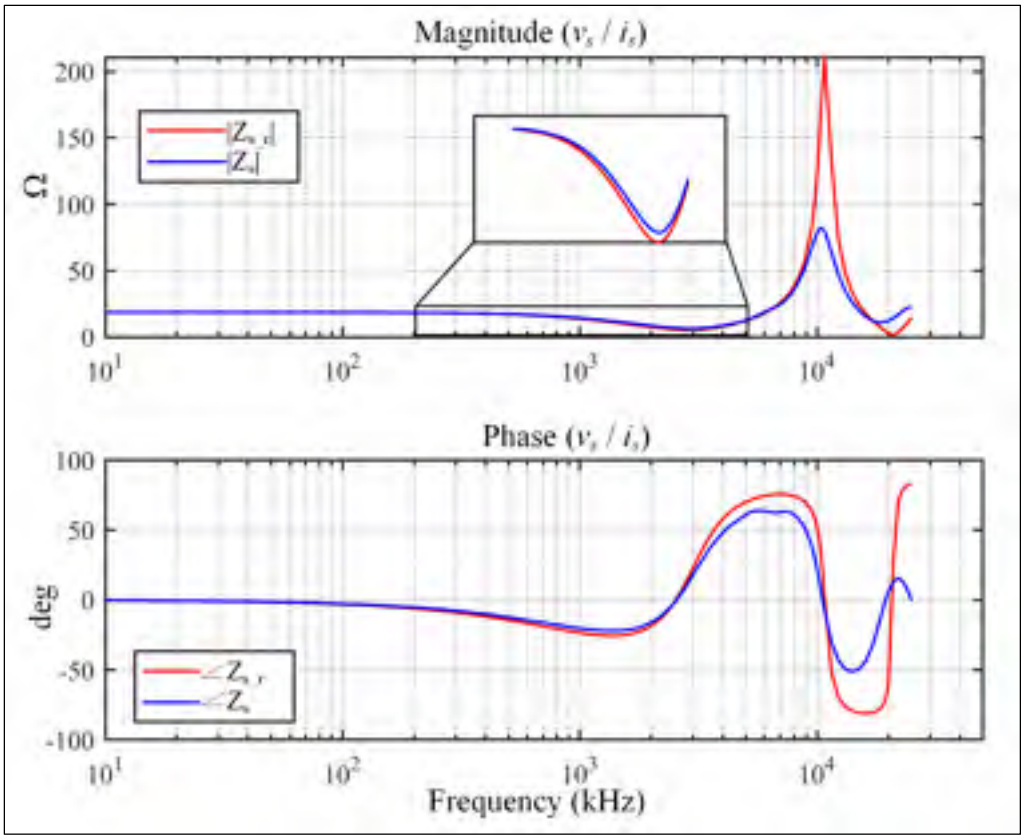

Figure 6.12 Frequency response (resistive load)

The difference between the two systems—in particular between 0 and 5 kHz—can be accounted for using an equivalent test bench series impedance. Using this impedance, it is possible to combine all unmodeled phenomena: dead time, sampling delays, compensation accuracy, real value of output filter components, forward wave resampling effect, RTS jitter and input/output accuracy. Figure 6.13 shows the equivalent resistance and inductance (real and imaginary components of the difference between Z_s and Z_{s_r}) that would be added in series with the test bench. Please note that at low frequencies (less than 1 kHz), the resistance value remains low since the compensation system operates adequately[14]. Since this compensation is not instantaneous, it adds an inductance of several hundred µH. Nonetheless, the system output

[14] Without compensation, this resistance would be 1.86 Ω.

impedance remains negligible at 60 Hz (R_{eq} = 0.05 Ω and X_{eq} = 0.1 Ω)) relative to the base impedance of the system, i.e. 14.4 Ω.

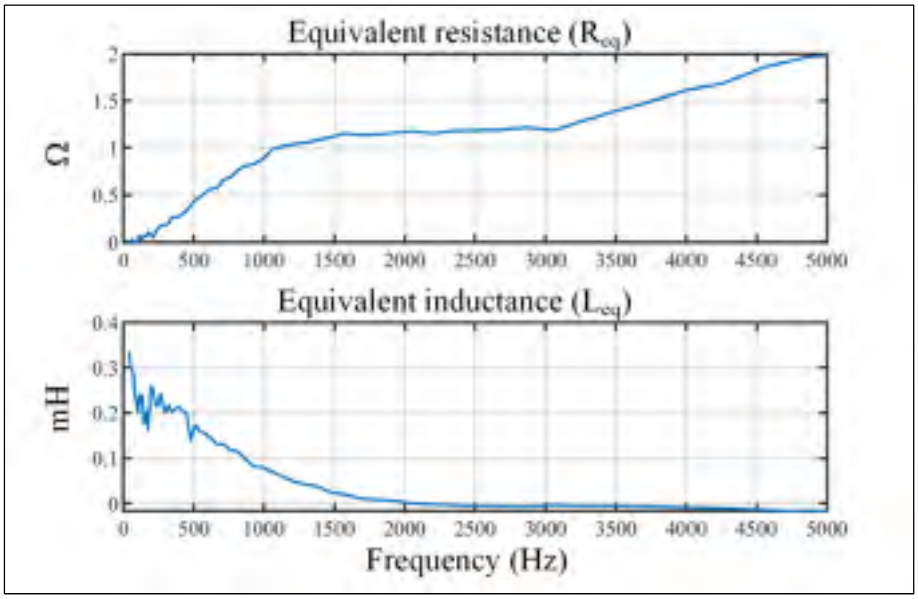

Figure 6.13 Equivalent impedance of test bench (Z_{eq})

6.6 Validation of impedance emulation operating mode

The impedance emulation operating mode is especially challenging for a digital interface algorithm (DIA) since the ROS-side impedances are in general of the same order of magnitude or greater than those of the DUT, thus creating major stability issues. However, the BTLM-PHIL method allows for a satisfactory representation of this operating mode, something that was difficult to achieve with previous DIAs.

In this configuration, the DUT is an electrical source with its own internal impedance and the ROS can be any type of impedance. In this operating mode, also named “islanded mode”, the effect on the voltage measured across the DUT only depends on the accuracy of the closed-loop system.

The experimental configuration (see Figure 6.14) involves connecting the experimental test bench directly to the 120-V laboratory outlet, which in our case is Hydro-Québec's power system. For these tests, two types of Z_l impedances are emulated on the ROS side: first, linear R-, L- and C-type impedances; and second, non-linear impedances (e.g. saturable inductor and induction motor). The experimental results—i.e. the voltage across the emulated impedance (v_s) and the current measured on the outlet side (i_d)—are compared with those generated by a reference model (v_{s_r} and i_{d_r}), whose input is the measured outlet voltage (v_d).

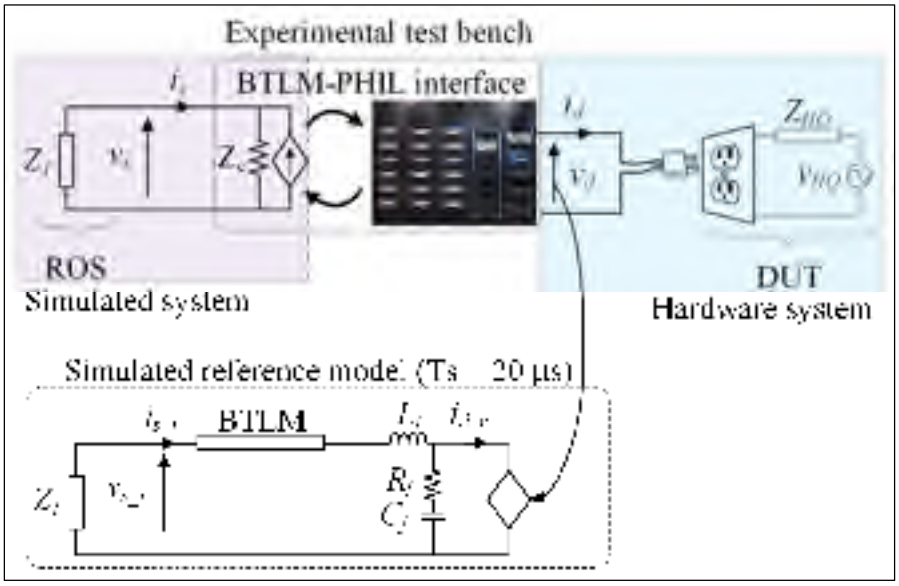

Figure 6.14 Active DUT testing (impedance emulator)

6.6.1 Linear impedance emulator (R, L and C)

The tests below involve the emulation of three typical linear impedances:

1. Resistive impedance: Z_l = 14,4 Ω.
2. Inductive impedance: Z_l = (1 + j14,4) Ω.
3. Capacitive impedance: (1 - j14,4) Ω.

Experimental results for the three tests are shown in Figure 6.15. Experimental and simulation results (blue and red curves, respectively) agree well for the resistive and inductive loads. For

the capacitive load, there are noticeable differences that are due to PA-VSC nonlinearities. As mentioned above, the main nonlinearity (due to the internal diodes of each H-bridge) is compensated by changing the reference voltage v_r^ according to the diode characteristics. However, the voltage still contains residual harmonics since this compensation is imperfect. The capacitor current is very sensitive to the harmonic artifacts which cause perceptible differences. However, the results show that the new DIA performs satisfactorily, thus validating the implementation of the BTLM-PHIL system. This new PHIL system implementation can therefore be used to conduct accurate islanded mode tests, something that was difficult or even impossible to do with other interface methods.

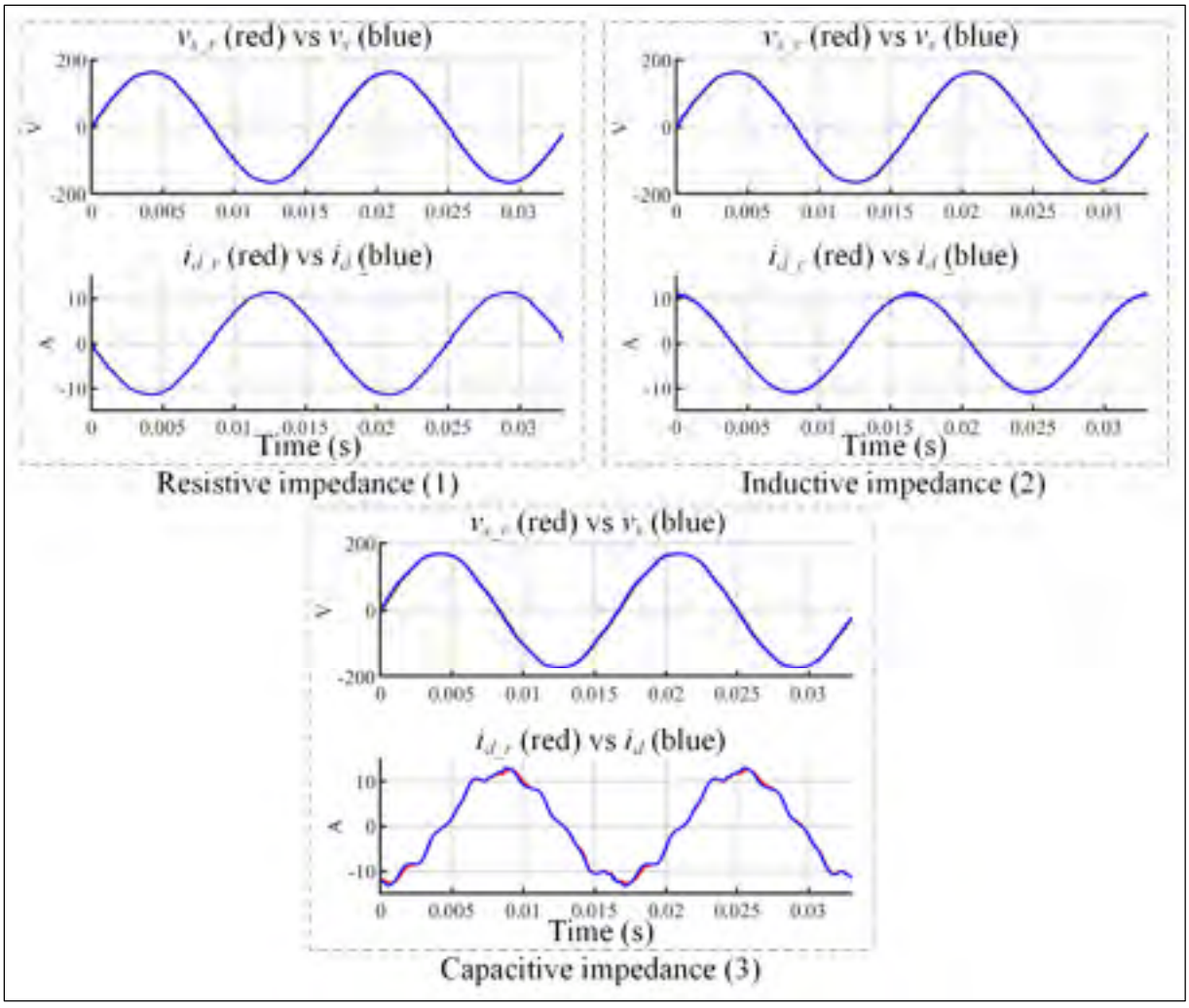

Figure 6.15 Linear impedance emulation results

6.6.2 Non-linear impedance emulator

Two components have been selected to demonstrate the BTLM-PHIL interface operates properly with non-linear impedances: a saturable inductor and an induction motor.

6.6.2.1 Saturable inductor

The following test involves emulating a saturable inductor on the ROS side, as shown in Figure 6.16. The Z_l impedance is composed of a resistance component with a value of 1 Ω and an inductive component with characteristic φ(i), modeled using three linear segments.

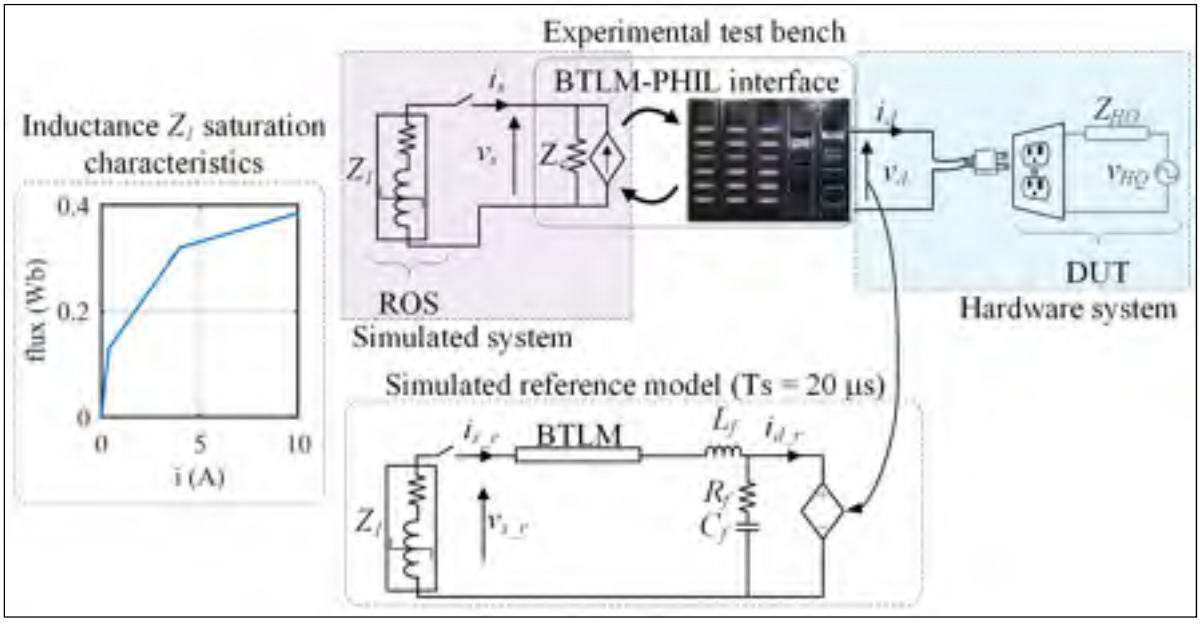

Figure 6.16 Active DUT testing (saturable inductor emulator)

The simulation involves switching the inductor on at the voltage zero-crossing. This brings the inductor into saturation since the initial flux is nil when the device is switched on and the flux—which is the voltage integral—reaches its maximum value after half a voltage cycle. Figure 6.17 shows the results measured when the saturable inductor is switched on: the first graph shows the DUT-side voltage (v_d) dropping by 6 V while the second graph reveals that the measured current (i_d) has a significant DC component. These results agree perfectly well

with those obtained using the reference model (i_{d_r}). During the transient magnetization period, there are slight differences due to the reference model not forming a closed loop with the DUT and the reference model neglecting the effect of the test bench equivalent resistance (Z_{eq}). The 6-V drop in voltage v_d clearly demonstrates the closed-loop operation of the system since the inrush current into the inductor emulated by the test bench is sufficiently large to affect the electrical outlet voltage.

These results show that the PHIL test bench can be used to accurately emulate transient phenomena associated with nonlinear impedances.

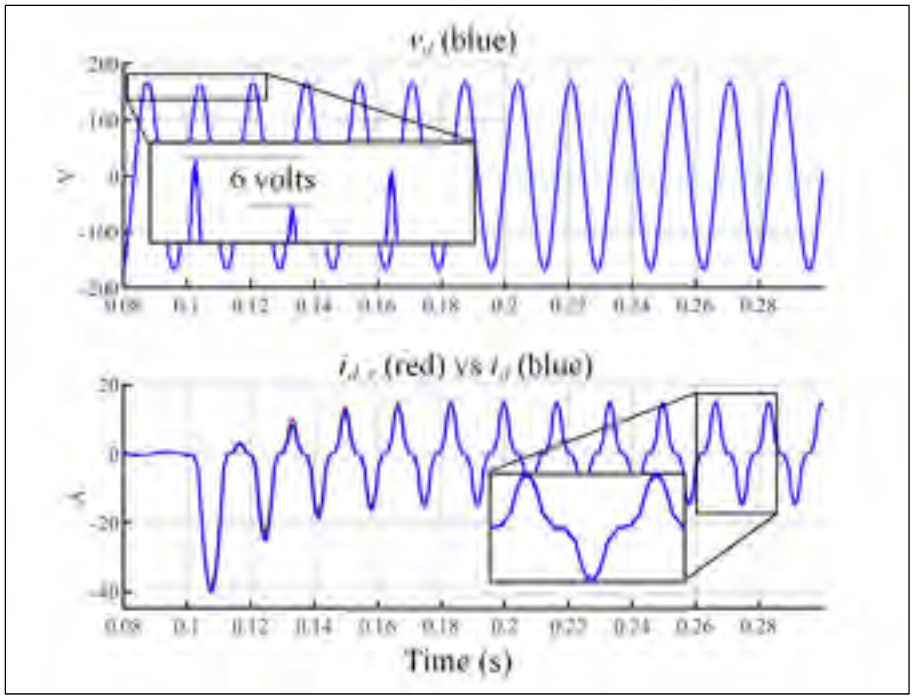

Figure 6.17 Saturable inductor emulation results

6.6.2.2 Induction motor

To validate the proper operation of the BTLM-PHIL interface, one last test was selected: the startup of an induction motor and its loading. To so, the single-phase induction machine model available in the *MATLAB/SPS* library has been used, as shown in Figure 6.18. In this machine,

the rotating field is created by an auxiliary winding using a starting capacitor until its speed exceeds 75% of the synchronous speed.

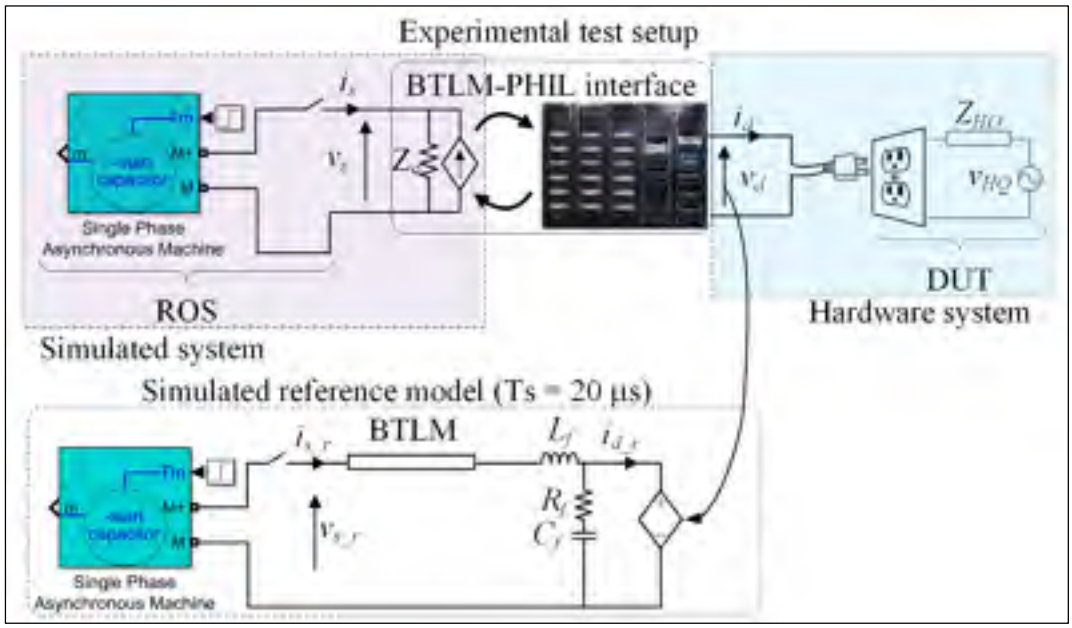

Figure 6.18 Active DUT testing (induction machine emulation)

The model parameters (see Figure 6.19) are set to the default values, i.e. nominal power of 185 W and synchronous speed of 1,800 rpm. This model is then imported into the Hypersim environment for a real-time run using the PHIL test bench.

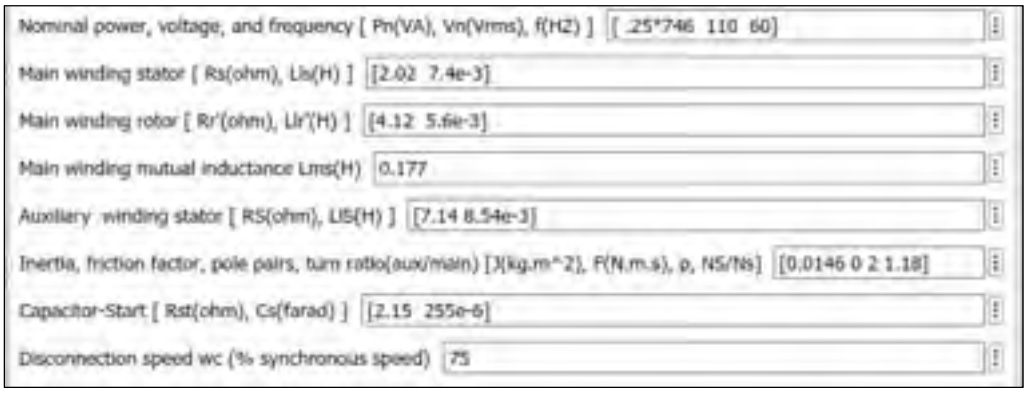

Figure 6.19 Single-phase induction machine model parameters

The experimental results are compared in Figure 6.20 with those for the reference model when the machine is started up and put on load. Four subgraphs show the signals below: (1) mechanical quantities such as the rotor speed and the average electromagnetic torque; (2) RMS electrical quantities such as the measured electrical outlet voltage and current; (3) the transient voltage and current during startup; and (4) the transient voltage and current when the machine is put on load.

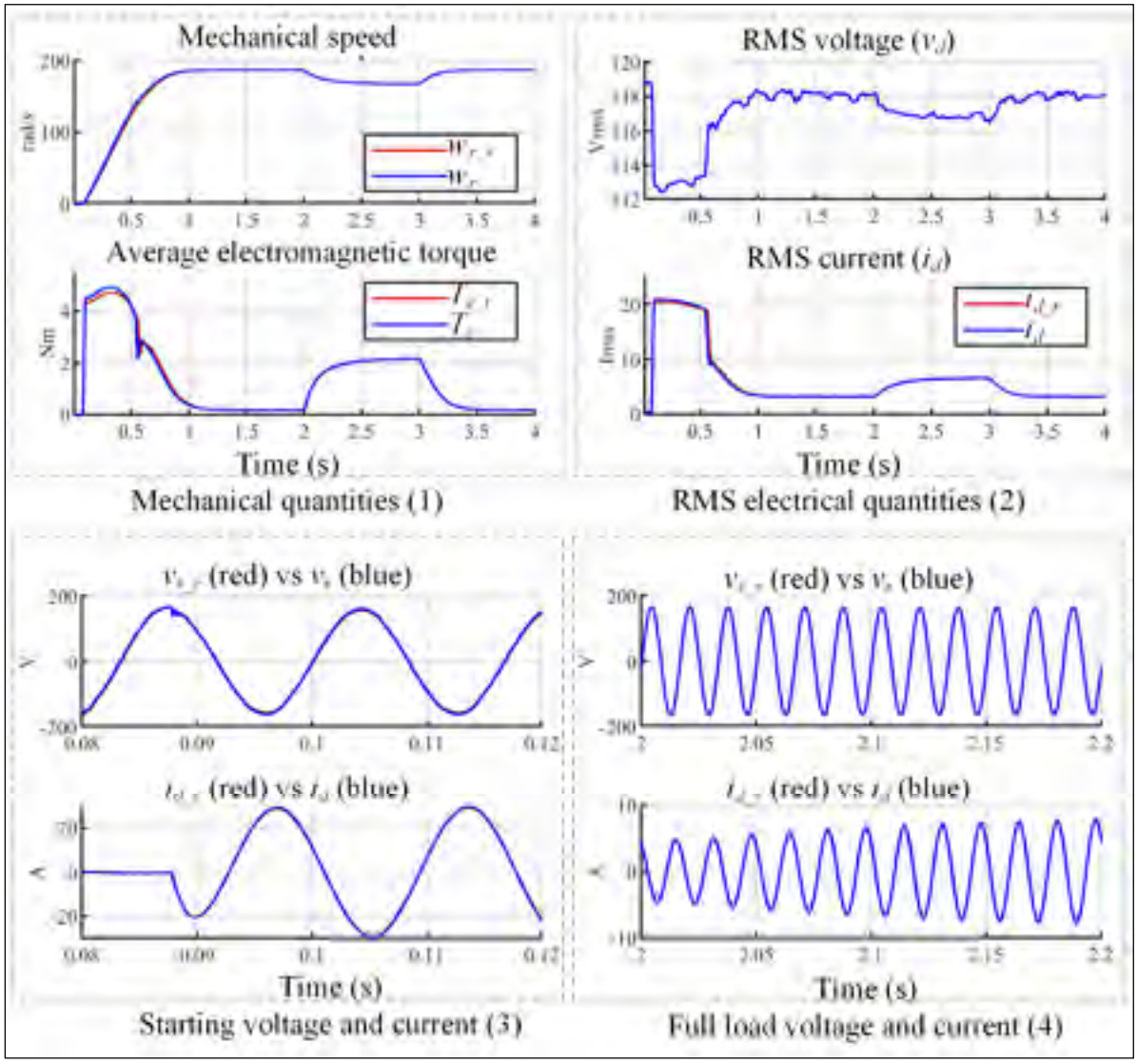

Figure 6.20 Induction machine emulation results

The machine is turned on at t = 0.0878 s using a series circuit breaker. At that moment, a large inrush current (i_d = 20 A_{RMS} for 0.5 s) allows the rotor to accelerate to 75% of its synchronous speed. Slight differences (500 mA) can be observed in the RMS current i_d (which also impact the couple T_e and the velocity w_r); these can be attributed to the equivalent impedance Z_{eq} of the PHIL test bench[15]. The inrush current is so large that it causes a drop in the electrical outlet RMS voltage (v_d), thus demonstrating once more how important it is to close the loop to model the overall behavior of the system properly and realistically.

At t = 0.56 s, the rotor speed reaches 141.4 rad/s and triggers the opening of the startup capacitor in the auxiliary circuit of the machine. The current then decreases instantaneously and continues to decrease until t = 1 s, when the no-load speed is reached. Since the speed of the machine on the test bench is slightly different from the reference case speed, the starting capacity is not disconnected exactly at the same moment.

At t = 2 s, a mechanical torque of 2 Nm (twice the nominal torque) is applied for 1 s. Please note the excellent agreement between the experimental results and those obtained for the reference model. This demonstrates once again the ability of the PHIL test bench to model accurately the behavior of this complex impedance.

6.7 Conclusions

In this chapter, the accuracy of the results obtained using the experimental PHIL test bench has been validated, including the BTLM-PHIL interface implementation. It was necessary to first ensure that the parameters used with the BTLM-PHIL had a negligible effect and that the effective line delay was the same as the theoretical value. Once this was done, it was possible to characterize the internal impedance of the power amplifier to adjust the compensation system parameters. Several benchmarks were then developed to test the PHIL system. In every

[15] As shown in section 6.5.2, this impedance varies according to the frequency and also depends on the current flowing through the power amplifier.

case, the results agreed with those obtained with fully simulated reference models. The PHIL can be used to emulate both power grids and impedances (linear or nonlinear), thus demonstrating the flexibility of its operating modes. These benchmarks can now be used as references for the development and the validation of new digital interface algorithms (DIAs). This is an additional contribution of this work.

The new BTLM-PHIL method has therefore allowed for the stable and accurate simulation of low-short-circuit-ratio power grids, islanded grids and even the switching of complex nonlinear loads, something that virtually impossible for other DIAs.

The good overall performance of the system is in part due to the careful design of each element of the system (simulator, inputs/outputs, FPGA, power amplifier, output filter and measurement system). A detailed understanding of the operation of each element combined with a careful implementation of the BTLM-PHIL algorithm are required to achieve this level of performance.

The next chapter will give an overview of some applications of the PHIL test bench, including its ability to extract the frequency response of a DUT and tests performed on residential photovoltaic panel inverters.

CHAPTER 7

PHIL TEST BENCH OPERATION

7.1 Introduction

The emergence of new distributed generation technologies that can be used at the residential level (e.g. PV panels, storage batteries and inverters) has raised concerns and questions regarding their impact on Hydro-Québec's transmission system. For example, the massive integration of residential PV inverters could have a major impact on the transmission system although they are connected at the distribution level. To properly assess their impact on Hydro-Québec's power system, it is therefore to acquire a detailed knowledge of the available control modes and the transient behavior of the main types of inverters that are likely to be connected to the grid.

The operation of the PHIL test bench has been identified by Hydro-Québec TransÉnergie (HQT) as an efficient means of better understanding the closed-loop operation of residential PV inverters. This decision stems from the sizing of the test bench, which supports the desired voltage and power levels, and its ability to operate in closed-loop mode with a simulated grid.

This chapter is divided in two. In the first section, the PHIL test bench is used to extract the impedance as a function of the frequency for the power grid behind the laboratory electrical outlet. Extracting this frequency response is key to assessing the stability of inverters connected to power grids. In the second section, the PHIL test bench is used to study the transient behavior of residential PV inverters. It will be shown that closed-loop testing helped identify operating anomalies in some inverters.

7.2 Frequency response of Hydro-Québec's laboratory grid

The ability of the PHIL test bench and the new BTLM-PHIL method to emulate various grids and impedances can be used to deal with an important issue involving the analysis of the

stability of inverters connected to various power systems as this method can be used to extract the frequency response of the grid using a current source. This can be used to check for harmonic interactions that could for example occur with series compensated power systems and low short-circuit capacity systems. For example, this type of interaction has been observed in a 500-kW solar generating station (Li, 2018) and it has been documented by (Ackermann, Bihler, & Rogalla, 2016; Adib, Mirafzal, Wang, & Blaabjerg, 2018). Furthermore, the North American Electric Reliability Corporation (NERC) issued in 2017 guidelines for the integration of inverters with low short-circuit capacity power systems[16].

This type of instability can be forecast using techniques that rely on the grid frequency response at the connection point and the frequency response of the inverter to be connected. The frequency response of the inverter can be obtained by connecting a controlled voltage source to it in an open-loop configuration. However, acquiring the frequency response of the power grid is more challenging since the DUT—which is in this case the power grid—behaves as a voltage source, thus making it necessary that the ROS be a current-source load. This current source operating mode is only compatible with a stable and accurate DIA such as the new BTLM-PHIL algorithm since the ROS impedance is theoretically infinite, which makes the above-mentioned DIAs unstable.

To demonstrate this ability, it is proposed to use the PHIL test bench to extract the frequency response of the equivalent power grid behind the laboratory electrical outlet. To do so, a harmonic current source is connected on the ROS-side, as shown in Figure 7.1. The i_s current is then set by this source, with a 2-A intensity at 60 Hz, to which an additional 2-A current is added at a frequency that ranges from 20 Hz to 5 kHz. The impedance seen on the electrical outlet side (Z_d) can then be calculated by applying the Fourier transform to the measured voltage v_d and the measured current i_d at each of the desired frequencies. To improve the

[16] “Integrating Inverter Based Resources into Low Short Circuit Strength Systems”, Reliability Guideline, December 2017

accuracy of the results, the current and voltage harmonics naturally present on the power grid are measured and removed from the processed signal.

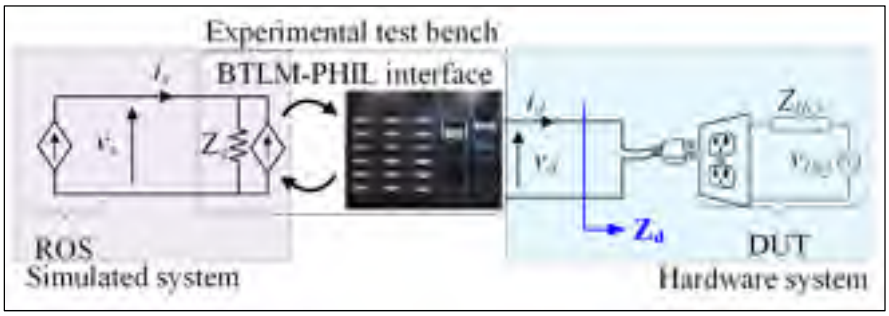

Figure 7.1 HQ laboratory electrical outlet tests

The real and imaginary components of the measured impedance Z_d are shown in Figure 7.2. The real component increases from 0.3 Ω (at 20 Hz) to 1.25 Ω (at 2 kHz), then falls back to 0.6 Ω (at 5 kHz). The imaginary component goes from 0 to 0.8 Ω, decreases to 0.25 Ω, then increases again linearly.

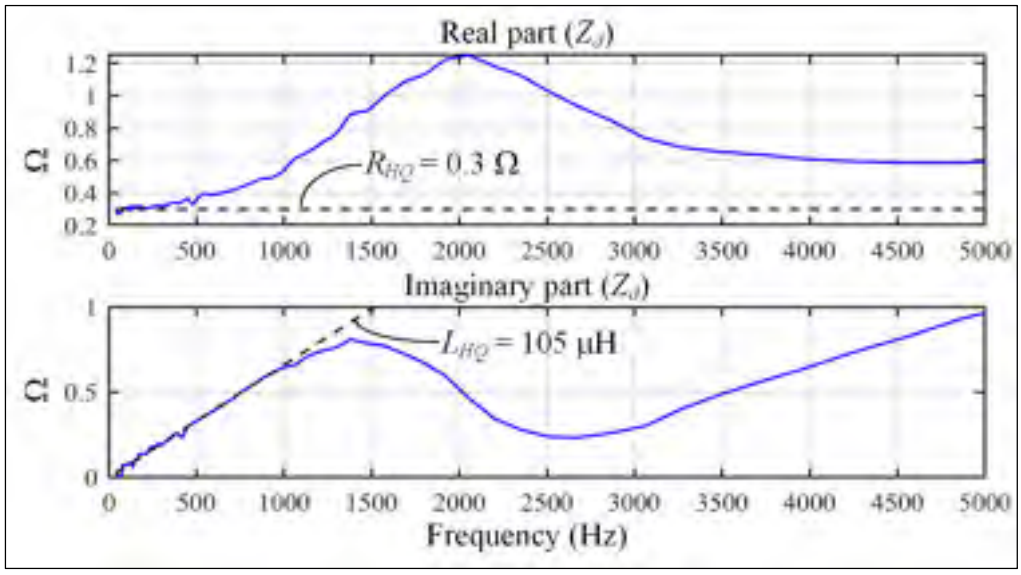

Figure 7.2 Frequency response of HQ's power system (laboratory outlet)

Although this is not a goal of this dissertation, this graph can be used as an input to the methods used to determine the stability of inverters connected to this power system.

For the purposes of this chapter, one important information to extract from this graph is the grid impedance at 60 Hz since this value will be used to validate the results obtained using the PHIL test bench connected to a PV inverter. Approximating this impedance using an equivalent resistance and inductance at 60 Hz yields: R_{HQ} = 0.3 Ω and L_{HQ} = 105 µH.

7.3 Study of the transient behavior of residential PV inverters

This study is the first phase of a project aimed at thoroughly understanding the operation and interactions of residential PV inverters to develop EMT-type simulation models. To do so, various tests modeling actual grid events (e.g. line losses, generation/load losses and even short-circuits) are performed on some PV inverters. The goal of this study is to check whether residential PV inverters can meet IEEE-1547 requirements under realistic conditions, i.e. with actual grid parameters.

Tests were first performed using a programmable open-loop source on eight residential PV inverters to assess their compliance with various current standards. These tests were used to validate, for example, whether these devices are immune to typical voltage and frequency variations. However, it was not possible to use these tests to check for potential interactions between these inverters and the various types of power systems to which they may be connected. Such interactions can only be replicated through closed-loop tests. Therefore, HQT decided to use the PHIL test bench to carry out this study.

Although the results of this study are restricted to confidential internal report, some device behaviors merit special attention and are covered in this section. First, the parameters of the system under study are presented along with an aggregation method. The PHIL test bench is then configured to model a residential electrical circuit and its parameters are set in accordance

with the aggregate system under study. Finally, the results for some tests on two residential inverters are presented.

7.3.1 Parameters of system studied

The residential inverter test must be performed in a representative environment, i.e. the inverters must be connected to a distribution system with realistic impedances. A typical connection of a home to a distribution feeder line is shown in Figure 7.3. In this case, a 120-kV transmission system supplies power to a distribution substation that consists in a wye-delta 120-kV/25-kV 47-MVA transformer (10% leak impedance) and a grounding transformer. An overhead feeder line then supplies electricity to each home through 14.4-kV–120-V/240-V single-phase low-voltage transformers with an equivalent nominal capacity of 10 kVA (leak impedance of 1.6%). In reality, a higher capacity transformer is used to supply several homes, but its equivalent capacity per home is approximately 10 kVA. Finally, low-voltage wires are used to connect each home to the transformer.

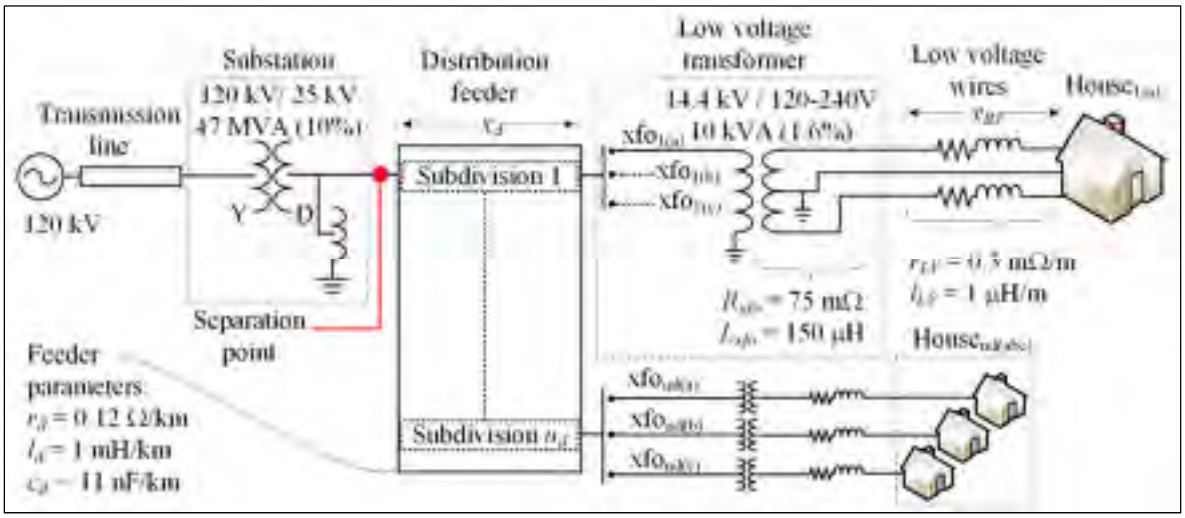

Figure 7.3 Typical feeder line connection

For this study, it is proposed to build an aggregate model to the right of the separation point, located in the secondary circuit of the distribution substation transformer. To do so, the distribution feeder line is treated as n_d subdivisions of identical feeder lines that are parallel to

each other, have the same length and are balanced. Each subdivided feeder line supplies power to a single home and carries a fraction n_d of the total power flowing over the feeder line. Each home has its own transformer, its own low-voltage cable and its own load. The transformers, lines and loads are the same for all homes.

In addition, to simplify the PHIL test bench implementation, the subdivided feeder line impedances are shifted to the low-voltage (240-V) side and represented as seen by a single home (see Figure 7.4). The low-voltage transformer magnetization branch is not considered for the time being although it could be implemented in the OFCIE.

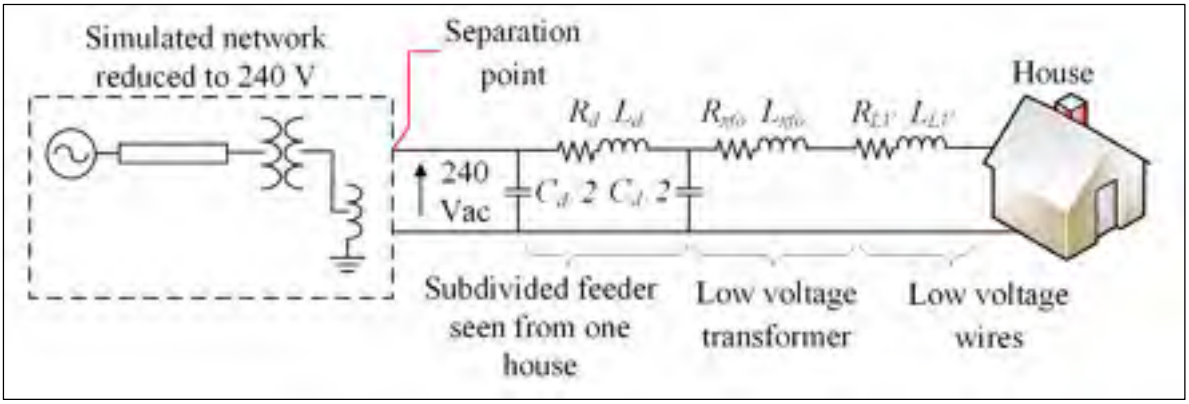

Figure 7.4 Equivalent impedances as seen from a home (aggregate model)

The equivalent R_d, L_d and C_d parameters (at 240 V) are determined for a typical case, i.e. 200 customers connected to each phase (number of subdivisions $n_d = 200$), a line length of 15 km (x_d = 15) and a low-voltage transformer winding ratio (n = 240/14400). This gives:

$$\begin{aligned} R_d &= n^2 n_d r_d x_d = 0.1\ \Omega \\ L_d &= n^2 n_d l_d x_d = 835\ \mu H \\ C_d &= \frac{c_d x_d}{n^2 n_d} = 2.979\ \mu F \end{aligned} \tag{7.1}$$

As for the low-voltage lines, a 25-m length (x_{BT}) was selected (giving a 50-m round-trip length):

$$R_{LV} = 2r_{LV}x_{LV} = 0.015\ \Omega$$
$$L_{LV} = 2l_{LV}x_{LV} = 50\ \mu H \quad (7.2)$$

7.3.2 Experimental setup

The selected residential photovoltaic (PV) panel inverters are connected at a nominal voltage of 240 V. Although the PHIL test bench is a three-phase system, it was configured as a two-phase system to replicate the residential 120-V/240-V circuit, as shown in Figure 7.5. Two of the test bench phases are used in a superimposed configuration to create this voltage level; this also gives access to the neutral point (as in the case of a residential circuit). A Keysight (*N8937APV*) DC voltage source is used to emulate the solar panels based on programmed V-I characteristics.

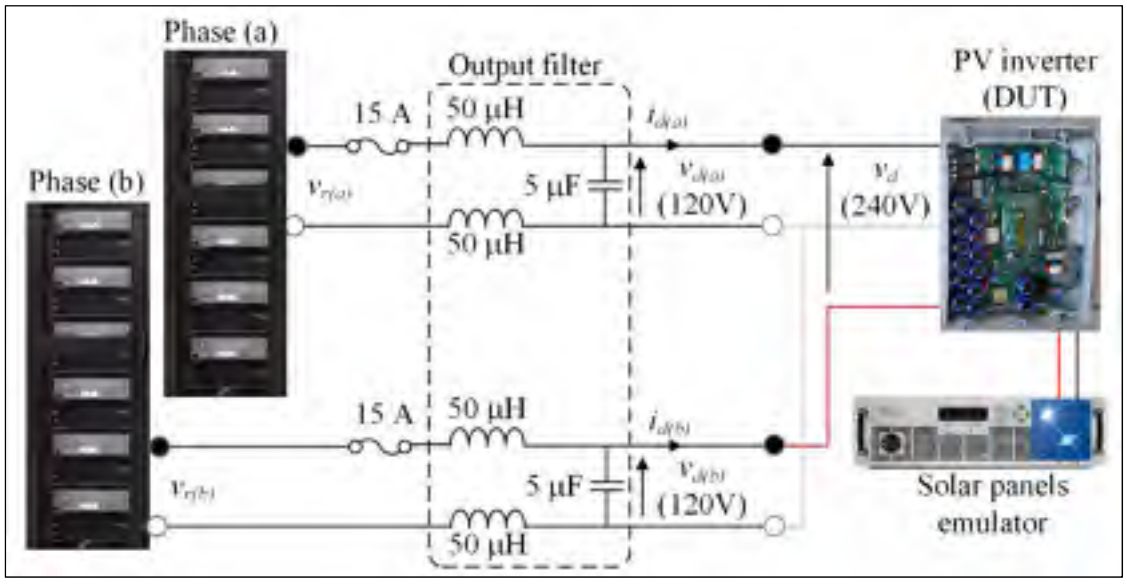

Figure 7.5 240-V test bench configuration

The equivalent diagram of the PHIL system used to model this configuration is shown in Figure 7.6. This system already includes impedances due to the output filter and the decoupling line (BTLM-PHIL interface), which must considered to properly model the aggregate system.

It is therefore necessary to match the parameters of the aggregate model shown in Figure 7.4 with those of the PHIL test bench shown in Figure 7.6. First, the total output filter inductance (L_f = 200 µH) is used to represent both the low-voltage transformer inductance (L_{xfo} = 150 µH) and the low-voltage line inductance (L_{BT} = 50 µH).

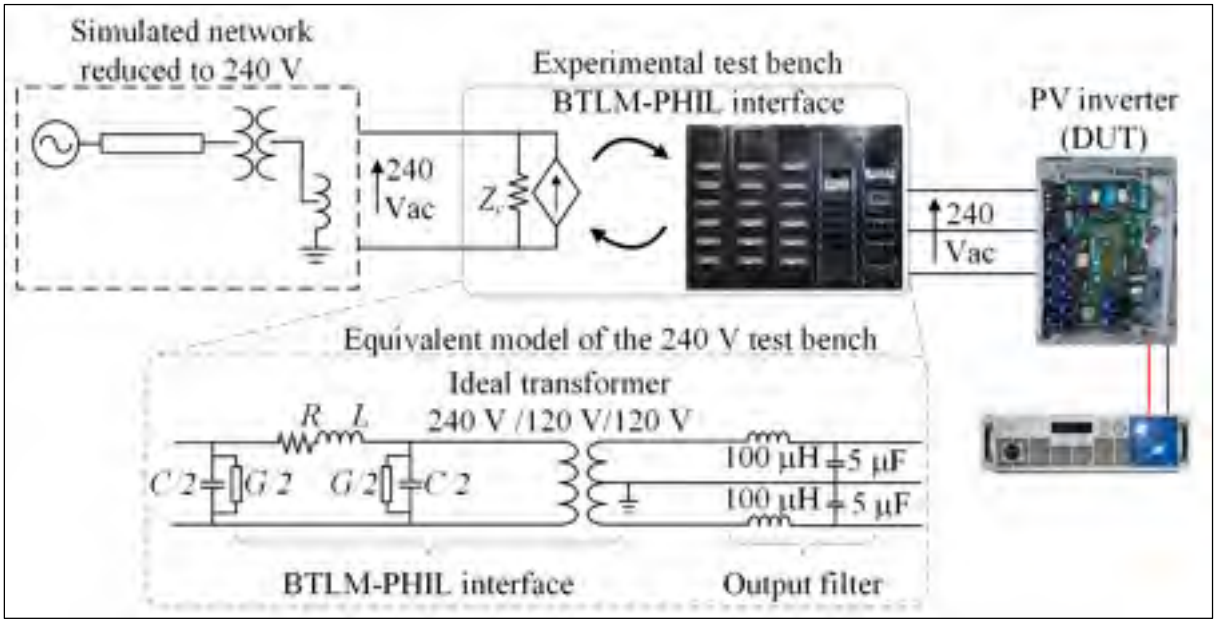

Figure 7.6 Equivalent diagram of 240-V PHIL test bench

Next, the parameters of the BTLM-PHIL interface are used to model the subdivided feeder line as seen by a home in addition to several other impedances. These impedances represent all the series resistances (feeder line, transformer and low-voltage lines), the feeder line inductance and the feeder line capacitance, from the 240-V output filter capacitance has been subtracted (C_f = 2.5 µF) since it is absent from the aggregate system. This results in the following set of parameters for the BTLM-PHIL line:

$$R = R_d + R_{xfo} + R_{LV} = 0.19\ \Omega \tag{7.3}$$
$$L = L_d = 835\ \mu H$$
$$C = C_d - C_f = 0.479\ \mu F$$

Since a lossy line is used, an equivalent conductance (G) appears[17]; it is calculated using equation (4.22):

$$G = \frac{RC}{L} = 109\ \mu S \tag{7.4}$$

In addition, using equation (4.39), it is possible to calculate the characteristic impedance Z_c and the propagation constant τ :

$$Z_c = \sqrt{\frac{L}{C}} = 41.79\ \Omega \tag{7.5}$$
$$\tau = \sqrt{LC} = 20\ us$$

This implies that the dynamic behavior of the 240-V PHIL test bench with a single home connected to an equivalent 240-V power system is similar to the behavior of 200 homes connected to each phase of the 25-kV feeder line. The simulated power system is then connected to the 25-kV feeder line at an equivalent distance of 15 km.

This power system will therefore be considered strong since the line load will be less than its rated capacity, i.e. approximately 500 customers per phase. To represent a weaker power system, it is possible to increase either: (1) the number of customers connected through the characteristic impedance of the equivalent line; or (2) the impedance of the simulated power system. The recommended approach in this case is to increase the impedance of the simulated power system since it would then be easier to change system parameters.

[17] At 240 V, the Joule losses associated with this conductance are only 6.28 W, which turns it negligible relative to the nominal power of the 2-kW system.

7.3.3 Residential inverter testing

The study conducted on the behalf of HQT involved several test cases for power systems with a strong/weak short-circuit capacity at various solar irradiance levels. For each of the five inverters that were tested, approximately 60 tests representing various power system contingencies were conducted. The results of two main tests—requiring a closed-loop configuration—are presented in this dissertation. The first test consisted in validating the ability of the PHIL test bench to replicate laboratory electrical circuit interactions when impedances are physically added. The second test showed that an inverter behaves abnormally if a disturbance occurs when it is connected to a higher impedance system, thus demonstrating the need for closed-loop testing.

7.3.3.1 Comparison of results – HQ outlet versus test bench

The setup used to compare the results is shown in Figure 7.7. The PV inverter (*Kaco blueplanet 5.0*[18])—connected to the solar panel emulator—is either connected to the laboratory electrical circuit or to the PHIL test bench emulating an equivalent circuit. Inductances and the test bench output filter are added in series to the laboratory electrical outlet to replicate the impedance of the PHIL test bench. For these comparative tests, the test bench no-load voltage (v_{HQ12}) has been adjusted to the same voltage as the electrical outlet. In addition, the total series impedance Z_{tot}—comprising R_{tot} and L_{tot}— of the test bench has been adjusted to make it equal to the sum of the series impedances of the electrical outlet and the additional series inductances.

Note 1: For the calculation of Z_{tot}, impedances Z_{HQ1} and Z_{HQ2} are treated as an RL impedance whose value is determined using Figure 7.2 ($R_{HQ1} = R_{HQ2} = 0.3\ \Omega$ and $L_{HQ1} = L_{HQ2} = 105\ \mu H$).

[18] Although this inverter has a rated capacity of 5 kVA, it is operated at 2 kVA, which is the rated capacity of the PHIL test bench.

Note 2: In this comparative test, some differences can be attributed to the electrical circuit behind the laboratory electrical outlet: presence of voltage harmonics, amplitude/frequency variability, and finally, differences between actual equivalent impedance Z_{HQ} and RL circuit.

Note 3: It has been established that the outlet filter capacitance does not affect the dynamics of the observed instability modes since tests with and without the output filter capacitance have given virtually identical results.

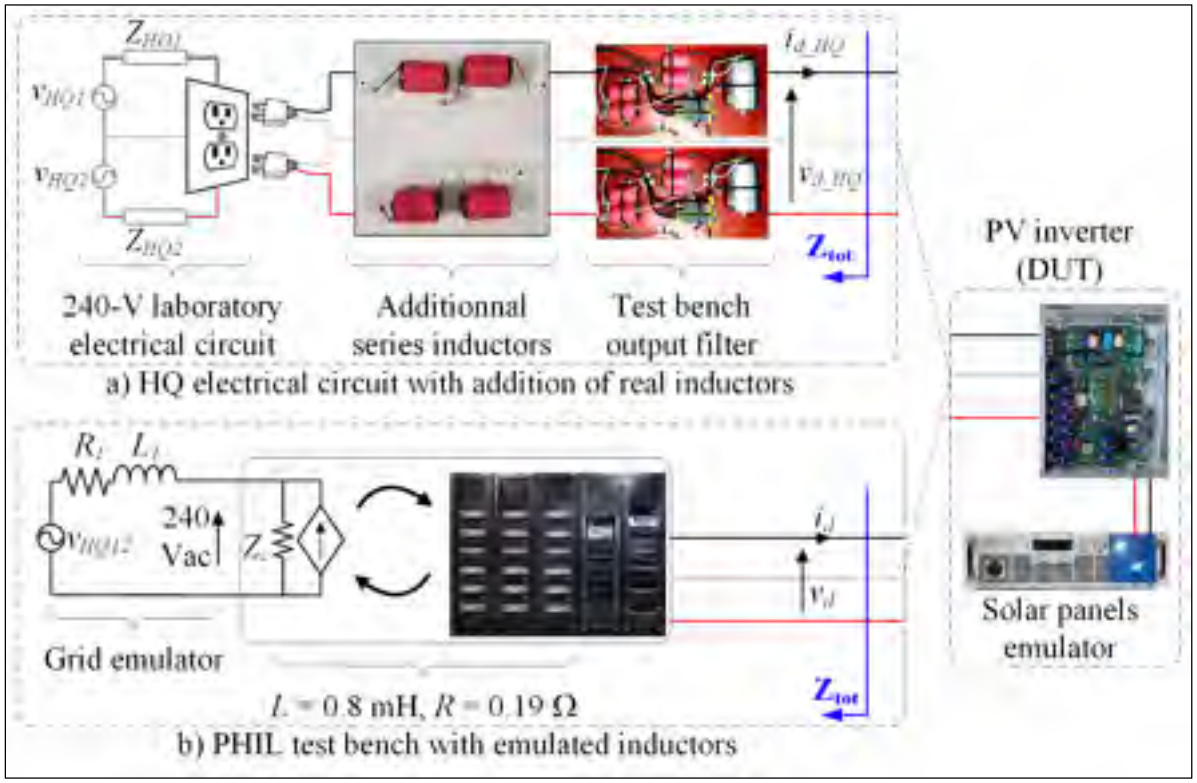

Figure 7.7 Comparative test setup: a) HQ outlet; b) PHIL test bench

Case 1: 47-kVA (X/R = 1.13) short-circuit capacity

The first test was carried out with a strong power system (L_{tot} = 2.4 mH and R_{tot} = 0.8 Ω), i.e. one whose short-circuit capacity is 25 times the inverter operating power and approximately 10 times its nominal capacity (SCR = 10). The RMS currents and voltages measured during startup and ramping are shown in Figure 7.8 (1). Please note the very good agreement between

the results and the slight voltage increase, given the relatively low power system impedance, due to the current increase. Figure 7.8 (2) shows the instantaneous currents and voltages at t = 4 s, while Figure 7.8 (3) shows the same signals at t = 9.8 s. It is possible to see the current distortions generated by the inverter and their weak impact on the voltage. When the inverter is connected to the PHIL test bench, the results are similar to those obtained by connecting it to the electrical outlet.

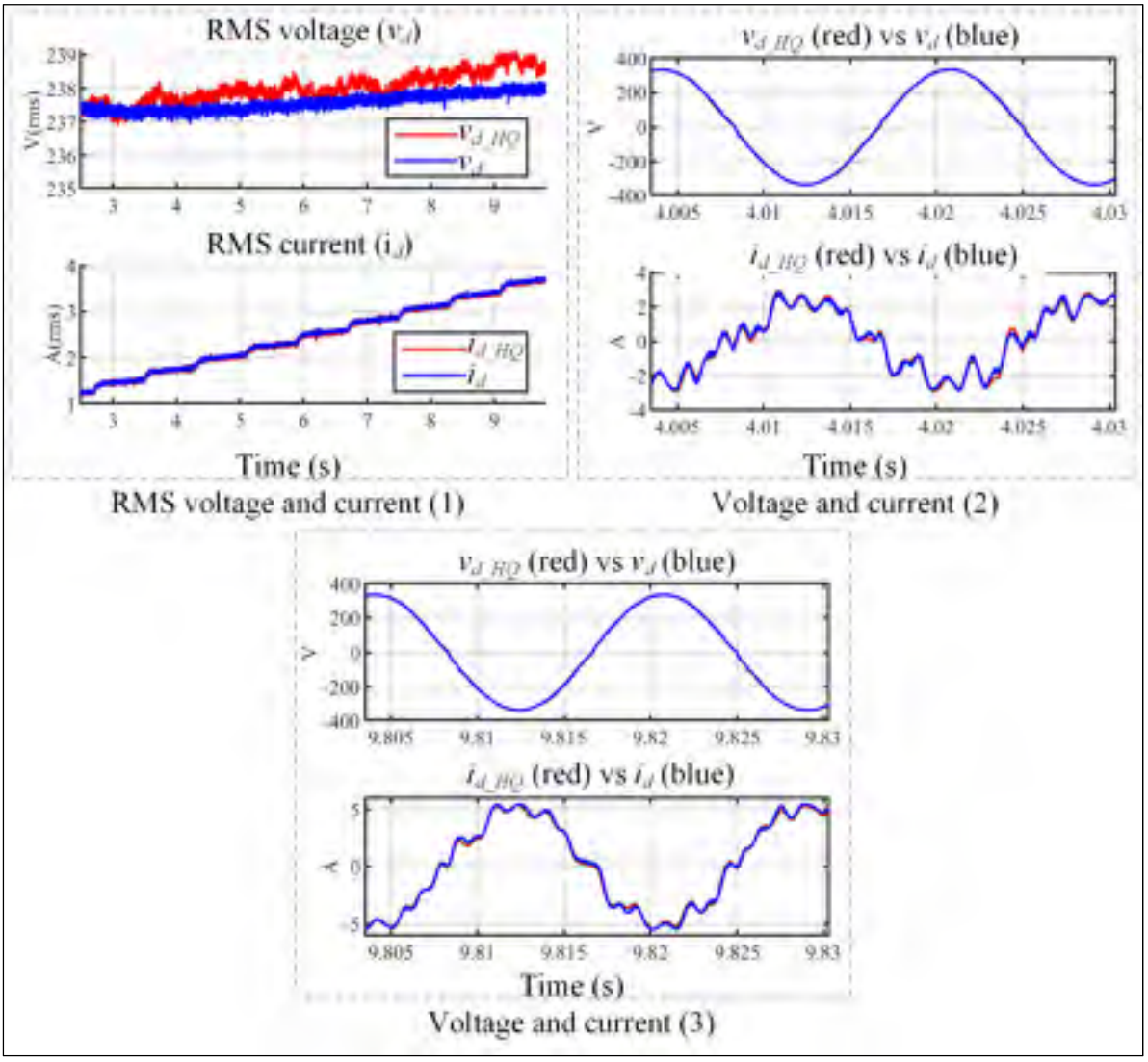

Figure 7.8 Kaco inverter results with strong power system (SCR = 10)

Case 2: 27-kVA (X/R = 1.18) short-circuit capacity

The second test was performed with a weaker power system (L_{tot} = 4.4 mH and R_{tot} = 1.4 Ω), but still 13 times more powerful than the operating power of the inverter and approximately 5 times stronger than its nominal power (SCR = 5). The RMS currents and voltages measured during startup and ramping are shown in Figure 7.9 (1). Despite slight differences in the voltage signal at startup, which results in a slight current offset, it is possible to observe an increase in the voltage as the current increases since the power system impedance is greater. Figure 7.9 (2) shows the instantaneous currents and voltages at startup (i.e. At t = 0.37 s), while Figure 7.9 (3) shows the same signals at t = 7.97 s. During startup, the current distortions generated by the inverter do not affect the voltage. However, an interaction occurs when the current increases; it results in such a voltage distortion that the inverter ends up disconnecting from the power system. The agreement between the PHIL test bench results and the electrical outlet results shows that these harmonics stem from a real interaction between the control system of the PV inverter and the impedance of the power system to which it is connected. This finding confirms once more that the PHIL test bench is capable of faithfully modeling the interactions between real hardware and emulated power system impedances.

The results obtained in both cases clearly show that:

- The PHIL test bench faithfully replicates the phenomena observed using the laboratory electrical circuit.
- Both the observed current distortions and their impacts on the voltage signal are therefore not artifacts caused by the test bench or the new BTLM-PHIL.

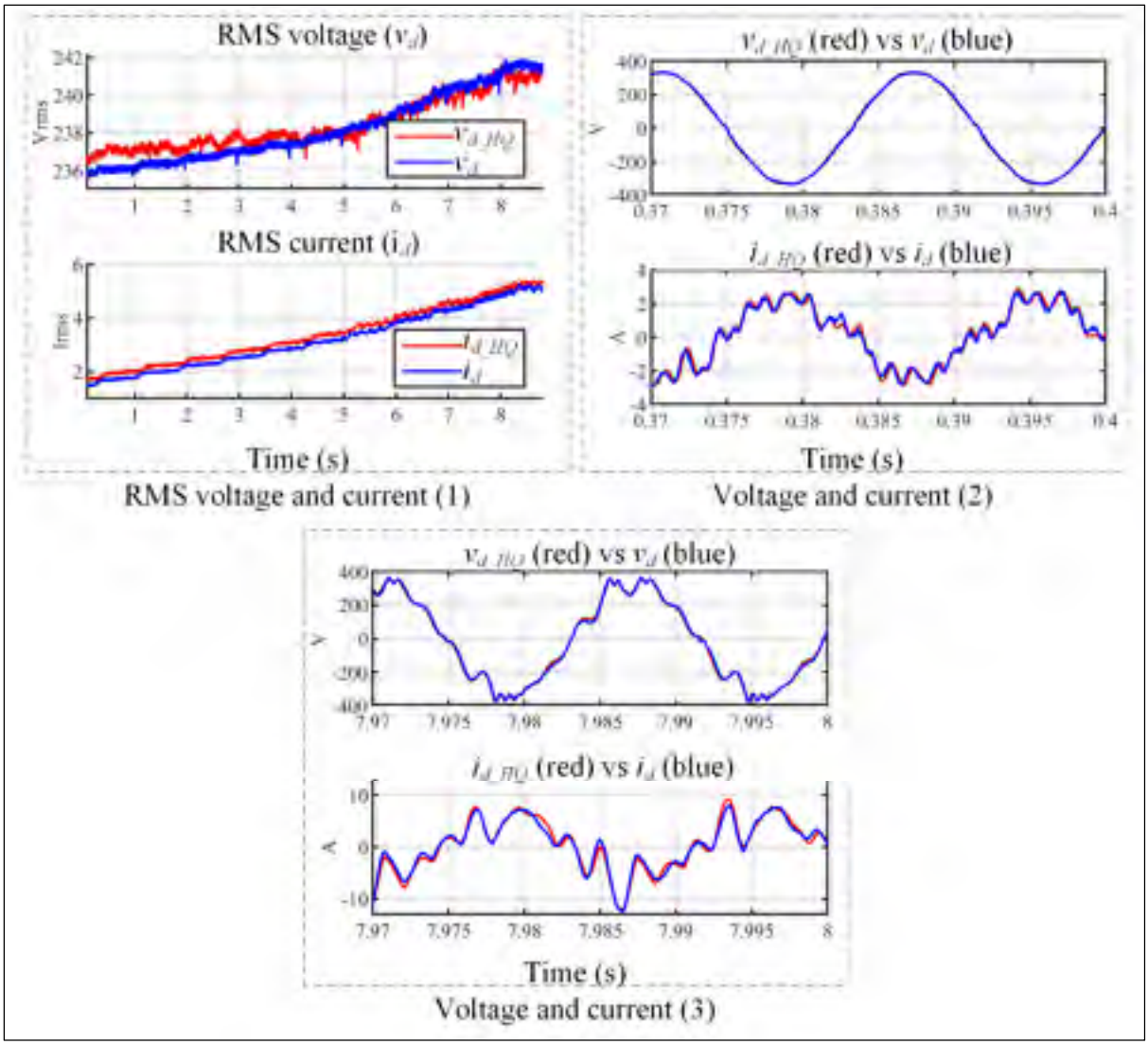

Figure 7.9 Kaco inverter results with weaker power system (SCR = 5)

7.3.3.2 Voltage dips – strong/weak power system

Using the PHIL test bench in a closed-loop configuration, it is possible to carry out an important test, which consists in generating a 25% voltage dip during 60 cycles for various power system impedances. Please note that this test cannot be performed using the laboratory electrical outlet since it would require the addition of a load of approximately 35 kVA, which would damage the power system.

Per Standard IEEE-1547, the inverters should remain connected during and after this voltage dip, something that inverter manufacturers normally verify through open-loop tests. Figure 7.10 shows the experimental results obtained for the SolarEdge inverter[19] (*SE-3000A-US*) for a very strong power system (SCR = 50), which is tantamount to performing an open-loop test, and also for a weak power system (SCR = 5). Figure 7.10 (1) shows the RMS currents and voltages measured before, during and after the voltage dip that occurs from 0.1 s to 1.1 s. In both cases, the inverter remains connected as required, but its behavior is noticeably different during the voltage dip, especially when the voltage is restored (in particular at t = 1.65 s). Figure 7.10 (2) reveals a similar behavior with respect to the instantaneous currents and voltages during the voltage dip at t = 0.1 s. Slight differences are caused by a different operating point due to the absence of a maximum power point tracker (MPPT). Finally, Figure 7.10 (3) shows the instantaneous currents and voltages in a region where the inverter behaves poorly when it is connected to a weak power system. At that moment, current harmonics generate significant voltage distortions and seem to cause the internal PLL of the inverter to lose synchronization (at t = 1.65 s and t = 1.7 s). The PV inverter finally resumes normal operation at t = 1.8 s, thus ending the unwanted voltage distortions.

[19] This inverter was tested without maximum power point tracker (MPPT) at a solar irradiance level of 50%, i.e. for an equivalent power of approximately 1 kW.

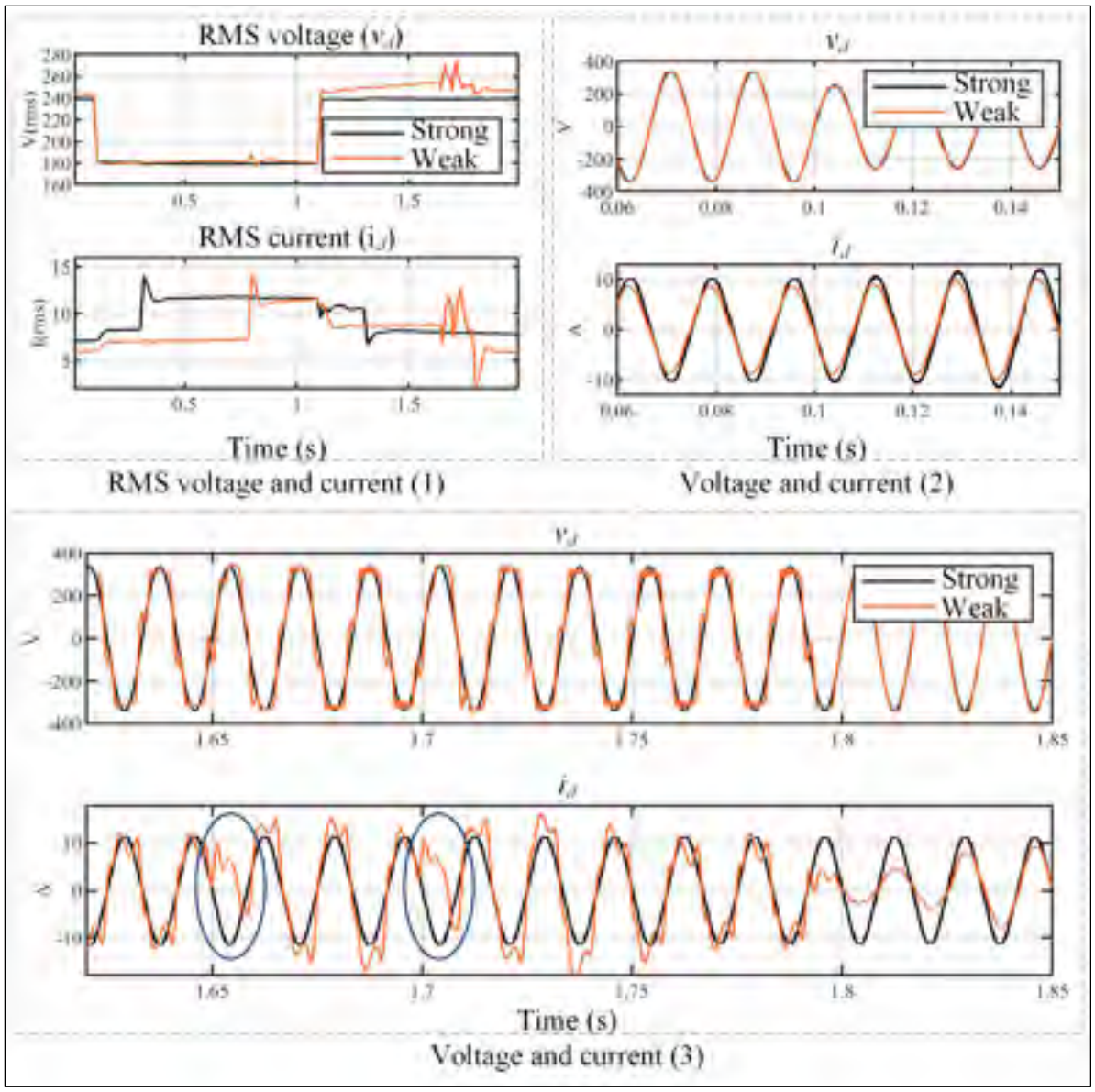

Figure 7.10 Voltage dips with strong/weak power system – SolarEdge inverter

These operating differences between a strong and a weak power system could not have been observed through open-loop testing of the inverter. Close-loop tests are therefore essential to check for potentially adverse interactions involving the inverter, neighboring equipment or even the transmission system if several similar inverters are operating simultaneously

7.4 Conclusions

This chapter covered the use of the PHIL test bench with the new BTLM-PHIL interface method. Closed-loop testing has been identified as an essential tool for studying in detail the interactions between PV inverters and the power systems to which they are connected. In fact, this work has been accepted for publication in the proceedings of the *IEEE Power and Energy Society General Meeting* (Rimorov et al., 2020).

A major contribution of this work is the development of a method for selecting the PHIL test bench parameters to model a realistic case involving the aggregated connection of a feeder line to a transmission system. To do so, it was necessary to take advantage of the flexibility of the test bench, which make it possible to reconfigure it as a two-phase residential circuit. A second contribution is demonstrating the necessity of closed-loop testing to validate interactions between the DUT and various types of ROS since the first tests were able to validate, using the laboratory electrical outlet, that the PHIL test bench can replicate faithfully major harmonic interactions between PV inverters and high-impedance power systems. It is only possible to replicate these interactions because the closed-loop BTLM-PHIL interface is operating properly. Finally, voltage dip tests on strong and weak power systems have revealed significantly different behaviors that could never have been replicated using an open-loop configuration. These tests are essential to ensure the seamless integration of distributed energy resources (DERs) with power systems that do not have a high short-circuit capacity.

CONCLUSIONS AND CONTRIBUTIONS

Hydro-Québec's research institute (IREQ) has been working since 2013 on the power simulator (SimP) project, which involves developing research and testing infrastructure to study the integration of distributed energy resources. Eventually, SimP will become an infrastructure comprising a 7.5-MVA 25-kV power amplifier connected to a real-time simulator in a closed-loop configuration designed to model transmission and distribution systems. One of the remaining major problems standing in the way of the implementation of a system of this type (i.e. a "PHIL" system) involved finding a method for interfacing the amplifier and the simulator that ensures the resulting system is transparent, stable, accurate and, most importantly, useful for conducting electromagnetic transient (EMT) studies at frequencies from 0 Hz to several kHz. When the work detailed in this dissertation began, no general solution to this problem was available in the literature.

The initial goal of this work was therefore to develop a digital interface algorithm (DIA) that was adapted to the conditions under which IREQ's PHIL system was to be used. The results achieved by the project demonstrate that this goal was reached by:

- Developing a PHIL system stability analysis method.
- Developing and implementing a new DIA based on the transmission line model.
- Building an experimental test bench, which was used to validate the DIA.
- Using the test bench to study the behavior of residential photovoltaic panel inverters.

The new PHIL system stability analysis method has resulted in a better understanding of the impact of sampling and discretization effects on the behavior of the closed-loop system. It was established that the hybrid (i.e. part analog, part digital) nature of the system must be taken into consideration when verifying its stability. This finding has led to a change in the stability criteria used until now. This work has in fact been published in *IET Generation, Transmission and Distribution* (Tremblay, Fortin-Blanchette, et al., 2017).

Once the stability problem was understood and the new analysis method had been developed, work began to focus on interface methods. Several methods were explored, from adding a filter to developing a predictive control system for time-delayed systems, including modifying the numerical integration method. These methods proved to work in simple, special cases, but they were not sufficiently general to meet the goals of this dissertation.

The most fundamental contribution to the field of PHIL systems is the development of the BTLM-PHIL method, published in *IEEE Transactions on Energy Conversion* (Tremblay et al., 2020). This method now makes it possible to interface a PHIL system using a transmission line while eliminating the physical constraints that used to make this concept unfeasible in practice. Therefore, this general method solves most of the PHIL system interface problems regardless of the nature or the complexity of the two systems to be connected.

The experimental PHIL test bench is a major asset of this project. Entirely designed and build at IREQ, this test bench was cofinanced by Natural Resources Canada (NRCan) through its Energy Innovation Program to prove the various concepts developed. This reduced-scale system made it possible to achieve a deep understanding of all the key elements of a PHIL system: topology, power switching devices, output filter, measurement system, digital simulator and FPGA implementation of DIA. This environment made it possible to implement and validate experimentally the BTLM-PHIL method. System performance was validated using reference cases. The results of these validation tests have demonstrated the ability of the PHIL system to properly emulate the behavior of power systems under various contingencies. The validation test cases developed could in fact be used as benchmarks for the development of future digital interface algorithms.

Because of the performance of the test bench, especially its flexibility and ability to faithfully model power system behavior, it was possible to carry out a study on the transient behavior of residential inverters. A significant contribution of this dissertation is the replication, using the PHIL test bench, of major adverse harmonic interactions with a weak power system. This confirms that, when connected to real hardware, such as a PV inverter, the PHIL test bench

can replicate the behavior of various types of impedances without requiring a complex experimental setup. The use of the test bench to carry out this study has also demonstrated that the methods developed for this dissertation are applicable to industrial cases. In addition, the closed-loop configuration proved essential to modeling major adverse phenomena and validating operating conditions under realistic assumptions.

Finally, this test bench provides an excellent showcase to demonstrate the feasibility and usefulness of PHIL testing of hardware. In fact, its completion was a key factor in the award of an additional NRCan grant for scaling the system up to 7.5 MVA and 25 kV.

RECOMMENDATIONS

Although the work completed as part of this dissertation has reached its goals, there are still several questions that merit further exploration.

The first recommendation is to improve the interface between the OFCIE and the power amplifier. As mentioned in section 4.6.1, the ideal transformer method (ITM) is used in some special cases, although it can become unstable. It would be interesting to widen current limits.

The second recommendation involves the output filter compensation system. This LC filter has a dynamic response that, in some cases, can interfere with the response of the system under study. A modern control approach could be used to mitigate this effect.

The final recommendation concerns the effect of the BTLM itself. As discussed in section 7.3.2, the DUT is not connected to the ROS directly, but rather through a line of a given length. In some use cases, it may not be realistic to add this line between the two systems. To eliminate this constraint, the ideal solution would be to develop a method that is based on the ideal transformer method (ITM), but preserves passivity, and hence stability.

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