Optimized Multilevel Inverters and Modulation Techniques for Power Electronics Applications

by

Mohammad SHARIFZADEH

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‘‘The man can have nothing but what he tries for’’

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Onduleurs Multiniveaux Optimisés et Techniques De Modulation Pour Les Applications D'Électronique De Puissance

Mohammad SHARIFZADEH

RÉSUMÉ

L'objectif principal de cette thèse est d'optimiser les techniques de modulation et les topologies d'onduleurs multiniveaux pour atteindre une efficacité plus élevée dans les applications d'électronique de puissance. Parmi les onduleurs conventionnels multiniveaux, les technologies compactes comme la cellule-U compacte est particulièrement intéressante pour les applications monophasées en raison de la structure continue de source CC. La cellule-U compacte apparaissait comme une topologie prometteuse qui pouvait trouver son chemin vers l'industrie, mais, elle se heurte à quelques inconvénients lorsqu'elle est étendue pour générer plus de niveaux. Le principal inconvénient est le problème de l'équilibrage de la tension des condensateurs qui nécessite une optimisation profonde pour atteindre une topologie d'onduleurs multiniveaux compacts innovantes et fiables. De même que l'optimisation de la topologie des onduleurs, les techniques de modulation doivent être optimisées pour améliorer l'efficacité des onduleurs dans les applications ciblées. Bien que les techniques populaires comme : « la Méthode du Vecteur Spatial et MLI Sinusoïdale » peuvent montrer leurs performances fiables, elles ont une fréquence de commutation élevée ce qui augmente les pertes de puissance. D'autre part, l'Élimination Sélective d'Harmoniques-MLI et l'Atténuation Sélective d'Harmoniques-MLI ont été introduites comme techniques prometteuses à basse fréquence de commutation où, elles peuvent être les candidats appropriés pour l'optimisation et l'utilisation dans les applications de haute puissance des onduleurs à multiniveaux. Comme principal effort d'optimisation de l'Élimination Sélective d'Harmoniques et de l'Atténuation Sélective d'Harmoniques, un nouvel angle de commutation a été obtenu pour une forme d'onde de tension à basse fréquence de commutation grâce à l'analyse mathématique précise sur les harmoniques triples pour auto-éliminer toutes les harmoniques triples sans faire de calculs supplémentaires. Ensuite, les harmoniques non triples déterminées sont éliminées ou atténuées par le fonctionnement normal de l'Élimination Sélective d'Harmoniques ou de l'Atténuation Sélective d'Harmoniques. Par conséquent, les amplitudes d'harmoniques maximales sont contrôlées tandis que la fréquence de commutation est au minimum.

Dans le prochain travail, l'Élimination Sélective d'Harmoniques est conçue de manière optimale pour les onduleurs triphasés 4 fils afin de fournir à la fois des charges symétriques et asymétriques en fonctionnement à basse fréquence de commutation. L'Élimination Sélective d'Harmoniques a été conçue de manière adaptable à la fois pour les deux configurations à 4 fils de l'onduleur à Point Neutre Fixe 3 phases, 4 branches 4 fils et 3 branches 4 fils. Il a été démontré que l'Élimination Sélective d'Harmoniques est plus compatible avec la configuration 3 branches 4 fils sur 4 branches 4 fils en termes de distorsion harmonique de la tension de phase de sortie, des calculs des angles de commutation et de la complexité de conception ainsi que des pertes de puissance. Le travail suivant présente une stratégie hybride de la technique de modulation l'Atténuation Sélective

d'Harmoniques pour contrôler la Tension en Mode Commun dans les onduleurs triphasés. Dans tous les travaux précédents où une solution logicielle basée sur les techniques de modulation était utilisée pour contrôler la Tension en Mode Commun, la technique appliquée a été conçue sur la base d'une sélection appropriée du vecteur de commutation. Toutefois, le travail proposé dans cette thèse, la Tension en Mode Commun est contrôlée sur la base de l'analyse harmonique afin de formuler la Tension en Mode Commun dans la technique hybride de l'Atténuation Sélective d'Harmoniques. Il a été montré que la Tension en Mode Commun a notablement été réduite par l'élimination des harmoniques triples tandis que le rapport de fréquence de commutation est maintenu sous 1 kHz. Enfin, les derniers travaux présentent un nouvel onduleur multiniveaux compact, appelé topologie Cellule-E compacte. La Cellule-E compacte est une optimisation en profondeur de la génération précédente d'onduleurs multiniveaux compacts; la Cellule-U compacte va atteindre d'autres niveaux de tension de sortie, réduire le nombre de composants et simplifier l'équilibrage de la tension des condensateurs. La Cellule-E compacte a été créé sur la base de l'idée d'étendre les condensateurs de manière horizontale contrairement à la manière verticale, ce qui se traduit par une structure plus optimisée par rapport à la Cellule-U compacte. Il a été démontré que la Cellule-E compacte peut être une topologie alternative appropriée et fiable pour remplacer la Cellule-U compacte.

Tous les travaux sont entièrement étayés par des analyses et des discussions théoriques, des simulations et des expérimentations.

Mots-clés : Onduleurs Multiniveaux, Techniques de Modulation à Faible Fréquence de Commutation, Élimination Sélective d'Harmoniques, Atténuation Sélective d'Harmoniques, Cellule-U Compacte, Cellule-E Compacte.

Optimized Multilevel Inverters and Modulation Techniques for Power Electronics Applications

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ABSTRACT

The main goal of this thesis is to optimize the modulation techniques and multilevel inverter topologies to reach a higher efficiency in power electronics applications. Among conventional multilevel inverters, compact topologies like Packed U-Cell is interesting particularly for single phase applications because of single dc source structure. Five-level Packed U-Cell appeared as a promising topology that could find its way to industry; but, it confronts some drawbacks when it is extended to generate more levels. The main drawback is the capacitor voltage balancing issue which demands a deep optimization to reach a novel and reliable compact multilevel inverter topology. Along with optimization of the inverter topology, modulation techniques need to be optimized to enhance the inverters efficiency in the targeted applications. Although popular techniques like SVM and SPWM could show their reliable performance, they have high switching frequency which increases power losses. On the other hand, SHE-PWM and SHM-PWM were introduced as a promising low switching frequency techniques where, they can be the appropriate candidates for optimization and utilization in high power applications of multilevel inverters. As the primary effort for optimization of the SHE and SHM, a new switching angles has been obtained for a low switching frequency voltage waveform through the precise mathematic analysis on the triplen harmonics to self-eliminate all triplen harmonics without doing any extra calculations. Then, the determined non-triplen harmonics are eliminated or mitigated by the normal operation of the SHE or SHM. Therefore, maximum harmonics amplitudes are controlled while the switching frequency is at minimum.

In the next work, SHE is optimally designed for 3phase 4wire inverters as to supply both symmetrical and asymmetrical loads under low switching frequency operation. SHE has been adaptably designed for both 4wire configurations of 3phase NPC inverter; 4leg 4wire and 3leg 4wire. It has been shown that SHE is more compatible with 3leg 4wire configuration over 4leg 4wire one in terms of harmonic distortion of output phase voltage, switching angles calculations and design complexity as well as power losses. Next work presents a hybrid strategy of SHM modulation technique for controlling CMV in 3phase inverters. In all previous works where software solution based on the modulation techniques was used to control CMV, the applied technique was deigned based on the proper selection of the switching vector. However, it the proposed work in this thesis, the CMV is controlled based on the harmonic analysis in order to formulize CMV in the hybrid SHM technique. It was shown that CMV is notably reduced by elimination of triplen harmonics while the switching frequency ratio is kept under 1KHz. Finally, last work introduces a novel compact multilevel inverter so-called as Packed E-Cell topology. Packed E-Cell is a deep optimization of previous generation of compact multilevel inverter; Packed U-Cell to reach further output voltage levels, reduced components counts and simplicity in capacitor voltage balancing. Packed E-Cell has been established based on the idea of extending the capacitors in

horizontal way unlike vertical way which results in more optimized structure compared to Packed U-Cell. It was shown that the Packed E-Cell can be a suitable and reliable alternative topology to replace Packed U-Cell.

All works are fully supported by theoretical, simulation and experimental analyses and discussion.

Keywords: Multilevel Inverters, Low Switching Frequency Modulation Techniques, Selective Harmonic Elimination, Selective Harmonic Mitigation, Packed U-Cell, Packed E-Cell.

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LIST OF ABREVIATIONS

CHB	Cascaded H-Bridge
DC	Direct Current
FC	Flying Capacitor
NPC	Neutral Point Clamped
PUC	Packed U-Cell
PEC	Packed E-Cell
SVM	Space Vector Modulation
SPWM	Sinusoidal Pulse Width Modulation
SHE-PWM	Selective Harmonic Elimination-Pulse Width Modulation
SHE-PWM	Selective Harmonic Mitigation-Pulse Width Modulation

INTRODUCTION

The DC-AC converters which are well-known as inverters can produce AC staircase voltage waveform using a combination of power semiconductor elements as well as DC sources and capacitors. The first generation of inverter was consist of two switches per phase forming a simple circuit structure and could produce two voltage levels, but it was not optimized in terms of the quality of output voltage and number of semiconductor devises. In order to reach further optimization, multilevel inverters with various topologies were emerged where they are capable of producing multilevel step voltage suitable for high voltage and power applications (Choudhury, Pillay et Williamson, at al., 2014; Masisi et al., 2016). The conventional topologies suffered from a non-optimized circuit design as numerous dc source and dc capacitors as well as semiconductor devices are used. During to the last decade, many modifications on classical multilevel structures as well as new topologies have been presented in literatures (Chattopadhyay et Chakraborty, 2014; Babaei, Alilu et Laali, 2014; Samadaei, et al., 2016; Taghvaie, Adabi et Rezanejad, 2017; Taghvaie, Adabi et Rezanejad, 2018). The main purpose was to reduce the number of active and passive components and achieve more voltage levels in AC terminal in order to design an optimized inverter topology. Beside the aforementioned point, inverter switches like all kind of power electronics converters must be optimally controlled to achieve further efficiency. There are several switching methods that have been presented and deeply researched to generate proper firing pulses for inverter switches (Ahmed et al., 2016; Leon et al., 2016). Although multilevel inverter topologies improved the quality of output voltage and current in comparison to the conventional two-level inverter, switching techniques still play a significant role to provide an excellent performance. They have significant influence on the designing of an optimized inverter particularly in two aspects, the switching power losses and output voltage harmonic distortion.

Continuous development of semiconductor devices as well as optimization of inverter topology and their switching techniques have led to the widespread utilization of inverter in various power electronics applications. Depending on the range of output power, inverters

applications include battery chargers, AC/DC motor derives, FACTS and HVDC system, interconnecting renewable energy sources to the grid, uninterruptible power supplies (UPS), etc. However, the inverter requirements must be provided to be adjusted for each specific application. For instance, the inverter should be designed and controlled for motor derives to produce lower common mode voltage or they must be equipped to neutral wire if they are used in four wire applications such as UPS. For grid connected applications, the inverter must be switched to inject the current with high quality and unity power factor. Moreover, conventional electrical AC equipment such as transformer is being replaced by power inverters. This can remove the bulky transformers that can result in manufacturing expenses reduction.

Consideration of High Power Applications of Multilevel Inverters (Problem Statement)

The proper selection as well as number of semiconductor devices can enhance the inverters efficiency and lead to the optimized design in terms of power losses. However, the switching technique has also a significant impact on the minimization of power losses of the inverter. The switching technique can be optimally designed as the efficiency of the inverter improved remarkably. In this case, switching frequency of modulation technique must be taken into account in designing process of inverter control method which needs to be optimized. The switching frequency in PWM converters is defined based on the number of turn of ON and OFF state for semiconductor switches in one complete cycle which its period is *T*. Each turn of ON and OFF state is considered as one switched auction. So, the switching frequency (for each power switch) with respect to the provided definition can be achieved multiplying number of switched action and output voltage fundamental frequency (*f=1/T*). The switching frequency leads to the switching losses and can affect the inverter's efficiency. So, it is one of the crucial issues that must be assumed in the optimization of the switching technique. In (Gupta, et Ghosh, et. Joshi, 2008), the switching losses are formulated as following equation:

$$P_S = \frac{f_s.E.I_S\ \left(T_{on} + T_{off}\right)}{2\pi}\ \&\ P_D = 0.125\ \left(V_D.I_D T_D.f_s\right) \tag{0.1}$$

Where, I_S, E, T_{on} and T_{off} are the peak current, maximum voltage cross the switch, the rise and fall time of switch, respectively. Also, V_D, I_D and T_D are diode peak voltage, peak reverse current and reverse time, respectively. According to the switching losses formulation, in high power application where the voltage and current are in the range of *kV* and *kA*, the switching losses must be considered as one of the inverter's efficiency factors. In this case, the high ratio of switching frequency can significantly increase switching and conduction losses and decrease inverter's efficiency. Moreover, the other key factor in optimization of the modulation technique is its capability in dealing with harmonic distortion of the output voltage. The modulation technique can be optimally designed according to the multilevel inverter application as to fulfill the required harmonic distortion quality for the targeted applications. In spite of excellent performance of the conventional modulation techniques in controlling the harmonic distortion of the output voltage, they require high switching frequency to obtain such achievement. So, the trend is to use methods with low switching frequency in high power application. Among all switching techniques, Selective Harmonic Elimination (SHE) and Selective Harmonic Mitigation (SHM) have the lowest switching frequency arbitrary can be reduced. According to SHE or SHM, selected harmonic amplitudes can be also precisely controlled while switching frequency is less than 1 kHz. But, these two techniques can be still optimized a long with multilevel inverter topology to enhance the efficiency for targeted power electronics applications.

Research Objectives

Multilevel inverters topologies benefits of more semiconductor switches, dc sources and capacitors for generation of more voltage level in AC output terminal which can create a waveform similar to sine wave, so less harmonic distortion is produced. Despite this, the modulation techniques that are used to control inverter switches plays an important role to enhance the power quality in terms of voltage and current THD. They can enhance the inverters' efficiency though decreasing switching frequency providing voltage balancing across DC capacitor with standard ripple and lower capacitance. This research concentrates on the optimization of multilevel inverter topology and low switching frequency modulation

techniques to achieve further efficiency in the targeted applications. For optimization of the multilevel topologies, this research focuses on developing compact multilevel inverter structure like Packed U-Cell topology in order to reach further optimized converter in terms of number of components, number of output voltage and simplicity in capacitor voltage balancing. For optimization of the modulation technique, SHE and SHM as the successful low switching frequency modulation techniques which they can reduce power losses and control low harmonic orders precisely have been accordingly chosen to be optimized for the targeted applications. Since these two modulation techniques are based on strong mathematic theory, they can be fully investigated to be optimized in dealing with more harmonic orders in lower switching frequency ratio so as they operate with higher efficiency in the existing or new applications. Consequently, the research objectives are summarized as below in order to optimize both modulation techniques and multilevel inverter topologies for power electronics applications:

- Optimizing SHE and SHM techniques to control more harmonics with lower switching frequency.
- Utilizing SHE and SHM for three-phase four-wire inverters applications.
- Reducing common mode voltage through the optimized SHE or SHM technique.
- Developing Packed U-Cell topology to achieve a further optimized compact multilevel inverter.

Research Methodology

This research needs to be accomplished according to the following steps: Mathematical analysis, simulation and experimental implementation.

Step I: a literature review is required to be done on the modulation techniques specially SHE and SHM as well as multilevel voltage source inverters particularly compact inverters topologies to fully perceive their drawback in order to propose some solution for developing them. The study should consider issues such as inverter's application, capacitor self-voltage

balancing and developed procedure for multilevel inverters and modulation techniques This step can be completed by some simulation of previous model or propose some improvement in order to find a way to optimize inverter topologies and their switching methods.

Step II: the thorough mathematic analysis must be done to modify conventional or even recent compact inverter topology and modulation technique. In this case, SHE and SHM technique due to the fact that they are established based on mathematic theory (Fourier series decomposition of voltage waveform) can be completely investigated to be improved in terms of having same switching frequency while more harmonic amplitude are controlled. This investigation must be extended to the compact multilevel inverter topology to find new solution for some existed drawbacks and in addition to develop compact inverter structure.

Step III: The developed compact inverter topology and modulation technique which were finalized in the step II will be evaluated though simulation analysis in MATLAB/Simulink environment first. After completing simulation results successfully, the improved switching technique and inverter structure will be experimentally tested in the laboratory.

Thesis Contribution

The main contributions and novelties of this thesis research are as below:

Maximum Harmonic Mitigation and Elimination with Minimum Switching Frequency Ratio

The conventional SHE or SHM is established as number of harmonic that can be eliminated or mitigated are equivalent to the number of variables in the trigonometric equations which are switching angles and/or the index of input voltages. This means that if more harmonics are required to be controlled, more variables specifically more switching angles are required. More switching angles also increase the switching frequency and complexity of solving the trigonometric equations. In this work, a new switching angles constraint is introduced for both SHE and SHM technique of a low switching frequency voltage waveform which results

in self-elimination of all triplen harmonics while the non-triplen harmonic are controlled (eliminated or mitigated) through normal operation of the SHE or SHM technique. Therefore, maximum number of harmonic is controlled while minimum switching frequency is used.

SHE or SHM Application for 3phase 4wire Inverter

3phase 4wire inverter topologies are used to supply different load character including 3phase, single phase, balanced and unbalanced as well as linear and nonlinear loads. In previous works, high switching frequency modulation techniques have been employed to control 3phase 4wire inverters. Although they have an excellent performance in dealing with such mentioned load, their main drawback is the high switching frequency which causes high power losses. In this work, SHE has been designed for two configurations of 4wire inverter including 3leg 4wire inverter and 4leg 4wire inverter. It is shown that SHE on both 4wire configurations has suitable performance in dealing with both symmetrical and asymmetrical loads, but SHE is more compatible with 3leg 4wire inverter compared to 4leg 4wire inverter in terms of harmonic content of output voltage, design complexity and power losses.

SHE or SHM Application for Common Mode Voltage Control In 3phase Inverter

Common Mode Voltage (CMV) is a voltage in 3phase inverters which is measured between the neutral points of load and inverter. CMV is main reason for some adverse effects such as bearing failure, shaft voltage stress on electrical drives and EMI noises which indicates that CMV must be properly controlled in 3phase inverters. There are two general solutions for CMV control which are based on hardware and software modifications. In hardware solutions, the CMV is controlled by the help of an external circuit such as filter that makes some extra expenses. On the contrary, the software modifications like modulation techniques do not make extra cost and they are further economical solution for controlling CMV in 3phase inverters. In general, modulation techniques are designed to control CMV through proper switching vector selection as lower CMV it is generated. The high switching frequency modulation techniques have acceptable performance on controlling CMV, but they cause some disadvantages such as high power losses, imprecise control on lower harmonic

amplitude as well as capacitor voltage balancing problem. Unlike the previous methods, SHM and SHE are hybridized in this work to reduce CMV based on harmonic analysis in a low switching frequency while low order harmonics are precisely controlled and capacitors voltages are balanced with acceptable voltage ripple.

Design an Optimized Compact Multilevel Inverter Topology

The compact multilevel inverter structures are interesting topology for single phase configuration. Although the well-known compact topology; Packed U-Cell, has several advantages like reduced components counts, self-voltage balancing in its five-level configuration and so on, it has other disadvantages like difficulty in capacitor voltage balancing in the extension version. Also, Packed U-Cell can be further optimized like other multilevel inverters topologies. In previous works, different control strategies were mainly investigated on Packed U-Cell for various applications and a few works were done to modify this structure. In this work, Packed U-Cell has been deeply optimized and a new compact multilevel inverter structure has been emerged which is so-called as Packed E-Cell topology. Unlike Packed U-Cell where the auxiliary capacitors are extended in a vertical way, Packed E-Cell horizontally develops the auxiliary capacitors which results in further components counts and simplicity in capacitor voltage balancing.

Thesis Outline

This thesis is written in six chapters which include a survey on multilevel inverters topologies and modulation techniques and the proposed optimization techniques for SHE and SHM on single phase and 3phase inverters applications as well as the novel compact multilevel inverter.

CHAPTER 1 includes a thorough investigation on conventional multilevel inverters topologies, their advantages and disadvantages as well as conventional switching technique. This chapter is completed by a comprehensive survey on the SHE and SHM as the targeted low switching frequency modulation techniques. CHAPTER 2 introduces a new switching

angles constraint which optimizes SHM technique for single phase inverter application to have self-elimination of all triplen harmonics as well as mitigation of selected non-triplen harmonics in a fundamental switching frequency operation. A new switching angles condition is also presented in CHAPTER 3 to optimize SHE technique for single phase inverter application in order to eliminate all triplen harmonics and remove selected non-triplen harmonics in low switching frequency operation. CHAPTER 4 design SHE technique for both 4wire inverters configurations including 3leg 4wire inverter and 4leg 4wire inverter in order to deal with both symmetrical and asymmetrical loads under low switching frequency operation. It is shown through precise analysis that SHE is more compatible with 3leg 4wire inverter over 4leg 4wire inverter in terms of the design complexity, harmonic content and power losses. CHAPTER 5 also presents a hybrid SHM technique for CMV control in 3phase inverter which is done based on the harmonic analysis of the CMV in order to include it in the hybrid SHM cost function. CHAPTER 6 introduces a novel compact multilevel inverter based on the optimization of the previous generation; Packed U-Cell to reach further components counts and more voltage levels as well as simplicity in capacitor voltage balancing. Finally, CHAPTER 7 summarizes the thesis conclusions and presents some novel ideas for the future works.

CHAPTER 1

A SURVEY ON CONVENTIONAL MULTILEVEL VOLTAGE SOURCE INVERTERS TOPOLOGIES AND MODULATION TECHNIQUES

1.1 Introduction

During last decade, power electronics converters particularly DC-AC and AC-DC types of converters could find their way into the power industrial market and nowadays they are being employed in various applications such renewable energy system, electrical drives, electrical vehicles, HVDC, UPS and so on. Due to this high attention of industry to the power electronics converter, many researches have comprehensibly investigated different aspects of them, including topology, control and applications. Starting from two level structure, multilevel topologies where emerged to overcome the drawbacks and restrictions which prevents utilization of power converters in higher voltage and current applications. Various topologies of multilevel converters were introduced where each of them possess a prominent advantage that makes them further suitable for particular applications. While the primary multilevel topologies concentrates on using numerous semiconductor devices and main dc sources, later many endeavor were conducted to optimize the conventional multilevel structures or to design an optimized novel structure. The optimization was a trade-off among number of output voltage, number of active and passive devices and dc sources. So, the trend was to produce more voltage levels with reduced components counts while other key parameters are considered.

A long with development of the converter topologies, their switching techniques have been taken into consideration to be optimized as they have a remarkable impact on the performance of the multilevel converters. One of the key points in optimization of the designing the modulation technique is the matter of the switching frequency operation. In general, the switching techniques of the multilevel converters are categorized into the high and low switching frequency methods. Since multilevel converter includes considerable number of semiconductor devices, they can generate notable power losses particularly in

high power applications if the high switching frequency modulation techniques are employed. On the other hand, the low frequency modulation technique must be adaptably optimized according to the targeted application so as they can enhance the efficiency of the converter performance. In this chapter a survey on the conventional multilevel inverters topologies and modulation techniques particularly on low switching frequency switching methods is done to have better understanding of their advantages and disadvantages.

1.2 Multilevel Voltage Source Inverters Topologies

During the last century, researchers focused on amplification of inverter output power. Some tried to increase the current level and some investigated on possibility of voltage level increment in order to achieve the aim. In 1981, Nabae *et al.* the output power by introducing new PWM inverter topology (Nabae, Takahashi et Akagi, 1981). The new inverter called NPC could generate three voltage levels. Presenting NPC topology led to emerging multilevel inverter topologies. Afterwards, different multilevel inverter topologies were emerged and employed in various applications. Some multilevel inverter structures have been surveyed in the following.

1.2.1 Diode Clamped Inverter

As it was mentioned, the three-level NPC inverter was the first attempt to introduce the multilevel inverter structure. The idea of designing NPC inverter is based on the modification of conventional two-level inverter with two switches in each leg as shown in Figure 1.1. In two-level inverter, each capacitor voltage is dropped on one of semiconductor power switches when it is OFF. Then, the switch must be selected in such way to stand with high voltage ratio if it is utilized in high power applications. On the contrary, the NPC topology consists of four power switches in each inverter's leg. Therefore, each capacitor voltage is divided between two switches. Moreover, a diode loop clamped two middle switches has been used in NPC structure to guarantee the proper voltage division between two OFF switches. Due to this fact, NPC inverter is more suitable for high power applications compared to conventional two-level inverter with similar semiconductor switch.

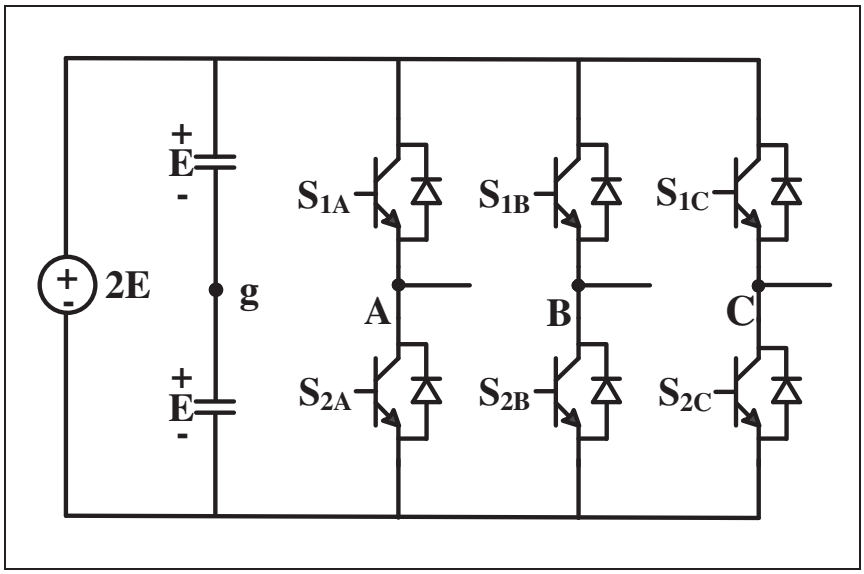


Figure 1.1 Conventional two-level inverter configuration

Table 1.1 Switching States of Three-Level Diode Clamped (NPC) Inverter

Switching States	**S_{1A}**	**S_{2A}**	**S_{3A}**	**S_{4A}**	**V_{out}**
1	1	1	0	0	+E
2	0	1	1	0	0
3	0	0	1	1	-E

Table 1.2 Switching States of Five-level Diode Clamped Inverter

Switching States	**S_{1A}**	**S_{2A}**	**S_{3A}**	**S_{4A}**	**S_{5A}**	**S_{6A}**	**S_{7A}**	**S_{8A}**	**V_{out}**
1	1	1	1	1	0	0	0	0	+E
2	0	1	1	1	1	0	0	0	+E/2
3	0	0	1	1	1	1	0	0	0
4	0	0	0	1	1	1	1	0	-E/2
5	0	0	0	0	1	1	1	1	-E

Figure 1.2-a depicts single-phase three-level NPC inverter topology. According to Figure 1.2-a, NPC inverter includes four switches and two diodes for each leg that can produce three voltage levels in output.

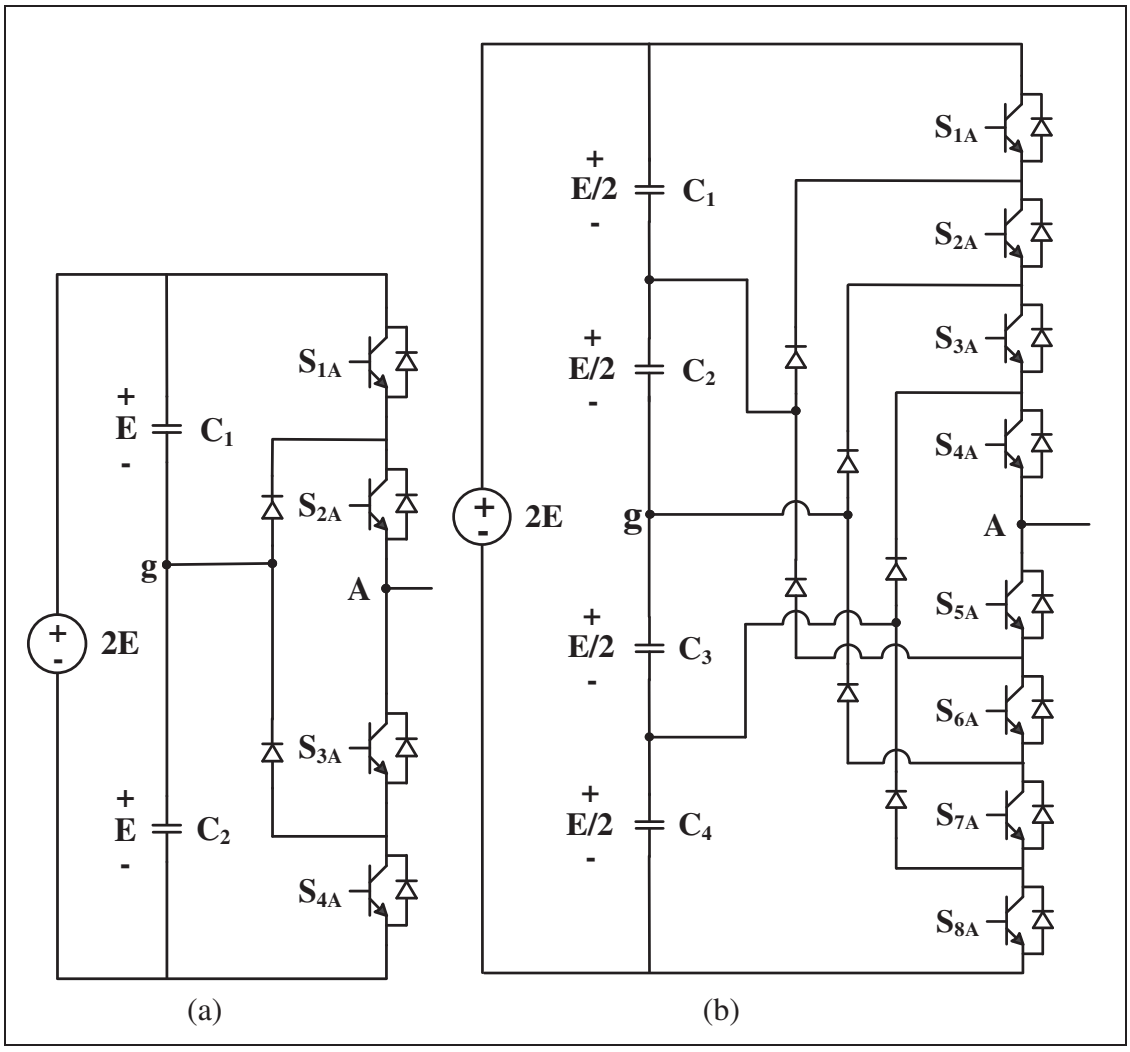


Figure 1.2 Single-phase three-level and five-level diode clamped (NPC) inverter configuration, (a) three-level NPC inverter, (b) five-level NPC inverter

In order to generate these three voltage levels (+E, 0, -E), there are three switching states. Considering the fact that (S_{1A}, S_{3A}) and (S_{2A}, S_{4A}) are complimentary switches, if two upper switches (S_{1A}, S_{2A}) are ON state, the output voltage will be $+E$ and if two lower switches (S_{3A}, S_{4A}) are ON state the voltage $-E$ will be appeared in output terminal. The output voltage zero will be produced when two middle switches (S_{2A}, S_{3A}) turn on. It must be mentioned that the fourth switching state in NPC will result in DC-link short circuit. The three switching state possibility have been listed in Table 1.1.

Three-level NPC inverter was developed and generalized as Diode Clamped multilevel inverter to have arbitrary multilevel voltage in output terminal using diode loops. Indeed, the three-level diode clamped inverter is known as NPC inverter. The single-phase five-level diode clamped inverter topology has been illustrated in Figure 1.2-b. According to Figure 1.2-b, five-level diode clamped includes eight power switches and six diodes as well as four DC capacitors in DC-link. Also, the corresponding switching state for five-level diode clamped inverter is shown in Table 1.2. In general, $(K\text{-}1)$ DC-link capacitors, $(K\text{-}1)(K\text{-}2)$ clamping diodes and $2(k\text{-}1)$ semiconductor power switches are required to produce K voltage level with diode clamped inverter topology. Furthermore, the diode clamped multilevel inverter advantages and disadvantages are briefly listed in below:

The advantages are summarized as: (I) less DC capacitors and sources are used in diode clamped compared to other multilevel structures. (II) the utilization of DC-link voltage is improved in diode clamped topology. (III) it is not required to employ isolated transformer in diode clamped inverter. The disadvantages are summarized as: (I) the complexity of DC-Link capacitor voltage balancing. (II) the problem of clamping diode selection in higher voltage range. (III) The limitation of its application to medium voltage one.

1.2.2 Flying Capacitor Inverter

Another multilevel inverter structure is Flying Capacitor inverter topology. The idea of designing flying capacitor inverter is to use capacitive loops instead of clamping diode to produce different voltage levels. Figure 1.3-a demonstrates three-level flying capacitor inverter. According to Figure 1.3-a, if the capacitor voltage (C_A) is equal to E (which is equivalent to each DC-link capacitor voltage), there would be four switching states possibility for three-level flying capacitor inverter. In this case, the output level $+E$ is caused by turning on two upper switches and $-E$ is produced by ON state of two lower switches. Also, there are two possible states for zero voltage level, turning on the switches (S_{1A}, S_{3A}) or the switches (S_{2A}, S_{4A}). These four switching states are listed in Table 1.3. As can be seen from Table 1.3, switches (S_{1A}, S_{4A}) and (S_{2A}, S_{3A}) are complementary. The five-level flying

capacitor inverter structure has been also shown in Figure 1.3-b that has eight power switches and six capacitors for capacitive loop as well as four capacitors used DC-link. Table 1.4 contains the corresponding switching states for five-level flying capacitor inverter. In order to produce *K* voltage level with flying capacitor inverter, *2*(*K-1*) power switches, (*K-1*)(*K-2)/2* balancing capacitors as well as (*K-1*) capacitors in DC-link are needed. Moreover, the advantages and disadvantages of flying capacitor inverter can be shortly expressed as follows:

The advantages are summarized as: (I) flying capacitor inverter topology requires only one DC-link. (II) it provides more switching states possibility compared to other multilevel inverter structures which can increase the chance of voltage balancing for DC-link capacitor. The disadvantages are summarized as: (I) more capacitor is used in flying capacitor structure which increases the total manufacturing cost. (II) The problem of voltage balancing for capacitor installed in capacitive loop.

Table 1.3 Switching States of Three-Level Flying Capacitor Inverter

Switching States	S_{1A}	S_{2A}	S_{3A}	S_{4A}	V_{out}
1	1	1	0	0	+E
2	1	0	1	0	0
3	0	1	0	1	0
4	0	0	1	1	-E

Table 1.4 Switching States of Five-Level Flying Capacitor Inverter

Switching States	S_{1A}	S_{2A}	S_{3A}	S_{4A}	S_{5A}	S_{6A}	S_{7A}	S_{8A}	V_{out}
1	1	1	1	1	0	0	0	0	+E
2	1	1	1	0	1	0	0	0	+E/2
3	1	1	0	0	1	1	0	0	0
4	1	0	0	0	1	1	1	0	-E/2
5	0	0	0	0	1	1	1	1	-E

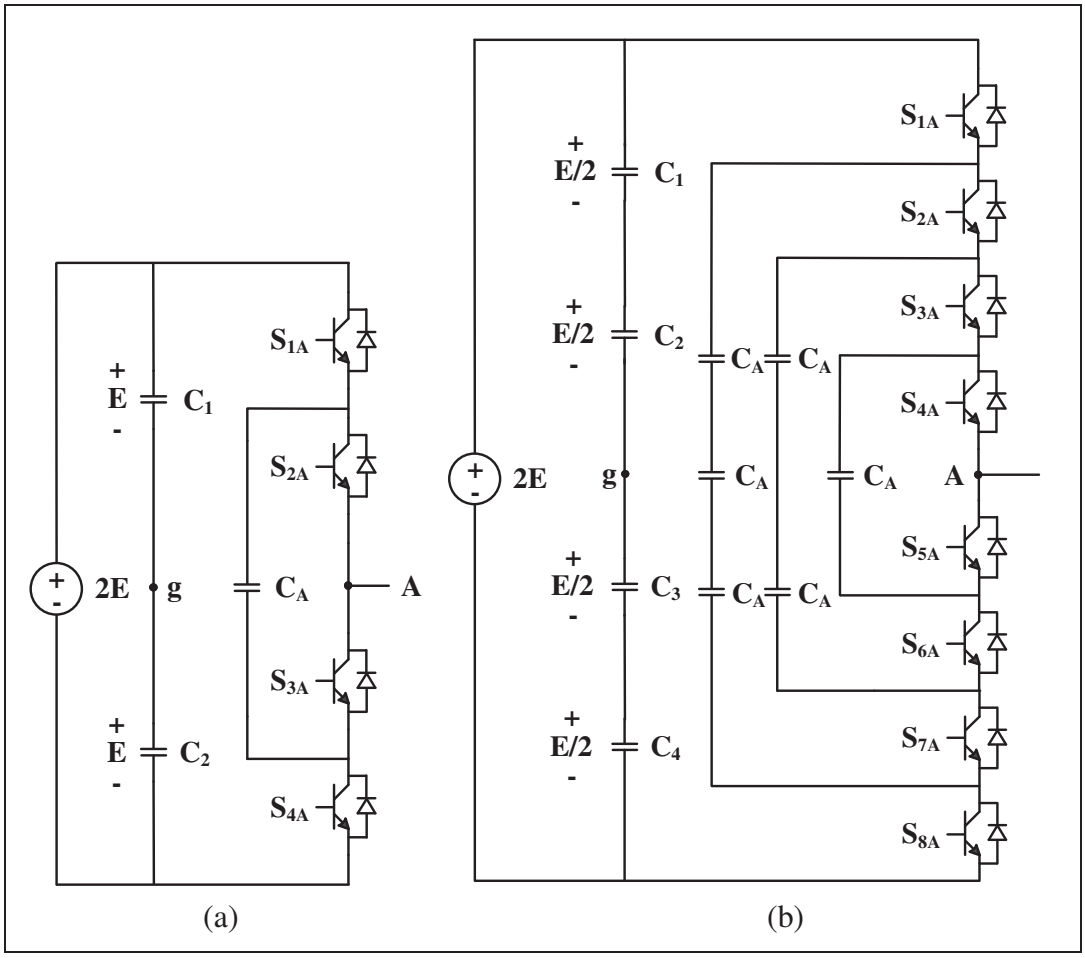


Figure 1.3 Single-phase three-level and five-level flying capacitor inverter configuration, (a) three-level flying capacitor inverter, (b) five-level flying capacitor inverter

1.2.3 Cascaded H-Bridge Inverter

Cascaded H-Bridge multilevel inverter does not require any clamping diode or capacitive loop in its structure. Figure 1.4 shows Cascaded H-Bridge (CHB) multilevel inverter topology built through cascading series of individual full-bridge inverter to receive arbitrary step voltage in the AC output terminal. Individual full-bridge inverters are connected to isolated DC source that can produce three voltage levels including $+V_{dc}$, 0, $-V_{dc}$. Considering complementary switches (S_1, S_2) and (S_3, S_4), there are four switching states possibility for full-bridge inverter in order to have the three voltage levels in output. In this case, $+V_{dc}$, 0, $-V_{dc}$ levels are produced by turning on switches (S_1, S_4), (S_1, S_3) or (S_2, S_4) and (S_2, S_3);

respectively. Then, the output voltage in CHB inverter is the sum of the voltages of each individual full bridge inverters. The CHB multilevel inverter with *K* DC sources can generate at least *2K+1* voltage levels in phase voltage. However, the line voltage can have *2K+3* or *2K+5* levels considering equal or unequal voltage for DC sources; respectively. Due to the fact that each DC sources is connected to one full-bridge inverter that contains four power switches, 4K power switches are required for CHB multilevel inverter in total. The advantages and disadvantages of CHB multilevel inverter are summarized in following items:

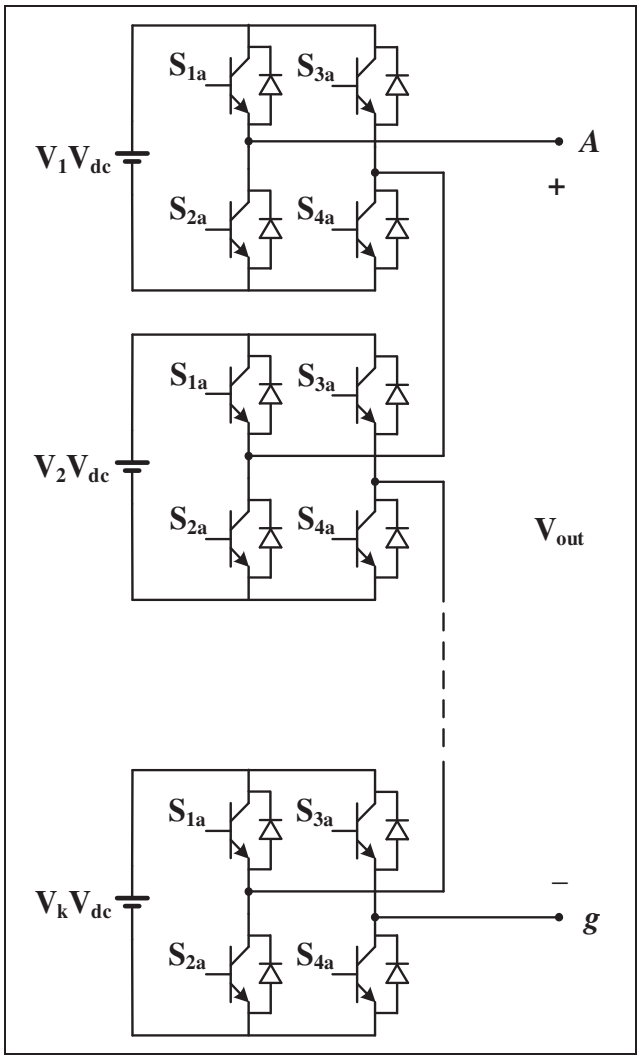


Figure 1.4 Configuration of single-phase Cascaded H-Bridge multilevel inverter

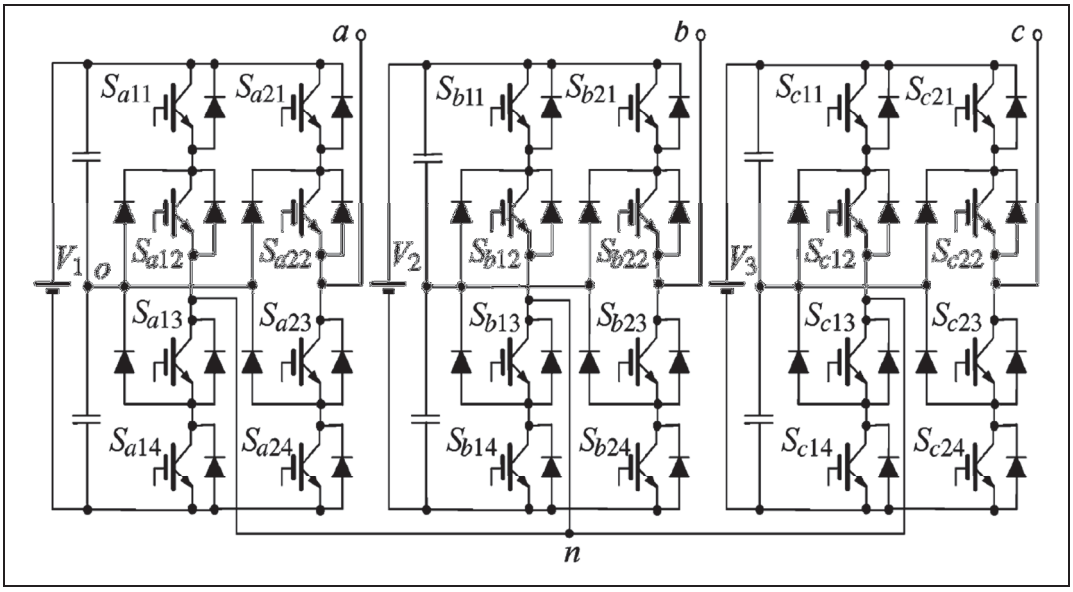


Figure 1.5 Five-level cascaded NPC inverter

The advantages of CHB topology are as: (I) there is no to use clamping diode or capacitive loop in CHB that minimizes number of components. (II) CHB has modular structure which decreases manufacturing and maintaining cost. The disadvantage of CHB is also as: (I) CHB requires more separated DC sources that confines its applications and increases the cost. The cascaded configuration was also spread to other multilevel inverter topology in order to make them modular structure and receive more voltage levels (Wu, Lau, et Chung, 1999). Figure 1.5 shows cascaded NPC inverter that can produce five-level voltage.

1.2.4 Packed U-Cell Inverter

Multilevel Packed U-Cell (PUC) inverter shown in Figure 1.6 includes single DC-source and one auxiliary capacitor as well as six power switches. PUC was firstly introduces in (Al-Haddad, Ounejjar, et Gregoire, 2011) as a modification on flying capacitor topology. By providing desire voltage balancing for the auxiliary capacitor through applying a control method, PUC inverter could generate seven voltage levels in output AC terminal. To simplify the complexity of controlling PUC inverter, PUC5 inverter was presented in (Vahedi, Labbé et Al-Haddad, 2016) with ability of having self-voltage balancing of auxiliary capacitor and without any changes in conventional PUC topology. However, PUC5 could only produce

five voltage levels. In this case, the capacitor voltage is half of DC source voltage. Table 1.5 shows the switching states of PUC5 for generating five-level voltage waveform as well as the capacitor state (charging, discharging and no effect) considering $|V_{dc}|=2E$ and $|V_c|$=E.

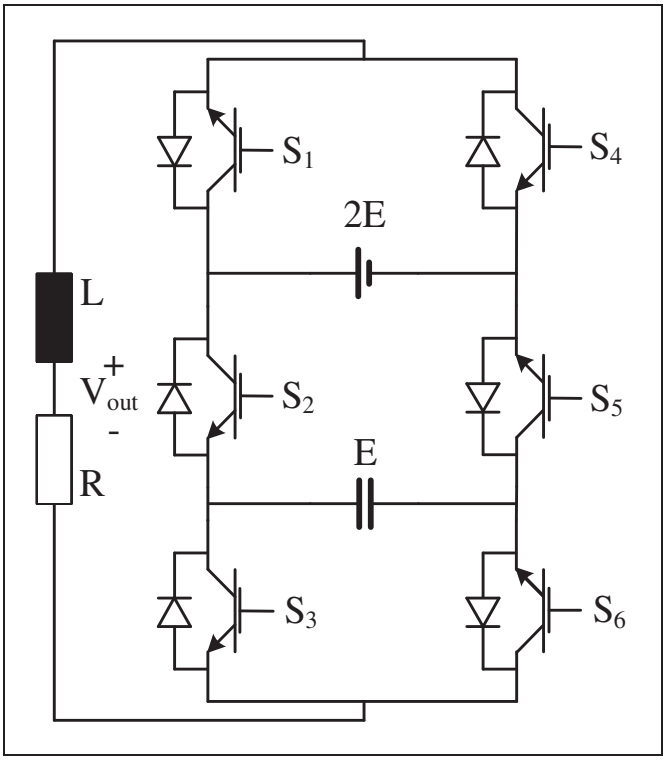


Figure 1.6 Configuration of Packed U-Cell inverter

Table 1.5 Switching States of Five-Level Packed U-Cell Inverter

Switching State	**S_1**	**S_2**	**S_3**	**S_4**	**S_5**	**S_6**	**V_{out}**	**Effect on Capacitor**
1	1	0	1	0	1	0	+2E	No effect
2	1	0	0	0	1	1	+E	Charging
3	0	0	1	1	1	0	+E	Discharging
4	0	0	0	1	1	1	0	No effect
5	1	1	1	0	0	0	0	No effect
6	1	1	0	0	0	1	-E	Discharging
7	0	1	1	1	0	0	-E	Charging
8	0	1	0	1	0	1	-2E	No effect

1.3 Switching Modulation Techniques for Multilevel Voltage Source Inverters

Depending on multilevel inverter applications, the inverter should be switched to control output voltage or current. The voltage control is mainly used in applications such as Distributed Generations (DGs) (Ko et al., 2006), active series filter (Buticchi et al., 2016) and uninterruptible power supplies (Pichan et Rastegar, 2017). Also, the current control is more common in applications like rectifiers (Lai et al., 2009) and active parallel filer (Buso, Malesani et Mattavelli, 1998). Besides, the switching techniques have important role in multilevel inverter efficiency in terms of increasing or decreasing power losses, they can be also classified from switching frequency point of view. In this case, multilevel inverter modulation techniques are featured by high and low switching frequency methods.

1.3.1 High Switching Frequency Modulation Techniques

Among the high switching frequency techniques, two voltage control methods; SPWM, SVM and one current control; hysteresis are mostly used in power electronics inverters. The prominent feature of these switching methods is that the harmonic distortion is decreased as the switching frequency increases; even though the control on low order harmonic will not be accurate anymore. This is the reason they have been classified into high switching frequency group. It must be also mentioned that the high switching frequency will result in following problems: (I) increased switching and conduction power losses in semiconductor devices. (II) Electromagnetic Compatibility (EMC) in devices worked in higher switching frequency must be further considered which will increase the expenses.

1.3.2 Sinusoidal Pulse Width Modulation (SPWM) Technique

This switching technique that was firstly introduced in (Schonung et al., 1964) is based on the direct comparison of desired reference waveform (sinusoid) and carrier waveform (saw tooth). Figure 1.7 illustrates the concept of SPWM technique. According to SPWM technique, if the sine wave is greater than the saw tooth waveform, the firing pulses will have 1 state otherwise if the sine wave is less than the saw tooth, the pulses will be in 0 positions.

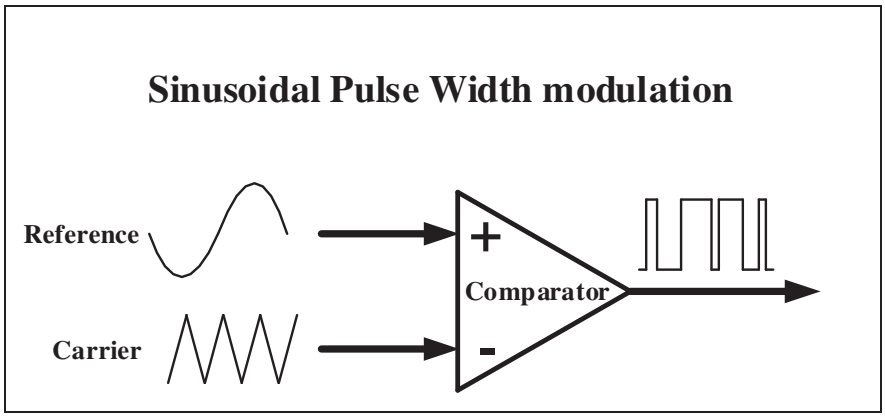


Figure 1.7 General diagram of SPWM method

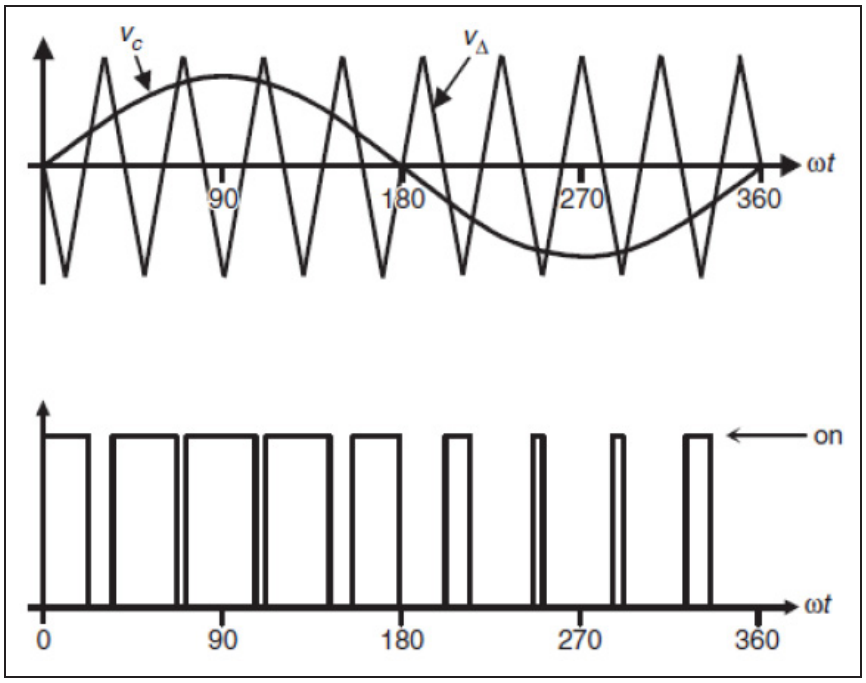


Figure 1.8 SPWM techniques for two-level inverter

Figure 1.8 demonstrates SPWM function for conventional two-level inverter. The frequency of saw tooth (f_s) and sinusoidal (f_1) waveforms is equal to switching frequency and fundamental frequency; respectively. f_s is also the frequency of devices that they are switched and f_1 is the output voltage frequency.

Considering these two frequencies, the frequency modulation index (m_f) is defined as $m_f=f_s/f_1$. m_f is the ratio that represents the frequency that harmonic are appeared. As well, the amplitude modulation index (m_a) is a ratio between the amplitude of sinusoidal (V_1) and saw tooth (V_s) waveforms as $m_a=V_1/V_s$. It shows what proportion of DC input voltage can be receivable in output AC terminal of inverter.

The SPWM technique has been used for different multilevel inverter and its advantages over other modulation techniques is the simplicity in implementation due to low volume of calculations of switching pulses. On the other hand, SPWM requires high switching frequency to lead to acceptable results which will increase the power losses and decrease inverter efficiency (Kim et Sul, 2004).

1.3.3 Space Vector Modulation (SVM) Technique

On the contrary to the SPWM that was based on the comparison, switching intervals in SVM technique are obtained using space vectors achieved from a three-phase system (Zhao et al., 2010). According to SVM principle, the three-phase voltages (V_a, V_b, V_c) are transferred to two voltages (V_d, V_q). In this case, the vector space is calculated as:

$$v = V_d + iV_q \tag{1.1}$$

Considering a balanced three-phase system with voltage amplitude and frequency V and ω, the vector space will be:

$$v = \frac{3}{2}\left(V\cos(\omega t) + iV\sin(\omega t)\right) = \frac{3}{2} Ve^{j\omega t} \tag{1.2}$$

The obtained relation in Eq. (1.2) is a circular trajectory with radius $1.5V$ as shown in Figure 1.9. Therefore, controlling of the inverter output voltage can be assumed as a vector that its amplitude is equal to V and rotates with the speed of ω. For three-phase two-level inverter, there are eight switching states as shown in Table 1.6 that each state is equivalent to one vector including V_0 to V_7.

Table 1.6 Switching States for Three-Phase Two-Level Inverter

State	S_{1A}	S_{1B}	S_{1C}	V_{Ag}	V_{Bg}	V_{Cg}	V_{An}	V_{Bn}	V_{Cn}	V_{AB}	V_{BC}	V_{AC}
V_0	0	0	0	-E	-E	-E	0	0	0	0	0	0
V_1	0	0	1	-E	-E	E	-2E/3	-2E/3	4E/3	0	-2E	-2E
V_2	0	1	0	-E	E	-E	-2E/3	4E/3	-2E/3	-2E	2E	0
V_3	0	1	1	-E	E	E	-4E/3	2E/3	2E/3	-2E	0	-2E
V_4	1	0	0	E	-E	-E	4E/3	-2E/3	-2E/3	2E	0	2E
V_5	1	0	1	E	-E	E	2E/3	-4E/3	2E/3	2E	-2E	0
V_6	1	1	0	E	E	-E	2E/3	2E/3	-4E/3	0	2E	2E
V_7	1	1	1	E	E	E	0	0	0	0	0	0

As instance, the vector V_0 is equivalent to switching state $S_{1A}S_{1B}S_{1C}=110$. Figure 1.10 illustrates the vector position of V_0 to V_7. As it is shown in Figure 1.10, the non-zero vectors (V_1 to V_6) make a regular hexagonal and two zero vectors (V_0 and V_7) are located at the center. The reference vector (V_{ref}) is arbitrarily considered in one these six sections.

In this case, V_{ref} can be calculated by averaging the vectors that encompassed it. As an example, it is supposed that the V_{ref} is located between vectors V_1 and V_2 as shown in Figure 1.10. Considering T as the period of output voltage, inverter is switched with respect to vectors V_1, V_2 and V_0 (or V_7) for duration of t_1, t_2 and t_0; respectively.

Also, t_0 is the corresponding time to zero vectors (V_0 and V_7) and is presumed common among all other six non-zero vectors in reference voltage calculation. t_1, t_2 and t_0 are obtained from Eq. (1.3).

$$\begin{cases} \frac{t_1}{T} = m_a \ \sin(\frac{\pi}{3} - \alpha) \\ \frac{t_2}{T} = m_a \ \sin(\alpha) \\ \frac{t_0}{T} = 1 - \frac{t_1}{T} - \frac{t_2}{T} \end{cases} \tag{1.3}$$

Up to now, the SVM technique has been applied for different inverter topologies (Leon et al., 2010; Bendre et al., 2004). It has the advantages such as reduction of harmonic distortion and increasing utilization of DC-link voltage in comparison to the SPWM. Although the switching frequency is decreased in SVM method, it is still in range of kHz. Moreover, SVM is further complicated and needs more memory capacity for implementation.

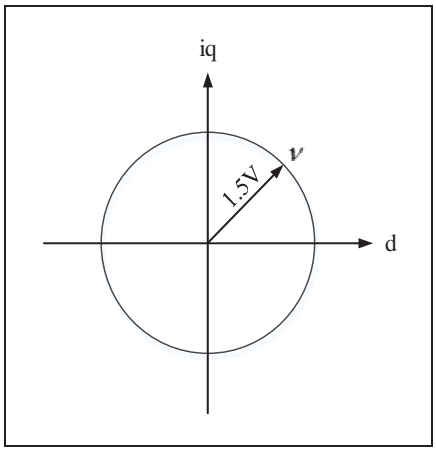
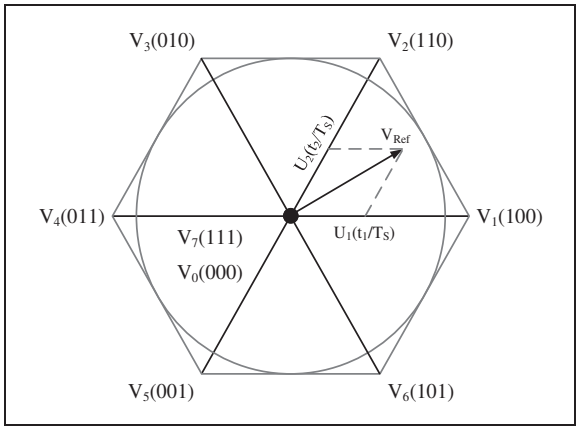


Figure 1.9 Locus of vector *V*



Figurer 1.10 Space vector of three-phase two-level inverter

1.3.4 Hysteresis Current Control

Among current control methods that have a good ability to track the reference current, hysteresis current control due to its simplicity, proper stability and its fast response was investigated by many researchers (Kapat et al., 2017). According to hysteresis current

control, the error signal obtained from comparison between the reference and actual current is used for switching pulses. In this case, the reference current is considered as a band that the actual current fluctuates between upper and lower band edges.

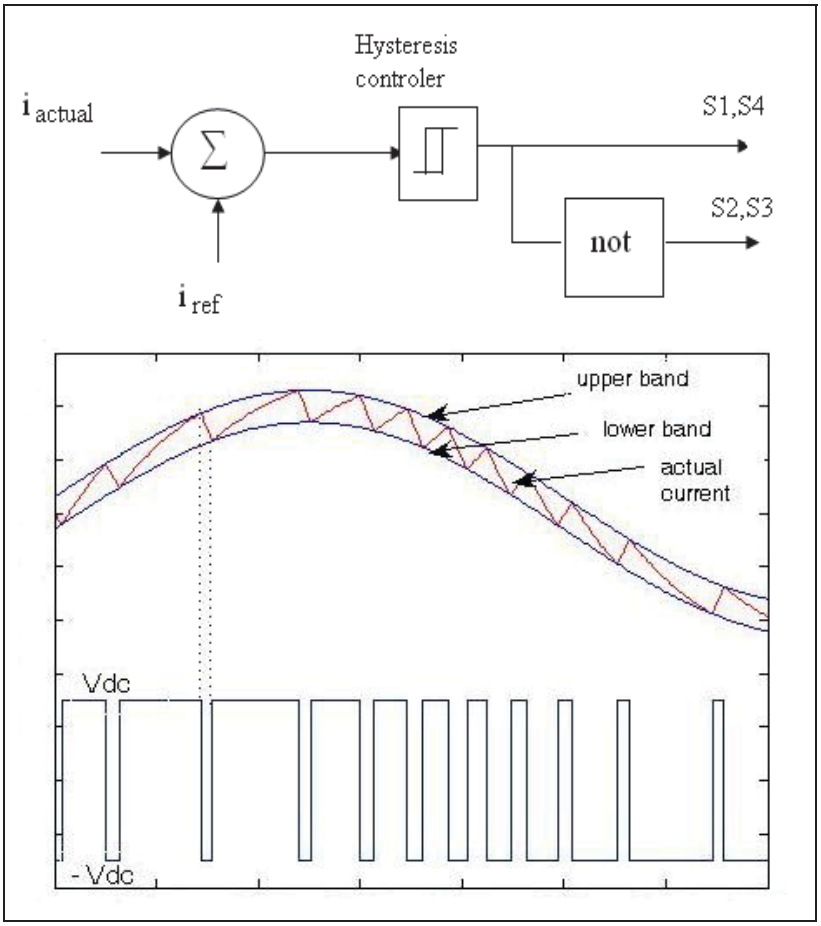


Figure 1.11 Hysteresis current controls for conventional two-level inverter

Figure 1.11 shows the hysteresis current control and the corresponding switching pulses for conventional two-level inverter. Besides the mention positive features for this switching technique, it has drawbacks such as high and variable switching frequency. The switching frequency in hysteresis current control is mainly depends on the parameters of output load (George et Mishra, 2009). In addition to the problems that cause by the high switching frequency, the variable switching frequency also complicates designing reactive (*LC*) output filter (Fereidouni, Masoum et Smedley, 2016). Another current control switching method that is similar to hysteresis current control is Delta modulation technique. In this approach, the

sign of error signal is detected by a comparator and then the switching intervals are commended to switches (Mertens, 1994). Delta technique injects sub harmonic in output voltage that needs to operate in higher switching frequency to overcome this problem. On the contrary to this disadvantage, it is simple for implementation on the hardware.

1.3.5 Low Switching Frequency Modulation Techniques

As it was explained, the high switching frequency modulation techniques increase the power losses particularly in multilevel inverter that contains more semiconductor devices. So, it is desired to decrease the switching frequency in order to enhance the efficiency of power inverters. To this end, many endeavors have been carried out to reduce the switching frequency of traditional methods like SPWM, SVM and so on. In (Ceballos et al., 2008) a modified carrier-based PWM was proposed to reduce switching frequency with discontinuous PWM and decrease switching losses stopping commutation during maximum value of output current. As well, an improved hysteresis current control with minimized switching frequency was presented in (Lohia et al., 2008) though monitoring the polarity of reference current. Although the switching frequency could be reduced by some modification, it is still as high as 3 to 5 kHz. On the other hand, there are two modulation techniques based on the voltage control, Selective Harmonic Elimination (SHE) and Selective Harmonic Mitigation (SHM) that can operate in a very low switching frequency with accurate control on low harmonic orders.

1.3.6 SHE-PWM Technique

Unlike switching techniques such as SPWM, switching angles in SHE technique are accurately calculated through solving some offline equations to eliminate undesired harmonic amplitudes and produce a desire fundamental voltage in the output waveform. To prevent SHE equations complexity, number of angles are assumed low which has the advantage of low switching frequency and power losses. The concept of harmonic elimination was established in 1960s to cancel low harmonic orders considering additional switching angles in voltage square-waveform and using Fourier series analysis (Dahidah, Konstantinou,et

Agelidis, 2015; Yang et al., 2016; Perez-Basante et al., 2017; Aleenejad, Mahmoudi et Ahmadi, 2016).

Later, the harmonic elimination was generalized to preprogrammed staircase voltage waveforms with number of switching angles to have desired first harmonic amplitude and some eliminated harmonic orders (Dahidah, Konstantinou,et Agelidis, 2015). Uninterrupted researches on the harmonic elimination idea; SHE-PWM was finally emerged for different voltage waveforms (Farokhnia et al., 2012; Song et al., 2016; Gao et al., 2016). The voltage waveform normally are assumed quarter-wave symmetry to remove even harmonic orders inherently, however, SHE also was applied on half-wave symmetry in some cases (Yang et al., 2015; Yang et al., 2017). The SHE equations must be solved for different modulation indices which leads to different switching angles are obtained. Since, the SHE equations are nonlinear it is possible to find several value for switching angles for one modulation index. Hereupon, the main challenge after introducing SHE technique concerned solving trigonometric equations.

Various approaches were used to find a general and trustworthy solution which optimization methods such GA, PSO, and so on are finally proposed in recent years to solve SHE equations (Kavousi et al., 2012). The optimization techniques not only can guarantee the harmonic elimination, but also is able to find all possible trajectories for switching angles. The obtained switching angles regarding to best trajectory that can cover the complete range of modulation index are saved in lookup tables to be used for pulse generating of inverter's switches control. As it was mentioned, SHE principle is based on Fourier series decomposition, so in the next section the general formula of Fourier series and its coefficients for an arbitrary waveform has been explained and extended for quarter-wave symmetry. Since this modulation technique can be used for all voltage waveforms, the harmonic amplitudes for unipolar, bipolar and multilevel voltage waveforms are obtained afterwards. Due to the advantages of quarter-wave symmetry over half-wave one, all the voltage waveforms in this research have been assumed as quarter-wave symmetry.

1.3.7 Fourier Series Expression

In general, Fourier series of a periodic waveform with periodicity *2L* is formulated as below (Patel et Hoft, 1973; Patel et Hoft, 1974):

$$U(t) = \frac{1}{2} a_0 + \sum_{n=1}^{\infty} (a_n \cos(n\omega t) + b_n \sin(n\omega t)) \tag{1.4}$$

Where a_n and b_n are Fourier series coefficients obtained using following equations:

$$a_n = \frac{1}{L} \int_{-L}^{L} V(\omega t).\ \cos(n\omega t) d(\omega t) \tag{1.5}$$

And

$$b_n = \frac{1}{L} \int_{-L}^{L} V(\omega t).\ \sin(n\omega t) d(\omega t) \tag{1.6}$$

In equations (1.5) and (1.6), *V(ωt)* is the periodic waveform supposed to be written as the sum of sine and cosine functions. Since the inverter output voltage waveforms are assumed odd quarter wave symmetry to have the advantage of self-elimination of even harmonics, the Fourier series formulation presented in Eq. (1.4) will be changed into:

$$U(t) = \sum_{n=1}^{\infty} (b_{2n-1} \sin((2n-1)\omega t)) \tag{1.7}$$

And the odd coefficient b_{2n-1} will be attained as:

$$b_n = \frac{4}{L} \int_{0}^{L/2} V(\omega t).\ \sin(n\omega t) d\,\omega t \qquad \forall n = 1,\ 3,\ 5,\ \ldots \tag{1.8}$$

Also, it must be mentioned that the Fourier series coefficients are equivalent to out voltage harmonic amplitudes.

1.3.8 Fourier Decomposition for Different Voltage Waveforms

Due to the fact that the harmonic amplitude formulation changes according to the voltage waveform, they need to be obtained for different type of staircase voltage.

1.3.9 Bipolar Voltage Waveform

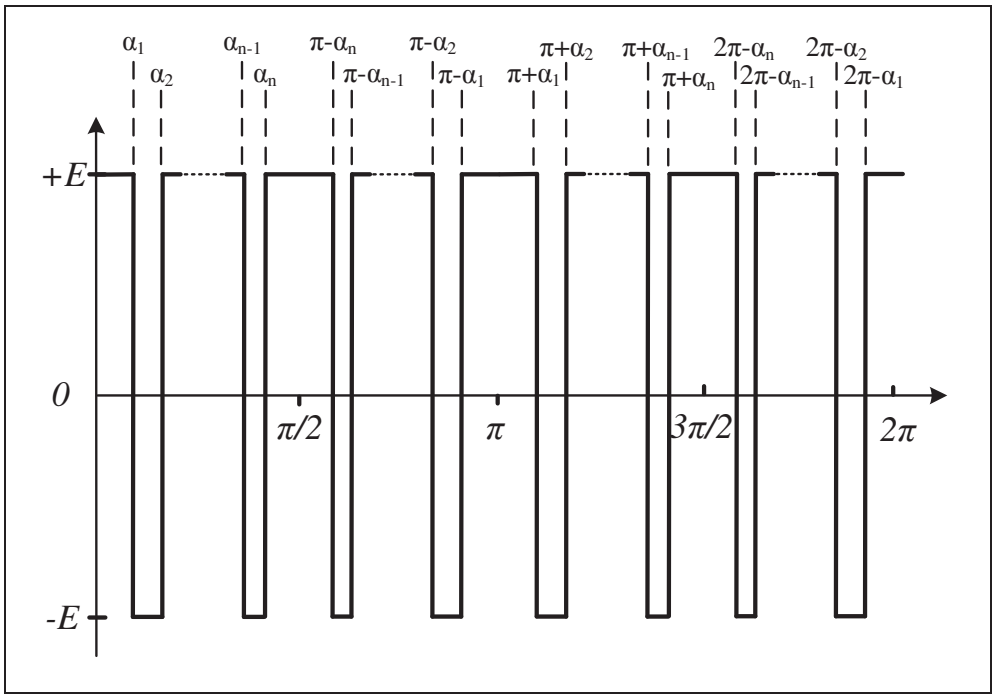


Figure 1.12 Bipolar voltage waveform

Bipolar voltage waveform contains only two $\pm E$ levels as shown in Figure 1.12. So, the harmonic amplitudes are achieved (Agelidis et al., 2006):

$$H_n = \frac{4E}{n\pi}\left(\frac{1}{2} + \sum_{i=1}^{k} (-1)^i \cos(n\alpha_i)\right) \tag{1.9}$$

1.3.10 Unipolar Voltage Waveform

The unipolar voltage waveform is generated using three levels $\pm E$ and 0 in which in the first half cycle the pulses are between +E and 0 and in the second one they are between –E and 0

as depicted in Figure 1.13. The harmonic amplitudes are also obtained as formulated in Eq. (1.10) (Chiasson et al., 2004).

$$H_n = \frac{4E}{n\pi} \sum_{i=1}^{n} (-1)^{i+1} \cos(n\alpha_i) \tag{1.10}$$

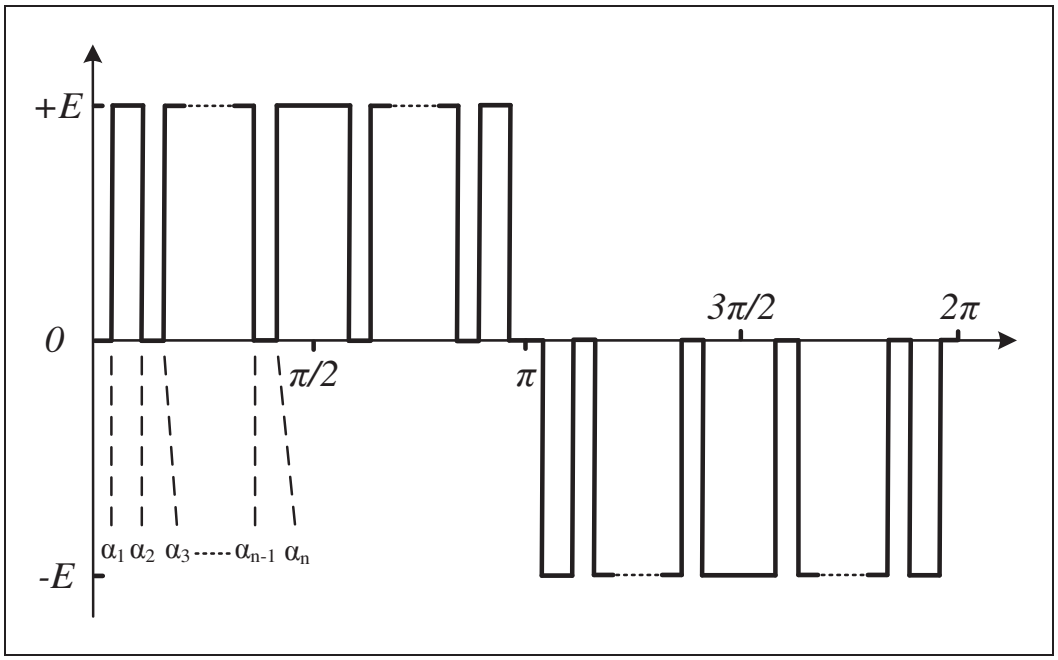


Figure 1.13 Unipolar voltage waveform

1.3.11 Multilevel Voltage Waveform

Like other switching methods, SHE was extended to multilevel voltage waveform (Fei, Ruan et Wu, 2009). There are two general types of multilevel staircase voltage waveforms, high switching frequency voltage waveform and low switching one. While, in low switching frequency voltage waveform, number of pulses depends on number of voltage levels, switching angles can be considered without any limitation in high switching one. These two general types of multilevel voltage waveform have been demonstrated in Figure 1.14.

The harmonic amplitudes in low switching frequency case are written as Eq. (1.11) and for the high switching frequency multilevel voltage waveform, harmonic amplitudes will be generally obtained as Eq. (1.12).

$$H_n = \frac{4}{n\pi} \sum_{i=1}^{k} \mathrm{V}_i \cos(n\alpha_i) \tag{1.11}$$

$$H_n = \frac{4}{n\pi} \sum_{i=1}^{m_k} \left[\begin{array}{l} \mathrm{V}_1 \left(\pm \cos(n\alpha_1) \pm \mathrm{L} \pm \cos(n\alpha_{m_1}) \right) + \mathrm{L} \\ + \mathrm{V}_2 \left(\pm \cos(n\alpha_{m_{k-1}}) \pm \mathrm{L} \pm \cos(n\alpha_{m_k}) \right) \end{array} \right] \tag{1.12}$$

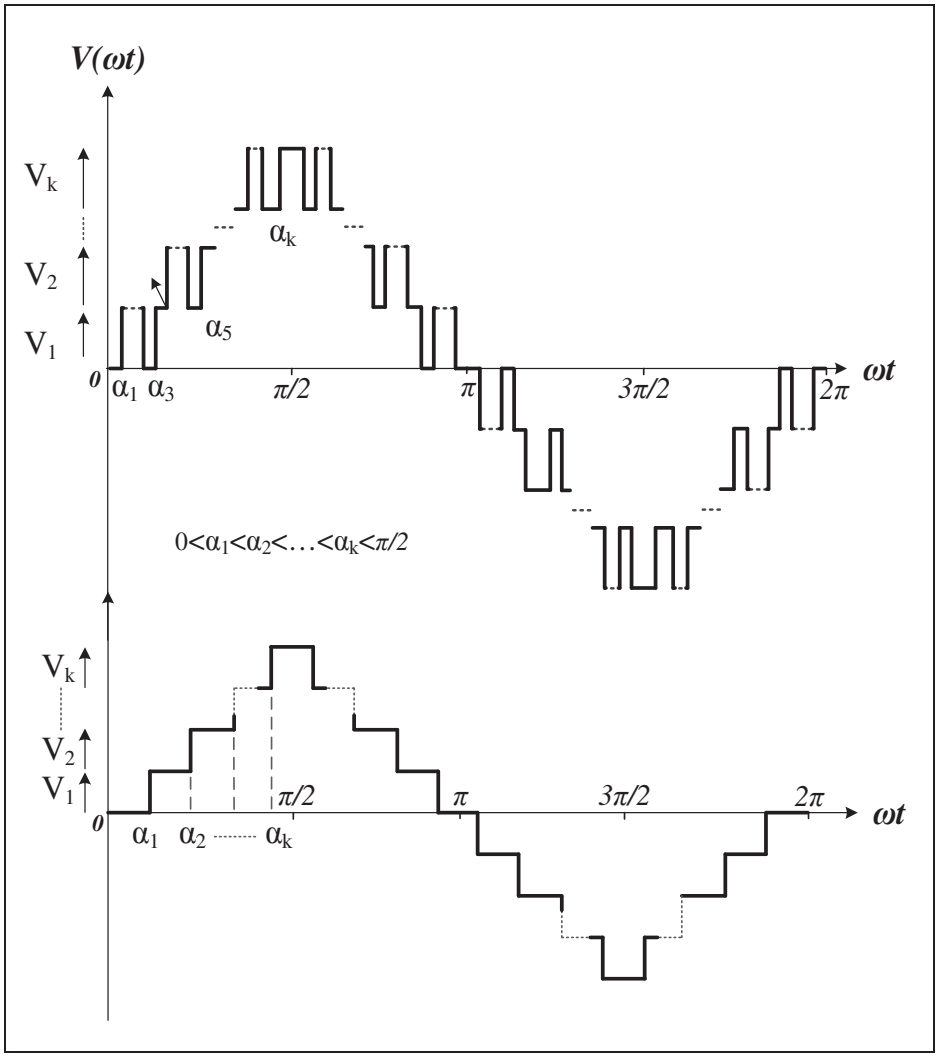


Figure 1.14 Multilevel voltage waveform

1.3.12 SHE Equations for 1/3-Phase Inverters

As it was mentioned in the introduction, switching angles are calculated in an offline computation solving some transcendental equations. To this end, SHE equations are provided through setting equivalent first harmonic amplitude to the desired fundamental voltage that must be generated in output as well as considering undesired harmonic amplitudes equal to zero.

The undesired harmonic orders are determined with respect to single or three-phase inverter topology. While in the single phase inverter both triplen and non-triplen orders are assumed in SHE equations, in the three-phase inverter only non-triplen orders are involved in equations due to cancellation of triplen harmonics in phase to phase voltage (Dahidah, Konstantinou,et Agelidis, 2015). Therefore, SHE equations for both single and three-phase inverters according to aforementioned descriptions will be provided as follows:

$$\begin{aligned} 3phase &: \begin{cases} H_1 = m_a \\ H_n = 0 \end{cases} \quad n = 5,\ 7,\ 11,\ \ldots \\ 1phase &: \begin{cases} H_1 = m_a \\ H_n = 0 \end{cases} \quad n = 3,\ 5,\ 7,\ \ldots \end{aligned} \tag{1.13}$$

Moreover, there is a correlation between number of pulses and harmonic orders which must be eliminated.

Considering *k* angles in the first quarter cycle, there would be *k-1* harmonics that can be removed from the output voltage harmonic spectrum. On the other hands, the SHE equations include trigonometric terms and they need specific methods to be solved.

1.3.13 SHE Equations Solving Strategies

Since SHE technique has been emerged, the main concern was to solve the trigonometric nonlinear equations (Ahmed, Hendawi et Taha, 2016). The most repetitive and efficient approaches that have been used to solve SHE equations in many research are listed as:

1.3.14 Repetition Methods:

Newton-Raphson is a well-known numerical analysis procedure for obtaining successively better approximations to the function's roots. So, that was one the first attempts to solve the SHE equations (Sun et Grotstollen, 1992), however, appropriates initial guesses are required to reach more accurate values. Indeed, the success of this method is greatly depends on initial guess.

Moreover, this method is not suitable when the notable number of angles is assumed in SHE equations (Sun et Grotstollen, 1992).

1.3.15 Walsh Functions:

The SHE transcendental nonlinear equations can be changed into linear equations using Walsh functions which will leads to simplify switching angle calculations.

However, the obtained angles would have optimum values which mean the exact elimination of selected harmonics is not guaranteed (Swift et Kamberis, 1993).

1.3.16 Resultant Theory:

This method was proposed in order to find all possible trajectories for switching angles through converting nonlinear equations into linear polynomial ones.

To this end, the equivalent polynomial equations are considered for trigonometric SHE equations and then switching angles are calculated applying resultant theory.

$$X_i = \cos(\alpha_i) \qquad i = 1,\ 2,\ 3,\ ...,\ k \tag{1.14}$$

In (Chiasson et al., 2004), the resultant theory has been applied into bipolar and unipolar voltage waveform to eliminate some low harmonic orders. The SHE equations for bipolar voltage with three angles in the first quarter cycle are:

$$\begin{cases} H_1 = \frac{4E}{\pi}\ (\frac{1}{2} - \cos(\alpha_1) + \cos(\alpha_2) - \cos(\alpha_3)) = m_a \\ H_5 = \frac{4E}{5\pi}\ (\frac{1}{2} - \cos(5\alpha_1) + \cos(5\alpha_2) - \cos(5\alpha_3)) = 0 \\ H_7 = \frac{4E}{7\pi}\ (\frac{1}{2} - \cos(7\alpha_1) + \cos(7\alpha_2) - \cos(7\alpha_3)) = 0 \end{cases} \tag{1.15}$$

$$\begin{cases} X_1 = \cos(\alpha_1) \\ X_2 = \cos(\alpha_2) \\ X_3 = \cos(\alpha_3) \end{cases} \tag{1.16}$$

Following trigonometric equations

$$\begin{cases} \cos(5\alpha_1) = 5\ \cos(\alpha_1) - 20\ \cos^3(\alpha_1) + 16\ \cos^5(\alpha_1) \\ \cos(7\alpha_1) = -7\ \cos(\alpha_1) + 56\ \cos^3(\alpha_1) - 112\ \cos^5(\alpha_1) \\ +64\ \cos^7(\alpha_1) \end{cases} \tag{1.17}$$

Therefore, polynomial SHE equations will be:

$$\begin{cases} H_1 = \frac{4E}{\pi}\ (\frac{1}{2} - X_1 + X_2 - X_3) = m_a \\ H_5 = \frac{4E}{5\pi}\ (\frac{1}{2} + \sum_{i=1}^{3}\ (-1)^i(5X_i - 20X_i^3 + 16X_i^5)) = 0 \\ H_7 = \frac{4E}{7\pi}\ (\frac{1}{2} + \sum_{i=1}^{3}\ (-1)^i(-7X_i + 56X_i^3 - 112X_i^5 + 64X_i^7)) = 0 \end{cases} \tag{1.18}$$

where X_1, X_2 & X_3 must be found to calculate regarding switching angles. Moreover, the equations below must be considered while Eq. (1.17) is being solved.

$$0 < X_3 < X_2 < X_1 < 1 \tag{1.19}$$

1.3.17 Polynomial Homotopy Method:

Homotopy is an algorithm based approach proposed to calculate SHE angles (Kato, 1999). Despite this, the developed model of Homotopy could act like algebraic methods which do not require presuming any condition for primary values then more possible angles trajectory can be available. However, the complexity problem of SHE equations when more angles are involved and optimum values for switching angles that may defeat the SHE purpose are the polynomial Homotopy method drawbacks. As well, this technique cannot find results for some modulation index less than *0.487* which has led to ignore it as a permanent solution for solving SHE equations.

1.3.18 Optimization Techniques:

In this method, SHE equations are defined as an objective function to be able to assume as an optimization problem. Since this technique is compatible with all kind of SHE equations without considering number of switching angles, it has become prevailing method in recent years (Taghizadeh et Hagh, 2010). It also should be mentioned that the obtained angles have optimum values; however, the harmonic elimination is thoroughly happening.

$$OF_{SHE} = \left(H_1 - m_a \right)^2 + \sum_{n=5,\,7,\,11,\,\ldots}^{\infty} \left(H_n \right)^2 \tag{1.20}$$

1.3.19 SHM-PWM Technique

Although SHE is a suitable switching technique in order to eliminate some harmonic orders, the critical challenge of SHE is to remain uncontrolled non-eliminated harmonics which have higher orders. Indeed, low order amplitude elimination leads to intensify the first non-eliminated harmonic amplitude. So, LC filters are required to overcome this SHE drawback through suppressing remained uncontrolled harmonic amplitudes.

In other words, even SHE can eliminate some harmonic amplitude, the inverter output voltage and current must be according to power quality standards to be able to use in real applications. Otherwise, the bulky and costly LC filter is needed to satisfy this condition which will result in increasing total system price. Although the number of angles can be increased instead of using bulky LC filters to eliminate more harmonic amplitudes, SHE equations complexity as well as switching frequency and power losses is increased and consequently further costly semiconductor power switches are required. Hence, in (Franquelo et al., 2007) another modulation technique based on SHE was introduced to mitigate harmonic amplitudes instead of eliminating them. In SHM technique, all harmonic orders up to 49^{th} as well as THD are considered and switching angles are calculated to reduce amplitudes below standard levels and minimize voltage THD.

In (Franquelo et al., 2007) a notable number of pulses were considered to reach that purpose. Although all non-triplen harmonic orders below 49^{th} were reduced properly, having a switching frequency over 1 kHz was necessary. As a solution, in (Napoles et al., 2010; Moeini, Iman-Eini et Bakhshizadeh, 2014) an Objective Function (*OF*) was defined for SHM equations to control higher harmonic orders in addition to mitigate lower ones with less angles.

In recent years, many researches have been also done to improve the conventional SHM switching method. In (Moeini, Zhao et Wang, 2016), the current reference instead of voltage was used to calculated switching angles in SHM technique for rectifier application, so it could control more higher harmonic orders compared to the conventional SHM-PWM in same switching frequency. In (Najjar et al., 2016) an optimal SHM was proposed to be used back-to-back converter applications such as active rectifier. According to optimal SHM, OF was defined based on strictest power quality requirement.

Beside the mentioned attempts that were proposed to modify conventional SHM technique, a hybrid SHM and SHE technique was proposed in (Sharifzadeh et al., 2015) to be used in four-leg four-wire inverter as a standalone application. According to proposed method, SHM

and SHE are combined to have both techniques' advantages simultaneously. It was also shown that the hybrid technique can result in phase voltage waveform symmetry which can guarantee the capacitor voltage balancing. As well, the capacitor voltage was formulized with respect to the switching angles that led to calculate the minimum required capacitance to have voltage ripple across capacitor less than 5%. Although the presented method was used for DC bus capacitors, it can be modified to be used to capacitance calculation in single DC sources topology, those have auxiliary capacitors in their structure like recently introduced Packed U cell (PUC) inverter.

Therefore, SHM technique is used to calculate switching angles as an optimization issue which will allow considering other factors such as THD. However, regardless of number of pulses all harmonic amplitudes below 49th which are important from standard point of view will be involved in SHM equations.

Table 1.7 shows the maximum acceptable value for both triplen and non-triplen harmonic amplitude with respect to the standard EN50160 and CIGRE WG 36-05 requirements (Voltage characteristics of electricity supplied by public distribution systems, 2001; Harmonics, characteristic parameters, methods of study, estimates of existing values in the network, 1981). Hence, the general formulation of SHM technique is as below:

$$\begin{cases} H_1 = m_a \\ H_n \leq m_a L_n \\ \forall\, n = 5,\ 7,\ 11,\ ...,\ 49 \\ 0 < \alpha_1 < \alpha_2 < ... < \alpha_K < \dfrac{\pi}{2} \end{cases} \tag{1.21}$$

And the *OF* is defined as:

$$OF(\alpha_1,\ ...,\ \alpha_K) = C_1(H_1 - \mathrm{m}_a)^2 + \left(\sum_{n=5,7,...49} C_n(H_n)^2 \right) + C_{THD}THD \tag{1.22}$$

Table 1.7 EN50160 and CIGRE WG 36-05 Requirements for Non-Triplen and Triplen Harmonics Amplitude

Non-Triplen Orders		**Triplen Orders**	
Harmonic order (n)	Maximum Allowable Level (L_n)	Harmonic order (n)	Maximum Allowable Level (L_n)
5	6%	3	5%
7	5%	9	1.5%
11	3.5%	15	0.5%
13	3%	21	0.5%
17	2%	>21	0.2%
19	1.5%		
23	1.5%		
25	1.5%		
>25	0.2+32.5/n		

Even though *OF* could enhance SHM flexibility, the proper mitigation of harmonics depends on *OF* coefficients (C_n). Therefore, more harmonics have a chance to fulfill grid code limit at the same switching frequency of SHE. However, the mitigation priority is for lower harmonic orders.

Actually, by selecting appropriate coefficient for each equation, *OF* provides a situation in which low harmonic orders have more chance to be mitigated compared to the higher orders. However, higher harmonic orders can also be controlled. To this end, the weighted penalty parameter coefficients C_n are modeled with respect to harmonic orders as following equation:

$$C_1 > C_5 > \ldots > C_{49} \tag{1.23}$$

Also, the coefficient of voltage THD (C_{THD}) is assumed as a different value. C_{THD} can be selected to increase the chance of mitigating higher harmonic orders. Moreover, it must be mentioned that the difference between *OF* in SHE and SHM is that in SHE number of

equations are equal to number of variables, but in SHM number of equations are exceeded than number of variables which means the equations need to be considered with different weight.

1.3.20 SHM versus SHE Technique

In order to show the superiority of SHM against SHE, the harmonic amplitudes as well as voltage THD in both techniques have been compared in (Sharifzadeh et al., 2015). Number of switching angles of SHE and SHM is same and selected 8. Considering 8 switching angles, 7 harmonic amplitudes including 5^{th} to 23^{rd} have higher chance to be eliminated or mitigated accurately.

However, SHM must control the higher harmonic orders better than SHE in same switching frequency. In this case, Figure 1.15-a illustrates the worst case of harmonic amplitudes in both SHE and SHM techniques. As can be seen, non-triplen harmonic orders 5^{th} to 23^{rd} are acceptably suppressed.

On the other hand, the higher harmonic amplitudes are less in SHM technique compared to SHE. Moreover, the depicted voltage THD in Figure 1.15-b proves that SHM technique due to considering THD formula in *OF* has suitable control in comparison to SHE.

Although SHM could improve SHE in terms of more harmonic order control, more switching angles are required in order to guarantee further harmonic amplitude suppression. To be precise, SHM can bring the possibility to have extra control on higher harmonic orders though considering special weight for equations in *OF*, however, there is no guarantee that more harmonic order can be controlled.

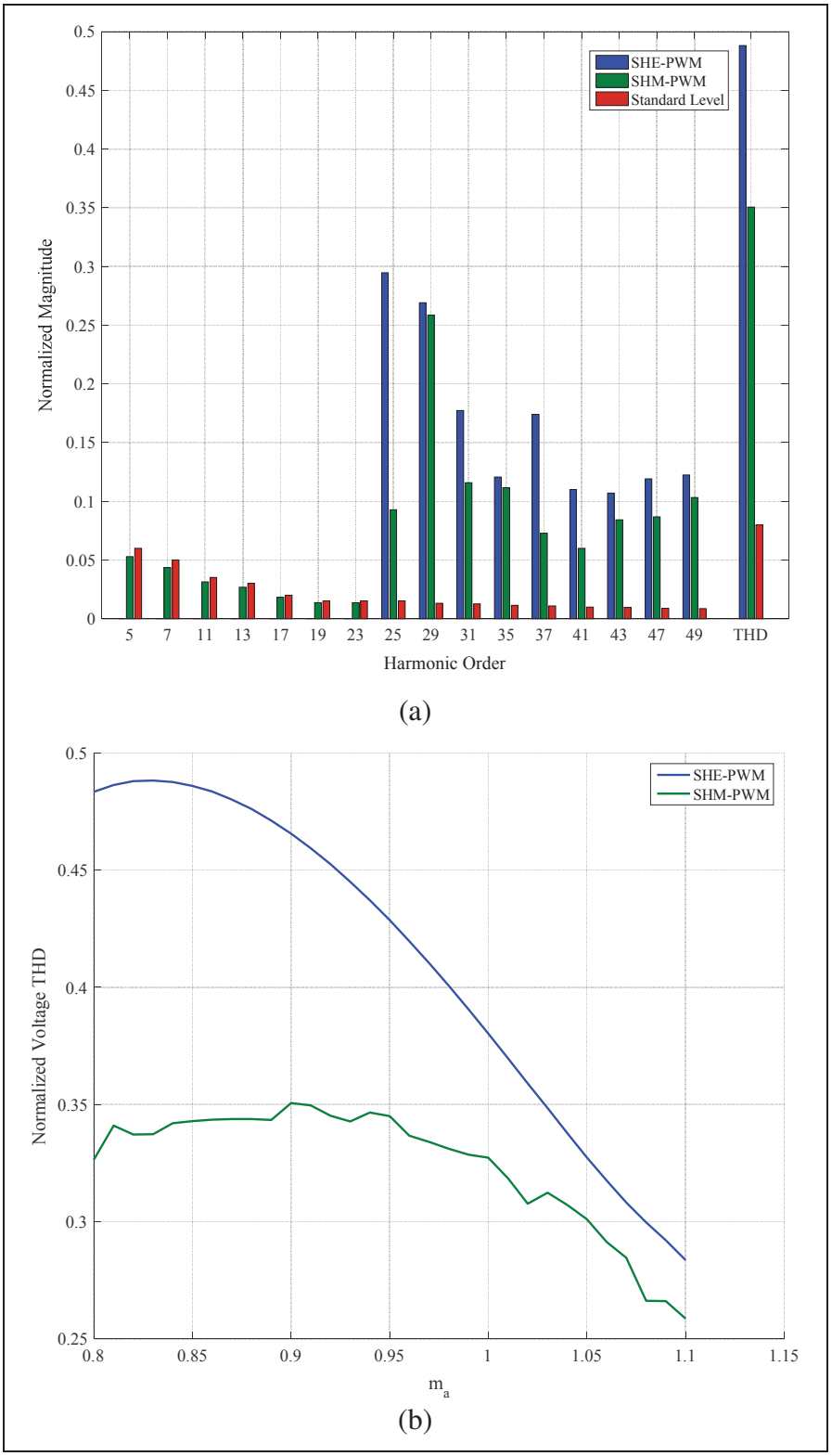


Figure 1.15 Harmonic amplitude and voltage THD comparison between SHM and SHE (a) worst case scenario for harmonic amplitudes (b) voltage THD

1.4 State of the Art and Originality of the Research

The compact multilevel inverters are suitable topologies for single phase application because of their appealing features particularly their single dc source structural. The three-level H-Bridge and five-level Packed U-Cell are two well-known and interesting compact multilevel inverter topologies. Although five-level Packed U-Cell is an optimized development of three-level H-Bridge because it has well-reduced components counts and has special feature in capacitor voltage balancing. Unfortunately, Packed U-Cell has not been deeply investigated in order to introduce the next generation for the compact multilevel inverter. The main difficulty in developing Packed U-Cell is the difficulty in capacitor voltage balancing while the compact multilevel inverters are extended to generate more than five-level voltage waveform. According to the proposed topology which is so-called as Packed E-Cell, the capacitors are extended in horizontal way unlike vertical extension in Packed-U-Cell, in order to reach in further optimized topology in terms of reduced components counts and simplicity in capacitor voltage balancing.

Moreover, regarding the optimization of the modulation technique it must mention that the high switching frequency methods have no robust control on low harmonic orders which may result in increasing the amplitude for some low orders and violating the standard levels for harmonics. On the other hand, the accurate calculations of switching angles in SHE and SHM techniques have led to precise elimination or mitigation of low harmonic orders. As well, the switching frequency ratio is restricted in these two switching techniques because of low number of switching angles. Considering the mentioned features for SHM and SHE, they are competitive switching techniques in standalone high power applications of voltage source inverters.

Since, multilevel inverters are on the state of the art in DC to AC converters; these switching techniques can be assumed in multilevel voltage waveforms to meet the grid code requirements for harmonic amplitudes and voltage THD with respect to the standard levels for harmonics. Due to the flexibility of SHM compared to the SHE, it would be able to

control more harmonic amplitudes at the same switching frequency of the SHE. Moreover, SHM will be tracked to control maximum number of harmonic order with minimum number of angles. This will be done through modification of solving strategy and considering different factors for SHM objective function in order to find the all possible trajectories for switching angles to determine which trajectory has led to control more harmonic amplitudes. In addition to the improvement of SHM and SHE techniques, they can be adjusted for employing in different power electronics applications like:

Three-phase Four-Wire Inverters

In order to supply asymmetrical loads such as single-phase, nonlinear loads, voltage source inverters must be designed with neutral wire. To this end, there are two four-wire configuration for inverters; three-leg four-wire and four-leg four-wire. The neutral wire in three-leg four-wire inverter is connecting the neutral point of loads to middle point of DC-link. Also, the fourth-wire in four-leg four-wire is provided through the fourth leg. Each configuration has its own advantages. The three-leg four-wire inverter has less power switches and consequently power losses, but it requires larger DC capacitors. On the contrary, four-leg needs smaller capacitors for DC-link; however, it has higher power losses. In (Zhang et Yan, 2009) SHE-PWM was proposed for two-level four-leg four-wire inverter and extended to three-level NPC in (Sharifzadeh et al., 2016a). According to proposed technique, the phase legs are switched to eliminate non-triplen harmonics and triplen harmonics are cancelled with the fourth leg. Also, the hybrid SHM-SHE PWM and PAM techniques were presented to improve the harmonic content of phase voltages in four-leg NPC inverter. In this case, the SHM is applied on phase legs to mitigated non-triplen harmonics and SHE is used for fourth-leg to eliminate triplen ones.

Common Mode Voltage Control

The common mode voltage (CMV) is a voltage between neutral point of loads and middle point of DC-link. Since CMV can cause some several problems such as bearing damage, electromagnetic interface winding failure, etc, it needs to be control particularly in electrical

motor applications. In (Zhao et al., 2012) a hybrid SHE-PWM method was reported to reduce CMV. According to proposed technique, the conventional SHE in high frequency and modified SHE in low frequency and smooth transition between them. Also, the SHM-PAM technique was employed to reduce CMV through controlling the input DC voltages.

CHAPTER 2

SELECTIVE HARMONIC MITIGATION BASED SELF-ELIMINATION of TRIPLEN HARMONICS FOR SINGLE-PHASE FIVE-LEVEL INVERTERS

Mohammad Sharifzadeh [a], Hani Vahedi [b],
Ramon Portillo [c], Leopoldo Garcia Franquelo [d], Kamal Al-Haddad [e]

[a, b, e] Department of Electrical Engineering, École de Technologie Supérieure,
1100 Notre-Dame West, Montreal, Quebec, Canada, H3C 1K3
[c, d] Department of Electrical Engineering, University of Seville,
Calle San Fernando, 4, 41004 Sevilla, Spain

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Abstract

In this chapter a modified Selective Harmonic Mitigation-Pulse Amplitude Modulation (SHM-PAM) is presented to be capable of canceling all triplen harmonic orders and suitable for single-phase application of five-level type of voltage source inverters. To this end, a new constraint is established for the two switching angles (α_1, α_2) to derive the new formula for the harmonics' amplitude which results in self-elimination of all triplen harmonics (e.g. 3rd, 9th, 15th, …). The fifth and seventh harmonic orders are mitigated through normal operation of the proposed SHM-PAM technique. It is also shown that the proposed technique is extendable to other multilevel voltage waveforms and a flowchart of self-elimination of all triplen harmonics has been presented. Mathematical analysis supported by experimental investigations show the desired performance of the proposed SHM-PAM algorithm on a 2-cell single-phase Cascaded H-Bridge (CHB) inverter as a typical five-level configuration in dealing with linear and nonlinear loads. Then, it is demonstrated that the maximum number of harmonic orders would be controlled with the minimum number of available angles in a low switching frequency voltage waveform.

2.1 Introduction

Minimization of low order harmonic amplitudes at low switching frequency to satisfy grid code requirements could find a way through Selective Harmonic Mitigation Pulse Width Modulation (SHM-PWM) technique (Pontt, Rodríguez, et Huerta, 2004; Moeini, Zhao et Wang, 2016; Steczek, Chudzik, et Szelag; 2017; Buccella et al., 2014). SHM has been introduced based on the optimized Selective Harmonic Elimination (SHE) (Dahidah, Konstantinou, et Agelidis, 2015) method as an improvement to control more harmonic orders. SHM-PWM has proven to involve all harmonic orders below 49^{th}, those are taken into power quality evaluation, in order to overcome SHE disadvantage of leaving non-eliminated orders uncontrolled (Franquelo et al., 2007; Napoles et al., 2010; Nápoles Luengoet al., 2013). Hence, an Objective Function (*OF*) has been defined to turn SHM equations into an optimization technique. The *OF* is adjusted to allocate appropriate coefficients to SHM equations in order to mitigate low order harmonics amplitudes and control non-eliminated ones. However, number of mitigated amplitudes is equal to the number of angles in the equations.

The first attempt to augment amplitude mitigation without increasing number of pulses was Pulse Width and Amplitude Modulation (PWAM) technique (Ghoreishy et al., 2012a; Ghoreishy et al., 2012b). According to the SHM-PWAM principle, both DC voltage magnitudes of inverter and switching angles are considered as variable in traditional SHM equations (Sharifzadeh et al., 2014). Thus, there is possibility of mitigating more harmonic orders proportional to the number of DC sources added into equations as variable. Afterwards, SHM-PWAM was simplified into PAM technique in (Sharifzadeh et al., 2016b) through generalizing a formulation that the fundamental output voltage component can be directly controlled via DC input voltage. Several modifications have been also conducted to improve SHM-PAM in order to deal with more harmonic orders with same number of variables. In (Najjar et al., 2016), SHM-PAM technique was applied on strictest power quality requirements and proposed to be used in back-to-back converter applications as active front end rectifiers.

Another critical challenge is in single-phase inverters where both triplen and non-triplen harmonics must be considered in the equations due to the fact that triplen harmonics are existing in single-phase systems inherently. Then, there would be more undesired low harmonic orders in single-phase equations compared to three-phase one which should be controlled. Furthermore, triplen harmonic orders have severer standard amplitude limitation than the non-triplen ones, which weakens SHM flexibility. The standard limitations for triplen orders higher than 15^{th} are below %0.2. In fact, SHM should have the ability of eliminating triplen harmonic orders in a single-phase inverter. In (Moeini, Iman-Eini, et Bakhshizadeh, 2014) it was shown that extra pulses are required to keep SHM flexibility in single-phase inverter in order to increase the chance of controlling triplen amplitudes below the determined limitations in addition to mitigate the non-triplen ones. Despite this, the number of properly minimized triplen orders was limited. Also, an optimization technique has been proposed in (Konstantinou, Agelidis, et Pou, 2014) for single-phase inverters to empower angles solving method to search for a solution to control maximum number of harmonic amplitudes with same switching frequency. However, the proposed method could only minimize two more triplen harmonic amplitudes for some specific modulation index. As well, there is no analytical investigation to support the reason for extra triplen harmonics minimization.

In this work, an improved SHM-PAM technique is presented to suppress maximum number of harmonics amplitudes in single-phase inverters using minimum possible number of angles. In fact, it is shown that all triplen harmonics would be eliminated through a proposed condition for two switching angles without adding extra pulses. For this purpose, a relation for two angles in five-level low switching voltage waveform with equal steps voltage has been found to eliminate all triplen harmonic amplitudes, inherently. Due to equality of voltage steps, it can be concluded that the proposed scheme is applicable on all five-level inverters including Diode Clamped (Hasegawa, et Akagi, 2012), Flying Capacitor (FC) (Shukla, Ghosh, et Joshi, 2008), CHB (Sahoo, et Bhattacharya, 2018), Pack U-Cell (PUC) (Vahedi, et al., 2017; Vahedi, Labbé, et Al-Haddad, 2016), etc. Then, the SHM-PAM

equations are rewritten using the new harmonic amplitude formulation derived from two angles condition to mitigate 5^{th} and 7^{th} harmonic orders in normal variables calculations. Some mathematical analysis has been done on harmonics amplitudes and voltage THD to confirm the obtained values for switching angles and input DC voltage index as well as possibility of more non-triplen harmonic amplitudes mitigation. The proposed algorithm is implemented on a single-phase five-level CHB inverter to verify its performance on eliminating and mitigating specified harmonic orders under both linear/nonlinear loads. Section 2.2 includes conventional SHM-PWM and PAM equations for low switching frequency five-level CHB inverters. The modified SHM-PAM equations with self-elimination of all triplen harmonic orders through applying new two angles condition is presented in section 2.3. Moreover, a general solution for self-elimination of all triplen orders in waveforms with arbitrary number of levels is formulated and described at the end of section 2.3. The achieved results for two angles and DC voltage are confirmed through analyzing the harmonic amplitudes and voltage THD in section 2.4. Experimental results are compared with simulation and theoretical ones and discussed in section 2.5.

2.2 Conventional Single-Phase SHM-PAM Technique

2.2.1 5-Level Inverter and Associated Waveform

Figure 2.1 shows single-phase two cells CHB inverter topology, which generates five-level voltage waveform. Each cell is connected to an independent DC voltage source. These two sources can have same or different voltage amplitudes to produce equal or unequal output voltage levels. Figure. 2.2 depicts five-level low switching frequency voltage waveform with two switching angles in the first quarter cycle. As it is evident, low switching five-level waveform can provide the minimum number of switching angles equations among all multilevel waveforms. In general, there are two types for multilevel voltage waveforms including low and high switching frequency. Although, number of angles is arbitrarily selected for each voltage level in high switching waveform, it is confined by levels in low switching one as shown in Figure 2.2.

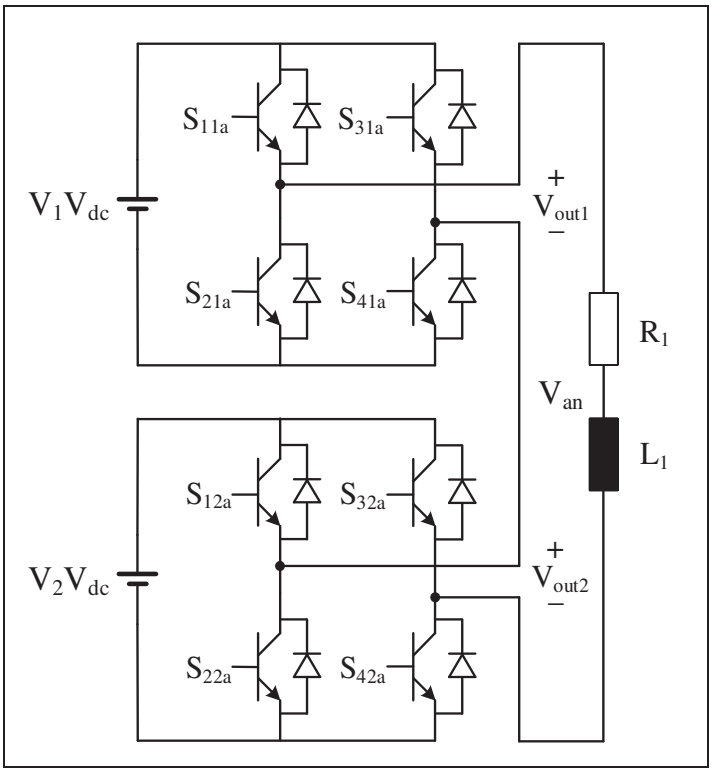

Figure 2.1 Single-phase five-level CHB inverter topology

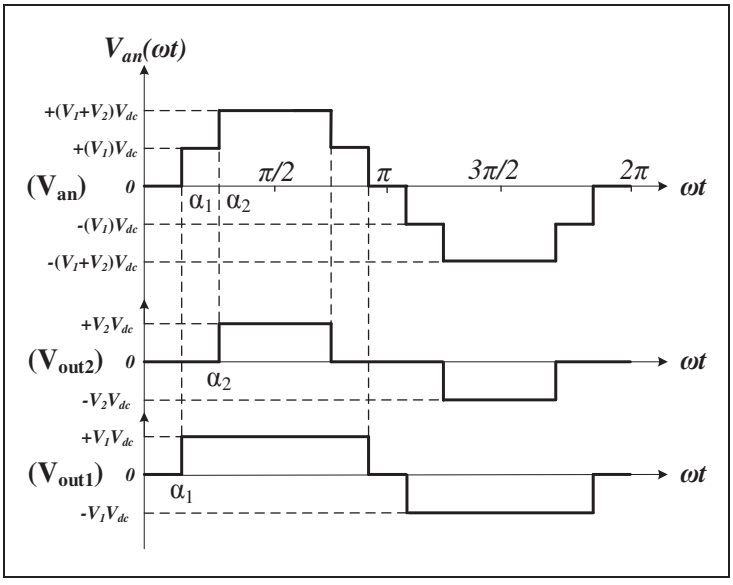

Figure 2.2 Five-level low switching frequency voltage waveform

2.2.2 Single-Phase SHM-PAM principle

The Fourier series decomposition of voltage waveform, with the quarter wave symmetry, includes only odd coefficients and can be expressed as follows:

$$V_{out} = \sum_{n=1,\,3,\,5,\,\ldots}^{\infty} (H_n \ \sin(n\omega t)) \tag{2.1}$$

Where (H_n) are the odd Fourier series coefficients and represent n^{th} harmonic orders amplitude. Using the five-level low switching frequency voltage waveform shown in Figure 2.2, H_n can be computed as:

$$\begin{cases} H_n = \dfrac{4}{n\pi} \left(V_1 \ \cos(n\alpha_1) + V_2 \ \cos(n\alpha_2) \right) \\ \forall\, n = 1,\ 3,\ 5,\ \ldots \end{cases} \tag{2.2}$$

Noticing Eq. (2.2), H_n is computed with respect to the two parameters values: switching angles and DC voltages indices. In SHM-PWM technique only switching angles must be calculated and the DC voltage indices are presumed as 1 p.u. So, there would be two available variables including two switching angles (α_1, α_2 & V_1=V_2=*1 p.u.*) in Figure 2.2 which means that only one harmonic amplitude can be precisely controlled. However, in SHM-PAM technique, DC voltages indices can be considered as variables in order to increase the chance of harmonic mitigation. Therefore, number of variables is increased to four; two switching angles as well as two DC voltages indices (α_1, α_2 & V_1, V_2). Since SHM-PAM provides more variables, it has more flexibility than SHM-PWM in five-level low switching frequency voltage waveform where number of pulses is limited. Moreover, the prominent feature of SHM-PAM technique is to decrease the calculations volume in terms of iteration. When the SHM-PWM equations need to be computed for each value of m_a in a specific range, the PAM relations are calculated once to cover same range of m_a. This will also hugely decrease the required memory capacity in a micro-controller for implementing PAM technique, since look up table is not required any more. The principle of PAM is on the idea that the amplitude of staircase output voltage changes while the pulse widths are kept

constant for different modulation indices. For this purpose, the DC voltages indices have to change proportionally with respect to the modulation index (m_a) as follows:

$$\begin{cases} V_1 = A_1.m_a \\ V_2 = A_2.m_a \end{cases} \tag{2.3}$$

where A_1 & A_2 are linear ratios between DC voltages indices and modulation index.

Table 2.1 Non-Triplen and Triplen Harmonics Amplitude Standard

Non-Triplen Orders		**Triplen Orders**	
Harmonic order (n)	Maximum Allowable Level (L_n)	Harmonic order (n)	Maximum Allowable Level (L_n)
5	6%	3	5%
7	5%	9	1.5%
11	3.5%	15	0.5%
13	3%	21	0.5%
17	2%	>21	0.2%
19	1.5%		
23	1.5%		
25	1.5%		
>25	0.2+32.5/n		

Regarding the SHM technique, the fundamental amplitude has to be set equal to modulation index to produce desired fundamental voltage. Moreover, the undesirable harmonics amplitudes must be mitigated below determined levels as given in Table 2.1. The determined levels ascertain maximum allowable magnitude for each harmonic order. The maximum harmonics amplitudes categorized in (Voltage characteristics of electricity supplied by public distribution systems, 2001; Harmonics, characteristic parameters, methods of study, estimates of existing values in the network, 1981) and listed in Table 2.1 are used as the reference in this work. Since both triplen and non-triplen harmonic orders below 49^{th} are

important in single-phase systems, the single-phase SHM equations include harmonic orders from 3^{rd} to 49^{th}. Considering Eq. (2.3) into the harmonic amplitude formula (Eq. 2), the conventional single-phase SHM-PAM equations for five-level low switching frequency voltage waveform of Figure 2.2 are written as the following:

$$\begin{cases} E_1 = \dfrac{4}{\pi}\ (A_1\ \cos(\alpha_1) + A_2\ \cos(\alpha_2)) = 1 \\ E_n = \dfrac{4}{n\pi}\ (A_1\ \cos(n\alpha_1) + A_2\ \cos(n\alpha_2)) \leq L_n \\ \forall\ n = 3,\ 5,\ ...,\ 49 \\ 0 < \alpha_1 < \alpha_2 < \dfrac{\pi}{2} \quad \& \quad 0 < A_{1,\,2} < 1 \end{cases} \tag{2.4}$$

According to Eq. (2.4), number of equations exceeds number of pulses, which reduces the chance of harmonic mitigation. In order to get a solution, due to the complexity and high non-linearity of Eq. (4), the set of equations is expressed as a unidimensional function, so called objective function (*OF*) of the problem. In this way, the problem has become a multivariable single function optimization problem that can be solved with several heuristic methods as Particle Swarm Optimization, Artificial Bee Colony Algorithm, Simulated Annealing, Tabu Search, etc (Beheshtaein, 2013; Kumar, Dasgupta, et Chatterjee, 2016). Eq. (2.5) shows a possible *OF* for the problem described by Eq. (2.4). It can be seen that every equation has been turned into a quadratic error term multiplied by a weighting coefficient. These weighting coefficients achieve to prioritize some terms versus others. With this formulation, other terms or figures of merit can be easily included like the THD.

$$OF(\alpha_1,\ \alpha_2\ \&\ A_1,\ A_2) = C_1(E_1 - \mathrm{m_a})^2 + \left(\sum_{n=3,\,5,\,...49} C_n(E_n - m_a L_n)^2 \right) + C_{THD} THD \tag{2.5}$$

As mentioned above, each harmonic order contributes with a weighted term on the *OF*. In one hand, the primary objective is to get desired fundamental harmonic amplitude so C_1 must be much higher than any others. In the other hand, it is preferred to mitigate low order harmonics and consequently their weighting coefficients should be greater. As the formulated problem is considering four variables (2 angles and 2 DC sources amplitudes), it is logical to assume that there will be at least a solution that achieve to fix the desired modulation index

and conveniently mitigate the three first harmonic orders (3rd, 5th and 7th). Also, if THD is considered in the *OF*, C_{THD} must be less than the 7th harmonic order but greater than 9th, since there is no guarantee for more harmonic mitigation. However, assuming C_{THD} greater than C_9 gives more control on remaining higher harmonic orders. Eq. (2.6) shows the harmonics orders and THD coefficients modeling.

$$C_1 >> C_3 > C_5 > C_7 >> C_{THD} > C_9 > ... > C_{49} \tag{2.6}$$

2.3 Self-Elimination of All Triplen Harmonics

2.3.1 Proposed Condition for Two Switching Angles (α_1 & α_2)

In conventional single-phase SHM-PAM, triplen harmonics are considered beside non-triplen ones which increases number of equations in *OF*. The main issue is the limitation of available variables in five-level low switching frequency voltage waveform. Although there are four variables in SHM-PAM equations (Eq. (2.4)), it is not ensured that more than three harmonic orders including 3^{rd}, 5^{th} and 7^{th} would be properly mitigated.

In this work, a new condition for switching angles of Figure 2.2 has been presented to control maximum number of harmonics with minimum number of variables. It will be proven that the new design criteria inherently results in full cancellation of all triplen harmonics and single-phase SHM-PAM equations could be written as three-phase ones excluding triplen harmonics. Triplen harmonics are multiple of third orders and have mathematical sequence. Hence, all of triplen harmonics can be removed if one of them is eliminated for a specific condition of angles. Therefore, the first triplen harmonic amplitude must be set to zero to obtain the condition for angles.

$$H_3 = \frac{4}{3\pi} \left(V_1 \cos(3\alpha_1) + V_2 \cos(3\alpha_2) \right) = 0 \tag{2.7}$$

The voltage levels should be identical to find a solution for Eq. (2.7) that yields to a simplified relation between two switching angles as Eq. (2.8). The voltage levels equality

means that the proposed switching technique can be also implemented on all single-DC-source five-level inverters such as FC, PUC, etc. Then, assuming equal steps in Figure 2.2, ($V_1=V_2=V$ & $A_1=A_2=A$ *then* $V=A.m_a$), the condition for two angles will be found by solving the following equation:

$$\cos(3\alpha_1) + \cos(3\alpha_2) = 0 \tag{2.8}$$

The general solution for trigonometric equation of $cos(x)=-cos(y)$ is $x=2K\pi\pm(\pi-y)$. Considering this fact, Eq. (2.9) is achieved from Eq. (2.8):

$$\alpha_2 = \frac{(2K \pm 1)\pi}{3} \pm \alpha_1 \tag{2.9}$$

K belongs to set of integers which is $Z=0, \pm1, \pm2,\ldots$, but the possible relation between two switching angles is attained only for $K=0$. For other values of K, the obtained relations are out of the valid range for switching angles, which is between 0 and $\pi/2$. In other words, they are in contrast to the main switching angles condition of $0<\alpha_1<\alpha_2<\pi/2$. Therefore, the following conditions are finally obtained for two angles (α_1 & α_2) when $K=0$:

$$\begin{cases} (a) : \alpha_2 = \dfrac{\pi}{3} - \alpha_1 \\ (b) : \alpha_2 = \dfrac{\pi}{3} + \alpha_1 \end{cases} \tag{2.10}$$

These two obtained angles conditions can be also examined through applying Eq. (2.10) on main angle condition ($0<\alpha_1<\alpha_2<\pi/2$) to designate a valid range for first switching angle (α_1). In this case, the valid range for α_1 is obtained for both conditions similarly as below:

$$0 < \alpha_1 < \frac{\pi}{6} \tag{2.11}$$

In order to find which condition must be used for writing single-phase SHM equations, first new harmonic amplitude formulation is attained for both conditions. The new H_n with equal

voltage level can be written as Eq. (2.12) by separately substituting these two conditions into Eq. (2.2):

$$\begin{cases} (a) : H_n = \dfrac{8V}{n\pi} \left(\cos(n \dfrac{\pi}{6}). \cos(n(\alpha_1 - \dfrac{\pi}{6})) \right) \\ (b) : H_n = \dfrac{8V}{n\pi} \left(\cos(n \dfrac{\pi}{6}). \cos(n(\alpha_1 + \dfrac{\pi}{6})) \right) \end{cases} \tag{2.12}$$

Since in the SHM technique the first triplen harmonic amplitude must be equal to m_a and $V=A.m_a$, so, the valid range of each fundamental harmonic amplitude presented in Eq. (2.12) is obtained when it is supposed that $0<\alpha_1<\pi/6$.

$$\begin{cases} (a) : \dfrac{\sqrt{3}}{2} < \cos(\alpha_1 - \dfrac{\pi}{6}) < 1 \\ (b) : \dfrac{\sqrt{3}}{2} < \cos(\alpha_1 + \dfrac{\pi}{6}) < \dfrac{1}{2} \end{cases} \tag{2.13}$$

As it can be seen from Eq. (2.13), second harmonic amplitude formulation derived from second switching angle condition does not have valid range for first harmonic amplitude and cannot be used for writing associated single-phase SHM equations. Consequently, the first harmonic amplitude related to the first condition ($\alpha_2=\pi/3-\alpha_1$) is considered to define new single-phase SHM equations with ability of self-elimination of all triplen harmonic orders as bellow:

$$\begin{cases} E_1^{new} = \dfrac{8A}{\pi} . \cos(\dfrac{\pi}{6}). \cos((\alpha_1 - \dfrac{\pi}{6})) = 1 \\ E_n^{new} = \dfrac{8A}{n\pi} . \cos(n \dfrac{\pi}{6}). \cos(n(\alpha_1 - \dfrac{\pi}{6})) \le L_n \\ \forall\, n = 5,\ 7,\ ...,\ 49 \\ 0 < \alpha_1 < \dfrac{\pi}{6} \ \&\ 0 < A < 1 \end{cases} \tag{2.14}$$

According Eq. (2.14), the triplen harmonic orders, as it has been already supposed, have zero amplitude owing to the term of *cos (nπ/6)*. Hence, it is not required to involve them into the equations, so the number of equations is lower than conventional single-phase SHM-PAM provided in Eq. (2.4). The way of solving switching angle (α_1) and the voltage relation (A)

from Eq. (2.14) is exactly as described for Eq. (2.4). Once Eq. (2.14) is turned into the unidimensional *OF* in Eq. (2.15), the weighting coefficients can be modeled in an identical manner summarized in Eq. (2.6), resulting for the proposed modified SHM-PAM as indicated in Eq. (2.16). Also, imposing SHM equations to be solved in specified angles range ($0<\alpha_1<\pi/6$) makes optimization algorithm acts faster to find the angles value since it is searching in smaller range compared to conventional SHM-PAM that it must search in the range of 0 to π/2.

$$OF(\alpha_1 \ \& \ A) = C_1^{new}(E_1^{new} - \mathrm{m_a})^2 + \left(\sum_{n=5,\,7,\,...49} C_n^{new}(E_n^{new} - m_a L_n)^2 \right) + C_{THD}^{new} THD \tag{2.15}$$

$$C_1^{new} >> C_5^{new} > C_7^{new} >> C_{THD}^{new} > C_{11}^{new} > ... > C_{49}^{new} \tag{2.16}$$

Table 2.2 Computed Values for Switching Angles (Radian) and Parameter A

α_1	α_2	A
0.2581	0.7891	0.470

The remaining angle (α_2) can be derived from α_1 using first formula of Eq. (2.10) ($\alpha_2=\pi/3-\alpha_1$). As well, the existence of three variables (α_1, α_2 & A) gives the mitigation of two harmonic orders (5^{th} & 7^{th}). The calculated switching angles and parameter *A* have been shown in Table 2.2. The voltage index for each separated DC source in single-phase five-level CHB inverter (*V*) is obtained based on $V=A.m_a$. Figure 2.3 shows the voltage index versus modulation index. Also, the proposed procedure of self-elimination of all triplen harmonic amplitudes has been demonstrated as a flow chart in Figure 2.4.

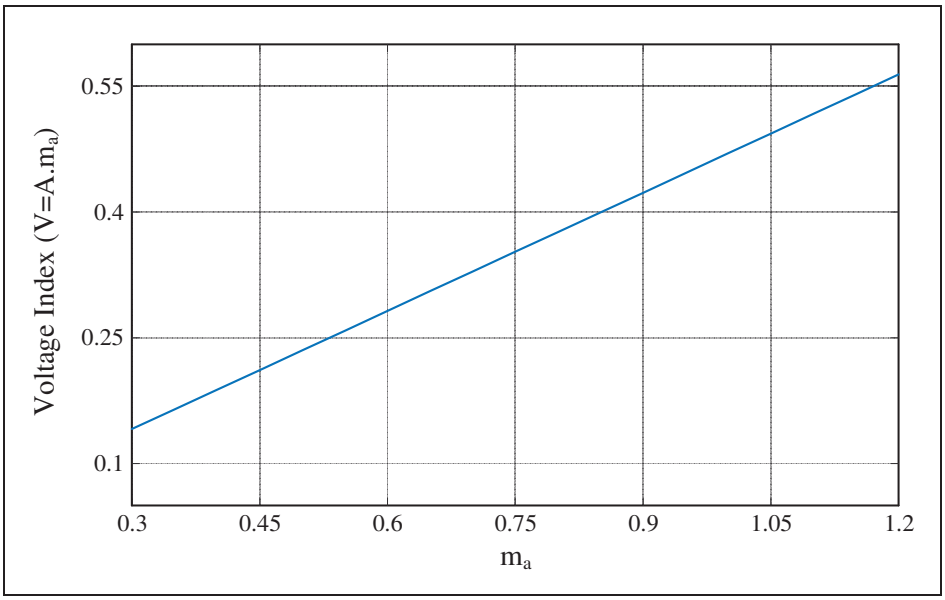

Figure 2.3 Voltage index of separated DC sources in single-phase five-level CHB inverter

2.3.2 A General Solution for Self-Elimination of Triplen Orders in Other Multilevel Voltage Waveforms

Although the proposed technique has been applied on five-level low switching frequency voltage waveform to deal with maximum number of amplitudes while minimum number of transitions is available, it can be extended to other types of multilevel voltage waveforms. As it has been illustrated in Eq. (2.10), a specified relation between two angles has been found to eliminate the first triplen harmonic order and all other triplen orders as the result. Accordingly, the same procedure can be used for other multilevel voltage waveforms to eliminate all triplen harmonic orders. The general format of first triplen harmonic amplitude for a *K*-level multilevel voltage waveform can be expressed as:

$$H_3 = \frac{4}{3\pi}\sum_{i=1}^{k}\left[\begin{array}{l} V_1\sum_{j=1}^{m_1}\left(\pm\cos(3\alpha_j)\right)+V_2\sum_{j=m_2}^{m_3}\left(\pm\cos(3\alpha_j)\right)\cdots \\ +V_i\sum_{j=m_{n-1}}^{m_n}\left(\pm\cos(3\alpha_j)\right) \end{array}\right] \qquad (2.17)$$

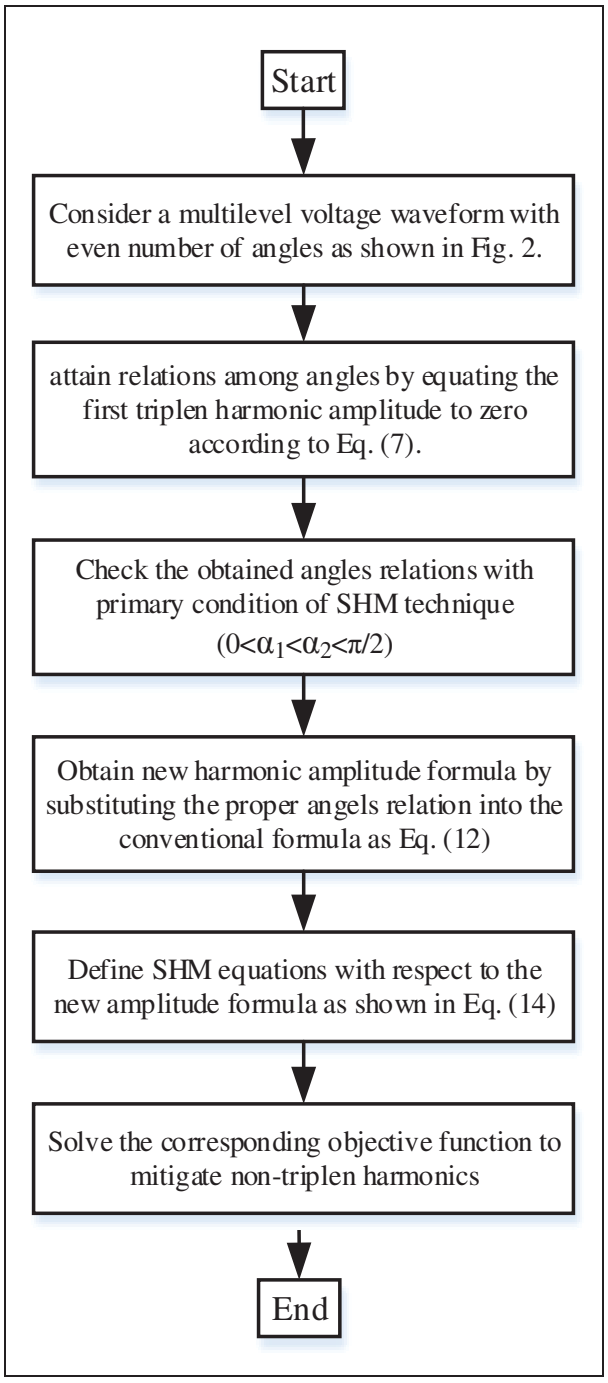

Figure 2.4 The flow chart of proposed procedure
for elimination of all triplen harmonics

m_n is the number of angles in each level. The sign of cosine functions depends on how switching angles are distributed among voltage levels and is precisely determined using Fourier series analysis. Then, the first triplen amplitude can be equivalent to zero if the

trigonometric terms for each voltage level in Eq. (2.17) are set to zero as presented in Eq. (2.18). Therefore, the conditions among switching angles will be attained by solving following equations:

$$\begin{cases} \sum_{j=1}^{m_1} \left(\pm \cos(3\alpha_j) \right) = 0 \\ \sum_{j=m_2}^{m_3} \left(\pm \cos(3\alpha_j) \right) = 0 \\ . \\ . \\ . \\ \pm \sum_{j=m_{n-1}}^{m_n} \left(\pm \cos(3\alpha_j) \right) = 0 \end{cases} \tag{2.18}$$

The corresponding single-phase SHM equations will be achieved from new harmonic amplitude formula considering the obtained conditions for switching angles.

2.3.3 Comparative Study among Conventional SHM-PWM/PAM and Modified SHM-PAM Techniques

Table 2.3 shows number of variables, number of harmonic orders that have chance to be controlled and number of equations in conventional single-phase SHM-PWM/PAM and modified single-phase SHM-PAM techniques in 5-level low switching frequency voltage waveform. In conventional single-phase SHM-PWM technique for low switching 5-level waveform, there are 2 switching angles so just 3^{rd} harmonic is controlled; but, it can be applied on any five-level inverter since it is independent from DC sources. The conventional single-phase SHM-PAM has 4 variables (two switching angles and two DC source) in a 5-level CHB that can control 3 harmonic orders including 3^{rd}, 5^{th} and 7^{th}. However, it is limited to five-level CHB inverter topology where there are enough DC sources to be used as variables in SHM equations. The modified single-phase SHM-PAM technique as the proposed method for self-elimination of triplen harmonics can control 10 harmonic orders in range of 3^{rd}-49^{th} while only three variables (two angles and one DC source) have been considered. Moreover, since the DC sources are assumed equal, it can be applied on any five-

level inverter topology. It must be mentioned that all triplen harmonics are eliminated in modified SHM-PAM technique due to obtained angles constraint. Therefore, the modified SHM-PAM technique not only controls more harmonic orders, but also it is not limited to particular inverter topology. In addition to the aforementioned points, the conventional single-phase SHM-PWM and PAM have 25 equations since they should consider both triplen and non-triplen harmonic orders. On the contrary, the modified single-phase SHM-PAM has only 17 equations since all triplen harmonics are naturally eliminated due to the obtained angles constraint of Eq. (2.10). Therefore, single-phase modified SHM-PAM equations have less complexity to be solved even with less number of variables.

Table 2.3 A Comparison Among Conventional SHM-PWM/PAM and Modified SHM-PAM

	Conventional SHM-PWM	**Conventional SHM-PAM**	**Modified SHM-PAM**
Number of variables (switching angles & DC sources)	2	4	3
Number of controlled harmonics in the range of 3^{rd}-49^{th}	1	3	10
Required inverter's type	Any five-level inverter	Five-level CHB inverter	Any five-level inverter
Number of single-phase SHM equations	25	25	17

2.4 Mathematical Analysis of Proposed Conditional for Two Switching Angles

2.4.1 Harmonic Amplitude

The Fourier series has been presented based on the conception that every periodic function can be defined by sum of sine and cosine functions. Since harmonics amplitude has been

defined by two variables in Eq. (2.12), it is possible to show the harmonics amplitude waveform to investigate the harmonics amplitudes mitigation capacity.

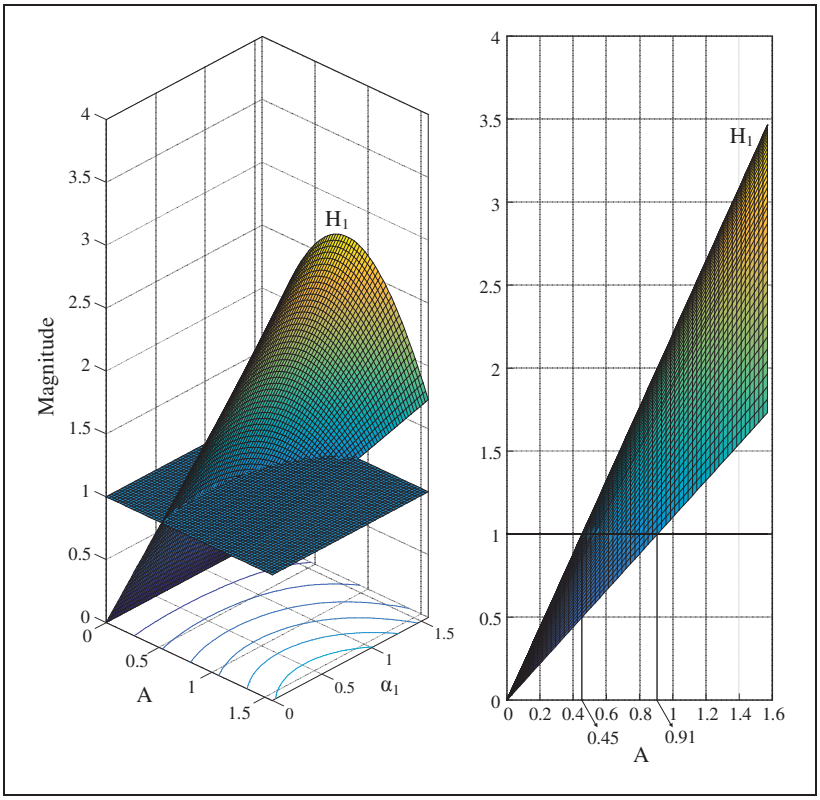

Figure 2.5 3-D waveform of first harmonic (H_1)

To this end, the amplitudes of harmonics orders (H_1, H_5, H_7 & H_{11}) considering SHM-PAM equations (Eq. (2.14)) have been outlined in 3-D space based on two variables (A, α_1). First equation containing first harmonic amplitude has been separately plotted in Figure 2.5 to determine the range of parameter A.

As it is shown in X-Z (*A-Magnitude*) view, two figures have intersected when $0.45<A<0.91$ which means the first harmonic has possibility of having the exact value in Eq. (2.14). 3-D waveform of three harmonics amplitudes (H_5, H_7 & H_{11}) have been drawn in Figure 2.6 to find accurate values of A and α_1 as well as to investigate if more harmonic orders can be mitigated. To prevent complexity in analysis, 3-D waveform of harmonic orders has been shown in Y-Z (α_1-*Magnitude*) view in Figure 2.6.

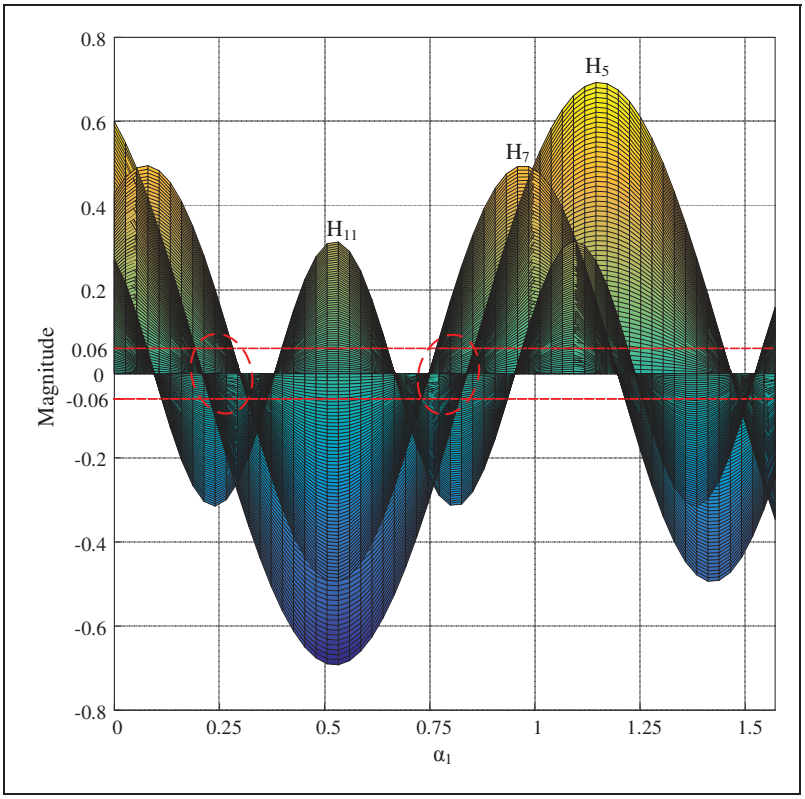

Figure 2.6 3-D waveform of harmonics orders H_5, H_7 & H_{11}

The horizontal dotted lines in Figure 2.6 determine standard value for 5th harmonic order which has the highest maximum allowable value among all harmonic orders. Two areas have been also specified by dashed ovals in which the 5th and 7th harmonic orders have chance to meet the grid codes.

By analyzing 3-D waveform of mentioned harmonic orders for various values of parameter *A*, it has been found out that 5th and 7th orders have admissible amplitude for *A= 0.470*. Figure 2.7 shows the amplitude of harmonic orders H_1, H_5, H_7 and H_{11} versus α_1 when *A=0.470*.

As illustrated in that figure, the first harmonic amplitude has the exact magnitude (*1*) in two points, which is regarding with two values in degree axis. These values represent the

obtained switching angles (α_1 & α_2) shown in Table 2.2. Therefore, the specific values of obtained switching angles have been validated by Figure 2.7 visualization.

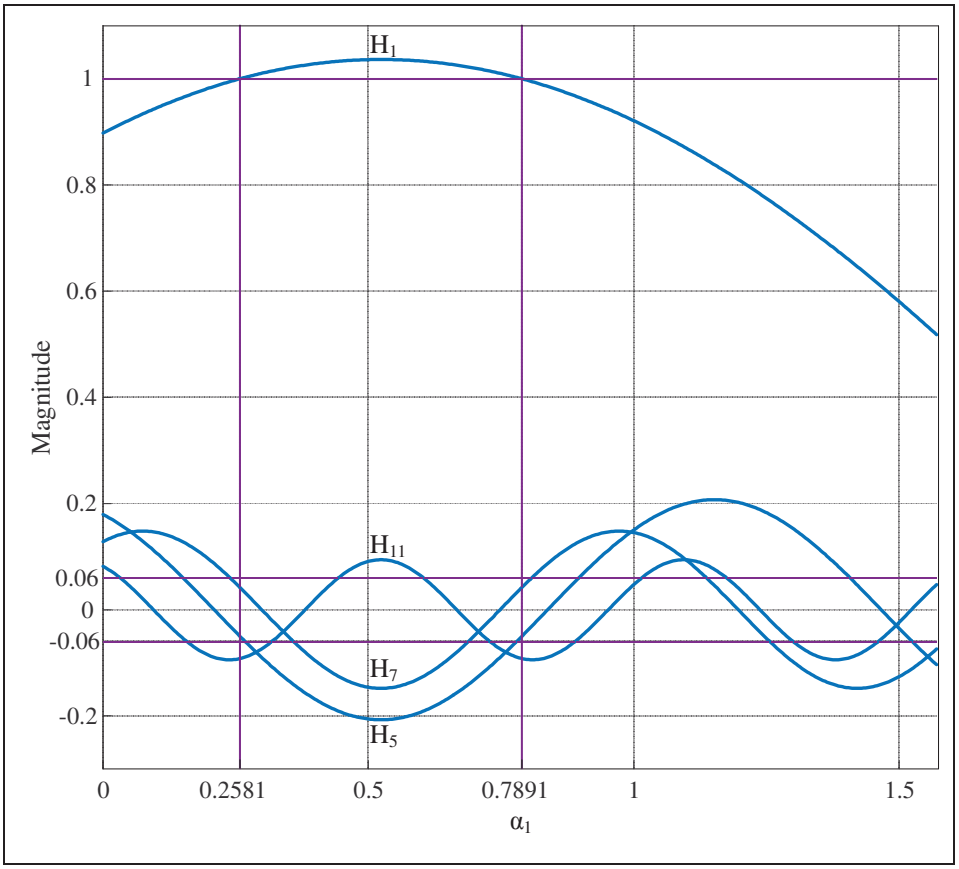

Figure 2.7 Sine waveform of harmonics amplitudes; H_1, H_5, H_7 & H_{11}

2.4.2 Voltage THD

Moreover, it is possible to obtain the THD graph with respect to the switching angles in the proposed single-phase SHM technique. It can be used to determine the range of switching angles value while THD has a minimum value. THD is figure of merit for quality evaluation of voltage or current waveform and is defined as:

$$THD = \frac{\sqrt{\sum_{n=3,\,5,\,7,\,\ldots} H_n^2}}{H_1} \tag{2.19}$$

The voltage THD formula for proposed switching technique with self-elimination of triplen harmonics is achieved substituting new equation of harmonic amplitudes (first formula of Eq. (2.12)) into Eq. (2.19) as:

$$THD = \frac{\sqrt{\sum_{n=5,\,7,\,11,\,\ldots} \frac{\left(\cos(n\,\frac{\pi}{6}).\ \cos(n(\alpha_1 - \frac{\pi}{6}))\right)}{n}}}{\left(\cos(\frac{\pi}{6}).\ \cos(n(\alpha_1 - \frac{\pi}{6}))\right)} \tag{2.20}$$

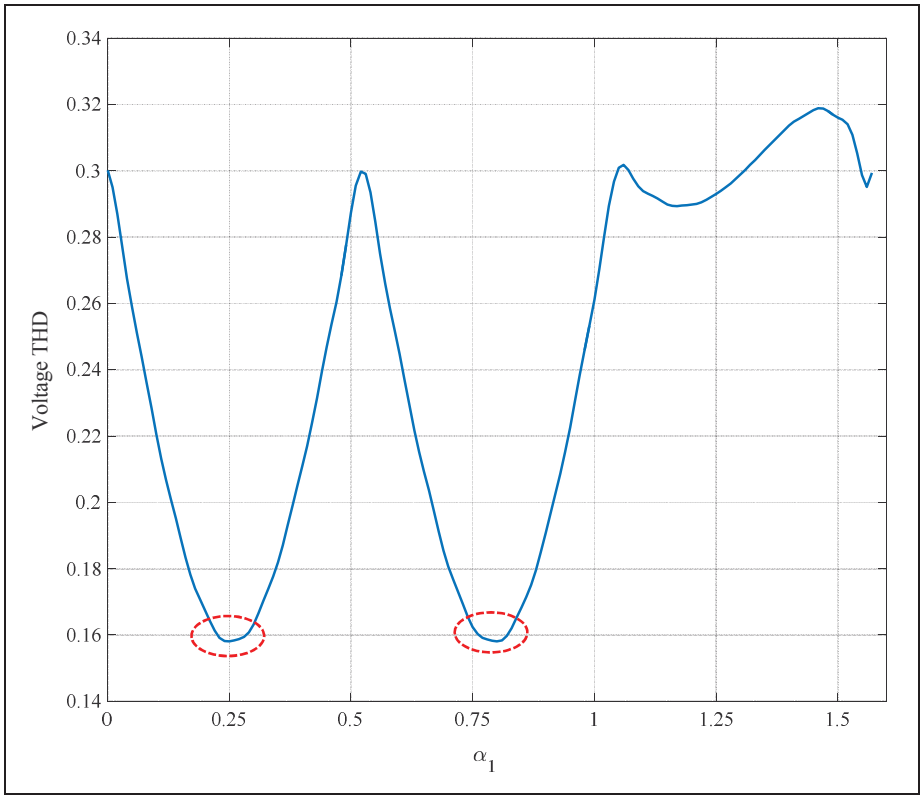

Figure 2.8 Voltage THD curve based on switching angle (α_1)

Since voltage THD formula of Eq. (2.20) is written based on only one switching angles (α_1), it would be also possible to depict the THD waveform with respect to the angle in order to find the minimum THD value. Figure 2.8 shows voltage THD versus the first switching angle (α_1). According to Figure 2.8, THD has two minimum points (shown by dashed circles) which are complying with two obtained switching angles values (α_1 & α_2) listed in Table 2.2.

It assures that the obtained angles have the optimum values and consequently lead to have minimum voltage THD.

2.5 Results Discussion

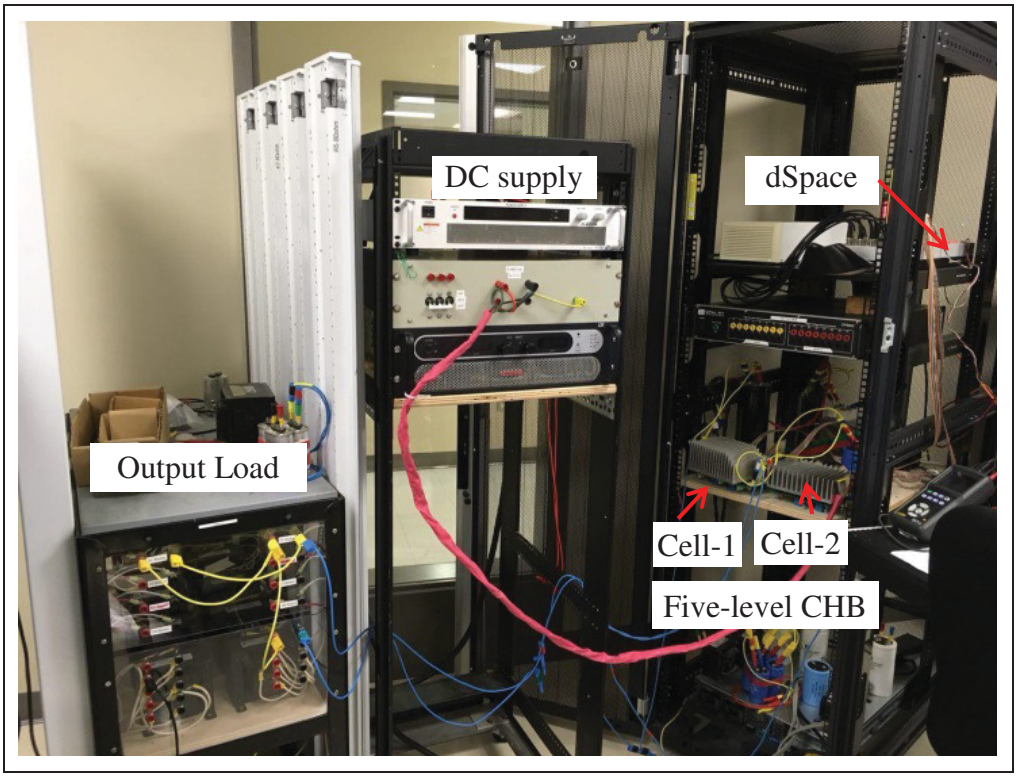

Figure 2.9 Experimental test setup of five-level CHB inverter

The harmonic contents of both conventional and improved single-phase SHM-PAM are compared to confirm that the proposed single-phase SHM-PAM technique results in better harmonic content. Afterwards, the proposed SHM-PAM technique is implemented on a single-phase five-level CHB inverter prototype built in the laboratory using dSpace as real-time controller and evaluated under both linear and nonlinear loads. Figure 2.9 shows the corresponding experimental test setup. The nominal DC source (V_{dc}) applied on each full bridge inverter and output voltage frequency are 200 V and 50 Hz, respectively. The PAM can be also done through a DC-DC converter with close loop system provided by a PI controller to produce the desired DC input voltage for CHB inverter as illustrated in Figure

2.10. Since the fundamental harmonic amplitude of output AC voltage is determined based on m_a and the input DC voltage linearly varies with respect to m_a in PAM technique, the output AC voltage is controlled if the input DC voltage is desirably regulated. Then, controlling of the output AC voltage can be done through adjusting m_a to produce desired input DC voltage as shown in close-loop controller of Figure 2.10.

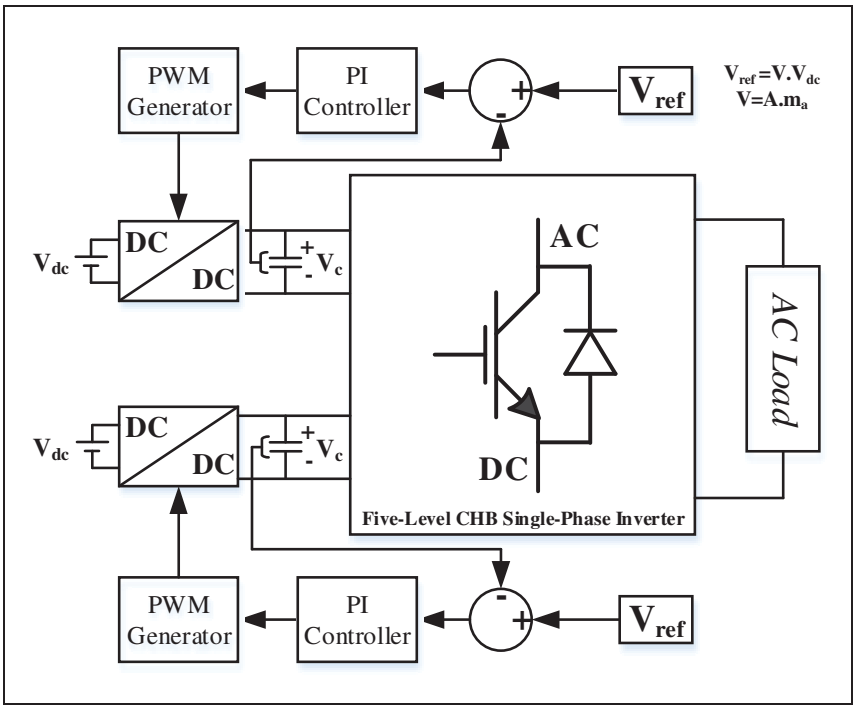

Figure 2.10 Close loop controller for implementation of PAM

2.5.1 Analytical Comparison of Harmonic Amplitudes

The conventional single-phase SHM-PAM with four variables (α_1, α_2 & V_1, V_2) in low switching frequency five-level leads to mitigation of three harmonics including 3rd, 5th, 7th and the first unmitigated order is 9th presented in (Ghoreishy et al., 2012a). On the other hand, it is shown that the improved single-phase SHM-PAM with proposed angles' condition eliminates all triplen harmonics in addition to mitigate harmonic amplitudes 5th, 7th and the first unmitigated harmonic amplitude is 11th. Then, more harmonic amplitudes have been reduced with less number of variables. Figure 2.11 illustrates a comparison among harmonic amplitudes of conventional and improved single-phase SHM-PAM with standard level in

range of 3rd to 49th. Figure 2.11-a shows non-triplen amplitudes as well as THD and Figure 2.11-b includes triplen ones.

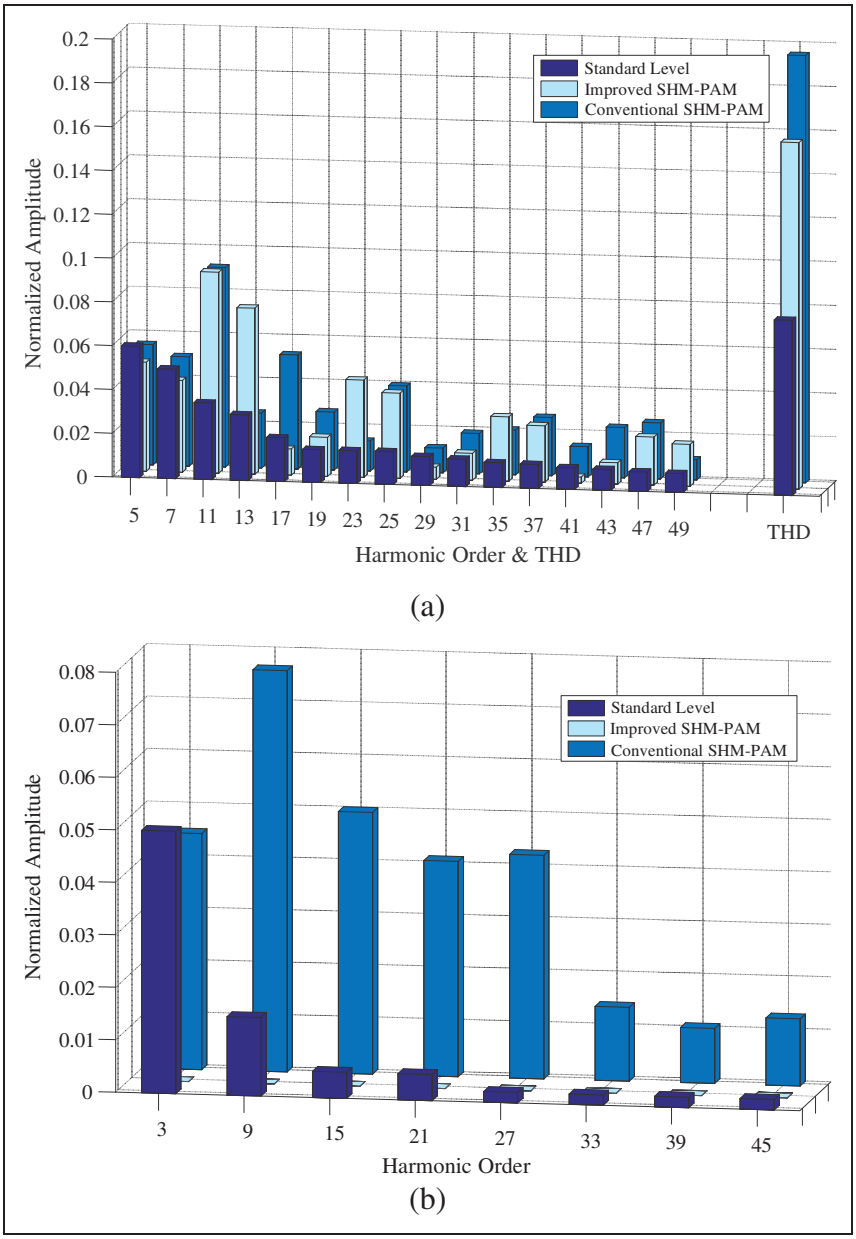

Figure 2.11 Non-triplen and triplen amplitudes in both conventional and improved single-phase SHM-PAM techniques, (a) non-triplen, (b) triplen

According to Figure 2.11-a, two non-triplen harmonic orders 5th and 7th have been mitigated properly in both techniques. For higher non-triplen orders, there are no remarkable

differences between two techniques; the conventional SHM has lower amplitude for some orders, while the improved technique has better results for some others. However, lower voltage THD in the improved single-phase SHM-PAM (15.8) is mainly due to cancellation of all triplen harmonics amplitudes demonstrated in Figure 2.11-b. Such acquired value for voltage THD is acceptable while the minimum number of angles is selected to decrease switching frequency to 100 Hz. Moreover, the remained uncontrolled harmonics can be removed using LC filter. Since the LC filter for modified single-phase SHM-PAM must be tuned on 11^{th}, it has smaller size compared conventional one that should be adjusted on 9^{th}.

2.5.2 Experimental Evaluation of Single-Phase CHB Performance under Linear/Nonlinear Loads

Figure 2.12 depicts the five-level voltage and load current waveforms for the modulation indices 0.45, 0.85 and 1.1. The single-phase CHB inverter is supplying linear R-L load that R=40 Ω and L=20 mH. As can be seen from voltage waveform, the width of the pulses is kept constant while modulation index changes. On the contrary, pulses amplitudes of output voltage change linearly with respect to modulation index. As a result of invariable pulses' width of output voltage waveform, voltage THD will have constant value, as well. Moreover, the harmonic amplitudes and voltage THD achieved from experimental result of Figure 2.12 related to modulation index 0.85 have been compared to the corresponding theoretical and simulation ones. In this case, Figure 2.13-a includes non-triplen harmonic orders while triplen ones are shown in Figure 2.13-b. Since it was proven that triplen harmonic amplitudes are theoretically zero, Figure 2.13-b contains only simulation and experimental results of triplen amplitudes. Also, the harmonics amplitudes have been normalized by the first harmonic amplitude. The harmonic contents of these three situations (theoretical, simulation and experimental) validate that the amplitudes of 5^{th} and 7^{th} harmonic orders have been mitigated below standard level along with self-elimination of all triplen harmonics, even though; there is a negligible difference among them. The ignorable difference means while triplen harmonics theoretically are zero, they have amplitude less than 0.001 in simulation and experimental results, which is approximately zero.

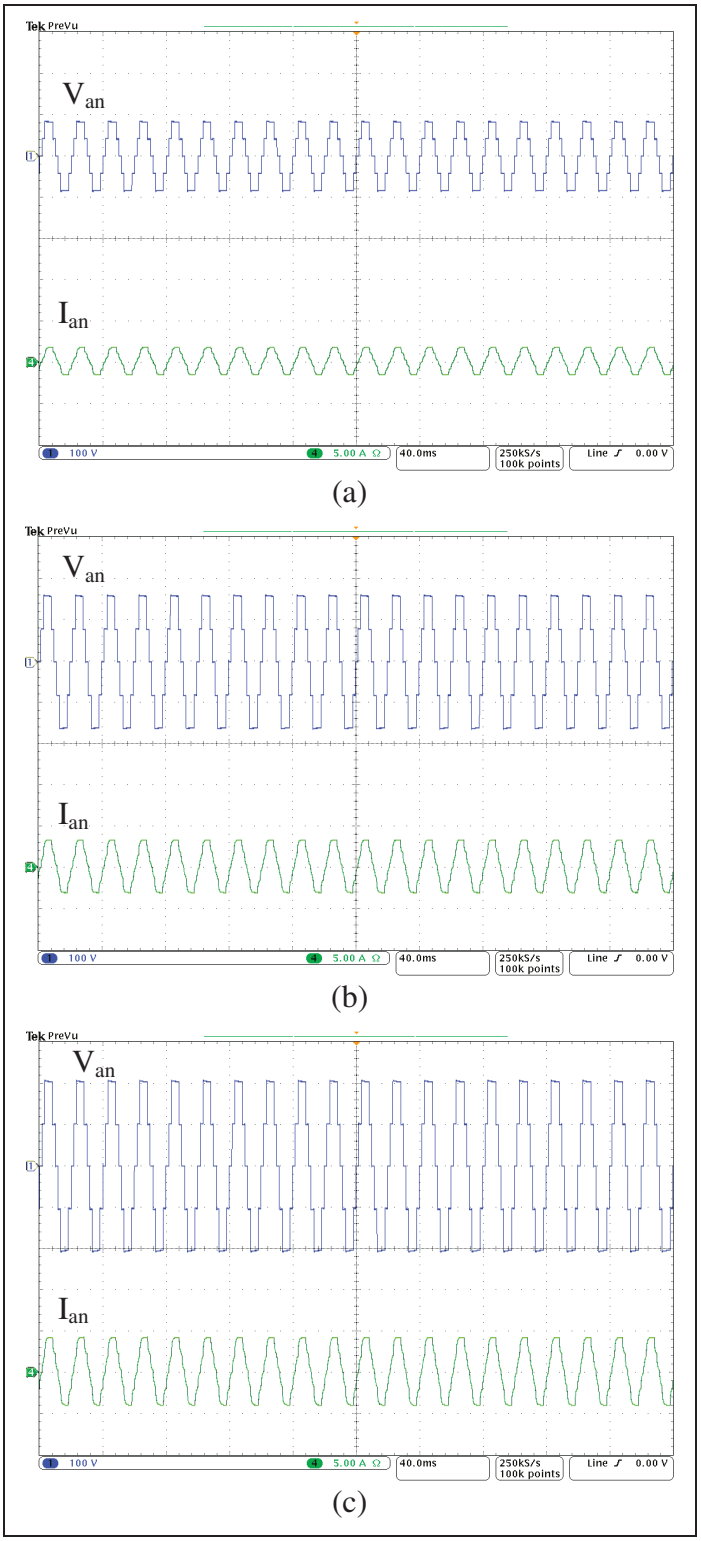

Figure 2.12 Output Voltage and current waveforms of five-level single-phase CHB inverter under linear R-L load for different the modulation indices,
(a) m_a=0.45, (b) m_a=0.85, (c) m_a=1.1

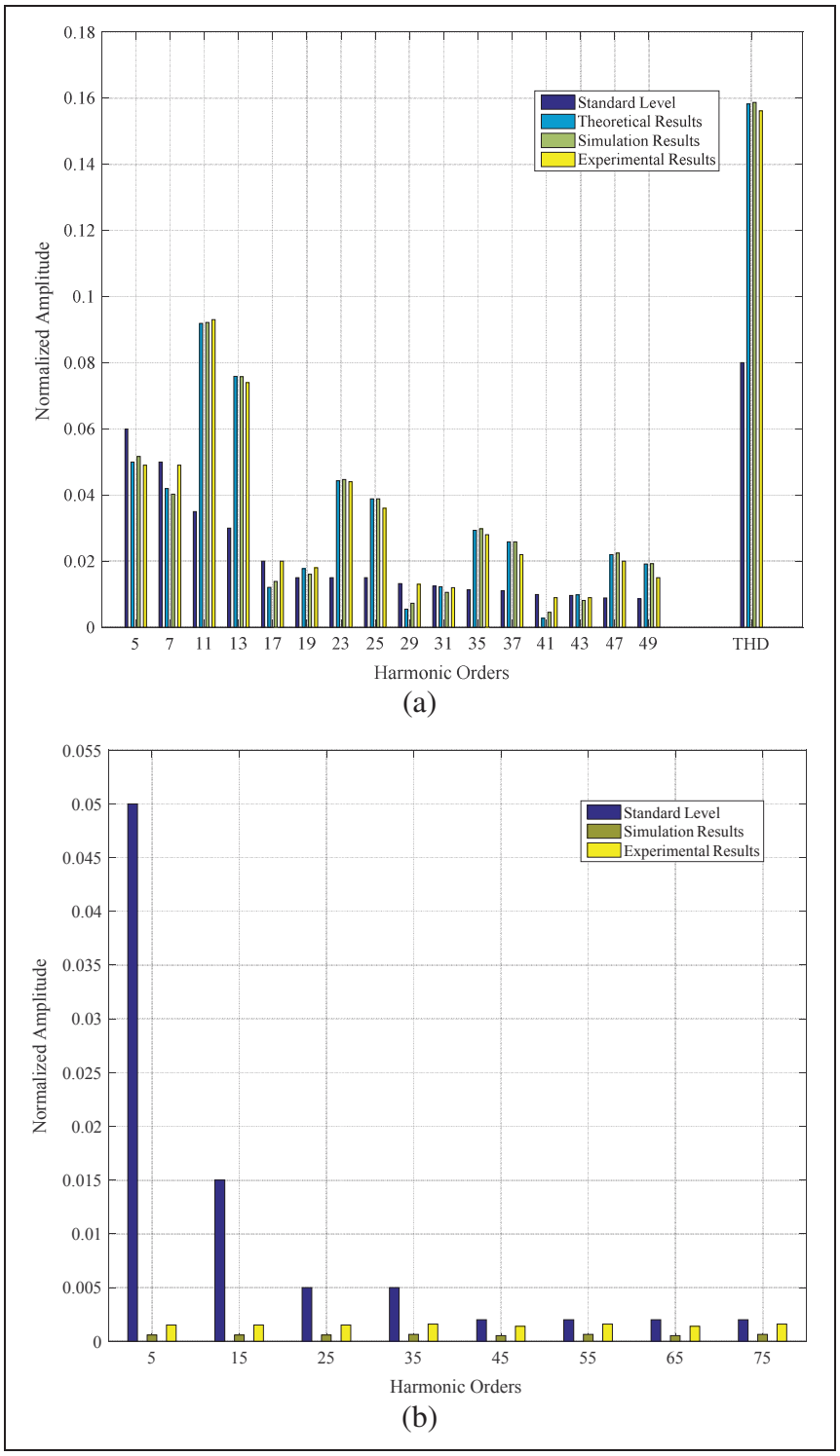

Figure 2.13 Harmonic amplitudes and voltage THD for theoretical, simulation and experimental results, (a) Triplen orders, (b) Non-triplen orders

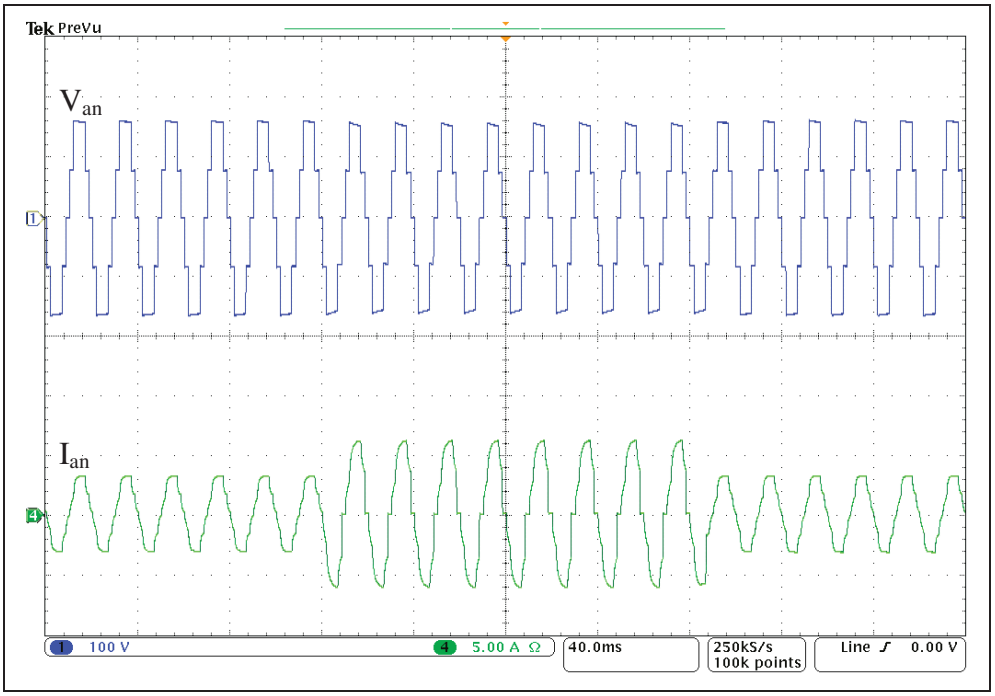

Figure 2.14 Voltage and current waveforms when five-level CHB inverter supplies both linear and harmonic loads

Furthermore, the elimination of all triplen harmonic orders enables CHB inverter to deal with nonlinear loads beside linear ones. A single-phase diode rectifier connected to R-L load has been assumed as a nonlinear load. The output rectifier load is R-L that R=40 Ω and L=50 mH. Figure 2.14 demonstrates output voltage and load current waveforms when five-level CHB inverter supplies both linear and nonlinear loads. According to Figure 2.14, there is no voltage or current transient when the diode rectifier is connected/disconnected to/from single-phase CHB inverter. Thus, the ability of handling linear/nonlinear loads because of controlling important non-triplen low orders besides all-triplen harmonics makes the proposed switching method suitable candidate for standalone single-phase Uninterruptible Power Supply (UPS) applications which deals with both normal and harmonic loads in practical situations.

Moreover, in a 3-phase UPS, the single-phase loads are usually fed through the fourth wire, which deals with those triplen harmonics inherently (Sharifzadeh et al., 2016b; Sharifzadeh et al., 2015). Since all triplen harmonics are eliminated in the proposed method, it can be also

employed in 3-phase 4-wire inverters for 3-phase UPS applications where triplen harmonics must be suppressed to keep phase voltages balanced under linear/nonlinear and single/three-phase loads. Considering the fact that the proposed technique is suitable for all type of five-level inverters, it can be applied on single-DC source inverter like NPC in case of 3-phase 4-wire system to use less DC sources. Furthermore, the proposed technique can be investigated for drive application where an electrical motor is supplied by back-to-back (AC-DC-AC) converters. In this regard, PAM converter has been already introduced in (Schwager et al., 2014; Kieferndorf, Forster, et Lipo, 2004) for drive application where the proposed SHM-PAM is a compatible technique to be applied in addition to that it removes all triplen harmonics that are harmful for electrical motors.

2.6 Conclusions

In this work, a new condition for two angles in five-level low switching frequency voltage waveform has been proposed to modify conventional SHM-PAM equations in order to eliminate all triplen harmonics. 5^{th} and 7^{th} harmonic orders have been also mitigated through solving normal SHM relations without considering extra pulses. Therefore, it has the advantage of controlling maximum number of harmonics amplitudes with minimum number of variables in single-phase inverter where both triplen and non-triplen order have to be considered in the equations. Due to elimination of all triplen harmonics, the modified SHM-PAM technique has been simplified in such way that it has fewer number of equations compared to conventional SHM-PAM technique while more harmonics could be controlled. The proposed technique has been applied on single-phase five-level CHB inverter and tested under both linear and nonlinear loads and consequently will be a suitable candidate for single-phase UPS application that must supply these type of loads in practical situations. On the other hand, it is also applicable in 3-phase 4-wire inverters where triplen harmonics must be cancelled out to keep the phase voltage balanced under linear/nonlinear and single/three-phase loads conditions as well as electrical drive using PAM converters. It has demonstrated that the presented method is extendable to other multilevel voltage waveforms and a general solution for triplen harmonics elimination has been derived. However, the details of

circumstances of angles calculations must be discussed in future works to generalize a formulation of self-elimination of triplen orders and mitigation of non-triplen one appropriate for standalone inverters applications.

CHAPTER 3

NEW CONSTRAINT IN SHE-PWM FOR SINGLE PHASE INVERTER APPLICATIONS

Mohammad Sharifzadeh [a], Hani Vahedi [b], Kamal Al-Haddad [c]

[a, b, c] Department of Electrical Engineering, École de Technologie Supérieure,
1100 Notre-Dame West, Montreal, Quebec, Canada, H3C 1K3

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Abstract

This chapter proposes new angles constraint for Selective Harmonic Elimination (SHE)-PWM utilized in single-phase inverter applications. The proposed angles constraint naturally eliminates all triplen harmonics whereas they were conventionally appeared in all single-phase output voltages. The harmonic amplitude formula is developed based on the obtained angles constraint and then modified single-phase SHE equations are defined to eliminate only specified low non-triplen harmonics. Therefore, more harmonics would be eliminated with same switching frequency in modified SHE-PWM. Five-level voltage waveform has been opted to implement the introduced method; but, it can be applied on all multilevel voltage waveforms such as seven-level with even number of angles. Unlike conventional SHE technique, voltage THD is analyzable in modified SHE to find optimum values for switching angles in order to control non-eliminated harmonic amplitudes and minimize THD. Moreover, the cancellation of triplen harmonics empowers single-phase inverter to supply nonlinear loads beside linear ones. Some experimental tests are accomplished using a single-phase 5-level Modified Packed U-Cell (MPUC) inverter. Results are discussed to prove the excellent performance of single-phase MPUC inverter under both normal and harmonic loads and accurate elimination of determined triplen and non-triplen harmonics by applying the presented angles constraint.

3.1 Introduction

Growing the exploitation of renewable energy sources in higher voltage and power ratios demands continuous improvement in power electronics converters (Franquelo et al., 2008; Wu et al., 2017; Xiao et al., 2015; Vahedi, Sharifzadeh, et Al-Haddad, 2018). During the last decade, multilevel inverters have been proven to be utilized in single/three-phase applications with higher range of power (Vahedi, Labbé, et Al-Haddad, 2016; Elias et al., 2014). Multilevel inverter topologies have more semiconductor components in order to decrease voltage stress and harmonic distortion through producing more voltage levels. On the other hand, additional switching elements can increase power losses particularly when high switching frequency methods are implemented (Vahedi et Al-Haddad, 2016; Edpuganti et Rathore, 2015; Vahedi, Sharifzadeh, et Al-Haddad; 2017). Selective Harmonic Elimination-Pulse Width Modulation (SHE-PWM) has been introduced to restrict switching frequency by selection of pulses in a predetermined voltage waveforms (Yang et al., 2016; Dahidah, Konstantinou, et Agelidis, 2015; Wang et Ahmadi, 2010; Yang et al., 2017).

Using Fourier analysis on the voltage, the harmonics amplitudes are formulized based on the pulses transitions which are called switching angles. Then, the precise suppression of harmonics is done solving a set of nonlinear trigonometric equations derived from amplitudes formula (Dahidah, Konstantinou, et Agelidis, 2015). Such interesting advantages have led to many accomplished research on different voltage waveforms including bipolar, unipolar and multilevel in single/three-phase inverters (Chiasson et al., 2004; Fei, Ruan, et Wu, 2009). Moreover, various studies have been conducted to adjust SHE operation for specific standalone applications such as four-leg inverter (Sharifzadeh et al., 2015), electrical motor drive (Zhang, Zhao, et Zhu, 2011), etc.

Despite this, one of the usual challenges that confine extension of SHE utilization is that the number of eliminated harmonics depends on the number of angles. In addition, there is no control on non-eliminated higher harmonics orders and THD consequently (Sharifzadeh, Vahedi, et Al-Haddad, 2017). This issue needs to be essentially noticed when SHE is applied

on single-phase inverters where triplen harmonics have same importance of non-triplen ones in the SHE equations. Therefore, more amplitude is involved compared to three-phase SHE equations. An effortless solution is to add more angles, however, extra pulses will increase switching frequency and complicate SHE computations undesirably (Sharifzadeh et al., 2016).

Some analytical methods were proposed in the literature to attain optimum switching angles and control non-eliminated orders. In (Agelidis et al., 2006; Agelidis, Balouktsis, et Cossar, 2008) a multiple set of solution were found for single-phase SHE equations to determine which angles trajectories have lower amplitudes for non-eliminated harmonics. Also, Selective Harmonic Mitigation (SHM)-PWM was derived through manipulating SHE to mitigate low order amplitudes and control higher order ones (Franquelo et al., 2007; Moeini, Iman-Eini, et Bakhshizadeh, 2014; Sharifzadeh et al., 2018; Sharifzadeh et al., 2017b). Although the output voltage harmonic content was improved, the switching angles calculations are further complicated in those presented approaches. In addition, more pulses are still required to increase number of proper controlled amplitudes (Sharifzadeh et al., 2016a). In (Konstantinou, Agelidis, et Pou, 2014), SHE-PWM for single-phase inverter was presented to investigate the possibility of controlling maximum number of harmonics without adding more angle. According to proposed technique, SHE solving method was modified to find an angles trajectory that has maximum amplitudes controlled. Even in this case, only two more harmonic amplitudes could be minimized. Also, there is no mathematical analysis to explain the extra harmonic minimization.

In this work, a new constraint on switching angles is developed to inherently remove all triplen harmonics from conventional single-phase SHE equations and consequently output voltage without increasing the switching frequency. Since the angles constraint is supposed to eliminate all triplen harmonics, it will be obtained through analysis on triplen amplitudes formula. Triplen orders unlike non-triplen ones follow regular mathematical sequence. Thus, if first triplen harmonic amplitude is removed for a particular angles condition, the rest of triplen harmonics are also eliminated for the same situation. Hereupon, some calculations are

performed for first triplen harmonic in five-level waveform to find the angles constraint considering inherent elimination of all triplen harmonics.

Afterwards, the conventional harmonics amplitude formula is developed with respect to the proposed angles constraint to modify single-phase SHE equations in order to eliminate only determined non-triplen harmonics through calculation of switching angles. Actually, the modified single-phase SHE equations are written as three-phase equations that results in less complexity because of including only non-triplen amplitudes. Then, more harmonic amplitudes could be eliminated with the same number of angles. Moreover, the proposed single-phase SHE equations are analyzed from THD point of view to obtain optimum values for switching angles while THD is minimized. In this case, the specified ranges for switching angles are obtained from THD analysis by which THD would have lower value. The minimization of voltage THD is acquired since the non-eliminated harmonics in modified single-phase SHE technique have lower amplitudes compared to conventional one. Therefore, unlike conventional SHE in which the THD is uncontrollable, modified single-phase SHE-PWM not only eliminates maximum harmonic amplitudes, but also reduces the THD value. Modified PUC (MPUC) inverter with two independent sources as a five-level inverter has been chosen to implement the modified single-phase SHE method. The cancellation of all triplen harmonic orders improves single-phase inverter performance to supply both linear and nonlinear loads. Furthermore, the proposed angles condition is also suitable for all type of multilevel voltage waveform with even number of angles which can make it as a permanent constraint in single-phase SHE-PWM. Section 3.2 describes the five-level MPUC inverter configuration. The conventional and proposed single-phase SHE-PWM is also explained in this section. Section 3.3 includes some analysis conducted on voltage THD to obtain optimum switching angles and minimum THD values. The angles constraint has been achieved for a seven-level voltage in section 3.4 to confirm that the proposed method is extendable for other voltage waveforms. Experimental results are presented in section 3.5 to evaluate the performance of single-phase MPUC inverter under linear/nonlinear loads when it is controlled by designed SHE switching technique.

3.2 Proposed SHE-PWM for Single-Phase Systems

3.2.1 Modified PUC (MPUC) Inverter

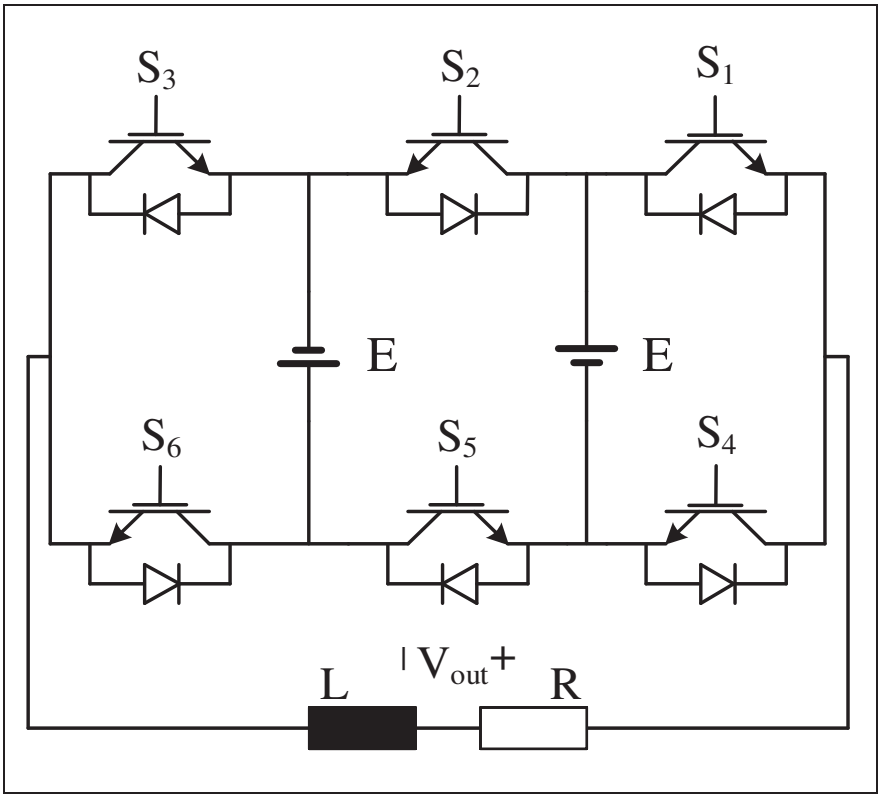

Figure 3.1 Five-level Modified PUC (MPUC) inverter topology

PUC inverter has been introduced in 2011 and then developed in 2016 as a el topology called PUC5 (Vahedi, Labbé, et Al-Haddad, 2016). PUC5 can produce five-level voltage with less power semiconductor switches and lower switching frequency compared to the conventional five-level inverters. The MPUC inverter with two separated DC sources shown in Figure 3.1 has been derived after a slight modification to PUC5 (Vahedi, Labbé, et Al-Haddad, 2016). MPUC is chosen in this work to implement the designed switching control strategy. Both DC sources have same voltage amplitudes. Switches ((T_1, T_4), (T_2, T_5) & (T_3, T_6)) are working complimentarily. Thus, there are eight switching states for MPUC inverter as listed in Table 3.1.

Table 3.1 Switching States of MPUC Inverters

Switching States	S_1	S_2	S_3	V_{out}
1	1	0	1	+2E
2	1	0	0	+E
3	0	0	1	+E
4	0	0	0	0
5	1	1	1	0
6	1	1	0	-E
7	0	1	1	-E
8	0	1	0	-2E

According to Table 3.1, there are two similar switching pairs (*6, 7*), (*4, 5*) and (*2, 3*) for the voltage levels *-E*, *0* and *+E*, respectively. MPUC switching pulses are adjusted to generate five-level voltage in such way that two switches (T_2 & T_5) have switching frequency equal to fundamental voltage frequency that leads to further power losses reduction. Since, there is no need to use all redundant switching states, only the states of *1*, *2*, *4*, *7* and *8* are used to fire the MPUC switches.

3.2.2 Conventional Single-Phase SHE Technique

Figure 3.2 depicts a general predefined five-level voltage waveform with quarter wave symmetry. Number of angles in each level of illustrated five-level is arbitrarily selected. Odd quarter wave symmetry in five-level voltage shown in Figure 3.2 results in disappearing even harmonic orders. Then, considering *m* and *k* angles in first and second levels (*+E, +2E*); respectively, the odd harmonic orders (H_n) are generally formulated as Eq. (3.1).

$$H_n = \frac{4E}{n\pi}\left[\sum_{i=1}^{m}\left((-1)^{i+1}\cos(n\alpha_i)\right)+\sum_{i=m+1}^{m+k}\left((-1)^{i}\cos(n\alpha_i)\right)\right] \quad \forall n=1,3,5,... \tag{3.1}$$

The amplitudes formulas are used to constitute SHE equations. According to SHE principle, first amplitude sets equal to modulation index to acquire desired fundamental *AC* voltage

amplitude. The remained amplitudes are equated to zero to be eliminated in voltage spectra. The involved harmonics in SHE equations contain both triplen and non-triplen orders for single-phase inverter because there is no phase-to-phase voltage, so triplen orders cannot be inherently removed by *120°* phase shift. SHE equations including both triplen and non-triplen harmonics for single-phase inverter are written as:

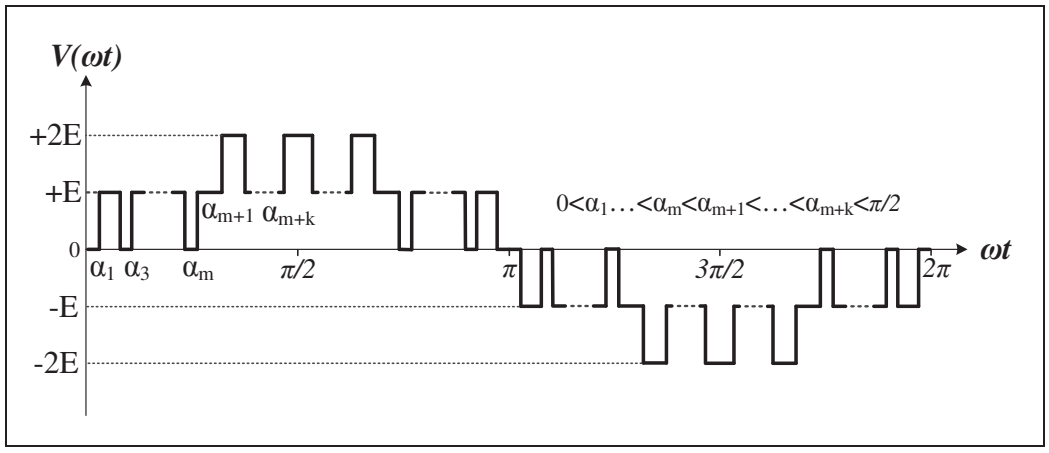

Figure 3.2 Typical predetermined five-level voltage waveform

$$\begin{cases} H_1 = \dfrac{4E}{\pi}\left[\sum_{i=1}^{m}\left((-1)^{i+1}\cos(\alpha_i)\right) + \sum_{i=m+1}^{m+k}\left((-1)^{i}\cos(\alpha_i)\right)\right] = m_a \\ H_n = \dfrac{4E}{n\pi}\left[\sum_{i=1}^{m}\left((-1)^{i+1}\cos(n\alpha_i)\right) + \sum_{i=m+1}^{m+k}\left((-1)^{i}\cos(n\alpha_i)\right)\right] = 0 \\ 0 < \alpha_1 \ldots < \alpha_m < \alpha_{m+1} < \ldots < \alpha_{m+k} < \pi/2 \\ \forall n = 3,\ 5,\ 7,\ \ldots \end{cases} \tag{3.2}$$

The switching angles are computed solving the SHE equations and considering the basic condition regarding to angles sequence in first quarter cycle of Figure 3.2 ($0<\alpha_1\ldots<\alpha_m<\alpha_{m+1}<\ldots<\alpha_{m+k}<\pi/2$). However, number of equations is restricted to the number of angles assumed as variables. In this case, *n-1* harmonics can be eliminated using *n* angles. Since more low harmonics are involved in single-phase SHE equations, additional angles are required to retain harmonic elimination capability. Adding more angles will also increase the number of equations and complicate finding solutions. Besides this, the higher switching frequency is imposed undesirably.

3.2.3 Proposed Single-Phase SHE Technique

Mandatory presence of triplen harmonics as well as non-triplen ones in single-phase SHE results in increasing number of equations compared to three-phase ones. As it was mentioned above, the traditional issue of SHE-PWM is to have limitation in the number of eliminated harmonics. Thus, more pulses should be considered in single-phase SHE for proper elimination of harmonics. If a considerable number of switching angles is assumed in SHE equations to cancel notable number of harmonic amplitudes, it defeats SHE principle in which switching frequency must be kept low. In other words, there is no justification to use SHE with notable number of angles results in high switching frequency. It is due to the fact that modulation techniques such as SPWM and SVM have superiority over SHE technique in case of high switching frequency ratio.

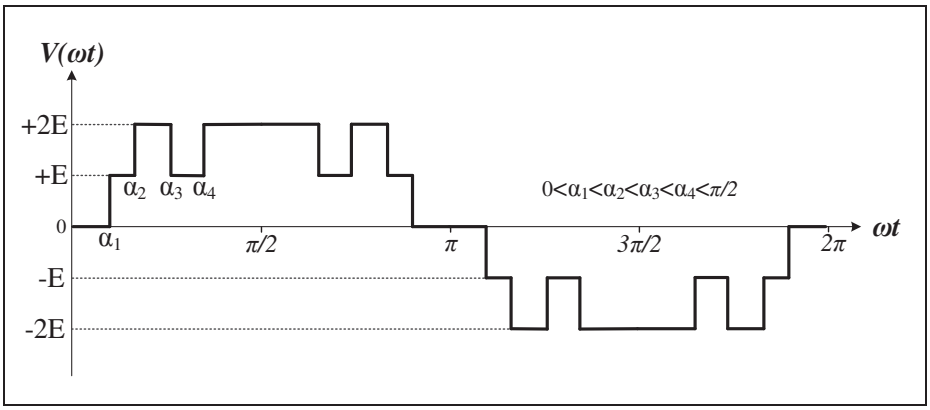

Figure 3.3 Proposed five-level voltage waveform for single-phase inverter

Therefore, a new mathematical angles constraint is introduced in this work to provide a distinct formulation for harmonic amplitude in single-phase SHE equations. According to the new amplitudes formula that is achieved with respect to the proposed angles constraints, all triplen harmonics are inherently eliminated without further angles. Then, it is no longer required to consider triplen harmonics in single-phase SHE equations while determined non-triplen harmonics are removed through the normal operation. As a result, more harmonics are eliminated in single-phase SHE technique at the same switching frequency when the proposed angles constraint is applied on a single-phase SHE technique. In order to obtain the

angles constraint and deal with all triplen harmonics cancellation, five-level voltage with four angles shown in Figure 3.3 is used. The corresponding harmonic amplitude of the proposed five-level voltage waveform will be expressed as Eq. (3.1) using Fourier series analysis:

$$H_n = \frac{4E}{n\pi}\left[\cos(n\alpha_1) + \cos(n\alpha_2) - \cos(n\alpha_3) + \cos(n\alpha_4)\right] \tag{3.3}$$

In conventional single-phase SHE operation, only three harmonic orders including 3rd, 5th and 7th can be eliminated with four switching angles. However, the presented angles constraint leads to more amplitude elimination at the same switching frequency. Since the new angles constraint is supposed to eliminate all triplen harmonics, it would be obtained by performing mathematical analysis on triplen harmonic amplitudes. Considering the fact that there is a determined mathematical order among all triplen harmonics; so, if first triplen order (H_3) could have zero magnitude for a particular condition of angles, the rest of them would be also eliminated for the same angles condition. So, the first triplen amplitude is required to be equal to zero to find the new angles constraint.

$$H_3 = \frac{4E}{3\pi}\left[\cos(3\alpha_1) + \cos(3\alpha_2) - \cos(3\alpha_3) + \cos(3\alpha_4)\right] = 0 \tag{3.4}$$

In order to make H_3 zero, two following trigonometric terms of Eq. (3.4) must be zero. Indeed, four switching angles in Figure 3.3 are selected to have even number of trigonometric terms in harmonic amplitudes, which can neutralize each other.

$$\begin{cases} \cos(3\alpha_1) + \cos(3\alpha_2) = 0 \\ \cos(3\alpha_4) - \cos(3\alpha_3) = 0 \end{cases} \tag{3.5}$$

Considering trigonometric equation $cos(x)=-cos(y)$, it a has general solution as $x=2K\pi\pm(\pi-y)$, then, two general solutions for above trigonometric functions of Eq. (3.5) are derived as:

$$\begin{cases} \alpha_1 = \dfrac{(2K \pm 1)\pi}{3} \pm \alpha_2 \\ \alpha_3 = \dfrac{(2K)\pi}{3} \pm \alpha_4 \end{cases} \tag{3.6}$$

Where, K is an integer parameter. Naturally, various relations are achieved for different values of K, but, the only valid value is $K=1$. It is because of the fact that the obtained angles constraint for other values of K violates the principle angles condition ($0<\alpha_1<\alpha_2<\alpha_3<\alpha_4<\pi/2$). Therefore, the following equations have been chosen as new angles constraint:

$$\begin{cases} \alpha_1 + \alpha_2 = \dfrac{\pi}{3} \\ \alpha_3 + \alpha_4 = \dfrac{2\pi}{3} \end{cases} \tag{3.7}$$

Moreover, the combination of trigonometric terms was assumed in Eq. (3.5) in such a way that it has been resulted in angles constraint of Eq. (3.7) to have higher possibility for solving SHE equations with respect to basic angles condition ($0<\alpha_1<\alpha_2<\alpha_3<\alpha_4<\pi/2$). For instance, if the combination of trigonometric terms as $cos(3\alpha_1)- cos(3\alpha_3)=0$ and $cos(3\alpha_2)+ cos(3\alpha_4)=0$ had been supposed in Eq. (3.5) to acquire angles constraint, the corresponding angles constraint for this combination would have obtained as $\alpha_1+ \alpha_3=2\pi/3$ and $\alpha_2+ \alpha_4=\pi/3$ that there was no chance to calculate switching angles.

Because, α_1 and α_3 should have value more than $\pi/3$ while α_2 and α_4 must be less $\pi/3$ and this is against condition $0<\alpha_1<\alpha_2<\alpha_3<\alpha_4<\pi/2$. Therefore, the acquired angles constraint for self-elimination of triplen harmonics in single-phase SHE technique must be always validated with basic angles constraint. Afterwards, the harmonics amplitude formula can be rewritten based on two switching angles using attained constraint. The new formulation for harmonics amplitude is provided in Eq. (3.8) substituting two terms ($\alpha_2=\pi/3-\alpha_1$) & ($\alpha_4=2\pi/3-\alpha_3$) into Eq. (3.3).

$$H_n = \frac{8E}{n\pi}\left(\cos(n\ \frac{\pi}{6})\ \cos(n(\alpha_1 - \frac{\pi}{6})) - \sin(n\ \frac{\pi}{3})\ \sin(n(\alpha_3 - \frac{\pi}{3})) \right) \tag{3.8}$$

Triplen harmonics cancellation can be confirmed by the existence of two trigonometric terms ($cos(n\pi/6)$ & $sin(n\pi/3)$) in which these two terms have zero value for $n=3, 9, 15, \ldots$ and then H_{3n} will be zero. By elimination of triplen amplitudes, single-phase SHE equations will be

modified to contain only non-triplen ones. Hence, the proposed single-phase SHE technique derived from harmonic amplitude formula of Eq. (3.8) would be as Eq. (3.9).

$$\begin{cases} H_1 = \frac{8E}{\pi}\left(\cos(5\frac{\pi}{6})\cos(\alpha_1-\frac{\pi}{6})-\sin(5\frac{\pi}{3})\sin(\alpha_3-\frac{\pi}{3})\right)=m_a \\ H_5 = \frac{8E}{5\pi}\left(\cos(5\frac{\pi}{6})\cos(5(\alpha_1-\frac{\pi}{6}))-\sin(5\frac{\pi}{3})\sin(5(\alpha_3-\frac{\pi}{3}))\right)=0 \\ H_7 = \frac{8E}{7\pi}\left(\cos(7\frac{\pi}{6})\cos(7(\alpha_1-\frac{\pi}{6}))-\sin(7\frac{\pi}{3})\sin(7(\alpha_3-\frac{\pi}{3}))\right)=0 \\ 0<\alpha_1<\alpha_3<\pi/2 \end{cases} \tag{3.9}$$

3.3 Voltage THD Analysis for Switching Angles Calculations in Five-level Voltage

THD has been defined as reliable criterion to evaluate power quality of output voltage in terms of proportion between undesired harmonics and the desire fundamental voltage. Although different methods exist to calculate THD, the most prevalent formulation is the root sum square of harmonics amplitudes (both triplen and non-triplen) divided by the first harmonic amplitude as Eq. (3.10).

$$THD = \frac{\sqrt{\sum_{n=3,5,\ldots}^{\infty} H_n^2}}{H_1} \tag{3.10}$$

In this section, voltage THD has been analyzed to investigate the possibility of calculating optimum value for switching angles to minimize THD. Unlike SHM technique in which THD formula is assumed in its cost function to be mitigated beside harmonic amplitudes, it cannot be involved in SHE and consequently remains uncontrolled. This is due to the fact that the conventional SHE is not flexible to eliminate amplitudes more than number of angles. Indeed, the goal of switching angles calculations in conventional SHE technique is to eliminate only low harmonic orders and THD is remained uncontrolled since there is no control on non-eliminated harmonics. However, THD can be analyzed in the improved single-phase SHE technique in a way that the angles would be calculated to optimize THD. In this case, switching angles in modified single-phase SHE equations are computed inside

specific ranges. Those ranges are achieved from voltage THD analysis where it would have lower value. To find the optimum range for switching angles values, the new harmonic amplitudes formula (Eq. (3.8)) should be substituted into THD formula (Eq. (3.10)). Thus, the analyzable THD formula for the proposed modified single-phase SHE technique of Eq. (3.9) will be expressed using only two angles (α_1 & α_3) as Eq. (3.11):

$$THD = \frac{\sqrt{\sum_{n=3,5,\dots}^{\infty} \left[\frac{8E}{n\pi} \left(\cos(n\frac{\pi}{6}) \cos(n(\alpha_1 - \frac{\pi}{6})) - \sin(n\frac{\pi}{3}) \sin(n(\alpha_3 - \frac{\pi}{3})) \right) \right]^2}}{\frac{8E}{\pi} \left(\cos(\frac{\pi}{6}) \cos(\alpha_1 - \frac{\pi}{6}) - \sin(\frac{\pi}{3}) \sin(\alpha_3 - \frac{\pi}{3}) \right)} \quad (3.11)$$

Expressing THD based on two switching angles in Eq. (3.11) makes it possible to depict its figure in 3D-waveform. Thus, the area that THD has minimum value can be found to specify the desired range for calculating optimum angles. Therefore, THD is controllable in the modified single-phase SHE through obtaining optimum switching angles. Figure 3.4 illustrates X-Z, 3D X-Y-Z and Y-Z views of THD in terms of two angles. X-Z and Y-Z views (Figure 3.4 (a) & (c)) depict THD regarding to angles α_1 and α_3, respectively. As it is illustrated in Figure 3.4 (a) & (c), THD with less than *0.3* has been indicated with dotted circle. Besides, THD has negative value for $0<\alpha_1<\pi/2$ and $0<\alpha_3<0.5$ that is not acceptable. Figure 3.4 (d) provides X-Y view of THD waveform to demonstrate the valid range for acquiring optimum values for two angles in which THD has value less than *0.3*. The specified area in Figure 3.4 (d) distinguished by dotted circle (named as *A*) demonstrates the section with highest possibility of calculating optimum angles with respect to the angles condition of Eq. (3.7). The THD is positive and less than *0.3* in this determined area. Therefore, two limitation for switching angles range are $0<\alpha_1<0.5$ and $0.5<\alpha_3<1$ regarding to Figure 3.4 (d) that can be assumed in the proposed single-phase SHE equations (Eq. (3.9)) to minimize THD. Optimum values for two switching angles (α_1 & α_3) are calculated solving proposed SHE equations and considering the mentioned range for angles ($0<\alpha_1<0.5$, $0.5<\alpha_3<1$). The other two angles (α_2 & α_4) are computed according to the switching angles condition (Eq. (3.7)). Figure 3.5 plots calculated optimum switching angles found for modulation index $1.9<m_a<2.1$.

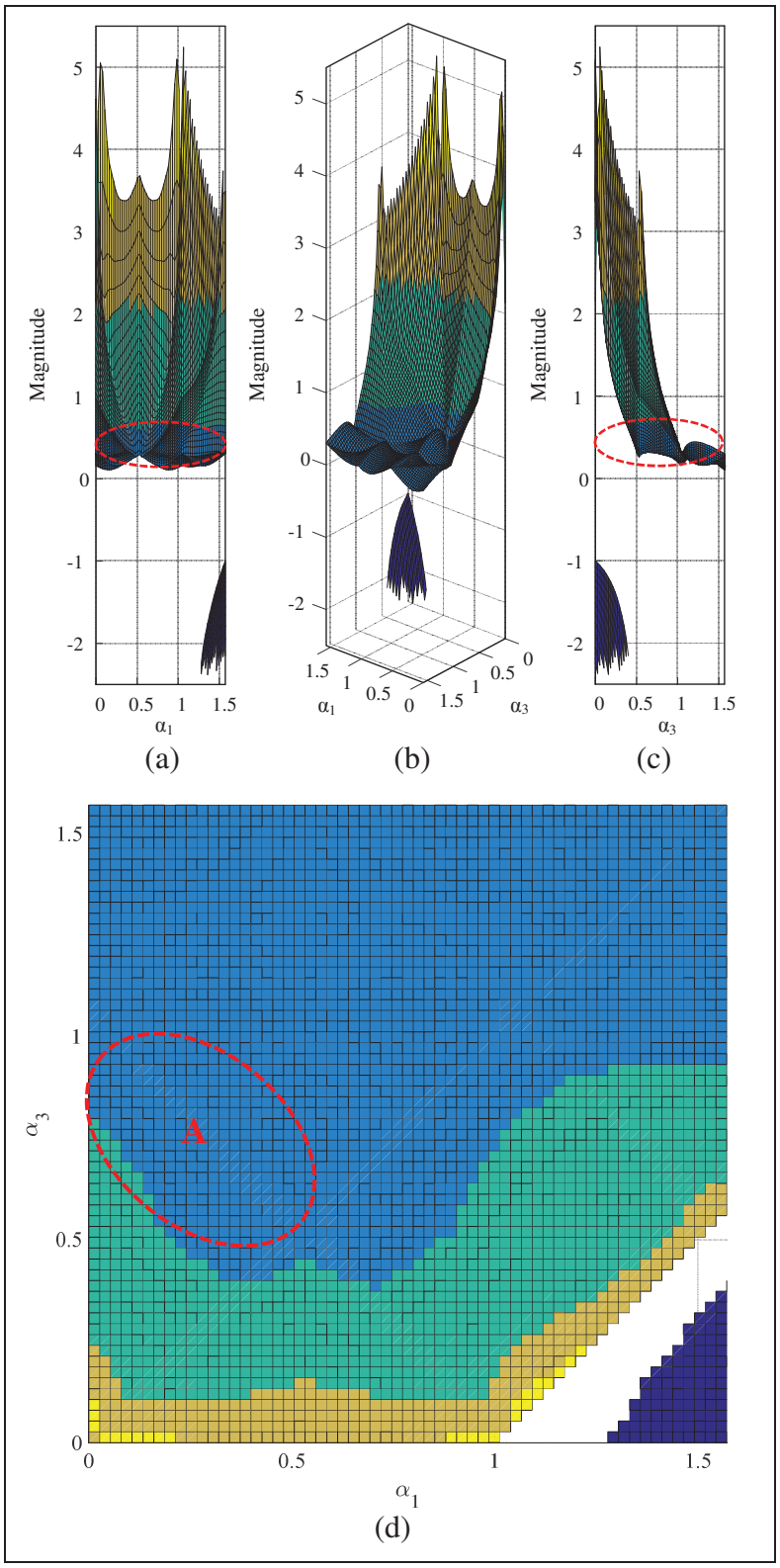

Figure 3.4 3D waveform of THD, (a) X-Z view, (b) Original view, (c) Y-Z view, (d) X-Y view

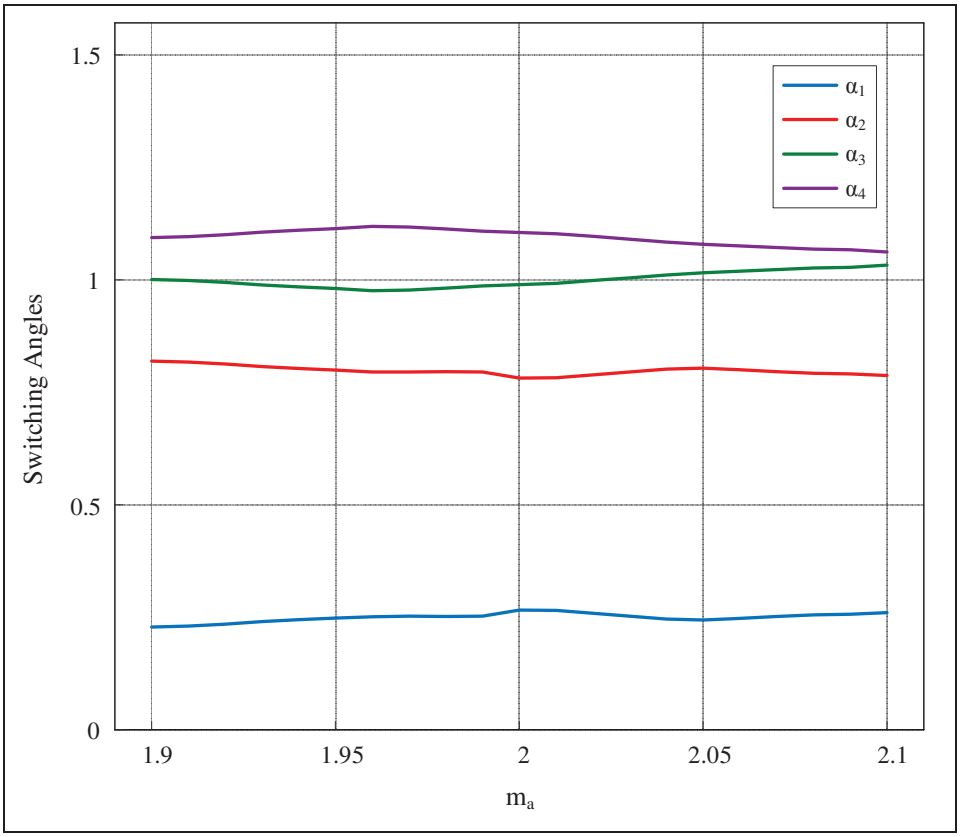

Figure 3.5 Obtained optimum switching angles

Moreover, the worst case of triplen and non-triplen amplitudes in order range of 3rd to 49th have been compared with conventional SHE to demonstrate the better performance of proposed SHE in terms of controlling harmonic amplitudes. In conventional single-phase SHE, three harmonics (*3rd*, *5th* and *7th*) are eliminated by four angles and first non-eliminated order is *9th*; while in the presented SHE, all triplen amplitudes and non-triplen ones of 5th and 7th are completely removed and first non-eliminated harmonic is *11th*. Therefore, the modified SHE eliminates more harmonics with same switching frequency of conventional technique because of using the proposed angles constrain. Figure 3.6 (a) & (b) depict worst case scenario of triplen and non-triplen harmonics; respectively, obtained for the mentioned range of modulation index (*1.9<ma<2.1*). As can be seen, all triplen amplitudes are eliminated while they have notable magnitude in conventional technique. Moreover, calculation of optimum value for switching angles not only has led to minimize THD but also controlled the amplitude of non-eliminated harmonics. Actually, the optimization of THD is

occurred because the amplitudes of higher harmonic orders are controlled. According to the Figure 3.6 (a), the non-eliminated harmonics amplitudes of proposed SHE are remarkably less than the conventional method. This is obvious from a comparison of first non-eliminated non-triplen amplitude (11^{th}) left uncontrolled in conventional single-phase SHE.

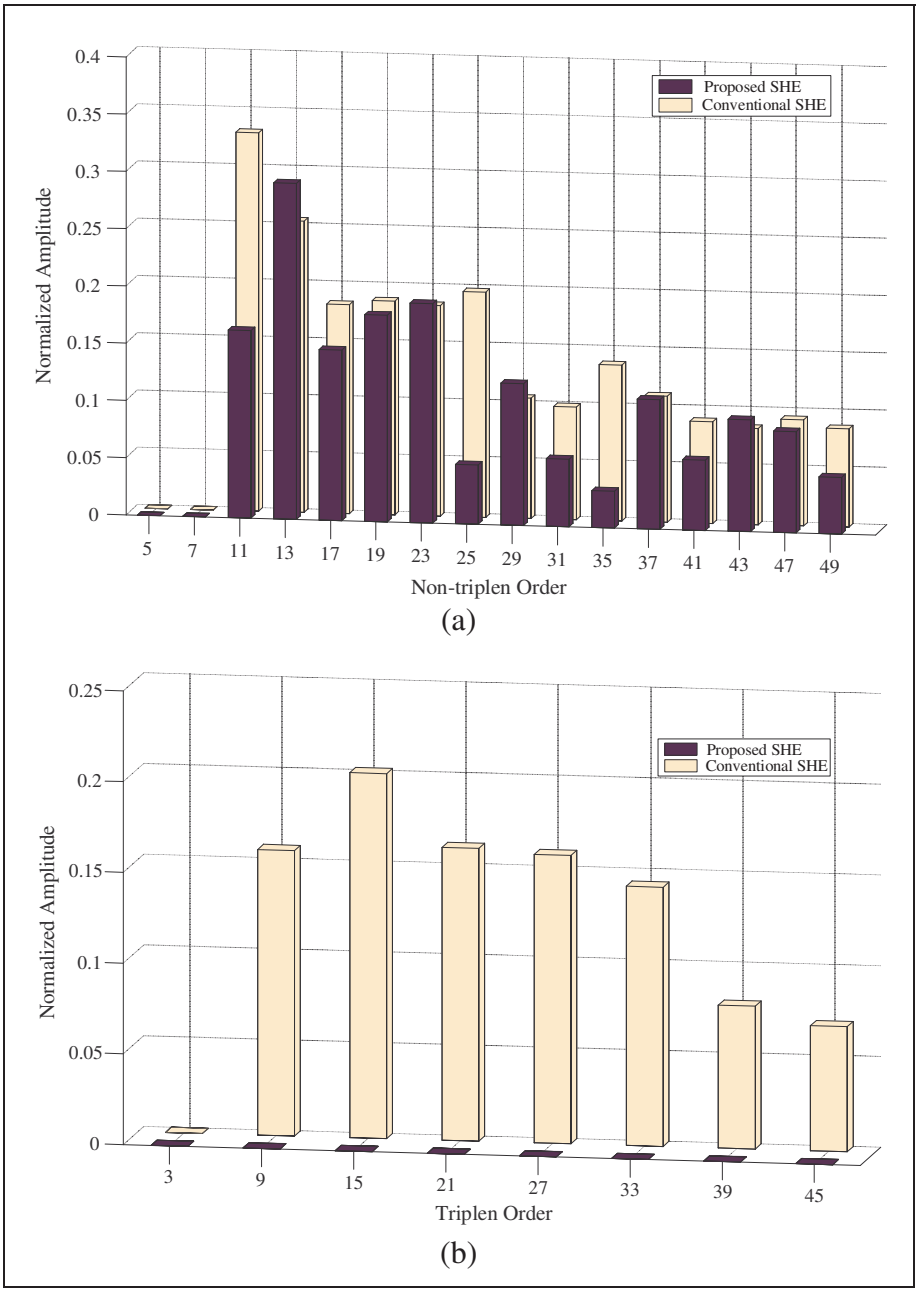

Figure 3.6 Worst case harmonic amplitudes of conventional and proposed SHE techniques (a) Non-triplen orders, (b) Triplen orders

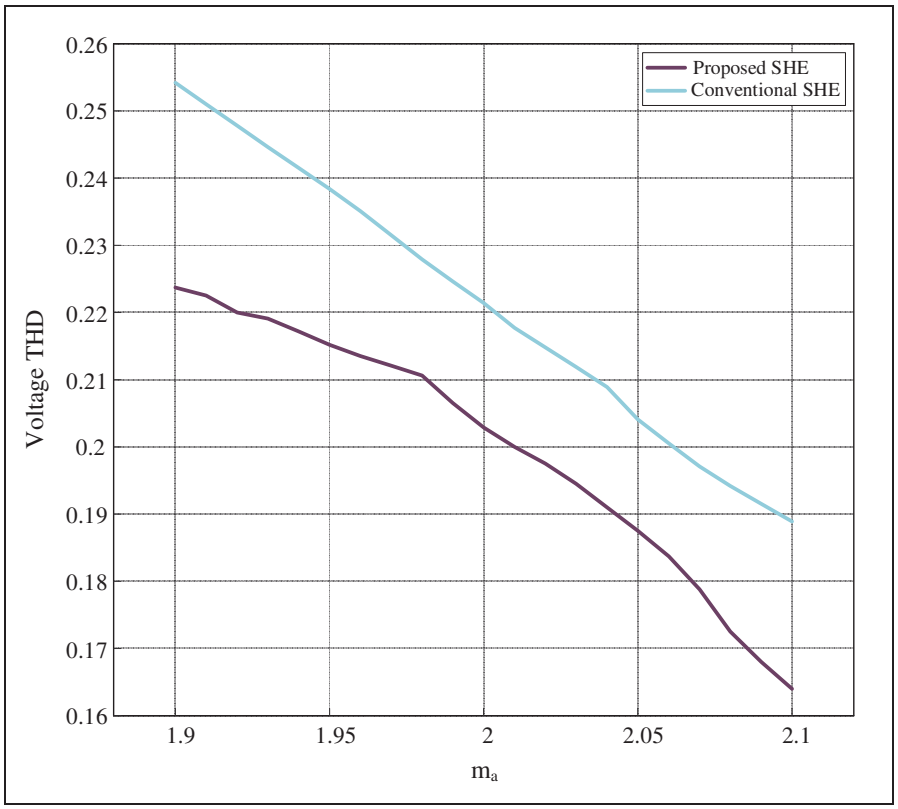

Figure 3.7 Voltage THD of single-phase conventional and proposed SHE techniques

In normal operation of single-phase SHE, higher triplen harmonic orders (including 9^{th} and higher orders) are remained uncontrolled, but, in the modified SHE all triplen harmonics are accurately suppressed. So, the proposed technique could lead to significant improvement of harmonic distortion for single-phase inverter. This is also confirmed by comparison of THD value in conventional and proposed SHE as shown in Figure 3.7. THD is calculated for harmonic orders 3^{rd}-to-49^{th}, the reduced amount in THD is a result of eliminating all triplen harmonics and controlling higher non-triplen ones.

3.4 Triplen Harmonic Cancellations for Higher Level Voltage Waveforms

The proposed method of obtaining angle constraint led to cancelation of all triplen orders is also valid for other multilevel voltage waveform than five-level one. Since there is no general amplitude formula for a typical multilevel voltage, the second example of presented procedure has been applied on seven-level voltage waveform. Figure 3.8 shows the proposed

seven-level voltage with four angles to eliminate all triplen harmonics. The associated harmonic amplitude formula of Figure 3.8 is written in Eq. (3.12).

$$H_n = \frac{4E}{n\pi}\left[\cos(n\alpha_1) + \cos(n\alpha_2) + \cos(n\alpha_3) + \cos(n\alpha_4)\right] \tag{3.12}$$

Similar to five-level voltage, number of switching angles is considered even in seven-level voltage of Figure 3.8 to have even number of trigonometric terms in corresponding harmonic amplitude that can neutralize each other. Thus, angles constraint harmonics is obtained equating the first triplen amplitude to zero as:

$$H_3 = \frac{4E}{3\pi}\left[\cos(3\alpha_1) + \cos(3\alpha_2) + \cos(3\alpha_3) + \cos(3\alpha_4)\right] = 0 \tag{3.13}$$

In this case, two following trigonometric terms must be separately set to zero to solve Eq. (3.13) and eliminate triplen harmonics.

$$\begin{cases} \cos(3\alpha_1) + \cos(3\alpha_3) = 0 \\ \cos(3\alpha_2) + \cos(3\alpha_4) = 0 \end{cases} \tag{3.14}$$

Consequently, two general solutions for Eq. (3.14) are:

$$\begin{cases} \alpha_3 = \dfrac{(2K \pm 1)\pi}{3} \pm \alpha_1 \\ \alpha_4 = \dfrac{(2K \pm 1)\pi}{3} \pm \alpha_2 \end{cases} \tag{3.15}$$

Various angles relations are obtained for different values of K. However, the angles relations must be checked by primary switching angles condition ($0<\alpha_1<\alpha_2<\alpha_3<\alpha_4<\pi/2$) to find the valid one. In this case, the angles relation for elimination of all triplen harmonics in seven-level voltage is achieved as:

$$\begin{cases} \alpha_1 + \alpha_3 = \dfrac{\pi}{3} \\ \alpha_4 - \alpha_2 = \dfrac{\pi}{3} \end{cases} \tag{3.16}$$

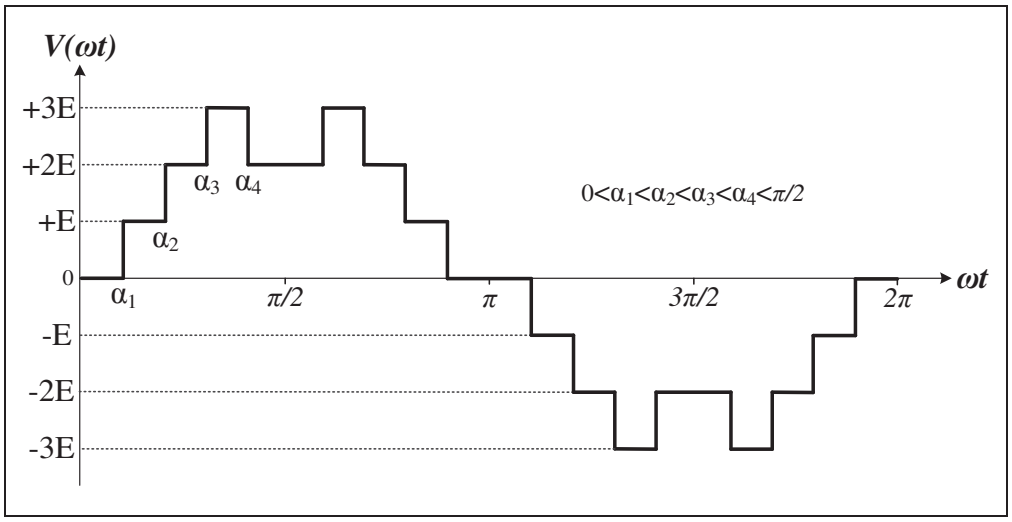

Figure 3.8 Proposed seven-level voltage waveform for single-phase inverter

The new harmonic amplitude formula can be defined with respect to Eq. (3.16) substituting two terms of ($\alpha_3=\pi/3-\alpha_1$) and ($\alpha_4=\pi/3+\alpha_2$) into Eq. (3.12) as:

$$H_n = \frac{8E}{n\pi}\cos(n\frac{\pi}{6})\left(\cos(n(\alpha_1 - \frac{\pi}{6})) + \cos(n(\alpha_2 + \frac{\pi}{6}))\right) \quad (3.17)$$

The cancelation of triplen amplitudes is confirmed by trigonometric term, $cos(n\pi/6)$ in Eq. (3.17). Afterwards, the related single-phase SHE equations for seven-level voltage of Figure 3.8 can be defined based on the new harmonic amplitude formula of Eq. (3.17).

3.5 Results Discussion

In this section some experimental results have been presented to evaluate the performance of the proposed SHE-PWM with elimination of triplen harmonics on single-phase MPUC inverter. MPUC prototype has been built in the laboratory and controlled by real time controller dSpace 1103. The parameters values used in experimental tests are listed in Table 3.2. Switching frequency (f_S) is also obtained through multiplying number of pulses (N) by fundamental frequency (f) as $f_S=N.f$. The pulses for MPUC switches are produced with respect to the proposed SHE technique and using the switching states *1, 2, 4, 7* and *8* of Table 3.1. Then, considering fundamental frequency as shown in Table 3.2 equal to *50 Hz*,

the switching frequency is *150 Hz* for two upper switches (T_1 & T_4), *50 Hz* (equal to fundamental frequency) for two middle switches (T_2 & T_5) and *250 Hz* for two lower switches (T_3 & T_6). Figure 3.9 shows output five-level voltage and load current waveforms with voltage harmonic spectrum when the MPUC inverter supplies R-L linear load and modulation index is selected *2*. According to the five-level voltage FFT analysis, in addition to the harmonic orders 5^{th} and 7^{th}, all triplen amplitudes have been completely eliminated. First non-eliminated harmonic order is 11^{th} and its amplitude has been controlled because of calculating optimum angles led to minimize THD.

Table 3.2 Utilized Parameters Characteristics for Single-Phase MPUC

DC sources voltage	100 V
Fundamental frequency	50 Hz
Load resistance (R)	40 Ω
Load reactance (L)	20 mH
Rectifier DC side load (R_{dc}, L_{dc})	80 Ω, 50 mH

Due to the cancellation of all triplen harmonics, this technique has also capability of dealing with nonlinear loads as well as linear ones. A single-phase diode rectifier has been considered as typical nonlinear harmonic load connected to the linear R-L load in parallel. Figure 3.10 shows experimental results of voltage and current of single-phase MPUC inverter when it is feeding both linear and nonlinear loads and modulation index is *2*. In this case, the single-phase five-level inverter is supplying linear load and parallel diode rectifier is connected and disconnected for some periods. As it is shown, there are no transient changes in the voltage and current waveforms during connection and disconnection of nonlinear load. The experimental results validate the accurate performance of proposed SHE for elimination of mentioned harmonics in real-time implementation.

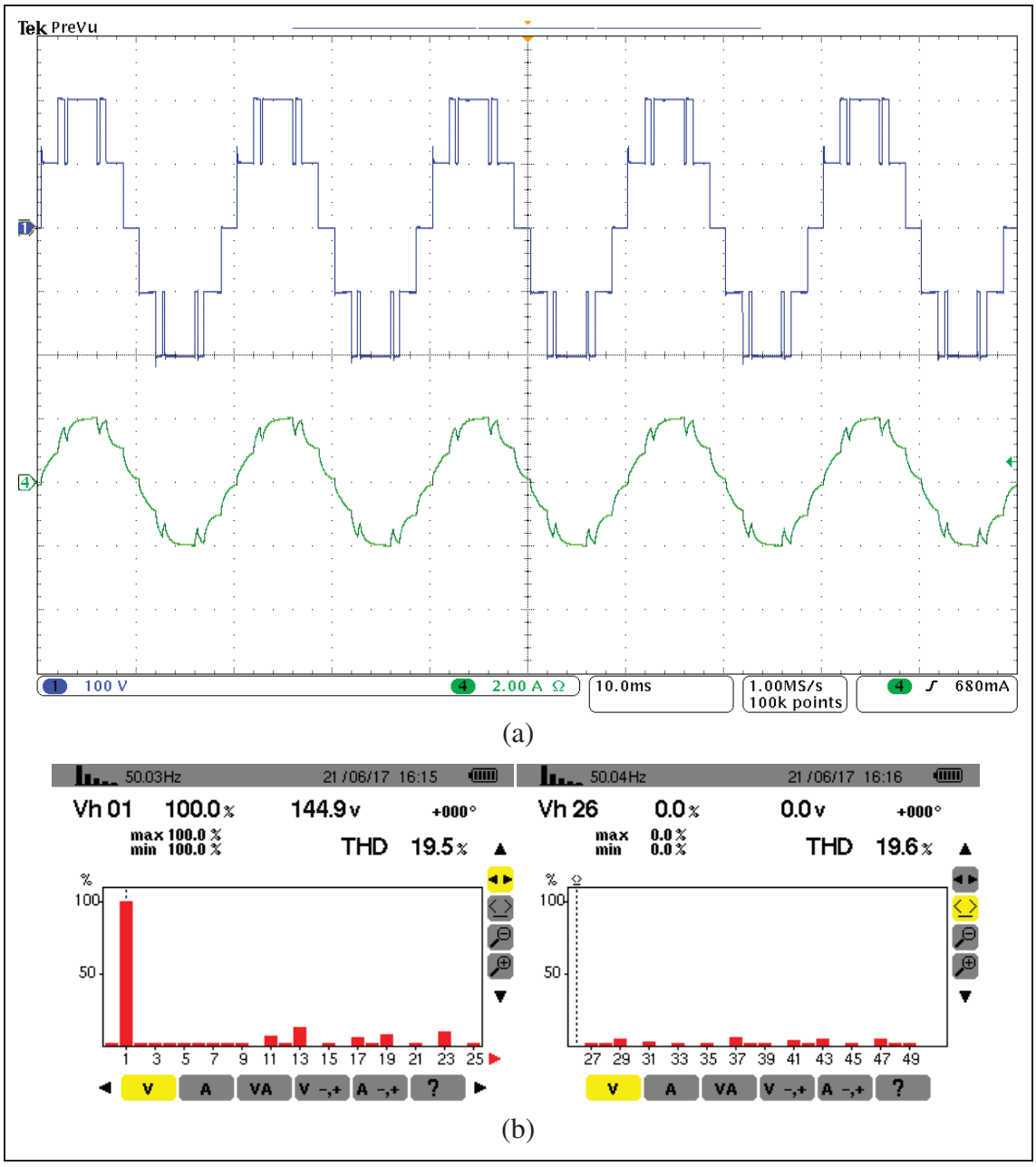

Figure 3.9 Experimental results of five-level voltage and current waveforms with voltage harmonic content of single-phase MPUC inverter, (a) voltage and current waveforms (b) voltage harmonic spectrum

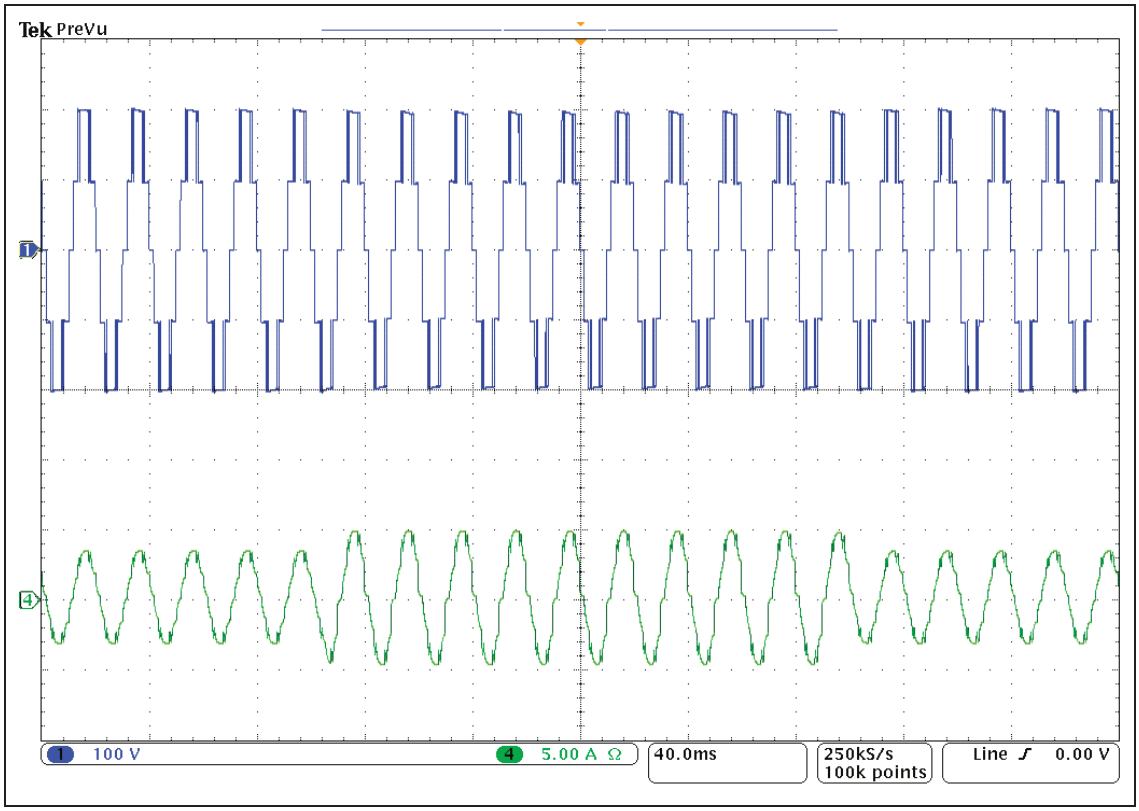

Figure 3.10 Experimental results of voltage and current of
single-phase MPUC inverter when it is supplying linear and nonlinear loads

3.6 Conclusions

The new switching angles constraint has been presented for single-phase SHE-PWM to eliminate all triplen harmonics inherently. Due to cancellation of triplen orders, they are no longer forced to presume in single-phase SHE equations which results in less complexity of angles calculations. The specified non-triplen harmonic amplitudes are eliminated to find switching angles values in normal operation of SHE. As well, the modified SHE has been analyzed from THD point of view to calculate optimum value for angles and acquire minimum THD. Thus, not only more harmonics have been eliminated compared to the conventional single-phase SHE-PWM with same switching frequency ratio, but also the amplitude of non-eliminated harmonics have been controlled. The presented SHE-PWM has been accomplished in five-level voltage waveform; however, it can be extended for all type of multilevel voltage waveform with even number of angles. The elimination of all triplen

harmonics enables the single-phase MPUC inverter to deal with both linear and harmonic loads which has been confirmed by experimental results. So, it would be highly suitable to adjust the designed technique in single-phase UPS applications where different types of loads are connected.

CHAPTER 4

COMPATIBLE SELECTIVE HARMONIC ELIMINATION FOR THREE-PHASE FOUR-WIRE NPC INVERTER WITH DC-LINK CAPACITOR VOLTAGE BALANCING

Mohammad Sharifzadeh [a], Gabriel Chouinard [b], Hani Vahedi [c], Kamal Al-Haddad [d]

[a, b, c, d] Department of Electrical Engineering, École de Technologie Supérieure,
1100 Notre-Dame West, Montreal, Quebec, Canada, H3C 1K3

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Abstract

In this work a Compatible Selective Harmonic Elimination (CSHE)-PWM is designed for three-leg four-wire (3L/4W) Neutral Point Clamped (NPC) inverter. The proposed CSHE-PWM is capable of eliminating both triplen and non-triplen harmonics from phase voltages and empowers 3L/4W NPC to handle both single/three-phase and linear/nonlinear loads. It has been mathematically proved that DC capacitors self-voltage balancing is achieved thanks to direct control of phase voltage waveform symmetry. Moreover, the cancellation of specified triplen and non-triplen orders has the advantage of having low capacitors voltage ripple. Therefore, the applied technique not only helps removing one leg of the inverter that reduces associate complex calculations and switching losses, but also directly controls phase voltage harmonic profile compared to SHE-PWM for four-leg four-wire (4L/4W) NPC. CSHE-PWM is practically tested on a NPC inverter prototype to validate the efficient harmonic elimination from the phase voltage waveforms along with capacitors voltages balancing under symmetrical/asymmetrical loads.

4.1 Introduction

Among various multilevel inverters, four-wire configuration of Neutral Point Clamped (NPC) is suitable to adjust in high power standalone industrial applications like Uninterruptible Power Supply (UPS) in which both single and three-phase loads should be fed independently and simultaneously (Vahedi, Labbe et Al-Haddad, 2016; Dai, Wong et Han, 2006). Four-leg four-wire (4L/4W) NPC inverter provides the neutral wire via middle point of fourth leg so it can control neutral current and unbalanced loads (Rojas et al., 2017). Since 4L/4W NPC has the particular configuration, it requires a complicated control strategy. Several high switching frequency modulation and control based techniques have been reported in the literature to control 4L/4W NPC and keep the phase voltage and current waveforms balanced and identical under both symmetrical and asymmetrical loads conditions (Wang, Zhang, et Xie, 2018; Yaramasu et al., 2013). However, 4L/4W NPC inverter needs to be controlled by a low switching frequency technique to decrease power losses generated by those extra power switches of the fourth leg (Kim, Sul, et Enjeti, 2008; Lohia et al., 2008; Ceballos et al., 2008).

Selective Harmonic Elimination (SHE)-PWM is a promising low switching frequency technique that accurately generates the devices gating pulses (Dahidah, Konstantinou, et Agelidis, 2015). SHE is established by set of nonlinear trigonometric type of equations acquired from Fourier series decomposition of a preprogramed voltage waveform defined by selected switching angles (Yang et a., 2016). The primary concerns regarding to the SHE-PWM is to precisely calculate switching angles (Yang et al., 2018), considering other parameters effects (Haghdar et Shayanfar, 2018), improving its conventional performance through employing new algorithm or combing with other control strategy (Zhao et Wang, 2017; Sanchez-Ruiz et al., 2017; Gao et al., 2017). In recent years, it has been appeared as an appealing modulation technique for some power converters applications due to the low switching frequency feature and accurate control on voltage/current harmonic content (He et al., 2018; Aleenejad et al., 2016; Pérez-Basante et al., 2018; Zhao, Wang et Moeini, 2019).

In (Zhang et Yan, 2009) SHE-PWM was presented to define for 4L/4W two-level inverter according to the phase voltage harmonic content and then it was extended for three-level one in (Sharifzadeh, 2016a). In the proposed scheme, the pulses of main legs are generated to eliminate the specified non-triplen harmonics and fourth leg suppresses determined triplen ones which is necessary in supplying asymmetrical loads. Although the proposed SHE for 4L/4W inverter could precisely control low harmonics orders, it does not achieve direct control on non-eliminated harmonics amplitudes particularly triplen ones in phase voltage. In (Sharifzadeh, 2015) Selective Harmonic Mitigation (SHM)-PWM has been combined with SHE and implemented on a 4L/4W NPC inverter to improve harmonic content. While SHM was applied on main legs to mitigate non-triplen harmonics, the fourth leg switching pattern is designed by SHE to eliminate triplen ones. However, the harmonic distortion of phase voltage was still high in (Sharifzadeh, 2015) due to the non-eliminated triplen harmonics amplitudes. Indeed, fundamental frequency of fourth leg needs to be three times greater than the main legs in (Zhang et Yan, 2009; Sharifzadeh, 2016b; Sharifzadeh, 2015), so as SHE patterns can produce only triplen harmonics to indirectly neutralize the specified triplen amplitudes of phase voltages. But it also leads to unwantedly amplify the non-eliminated triplen orders and consequently increase phase voltage THD (Sharifzadeh, 2016a).

Three-leg four-wire (3L/4W) NPC inverter is another four-wire configuration that provides natural access via middle point of DC-link capacitors and so the fourth leg is no longer required (Vodyakho et Kim, 2009; Wang, Si, et Xin, 2016; Srikanthan et Mishra, 2010; Luo, Loo, et Lai, 2016; Vodyakho et Mi, 2009). In comparison to 4L/4W NPC inverter, 3L/4W topology is more economical solution for creating four-wire inverter. The obvious superiority of 3L/4W over 4L/4W is the lower number of power switches which reduces the manufacturing cost and size as well as switching power losses (Dai, Wong et Han, 2006). Such factors are matters of importance leaning toward choosing the suitable four-wire inverter for high power UPS applications (Rojas et al., 2017). Moreover, there would be less complexity to scheme a switching method for 3L/4W compared to 4L/4W one. However, the associated modulation technique should be appropriately designed to balance DC-link capacitors voltages with low ripple; so as 3L/4W NPC inverter is empowered to handle

asymmetrical loads. As the neutral current collected by phase currents directly flows into the DC-link, capacitors voltages ripple will be significantly increased if the harmonic distortion of phase voltages is not controlled. Thus, the harmonic orders particularly triplen ones need to be properly suppressed in phase voltages to regulate DC capacitors voltages ripple (Luo, Loo, et Lai, 2016; Vodyakho et Mi, 2009; Maheshwari, Munk-Nielsen, et Busquets-Monge, 2013). As a result, 3L/4W NPC can deal with unbalanced loads as strong as 4L/4W NPC while the capacitors voltages ripples are kept low (Wang, Si, et Xin, 2016; Srikanthan et Mishra, 2010; Luo, Loo, et Lai, 2016; Vodyakho et Mi, 2009; Maheshwari, Munk-Nielsen, et Busquets-Monge, 2013; Tafti et al., 2016).

In this work, a compatible SHE (CSHE)-PWM control strategy is presented to apply for 3L/4W NPC inverter and overcome normal SHE drawbacks for fourth leg switching patterns as mentioned above. The proposed CSHE-PWM makes use of low switching frequency ratio to keep DC-link capacitors voltages balanced in sensor-less approach with low ripple so 3L/4W NPC can properly deal with linear/nonlinear single/three-phase loads. Since the branch and phase voltages are equal in 3L/4W NPC, the latter's exhibit same harmonic content. Consequently, specific harmonic orders will be removed from phase voltages if they are eliminated in branch voltages as imply by mathematical equations. Since both triplen and non-triplen harmonics must be controlled in phase voltages, they are considered in the CSHE equations derived from predetermined three-level branch voltage waveform to be simultaneously suppressed. By performing mathematical analysis on DC-link capacitors voltages, it is proved that CSHE-PWM keeps the phase voltage waveform symmetrical; so, DC capacitors are equally charged and discharged and would be balanced to the desired level. Also, the cancelation of low order triplen and non-triplen harmonics leads to reduce capacitors voltages ripple. Since CSHE directly suppresses both triplen and non-triplen orders in phase voltage of 3L/4W NPC, the non-eliminated higher harmonics orders are not amplified compared to the SHE for 4L/4W NPC. Moreover, CSHE has less complexity of angles calculations unlike the SHE for 4L/4W NPC where two different set of equations need to be separately solved for main and fourth legs. In section 4.2 normal SHE and proposed CSHE techniques are formulized for 4L/4W and 3L/4W NPC inverters, respectively.

Harmonic content and switching power losses analysis is done in section 4.3 to prove the superiority of CSHE for 3L/4W NPC. Experimental results are discussed in section 4.4 to evaluate the performance of 3L/4W NPC under different load conditions when it is controlled by CSHE.

4.2 SHE-PWM for 4L/4W and 3L/4W NPC Topologies

In this section, SHE for 4L/4W NPC presented in (Sharifzadeh, 2016a) is firstly explained. Then, SHE is compatibly designed as CSHE for 3L/4W NPC to handle symmetrical/asymmetrical loads with further efficiency compared to SHE for 4L/4W NPC.

4.2.1 SHE-PWM for 4L/4W NPC Inverter

Figure 4.1 shows 4L/4W configuration of NPC inverter. All four legs are identical in number of components and switching state possibility. So, the same number of voltage levels is generated between middle point of each leg (*A, B, C & N*) and middle point of DC-link (*g*) named as branch voltages (V_{Ag}, V_{Bg}, V_{Cg} & V_{Ng}). Figure 4.2 depicts a predefined three-level branch voltage with quarter wave symmetry. Using Fourier analysis, the branch voltage and harmonics amplitudes (H_n) are expressed as:

$$\begin{cases} V(t) = \sum_{n=1}^{\infty} (H_n \sin(n\omega t)) \\ H_n = \dfrac{4E}{n\pi} \sum_{i=1}^{k} (-1)^{i+1} \cos(n\alpha_i) \quad \forall n = 1,3,5,7,\ldots \end{cases} \tag{4.1}$$

The phase voltages of 4L/4W NPC measured across the output loads (V_{An}, V_{Bn} & V_{Cn}) are also written with respect to the branch voltages as follows:

$$V_{xn} = V_{xg} - V_{Ng} \quad \forall\, x = A,\ B\ \&\ C \tag{4.2}$$

In order to keep phase voltages balanced under different loads conditions, SHE for 4L/4W NPC is defined to cancel both triplen and non-triplen harmonics of phase voltages (Zhang et

Yan, 2009; Sharifzadeh, 2016a). Since phase voltages depend on branch voltages as shown in Eq. (4.2), SHE cannot be directly applied on phase voltages. Indeed, SHE equations are derived from branch voltages of main and fourth legs and switching angles are found to eliminate determined triplen and non-triplen harmonics in phase voltages indirectly. According to SHE principle for main legs of 4L/4W NPC, switching angles of leg A are calculated to cancel specified non-triplen orders while first order is set to modulation index (m_a). The angles for leg B and C are attained using 120° phase shift of leg A's angles. So, SHE equations of leg A are derived based on its harmonics amplitude (H_n^A) using Eq. (4.1) as:

$$Leg(A):\begin{cases} H_1^A = \dfrac{4E}{\pi}\sum_{i=1}^{k}(-1)^{i+1}\cos(\alpha_i) = m_a \\ H_n^A = \dfrac{4E}{n\pi}\sum_{i=1}^{k}(-1)^{i+1}\cos(n\alpha_i) = 0 \;\; \forall n = 5,7,...q_1 \end{cases} \tag{4.3}$$

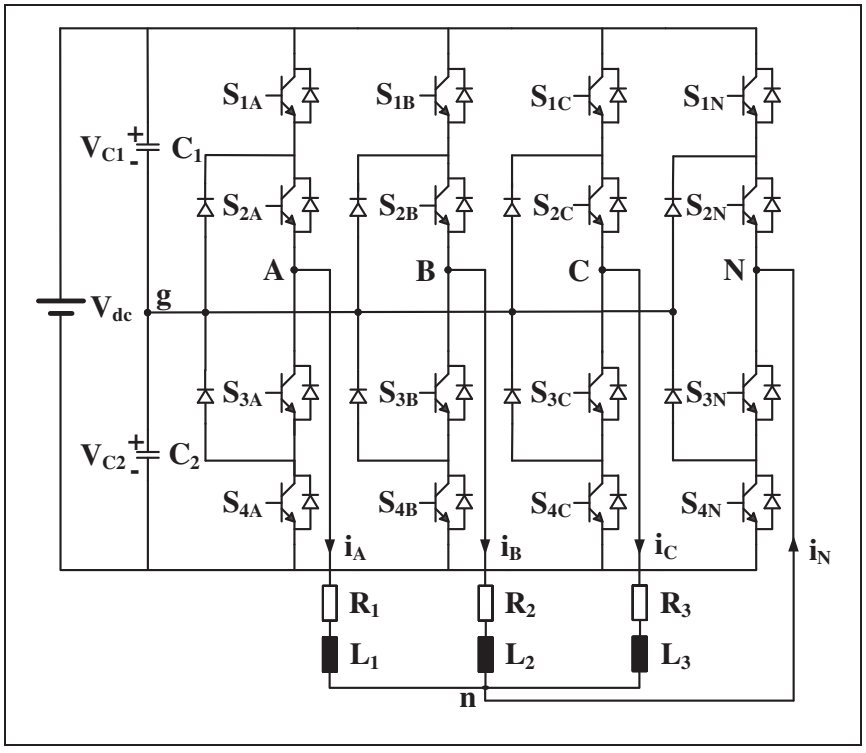

Figure 4.1 4L/4W NPC inverter configuration

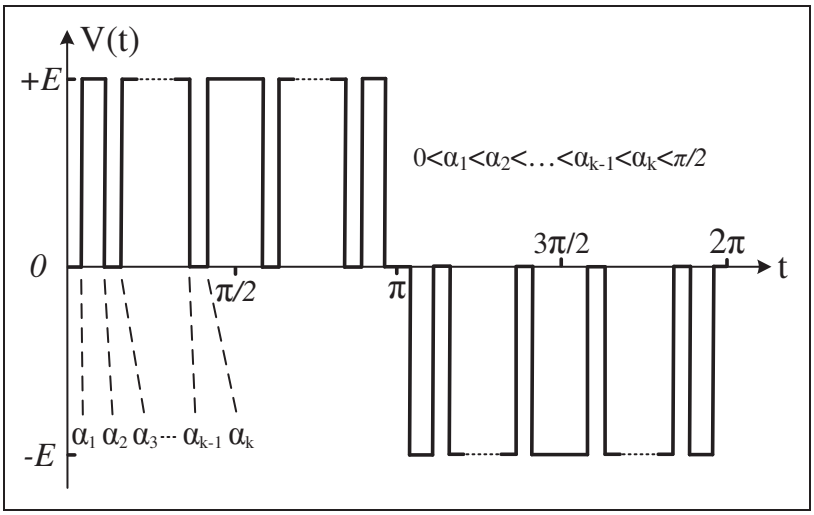

Figure 4.2 A typical three level of predefined branch voltage waveform

Also, SHE equations are established for leg N as triplen harmonics are produced to eliminate specified triplen harmonics of main legs. To this end, the voltage frequency of leg N is tripled to voltage frequency of main legs so as only triplen harmonics are generated ($f^N = 3f^A, then\ V_{Ng} = \sum_{n=1}^{\infty} H_n^N \sin(3n\omega t)$). Considering switching angles $\beta_1,\ldots,\beta_m$ in Eq. (4.1), SHE equations of fourth leg are defined equating harmonic amplitudes of leg N (H_n^N) to triplen harmonics of leg A (H_{3n}^A) as Eq. (4.4).

$$Leg(N):\begin{cases} H_n^N = \dfrac{4E}{n\pi}\sum_{j=1}^{m}(-1)^{j+1}\cos(n\beta_j) \\ H_n^N = H_{3n}^A \quad \forall\, n = 1,3,5,...q_2 \end{cases} \tag{4.4}$$

Therefore, the determined triplen and non-triplen harmonics are indirectly removed in phase voltages by calculating switching angles of leg A and N. This is verified by analyzing phase voltage harmonic content of leg A based on the Fourier decomposition of branch voltages of leg A and N as:

$$\begin{cases} V_{Ag} = H_1^A \sin(\omega t) + H_3^A \sin(3\omega t) + H_5^A \sin(5\omega t) + \ldots \\ V_{Ng} = H_1^N \sin(3\omega t) + H_3^N \sin(9\omega t) + H_5^N \sin(15\omega t) + \ldots \\ V_{An} = V_{Ag} - V_{Ng} = H_1^A \sin(\omega t) + (H_3^A - H_1^N)\sin(3\omega t) \\ + H_5^A \sin(5\omega t) + H_7^A \sin(7\omega t) + (H_9^A - H_3^N)\sin(9\omega t) + \ldots \end{cases} \tag{4.5}$$

As can be perceived from Eq. (4.5), specific non-triplen harmonics of phase voltage are eliminated by calculating leg A's angles. Certain triplen harmonics of phase voltage are removed by computing leg N' angles through subtracting $H_{3n}^{A} - H_{n}^{N}$. Number of eliminated harmonics in phase voltage depends on the number of angles for leg A and N. Parameters (q_1) and (q_2) are the highest eliminated non-triplen and triplen orders in phase voltages; respectively, attained with respect to the number of switching angles for leg A (k) and leg N (m) as:

$$\begin{cases} q_1 = 3k-1 & k \text{ is even} \\ q_1 = 3k-2 & k \text{ is odd} \\ q_2 = 6m-3 \end{cases} \tag{4.6}$$

Number of leg N's angles is also obtained based on the number of leg A's angles as Eq. (4.7).

$$m = \left\lceil \frac{k}{2} \right\rceil \tag{4.7}$$

4.2.2 Proposed CSHE-PWM for 3L/4W NPC Inverter

Although SHE empowers 4L/4W NPC to handle unbalanced loads by elimination of low triplen and non-triplen harmonics, it has some drawbacks related to the SHE operation on fourth leg as listed below:

I. As the specific triplen harmonics of phase voltages are removed through subtracting ($H_{3n}^{A} - H_{n}^{N}$), the non-eliminated triplen orders are intensified when $H_{3n}{}^{A}$ and $H_{n}{}^{N}$ have opposite signs that increase phase voltage THD.

II. SHE for 4L/4W NPC has a complex procedure as the switching angles of leg A and N are separately computed that increases the volume of calculations. It has been explained in (Sharifzadeh, 2016a) that it is not always guaranteed to solve fourth-leg's equations for all m_a.

III. The 4L/4W NPC has more power losses because of the extra leg. Besides, the fundamental frequency of leg N is tripled according to SHE principle that makes switching frequency inequality and further increases power losses.

Hence, SHE has compatibly designed as CSHE-PWM for 3L/4W NPC to overcome the aforementioned disadvantages of SHE-PWM for 4L/4W NPC that are because of switching pattern of fourth leg. CSHE not only empowers 3L/4W NPC to deal with symmetrical/asymmetrical loads, but also it has higher efficiency compared to SHE for 4L/4W NPC in terms of phase voltage harmonic content, switching power losses and complexity of angles calculations. Figure 4.3 depicts 3L/4W NPC inverter that the fourth wire is provided by connecting the neutral point of loads and middle point of DC-link. Since the common mode voltage is zero, the phase and branch voltages are equivalent as Eq. (4.8).

$$V_{xn} = V_{xg} \quad \forall\, x = A,\ B\ \ \&\ \ C \tag{4.8}$$

In order to understand how CSHE-PWM should be defined for 3L/4W NPC, the phase voltage of leg A is decomposed to specify its harmonic content. As the branch and phase voltages are equal in 3L/4W NPC, the harmonic content of V_{An} is obtained as Eq. (4.9) using Fourier analysis of V_{Ag}.

$$V_{An} = V_{Ag} = H_1^A \sin(\omega t) + H_3^A \sin(3\omega t) + H_5^A \sin(5\omega t) + \ldots \tag{4.9}$$

Eq. (4.9) implies that specific triplen and non-triplen harmonics are directly removed in the phase voltages of 3L/4W NPC if they are eliminated in branch voltages. Therefore, the CSHE equations for 3L/4W NPC are defined as Eq. (4.10) using harmonics amplitudes formula of V_{Ag} presented in Eq. (4.1) to contain both triplen and non-triplen harmonics.

$$\begin{cases} H_1^A = \dfrac{4E}{\pi} \displaystyle\sum_{i=1}^{k} (-1)^{i+1} \cos(\alpha_i) = m_a \\ H_n^A = \dfrac{4E}{n\pi} \displaystyle\sum_{i=1}^{k} (-1)^{i+1} \cos(n\alpha_i) = 0 \quad \forall\ n = 3,5,7,9,\ldots p_1 \end{cases} \tag{4.10}$$

According to CSHE-PWM for 3L/4W NPC, first harmonic is equal to m_a to generate desire fundamental component in output AC voltage and certain triplen harmonics along with non-triplen ones are set to zero to be removed in branch voltages and consequently phase voltages. The highest eliminated harmonic order (p_1) in phase voltages of 3L/4W NPC depends on the number of angles (k) and is obtained as:

$$p_1 = 2k - 1 \tag{4.11}$$

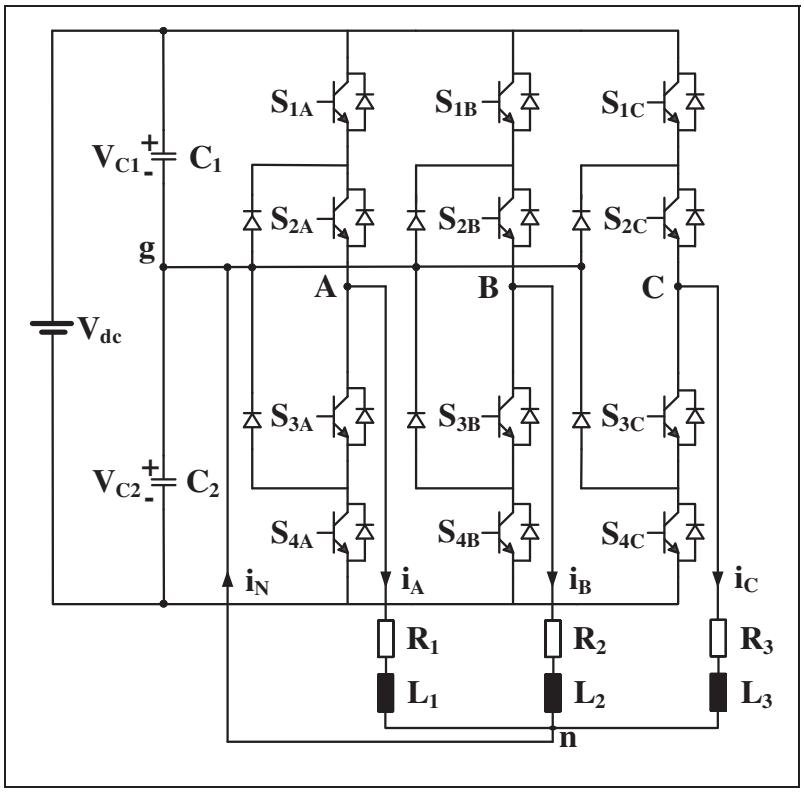

Figure 4.3 3L/4W NPC inverter configuration

As a result of direct triplen harmonics elimination in phase voltages of 3L/4W NPC through applying CSHE, the non-eliminated triplen harmonics of phase voltage are not amplified unlike in SHE for 4L/4W NPC. It is due to the fact that triplen orders are directly suppressed in CSHE while they are cancelled in normal SHE through subtracting $H_{3n}^{A} - H_{n}^{N}$ that can result in amplification of higher triplen harmonics if H_{3n}^{A} or H_{n}^{N} have opposite signs. The proposed CSHE has less complexity compared to SHE as the angles are obtained by solving

one set of equations. Moreover, the power losses is reduced in CSHE for 3L/4W NPC in comparison to SHE for 4L/4W NPC as the fourth leg and extra switches are omitted.

4.2.3 Regulation of Capacitor Voltage Ripple and Importance of Triplen and Non-Triplen Elimination in 3L/4W NPC Inverter

The crucial issue in designing a switching pattern for four-wire NPC inverter is to balance capacitors voltages with low ripple, so it is capable of handling asymmetrical loads. It is mathematically proved that CSHE-PWM regulates DC-link capacitors voltages in sensor-less approach and controls ripple by cancellation of low harmonics orders. Using Kirchhoff's current law at middle point of DC-link (g), the general capacitor voltage formula in 3L/4W NPC has been presented in (Zhang, Thomsen et Andersen, 2013) as Eq. (4.12).

$$V_c = \frac{-k_x}{2C}\int i_N . d\omega t \tag{4.12}$$

Where, V_c, C and i_N are capacitor voltage ripple, capacitor capacitance and neutral current; respectively. k_x indicates time ratio of switch pulsating that is a proportion between total ON and OFF state intervals during one cycle and is identical for all switches in NPC inverter (Zhang, Thomsen et Andersen, 2013). Also, i_N is the summation of all phase currents as $i_N=i_A+i_B+i_C$ and each phase current is defined as division of related phase voltage by loads impedance (Z). As phase and branch voltages are equal in 3L/4W NPC, i_N would be as:

$$i_N = \frac{V_{Ag}}{Z_1} + \frac{V_{Bg}}{Z_2} + \frac{V_{Cg}}{Z_3} \tag{4.13}$$

By replacing Eq. (4.13) into Eq. (4.12) and expressing branch voltages with respect to their Fourier decomposition using Eq. (4.1), V_c is written as:

$$V_c = \frac{-k_x}{2C} \times \int \left(\sum_{n=1}^{\infty} H_n \left(\frac{\sin(n\omega t)}{Z_1} + \frac{\sin(n\omega t + \frac{2n\pi}{3})}{Z_2} + \frac{\sin(\omega nt + \frac{4n\pi}{3})}{Z_3} \right) \right) . d\omega t \tag{4.14}$$

Where, ω is radian frequency set as $2\pi f$ and f is fundamental frequency. By separately integrating V_c in two intervals [0 π] and [π 2π], it is ascertained that DC capacitors are equally charged and discharged in a sensor-less approach using CSHE because V_c has same magnitude in both intervals as:

$$\left|V_c\right|_0^{\pi} = \left|V_c\right|_{\pi}^{2\pi} = \frac{k_x}{2C}\sum_{n=1}^{\infty}\left(\frac{2H_n}{n}\right)\left(\frac{1}{Z_1} + \frac{\cos\left(\frac{2n\pi}{3}\right)}{Z_2} + \frac{\cos\left(\frac{4n\pi}{3}\right)}{Z_3}\right) \tag{4.15}$$

Moreover, the necessity of elimination of low triplen and non-triplen harmonics in CSHE-PWM is validated as V_c expressed with respect to the harmonics amplitudes of branch voltages. By integrating Eq. (4.14) in time domain (dt), V_c is acquired as Eq. (4.16):

$$V_c = \frac{k_x}{2C\omega}\sum_{n=1}^{\infty}\left(\frac{H_n}{n}\right)\left(\frac{\cos(n\omega t)}{Z_1} + \frac{\cos\left(n\left(\omega t + \frac{2\pi}{3}\right)\right)}{Z_2} + \frac{\cos\left(n\left(\omega t + \frac{4\pi}{3}\right)\right)}{Z_3}\right) \tag{4.16}$$

According to Eq. (4.16), V_c is influenced by both triplen and non-triplen harmonics; but, the lower orders have further effect as the amplitudes are divided by orders (H_n/n). Hence, it is essential to cancel both low order triplen and non-triplen harmonics in 3L/4W NPC as Eq. (4.4) to control voltage ripple. The effect of triplen orders is more clarified when the loads are assumed identical (Z_1=Z_2=Z_3=Z) in Eq. (4.16), so V_c will be:

$$V_c = \frac{k_x}{2C\omega Z}\left(\sum_{n=1}^{\infty}\left(\frac{H_{3n}}{n}\right)\right)\cos(3n\omega t) \tag{4.17}$$

As shown in Eq. (4.17), V_c only includes triplen orders (H_{3n}) that emphasizes their elimination. Similar to Eq. (4.16), triplen amplitudes are divided by harmonics orders (H_{3n}/n) in Eq. (4.17) that indicates the higher triplen orders have negligible effects on V_c compared to lower ones. So, the suppression of amplitudes of low order non-triplen and particularly triplen harmonics leads to control the DC capacitor voltage ripple and vice versa.

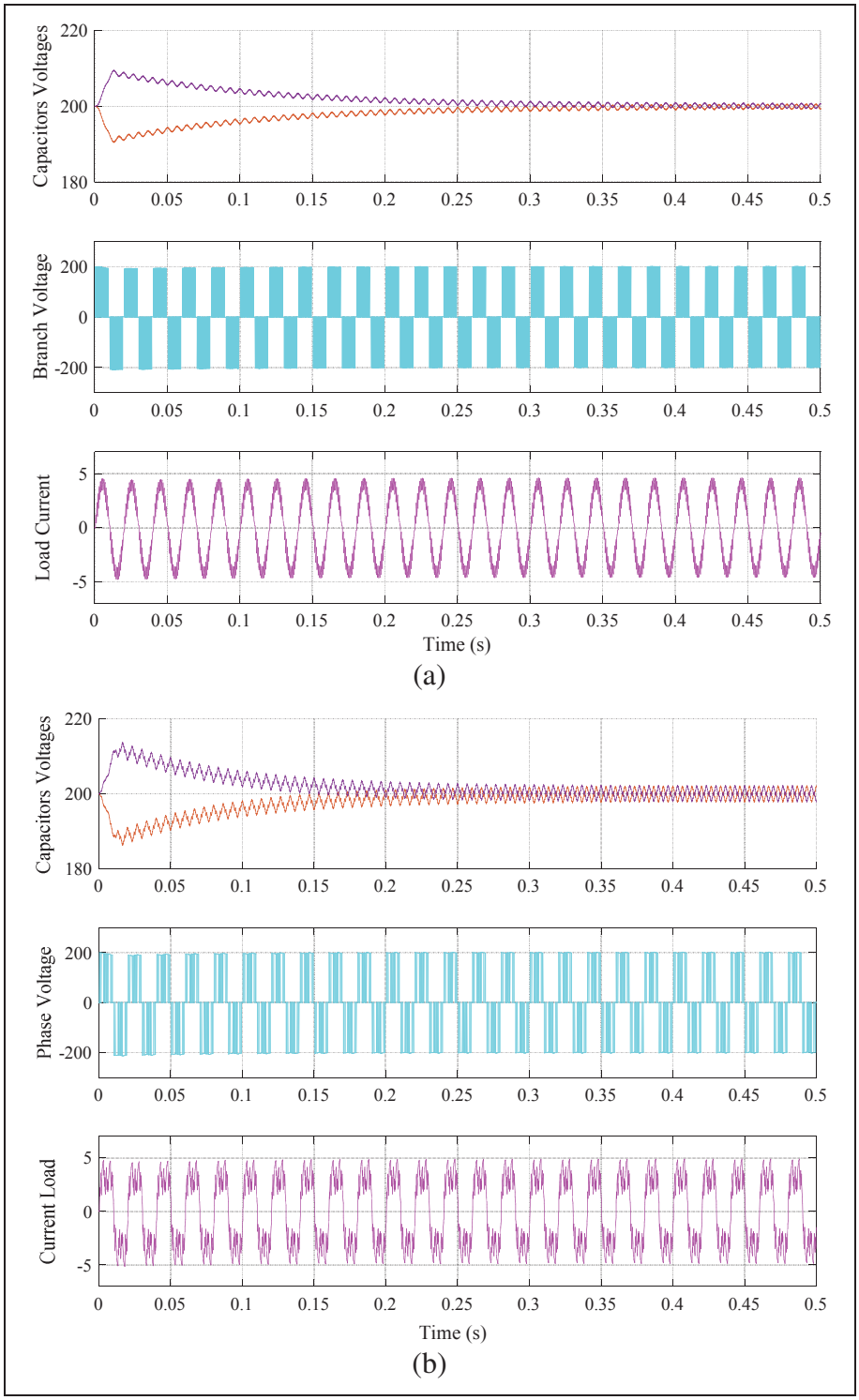

Figure 4.4 The effects of triplen harmonics on the capacitors voltages and load current in SHE for 3L/4W NPC inverter, (a) SHE with elimination of triplen harmonics, (b) SHE without elimination of triplen harmonics

In order to show the effects of the elimination of the low order harmonics amplitudes on capacitor voltage ripple in the 3L/4W NPC inverter, two situations is SHE-PWM with same number of switching angles including triplen harmonics amplitudes elimination and without triplen harmonics amplitudes elimination has been considered. Figure 4.4-a and Figure 4.4-b shows the DC capacitors voltages, phase voltage and load current of 3L/4W NPC inverter according to the two mentioned SHE conditions. By comparing Figure 4.4-a and Figure 4.4-b, when the low order triplen harmonics are not eliminated, although the capacitor voltage are balanced due to the symmetry in phase voltage waveform, the voltage ripple is subsequently increased. Also, as it is shown in Figure 4.4-b, the load current is out of sine form, since the triplen harmonic are remained in phase voltage of 3L/4W NPC inverter. In fact, when triplen harmonics amplitudes are not eliminated in 3L/4W NPC inverter the load current is distorted which increases the capacitor voltage ripple. Therefore, DC capacitors are properly self-balanced with low voltage ripple applying CSHE-PWM to generate appropriate pulses for elimination of both triplen and non-triplen orders that makes 3L/4W NPC inerter capable of dealing with both symmetrical and asymmetrical loads.

4.3 Harmonic Content and Power Losses Analysis

In this work, SHE technique has been applied for two four-wire NPC inverter topologies. In four-wire inverters, SHE equations are defined based on the phase voltage harmonic content obtained from the Fourier decomposition of the predefined branch voltage waveform. Since the relationships between phase and branch voltages of 3L/4W and 4L/4W inverters are different, two designed SHE equations for two four-wire inverters will be also different. Consequently, the performances of two SHE techniques are distinct by which compatibility of SHE-PWM with four-wire NPC inverter topologies can be investigated. The proposed CSHE-PWM for 3L/4W is compared to the SHE for 4L/4W NPC in the following items to prove the superiority of CSHE in the case of having excellent performance in four-wire topology. In this case, 12 switching angles have been selected in CSHE-PWM to eliminate both triplen and non-triplen orders between 3^{rd} and 23th. Thus, number of eliminated harmonics in CSHE for 3L/4W is as equal as SHE for 4L/4W NPC presented in

(Sharifzadeh, 2016a) that a fair comparison can be conducted. Figure 4.5 shows the obtained pulses in CSHE-PWM for 3L/4W NPC inverter. It must be noticed that *E* is assumed as *1* p.u in CSHE equations.

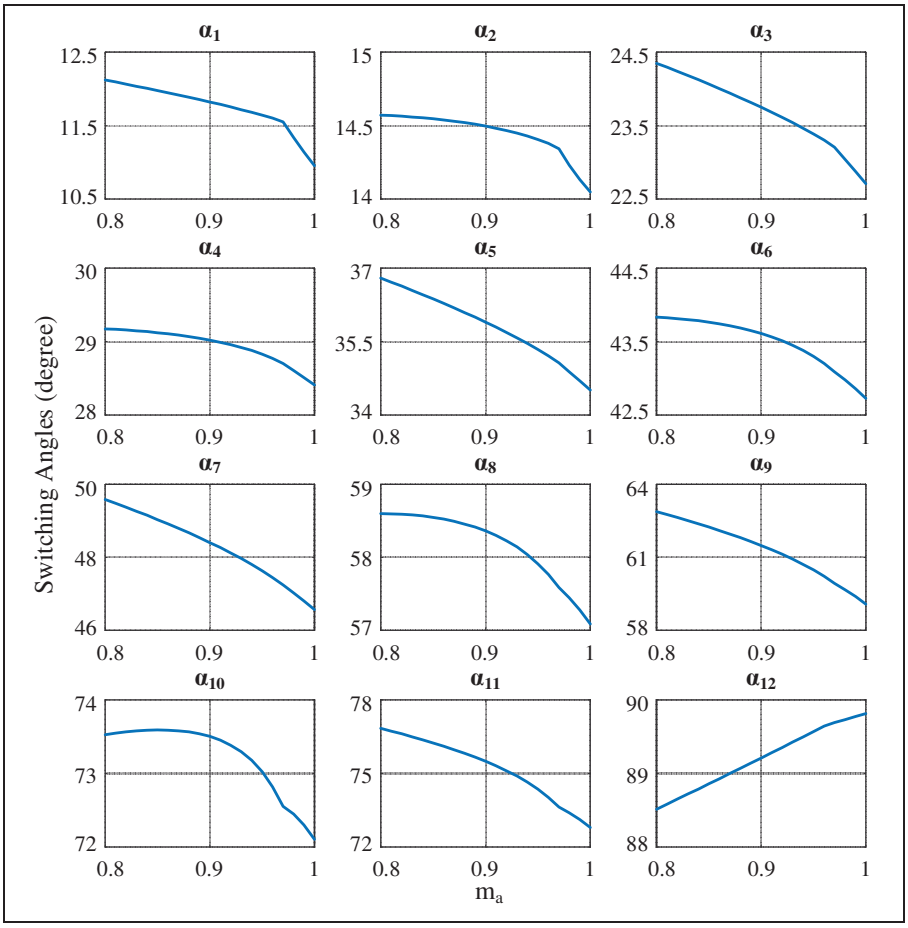

Figure 4.5 Obtained values for 12 switching angles of CSHE for 3L/4W NPC

4.3.1 Phase Voltage Harmonic Content Quality

According to the SHE principle for 4L/4W NPC, the fourth leg generates only triplen orders to cancel the specified triplen harmonics of phase voltages indirectly. However, this leg also amplifies non-eliminated triplen amplitudes of phase voltages and noticeably increases phase voltages THD which means further bulky and costly filter is required.

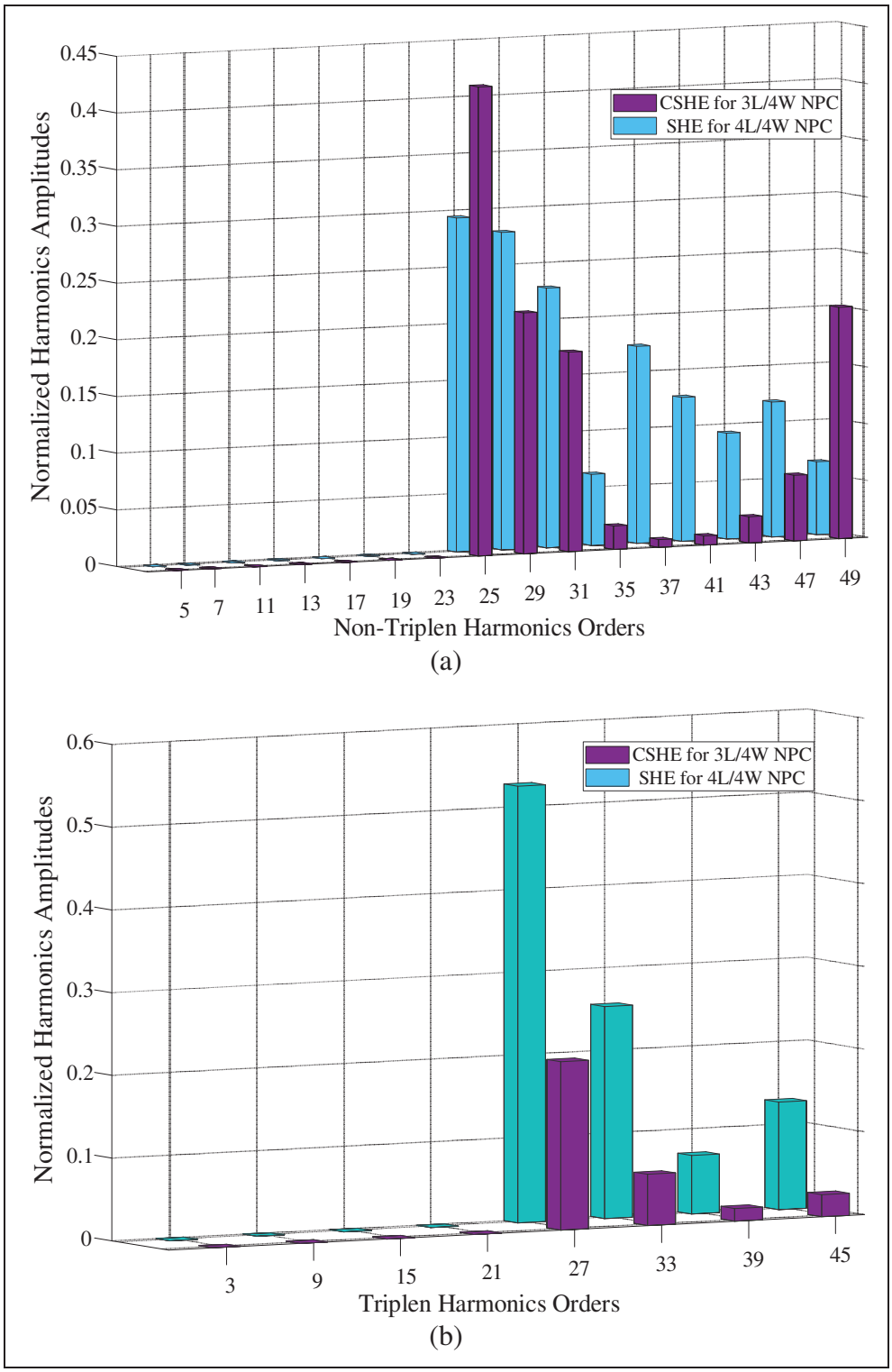

Figure 4.6 Worst case amplitudes of non-triplen and triplen orders of both SHE techniques for 4wire NPC inverters, (a) non-triplen orders (b) triplen orders

On the other hand, as the branch and phase voltages are equal in 3L/4W NPC, CSHE cancels low harmonics orders in the phase voltage directly. Indeed, as a result of direct control of phase voltage harmonic content in the CSHE thanks to the 3L/4W NPC inverter topology, the higher triplen orders are not intensified and the phase voltage THD is controlled. Two different analysis methods are done to provide a harmonic content comparison between both SHE control strategies for four-wire NPC inverters. The reason for performing the harmonic content analysis is to show the effect of indirect and direct control of phase voltage harmonic profile by the designed SHE techniques and also to investigate how much the higher non-eliminated harmonics amplitudes are intensified in SHE for 4L/4W NPC inverter. First, the worst case amplitudes for triplen and non-triplen orders up to 49^{th} are compared. Second, the phase voltage THD is depicted for all modulation indices to analyze harmonic distortion of triplen and non-triplen orders. THD is computed in two situations; for all harmonics orders up to 49^{th} and when the Nyquist frequency is assumed as the maximum frequency in Matlab FFT analysis. In the case of Nyquist frequency, all harmonics amplitudes without any limitation for highest order are assumed in THD computation.

Figure 4.6-a and Figure 4.6-b shows the worst case scenario of non-triplen and triplen amplitudes in CSHE and SHE applied on 3L/4W and 4L/4W NPC. As it is clear in Figure 4.6-a, non-triplen amplitudes of CSHE are less than SHE exceptionally for two harmonics orders (25^{th} & 49^{th}). As well, all triplen orders in CSHE are significantly lower than SHE as shown in Figure 4.6-b since fourth leg switching operation intensifies non-eliminated triplen harmonics. To ascertain that the triplen harmonics are generally greater in SHE than CSHE, the ratio between non-eliminated triplen amplitudes are calculated for all modulation indices as well.

Figure 4.7 presents the proportion of similar non-eliminated triplen amplitudes including 27^{th}, 33^{rd}, 39^{th} and 45^{th} in CSHE for 3L/4W and SHE for 4L/4W NPC. These ratios show that all non-eliminated triplen amplitudes are amplified in SHE for 4L/4W NPC in entire range of modulation index that the average values for proportion of $H_{27}^{SHE}/H_{27}^{CSHE}$, $H_{33}^{SHE}/H_{33}^{CSHE}$, $H_{39}^{SHE}/H_{39}^{CSHE}$ and $H_{39}^{SHE}/H_{39}^{CSHE}$ are *13.78, 8.75, 5.93* and *6.05*, respectively. As well, the

amplitudes of H_{39}^{CSHE} have zero value for $0.8<m_a<0.88$; so, $H_{39}^{SHE}/H_{39}^{CSHE}$ is indeterminate. The phase voltages THD of both SHE techniques have been also compared to further scrutinize the harmonic amplitudes and to show the impact rate of the amplification of the non-eliminated triplen harmonics on the harmonic quality.

Figure 4.8 shows phase voltage THD of CSHE for 3L/4W and SHE for 4L/4W NPC inverters. The dashed line depicts THD for the harmonics orders between 3rd-to-49th while the continuous line shows THD of Nyquist frequency calculations. As it can be seen, the amplification of all non-eliminated triplen harmonics in SHE operation for 4L/4W NPC has been led to increase the phase voltage THD observably. The phase voltage THD ratio between CSHE and SHE for harmonic orders up to 49th is *1.415* and for Nyquist frequency is equal to *1.40*.

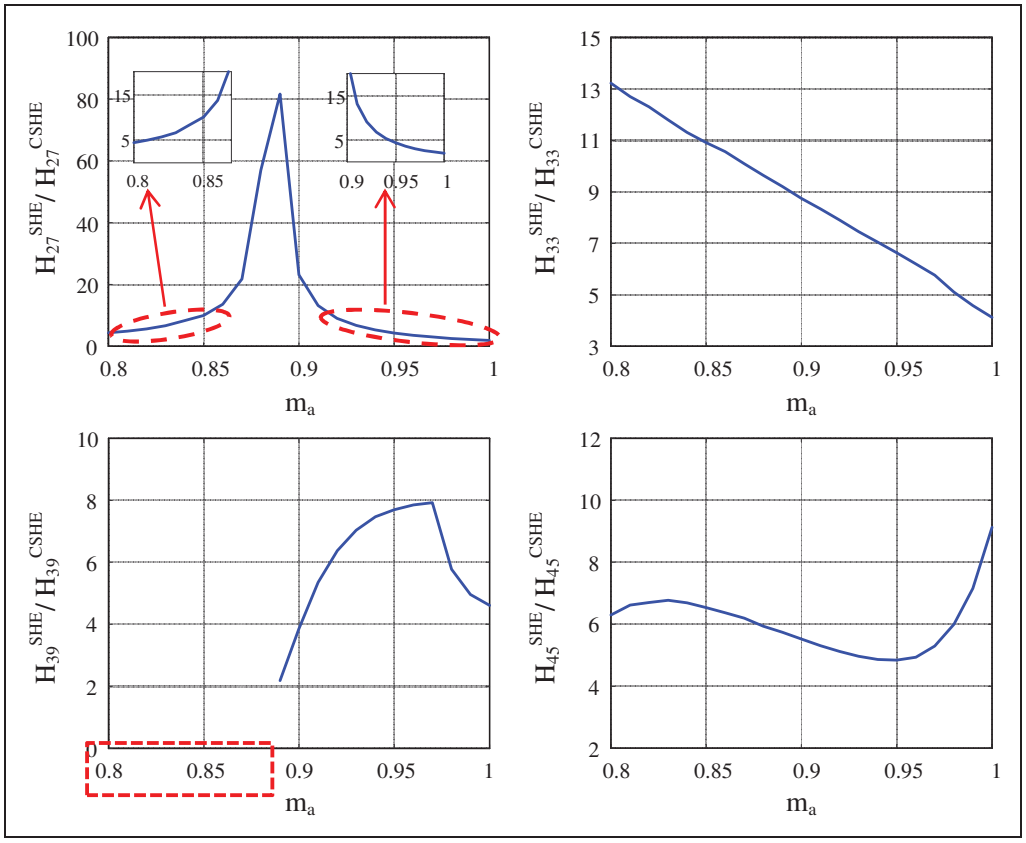

Figure 4.7 Proportion of similar non-eliminated triplen amplitudes in CSHE for 3L/4W NPC and SHE for 4L/4W NPC

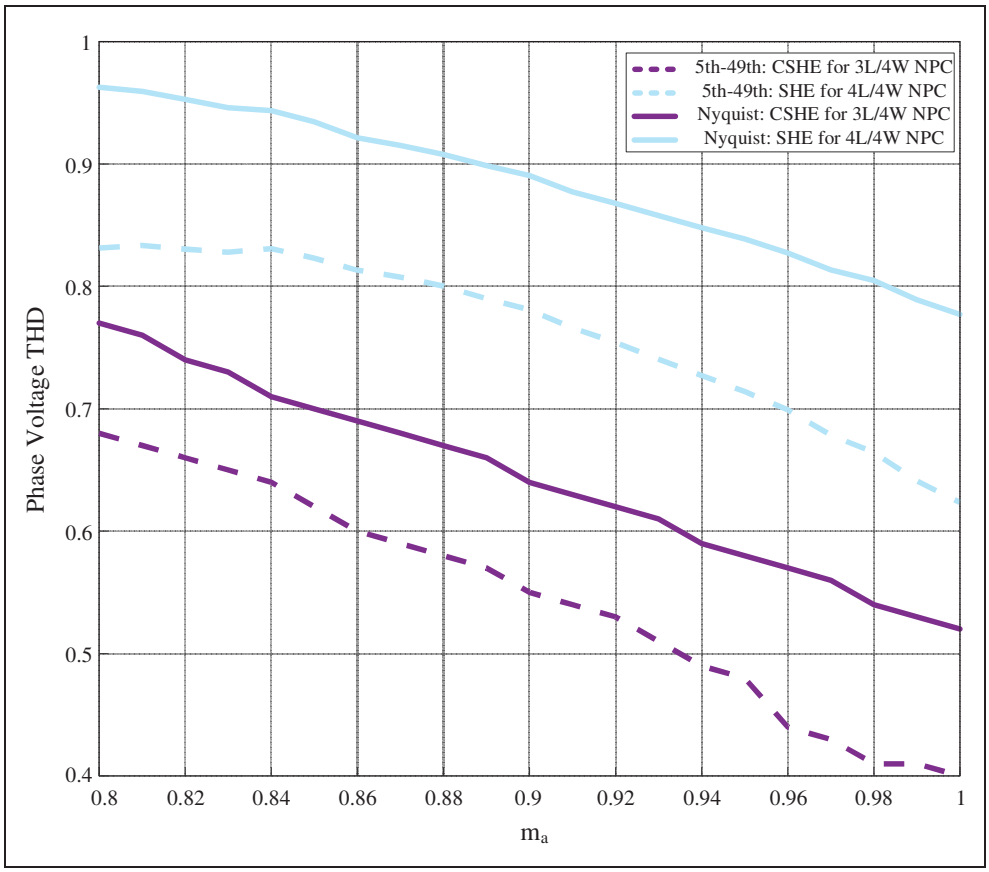

Figure 4.8 Phase voltage THD of CSHE-PWM and normal SHE-PWM for harmonic orders up to 49th and Nyquist frequency

4.3.2 Switching Frequency and Power Losses Concerns

Switching frequency (f_s) in SHE-PWM is computed by multiplying number of pulses by fundamental frequency of output voltage (f) (Sharifzadeh, 2016a). Since number of pulses and angles (k) are equal in NPC, the switching frequency is obtained as:

$$f_s = k.f \tag{4.18}$$

In SHE for 4L/4W NPC, the main and fourth legs switching frequencies are different because of inequality in number of switching angles and fundamental frequency. The switching frequency for main (f_s^A) and neutral (f_s^N) legs is as below:

$$\frac{f_s^A}{f_s^N} = \frac{k.f^A}{m.f^N} \quad \& \quad f^N = 3f^A \tag{4.19}$$

The switching frequency inequality and more semiconductor devices of fourth leg increase the switching power losses in SHE for 4L/4W NPC compared to CSHE for 3L/4W NPC. The switching power losses is approximately calculated for power switch (P_S) and anti-parallel diode (P_D) using Eq. (4.20) presented in (Gupta, Ghosh, et Joshi, 2008) as:

$$\begin{cases} P_S = \dfrac{f_s.V_s.I_S(T_{on}+T_{off})}{2\pi} \\ P_D = 0.125(V_D.I_D.T_D.f_s) \end{cases} \tag{4.20}$$

And the total switching power losses (P_T) will be:

$$P_T = P_S + P_D \tag{4.21}$$

Where, I_S, V_s, T_{on} and T_{off} are the peak current, maximum voltage across the switch, the rise and fall time, respectively. Also, V_D, I_D and T_D are diode peak voltage, peak reverse current and reverse time, respectively. The power switch used in prototype of NPC inverters is 1.2-kV 35-A SiC MOSFETs of type SCT2080KE. V_s and V_D are assumed identical and equal to the capacitor voltage (E).

Moreover, I_s and I_D have same values and calculated for each m_a value. Switching frequency of CSHE-PWM and SHE-PWM is calculated using equations (4.18) and (4.19) while fundamental frequency is 50 Hz. Considering 8 angles for main legs and 4 angles for fourth leg in SHE for 4L/4W NPC, switching frequency is obtained 400 Hz and 600 Hz accordingly.

As well, 12 switching angles for CSHE results in switching frequency equal to 600 Hz. Figure 4.9-a and Figure 4.9-b show calculated switching power losses of CSHE for 3L/4W and SHE for 4L/4W NPC when both topologies are supplying same loads conditions. Figure 4.9-a presents switching power losses when three-phase balanced loads are connected and in Figure 4.9-b only a single-phase unbalanced load is supplied.

As can be seen from Figure 4.9, the normalized power losses of SHE for 4L/4W NPC is approximately *3.21* and 3.1 times greater in balanced and unbalanced loads conditions compared to CSHE for 3L/4W NPC.

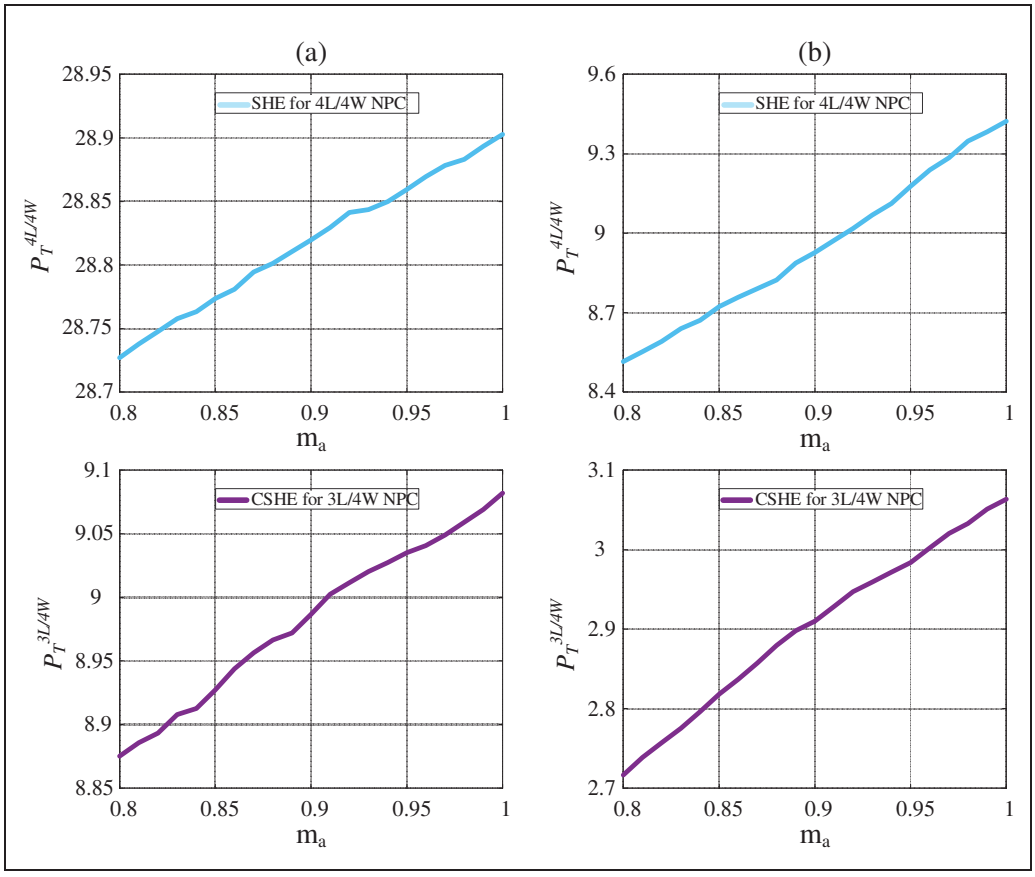

Figure 4.9 Switching power losses in CSHE for 3L/4W and SHE for 4L/4W NPC, (a) balanced three-phase load, (b) unbalanced single phase load

4.4 Simulation and Experimental Results Analysis of the Proposed CSHE for 3L/4W NPC Inverter

In order to evaluate the CSHE-PWM and confirm its compatibility with 3L/4W inverter, it has been tested through both simulation and experimental analysis. For the experimental CSHE-PWM has been applied for 3L/4W NPC inverter prototype using dSpace 1103 as the hardware controller to obtain the experimental results.

The 3L/4W NPC is tested with different loads including linear/nonlinear, balanced/unbalanced to analyze the CSHE under different loads conditions. The simulation and experimental tests parameters are shown in Table 4.1.

Table 4.1 Tested NPC Inverter System Parameters

DC source voltage (V_{dc})	300 V
Fundamental and switching frequency	50 Hz, 600 Hz
Load resistance and reactance (R, L)	40 Ω, 20 mH
Rectifier DC side load (R_{dc}, L_{dc}) as the nonlinear load	80 Ω, 50 mH
Capacitance of DC-link capacitors (C_1, C_2)	650 µF
Modulation index	0.85

Figure 4.10-(a and b) shows simulation and experimental results of the phase and line voltages as well as load current with their harmonics spectrums of the proposed CSHE-PWM when 3L/4W NPC inverter is feeding three-phase linear balance R-L loads.

The determined triplen and non-triplen harmonics orders are eliminated in phase voltage harmonic spectrum while the higher harmonics orders are not amplified. Also, all triplen harmonics orders are removed in line voltage owing to 120° phase shift between inverter's legs.

Since the selected harmonics amplitudes are eliminated in phase voltage and load current is the division of phase voltage and output load, same selected harmonics amplitudes is suppressed in load current as well. The current harmonic analysis of both simulation and experimental results of Figure 4.10-(a and b) illustrates that same harmonics amplitudes are eliminated in load currents.

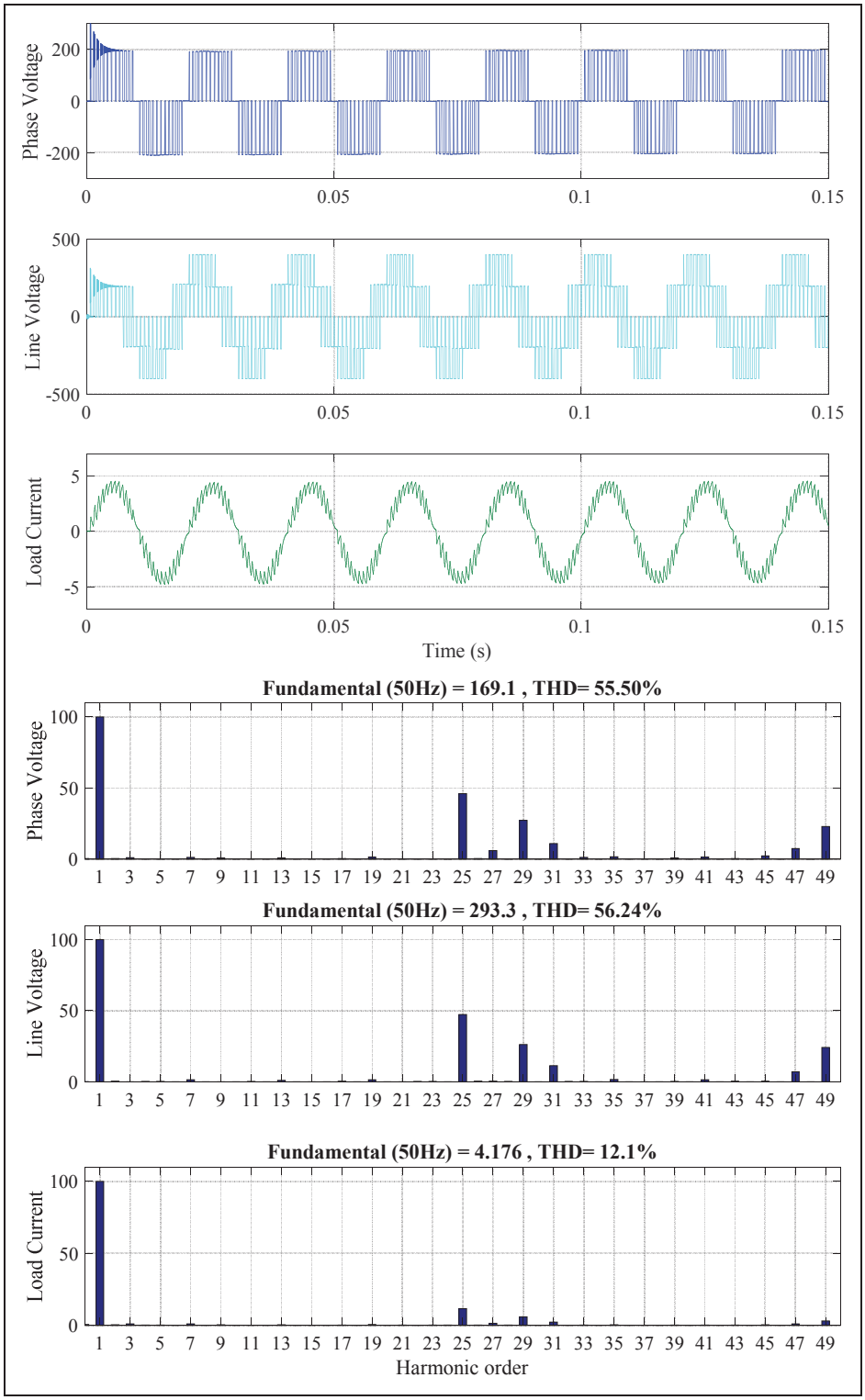

Figure 4.10-a Simulation results of phase, line voltages and load current along with their harmonic spectrum results when 3L/4W NPC connected to linear/balance load

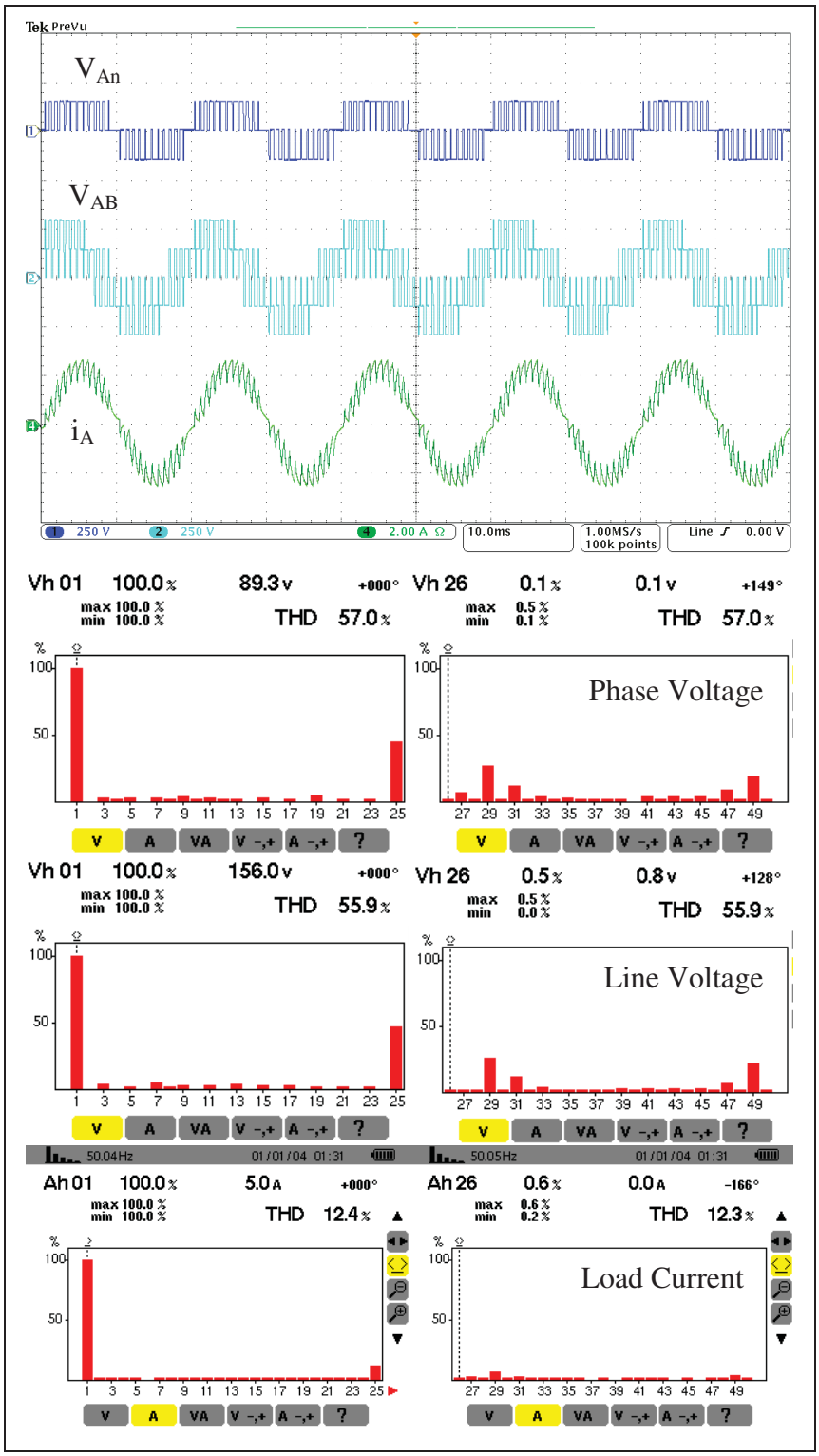

Figure 4.10-b Experimental result of phase, line voltages and load current and experimental analysis of harmonic spectrum of phase, line voltages and load current when 3L/4W NPC connected to linear/balance load

Figure 4.11 also demonstrates the experimental results of DC-link capacitors voltages as well as phase voltage and load current when 3L/4W NPC inverter is controlled by the designed SHE and supplies three-phase linear and balanced loads. It has been clearly shown that both DC capacitors are desirably balanced to half of DC input voltage oscillating with low voltage ripple.

Figure 4.12 demonstrates the experimental results of phase voltage and current with neutral current and capacitors voltages when the 3L/4W NPC inverter supplies three-phase R-L loads and single-phase diode rectifier as unbalanced and nonlinear load condition. Diode rectifier is considered as a nonlinear situation with output R-L load, using same values for resistance and reactance shown in Table 4.1. In first case, the rectifier is connected between leg A and B that results are shown in Figure 4.12-a. Secondly, it has been connected to the points A and n of NPC inverter and results are illustrated in Figure 4.12-b that validates the low voltage THD as well as low voltage ripple of DC capacitors.

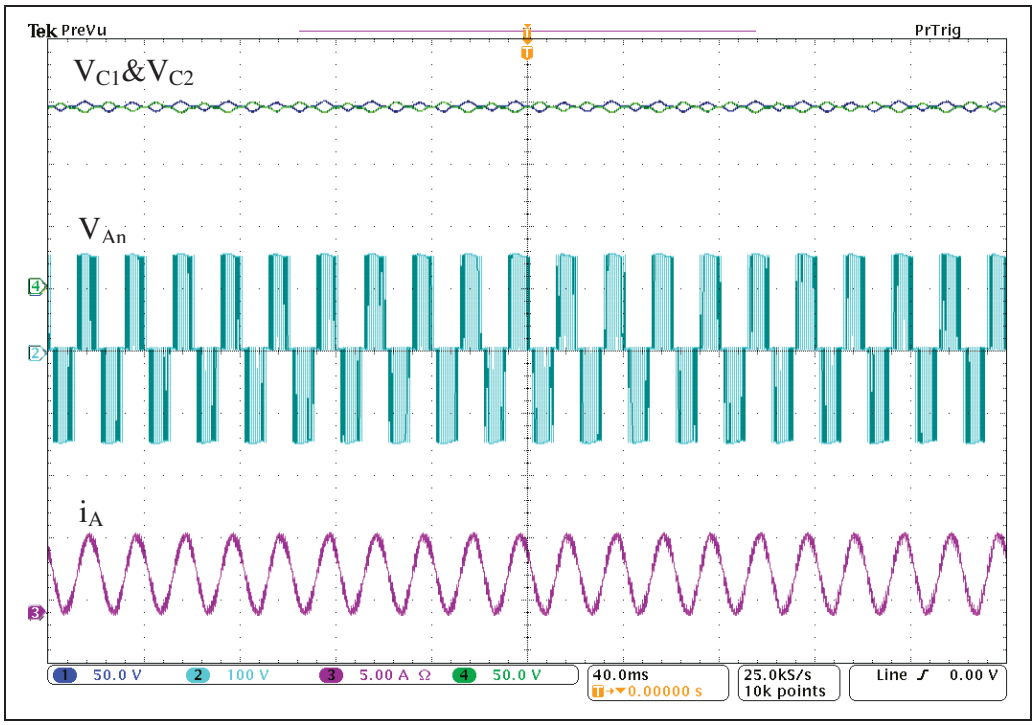

Figure 4.11 Experimental results of DC-link capacitors voltages and phase voltage and load current when 3L/4W NPC connected to linear/balance load

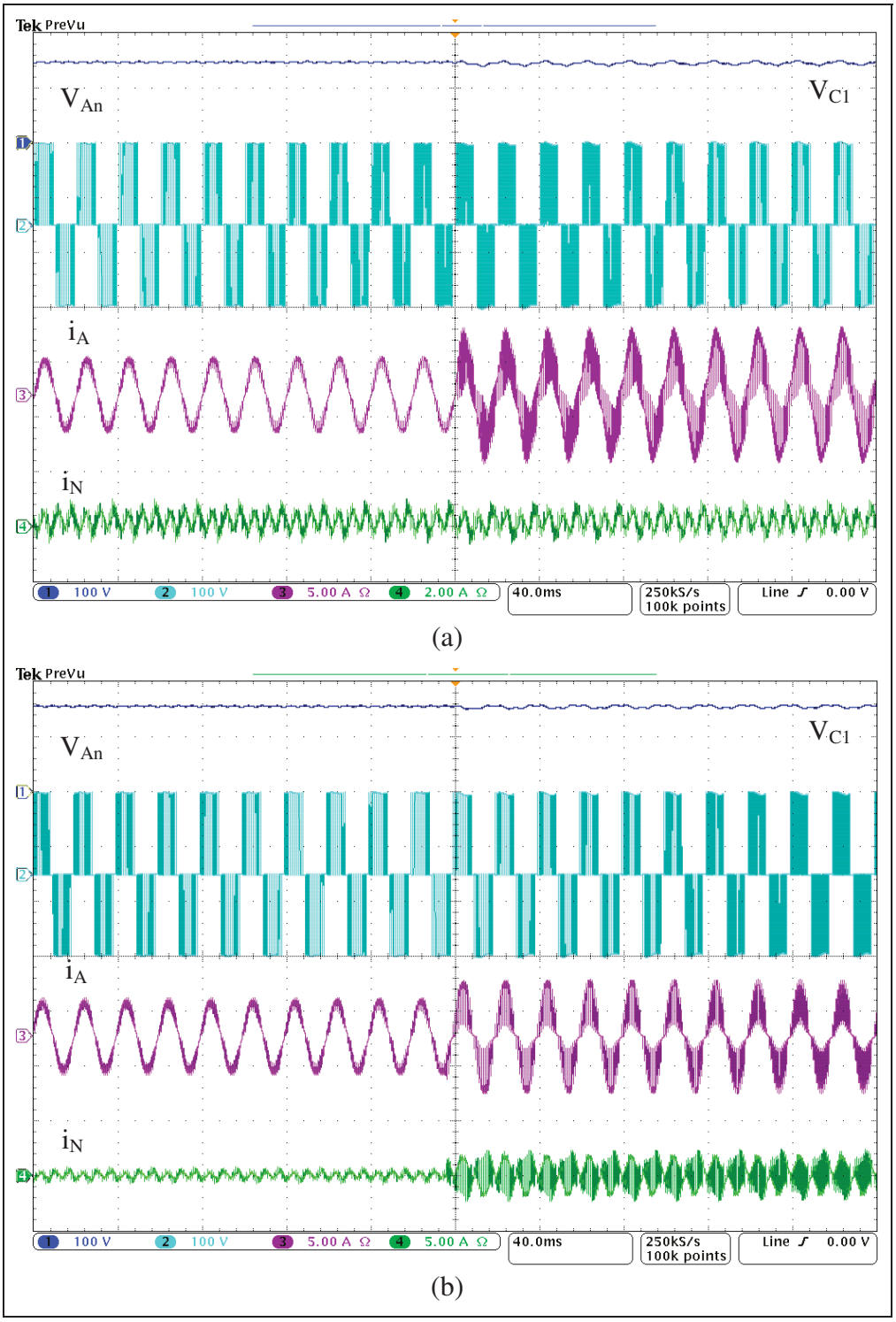

Figure 4.12 Experimental results of phase voltage and current when nonlinear load is connected to 3L/4W NPC, (a) nonlinear load is between leg A and B, (b) nonlinear load is between leg A and neutral wire

Afterwards, the loads of phases B and C are disconnected while the diode rectifier is still between neutral wire and leg A. Figure 4.13 shows the corresponding experimental results. Although the asymmetrical load situation is aggravated, the DC capacitors voltages are remained balanced with acceptable voltage ripple. Figure 4.14 also illustrates three-phase and neutral currents regarding to the experimental results of Figure 4.13 when output loads of leg B and C are disconnected. As can be seen, the neutral current is increased after disruption of two phases. Since the neutral current is the sum of phases' current ($i_N=i_A+i_B+i_C$), after that change, it is equal to leg A's current ($i_N=i_A$).

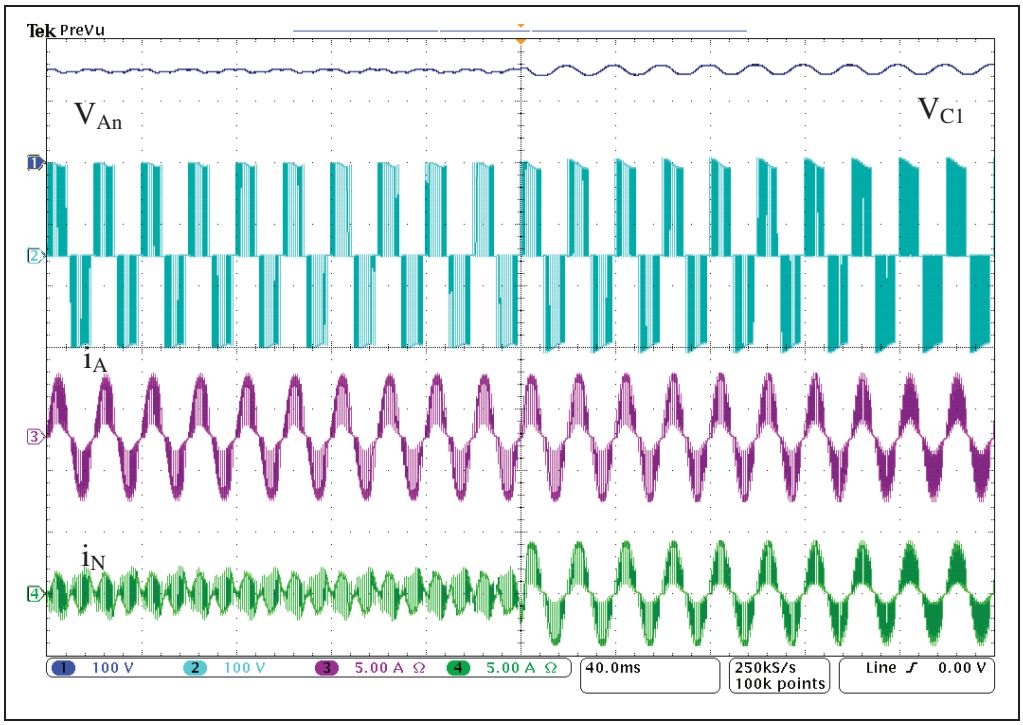

Figure 4.13 Experimental results of phase voltage and current when 3L/4W NPC supply single phase linear and nonlinear loads

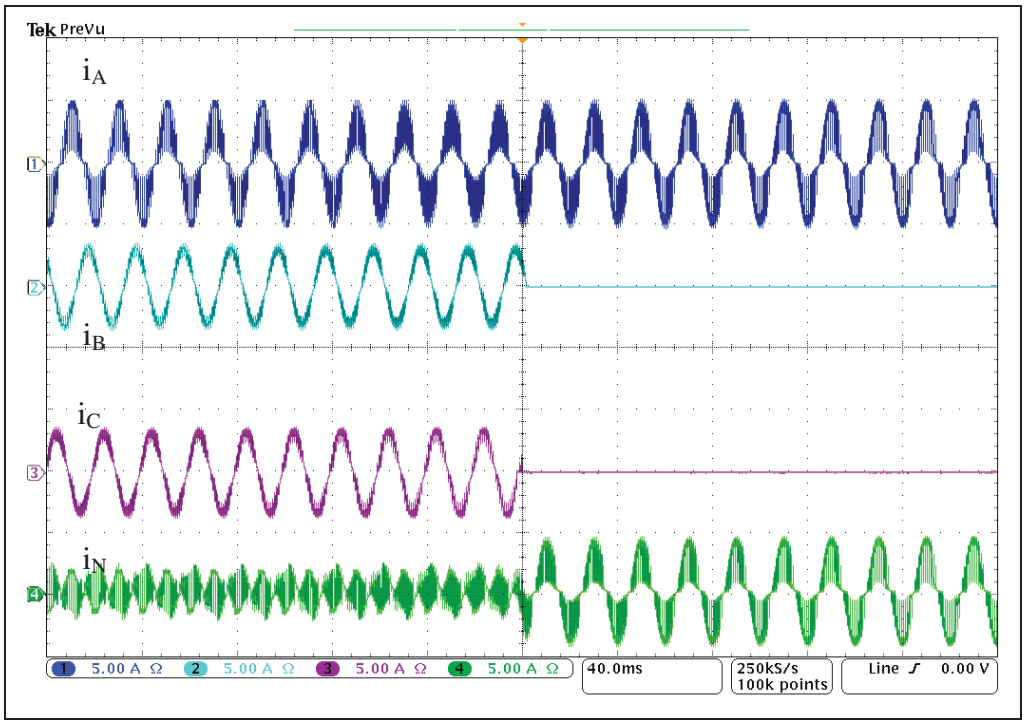

Figure 4.14 3phase and neutral currents related to experimental results of Figure 4.12

4.5 Conclusions

In this work, CSHE-PWM has been proposed for 3L/4W NPC to self-regulate DC capacitors voltage with low ripple as symmetrical/asymmetrical loads can be supplied in a cost effective way in comparison to SHE for 4L/4W NPC. As phase voltage harmonic profile should be controlled in four-wire inverters topologies, SHE equations are expressed based on its harmonics amplitudes. On the other hand, the phase voltage harmonic spectrum which is formulized with respect to the preprogramed branch voltage waveform using Fourier decomposition is different for each four-wire NPC inverter topology. As a result, there is a difference between two designed SHE equations for two four-wire NPC inverters which makes difference between the operations of two SHE techniques. Therefore, unlike SHE for 4L/4W NPC that the specific triplen harmonics are indirectly cancelled in phase voltages through particular switching operation of fourth leg, CSHE directly eliminates both triplen and non-triplen harmonics in phase voltages. By direct control of phase voltage harmonic content, the corresponding THD is noticeably decreases in the designed SHE for 3L/4W NPC

compared to the SHE for 4L/4W NPC since the higher triplen orders are not amplified. Hence, not only switching power losses is decreased by removing the fourth leg, but also there is less angles' calculations complexity in CSHE. Theoretical and experimental discussions confirm that SHE is compatible to be designed for 3L/4W than 4L/4W NPC to handle unbalanced loads suitable for UPS application.

CHAPTER 5

HYBRID SHM-PWM FOR COMMON MODE VOLTAGE REDUTION IN THREE-PHASE THREE-LEVEL NPC INVERTER

Mohammad Sharifzadeh [a], Mohammad Babaie [b], Gabriel Chouinard [c], Kamal Al-Haddad [d], Ramon Portillo [e], Leopoldo Garcia Franquelo [f], K. Gopakumar [g]

[a, b, c, d] Department of Electrical Engineering, École de Technologie Supérieure,
1100 Notre-Dame West, Montreal, Quebec, Canada, H3C 1K3
[e, f] Department of Electrical Engineering, University of Seville,
Calle San Fernando, 4, 41004 Sevilla, Spain
[g] Department of Electronic Systems Engineering, Indian Institute of Science (IISc)
CV Raman Rd, Bengaluru, Karnataka 560012, India

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Abstract

This chapter proposes Hybrid Selective Harmonic Mitigation (SHM)-PWM which is characterized by both features harmonic mitigation and elimination aimed to reduce Common Mode Voltage (CMV) and to mitigate selected non-triplen harmonics in 3phase NPC inverter. As CMV harmonic modeling only shows triplens, the specified triplens are eliminated using SHE operation to control CMV pulses widths and consequently to mitigate CMV magnitude which appears as its RMS reduction. The determined non-triplen harmonics are also mitigated using SHM approach by same cost function. The proposed Hybrid SHM-PWM empowered by both harmonic elimination and mitigation is implemented on 3phase NPC inverter to confirm its performance on reducing CMV through experimental and theoretical analyses. It is shown that Hybrid SHM is superior over pure SHE or SHM in dealing with multi-objective system including CMV reduction and non-triplen harmonics mitigation.

5.1 Introduction

Three-phase Three-level Diode Clamped inverter which is so-called as Neutral Point Clamped (NPC) in literature has emerged as first multilevel topologies generation to overcome the restriction of two-level structure for operation in higher power application (Abari et al., 2018; Wang, Zhang et Xie, 2018). Due to the prominent advantages like convenience in capacitor balancing, fewer components and single-DC source, 3phase NPC is widely employed for various industrial applications (Giri, Banerjee et Chakraborty, 2018). One of the 3phase NPC challenges is the generation of Common Mode Voltage (CMV) where it must be controlled to reduce the adverse effects like bearing failure, shaft voltage stress on electrical drives and Electromagnetic Interface (EMI) noises (Wu et al., 2016; Liu et al., 2016).

Two general solutions; topology modification and control development, are tracked in literatures to attenuate CMV (Shang et al., 2014). The structure correction by adding auxiliary circuit or using active/passive filters, not only cause extra side expenses but also an exclusive modification for each topology is required (Morris, Han, et Sarlioglu, 2017). On the contrary, PWM techniques are further reliable and economical solution for CMV control without any structure amendment (Le et Lee, 2017; Liu et al., 2018). In (Cacciato et al., 1999; Un et Hava, 2007), Space Vector Modulation (SVM) was improved by different strategies as Active Zero State, Remote State and Near State to optimize the switching vectors selection and generate smaller CMV. In Carrier-Based (CB)-PWM methods, CMV peak value was suppressed by changing modulation as Phase/Level-Shifted methods (Kimball et Zawodniok, 2011) or by carrier signal correction as Carrier Peak Position Modulation (Huang et Shi, 2014). Even though the high switching frequency PWM based techniques successfully reduced CMV, they caused a very challenging issue which is offset voltage in the capacitors neutral point of inverter (Xing et al., 2018). In (Wang et al., 2018) a discontinuous (CB)-PWM technique was introduced to mitigate CMV as well as the offset voltage of the capacitors neutral point using different PWM control strategies. Although SVM and CB techniques properly control CMV, they have disadvantages like limitation in

the modulation index range, adverse effects on DC-Bus capacitors voltages ripple and the high switching frequency (Lian et al., 2017). The main reason of the disadvantages in the PWM based control techniques is the ignoring of the switching vectors which generates CMV. The problem has been improved by designing the CMV control techniques using exact model of inverter in terms of CMV and capacitors voltages dynamics. Model Predictive Control (MPC) is the strategy which employs exact model of inverter to control CMV and the capacitors voltages. The implementation results in (Wang et al., 2019; Babaie et al., 2020) show that MPC successfully mitigated CMV and balanced the capacitors voltages and any switching vector was discarded. While MPC provides more satisfactory results than the PWM based techniques, it causes high and variable switching frequency which results more harmonic distortion and power losses. Moreover, MPC needs several voltage and current measurements even in stand-alone applications that are costly in industrial scale.

Selective Harmonic Elimination (SHE)-PWM is a low frequency technique appealing for multilevel inverters since pulses are predefined by offline computation (Enjeti, Ziogas, et Lindsay, 1988; Dahidah, Konstantinou, et Agelidis, 2015; Patel et. Hoft, 1973; Patel et. Hoft, 1974). So far, SHE has been used in various applications which is aimed to control multilevel inverter under low switching frequency operation so as the power losses can be decreased remarkably (Dahidah, Konstantinou, et Agelidis, 2015; Sharifzadeh et al., 2019). This promising feature of SHE made it an appealing modulation technique for high power single-phase applications such as fault tolerant strategy (Ni, Abuelnaga, et Narimani, 2020), grid-tied inverters (Dabbaghjamanesh et al., 2020), renewable energy systems (Panda, Lee, et Panda, 2019) and so on. SHE is also a reliable modulation technique that can guarantee the capacitor voltage balancing in the multilevel inverters where it can achieve this challenging matter autonomously for active capacitor voltage balancing or by means of a controller like Model Predictive Control (MPC) for external capacitor voltage regulation (Wu, Li, et Konstantinou, 2020; Hong et Cao, 2020). In spite of the single-phase applications, SHE is also interesting for three-phase multilevel topologies such as 3phase four-wire inverters and 3phase Modular Multilevel Converters (MMC) (Sharifzadeh et al., 2019; Xin et al., 2020). In (Zhao et al., 2012), Hybrid SHE-PWM was proposed to reduce CMV using a combination of

conventional and modified SHE-PWM for high and low modulation range; respectively. But, transient between two SHE methods affects elimination capability. Also, an auxiliary LC filter is required for CMV reduction under low modulation operation of modified SHE. Selective Harmonic Mitigation (SHM)-PWM is another low frequency method as a SHE expansion pattern to further control harmonic distortion particularly non-eliminated orders. SHM was improved in (Ghoreishy et al., 2010), to reduce CMV by controlling the DC source as both pulses and amplitudes widths are considered as variable; but, a rectifier is required for flexible DC sources.

In this work, SHM-PWM and SHE-PWM are hybridized to simultaneously include both features of harmonic elimination and mitigation through a single cost function to control two control objectives; CMV reduction and selected non-triplen harmonics mitigation. The idea of hybridizing two techniques has emerged in (Sharifzadeh et al., 2015; Sharifzadeh et al., 2016b) where a combination of SHM and SHE was proposed for 3phase 4leg NPC. It was shown that hybrid SHM and SHE has better performance than their pure operation. Also, SHM and SHE presented in (Sharifzadeh et al., 2015; Sharifzadeh et al., 2016b) were combined by two separated cost functions through a complex angles computation where the final technique is only specified to 4leg inverter applications. Indeed, SHM and SHE are normally implemented; but, they are operating in harmony which results in better efficiency. This work, however proposes a Hybrid SHM-PWM to have harmonic mitigation and elimination at the same time to control both output voltage harmonic distortion and CMV magnitude suitable for various types of 3phase inverters. Unlike the previous methods where CMV was controlled using the proper selection of the switching vectors, in this work it is controlled based on harmonic modeling and analysis in a low switching frequency operation where CMV reduction appears as CMV pulses widths reduction. CMV is firstly decomposed using Fourier analysis to its harmonics content to be included as an additional objective in the designed cost function. Since CMV contains only triplen harmonics, its magnitude is controlled if they are controlled. So, the selected triplens are cancelled and total triplen harmonics distortion is also controlled to reduce CMV. Indeed, triplens elimination results in CMV pulses widths become smaller and less effective which reduces CMV magnitude as its

RMS is decreased. The determined non-triplen harmonics are also mitigated in same cost function. Artificial Bee Colony (ABC) algorithm is used to find the angles of Hybrid SHM while all desired control objectives are obtained. The optimization performance of ABC is compared with two other meta-heuristic algorithms to validate the optimality of the attained angles. Hybrid SHM is evaluated by theoretical and experimental analyses to confirm its excellent reliability on reducing CMV and mitigation of selected harmonics. In Section 5.2, 3phase NPC is described and CMV harmonic modeling is obtained. Hybrid SHM is established in section 5.3 using CMV harmonic content to derive the related equations and cost function. In section 5.4, some theoretical analysis on voltage harmonics spectrum is done to survey the validity of pulses calculation. The experimental results of Hybrid SHM on 3phase NPC inverter are provided in Section 5.5.

5.2 CMV Harmonic Modeling of 3Phase 3Level NPC

5.2.1 3Level 3Phase Configuration of NPC Inverter Topology

Figure 5.1 shows 3level 3phase NPC inverter that each leg is configured by four switches and two clamped diodes. As listed in Table 5.1, there are three switching states for each leg. By application of these switching states two upper switches ($S_{1,2x}$) are working in complementary with two lower ones ($S_{3,4x}$). Applying the switching states, 3level branch voltage (V_{xg}) is produced between output poles of each leg (x=*A, B & C*) and DC-Bus capacitors (g). Figure 5.2 depicts a generalized 3level branch voltage displayed as the odd quarter wave symmetry. The phases voltages (V_{xn}) dropped across the loads are also measured using the branch voltages and CMV (V_{ng}) as Eq. (5.1).

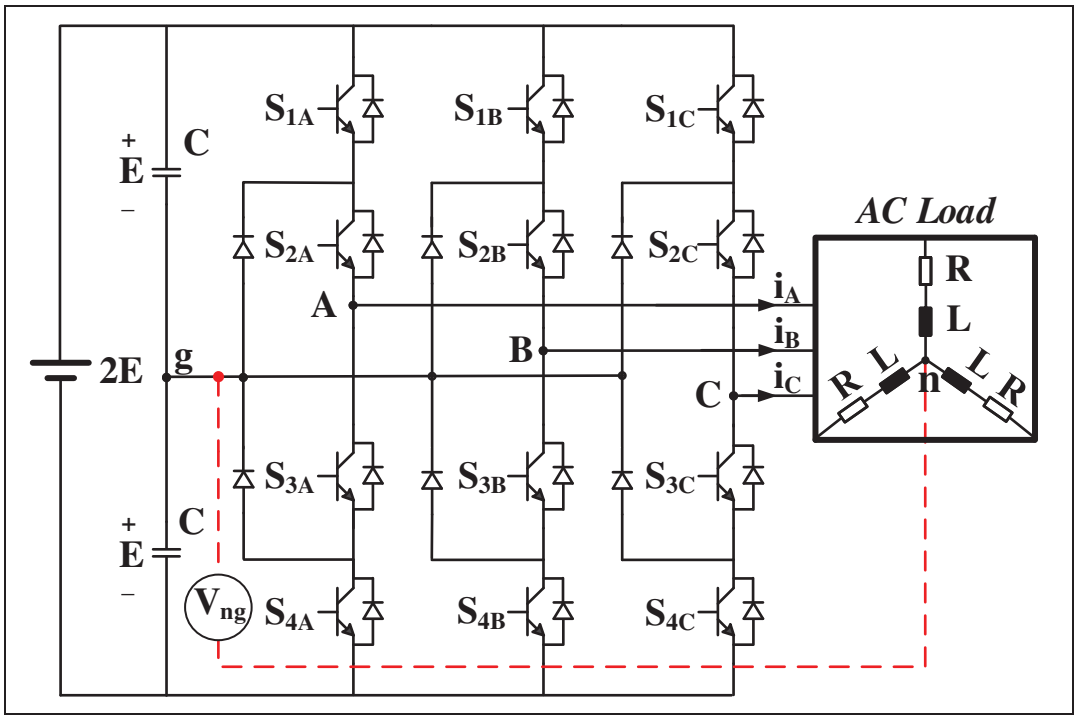

Figure 5.1 3phase configuration of 3level NPC inverter

Table 5.1 Switching States of Each Leg in 3Phase NPC Inverter

State	S_{1X}	S_{2X}	S_{3X}	S_{4X}	V_{XG}
1	1	1	0	0	+E
2	0	1	1	0	0
3	0	0	1	1	-E

$$V_{xn} = V_{xg} - V_{ng} \quad \forall x = A,\ B\ \&\ C \tag{5.1}$$

Since summation of 3phase voltages of a balanced system is zero, CMV is obtained based on branch voltages as in Eq. (5.2) (Zhao et al., 2012).

$$V_{ng} = \frac{V_{Ag} + V_{Bg} + V_{Cg}}{3} \tag{5.2}$$

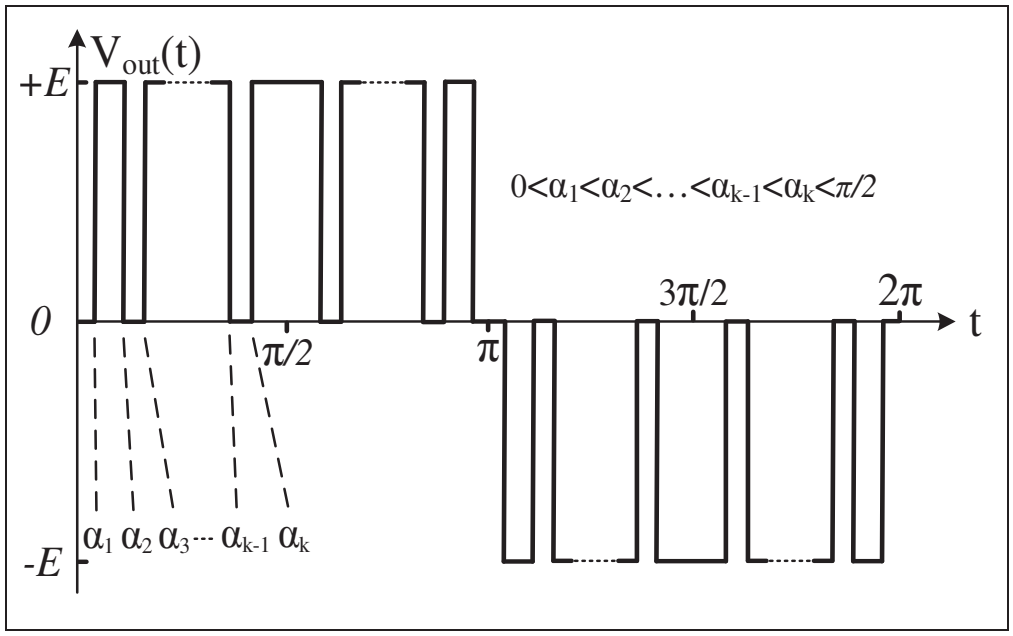

Figure 5.2 Generalized odd quarter wave symmetry of three-level voltage

5.2.2 Mathematical Formulation of CMV Harmonic Content

In order to design Hybrid SHM-PWM, it is firstly needed to model CMV harmonic profile. Since CMV is stated by V_{xg} as Eq. (5.2), it is decomposed by V_{xg} Fourier analysis. Assuming capacitors voltages as 1p.u ($E=1$), V_{xg} harmonic content of Figure 5.2 contains odd triplen and non-triplen harmonics (H_n) as:

$$\begin{cases} V(t) = \sum_{n=1,3,5,\ldots}^{\infty} (H_n \sin(n\omega t)) \quad \forall n = 1, 3, 5, \ldots \\ H_n = \frac{4}{n\pi} \sum_{i=1}^{k} (-1)^{i+1} \cos(n\alpha_i) \end{cases} \tag{5.3}$$

By expressing V_{xg} harmonic content using Eq. (5.3) with $2\pi/3$ phase shift and replacing to Eq. (5.2), CMV harmonic content is:

$$V_{ng} = \frac{\sum_{n=1,3,\ldots}^{\infty} H_n(\sin(n\omega t)+\sin(n(\omega t+2\pi/3))+\sin(n(\omega t-2\pi/3)))}{3} \tag{5.4}$$

Trigonometric terms of Eq. (5.4) is extendable using $\sin(x)+\sin(y)=2\sin\left(\frac{x+y}{2}\right).\cos(\frac{x-y}{2})$. As $x=n(\omega t+2\pi/3)$ and $y=n(\omega t-2\pi/3)$, three trigonometric functions of Eq. (5.4) are simplified based on single terms expressed as Eq. (5.5).

$$\sin(n\omega t)+\sin(n(\omega t+2\pi/3))+\sin(n(\omega t-2\pi/3))=3\sin(3n\omega t) \tag{5.5}$$

Therefore, V_{ng} is attained with tripled frequency as Eq. (5.6).

$$V_{ng} = \sum_{n=1,\,3,\,5,\,\ldots}^{\infty} H_{3n} \sin(3n\omega t) \tag{5.6}$$

So, CMV presents same triplens as V_{xg} and it is mitigated if they are properly controlled in the designed hybrid technique.

5.3 Hybrid SHM-PWM for CMV Reduction

5.3.1 Conventional SHE-PWM and SHM-PWM Techniques

SHE-PWM is formed to predetermine pulses by solving a set of harmonic-based equations. Conventional 3phase SHE is to eliminate undesired non-triplen harmonics whereas first harmonic is also desired by modulation index (m_a) as shown in Eq. (5.7). Although SHE suppresses selected harmonics, it confronts an imposing defect in dealing with higher orders.

$$\begin{cases} \left(H_1 = \frac{4}{\pi} \sum_{i=1}^{k}((-1)^{i+1}\cos(\alpha_i)) \right) = m_a \\ \left(H_n = \frac{4}{n\pi} \sum_{i=1}^{k}((-1)^{i+1}\cos(n\alpha_i)) \right) = 0 \;\; \forall\, n = 5,\ 7,\ \ldots \end{cases} \tag{5.7}$$

So, SHE is stated as SHM to reduce harmonics below the levels instead of suppressing them. SHM is further flexible to involve all harmonics below 49^{h}. Maximum acceptable amplitude for each harmonic is determined in (Voltage characteristics of electricity supplied by public distribution systems, 2001; Harmonics, characteristic parameters, methods of study,

estimates of existing values in the network, 1981) as Table 5.2 and is utilized as the limitation. Conventional 3phase SHM is defined using Eq. (5.7) into inequality equations as:

$$\begin{cases} \left(E_1 = \left(\left(\frac{4}{\pi} \sum_{i=1}^{k} ((-1)^{i+1} \cos(\alpha_i)) \right) - m_a \right) \right) \le L_1 \\ \left(E_n = \left(\frac{4}{n\pi} \sum_{i=1}^{k} ((-1)^{i+1} \cos(n\alpha_i)) \right) \right) \le m_a . L_n \quad \forall n=5,7,...,49 \end{cases} \tag{5.8}$$

Since each harmonic has different allowable level as listed in Table 5.2 and number of variables is normally less than number of SHM equations, Eq. (5.8) is expressed as a cost function. The cost function sets a mitigation priority specifies the importance of lower harmonics for reduction through the weighting factors for the terms corresponding to such lower harmonics.

Also, other terms such as THD can be contributed with different weighting factor. So, SHM-PWM of Eq. (5.8) turn into an optimization issue described as a multivariable one-dimensional function that is merit to be solved with heuristic approaches like Particle Swarm Optimization, Artificial Bee Colony, Imperialist Competitive Algorithm and so on (Beheshtaein, 2013; Kumar, Dasgupta et Chatterjee, 2016). Considering quadratic error term multiplied by a weighting factor for each equation, SHM cost function is written as Eq. (5.9) to control both harmonics and THD.

$$\begin{cases} CF_{SHM}(\alpha_1,...,\alpha_K) = C_1 (F_1 - L_1)^2 + \sum_{n=5,...,49} C_n (F_n - m_a L_n)^2 + C_{THD} THD \\ THD = \dfrac{\sqrt{\sum_{n=5,7,11,...,49} (H_n)^2}}{H_1} \end{cases} \tag{5.9}$$

Eq. (5.9) weighting factors should prioritize sequence of harmonic mitigation. C_1 should have the greatest value as controlling the first harmonic is the primary aim. Other coefficients are adjusted to set higher chance for mitigation for lower order as C_5 is bigger than C_7 and so on.

Despite this, number of proper reduced harmonics is still proportional to number of angles. To have further control on higher harmonics, THD coefficient (C_{THD}) is chosen greater than coefficients of harmonics with less mitigation chance. Then, the cost function coefficients are modeled as:

$$C_1 >> C_5 > C_7 >> ... > C_{THD} > ... > C_{49} \tag{5.10}$$

Table 5.2 Standard Limitation for Non-Triplen/Triplen Amplitudes

Non-Triplen Harmonics		**Triplen Harmonics**	
order (n)	Allowable Level (L_n)	order (n)	Allowable Level (L_n)
5	6%	3	5%
7	5%	9	1.5%
11	3.5%	15	0.5%
13	3%	21	0.5%
17	2%	>21	0.2%
19	1.5%		
23	1.5%		
25	0.2+32.5/n %		

5.3.2 Hybridizing SHM-PWM Based on SHE-PWM

In conventional 3phase SHM or SHE, triplens are removed in phase-to-phase voltages. But, since CMV harmonic content indicates only triplens, they must be also controlled to reduce CMV. As much as triplens are suppressed, CMV is further mitigated. Since all triplens cannot be involved, lower orders that have notable impact on CMV are in higher priority for suppression.

The reason of low triplens elimination is to have further CMV reduction as in mitigation operation they have some amplitude that affects CMV. So, the determined triplens must be

removed to control CMV. The specified non-triplens are also mitigated using Table 5.2 limitation. So, the concepts of harmonic elimination and mitigation are hybridized as Eq. (5.11) by elimination of determined triplens and mitigation of specified non-triplens.

$$\begin{cases} \left(E_1 = \left(\left(\frac{4}{\pi} \sum_{i=1}^{k} (-1)^{i+1} \cos(\alpha_i) \right) - m_a \right) \right) \le L_1 \\ SHM: \left(E_n = \left(\frac{4}{n\pi} \sum_{i=1}^{k} (-1)^{i+1} \cos(n\alpha_i) \right) \right) \le m_a . L_n \ \forall \ \text{n=5,7,...,49} \\ SHE: \left(E_{3n} = \left(\frac{4}{3n\pi} \sum_{i=1}^{k} (-1)^{i+1} \cos(3n\alpha_i) \right) \right) = 0 \ \forall \ \text{n=1,3,5...} \end{cases} \tag{5.11}$$

The Hybrid SHM-PWM formulation of Eq. (5.11) contains harmonics below 49^h to mitigate and eliminate specified non-triplens and triplens, respectively. Hence, it must be expressed as a cost function following the same principle of conventional SHM. As CMV reduction depends on controlling triplens, it is totally cancelled if all of them are removed.

Since the elimination process of each triplen needs one extra angle in Hybrid SHM, all triplen equations cannot be solved; so, only low triplens are assumed. But, THD of remained triplen below 49th ($THD_{Triplen}$) is also assumed in the cost function weighted by C_{THD1} to control total triplen harmonics distortion. As well, THD of non-triplen harmonics ($THD_{Nontriplen}$) weighted by C_{THD2} is to further control total non-triplen harmonics distortion. The cost function of Hybrid SHM-PWM is defined as:

$$\begin{aligned} CF_{SHME}(\alpha_1, \ ..., \ \alpha_K) = & C_1 (E_1 - L_1)^2 + \sum_{n=5, \ ..., \ 49} C_n (E_n - m_a L_n)^2 + \\ & \sum_{n=1, \ ..., \ 15} C_{3n} (E_{3n})^2 + C_{THD1} THD_{Triplen} + C_{THD2} THD_{Nontriplen} \end{aligned} \tag{5.12}$$

The cost function coefficients of Eq. (5.12) are also modeled with the same principle of conventional SHM. Following the direct effect of triplens on CMV, triplens supposed for elimination are equally weighted and chosen greater than non-triplen ones to prioritize CMV reduction. C_{THD1} is also chosen greater than C_{THD2} and non-triplens with lower mitigation

chance to emphasize on CMV reduction. Nevertheless, the weighting factor of first harmonic still has the greatest value. The cost function weighting factors of Hybrid SHM-PWM is:

$$\begin{aligned} &C_1 >> C_{3n} > C_5 > C_7 > \ldots > C_{THD_1} >> C_{THD_2} > \ldots > C_{49} \\ &C_3 = C_9 = \ldots = C_{3n} \qquad \forall\, n = 1,\ 3,\ 5\ldots \end{aligned} \tag{5.13}$$

5.3.3 Switching Angles Calculations Using ABC Algorithm

In order to find number of triplens needs to be eliminated to achieve acceptable CMV reduction, Hybrid SHM is designed in four different angle scenarios. Each scenario includes (*0, 1, 2 & 3*) triplens that requires equivalent angles. Fixed number of angles is involved in all scenarios for non-triplens mitigation and first harmonic regulation. Hybrid SHM equations are separately solved for each scenario when (*8, 9, 10 & 11*) angles are used.

In case of *8* angles, only non-triplens are assumed where (5^{th}, 7^{th}, 11^{th}, 13^{th}, 17^{th}, 19^{th} & 23^{th}) have highest chance for proper mitigation. In other scenarios; as one angle is added, one triplen is removed. So, triplens containing (3^{rd}), (3^{rd} & 9^{th}) and (3^{rd}, 9^{th} & 15^{th}) are respectively eliminated along with determined non-triplens mitigation in each scenario. Artificial Bee Colony (ABC) as a swarm intelligence algorithm with advantages like local minimum detection, low iteration and suitability for multi-objectives is chosen to solve Eq. (5.12) for four scenarios and is done by following steps:

I. Initializing: *D* foods (food is a vector includes angles α_1-α_n) as possible solutions for the optimization problem with *N* dimensions are randomly initialized by Eq. (5.14).

$$\alpha_{ji} = \alpha_i^{\min} + \text{rand}(0,1)(\alpha_i^{\max} - \alpha_i^{\min}) \quad i=1,\ldots,N,\ \&\ j=1,\ldots,D \tag{5.14}$$

α_{ji} is a random amount for i^{th} angle (α_i) in j^{th} food bounded in $\alpha^{\min}{}_i$ and $\alpha^{\max}{}_i$ as lower and upper bands of possible angle.

II. Employed Bees: *D* employed Bees are assigned to evaluate *D* foods and their neighborhoods by Eq. (5.15).

$$V_{ji} = \alpha_{ji} + \varphi(\alpha_{ji} - r_{ij}) \tag{5.15}$$

V_{ji} is new amount for i^{th} angle, α_{ji} and r_{ji} are current and random amounts for i^{th} angle in j^{th} food and φ is randomly bounded in [*-1 1*]. Initialized and new foods of Eq. (5.15) are evaluated by Eq. (5.12) to compute Bees performance (P_j) as:

$$fit_j = \begin{cases} \dfrac{1}{1+f_j} & f_j > 0 \\ 1+\left|f_j\right| & f_j < 0 \end{cases}, \quad P_j = \frac{fit_j}{\sum_{j=1}^{D} fit_j} \tag{5.16}$$

Using Eq. (5.16), a limit index is defined to return Bees fitness to initial foods if new foods have weak fitness.

III. Onlooker Bees: according to overall fitness of employed Bees obtained by Eq. (5.16), the other Bees group called onlookers select foods with best fitness. Then, solutions with minimum fitness are further examined to find optimal angles.

IV. Scout Bees: if the limit index of employed and onlooker Bees exceeds a predefined value, related Bee is transformed to scout Bee. Scout Bees move to random foods using Eq. (5.14); so, the chance of new solutions is increased by evaluating entire area of the problem search-space. ABC is implemented with initial parameters presented in Table 5.3 to compute the switching angles in four scenarios. Figure 5.3 shows the calculated angles of Hybrid SHM using ABC for four scenarios.

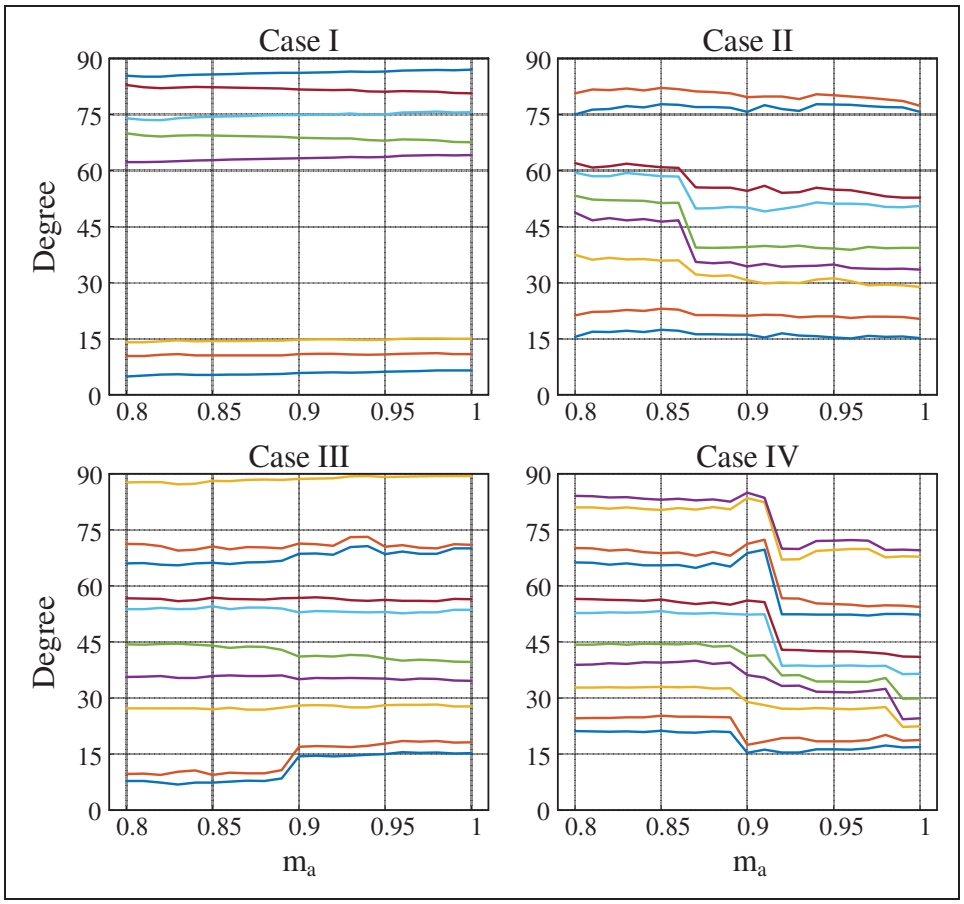

Figure 5.3 Obtained switching angles for four scenarios in Hybrid SHM-PWM; case I, II, III & IV: 8, 9, 10 & 11 angles, respectively

Table 5.3 Initialization of ABC Algorithm

Number of Bees and foods	3000 & 1500
Limit index	2950
Maximum iteration	3000
α_i	[0 π/2]
Number of Bees and foods	3000 & 1500

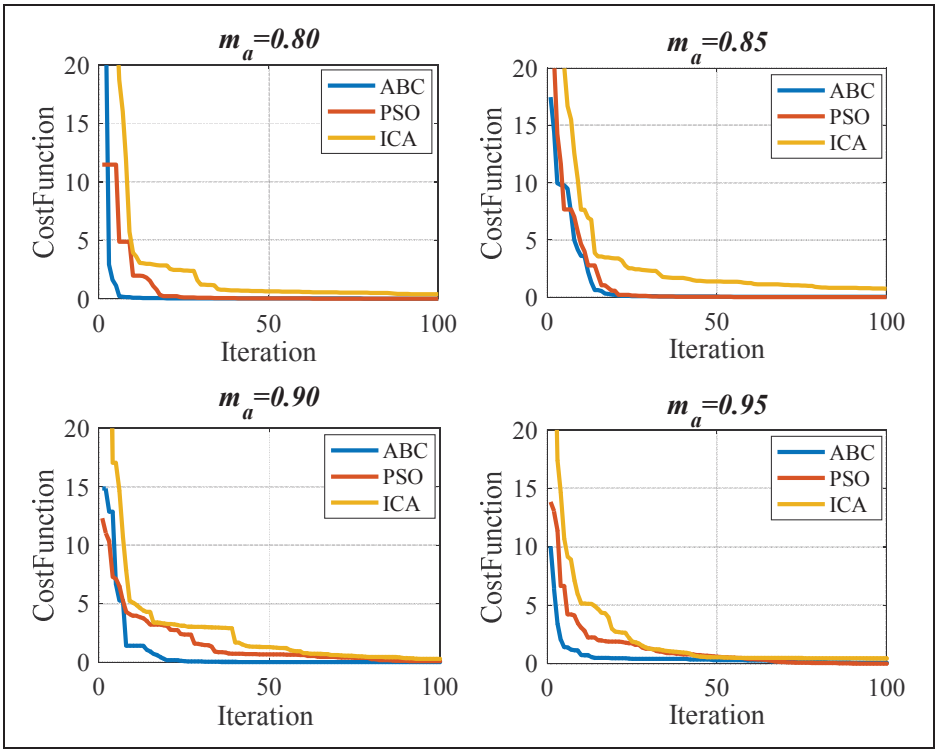

Figure 5.4 Comparison results of ABC, PSO and ICA to calculate the switching angles for different values of modulation index including m_a=*0.80*, m_a=*0.85*, m_a=*0.90* and m_a=*0.95*

The optimization performance of ABC in terms of error and time is compared with Particle Swarm Optimization (PSO) and Imperialist competitive Algorithm (ICA) to ensure that the obtained switching angles are optimally calculated. This comparison is done for different modulation indexes including m_a=*0.80*, m_a=*0.85*, m_a=*0.90* and m_a=*0.95* to cover the whole variation range.

The corresponding comparison results for the first *100* iteration are depicted in Figure 5.4. The simulation results of the optimization competition in Figure 5.4 disclose that ABC is much faster and accurate than PSO and ICA. Thanks to the ABC, the calculated angels of Hybrid SHM have the most optimum values where all desired control objectives including CMV magnitude reduction and the selected harmonics amplitudes mitigation/elimination are perfectly fulfilled.

5.4 Harmonic Spectrum and CMV Reduction Analyses

5.4.1 Harmonic Amplitudes and Voltage THD Analysis

SHM is hybridized based on SHE to benefit of both harmonic mitigation and elimination aimed to reduce CMV by elimination of triplens and to control output harmonic by mitigation of non-triplens. Thanks to flexibility of Hybrid SHM, $THD_{Triplen}$ and $THD_{Nontriplen}$ are also considered in the same cost function to have extra control on the remained harmonics. This section presents some harmonic analyses to survey the performance of Hybrid SHM-PWM. Figure 5.5 shows the worst case triplens between 3^{rd}-to-45^{th} of four scenarios in comparison to Table 5.2. As it is shown in Figure 5.5, the worst case amplitudes of non-eliminated triplens are decreased as more angles are involved for triplen cancelation. The non-eliminated triplens are notably reduced in case IV where *3* triplens (3^{rd}, 9^{th} & 15^{th}) are removed. Thus, not only determined triplens are eliminated but also the distortion of higher orders is controlled since $THD_{Triplen}$ is highly prioritized in the cost function. Figure 5.6 shows the worst case non-triplen between 5^{th}-to-49^{th} of four scenarios that harmonics (5^{th}, 7^{th}, 11^{th}, 13^{th}, 17^{th}, 19^{th} & 23^{rd}) are satisfactorily mitigated with respect to Table 5.2. The harmonic distortions of higher non-triplens are almost similar in all scenarios which indicate the capability of Hybrid SHM-PWM in controlling the non-triplen harmonic distortion using only seven angles in all scenarios. In order to further scrutinize harmonics amplitudes of four scenarios, THD of branch and line voltages and CMV (THD_{Branch}, THD_{Line} & $THD_{Triplen}$) are also analyzed. Figure 5.7 shows THD_{Branch}, THD_{Line} and $THD_{Triplen}$ versus modulation index. Since the difference between THD_{Branch} and THD_{Line} is triplen harmonics, $THD_{Triplen}$ will be:

$$(THD_{Triplen})^2 = (THD_{Branch})^2 - (THD_{Line})^2 =$$
$$THD_{Triplen} = \sqrt{(THD_{Branch} - THD_{Line})(THD_{Branch} + THD_{Line})} \quad (5.17)$$

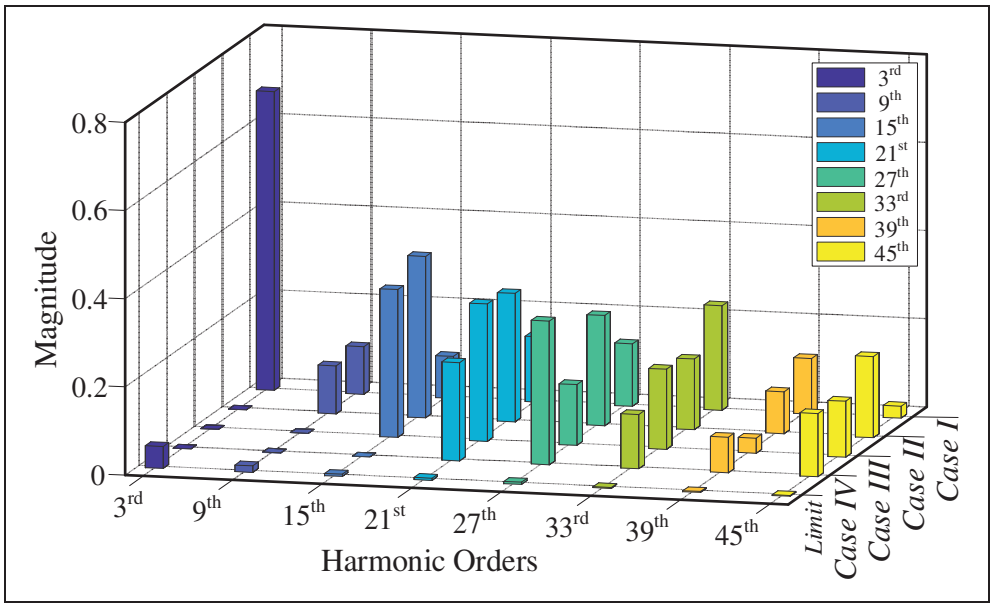

Figure 5.5 Worst case triplen harmonics between 3rd-to-45th in four angle scenarios of Hybrid SHM-PWM compared to Table 5.2

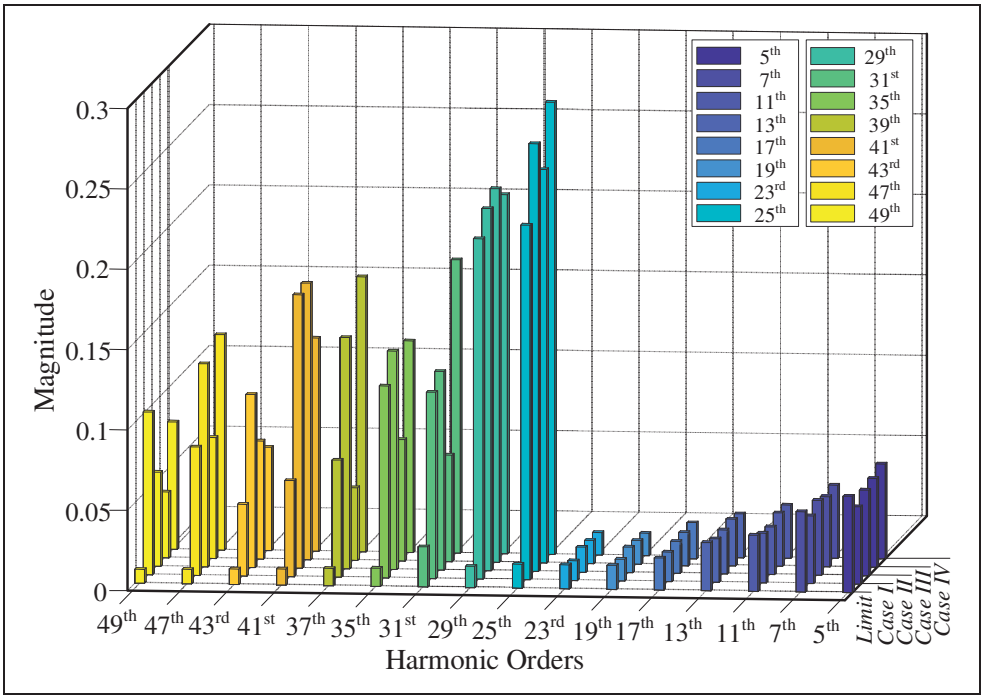

Figure 5.6 Worst case non-triplen harmonics between 5th-to-49th in four angle scenarios of Hybrid SHM-PWM compared to Table 5.2

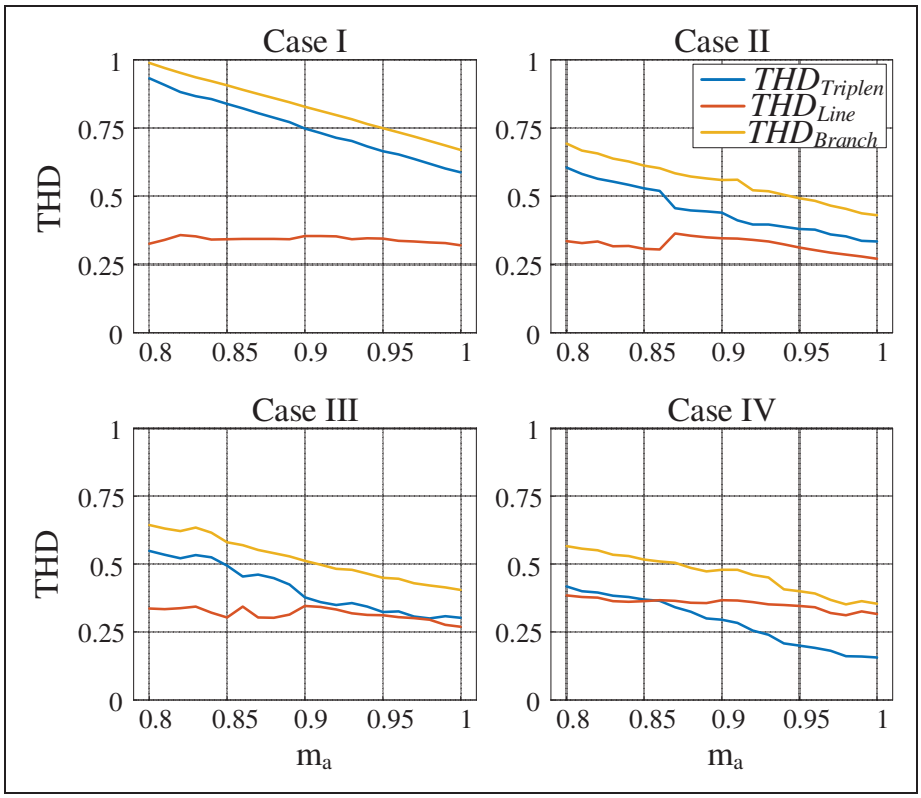

Figure 5.7 Phase, line and CMV THD in all scenarios of Hybrid SHM-PWM

According to Eq. (5.17), minimization of $THD_{Triplen}$ converges THD_{Branch} and THD_{Line}. The comparison of THD_{Branch}, THD_{Line} and $THD_{Triplen}$ of Figure 5.7 shows the greatest triplen harmonics distortion appears in case I where no triplen is removed. By cancelling more triplens and controlling higher order ones; $THD_{Triplen}$ is properly minimized in the last scenario where 3 triplens (3^{rd}, 9^{th} & 15^{th}) are removed. Also, it is clear that total non-triplen harmonic distortion has approximately similar level in all scenarios. So, Hybrid SHM is able to deal with non-triplen distortion using same number of angles in all scenarios. In other words, the extra angles of each scenario are just used for controlling triplen harmonics.

5.4.2 Root Mean Square (RMS) Analysis of CMV Reduction

According to the proposed Hybrid SHM, low triplens are eliminated and distortion of higher ones is controlled to mitigate CMV. By controlling triplen harmonics, CMV is subsequently reduced as its pulses widths are becoming smaller which makes less effective value and can

be shown through RMS measurement. Figure 5.8 shows RMS of CMV for all scenarios using true RMS analysis to accurately measure amount of CMV reduction. Based on RMS analysis, CMV is reduced as more triplens are controlled in Hybrid SHM-PWM.

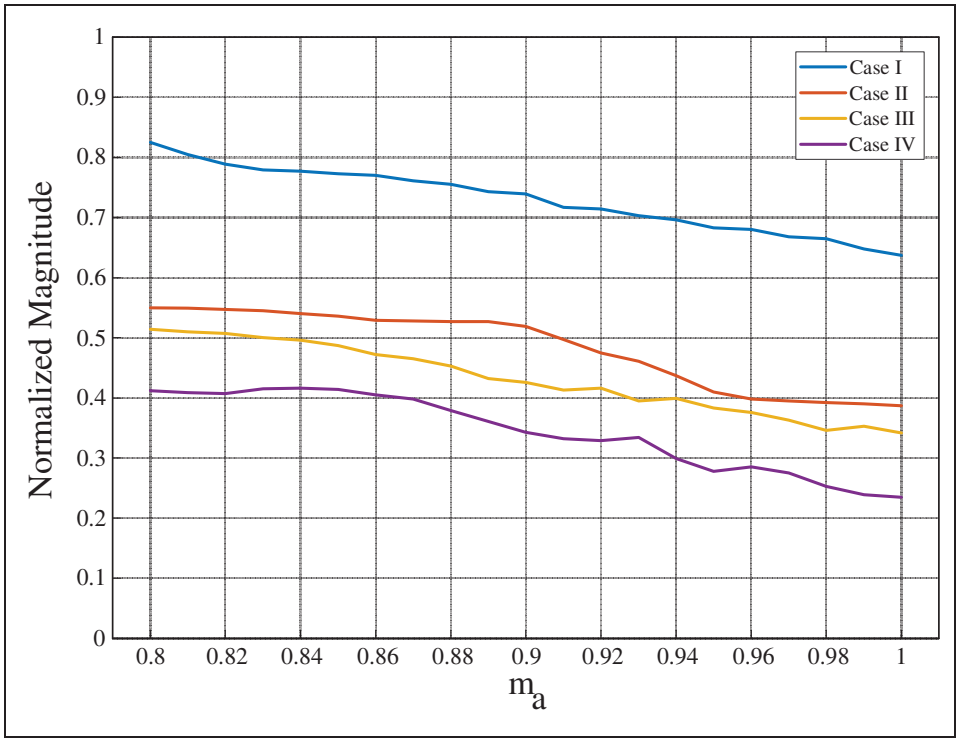

Figure 5.8 CMV true RMS for four angle scenarios of Hybrid SHM-PWM

5.4.3 Hybrid SHM-PWM versus SHM-PWM and SHE-PWM

Hybrid SHM is compared to pure SHE and SHM when they are designed to include both determined triplens and non-triplens using 11 angles as case IV. Figs. 5.9-a and 5.9-b show the worst case harmonics and THD; respectively, when SHE, SHM and Hybrid SHM are accordingly designed using 11 angles like case IV to deal with triplens (3^{rd}-to-15^{th}) and non-triplens (5^{th}-to-23^{rd}). For pure SHE, harmonics between 3^{rd}-to-23^{rd} are eliminated as there is no control on higher orders. For pure SHM, all harmonics between 3^{rd}-to-49^{th} are involved; but, only determined harmonics have chance of proper mitigation.

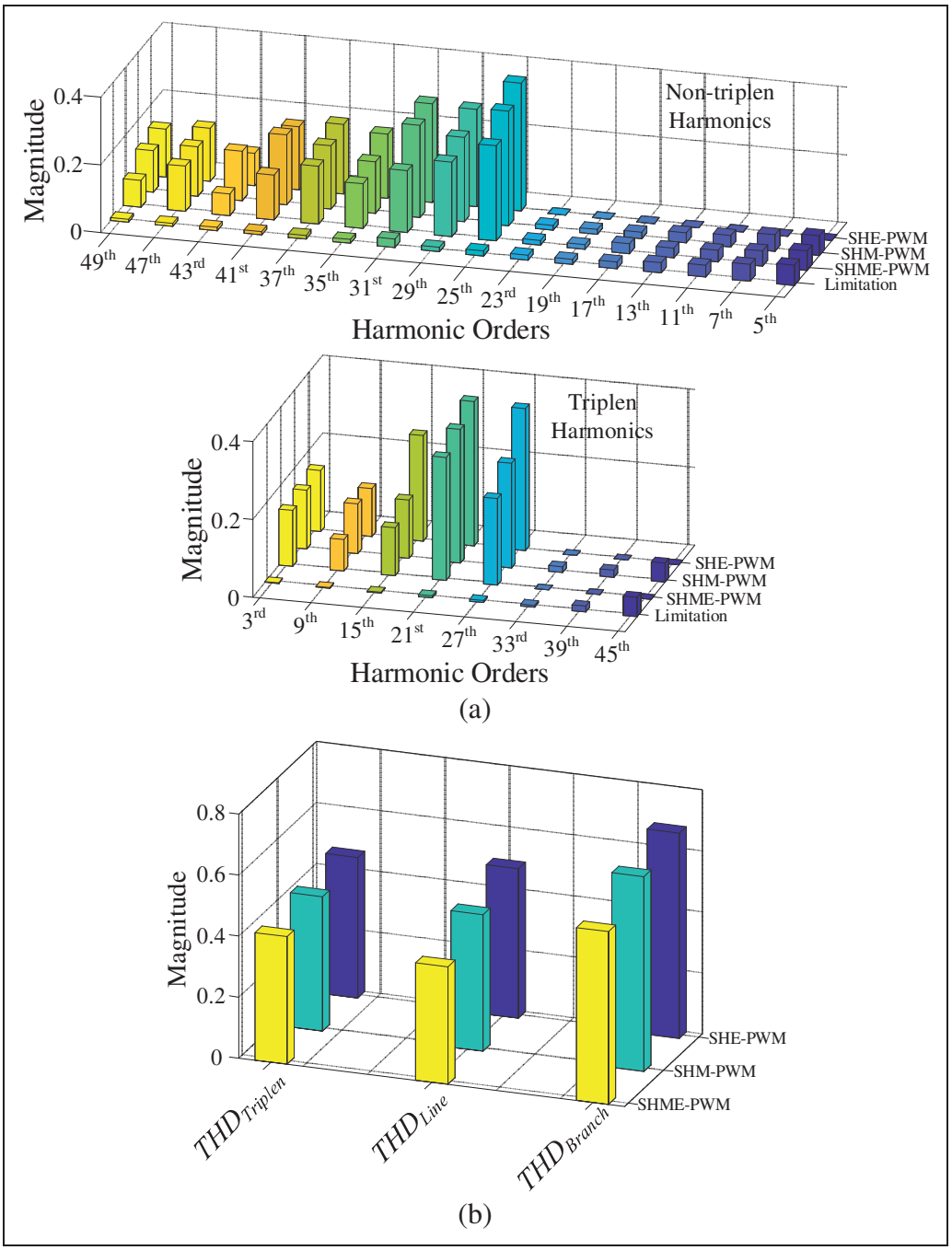

Figure 5.9 Worst case triplens and non-triplens and THD of SHE, SHM and Hybrid SHM designed according to case IV, (a) worst case of triplens and non-triplens, (b) worst case of THD_{Branch}, THD_{Line} and $THD_{Triplen}$

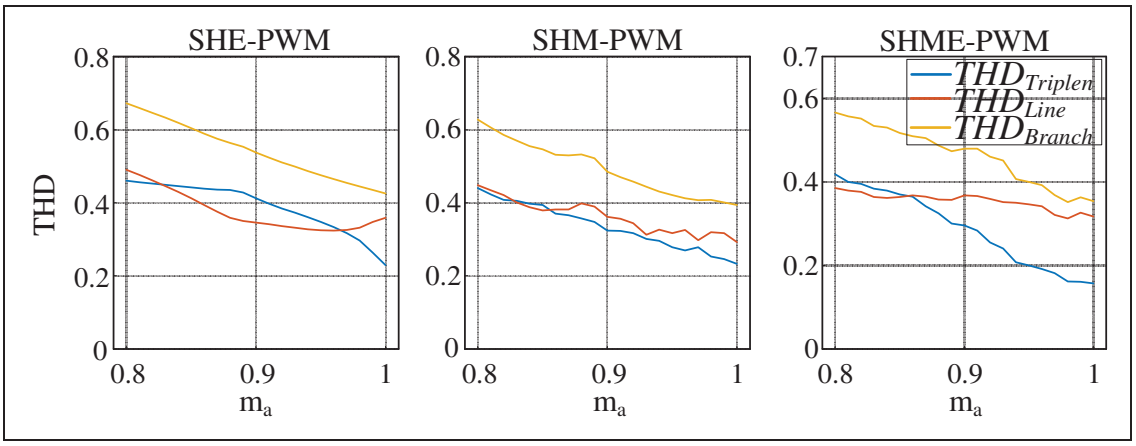

Figure 5.10 Phase, line and CMV THD of SHM-PWM, SHM-PWM and Hybrid SHM-PWM designed according to case IV

In Hybrid SHM, determined triplens are eliminated and specified non-triplens are mitigated and total harmonic distortion is also controlled thanks to flexibility of defining equations through a cost function. As it is clear, both SHM and Hybrid SHM achieve better triplen and non-triplen THD compared to SHE as they are further flexible in dealing with higher orders whereas SHE increases their amplitudes. Even though both SHM and Hybrid SHM have same THD for non-triplens, Hybrid SHM has better THD for triplens as low orders are removed and higher orders distortion is controlled. It is due to the fact that Hybrid SHM provides enough flexibility to consider different objectives terms including both harmonic elimination and mitigation at the same time. Figure 5.10 illustrates THD_{Branch}, THD_{Line} and $THD_{Triplen}$ versus modulation index which clearly demonstrates Hybrid SHM has further harmonic profile efficiency over pure SHE and SHM.

5.5 Simulation and Experimental Results Discussion and Analysis of Proposed Hybrid SHM-PWM

All angles scenarios are tested experimentally on 3phase 3level NPC inverter using the real-time hardware controller dSpace 1104 to send the generated PWM signals of the Hybrid SHM technique to the inverter switches through its associated I/Os; so, to validate the performed theoretical analyses. The parameters used in experimental test are listed in Table IV. Fig. 5.11 shows the experimental setup of 3phase 3level prototype of the NPC inverter

which is tested under the proposed Hybrid SHM-PWM modulation technique. The NPC DC-Bus capacitors are perfectly self-voltage balanced to half of input DC source voltage by the right implementation of Hybrid SHM which leads to the symmetrical phase voltage waveforms. Fig. 5.12-(a, b, c and d) illustrates line, phase, branch voltages and CMV of all switching angles scenarios of Hybrid SHM-PWM and the harmonic contents of these mentioned voltages. The harmonic content of line, phase, branch voltages and CMV are attained from experimental analysis using a power analysis and the obtained results are depicted in Matlab environment to have all these mentioned voltages harmonic contents as one figure so as it is easier to compare them.

The three-level branch voltages of each case of switching angle scenario signally illustrate that the dc capacitors of 3phase NPC inverter are perfectly balanced to the half of dc input voltage. Also, the branch voltages display number of involved switching angles where there are 8, 9, 10 and 11 switching angles in the branch voltages of case I, case II, case III and case IV; respectively. The switching angles are distributed in the region of [0, $\pi/2$] of branch voltage as it is described in Fig. 5.2 and for other regions; [$\pi/2$, π], [π, $3\pi/2$] and [$3\pi/2$, 2π], the phase shifted of switching angles of [0, $\pi/2$] are distributed where an odd quarter-wave symmetry branch voltage waveform is shaped. As a result, this symmetrical waveform is also occurred for phase voltage which guarantees self-voltage balancing of DC-Bus capacitors voltages of 3phase NPC inverter.

Also, the obtained experimental results of the harmonic contents of the line, phase, branch voltages as well as CMV in the four switching angles scenario clearly show that the selected triplen and non-triplen are eliminated and mitigated, respectively. It is obvious that the triplen THD has been decreased as more triplens are eliminated which would results in CMV magnitude reduction. The line voltage THD which just includes the non-triplen harmonics is approximately identical in all angles scenario. It must be noticed that all triplen harmonic are self-cancelled in line voltage due to 120 degree phase shifts among 3phase NPC inverters' legs.

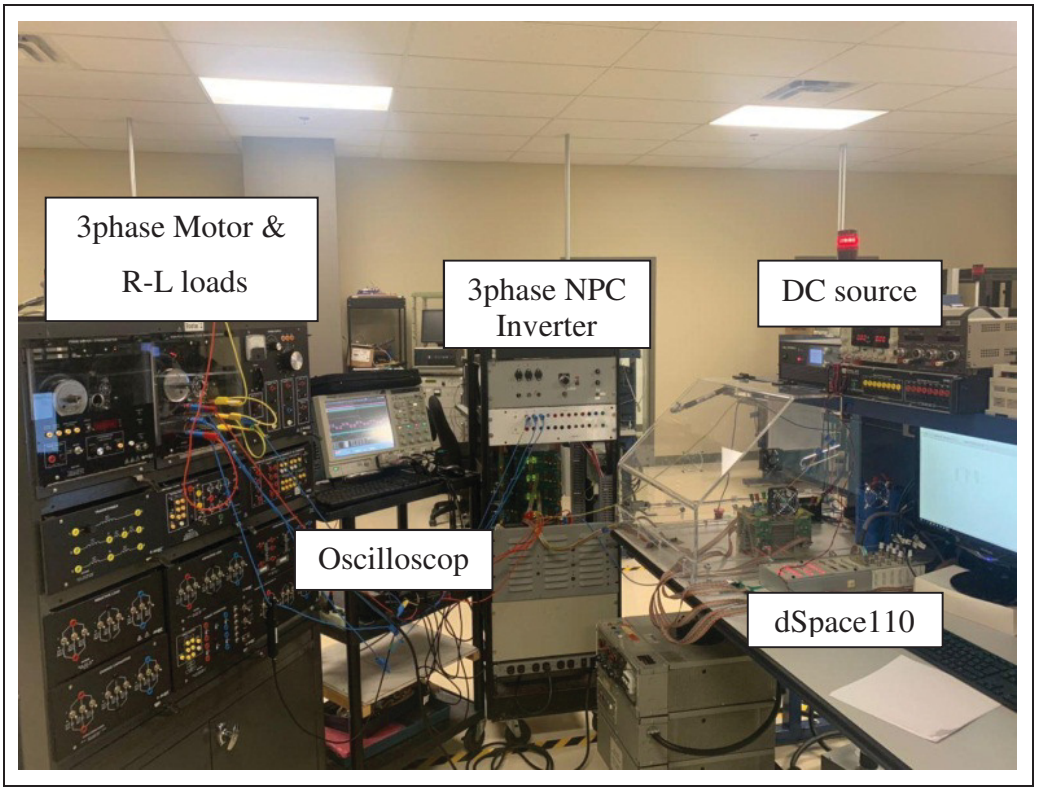

Figure 5.11 The experimental setup of the 3phase 3level prototype of NPC inverter tested under Hybrid SHM-PWM

Table 5.4 Parameters Values Utilized in Experimental Tests of 3Phase NPC

Input DC voltage (2*E*)	300 V
Fundamental frequency	50 Hz
Switching frequency (each scenario)	400, 450, 500 & 550 Hz
DC-Bus capacitor (C_1 & C_2)	650 µF
Output (*R* & *L*) load	80 Ω & 50 mH
Amplitude modulation index (m_a)	0.8
Sampling time (*Ts*)	80US

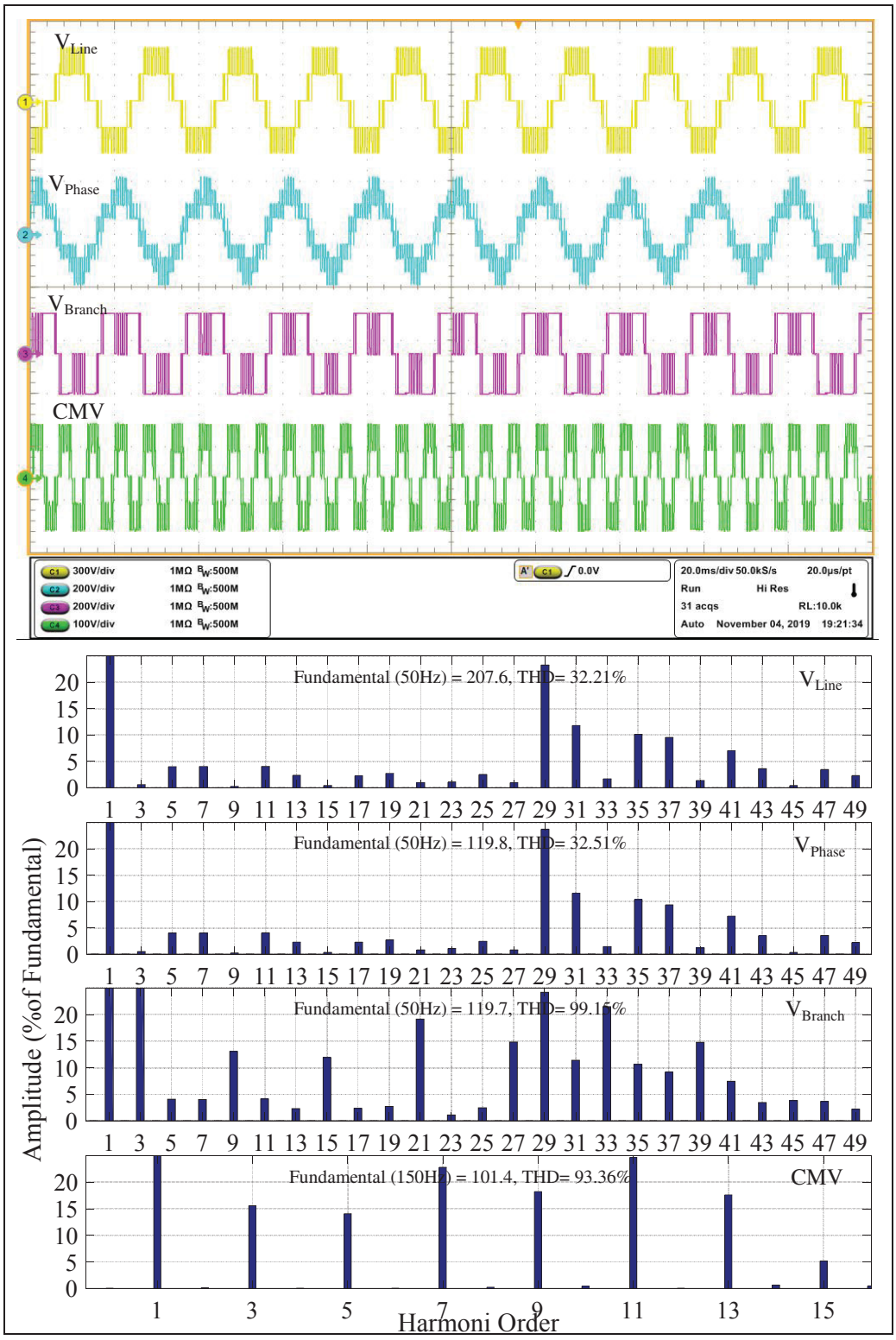

Figure 5.12-a Experimental results of line, phase, branch voltages and CMV and the harmonic contents (from up to down) in all scenarios of Hybrid SHM, Case I

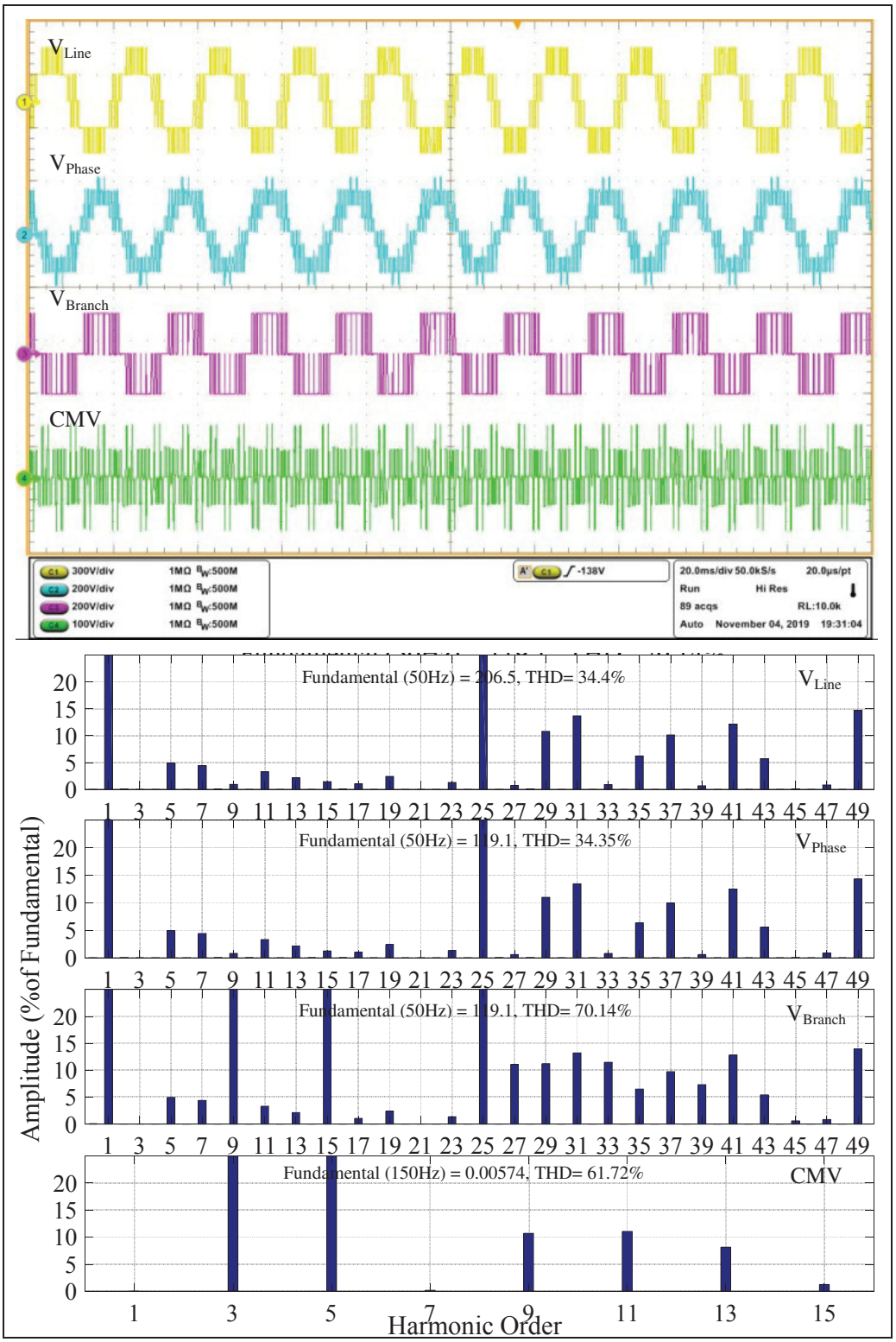

Figure 5.12-b Experimental results of line, phase, branch voltages and CMV and the harmonic contents (from up to down) in all scenarios of Hybrid SHM, Case II

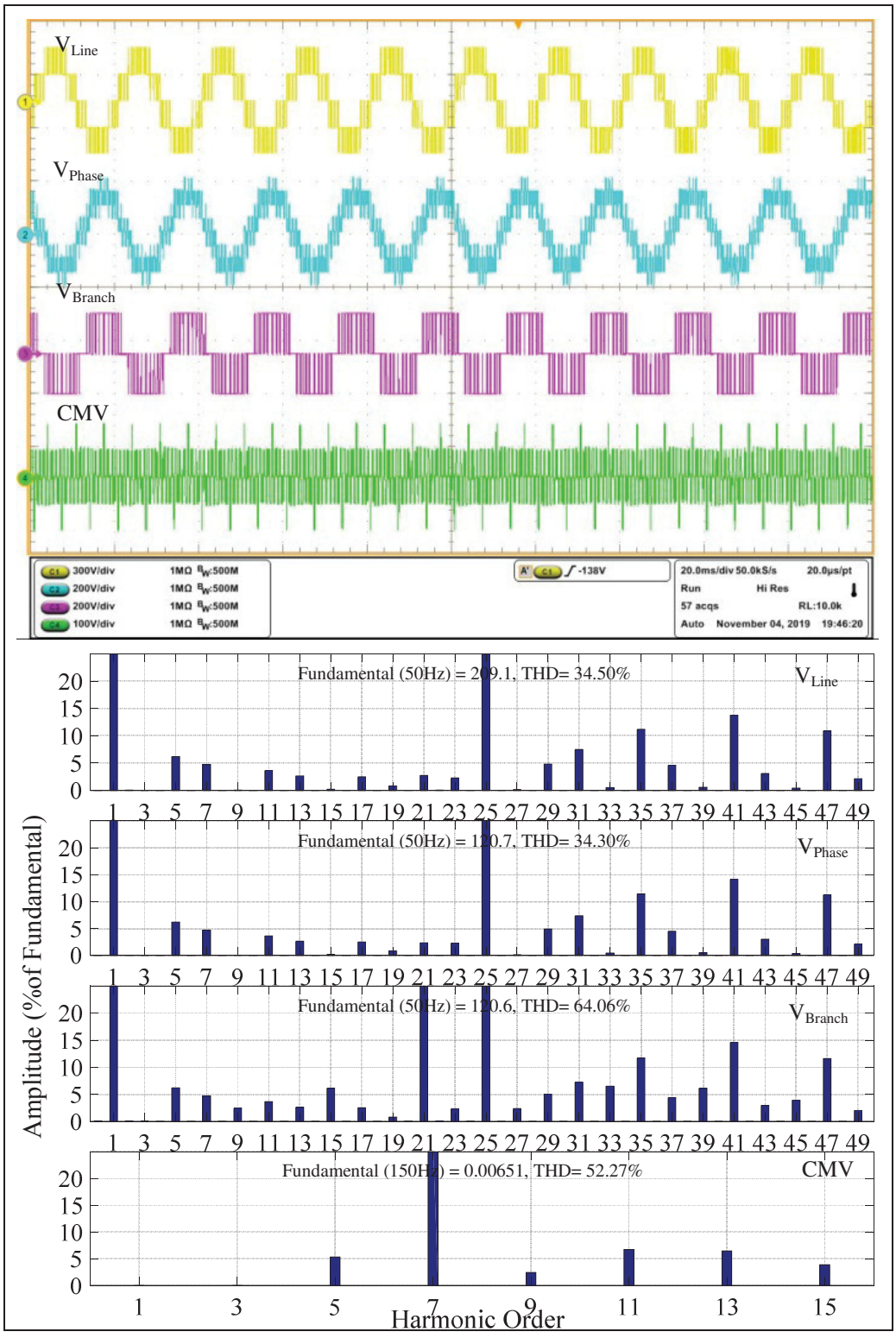

Figure 5.12-c Experimental results of line, phase, branch voltages and CMV and the harmonic contents (from up to down) in all scenarios of Hybrid SHM, Case III

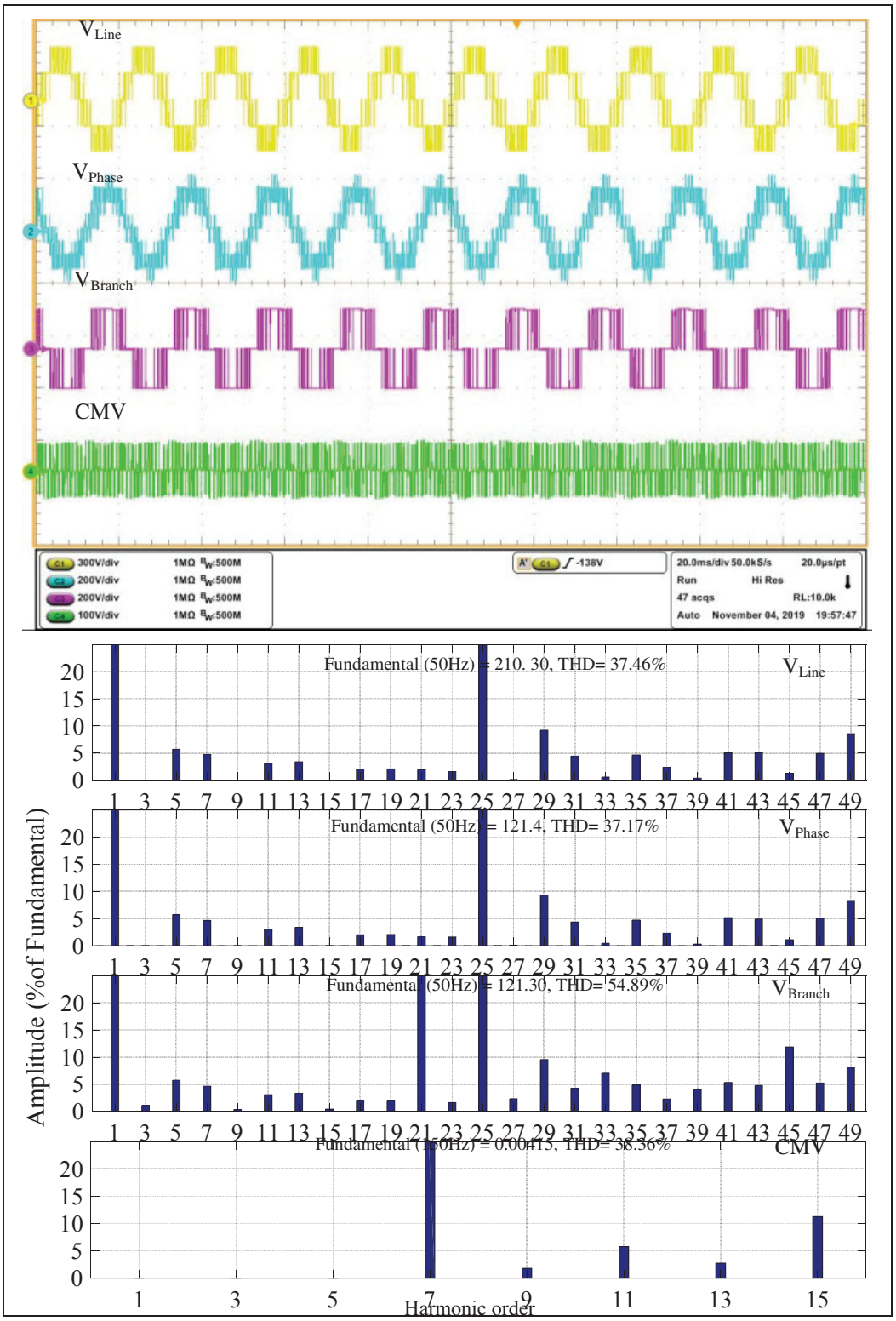

Figure 5.12-d Experimental results of line, phase, branch voltages and CMV and the harmonic contents (from up to down) in all scenarios of Hybrid SHM, Case IV

Considering these two points it can be concluded that the switching angles of Hybrid SHM-PWM have been calculated optimally as the CMV magnitude is successfully reduced and output voltage harmonic distortion is controlled. As it is clear, CMV magnitude has been decreased by further decreasing triplen harmonic distortion so as CMV RMS value is reduced by 60% in case IV compared to case I. While there is a notable mount of CMV magnitude in case I which forms five-level voltage because of no control on triplen harmonic, CMV magnitude is remarkably reduced in case IV to a three-level voltage as selected triplen harmonics are eliminated and total triplen harmonic distortion is also controlled. Indeed, the CMV reduction in Hybrid SHM-PWM appears as decreasing voltage levels and reduction of CMV pulses widths where CMV pulses are becoming thinner and less effective by elimination more triplens; so, RMS value of CMV magnitude is decreased.

Moreover, it must be mentioned that it is expected CMV is further reduced by eliminating more low order triplen harmonics amplitudes and by more decreasing total triplen harmonic distortion. To this end, CMV is further decreased as more switching angles are involved in the proposed Hybrid SHM-PWM technique. Significant reduction of CMV leads to the identical waveforms for both branch voltage and phase voltage according to Eq. (5.1) ($V_{ng}=V_{xn}-V_{xg}$; $x=A, B \& C$) where both voltage will be a three-level voltage waveform. it is due to the fact that CMV is the only difference between branch voltage and phase voltage and since branch voltage is predefined as a three-level voltage waveform, phase voltage will also be like branch voltage whenever CMV is approximately cancelled.

5.6 Conclusions

In this work, Hybrid SHM is proposed by combination of both harmonic elimination and mitigation to reduce CMV magnitude and control harmonic distortion of output voltage. As CMV harmonic modeling is only composed of triplens, the specified triplens are eliminated to reduce CMV through controlling its pulses widths. Indeed, triplen elimination makes CMV pulses widths smaller which results in less RMS value. The determined non-triplens are mitigated through the same cost function as well. The theoretical and experimental

analyses are conducted on 3phase NPC inverter to prove the reliable performance of Hybrid SHM in CMV reduction. But, the proposed technique is a suitable alternative of pure SHE or SHM even for other applications and inverters since it can control more harmonics in same switching frequency.

CHAPTER 6

PACKED E-CELL (PEC) CONVERTER TOPOLOGY OPERATION AND EXPERIMENTAL VALIDATION

Mohammad Sharifzadeh [a], Kamal Al-Haddad [b]

[a, b] Department of Electrical Engineering, École de Technologie Supérieure,
1100 Notre-Dame West, Montreal, Quebec, Canada, H3C 1K3

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Abstract

This work proposes a novel single-DC source multilevel inverter called Packed E-Cell topology to achieve nine-level with noticeably reduced components count while DC capacitors are actively balanced. The nine-level Packed E-Cell (PEC9) is composed of seven active switches, two DC capacitors that are shunted by a four-quadrant switch to from the E-Cell, and it makes use of a single DC-link. With the proper design of corresponding PEC9 switching states, the DC capacitors are balanced using redundant charging/discharging states. Since the shunted capacitors are horizontally extended, both capacitors are simultaneously charged or discharged with redundant states so as only the auxiliary DC-link voltage needs to be sensed and regulated to half of input DC source voltage and consequently DC capacitors voltages are inherently balanced to one quarter of the DC bus voltage. To this end, an active capacitor voltage balancing integrated to the level shift half parabola carrier PWM technique has been designed based on the redundant charging/discharging states to regulate the DC capacitors voltages of PEC9. Furthermore, using E-Cell not only reduces components count but also the proposed topology permits multi AC terminal operation. So, five-level inverter operation can be achieved during four-quadrant switch fault which confer to the structure high reliability. Theoretical analysis as well as experimental results are presented and

discussed showing the basic operation, multi-functionality as well as the superior performance of the proposed novel PEC9 inverter topology.

6.1 Introduction

Lately, Multilevel Voltage Source Inverters (MVSIs) have been emerged as a competitive power converter in various industrial applications including uninterruptible power supply, renewable energy integration, electrical drives, active power filters, etc (Norambuena et al., 2018; Vahedi et al., 2017). MVSIs comprise more semiconductor devices, auxiliary capacitors powered by DC sources. The latter not only produce more voltage levels but also capable of operating at high power ratio as switches endure lower voltage stress (Abu-Rub et al., 2010). Neutral Point Clamped inverter (NPC), Flying Capacitors inverter (FC) and Cascaded H-Bridge (CHB) appeared as the first generation of MVSIs promising topologies for industry over bipolar VSIs due to EMI and dv/dt stress reduction, higher reliability and improved output voltage harmonic profile (Arun et Noel, 2017; Babaei et Laali, 2015).

Following development of MVSIs led by tremendous researches that were oriented toward new topologies mainly concentrated on increasing the number of output voltage levels (Barzegarkhoo et al., 2016). As the primarily attempt and being inspired by conceptual of CHB, the hybrid structures of conventional MVSIs such as symmetrical and asymmetrical cascaded topology were utilized for HB, NPC and FC to increase the number of voltage levels and operate with higher efficiency (Castillo, Diong et Biggers, 2017; Roshankumar et al., 2012; Roshankumar et al., 2015; Nami et al., 2011; He et Cheng, 2016). The asymmetrical series connection of half and full bridge has been proposed in (Chattopadhyay et Chakraborty, 2017) for the wide variation of DC-link voltage and level doubling of the network. In (Mariethoz, 2012; Mariethoz, 2014) asymmetrical cascaded of HB of NPC and conventional two-level inverters have been presented with advantages of low switching frequency operation for high voltage cell and high dynamic response. In (Zambra, Rech et Pinheiro, 2010) symmetrical and hybrid asymmetrical cascaded HB and NPC inverter have been compared to investigate their performance from different point of view. As well, a novel

generalized circuit topology of the n-time quadrupled hybrid NPC converter and a new decomposed modulation method was proposed in (Abarzadeh et Al-Haddad, 2019), to multiply the number of output voltage levels of the 5L-HNPC through asymmetrical connection. In comparison to symmetrical cascaded MVSIs which benefit the simple circuit's topology as similar VSIs are combined, the asymmetrical ones have higher efficiency since more voltage levels are attained with less number of cells. Despite this, hybridizing the conventional MVSIs based on the symmetrical and asymmetrical cascaded connection does not optimize the final MVSIs design and it significantly increases number of components and separated DC sources and consequently manufacturing cost (Zambra, Rech et Pinheiro, 2010). Recently, some novel inverter topologies have been introduced to be used as an individual cell in symmetrical and asymmetrical connections. In (Samadaei et al., 2017; Samadaei et al., 2016) a square and an envelope T-Type module has been presented for asymmetrical MVSIs. The K-Type with two DC source has been also reported in (Samadaei, Kaviani, et Bertilsson, 2019) to be used as a module for multilevel structure. However, they suffer from large number of main DC source. Moreover, MVSIs with large number of DC sources are limited to PV applications particularly when they are configured in series (Chattopadhyay et Chakraborty, 2017; Zhang et al., 2018). In (Saeedian, Adabi, et Hosseini, 2017; Samsami, Taheri, et Samanbakhsh, 2017; Lee et al., 2018; Kangarlu et Babaei, 2013; Mokhberdoran et Ajami, 2014) some innovative MVSIs have been proposed to produce notable number of levels as similar as sinusoidal waveform without using asymmetrical and symmetrical connections. But, they have complex structure because of the number of semiconductor devices, gate drivers, DC sources and voltage levels capacitors.

Hence, researchers have focused on establishing optimized MVSIs by making a tradeoff between number of components, voltage levels, structure complexity and replacement of DC sources by appropriate capacitors. Therefore, single-DC source multilevel inverters have been extensively investigated as a competitive and cost-effective topology over other MVSIs which are also the most suitable structure to be used in symmetrical and asymmetrical cascaded connection as each cell has only one DC source (Taghvaie, Adabi, et Rezanejad, 2018; Taghvaie, Adabi et Rezanejad, 2017; Taghvaie, Adabi et Rezanejad, 2016). However,

balancing auxiliary capacitors voltages in single-DC source inverter remains a challenge that must be considered in the design phase by providing adequate charging and discharging paths. In case of single DC source MVSIs, the compact topology has been recognized as a promising structure since the capacitor voltage balancing can be achieved in easier approach and they are much appropriate to be used as the individual cell for series connection (Xiang et al., 2018). Among the compact MVSIs, single-DC source well-known Packed U-Cell (PUC) inverter has been lately attracting lots of attention due to its advantages (Vahedi, Sharifzadeh et Al-Haddad, 2018; Babadi et al., 2017). PUC was introduced in (Ounejjar, Al-Haddad et Gregoire, 2011; Ounejjar, Al-Haddad et Dessaint, 2012) as a hybrid topology combining the advantages of FC and CHB in which the U-Cell are placed in compact structure. PUC was optimally designed using six switches and one DC capacitor to achieve seven-level by adjusting the auxiliary capacitor to one third of DC input voltage, or achieving five-level output voltage while the capacitor voltage is self-balanced using redundant switching states (Vahedi, Labbé et Al-Haddad, 2016). The main complicated issue of PUC topology is capacitors voltages regulation when it is extended to employ an important number of U-Cells. Since U-Cells create individual auxiliary DC-link, capacitors are not simultaneously charging and/or discharging with the redundant states for a particular voltage level. Thus, utilization of a complex controller is inevitable to achieve the capacitor voltage balancing in the extended PUC (Vahedi et Al-Haddad, 2016). Even in the case of external controller, as individual capacitors voltages should be adjusted to different voltage levels, separate sensors are needed to measure their voltages and consequently tuning the weighting factors of voltages regulator controllers becomes challenging.

In this paper, a novel single-DC source inverter is presented where the U-Cells are replaced by E-Cell in the packed structure; therefore, number of the auxiliary DC-link and components are reduced by horizontal extension of shunted capacitors. The proposed Packed E-Cell (PEC) inverter is a deep pivotal modification on previously introduced Packed U-Cell (PUC), which permitted to have higher capability in which two U-Cells are replaced by one E-Cell; so, not only nine voltage levels are achieved but also capacitors voltages are actively balanced by redundant switching states. As a result of using E-Cell and horizontal extension

of capacitors, both DC-link capacitors are simultaneously charged or discharged with redundant states which can be effectively used to guarantee capacitors voltages regulation without need of external and complex controller. To this end, an active capacitor voltage balancing integrated into half parabola carrier has been designed to use the redundant state for capacitor voltage balancing. Moreover, only DC-link voltage needs to be regulated to half of input voltage and the capacitors voltages are inherently balanced to one quarter of main DC source voltage. Another interesting feature of PEC9 is its capability of operating during fault occurrence on four-quadrant switch as a five- or seven-level inverter depends on regulating DC-link to half or one third of the input voltage. This feature recognizes PEC as a reliable single-DC source converter as five/seven/nine-level can optimally be designed and achieved compared to other topologies. Therefore, in addition to the prominent and exclusive advantages of PEC inverter, it can also cover PUC operation and keeping its benefits because of having multi AC terminal access. The proposed Packed E-Cell inverter topology as well as the capacitors voltages balancing method integrated to the modulation technique have been filed as U.S. provisional patent application No. 62 / 728,734. The Packed E-Cell inverter topology and switching states are fully described in section 6.2. Section 6.3 explains the proposed active voltage balancing algorithm integrated into PWM technique. A comparative component study on nine-level inverters is presented in section 6.4 to prove the optimum design of PEC9. Experimental results are presented and discussed in section 6.5 meant to evaluate the capacitors active voltage balancing and converter performance under different operation conditions.

6.2 Proposed Nine-Level Packed E-Cell (PEC9)

6.2.1 PEC9 Circuit Topology

The proposed PEC9 structure is constituted by six active bidirectional current devices S1, S2, S3, S4, S5 and S6; one four-quadrant switch S7, one DC source Vdc, and two capacitors C1 and C2 to form nine-level single-phase converter topology. The designed topology is based on the idea of using E-Cell type of connection to develop the auxiliary capacitor in a row horizontal structure as depicted in Figure 6.1. The four-quadrant type of switch is connected

between the midpoint of two capacitors and the inverter AC terminal point. In E-Cell nine-level connection, DC capacitors are set in row to create single auxiliary DC-link that both capacitors can be charging and discharging accordingly. As a result, both capacitors are synchronized during charging or discharging with redundant states required balancing the auxiliary DC-link to inherently set the shunted capacitors voltages to the desired voltage level. E-Cell also makes multi-output voltage levels due to the four-quadrant switches that five, seven or nine-level are obtainable without changing the structure.

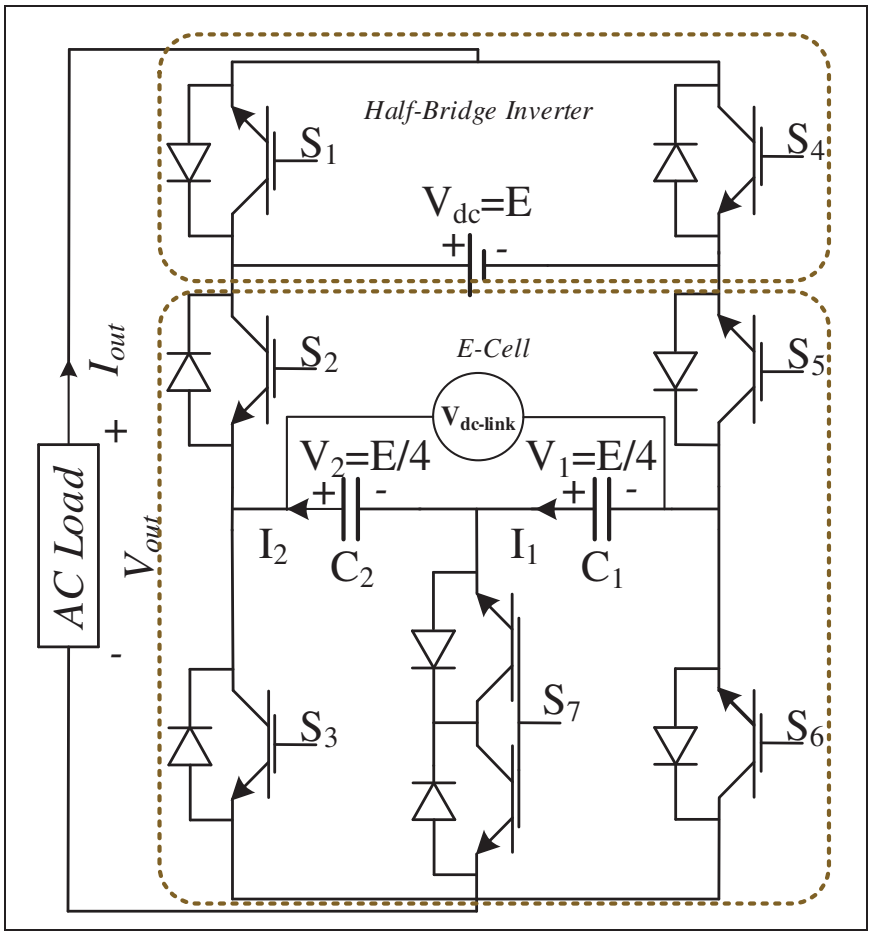

Figure 6.1 Proposed nine-level Packed E-Cell (PEC9) inverter topology

6.2.2 PEC9 Switching States

With the right selection of switching states, each of C_1, C_2 capacitors voltages (V_1, V_2) is balanced to one quarter of DC input voltage (V_{dc}) so as PEC9 generates nine-level waveform.

Table 6.1 shows switching states possibility of PEC9 inverter. Based on Table 6.1, switches (S_1, S_4), (S_2, S_5) as well as (S_3, S_6, S_7) are operating as complementary. The mechanism of charging and discharging shunted capacitors C_1, C_2 depends on the load current direction. If the current flows into the capacitor from positive side, it is charging if not it is discharging. Also, the capacitor voltage does not change if it is bypassed. The states of capacitors voltages are illustrated in Table 6.1.

They have one charging and discharging state in $\pm E/2$ as a result of horizontal extension of auxiliary DC-link. Indeed, this is one of the PEC advantages that can provide same charging and/or discharging states for both capacitors by using the E-Cell. For output levels $\pm E/4$ *and* $\pm 3E/4$ one capacitor in charging or discharging condition, they are not affected by the switching states of the levels 0 and $\pm E$. Figure 6.2 depicts the conducting paths of capacitors for the switching states of PEC9 as presented in Table 6.1. Note that the upper switches (S_1 & S_4) connected to the DC source are switched at low frequency. The other switches operate at the switching frequency. While two upper switches (S_1 & S_4) should withstand the DC input voltage, the auxiliary DC-link voltage that is half of the DC input across the E-Cells 6 remaining switches; so, similar lower voltage switches can be selected for high frequency part.

6.2.3 Multi-Level Terminal Capability of PEC9 Topology

As mentioned, E-Cell provides multilevel output AC terminal voltage where different number of voltage levels without changing in topology is attainable which make PEC9 a reliable configuration. For example, PEC9 can continue its operation if a fault occurs on four-quadrant switch. In this case, five or seven output voltage levels are achievable as DC-link voltage is balanced to half or one third of DC supplies input voltage. Assuming the open circuit state for four-quadrant switch during fault occurrences, the capacitors are assumed as one equivalent capacitor C_{eq} having half the value of C_1 and C_2 since they are connected in series. The DC-link voltage is regulated to half by redundant switching states for five-level inverter or to one-third using current controller to produce seven voltage levels.

Table 6.1 PEC9 Switching States (↑ : Charging, ↓ : Discharging, – : No Effect)

State	S1	S2	S3	S4	S5	S6	S7	I_{out}	C_1	C_2	V_{out}
1	1	0	0	0	1	1	0	> 0	–	–	V_{dc}=+E
2	1	0	0	0	1	0	1	> 0	↓	–	V_{dc}-V_1=+3E/4
3	1	0	1	0	1	0	0	> 0	↓	↓	V_{dc}-V_1-V_2=+E/2
4	1	1	0	0	0	1	0	> 0	↑	↑	V_1+V_2=+E/2
5	1	1	0	0	0	0	1	> 0	–	↑	V_2=+E/4
6	0	0	0	1	1	1	0	> 0	–	–	0
7	1	1	1	0	0	0	0	> 0	–	–	0
8	0	0	0	1	1	0	1	> 0	↓	–	-$V_{1=}$-E/4
9	0	1	0	1	0	1	0	> 0	↑	↑	-V_{dc}+V_1+V_2=-E/2
10	0	0	1	1	1	0	0	> 0	↓	↓	-V_1-V_2=-E/2
11	0	1	0	1	0	0	1	> 0	–	↑	-V_{dc}+V_2=-3E/4
12	0	1	1	1	0	0	0	> 0	–	–	V_{dc}=-E
13	1	0	0	0	1	1	0	< 0	–	–	V_{dc}=+E
14	1	0	0	0	1	0	1	< 0	↑	–	V_{dc}-V_1=+3E/4
15	1	0	1	0	1	0	0	< 0	↑	↑	V_{dc}-V_1-V_2=+E/2
16	1	1	0	0	0	1	0	< 0	↓	↓	V_1+V_2=+E/2
17	1	1	0	0	0	0	1	< 0	–	↓	V_2=+E/4
18	0	0	0	1	1	1	0	< 0	–	–	0
19	1	1	1	0	0	0	0	< 0	–	–	0
20	0	0	0	1	1	0	1	< 0	↑	–	-$V_{1=}$-E/4
21	0	1	0	1	0	1	0	< 0	↓	↓	-V_{dc}+V_1+V_2=-E/2
22	0	0	1	1	1	0	0	< 0	↑	↑	-V_1-V_2=-E/2
23	0	1	0	1	0	0	1	< 0	–	↓	-V_{dc}+V_2=-3E/4
24	0	1	1	1	0	0	0	< 0	–	–	V_{dc}=-E

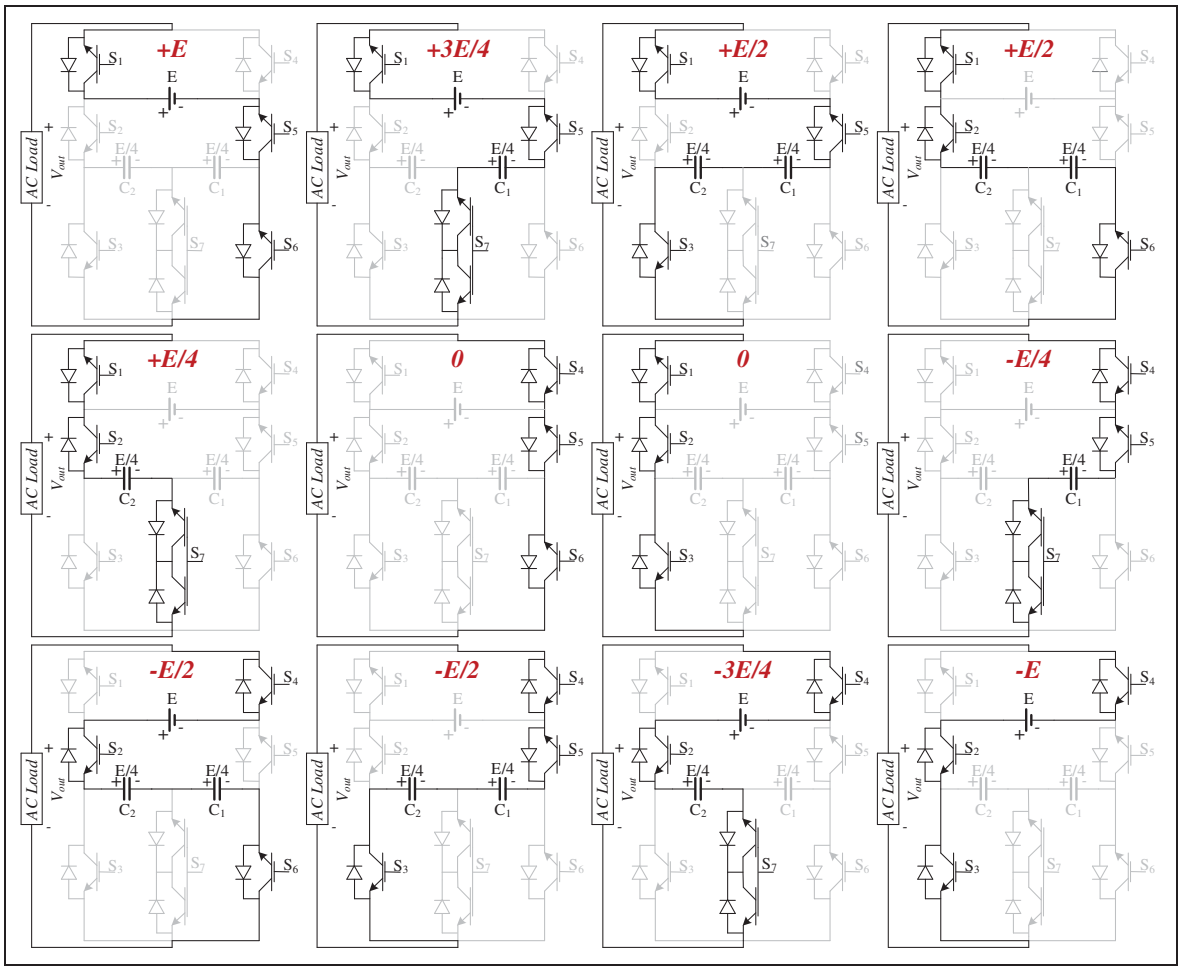

Figure 6.2 Operating sequences of PEC9 inverter showing devices, shunted capacitors and DC link connection during the 12 operating sequences forming according to the switching states possibility

6.3 Proposed PWM Active Voltage Balancing

6.3.1 E-Cell Capacitors Voltages Equations

In order to design the voltage balancing control, the capacitors charging and discharging formulation is firstly expressed during one cycle for nine-level voltage operation. The capacitors voltages (V_1 & V_2) equations are formulized based on the output voltage (V_{out}), load current I_{out} and capacitors currents (I_1, I_2). Since load current flows into and out of the capacitors, during voltage levels ($\pm E/4$, $\pm E/2$, $\pm 3E/4$), I_{out} is then equal to I_1 and I_2 during these time intervals. Using Table 6, the capacitors charging and discharging states are shown

for a predetermined nine-level waveform as it is depicted in Figure 6.3. As C_1 and C_2 are forming the levels ($\pm E/2$, $+3E/2$, $-E/4$) and ($+E/4$, $\pm E/2$, $-3E/4$); then I_1 and I_2 can be obtained as follow:

$$\begin{cases} I_1(t)=I_{out}(t) \ : \begin{cases} (\alpha_2<t<\alpha_4)\&(\pi-\alpha_4<t<\pi-\alpha_2) \\ (\pi+\alpha_1<t<\pi+\alpha_3)\&(2\pi-\alpha_3<t<2\pi-\alpha_1) \end{cases} \\ I_2(t)=I_{out}(t) \ : \begin{cases} (\alpha_1<t<\alpha_3)\&(\pi-\alpha_3<t<\pi-\alpha_1) \\ (\pi+\alpha_2<t<\pi+\alpha_4)\&(2\pi-\alpha_4<t<2\pi-\alpha_2) \end{cases} \end{cases} \tag{6.1}$$

Considering I_{out} is the division of the output voltage (V_{out}) and load impedance (Z) as V_{out}/Z. Where Z is considered generally as $Z=R+jL\omega$ which mean any value can be assumed for the resistor and inductance. The angular frequency (ω) is also $\omega=2\pi f$ and f is fundamental frequency which is assumed as 50 Hz or 60 Hz. The capacitors currents can also be computed as a function of I_{out} therefore Eq. (6.1) will become:

$$\begin{cases} C_1\left(\frac{dV_1(t)}{dt}\right)= \frac{V_{out}(t)}{Z} \ : \begin{cases} (\alpha_2<t<\alpha_4)\&(\pi-\alpha_4<t<\pi-\alpha_2) \\ (\pi+\alpha_1<t<\pi+\alpha_3)\&(2\pi-\alpha_3<t<2\pi-\alpha_1) \end{cases} \\ C_2\left(\frac{dV_2(t)}{dt}\right)= \frac{V_{out}(t)}{Z} \ : \begin{cases} (\alpha_1<t<\alpha_3)\&(\pi-\alpha_3<t<\pi-\alpha_1) \\ (\pi+\alpha_2<t<\pi+\alpha_4)\&(2\pi-\alpha_4<t<2\pi-\alpha_2) \end{cases} \end{cases} \tag{6.2}$$

Presuming the nine-level voltage of Figure 6.3 as a quarter symmetry waveform, V_{out} is mathematically defined based on its harmonics amplitudes (H_n) using Fourier analysis as:

$$V_{out}(t) = \sum_{n=1}^{\infty} H_n \ \sin(n\omega t) \tag{6.3}$$

By substituting Eq. (6.3) into Eq. (6.2), the capacitors voltages are calculated by integrating Eq. (6.2) in time domain as Eq. (6.4).

$$\begin{cases} V_1 = \frac{1}{ZC_1} \int_{t_1}^{t_2} \sum_{n=1}^{\infty} \left(H_n \ \sin(n\omega t) \right) dt \\ V_2 = \frac{1}{ZC_2} \int_{t_1}^{t_2} \sum_{n=1}^{\infty} \left(H_n \ \sin(n\omega t) \right) dt \end{cases} \tag{6.4}$$

According to Eq. (6.4), both capacitors follow the same formulation and they can results in

same voltage amplitude if the time duration of both integral functions are equal. Integration of the capacitors voltages V_1 and V_2 result into a constant value imposed by ripple, which should be controlled through proper switching states selections to keep both voltages convergent to the same value. To this end, the voltage ripple of both capacitors must have same value in first and second half cycles *([0, π] & [π, 2π]*), so as the capacitors can be appropriately adjusted to the desired amplitude to $V_{dc}/4$. The capacitors voltages ripple are obtained for two half cycles:

$$
\begin{aligned}
&V_1\Big|_0^{\pi} = V_1\Big|_{\pi}^{2\pi} \\
&\frac{2}{ZC_1}\Big(\underbrace{\sum_{n=1}^{\infty}\frac{-H_n}{n\omega}\cos(n\omega t)\Big|_{\alpha_2}^{\alpha_3}}_{C_1, C_2 \text{ in } \frac{\pm E}{2}} + \underbrace{\sum_{n=1}^{\infty}\frac{-H_n}{n\omega}\cos(n\omega t)\Big|_{\alpha_3}^{\alpha_4}}_{C_1 \text{ in } \frac{+3E}{4}}\Big) = \\
&\frac{2}{ZC_1}\Big(\underbrace{\sum_{n=1}^{\infty}\frac{-H_n}{n\omega}\cos(n\omega t)\Big|_{\pi+\alpha_1}^{\pi+\alpha_2}}_{C_1 \text{ in } \frac{-E}{4}} + \underbrace{\sum_{n=1}^{\infty}\frac{-H_n}{n\omega}\cos(n\omega t)\Big|_{\pi+\alpha_2}^{\pi+\alpha_3}}_{C_1, C_2 \text{ in } \frac{\pm E}{2}}\Big)
\end{aligned}
\tag{6.5}
$$

$$
\begin{aligned}
&V_2\Big|_0^{\pi} = V_2\Big|_{\pi}^{2\pi} \\
&\frac{2}{ZC_1}\Big(\underbrace{\sum_{n=1}^{\infty}\frac{-H_n}{n\omega}\cos(n\omega t)\Big|_{\alpha_1}^{\alpha_2}}_{C_2 \text{ in } \frac{+E}{4}} + \underbrace{\sum_{n=1}^{\infty}\frac{-H_n}{n\omega}\cos(n\omega t)\Big|_{\alpha_2}^{\alpha_3}}_{C_1, C_2 \text{ in } \frac{\pm E}{2}}\Big) = \\
&\frac{2}{ZC_1}\Big(\underbrace{\sum_{n=1}^{\infty}\frac{-H_n}{n\omega}\cos(n\omega t)\Big|_{\pi+\alpha_2}^{\pi+\alpha_3}}_{C_1, C_2 \text{ in } \frac{\pm E}{2}} + \underbrace{\sum_{n=1}^{\infty}\frac{-H_n}{n\omega}\cos(n\omega t)\Big|_{\pi+\alpha_3}^{\pi+\alpha_4}}_{C_2 \text{ in } \frac{-3E}{4}}\Big)
\end{aligned}
\tag{6.6}
$$

Since the time duration for integral functions of Eq. (6.5) and Eq. (6.6) is changed by changing the pulses width as a result of changing the modulation index of switching technique, the redundant switching state must be deal into a PWM technique to adjust the charging and discharging time and regulate the capacitors voltages to the desired amplitude level. As it shown in Eq. (6.5) and Eq. (6.6), controlling both capacitors voltages to the levels *±E/2* leads to equal ripple values in both of half cycle that consequently guarantee voltage balancing. Indeed, both DC capacitors have same state for *±E/2*; however, only one of them

is charged/discharged for ±*E/4* and ±*3E/4*. Since C_1 is charging in +*3E/4* and discharging in -*E/4*; so, by regulating capacitors voltages in levels ±*E/2* using redundant switching states, charging and discharging of C_1 would be equal in the +*3E/4* and -*E/4*; respectively. Same procedure occurs for C_2 that is charging in -*3E/4* and discharging in +*E/4*. Therefore, the redundant switching states for middle levels (±*E/2*) adjust amount of charging and discharging time and with respect to Eq. (6.5) and Eq. (6.6) to keep capacitors voltages balanced to the desired DC levels during a full cycle. Therefore, it is proven that DC-link capacitors of PEC inverter are perfectly balanced if a PWM control is accordingly designed to integrate the redundant switching states particularly ones regarding to the middle levels (±*E/2*) with modulation technique.

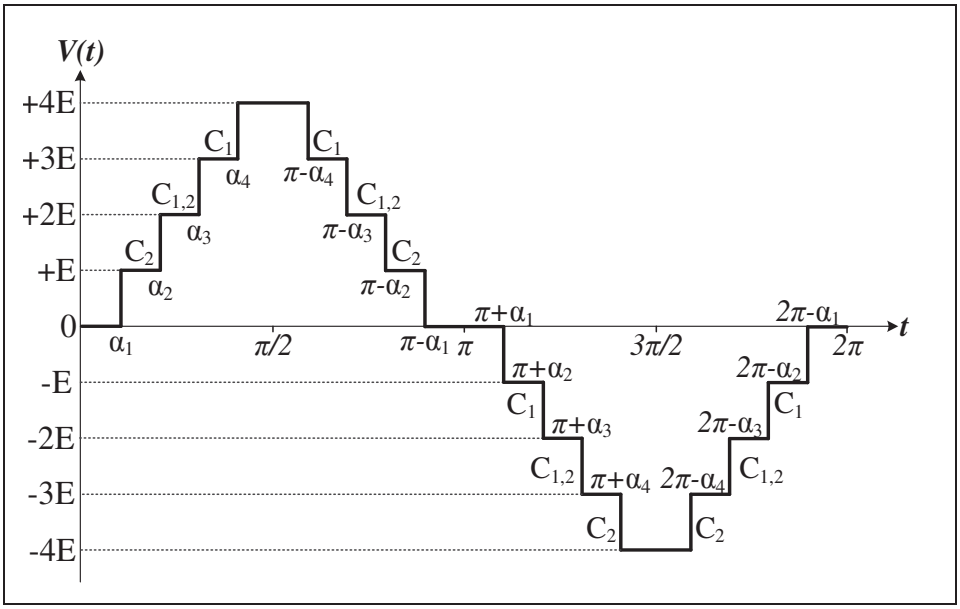

Figure 6.3 Split capacitors charging/discharging states in nine-level voltage

6.3.2 Proposed Active Capacitor Voltage Balancing PWM Technique Using Single Voltage Sensor for Auxiliary DC-Link

It was mathematically discussed and proved in section 6.3 A that the redundant switching states regarding to the middle voltage levels (±*E/2*) are adequate to adjust the charging and discharging time of capacitors and regulate their voltages to one quarter of input DC voltage

amplitude. Using the performed capacitors voltages analysis, the corresponding flowchart for active capacitor voltage balancing of PEC9 inverter has been drawn and shown in Figure 6.4.

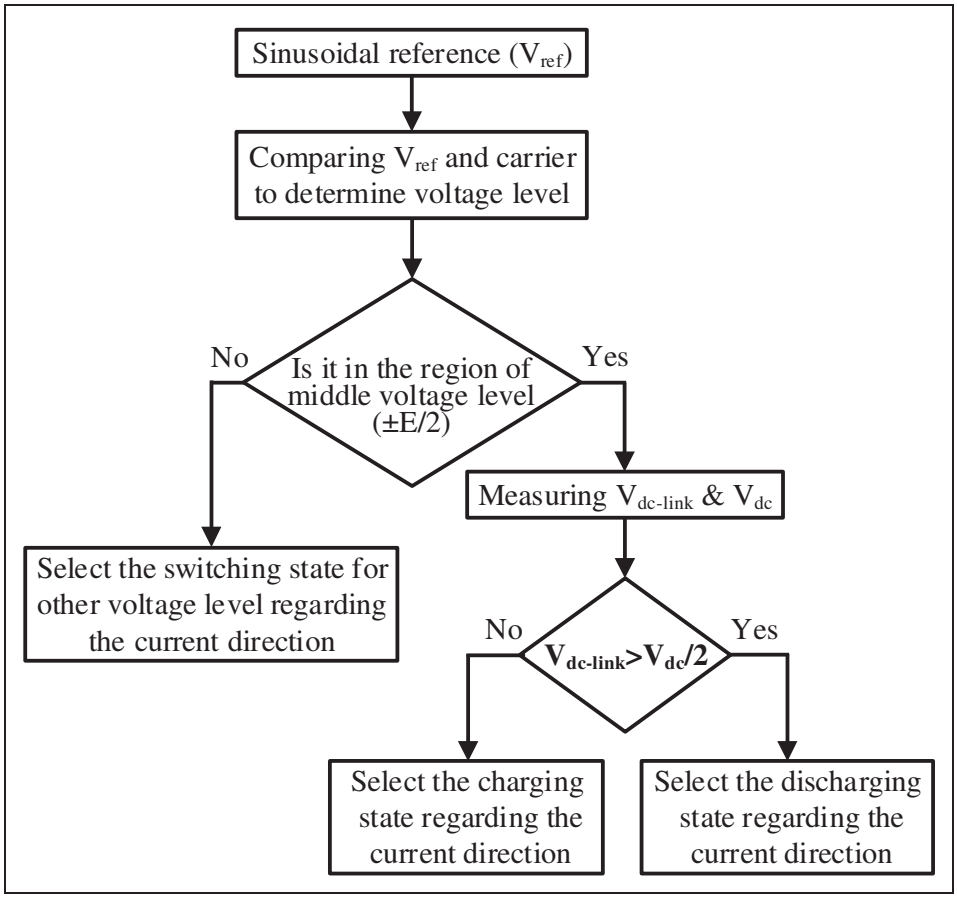

Figure 6.4 The designed flowchart for the active capacitor voltage balancing of PEC9 inverter

Figure 6.5 also shows the block diagram of proposed active capacitor voltage balancing algorithm approach integrated into the nine-level PWM technique to regulate the capacitors voltages to one quarter of DC input amplitude by controlling auxiliary DC-link voltage. According to the designed active voltage balancing PWM technique, the DC-link voltage that is the summation of both capacitors is measured by a single voltage sensor, and then compared to half of DC input reference voltage in order to find the error signal (ΔV). Therefore, it is not needed to control each DC capacitor separately. Using the redundant switching state would balance the DC-link voltage to E/2 and DC capacitors voltages are

inherently regulated to E/4. According to the proposed method, if $\Delta V>0$ the discharging states (*3, 10, 16 & 21 for* $I_{out}>0$) and if $\Delta V<0$ the charging states (*4, 9, 15 & 22 for* $I_{out}<0$) are chosen for the voltage levels $\pm E/2$. By fluctuating between charging and discharging in these two levels, the input DC voltage is equally shared between capacitors during one full cycle that each capacitor voltage is balanced to *E/4*. Since zero voltage level has redundant states, they are used to reduce the switching frequency. In this case, if the reference signal is positive the state 6 is chosen and if it is negative the state 7 is used to generate zero voltage level. It must be mentioned that for zero and $\pm E$ voltage levels the current direction is not considered because no capacitor is involved.

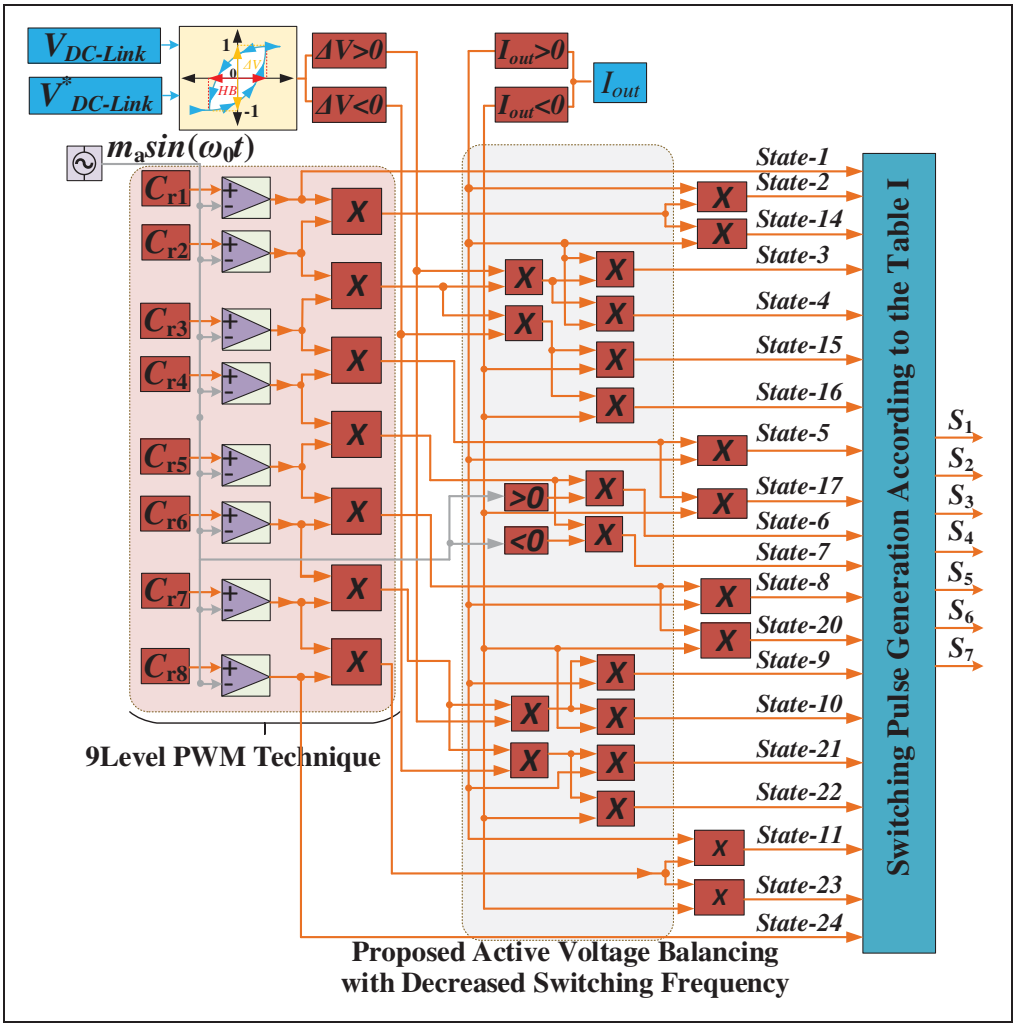

Figure 6.5 The block diagram of the proposed single sensor active voltage balancing method

6.3.3 PWM Technique Using Half-Parabola Carrier

New carrier waveform for PWM technique based on parabolic function has been designed to have better performance in controlling voltage profile harmonic distortion at lower switching frequency. Figure 6.6 demonstrates the process of generating parabolic carrier signals that is defined using sinusoidal and pulse functions. Considering the frequency of pulse function f_1 two times greater than the sinusoidal function f_2 ($f_1=2f_2$) the half-parabola waveform is attained. However, based on the frequency ratio between f_1 and f_2, various types of parabolic functions can be generated. The factors K_1, K_2 and K_3 are also selected as *0.5*, *1* and *0.25*, respectively. Figure 6.7 displays the nine hybrid level shift-PWM which consists of 8 carrier signals defined as half-parabolic function with switching frequency identified as C_{r1}, C_{r2}, C_{r3}, C_{r4}, C_{r5}, C_{r6}, C_{r7} & C_{r8} and sinusoidal reference signal with fundamental frequency as V_{ref}. Each carrier is used for the firing signals of one voltage level so as by comparing V_{ref} and C_{r1}, C_{r2}, C_{r3}, C_{r4}, C_{r5}, C_{r6}, C_{r7} and C_{r8} the related pulses for *+E*, *+3E/4*, *+E/2*, *+E/4*, *-E/4* ,*-E/2*, *-3E/4* and *-E* are generated, respectively. Also, the zero level is generated when V_{ref} is between C_{r4} and C_{r5}.

6.4 PEC versus Other Recently Presented Multilevel Inverters; Components Comparison

Since PEC basic configuration has nine voltage levels, it is compared to the innovative single-DC source nine-level topologies which have been recently introduced. Table 6.2 lists the components comparison among nine-level topologies presented in (Liu et al., 2017; Wang et al., 2017; Sandeep et Yaragatti, 2017; Sandeep et Yaragatti, 2017; Vahedi et al., 2013; Kshirsagar et al., 2017) and PEC9. Based on Table 6.2, PEC9 has minimum number of active components (7 switches) and an auxiliary DC-link compared to other recent presented nine-level topologies. In comparison to nine-level PUC type, the PEC9 not only requires one less power switches and gate driver circuits, but also it reduces auxiliary DC-link and voltage sensors that has the advantages of active voltage balancing through redundant switching states without adding external complex current controllers.

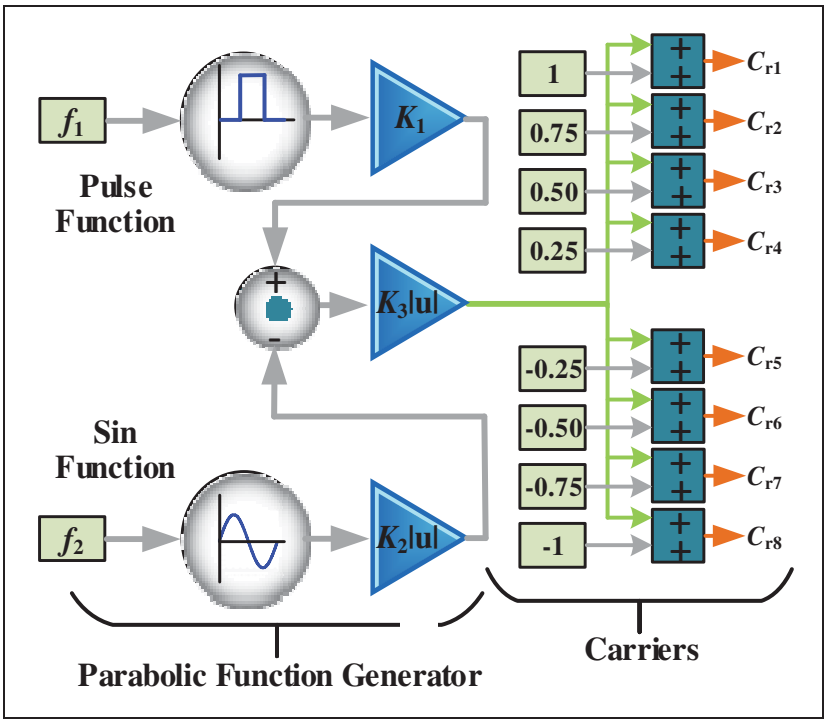

Figure 6.6 Parabolic waveforms generator using sinusoidal and pulse functions

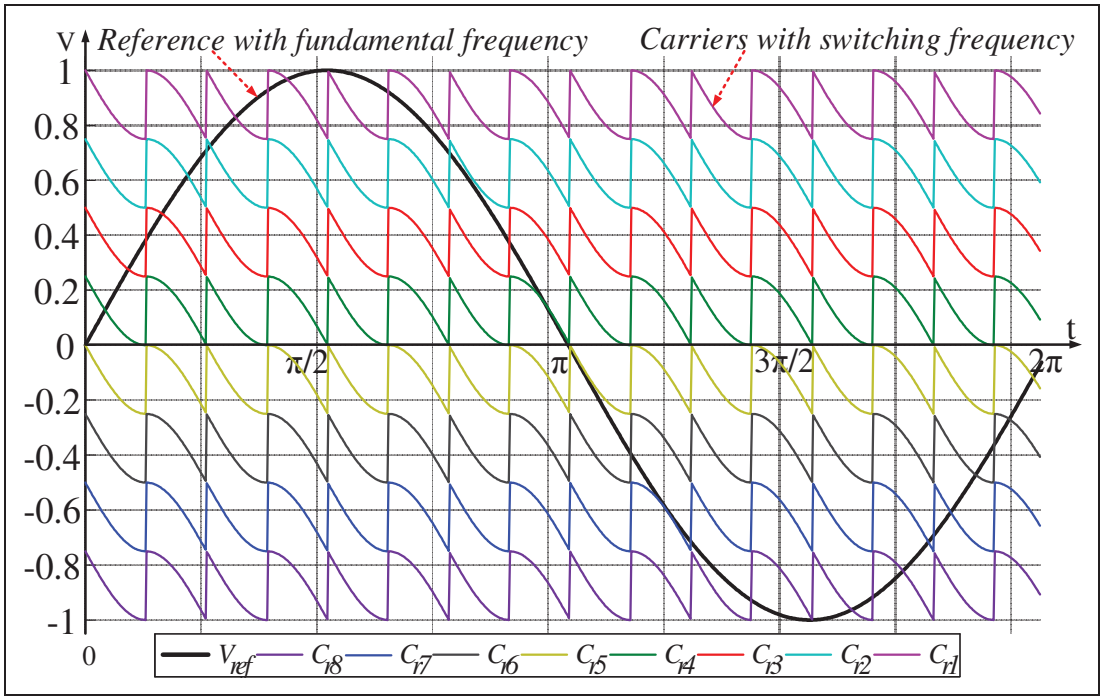

Figure 6.7 9level hybrid PWM with half-parabola vertically shifted carriers

Table 6.2 Component Comparison among 9Level Converters and PEC9

Inverter Type	DC Sources	Auxiliary Capacitor	Power Switch	Diode Clamped	Control Complexity
DSCC-HBC	1	2	9	2	Low
Hybrid HB	1	4	12	0	Low
DHANPC	1	3	12	0	High
RDCANPC	1	3	10	0	High
CSC	1	1	10	0	Very high
CFC	2	2	8	0	High
PUC9	1	3	10	0	Very High
PEC9	1	1	7	0	Low

Figure 6.8 also presents a general comparison among PEC and other converters including CHB, NPC, FC and PUC as well as some novel topologies in terms of total number of passive and active components in comparable operation type of multilevel structure. The comparative study for number of components is done based on the number of levels (m) generated at the converter output. Figures 8-a and 8-b display the number of components and DC-link in PEC and other studied converters, respectively. As a result of horizontal extension capacitors through four-quadrant switch, the PEC inverter requires minimum auxiliary DC-link, semiconductor devices, and gate deriver circuits when it is configured to generate more than nine-level as shown in Figure 6.8.

As a comparison among CHB, NPC, FC and PEC, the latter makes use of fewer components, which decrease manufacturing cost. As well, while PEC regulates the floating capacitors voltages by redundant switching states, the NPC and FC need to use complex controllers when operating with extended number of levels. As for the CHB, one can notice that not only more active devices are required; but also isolated DC-sources are employed which confines it to renewable energy applications. On the other hand, floating capacitors expansion in the form of E-Cell notably decreases the number of auxiliary DC-link. This will also lead to simultaneous capacitors charging or discharging with redundant states that effectively

guarantee active voltage regulations with no need to complex additional external voltage controllers. As the number of levels increase, there will be more switching states as the result of E-Cell connection, which enhance the reliability of the PEC structure.

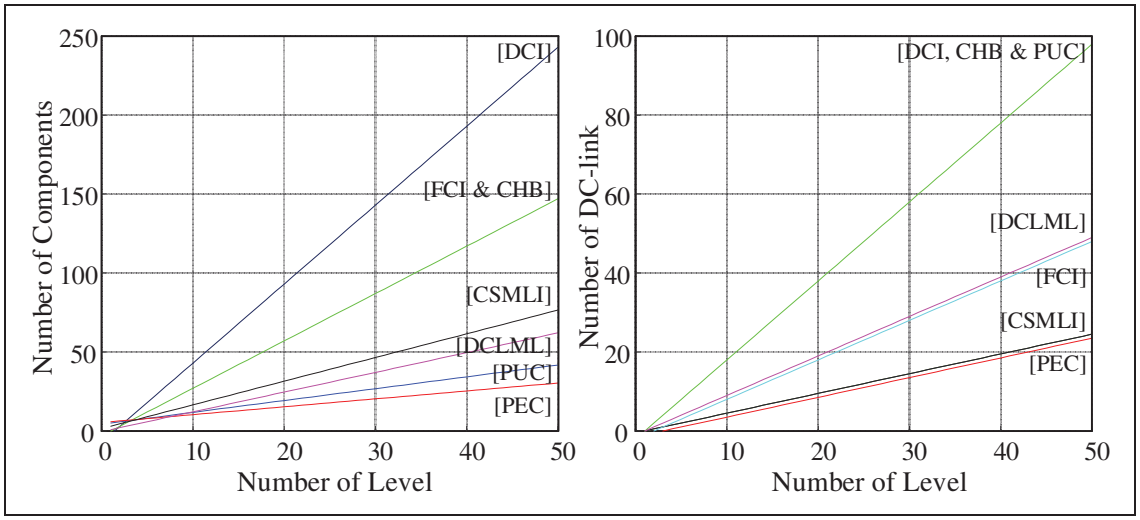

Figure 6.8 Component comparisons among multilevel topologies and PEC, (a) number of active devices and gate driver circuits (b) number of DC-link

6.5 Experimental Validation and Analysis of PEC9

In this section, the proposed PEC inverter topology and designed active voltage balancing PWM technique has been analyzed through experimental analysis. A prototype of PEC9 inverter has been built and practically tested as an Uninterruptible Power Supply (UPS) application to evaluate its performance under different operating conditions including with and without voltage balancing method, switch fault condition, changing modulation index, increased or decreased of DC input voltage amplitude, and output load variations. The considered output load is constituted of an R-L circuit. The dSpace 1104 has been used as a fast prototyping real time controller with sampling time T_s=*20*µs to implement the proposed active voltage balancing algorithm integrated into PWM technique designed by half-parabola carrier waveforms. Load current, main and auxiliary DC-link voltages are sensed by OPAL-RT high voltage/current measurement and sent to ADC of dSpace 1104. The experimental system parameters of PEC9 are listed in Table 6.3.

Table 6.3 PEC9 Parameters Used for Experimental Tests

DC bus voltage (V_{dc})	200 V
Fundamental and switching frequency	60 Hz & 1500 Hz
Auxiliary capacitor capacitance (C_1 & C_2)	2500 µF
Linear load; resistor and inductor (R & L)	(40, 80) Ω & 50 mH

6.5.1 Test1: Multilevel Voltage Operation

In order to ascertain the excellent performance of the proposed active voltage balancing PWM method in regulating the capacitors voltages to the desired level, PEC9 has been operated with and without the designed technique under same amplitude modulation index (*MI=0.85*). Figure 6.9 illustrates the experimental results of output voltage and current and C_1, C_2 voltages for nine-level PEC inverter. As it was discussed in section 6.3-A, the proposed active voltage balancing method has been accordingly designed to control the DC-link voltage to $V_{dc}/2$ by adjusting the charging and discharging time so as the capacitors voltages are inherently balanced to $V_{dc}/4$. As can be seen from Figure 6.9, the capacitors voltages are less than desired level when the active voltage balancing is not applied; however, they are accurately tracks the determined amplitude and a perfect nine-voltage level waveform is then shaped when PEC9 is run by the designed technique. Afterwards, the start-up mode of PEC9 has been demonstrated in Figure 6.10 to prove that the proposed active voltage balancing PWM technique is able to regulate the capacitors voltages to $V_{dc}/4$ as auxiliary DC-link is charged up to $V_{dc}/2$. The acquired results illustrates no pre-charged capacitors is needed for the PEC topology with the proposed control technique. Figure 6.11 also shows the zoom of Figure 6.10 which confirms that the capacitors voltages ripple is less than 5%. Also, output voltage and current harmonic contents are depicted when PEC is controlled by the proposed half-parabola PWM technique with modulation index equal to *0.85* and an output load $R=80$ Ω and $L=50mH$. The detail amplitude of every voltage and current harmonic order of nine-level PEC inverter has been shown in Table 6.4.

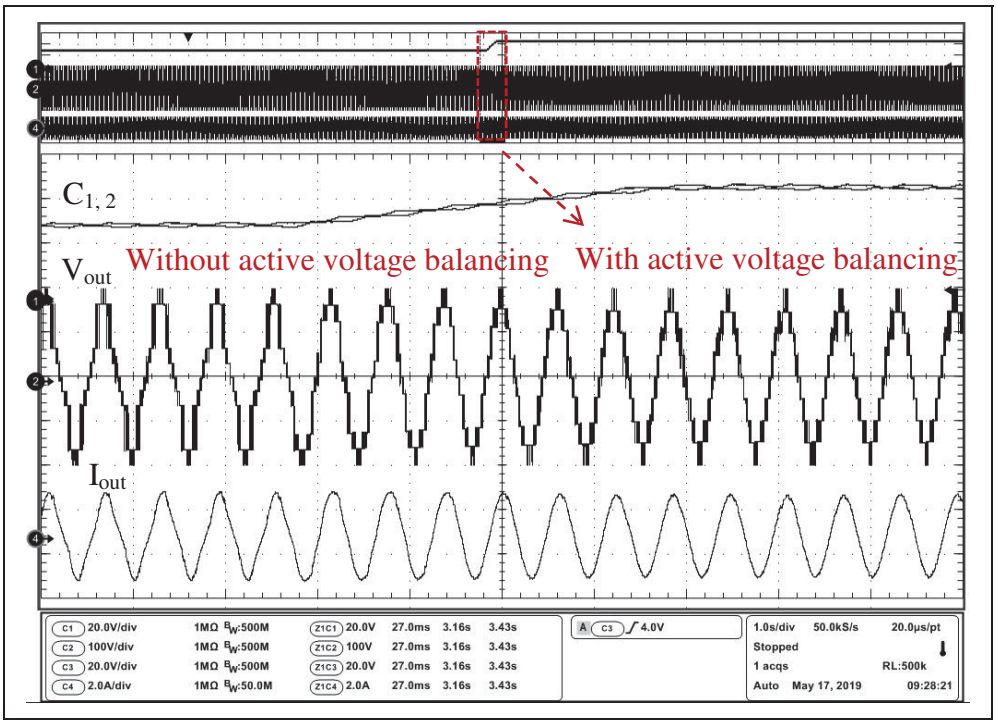

Figure 6.9 Experimental results of PEC9 operations with and without designed active voltage balancing PWM technique

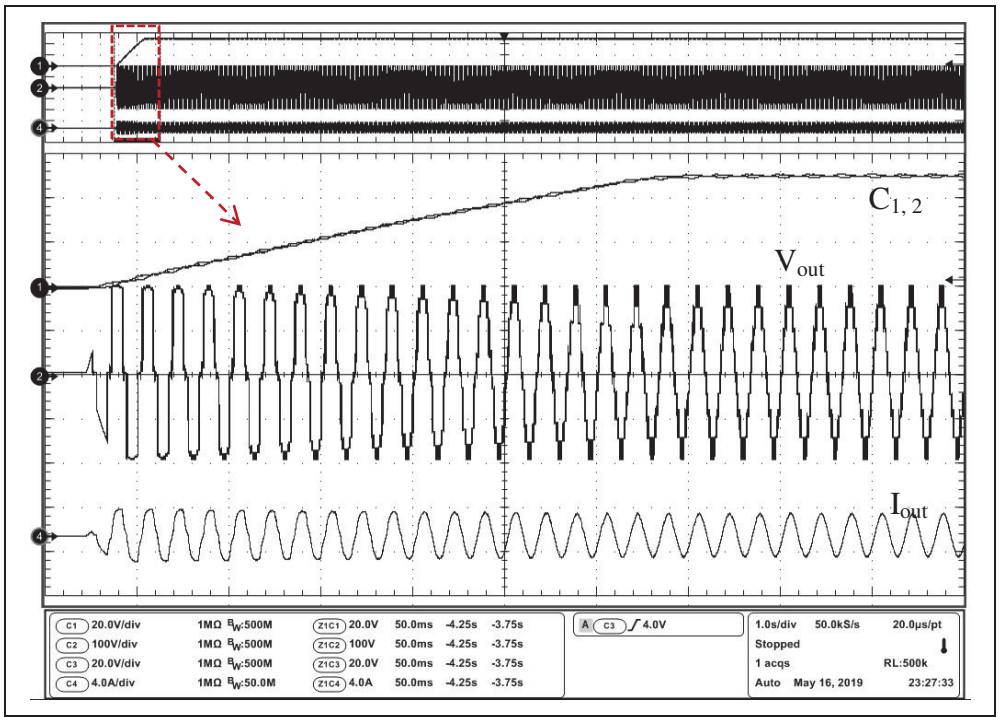

Figure 6.10 Experimental results of start-up mode of PEC9 operation controlled by the proposed active voltage balancing PWM technique

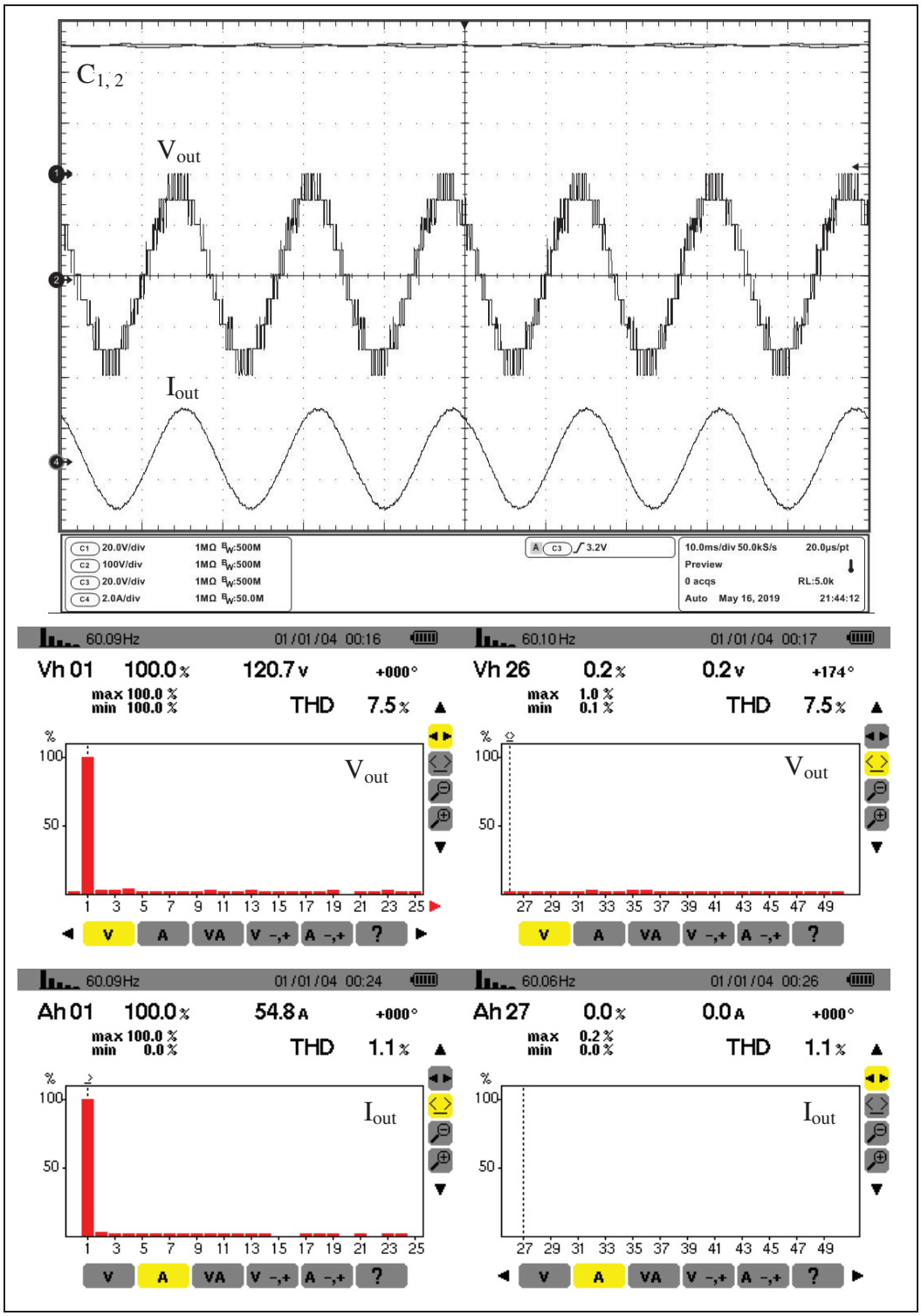

Figure 6.11 Steady state nine-level voltage waveform along with harmonic spectrum of nine-level output voltage and load current

Table 6.4 The Amplitude of Harmonic Spectrum of Nine-Level Output Voltage and Load Current of Figure 6.11

Voltage Harmonic (%)						**Current Harmonic (%)**					
H1	100	H18	0.1	H35	2.5	H1	100	H18	0.1	H35	0.3
H2	0.2	H19	1.8	H36	1.1	H2	0.1	H19	0.1	H36	0.2
H3	0.5	H20	0.5	H37	0.5	H3	1.2	H20	0.1	H37	0.1
H4	0.7	H21	0.5	H38	0.5	H4	0.1	H21	0	H38	0.1
H5	0.4	H22	0.5	H39	1.2	H5	0.3	H22	0	H39	0.2
H6	0.5	H23	0.7	H40	0.1	H6	0.4	H23	0.1	H40	0.1
H7	1.3	H24	0.4	H41	0.7	H7	0.4	H24	0.1	H41	0.3
H8	1	H25	0.9	H42	1.2	H8	0.3	H25	0.1	H42	0.1
H9	1.1	H26	1.9	H43	0.7	H9	0.5	H26	0.2	H43	0.2
H10	0.9	H27	1.3	H44	0.6	H10	0.4	H27	0.1	H44	0.1
H11	1.1	H28	0.9	H45	1.6	H11	0.3	H28	0.1	H45	0.2
H12	0.5	H29	1.5	H46	0.8	H12	0.2	H29	0.1	H46	0.1
H13	0.9	H30	0.9	H47	1.7	H13	0.1	H30	0.2	H47	0.1
H14	0.4	H31	1.2	H48	4.4	H14	0.1	H31	0.3	H48	0.3
H15	0.3	H32	0.6	H49	0.3	H15	0.2	H32	0.1	H49	0.1
H16	0.2	H33	0.9	H50	0.3	H16	0.2	H33	0.2	H50	0.2
H17	1.2	H34	1.2			H17	0.2	H34	0.1		

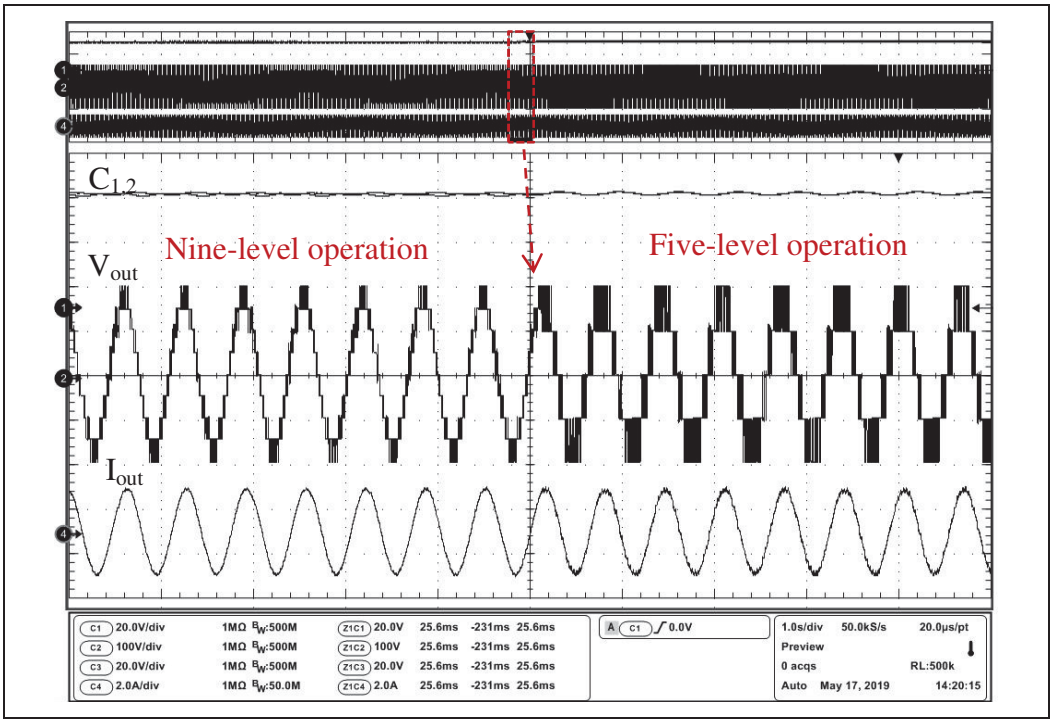

Figure 6.12 Experimental results of dynamic changes from nine- to five-level voltages of PEC9 inverter under faulty four-quadrant switch condition

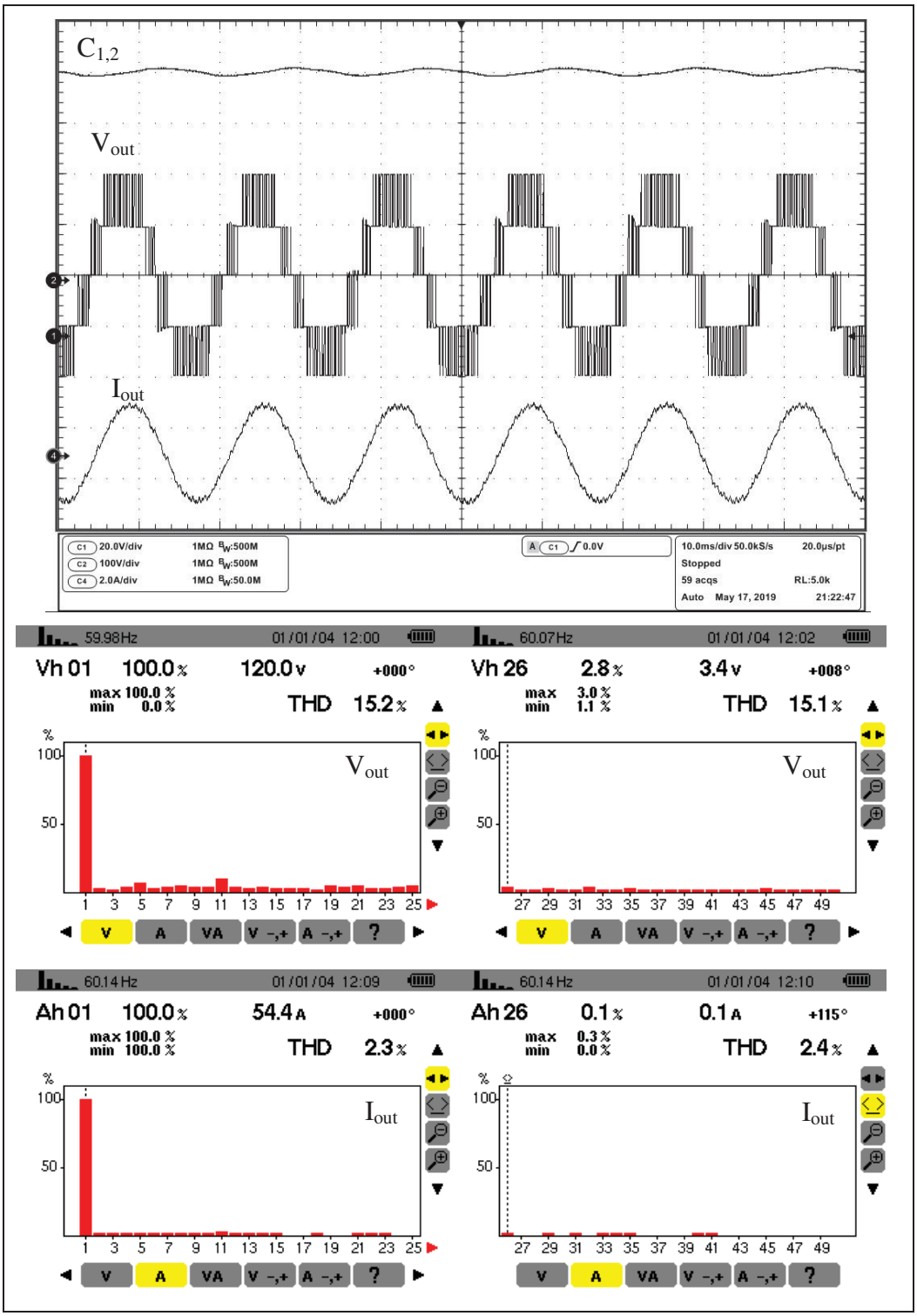

Figure 6.13 Steady state five-level voltage operation of PEC inverter along with output voltage and load current harmonic spectrum

As it was mentioned, PEC9 has the ability of generating multilevel voltage waveforms by applying appropriate switching patterns. To further illustrate highly capability of multilevel voltage operation PEC inverter, it has been tested under switch fault condition by which the four-quadrant switch is set to OFF state so nine-level PEC operates as five-level inverter. Figure 6.12 demonstrates the experimental results of dynamic PEC9 operation including output voltage and current as well as DC capacitors voltages waveforms when the inverter immediately changes from nine-to five-level operations. By turning OFF the four-quadrant switch, both series connected capacitors C_1 and C_2 are considered as one and consequently five-level voltage is achieved when DC-link voltage is kept balanced to $V_{dc}/2$. There is no transient between five- and nine-level output voltage operations of PEC inverter and the capacitors voltages are balanced to $V_{dc}/4$ in both cases operations. In addition, experimental results of five-level operation of PEC inverter shows variables of Figure 6.12 as well as the voltage and current harmonics spectrum are depicted in Figure 6.13. The details amplitude of each voltage and current harmonic order of five-level operation of PEC inverter are listed in Table 6.5. Furthermore, it needs to be mention that seven and eleven voltage levels are also achievable through PEC9 topology; but, it requires an external current controller to adjust the auxiliary DC-link voltage to one third and two fifth of input DC voltage, respectively. As can be seen from harmonic spectrum analysis of five-and nine-level voltages, the THD has been obtained as *15.2%* and *7.4%*; respectively, when switching frequency is *1500 Hz*. It must be noticed that S_1 and S_4 are switched at the fundamental frequency; whereas the remaining S_2, S_3, S_5, S_6, S_7, are fired at the switching frequency.

6.5.2 Test2: Modulation Index and DC Input Voltage Variations

In order to investigate the reliability of the proposed active voltage balancing method, the PEC9 inverter has been tested for pulse width and input voltage changes. Figure 6.14-a shows PEC9 experimental results of output voltage, load currents and floating capacitors voltages while modulation index changes from *0.75*-to-*0.95* and the DC input voltage is fixed to *200 V*. As it is clear from Figure 6.14-a, seven voltage levels are obtained when modulation index (MI) is set to 0.75 since the reference sinusoidal signal is lower than last carrier signals (C_{r1}

and C_{r8}) to generate the ninth level that is obtained for MI higher than 0.95. Moreover, the input current is increased by changing modulation index from 0.75-to-0.95 as the output voltage changes from seven-level to nine-level. Despite modulation index changes, one can notice capacitors voltages perfectly track their references and remain balanced and equal to $V_{dc}/4$ without being affected by transient while the capacitors voltages ripple is kept below 5%. Figure 6.14-b displays the same results of PEC9 when MI=0.85 kept constant, and DC source voltage increased from *200V* to *250V*. As depicted in Figure 6.14-b, once again the capacitors voltages inherently track their reference of $V_{dc}/4$ with voltage ripple below 5% which is acquired by controlling the DC-link voltage to $V_{dc}/2$ using redundant switching states.

Table 6.5 The Amplitude of Harmonic Spectrum of Five-Level Output Voltage and Load Current of Figure 6.13

Voltage Harmonic (%)						**Current Harmonic (%)**					
H1	100	H18	0.2	H35	3.1	H1	100	H18	0.2	H35	0
H2	0.2	H19	2.3	H36	1.3	H2	0.1	H19	0.3	H36	0.3
H3	0.8	H20	0.6	H37	0.6	H3	0.9	H20	0.4	H37	0.2
H4	0.5	H21	0.5	H38	0.4	H4	0.2	H21	0.1	H38	0.4
H5	0.3	H22	0.6	H39	1.5	H5	0.5	H22	0.1	H39	0.1
H6	0.2	H23	0.9	H40	0.1	H6	0.6	H23	0.2	H40	0.2
H7	1.5	H24	0.5	H41	0.1	H7	0.6	H24	0.3	H41	0.1
H8	1.2	H25	1.2	H42	1.5	H8	0.6	H25	0.1	H42	0.2
H9	0.5	H26	2.1	H43	0.5	H9	0.4	H26	0.5	H43	0.3
H10	0.3	H27	1.1	H44	0.5	H10	0.2	H27	0.2	H44	0.2
H11	1.3	H28	1.3	H45	1.1	H11	0.1	H28	0.2	H45	0.1
H12	0.8	H29	1.2	H46	1	H12	0.1	H29	0.4	H46	0.2
H13	0.5	H30	0.5	H47	2	H13	0.5	H30	0.1	H47	0.2
H14	0.2	H31	1.6	H48	3.8	H14	0.5	H31	0.1	H48	0.1
H15	0.1	H32	0.9	H49	0.9	H15	0.3	H32	0	H49	0.1
H16	0.1	H33	0.6	H50	0.5	H16	0.3	H33	0.1	H50	0.1
H17	1.3	H34	1.8			H17	0.1	H34	0.2		

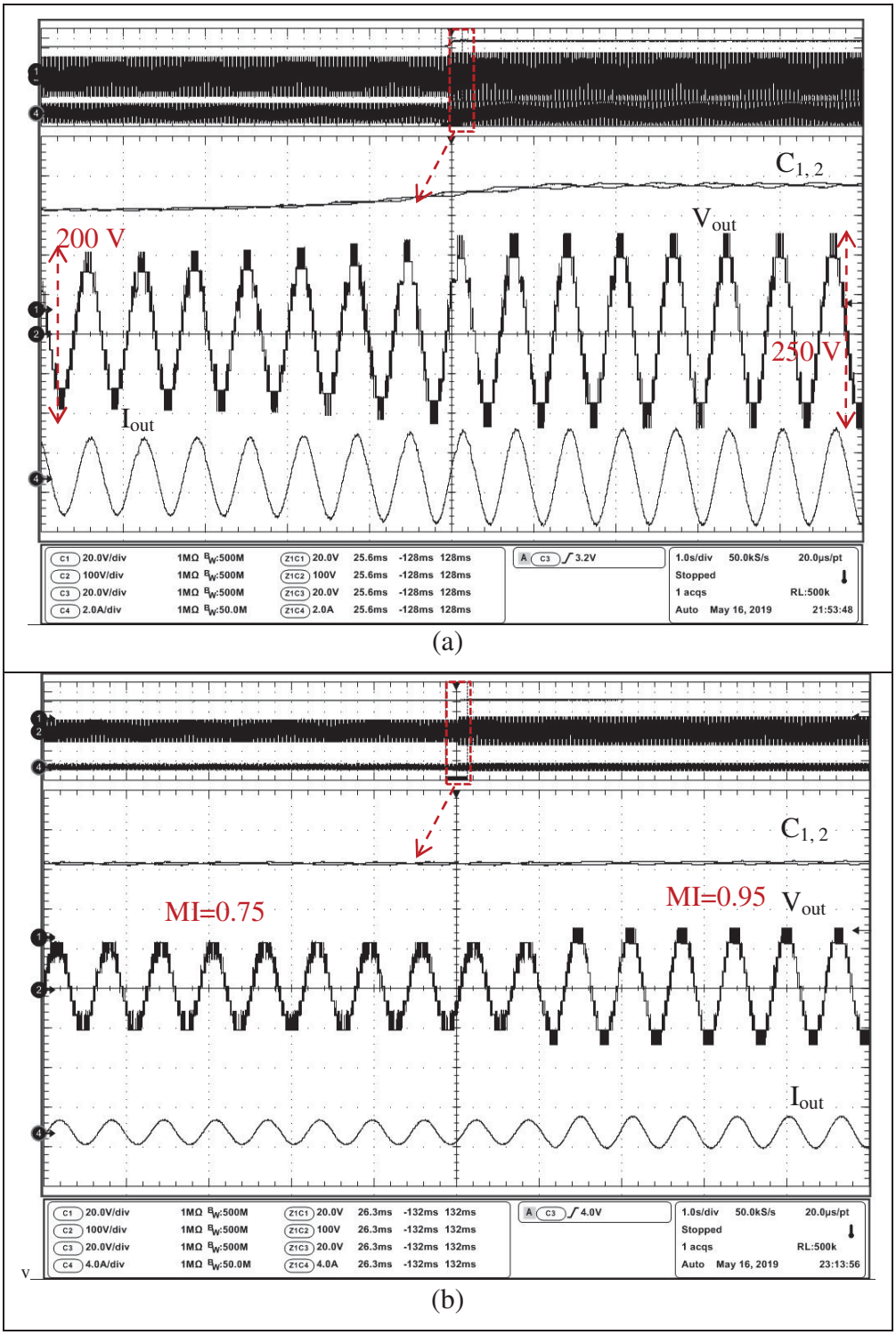

Figure 6.14 Experimental results of nine-level voltage (Vout), load current (Iout) and split DC capacitors voltages ($C_{1,2}$) of PEC9,(a) modulation index changes, (b) DC input variations

6.5.3 Test3: Output Load Changes

The floating capacitors regulated voltages has been tested for output loads power and frequency variations to scrutinize proposed active voltage balancing PWM based half-parabola type of carrier signal. Figure 6.15 shows experimental results of output voltage, load current and floating capacitors voltages when the load resistance changes from *40* Ω to *80* Ω and then back to *40* Ω, while the inductive component remains constant equal to *50 mH*. According to Figure 6.15, output load variations do not affect the split capacitors voltages regulations neither the voltage ripple as they are balanced and equal to the desired reference amplitude $V_{dc}/2$ with ripple less than 5%. Moreover, no transition or changing in DC capacitors voltages ripple during the load variation can be observed.

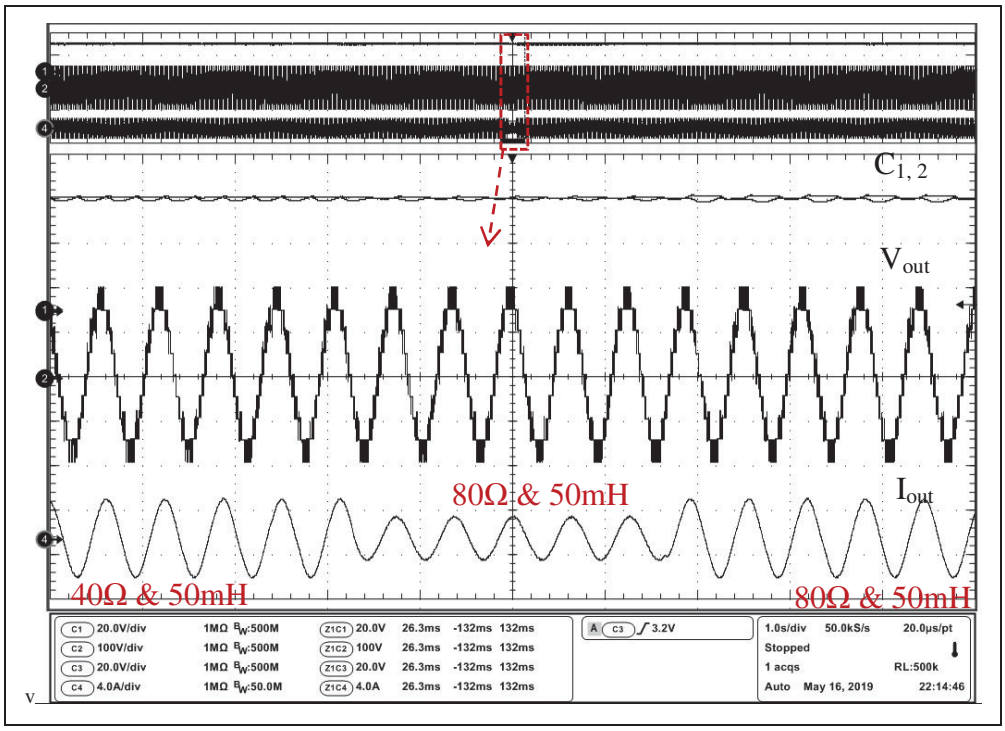

Figure 6.15 Experimental results of nine-level voltage (Vout), load current (Iout) and split DC capacitors voltages (C1,2) of PEC9 for load changes from 40Ω to-80Ω and back to 40Ω

6.6 Conclusions

In this work, a novel nine-level single-DC source Packed E-Cell (PEC9) topology has been introduced as a promising candidate for single-phase inverter suitable for symmetrical and asymmetrical series of connection. The presented structure is indeed an optimized compact design topology which permits the reduction of auxiliary DC-link and components count by using E-Cell type of connection. Moreover, by horizontal extension of auxiliary DC-link, in the form of E-Cells, simultaneous charging or discharging with redundant state are achieved that guarantees floating capacitors voltage balancing under all operating conditions. An active voltage-balancing algorithm was integrated to the half parabola carrier PWM based technique to efficiently regulate floating capacitors voltages. It was also demonstrated that different output stepped voltage waveforms are achievable without changing in converter circuit design. The presented experimental results of PEC9 validated its reliable performance in keeping capacitors voltages balanced under different load and source conditions that can emerge as a competitive topology for various industrial standalone and grid-tied applications.

CONCLUSION

Nowadays, multilevel inverters are the inseparable part of the power industry and they are widely employed in various applications including HVDC, UPS, electrical vehicles, battery chargers, ac and dc electrical motor drives, active power filters and so on. This widespread utilization has led to tremendous research on developments of multilevel inverters topologies or control technique in order to improve their operation performance in the targeted applications. Although emerging multilevel inverters could overcome the primarily restriction of the conventional two-level inverters, they still needs developments in terms of hardware and software modification. During last decade, numerous novel multilevel inverters topologies have been proposed to reach to further optimized structure. The optimization concentrated on introducing a topology with less semiconductor devices, generating more voltage levels, single dc source structure and simplicity in dc capacitor voltage regulation. Moreover, various researchers also investigated on optimization of the switching techniques of the multilevel inverters as the other key factor of the operation efficiency. There are different parameters that can be investigated to optimize the switching technique, but switching frequency ratio and capability of controlling harmonics amplitudes are two fundamental parameters where modulation techniques can be optimized based on them.

The conclusion of the thesis can be briefly states that the optimization has been done on both multilevel inverter topology and modulation technique in order to enhance the efficiency on the targeted applications. For developing the inverter topology, the optimization has been applied to compact multilevel structure; Packed U-Cell, to achieve more operational, functional, optimized and reliable multilevel converter topology. The proposed topology in the thesis which is called as Packed E-Cell benefits of generating more voltage levels while the components are reduced. Moreover, the optimization on the modulation techniques has been implemented on the two low switching frequency methods, SHE and SHM strategies. These two modulation technique inherently benefits of low switching frequency ratio and precise control on the harmonics amplitudes. Therefore, SHE and SHM have been chosen to be developed in three different steps. First they have been optimized to deal with more

harmonics amplitude under very low switching frequency operation. Second, they have been designed for 4 wire inverters to handle different loads conditions under low switching frequency operation. And finally, they have been hybridized to have both feature of harmonic elimination and mitigation simultaneously in order to deal with different control objectives including CMV magnitude control at the same time. The conclusion of each chapter has been separately and comprehensively explained as the following:

In chapter 1, a comprehensive literature review on the conventional multilevel inverters and modulation techniques especially on low switching frequency methods including SHE-PWM and SHM-PWM is done. The full investigation on previous researches is greatly helpful to understand the advantages and disadvantages of the conventional modulation techniques and multilevel inverters which are required to perceive how their optimization can be done. It was reveal that the compact multilevel inverters like Packed U-Cell are appealing topology for single phase applications due to the single dc source structure. The five-level Packed U-Cell was emerged as promising compact multilevel converter topology, but, this structure confronts some drawbacks when it is extended to generates more voltage levels. Also, it was also investigated that low switching frequency techniques such as SHE-PWM and SHM-PWM are the appropriate switching strategies for high power applications of the multilevel inverters; but, they must be optimally designed for the targeted inverter topology and application.

Chapter 2 and Chapter 3 introduces an optimization strategy for SHM and SHE modulation technique in which a new constraint for switching angles is obtained based on the triplen harmonics analysis. According to the proposed switching angles constraint, all triplen harmonics are self-eliminated so as they are not required to be considered in the single phase equation of SHM and SHE. The proposed switching angles condition is obtained for a low switching frequency voltage waveform where number of angles is limited to the possible minimum. As a result, the optimized SHE and SHM are designed considering only non-triplen harmonics and their selected amplitudes are controlled through normal operation of switching angles calculations. Therefore, maximum harmonic amplitudes are controlled

while minimum number of switching angles is used. The proposed SHE and SHM with the optimal design are the appropriate alternative for single phase standalone application of multilevel inverters.

In chapter 4, SHE-PWM has been designed adaptably for both 4 wire configurations of the 3phase NPC inverters; 4leg 4wire NPC inverter and 3leg 4wire NPC inverter in order to capable them to deal with both symmetrical and asymmetrical loads under low switching frequency operation. It is clearly shown that SHE is more compatible to be used for 3leg 4wire NPC inverter over 4leg 4 wire NPC inverter because of less complexity in design process and switching angles calculations, better phase voltage harmonic content, less power losses. Also, it is shown that SHM can be also used for 4wire configurations of NPC inverter while it can be designed further optimal compared to SHE that can reach to better harmonics performance for inverter.

Chapter 5 illustrated that CMV can be reduced under low switching frequency operation based on the harmonics analyses. It is shown that CMV can be decomposed to its harmonics contents which contains only triplen harmonics and can be considered as on separated objective in the hybrid SHM technique. The proposed hybrid SHM contains both harmonic mitigation and harmonic elimination through a single cost function in order to control different objectives control. As to reach maximum CMV magnitude reduction, it is proven through precise mathematical analysis that selected triplen harmonics needs to be eliminated while selected non-triplen harmonics are mitigated to control the output voltage harmonic content. Therefore, two different objectives are tracked by the hybrid SHM technique including CMV magnitude and output voltage harmonic content due to the fact that the proposed hybrid SHM is empowered by both harmonic elimination and harmonic mitigation. It is proven that the hybrid SHM has better harmonic content performance in comparison to the pure operation of the SHE or SHM techniques.

Eventually, chapter 6 has proposed the novel compact multilevel structure so-called as Packed E-Cell which is a deep optimization of the Packed U-Cell structure. The idea of

Packed E-Cell is raised from using one E-Cell instead of two U-Cells in a compact structure which results in further reduced components counts, auxiliary dc link and simplicity of capacitor voltage balancing. While each U-Cell contains one dc capacitor which form a single auxiliary dc link, each E-Cell contains two dc capacitors which are horizontally placed and formed a single auxiliary dc link. In other words, while the capacitors are vertically extended in Packed U-Cell to create auxiliary dc link, the capacitors are horizontally developed in Packed E-Cell to form a single auxiliary dc link which also results in optimization of whole design of the converter topology. In addition, Packed E-Cell has the appealing feature in capacitor voltage balancing as the capacitors voltage can be easily regulated to the desired voltage level using the redundant switching states. Indeed, as a result of using E-Cell and horizontal extension of the dc capacitors, there would be the simultaneous charging and/or discharging states with effective redundant switching states that can guarantee the capacitor voltage balancing without any extra and complex voltage controller. Moreover, Packed E-Cell provides a unique feature which is the capability of continuing its operation under a faulty switch in which it can generate five- or seven-level voltage if a fault occurs for the bottom switches. Therefore, Packed E-Cell can cover the operation of Packed U-Cell that can be the reliable and optimized alternative for this converter. It also must be mentioned that nine-level Packed E-Cell topology can generate five-, seven-, nine- and eleven-level if the auxiliary dc link and dc capacitors are properly adjusted to the right voltage levels.

Future Works

This thesis concentrated on the optimization of the low switching frequency modulation technique; SHE-PWM and SHM-PWM, as well as development of Packed U-Cell topology by which new structure so-called as Packed E-Cell was introduced. However, it is not the final optimization for the modulation techniques and multilevel inverters topologies. This optimization can be continued as the future works for many years of research. Some initial ideas have been summarized in the following which can be considered in the future works:

Design A New Procedure for Optimization of the SHE and/or SHM Techniques

In this thesis a new switching angles constraint is obtained to optimize the conventional SHE and SHM technique as all triplen harmonics are self-eliminated without any extra calculations effort; so, maximum harmonics are controlled while switching frequency is minimized. However, other procedure can be also developed to optimize these modulation techniques. One solution is to develop an intelligent algorithm to solve the SHE and SHM equations in order to find more optimum switching angles. Other possibility is to develop the SHE and SHM equations based on the harmonic analysis so as the optimized switching angles can be obtained.

Developing SHE and SHM Technique for Other Multilevel Inverters Applications

In this thesis, SHE and SHM have been designed for two applications including 4wire inverters and CMV control; but, they still can be investigated for other standalone applications of multilevel inverters. One possible application is to use the SHE or SHM to control 3phase 4wire inverters (3leg 4wire inverter or 4leg 4wire inverter) for supplying two phase induction motor which demands particular design of these modulation techniques.

Design an Intelligent Based SHE and/or SHM Modulation Techniques

SHE and SHM are two offline modulation techniques in nature which are suffering from low dynamic operation. One solution is that to use intelligent control like ANN to find the most optimized switching angles. In this case, a large look up table with various trajectories of switching angles for a specific voltage waveform is obtained and ANN can be developed even using machine learning or deep learning techniques for find the best trajectory, or to complete a trajectory in an optimum way. Therefore, the most optimized switching angles can be applied to the multilevel inverters switches which improve the efficiency significantly.

Hybridizing SHE and SHM Modulation Techniques with Model Predictive Control

Another point that makes low dynamic feature for these two modulation techniques is the offline selection of the switching states of the targeted multilevel inverter topology. On the other hand, the conventional SHE and SHM confront an imposing challenge to be utilized for the multilevel inverters topologies where their capacitors voltages must be balanced using the redundant switching states. One solution is to combine the SHE or SHM technique with Model Predictive Control where switching states are being selected using model predictive control which can guarantee the capacitor voltage balancing. This strategy can be also used for other application like fault tolerant.

Designing a Single DC Source 3phase Compact Multilevel Inverter

As it was mentioned in the thesis, compact multilevel inverters topologies are very appealing for single phase application due to the fact single dc source structure. However, the conventional compact multilevel inverters needs three separated dc sources for three phase configuration which has its own challenging issue to be used in industry. Therefore, it is necessary to develop single dc source 3 phase multilevel inverters topologies which are more appropriate for three phase applications.

APENDIX I

DEADTIMES AFFECTS ON SWITCHING ANGLES

This appendix is related to chapter 3 which investigate the effect of delay in switching angles and capability in harmonic elimination. If the right side of switching angles constraints in five-level voltage waveform means π/3 or 2π/3 are affected by a delay of δ come from non-ideal effect such as dead time in real time implementation, the switching angles constraints will be:

$$\begin{cases} \alpha_1 + \alpha_2 = \dfrac{\pi}{3} \pm \delta \\ \alpha_3 + \alpha_4 = \dfrac{2\pi}{3} \pm \delta \end{cases} \quad \text{(A I-1)}$$

Then, the harmonics amplitude formula of Eq. (2.8) in chapter 2 will be as below that is affected by δ:

$$H_n = \frac{8E}{n\pi}\left(\cos(n(\frac{\pi}{6} \pm \frac{\delta}{2}))\ \cos(n(\alpha_1 - \frac{\pi}{6} \mp \frac{\delta}{2})) - \sin(n(\frac{\pi}{3} \pm \frac{\delta}{2}))\ \sin(n(\alpha_3 - \frac{\pi}{3} \mp \frac{\delta}{2})) \right) \quad \text{(A I-2)}$$

Two trigonometric terms that would have zero values for triplen harmonics are cos(n(π/6±δ)) and sin(n(π/3±δ)). Considering the fact that such non-ideal effects are really small as *δ=0.001*, the triplen harmonics would still have zero amplitude, approximately. However, due to developed technologies of the semiconductor devices, real-time controllers, sensors, ADCs, etc, that such delay is high enough and won't influence on the proposed technique to self-eliminate all triplen harmonics in single-phase applications.

Table-A-I-1 also shows a comparison study on the suitability of the SHE and SHM modulation techniques on the multilevel converters which are designed based on two well-known semiconductor switches technology including Qorvo Gallium Nitride (GaN) switches and Silicon-Carbide (SiC) switches. In general both techniques are suitable with these two types of switches. However, more efficiency and optimization is achievable if they are

applied on GaN switches as this switch technology is used for the high-efficiency power converter; so, there will be further power losses reduction. It must be again emphasized that these two low switching frequency modulation techniques are appropriate with all type of switches; but, maximum design optimization and efficiency achieved if they are applied on GaN switches. Also, as GaN can operates faster for turning ON and turning OFF the switches, the obtained experimental results for the harmonic amplitude mitigation of SHM and for the harmonic elimination of SHE would be much more closer to theoretical analyses.

Table-A I-1 Comparison study on the suitability of
SHE and SHM techniques for GaN and SiC switches

	(GaN) Switches	(SiC) switches
SHE-PWM or SHE-PAM	Highly Suitable	Suitable
SHM-PWM or SHM-PAM	Highly Suitable	Suitable
Hybrid technique of SHE and SHM	Highly Suitable	Suitable

APENDIX II

PROPOSED SELECTIVE HARMONIC MITIGATION FOR 3L/4W INVERTERS

This appendix is related to the chapter 4 introduces a Selective Harmonic Mitigation for the further THD reduction in 3L/4W NPC inverter. The comparison between two SHE for two four-wire inverters has shown that SHE as a low switching frequency method which pulses are precisely calculated is more compatible for 3L/4W topologies rather than 4L/4W ones because of the direct control on phase voltage harmonic content. However, SHE traditionally has an imposing challenge in controlling the voltage THD directly. Indeed, the only SHE purpose is to eliminate the amplitudes of the specified low harmonics orders while it has no control on the amplitudes of higher harmonics orders and consequently voltage THD remains uncontrolled. In this case, SHM technique can deal with controlling the amplitudes of low harmonics orders as well as voltage THD reduction (Sharifzadeh et al., 2018). SHM equations are derived from SHE principle; but, harmonics amplitudes are considered for mitigation instead of elimination. So, the direct voltage THD reduction is accessible and the voltage harmonic profile is subsequently improved compared to the SHE in the same switching frequency ratio. The mitigation criteria for harmonics amplitudes are set according to the standard level which have been identified in (Voltage characteristics of electricity supplied by public distribution systems, 2001; Harmonics, characteristic parameters, methods of study, estimates of existing values in the network, 1981) and presented in Table-A-II-1.

$$\begin{cases} F_1 = \left(\dfrac{4}{\pi} \sum_{i=1}^{k} (-1)^{i+1} \cos(\alpha_i) - m_a \right) \le L_1 \\ F_n = \dfrac{4}{n\pi} \sum_{i=1}^{k} (-1)^{i+1} \cos(n\alpha_i) \le m_a . L_n \;\; \forall \; n = 3,5,7,9...,49 \end{cases} \tag{A II-1}$$

In spite of this, SHM equations must be compatibly defined with the similar principle of the SHE for 3L/4W NPC inverter to empower it for handling the symmetrical and asymmetrical loads. To this end, SHM equations are defined for 3L/4W NPC inverter to include all triplen and non-triplen harmonics amplitudes below 49th in order to simultaneously mitigate the

selected non-triplen and triplen harmonics orders below standard criteria. Therefore, the proposed SHM equations for 3L/4W NPC inverter are expressed as Eq. (A II-1).

Table-A II-1 Allowable Amplitude for Harmonics

Non-Triplen Harmonics		**Triplen Harmonics**	
order (n)	Allowable Level (L_n)	order (n)	Allowable Level (L_n)
5	6%	3	5%
7	5%	9	1.5%
11	3.5%	15	0.5%
13	3%	21	0.5%
17	2%	>21	0.2%
19	1.5%		
23	1.5%		
25	0.2+32.5/n %		

Since SHM equations for 3L/4W NPC inverter are defined based on inequality relations and number of equations is more than number of switching angles, Eq. (A II-1) must be represented as an objective function; so, each SHM equations is engaged with a weighting factors. Moreover, defining SHM equations as an objective function would provide adequate flexibility to assume different parameters like voltage THD which need to be controlled. Therefore, the objective function of SHM equations for 3L/4W NPC inverter is stated as below:

$$OF(\alpha_1,\alpha_2,...,\alpha_K) = K_1(F_1 - L_1)^2 + (\sum_{n=3,5,7,9...49} K_n(F_n - m_a L_n)^2) + K_{THD\,2}THD \qquad \text{(A II-2)}$$

$$K_1 >> K_3 > K_5 > K_7 > K_9 ... > K_{THD} > ... > C_{49} \qquad \text{(A II-3)}$$

The harmonics amplitudes factors in objective function (K_1, K_2, …, K_n) are nonlinearly designated as Eq. (A II-3) so as the amplitudes of the determined non-triplen and triplen low harmonics orders are prioritized for proper mitigation with respect to the standard level of

Table-A-II-1. Also, the voltage THD factor (K_{THD}) is considered higher than harmonics amplitudes which have less chance for proper mitigation. Therefore, considering 12 angles in SHM equations for 3L/4W NPC inverter and solving the corresponding objective function, the triplen harmonics orders including 3^{rd}, 9^{th}, 15^{th} and 21^{st} as well as the non-triplen harmonics orders containing 5^{th}, 7^{th}, …, 23^{rd} are acceptably mitigated. Also, the amplitude of higher harmonics orders as well as voltage THD are controlled through the same objective function of SHM for 3L/4W NPC inverter, so as the THD value is decreased compared to SHE for 3L/4W one. Table-A II-2 shows the voltage THD values of the proposed SHM and SHE technique for 3L/4W NPC inverter when modulation index is 0.85. It must be noticed that the proposed SHM-PWM for 3L/4W NPC inverter can be further investigated for the future works.

Table-A II-2 Voltage THD Values Comparison Between
the Proposed SHM and SHE Techniques for 3L/4W NPC Inverter

Modulation Index	**Proposed SHM-PWM**	**Proposed SHE-PWM**
0.85	32%	56%

APENDIX III

CAPACITORS SELF-VOTAGE BALANCING AND ELECTRICAL MOTOR CONTROL IN THE PROPOSED HYBRID SHM-PWM TECHNIQUE

This appendix is related to the chapter 5 which investigate capacitor self-voltage balancing of 3phase 3level NPC inverter and electrical motor control when the proposed Hybrid SHM-PWM technique is applied. As it was mentioned in the paper, the 3phase NPC DC-Bus capacitors voltages are accurately self-balanced to the half of dc input voltage as it is shown in the Fig. 5.1. This capacitors self-voltage balancing occurs thanks to the quarter-wave symmetry of the output voltage waveforms which leads to the charging and discharging equality of DC-Bus capacitors. Figure-A III-1 shows the simulation results of the 3phase NPC inverter to analyze the dc capacitor voltages ripple in the switching angles scenarios of case I and case IV. As it can be seen, capacitors voltages are well-balanced to half of dc input voltage in both scenarios while the capacitors voltages ripples have been reduced in case IV compared to case I as a result of better harmonic control performance in case IV. Since, the selected triplen harmonics are eliminated and total triplen harmonic distortion is also controlled in the switching angle scenario of case IV, it not only leads to CMV magnitude reduction but it also suitably decreases the DC-Bus capacitors voltages ripples. Therefore, both CMV magnitude and dc capacitors voltages ripples reductions occur at the same time with the proposed Hybrid SHM-PWM technique which confirms its feasibility in dealing with multi-objectives control problems.

In this work, two well-known low switching frequency modulation techniques; SHE-PWM and SHM-PWM have been hybridized through a single cost function that both harmonic elimination and harmonic mitigation capability can be done simultaneously. It was shown that the proposed hybrid technique has better harmonic performance compared to pure operations of SHE and SHM since it is empowered by both harmonic elimination and mitigation where it can be an appropriate alternative for these two conventional modulation techniques.

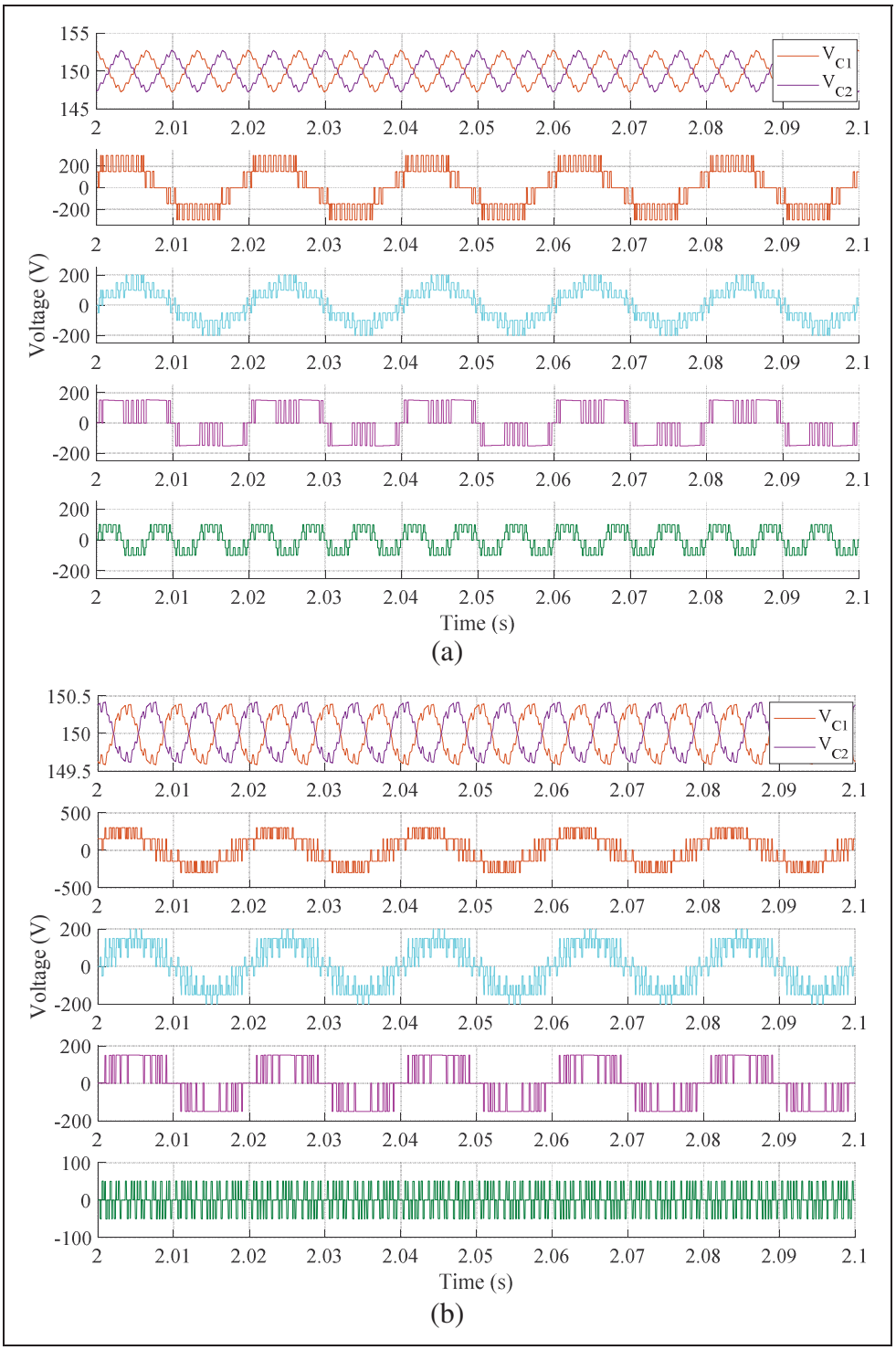

Figure-A III-1 Simulation results of 3phase NPC inverter for analysing DC-Bus capacitors voltages ripple in switching angles scenarios of case I and case IV,
(a) simulation results for switching angles scenarios of case I,
(b) simulation results for switching angles scenarios of case IV

The proposed technique has been applied to obtain two objectives, CMV magnitude reduction and output voltage harmonic distortion control. In order to demonstrate its capability of dealing with CMV magnitude reduction in motor drive application, some experimental analyses has been done accordingly. Figure-A III-2 shows the experimental results of 3phase NPC inverter when it supplies an AC motor while it is controlled by the proposed Hybrid SHM-PWM technique of the fourth scenario (where CMV is well-mitigated) and the dc input voltage changes during the test. As it can be seen from the provided experimental results, the CMV magnitude is being controlled as it was expected while the AC motor current was also controlled even under the sudden variation of the dc input voltage. Also, the capacitors voltages of the 3phase NPC inverter have been kept self-balanced under this dynamical condition while they also tracked the dc input voltage variation.

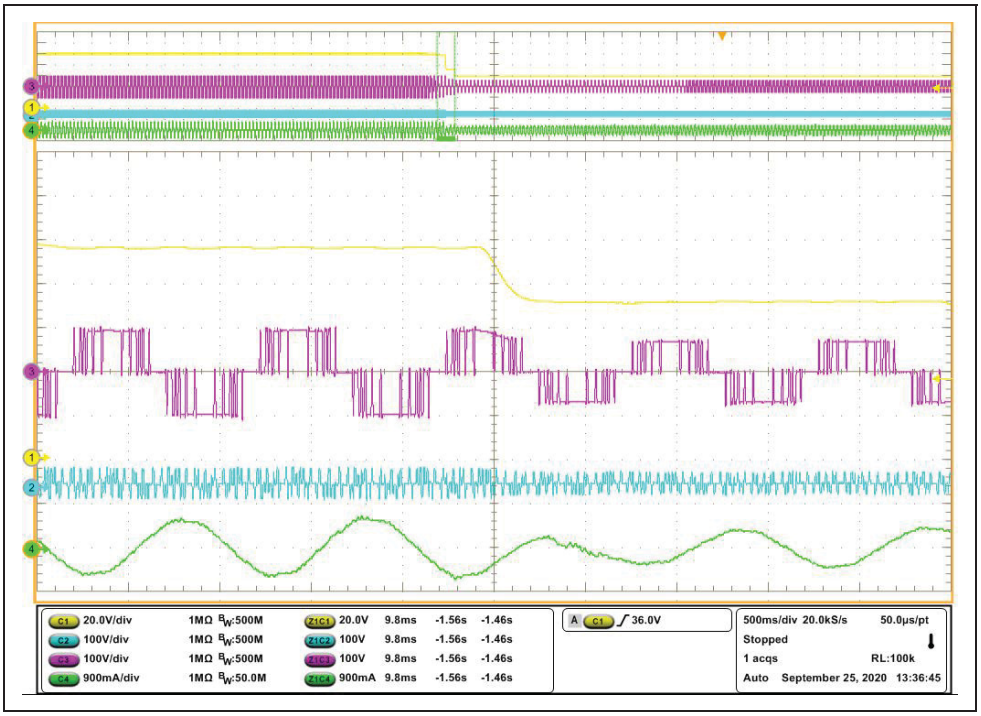

Figure-A III-2 Experimental results of dc capacitor voltage, branch voltages and CMV as well as motor current while 3phase NPC inverter supplies AC motor and dc input voltage suddenly changes

APENDIX IV

VOLTAGE/CURRENT THD AND CAPACITORS RIPPLES ANALYSES OF PEC9

In this appendix, some issue related to chapter 6 which is about the proposed compact structure; Packed E-Cell converter topology is being investigated. The half parabola waveform has been used as the carrier signal in the designed active voltage balancing PWM technique. Although any other carrier waveform could be utilized, half parabola has some interesting advantages. In comparison to the conventional triangular carriers, half parabola leads to improve the total harmonic distortion of voltage and current waveform. Figure-A IV-1 displays the output voltage THD obtained over a wide range of modulation index when the half parabola and triangular carriers are used with the same frequency in the proposed active voltage balancing PWM technique to control PEC9 inverter.

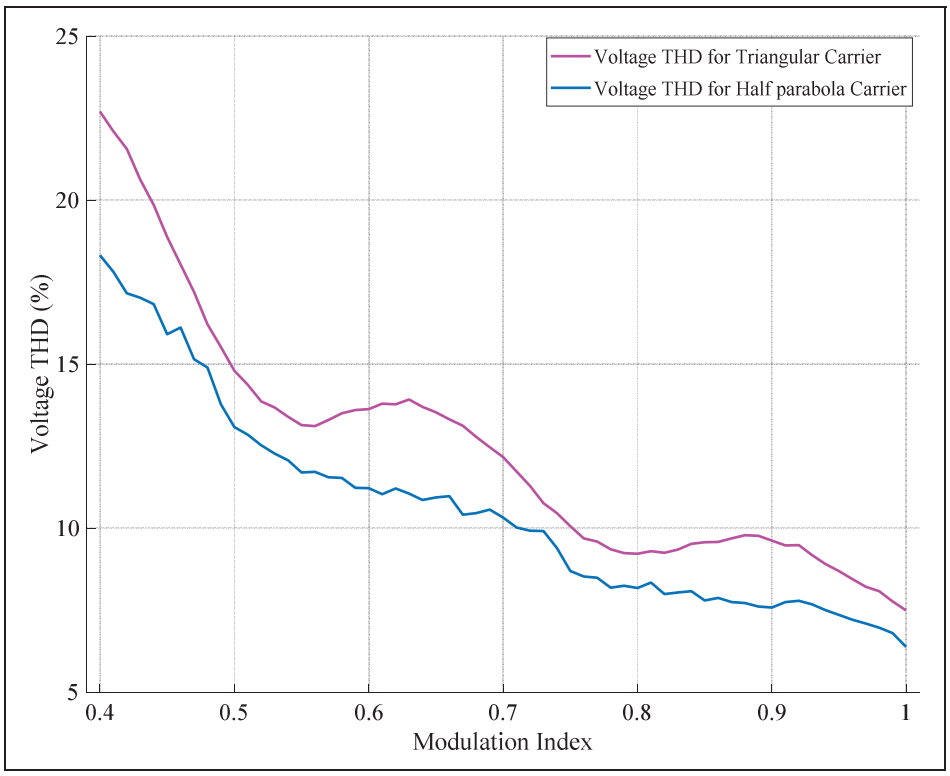

Figure-A IV-1 Voltage THD comparison of PEC9 inverter when triangular and proposed half parabola carriers are separately used for PWM technique

The inverter is connected to the linear R-L load (R=80 Ω and L=50mH) in both case of operation. The results show that using half parabola carrier reduces the voltage THD compared to the traditional triangular one. Moreover, in order to evaluate the quality of generated voltage/current waveform of PEC9 inverter using the designed half parabola carrier for the switching method, their THD value has been surveyed for a wide range of modulation index and different power factors. Figure-A IV-2 illustrates the voltage and current THD while the modulation index changes from 0.4 to 1. The result demonstrates that voltage and current THD are decreased as modulation index is increased which confirms the performance of the proposed half parabola PWM technique.

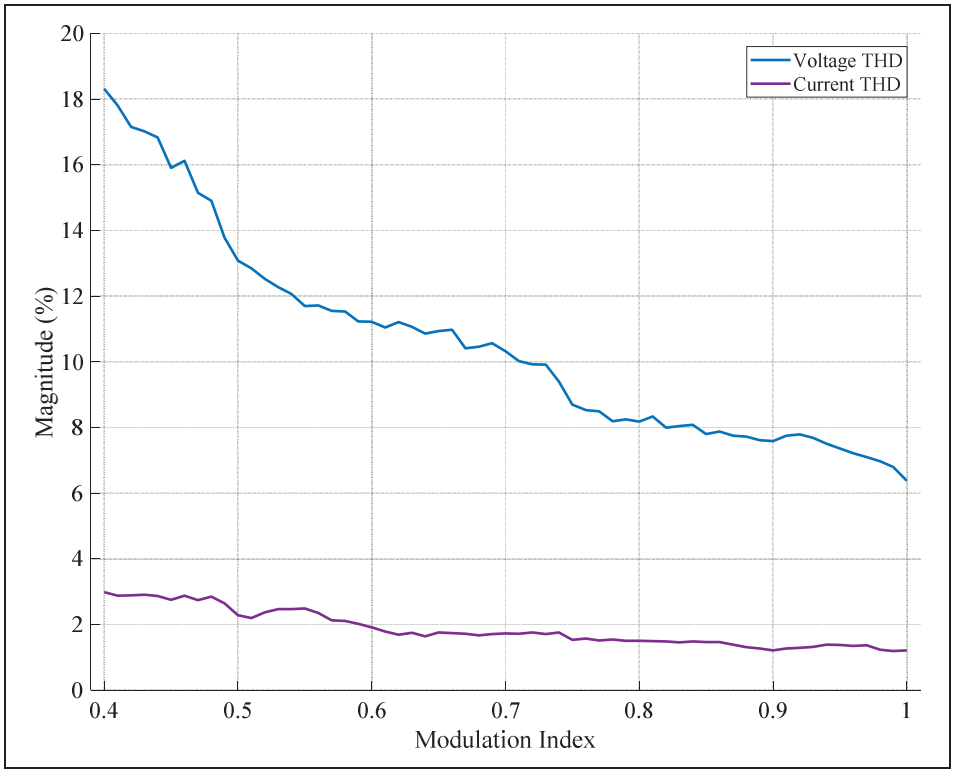

Figure-A IV-2 The obtained THD of voltage and current of PEC9 inverter for wide range of modulation index when it is controlled by proposed half parabola PWM technique

Also, the impact of the load value on the current THD is analysed. Figure-A IV-3 also shows the current THD for different values of linear resistor-inductance type of load. The value of resistor (R) is 80 Ω and the inductance values (L) have been considered as (10, 20, 30, 40 & 50) mH and the current THD has been obtained for each of these load condition when

modulation index is 0.8, 0.85, 0.9, 0.95 and 1. As it is clear in Figure-A IV-3, the current THD is significantly decreased by raising amplitude modulation index as well as increasing the inductance load value which acts as a filter.

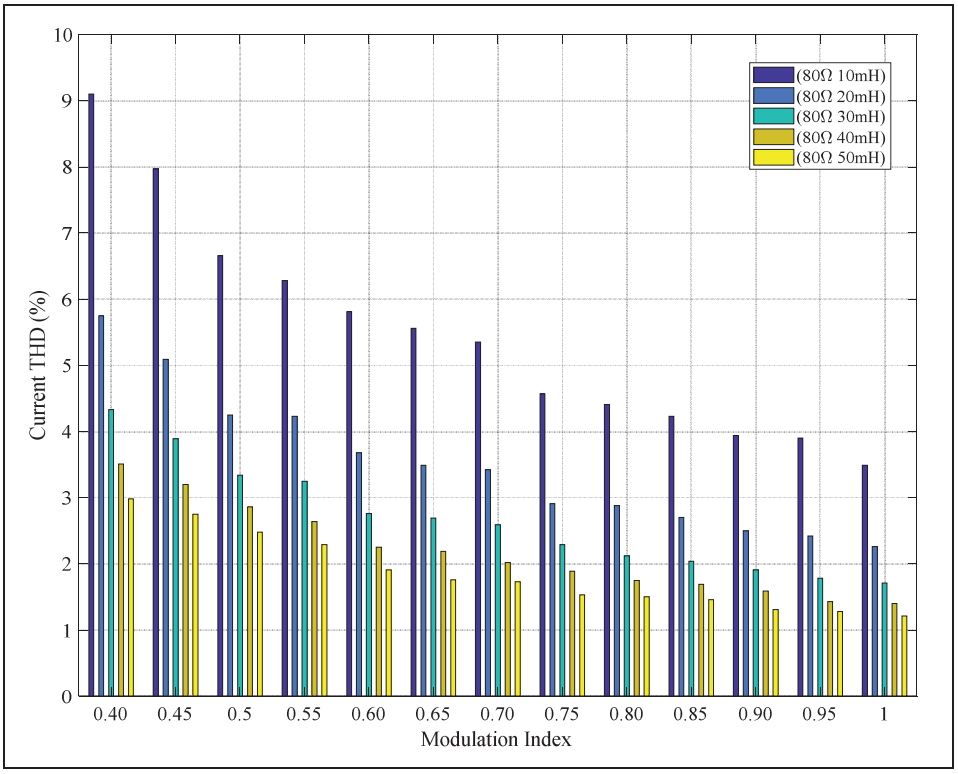

Figure-A IV-3 The attained current THD of PEC9 for different loads condition and modulation index

An active capacitor voltage balancing based half parabola PWM technique was designed to guarantee the desired regulation performance of DC-link capacitors voltages of PEC9 by adjusting the charging and discharging time using the redundant switching states of middle voltage level (±E/2). The various experimental tests of PEC9 illustrated that the proposed balancing technique is perfectly able to balance the capacitor voltage to one quarter of input DC voltage with acceptable voltage ripple below 5% under different operation conditions. Figure-A IV-4 displays simulation results of PEC9 inverter including DC capacitors voltages, output voltage and current when the modulation index varies for a vast range from 0.4 to 1. As it is clear, the capacitor voltages are balanced with voltage ripple kept less than 5% while the modulation index changes in a wide range. Number of voltage levels has been increased

from five- to seven- and to nine-level as a result of raising modulation index. The output current has been also increased consistent with rising of number of voltage levels.

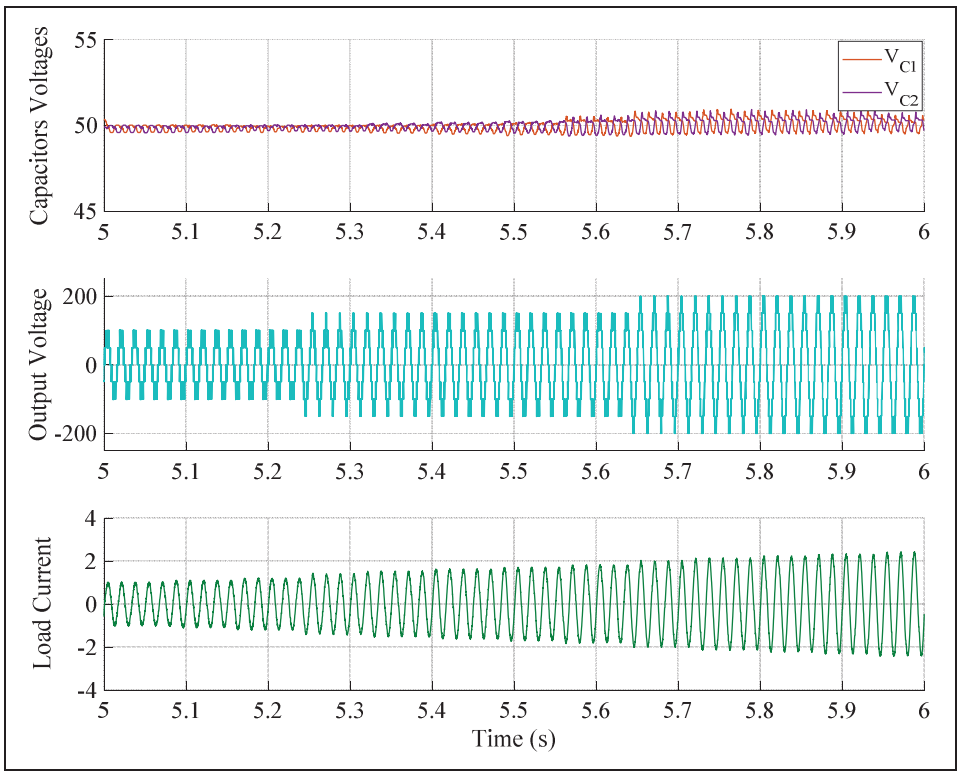

Figure-A IV-4 The capacitors voltages ripple of PEC9 while the modulation index changes from 0.4 to 1.1

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