Study, Modelling and Control of Bidirectional Battery Chargers for Real-Time Simulation Applications

by

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Étude, modélisation et commande de chargeurs de batterie bidirectionnels pour applications en simulation en temps-réel

Kevin-Rafael SORTO-VENTURA

RÉSUMÉ

Le travail réalisé dans ce projet a pour but de proposer une topologie de convertisseur AC-DC et une commande appropriées pour des chargeurs de batterie bidirectionnels à haute puissance. D'autre part, l'objectif est aussi de concevoir des modèles équivalents de ces convertisseurs afin de les implémenter en simulation en temps-réel. Cette recherche est motivée par la présence croissante des véhicules électriques sur les routes ainsi que par la demande accrue pour des stations de charge rapides et bidirectionnelles. En plus d'offrir une densité énergétique élevée et un écoulement de puissance bidirectionnel, les convertisseurs employés dans les chargeurs de batterie devraient assurer une bonne qualité de l'énergie. Par conséquent, ce mémoire étudie deux topologies de convertisseurs multiniveaux qui sont capables de minimiser la distorsion harmonique sur le réseau électrique grâce à leur nombre élevé de niveaux de tension. Donc, le convertisseur monophasé H-PUC à 23 niveaux est proposé avec une commande de type model predictive control. Ce convertisseur est implémenté en simulation en temps-réel avec le logiciel RT-LAB sur le simulateur OP4510 et il est démontré que cette topologie réduit considérablement les exigences de filtrage du courant AC lorsque comparé à des convertisseurs conventionnels. Ensuite, une commande de type deadbeat predictive control pour un écoulement bidirectionnel de la puissance est développé pour le convertisseur triphasé à 13 niveaux PM-ANPC. Des résultats de simulation obtenus dans Simulink confirment que la méthode de commande proposée peut efficacement réguler le courant AC et la tension du lien DC autant lorsque le convertisseur est en mode charge que lorsqu'il est en mode décharge. Finalement, un modèle équivalent du PM-ANPC est présenté et validé à l'aide d'un modèle référence qui utilise des blocs de SimPowerSystems dans Simulink. Puis, un simulateur en temps-réel OP4510 est utilisé afin d'illustrer la performance de simulation supérieure du modèle équivalent proposé par rapport au modèle référence.

Mots-clés: chargeur de batterie, véhicule électrique, convertisseur multiniveaux, qualité de l'énergie, simulation en temps-réel

Study, Modelling and Control of Bidirectional Battery Chargers for Real-Time Simulation Applications

Kevin-Rafael SORTO-VENTURA

ABSTRACT

The work done in this project aims to propose a suitable AC-DC converter topology and control method for high power, bidirectional battery chargers. Moreover, another objective is to design equivalent converter models suitable for real-time simulation applications. This research is motivated by the growing presence of electric vehicles and the increasing demand for faster and bidirectional battery chargers. In addition to high power density and bidirectional power flow capability, the converter used in the battery charger should offer good power quality. Therefore, this thesis studies two multilevel converter topologies, which are able to minimize harmonic distortion on the grid due to their high number of output voltage levels. Thus, the single-phase 23-level H-PUC is proposed with a model predictive controller. By implementing this converter in real-time simulation using the RT-LAB software and OP4510 simulator, it is shown that the topology greatly reduces the AC current filtering requirements when compared to conventional converter topologies. Then, a deadbeat predictive controller for bidirectional power flow is developed for the three-phase PM-ANPC 13-level converter. Simulation results obtained in Simulink demonstrate that the proposed controller can effectively regulate the AC current and DC link voltage during both charging and discharging modes of operation. Finally, an equivalent model of the PM-ANPC converter is presented and validated against a reference model that uses blocks from the SimPowerSystems library in Simulink. Then, an OP4510 real-time simulator is used to illustrate the improved simulation performance of the equivalent model with respect to the reference model.

Keywords: battery charger, electric vehicle, multilevel converter, power quality, real-time simulation

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LIST OF ABBREVIATIONS

AB2	Adams-Bashforth 2
AC	Alternating current
ANPC	Active-neutral-point-clamped
CHB	Cascaded H-Bridge
CPU	Central processing unit
DC	Direct current
DPC	Deadbeat predictive control
EMI	Electromagnetic interference
EV	Electric vehicle
FCS-MPC	Finite control set model predictive control
FE	Forward Euler
FFT	Fast Fourier transform
HB	Half-bridge
HF	High frequency
HIL	Hardware-in-the-loop
HNPC	Hybrid neutral-point-clamped
H-PUC	Hybrid Packed U-cell
IGBT	Insulated-gate bipolar transistor
KVL	Kirchoff voltage loop

LF	Low frequency
MLC	Multilevel converter
MLI	Multilevel inverter
MOSFET	Metal oxide semiconductor field-effect transistor
MPC	Model predictive control
NPC	Neutral-point-clamped
PCC	Point of common coupling
PFC	Power factor corrector
PLL	Phase-locked-loop
PM-ANPC	Paralleled modular active-neutral-point-clamped
PUC	Packed U-cell
RCP	Rapid control prototyping
RTS	Real-time simulation
SIL	Software-in-the-loop
SPS	SimPowerSystems
SPWM	Sine pulse width modulation
SVM	Space vector modulation
THD	Total harmonic distortion
VSC	Voltage source converter
VSI	Voltage source inverter

INTRODUCTION

The presence of electric vehicles (EVs) is steadily increasing on the roads worldwide. This increase is prompting the implementation of a higher number of battery charging stations due to the higher demand. In addition, EVs are themselves becoming more power hungry and are starting to carry batteries with larger capacities. As a result, even more high power, fast DC battery chargers need to be installed (Burnham *et al.*, 2017; Khaligh & Antonio, 2019). Indeed, manufacturers are constantly pushing the limits of their peak charging rates with Tesla, for example, achieving up to 250kW of power delivery from the third version of their supercharger (Tesla, 2019). However, high peak power delivery is not the only feature that is desirable in battery chargers. In fact, manufacturers and researchers have also been developing battery chargers with bidirectional power flow capabilities (Restrepo, Morris, Kazerani & Cañizares, 2018). Bidirectional battery chargers have the ability to use the connected EV batteries as storage devices and thus, can send the battery power back to the grid. Another consideration when designing these chargers is the control of the power quality at the point of interconnection with the grid. Since charging stations are typically composed of multiple high power chargers all on the same grid connection, and if we consider that these are bidirectional chargers, then ensuring good power quality becomes even more important.

Objectives

Therefore, one of the objectives of this thesis is to propose an AC-DC converter topology and control method that will satisfy the high power density, bidirectional power flow and good power quality requirements for battery charger applications. Then, in an effort to facilitate the study of large systems containing multiple units of the proposed battery charger, this thesis also aims to develop an equivalent model of the proposed converter topology. This model is to be tested and validated for real-time simulation applications.

Thesis Outline

The first chapter of this thesis is a literature review that goes over conventional AC-DC converter topologies, such as the full-bridge and neutral-point-clamped (NPC) converters, that are commonly used in battery chargers. Then, an overview of some multilevel converter topologies is done with an emphasis on their advantages over the conventional topologies. Next, the literature review gives a brief overview of real-time simulation, its main features and the importance of equivalent converter models used in real-time simulation. In chapter 2, the single-phase Hybrid-PUC 23-level converter topology and its associated model predictive controller (MPC) are proposed. A simple equivalent model is also developed for the Hybrid-PUC and real-time simulation results are provided to validate the design. Chapter 3 studies the three-phase paralleled modular active-neutral-point clamped (PM-ANPC) 13-level converter and proposes a deadbeat predictive control method for it that allows for bidirectional power flow. The proposed system is tested and offline simulation results are given. Next, chapter 4 proposes a detailed equivalent model with a decoupled DC link for the PM-ANPC. The equivalent model is compared to a reference model in order to confirm its validity. Then, a comparison of their performance is done for both offline and real-time simulation to highlight the improved performance of the proposed equivalent model. Finally, the conclusion of this thesis regroups the main takeaways of the research done and gives recommendations for potential future works.

CHAPTER 1

LITERATURE REVIEW OF ELECTRIC VEHICLE BATTERY CHARGERS, MULTILEVEL CONVERTERS AND REAL-TIME SIMULATION

1.1 Introduction

The increasing rate of the electrification of transportation combined with larger battery capacities are prompting more research to be done in the field of fast DC battery chargers. Since this thesis aims to contribute to the field of battery charger topologies and equivalent converter models, an appropriate literature review needs to be done. Indeed, it is relevant to assess the current state-of-the-art in terms of the power electronic converters that are commonly used in battery chargers currently. This assessment can provide information as to what are the important features that a converter needs in order to properly operate as a battery charger. Then, in an effort to iterate upon conventional battery charger topologies, a study of the main multilevel converter topologies is done to show their inherent advantages. Moreover, it is relevant to define the importance of real-time simulation and how it can benefit the testing and prototyping of large and complex circuits such as those containing multilevel converters.

Therefore, this literature review begins by reviewing the main power electronic converter topologies used currently in fast DC battery chargers. Next, an overview of the main multilevel converter topology families is done with an emphasis on their advantages when compared to conventional two or three-level converters. Finally, a brief review of real-time simulation and equivalent converter models is presented so as to highlight their importance in the field of prototyping and testing of large electrical systems.

1.2 Converters Commonly Used for Battery Chargers

There exist different types of EV battery chargers, which are classified by their power levels ranging from levels 1 to 3. Levels 1 and 2 are lower power on-board chargers that are integrated within the vehicle's own power electronics, and are typically fed by single-phase grid connections.

In comparison, level 3 charging stations output much higher peak power (50kW +) and usually perform the three-phase AC to DC conversion through a dedicated power electronic converter in the station itself (Tran, Sutanto & Muttaqi, 2017). The latter type, also known as fast DC charging, is the focus of this thesis. As such, the full bridge and the neutral-point-clamped converters, two of the more common three-phase AC-DC converters used in battery chargers (Yilmaz & Krein, 2013), are reviewed in this section.

1.2.1 The Three-phase Full Bridge Converter

Probably the most common three-phase converter is the full bridge converter pictured in Fig. 1.1. It is used in many different applications as a power factor corrector (PFC) and has multiple interesting advantages.

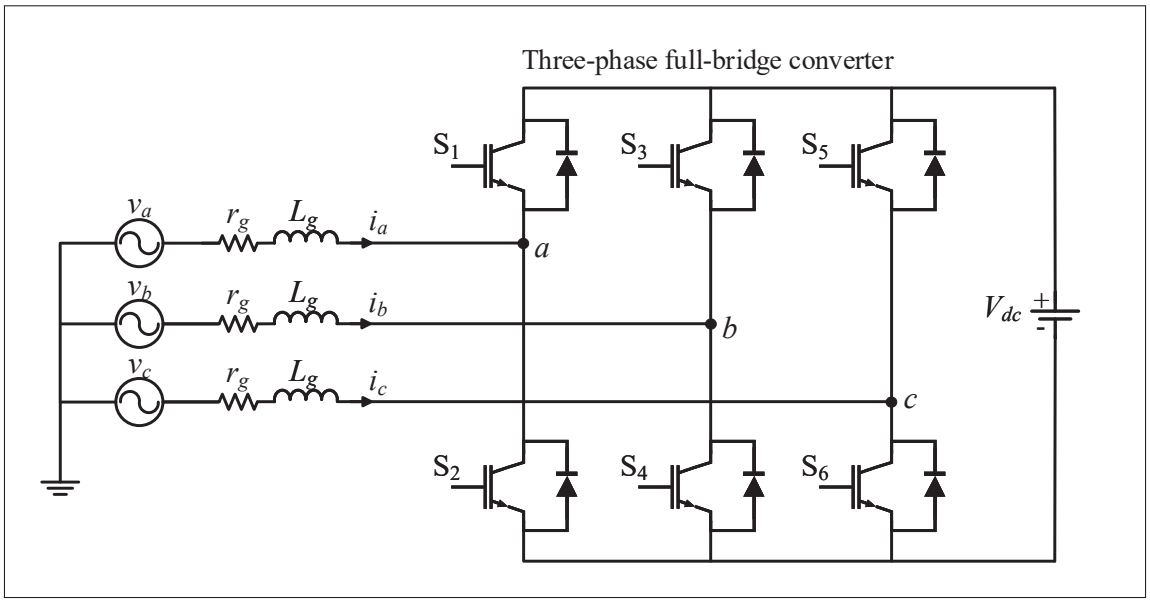

Figure 1.1 Circuit diagram of the three-phase full-bridge converter

Firstly, it is composed of relatively few power electronic switches with only six of them across all three phases. The full bridge converter's simple topology also makes designing control systems for it an easy task. All this can be achieved while still maintaining relatively good power efficiency and near unit power factor (Kolar & Friedli, 2013).

However, there are some drawbacks with this converter. Indeed, since this is only a three-level voltage converter, the input AC side requires large and bulky inductors in order to filter the current and achieve acceptable total harmonic distortion (THD) levels. Furthermore, the maximum voltage stress experience by the semiconductor switches is equal to the full value of the DC link voltage, which means that their reliability is reduced in the long term (Yilmaz & Krein, 2013).

1.2.2 The Neutral-point-clamped Converter

Some of the disadvantages mentioned above are mitigated in battery chargers using the neutral-point-clamped (NPC) converter. The general topology of this converter is illustrated in Fig. 1.2. Unlike the full-bridge converter, the NPC converter uses a combination of active semiconductor switches, passive diodes and capacitors (Rodriguez, Bernet, Steimer & Lizama, 2010).

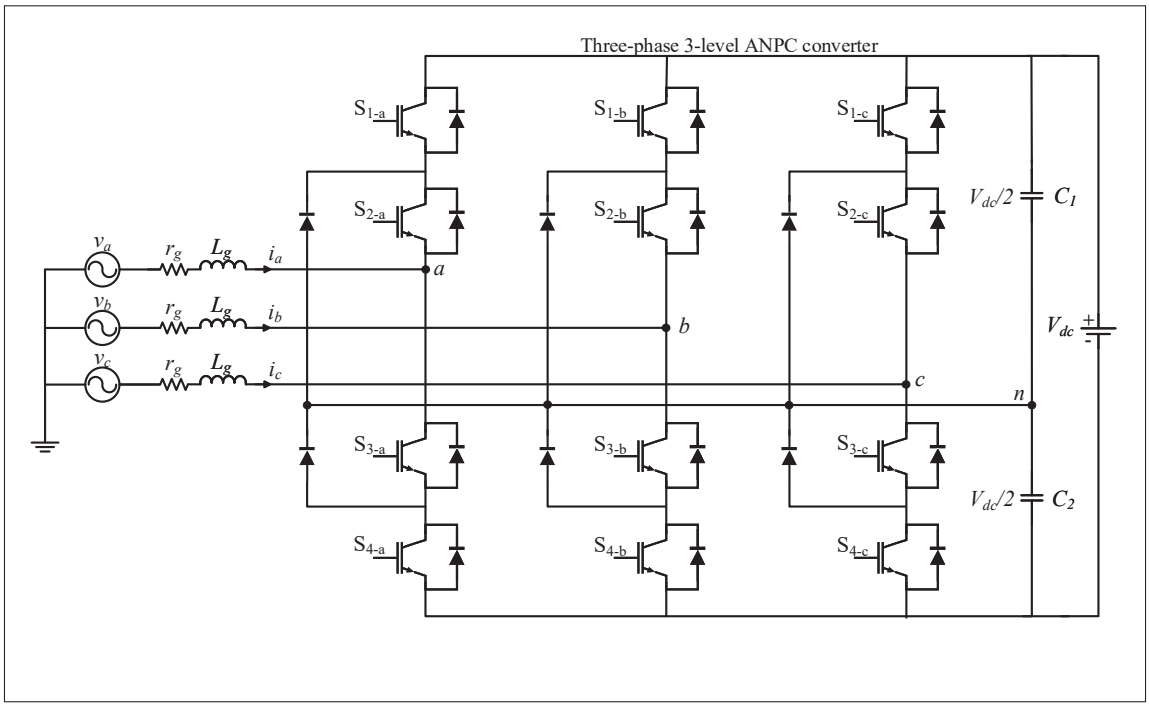

Figure 1.2 Circuit diagram of the three-phase NPC converter

More precisely, the three-phase converter has a total of 12 switches, 6 diodes and 4 capacitors. It is also relatively simple to control and can achieve good efficiency and power factor.

In addition, the configuration of the NPC makes it so that the semiconductor switches only need to support the stress of half of the DC link voltage, meaning that it is possible to use devices rated for smaller voltages which can achieve higher frequencies. The NPC converter also produces three phase-to-ground or five line-to-line output voltage levels, making its output naturally more sinusoidal that the full-bridge. These features combine to result in higher power density and a reasonable current THD value while using smaller filtering inductances (Yilmaz & Krein, 2013; Rivera, Wu, Kouro, Yaramasu & Wang, 2015).

1.3 Multilevel Converters and Their Advantages

Many of the limitations that exist in the conventional AC-DC converters can be remedied with multilevel converters (MLC). These advantages are important when considering that battery chargers must satisfy grid interconnection standards such as the IEEE 1547 (Standard for Interconnection and Interoperability of Distributed Energy Resources with Associated Electric Power Systems Interfaces), which requires the current THD to be less than 5% at the point of interconnection (IEEE, 2018). In fact, these converters, when coupled with appropriate modulation techniques and control methods, can generate a high number of output voltage levels, which results in a staircase shaped voltage waveform that is much closer to a sinusoidal wave than a two or three-level converter (Rodriguez, Jih-Sheng & Fang Zheng, 2002; Akagi, 2017). This comparison is further illustrated in Fig. 1.3 with examples of a 3-level waveform and a 7-level waveform.

In fact, the improvement of MLCs in terms of THD are well illustrated in the graph in Fig. 1.4. In the plot, it becomes clear that by increasing the number of output voltage levels, the value of the voltage THD significantly decreases. Moreover, once a high enough number of voltage levels is reached, such as the 23-level seen in the graph, an almost filter-less implementation becomes possible since the THD obtained there is already less than the maximum 5% mandated by the IEEE 1547 standard.

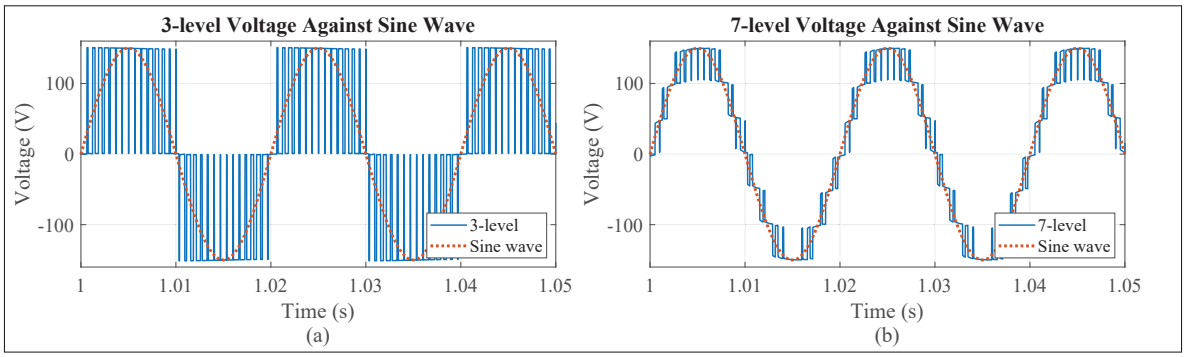

Figure 1.3 Waveform comparison of a perfect sine wave with (a) a three-level voltage and (b) a 7-level voltage

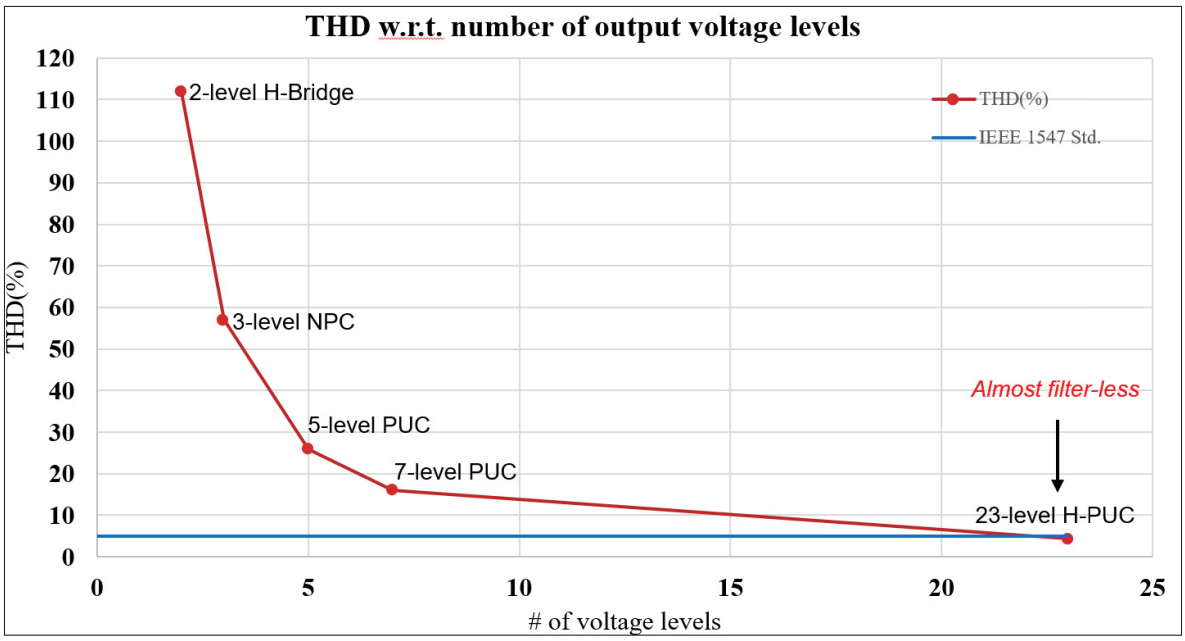

Figure 1.4 Voltage THD with respect to the number of voltage levels

Hence, MLCs can help in greatly reducing the harmonic content of the AC current and voltage, as well as decreasing the dv/dt and electromagnetic interference. Ultimately, MLCs generate nearly sinusoidal voltages with lower THD, which considerably reduces the filtering requirements on the input AC current and more easily respect the interconnection standards (Rodriguez *et al.*, 2009; Abu-Rub, Holtz, Rodriguez & Baoming, 2010; Kouro *et al.*, 2010). Therefore, a review of three major types of MLCs is done in this section.

1.3.1 The Cascaded H-bridge Converter

The first type of MLC that is being studied in this thesis is the cascaded H-bridge (CHB). As its name suggests, this converter is composed of a cascade of multiple half-bridge converters. Indeed, the cascading of multiple half-bridge modules has the effect of augmenting the total number of output voltage levels produced by the CHB converter (Malinowski, Gopakumar, Rodriguez & Pérez, 2010; Zhang & Gao, 2019). An example of a single-phase CHB converter is displayed in Fig. 1.5.

The circuit diagram reveals the modularity of the CHB topology. In fact, any number of half-bridge modules can be added as illustrated by the ellipses between the connection of modules 1 and n. Naturally, the number of modules n will determine the number of output voltage levels N_L as defined by:

$$N_L = 2n + 1. \tag{1.1}$$

Therefore, if we take for example the case with two half-bridge modules, then it would produce 5 phase-to-ground voltage levels and this would become 9 line-to-line voltage levels in a three-phase configuration. For the latter case, the three-phase circuit would contain a total of 24 semiconductor switches, which is considerably more than either the three-phase full bridge or NPC converters and hence increases the overall cost. Another drawback is that each of the half-bridge modules requires its own DC voltage source. This configuration is not ideal in the context of a battery charger for which it is more desirable to have a single DC link through which all of the converter's power is transferred. For the CHB, this means that each of the DC voltage links could supply power to separate loads but only at a fraction of the rated converter power. For a high power battery charger, the objective is to supply as much power as the converter can support to a single battery load. In that case, there would have to be an additional conversion stage that would consolidate all the DC sources into a single DC link, and this would further increase the cost and complexity of the device.

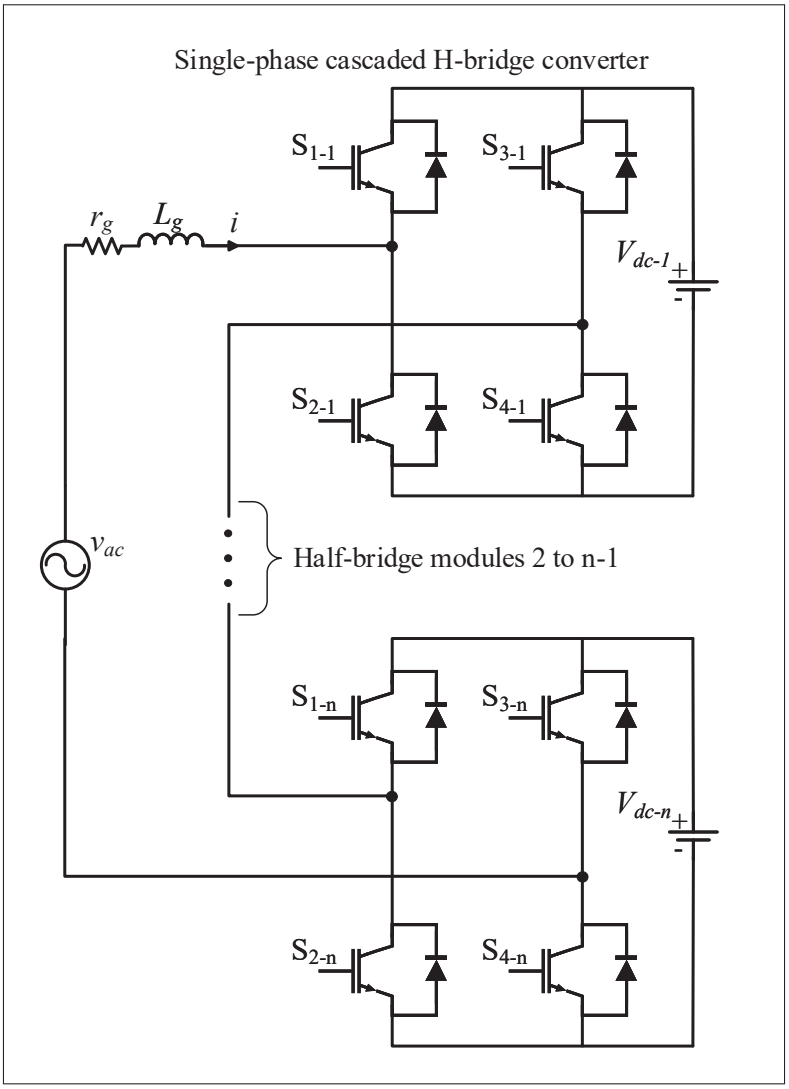

Figure 1.5 Circuit diagram of a single-phase cascaded H-bridge converter

In conclusion, the CHB converter offers the same advantages as the full-bridge converter: easy control, good efficiency and near unity power factor. Additionally, it also benefits from the high number of voltage levels, which considerably reduce the THD of the input AC current and voltage (Villanueva, Correa, Rodriguez & Pacas, 2009). However, the high number of semiconductor switches and the need for multiple DC sources keep the CHB topology from being the ideal choice for a battery charger.

1.3.2 The Active-neutral-point-clamped Multilevel Converter

The next type of multilevel converter topology is the active-neutral-point-clamped (ANPC) converter. There are multiple variations of this topology, but the basic circuit is essentially the same as the NPC converter, except that the passive diodes are replaced with active semiconductor switches (Rodriguez *et al.*, 2010). The corresponding circuit diagram is reproduced in Fig. 1.6 for the three-level ANPC (3L-ANPC) converter.

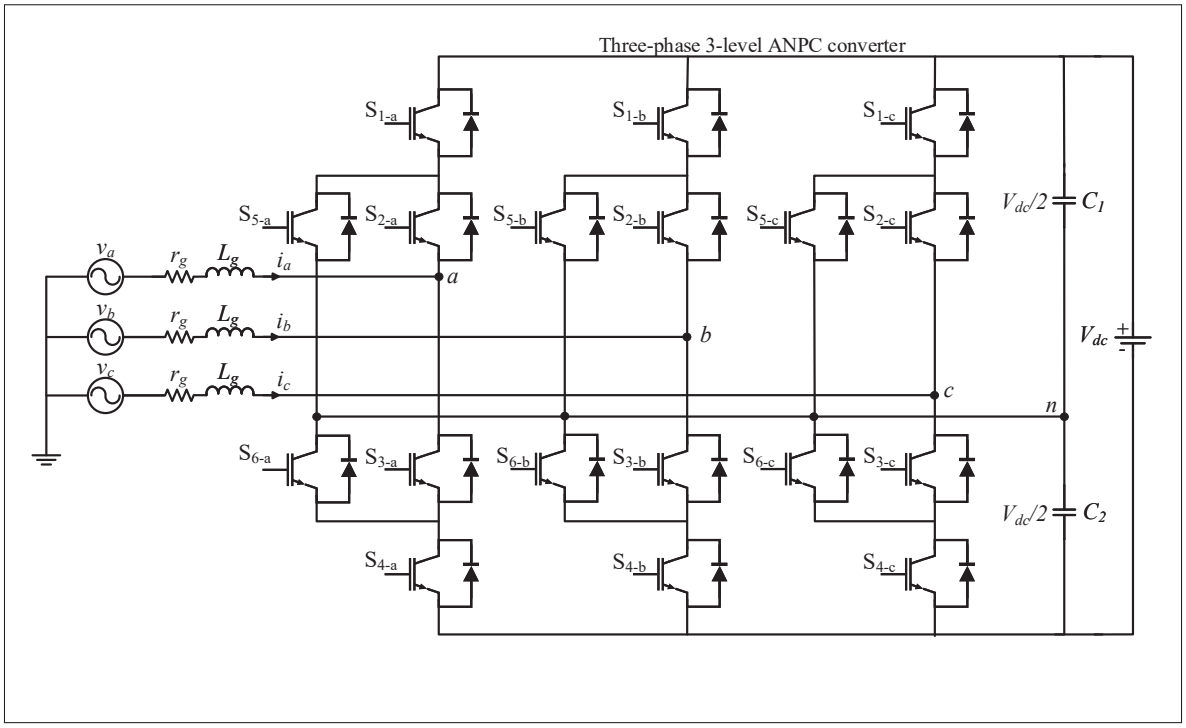

Figure 1.6 Circuit diagram of the three-phase 3L-ANPC converter

The main advantage of the ANPC over the NPC is that the active control of the switches allows to mitigate the unequal loss distribution caused by the diodes in the NPC (Rodriguez *et al.*, 2010). However, this implementation of the ANPC does not increase the number of output voltage levels when compared to the NPC. Hence, more advanced, modular implementations of the ANPC have been developed that increase the number of voltage levels (Abarzadeh, Kojabadi & Chang,

2016). An example of these, the five-level ANPC (5L-ANPC), in single-phase form is shown in Fig. 1.7.

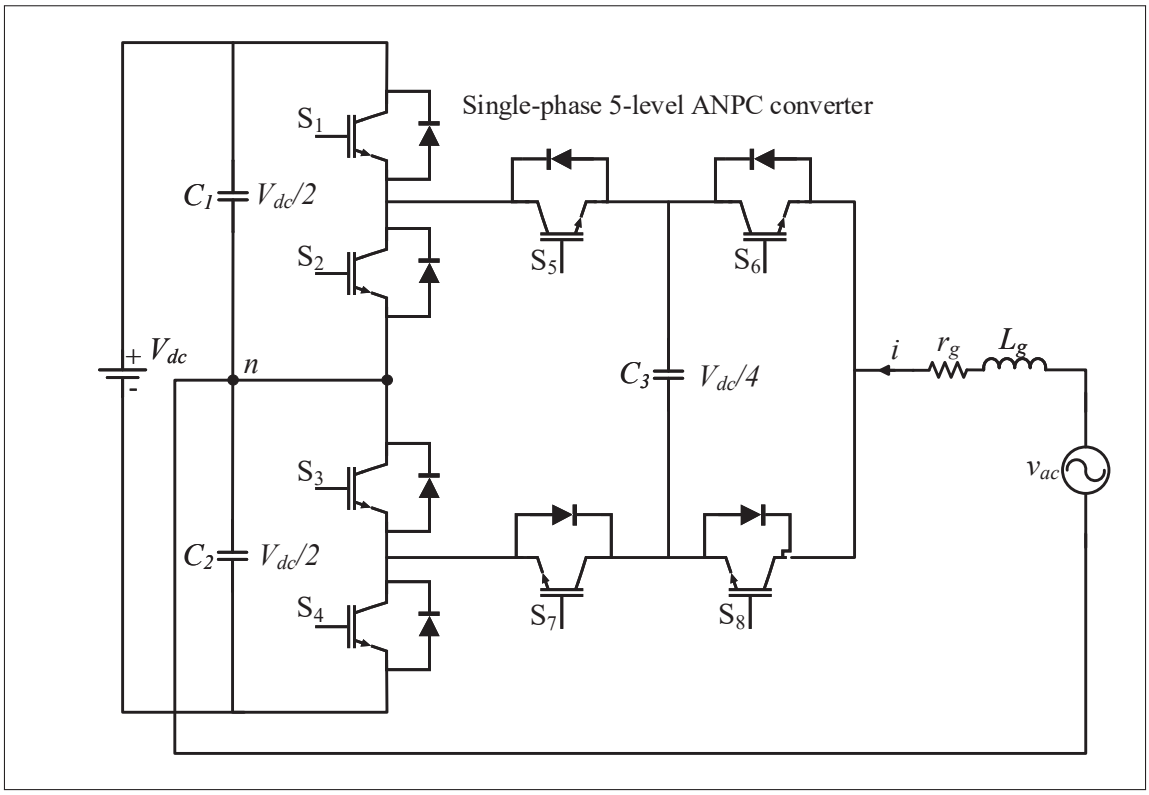

Figure 1.7 Circuit diagram of the single-phase 5L-ANPC converter

The diagram demonstrates that by adding a cell to the converter like the one shown in the diagram, it is possible to increase the number of output voltage levels by two. The added cell results in two additional switches and one capacitor per phase when compared to the 3L-ANPC. By regulating the voltage of the added capacitor to 1/4 of the DC link voltage and by employing the appropriate switching patterns, the five voltage levels are achieved. Besides, this approach is also modular, which means that by adding more cells, it is possible to further multiply the number of output voltage levels (Dargahi *et al.*, 2019; Li, Bhattacharya & Huang, 2011).

As such, for the three-phase 5L-ANPC, the converter is composed of 24 active power switches, which is equal to the 5-level CHB described previously. However, it should be noted that

the 5L-ANPC also adds a total of 9 capacitors when compared to the CHB topology. These capacitors increase the cost and the control complexity as they need to be actively regulated at specific values in order to achieve the 5 voltage levels. Despite these limitations, the ANPC might still be more attractive than the CHB for a battery charger since the former requires only a single DC voltage source. Furthermore, like for the NPC, the semiconductor devices do not need to be rated for the full values of the DC link voltage. In fact, for one phase of the 5L-ANPC, four of the switches are rated for half of the DC link voltage, and the other four are rated for a quarter of that, thus giving this converter a considerably higher power density than the CHB topology.

1.3.3 The Packed U-cell Family of Multilevel Converters

A newer family of multilevel converters is one called the packed U-Cell (PUC) family. They are capable producing a high number of voltage levels while using fewer active components than either the CHB or ANPC topologies (Ounejjar, Al-Haddad & Gregoire, 2011). A circuit diagram of the single-phase five-level PUC (PUC5) is given in Fig. 1.8.

The circuit is composed of 6 semiconductor switches, one DC voltage source and one capacitor. These numbers are of course multiplied by three when considering the three-phase implementation of this converter. It is through proper regulation of the capacitor voltage at one half of the DC source's value that the five voltage levels are achieved. Moreover, it has also been shown that the same topology can generate seven voltage levels when the capacitor is instead regulated at a third of the DC source voltage and an appropriate modulation method is used (Ounejjar, Al-Haddad & Dessaint, 2012). Also, like for the ANPC topology, the number of voltage levels of the PUC can be augmented even more by adding cells composed of one capacitor and two switches. Indeed, there exist implementations of the PUC converter that achieve 9 voltage levels (Abdelbasset, Refaat & Trabelsi, 2019) as well many other PUC derivatives that can generate even higher numbers of voltage levels (Sharifzadeh & Al-Haddad, 2019; Arazm & Al-Haddad, 2020).

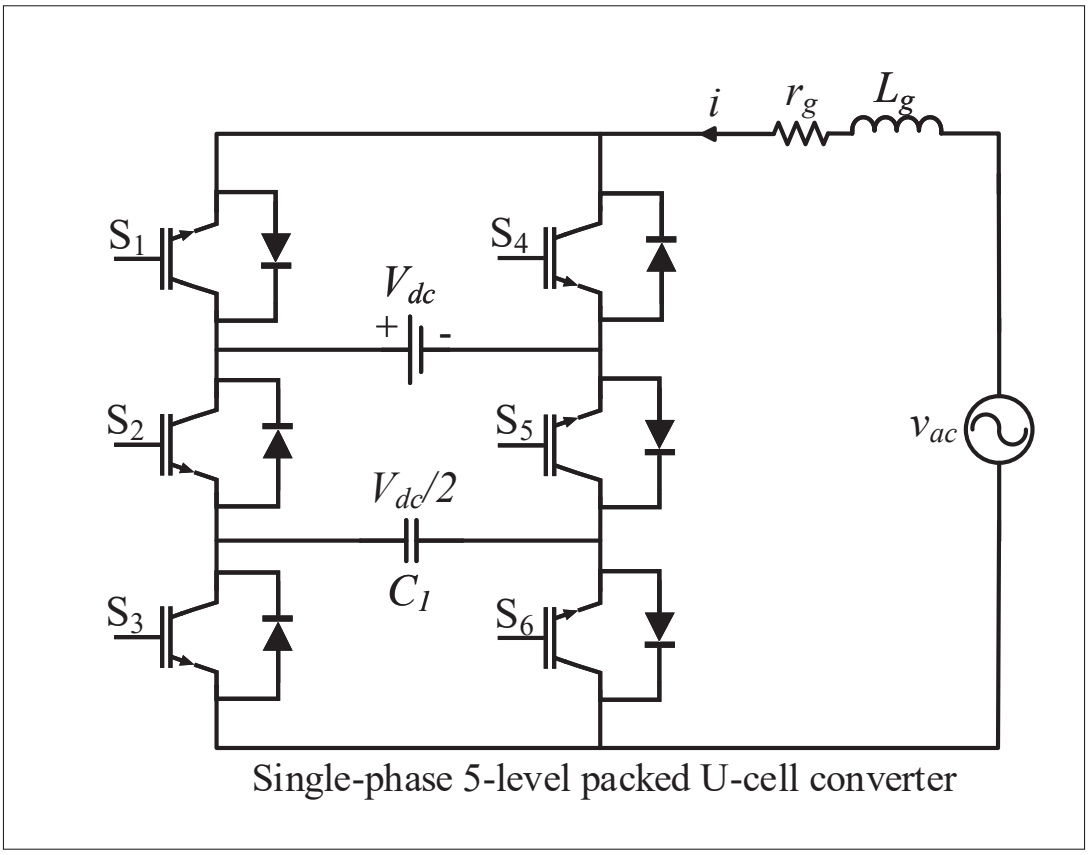

Figure 1.8 Circuit diagram of the single-phase PUC5 converter

Once again, if the three-phase 5-level PUC5 is considered, the circuit would contain a total of 18 semiconductor switches, 3 capacitors and 3 voltage sources. As it was discussed previously with the CHB converter, the multiple DC sources in the three-phase PUC are not desirable for battery charger applications. However, it is important to note that the PUC5 still requires six fewer active switches than both the CHB and ANPC variants for the same number of voltage levels. Furthermore, it also requires 6 fewer capacitors than the corresponding ANPC topology, making the PUC the option with the best number of voltage levels to component number ratio. Consequently, the PUC family of multilevel converters is determined to be one of the more promising options for designing a high power density battery charger.

1.4 Real-time Simulation and Equivalent Converter Models

This thesis aims to study bidirectional battery chargers based on multilevel converter topologies that are large and complex. Such systems are not always easily implemented as hardware prototypes and therefore, simulation is often employed when trying to design and validate these systems. However, normal or offline simulation is not always sufficient to properly validate complex electrical systems like those that contain power electronic converters.

1.4.1 The Importance of Real-time Simulation

Indeed, it is often important to be able to test power converters with real hardware controllers. This kind of setup is known as hardware-in-the-loop (HIL) simulation, where a real hardware controller is physically connected to a simulator that is emulating the electrical system under test (Javadi, Abarzadeh, Grégoire & Al-Haddad, 2019). Because the simulated system is connected to a real device, the simulation needs to be performed in real-time, hence the importance of real-time simulation (RTS). Indeed, RTS makes use of high performance simulators, such as the OP4510 from Opal-RT, in order to perfectly match every simulation second with every real-time second (Yamane *et al.*, 2019; Bouzid, Sicard, Paquin & Yamane, 2016). In other words, for a given fixed time step, every necessary computation of the simulated model needs to be completed within that time step. This way, the hardware controller and the simulated system can communicate properly and an HIL test can be performed. A visual representation of the differences between offline simulation that is slower than real-time and true real-time simulation is depicted in Fig. 1.9.

As can be seen in the diagram, a real-time simulation can complete all necessary operations $f(t)$ within each fixed time step. These computations include the calculations of the simulated system but also other overhead operations such as operating system calls and interrupt handling (Parizad, Baghaee, Iranian, Gharehpetian & Guerrero, 2020; Lauss, Faruque, Schoder, Dufour, Viehweider & Langston, 2016). In comparison, offline simulations will not always complete all

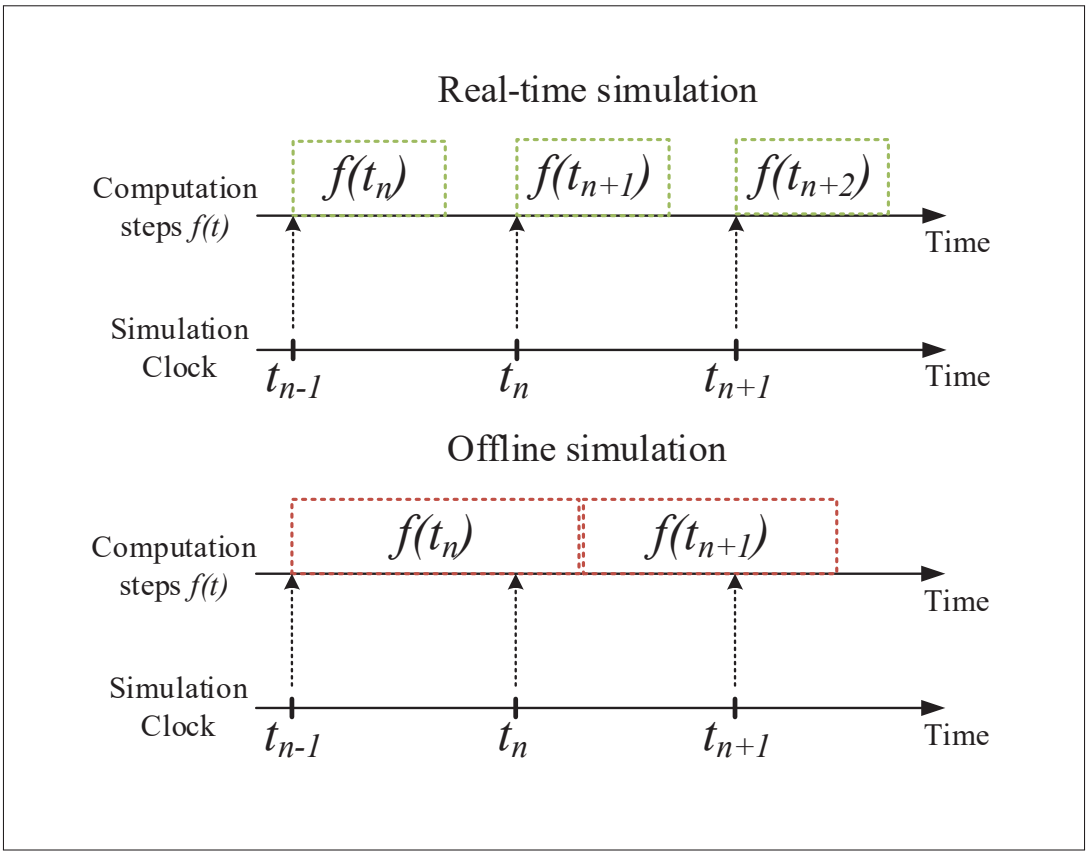

Figure 1.9 Diagram of the computational differences between offline and real-time simulation

calculations within a fixed time step, especially since the time step needs to be quite small in order for the simulated system to yield accurate and precise results.

1.4.2 Performance Considerations and Equivalent Converter Models for Real-time Simulation

However, there are some performance limitations with RTS that exist when dealing with both small computation time steps and systems composed of large numbers of semiconductor switches, such as the MLCs that are studied in this thesis. Additionally, those switches are typically operated at high frequencies, which further increases the already considerable computational burden in simulating MLCs. This burden is a result of the different circuit solving methods that are employed by discrete time step simulation software such as Matlab/Simulink. These

solving methods essentially store and solve large sets of matrices at every computation time step depending on the number of possible switching states of the converters under test. Furthermore, the sizes of these matrices increase either when the number of switches increases, when the switching frequency is increased or when the fixed time step is decreased. All of these factors contribute to adding more computations at every time step, thus making the real-time simulation of MLCs at reasonably low time steps difficult (Dommel, 1969; Dufour, Mahseredjian, Bélanger & Naredo, 2010). Therefore, researchers have proposed some interesting workarounds that would allow to overcome these limitations and achieve true real-time simulation of MLCs.

One of the potential solutions to these limitations is to replace the converters that are usually modelled with non-linear, diode-based semiconductor models, with equivalent models based on controlled voltage sources and switching functions. Indeed, some of these equivalent models that use controlled voltage sources and switching functions are already detailed in the literature (Zhang & Li, 2019; Li & Zhang, 2019) for topologies that are based on the half-bridge converter. Such equivalent models that do not contain detailed switches are advantageous since their logic is more similar to a simple look-up table and thus, it is no longer required to recalculate the matrices of every possible switching state at every time step. As a result, it becomes possible to decrease the time step to acceptable levels while maintaining good accuracy. Hence, true real-time simulation of a MLC could be achieved by developing an appropriate equivalent model of the MLC that is being studied.

1.5 Conclusion

Fast electric vehicle battery chargers are becoming an increasingly popular commodity. As the demand grows and the number of charging stations increases with it, maintaining acceptable power quality on the grid will become a greater challenge, especially for bidirectional chargers. The more popular AC-DC converters used in the present for fast DC battery chargers are attractive due to their simplicity in both their configurations and control. However, they typically only generate up to three output voltage levels and thus require considerably large and costly filtering inductances to smooth out the input AC current and maintain acceptable THD levels. In

comparison, multilevel converters have more complex topologies, but they offer higher power density and improved power quality thanks to their high number of output voltage levels. Finally, the complexity of MLCs highlights the usefulness of real-time simulation when it comes to studying and validating large systems that would be composed of multiple MLC-based battery chargers. Hence, by developing robust and accurate equivalent models of MLCs, it becomes possible to perform large system studies of bidirectional battery chargers by using real-time simulators.

CHAPTER 2

23-LEVEL SINGLE DC SOURCE HYBRID PUC (H-PUC) CONVERTER TOPOLOGY WITH REDUCED NUMBER OF COMPONENTS: REAL-TIME IMPLEMENTATION WITH MODEL PREDICTIVE CONTROL

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Abstract

In this paper, a new configuration of single DC source hybrid packed U-cell (H-PUC) converter with reduced number of components is proposed. The proposed H-PUC only requires one dc source, twelve power switches, and three capacitors to provide 23-level output voltage. It is comprised of two high voltage low frequency (LF) and low voltage high frequency (HF) sub-modules which leads to less power losses and higher efficiency of the proposed H-PUC converter. Moreover, a finite control set model predictive control (FCS-MPC) method is proposed to generate 23-level staircase output voltage with low THD and to regulate voltages of three capacitors to their desired values simultaneously. A real-time model of the proposed 23-level H-PUC converter and its suggested FCS-MPC are developed and implemented in OPAL-RT OP4510 platform to evaluate and validate the feasibility of the proposed H-PUC in grid-connected operation mode. The provided real-time implementation results verify and demonstrate the performance and viability of the proposed 23-level H-PUC and its associated FCS-MPC to provide low THD 23-level output voltage and all three capacitors voltages balancing.

2.1 Introduction

The global adoption rate of renewable energy sources has been increasing significantly in the past years and shows no sign of slowing down. More specifically, solar energy is becoming increasingly popular in many parts of the world. As such, proper power electronic devices need to be developed in order to meet the appropriate grid power quality requirements (Carrasco *et al.*, 2006). Indeed, the main requirement for a photovoltaic system is a suitable voltage source inverter (VSI), which converts the DC voltage generated by the photovoltaic arrays to AC voltage that can be injected to the grid (Akbari, Poloei & Bakhshai, 2019).

Furthermore, the injected current to the grid must meet requirements compelled by stringent standards in terms of harmonic content reduction, identified as total harmonic distortion (THD). One method of reducing this harmonic pollution on the grid is to use passive, active or hybrid filters as interfacing components connected between the inverter circuit and the grid at the point of common coupling (PCC) (Javadi *et al.*, 2019).

Nonetheless, it is possible to considerably reduce the harmonic content of the injected power without the use of additional filters by using multilevel types of inverters. The latter offer a better solution than conventional inverters as they are capable of providing low THD staircase multilevel output voltage, low electromagnetic interference (EMI), low dv/dt (responsible for unintentional semiconductor turn-on), and low switching frequency. This results in overall cleaner waveforms with less harmonic distortion, which in turn reduces or even eliminates the requirement for bulky passive or hybrid filters (Rodriguez *et al.*, 2002, 2009; Abu-Rub *et al.*, 2010; Kouro *et al.*, 2010; Akagi, 2017). Some popular multilevel inverter topologies include the cascaded H-bridge (CHB), the neutral-point-clamped (NPC) and the active neutral-point-clamped (ANPC) inverters. However, these topologies are only feasible to provide lower number of output voltage levels and the number of required DC sources, power switches, diodes, and capacitors are significantly increased at higher number of output voltage levels (Zhang & Gao, 2019; Rodriguez *et al.*, 2010; Abarzadeh *et al.*, 2016; Dargahi *et al.*, 2019; Li *et al.*, 2011; Abarzadeh & Kojabadi, 2016).

A new breed of multilevel inverters, known as the packed U-Cell, is able to overcome the limitations previously mentioned. These inverters can generate a high number of voltage levels while using a smaller number of active switches and passive components (Arazm & Al-Haddad, 2020; Sharifzadeh & Al-Haddad, 2019; Babadi, Salari, Mojibian & Bina, 2018; Ounejjar *et al.*, 2011). In fact, some specific applications of the PUC converters have shown the ability to generate 7, 9 and even 15 voltage levels with a single DC source, isolated or generated by photovoltaic arrays (Sahli, Krim, Laib & Talbi, 2019; Makhamreh, Trabelsi, Kükrer & Abu-Rub, 2020; Abdelbasset *et al.*, 2019). These higher number of output voltage levels are attained by using more complex control methods that usually employ some form of sine pulse width modulation (SPWM) or space vector modulation (SVM) (Biricik & Komurcugil, 2018; Grigoletto, Schuetz, Junior, Carnielutti & Pinheiro, 2018).

Recently, hybrid multilevel inverters formed by cascade connection of two or more sub-modules are introduced in the literature. Applying asymmetrical ratio of isolated DC links to the sub-modules results in higher number of output voltage levels by employing reduced number of components in hybrid multilevel inverters (Lezana & Aceiton, 2011; Malinowski *et al.*, 2010). However, hybrid multilevel inverters require two or more isolated DC sources or high frequency links to provide multiple isolated DC links. Hence, the complexity and cost of hybrid multilevel inverters are increased (Xia & Li, 2013).

To overcome the above mentioned frailties, this paper proposes the single DC source hybrid PUC (H-PUC) inverter and its suggested FCS-MPC to provide 23-level output voltage with less number of components. The 23-level output voltage with low THD and voltage balancing of all capacitors are obtained by employing the proposed FCS-MPC in the proposed H-PUC. Hence, the proposed H-PUC only needs one isolated DC source and the high frequency link is eliminated from this configuration. This paper is organized as follows. The general topology and its mathematical model are developed and presented in Section 2.2. Then, in Section 2.3, the model predictive controller is designed for 23 output voltage levels and tested in grid-connected mode. Subsequently, in Section 2.4, the real-time equivalent model of the proposed converter is

discussed. Finally, the designed converter-controller is simulated in real-time and validated in Section 2.5.

2.2 Hybrid PUC (H-PUC) Inverter Topology

2.2.1 Presentation of the Circuit Topology

The proposed H-PUC configuration is comprised of two sub-modules that are based on the PUC topology. This PUC converter was first introduced in (Ounejjar *et al.*, 2011). It is composed of 6 active switches, one DC voltage source and one DC capacitor. This topology can be used in single-phase system configuration, operating in either inverter or rectifier modes. In single-phase inverter mode, the basic form of the converter, called PUC5, can generate five voltage output levels and has the ability to self-balance the DC capacitor voltage to one half of the main DC source without the use of voltage sensors thanks to appropriate modulation techniques (Abarzadeh, Vahedi & Al-Haddad, 2019). In addition, the same converter topology is capable of generating 7 voltage output levels (PUC7) when paired to an appropriate control technique that regulates the DC capacitor voltage to one third of the main DC source (Ounejjar *et al.*, 2012). The proposed single DC source H-PUC inverter is formed by cascade connection of two PUC5 sub-modules with quinary ratio.

In (Meraj *et al.*, 2019) and (Lodi *et al.*, 2020), multilevel converter composed of two cascaded PUC7 converters have been introduced, but they require two or more DC sources to achieve a high number of voltage output levels. Similarly in (Abarzadeh & Al-Haddad, 2019), the Q-HNPC is proposed as a modular approach to cascaded multilevel inverters based on HNPC and PUC5 converters has been presented, but again multiple DC sources are necessary for proper operation. In this paper, the proposed topology, shown in Fig. 2.1, is based on a cascade connection of two PUC5 inverters where the DC source of the second converter is replaced by a voltage regulated DC capacitor, which reduces the burden of using multiple isolated bidirectional DC sources. Additionally, as shown in Fig. 2.1, only 4 of the 12 switches operate at high switching frequency, whereas 6 switches operate at lower frequencies, and the first 2 complementary switches operate

at fundamental frequency. This results in overall higher efficiency since higher voltages like V_{dc} are switched at lower frequencies.

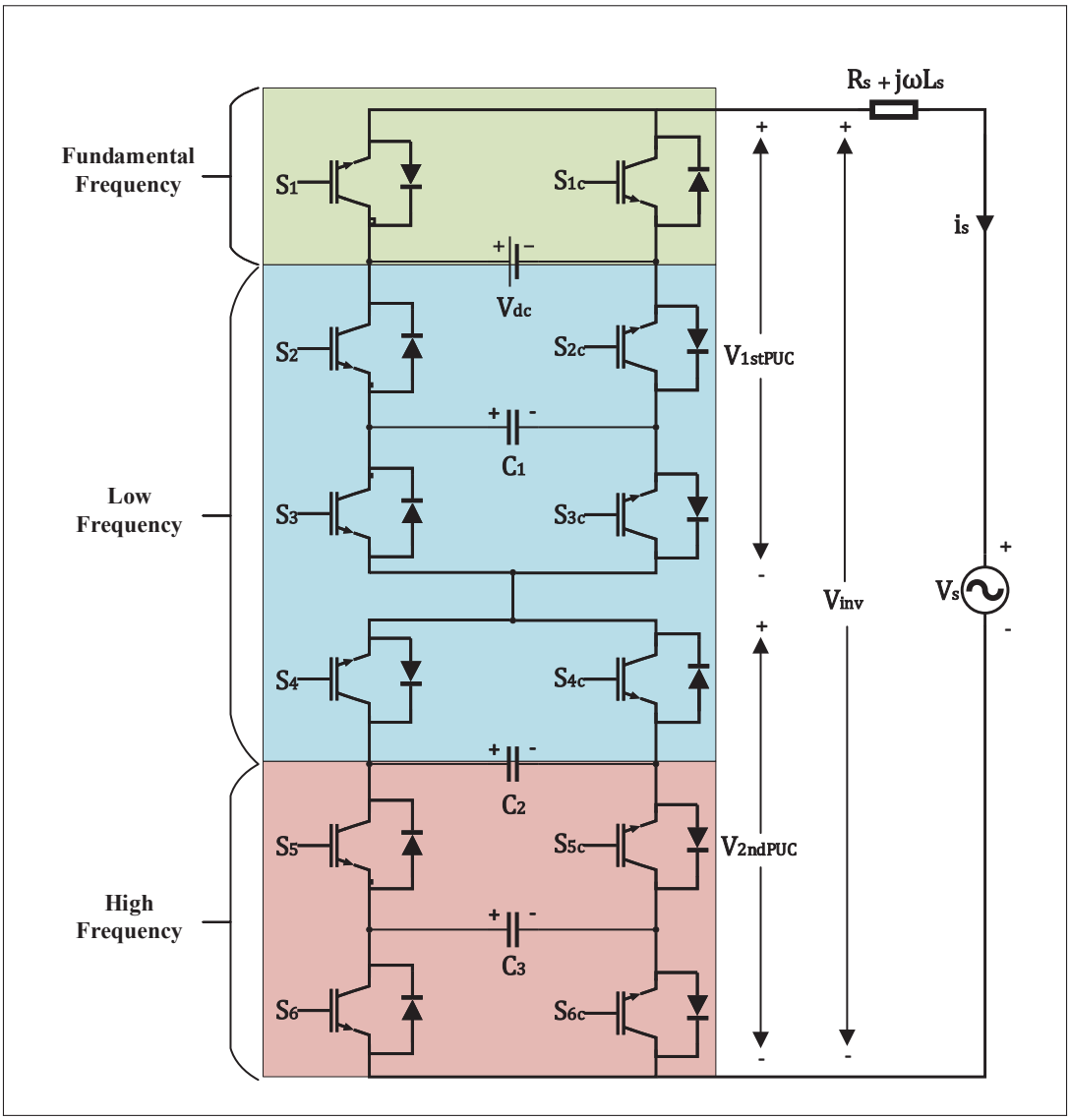

Figure 2.1 The Proposed Hybrid PUC (H-PUC) Inverter Topology with Single DC Source

The use of a model predictive controller requires prior knowledge of all possible switching states of the converter (Kouro, Cortes, Vargas, Ammann & Rodriguez, 2009; Metri, Vahedi, Kanaan & Al-Haddad, 2016; Trabelsi, Bayhan, Ghazi, Abu-Rub & Ben-Brahim, 2016). Since

the proposed converter is composed of 6 pairs of complementary switches (S_1 to S_6 and S_{1c} to S_{6c}), there are in total $2^6 = 64$ possible switching states for this topology. However, individually each of the two PUC5 converters has $2^3 = 8$ possible switching states. Thus, for the sake of conciseness, only the states of each individual PUC5s (1st PUC and 2nd PUC) are shown in Table 2.1.

Table 2.1 Possible Switching States and Capacitor Charging States of 1st and 2nd PUC

1st PUC States					
State	**S1**	**S2**	**S3**	**C1**	V_{1stPUC}
1	0	0	0	–	0
2	0	0	1	↓	$-V_{c1}$
3	0	1	0	↑	$V_{c1} - V_{dc}$
4	0	1	1	–	$-V_{dc}$
5	1	0	0	–	V_{dc}
6	1	0	1	↑	$V_{dc} - V_{c1}$
7	1	1	0	↓	V_{c1}
8	1	1	1	–	0

2nd PUC States						
State	**S4**	**S5**	**S6**	**C2**	**C3**	V_{2ndPUC}
1	0	0	0	–	–	0
2	0	0	1	–	↓	$-V_{c3}$
3	0	1	0	↓	↑	$V_{c3} - V_{c2}$
4	0	1	1	↑	–	$-V_{c2}$
5	1	0	0	↑	–	V_{c2}
6	1	0	1	↓	↑	$V_{c2} - V_{c3}$
7	1	1	0	–	↓	V_{c3}
8	1	1	1	–	–	0

The overall 64 switching states can then be obtained by listing every combination of the two individual converters' states. The following definitions should be observed:

$$S_i = \bar{S}_{ic} = \begin{cases} 1 & \text{if} \quad S_i \text{ is ON} \\ 0 & \text{if} \quad S_i \text{ is OFF} \end{cases} \qquad i = 1, 2, 3, 4, 5, 6 \tag{2.1}$$

where S_i ans S_{ic} are pairs of complementary switches that are never ON simultaneously in order to avoid short-circuiting the DC source.

2.2.2 Determination of Capacitor Values

The selection of capacitor values is influenced by their peak current, their charging and discharging period, and their voltage ripple as expressed in the following equation:

$$C_i = \frac{I_{peak} \times \Delta t_{ci}}{V_{ripple}}, \qquad i = 1, 2, 3 \tag{2.2}$$

where I_{peak} is load current peak value, V_{ripple} is desired capacitor voltage ripple and Δt_{ci} is the duration of charge and discharge of i-th capacitor. The values of I_{peak} and V_{ripple} are imposed by the user, but they still depend on Δt_{ci}. Thus, in Fig. 2.2 the charging and discharging currents of all three capacitors C_1, C_2 and C_3 are depicted over two fundamental cycles.

It is observed that the charging and discharging periods of C_1 and C_3 are balanced with about sampling frequency (f_s), whereas the charging and discharging period of C_2 is balanced with about 5 times of fundamental frequency ($5\times f_0$). In other words, the currents in C_1 and C_3 complete their charging and discharging cycles (balancing) a lot faster than C_2. As such, the values of Δt_c of C_1 and C_3 are much smaller than that of C_2 and consequently, considering (2.2), the selected values of C_1 and C_3 can be considerably smaller than the value of C_2. With this knowledge, and by considering a peak current of 10A as seen in Fig. 2.2 and voltage ripple of 5V, one can find approximate ranges for the optimal capacitor values. Since the MPC method does not use a fixed switching frequency, the precise value of Δt_{ci} is unknown. So, based on the previous discussion and some iterative tests, some capacitor values are selected in an effort minimize their sizes. More specifically, the capacitor values utilized in this work are $C_1 = 500\mu F, C_2 = 1500\mu F$ and $C_3 = 500\mu F$.

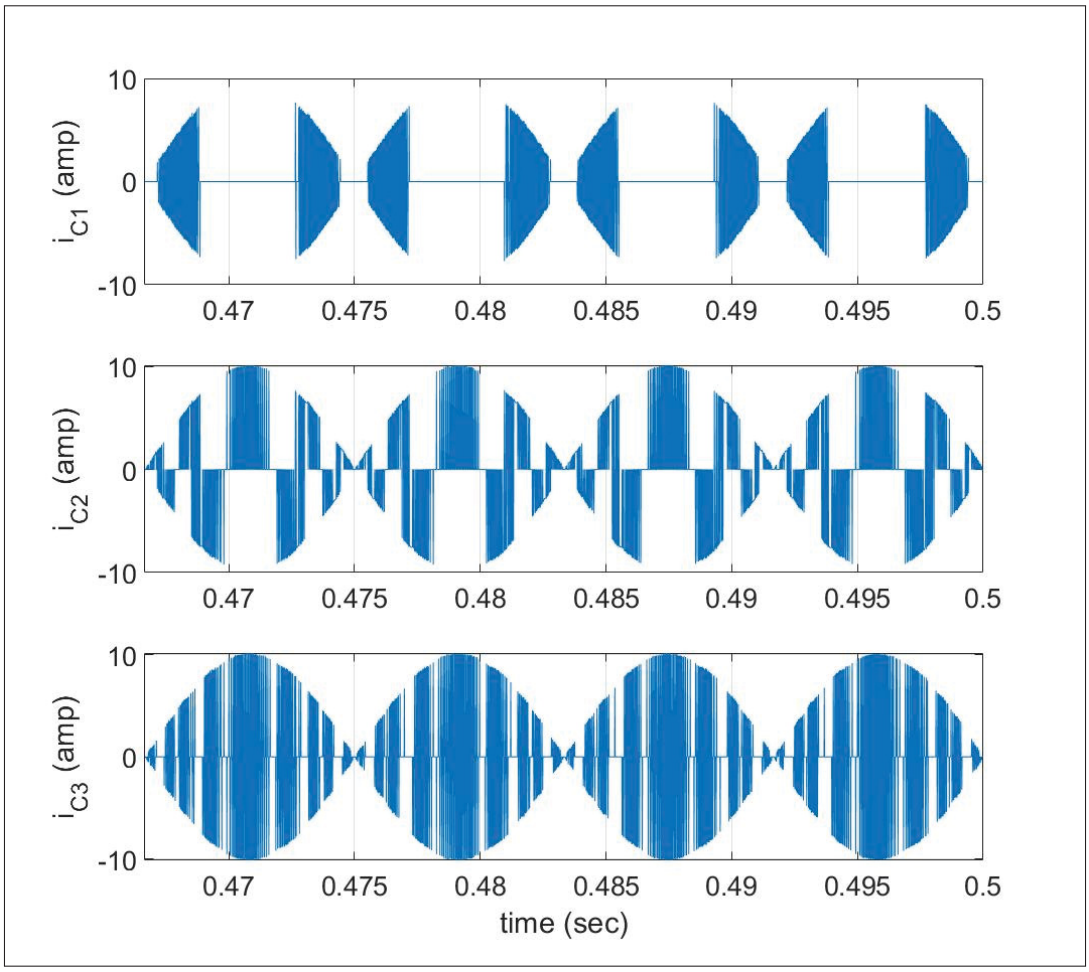

Figure 2.2 Charging and discharging currents of all three capacitors of the H-PUC converter during two fundamental cycles

2.2.3 Comparison of the H-PUC with Other MLI topologies

The proposed 23-level H-PUC converter is compared to other MLI converters in Table 2.2. The table lists the number of DC sources, capacitors, diodes, high frequency (HF) switches and low frequency (LF) switches for the CHB, Q-HNPC, PUC, ANPC and H-ANPC converters with similar numbers of voltage output levels. As such, Table 2.2 demonstrates that the proposed H-PUC is able to considerably reduce the number of HF and LF switches when compared to other topologies, even decreasing the number of LF switches by two with respect to the 25-level H-ANPC (Abarzadeh & Kojabadi, 2016) and by four with respect to the 21-level Q-HNPC

Table 2.2 Comparison of the Proposed 23L H-PUC Converter with other Presented Converters in the Literature in Terms of the Number of Components

MLI Type	**HF Switches**	**LF Switches**	**Diodes**	**Caps.**	**DC Sources**
23L-CHB	44	-	-	-	11
21L Q-HNPC	4	10	4	3	2
23L-PUC	22	2	-	10	1
23L-ANPC	22	4	-	12	1
25L H-ANPC	8	6	-	3	3
Proposed 23L-H-PUC	8	4	-	3	1

(Abarzadeh & Al-Haddad, 2019). In addition, the H-PUC requires only one DC source, three capacitors and no clamped diodes. Hence, the H-PUC inverter is capable of attaining a high number of output voltage levels with a reduced number of components.

2.3 The Proposed Finite Control Set Model Predictive Controller (FCS-MPC)

2.3.1 Mathematical Modelling of the Inverter

It is necessary to define a mathematical model of the converter in order to use a model predictive controller effectively. This is because the basis of MPC is the prediction of the future state of the converter model (Metri *et al.*, 2016). Hence, a simple and discretized converter model based on the Forward Euler approximation is developed and presented in this section.

The first equation that can be defined is the overall inverter AC output voltage in the time domain as:

$$V_{inv}(t) = V_{1stPUC}(t) + V_{2ndPUC}(t). \tag{2.3}$$

Because the objective of the model predictive controller is to select an appropriate switching state, it is more useful to express V_{inv} as a function of the individual switches' states (S_1 to S_6).

This approach was used in (Metri *et al.*, 2016) and is reproduced here. Indeed, by examining the relationships between the states of the switches S_i and the converter output voltage, which is defined by the sum of V_{1stPUC} and V_{2ndPUC}, two switching functions can then be defined:

$$V_{1stPUC}(t) = (S_1 - S_2)V_{dc}(t) + (S_2 - S_3)V_{c1}(t) \tag{2.4}$$

$$V_{2ndPUC}(t) = (S_4 - S_5)V_{c2}(t) + (S_5 - S_6)V_{c3}(t). \tag{2.5}$$

These equations can be further simplified by introducing four new switching variables constructed by combining each two consecutive switching functions, namely:

$$S_a = S_1 - S_2 \tag{2.6}$$

$$S_b = S_2 - S_3 \tag{2.7}$$

$$S_c = S_4 - S_5 \tag{2.8}$$

$$S_d = S_5 - S_6. \tag{2.9}$$

Therefore, new simplified switching states are obtained based on the newly introduced intermediate switching states, as can be shown in Table 2.3. These new switching variables are used in the MPC to generate the appropriate output voltage level of the converter.

With the new variables defined in (2.6) to (2.9), it is then possible to combine equations (2.3) to (2.9) to write the following discrete expression

$$V_{inv}(k) = S_aV_{dc}(k) + S_bV_{c1}(k) + S_cV_{c2}(k) + S_dV_{c3}(k) \tag{2.10}$$

for the inverter output voltage, where $k = 0, 1, 2, 3...$ is the discrete index chosen to denote the value of a variable at a given computation time step. One can observe that the output voltage is a combination of the switching variables that multiply each of the V_{dc} and the three capacitor voltages V_{c1}, V_{c2} and V_{c3}. Subsequently, the equations of the C_1, C_2, and C_3 capacitors currents

Table 2.3 Simplified Switching States and Capacitor Charging States of 1st and 2nd PUC for MPC

1st PUC States				
State	**Sa**	**Sb**	**C1**	V_{1stPUC}
1	0	0	–	0
2	0	-1	↓	$-V_{c1}$
3	-1	1	↑	$V_{c1} - V_{dc}$
4	-1	0	–	$-V_{dc}$
5	1	0	–	V_{dc}
6	1	-1	↑	$V_{dc} - V_{c1}$
7	0	1	↓	V_{c1}
8	0	0	–	0
2nd PUC States					
State	**Sc**	**Sd**	**C2**	**C3**	V_{2ndPUC}
1	0	0	–	–	0
2	0	-1	–	↓	$-V_{c3}$
3	-1	1	↓	↑	$V_{c3} - V_{c2}$
4	-1	0	↑	–	$-V_{c2}$
5	1	0	↑	–	V_{c2}
6	1	-1	↓	↑	$V_{c2} - V_{c3}$
7	0	1	–	↓	V_{c3}
8	0	0	–	–	0

as functions of the new switching variables along with the grid current $i_s(t)$ can be written as

$$i_1(t) = C_1 \frac{dV_{c1}(t)}{dt} = -S_b i_s(t) \tag{2.11}$$

$$i_2(t) = C_2 \frac{dV_{c2}(t)}{dt} = -S_c i_s(t) \tag{2.12}$$

$$i_3(t) = C_3 \frac{dV_{c3}(t)}{dt} = -S_d i_s(t). \tag{2.13}$$

Next, the derivative terms in equations (2.11) to (2.13) can be discretized by using the Forward Euler approximation

$$\frac{dV_{c1}(t)}{dt} = \frac{V_{c1}(k+1) - V_{c1}(k)}{T_s} \tag{2.14}$$

$$\frac{dV_{c2}(t)}{dt} = \frac{V_{c2}(k+1) - V_{c2}(k)}{T_s} \tag{2.15}$$

$$\frac{dV_{c3}(t)}{dt} = \frac{V_{c3}(k+1) - V_{c3}(k)}{T_s} \tag{2.16}$$

where T_s is the sampling time. Finally, by replacing (2.14), (2.15) and (2.16) into (2.11), (2.12) and (2.13), respectively, the equations for the predicted future values of the capacitor voltages as functions of the switching variables are obtained as:

$$V_{c1}(k+1) = V_{c1}(k) - \frac{T_s S_b}{C_1} i_s(k) \tag{2.17}$$

$$V_{c2}(k+1) = V_{c2}(k) - \frac{T_s S_c}{C_2} i_s(k) \tag{2.18}$$

$$V_{c3}(k+1) = V_{c3}(k) - \frac{T_s S_d}{C_3} i_s(k). \tag{2.19}$$

In the time domain, the inverter voltage as a function of grid current and grid voltage $V_s(t)$ is expressed as:

$$V_{inv}(t) = R_s i_s(t) + L_s \frac{di_s(t)}{dt} + V_s(t) \tag{2.20}$$

which is simply obtained by performing a Kirchoff voltage loop of the H-PUC in Fig. 2.1. The derivative term can be discretized by employing the Forward Euler approximation

$$\frac{di_s(t)}{dt} = \frac{i_s(k+1) - i_s(k)}{T_s} \tag{2.21}$$

and the equation for the predicted future value of the grid current is derived by combining (2.20) and (2.21)

$$i_s(k+1) = i_s(k) + \frac{T_s}{L_s}(V_{inv}(k) - V_s(k) - R_s i_s(k)). \tag{2.22}$$

The next step in the MPC design is to define the control objectives.

2.3.2 Control Objectives and Implementation of the MPC

The proper operation of the proposed H-PUC converter depends on the regulation of the DC capacitor voltages and on the synchronization of the injected current with the grid voltage.

Thus, there are four control objectives for the MPC: regulation of voltages V_{c1}, V_{c2}, V_{c3} and the synchronization of grid current i_s. Thus, the MPC cost function G takes the following form:

$$G(k) = k(i_s(k+1) - i_s^*)^2 + \frac{k}{5}(V_{c1}(k+1) - V_{c1}^*)^2 + \frac{k}{3}(V_{c2}(k+1) - V_{c2}^*)^2 + \frac{k}{2}(V_{c3}(k+1) - V_{c3}^*)^2 \quad (2.23)$$

where k is used as a weighted factor to decouple one objective from the other, and the variables denoted by a star (*) are the reference values. In this work, the weights attributed to the control of the three capacitor voltages are normalized with respect to the current gain k, and the specific gain ratios in (2.23) are determined by iteration to obtain satisfactory performance. Furthermore, this implementation considers only a single prediction horizon in order to reduce the number of computations per time step.

The schematic diagram of the proposed FCS-MPC method is shown in Fig. 2.3 along with a flowchart of the process in Fig. 2.4. At every time step, the MPC measures the present values of V_{dc}, V_{c1}, V_{c2}, V_{c3}, i_s and V_s and uses them to compute the predicted future values based on equations (2.10), (2.17), (2.18), (2.19) and (2.22) also at every time step. These future values are represented by the vector $X(k+1)$ in Fig. 2.3. Then, once every computation time step, the controller computes the aforementioned predicted values for all 64 possible states of the switching variables S_a, S_b, S_c, S_d and determines which one of these states results in the minimum value of the cost function G. The selected state is then used to apply the corresponding pulses to the inverter switches' gates and the process is repeated for the next time step.

2.3.3 Reference Values for 23 Output Voltage Levels

In order to achieve the desired number of output voltage level, which is 23 in this case, it is important to apply the proper voltage ratio between the source V_{dc} and the DC capacitor voltage V_{c2}. In the H-PUC converter, the following formula can be used to calculate the number of output voltage levels

$$N = M_1 \times M_2 - 2 \quad (2.24)$$

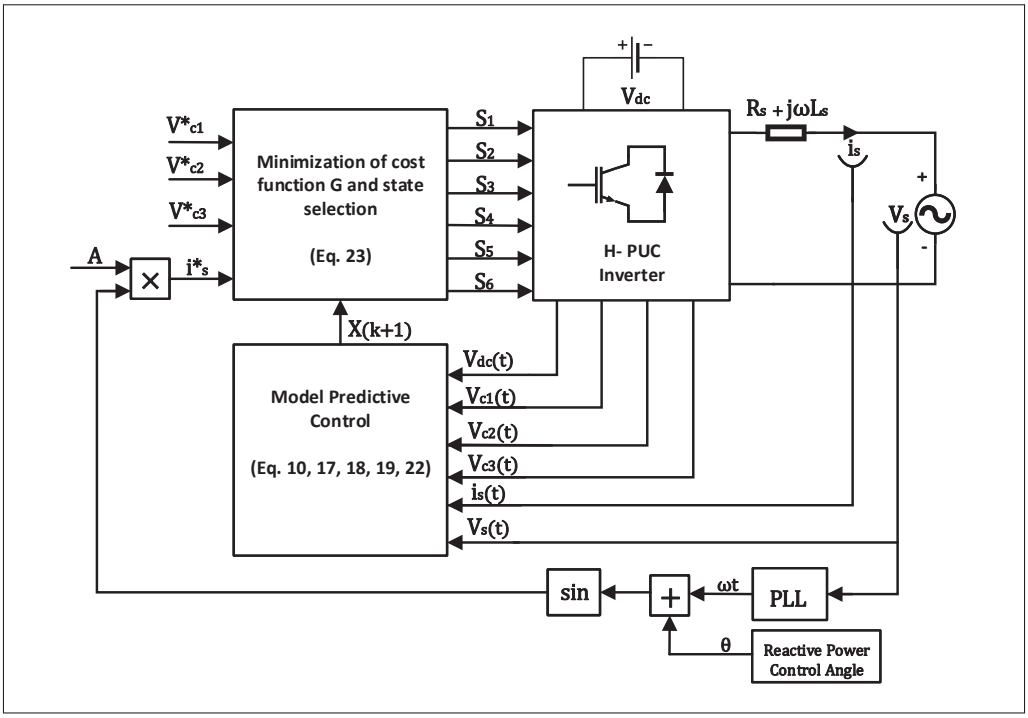

Figure 2.3 The Schematic Diagram of the Proposed FCS-MPC for the H-PUC Inverter

where N is the number of output voltage levels, M_1 and M_2 are the number of output voltage levels of the first PUC and second PUC respectively, and the subtraction by 2 is for providing enough redundant switching states for voltage balancing of all capacitors. Then, the voltage ratio $\frac{V_{dc}}{V_{c2}}$ should be equal to the number of voltage output levels of the second PUC. In this case, because both converters are 5-level PUC5's, the ratio is $M_2 = 5$ or:

$$V_{c2}^{*} = \frac{V_{dc}}{5}. \tag{2.25}$$

In (2.25), V_{dc} is the input DC source voltage. Furthermore, because each of the two converters are operated as 5-level PUC5 inverters, the auxiliary DC capacitors should be regulated at half the value of the main DC voltage:

$$V_{c1}^{*} = \frac{V_{dc}}{2} \tag{2.26}$$

$$V_{c3}^{*} = \frac{V_{c2}^{*}}{2} = \frac{V_{dc}}{10}. \tag{2.27}$$

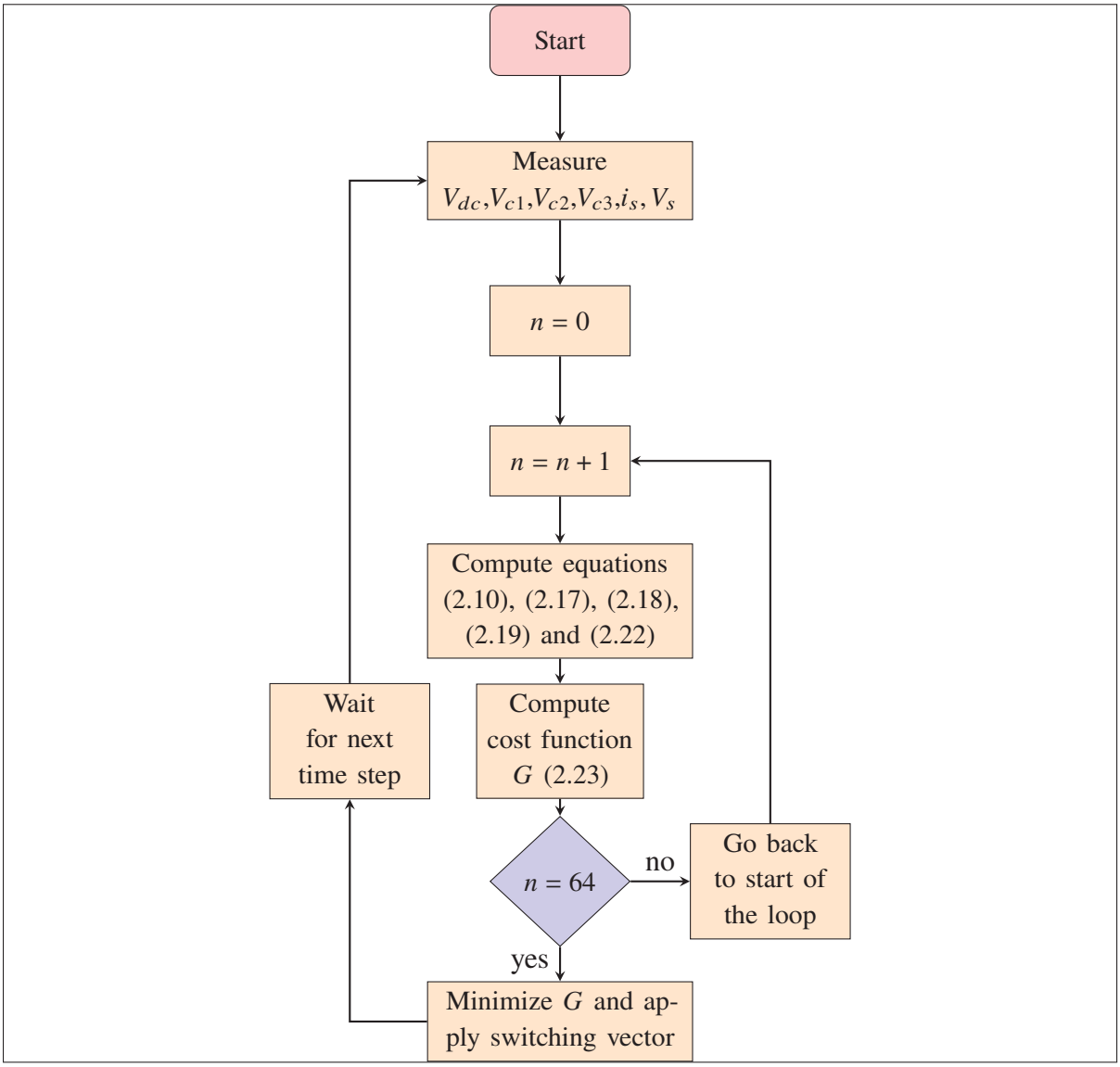

Figure 2.4 Flowchart of the Proposed FCS-MPC Process

Moreover, as seen in Fig. 2.3, the sinusoidal current reference is obtained by measuring the grid voltage angle and generating a synchronized sine wave

$$i_s^* = A \times sin(\omega t) \tag{2.28}$$

where A is the amplitude of the reference injected current to the grid and ωt is the measured grid voltage angle.

2.4 Converter Modeling for Real-Time Simulation on the OPAL-RT Platform

2.4.1 Software-in-the-Loop Simulation

In a typical production process, the steps generally consist of some initial research, mathematical modeling, offline simulations and then hardware prototyping. Real-time simulation (RTS) is to be used as an intermediate step before any real hardware is developed. Indeed, real-time simulations offer the possibility of connecting the simulated system to a larger digital plant (e.g. distribution grid). This better flexibility is due to the fact that in RTS, one second of simulation represents one second of the real life system running. In other words, the simulation runs at the same rate as the real system would. This feature also allows for hardware-in-the-loop (HIL) simulations in which hardware components such as controllers can be introduced in the simulation loop. This helps in further reducing the complexity and cost of the production process (Javadi *et al.*, 2019; Yamane *et al.*, 2019; Bouzid *et al.*, 2016).

Specifically, the type of real-time simulation employed in this work is called software-in-the-loop (SIL) simulation. It gets this name because there is no hardware controller or plant involved in the process, like there would be for HIL. Nonetheless, SIL still results in more true to life behaviour of the simulated system. A schematic of the SIL process is illustrated in Fig. 2.5. In the case of this paper, both the model predictive controller and the inverter are modeled in Matlab/Simulink, compiled on the RT-LAB software and then simulated in real-time on an OP4510 CPU.

2.4.2 Real-Time Model of the H-PUC Inverter

The large number of active switches in the proposed inverter makes it difficult to perform CPU-based real-time simulation with a low enough computation time step. A low time step is necessary because the performance of the MPC increases when the time step decreases. For this reason, an equivalent inverter model where the first and second PUC converters are replaced by a controlled voltage source is developed (Meng *et al.*, 2020). The diagram in Fig. 2.6 shows the

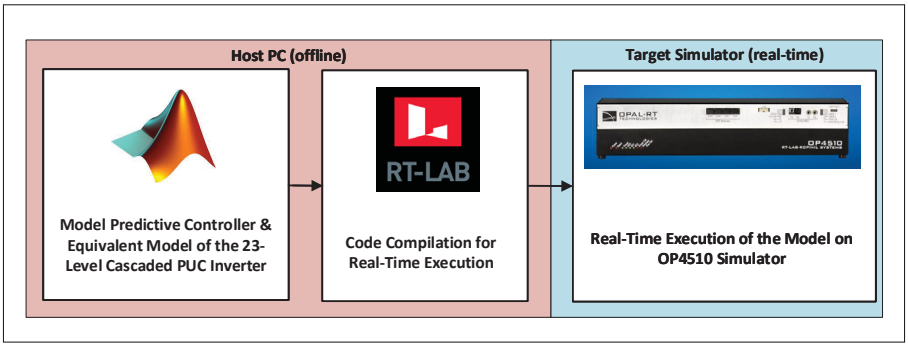

Figure 2.5 Schematic of the Simulation Process with OP4510

aforementioned equivalent converter model.

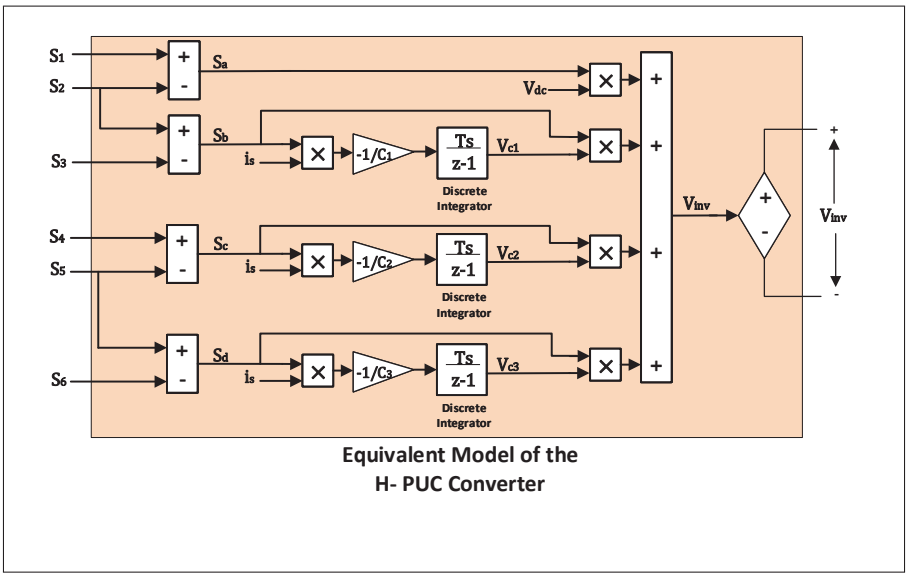

Figure 2.6 Diagram of the Equivalent H-PUC Model

By using the switching vector (S_1 to S_6), the current measurement i_s and the value of the DC source V_{dc} as inputs, the inverter output voltage V_{inv} can be accurately reproduced thanks to equations (2.10), (2.11), (2.12) and (2.13). The rest of the circuit, namely the AC voltage source V_s and the line impedance $R_s + j\omega L_s$ depicted in Fig. 2.1, are modeled using SimPowerSystems (SPS) components. Finally, the model predictive controller is constructed with a Matlab Function block that stores the vectors of S_a to S_d and S_1 to S_6, and computes equations (2.10), (2.17),

(2.18) (2.19), (2.22) and (2.23) and applies the selected switching vector to the equivalent converter model as shown in Fig. 2.6.

2.4.3 Validation of the Equivalent Real-Time Model of the H-PUC Inverter

The equivalent voltage source model of the H-PUC inverter presented in the previous subsection is validated through offline simulations in Simulink. The circuit presented in Fig. 2.1 is constructed in two versions: one using IGBT power switches and capacitors from the SPS library and another one using the voltage source equivalent model. The simulation parameters for both versions are the same and are outlined in Table 2.4. In order to validate the accuracy of the proposed equivalent model, the waveforms of the simulation measurements of both circuit versions are superimposed in the subsequent Fig. 2.7, Fig. 2.8 and Fig. 2.9.

Firstly, the system transient response is simulated. The results for the output voltage V_{inv} and the grid current i_s are shown in Fig. 2.7 while the three capacitor voltages V_{c1}, V_{c2}, V_{c3} are illustrated in Fig. 2.8.

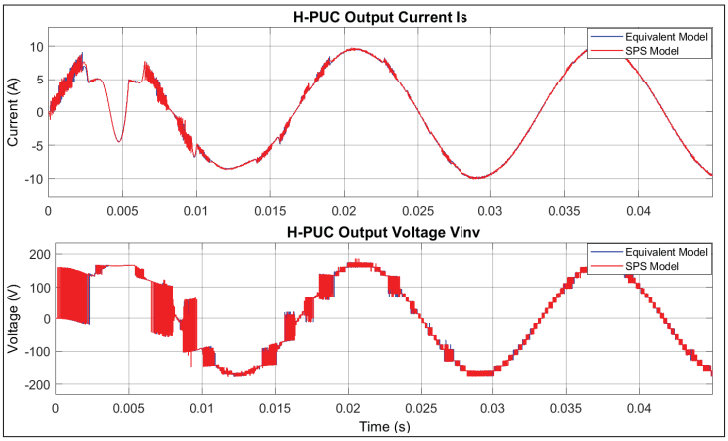

Figure 2.7 Output voltage and grid current transient response: comparison of SPS and equivalent model

It can be observed from Fig. 2.7 and Fig. 2.8 that the equivalent model of the converter is able to closely match the behaviour of the circuit made from SPS power switches. Secondly, a closer inspection of the capacitor voltages in steady-sate is performed as displayed in Fig. 2.9.

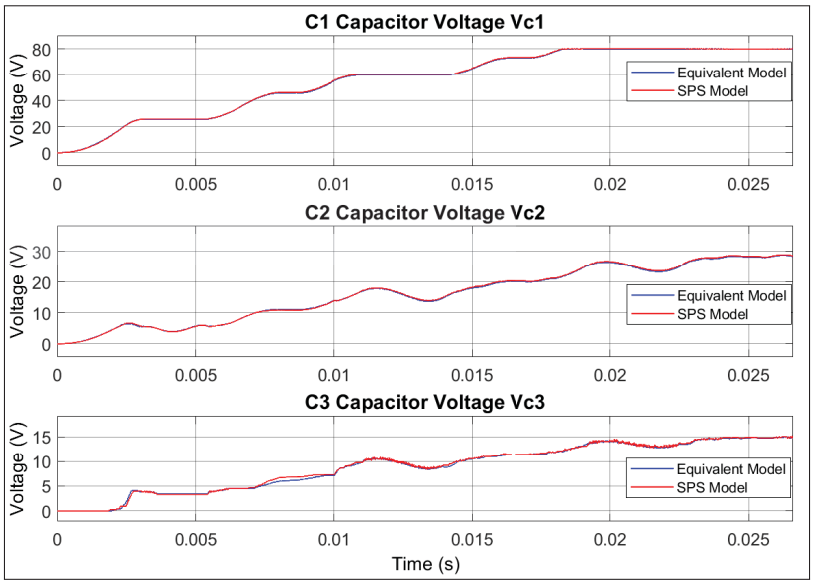

Figure 2.8 Capacitor voltages transient response: comparison of SPS and equivalent model

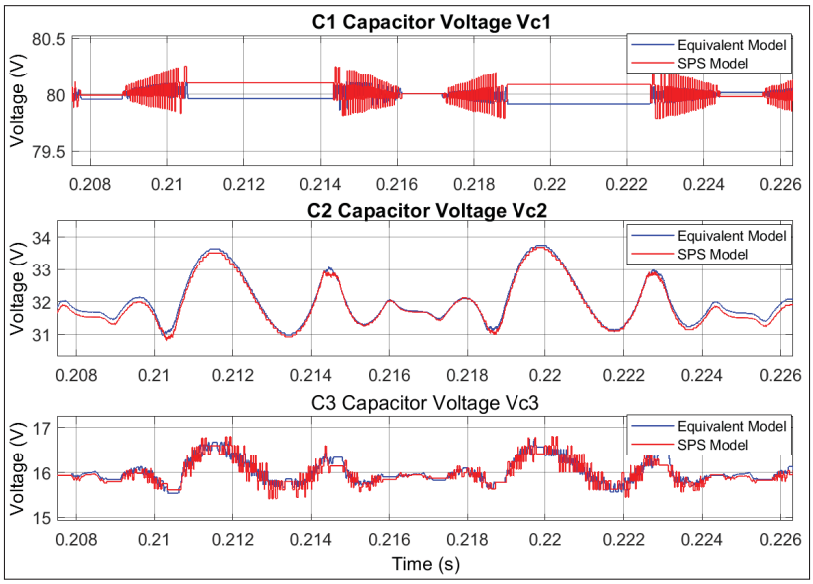

Figure 2.9 Capacitor voltages ripple: comparison of SPS and equivalent model

These measurements demonstrate that even the small voltage ripples of the DC capacitors are well reproduced by the equivalent model. Indeed, it is observed that the overall voltage waveforms are nearly identical between the two models. Plus, the absolute errors between the

voltage values are very minimal with only about 0.25V of error in the V_{c1} waveforms. This represents only a 0.31% discrepancy with respect to the nominal 80V. Hence, the equivalent H-PUC model is used to obtain real-time simulation results in the next section.

2.5 Real-Time Simulation Results

The proposed 23-level grid-connected H-PUC inverter and associated model predictive controller have been implemented in OPAL-RT OP4510 real-time simulator and the RT-LAB real-time simulation software, which is based on the Matlab/Simulink platform. In addition to steady-state and transient results, a step change in the current amplitude reference is applied to demonstrate the dynamic performance of the system in tracking the reference injected current to the grid. Reactive power and voltage sag tests are also performed to further demonstrate the converter and controller performance. The parameters used for the simulation are listed in Table 2.4.

Table 2.4 Simulation Parameters

Parameter	**Value**
Grid Frequency	$f = 60Hz$
DC Source Voltage	$V_{dc} = 160V$
First DC Capacitor	$C_1 = 500\mu F$
Second DC Capacitor	$C_2 = 1500\mu F$
Third DC Capacitor	$C_3 = 500\mu F$
Grid Link Inductance	$L_s = 500\mu H$
Grid Link Resistance	$R_s = 0.1\Omega$
Grid Voltage	$V_s = 120Vrms$
Cost Function Gain	$k = 10$
Real-Time Simulation Time Step	$T_s = 10\mu s$

With the chosen 160V DC source voltage, the DC capacitor voltages should be regulated at $V_{c1}^* = 80V, V_{c2}^* = 32V$ and $V_{c3}^* = 16V$ according to (2.25) to (2.27).

The steady-state waveforms for the inverter output voltage V_{inv}, the first and second PUC output voltages V_{1stPUC}, V_{2ndPUC} and the grid current i_s are depicted in Fig. 2.10 for a current reference of 10A.

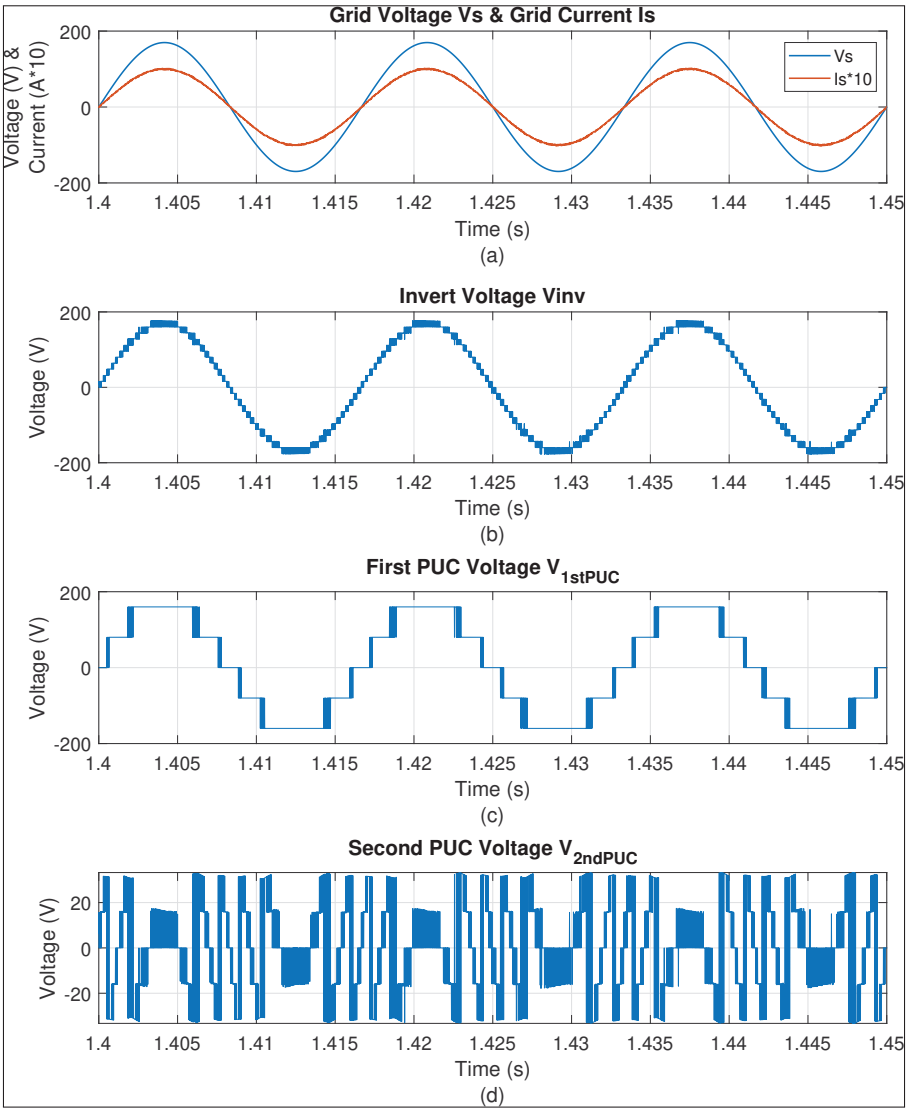

Figure 2.10 Real-time simulation results of the proposed H-PUC converter. (a) Grid voltage and current. (b) The output voltage of the proposed 23-level H-PUC inverter (c) The first PUC sub-module output voltage. (d) The second PUC sub-module output voltage

The 23 output voltage levels are easily identified in the V_{inv} waveform. Furthermore, the behaviours of the two PUCs can be observed individually. In fact, the first PUC operates as a high voltage, low frequency five-level converter with high efficiency, whereas the second PUC operates at higher switching frequency and lower DC voltages to generate extra minor voltage levels between provided major voltage levels of the first PUC sub-module that are needed to

achieve the required overall 23 voltage levels. In addition, the injected current to the grid is almost sinusoidal, which implies that its harmonic content is minimal. Another interesting feature of this topology is that the high frequency switches withstand much lower DC bus voltage while conducting the same load current, which leads to less power loss in the power switches and higher overall efficiency of the proposed H-PUC inverter.

The transient response of the three DC capacitors is also measured. In Fig. 2.11, the capacitor voltage waveforms form startup until they reach steady-state are displayed. The measurements confirm the accuracy of the controller and they also show the quick transient period of the capacitor voltages. Indeed, all three voltages reach steady-state in under 0.06s.

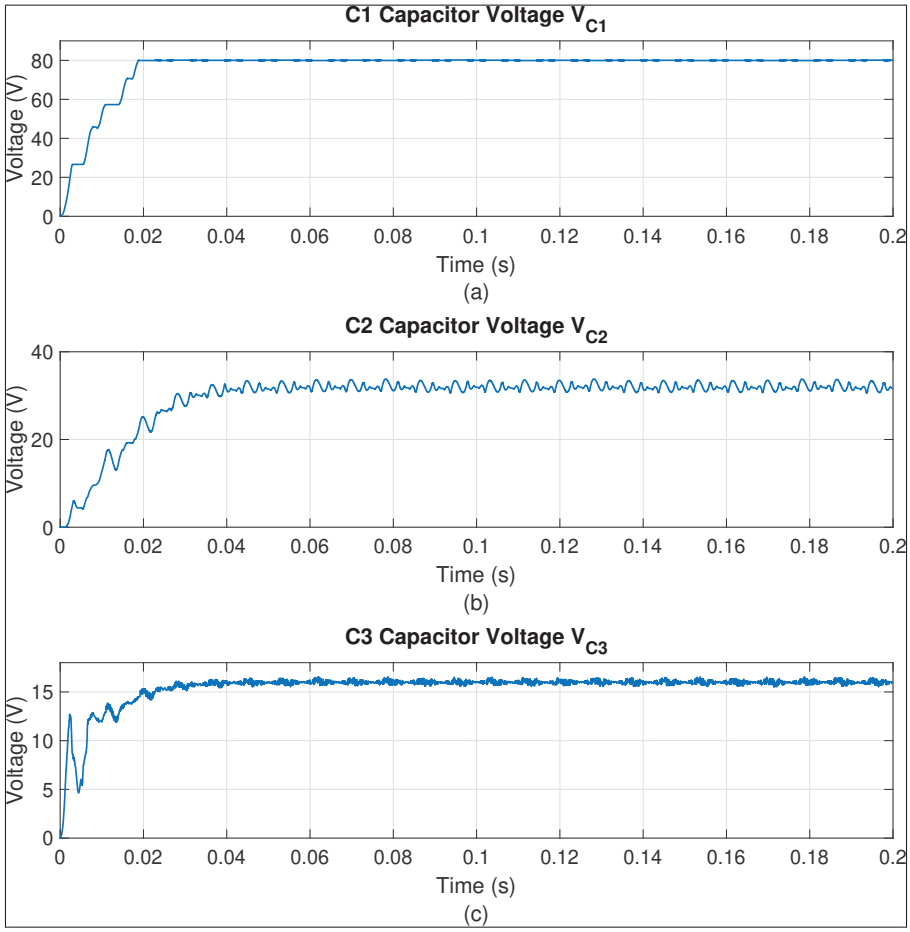

Figure 2.11 Transient response of (a) C1 capacitor voltage. (b) C2 capacitor voltage. (c) C3 capacitor voltage

The six gating signals S_1 to S_6 are also measured over one fundamental 60Hz cycle once the system has reached steady-state. The results confirm the behaviour seen in Fig. 2.10. Indeed, Fig. 2.12 indicates that the first PUC's switches operate at a much lower frequency than the second one, with S_1 switching at fundamental frequency. This behaviour results in overall lower switching losses since the higher DC voltages of the first PUC are switched at low frequencies and only the smaller DC voltages of the second PUC converter are switched at high frequencies.

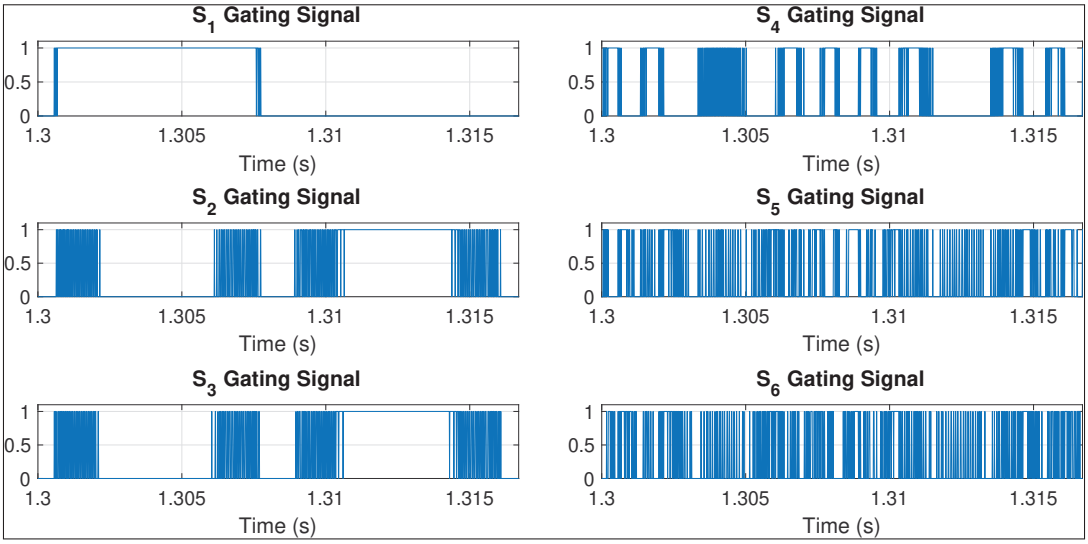

Figure 2.12 Gating Signals for Switches S1 to S6 Over a Steady-State 60Hz Cycle

The dynamic performance of the inverter is evaluated by applying a current amplitude reference change from 5A to 10A and thereafter back to 5A. Fig. 2.13 shows the response of the three capacitor voltages, the inverter voltage and the grid current during the transients.

The results demonstrate that the inverter voltage and DC voltages show little to no disturbance in response to the step change in current amplitude. The system is able to maintain constant voltage operation.

The converter's capacity to inject reactive power into the grid is also tested. This is done by adding an offset angle to the one measured by the PLL in Fig. 2.3. Indeed, the results in

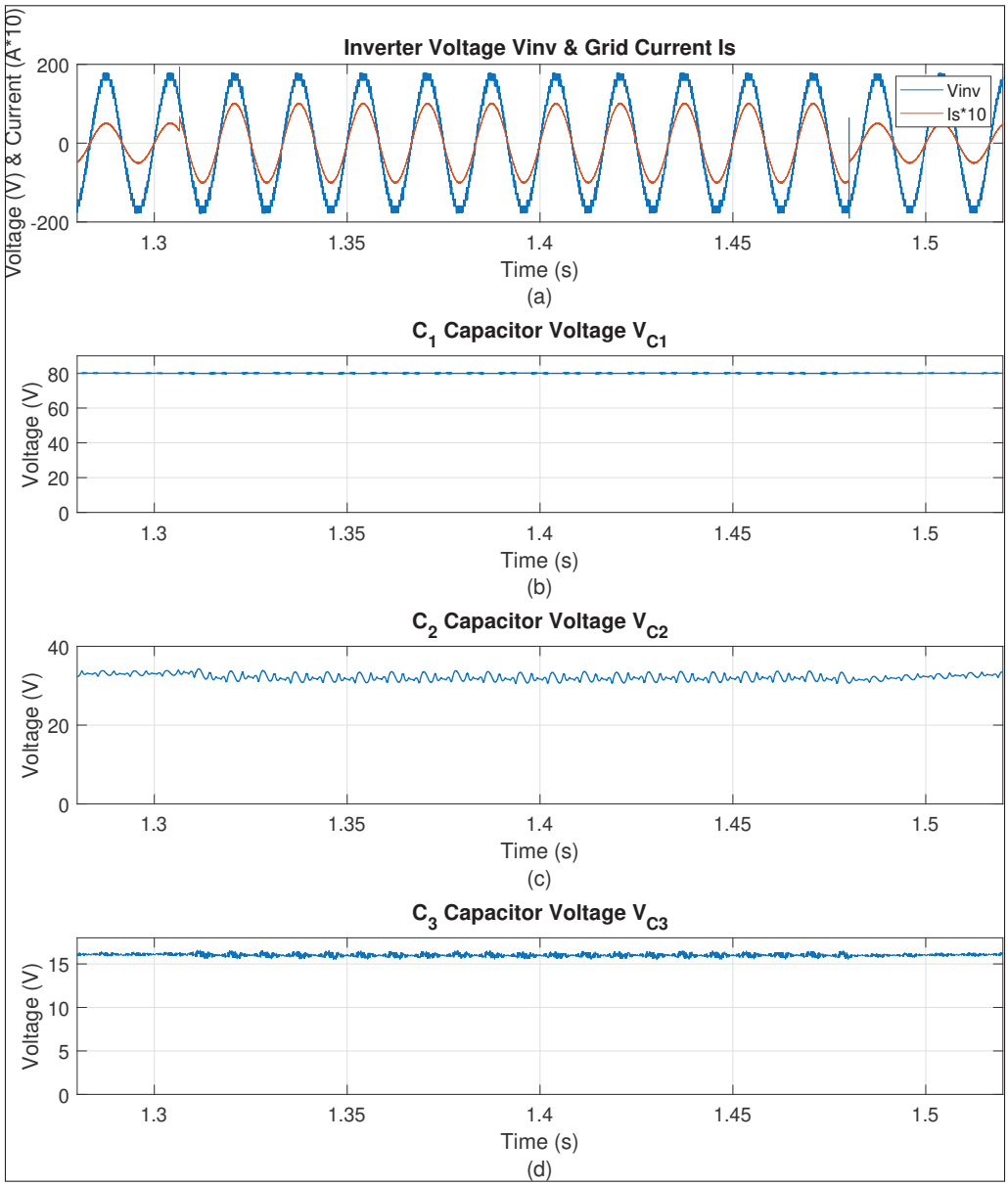

Figure 2.13 Response for the (a) inverter voltage and grid current, (b) C1 voltage, (c) C2 voltage and (d) C3 voltage during a step current change

Fig. 2.14 are obtained when the angle of the reference current is shifted by 30°at 1.34s, and subsequently brought back to zero at 1.51s.

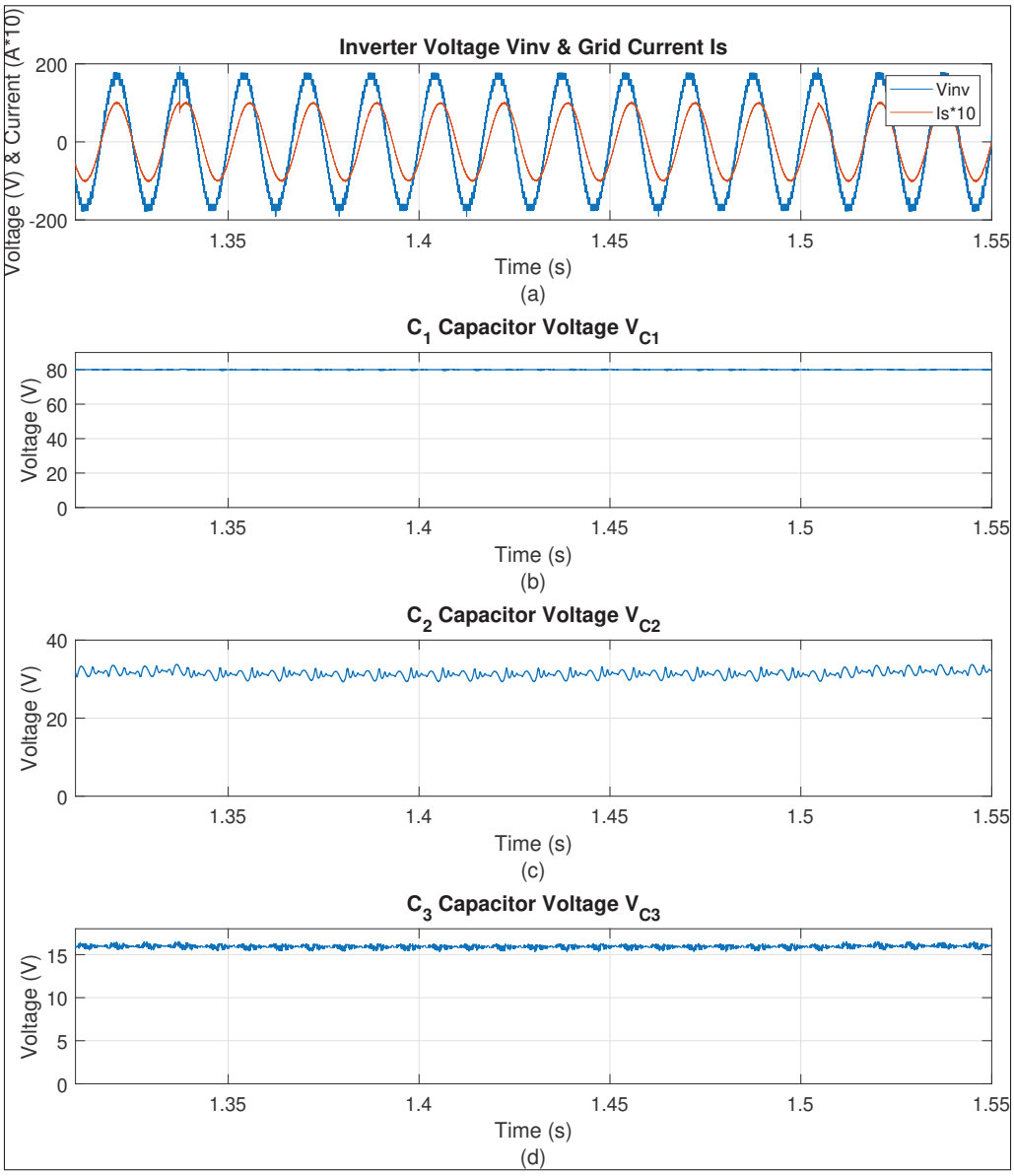

Figure 2.14 Response for the (a) inverter voltage and grid current, (b) C1 voltage, (c) C2 voltage and (d) C3 voltage during a current phase change

The measurements show that the controlled variables respond well to the change in current angle. In fact, the only noticeable disturbance is in V_{c2}, which seems to decrease slightly below its target value. Nonetheless, the other DC capacitor voltages show almost no disturbance.

A voltage sag test is also done to illustrate the parameter sensitivity of the converter and controller. A simulation is run in which the grid voltage V_s amplitude is decreased by 10% at 1.42s and then increased back to nominal value at 1.64s. The results of this test are seen in Fig. 2.15.

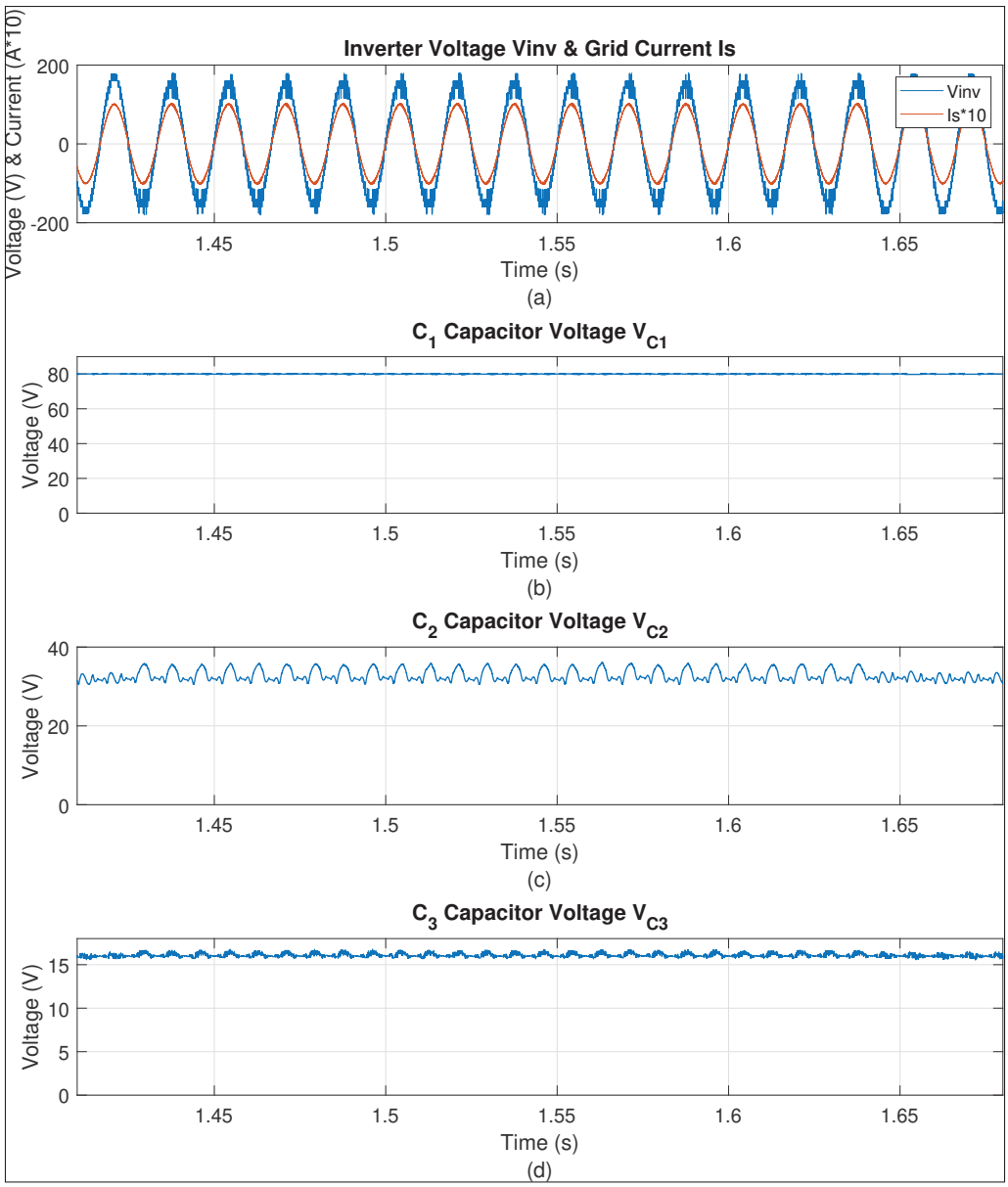

Figure 2.15 Response for the (a) inverter voltage and grid current, (b) C1 voltage, (c) C2 voltage and (d) C3 voltage during a voltage sag test

During the voltage sag, the DC capacitor voltages remain around their reference values, but they also start oscillating considerably and this is visible in the V_{inv} waveform. Despite this, the grid current is able to maintain a smooth sinusoidal shape.

Finally, the harmonic spectra and THD values for the inverter voltage and grid current are shown in Fig. 2.16 and Fig. 2.17 for a current reference of 10A. Here, the analysis is done for a spectrum of up to 25kHz despite the $10\mu s$ time step which suggests a spectrum of 100kHz. In this case, 25kHz is deemed sufficient because the MPC method does not operate at fixed PWM frequency and thus, there are no major switching clusters that contribute much THD at higher frequencies.

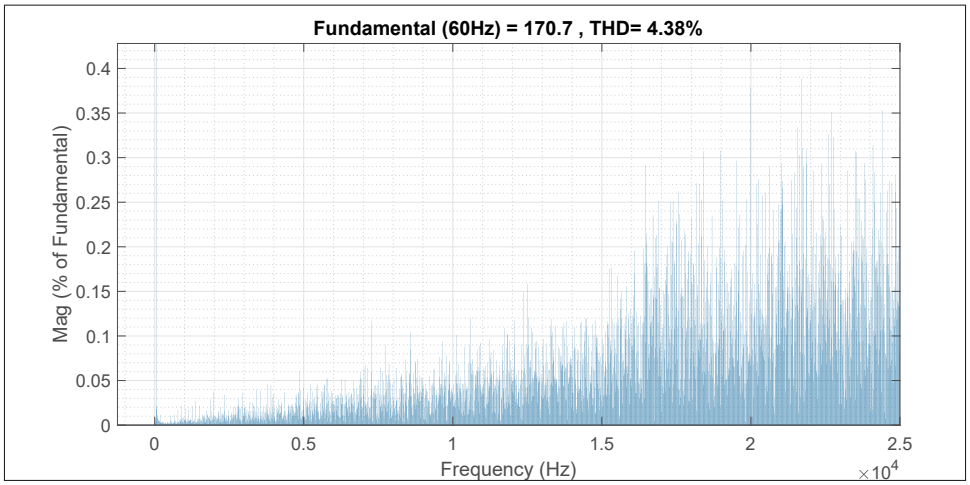

Figure 2.16 Inverter Voltage (Vinv) FFT Analysis

The analyses show a THD of 4.38% for the inverter output voltage and a harmonic spectrum that seems relatively spread out. As for the current, the THD is only 1.35% with the highest individual harmonic being the third order at 0.29% of the fundamental. This low current THD value is achieved despite the low value of the grid inductance ($500\mu H$) thanks to the high number of output voltage levels.

Furthermore, to evaluate the conduction and switching losses of the proposed H-PUC converter, the conduction and switching loss models of C3M0120090D MOSFET has been developed in

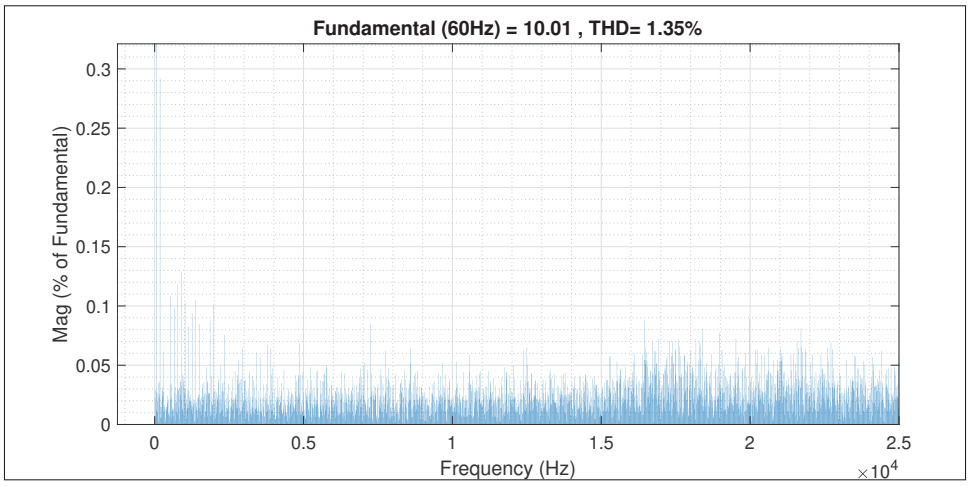

Figure 2.17 Grid Current (Is) FFT Analysis

MATLAB/Simulink platform. Then, based on the switch loss model, the power loss model of the proposed H-PUC converter has been developed and the efficiency of the proposed H-PUC converter has been evaluated. The total efficiency of the proposed H-PUC converter operating at 120VAC, 850W, and sampling time of $10\mu s$ is calculated as 93.56%.

Thus, the real-time simulation results demonstrated in this section confirm the effectiveness of the proposed model predictive controller in generating the desired number of output voltage levels in a cascaded PUC converter with a single DC source. The MPC also simplifies the controller design process since it does not require the use of a modulation technique. Moreover, the controller is capable of accurately tracking the reference DC capacitor voltages and grid current references even during step changes in current. Meanwhile, these results are obtained with minimized switching losses due to the hybrid inverter configuration in which higher DC voltages are switched at lower, close to fundamental frequencies.

2.6 Conclusion

The single DC source 23-level H-PUC inverter with reduced number of components and its associated FCS-MPC were proposed in this paper. It is comprised of only one DC source, twelve power switches, and three capacitors to provide 23-level output voltage. The proposed H-PUC

inverter is formed by cascade connection of two high voltage low frequency and low voltage high frequency PUC5 sub-modules which leads to less power losses and higher efficiency of the proposed H-PUC converter. The DC source of the second PUC5 sub-module was replaced by capacitor, then the single dc source hybrid multilevel inverter was achieved. Moreover, the proposed FCS-MPC method was applied to the H-PUC inverter to generate 23-level staircase output voltage with low THD and to regulate voltages of three capacitors to their desired values simultaneously. The real-time model of the proposed grid-connected H-PUC inverter and its associated FCS-MPC were implemented in OPAL-RT OP4510 real-time simulator. The provided real-time implementation results verified the feasibility and viability as well as steady-state and dynamic performance of the proposed grid-connected H-PUC inverter and its suggested FCS-MPC.

Acknowledgement

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CHAPTER 3

THE PARALLELED MODULAR ANPC CONVERTER AS A BIDIRECTIONAL BATTERY CHARGER WITH DEADBEAT PREDICTIVE CONTROL

3.1 Introduction

The automotive market is seeing a steady increase in the adoption rate of electric vehicles. Consequently, EV charger technologies are evolving rapidly in order to keep up with the increasing demand in charging speed and battery capacities. This means of course that manufacturers are trying to improve the charging rates of EV batteries by pushing for higher power fast DC chargers (Tu, Feng, Srdic & Lukic, 2019; Burnham *et al.*, 2017). Besides, the high number of batteries on the roads is an interesting prospect for electrical grid operators, as these represent a good potential for additional energy storage on the distribution grid. As a result, lots of research is being conducted regarding high power density AC-DC converters that have bidirectional power flow capabilities (Khaligh & Antonio, 2019; Restrepo *et al.*, 2018; He & Khaligh, 2017). Such converters would not only allow for battery chargers that benefit the EV owners with shorter battery charging times, but would also offer the ability to send power back to the grid when it is not needed by the users.

Other than offering high power density and bidirectional power flow, the power converters used in EV chargers should also ensure proper power quality and low harmonic distortion levels once they are connected to the grid. One increasingly popular method of achieving this good power quality is to employ multilevel converters that are capable of generating a high number of output voltage levels. When compared to traditional 2 or 3-level converters, MLCs output a voltage that is naturally more sinusoidal and thus requires much less filtering in terms of passive or active filters in order to achieve acceptable power quality. Some examples of such MLCs are the cascaded H-bridge, the neutral-point-clamped and the packed U-cell converters (Zhang & Gao, 2019; Rodriguez *et al.*, 2010; Abarzadeh *et al.*, 2016; Ounejjar *et al.*, 2011; Arazm & Al-Haddad, 2020).

The previous chapter provides an example of how these MLCs can help achieve low levels of harmonic distortion without requiring large and expensive passive or active filters between the grid and the converter. In fact, the 23-level H-PUC converter displays good dynamic performance and power quality. Nonetheless, it still lacks one important feature that is desirable for a bidirectional battery charger. Namely, most commercial fast DC chargers (Level 3) are based on three-phase converters (Yilmaz & Krein, 2013) as opposed to the single-phase H-PUC. Moreover, while expanding the H-PUC converter to a three-phase topology is certainly possible, this would require the use of three separate DC links: one per phase. Such an implementation is not ideal for battery chargers since it is preferable to have a single DC link that transfers maximum power to and from the battery.

Therefore, this chapter focuses on developing a control method for a bidirectional battery charger based on the three-phase MLC proposed by the authors of (Abarzadeh, Khan, Weise, Al-Haddad & Refaie, 2020). Indeed, in their paper, these authors develop and experimentally validate the paralleled modular active-neutral-point-clamped (PM-ANPC) converter that achieves 13 line-to-line output voltage levels. More specifically, they show how this converter can be used as a high power density and high efficiency battery charger. Since their implementation only considers unidirectional power flow from the grid to the battery, this chapter develops and implements a deadbeat predictive control method for this converter that validates the feasibility of the bidirectional operation of the PM-ANPC.

In summary, this chapter first introduces the PM-ANPC topology in section 3.2. Then, it gives an overview of its associated modulation method in section 3.3. The proposed system under test and deadbeat predictive controller are developed in section 3.4 and finally, section 3.5 presents the simulation results and validation of the proposed system.

3.2 Presentation of the PM-ANPC Converter Topology

In an effort to develop an efficient, modular and high power density converter for battery charger applications, the authors of (Abarzadeh *et al.*, 2020) proposed a multilevel three-phase converter

topology based on the 3-level active-neutral-point-clamped (3L-ANPC) converter. Namely, the PM-ANPC converter is a parallel arrangement of three 3L-ANPC cells per phase. As such, for a three-phase configuration, this converter is composed of a total of nine identical 3L-ANPC cells and is capable of generating 13 line-to-line voltage levels.

The per phase circuit diagram of the PM-ANPC converter is depicted in Fig. 3.1. The diagram shows how each of the 3L-ANPC cells is made up of six power electronic switches and connects to a leg inductance. The sum of the three leg currents that flow through those inductances sum up to become the corresponding phase current. In addition, the 3L-ANPC cells all share positive and negative DC voltage terminals as well as a neutral connection, together with the two DC link capacitors. Finally, the three-phase circuit diagram is obtained by replicating the per phase digram two more times while still sharing the same aforementioned DC side connections.

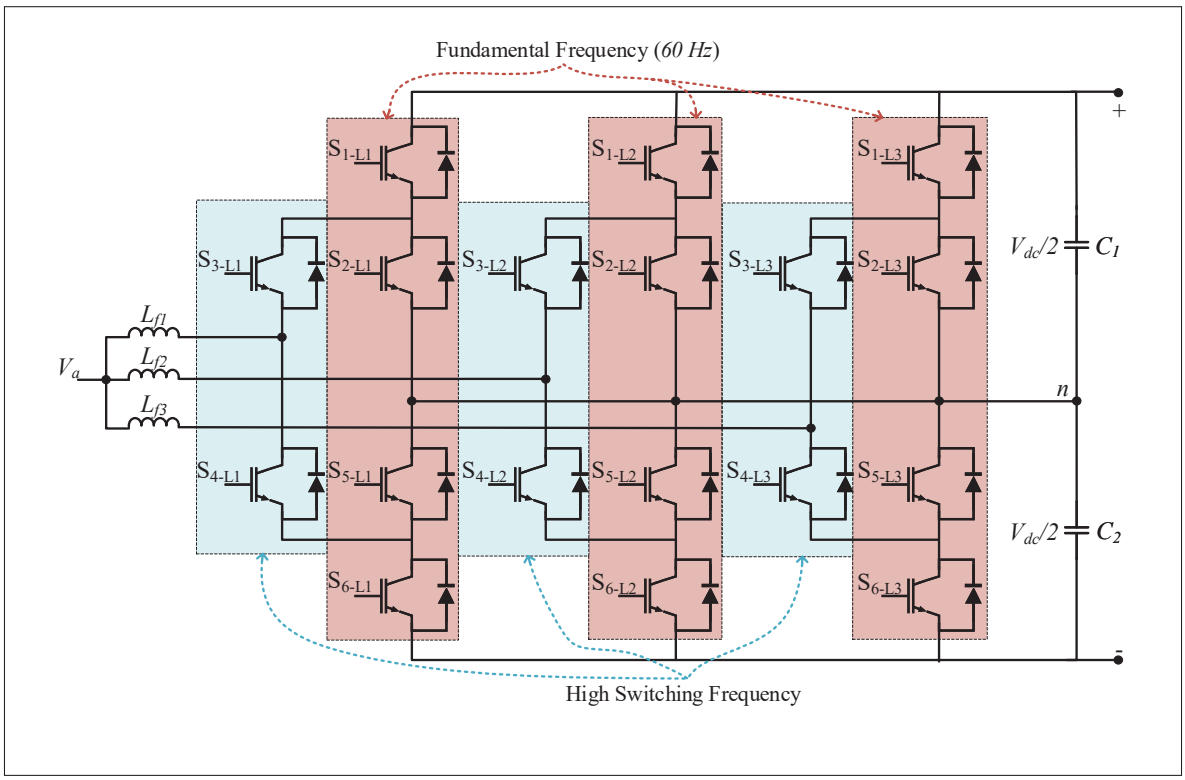

Figure 3.1 Per phase circuit diagram of the PM-ANPC converter

It should also be noted that one of the particularities of this topology is that only six of the 18 switches per phase are operated at switching frequency, while the rest operate at the low fundamental grid frequency. This feature helps in decreasing power losses due to the commutation of semiconductor switches.

3.3 Overview of the Modulation Method

The PM-ANPC converter is not complete without the associated modulation method that was also proposed in (Abarzadeh *et al.*, 2020). Indeed, it is thanks to this improved switching pattern that it is possible to achieve 7 phase-to-neutral or 13 line-to-line output voltage levels. Furthermore, this modulation method allows for four of the six switches in a 3L-ANPC cell to be operated at fundamental frequency and only two at switching frequency, which helps in reducing switching losses. Another particularity of this modulation technique is that the triangular carriers are phase-shifted by a third of the switching period between each of the three 3L-ANPC cells in a phase. This phase shift is what allows the high number of output voltage levels, but it also has the effect of shifting the first switching harmonic cluster by a factor of three.

The modulation technique is defined per 3L-ANPC cell, whose possible switching states are shown in Table 3.1. Since the full details of the switching technique are well documented by

Table 3.1 Switching States of a 3L-ANPC Cell

State	S_{1-x}	S_{2-x}	S_{3-x}	S_{4-x}	S_{5-x}	S_{6-x}	V_{leg-n}
1	1	0	1	0	1	1	$V_{dc}/2$
2	0	1	1	0	0	1	0
3	1	0	0	1	1	0	0
4	0	1	0	1	0	1	$-V_{dc}/2$

Abarzadeh *et al.* (2020), this chapter only presents a summary of the technique.

Hence, the first part of the modulation method is the generation of the switching signals for the fundamental frequency switch pairs S_{1-x}, S_{2-x} and S_{5-x}, S_{6-x}. This is achieved with a simple zero-crossing detection on the input reference voltage V_{ref}:

$$S_{1-x} = \overline{S_{2-x}} = S_{5-x} = \overline{S_{6-x}} = \begin{cases} 1 & \text{if} \quad V_{ref} \geq 0 \\ 0 & \text{if} \quad V_{ref} < 0. \end{cases} \tag{3.1}$$

where the bar over a variable denotes the NOT logical operator.

Next, the switching signals for the high frequency switch pair S_{3-x}, S_{4-x} are obtained by comparing a modified reference voltage $V_{ref-mod}$ to a triangular carrier C_{r-x}. The modified reference voltage is defined as

$$V_{ref-mod} = \begin{cases} V_{ref} & \text{if} \quad V_{ref} \geq 0 \\ 1 + V_{ref} & \text{if} \quad V_{ref} < 0 \end{cases} \tag{3.2}$$

and the carrier is a simple triangular wave going from 0 to 1 at the selected switching frequency. The switching signals are then obtained similarly to (3.1) such that

$$S_{3-x} = \overline{S_{4-x}} = \begin{cases} 1 & \text{if} \quad V_{ref-mod} \geq C_{r-x} \\ 0 & \text{if} \quad V_{ref-mod} < C_{r-x}. \end{cases} \tag{3.3}$$

Moreover, the triangular carriers are shifted by a third of the switching period between the three 3L-ANPC cells. In other words, if the three cells have carriers C_{r-1}, C_{r-2} and C_{r-3} with a switching period of T_{sw}, then C_{r-2} is equal to C_{r-1} with a time delay of $T_{sw}/3$ and C_{r-3} is equal to C_{r-1} with a time delay of $2 \times T_{sw}/3$. This time shift between each cell allows for the high number of output voltage levels and it also results in shifting the first cluster of switching harmonics by a factor of three. Hence, the use of the PM-ANPC converter with its associated modulation method results in better power quality, reduced harmonic distortion and reduced power losses.

3.4 Implementation of the Deadbeat Predictive Controller

3.4.1 The Deadbeat Predictive Controller for the PM-ANPC

There exist many types of control methods for grid-connected MLCs and most of them require the use of phase-locked-loops (PLL) to ensure proper synchronization with the grid. However, a different approach is used in (Abarzadeh, Weise, Katebi, Javadi & Al-Haddad) where a constant switching frequency deadbeat predictive controller (DPC) is developed. In fact, this method makes use of the stationary $\alpha - \beta$ reference frame to effectively remove the necessity of a PLL. This method also has an advantage over the previously discussed model predictive controller since DPC works with the more conventional constant frequency PWM modulation methods, meaning that the controller outputs a reference voltage signal that is input to a PWM pulse generator. This is different from the MPC method that directly outputs the gating signals and thus, has to pre-calculate every possible switching state at every time step. Moreover, the DPC is still able to provide good dynamic performance and reacts quickly to parameter variations. An overview of the DPC method implemented in this work is displayed in Fig. 3.2.

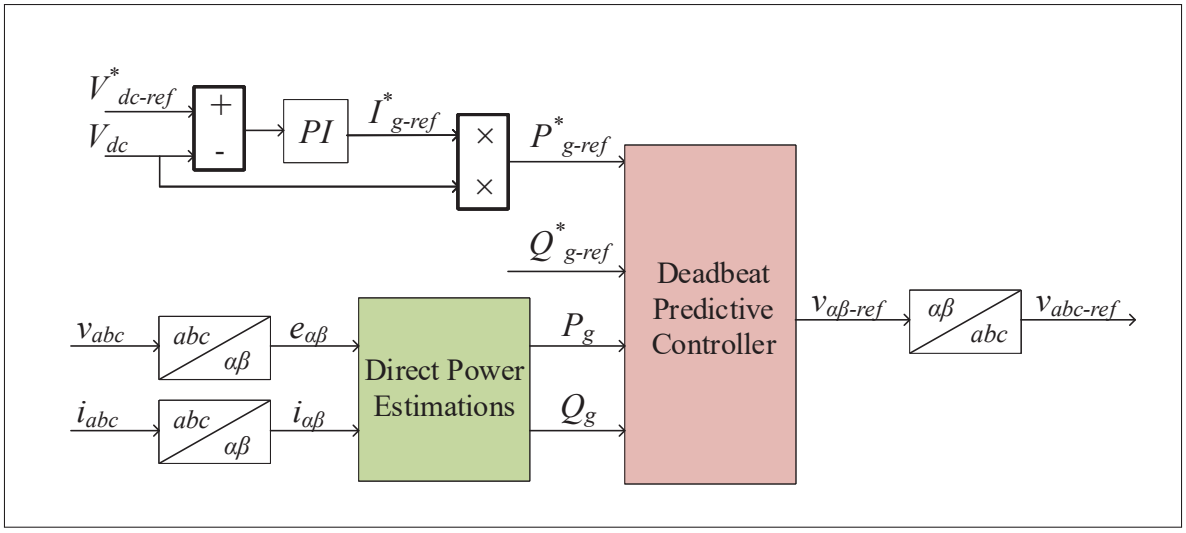

Figure 3.2 Diagram of the deadbeat predictive control system

The general idea behind the DPC is to regulate the converter's active and reactive power with direct power estimation equations that use the $\alpha - \beta$ transformations of the measured grid phase voltage v_{abc} and current i_{abc}. The simplified $\alpha - \beta$ (or Clarke) transformation

$$\begin{bmatrix} u_\alpha \\ u_\beta \end{bmatrix} = \frac{2}{3} \begin{bmatrix} 1 & -\frac{1}{2} & -\frac{1}{2} \\ 0 & \frac{\sqrt{3}}{2} & -\frac{\sqrt{3}}{2} \end{bmatrix} \begin{bmatrix} u_a \\ u_b \\ u_c \end{bmatrix} \tag{3.4}$$

is used in this work since the studied three-phase system is designed to be balanced and thus $u_0 = 0$. Then, the power estimation equations are:

$$P_g = \frac{3}{2}(i_\alpha v_\alpha + i_\beta v_\beta) \tag{3.5}$$

$$Q_g = \frac{3}{2}(i_\alpha v_\beta - i_\beta \, v_\alpha). \tag{3.6}$$

In addition, the active power reference value P^*_{g-ref} is determined by the output of the DC link voltage proportional-integral regulator, multiplied by the measured DC link voltage V_{dc}. This makes it so that the DC link can stay regulated at its target value regardless of the battery power reference given to the inner control loop of the DC-DC converter. As for the reactive power reference Q^*_{g-ref}, this one is maintained at 0 in order to ensure maximum active power transfer and unity power factor.

Now, the design of the deadbeat predictive controller starts with the Kirchoff voltage loop (KVL) equation between the grid voltage (v_{abc}) and the PM-ANPC converter voltage (e_{abc}),

$$e_{\alpha\beta}(t) = r_g i_{\alpha\beta}(t) + L_g \frac{di_{\alpha\beta}(t)}{dt} + v_{\alpha\beta}(t) \tag{3.7}$$

written in the $\alpha - \beta$ reference frame, where r_g and L_g are the line resistance and inductance defined in Fig. 3.3. Similarly to the model predictive control proposed in the previous chapter, the predictive element of the DPC comes from the discretization of the derivative term in (3.7).

Thus, by using the Forward Euler approximation,

$$\frac{di_{\alpha\beta}(t)}{dt} \approx \frac{i_{\alpha\beta}(k+1) - i_{\alpha\beta}(k)}{T_s} \tag{3.8}$$

where T_s is the computation time step and k is the discrete sampling index. Then, equation (3.7) can be rewritten in a discretized form:

$$i_{\alpha\beta}(k+1) - i_{\alpha\beta}(k) = \frac{T_s}{L_g}(e_{\alpha\beta}(k) - v_{\alpha\beta}(k)). \tag{3.9}$$

It should be noted that (3.9) is valid only under the assumption that the value of r_g is very small such that it can be considered to be 0. Additionally, since the sampling period is typically much smaller than the period of the fundamental grid frequency, then the difference in the voltage $e_{\alpha\beta}$ between each time step is also negligible. Therefore, the approximation $e_{\alpha\beta}(k+1) \approx e_{\alpha\beta}(k)$ can be made. With this simplification, equations for the time step change in active and reactive power can be defined:

$$\begin{bmatrix} P_g(k+1) - P_g(k) \\ Q_g(k+1) - Q_g(k) \end{bmatrix} = \begin{bmatrix} e_\alpha(k) & e_\beta(k) \\ e_\beta(k) & -e_\alpha(k) \end{bmatrix} \begin{bmatrix} i_\alpha(k+1) & -i_\alpha(k) \\ i_\beta(k+1) & -i_\beta(k) \end{bmatrix}. \tag{3.10}$$

Next, by substituting (3.9) in (3.10), the equation becomes:

$$\begin{bmatrix} P_g(k+1) - P_g(k) \\ Q_g(k+1) - Q_g(k) \end{bmatrix} = \frac{T_s}{L_g} \begin{bmatrix} e_\alpha(k) & e_\beta(k) \\ e_\beta(k) & -e_\alpha(k) \end{bmatrix} \left[\begin{pmatrix} e_\alpha(k) \\ e_\beta(k) \end{pmatrix} - \begin{pmatrix} v_\alpha(k) \\ v_\beta(k) \end{pmatrix} \right]. \tag{3.11}$$

Now, for the deadbeat predictive control to work, the predicted values of the active and reactive powers $P_g(k+1)$ and $Q_g(k+1)$ should be equal to the predicted values of their references, namely $P^*_{g-ref}(k+1)$ and $Q^*_{g-ref}(k+1)$. Since the reference values of power are not expected to vary significantly between time steps, the approximations $P^*_{g-ref}(k+1) \approx P^*_{g-ref}(k)$ and $Q^*_{g-ref}(k+1) \approx Q^*_{g-ref}(k)$ can be made. Again, these are the two reference values first defined in Fig. 3.2, where $P^*_{g-ref}(k)$ is the active power reference generated by the DC link voltage regulator and $Q^*_{g-ref}(k)$ is the reactive power reference which is kept at 0. Finally, (3.11) can be

rearranged and the power reference values can be substituted in to obtain the following deadbeat predictive control rules:

$$\begin{bmatrix} v_{\alpha-ref}(k) \\ v_{\beta-ref}(k) \end{bmatrix} = \begin{bmatrix} e_\alpha(k) \\ e_\beta(k) \end{bmatrix} - \frac{L_g}{T_s(e_\alpha^2(k) + e_\beta^2(k))} \begin{bmatrix} e_\alpha(k) & e_\beta(k) \\ e_\beta(k) & -e_\alpha(k) \end{bmatrix} \begin{bmatrix} P^*_{g-ref}(k) - P_g(k) \\ Q^*_{g-ref}(k) - Q_g(k) \end{bmatrix} \quad (3.12)$$

where $v_{\alpha-ref}(k)$ and $v_{\beta-ref}(k)$ are the calculated reference voltages that are then passed through the inverse simplified $\alpha - \beta$ transformation

$$\begin{bmatrix} u_a \\ u_b \\ u_c \end{bmatrix} = \frac{3}{2} \begin{bmatrix} \frac{2}{3} & 0 \\ -\frac{1}{3} & \frac{\sqrt{3}}{3} \\ -\frac{1}{3} & -\frac{\sqrt{3}}{3} \end{bmatrix} \begin{bmatrix} u_\alpha \\ u_\beta \end{bmatrix} \quad (3.13)$$

to become $v_{abc-ref}$. This reference voltage is the input to the modulation method described in section 3.3.

To conclude, the DPC method presented in this section allows for bidirectional power flow control, good dynamic performance and resilience to parameter variations, while also removing the requirement for a PLL thanks to the use of the stationary $\alpha - \beta$ reference frame.

3.5 Simulation Results and Validation

3.5.1 System Under Test

Now that the converter and its modulation method are defined, a test system can be developed that will allow to implement a bidirectional power flow control system. This system under test is composed of the PM-ANPC three-phase converter itself connected to a three-phase voltage source on the AC side and to a bidirectional DC-DC converter. These connections are show in Fig. 3.3, where the battery is also seen on the right side of the bidirectional chopper.

Thus, there are two parts to the overall control system: the DC-DC converter uses a simple proportional-integral controller to control the power amplitude and direction at the battery, and

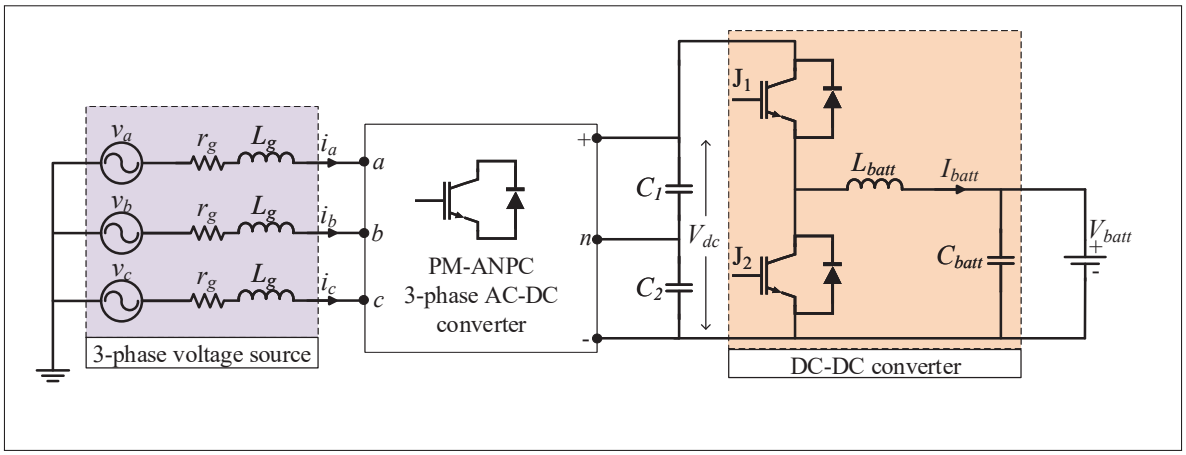

Figure 3.3 Diagram of the system under test

the PM-ANPC converter uses the proposed deadbeat predictive controller to regulate the DC link voltage along with the AC current.

3.5.2 Pulse Generation for the DC-DC Converter

The inclusion of the bidirectional chopper in this system is meant to facilitate the control of the bidirectional power flow from the battery on the DC side (Zhang, Lai, Kim & Yu, 2007). Indeed, this is possible because this DC-DC converter can operate in both buck and boost modes by selecting which of the two switches J_1, J_2 is driven by the PWM signal. As such, power flows from the grid to the battery (charging) when J_1 is being driven by the PWM signal and J_2 is maintained open. Conversely, power flows from the battery to the grid (discharging) when J_2 is being driven by the PWM signal and J_1 is maintained open. The control method for generating these PWM pulses is illustrated in Fig. 3.4.

Therefore, pulse train P is a PWM signal generated by comparing the duty cycle d (between 0 and 1) to a unit sawtooth carrier signal at switching frequency. The duty cycle d is determined by a proportional-integral controller that takes as its input the error between the reference battery current I^*_{ref} and the measured current I_{batt}, as defined in Fig. 3.4. The reference current is itself calculated as a function of the constant battery voltage V_{batt} and the user-defined reference

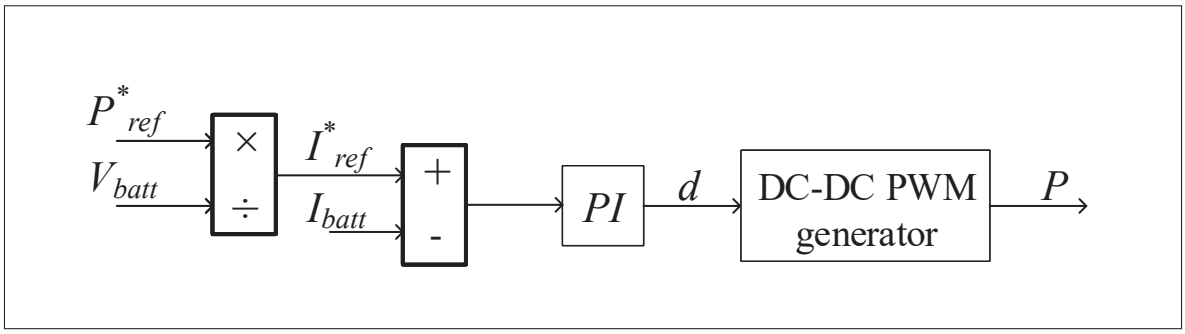

Figure 3.4 Diagram of DC-DC converter pulse generation

battery power P^*_{ref}. It should be noted that the convention used in this work is such that a positive P^*_{ref} corresponds to the charging mode and a negative value represents the discharging mode of operation. Furthermore, the gating signals for J_1 and J_2 are determined as follows:

$$J_1 = P, \quad J_2 = 0 \quad \text{if} \quad I^*_{ref} \geq 0 \tag{3.14}$$

$$J_1 = 0, \quad J_2 = \overline{P} \quad \text{if} \quad I^*_{ref} < 0. \tag{3.15}$$

The definitions in (3.14) and (3.15) ensure that the bidirectional chopper will operate in the correct mode with respect to the sign of the reference current, which itself indicates the direction of the power flow. Thus, the proposed inner control loop for the bidirectional DC-DC converter allows regulate the amplitude and direction of the power in the battery charger.

3.5.3 Simulation Setup

In this section, the proposed DPC bidirectional power flow controller is implemented with the PM-ANPC converter in the Matlab/Simulink environment. Simulation results are provided to validate the performance of the proposed control method during a transition between charging and discharging modes. In addition, analyses of the harmonic spectra of the AC voltage and current are performed in order to illustrate the improved power quality of the PM-ANPC. The simulated system is the same as the system under test pictured in Fig. 3.3 and the parameters

used for the simulation are listed in Table 3.2. Finally, it should be noted that the simulation time step is set to $1\mu s$ based on the fact that the switching frequency is 10 kHz. This allows to sample 100 data points per switching period. While the effective switching bandwidth of the PM-ANPC is potentially higher than 10 kHz due to the 13 voltage levels, a sampling period of $1\mu s$ is considered more than sufficient for accurate results in this work.

Table 3.2 Circuit and simulation parameters

Parameter	**Values**
DC link voltage	$V_{dc} = 750V$
DC battery voltage	$V_{batt} = 500V$
Battery inductance	$L_{batt} = 750\mu H$
Battery capacitance	$L_{batt} = 200\mu F$
DC switching frequency	$f_{sw} = 20kHz$
AC 3Φ voltage source	$V_{ac} = 480Vrms$
Fundamental frequency	$f = 60Hz$
AC switching frequency	$f_{sw} = 10kHz$
Leg inductance	$L_f = 800\mu H$
Grid inductance	$L_g = 200\mu H$
Grid resistance	$r_g = 0.1\Omega$
DC capacitor	$C_1 = C_2 = 4.6mF$
Simulation time step	$T_s = 1\mu s$

3.5.4 Bidirectional Power Flow Results

Accordingly, the first test aims to confirm the capability for bidirectional power flow as well as the dynamic performance of the controller. Thus, the battery power reference is initially set to +50kW and at $t = 0.2s$, a decreasing ramp lasting three fundamental cycles (0.05 s) brings the reference from +50kW to -50kW. In Fig. 3.5, the simulation results from this test are shown for the battery current I_{batt} and the DC link voltage V_{dc}.

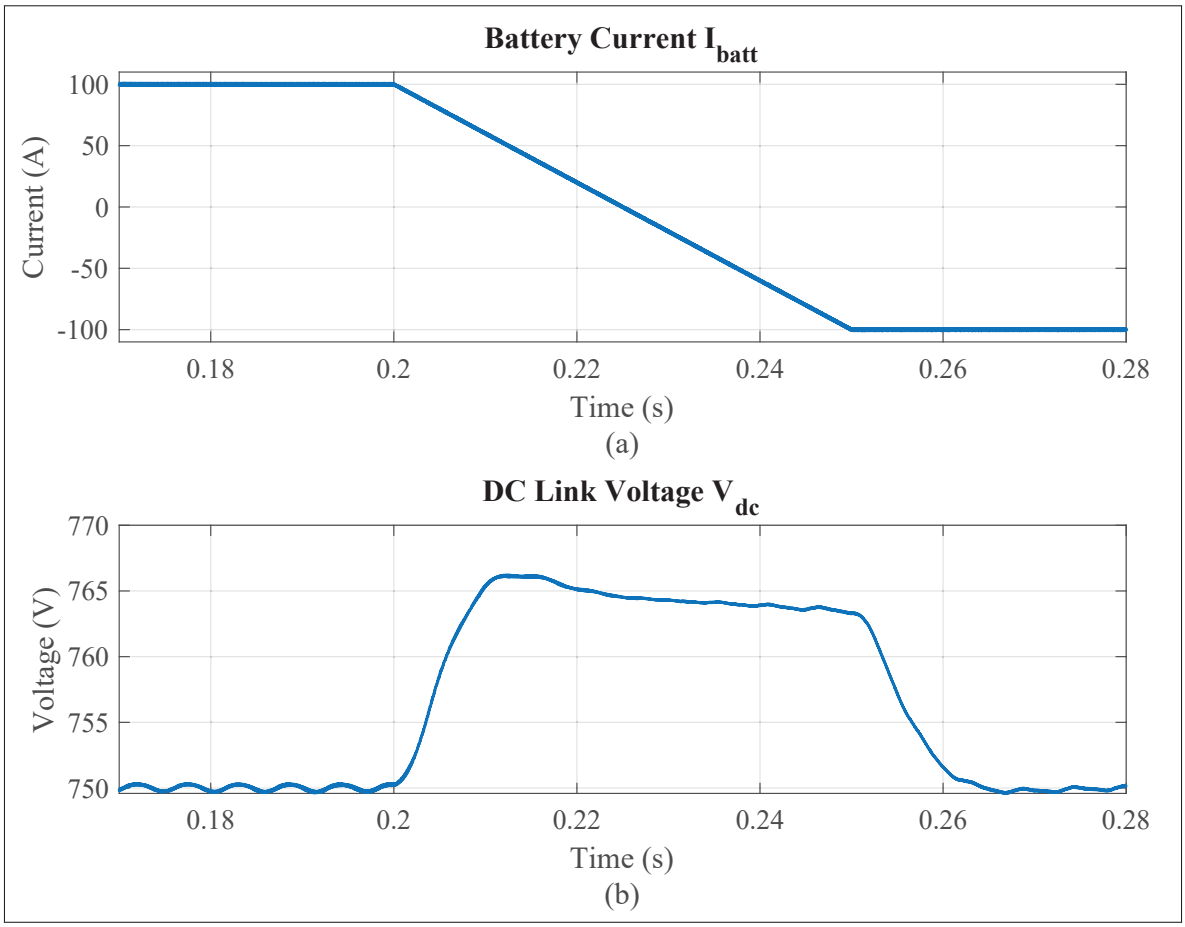

Figure 3.5 Simulation results during a reversal in the power flow direction for (a) the battery current and (b) the DC link voltage

As expected, the measured battery current goes from positive to negative 100A on a decreasing ramp that starts at $t = 0.2s$. Since the battery voltage in this system is a constant 500V, then the power at the battery does in fact properly track the +50kW to -50kW reference. In addition, the measured DC link voltage is quickly regulated back to its reference of 750V once the ramp is over, and the overshoot is 2.1% of the nominal value during the transition.

Next, Fig. 3.6 illustrates the simulation results during the same test for the AC grid voltage and current as well as the PM-ANPC converter voltage. Note that only one phase of each AC measurement is displayed and that the current measurement is multiplied by two so that it is easier to see against the voltage. Also, while the grid voltage shown is the phase-to-ground

measurement, it is the line-to-line voltage measurement of the PM-ANPC that is shown in order to highlight the 13 voltage levels that characterize this converter.

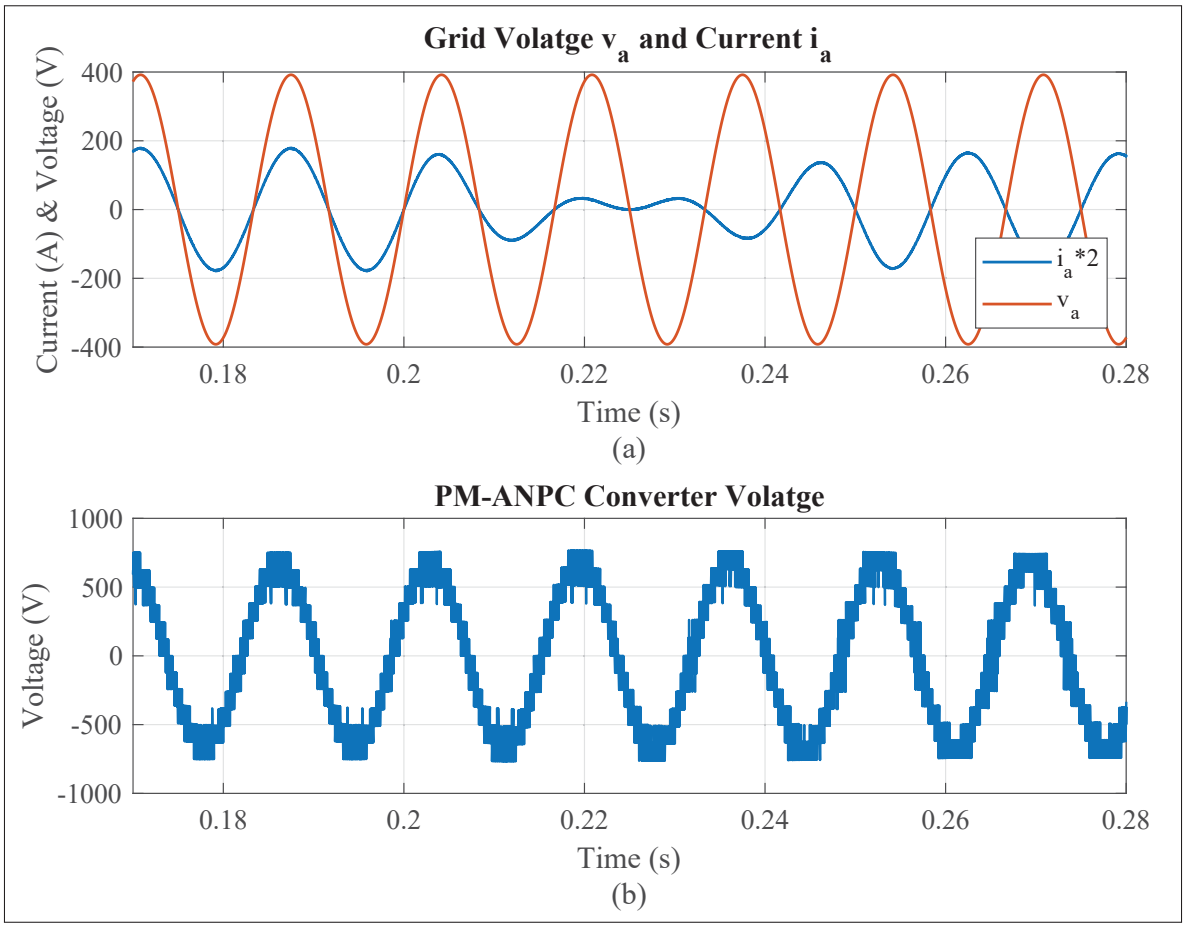

Figure 3.6 Simulation results during a reversal in the power flow direction for (a) the grid current & voltage and (b) the PM-ANPC converter voltage

The first observation that can be made is that the measured grid current is perfectly in phase with the grid voltage before $t = 0.2s$ when the battery power reference is positive. This behaviour is expected considering the current measurement direction defined in Fig. 3.3. It means that the grid is generating active power and thus, that power is flowing from the grid to the battery. Conversely, after the ramp when the power reference is negative, the measured grid current is perfectly out of phase with the voltage, which means the grid is consuming active power and that the direction of power flow is indeed reversed. Meanwhile, the line-to-line PM-ANPC converter

voltage shows almost no disturbance during the ramp in power reference. Indeed, the waveform maintains 13 voltage levels in both charging and discharging modes.

Therefore, the proposed DPC is capable of properly tracking the DC link voltage and maintains smooth AC current and voltage waveforms regardless of the direction of power flow.

3.5.5 Analysis of the Harmonic Spectra

Since one of the main features of the PM-ANPC multilevel converter is its improved power quality and harmonic mitigation, it is relevant to analyse the harmonic spectrum of the converter voltage. These analyses are performed by using the fast Fourier transform (FFT) tool in Simulink on the PM-ANPC 13-level voltage waveform for both charging (+50kW) and discharging (-50kW) modes.

The harmonic spectrum of the PM-ANPC voltage during charging mode is seen in Fig. 3.7.

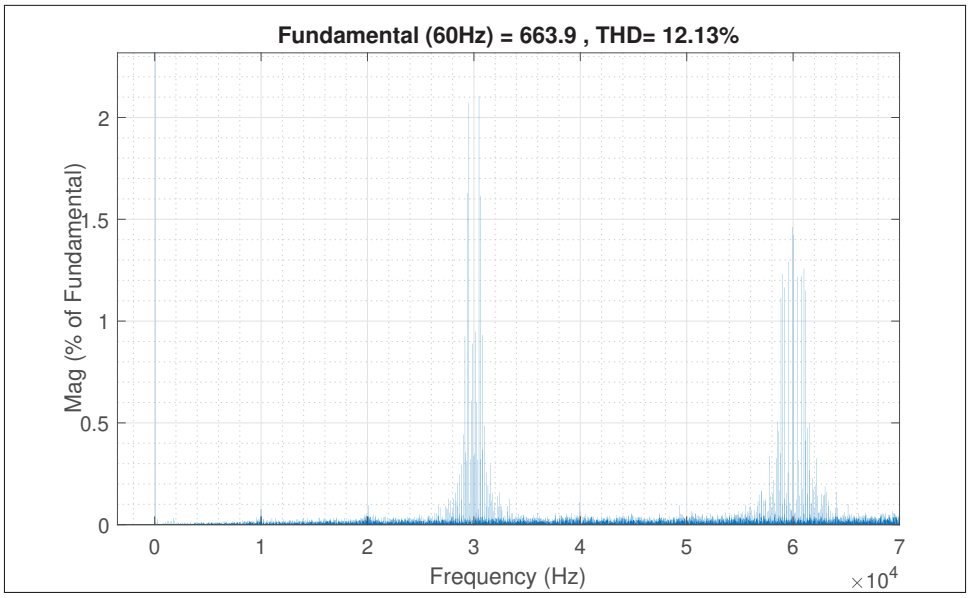

Figure 3.7 Harmonic spectrum of the converter voltage during charging mode

It should already be expected that the more sinusoidal voltage shape given by the 13 voltage

levels would result in a low total harmonic distortion (THD) value. However, as it is explained in section 3.3, the modulation method employed with the PM-ANPC allows to shift the first switching harmonic cluster by a factor of three. This feature is confirmed here as it is clear that while the the AC switching frequency is 10kHz, the first harmonic cluster appears around 30 kHz and then at every subsequent integer multiple of that value. The 13 voltage levels coupled with the harmonic cluster shift result is a low THD value of 12.13%. Additionally, the measured THD of the grid current over the same period is only 0.36%, which further validates the good power quality of the PM-ANPC.

Next, the converter voltage harmonic spectrum is also displayed for the discharging mode in Fig. 3.8 to confirm that the power quality is good regardless of the direction of power flow.

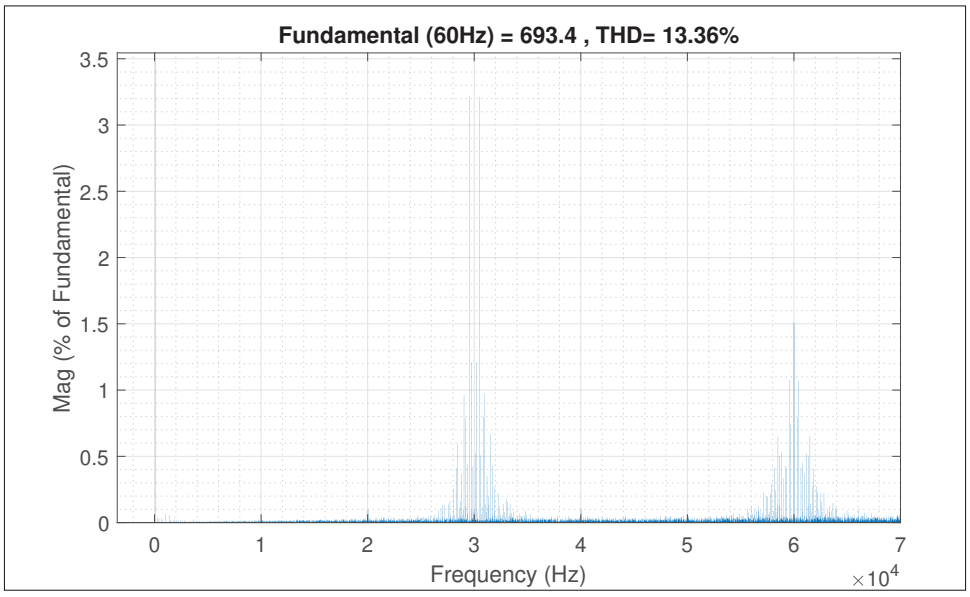

Figure 3.8 Harmonic spectrum of the converter voltage during discharging mode

Indeed, the graph displays very similar results to the spectrum from the charging mode. The major harmonic clusters are still at the multiples of 30kHz and while the voltage THD is a bit higher, it is still relatively low at 13.36%. The measured current THD is also still very low at

0.45%, thus confirming that the inherent harmonic mitigation from the PM-ANPC 13-level voltage and its switching technique also work well in the discharging mode.

Hence, the simulation results presented in this section validate the performance of the PM-ANPC converter coupled with the proposed DPC control system. In fact, the controller allows to accurately track the battery power reference for positive and negative values. Meanwhile, the DC link voltage remains well regulated at its nominal value and the AC voltage and current remain smooths and nearly undisturbed during changes in the power reference. All of this is achieved while also keeping THD levels relatively low on the AC side measurements.

3.6 Conclusion

The 13-level PM-ANPC three-phase converter is investigated in this chapter due to its high power density and good harmonic mitigation performance, which make it an appealing option for battery chargers. More specifically, a bidirectional battery charging system based on this converter is designed in conjunction with the proposed DPC control system. The associated PM-ANPC modulation method allow for only 6 out 18 switches per phase to be operated at switching frequency while the rest operate at low fundamental frequency, which leads to less switching power losses. Then, a deadbeat predictive control system is developed to be able to deliver active power from the grid to the battery or from the battery back to grid. The DPC achieves this bidirectional power control and it also regulates the DC link voltage as well the AC current and converter voltage. Moreover, the controller reacts quickly to changes in the power reference, as is demonstrated in the simulation results. Finally, these results also validate the improved power quality of the PM-ANPC with the proposed DPC system.

CHAPTER 4

AN EQUIVALENT MODEL OF THE PARALLELED MODULAR ANPC CONVERTER WITH A DECOUPLED DC LINK FOR REAL-TIME SIMULATION

4.1 Introduction

The bidirectional battery charging system based on the PM-ANPC converter that is presented in Chapter 3 is a complicated system due to its large number of power electronic switches. Consequently, it would be difficult and costly to do a hardware implementation of one of these battery chargers. Moreover, commercially available battery chargers are typically installed in groups of multiple units, meaning that it would be more relevant to analyse a system composed of multiple PM-ANPC bidirectional battery chargers all connected to the same grid. In this case, a hardware implementation becomes all the more difficult, which is why simulations become the preferred alternative.

Indeed, simulations of such large, high power electrical systems are often performed by manufacturers before any kind of hardware implementation. In fact, one possible intermediary step before hardware prototyping is real-time simulation (RTS). RTS is an essential tool when doing rapid control prototyping (RCP) of large electrical systems as it allows for hardware-in-the-loop (HIL) testing, in which simulated electrical systems can be tested in conjunction with real hardware controllers (Dufour & Bélanger, 2014). However, some difficulties with RTS arise when dealing with the aforementioned MLCs. In fact, the large number of power electronic switches paired with the high switching frequencies of MLCs result in considerable computational burden in simulation. This burden is due to the different circuit solving methods, which often rely on storing and solving large sets of matrices whose sizes increase with the number of switches and switching states. Furthermore, high switching frequencies means that more of these matrix calculations must be performed at every computation time step (Dommel, 1969; Dufour *et al.*, 2010). Plus, as it is shown in Chapter 3, a low value of simulation time step is required to achieve accurate results for the PM-ANPC. Hence, it becomes difficult if not

impossible to achieve true real-time when simulating large circuits with multiple MLCs, each containing many power electronic switches.

A solution to these drawbacks is to use equivalent converter models based on switching functions, which already exist in the literature for some converter types (Zhang & Li, 2019; Li & Zhang, 2019). No power electronic switches are present in these models. Instead, they make use of controlled voltage and current sources whose equations depend on the switching signals of the converter. Since there are no switches in these models, it is not necessary to store or recalculate the matrices for each possible switching state of a given converter. Therefore, the simulations can run more quickly while still being accurate. Thus, it also becomes possible to simulate in true real-time.

In this chapter, a switching function-based equivalent converter model for the 13-level PM-ANPC converter (Abarzadeh *et al.*, 2020) with a decoupled DC link is developed and tested. This converter is chosen due to its potential for high power density and its good total harmonic distortion (THD) mitigation. Furthermore, the proposed model aims to generate fast simulation results while minimizing the error with respect to a reference, switch-based model. This equivalent model is developed in section 4.2. Then, section 4.3 presents the decoupled DC link of the equivalent model. Finally, the comparisons and simulation results that validate the efficacy of the proposed model are discussed in section 4.4.

4.2 Equivalent Model of a PM-ANPC Cell

4.2.1 The 3L-ANPC Cell

A more detailed description of the PM-ANPC converter is already given in the previous chapter. Hence, this section only repeats the details that are the most relevant for the equivalent model. The per phase circuit diagram of the PM-ANPC is reproduced in Fig. 4.1 with a highlight on one of the 3L-ANPC cells.

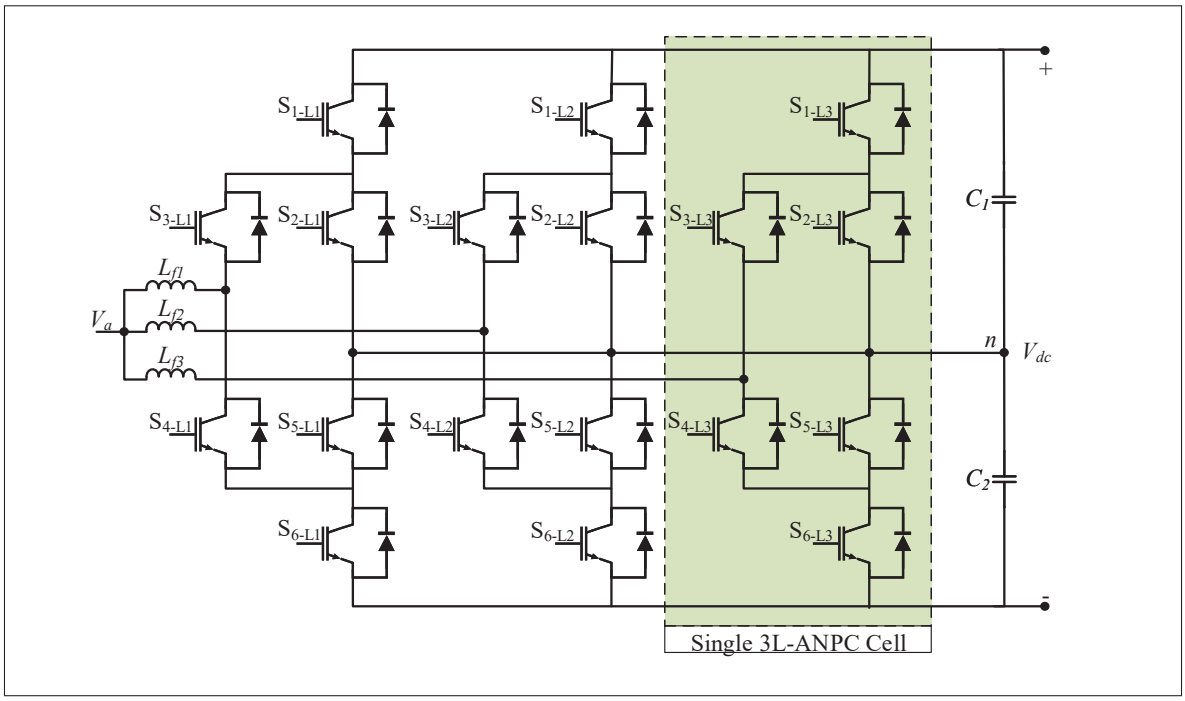

Figure 4.1 Per phase circuit diagram of the PM-ANPC converter highlighting a 3L-ANPC cell

This cell is important since it is the basis of the model developed in this chapter. Indeed, the next subsection takes this cell and replaces it with a switching function based controlled voltage source model. Once the equivalent model is defined, then by connecting nine of them appropriately, the full three-phase converter is obtained. Finally, unlike in Fig. 4.1, a separate DC link model is proposed in this chapter that is electrically decoupled from the rest of the converter.

4.2.2 Model of a Half-Bridge Converter

The equivalent PM-ANPC cell model developed in this work is based on similar equivalent voltage source converter (VSC) models that are presented in the literature. More specifically, in (Li & Zhang, 2019) the authors propose a general interpolated VSC model based on the equivalent model of a half-bridge (HB) converter.

The general idea behind the equivalent HB model is to replace the circuit, which is normally composed of two power electronic switches, with two parallel controlled voltage sources (V_{sp}, V_{sn}) each in series with antiparallel diodes (D_p, D_n). Here, the subscripts p and n represent the positive and negative directions of current. This equivalent circuit is illustrated in Fig. 4.2. The antiparallel diodes emulate the positive and negative directions of current flow. Furthermore, the voltages are calculated using a switching function that depends on the input voltage V_{in} and the switching pulses S_U and S_L, where the subscripts U and L denote the upper and lower switches of the HB converter respectively.

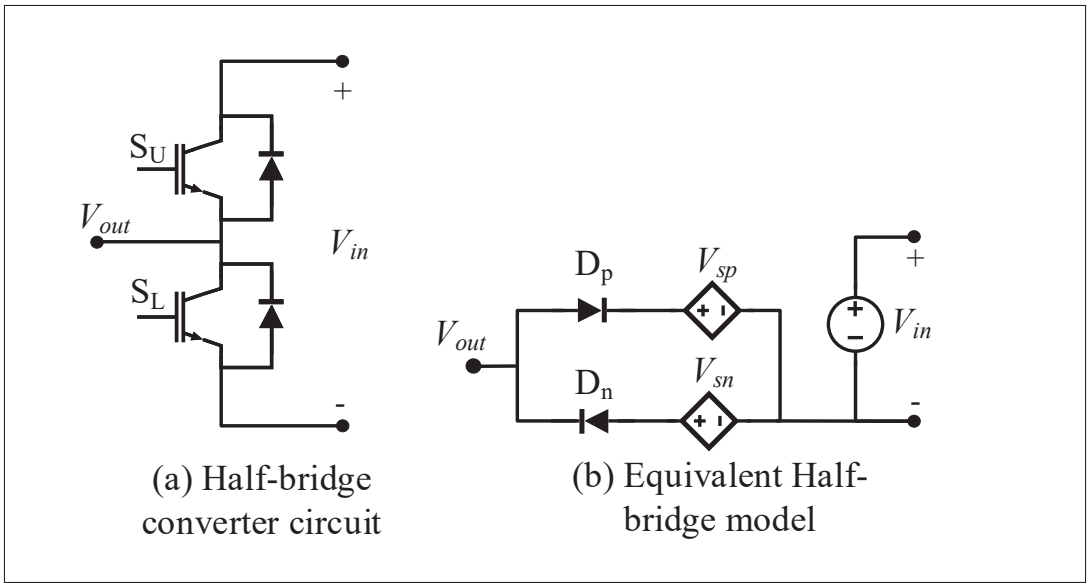

Figure 4.2 (a) Half-bridge converter and (b) equivalent model with controlled voltage sources

Such a model also allows to emulate the different modes of operation that determine the current path in a half-bridge converter: insert, bypass, diode and fault. Depending on the mode of operation, the controlled voltage sources will either be equal to the input voltage V_{in} or zero. A table summarizing the values of the voltage sources with respect to the switching pulses is presented in (Li & Zhang, 2019) and reproduced in Table 4.1.

The definitions in this table are used in order to develop the voltage equations discussed in the next subsection.

Table 4.1 Positive and negative path voltages with respect to the switching pulses

Mode of Operation	S_U	S_L	K_p	K_n	V_{sp}	V_{sn}
Insert	1	0	1	1	V_{in}	V_{in}
Bypass	0	1	0	0	0	0
Blocking	0	0	1	0	V_{in}	0
Fault	1	1	0	0	0	0

4.2.3 Full 3L-ANPC Cell Model and Voltage Calculations

The PM-ANPC converter is made up of nine identical 3L-ANPC cells. A circuit diagram of a single 3L-ANPC cell is shown in Fig. 4.3. By inspecting this circuit, it becomes apparent that it can be deconstructed into three switch pairs, labelled x, y and z, that could each be considered as half-bridge submodules.

Moreover, for the purpose of the equations presented in this section, switch pairs $S_1 - S_2$ and $S_3 - S_4$ follow the upper and lower switch notation (S_U, S_L) defined in Fig. 4.2, but this notation is reversed for switch pair $S_5 - S_6$. In other words,

$$S_{Ux} = S_1, \qquad S_{Uy} = S_6, \qquad S_{Uz} = S_3$$

$$S_{Lx} = S_2, \qquad S_{Ly} = S_5, \qquad S_{Lz} = S_4.$$

In fact, based on the variables in Table 4.1, it is possible to write logical equations that define the insertion factors K_p, K_n for each switch pair:

$$K_{pi} = (1 - S_{Li}), \qquad i = x, y, z \tag{4.1}$$

$$K_{ni} = S_{Ui} \cdot (1 - S_{Li}), \qquad i = x, y, z. \tag{4.2}$$

In the previous equations, the binary variables S_{Ui} and S_{Li} are the switching pulses obtained from the modulation method of the PM-ANPC.

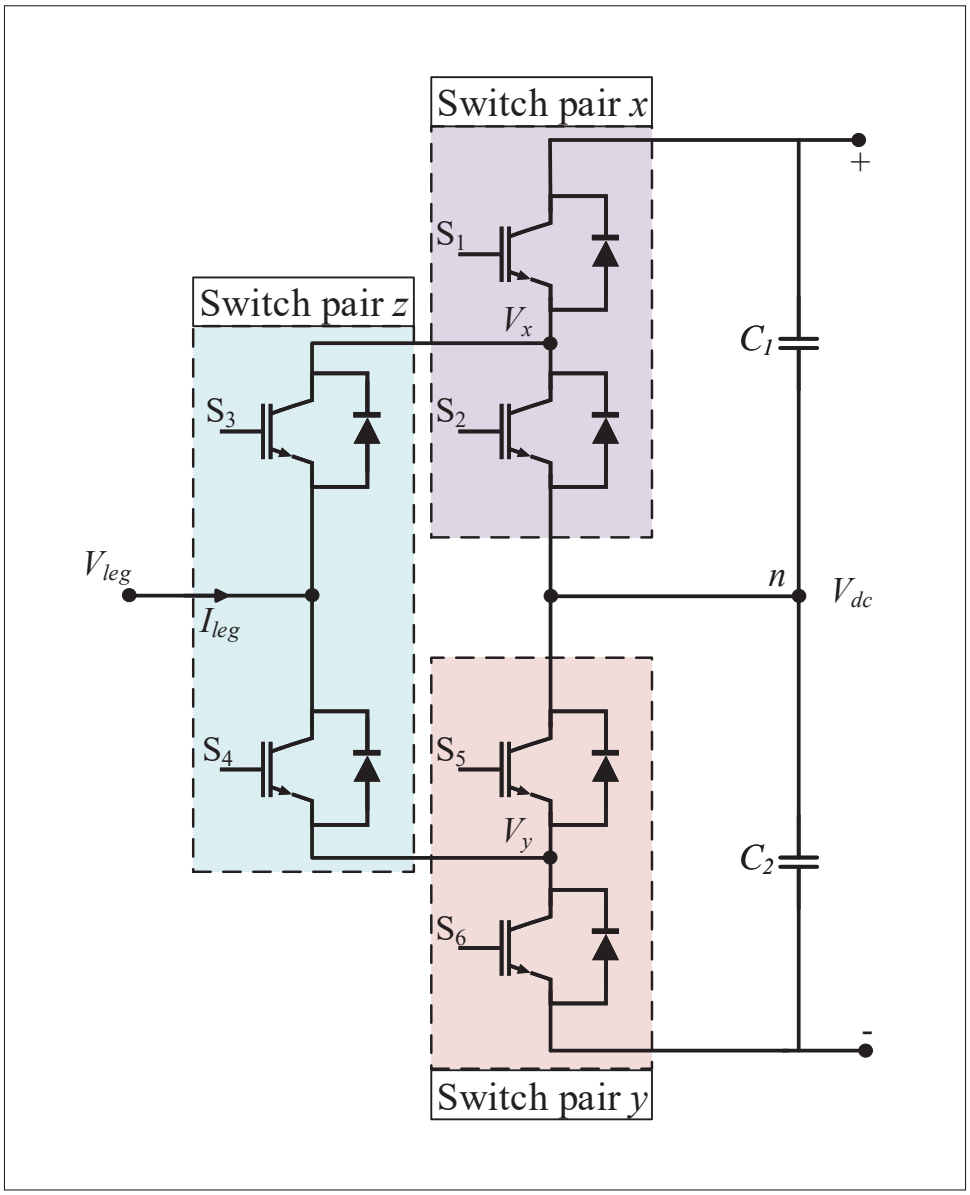

Figure 4.3 Circuit diagram of a 3L-ANPC cell highlighting the half-bridge submodules

Additionally, this circuit has two connection points: the neutral point labelled n and the output leg connection labelled V_{leg}. It is possible to separate the leg-to-neutral voltage in two parts: one part from switch pair x (V_x) and the other from switch pair y (V_y) as defined previously. Indeed, the two voltages can be calculated as functions of the input capacitor voltages and the

insertion factors in (4.1) and (4.2):

$$V_{jx} = K_{jx} \cdot V_{C1}, \qquad j = p, n \tag{4.3}$$

$$V_{jy} = -K_{jy} \cdot V_{C2}, \qquad j = p, n. \tag{4.4}$$

As such, the proposed equivalent 3L-ANPC model is obtained by further simplifying the equivalent HB circuit as in Fig. 4.4.

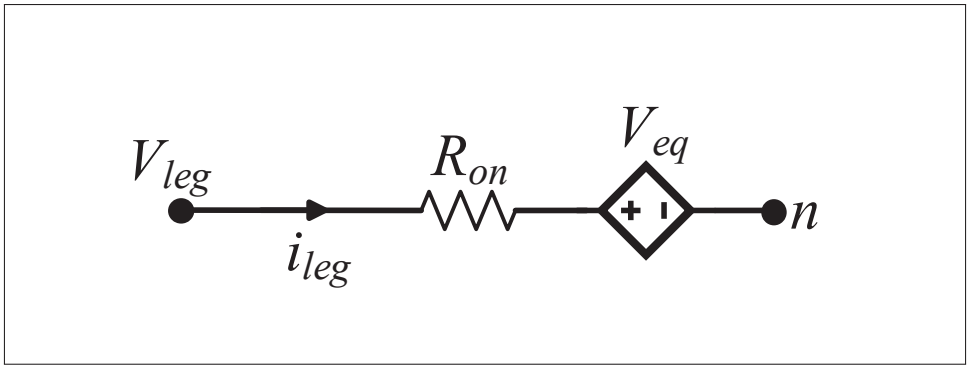

Figure 4.4 Equivalent 3L-ANPC cell model

In this equivalent model, a single controlled voltage source replaces the pairs of voltage sources and diodes seen in Fig. 4.2 and the resistor R_{on} emulates the on resistance of semiconductor switches. The equation for the V_{eq} voltage source is

$$V_{eq} = \begin{cases} K_{pz} \cdot V_{px} + (1 - K_{pz}) \cdot V_{py} & \text{if} \quad i_{leg} \geq 0 \\ K_{nz} \cdot V_{nx} + (1 - K_{nz}) \cdot V_{ny} & \text{if} \quad i_{leg} < 0 \end{cases} \tag{4.5}$$

where the function is defined piecewise with respect to a zero-crossing condition on the leg current so as to reproduce the effect of two parallel voltage sources with antiparallel diodes.

Unlike the HB submodule in Fig. 4.2, here the input neutral connection does not connect to an input voltage source or DC link. Indeed, the next subsection presents the decoupled DC link that completes the proposed equivalent model.

Therefore, the proposed switching function based equivalent model allows to simulate the appropriate leg-to-neutral voltage while being able to emulate the insert and bypass modes of operation. While the proposed model does not properly reproduce the blocking mode, it manages to reduce the complexity and improve the performance when compared to previous implementations in the literature. Finally, by connecting nine 3L-ANPC equivalent circuits as shown in Fig. 4.4, the full three-phase PM-ANPC equivalent circuit is obtained.

4.3 Modelling of the Decoupled DC Link Capacitors

4.3.1 Decoupled DC Link Model and Current Calculations

In the previous section, the equivalent model of a 3L-ANPC model is developed. Because the approach chosen in this paper is to decouple the DC link from the rest of the circuit, it is necessary to also have an accurate DC link model from which the capacitor voltage measurements V_{C1} and V_{C2} can be sent to the 3L-ANPC model. Similarly, the leg current measurements from the 3L-ANPC cells are used in the DC link model.

The decoupled DC link circuit is shown in Fig. 4.5, in which it is seen to be made up of the two DC capacitors C_1 and C_2, and three controlled current sources. There is also a separate controlled voltage source that represents the DC side of the overall PM-ANPC converter circuit.

The two left-hand side current sources labelled I_1 and I_2 are obtained from the aforementioned 3L-ANPC cell leg currents according to the equations

$$I_1 = \sum_{m=1}^{9} i_{leg}^m \times \begin{cases} K_{pz}^m \cdot K_{px}^m & \text{if} \quad i_{leg} \geq 0 \\ K_{nz}^m \cdot K_{nx}^m & \text{if} \quad i_{leg} < 0 \end{cases} \tag{4.6}$$

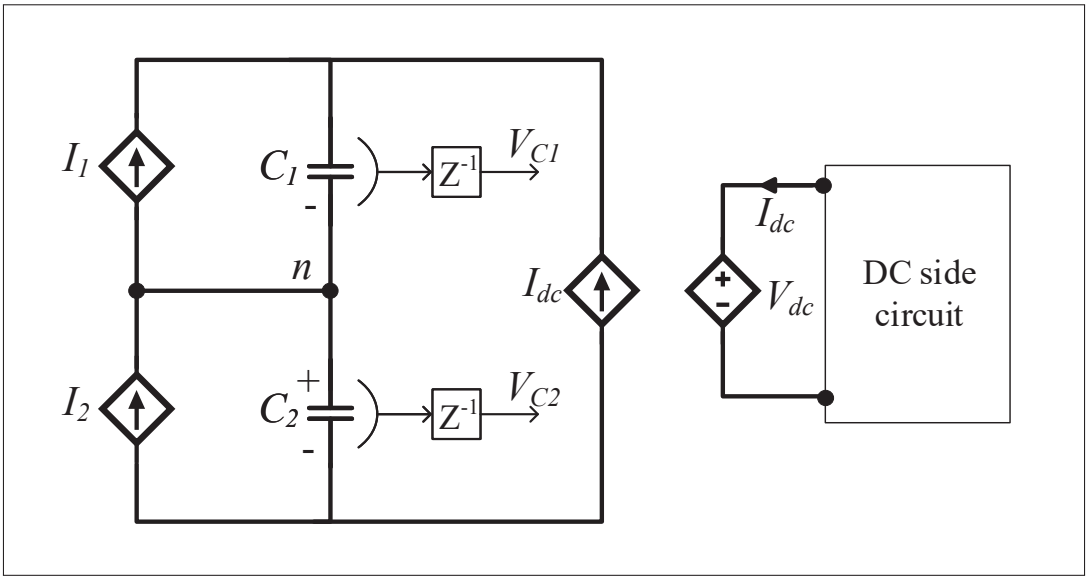

Figure 4.5 Circuit diagram of the decoupled DC link

$$I_2 = -\sum_{m=1}^{9} i_{leg}^{m} \times \begin{cases} (1 - K_{pz}^{m}) \cdot K_{py}^{m} & \text{if} \quad i_{leg} \geq 0 \\ (1 - K_{nz}^{m}) \cdot K_{ny}^{m} & \text{if} \quad i_{leg} < 0 \end{cases} \tag{4.7}$$

in which the superscript m is an index that denotes the m-th 3L-ANPC cell. In essence, equations (4.6) and (4.7) reproduce the C_1 and C_2 capacitor currents coming from the PM-ANPC converter as functions of the measured leg currents and the insertion factors defined in Table 4.1.

The single current source on the right-hand side of the circuit, labelled I_{dc}, is simply the measurement of the current coming in from the DC side of the circuit and into the controlled voltage source V_{dc}. The voltage of the latter is the sum of the measurements of V_{C1} and V_{C2}. This arrangement allows to have a DC link that is electrically decoupled from both the AC converter side and from the DC side. In addition, the DC side could either be a load in the case of rectifier operation or any kind of voltage source in the case of inverter operation. This means that this model is suitable to simulate the bidirectional power flow of a battery charger based on the PM-ANPC converter.

Finally, one drawback to the decoupled DC link is the need to employ a step delay in the measurements of V_{C1} and V_{C2}. This delay is required in simulation in order to break the algebraic

loop that arises from the fact that the values of V_{C1} and V_{C2} are calculated from the measurements of the currents I_1, I_2, I_{dc}, and vice-versa. While it is not always significant, such a delay results in a small error in the values involved in the algebraic loop.

4.3.2 Further Simplification of the DC Link Model

One way to deal with the measurement step delay error is to further simplify the decoupled DC link model. Indeed, it is possible to eliminate the capacitors and replace them with discrete integrators, as illustrated in Fig. 4.6, where the blocks labelled AB2(z) are discrete integrators that are discussed later in this section.

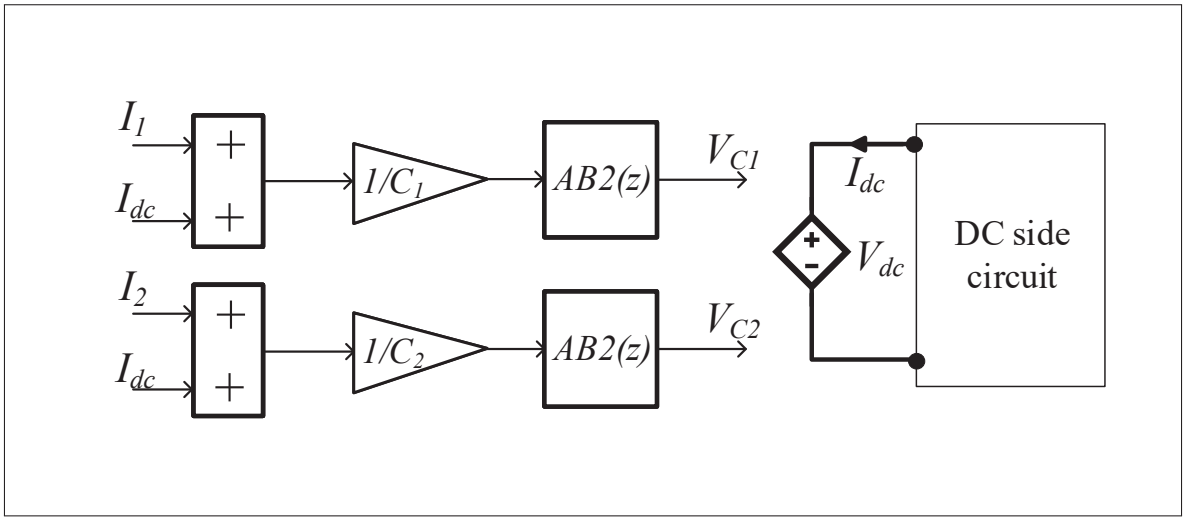

Figure 4.6 Diagram of the simplified decoupled DC link

Each discrete integrator takes a sum of currents as inputs. The currents I_1 and I_2 are the currents coming from the converter to capacitors C_1 and C_2 respectively and I_{dc} is the current coming form the DC side of the circuit. Input currents I_1 and I_2 are the same currents as previously defined in (4.6) and (4.7).

One important consideration when using discrete integrators is that they also may create algebraic loops. Specifically, methods such as the trapezoidal (Tustin) integrator are implicit in nature,

meaning that they require both past and present input values to compute the integral. As such, by instead employing an explicit integration method, such as the single step Forward Euler (FE) approximation, that only requires past values to compute the integral, it is possible to avoid algebraic loops (Atkinson, Han & Stewart, 2011). However, the FE integrator gives up some precision when compared to the trapezoidal method for a given time step. For these reasons, this equivalent model instead uses the second order Adams-Bashforth (AB2) discrete integrator. The AB2 integrator is an explicit linear multistep method that use one more past data point than the FE method in order to extrapolate a more accurate approximation of the integral for a given time step (Atkinson *et al.*, 2011). The following AB2 discrete transfer function is implemented in the DC link model seen in Fig. 4.6

$$AB2(z) = \frac{T_s}{2}\frac{3z-1}{z(z-1)} \tag{4.8}$$

where T_s is the computation time step.

Thus, by using discrete integrators based on the AB2 approximation and the currents I_1, I_2, I_{dc} defined previously, the capacitor voltages V_{C1} and V_{C2} can be calculated

$$V_{C1} = \frac{1}{C_1}\int_t^{t+T_s} (I_1 + I_{dc})dt \tag{4.9}$$

$$V_{C2} = \frac{1}{C_2}\int_t^{t+T_s} (I_2 + I_{dc})dt. \tag{4.10}$$

By employing this integrator method, the model is simplified by not requiring actual capacitors in the circuit and the accuracy is maintained even at larger time steps. More importantly, the voltages calculated from (4.9) and (4.10) can be sent directly to the 3L-ANPC cells and to the V_{dc} controlled source without any additional step delays, thus reducing the risk for delay propagation errors.

4.4 Comparison of Offline and Real-Time Simulation Results

The proposed equivalent model is validated in this section by comparing the simulation results of the reference SimPowerSystems (SPS) model with those of the proposed model. More precisely, the MOSFET and capacitor blocks from the SPS library in Simulink are used to build a three-phase PM-ANPC rectifier with a resistive load. The same circuit is reproduced also in Simulink but with the equivalent model and decoupled DC link, such that no MOSFET or capacitor blocks are employed. The simulated system is shown in Fig. 4.7. The two models are otherwise identical in terms of the circuit and simulation parameters listed in Table 4.2.

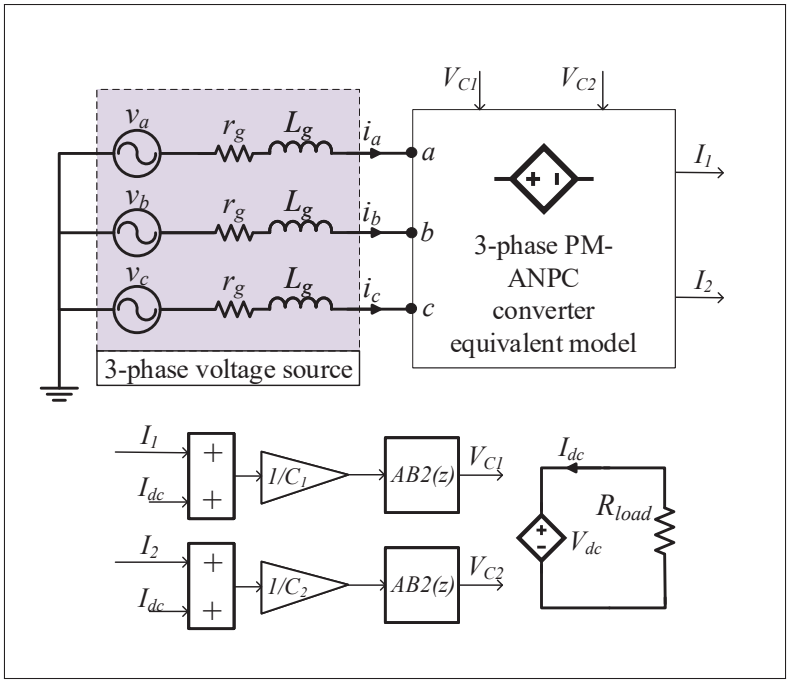

Figure 4.7 Diagram of the overall simulated system

The system described previously is simulated with a computation time step of 1 μs for the reference model (as in Chapter 3) and 10 μs for the equivalent model. By choosing a time step 10 times higher for the equivalent model, the objective is to show that accurate results can be obtained with less computations. In this test, the resistive load undergoes a 50% step change from 12Ω to 6Ω at $t = 0.05s$ to validate the dynamic performance of the proposed model.

Table 4.2 Circuit and simulation parameters

Parameter	Values
DC link voltage	$V_{dc} = 750V$
AC voltage source	$V_{ac} = 480Vrms$
Fundamental frequency	$f = 60Hz$
Switching frequency	$f_{sw} = 10kHz$
Switch ON resistance	$R_{on} = 0.001\Omega$
Leg inductor	$L_f = 800\mu H$
DC capacitor	$C_1 = C_2 = 4.6mF$
Simulation time step	$T_s = 1\mu s, 10\mu s$

In Fig. 4.8, the DC link voltages for the reference SPS model and the equivalent model are superimposed on two graphs: one that shows the entire transient response from the load step change and one that is more zoomed in during the same transition. These results demonstrate that despite the larger time step, the equivalent model can accurately track the behaviour of the reference model even during a transient event. Furthermore, the zoomed graph shows that the error between the two curves stays below 1.5V during the transient, which is less than 0.2% error with respect to the nominal value of 750V.

Similarly, Fig. 4.9 shows the comparison of the AC line currents and the converter output line-to-line voltages for both models during the transient. These waveforms once again illustrate the effectiveness of the equivalent model in emulating the results of the reference model, including the 13-level output voltage. Even in the zoomed graphs, it can be seen that the error is minimal in the AC current and voltage.

Moreover, the execution times of the two models, with the simulation time set at 5s, are compared in Table 4.3 in order to validate the performance increase of the proposed equivalent model.

As expected, the equivalent model running at 10 μs offers considerably faster simulation performance than the reference SPS model. Specifically, the execution time of the equivalent model is almost 10 times faster than the reference model. Furthermore, it should be noted that

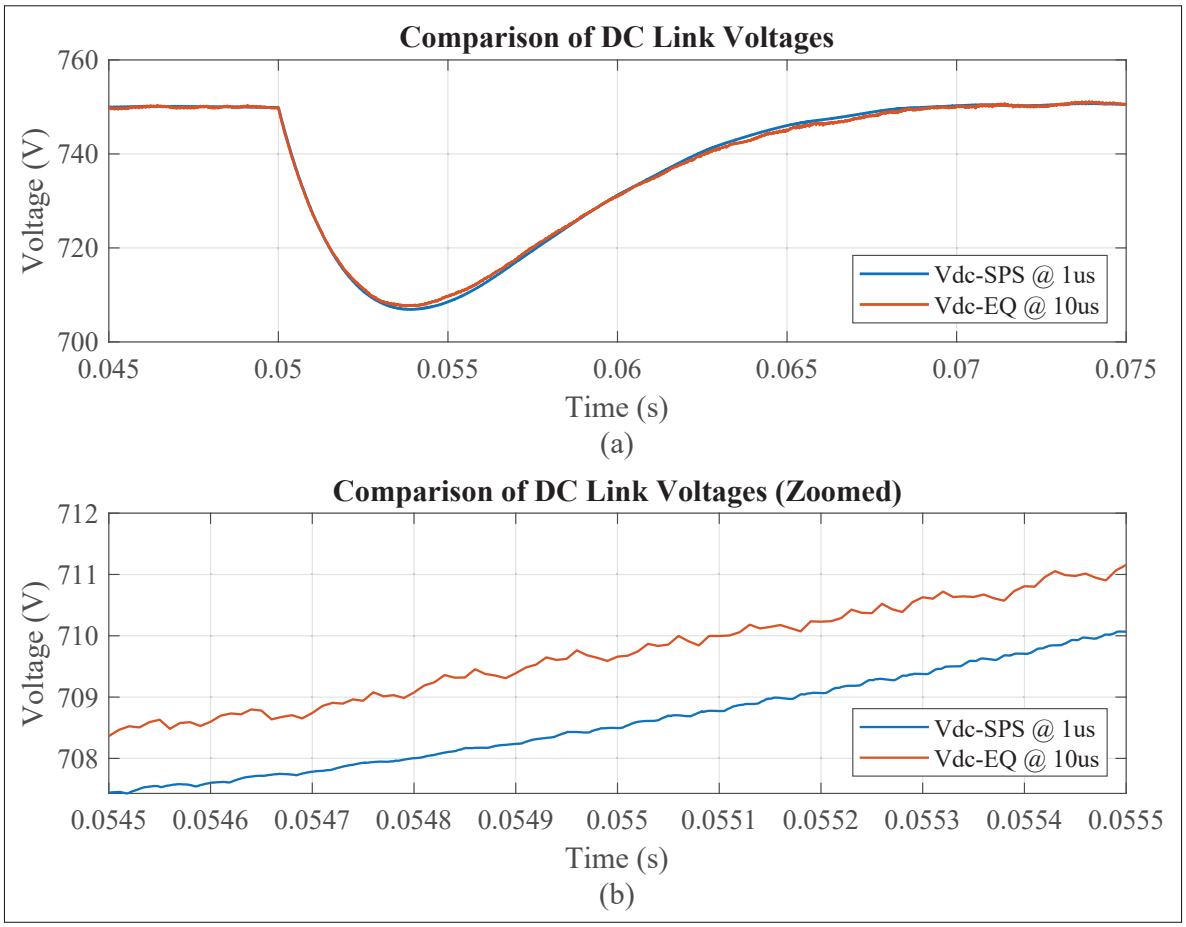

Figure 4.8 Comparison of DC voltages: (a) during transient response and (b) zoomed in

using a larger time step in the reference model might produce faster simulations, but the accuracy of the results would be sacrificed. Besides, the equivalent model offers other advantages in terms of increased simulation stability since the model is completely linear. This means that unlike the reference SPS model that uses diodes, the proposed equivalent model generates zero non-linearities and discontinuities.

Finally, the real-time performance of the proposed equivalent model is compared against the reference model in RT-LAB software running on the OP4510 simulator. This comparison is also shown in Table 4.3. The results show what is the minimum possible time step that the model can achieve without any overruns, which are a measure of the amount of operations that are not completed before the next computation step.

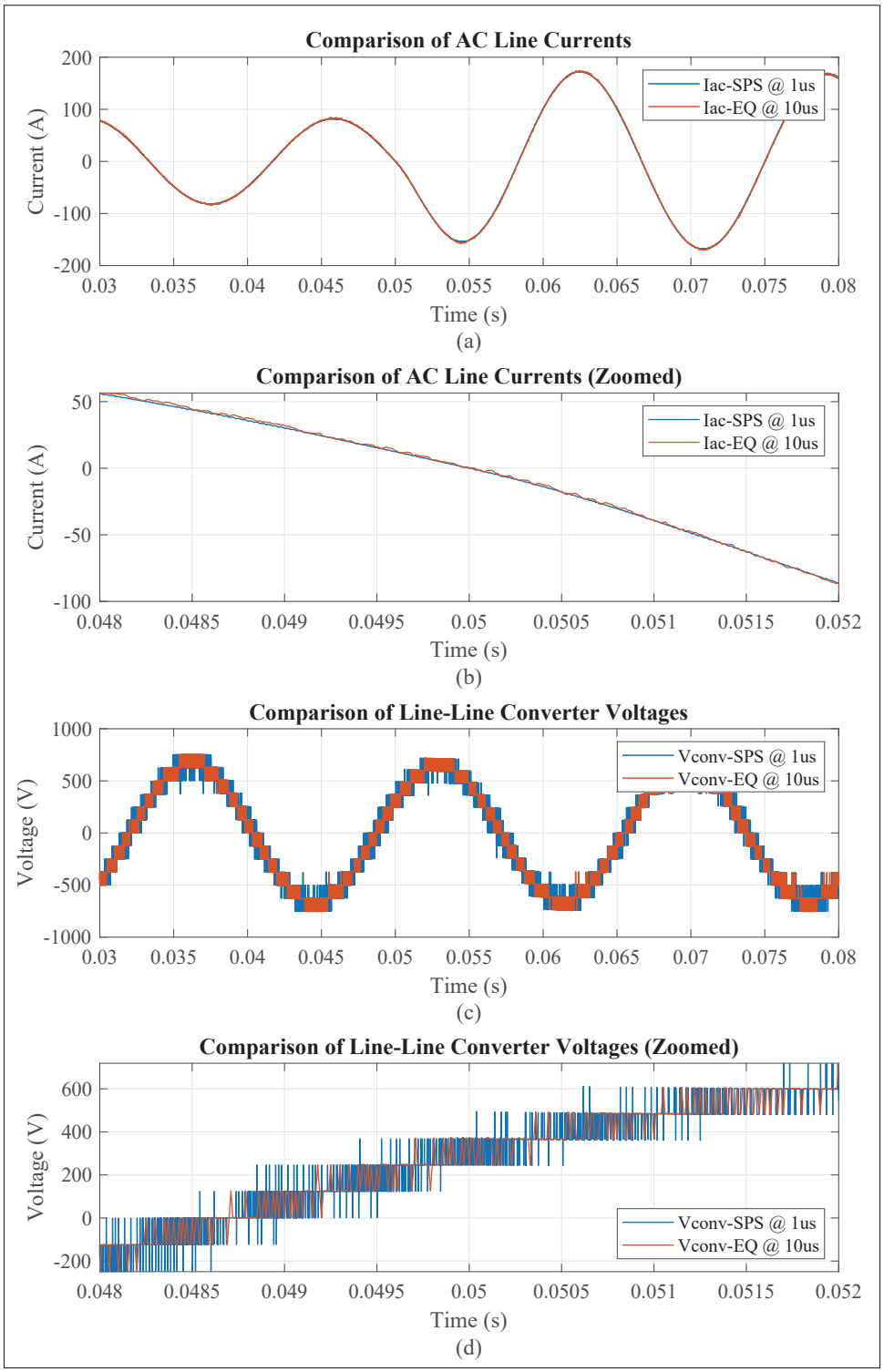

Figure 4.9 Comparison of AC measurements: (a) AC line current, (b) zoomed in AC line current, (c) line-to-line converter voltage and (d) zoomed in converter voltage

Table 4.3 Comparison of execution times and RT performance between the reference and equivalent models

Measurement	**Ref. (1 us)**	**Eq. (10 us)**
Offline execution time	344.7 s	34.7 s
Acceleration factor	n/a	9.93
Minimum RT time step	>50 μs	6μs

Accordingly, the equivalent model can run in real-time at a time step of 6 μs with zero overruns, whereas the reference SPS model still produces many overruns at 50 μs, which is already many times greater than the 1 μs required for accurate results. This is a significant advantage for the equivalent model because this means that a single CPU core with a 50 μs time step would be capable of simulating eight converters in real-time.

Hence, the proposed equivalent model with decoupled DC link is demonstrated to accurately reproduce the behaviour of the reference model while offering increased offline and real-time simulation performance despite having a larger computation time step.

4.5 Conclusion

The equivalent model of the PM-ANPC converter with decoupled DC link was proposed and validated in this paper. The model replaces active power electronic switches with an arrangement of controlled voltage sources determined by switching functions. Moreover, the proposed DC link of the equivalent model is simplified and electrically decoupled from the rest of the circuit. This implementation allows to maintain accurate results and to minimize simulation errors due to the delays in the measurements. The equivalent model and the reference SPS model were both implemented in Simulink to validate the accuracy of the proposed model and to compare their performance in both offline and real-time simulations. The simulation results verified the accuracy and improved performance of the proposed equivalent model despite running at a larger computation time step.

CONCLUSION AND RECOMMENDATIONS

The landscape of transportation is rapidly transitioning to a more electrified fleet of vehicles. Such a change requires fast and reliable charging infrastructures to be available in large quantities. Moreover, the potential for electric vehicle batteries to become energy storage devices on the grid means that these chargers would greatly benefit from bidirectional power flow capabilities. Therefore, this thesis aimed to study and model bidirectional battery chargers. More precisely, research was done on the modelling and of multilevel converters as battery chargers and on their equivalent models for real-time simulation applications.

Firstly, a literature review was presented in order to illustrate the benefits and drawbacks of the current AC-DC converter topologies used in battery chargers. In addition, a review of some of the more popular multilevel converter topologies, such as the CHB, ANPC and PUC, was done so as to compare them to the more conventional 3-level converters. In summary, it was determined that the higher number of output voltage levels of multilevel converters made them a more attractive solution for grid-connected battery chargers as they considerably help to reduce the AC current filtering requirements. Furthermore, the literature review also provided a brief overview of real-time simulation and how it can benefit the study of large and complex electrical systems. Hence, it was shown that developing appropriate equivalent models of the multilevel converters can enhance the performance of real-time simulation and thus helps in expanding the scope of the studies that can be done using real-time simulators.

In the second chapter, a multilevel converter topology named the 23-level Hybrid-PUC was proposed along with its associated model predictive control (MPC) method. The proposed single-phase converter is capable of generating a high number of output voltage levels with a reduced number of total components. Also, a simple equivalent model of the converter was developed and implemented in real-time simulation. Furthermore, the MPC method allowed to accurately track multiple DC voltage references while still keeping the AC current well regulated.

This resulted in a converter that has good steady-state and dynamic performance and also good power quality thanks to its 23 output voltage levels.

Then, in an effort to develop a bidirectional battery charger based on a three-phase topology, the 13-level PM-ANPC three-phase converter was studied and a deadbeat predictive controller (DPC) was developed for bidirectional power flow operation. The PM-ANPC's high power density and inherent harmonic mitigation performance made it a very interesting topology for battery chargers. In addition, the proposed DPC method was able to keep some of the advantages of the MPC while still being able to operate at a fixed switching frequency. It was demonstrated that the proposed controller is capable of accurately tracking the battery power reference in either charging or discharging modes of operation. Moreover, despite generating fewer voltage levels than the 23-level H-PUC, the PM-ANPC's 13 levels are still enough to considerable improve the the power quality of the converter.

Finally, a more detailed equivalent model of the PM-ANPC converter with a decoupled DC link was proposed. By replacing the semiconductor switch models with controlled voltage sources based on switching functions, true real-time simulation could be achieved. Additionally, the proposed model presented a decoupled DC link capacitor representation that uses discrete integrators. This combination helped in making the equivalent model accurate with respect to the reference model while greatly improving the simulation performance, which was validated using the OP4510 real-time simulator.

While this thesis focused on the development of multilevel converter equivalent models, it remains relevant to consider some recommendations for potential future works. One aspect that could be expanded upon is the flexibility of the PM-ANPC equivalent model. Indeed, the proposed model was validated for the insert and bypass modes only, and lacks the ability to properly emulate the blocking mode. As such, it would be beneficial to further expand the model to include the capability to emulate all modes of operation. Then, another potential future

work would be a more practical application of the aforementioned equivalent model. More specifically, it would be interesting to implement a hardware-in-the-loop system with a real controller and a simulator running a system composed of multiple battery chargers on the same grid connection. This type of more in-depth study would help in further demonstrating the practicality of real-time simulation.

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