Measurement techniques to characterize SiC, GaN, and Si power MOSFETs for transportation applications

by

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FOREWORD

This document presents the work that I carried out as part of my master's studies at École de technologie supérieure between May 2019 and April 2021. The main objective of this research work is to conduct a comparative study on emerging Wide Bandgap (WBG) MOSFETs technologies in energy conversion applications. Although the guideline has been retained, the multiple challenges of reproducing simulation results by experimentation led to paying particular attention to methods of extracting experimental data. Most of the time not enough attention is given to establishing an experimental data extraction methodology which lead to unexpected perturbations, false observations, and inaccurate conclusions.

ACKNOWLEDGEMENTS

First of all, I would like to thank my thesis director, Professor Handy Fortin Blanchette from the Department of Electrical Engineering at École de technologie supérieure. It is the passion of Professor Fortin Blanchette that made me want to pursue graduate studies. His dedication, both personally and professionally, is a real source of inspiration for me. I would also like to thank my co-supervisor, Professor Amin Ghazanfari from Hydro-Québec's Center of Excellence in Transportation Electrification and Energy Storage (CETEES). Dr. Ghazanfari has always been altruistic, providing technical support as well as personal support. His dedication to science, to sharing knowledge, and his involvement in making energies cleaner are exemplary behaviors to adopt. I would like to thank them both for their support, advice and confidence in carrying out this project.

Thanks go to Mr. Christian Perreault, Head of Expertise and Systems at CETEES. Without his confidence and financial support to carry out this project, none of this would have been possible. The initiative of the Mitacs organization also deserves thanks and mention for supporting innovation by granting research partnerships, advice and funding.

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Simulation et expérimentation des caractéristiques des semi-conducteurs de puissance Si, SiC et GaN dans les applications de conversion de l'énergie

Yan Bérubé

RÉSUMÉ

Les semiconducteurs à large bande (WBG) ont le potentiel de franchir les barrières qui limitent l'adoption à grande échelle des véhicules électriques (VE). Les WBG améliorent la densité de puissance et permettent aux circuits électroniques de puissance (PE) d'atteindre des points de fonctionnement et une efficacité au-delà de ce que le Silicium (Si) standard peut offrir. Actuellement, les semiconducteurs WBG à base de Carbure de Silicium (SiC) et Nitrure de Gallium (GaN) sont les candidats les plus viables pour remplacer les semiconducteurs Si. Pour l'instant, la littérature apporte encore de la confusion lorsqu'il s'agit de choisir entre les SiCs et les GaNs pour tirer le meilleur parti des applications des convertisseurs d'énergie. Afin de faire pencher la balance face à ce débat, cette thèse présente une analyse comparative par simulation et expérimentation entre les MOSFETs Si, SiC et GaN dans les applications de conversion d'énergie.

Une revue des équations de simulation basées sur les paramètres intrinsèques du modèle mathématique équivalent du MOSFET expose les hypothèses, limites et possibilités d'améliorations du modèle de calcul. Ensuite, la simulation de multiples conditions expérimentales révèle des résultats de commutations favorables envers les SiCs tout en mettant en évidence les avantages marqués de cette technologie à haute température. Bien que les résultats de simulation soient prometteurs, la validation expérimentale reste nécessaire pour tirer des conclusions finales sur les observations. Dans cette optique, la conformité des hypothèses théoriques est satisfaite à des fins de comparaison entre les résultats de simulation et d'expérimentation. L'analyse des méthodologies d'extraction de données expérimentales met en évidence l'importance des perturbations des inductances parasites, capacités parasites, du couplage mutuel et des interférences électromagnétiques (EMI) sur le processus de commutation et de prise de mesures. De cela, une méthodologie d'extraction de tension et de courant est proposée pour minimiser les perturbations sur les mesures expérimentales et processus de commutation. Enfin, la comparaison relative des résultats expérimentaux montre les grandes tendances de chaque technologie par le biais de l'analyse statistique. Leur interprétation fait le pont avec les paramètres intrinsèques des MOSFETs.

Mots-clés: Wide Bandgap (WBG), semiconducteur de puissance, Carbure de silicium (SiC), Nitrure de gallium (GaN), électronique de puissance (PE), véhicules électriques (VE), modélisation, mesures expérimentales

Measurement techniques to characterize SiC, GaN, and Si power MOSFETs for transportation applications

Yan Bérubé

ABSTRACT

Wide Bandgap (WBG) semiconductors have the potential to cross the barriers that limit the widespread adoption of power electronics (PE) circuits in various energy conversion applications. The WBG devices improve power density and allow PE circuits to reach operating points and efficiency beyond what standard Silicon (Si) can offer. Currently, Silicon Carbide (SiC) and Gallium Nitride (GaN) are the most viable WBG semiconductor candidates to replace Si-based devices. For now, the state-of-the-art technologies still bring confusion when it comes to choosing between SiCs and GaNs to get the most benefits of them for power converter applications. To tilt the balance in the face of this debate, this thesis presents a comprehensive comparative computation and experimental analysis among Si, SiC, and GaN MOSFETs in energy conversion applications.

A presentation of simulation equations based on intrinsic parameters of MOSFET's equivalent mathematical model highlights the assumptions, limitations, and opportunities for improvement of the computational model. Then, simulation of multiple experimental conditions reveals favorable switching results towards SiCs while highlighting the marked advantages of this technology at high temperature. Although the simulation results are promising, the experimental validation remains necessary to make the concluding remarks. Analysis of experimental data extraction methodologies highlights the perturbation from parasitic inductances, parasitic capacitances, mutual coupling, and electromagnetic interference (EMI) on the switching process and measurements. Based on the detailed assessment of parasitic perturbations, this work proposes a voltage and current extraction methodology to remarkably minimize disturbances on measurements and the switching process. Finally, interpretation of experimental results through statistical analysis of relative comparison presents major trends from each technology while providing an interpretation of observations based on intrinsic parameters.

Keywords: Wide Bandgap (WBG), power semiconductor, Silicon Carbide (SiC), Gallium Nitride (GaN), power electronic (PE), electric vehicles (EVs), modelization, experimental measurements

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LIST OF ABBREVIATIONS

2DEG	Two-Dimensional Electron Gas
APE	Automotive Power Electronic
APEEM	Advanced Power Electronics and Electric Motors
ARPA-E	Advanced Research Projects Agency-Energy
BJT	Bipolar Junction Transistor
BNC	Bayonet Neill-Concelman
CETEES	Center of Excellence in Transportation Electrification and Energy Storage
CMRR	Common-Mode Rejection Ratio
DC	Direct Current
DOD	Department of Defense
DOE	Department of Energy
EDV	Electric Drive Vehicle
EMI	Electromagnetic Interference
EV	Electric Vehicle
FE	Field-Effect
FET	Field-Effect Transistor
GaN	Gallium Nitride
GPI	GaNPower International
HEMT	High Electron Mobility Transistor

HEV	Hybrid Electric Vehicle
HS-EC	High Side Estimated Current
HV	High Voltage
IAPG	Interagency Advanced Power Group
ICE	Internal Combustion Engine
IECON	Industrial Electronics, Control, and Instrumentation Conference
IEEE	Institute of Electrical and Electronics Engineers
IGBT	Insulated-Gate Bipolar Transistor
JEDEC	Joint Electron Device Engineering Council
JFET	Junction-Gate Field-Effect Transistor
LS-VDS	Low Side Drain-Source Voltage
LV	Low Voltage
MKP	Metallized Polypropylene
MOSFET	Metal-Oxide-Semiconductor Field-Effect Transistor
NEDO	New Energy and Industrial Technology Development Organization
NMI	National Network for Manufacturing Innovation
OBC	On-Board Charger
OEM	Original Equipment Manufacturer
ORNL	Oak Ridge National Laboratory
PCB	Printed Circuit Board

PE	Power Electronic
PHEV	Plug-In Hybrid Electric Vehicle
PWM	Pulse-Width Modulation
RMS	Root Mean Square
Si	Silicon
SiC	Silicon Carbide
SMA	SubMiniature A
SNR	Signal-To-Noise-Ratio
TSMC	Taiwan Semiconductor Manufacturing Company
TTL	Transistor-Transistor Logic
UCS	Union of Concerned Scientists
VDMOS	Vertical Double-Diffused MOS
VE	Véhicule Électrique
VTO	Vehicle Technologies Office
VVMOS	Vertical V-groove MOSFET
WBG	Wide Bandgap

LIST OF SYMBOLS AND UNITS OF MEASUREMENTS

A	Ampere
°C	Degree Celsius
Hz	Hertz
J	Joule
Ω	Ohm
pu	Per-unit
V	Volt
W	Watt
Wh	Watt-Hour

INTRODUCTION

New emerging Wide Bandgap (WBG) MOSFETs technologies are increasingly analyzed using experimental and simulation studies. Although the simulation remains generally well defined to compare MOSFET's semiconductors, the experiments generally show much less rigor in terms of methodology which can lead to large disparities in conclusions and raise a global debate for choosing among WBG semiconductors. Choosing an appropriate experimental measurement technique can be a challenging topic, and depending on the applied technique, the experimental results may significantly defer from simulation results. Tiny details such as mutual coupling can generate great influences on the results, which is why it is necessary to develop a rigorous experimental measurement methodology. This condition can be even more crucial when comparing semiconductors with different internal characteristics because experimental measurements are very sensitive to parasitic elements in power converter applications. To settle this unprecedented debate between WBG and Si MOSFETs in power converter applications, a detailed analysis by simulation and experimentation is required. Particular attention is paid to analyze the best practices in the industry and propose new effective measurement technique to minimize perturbations on the switching behavior. This thesis is organized as follows:

Chapter 1 highlights the great importance of introducing the WBG MOSFETs for power converter applications, particularly on electric mobility. This literature review presents the current state of Si, SiC, and GaN MOSFET's semiconductor on the market, the need to orient future development towards more efficient technologies, and the benefits of each technology. This also highlight the great debate between GaN, SiC, and standard Si MOSFET under PE applications.

Chapter 2 presents the chosen modeling approach based on intrinsic characteristics of MOSFET's structure as defined in the literature. Partial development of computational equations highlights the assumptions and limitations of the modeling approach while improving the modeling accuracy.

Chapter 3 defines the experimental configuration and selected Si, SiC and GaN MOSFET of similar characteristics for comparison purpose. Then, computational results based on the modeling approach of Chapter 2 gives early remarks on Si, SiC, and GaN MOSFETs in a half-bridge power converter application.

In Chapter 4, the disturbances of taking measurements in energy conversion applications is presented, outlining the importance to develop a method of carefully extracting experimental data. Then, a comparison method between MOSFETs is defined due to difference in internal characteristics between technologies. In addition, several switching current extraction methodologies are developed and analyzed. In the end, a comparative measurement methodology is defined to take experimental results between Si, SiC, and GaN MOSFETs while minimizing disturbances on measurements and the switching process.

Finally, Chapter 5 presents the interdependency of established measurements points with internal characteristics of MOSFETs. In total, experimental switching waveforms of MOSFETs are analyzed under four distinct configurations in a half-bridge hard commutation test circuit. Statistical analysis and interpretation of relative comparison highlight major trend in the switching process for Si, SiC, and GaN MOSFETs.

CHAPTER 1

RECENT ADVANCES IN WIDE BANDGAP DEVICES FOR AUTOMOTIVE INDUSTRY

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Currently, there is a big debate to know which Wide Bandgap (WBG) technology will dominate the power semiconductor market for power converters and electric vehicle applications. It is necessary to start with an in-depth literature review to take the pulse of this question. Also, it is essential to shed the light on the reasons for the appearance of WBG devices on the market. This paper presented in the 46th Annual Conference of the IEEE Industrial Electronics Society contains main remarks to draw a basic understanding of the state-of-the-art of WBG semiconductors, particularly for the automotive industry. A presentation of the benefits for each WBG technology, as well as an overview of the current availability of these technologies makes it possible to demonstrate the current state of the art of WBGs. Finally, challenges in design integration, actual innovations, and development partnerships on WBGs open the door to future applications and possibilities.

1.1 Overview

The main barriers in the widespread adoption of electric vehicles (EVs) include limited autonomy, high upfront cost, low availability of charging infrastructure, and long charging time. Wide Bandgap (WBG) semiconductors are key industry players in the electronics circuit design because they are advantageous in terms of high operating temperature, high efficiency, low volume and weight. The WBG devices improve power density and allow power electronics (PE) circuits to reach operating points and temperatures that have not been considered before. Currently, SiC and GaN are the most viable WBG semiconductor candidates to replace Si-based devices. However, cost, packaging limitations, reliability, safety, low manufacturing, and demand level of WBGs are issues that should be addressed; the integration of these devices into the automotive power electronic (APE) systems can then successfully be realized. This paper presents an industrial oriented overview of WBG power semiconductors including their advantages, recent progress, challenges, and development partnerships.

1.1.1 Introduction

The global demand for energy continues to grow due to the economic and population growth. The worldwide primary energy consumption by sources and energy use per capita is demonstrated in Fig 1.1. The increase in GHG emissions is one of the main challenges of the growing global energy demand (Das, Marlino & Armstrong, 2018). Most governments have been actively engaged in the fight against climate change by reducing GHG emissions and oil dependence (Natural Resources Canada, 2016). Because a large proportion of GHG emissions is released by the transportation sector, transportation electrification can significantly contribute in mitigating climate change (STMicroelectronics, 2019b; Transports Québec, 2020). In 2017, the transportation sector accounted for over 29% of GHG emissions in the United States (United States Environmental Protection Agency, 2020) and 24% of the total CO_2 emissions globally (International Energy Agency, 2019a). Fig. 1.2 presents the percentage of CO_2 emissions from fuel combustion by different sectors and evolution of worldwide CO_2 emissions from 1990 to 2017.

Even in coal-intensive electricity generation, electric vehicles (EVs) are cleaner than the most efficient conventional internal combustion engine (ICE) vehicles (Hausfather, 2019; Hodges, 2019; Reichmuth, 2020). Moreover, because grid decarbonization occurs globally, the footprints of EVs will continue to decrease (Hausfather, 2019; Hodges, 2019; Reichmuth, 2020). According to the Union of Concerned Scientists (UCS), consumers can further decrease their footprints by opting for the most efficient EV in the market (Reichmuth, 2020). Given its benefits for the environment and energy consumption, efforts in technological designs translate into higher power density and efficiency requirements (Bartolomeo, Abbatelli, Macauda, Giovanni, Catalisano, Ryzek & Kohout, 2016). For manufacturers, these benefits can result in the use of more energy-efficient components, topologies, and energy management techniques (Bartolomeo *et al.*, 2016).

According to Bloomberg New Energy Finance (Shankleman, 2017), sales of EVs would exceed those of ICE vehicles by 2038. The limited autonomy, high cost, low availability of charging

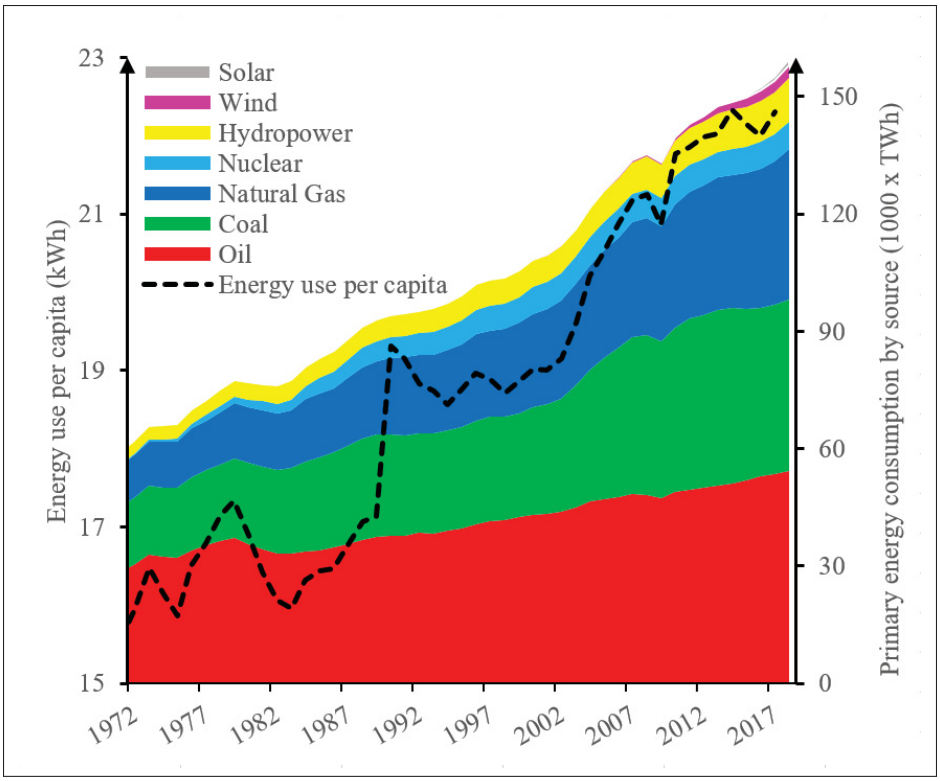

Figure 1.1 Global annual energy consumption by source (TWh) and average annual energy use per capita (kWh)
Adapted from Ritchie & Roser (2014); International Energy Agency (2019b)

infrastructure, and long charging time are barriers in the widespread adoption of EVs, and these limitations compel car manufacturers to invest in R&D (Szymkowski, 2019). Wide Bandgap (WBG) semiconductors can improve the electrification of the transport sector because they are advantageous in terms of their operating temperatures, voltages, and maximum powers. These semiconductors can significantly increase the efficiency of electrical power systems by reducing the losses, dimensions, and weights of vehicles (Das *et al.*, 2018; Bartolomeo *et al.*, 2016; Matthews, 2019).

The objective of this study was to clarify the effect of WBG semiconductors on the automotive industry, specifically Silicon Carbide (SiC) and Gallium Nitride (GaN). This study also aimed to determine the state of WBG in the transport sector. The remainder of this paper is organized as follows. Section 1.1.2 discussed the reasons that led to the development of WBG technologies.

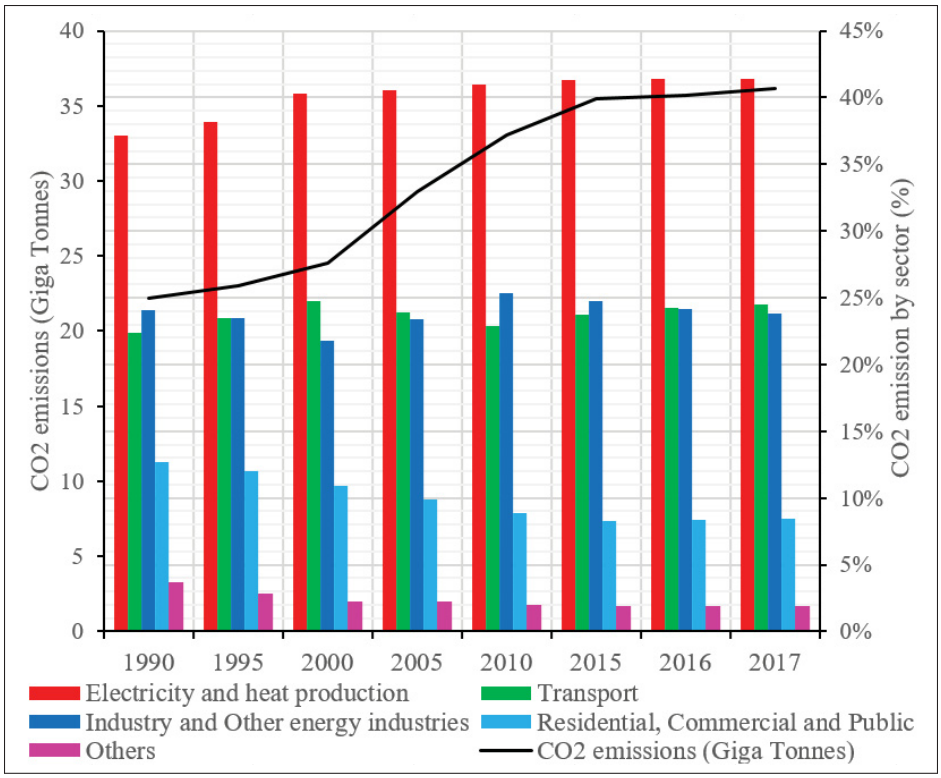

Figure 1.2 Percentage of global CO_2 emissions from fuel combustion by sectors from 1990 to 2017 (%) and annual CO_2 emissions from 1990 to 2017 (Giga tonnes per year)
Adapted from International Energy Agency (2019a); Ritchie & Roser (2017)

In section 1.1.3, the benefits and classification of WBG semiconductors based on intrinsic characteristics of commercially available devices, respectively, were discussed. Then, the advantages and challenges of the integration of WBG semiconductors into the automotive industry are presented in sections 1.1.4 and 1.1.5. Section 1.2 presents the industrial partnerships and prospects of WBG semiconductors. Finally, section 1.3 concludes the main remarks.

1.1.2 Why WBGs?

Investing in new power semiconductors is required to achieve higher efficiency. Power MOSFETs appeared approximately 30 years ago on the market. Overtime, many improvements have been achieved, and the fabrication of silicon (Si) MOSFETs is currently close to its theoretical limits

(Baliga, 2008; Lidow, Strydom, de Rooij & Reusch, 2015). The theoretical specific on-resistance of Si MOSFETs is almost attained, and the performance improvement of the Si-based IGBTs is approaching its limit. The theoretical on-resistance versus blocking voltage capability of Si and WBGs are shown in Fig 1.3 The Si semiconductors lack the capability to efficiently operate in high temperatures and high range of voltage and power. These limitations are pushing manufacturers to look for new solutions such as WBG materials (Baliga, 2008; Lidow, 2011; Lidow *et al.*, 2015; NIKKEI XTECH, 2012). Specifically, WBG semiconductors are great sources of investigation in the automotive sector to support electric mobility.

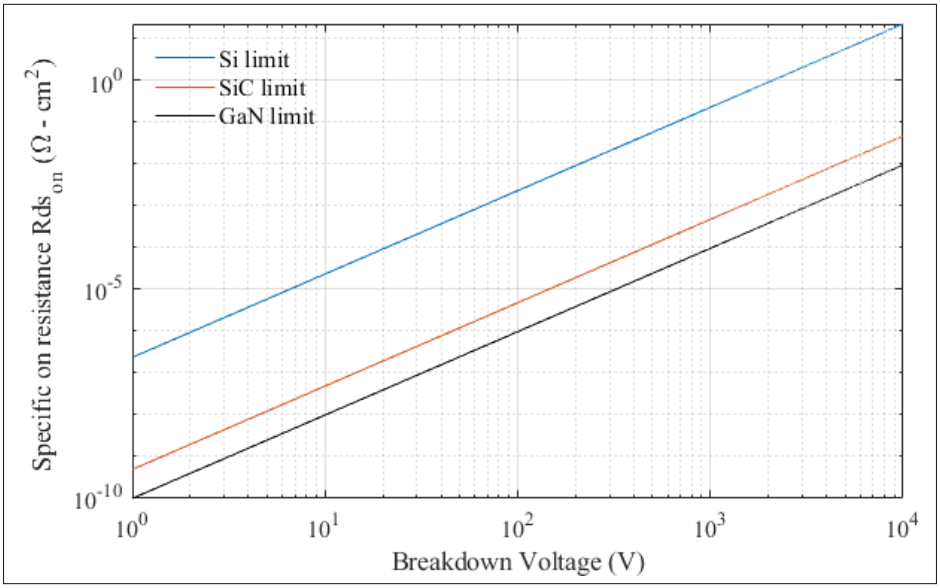

Figure 1.3 Theoretical on-state resistance versus blocking voltage capabilities of Si, SiC and GaN
Adapted from Baliga (2008); Lidow *et al.* (2015)

1.1.3 Benefits of WBG semiconductors

The introduction of WBG semiconductors into the power electronics conversion topologies can significantly reduce power losses (Das *et al.*, 2018; Ghazanfari, Perreault & Zaghib, 2019). SiC and GaN are two of the most popular WBGs that offer different advantages compared to that of the standard Si technology. These advantages allow manufacturers to achieve a performance level that cannot be achieved by the Si technology. From a general overview, WBGs allow operations

at higher voltage and current while reliably withstanding high temperatures (Ghazanfari *et al.*, 2019; Charged EVs, 2017). The higher capabilities of WBG semiconductors helps to track key efficiency objectives.

There are different expectations regarding the improved performance, reliability, efficiency, and cost of the WBG materials in all switching applications. However, the introduction of WBGs to the market does not mean the end of well-established Si semiconductors. Although WBGs are necessary to improve efficiency, each semiconductor technology has its own advantages depending on the application. A summary of typical ratings of commercially available Si and WBG semiconductors is shown in Fig. 1.4.

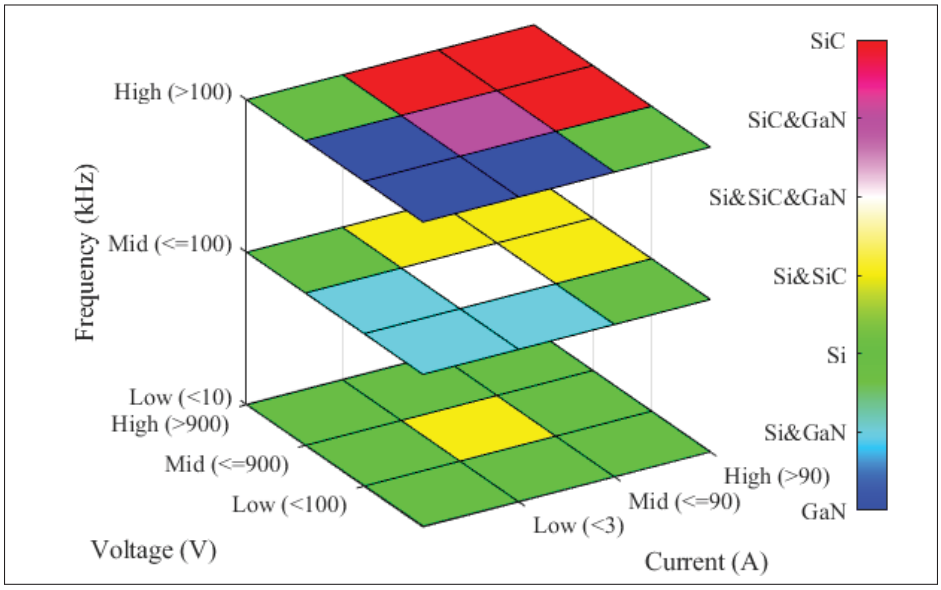

Figure 1.4 Summary of typical ratings of commercially available Si and WBG semiconductors

GaN has similar features with SiC such as low conduction losses, low switching losses, and high voltage carrying capacity. Similar to SiC, GaN also offers some advantages in system and design levels (Di Paolo Emilio, 2019; STMicroelectronics, 2019a). However, GaN is rarely used by manufacturers in energy conversion applications because of its lack of maturity (Matthews, 2019). Specifically, most GaNs are lateral devices on Si substrates because of their low cost and availability. Thus, large current capabilities require large area devices and result in low-voltage

capabilities and poor thermal handling (Das *et al.*, 2018). The vertical GaN has a theoretical potential for higher breakdown voltages, but it requires a GaN substrate which is less mature than the standard Si or SiC and is expensive (Das *et al.*, 2018). To avoid the high cost of the GaN substrate, there has been a global effort to grow vertical GaN on Si substrates (Hu, Zhang, Sun, Piedra, Chowdhury & Palacios, 2018). However, because of the lattice constant and thermal expansion mismatches between GaN and Si, the process of vertical high-voltage GaN devices is a challenge (Hu *et al.*, 2018). Currently, GaN is not mature enough for high-power applications because of its limited thermal and voltage handling capabilities. Nonetheless, GaN has a higher value of electron saturation velocity which gives it favorable characteristics for fast switching applications such as audio amplifiers and miniaturized switched-mode power supplies (Bartolomeo *et al.*, 2016). The poor thermal capability and limited power of GaN make it suited for low to mid power applications at mid to high frequency. According to Wolfspeed, although GaN may not be a great fit for EV powertrain inverter applications, it is most appropriate in applications starting at approximately 40 to 600 V. The limitation comes from the way the technology was built, and it requires bigger chips to support high current, which results in a higher cost and larger package size. Accordingly, GaNs are barely available at 900 V as cascode devices (Das *et al.*, 2018; Charged EVs, 2017).

On the other hand, the presence of SiC in the low voltage and power market is limited and does not offer competitive properties compared to that of Si and GaN devices. However, SiC have excellent thermal, voltage, power, and speed capabilities, which makes it suited for mid to high voltage, power, and frequency applications. SiC is currently more mature, which makes it the preferred WBG semiconductor for power electronic applications (Das *et al.*, 2018). According to Wolfspeed, SiC provides more efficient power conversion, and there is a growing market for it in the form of legislation, consumer demand, and energy cost (Charged EVs, 2017).

Finally, Si devices offer competitive proprieties for low frequencies, mid voltages, and power applications. Moreover, specific application requirements such as high voltage and low current or low voltage and high current are not covered by WBG semiconductors, giving exclusivity to the standard Si devices.

It is evident that high frequency and power applications and high frequency and low-power applications are favored by SiC and GaN devices, respectively. However, in the middle range of voltage, current, power, and frequency, the most suited technology depends on the specific requirements of the application. The ratings of the SiC and GaN devices for middle voltage and current range obtained from most distributors are shown in Fig. 1.5 (>100V to ≤900V & >3A to ≤90A). Because there were no WBG field-effect transistors (FETs) between 300 and 600 V, the middle range was divided into two subsections: the lower and higher voltage devices. For the lower voltage, the SiC devices have poor power and speed capabilities, making GaN dominant for that part in the middle range. However, for the 600 to 900 V, SiC offer higher voltage and twice the power capability of the GaN devices. Thus, it is evident that SiC dominates the market of the middle to high voltage, power, and frequency applications.

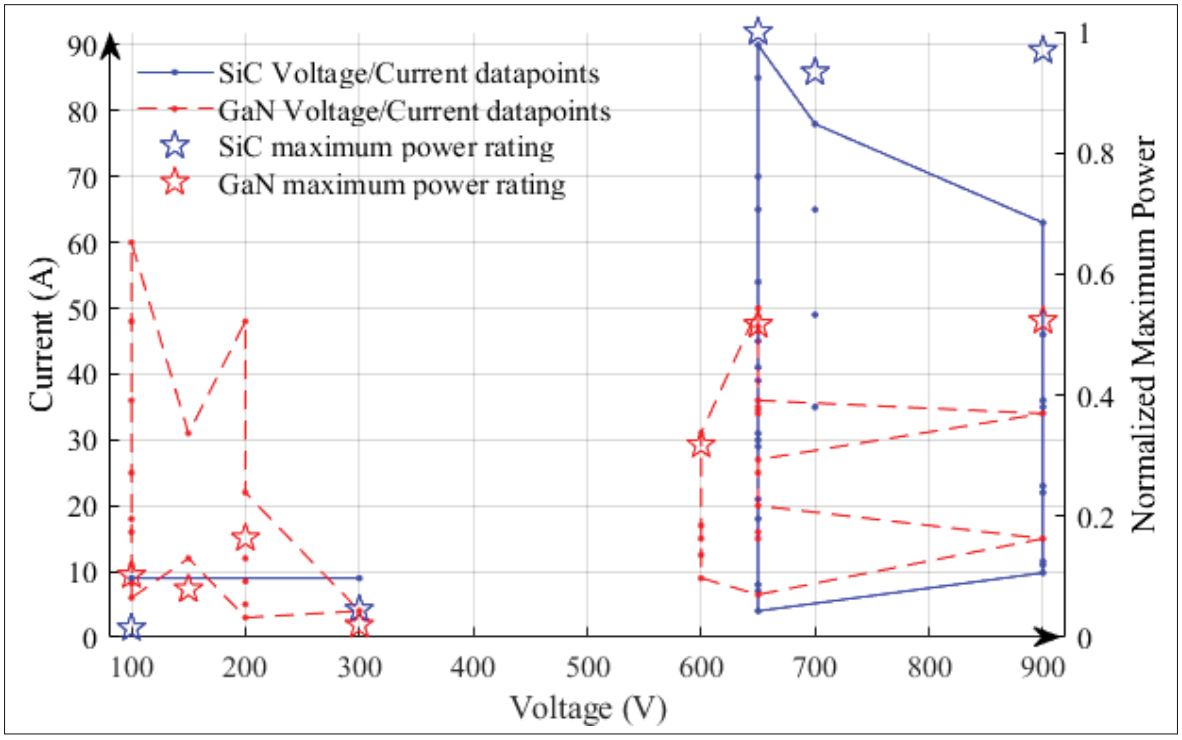

Figure 1.5 Ratings of commercially available SiC and GaN devices for middle voltage and current range (>100V to ≤900V & >3A to ≤90A) and normalized maximum power (p.u.) based on the highest power capability of the SiC device in the middle range (1 pu)

In comparison to the ratings of Si technologies, SiCs can operate at 10 times higher frequency and voltage (Das *et al.*, 2018; STMicroelectronics, 2019b; Bartolomeo *et al.*, 2016; STMicroelectronics, 2018; Bosch Media Service, 2019; NIKKEI XTECH, 2012; Charged EVs, 2017; Garrou, 2019; Hamblen, 2019; Huntley, 2019). This advantage reduces the size, weight, and cost of all the magnetic elements of converters, resulting in an overall reduction in the space, weight, and cost of designs (Das *et al.*, 2018; Bartolomeo *et al.*, 2016; NIKKEI XTECH, 2012; Charged EVs, 2017; Garrou, 2019; Huntley, 2019). Moreover, higher operating temperature (Das *et al.*, 2018; STMicroelectronics, 2019b, 2018; NIKKEI XTECH, 2012; Ghazanfari *et al.*, 2019; Garrou, 2019; Hamblen, 2019) (of up to 200 °C) (STMicroelectronics, 2018; NIKKEI XTECH, 2012) and better thermal conductivity (Bartolomeo *et al.*, 2016; Huntley, 2019) can reduce the complexity of cooling systems (Das *et al.*, 2018; NIKKEI XTECH, 2012; Garrou, 2019). This feature reduces the cost and increases durability and reliability of the systems (Els, 2018). Moreover, the smaller form factor (STMicroelectronics, 2019b, 2018; Els, 2018; Hamblen, 2019) and lower on-resistance per area (Bartolomeo *et al.*, 2016; STMicroelectronics, 2018; Els, 2018; Bosch Media Service, 2019; Huntley, 2019; ROHM CO., LTD., 2020a) of SiC respectively reduces PCB form factor (Els, 2018) and thermal losses by up to 90% (STMicroelectronics, 2018; Bosch Media Service, 2019). These advantages result in lower conduction and switching losses by a factor of 100 (Els, 2018; Huntley, 2019). According to STMicroelectronics, the variation of the on-resistance and switching losses are approximately independent of the junction temperature (Els, 2018).

1.1.4 SiC as an Enabler of Transportation Electrification

According to the Oak Ridge National Laboratory, the transportation sector can significantly benefit from the advantages of WBG; however, this potential is dependent on the future production of WBGs and its adoption by hybrid EVs (HEVs) and EV manufacturers (Das *et al.*, 2018). The innovations in EV manufacturing are strongly motivated by the need to increase autonomy and reduce energy consumption, but restrained by issues on cost and safety. SiCs can be used in the development of battery-dependent vehicles in several aspects, including the reduction of energy

losses in the conversion stages (Das *et al.*, 2018; Bartolomeo *et al.*, 2016). A summary of the main advantages of SiCs in APE systems is described in Fig. 1.6.

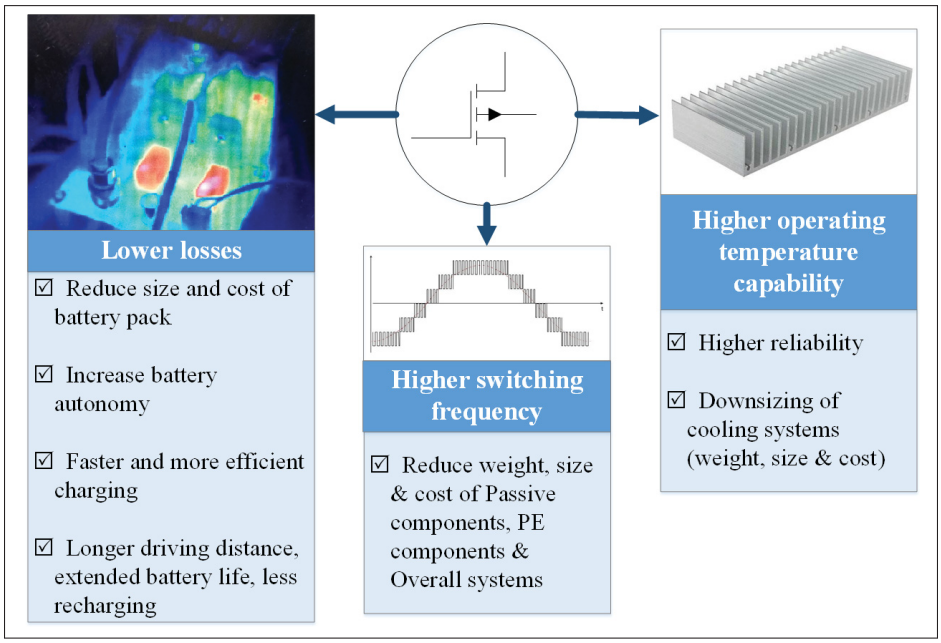

Figure 1.6 Main advantages of SiCs in APE systems

Practically, losses associated with EV traction inverter correspond to a small part of the total losses in the system. According to Wolfspeed, the associated loss accounts for approximately 7% of total losses (Charged EVs, 2017). The increase in the energy efficiency of SiC makes it possible to considerably reduce these losses to 2% of total losses (Charged EVs, 2017). Hence, it is possible to reduce the size and cost of the battery pack to achieve the same autonomy or increase it by up to 6% (Bosch Media Service, 2019) for the same battery pack (Bartolomeo *et al.*, 2016; STMicroelectronics, 2018; Cree, Inc., 2019a; Bosch Media Service, 2019; Charged EVs, 2017; Delphi Technologies, 2019; Chin, 2019; ROHM CO., LTD., 2020b). The lower losses mean longer driving ranges and less recharging, which allow the battery life to be extended (STMicroelectronics, 2018; Els, 2018; Charged EVs, 2017; Infineon Technologies AG, 2020). In addition to efficiency, SiCs contribute to other characteristics including favorable weight, size, reliability, and total system cost (Das *et al.*, 2018). Increasing the switching frequency, voltage, and operating temperature of converters are major factors in reducing the weight, dimension,

cost of passive and power electronics components, and overall systems of EVs (Das *et al.*, 2018; Els, 2018; The National Renewable Energy Laboratory, 2020; Charged EVs, 2017; ROHM CO., LTD., 2020a; Delphi Technologies, 2019; Chin, 2019; Council, 2015). Moreover, the higher voltage of EVs can significantly extend the vehicle range and reduce the charging time (ROHM CO., LTD., 2020a; Delphi Technologies, 2019; Infineon Technologies AG, 2020). Although a high switching frequency may negatively affect the efficiency of the converter, the operating point should be optimized to get the best compromise between the efficiency, weight, space, reliability, and total cost. These perspectives provide different design options and flexibility in EV layouts and battery sizes (Das *et al.*, 2018; Els, 2018; Delphi Technologies, 2019; Chin, 2019).

SiC material can operate at higher temperatures while keeping high reliability. This feature results in the reduction in size, weight, and cost of cooling systems, particularly through design simplification (Das *et al.*, 2018; Bartolomeo *et al.*, 2016; Els, 2018; Charged EVs, 2017; Council, 2015). This advantage could be beneficial to EVs through systems combination. For example, (Das *et al.*, 2018) and (Council, 2015) explained that it is possible in HEV and plug-in hybrid electric vehicle (PHEV) applications to combine the inverter and ICE cooling systems. Thus, the higher operating temperature of SiCs can reduce the traction system size and weight; however, this is not ready to be implemented because other power electronics components should also be accommodated to the higher temperature (Das *et al.*, 2018).

Altogether, the performance characteristics of SiCs is favorable for designing compact, high-power, fast, and efficient power converters such as battery chargers and inverters (STMicroelectronics, 2018; Cree, Inc., 2019a; Charged EVs, 2017; Huntley, 2019; Delphi Technologies, 2019; Chin, 2019; Infineon Technologies AG, 2020). The commercialization of SiC with enhanced performance, robustness, and reliability accelerates the transportation electrification (STMicroelectronics, 2018; Els, 2018; Cree, Inc., 2019a).

1.1.5 Challenges of WBGs integration

The main challenges of the automotive industry are reflected in the power electronics manufacturing industry. The original equipment manufacturers (OEMs) have been trying to meet the needs of the consumers and be as competitive as possible on the market. This competitiveness refers to the demand for higher efficiency and reduction in weight and volume of EV systems to increase the mileage range (Bartolomeo *et al.*, 2016). There are major changes in the design of the automotive industry to meet objectives and expectations of the consumers. Increasing the design voltages up to 1200 V, targeting the power to hundreds of kilowatts, opting for a high-temperature environment as well as enormous thermal cycling constraints, integrating complex mechatronic systems, and designing new cooling techniques and functional safety boundaries are some of the recent changes in the industry (Bartolomeo *et al.*, 2016). More importantly, it is essential to maintain an affordable cost. To keep up with all these developments, WBG power semiconductors have been investigated.

Although energy losses are lower for WBGs, using the higher form factor of SiC to increase power density with a smaller die size at a lower cost results in greater heat fluxes, higher temperatures, and higher thermal gradients in PE systems (Moreno, 2017). Thus, other components such as passive elements and soldering can potentially exceed their limits because they are exposed to a higher temperature. Therefore, there are some challenges in the thermal management and cooling systems to maintain a high level of reliability (Moreno, 2017). Excessive temperature degrades performance, lifetime, and reliability of power electronic components (MIL-217, 1991). Thus, advanced thermal management technologies are required to keep the temperature below acceptable limits, while maintaining increased power density and reduced costs related to materials, configurations, and systems. On a larger scale, advanced thermal techniques ensure reliability, increase lifespan, and can be used to develop predictive lifespan models (Narumanchi, 2017).

The high cost of WBG semiconductors is a challenge for APE manufacturers (Das *et al.*, 2018; STMicroelectronics, 2018; Charged EVs, 2017; Council, 2015; National Renewable Energy

Laboratory, 2019). In the following years, SiCs will remain more expensive than the traditional Si technology, which will slow down its adoption on a larger scale (Charged EVs, 2017; National Renewable Energy Laboratory, 2019). This is partly due to the higher cost of raw materials and difficulty of manufacturing substrates (STMicroelectronics, 2018; Charged EVs, 2017). Some new manufacturing methods result in cost reduction and consequently promote the production of WBG devices. This trend creates numerous transformations in industries that rely on high-voltage systems such as power converters (STMicroelectronics, 2018). Different power applications could benefit from the increase in efficiency from WBGs to achieve reduced costs at the system (Charged EVs, 2017). However, this cost reduction at the system level may not always be enough to address the high cost of WBG semiconductors (Das *et al.*, 2018).

The availability of WBGs is another issue caused by the low manufacturing and increased demand levels (Das *et al.*, 2018). The higher demand of SiC semiconductors resulted in the global shortage of wafers supply, which is a major challenge for both the APE and PE industries (Shao, 2019).

Reliability and safety are the major concerns of APE manufacturers. The failure of the PE systems of a vehicle could have a major impact on the safety and performance of EVs (Das *et al.*, 2018). WBGs have not yet been proved to be reliable at the level demanded by the industry (Das *et al.*, 2018). The lack of maturity of WBGs evidently impacts their reliability. Moreover, their cost limits their market penetration (Das *et al.*, 2018; Els, 2018). Although some WBGs have passed automotive reliability testing for semiconductors, it is known by automotive manufacturers that WBGs can fail differently from conventional Si devices (Das *et al.*, 2018). Thus, the reliability tests of standard Si may not be suitable for WBGs. Specifically, JEDEC, a leading developer of microelectronic standards, is currently working on developing WBG standards for Power Electronic Conversion under the JC-70 Committee (Das *et al.*, 2018; Els, 2018; JEDEC, 2020a). Currently, only the dynamic on-resistance test method guidelines and switching reliability evaluation procedures for GaN is available on the JEDEC website. In the automotive industry, tests are rigorous and undergo a long design cycle, but the validation of the final reliability is based on hours of reliable operation (Charged EVs, 2017). Hence, quality

and reliability must be impeccable to meet the needs of the automotive industry (Charged EVs, 2017).

The packaging limitation is another major challenge, which is considered as the bottleneck for WBG device integration (Garrou, 2019). Compared to WBGs, the Si modules switch slowly and are often packed on clunky design that diminishing parasitic inductances is not considered a priority. Therefore, simply replacing the Si chip with a SiC and expecting improved performance is not realistic (Els, 2018; Charged EVs, 2017; Garrou, 2019). To benefit from the profitable characteristics of WBGs, the voltage insulation, partial discharges, EMI, and thermal management of the whole system must be reviewed (Els, 2018; Charged EVs, 2017; Garrou, 2019). The need to redesign because of WBG integration, risk aversion of manufacturers, and changing requirements for energy accountability remain to be major challenges for the automotive industry (Das *et al.*, 2018).

All the aforementioned constraints considered, OEMs have not openly adopted WBGs. Accordingly, this hesitation impacts power electronics manufacturers who are reluctant to increase the level of production of SiCs, which if done, can result in further cost reduction (Das *et al.*, 2018). Consequently, government-sponsored research institutes such as PowerAmerica have been trying to close the gap among the manufacturers to help WBGs become more competitive in the power electronics industry (Das *et al.*, 2018). Moreover, the Vehicle Technologies Office (VTO) of the U.S. Department of Energy (DOE) has actively been working to reduce the cost of EVs to encourage consumers to adopt this technology (Vehicle Technologies Office, 2019). Researches have focused on inverter technology to reduce its cost, weight, and volume while increasing performance, reliability, efficiency, and innovative modular designs and evolved concepts. The two main objectives were to improve manufacturability and accelerate commercialization (Vehicle Technologies Office, 2019). The efforts have mainly been focused on the integration of WBGs, improvements in thermal management, improvements in reliability, and integration of power electronics functions (Vehicle Technologies Office, 2019). Within the DOE, VTO collaborates with the Office of Science, ARPA-E, and Clean Energy Manufacturing Initiative (Vehicle Technologies Office, 2019). Moreover, across the federal U.S. government,

the subprogram of APEEM DOE works with the National Network for Manufacturing Innovation (NNMI), Interagency Advanced Power Group (IAPG), and Department of Defense (DOD). Moreover, different subprograms are conducted with industry partners through the U.S. DRIVE Partnership and 21st-century Truck Partnership (Vehicle Technologies Office, 2019).

1.2 Advancements and Future prospects of WBG semiconductors

NREL released a report in October 2017 claiming that WBGs were not being used at the traction drive converter level (e.g. inverter) for commercial vehicles available to the general public (Moreno, 2017). Alongside that, as of 2017, Wolfspeed have been claiming that different EVs from different manufacturers contained Wolfspeed's SiC power products, especially for the on-board charging and DC-to-DC converter (Charged EVs, 2017). Currently, several manufacturers such as Toyota and Mitsubishi have been working on the development and manufacturing of SiC and GaN devices within the company (Das *et al.*, 2018). With all the interest in WBGs, several large manufacturers in the automotive industry have teamed up with PE manufacturers or R&D centers to develop solutions. Fig. 1.7 shows an overview of industrial partnerships between EV manufacturers and power electronics WBG suppliers.

In 2017, Mitsubishi announced the development of an ultra-compact inverter model incorporating full-SiC semiconductor modules for HEVs, which was partially supported by Japan's New Energy and Industrial Technology Development Organization (NEDO). According to Mitsubishi, this design is believed to be the world's smallest SiC inverter with the highest power density for two motor HEVs. Achieving superior heat dissipation from SiC is one of the reasons for the innovative concepts of the inverter, which is expected to be commercially available for HEVs and EVs in 2021 (Els, 2018; Mitsubishi Electric Corporation, 2017).

In 2019, STMicroelectronics was chosen by the Alliance of Electric Vehicles, namely Renault-Nissan-Mitsubishi, as the power electronics supplier of SiC MOSFETs and standard devices (STMicroelectronics, 2019b; Hamblen, 2019). The interest of this agreement focused on the development of on-board chargers (OBCs) with SiC MOSFETs (STMicroelectronics, 2019b;

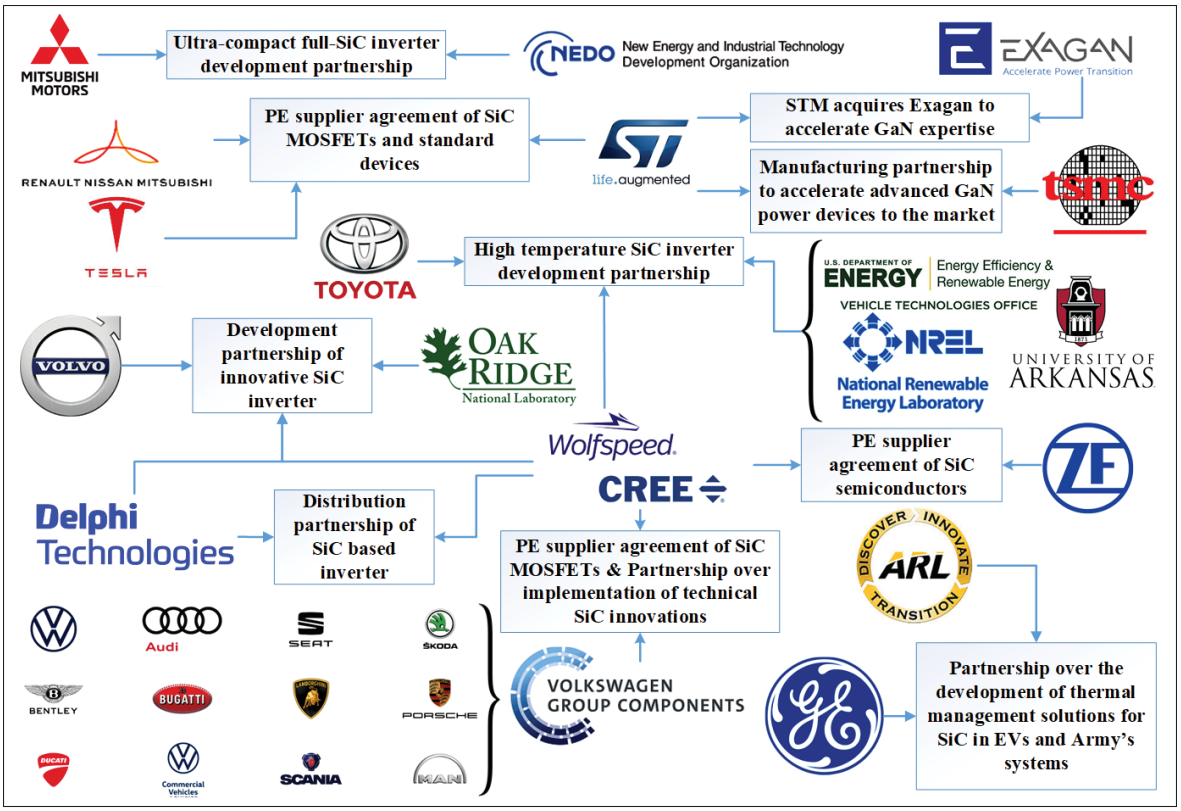

Figure 1.7 An overview of industrial partnerships between EV manufacturers and PE WBG suppliers

Hamblen, 2019). The goal was to optimize the performance and reliability of OBCs and make EV more attractive to consumers (STMicroelectronics, 2019b; Hamblen, 2019). Moreover, in order to secure further development and production of SiC semiconductors, STMicroelectronics signed a SiC wafers supply agreement with SiCrystal in January 2020 (STMicroelectronics, 2020a).

Tesla is also taking advantage of the benefits that SiC can provide for the conversion systems of their vehicles. In 2018, it was confirmed by the Munro Associates and System Plus Consulting, via reverse engineering process, that the Tesla Model 3 inverter uses STMicroelectronics SiC MOSFETs (Garrou, 2019; Avron, 2018).

Between 2016 and 2018, Delphi, Cree, Oak Ridge National Laboratory (ORNL), and Volvo Car Corporation collaborated to develop and demonstrate the functionality of an integrated WBG

power module (Hayes, 2019). The project resulted in a 650 V SiC MOSFETs-based inverter with double-sided cooled packaging to optimize thermal performance (Hayes, 2019). All the expectations from DOE's 2020 Electric Drive Vehicles (EDVs) inverter were exceeded in terms of the size, cost, weight, efficiency, and OEM-customer requirements of future EVs (Hayes, 2019).

In 2016, NREL in partnership with Wolfspeed (Cree), Toyota, the National Center for Reliable Electric Power Transmission at the University of Arkansas, and DOE's Vehicle Technologies Office collaborated together to design an inverter using SiC MOSFETs suitable for high temperatures (The National Renewable Energy Laboratory, 2020). Their joint expertise in thermal management, thermodynamics, and reliability has made it possible to develop an inverter that can operate at an ambient temperature of 140 °C (The National Renewable Energy Laboratory, 2020). Similarly, GE Research and US Army Research Laboratory (ARL) have been collaborating since 2020 to develop thermal management solutions for SiC semiconductors in EV applications and other military services (Editorial Staff, 2020).

As of 2019, Delphi Technologies has developed an 800-V inverter as opposed to opting for the conventional 400 V. Doubling the voltage allows a number of benefits for both the user and manufacturers in terms of space, weight, and efficiency of EVs (Delphi Technologies, 2019). Accordingly, Cree and Delphi agreed to a partnership for the distribution of SiC MOSFETs-based 800-V inverter; hence, a high volume distribution is expected for 2022 (Delphi Technologies, 2019; Chin, 2019). Moreover, in 2019, Hitachi Automotive Systems has been manufacturing an internally developed 800-V inverter and started large-scale production at the end of 2019 (Hitachi Automotive Systems, Ltd., 2019).

Since the end of 2019, Cree have the exclusive SiC partnership of Volkswagen Group FAST Program. The objective was to implement technical innovations for future Volkswagen Group vehicles with SiC-based solutions (Cree, Inc., 2019a). Alongside that, Cree has initiated a partnership with ZF Friedrichshafen, the German parts supplier, to supply SiC semiconductors for the electric drive of EVs. ZF intends to use the Cree technology to complete existing orders

from auto manufacturers and hopes to make SiC drivelines available on the market by 2022 (Cree, Inc., 2019b).

As of June 2020, ROHM Semiconductor and Continental Vitesco Technologies agreed over a development partnership in order to further increase the efficiency of APEs through the use of high efficiency SiC semiconductors (ROHM CO., LTD., 2020b). Then, in July 2020, knowing the importance of SiC devices in the automotive industry, ROHM and LEADRIVE have recently partnered together to establish a joint laboratory to develop SiC devices for APEs (ROHM CO., LTD., 2020c).

For GaNs, GaNPower International Inc. (GPI) announced a three-way research agreement with Magna International Inc. and Queen University in June 2018 (GaNPower, 2018). The project concerns the development of high-performance auxiliary DC/DC converters for EVs with GaN-based switching mode power systems (GaNPower, 2018). In 2020, STMicroelectronics and Taiwan Semiconductor Manufacturing Company (TSMC) agreed to a manufacturing partnership of the GaN product of STM through the GaN process technology of TSMC (STMicroelectronics, 2020b). Through this collaboration, both companies wish to accelerate the development and delivery of advanced power GaN solutions to the market (STMicroelectronics, 2020b). Recently, STMicroelectronics signed an agreement to obtain a majority stake in the GaN innovator Exagan (STMicroelectronics, 2020c). The objectives of STM are to acquire even more GaN expertise to accelerate its GaN roadmap and business for high-frequency, high-power automotive, and consumer and industrial applications (STMicroelectronics, 2020c). Moreover, as of 2020, Nexperia and Ricardo are in a partnership agreement to develop GaN-based EV inverter design. The objective is to demonstrate the high potential of GaN semiconductors over Si and SiC for the traction inverter (Nexperia, 2020b).

There have been efforts by automotive and PE manufacturers, government organizations, and research centers to effectively integrate WBGs on the EV market, specifically SiC. These efforts will make EVs more attractive to consumers and accelerate both the adoption of WBGs and EVs.

1.3 Statement of the Problem and Research Objectives

WBGs have been important in the improvement of the automotive industry. Their intrinsic characteristics have allowed new EV generations to be more attractive to consumers by improving their performance in every aspect. The characteristics, maturity, and availability of SiC make it favorable for PE applications such as EV inverters, DC to DC, and on-and-off board chargers. Further improvements in GaN vertical structure may result in excellent semiconductors for power applications due to lower theoretical on-resistance limits. Currently, studies demonstrate that SiC has better characteristics to suit PE requirements of EVs. All challenges considered, major industrial mobilization through innovative partnership can lead to the efficient improvements of EVs with the integration of SiC WBG semiconductors on PE systems.

1.4 Thesis Outline and Methodology

Although the literature seems favorable towards SiCs for power applications, it is a field in proactive evolution where both major WBG semiconductors have much to offer. For example, in just a few months after the publication of the literature review (Bérubé, Ghazanfari, Blanchette, Perreault & Zaghib, 2020), already three new evaluation standards for WBGs were published by JEDEC, including one regarding SiCs (JEDEC, 2020b). For now, the state of the art about WBG semiconductors still bring confusion to engineers when it comes to choosing the most efficient technology for a specific board design. Then, in the objective to bring clarity about major considerations of WBG and Si MOSFETs, there is nothing better than going through simulation and experimentation to express major advantages and drawback linked to each technologies under a switching configurations.

However, simulation is a vast domain often with lots of hypothesis. Then, it is essential to understand first the chosen simulation model and its limitations in order to interpret the results obtained, and the influence of internal and external parameters on the switching behavior.

CHAPTER 2

UNDERSTANDING CHARACTERISTICS AND SWITCHING PERFORMANCE OF MOSFETS

This chapter presents MOSFETs modeling and explanation of parasitic components based on material structure. Then, a MOSFET's computational model under an inductive configuration is proposed. The benchmark computational model from (Clemente, Pelly & Isidori, 1982) is explored in detail and compared with further development of equations for the first and second turn-on interval. This methodology allows to compare WBG and Si MOSFETs based on intrinsic characteristics, making approximated observations on all MOSFETs technologies possible.

2.1 MOSFET Modeling Technique and Parasitic Components

Since the first patent in the 1920s and 1930s of free carriers' modulation through the static transverse electric field, commonly known as the Field Effect (FE) by Lilienfeld and Heil, many improvements were born from Field-Effect Transistor devices (FET). Several successive failures to exploit the field effect have led to countless successful architecture devices based on that principle. The n-channel lateral MOSFET appeared in the early 1960s, further technological improvement led to the manufacture of Vertical V-groove MOSFET (VVMOS) and eventually to the Vertical Double-Diffused MOS structure with a polycrystalline silicon gate (VDMOS). The latter has been highly favored in high power applications because of its higher current and voltage capability compared to lateral devices (Grant & Gowar, 1989). Inversely, lateral power MOSFETs normally have lower capacitances, allowing a faster switching speed with less gate drive power (Balogh, 2018). Improved fabrication techniques of cellular geometry allow very wide gate structure, resulting in high transconductance and low on-state resistance of MOSFETs (Grant & Gowar, 1989). Nowadays, many improvements in manufacturing techniques and technological advancement introduce even more increased performance MOSFETs like super-junction structures and WBG materials.

There are a lot of different modeling methods viable for MOSFETs representation (Grant & Gowar, 1989; Balogh, 2018), and they are mainly developed for specific applications (Balogh, 2018). Firstly, MOSFETs characteristics may be represented by an equivalent circuit made of linear and nonlinear components like capacitors, resistors, current sources, etc. This is normally the preferred method because it is possible to approximate the device's behavior around a steady point with a linear representation when considering small signal variation. Many different modeling approaches have been explored such as process modeling from physical and chemical device structure or modeling from static and mobile charge distribution. To have a better understanding of MOSFETs behavior, the equivalent component modeling approach from electron energy-level in (Grant & Gowar, 1989) was chosen as the reference behavioral model of MOSFET. However, understanding the interactions and limitations of parasitic components on the material level is required to represent an accurate equivalent model. Accordingly, the assumption from (Grant & Gowar, 1989) is considered to explain the standard MOSFET modeling from material layers. Based on equations development resulting from a deep understanding of material science (Grant & Gowar, 1989), the representation of the equivalent model and its internal parasitic components is obtained as illustrated by Fig. 2.1 in an n-channel power MOSFET. Accordingly, this can be translated into the equivalent internal electrical circuit of the MOSFET as illustrated by Fig. 2.2.

The equivalent electrical circuit incorporates different passive and active components which influence the steady and transient behavior of the MOSFET, and are particularly useful to understand its switching characteristics. To be more explicit, Table 2.1 summarize the main passive and active components included in Fig. 2.2. To study the impact of each of the passive and active components, a deep knowledge of semiconductor material science is required. Therefore, this chapter briefly covers only major elements discussed in (Grant & Gowar, 1989).

2.1.1 Resistance, Parasitic JFET

The p-doped body is playing the role of the gate in the n-type drain drift region. The addition of resistance from the JFET effect can account for up to 25% of the total $R_{ds(on)}$, especially for high-

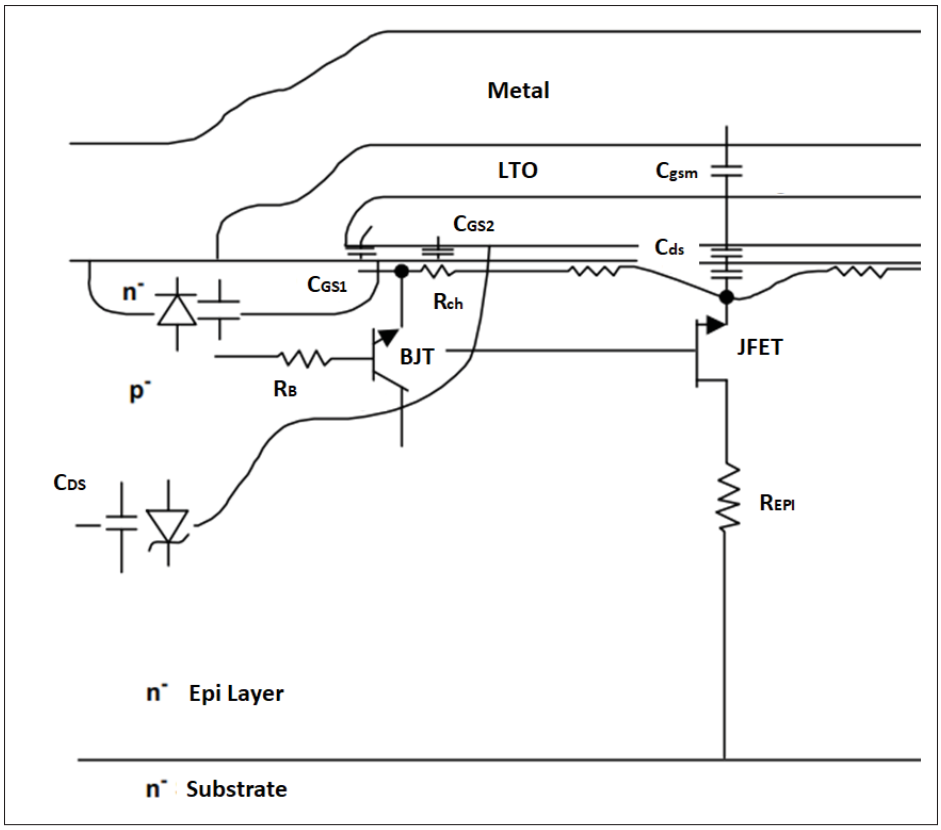

Figure 2.1 Schematic diagram of an n-channel power MOSFET with its parasitic components
Adapted from Barkhordarian (1997)

voltage devices. Since it has a considerable impact on the total $R_{ds(on)}$ of high voltage device, it is important to consider the parasitic JFET in the equivalent circuit model (Grant & Gowar, 1989).

2.1.2 Internal Parasitic Capacitances

There are three-terminal capacitors specified in the MOSFETs datasheet, respectively the input capacitance (C_{iss}), the output capacitance (C_{oss}), and the reverse transfer or Miller capacitance (C_{gd}). Typically measured at 1 MHz, their values are usually specified at a drain-source voltage (v_{ds}) of 25 V and a gate-source voltage (v_{gs}) of 0 V, but they are all function of the DC drain-source voltage (Grant & Gowar, 1989). Based on MOSFET's equivalent electrical model

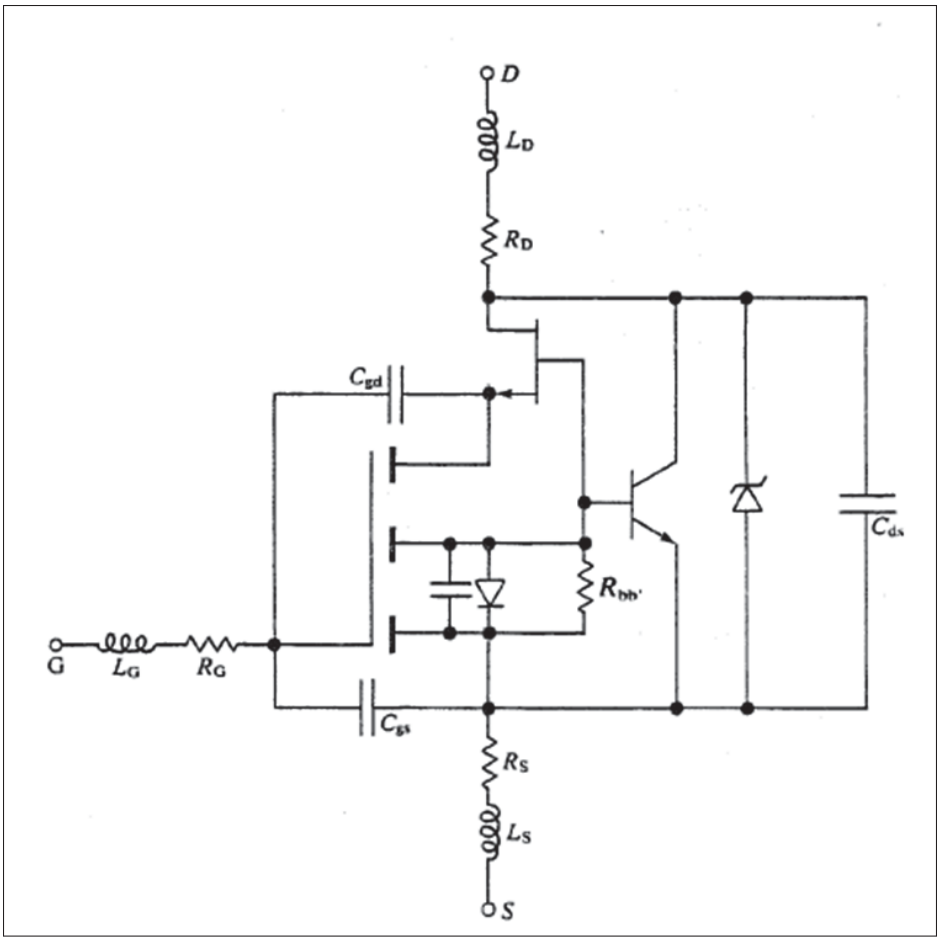

Figure 2.2 MOSFET equivalent electrical circuit with parasitic components
Adapted from Grant & Gowar (1989)

presented in Fig. 2.2, terminal capacitors are related to internal capacitors often referred to as parasitic capacitances through the following relations:

1. C_{iss}, the input capacitance is the sum of C_{gs} and C_{gd} (Grant & Gowar, 1989) since they are in parallel.

$$C_{iss} = C_{gs} + C_{gd} \tag{2.1}$$

2. C_{oss}, the output capacitance correspond to the total capacitance between the drain-source terminal as the gate and source are shorted together (Grant & Gowar, 1989).

$$C_{oss} = C_{ds} + C_{gd} \tag{2.2}$$

3. C_{rss}, the reverse transfer (Miller) capacitance is the gate-drain capacitance as the gate-source voltage v_{gs} equal 0V (Grant & Gowar, 1989).

$$C_{rss} = C_{gd} \tag{2.3}$$

First, the Miller capacitance C_{gd} is a combination of the gate oxide capacitances and the drain depletion layer capacitances underneath the gate oxide. However, these combination of depletion layer capacitances exist only when the voltage potential of the drain region is more positive than the gate potential. Inversely, when the gate potential is larger than the drain-source voltage, an accumulation layer forms at the semiconductor's surface and the value of C_{gd} falls rapidly and progressively as the depletion layer extends into the epilayer (Grant & Gowar, 1989; Balogh, 2018).

Independent of the voltage bias, the gate-source capacitance C_{gs} is composed of the overlap capacitance, the gate-channel capacitance, and the capacitance through the field oxide of the source overlay. Then, the drain-source capacitance C_{ds} mainly referred to as the body diode's capacitance is composed of the junction capacitance between the p diffusion and the epilayer (Grant & Gowar, 1989; Balogh, 2018).

Table 2.1 Inclusion from the Main Passive and Active Components of the Equivalent MOSFET Electrical Schematic with Parasitic Components Adapted from Grant & Gowar (1989)

Passive Components
Resistive elements contributing to $R_{DS(on)}$
Inductance of pin connections
Gate-Source metallization & Gate-Source diffusion capacitances
Gate-Body & Gate-Epilayer capacitances
pn junctions' capacitances
Normal diode behavior of pn junctions
Active Components
N-channel junction field-effect transistor (JFET)
NPN bipolar junction transistor (BJT) between the source, the body, and the drain

To overcome the influence of voltage bias on internal capacitances, a graph of terminal capacitances as a function of the drain-source voltage is normally provided in datasheets. Since this graph is only provided for limited values of v_{gd}, it does not show the full variation of internal capacitances. To address this issue, the amount of charge required to change the gate voltage to an appropriate driving voltage is specified for a pre-defined load current in MOSFETs datasheets (Grant & Gowar, 1989).

2.1.3 Bipolar Junction Transistor and Body-Drain Diode

As listed in Table 2.1 and shown in the equivalent electrical model in Fig. 2.2, a parasitic bipolar junction transistor (BJT) is formed inside the MOSFET structure. In steady-state conditions, only the body-drain diode of the BJT is effective because the base and emitter are shorted. However, in transient and avalanche breakdown conditions, the MOSFET's performance will be remarkably diminished if the BJT is triggered.

Fortunately, the parasitic diode has a similar current rating to the MOSFET. Therefore, the reversed bias voltage of the MOSFET puts the parasitic diode in conduction mode, without causing excessive heat dissipation or external circuit problems. Forward parasitic diode voltage ($V_{sd(on)}$) should be kept low, and the typical values are between 2V and 2.5V. Furthermore, the parasitic diode should exhibit a fast and smooth recovery waveform with a low reverse recovery charge (Q_{rr}) (Grant & Gowar, 1989).

The reverse avalanche-breakdown characteristic of the MOSFET's body-drain diode determines the forward voltage rating of the device, commonly named the breakdown voltage (BV_{DSS}). Many modern devices are designed to withstand substantial current under controlled avalanche breakdown. This condition allows to quench forward transients and dissipate inductive energy without external clamping or snubber circuit. However, it is important to keep both Avalanche Energy, single pulse (Eas) and Avalanche Energy, repetitive (Ear) below the maximum rating of the device (Charge x BV_{DSS}). Under these circumstances, the current flowing through the ohmic resistance of the pinch-base (R_{bb}) may initiate the parasitic BJT if its voltage drop exceeds

0.6V. In that case, the activated BJT withstands all the current and eventually results in thermal runaway, and device destruction (Grant & Gowar, 1989).

2.1.4 An Introduction to the Temperature Effect

Except for internal capacitances, temperature significantly impacts MOSFET's characteristics and performances. Saturation velocity and carrier mobility decrease as the temperature rises and the bulk region resistance increases. As a result of the temperature rise, the junction breakdown voltage increases by 1% for each increase of 10°C, and the device lifetime is expected to decrease. In addition, lower $V_{sd(on)}$ is required to support a specific current at elevated temperature, but the BJT is easily turned on because the pinch-base resistance is increased (Grant & Gowar, 1989).

2.2 MOSFET Transient Behavior

The main principle behind the field-effect transistor action lies in the control of the drain current by the gate voltage (Grant & Gowar, 1989). The most typical way to represent the MOSFET behavior depending on gate voltage is a simple current controlled source, as illustrated in Fig. 2.3.

For simplification purpose of the analysis of the transient behavior of MOSFETs, the following approximations and assumptions are considered.

1. Simplified linear transfer characteristic under valid conduction criterion of (v_{gs}) greater than the threshold voltage (V_T) between the drain-source current (i_{ds}) and gate-source voltage (v_{gs}).

$$i_{ds} = \text{gfs}(v_{gs} - V_T), \text{ as long as } v_{gs} > V_T \text{ and } v_{ds} > i_{ds} \times R_{\text{ds(on)}} \tag{2.4}$$

2. Complete absence of the drain-source current (i_{ds}) under invalid conduction criterion.

$$\text{When } v_{gs} < V_T, i_{ds} = 0 \tag{2.5}$$

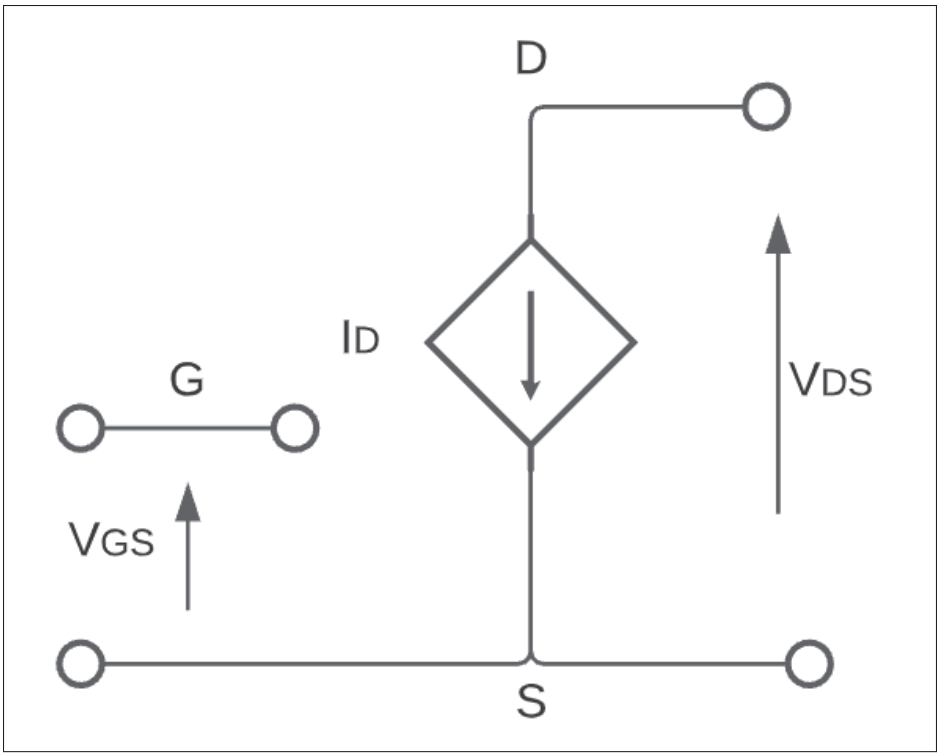

Figure 2.3 Simple MOSFET model for transient analysis
Adapted from Grant & Gowar (1989)

3. Ohm's law define the conducting drain-source current after saturation.

$$\text{For gfs}(v_{gs} - V_T) > \frac{v_{ds}}{R_{\text{ds(on)}}}\text{, the MOSFET is completely ON and } i_{ds} = \frac{v_{ds}}{R_{\text{ds(on)}}} \qquad (2.6)$$

The first assumption means that a linear approximation of the MOSFET's transconductance, as presented in Fig. 2.4, is considered. Since the transition between the non-conducting state to the conducting state is normally very short, there is only a very minor impact on neglecting the transition curve of the transconductance relation on the switching simulation. In connection with the assumption of a linear transconductance, the second assumption implies that the MOSFET is completely OFF when the gate-source voltage is under the threshold voltage, therefore there are no leakage currents of any sort. Thirdly, when the theoretical drain-source current computed with the transfer characteristic and gate-source voltage is over the actual current calculated with Ohm's law, the MOSFET is fully ON. In that case, fully ON means that the field-effect is

not (theoretically) restraining the drain-source current to flow, only the equivalent resistance of materials elements $R_{ds(on)}$ is limiting the current (Grant & Gowar, 1989). An example of the approximated and exact relation between the drain-source current and gate-source voltage, commonly known as transconductance (gfs), is shown in Fig. 2.4.

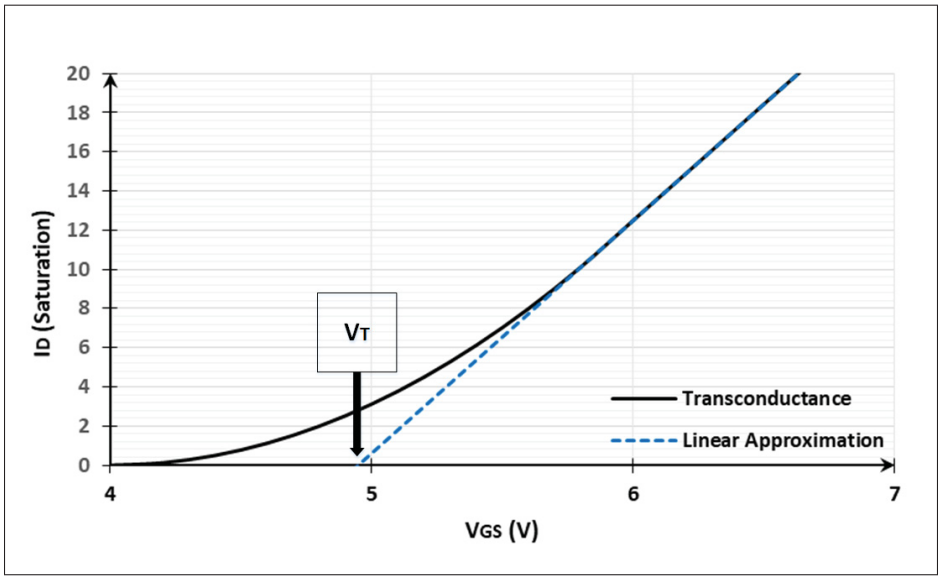

Figure 2.4 Example of linear approximation of the transfer characteristic of a MOSFET

The time it takes for the drain-source current to react to a change in gate-source voltage is dependent on the speed of carriers in the inversion layer and the transit time along the length channel. Thus, the response time depends on the channel length and either the carriers mobility or the saturation drift velocity. Typically, the response time of the MOSFET to the gate charge is not the speed limiting factor. The maximum switching speed of the MOSFET is normally limited by the parasitic elements of the circuit itself. Thus, at very high frequencies, it is necessary to solve the semiconductor transient equations simultaneously with the circuit equations (Grant & Gowar, 1989). In practice, the time required to establish voltage change across parasitic capacitances and current change across parasitic inductances determine the switching speed and frequency response (Grant & Gowar, 1989; Balogh, 2018) which is highly related to the switching performance of the MOSFET (Balogh, 2018). The equivalent MOSFET model including the most relevant parasitic components is illustrated in Fig. 2.5.

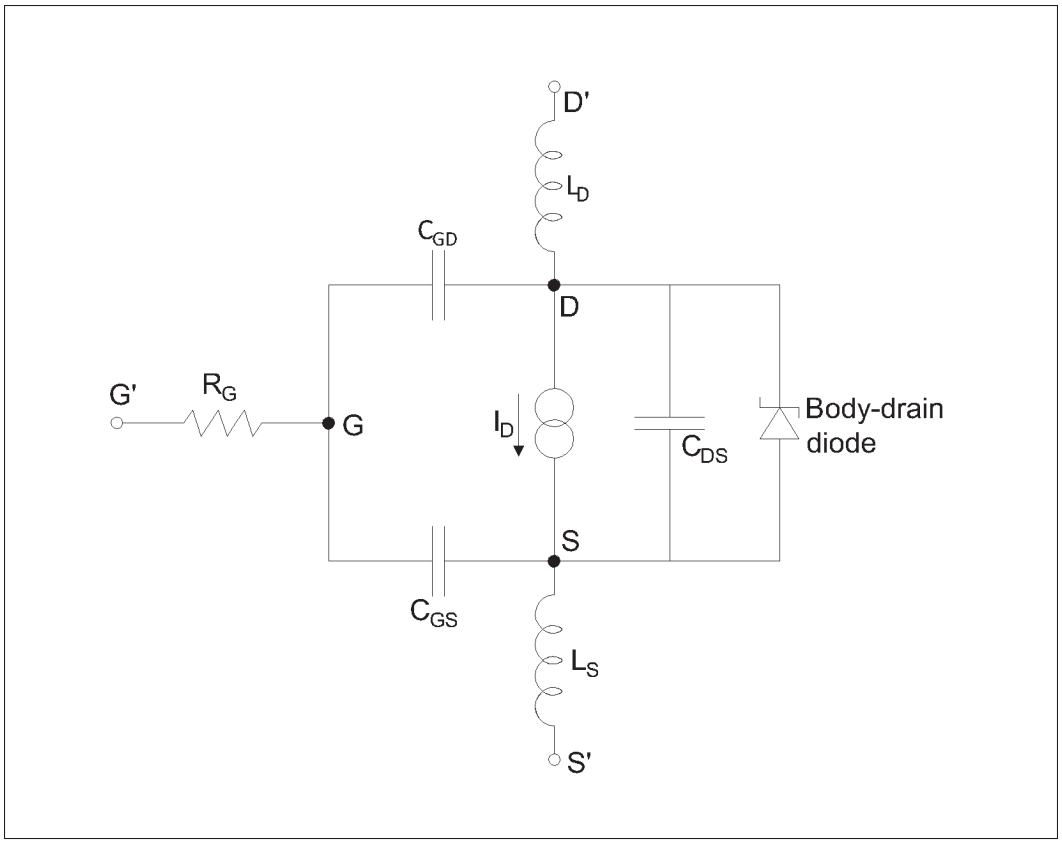

Figure 2.5 Equivalent MOSFET model with its most important parasitic components
Adapted from Grant & Gowar (1989)

Model of Fig. 2.5 is the usual approximation used at the electrical engineering level to study MOSFETs transient behavior. It includes equally distributed interelectrode parasitic capacitances, parasitic inductances of source and drain leads, and the distributed resistance of the polycrystalline silicon gate. Typical values of lead inductances are around 5 to 15nH whilst the polycrystalline gate resistance is typically around 20 Ωmm^2 (Grant & Gowar, 1989). At this point, the main question to answer is why it is important to study the transient behavior of semiconductors? Understanding the transient behavior of MOSFETs can be helpful to realize what the influence of external parameters is and help designers to minimize losses in switching circuits. During the turn-on interval, energy is stored in parasitic capacitances, then it is transferred to parasitic inductances at turn-off (Grant & Gowar, 1989). The total energy dissipated by MOSFETs can be subdivided into three intervals as follow: turn-on energy, turn-off

energy, and steady conduction state energy. Then, the total average power dissipated by the MOSFET within the switching process can be computed with (2.7).

$$P_{total} = (E_{on} + E_{conduction} + E_{off}) \times Frequency \tag{2.7}$$

Typical applications of MOSFETs are often related to a constant or modulated current with a machine or transformer winding. Thus, analysis of transient losses through a resistive circuit would not be relevant for real applications. An equivalent circuit with a clamped inductive load, as illustrated by Fig. 2.6, is used as a reference circuit to conduct transient losses analysis.

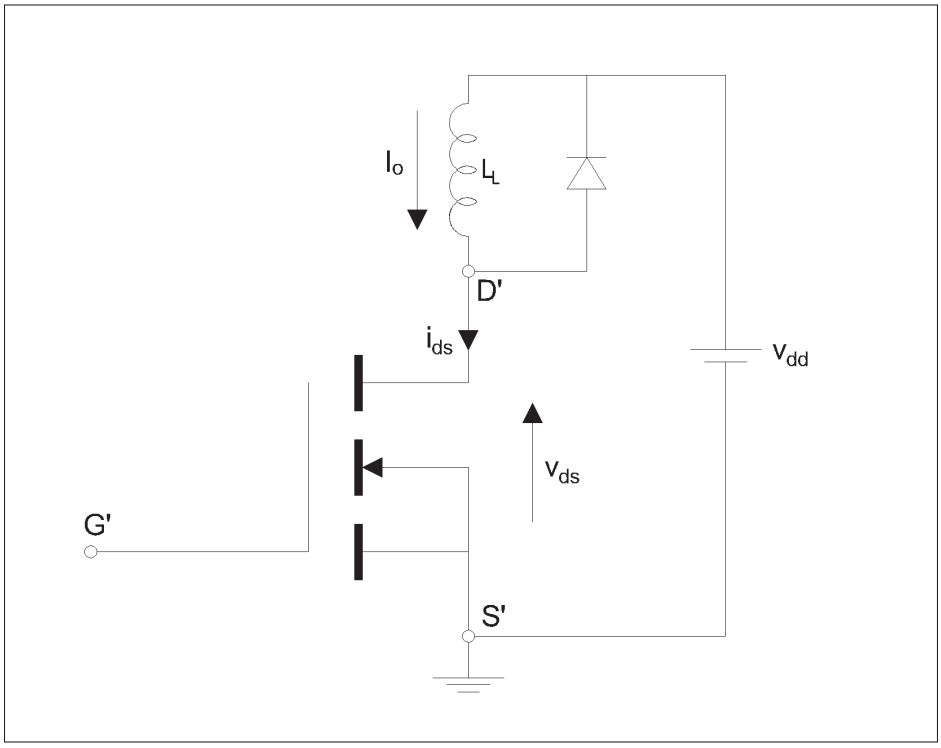

Figure 2.6 Clamp inductive load equivalent transient analysis circuit
Adapted from Grant & Gowar (1989)

In contrast to the resistive circuit, in the inductive circuit the MOSFET's drain-source voltage has to increases to the supply voltage (V_{dd}) plus the diode's forward voltage (V_{diode}) during the turn-off interval. Otherwise, the diode is not conducting and the current cannot start flowing

through the freewheeling diode. Similarly, the drain-source voltage is clamped to V_{dd} plus V_{diode} at turn-on until the drain current increases to its nominal value (I_0). Compared to a resistive equivalent circuit, the clamped inductive circuits increase transient power dissipation by a factor of three (Grant & Gowar, 1989). Not clamping the inductive load may result in lower turn-on losses. However, the inductance stored energy is dissipated at turn-off which adds up to the total turn-off losses by driving the MOSFET into avalanche breakdown. Even if actual devices can withstand avalanche breakdown for a specific maximum non-repetitive energy, the breakdown voltage of MOSFETs is higher than the supply voltage. This higher voltage might result in higher total losses than clamping the load current with a freewheeling diode (Grant & Gowar, 1989). Thus, it should be avoided unless it is required by the application (Nexperia, 2020a; Infineon Technologies AG, 2017).

Several simulation models have been proposed in the literature to represent the switching performance of MOSFETs. The model proposed by International Rectifier (IRF) (Clemente *et al.*, 1982) offers a systematic approach to decompose the impact of every internal parameter on the switching intervals of MOSFETs. This mathematical model based on the equivalent circuit presented in Fig. 2.6 is easily reproducible. However, the accuracy of the model is impacted due to multiple assumptions as presented in section 2.3.

2.3 Hypotheses of MOSFET's Simulation Model

The proposed simulation model in (Clemente *et al.*, 1982) provides a strong platform to compare MOSFETs' behavior under different switching conditions. However, there are some considerations and limitations that come with it, as follows.

- Self-capacitances are nonlinear functions of the applied voltage and also to some extent of the drain-source current (Clemente *et al.*, 1982). In MOSFET's datasheets, internal capacitances (C_{iss}, C_{oss}, C_{rss}) depend on the drain-source voltage. However, these capacitances are assumed to be fixed based on the supply voltage.
- Assumed fixed transconductance (gfs) around nominal drain-source current (i_{ds}).

- Fixed gate threshold voltage determined by the typical value extracted from the datasheets for the fixed temperature of 25 °C unless otherwise specified.
- For operations of the MOSFET in the active region, the external drain-source current is assumed to be instantaneously responsive to the gate-source voltage (Clemente *et al.*, 1982).
- Capacitive currents flowing through various internal capacitive elements during transient switching conditions are assumed not to affect the transfer characteristic between external drain current and the gate-source voltage (Clemente *et al.*, 1982).
- C_{ds} is ignored for operations in the active region. This assumption is valid because the effect of the gate-drain capacitance (C_{gd}) provides a coupling path from the drain circuit to the relatively sensitive gate circuit which generally swamps the effect of C_{ds} (Clemente *et al.*, 1982).
- The clamped inductive load is assumed to be inductive enough to allow a constant current value throughout the whole switching process (Clemente *et al.*, 1982).
- The total *unclamped* stray inductance is represented through L_d (Clemente *et al.*, 1982).
- The effect of the common source inductance L_s is generally neglected in the analysis. The impact of this parameter will be further discussed to observe its effect on the early stage of the transient intervals (Clemente *et al.*, 1982).

2.4 MOSFET's Simulation Modeling

For each switching interval, each turn-on and turn-off period are divided into four sub-intervals (Grant & Gowar, 1989; Clemente *et al.*, 1982). Each sub-interval refers to independent equations associated with that specific interval to illustrate the switching behavior of the MOSFET. For each sub-interval, the time reference is set to zero and the end conditions of a given sub-interval are the initial conditions of the following one. Fig. 2.7 illustrate a general overview of the computational approach. Transient equations and typical waveforms from simulation are presented following a global explanation of each sub-interval.

The equivalent simulated clamped inductive load circuit including MOSFET's parasitic components compliant with modeling's assumptions is illustrated in Fig. 2.8. Only the load inductance

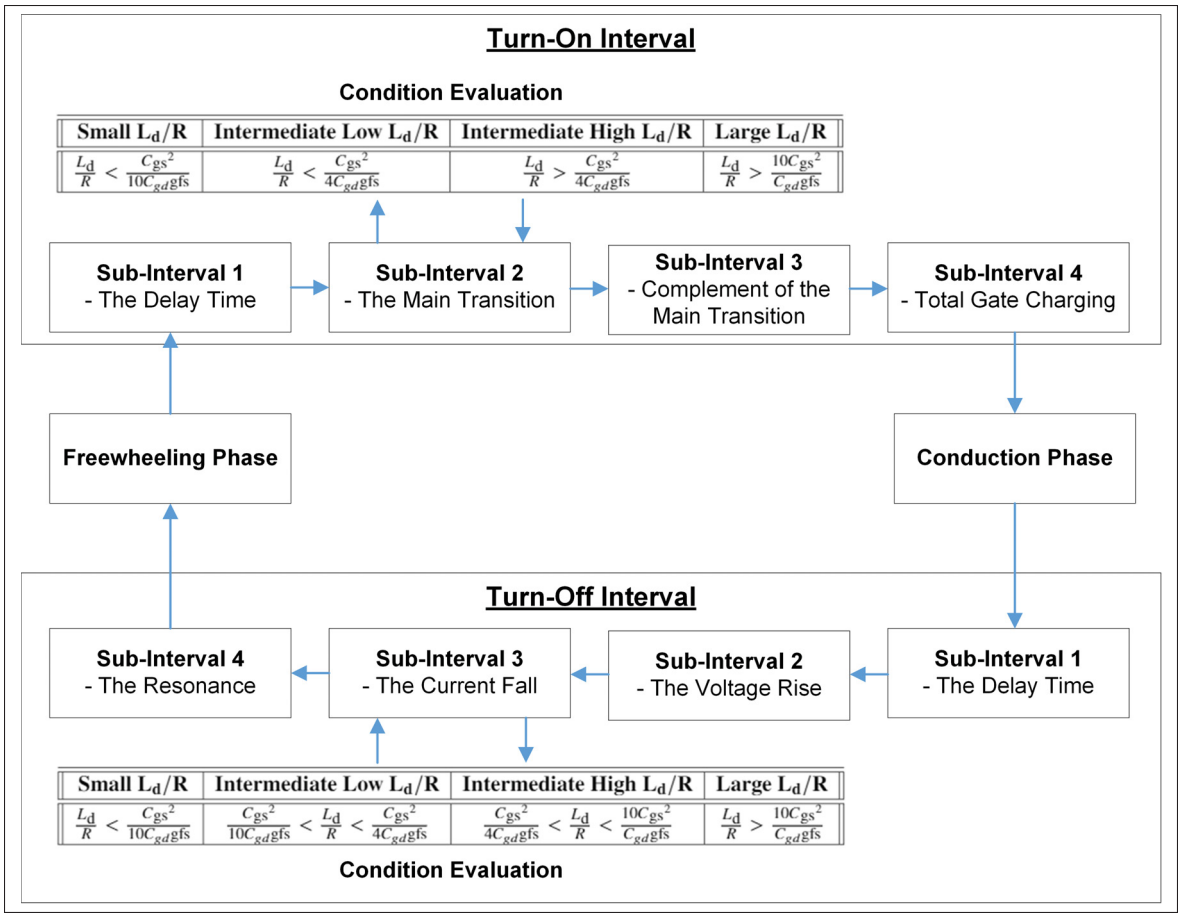

Figure 2.7 General overview of the computational approach

is clamped because it is not possible to do so with lead inductance. Moreover, any other unclamped portion of inductances is included in the drain inductance L_d. This frequently used arrangement is our reference model to detail transient intervals of MOSFETs.

For consistency reasons, a very similar nomenclature as defined in (Clemente *et al.*, 1982) to determine transient equations has been used to express simulation variables in MATLAB, and to further develop the mathematical model, as illustrated in the section 2.4.1.

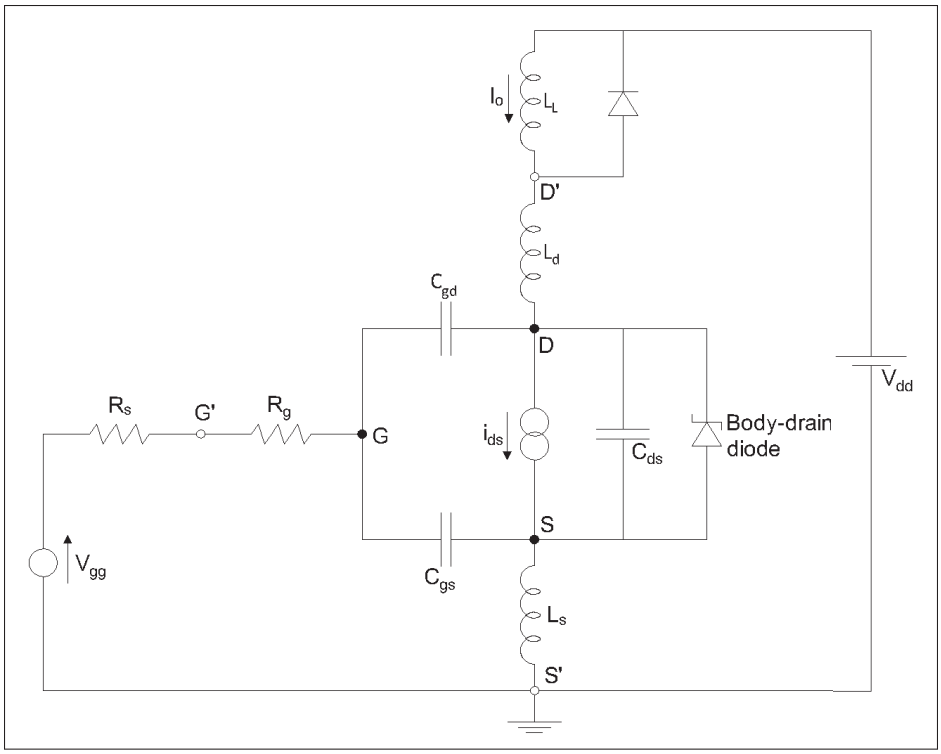

Figure 2.8 Reference simulation model of clamp inductive MOSFET's transient analysis circuit
Adapted from Clemente *et al.* (1982)

2.4.1 Mathematical and Simulation Modeling's Nomenclature

Detailed simulation and adapted mathematical nomenclature from (Clemente *et al.*, 1982) is expressed as follows.

- v_{ds} : Instantaneous drain-source voltage.
- v_{gs} : Instantaneous gate-source voltage.
- v_{gd} : Instantaneous gate-drain voltage.
- V_{dd} : Steady drain-circuit voltage.
- V_T : Gate threshold voltage.
- V_{gg} : Gate driving voltage.
- V_{GH} : Applied positive gate driving voltage (turn-on).
- V_{GL} : Applied null or negative gate driving voltage (turn-off).

- V_F : Positive forced gate driving voltage over the threshold voltage (V_{GH}-V_T).
- V_{ds}^* : Initial value of the MOSFET's drain-source voltage at the beginning of an interval.
- V_{gs}^* : Initial value of the MOSFET's gate-source voltage at the beginning of an interval.
- V_{clamp} : Drain-source clamping voltage.
- i_{ds} : Instantaneous drain-source current.
- i_{gs} : Instantaneous Cgs current.
- i_{gd} : Instantaneous Cgd current.
- i_g : Instantaneous total gate current.
- I_0 : Constant current in the clamped inductance, also the nominal drain current.
- I_{ds}^* : Initial value of the MOSFET's drain current at the beginning of an interval.
- R_s : External gate driving resistance.
- R_g : Internal gate resistance.
- R : Total gate resistance ($R_s + R_g$).
- $R_{ds(on)}$: Fully on-state drain-source resistance of the MOSFET.
- R_d : Resistance of the drain circuit's stray.
- L_d : Total unclamped inductance plus the drain lead inductance.
- L_s : Common source inductance.
- C_{gs} : Gate-source capacitance.
- C_{gd} : Gate-drain capacitance or Miller capacitance (C_{rss}).
- C_{ds} : Drain-source capacitance.
- C_g : Total input capacitance $C_{iss} = C_{gs} + C_{gd}$.
- C_d : Total output capacitance $C_{oss} = C_{ds} + C_{gd}$.
- gfs : Approximation of fixed transconductance.

2.4.2 Turn-On Intervals

For analysis, the initial state of the MOSFET is completely turned off without any voltage applied on the gate circuit with the load current flowing through the freewheeling diode. This condition

is similar to driving the MOSFET for the first time. Therefore, drain-source voltage is initially equal to the supply voltage, drain current is null and the driving voltage is null too.

2.4.2.1 Turn-On 1st Interval: The Delay Time

The turn-on interval starts with a delay caused by the required time to charge the gate-source capacitance to the threshold voltage. Since computational assumptions considered a linear transconductance without any conduction current below the threshold voltage, there is not any losses nor change in the drain voltage and current. It is only the gate voltage that changes over time in this first interval. The initial conditions are as follows.

$$v_{gs}(t_o) = V_{GL} < V_T \tag{2.8}$$

$$v_{gg}(t_o) = V_{GL} \text{ and } v_{gg}(t_o^+) = V_{GH} \tag{2.9}$$

The gate-source capacitance voltage v_{gs} is stabilized at the turn-off driving voltage V_{GL}, and the gate driving voltage v_{gg} instantly changes from its low value V_{GL} to its high value V_{GH} at the beginning of this interval. There is no change in both the drain-source voltage and current of the MOSFET during this first interval.

$$i_{ds} = 0 \text{ and } v_{ds} = V_{dd} + 0.7V$$

When the gate voltage v_{gs} turns to its high value, the gate capacitance charges gradually depending on the total resistance and capacitance values. The higher the internal capacitances and gate resistor, the longer it takes to reach the threshold voltage. For the first interval, the depletion channel is not formed yet. Therefore, there are no interactions from the drain-source voltage nor drain current with the gate capacitance. As shown in Fig. 2.8, the total gate

capacitance is formed by a parallel arrangement of the gate-drain capacitance C_{gd} and the gate-source capacitance C_{gs} for this interval. This specific parallel combination of capacitance is known as the input capacitance C_{iss}. Since the drain-source voltage is steady for this interval, the total input capacitance is also constant. At high frequencies, the required time to complete each interval may limit the device's capability to reach the desired switching frequency. The duration of delay is especially critical for fast switching devices such as GaN and SiC MOSFETs. Mathematical equations are developed to describe the first turn-on interval considering the previous enumerated assumptions, as follows.

$$V_{GH} = i_g(R_s + R_g) + v_{gs} + L_s\frac{di_g}{dt} \tag{2.10}$$

$$With \begin{cases} R = R_s + R_g \\ i_g = C_{iss}\frac{dV_{Ciss}}{dt} \\ v_{L_s} = L_s\frac{di}{dt} \\ \frac{di_g}{dt} = C_{iss}\frac{d^2V_{Ciss}}{d^2t} \end{cases}$$

$$V_{\mathrm{GH}} = (RC_{\mathrm{iss}})v_{\mathrm{gs}}{}' + v_{\mathrm{gs}} + (L_{\mathrm{s}}C_{\mathrm{iss}})v_{\mathrm{gs}}{}''$$

$$(L_{\mathrm{s}}C_{\mathrm{iss}})v_{\mathrm{gs}}{}'' + (RC_{\mathrm{iss}})v_{\mathrm{gs}}{}' + v_{\mathrm{gs}} - V_{\mathrm{GH}} = 0 \rightarrow f(t) \tag{2.11}$$

A second-order equation presents the first turn-on interval due to the presence of the common source lead inductance L_s. Since there is no variation of the drain-source voltage or drain current at this sub-interval, the source lead inductance can be defined as the combination of the gate-source circuit loop inductance and the source lead inductance. The equation (2.11) presents the simplified approximation of the first turn-on sub-interval. The complete mathematical analysis of the first interval considering the common source inductance is presented

in appendix I. A comparison between the simplified and complete analysis shows the impact of the commonly neglected common source inductance in MOSFET's modeling approach as proposed in (Clemente *et al.*, 1982). By neglecting the impact of the source inductance L_s, the simplified equations for the first turn-on sub-interval are as follows.

$$\cancel{(L_s C_{iss}) v_{gs}''} + (RC_{iss}) v_{gs}' + v_{gs} - V_{GH} = 0 \rightarrow f(t)$$

$$\mathscr{L}\{f(t)\} = F(s) = (RC_{iss}) \left(s \cdot v_{gs}(s) - v_{gs}(0)\right) + v_{gs}(s) - \frac{V_{GH}}{s} = 0 \tag{2.12}$$

With,

$$v_{gs}(0) = V_{GL}$$

$$(RC_{iss}) s \cdot v_{gs}(s) + v_{gs}(s) = \frac{(RC_{iss}) s \cdot V_{GL} + V_{GH}}{s}$$

$$v_{gs}(s) = \frac{s \cdot V_{GL} + \frac{V_{GH}}{RC_{iss}}}{s(s + \frac{1}{RC_{iss}})} = \frac{k_1}{s} + \frac{k_2}{s + \frac{1}{RC_{iss}}}$$

$$s \cdot V_{GL} + \frac{V_{GH}}{RC_{iss}} = (k_1 + k_2) s + \frac{k_1}{RC_{iss}}$$

$$\begin{cases} k_1 = V_{GH} \\ k_1 + k_2 = V_{GL} \rightarrow k_2 = V_{GL} - V_{GH} \end{cases}$$

$$v_{\mathrm{gs}}(s) = \frac{V_{\mathrm{GH}}}{s} + \frac{V_{\mathrm{GL}} - V_{\mathrm{GH}}}{s + \frac{1}{RC_{\mathrm{iss}}}}$$

$$\mathscr{L}^{-1}\{F(s)\} = f(t) = v_{\mathrm{gs}}(t) = V_{\mathrm{GH}} + (V_{\mathrm{GL}} - V_{\mathrm{GH}})e^{\frac{-t}{RC_{\mathrm{iss}}}}$$

$$v_{\mathrm{gs}}(t) = (V_{\mathrm{GH}} - V_{\mathrm{GL}})(1 - e^{\frac{-t}{RC_{\mathrm{iss}}}}) + V_{\mathrm{GL}}$$

Then, the time constant of the interval τ_{g} can be define as follow.

$$\tau_{\mathrm{g}} = RC_{\mathrm{iss}} = (R_{\mathrm{s}} + R_{\mathrm{G}})(C_{\mathrm{gd}} + C_{\mathrm{gs}})$$

$v_{gs}(t)$ becomes,

$$v_{\mathrm{gs}}(t) = (V_{\mathrm{GH}} - V_{\mathrm{GL}})(1 - e^{\frac{-t}{\tau_{\mathrm{g}}}}) + V_{\mathrm{GL}} \tag{2.13}$$

The time for $v_{gs}(t)$ to reach the threshold voltage V_T, commonly known as the delay time, is derived below.

$$v_{\mathrm{gs}}(t_{\mathrm{Delay}}) = V_{\mathrm{T}} = V_{\mathrm{GH}} + (V_{\mathrm{GL}} - V_{\mathrm{GH}})e^{\frac{-t}{\tau_{\mathrm{g}}}}$$

$$V_{\mathrm{T}} = V_{\mathrm{GH}} + (V_{\mathrm{GL}} - V_{\mathrm{GH}})e^{\frac{-t}{\tau_{\mathrm{g}}}}$$

$$\frac{V_{\mathrm{GH}} - V_{\mathrm{T}}}{V_{\mathrm{GH}} - V_{\mathrm{GL}}} = e^{\frac{-t}{\tau_{\mathrm{g}}}}$$

$$\tau_{\mathrm{g}} \cdot \ln \frac{V_{\mathrm{GH}} - V_{\mathrm{GL}}}{V_{\mathrm{GH}} - V_{\mathrm{T}}} = t = t_{\mathrm{Delay}} \tag{2.14}$$

According to (2.14), the time constant τ_{g}, which is directly function of the input capacitance $\mathrm{C_{iss}}$ and the total gate resistance ($R = R_s + R_g$), has a major impact on the delay time. Moreover, higher positive and negative gate driving voltage results in a faster increase in gate-source capacitance to reach the threshold voltage. A higher threshold voltage tends to increase the delay time. The effect of the parameters on the delay time ($\mathrm{t_{Delay}}$) is illustrated below.

$$t_{\mathrm{Delay}} \uparrow \text{ when } \begin{cases} R \uparrow = R_{\mathrm{s}} \uparrow \text{ or } R_{\mathrm{g}} \uparrow \\ C_{\mathrm{iss}} \uparrow = C_{\mathrm{gd}} \uparrow \text{ or } C_{\mathrm{gs}} \uparrow \\ V_{\mathrm{GH}} \downarrow \\ V_{\mathrm{GL}} \downarrow \\ V_{\mathrm{T}} \uparrow \end{cases}$$

Fig. 2.9 gives a general representation of the first turn-on interval of MOSFETs based on (2.14) given the established assumptions and negligence of the common source inductance $\mathrm{L_s}$.

Equations 2.14 and 2.15 represent the switching equations of the first sub-interval without and with the common source inductance respectively. Comparison between these equations allows observing the impact of neglecting the common source inductance $\mathrm{L_s}$ on the first switching interval of MOSFETs. For comparison purposes in a real situation, characteristics of the Si MOSFET IPW65R080CFDA (Infineon Technologies AG, 2012) were used as the reference model at a supply voltage of 325V. The final representation of the complete mathematical development considering the common source inductance is derived in (2.15). The complete mathematical development is presented in Appendix I,

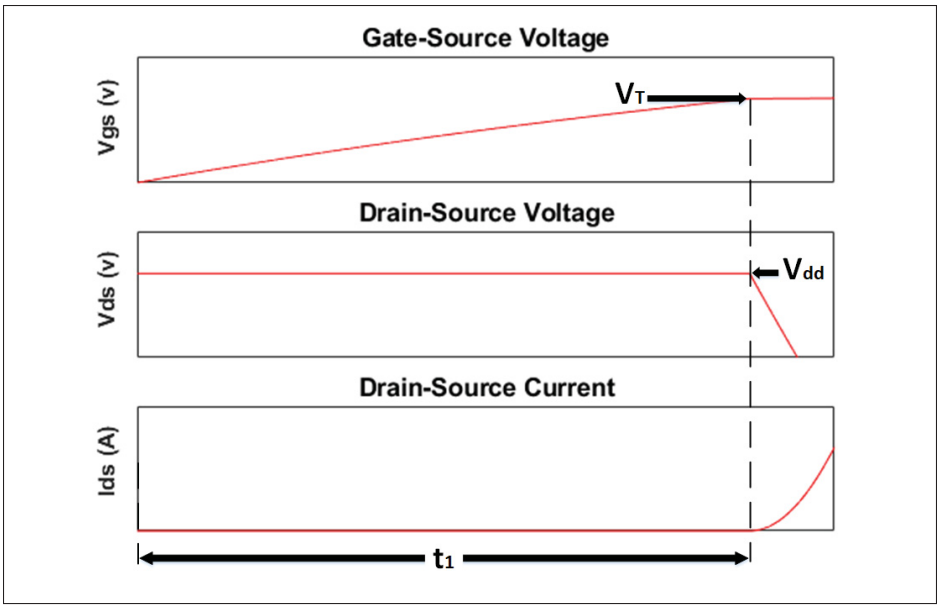

Figure 2.9 Expected waveforms of MOSFET's
Transient Analysis for the 1st turn-on interval
Simulation results based on equations of Clemente *et al.* (1982)

$$\mathscr{L}^{-1}\{v_{gs}(s)\} = v_{gs}(t) = V_{GH} + \frac{(V_{GH} - V_{GL})\left(\tau_g - \sqrt{\tau_g{}^2 - 4L_sC_{iss}}\right)}{2\sqrt{\tau_g{}^2 - 4L_sC_{iss}}} e^{-\left(\frac{\tau g + \sqrt{\tau g^2 - 4L_sC_{iss}}}{2L_sC_{iss}}\right)t} + \frac{(V_{GL} - V_{GH})\left(\tau_g + \sqrt{\tau_g{}^2 - 4L_sC_{iss}}\right)}{2\sqrt{\tau_g{}^2 - 4L_sC_{iss}}} e^{-\left(\frac{\tau g - \sqrt{\tau g^2 - 4L_sC_{iss}}}{2L_sC_{iss}}\right)t} \tag{2.15}$$

Fig. 2.10 shows a comparison between waveforms from simplified equation of 2.14 and complete equation of 2.15 for the first turn-on sub-interval. First, both equations give identical responses for an absence of the common source inductance L_s. Then, as L_s increase to a maximum simulated value of 50 nH, the delay time of the first interval increase by 14.54%. The inductance tends to limit the speed of change of the current, as noticeable for the gate circuit in the first switching interval. An even higher value of inductance in the gate circuit or common source inductance would affect to increase even more the duration of this interval. Since there is no

drain current yet, there are no losses from the drain circuit at this interval, and this inductance does not influence the MOSFET's behavior at this point. However, this is very different for intervals with a change in the drain current. Moreover, considering the total gate inductance for this interval is useful to determine the maximum frequency at which the MOSFET could be commuted without causing accidental momentary shoot-through in a commutation leg.

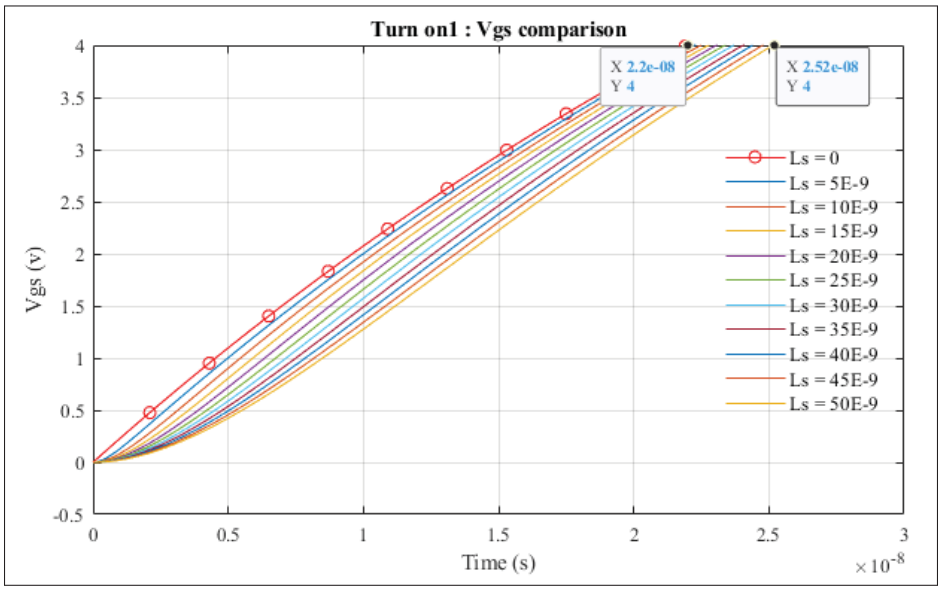

Figure 2.10 Comparison between Vgs computed with the abbreviated equation 2.14 and the complete equation 2.15 for L_s between 5nH and 50nH

2.4.2.2 Turn-On 2nd Interval: Main Transition Period

When the gate voltage $v_{gs}(t)$ approaches the threshold voltage V_T, the MOSFET drain current starts increasing gradually as the transconductance follows a linear approximation. Thus, the current deviates from the freewheeling diode in parallel to the load inductance toward the MOSFET drain. Since the freewheeling diode is still active until all the current deviates through the MOSFET, v_{ds} is kept at V_{dd} + 0.7V, because it implies a perfect diode behavior, then it means that v_{ds} is no longer equal to $v_{d's'}$. As the drain current increases, the voltage drops across $v_{d's'}$ because of the unclamped inductance. The change in voltage across the MOSFET results in a voltage drop across the Miller capacitance C_{gd} that pulls the gate current through it. This gate current switch between the gate-source and Miller capacitance and slows down even

more the turn-on process. This second sub-interval of the turn-on is critical because the voltage across the MOSFET is high and the current is increasing rapidly which results in high losses. If the unclamped inductance is small and the gate circuit response is slow because the total gate resistance (R) is high, the drain current will reach its final value before the drain voltage could decrease far from V_{dd} + 0.7V. Inversely, if the unclamped inductance value is high and the gate circuit response is fast, the rapid variation of the drain current will result in very high voltage across the unclamped inductance meaning that the voltage across the MOSFET decreases faster than the increase in current. Then, the voltage across the MOSFET reaches its final value before the drain current. Initial conditions of the second interval are as follow.

$$v_{\mathrm{gs}}(t_{\mathrm{o}}) = V_{\mathrm{T}}$$
$$i_{\mathrm{ds}}(t_{\mathrm{o}}) = 0$$
$$v_{\mathrm{ds}}(t_{\mathrm{o}}) = v_{\mathrm{d's'}}(t_{\mathrm{o}}) = v_{\mathrm{dd}} + 0.7V$$

For the analysis, the impact of the source inductance, the drain-source capacitance, and the gate inductance are neglected to simplify the equations. Fig. 2.11 shows the equivalent circuit under analysis to assess the second turn-on interval of MOSFETs.

For this second interval of the turn-on, the drain current now rises as the drain voltage falls simultaneously. The first to reach its final value ends the interval. For simplification purposes, these equations are normally presented for four different cases as explained in (Clemente *et al.*, 1982). Based on Fig. 2.11, the following mathematical development illustrates the complete resolution of the variables of interest up to the time domain. Expressions (2.26, 2.28 and 2.30) present final time-domain equations.

$$v_{\mathrm{gg}} = V_{\mathrm{GH}} = i_{\mathrm{g}}(R_{\mathrm{s}} + R_{\mathrm{g}}) + v_{\mathrm{gs}} \tag{2.16}$$

With,

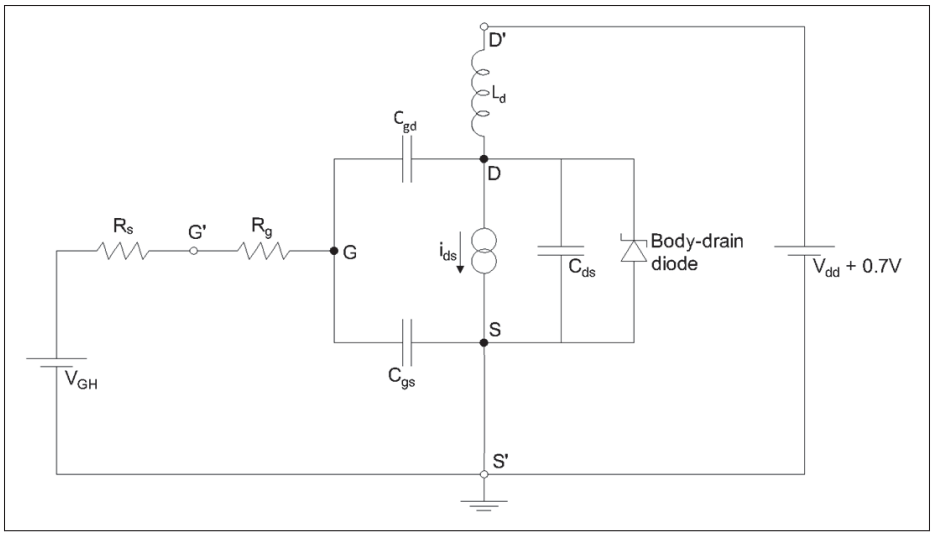

Figure 2.11 Reference model of MOSFET's transient analysis circuit for the 2nd interval of turn-on
Adapted from Grant & Gowar (1989)

$$i_g = i_{gs} + i_{gd} = C_{gs}\frac{dv_{gs}}{dt} + C_{gd}\frac{dv_{gd}}{dt} \tag{2.17}$$

and

$$R = (R_s + R_g)$$

By replacing (2.17) in (2.16), one obtain

$$RC_{gs}\frac{dv_{gs}}{dt} + v_{gs} + C_{gd}\frac{dv_{gd}}{dt} = V_{GH} \tag{2.18}$$

Then, analysis of the switching loop of Fig. 2.11 as presented below gives a way to substitute v_{gd} in (2.18).

$$v_{\mathrm{gd}} = v_{\mathrm{gs}} - V_{\mathrm{dd}} - 0.7 + V_{\mathrm{L_d}} \tag{2.19}$$

with,

$$V_{L_d} = L_d \frac{di_{ds}}{dt}$$

Considering a linear relation between the gate voltage and the current, in other words, a linear approximation of the transconductance, the drain current - gate-source voltage relation state as follows.

$$i_{ds} = \mathrm{gfs}(v_{gs} - V_T) \tag{2.20}$$

Then, the derivative of i_{ds} gives,

$$\frac{i_{\mathrm{ds}}}{dt} = \mathrm{gfs}\frac{dv_{\mathrm{gs}}}{dt} \tag{2.21}$$

Thus, by substituting the relation of the drain current and the unclamped inductance's voltage in equation (2.19), a new relation of the Miller capacitance's voltage is obtained.

$$v_{\mathrm{gd}} = L_{\mathrm{d}} \cdot \mathrm{gfs} \cdot \frac{dv_{\mathrm{gs}}}{dt} + v_{\mathrm{gs}} - V_{\mathrm{dd}} - 0.7 \tag{2.22}$$

Then, derivation of (2.22) gives,

$$\frac{dv_{\mathrm{gd}}}{dt} = L_{\mathrm{d}} \cdot \mathrm{gfs} \cdot \frac{d^2 v_{gs}}{d^2 t} + \frac{v_{gs}}{dt} \tag{2.23}$$

Using (2.23) in (2.18), the first resolvable differential equation of the circuit state as follow.

$$RC_{\mathrm{gs}}\frac{dv_{\mathrm{gs}}}{dt} + v_{\mathrm{gs}} + RC_{\mathrm{gd}}\left(L_{\mathrm{d}}\mathrm{gfs}\frac{d^2v_{gs}}{d^2t} + \frac{dv_{gs}}{dt}\right) = V_{GH}$$

$$\left(RC_{\mathrm{gd}}L_{\mathrm{d}}\mathrm{gfs}\right)\frac{d^2v_{gs}}{d^2t} + RC_{\mathrm{iss}}\frac{dv_{\mathrm{gs}}}{dt} + v_{gs} - V_{GH} = 0 \tag{2.24}$$

With Laplace transformation of (2.24), one gets

$$\begin{aligned}\mathscr{L}\{f(t)\} = F(s) = (RC_{gd}L_d\mathrm{gfs})(s^2v_{gs}(s) - sv_{gs}(0) - v_{gs}(0))+\\ RC_{iss}(sv_{gs}(s) - v_{gs}(0)) + v_{gs}(s) - \frac{V_{GH}}{s} = 0\end{aligned} \tag{2.25}$$

With initial conditions on v_{gs} defined as follow :

$$v_{gs}(0) = V_T$$
$$v'_{gs}(0) = 0$$

To simplify the resolution of the differential equation (2.25), the initial rate of change of the gate-source voltage is considered to be null at the beginning of the 2nd interval. In most cases, the rate of change of $\mathrm{v_{gs}}$ would be highly reduced at the beginning of the interval because of the impact of the increase in drain current on the gate circuit. Considering an initial condition not equal to zero would only slightly affect the transient between the first and the second interval while complicating the analytic resolution without adding a considerable change to the result. Substitution of the initial conditions in (2.25) yields

$$(RC_{gd}L_d\mathrm{gfs})(s^2v_{gs}(s) - sV_T) + RC_{iss}(sv_{gs}(s) - V_T) + v_{gs}(s) - \frac{V_{GH}}{s} = 0$$

Then, it gives the differential equation of the gate-source voltage in Laplace domain

$$v_{gs}(s) = \frac{(RC_{gd}L_d\text{gfs}V_T)s^2 + (RC_{iss}V_T)s + V_{GH}}{s((RC_{gd}L_d\text{gfs})s^2 + (RC_{iss})s + 1)}$$

$$v_{gs}(s) = \frac{(RC_{gd}L_d\text{gfs}V_T)s^2 + (RC_{iss}V_T)s + V_{GH}}{s((RC_{gd}L_d\text{gfs})s^2 + (\tau_g)s + 1)} \tag{2.26}$$

With the relation of the gate-source voltage in the Laplace domain presented as equation 2.26, the expression of the drain current and drain-source voltage can be defined as follow. First, Laplace transform of (2.20) gives the following relation.

$$i_{ds} = (\text{gfs})v_{gs} - \frac{V_T}{s} \tag{2.27}$$

By replacing v_{gs} from (2.26) in (2.27), one get the relation of the drain current in Laplace domain.

$$i_{ds}(s) = \frac{(RC_{gd}L_d\text{gfs}^2V_T)s^2 + (RC_{iss}\text{gfs}V_T)s + \text{gfs}V_{GH}}{s((RC_{gd}L_d\text{gfs})s^2 + (\tau_g)s + 1)} - \frac{V_T}{s}$$

$$i_{ds}(s) = \frac{(RC_{gd}L_d\text{gfs}V_T)(\text{gfs}-1)s^2 + (\tau_g V_T)(\text{gfs}-1)s + (\text{gfs}V_{GH} - V_T)}{s((RC_{gd}L_d\text{gfs})s^2 + (\tau_g)s + 1)} \tag{2.28}$$

Similarly, analysis of the equivalent circuit of the 2nd interval of Fig. 2.11 gives the mathematical relation of the drain-source voltage in the Laplace domain as follow.

$$v_{ds}(s) = -L_d \cdot s \cdot i_{ds}(s) + \frac{V_{dd}}{s} + \frac{0.7}{s} \tag{2.29}$$

By substituting equation (2.28) in (2.29), the relation of the drain-source voltage in Laplace domain can be defined as follow.

$$v_{ds}(s) = -L_d\left(\frac{(RC_{gd}L_d\text{gfs}V_T)(\text{gfs}-1)s^2 + (\tau_g V_T)(\text{gfs}-1)s + (\text{gfs}V_{GH} - V_T)}{(RC_{gd}L_d\text{gfs})s^2 + (\tau_g)s + 1}\right) + \frac{V_{dd}+0.7}{s}$$

The final representation of the drain-source voltage in the Laplace domain is illustrated as (2.30) under two distinct terms for aesthetic reason.

$$v_{ds}(s) = \frac{(RC_{gd}L_d^2\text{gfs}V_T)(1-\text{gfs})s^3 + (L_d\tau_g V_T(1-\text{gfs}) + RC_{gd}L_d\text{gfs}(V_{dd}+0.7))s^2}{s((RC_{gd}L_d\text{gfs})s^2 + (\tau_g)s + 1)} + \frac{(L_dV_T - L_d\text{gfs}V_{GH} + \tau_g(V_{dd}+0.7))s + (V_{dd}+0.7)}{s((RC_{gd}L_d\text{gfs})s^2 + (\tau_g)s + 1)} \tag{2.30}$$

Equations (2.26, 2.28 and 2.30) are the final Laplace representation of respectively the gate-source voltage, drain-source current and drain-source voltage for the second turn-on switching interval of MOSFETs. The inverse Laplace of these equations have been solved with Matlab, temporal expressions are stated as follow.

$$v_{gs}(t) = V_{GH} - \frac{f_1(t)(C_{gd}\text{gfs}L_dRV_{GH} - C_{gd}\text{gfs}L_dRV_T)e^{-\frac{C_{iss}t}{2C_{gd}\text{gfs}L_d}}}{C_{gd}\text{gfs}L_dR} \tag{2.31}$$

Where

$$f_1(t) = \cosh\left(\frac{t\sqrt{\frac{RC_{iss}^2}{4} - C_{gd}\text{gfs}L_d}}{C_{gd}\text{gfs}L_d\sqrt{R}}\right) + \frac{C_{gd}\text{gfs}L_d\sqrt{R}\cdot\sinh\left(\frac{t\sqrt{\frac{RC_{iss}^2}{4} - C_{gd}\text{gfs}L_d}}{C_{gd}\text{gfs}L_d\sqrt{R}}\right)\left(\frac{RC_{iss}V_{GH} - RC_{iss}V_T}{C_{gd}\text{gfs}L_dRV_{GH} - C_{gd}\text{gfs}L_dRV_T} - \frac{C_{iss}}{2C_{gd}\text{gfs}L_d}\right)}{\sqrt{\frac{RC_{iss}^2}{4} - C_{gd}\text{gfs}L_d}}$$

Then

$$i_{ds}(t) = \text{gfs}(V_{GH} - V_T) - \frac{f_2(t)(C_{gd}\text{gfs}^2 L_d R V_{GH} - C_{gd}\text{gfs}^2 L_d R V_T) e^{-\frac{C_{iss}t}{2C_{gd}\text{gfs}L_d}}}{C_{gd}\text{gfs}L_d R} \tag{2.32}$$

Where

$$f_2(t) = \cosh\left(\frac{t\sqrt{\frac{RC_{iss}^2}{4} - C_{gd}\text{gfs}L_d}}{C_{gd}\text{gfs}L_d\sqrt{R}}\right) + \frac{C_{gd}\text{gfs}L_d\sqrt{R}\cdot\sinh\left(\frac{t\sqrt{\frac{RC_{iss}^2}{4} - C_{gd}\text{gfs}L_d}}{C_{gd}\text{gfs}L_d\sqrt{R}}\right)\left(\frac{RC_{iss}V_{GH}\text{gfs} - RC_{iss}V_T\text{gfs}}{C_{gd}\text{gfs}^2 L_d R V_{GH} - C_{gd}\text{gfs}^2 L_d R V_T} - \frac{C_{iss}}{2C_{gd}\text{gfs}L_d}\right)}{\sqrt{\frac{RC_{iss}^2}{4} - C_{gd}\text{gfs}L_d}}$$

And finally

$$v_{ds}(t) = V_{dd} - \frac{2\sinh\left(\frac{t\sqrt{RC_{iss}^2 - 4C_{gd}\text{gfs}L_d}}{2C_{gd}\text{gfs}L_d\sqrt{R}}\right)(\text{gfs}L_d V_{GH} - \text{gfs}L_d V_T) e^{-\frac{C_{iss}t}{2C_{gd}\text{gfs}L_d}}}{\sqrt{R}\sqrt{RC_{iss}^2 - 4C_{gd}\text{gfs}L_d}} + \frac{7}{10} \tag{2.33}$$

These equations are typically presented for four different cases as explained in (Clemente *et al.*, 1982). These different cases are related to the ratio between the impact of the unclamped inductance and the drive circuit on the switching behavior. If the unclamped inductance is very small, the change in MOSFET's voltage during this interval will be negligible, then the freewheeling diode is going to stay in conduction until the MOSFET reaches its full conduction. Table 2.2 illustrates the conditions used to determine which set of equations for the second turn-on interval from (Clemente *et al.*, 1982) that will provide the best approximation.

Table 2.2 Condition Evaluation's Equations of 2nd Turn-On Switching Interval Taken from Clemente *et al.* (1982)

Small L_d/R	**Intermediate Low L_d/R**	**Intermediate High L_d/R**	**Large L_d/R**
$\frac{L_d}{R} < \frac{C_{gs}{}^2}{10C_{gd}gfs}$	$\frac{L_d}{R} < \frac{C_{gs}{}^2}{4C_{gd}gfs}$	$\frac{L_d}{R} > \frac{C_{gs}{}^2}{4C_{gd}gfs}$	$\frac{L_d}{R} > \frac{10C_{gs}{}^2}{C_{gd}gfs}$

A large unclamped inductance means a slow rate of change of drain current, while small driving resistance means fast gate circuit response. For the small ratio case, the potential rate of change of the drain current is much faster than the drive circuit. It is similar to have a really slow gate drive that could be represented by a very large gate resistance for a relatively low unclamped inductance. Inversely, for the large ratio case, the "Miller Effect" from the high unclamped inductance predominates and decreases the rate of change of the gate-source voltage. It means that the switching speed is severely limited by the constraints of the drain circuit, while the drive circuit is too fast for the drain circuit. However, extremums scenarios are unlikely to be observed in real switching configuration. Consequently, both intermediate cases are favorable since they might be considered as a "correct" design configuration meaning that the gate circuit is neither too fast nor too slow for the drain circuit (Clemente *et al.*, 1982). Fig. 2.12 gives a general representation of the expected waveforms for the gate-source voltage, drain-source voltage and drain current during the second interval of turn-on. The drain current rises as the drain voltage falls simultaneously, which of these events is completed first ends the interval by either reaching the load current I_o or the drain-source voltage reaches $i_{ds} \times R_{ds(on)}$, meaning that the gate circuit is no longer limiting the increase in drain current.

Since the mathematical relations developed by International Rectifier (Clemente *et al.*, 1982) are used as the reference model for the simulation, and that only intermediate scenarios are relevant to real switching observations of the 2nd turn-on interval, only equations related to both intermediate cases from (Clemente *et al.*, 1982) are presented. Intermediate low scenario's equations are stated as follow.

$$v_{gs}(t) = V_T + V_F - \frac{V_F}{(T_1 - T_2)}\left(T_1 e^{\frac{-t}{T_1}} - T_2 e^{\frac{-t}{T_2}}\right) \tag{2.34}$$

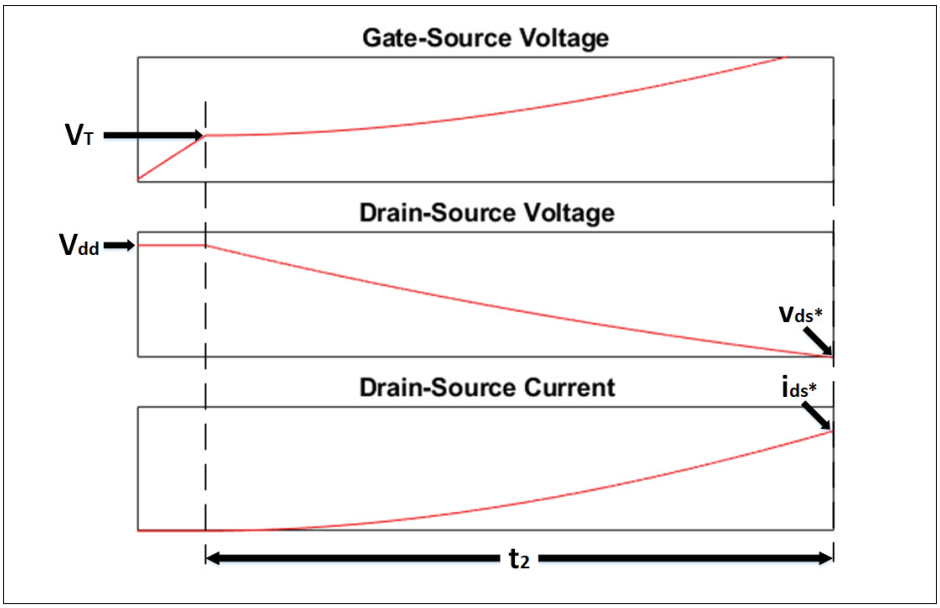

Figure 2.12 Expected waveforms of MOSFET's transient analysis for the 2nd turn-on interval
Simulation results based on equations of Clemente *et al.* (1982)

$$i_{ds}(t) = \text{gfs}V_F\left(1 - \frac{1}{(T_1 - T_2)}\right)\left(T_1 e^{\frac{-t}{T_1}} - T_2 e^{\frac{-t}{T_2}}\right) \tag{2.35}$$

$$v_{ds}(t) = V_{dd} - \left(\frac{\text{gfs}V_F L_d}{(T_1 - T_2)}\right)\left(e^{\frac{-t}{T_2}} - e^{\frac{-t}{T_1}}\right) \tag{2.36}$$

Where $T1$ and $T2$ are defined by (2.37) and (2.38) from (Clemente *et al.*, 1982).

$$T_1 = \frac{2L_d C_{gd} R\text{gfs}}{RC_{gs} + \sqrt{R^2 C_{gs}^2 - 4L_d C_{gd} R\text{gfs}}} \tag{2.37}$$

$$T_2 = \frac{2L_d C_{gd} R\text{gfs}}{RC_{gs} - \sqrt{R^2 C_{gs}^2 - 4L_d C_{gd} R\text{gfs}}} \tag{2.38}$$

Then, intermediate high scenario's equations are stated as follow from (Clemente *et al.*, 1982).

$$v_{gs}(t) = V_T + V_F - V_F e^{\frac{-t}{T_3}} \left(\cos \omega_3 t + \frac{\sin \omega_3 t}{\omega_3 T_3} \right) \tag{2.39}$$

$$i_{ds}(t) = \text{gfs} V_F - \text{gfs} V_F e^{\frac{-t}{T_3}} \left(\cos \omega_3 t + \frac{\sin \omega_3 t}{\omega_3 T_3} \right) \tag{2.40}$$

$$v_{ds}(t) = V_{dd} - \text{gfs} V_F \omega_3 L_d e^{\frac{-t}{T_3}} \left(1 + \frac{1}{\omega_3^2 T_3^2} \right) \sin \omega_3 t \tag{2.41}$$

Where $T3$ and ω_3 are defined by Eq.2.42 and 2.43 from (Clemente *et al.*, 1982).

$$T_3 = \frac{2 L_d C_{gd} \text{gfs}}{C_{gs}} \tag{2.42}$$

$$\omega_3 = \frac{\sqrt{4 L_d C_{gd} R \text{gfs} - \text{R}^2 \text{C}_{\text{gs}}^2}}{2 L_d C_{gd} R \text{gfs}} \tag{2.43}$$

Fig. 2.13 to 2.20 are illustrating the behavior of the Silicon MOSFET IPW65R080CFDA at 325V with a nominal load current of 10A (Infineon Technologies AG, 2012) under fixed or varying gate resistance and unclamped drain inductance. Comparison is made between IRF's equations 2.34 to 2.41 (Clemente *et al.*, 1982) and the complete set of 3$^{\text{rd}}$ order equations, respectively (2.26), (2.30) and (2.28) at a fixed gate resistance of 10Ω and a total unclamped inductance of 100nH for validation of the 3$^{\text{rd}}$ order's equations. Based on IRF's equations, this configuration is related to the intermediate high scenario because the unclamped inductance has a significant impact on the turn-on process.

Two different simulation scenarios are presented on Fig. 2.13 to 2.16 then on Fig. 2.17 to 2.20 respectively, to illustrate the impact of the gate resistance and the unclamped inductance on the second interval of the turn-on process. In each simulations, waveforms of the gate-source

voltage v_{gs}, drain-source voltage v_{ds}, drain current i_{ds} and the total energy of the interval are presented.

For the first simulation case of Fig. 2.13 to 2.16, results from the 3rd order equations for a fixed unclamped inductance value of 100nH and a total gate resistance varying from 1Ω to 50Ω present the impact of the gate resistance on the 2nd turn-on switching interval.

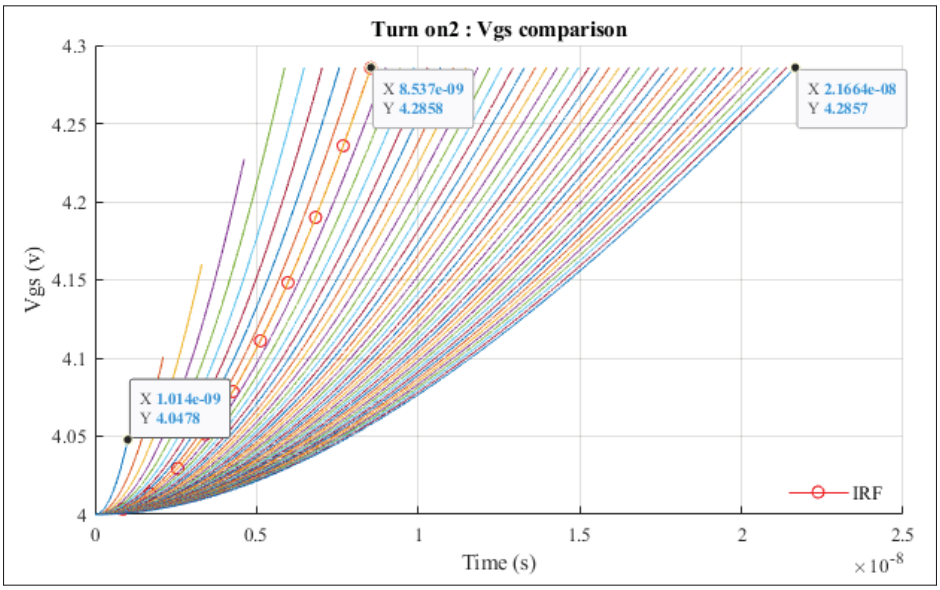

Figure 2.13 2nd Turn-on interval: v_{gs} comparison for total gate resistance from 1Ω to 50Ω by increments of 1Ω (left to right) with L_d = 100nH

As shown in Figs. 2.13 to 2.16, as the total gate resistance increases, the second interval of the turn-on process tends to last longer due to lower gate current and slower gate-source capacitance charging. Inversely, for a very low gate resistance value, the gate-source capacitance tends to charge quickly because of the high gate current which results in high drain current slope. This high drain current slope causes a very fast decrease of the drain-source voltage because of the unclamped inductance L_d. As a result, the drain-source voltage reaches its final value of $R_{ds(on)} \times i_{ds}$ before the drain current could reach its final value. This case is known as the intermediate-large or large case from (Clemente *et al.*, 1982), where the gate circuit is fast and the impact of the unclamped inductance is not negligible. For a very low gate resistance

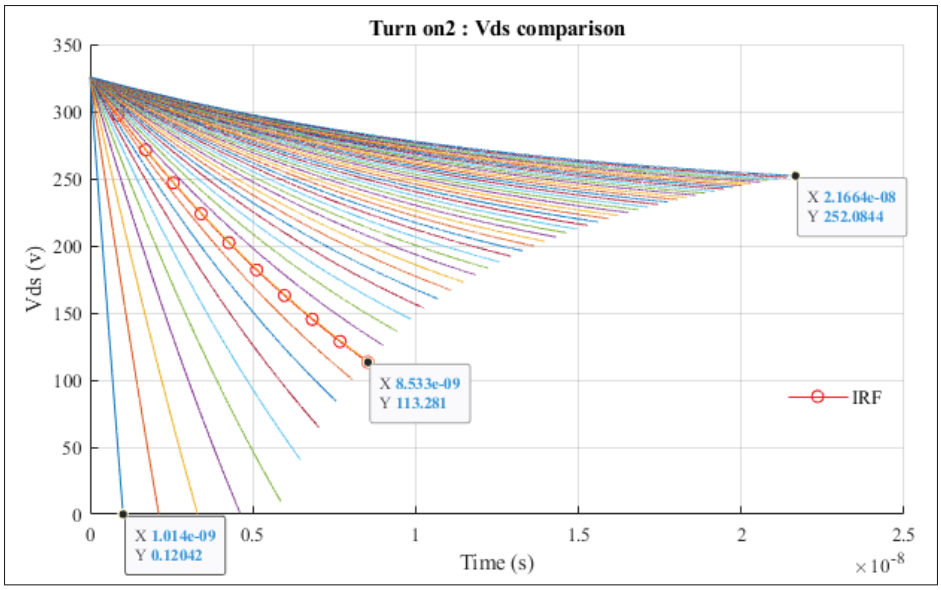

Figure 2.14 2nd Turn-on interval: v_{ds} comparison for total gate resistance from 1Ω to 50Ω by increments of 1Ω (left to right) with L_d = 100nH

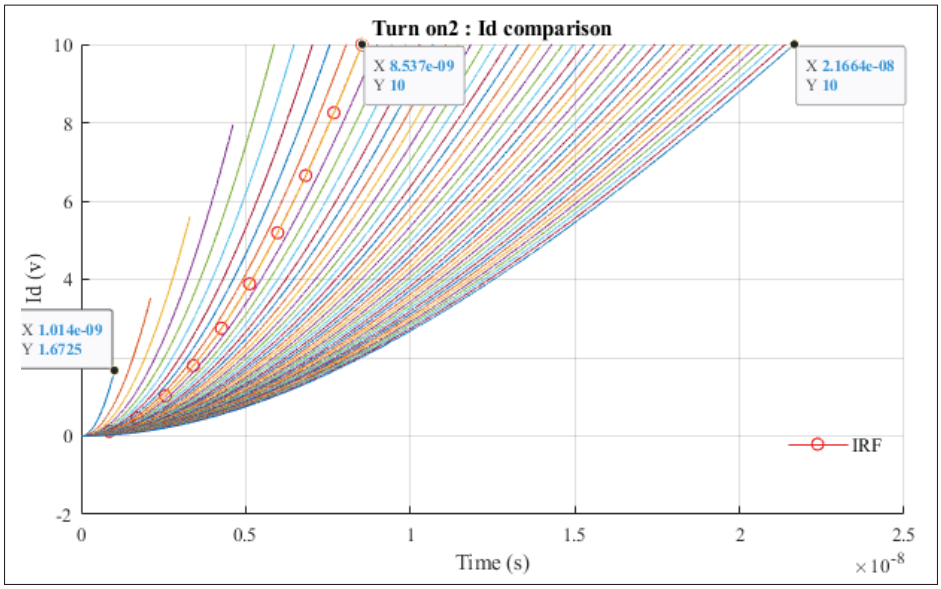

Figure 2.15 2nd Turn-on interval: i_{ds} comparison for total gate resistance from 1Ω to 50Ω by increments of 1Ω (left to right) with L_d = 100nH

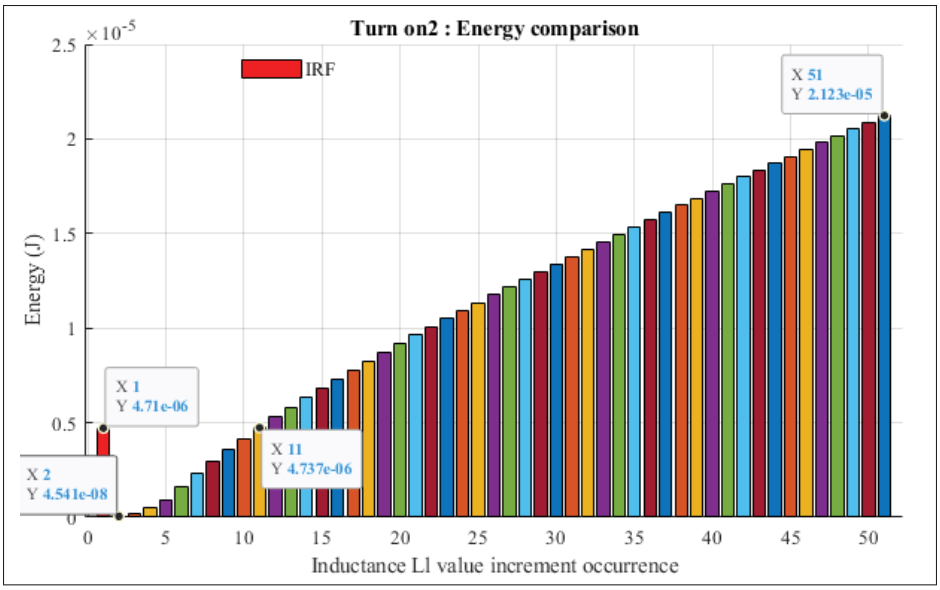

Figure 2.16 2nd Turn-on interval: energy comparison for total gate resistance from 1Ω to 50Ω by increments of 1Ω (left to right) with L_d = 100nH

and very high unclamped inductance, the drain-source voltage is expected to reach its final value before the current did. For this particular case, the final value of the drain current and gate-source voltage is only slightly over their initial values because of the very fast decrease of the drain-source voltage. However, $v_{d's'}$ is kept at V_{dd} plus 0.7V until the MOSFET reaches its full conduction. In another word, the total voltage is fixed until the current flowing through the freewheeling diode is null.

Moreover, by comparing the evolution of v_{gs} of the second interval in Fig. 2.13 with its evolution during the first interval in Fig. 2.10, the rate of change of the gate-source voltage during the 2_{nd} turn-on interval is highly decreased. When the voltage changes across the MOSFET as observed for this second interval, the voltage also changes across the Miller capacitance C_{gd} which drags some of the gate currents through it, resulting in a major reduction of the gate current charging the gate-source capacitance. A fast gate circuit and a high unclamped inductance slow down the gate charging in this second interval.

Then, as the gate resistance increases, the gate circuit response gets slower until the drain current reaches its final value before $R_{ds(on)}$ gets to its nominal conduction value. High gate resistance and slow gate circuit will result in a reduced rate of change of the gate-source capacitance voltage. Consequently, this slow increase in the gate-source voltage results in a slow rate of change of the drain current, reducing the impact of the unclamped inductance on the Miller capacitance and gate circuit.

For this second interval, a faster gate circuit means reduced losses. The voltage across the MOSFET decreases very quickly with a reduced gate configuration without allowing the drain current to reach high values. However, the drain-source voltage plus the voltage across the unclamped inductance ($v_{d's'}$) has to be maintained at V_{dd} plus 0.7V to keep the freewheeling diode in conduction until all the current flows through the MOSFET. Thus, the energy not dissipated by the MOSFET is stored in the unclamped inductance which will inevitably dissipate its energy in the following interval.

Although these waveforms provide a good approximation of the second interval of the switching, none of the analytical expressions takes into account the non-linear behavior of the internal capacitances. The Miller capacitance C_{gd} increases drastically when the drain-source voltage falls under the gate-source voltage. As a result of this sharp increase, the rate of fall of the drain voltage is quite reduced which could significantly increase losses of this interval in its last moments (Grant & Gowar, 1989).

Then, for the second simulation case presented on Fig. 2.17 to 2.20, the gate resistance is fixed at 10Ω and the unclamped inductance value vary from 1nH to 500nH. Comparison is also made with IRF's equations (Clemente *et al.*, 1982) with a gate resistance of 10Ω and an unclamped inductance L_d of 100nH.

As shown in Figs. 2.17 to 2.20, for a very low value of the unclamped inductance, the drain-source voltage is firmly steady at V_{dd} plus 0.7V until the current reaches its final value. Moreover, there is no significant slowdown of the gate driving circuit under low inductance configurations. As the unclamped inductance is increased, its influence on both the drain-source voltage and the

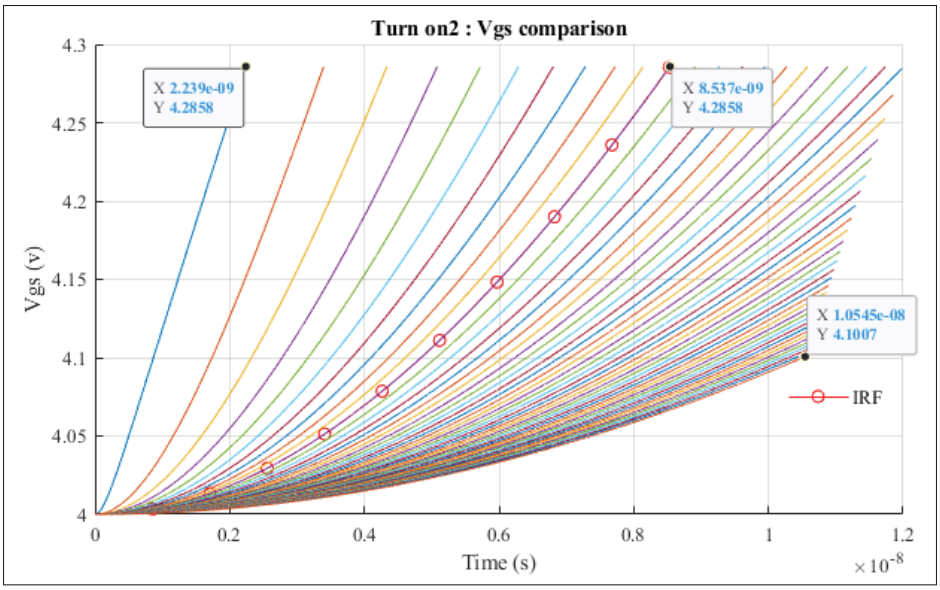

Figure 2.17 2nd Turn-on interval: v_{gs} comparison for total unclamped inductance from 1nH to 500nH by increments of 10nH (left to right) with R = 10 Ω

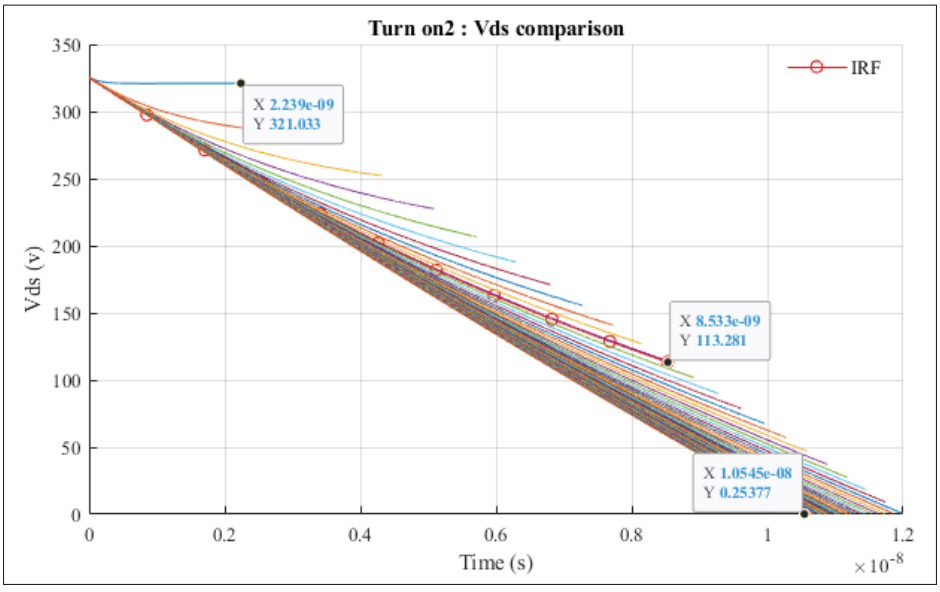

Figure 2.18 2nd Turn-on interval: v_{ds} comparison for total unclamped inductance from 1nH to 500nH by increments of 10nH (left to right) with R = 10 Ω

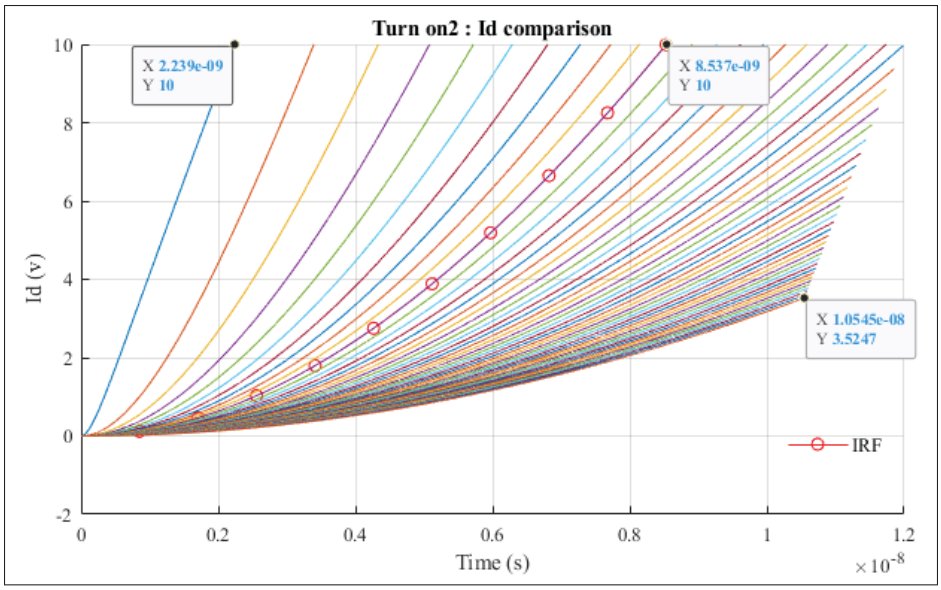

Figure 2.19 2nd Turn-on interval: i_{ds} comparison for total unclamped inductance from 1nH to 500nH by increments of 10nH (left to right) with R = 10 Ω

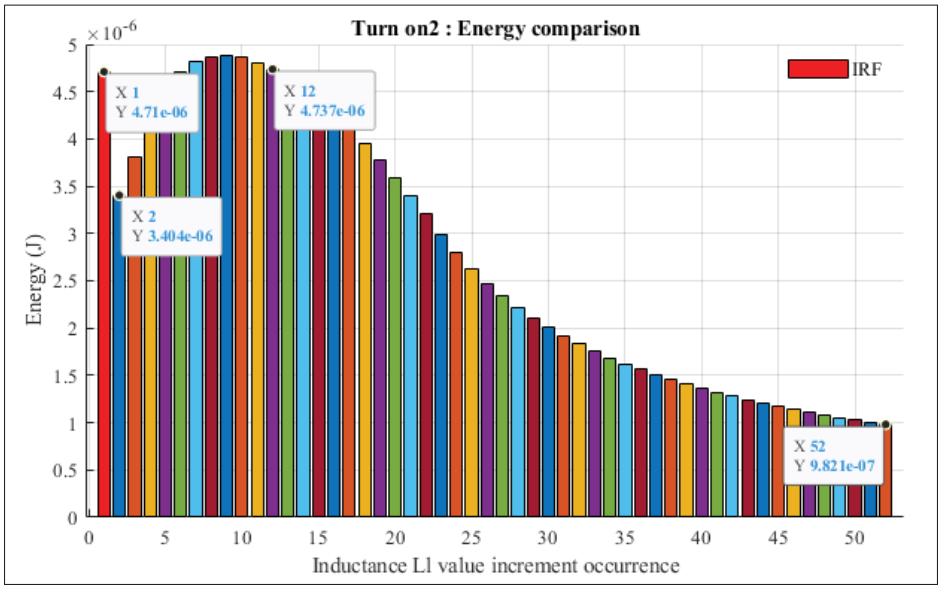

Figure 2.20 2nd Turn-on interval: Energy comparison for total unclamped inductance from 1nH to 500nH by increments of 10nH (left to right) with R = 10 Ω

gate circuit becomes very significant. However, what matters is the proportion between the speed of the gate circuit and the influence of the unclamped inductance. In other words, the proportion between the unclamped inductance and the total gate resistance dictates how the switching behaves.

As shown in Fig. 2.20, the computed MOSFET's losses of the second interval tend to decrease as the inductance value increases. As the unclamped inductance value increases, its stored energy increases and less energy is dissipated through the MOSFET during the interval. Inversely, if the inductance value is extremely low, all losses are dissipated in the MOSFET. However, for this particular non-realistic case with an unclamped inductance value under 70 nH, the total energy dissipated in the MOSFET is lower than for an intermediate unclamped inductance value. In fact, with a very low unclamped inductance value, there is no significant slowdown of the gate circuit. Inversely, a slightly higher inductance value has a direct influence on the gate circuit, causing the switching process to take longer and resulting in higher energy dissipation through the MOSFET.

Most cases illustrated in Figs. 2.13 to 2.20 are not relevant to real situations but are helpful to understand the influence of external parameters on the switching behavior. In realistic configurations, an intermediate case is expected which translates into non-extremum influence of neither the gate resistance nor the unclamped inductance. Therefore, either the drain current or the drain voltage could reach its final value, but neither will stay close to their initial values.

Equations of third-order provide very similar results compared to equations proposed by IRF. However, IRF's equations are provided for a known condition of the proportion between the unclamped inductance and gate resistance. Thus, for external parameters almost in-between two possible conditions as listed in Table 2.2, two different sets of equations with different simplifications are obtained for a slight difference of the external parameters. Then, different results for a minor difference in the external parameters are obtained. The third-order equations are harder to implement on computational software, but only one set of the equation have to be implemented, without worrying about external parameters proportions. Since the objective

is to simulate the switching behavior of MOSFETs under realistic scenarios, there is no need to further develop high-order equations to gain only a little in precision. Then, for all other switching intervals, equations from (Clemente *et al.*, 1982) will be used as the reference model.

2.4.2.3 Turn-On 3rd Interval: Complement Of The Main Transition Period

Depending on the outputs of the second interval, the 3rd turn-on interval consists of the completion of the voltage fall or the increase of the drain current to its nominal value. First, let's consider the case where the voltage continues to collapse. At the beginning of the interval, the drain-source voltage (v^*_{ds}) is located between the supply voltage v_{dd} and the conduction voltage whilst the drain current is at the nominal current (I_0). Since the drain current is constant and the drain-source voltage is falling quickly, the gate-source voltage is also considered constant because most of the gate current flows in the Miller capacitance (C_{gd}) (Clemente *et al.*, 1982). Fig. 2.21 illustrates an approximation of the switching waveforms during the fall of the drain-source voltage based on IRF's equations (Clemente *et al.*, 1982). Equations from (Clemente *et al.*, 1982) for the 3^{rd} turn-on interval are stated as follows for the drain-source voltage fall.

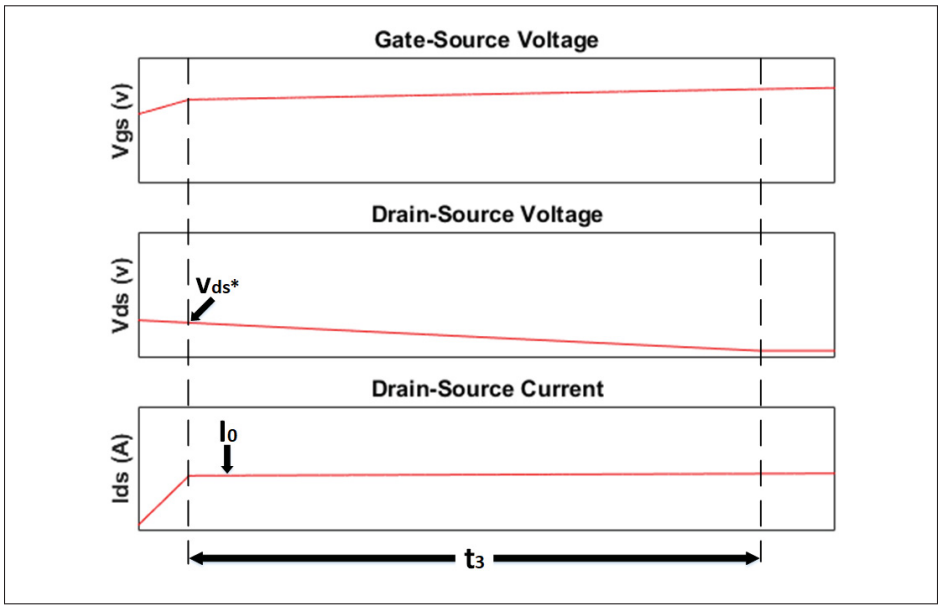

Figure 2.21 Expected waveforms of MOSFET's transient analysis for the 3rd turn-on interval : The Drain-Source Voltage Fall Simulation results based on equations of Clemente *et al.* (1982)

$$v_{gs} = V_T + \frac{I_0}{\text{gfs}} \tag{2.44}$$

$$i_{ds} = I_0 \tag{2.45}$$

$$v_{ds}(t) = v^*_{ds} - \left(\frac{V_{GH} - (V_T + I_0/\text{gfs})}{RC_{gd}}\right) t \tag{2.46}$$

Then, for the second case, the drain-source voltage has already reached its conducting value, which could be interpreted as reaching the nominal $R_{ds(on)}$. Then, the drain current completes its rise to the nominal current (I_0). Fig. 2.22 illustrates an approximation of the switching waveforms during the rise of the drain-source current based on IRF's equations (Clemente *et al.*, 1982). Equations from (Clemente *et al.*, 1982) for the 3^{rd} turn-on interval are stated as follows for the rise of the drain current case.

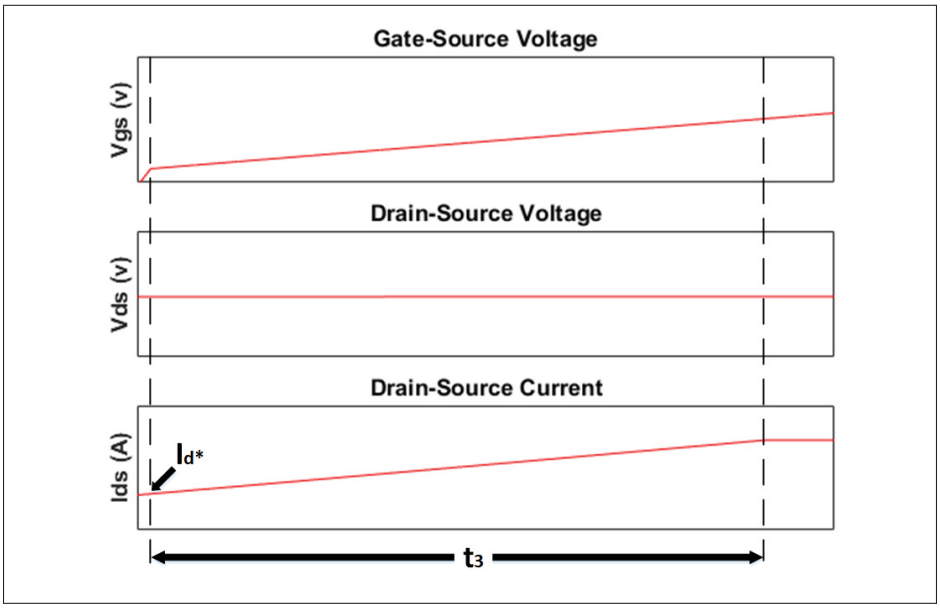

Figure 2.22 Expected waveforms of MOSFET's transient analysis for the 3rd Turn-on interval : The Rise of the Drain Current Simulation results based on equations of Clemente *et al.* (1982)

$$v_{gs}(t) = V_{GH} + \left(\frac{i_{ds}^{*}}{\text{gfs}} - V_{GH} + V_T\right) e^{-\frac{t}{\text{gfs}(C_{gd}+C_{gs})R}} \tag{2.47}$$

$$i_{ds}(t) = i_{ds}^{*} + \frac{V_{dd}}{L_d} t \tag{2.48}$$

$$v_{ds}(t) = i_{ds}(t) \cdot R_{ds(on)} \tag{2.49}$$

Then, at the end of this the 3rd turn-on interval, both the drain current and the drain-source voltage have reached their nominal value. Only the gate charge remains uncompleted, even if the MOSFET is theoretically fully turned on because the on state resistance $R_{ds(on)}$ is already at its conduction value.

2.4.2.4 Turn-On 4th Interval: Total Gate Charging

For the last turn-on interval, the gate-source voltage is not yet steady at the positive driving voltage V_{GH}, but no change occurs on both the drain current or the drain-source voltage, so no further reduction in losses. This interval is characterized by an exponential increase in the gate-source voltage similar to the first turn-on interval as illustrated in Fig. 2.23. The interval ends when the gate-source capacitance's voltage gets to the nominal turn-on driving voltage V_{GH}. Equations from (Clemente *et al.*, 1982) for the 4^{th} turn-on interval are stated as follow.

$$v_{gs}(t) = V_{GH} + (v_{gs}^{*} - V_{GH}) e^{-\frac{t}{\tau_g}} \tag{2.50}$$

$$i_{ds} = I_0 \tag{2.51}$$

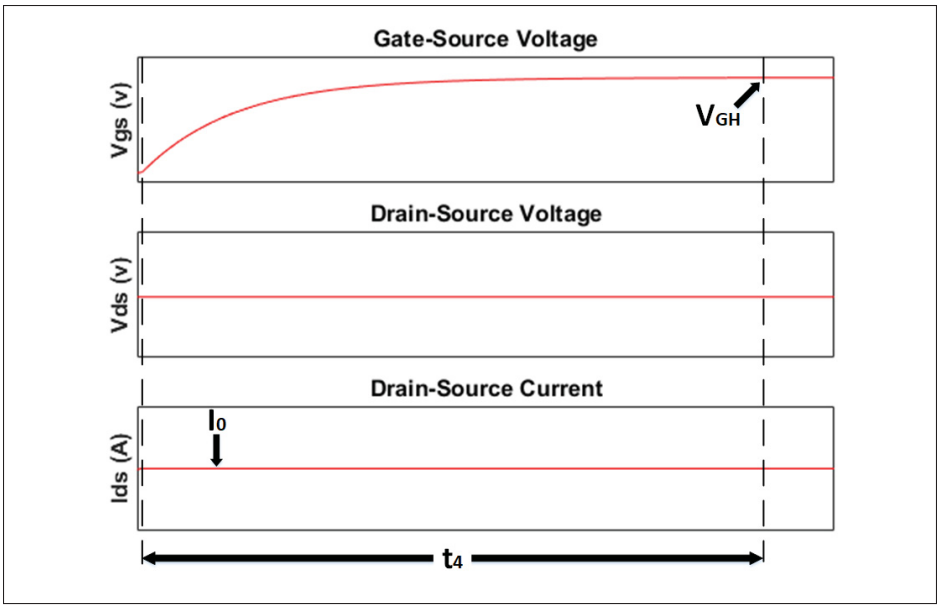

Figure 2.23 Expected waveforms of MOSFET's
transient analysis for the 4th turn-on interval
Simulation results based on equations of Clemente *et al.* (1982)

$$v_{ds} = i_{ds} \cdot R_{ds(on)} \tag{2.52}$$

The parameters stay unchanged during the conduction phase until the turn-off process starts. In real conditions, it would be required to place a resistance in series with the load inductance. Otherwise, the increase in load current would not be limited. Based on the established assumptions, the nominal current is unchanged during the switching and conduction intervals.

2.4.3 Turn-Off Intervals

For the turn-off intervals, the circuit is initially in a steady-state where the MOSFET is completely turned on. The drain voltage (v_{ds}) is equal to the conduction voltage ($I_0 \cdot R_{ds(on)}$), the drain current is equal to the nominal load current (I_0) and the gate voltage (v_{gs}) is equal to the positive driving voltage (V_{GH}). As for the turn-on process, the turn-off interval is divided into

four distinct sections as defined in (Clemente *et al.*, 1982), which is going to be the reference equations for the turn-off switching process.

2.4.3.1 1st Turn-Off Interval: The Delay Time

As for the 1st turn-on interval, the 1st turn-off interval starts with the delay time which consists of discharging the gate-source capacitance to the minimum gate-source voltage able to sustain the nominal drain current, which is normally a few volts over the threshold voltage. There are no changes in the drain voltage nor the drain current during this interval. Only the gate voltage is changing overtime at a rate determined by the time constant of the gate circuit. In physical implementations, two distinct gate driving paths are normally used, meaning that the time constant can be adjusted by having different driving resistance values for the turn-on and turn-off process. The driving voltage v_{gg} is assumed to change instantly to the turn-off driving voltage V_2 at the beginning of the interval. This assumption is justified by the rise and fall times of commercial gate drivers (typically < 10ns). Fig. 2.24 gives a general representation of this interval, and the equation of v_{gs} for the first turn-off interval from (Clemente *et al.*, 1982) is stated as (2.53).

$$v_{gs}(t) = (V_{GH} + V_2)e^{-\frac{t}{\tau_g}} - V_2 \tag{2.53}$$

The first turn-off interval ends when the gate-source voltage falls to the minimum value to keep the nominal drain current I_0 as stated by (2.54). Then, the second turn-off interval begins.

$$v_{gs} = V_T + \frac{I_0}{\text{gfs}} \tag{2.54}$$

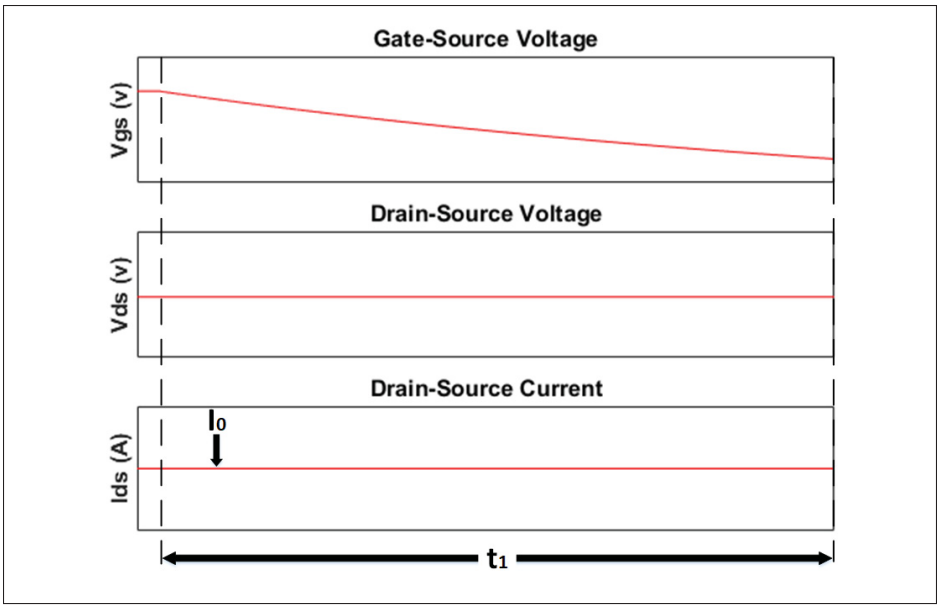

Figure 2.24 Expected waveforms of MOSFET's transient analysis for the 1st turn-off interval : The Delay Time
Simulation results based on equations of Clemente *et al.* (1982)

2.4.3.2 2nd Turn-Off Interval: The Voltage Rise

During this interval, the drain voltage rises to the supply voltage plus the forward diode polarity voltage around 1.2V whilst the drain current remains constant at the nominal current, and so is the gate-source voltage at ($V_T + I_0$/gfs). In order to decrease the drain current, the drain-source voltage of the MOSFET has to be slightly higher than the supply voltage (V_{dd}). Otherwise, the freewheeling diode cannot start conducting and the drain current cannot decrease. Since the current does not theoretically change during this phase, there is no voltage drop across the unclamped inductance, meaning that the supply voltage in addition to the forward freewheeling diode's conducting voltage has to appear through the drain source of the MOSFET. Fig. 2.25 provides a general representation of the approximation of the 2nd turn-off interval waveforms. The process is not so interspersed, but the major time-varying element is the drain-source voltage. In order to have a change in the drain-source voltage, there must be a change in the drain current through a reduction of the gate-source voltage. As the gate-source voltage continues to slightly and slowly decrease under the quasi-constant value, a slight decrease in the current results in a

fast voltage increase, which results in a fast increase of the MOSFET's drain-source voltage, forcing the freewheeling diode into conduction. The interval ends when the drain-source voltage reaches the supply voltage (V_{dd}) as stated in (Clemente *et al.*, 1982). The evolution of the drain-source voltage is characterized by (2.55) from (Clemente *et al.*, 1982) for the second turn-off interval whilst the drain current and gate-source voltage are steady as stated by (2.51) and 2.54, respectively.

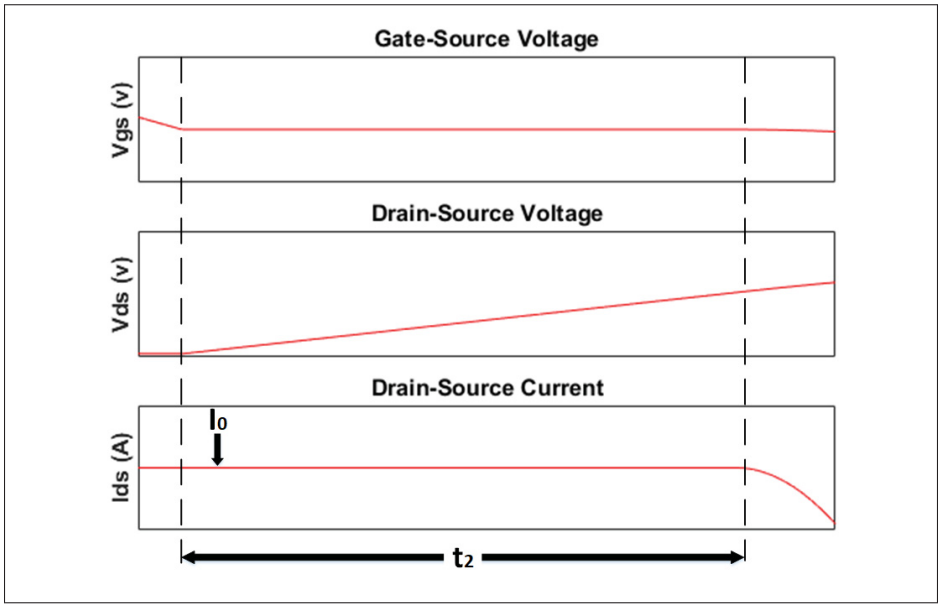

Figure 2.25 Approximated waveforms of MOSFET's transient analysis for the 2nd turn-off interval : The Voltage Rise Simulation results based on equations of Clemente *et al.* (1982)

$$v_{ds}(t) = \frac{(\frac{I_0}{\text{gfs}} + V_T + V_2)}{C_{gd}R}t \tag{2.55}$$

2.4.3.3 3rd Turn-Off Interval: The Current Fall

At the beginning of the 3rd turn-off interval, the nominal current is still flowing into the MOSFET, and the diode is about to enter in its conduction state. For the drain current to be commutated into the freewheeling diode, it is necessary that the drain voltage increase slightly above the

supply voltage (V_{dd}) to allow the diode to reach its forward conducting voltage. The voltage across the unclamped leakage inductance and load inductance must reverse in order for the current in it to reduce. A voltage-time integral must be developed for the drain current to return to zero (Clemente *et al.*, 1982). In the absence of an external voltage clamp, the MOSFET can potentially be driven into an avalanche, acting as a voltage clamp and preventing further increase of voltage due to the unclamped inductance (Clemente *et al.*, 1982).

In this third interval, both the current and voltage are changing. These two dynamics are interleaved. A change of the drain current produces a change of voltage across the unclamped inductance (L_d) which results in a current flowing through the Miller capacitance (C_{gd}). This condition reduces the rate of decrease of the gate-source voltage (C_{gs}), resulting in a slower rate of change of the drain current. As expected, the analytical solutions depend upon the ratio between the unclamped inductance (L_d) and total turn-off gate resistance (R). Table 2.3 illustrates the condition to determine which set of equations from (Clemente *et al.*, 1982) will provide the best approximation for the third turn-off interval.

Table 2.3 Condition Evaluation's Equations of 3rd Turn-Off Switching Interval Taken from Clemente *et al.* (1982)

Small L_d/R	**Intermediate Low L_d/R**	**Intermediate High L_d/R**	**Large L_d/R**
$\frac{L_d}{R} < \frac{C_{gs}^2}{10 C_{gd} gfs}$	$\frac{C_{gs}^2}{10 C_{gd} gfs} < \frac{L_d}{R} < \frac{C_{gs}^2}{4 C_{gd} gfs}$	$\frac{C_{gs}^2}{4 C_{gd} gfs} < \frac{L_d}{R} < \frac{10 C_{gs}^2}{C_{gd} gfs}$	$\frac{L_d}{R} > \frac{10 C_{gs}^2}{C_{gd} gfs}$

Because only intermediate scenarios are more likely to be found in real switching applications of the 3rd turn-off interval, only equations related to both intermediate cases from (Clemente *et al.*, 1982) are presented. Intermediate low scenario's equations are stated as follows.

$$v_{gs}(t) = \frac{\left(\frac{I_0}{gfs} + V_T + V_2\right)}{(T_1 - T_2)} \left(T_1 e^{\frac{-t}{T_1}} - T_2 e^{\frac{-t}{T_2}}\right) - V_2 \tag{2.56}$$

$$i_{ds}(t) = \frac{(I_0 + gfs(V_T + V_2))}{(T_1 - T_2)} \left(T_1 e^{\frac{-t}{T_1}} - T_2 e^{\frac{-t}{T_2}}\right) - gfs(V_T + V_2) \tag{2.57}$$

$$v_{ds}(t) = V_{dd} + \frac{(I_0 + \text{gfs}(V_T + V_2))L_d}{(T_1 - T_2)}\left(e^{\frac{-t}{T_2}} - e^{\frac{-t}{T_1}}\right) \tag{2.58}$$

Where T_1 and T_2 are unchanged from the second turn-on interval, given by (2.37) and (2.38), respectively. Then, intermediate high scenario's equations are stated as follow from (Clemente *et al.*, 1982). As for the previous case, T_3 and ω_3 are defined by (2.42) and (2.43).

$$v_{gs}(t) = \left(\frac{I_0}{\text{gfs}} + V_T + V_2\right)e^{\frac{-t}{T_3}}\left(\cos\omega_3 t + \frac{\sin\omega_3 t}{\omega_3 T_3}\right) - V_2 \tag{2.59}$$

$$i_{ds}(t) = (I_0 + \text{gfs}(V_T + V_2))e^{\frac{-t}{T_3}}\left(\cos\omega_3 t + \frac{\sin\omega_3 t}{\omega_3 T_3}\right) - \text{gfs}(V_T + V_2) \tag{2.60}$$

$$v_{ds}(t) = V_{dd} + (I_0 + \text{gfs}(V_T + V_2))\omega_3 L_d e^{\frac{-t}{T_3}}\left(1 + \frac{1}{\omega_3^2 T_3^2}\right)\sin\omega_3 t \tag{2.61}$$

Fig. 2.26 gives a general representation of the expected waveforms for the third turn-off interval. The interval ends when the drain-source current reaches zero.

However, equations presented for the third turn-off interval assume that the voltage can increase indefinitely, but in a real application, this surge voltage can reach the clamping voltage of the MOSFET and drive it into an avalanche, limiting further increase of the voltage (Clemente *et al.*, 1982). This is especially true for high unclamped inductance designs with fast gate drives. If the MOSFET cannot handle the avalanche energy, an external clamping circuit could be added to the circuit to avoid possible destruction of the device. If the clamping voltage is reached during the third turn-off interval, the drain-source voltage is kept at the clamping voltage whilst the gate-source continue to follow the same relation as presented on (2.56) or (2.59) depending on the conditions, and the drain current follows the relation of (2.62) from (Clemente *et al.*, 1982).

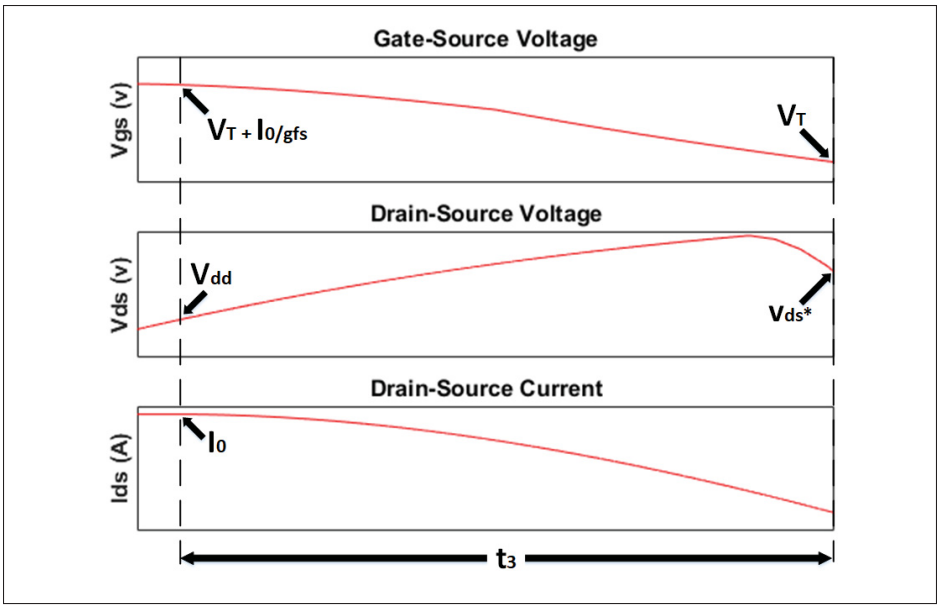

Figure 2.26 Approximated waveforms of MOSFET's transient analysis for the 3rd turn-off interval : The Current Fall Simulation results based on equations of Clemente *et al.* (1982)

$$i_{ds}(t) = I^*_{ds} - \frac{(V_{CLAMP} - V_{dd})}{L_d} t \tag{2.62}$$

2.4.3.4 4th Turn-Off Interval: The Resonance

At the end of the third turn-off interval, the drain current is back to zero, and the drain-source voltage is either over the circuit voltage or at the clamping voltage. Then, as the gate-source voltage continues to decrease following the relation of (2.53), the output capacitance (C_{oss}) resonates with the unclamped inductance, slowly damped by the stray resistance over time. Fig. 2.27 illustrate a general representation of the last turn-off interval, and equations 2.63 from (Clemente *et al.*, 1982) present the evolution of the drain-source voltage during this last switching interval.

$$v_{ds}(t) = V_{dd} + (v^*_{ds} - V_{dd}) e^{\frac{-t}{T_4}} \cos \omega_4 t \tag{2.63}$$

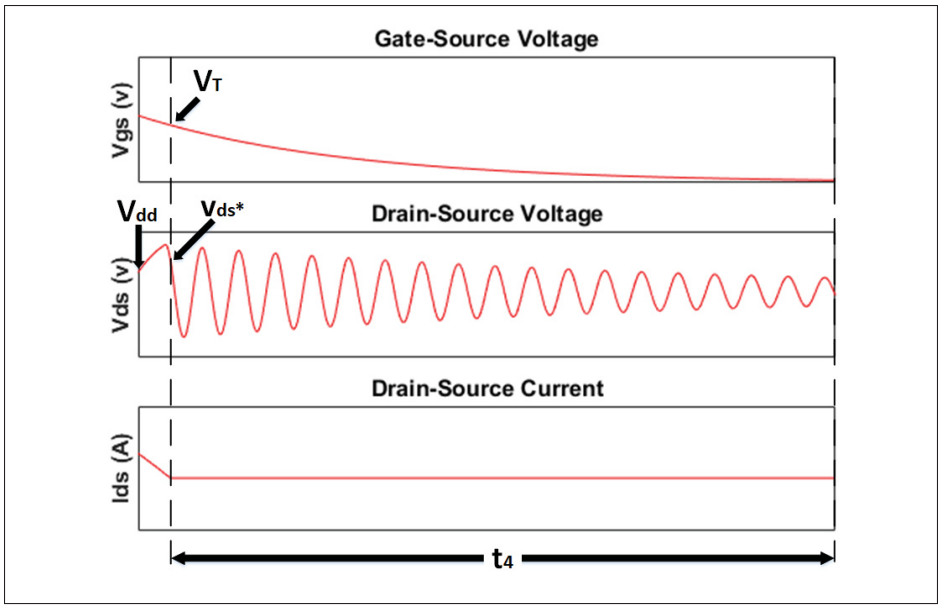

Figure 2.27 Approximated waveforms of MOSFET's transient analysis for the 4th turn-off interval : The Resonance Simulation results based on equations of Clemente *et al.* (1982)

Where $T4$ and ω_4 are defined by Eq.2.64 and 2.65 from (Clemente *et al.*, 1982).

$$T_4 = \frac{2L_d}{R_d} \tag{2.64}$$

$$\omega_3 = \frac{\sqrt{4L_dC_{oss} - C_{oss}^2R_d}}{2L_dC_{oss}} \tag{2.65}$$

Since the current is already zero at the beginning of this last interval, there are no added losses. The last switching interval ends when the gate-source voltage reaches the turn-off driving voltage(V_2), and when the voltage resonance is enough damped.

2.5 Conclusions and remarks

The proposed modeling approach from (Clemente *et al.*, 1982) gives a simplistic, and accessible computational methodology with known assumptions. This method allows simulating WBG and Si MOSFETs based on intrinsic characteristics for identical computational configuration and multiple gate configurations, making approximated observations on all MOSFETs technologies possible. To assess the computational and experimental behavior of WBG and Si power MOSFETs, chosen devices have to be of appropriate comparative ratings and of identical package. The following chapter presents the simulation results of chosen WBG and Si MOSFETs based on established criteria suited for both the experimental and computational analysis.

CHAPTER 3

SIMULATION RESULTS

In this chapter, the definition of the experimental setup allows to select WBG and Si MOSFET's based on the voltage range of 600V to 900V as highlighted in Chapter 1. Despite major differences in the internal characteristics of Si MOSFETs compared to WBGs, it is inevitable to add it to the study as a baseline to represent the current state of the art in the industry since it is the most mature technology on the market as of today. Based on the proposed modeling approach in Chapter 2, switching and conduction losses have been computed for multiple gate resistance and driving voltage for all MOSFETs under a defined configuration at 400V and 20A. All considered, temperature dependency of conduction losses ends in favorable simulation results for the SiC MOSFETs.

3.1 Criterion for Choosing MOSFETs and Final Choice

In the objective to compare WBG and Si MOSFETs under the proposed modeling approach of Chapter 2 as well as in an experimental configuration compliant with the modeling assumptions, selected MOSFETs have to be of similar ratings and identical package. Since it is not the main purpose of this analysis to design a board, and to speed up the evaluation process, the evaluation board R-REF01-HB from (RECOM Power, 2019) has been chosen as the experimental setup to compare MOSFETs under study. This evaluation board consists of a Half-Bridge Gate-Drive Power Supply with a fully isolated driver stage supplied by interchangeable DC converters. MOSFETs package for RECOM's board is the TO-247 with an optional Kelvin connection. It allows the specific reverse GaN lead configuration of gate-source-drain instead of the typical gate-drain-source under this package as well. This package is often used for high voltage and power MOSFETs devices, giving a convenient way to compare Si, SiC, and GaN MOSFETs.

As mentioned in the literature review Section of Chapter 1, the gray zone for selecting among WBG and Si MOSFETs is mainly from 600V to 900V devices for mid-power applications. In addition to similar package and voltage, selected MOSFETs must have similar current ratings and

they must be in N-channel enhancement mode. The Automotive Qualified devices (AEC-Q101) allows restricting the choice of MOSFETs only for the most reliable devices on the market, especially for automotive applications. Accordingly, the following criterion were established to find WBG and Si MOSFETs of similar characteristics to compare their switching performance under the modeling approach of Chapter 2 as summarized as follow:

- Identical drain-source voltage rating of 600V to 900V;
- Similar nominal current rating;
- N-channel enhancement mode MOSFETs;
- Identical Power package of TO-247-3 or TO-247-4;
- Automotive Qualified Device (AEC-Q101).

Based on those criteria, Si MOSFET IPW65R080CFDA (Infineon Technologies AG, 2012), SiC MOSFET SCT3060ALHR (Rohm Semiconductor, 2017), and GaN MOSFETs TPH3205WSBQA (Transphorm Inc., 2017) were selected to conduct the proposed study. Table 3.1 summarizes the main characteristics for all selected devices under study.

For each technology assess in the experimental configuration as well as in simulation, multiple recommendations from manufacturers guid to obtain the best switching behavior. For Si, Infineon Technologies AG (2012) recommends choosing external gate resistance not to exceed a dV/dt of 50V/ns, to use ferrite bead on the gate to suppress potential spikes, and to keep low coupling capacitance from the board gate layout.

Regarding SiC, Rohm Semiconductor (2020) recommends using a combination of gate driving voltage of +18/0V. However, using a negative turn-off driving voltage of -3V to -5V can minimize noise and maintain fast switching. Moreover, to obtain very high reliability, Infineon Technologies AG (2018) suggests decreasing the positive gate driving voltage to 15V to trade-off between lifetime and low on-resistance. Also, the use of SiC body diode is not recommended (Callanan, 2011) due to its high forward voltage as presented in Table 3.1. At last, using two separate driving path resulting in respective gate resistance for turn-on and turn-off is highly recommended to provide a more controllable slew rate of switching intervals (Microsemi, 2017).

Table 3.1 Main Characteristics of Si IPW65R080CFDA, SiC SCT3060ALHR and GaN TPH3205WSBQA MOSFETs Taken from Infineon Technologies AG (2012); Rohm Semiconductor (2017); Transphorm Inc. (2017)

Parameters	**Si MOSFET (IPW65R080CFDA)**	**SiC MOSFET (IPW65R080CFDA)**	**GaN MOSFET (TPH3205WSBQA)**
Drain-Source Breakdown Voltage ($V_{(BR)DSS}$)	650 V	650 V	650 V
Maximum Continuous Drain Current (I_D) @ T_c = 25°C	43.3 A	39 A	35 A
Typical Drain-Source On-State Resistance ($R_{ds(on)}$) @ T_j = 25°C	72 $m\Omega$	60 $m\Omega$	49 $m\Omega$
Typical Gate Threshold voltage ($V_{GS(th)}$)	4 V	4.7 V	2.1 V
Input Capacitance (C_{iss}) @ f = 1MHz	4440 pF @ 500V	852 pF @ 500V	2200 pF @ 400V
Output Capacitance (C_{oss}) @ f = 1MHz	210 pF @ 500V	55 pF @ 500V	135 pF @ 400V
Miller Capacitance (C_{rss}) @ f = 1MHz	23 pF @ 500V	24 pF @ 500V	23 pF @ 400V
Gate Resistance (R_G) @ f = 1MHz	0.75 Ω	12 Ω	2.2 Ω
Total Gate Charge (Q_G) Specified conditions in datasheets	161 nC	58 nC	28 nC
Internal Diode's Forward Voltage (V_{sd})	0.9 V @ I_F = 26.3A	3.2 V @ I_F = 13A	2.4 V @ I_F = 22A
Reverse Recovery Charge (Q_{rr}) Specified conditions in datasheets	1200 nC	55 nC	136 nC
Reverse Recovery Time (T_{rr}) Specified conditions in datasheets	180 ns	15 ns	40 ns
FET Type	Enhancement N-Channel	Enhancement N-Channel	Enhancement N-Channel
Package	TO-247-3	TO-247-3	TO-247-3
Qualification	AEC-Q101	AEC-Q101	AEC-Q101

Regarding GaN, Transphorm suggests using an external turn-on gate resistance of 15 Ω with a driving voltage of 0V to 10V/12V (Transphorm Inc., 2020). Generally speaking, an optimized PCB layout with a large area ground plane can reduce noise potential, and gate ferrite bead can help to prevent high-frequency noise from the gate driver and logic circuits (Transphorm Inc., 2020). GaN from Transphorm under the TO-247 package also includes a built-in gate ferrite bead (Transphorm Inc., 2020). Thus, it is not required to use an external gate ferrite

bead for those specific devices. Also, adding a switching-node RC snubber can highly reduce high-frequency ringing and help to control dI/dt transients (Transphorm Inc., 2020).

Most recommendations from all manufacturers can be applied for all MOSFETs, independently of the specific technology. Mitigation of noise and ringing from added gate ferrite bead, RC snubbers, and optimization of PCB layout can always be applied to reduce strain and perturbations on MOSFETs during the switching process. However, this might not always improve losses, for example with the use of external snubbers. Also, specific turn-on and turn-off driving voltage with an adapted separate gate driving resistance under optimized PCB layout should always be applied to provide a controllable slew rate. At last, the maximum specified dI/dt and dV/dt should always be respected to avoid excessive losses, surge voltage, and possible breakdown.

Recommendations are mainly related to experimental configurations, but elements regarding gate configuration as separate gate paths and recommended driving voltage are considered to assess computation of switching performances.

3.2 Simulation Methodology and Results

Based on detailed equations from 1982 International Rectifier Databook (Clemente *et al.*, 1982) presented in Chapter 2, all switching equations were implanted in MATLAB to assess the switching performance of selected MOSFETs presented in Table 3.1.

To observe switching performance at a realistic operating point based on MOSFETs characteristics of Table 3.1, supply voltage and nominal current have been respectively fixed at 400V DC and 20A. MOSFET's characteristics under nominal conditions and nominal computation conditions are summarized in Table 3.2.

First, turn-on and turn-off losses and duration have been computed from the proposed model in chapter 2 for a turn-on driving voltage ranging from 7V to 20V and a turn-off driving voltage from 0V to -5V. For all those simulation scenarios, independent turn-on and turn-off gate resistance values range from 2 Ω to 30 Ω, with 2 Ω steps. Switching losses and intervals

Table 3.2 Main Computation Conditions and Characteristics of Si IPW65R080CFDA, SiC SCT3060ALHR and GaN TPH3205WSBQA MOSFETs Taken from Infineon Technologies AG (2012); Rohm Semiconductor (2017); Transphorm Inc. (2017)

Parameters	Si MOSFET (IPW65R080CFDA)	SiC MOSFET (SCT3060ALHR)	GaN MOSFET (TPH3205WSBQA)
Supply Voltage (V_{dd})	400 V		
Nominal Current (I_0)	20 A		
Unclamped Inductance (L_d)	200 nH		
Stray Resistance (R_d)	100 mΩ		
Conduction Duration	50 ns		
Clamping Voltage ($V_{(BR)DSS}$)	650 V		
Drain-Source On-State Resistance ($R_{ds(on)}$) @ T_j = 25°C	72 $m\Omega$	60 $m\Omega$	49 $m\Omega$
Drain-Source On-State Resistance ($R_{ds(on)}$) @ T_j = 75°C	105 $m\Omega$	60 $m\Omega$	69 $m\Omega$
Gate Threshold voltage ($V_{GS(th)}$) @ T_j = 25°C	4 V No chart in datasheet	4.7 V	2.1 V No chart in datasheet
Gate Threshold voltage ($V_{GS(th)}$) @ T_j = 75°C		4.3 V	
Input Capacitance (C_{iss}) @ 400V	4300 pF	800 pF	2200 pF
Output Capacitance (C_{oss}) @ 400V	100 pF	90 pF	135 pF
Miller Capacitance (C_{rss}) @ 400V	18 pF	43 pF	23 pF
Transconductance (gfs) @ I_0 = 20A	35	10	53

duration are assessed for all technologies under study for 18900 computed combinations of the gate driving voltage and resistance to determine their best realistic configuration. The most appropriate configurations consider respective recommendations on driving voltage, gate resistance, and give proper on-state resistance value. Then, the best respective configurations for all MOSFETs technologies are compared to each other at a junction temperature of 25°C and 75 °C for variable conduction duration and variable nominal current.

Since the modeling approach is subdivided into multiple sub-intervals neglecting some parameters to minimize computation's complexity, a slight difference in computed parameters can result in moderate differences in obtained waveforms. Then, only intermediate scenarios as detailed in chapter 2 are considered to cope with realistic configurations. Then, there will not be major

differences in proposed configurations for all MOSFETs. Otherwise, most optimal configurations would have pointed to a very aggressive choice of gate voltage and resistance combination without considering the value of the internal gate resistance.

3.2.1 Turn-On Switching Performances

Equations regarding the turn-on switching performance as presented in chapter 2 are mainly independant of turn-off parameters except for the turn-off driving voltage and gate resistance. However, the selected experimental configuration from RECOM (RECOM Power, 2019) also includes distinct driving path for the turn-on and turn-off process. Then, the simulation process can easily be divided into two distinct computation model, only considering the turn-off driving voltage in the turn-on computation. To be more explicit, the first interval of turn-on is not contributing to switching losses based on assumptions of the modeling technique. Then, considering the turn-off driving voltage in the first turn-on interval will only result in a slight extended duration by a few nanoseconds without increasing losses.

Neglecting the turn-off driving voltage and resistance on the turn-on process allows to minimize the number of computation required to determine the best suited configurations to only 210. Since the amount of computation have been highly reduce to observe turn-on performances, turn-on driving voltage and resistance have not been reduce to only consider realistic scenarios for each technologies under study.

3.2.1.1 Silicon (Si) MOSFET: Optimal Operating Point to Minimize Turn-On Losses

Even if all turn-on configurations were computed to evaluate turn-on switching performances of the selected Silicon MOSFET, only driving voltage between 8V to 14V are suited for experimental configurations. Moreover, voltage over 10V shall be used to ensure low conduction losses (Infineon Technologies AG, 2012). Fig. 3.1 presents computed turn-on losses for all configurations based on intrinsic characteristics of the Si MOSFET under study.

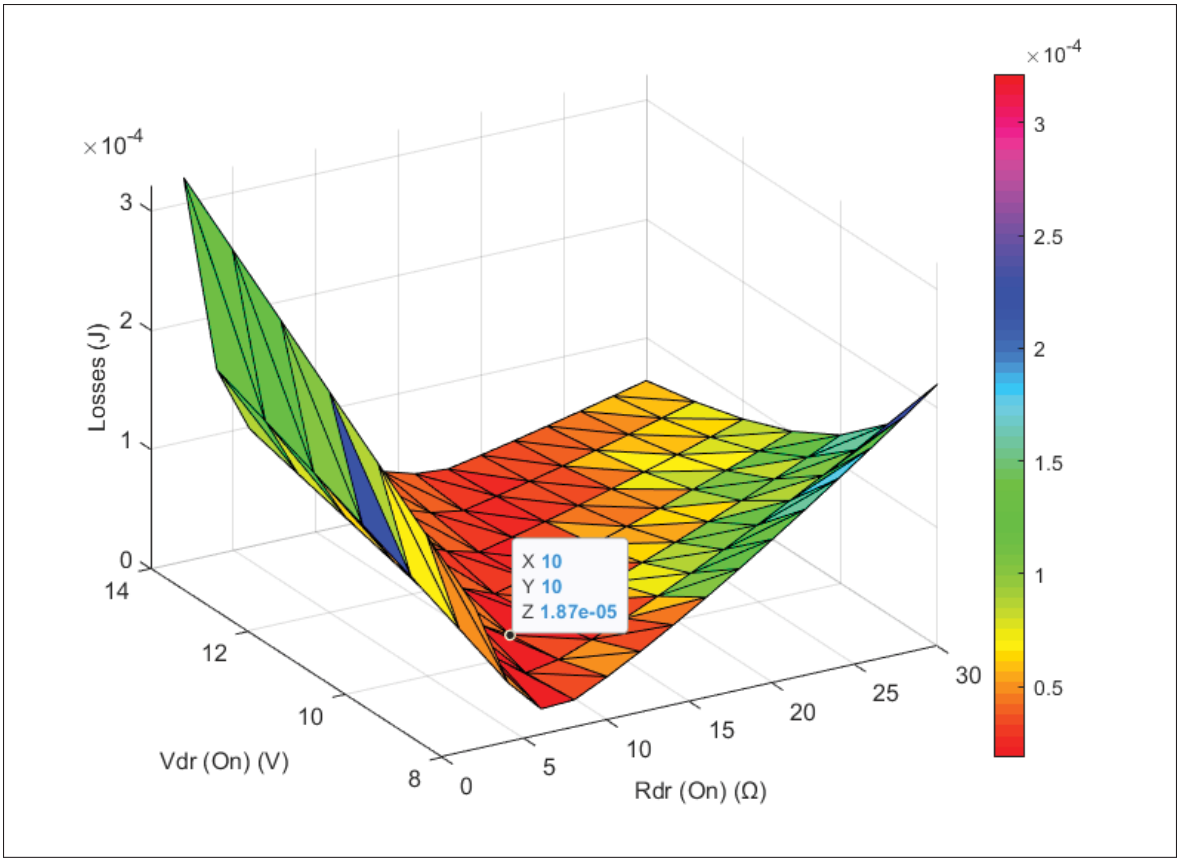

Figure 3.1 Si MOSFET: impact of the turn-on driving voltage and resistance on total turn-on energy

Fig. 3.1 shows that only few configurations are really interesting to minimize total turn-on losses of the Silicon MOSFET. Table 3.3 highlight the five best realistic combination of turn-on resistance and driving voltage to attain minimal turn-on losses. In this case, realistic means that the turn-on driving voltage must be between 8V to 14V and there are no limitations on gate resistance.

There is potentially a trade-off between the driving voltage and the resistance to get a fast turn-on process at low switching losses. Table 3.3 shows that the best configuration to obtain minimal turn-on losses of 18.7μJ with the Si MOSFET consist of a turn-on driving voltage of 10V with a total turn-on gate resistance of 10Ω. Since the internal gate resistance of the selected Silicon MOSFET is of 0.75Ω (Infineon Technologies AG, 2012), the external turn-on gate resistance

Table 3.3 Best Computational Suited Configurations for Minimal Turn-on Losses and Duration of the Si MOSFET IPW65R080CFDA

Turn-On Energy	Turn-On Duration	Turn-On Driving Voltage	Turn-On Gate Resistance
18.7 μJ	326 ns	10 V	10 Ω
19.6 μJ	394 ns	9 V	8 Ω
20.8 μJ	375 ns	11 V	12 Ω
23.1 μJ	441 ns	12 V	14 Ω
24.7 μJ	309 ns	9 V	10 Ω

have to be of 9.25Ω to reach minimum turn-on losses. Moreover, this configuration also gives the second minimal turn-on duration of 326 ns.

3.2.1.2 Silicon Carbide (SiC) MOSFET: Optimal Operating Point to Minimize Turn-On Losses

For the SiC MOSFET, driving voltages between 13V to 20V are suited for the experimental configurations, and preferably at least 15V shall be used to ensure low conduction losses (Rohm Semiconductor, 2017). Fig. 3.2 presents computed turn-on losses and duration for all analyzed configurations based on intrinsic characteristics of the SiC MOSFETs was listed in Table 3.2. Table 3.4 highlights the five best realistic combinations of turn-on resistance and driving voltage to achieve minimal turn-on losses with the selected SiC MOSFET.

Table 3.4 Best Computational Suited Configurations for Minimal Turn-On Losses and Duration of the SiC MOSFET SCT3060ALHR

Turn-On Energy	Turn-On Duration	Turn-On Driving Voltage	Turn-On Gate Resistance
15 μJ	176 ns	18 V	14 Ω
15.2 μJ	115 ns	19 V	16 Ω
15.4 μJ	102 ns	17 V	14 Ω
15.7 μJ	194 ns	15 V	12 Ω
16 μJ	231 ns	20 V	16 Ω

As illustrated in Table 3.4, minimal turn-on losses of 15μJ with the SiC MOSFET are attained with a turn-on driving voltage of 18V under a total turn-on gate resistance of 14Ω. Thus, the

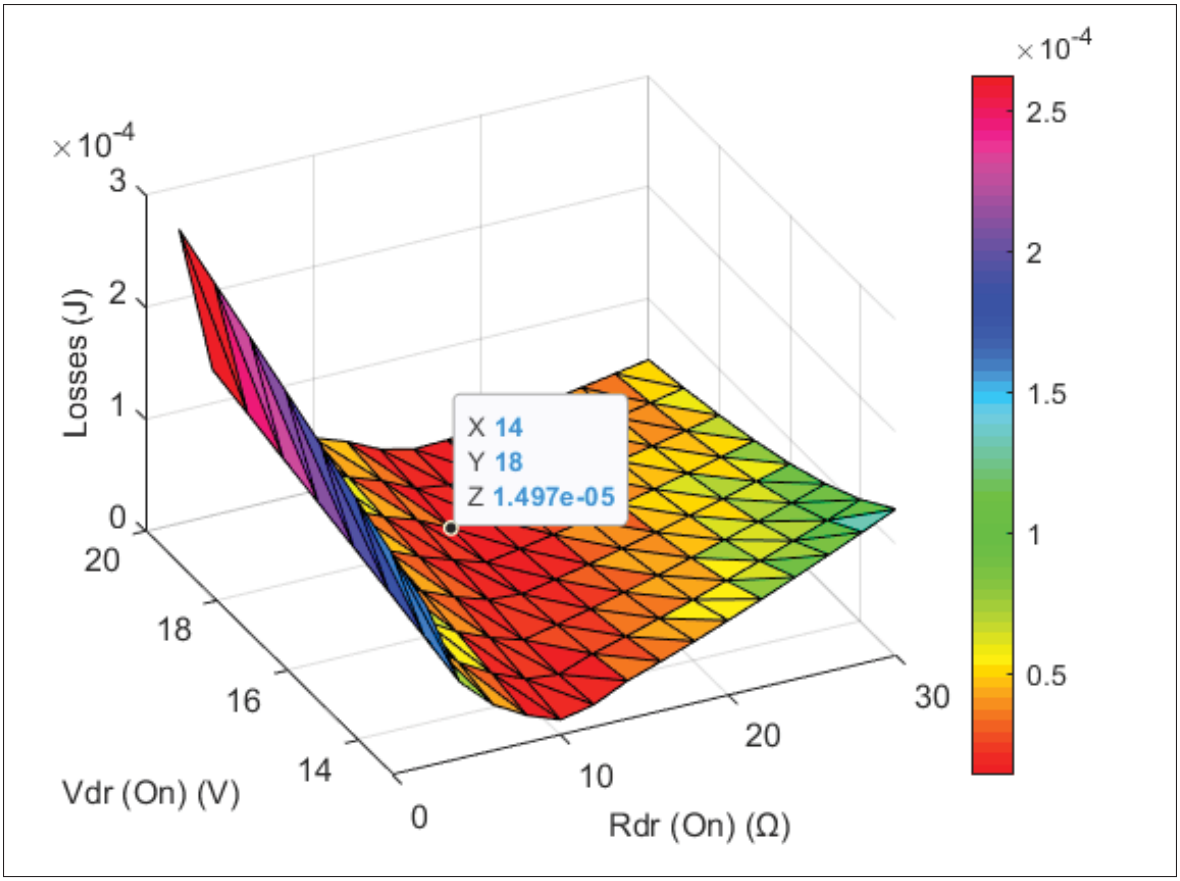

Figure 3.2 Impact of the turn-on driving voltage and resistance on total turn-on energy for SiC MOSFET SCT3060ALHR

external turn-on gate resistance should be 2Ω to reach minimum turn-on losses because the internal gate resistance is of 12Ω with the SiC MOSFET (Rohm Semiconductor, 2017).

3.2.1.3 Gallium Nitride (GaN) MOSFET: Optimal Operating Point to Minimize Turn-On Losses

The driving voltage between 7V to 12V is suited for experimental configurations with the GaN MOSFET, and voltage over 8V shall be used to ensure low conduction losses (Transphorm Inc., 2017). Fig. 3.3 presents computed turn-on losses and time for all analyzed configurations, and Table 3.5 illustrates the five lowest losses realistic combinations of turn-on resistance and driving voltage.

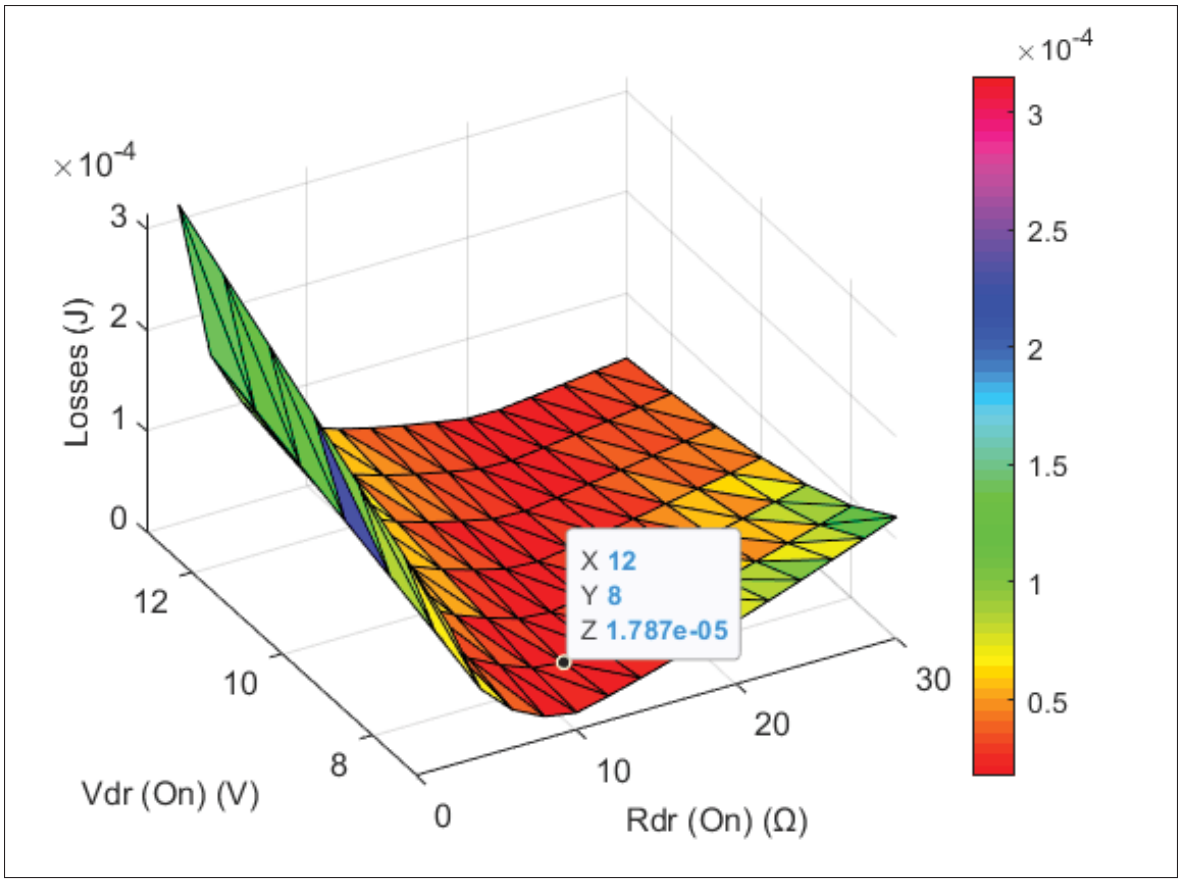

Figure 3.3 Impact of the turn-on driving voltage and resistance on total turn-on energy for GaN MOSFET TPH3205WSBQA

Table 3.5 Best Computational Suited Configurations for Minimal Turn-On Losses and Duration of GaN MOSFET TPH3205WSBQA

Turn-On Energy	Turn-On Duration	Turn-On Driving Voltage	Turn-On Gate Resistance
17.9 μJ	196 ns	8 V	12 Ω
18.3 μJ	228 ns	9 V	14 Ω
18.9 μJ	262 ns	10 V	16 Ω
19.4 μJ	296 ns	11 V	18 Ω
20 μJ	330 ns	12 V	20 Ω

With an internal gate resistance of 2.2Ω (Transphorm Americas Sales Representative, 2020), the external gate resistance have to be set at 9.8Ω to reach minimum turn-on losses of 17.9μJ with the GaN MOSFET under a driving voltage of 8V.

3.2.2 Conduction Losses and Dependency of Si, SiC and GaN MOSFET's Intrinsic Parameters on Temperature

Computed conduction losses are compared based on respective on-state resistance ($R_{ds(on)}$) as presented in Table 3.2. This approach has been used since MOSFETs are considered to be completely turned on during the conduction phase under invariable temperature conditions. Thus, losses can be computed using the assumption of constant drain current, on-state resistance and temperature. At 25 °C, the Si MOSFET exhibit a $R_{ds(on)}$ of 72 mΩ, the GaN MOSFET of 49 mΩ, and 60 mΩ for the SiC MOSFET (Infineon Technologies AG, 2012; Rohm Semiconductor, 2017; Transphorm Inc., 2017). Thus, compared to the GaN MOSFET at the same operating point, conduction losses are increased by 47% with the Si MOSFET and 22% for the SiC MOSFET.

However, the trends are different at high temperatures. At 75 °C, the Si and GaN MOSFETs show increased conduction losses with a $R_{ds(on)}$ of respectively 105 mΩ and 69 mΩ whilst SiC's $R_{ds(on)}$ is kept mostly unchanged at 60 mΩ. Then, the SiC MOSFET exhibits the lowest conduction losses, followed by the GaN MOSFET and finally the Si MOSFET. The first comparison of conduction losses at 25 °C is not a realistic scenario. As MOSFET exhibits switching and conduction losses, the temperature will certainly increase far over the ambient temperature, making this last scenario a more realistic evaluation of conduction losses.

It is observed that the change in on-state resistance for the SiC MOSFET at increased temperature is almost negligible, but is it a common property of SiC MOSFETs? To answer this question, Table II-1 from appendix II presents the influence of temperature on the on-state resistance and threshold voltage of a random sampling of WBG and Si MOSFETs. This random sampling of MOSFETs between 200V and 900V includes variable current rating and package to determine if the trend from the influence of temperature is stable under variable conditions. Then, Table 3.6 presents an overview of the average temperature dependency of $R_{ds(on)}$ and $V_{gs(th)}$ for all MOSFET's technology under study based on voltage, current rating, and package type. The computed average data of Table 3.6 are based on data presented in Table II-1.

Table 3.6 Average Influence of Increasing the Temperature from 25°C to 75°C on MOSFET's $R_{ds(on)}$ and $V_{gs(th)}$ Depending on Voltage and Current Rating, Package Type and Technology

Type	$V_{(BR)DSS}$	I_D @ T_c = 25 °C	**Package**	**Average** $\Delta R_{ds(on)}$	**Average** $\Delta V_{gs(th)}$
Si	200 V	15 - 25 A	DPAK (T0-252-3)	+46 % (10 data)	-11.25 % (4 data)
Si	650 V	20 - 30 A	TO-220-3	+50.83 % (6 data)	-12 % (2 data)
Si	650 V	30 - 50 A	TO-247-3	+47.50 % (8 data)	-11.20 % (5 data)
Si	900 V	10 - 15 A	Variable	+48.75 % (4 data)	-14 % (1 data)
Si	**200 - 900 V**	**10 - 50 A**	**ALL**	**Weighted Average +47.86 % (28 data)**	**Weighted Average -11.58 % (12 data)**
GaN	200 V	5 - 50 A	Variable DIE	+36.67 % (6 data)	-2.6 % (5 data)
GaN	650 V	15 - 20 A	TO-220-3	+35 % (2 data)	- (0 data)
GaN	650 V	35 - 50 A	TO-247-3	+35 % (4 data)	- (0 data)
GaN	900 V	15 A	TO-220-3	+30 % (1 data)	- (0 data)
GaN	**200 - 900 V**	**5 - 50 A**	**ALL**	**Weighted Average +35.4 % (13 data)**	**Weighted Average -2.6 % (5 data)**
SiC	200 V	-	-	-	-
SiC	650 V	29 A	TO-220-3	+10 % (1 data)	-15 % (1 data)
SiC	650 V	20 - 120 A	TO-247-3	+5.5 % (4 data)	-9.5 % (4 data)
SiC	900 V	10 - 20 A	Variable	+10 % (2 data)	-11.5 % (2 data)
SiC	**650 - 900 V**	**10 - 120 A**	**ALL**	**Weighted Average +7.43 % (7 data)**	**Weighted Average -10.85 % (7 data)**

In Table 3.6, the Si MOSFET seems to have the worst temperature dependency of the on-state resistance. Moreover, it typically exhibits a higher $R_{ds(on)}$ compare to SiC and GaN MOSFETs. Then, higher conduction losses are expected from Si MOSFETs. Regarding WBG MOSFETs, it seems that the GaN exhibits higher variability of the on-state resistance between 25 °C and 75 °C. However, the initial value of $R_{ds(on)}$ is also normally a little lower for the GaN MOSFET, which can result in similar conduction losses between GaN and SiC MOSFETs at increased temperature. It was not possible to compare SiC MOSFETs at reduced voltage since there is no available device under 600V on the market at the time of this research. Also, there are only a few datasheets providing information on threshold voltage temperature's dependency based on observations presented in Table 3.6. Then, there is not enough relevant data to highlight major trend between technologies regarding the threshold voltage.

3.2.3 Turn-Off Losses

Similar to turn-on switching intervals, the turn-on driving voltage has a small impact on turn-off losses. The turn-off losses computation starts instantly when the turn-off voltage is applied as the driving voltage after the end of the conduction interval. At this moment, and until the first turn-off interval ends, the MOSFET is kept fully on at the nominal current. Then, for the same turn-off driving voltage, higher turn-on driving voltage will result in extended duration and losses of the first turn-off interval. All scenarios have been computed for all possible combinations of turn-on and off driving voltage and turn-off resistance, which results in analyzing 840 different cases for all MOSFETs. For all scenarios of each MOSFETs under study, the impact of the positive driving voltage correspond to a maximum of 0.6 % of the total turn-off losses. Since the turn-on driving voltage does not result in a significant increase in turn-off losses, turn-off losses results are presented only considering the respective optimal turn-on configuration for all MOSFETs.

In addition to considering the minimal value of allowed turn-off resistance based on respective internal gate resistance, turn-off configurations resulting in driving the MOSFETs into avalanche are not considered as realistic configurations. For all configurations, computed losses and minimum turn-off driving resistance are presented for all turn-off driving voltage under study.

3.2.3.1 Silicon (Si) MOSFET: Optimal Operating Point to Minimize Turn-Off Losses

For the Si MOSFET, the optimal turn-on configuration to minimize switching losses consists of a turn-on driving voltage of 10V. Since the turn-on gate resistance does not interact in the turn-off switching equations, it is not necessary to consider its value. Fig. 3.4 and 3.5 respectively presents computed turn-off losses and duration for all combinations of turn-off driving voltage and resistance between 1 Ω and 10 Ω for the Si MOSFET.

Figs. 3.4 and 3.5 show that the lower is the turn-off driving voltage and turn-off resistance, and the lower will be the turn-off duration and total energy. However, very aggressive configurations at turn-off are more likely to result in a very high surge voltage, possibly driving the MOSFET

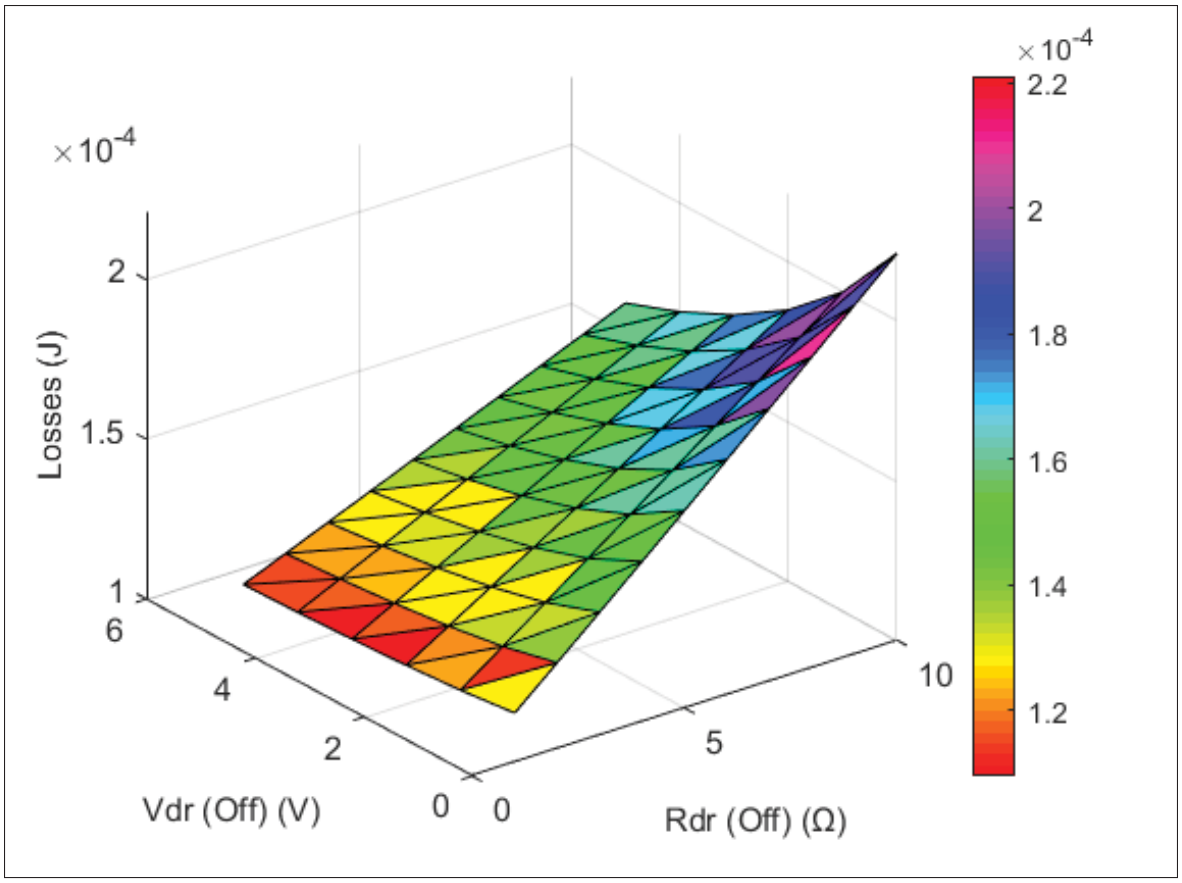

Figure 3.4 Si MOSFET: impact of the turn-off driving voltage and resistance on total turn-off energy

into avalanche, acting as its own voltage clamp (Clemente *et al.*, 1982). Nowadays, MOSFETs are often rated to sustain avalanche conditions for a very short time. However, driving the MOSFET into such conditions only results in a very stressful configuration, highly decreasing the MOSFET's reliability, and it is not suited for real industrial applications. Table 3.7 presents the minimum turn-off resistance with its respective total turn-off energy to avoid voltage clamping for every turn-off voltage between 0V and -5V.

Aggressive combination of gate resistance and voltage may result in a very high surge voltage causing voltage clamping under the defined operating point of 400V and 20A. As shown in Table 3.7, there is a trade-off between the driving voltage and gate resistance to ensure low losses and short duration of the turn-off interval. Still, there is no gain in strongly reducing the turn-off

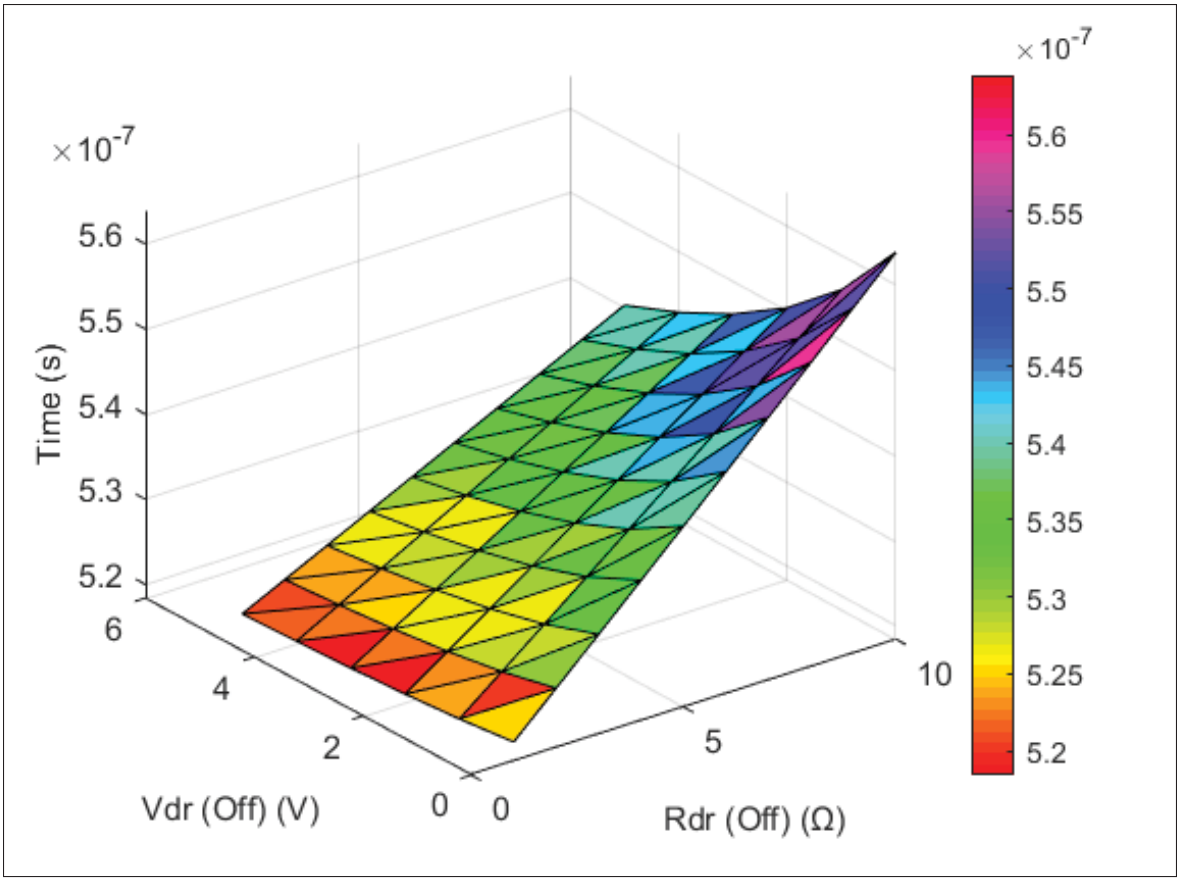

Figure 3.5 Si MOSFET: impact of the turn-off driving voltage and resistance on total turn-off time duration

Table 3.7 Suited Computational Configurations for Minimal Turn-Off Losses without Voltage Clamping of the Si MOSFET (IPW65R080CFDA)

Turn-Off Driving Voltage	**Minimum Turn-Off Gate Resistance without Clamping**	**Turn-Off Losses at Minimun Turn-Off Gate Resistance**
0 V	$\geq$ 17 Ω	305.4 μJ
-1 V	$\geq$ 20 Ω	298.3 μJ
-2 V	$\geq$ 24 Ω	301.6 μJ
-3 V	$\geq$ 28 Ω	304.0 μJ
-4 V	Always Clamp from 0 Ω to 30 Ω	-
-5 V	Always Clamp from 0 Ω to 30 Ω	-

driving voltage while increasing the gate resistance to slow down the switching process. It is mainly like pushing on one side to pull on the other, not resulting in any major improvements of

the switching process. Since the difference in turn-off switching losses of suited configurations presented in Table 3.7 is very low, opting for a null driving voltage might be a good solution to avoid using a negative turn-off driving voltage and reduce the design complexity. On the other hand, opting for a negative driving voltage helps mitigate the risk of parasitic turn-on. For those reasons, configurations with a turn-off driving voltage of 0V and -1V with their respective minimum turn-off gate resistance are both selected as proper solutions for the Si MOSFET. With a turn-off driving voltage of 0V, the total turn-off gate resistance have to be 17 Ω, and at -1V the total gate resistance has to be 20 Ω, respectively resulting in 305.4 μJ and 298.3 μJ. Those computed value of total gate resistance does not consider the value of the internal gate resistance of 0.75 Ω for the Si MOSFET under study (Infineon Technologies AG, 2012). Then, external turn-off gate resistances have to be at least 16.25 Ω and 19.25 Ω with a turn-off driving of 0V and -1V to avoid reaching the breakdown voltage during the turn-off switching interval.

3.2.3.2 Silicon Carbide (SiC) MOSFET: Optimal Operating Point to Minimize Turn-Off Losses

For the SiC MOSFET, the optimal turn-on configuration to minimize switching losses consists of a turn-on driving voltage of 18V. As already mentioned, the turn-on gate resistance does not interact in the turn-off switching equations, so it is not necessary to consider its value.

As for the Si MOSFET, the impact of the turn-off driving voltage and gate resistance shows the same tendency on turn-off losses and duration as for the SiC MOSFET. To be more explicit, the more aggressive is the configuration and faster is the turn-off process. Very aggressive turn-off configurations possibly results in lower losses, but can cause very stressful switching conditions impacting the reliability due to repetitive avalanche conditions and possible failures. Table 3.8 presents turn-off configurations and switching losses of the SiC MOSFET under study to avoid voltage clamping for every turn-off voltage between 0V and -5V.

Based on computed results presented in Table 3.8, the optimal turn-off configuration of gate resistance and driving voltage for the SiC MOSFET under study consists of 0V at 14 Ω, resulting

Table 3.8 Suited Computational Configurations for Minimal Turn-Off Losses without Voltage Clamping of the SiC MOSFET (SCT3060ALHR)

turn-off Driving Voltage	Minimum Turn-Off Gate Resistance without Clamping	Turn-Off Losses at Minimun Turn-Off Gate Resistance
0 V	$\geq$ 14 Ω	337.5 μJ
-1 V	$\geq$ 17 Ω	347.1 μJ
-2 V	$\geq$ 19 Ω	342.2 μJ
-3 V	$\geq$ 22 Ω	349.1 μJ
-4 V	$\geq$ 25 Ω	354.7 μJ
-5 V	$\geq$ 27 Ω	350.5 μJ

in a total turn-off losses 337.5 μJ. Since the internal gate resistance of the SiC MOSFET is 12 Ω (Rohm Semiconductor, 2017), the external turn-off gate resistance has to be 2 Ω.

3.2.3.3 Gallium Nitride (GaN) MOSFET: Optimal Operating Point to Minimize Turn-Off Losses

The optimal turn-on gate driving voltage of 8V is considered during turn-off losses computation with the selected GaN MOSFET. Table 3.9 presents turn-off configurations and switching losses of the GaN MOSFET to avoid voltage clamping for every turn-off voltage between 0V and -5V.

Table 3.9 Suited Computational Configurations for Minimal Turn-Off Losses without Voltage Clamping of the GaN MOSFET (TPH3205WSBQA)

Turn-Off Driving Voltage	Minimum Turn-Off Gate Resistance without Clamping	Turn-Off Losses at Minimun Turn-Off Gate Resistance
0 V	$\geq$ 11 Ω	362.8 μJ
-1 V	$\geq$ 16 Ω	371.4 μJ
-2 V	$\geq$ 20 Ω	363.8 μJ
-3 V	$\geq$ 25 Ω	369.1 μJ
-4 V	$\geq$ 30 Ω	372.7 μJ
-5 V	Always Clamp from 0 Ω to 30 Ω	-

Based on computed results presented in Table 3.9, the optimal turn-off configuration of gate resistance and driving voltage for the GaN MOSFET under study is at 0V and 11 Ω. This combination results in a total turn-off losses 362.8 μJ. Since the internal gate resistance of

the GaN MOSFET is 2.2 Ω (Transphorm Americas Sales Representative, 2020), the external turn-off gate resistance shall be 8.8 Ω.

3.3 Comparison of Switching Losses of Simulation Results

Simulation of all possible suited configurations allows to determine the best combinations of driving voltage and gate resistance to minimize total losses for all MOSFETs under study at an operating point of 400V with 20A. Since switching losses are fixed for a defined operating point, and conduction losses are dependant on the conduction duration and temperature, optimal device to minimize total losses is dependant on the conduction duration of the MOSFETs. Table 3.10 summarizes the optimal configurations and losses of all MOSFETs under study. Maximum operating frequency based on turn-on and off duration, and maximum conduction time and switching frequency to minimize total losses at 400V and 20A are highlighted.

As presented in Table 3.10, the Si MOSFET offers the smallest switching losses at 400V - 20A under its lower losses switching configuration. Both SiC and GaN are only slightly higher for a total switching duration half of the Si MOSFET. However, conduction losses are way higher for the Si MOSFET compared to WBG devices, especially at increased temperature. Then, it means that at increased conduction time, SiC and GaN MOSFETs under study offer smaller total losses per cycle.

At 25 °C, the Si MOSFET exhibits lower total losses for a conduction time between 0 to 5.92 / 7.4 μs depending on the turn-off configuration. Then, for a conduction time slightly higher, between 5.92 to 6.41 μ s, the SiC MOSFET offer lower total losses until the GaN MOSFET quickly take over. However, 25 °C is not a realistic junction temperature to compare total losses since losses inevitably lead to an increase in devices temperature over the ambient temperature. Then, at an increased temperature of 75 °C, the Si MOSFET only exhibit lower total losses for a very limited conduction time of maximum of 1.97 μs before the SiC MOSFET take over as the best suited device to minimize total losses after this point. Since the SiC MOSFET offers lower switching losses and lower conduction losses at 75 °C than the GaN MOSFET, this last

device cannot be considered as the best device under any circumstance at increased temperature. Unfortunately, only the temperature dependency of the $R_{ds(on)}$ is considered to compare total losses at increased temperature since the impact of temperature on the threshold voltage is not defined for all MOSFETs under study in datasheets.

Then, based on the maximum total switching time under optimal parameters, the SiC MOSFET seems to offer the faster switching process of all MOSFETs under study, quickly followed by GaN as presented in Table 3.10. Finally, maximum switching frequency at maximum optimal conduction time is illustrated in Table 3.10. This last value highlights the theoretical maximum switching frequency of the device with its respective total power loss at both 25 and 75 °C when it exhibits the lowest total losses compare to the other devices under study. The power loss at the maximum theoretical switching speed is not relevant because this operating point is not likely to happen in a real design. Anyhow, it shows that it would be possible to use an increased switching speed with SiC and GaN MOSFETs in comparison to Si MOSFET for the same conduction time, as illustrated by the total switching time and maximum switching frequency with a null conduction time.

In general, it seems like the Si MOSFET exhibits lower switching losses, followed by SiC and then GaN MOSFETs. The difference in total switching losses is very small and the difference in conduction losses is very considerable, especially at increased temperature. Due to the very low dependency of conduction losses of the SiC MOSFET between 25 °C and 75 °C compared to Si and GaN MOSFETs, it largely compensates for slightly higher switching losses with very reduced conduction losses. In order to determine if this is just an isolated result, Fig. 3.6 illustrates a relative comparison of total losses per cycle between MOSFETs under study for all possible combinations of nominal current between 5A and 20A and conduction time between 1 μs and 120 μs by increments of 1A and 1 μs at 75 °C. A voltage fixed at 400V is used for computation, and MOSFET's turn-on and off voltage and resistance configurations are respectively fixed at their best configuration for a turn-off voltage of 0V.

Table 3.10 Summary of Optimal Computed Configuration and Corresponding Minimal Switching Losses of Si, SiC and GaN MOSFETs under study for an Operating Point of 400V & 20A, without Clamping

Optimal Parameters & Results	**Si MOSFET (IPW65R080CFDA)**		**SiC MOSFET (IPW65R080CFDA)**	**GaN MOSFET (TPH3205WSBQA)**
Turn-On Driving Voltage	10 V		18 V	8 V
Turn-On Gate Resistance	10 Ω		14 Ω	12 Ω
Turn-On Losses	18.7 μJ		15.0 μJ	17.9 μJ
Turn-On Duration	325.8 ns		176.3 ns	195.6 ns
Turn-Off Driving Voltage	0 V	-1 V	0 V	0 V
Turn-Off Gate Resistance	17 Ω	20 Ω	14 Ω	11 Ω
Turn-Off Losses	305.4 μJ	298.3 μJ	337.5 μJ	362.8 μJ
Turn-Off Duration	440.2 ns	493.8 ns	127.6 ns	191.5 ns
Total Switching Losses	324.1 μJ	317.0 μJ	352.5 μJ	380.7 μJ
Total Switching Time	766.0 ns	819.6 ns	303.9 ns	387.1 ns
Maximum Switching Frequency @ Conduction Time = 0 s & DT = 100%	1.31 MHz	1.22 MHz	3.29 MHz	2.58 MHz
Drain-Source On-State $R_{ds(on)}$ @ T_j = 25°C	72 $m\Omega$		60 $m\Omega$	49 $m\Omega$
Drain-Source On-State $R_{ds(on)}$ @ T_j = 75°C	105 $m\Omega$		60 $m\Omega$	69 $m\Omega$
Optimal Conduction Time Range for Lower Total Losses @ 400V, 20A & T_j = 25°C	0 to 5.92 μs	0 to 7.4 μs	5.92 μs to 6.41 μs -	6.41 μs to ∞ 7.4 μs to ∞
Total Energy/Cycle at Max. Optimal Conduction Time @ T_j = 25°C	487.5 μJ	530.1 μJ	487.5 to 506.3 μJ	506.3 / 530.1 μJ & Over
Max. Switching Frequency & Power Loss at Maximum Optimal Conduction Time @ T_j = 25°C & DT = 50%	74.8 kHz 36.5 W	60.8 kHz 32.2 W	74.5 to 80.3 kHz 36.3 to 40.7 W	73.6 / 64.2 kHz 37.3 W / 34 W
Optimal Conduction Time Range for Lower Total Losses @ 400V, 20A & T_j = 75°C	0 to 1.58 μs	0 to 1.97 μs	1.58 μs to ∞ 1.97 μs to ∞	- -
Total Energy/Cycle at Max. Optimal Conduction Time @ T_j = 75°C	390.5 μJ	399.7 μJ	390.5 / 399.7 μJ & Over	-
Max. Switching Frequency & Power Loss at Maximum Optimal Conduction Time @ T_j = 75°C & DT = 50%	213.1 kHz 83.2 W	179.2 kHz 71.6 W	265.4 / 219.9 kHz 103.7 W / 87.9 W	- -

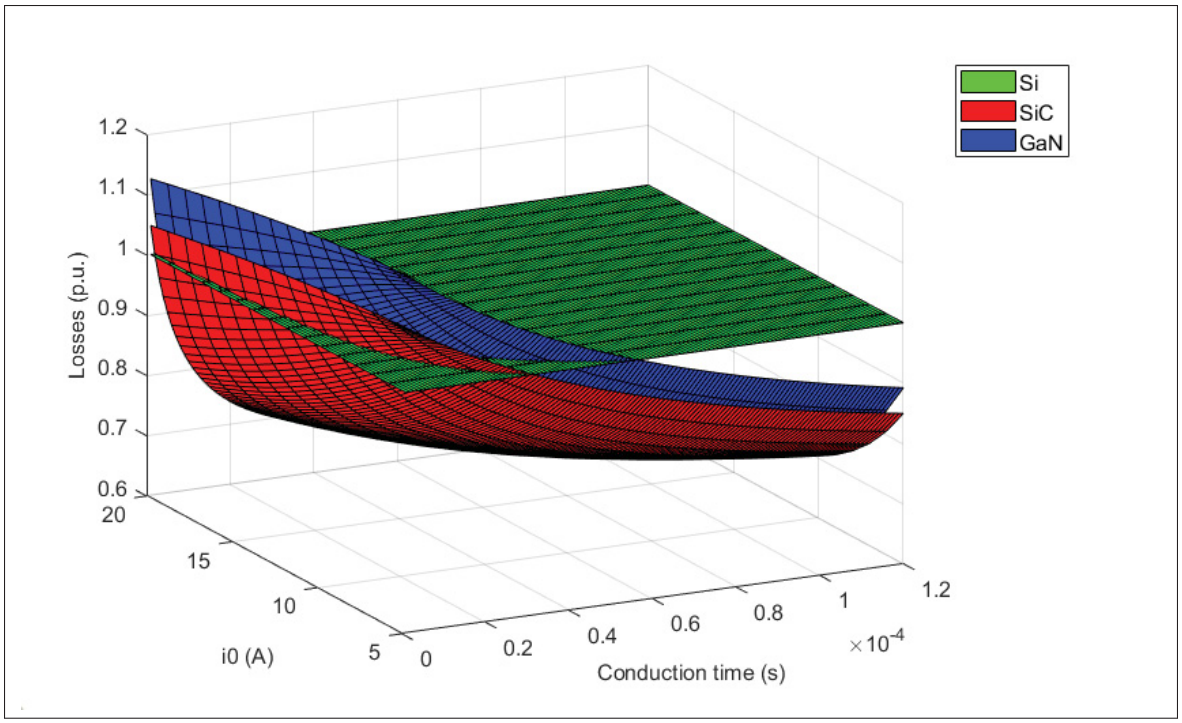

Figure 3.6 Relative comparison of total losses per cycle of SiC and GaN MOSFET compared to the Si MOSFET at 400V with a nominal current between 5A and 20A, and conduction time between 1 μs and 120 μs at 75 °C

In Fig. 3.6, the Si MOSFET still shows lower switching losses for a variable nominal current. However, the increase in conduction losses at high temperature quickly results in higher total losses for the Si MOSFET compared to both SiC and GaN MOSFETs under the same conditions.

3.3.1 Computational Observations at Reduced Operating Point

MOSFET's total losses are highly dependent on the external configuration and nominal conditions of the experiment. For the defined conditions at 400V and 20A, large gate resistance has to be used to avoid reaching avalanche conditions at turn-off, showing that it could be really beneficial to choose over rated MOSFETs to achieve more aggressive driving configurations to minimize total losses. However, this will surely result in increased cost for the device itself. In contrast, reducing the chosen operating point to 325V and 10A might be a more appropriate operating point for the selected devices to further reduce gate resistance and accelerate the

switching process whilst reducing losses. Table 3.11 presents a summary of optimal switching configurations of MOSFETs under study to minimize switching losses at 325V and 10A. Optimal configurations are determined to minimize total switching losses as well as switching time while respecting allowed driving voltage and resistance. This is also considering the internal gate resistance of the MOSFETs for all possible combinations of gate resistance and driving voltage between -5V to 20V, and from 0Ω to 50Ω. Respective recommended driving voltage range from manufacturers are favored to present optimal computational results because of experimental unavailability of custom driving voltage despite possible improved computed results. Also, the reproducibility of computational results on the test circuit is considered to illustrate the best realistic configurations. Transconductances and internal capacitances of all MOSFETs have been adapted to be compliant with the operating point at 325V and 10A to assess computational results.

Table 3.11 Summary of Optimal Computed Configuration and Corresponding Minimal Switching Losses of Si, SiC and GaN MOSFETs under study for an Operating Point of 325V & 10A, without Clamping

Optimal Parameters & Results	**Si MOSFET (IPW65R080CFDA)**	**SiC MOSFET (IPW65R080CFDA)**	**GaN MOSFET (TPH3205WSBQA)**	
Turn-On Driving Voltage	12 V	18 V	8 V	12 V
Turn-On Gate Resistance	10 Ω	12 Ω	8 Ω	13.5 Ω
Turn-On Losses	5.7 μJ	4.9 μJ	3.9 μJ	4.6 μJ
Turn-On Duration	312.4 ns	84.8 ns	128.4 ns	221.3 ns
Turn-Off Driving Voltage	0 V	0 V	0 V	0 V
Turn-Off Gate Resistance	6 Ω	12 Ω	3.5 Ω	
Turn-Off Losses	45.3 μJ	97.0 μJ	53.9 μJ	
Turn-Off Duration	542.5 ns	558.0 ns	564.5 ns	
Total Switching Losses	51 μJ	101.9 μJ	57.8 μJ	58.5 μJ
Total Switching Time	854.9 ns	642.8 ns	692.9 ns	785.8 ns

GaN's results are also presented for a 12 V gate driving voltage due to unavailability of compliant experimental dual 8V gate driving with the test circuit. Moreover, all MOSFETs show slightly

improved turn-off switching speed and losses at reducing negative turn-off voltage despite the increase in surge voltage and the necessity to increase the gate resistance to avoid voltage clamping. There is no interest in showing miraculously low switching losses if it brings the MOSFET to the point of breaking down due to the very aggressive configuration of gate resistance and voltage. For those reasons, only null negative turn-off voltage is considered to compare computational switching results of MOSFETs under study since uncommon configurations as a low positive driving voltage with high negative turn-off voltage require self-design experimental solutions due to unavailability of such commercial gate drivers compliant with RECOM's evaluation board.

In Table 3.11, it seems that all MOSFETs exhibit very similar turn-on losses under their lowest losses viable configuration. GaN seems to show slightly lower turn-on losses, followed by SiC then Si MOSFETs with a difference below 2 μJ which does not highlight considerably improved turn-on losses for any devices under study. However, computed turn-on switching time of the SiC MOSFET is almost 4 times smaller and between 1.5 to 3 times lower than the GaN MOSFET. Then, turn-off losses highly favor Si and GaN MOSFET which both provide about half of SiC turn-off losses. In total, switching losses favor the Si MOSFET by only an insignificant difference with the GaN MOSFET. Surprisingly, the SiC MOSFET is way behind due to higher turn-off losses, but still shows the fastest total switching duration with the lowest conduction losses at increased temperature, which can highly compensate for increased switching losses at reduced switching speed.

3.4 Observations, Recommendations and Drawback of Simulation Results

Based on computational results from the proposed modeling approach of Chapter 2 (Clemente *et al.*, 1982), the Silicon MOSFET seems to offer minimal switching losses highly compensated by its increased conduction losses, especially at a higher temperature. In the end, the SiC MOSFET seems to exhibit the best compromise to achieve high switching speed at reduced total losses. Still, GaN is not far behind showing that in real conditions, things might not be as observed in computed results.

Model-based computation is a good approach to observe the general switching performance of MOSFETs. Surely, a more complete methodology considering the variability of internal parameters might have resulted in a better approximation. However, uncertainty from experimental conditions like board layout parasitic inductance, measurement accuracy and methodology, probe capacitances and any other perturbations might highly overcompensate the benefits from a very reliable computational model. Since taking reliable experimental measurements is critical to observe exact switching performances of MOSFETs, experimental methodology has to be carefully defined to minimize perturbations on measurements as proposed by Chapter 4.

CHAPTER 4

MEASUREMENT METHODOLOGIES

In this chapter, the simulation model is reproduced in experimentation for comparison purposes between observations. First, a basic analysis of voltage and current measurement methods illustrates the importance of considering the parasitic elements of probes themselves and the mutual influence with the board. The next objective is to assess experimental switching losses. A comparison of the proximity field and lead current measurement techniques allows to define of a switching current extraction methodology whilst minimizing further perturbations on the switching behavior. Finally, detailed assessment and comparison of multiple switching topologies under the half-bridge experimental configuration allow defining the best configuration for overall minimal perturbations on both the measurements and the switching process.

4.1 Presentation of the Experimental Configuration

As specified in chapter 3, evaluation board R-REF01-HB from (RECOM Power, 2019) have been chosen as the experimental setup to compare Si and WBG MOSFETs under study. This experimental configuration consists of a Half-Bridge Gate-Drive Power Supply with a fully isolated driver stage of interchangeable DC converters. Board's power device package is TO-247-3/4 compliant with selected WBG and Si MOSFETs. High insulation gate driver SI8274GB4D-IS1 has been mounted on RECOM's board to achieve complementary driving of high and low side MOSFETs with a programmable dead time fixed at 200 *ns* only using one TTL PWM signal generated from a function generator.

In order to observe the switching behavior of WBG and Si MOSFETs compliant with the assumptions of the computational model from (Clemente *et al.*, 1982), the experimental load has to be defined consequently. To compare experimental results with the ones in chapter 3, the load has been designed to operate at a nominal voltage of 325 V, nominal current of 10A, and a fixed switching frequency of 25 kHz with a duty cycle (DT) of 50 %. Simulation of the half-bridge configuration on Simulink as illustrated in Fig. 4.1 allows determining an appropriate load

inductance and resistance value to obtain the desired average nominal current of 10 A with the lowest maximum current deviation. Table 4.1 illustrates the results of the average nominal current value and deviation as a function of the load configuration without considering the influence from parasitic components of the experimental board.

Table 4.1 Average Current Value and Deviation as a Function of the Load Configuration from Simulink

Total Load Configuration	**Maximum Current Deviation from Average Value**	**Average Nominal Current Value**
25μH & 16Ω	≈ 199.92%	10.11 A
2.5mH & 16Ω	≈ 12.84%	10.11 A
5mH & 16Ω	≈ 6.47%	10.11 A
10mH & 16Ω	≈ 3.18%	10.11 A

To be compliant as much as possible with computational assumptions, the load configuration has been fixed to 10 mH with a total resistance of 16 Ω. The resistance limits the maximum value of the current whilst the inductance helps to reduce the deviation between switching intervals. It is not appropriate to only use an inductive load without resistance because it would inevitably result in a theoretical unlimited maximum current value which makes it very hard to find a stable point around a fixed average current value. As long as the current is mostly steady during switching intervals, it will be possible to compare experimental losses with the computational model.

Moreover, early measurements at very reduced voltage supply and nominal current showed major resonance and fluctuation of the supply voltage. The initial input capacitance of the experimental board of only 1 μF was not sufficient to respect the assumption of a steady supply voltage from the computational model. Thus, an external capacitor bank totaling 180 μF MKP capacitors has been added to the input supply of the experimental board through close soldering joint. Connecting the capacitor bank with cables soldered on the board inevitably adds some inductance in series with the capacitance, it would have been preferable to add it by completely redesigning the half-bridge board because closer PCBs traces normally provides a low inductance path compared to cables. Top and bottom capacitors are soldered on opposites sides to balance the current on each layer of the capacitor bank and reduce as much as possible the parasitic elements

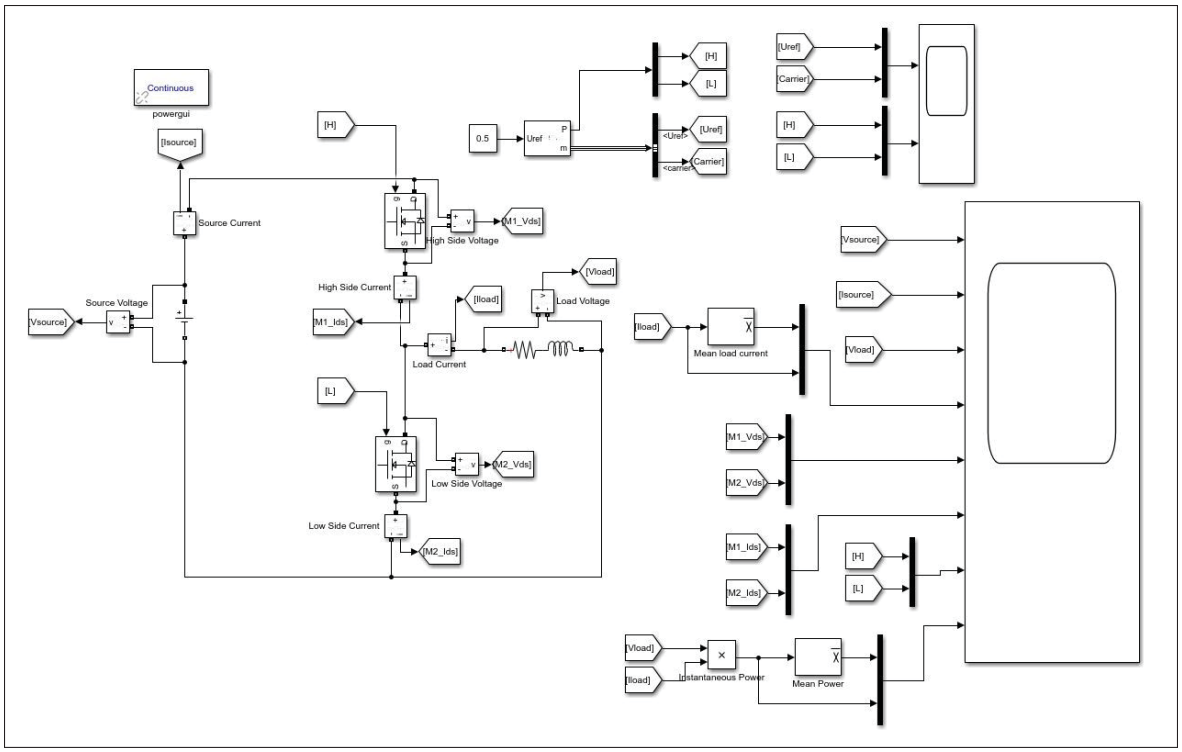

Figure 4.1 Simulink model of the experimental configuration of the Half-Bridge board

(leakage inductances). Table 4.2 illustrates the selected capacitor's properties in accordance with the nominal fixed operating point at 325 V and 10 A, and Fig. 4.2 shows the final configuration of the half-bridge board including the externally added capacitance. In overall, the capacitor bank allowed to stabilize the supply voltage during normal utilization of the board.

Table 4.2 Film Capacitor's Properties of the External Capacitor Bank

Part Number	**Capacitance**	**Voltage Rating**	**Maximum dV/dt**	**Peak Current**	**RMS Current**	**ESR**	**ESL**
FB37M6A03006KC	30 μF	700 V	21 $V/\mu s$	630 A	16 A	4.5 $m\Omega$	33 nH

As for the computation results presented in chapter 3, losses are computed using both the voltage and current measurement of MOSFETs. In this particular experiment, the high side MOSFET is considered the switching device since the load is placed between the middle point and the ground, leaving the low side MOSFET as the freewheeling diode. In addition to observing switching losses of each particular technology under study, using the low side MOSFET as the

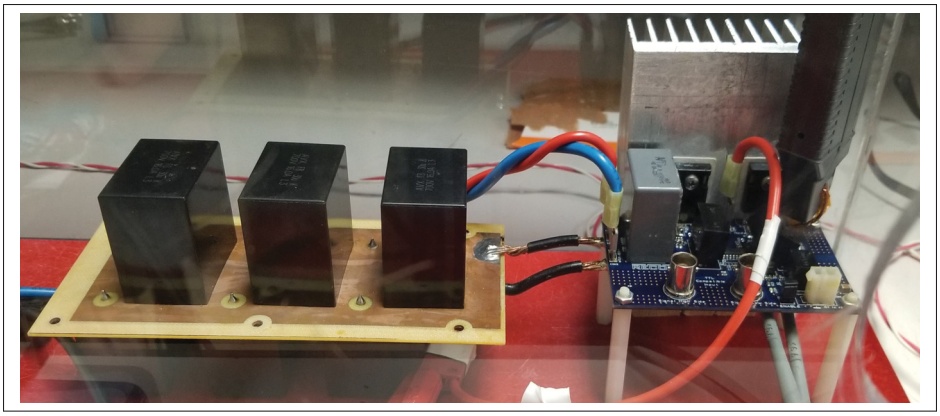

Figure 4.2 Capacitor bank assembly on the Half-Bridge board

freewheeling diode allows to assess the internal diode's performance and highlight any peculiar details about it. However, probing currents and voltages experimentally requires carefully establish the measurement methodologies to achieve high precision and reliability of assessing data.

4.2 Experimental Measurement Technique and Recommendations

There are no experimental measurement techniques that will allow observing experimental data without influencing it at all. Every little detail can have a major impact on experimental measurements. Therefore, it is necessary to define a standardized methodology to extract experimental waveform while minimizing perturbations. In addition to the difficulty alone of getting very reliable measurements, the current measurement of a MOSFET in a switching leg can hardly be done without considerably influencing its behavior by the introduction of parasitic components. Since there is no direct way to observe the high side MOSFET's current, it is mandatory to develop a current extraction methodology. In addition, it is also very important to establish the basic general measurement rules to minimize perturbations on both voltage and current measurements in the experimental setup.

4.2.1 The Basic Early Essentials

Using differential probes for high side voltage measurements is preferable to avoid possible short circuits between the oscilloscope and the power supply's grounds. Performing high side voltage measurements with passive probes are possible, but this requires perfect insulation between the power supply and the oscilloscope grounds. Nowadays, high voltage differential probes provide high insulated voltage measurements with low added capacitance, and short rise time and propagation time which makes them perfectly suited for high and low side voltage measurements without inducing any short circuit risk.

Observing multiple experimental variables at the same time while ensuring perfect time synchronization and minimal perturbations between measurements can be very challenging. Placing the trigger on a common current measurement is a suitable solution to synchronize voltage measurements taken on different occurrences of the short time interval with each other. Also, a stabilized experimental board's temperature minimizes the variability of MOSFET's characteristics during experimental observations and eases the comparative process between multiple voltage and current measurements.

The geometry and position of probes and cables are also very important to minimize further avoidable perturbations on both measurements and switching performances of MOSFETs. Minimizing the surface between probe's wire by twisting them together highly reduce the interference from near magnetic field on measurements. Moreover, avoiding parallelism of measurement wires with power cable is preferable to reduce magnetic coupling as much as possible. Also, twisting power supply cables together helps to minimize the total added inductance of the power supply on the switching loop. Fig. 4.3 illustrates a general comparison of mutual coupling between a differential probe and passive probe with a pigtail on low side MOSFET's drain-source voltage measurement. Voltage measurements are taken during high side turn-on with the Silicon MOSFET at reduced voltage supply of 25 V. Reduced total measurement surface of the pigtail passive probe results in a decrease of the measured low side drain-source surge voltage by 32.1 % compared to the results from the differential probe.

Non-isolated probes are not suitable for high side voltage measurements under a high side switching configuration. This makes the use of the pigtail probe inappropriate for the current experiments in this work.

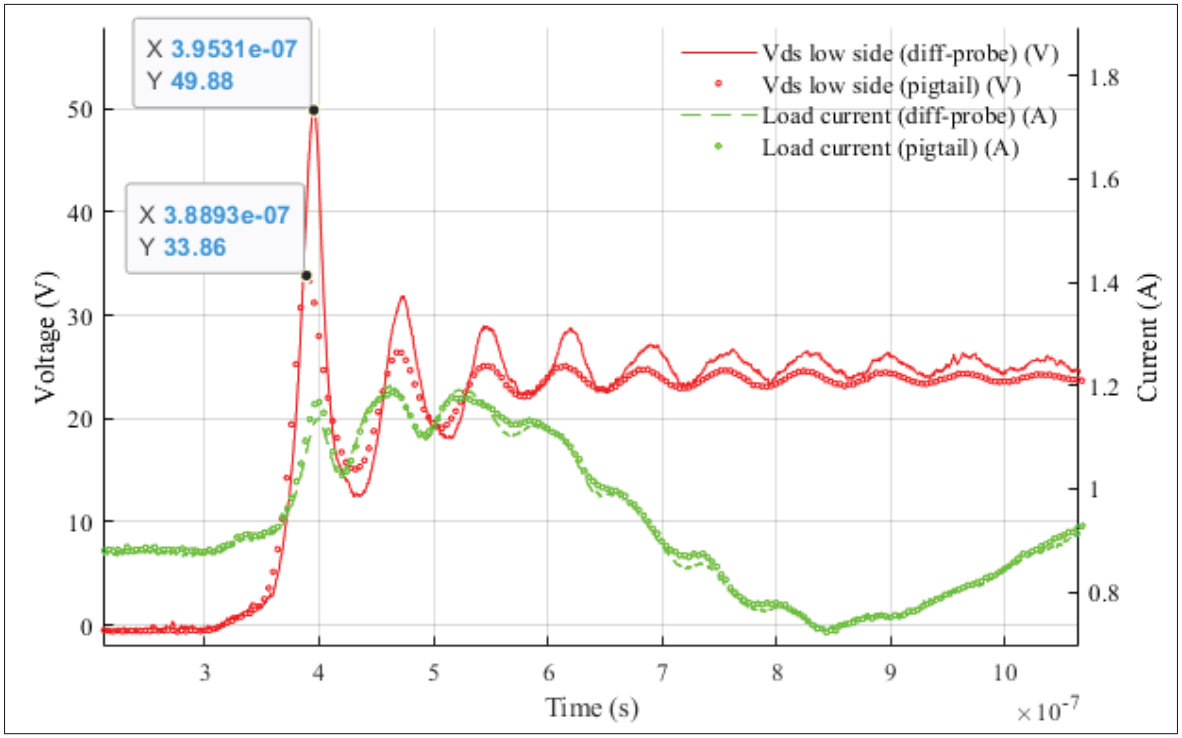

Figure 4.3 General comparison between differential probe ADP305 and passive pigtail probe PP0006A on low side drain-source surge voltage

Both voltage and current probes exhibit a rise and propagation time which have to be considered to ensure very precise synchronization between measurements. Even if some oscilloscopes provide the opportunity to directly adjust a specific delay for each experimental waveform during measurements, it is not ideal to have multiple voltage measurements with a common measurement point. The source of the high side MOSFET is only separated from the drain of the low side MOSFET by the unclamped inductance formed from the PCB trace under the RECOM's board. The probes with a direct contact connection as voltage probes add an inductive loop with a capacitive connection to the board. This addition of parasitic components slightly influences MOSFET's switching behavior, and can highly influence other measurements under a common measurement point. Then, to reduce probe coupling with each other and

further influence from voltage probes on switching performance, only one voltage measurement is realized at a time with multiple current measurements. Matlab software helps to compile multiple voltage measurements under the same graph from different occurrences. This allows to get a perfect time synchronization through a common trigger on current measurement while considering specific propagation and rise time of all measurements. This approach leads to minimal perturbations on the device switching performance.

4.2.2 The Proximity Magnetic Field

Voltage probes need a direct connection on the circuit, making it prone to mutual coupling and perturbations under fast voltage and current change conditions. Conversely, current measurements based on contactless methods such as Hall effect probes do not induce much disturbance on the circuit nor do they influence other measurements, making it less susceptible to perturbations compared to voltage measurements. In this experimental configuration, there is not enough space on the circuit to add any current probe to capture the switching current from the high side MOSFET. Then, the high side switching current is computed from the difference between the load current and the low side freewheeling MOSFET's current. However, since it is not possible to perform any direct current measurement on PCB's trace, a magnetic field probe illustrated in Fig. 4.4 has been designed with a coaxial cable. This magnetic probe allow to measure the low side MOSFET's reverse recovery current through the integration of its magnetic field from an isolated surface as illustrated in Fig. 4.5.

To observe the reverse recovery current waveform, it is required to multiply the integration of the field measurement by the coupling factor between the probe and the PCB's trace. Since the maximum reverse recovery current is not known, it is not possible to determine the coupling factor with the high side turn-on waveform alone. Since the only viable path for the load current during the freewheeling period is through the internal diode of the low side MOSFET, calibration of the coupling factor is possible through a comparison with the directly measured load current during the freewheeling period. Then, this same coupling factor can be applied to the integration

Figure 4.4 Magnetic field probe built from a coaxial cable covered with Kapton tape

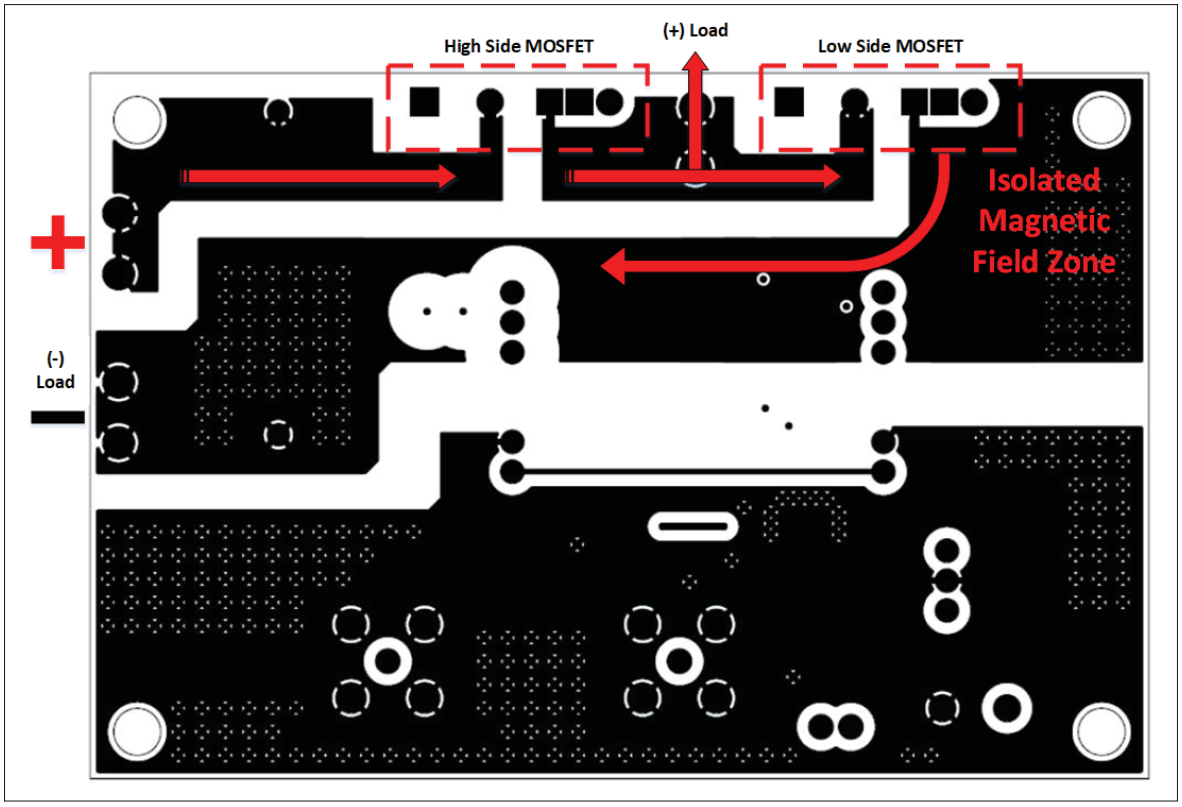

Figure 4.5 Board's bottom layout magnetic field measurement from low side MOSFET's reverse recovery current

of the field measurement during the high side turn-on waveform to obtain an approximation of the reverse recovery current.

Multiple experimental scenarios have shown major influence on the magnetic field measurements from any voltage measurements taken simultaneously. As long as there is a voltage probe connected to the oscilloscope and on the experimental board, reduction of the signal-to-noise ratio (SNR) is perceptible on the field measurement. Since both voltage and current measurements are required to compute switching losses, extraction of voltage and field measurements are done on separate time frames to minimize possible perturbations. Therefore, synchronization on a common current measurement as the load current with a fixed trigger position helps to recover a proper time synchronization between voltage, magnetic field and current measurements on Matlab. In addition to taking field measurements without any voltage measurements simultaneously, suppression of the proximity field is realized without the nominal current to minimize perturbations of surrounding magnetic fields on the field current measurement. For all measurements, the magnetic field probe is fixed on the isolated field measurement zone defined in Fig. 4.5. At last, it may look that the function generator can synchronize signals from different occurrences with each other. However, in such scenarios, the function generator offers a simultaneous connection between the experimental board and the oscilloscope which provides a path for the noise to propagate. Even if the experimental board offers a very high level of insulation and immunity to noise between the control and power signals, high-frequency noise from switching is hardly avoidable and can easily perturb very sensitive measurements such as magnetic field. For example, Fig. 4.6 illustrates perturbations from a direct connection to the function generator as external trigger on measurements of the proximity magnetic field.

Then, Fig. 4.7 shows the recovery of the low side MOSFET current through integration and multiplication of the measured magnetic field. However, to recover a current measurement close to the actual load current, it has been necessary to multiply the first fast variation of the corrected field measurement by a coupling factor of 2.5, and the rest of the average signal by a coupling factor of 0.6. Due to the low SNR ratio during the slow variation of the field, the average value of the corrected field measurement is used to recover the load current measurement through

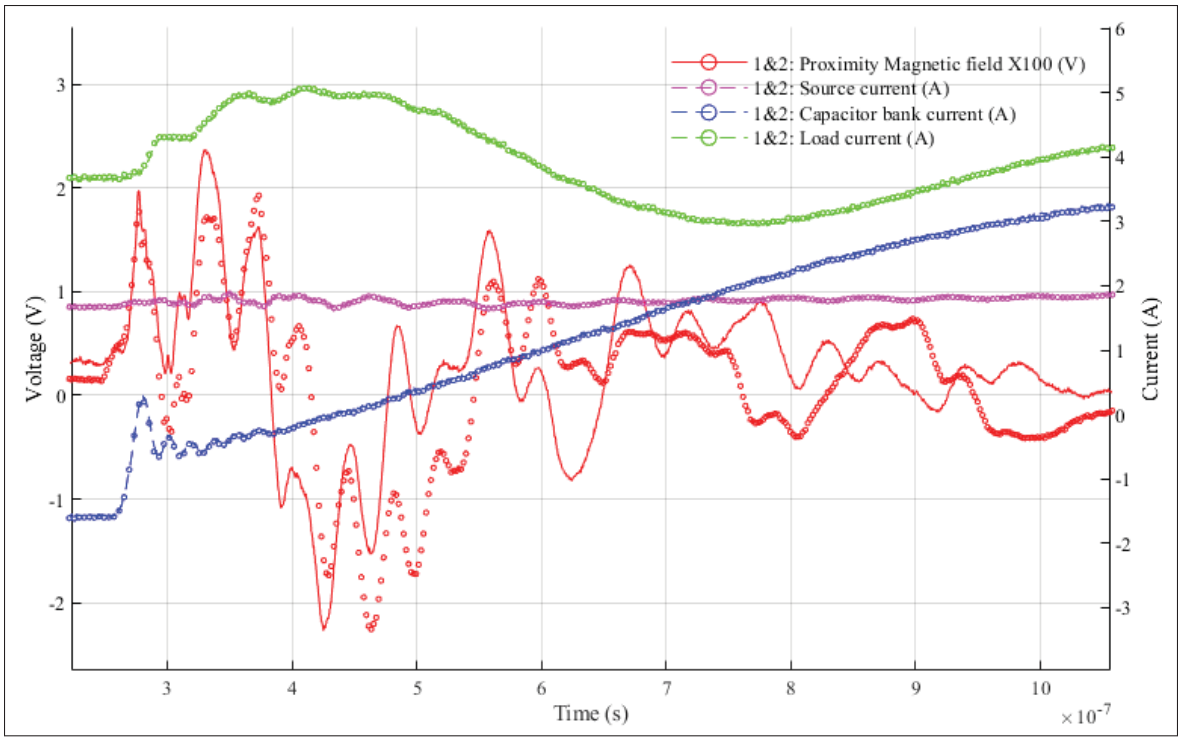

Figure 4.6 Perturbations from the function generator as the external trigger on measurements of the proximity magnetic field

multiplication of the integrated signal. Otherwise, a recovered current with a similar shape to the load current is observed, but with a decreased value. Then, integration and multiplication of the field measurement from the established coupling factor during turn-off transient allow observing the reverse recovery current during high side turn-on as illustrate in Fig. 4.8.

As shown in Fig. 4.8, the coupling factor has been readjusted to 2 instead of 2.5 because it was not possible to observe a reverse recovery current ending to approximately $0A$ with the original coupling factor of 2.5. In a last attempt to make the near magnetic field a suitable non-intrusive current measurement solution, ferrite beads of mix 43-44 have been added to the coaxial cable of the magnetic probe to reduce common-mode conducted electromagnetic interference (EMI). Multiple experiments showed that the wide frequency spectrum of the magnetic field signal resulted in a variable impact from the added frequency dependant impedance of the ferrite beads. Accordingly, there are no considerable improvements of the field waveform by adding ferrite

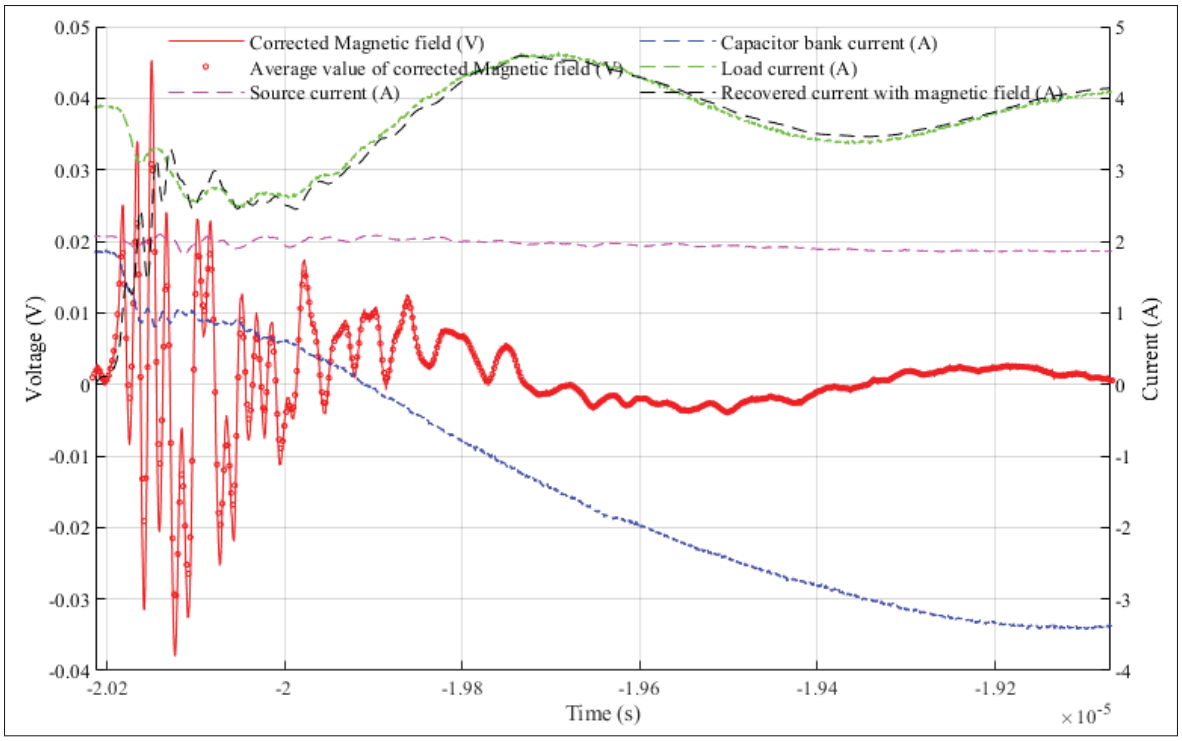

Figure 4.7 Integration of the magnetic field measurement to adjust the magnetic coupling factor during turn-off waveform

beads, and since its impact on the signal of interest is unknown, there is no reason to proceed with it.

Comparison between measurements of the magnetic probe and current from low side MOSFET's isolated PCB's trace during the freewheeling period allowed to define the coupling factor to recover the current from the integration of the magnetic field. However, the field measurement is a very low amplitude signal and tends to capture all other magnetic fields from any surrounding sources, making the final result very doubtful. Also, any direct interactions or intermediate link between the magnetic field probe and the power signals of the experimental board tends to reduce considerably the SNR of the magnetic measurement. Moreover, the magnetic measurement is highly dependant on the position of the probe on the experimental board and the direction of the magnetic field making this current measurement solution very easily perturbed and not reliable. To compute switching losses and have a better understanding of the switching behavior

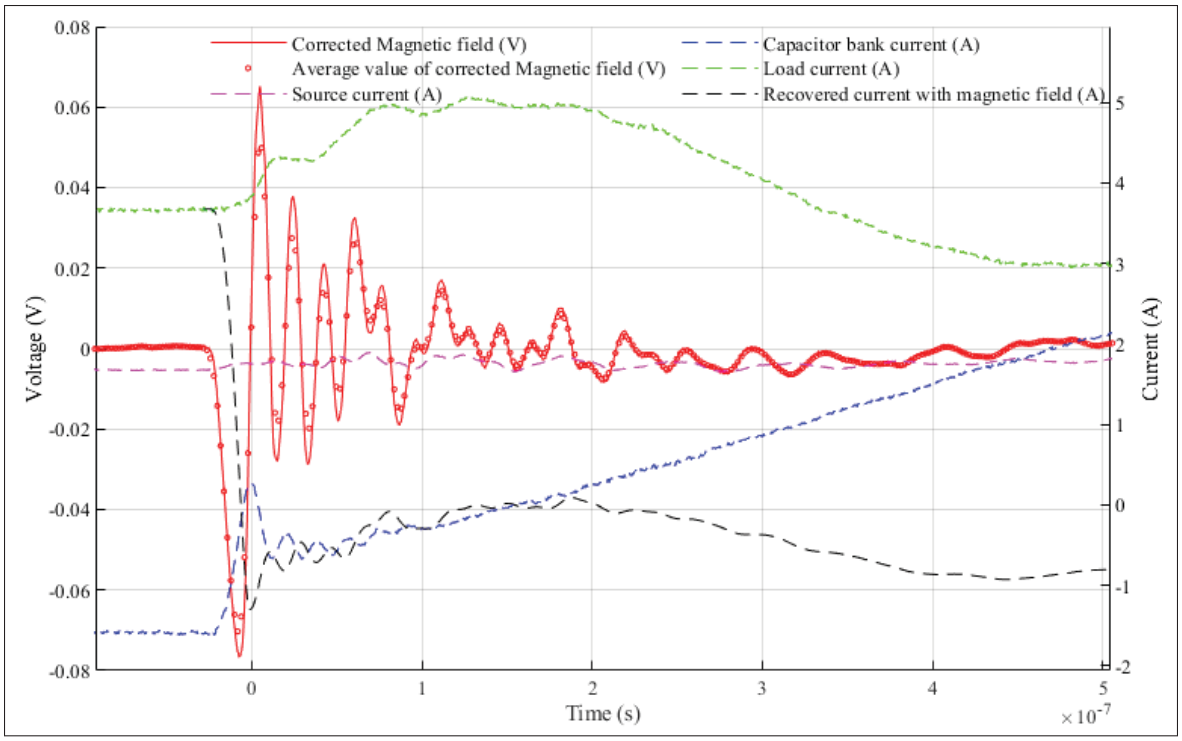

Figure 4.8 Approximation of the reverse recovery current through integration of the magnetic field during turn-on waveform

of MOSFETs, an added wire has been soldered to the low side MOSFETs to have a direct measurement of the reverse recovery current from a Hall effect contactless current probe.

4.2.3 Introduction to the Lead Wire Current Measurement Technique

The added wire consist of an isolated magnetic wire of American Wire Gauge (AWG) 10 to sustain the RMS current of 10A at the nominal operating point of 325 V. As a first experiment, the added wire has been soldered on the source lead of the low side MOSFET. Since selected MOSFETs are not provided with a Kelvin connection, the current measurement will also capture the gate-source current of the low side MOSFET. However, this does not have any impact on the current measurement of the reverse recovery current since the change in the low side gate circuit is occurring before the turn-on process of the high side MOSFET. Fig. 4.9 illustrates a close view of the modification completed on the low side MOSFET in order to add a Hall effect

CP031 current probe to the circuit. To minimize the added parasitic inductance, the current measurement lead wire has been tightly adjusted to the shape of the CP031 current probe. To avoid a possible short circuit with the current probe, Kapton tape had been added to the lead wire to offer an additional insulation layer.

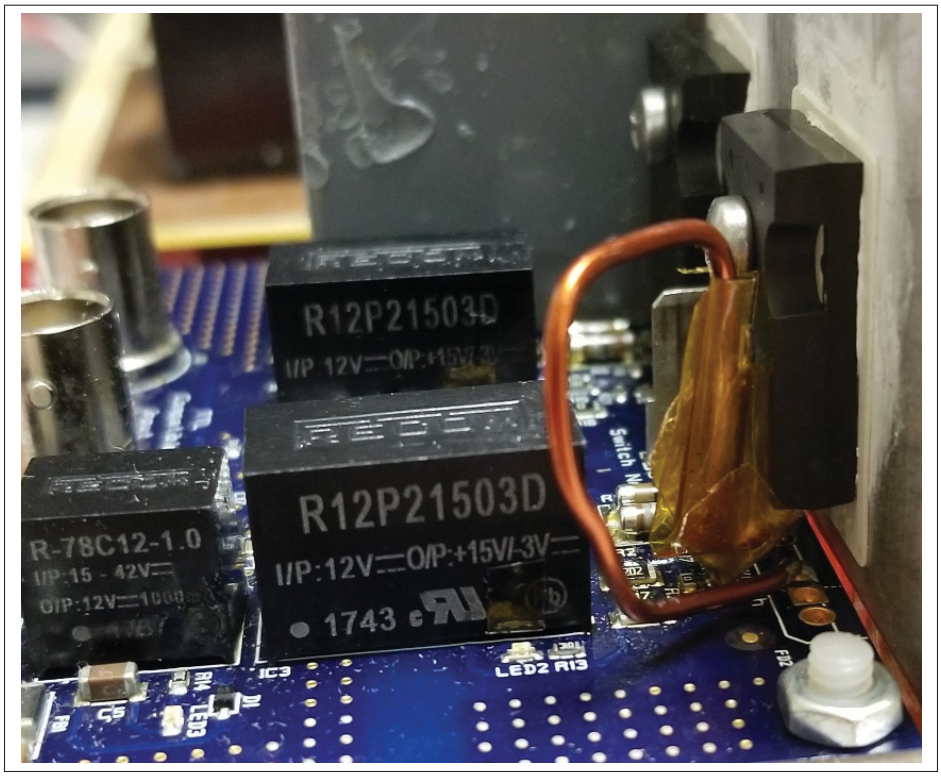

Figure 4.9 Additional current measurement wire on the source lead of the low side MOSFET partially covered with Kapton tape

This added wire ensures precise measurement of the actual current flowing through the low side MOSFET. However, this wire inevitably introduces some leakage inductance into the switching loop, which will influence the switching behavior. To evaluate the impact of this modification on the switching behavior, Figs. 4.10 and 4.11 respectively illustrate a comparison between voltage and current waveform before and after the addition of the lead wire on turn-off and turn-on intervals.

As predicted, both Fig. 4.10 and 4.11 show that there is an influence from adding even the shortest wire on the switching behavior of MOSFETs. Comparison show only small differences

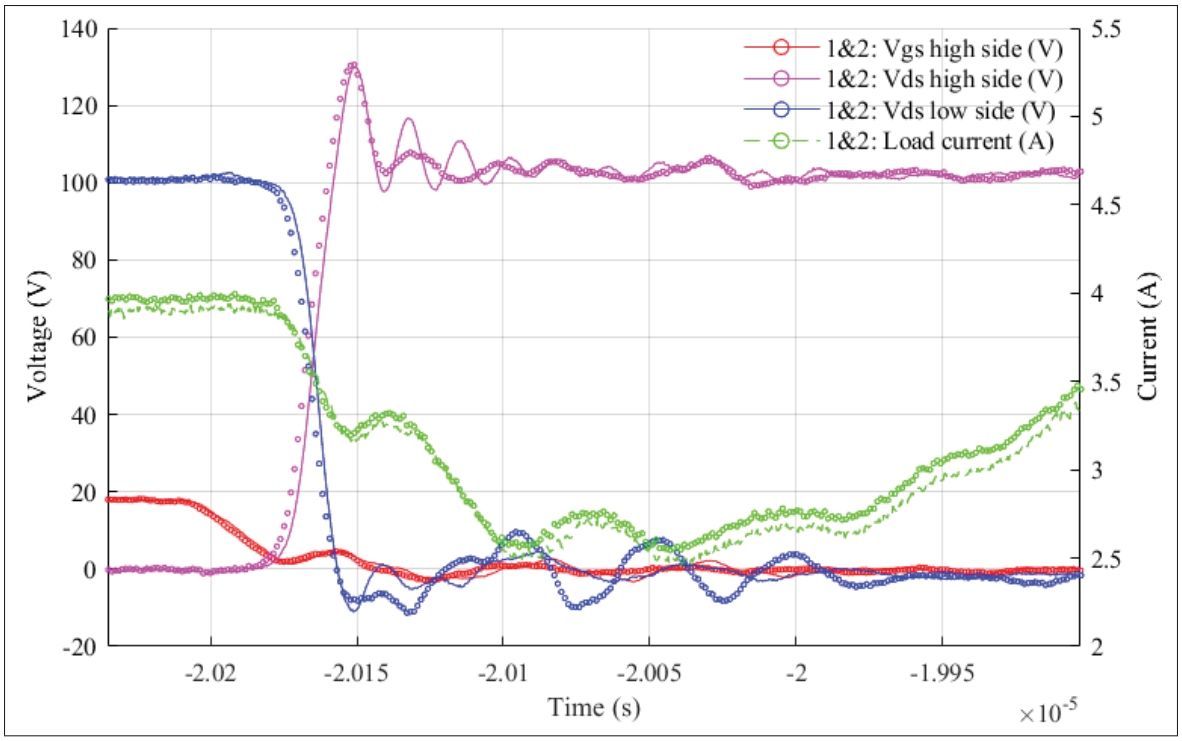

Figure 4.10 Impact of the source lead wire on turn-off waveforms (rounded results with added source lead wire)

leading toward expectations of a precise approximation of the low side MOSFET's current as if there was not any added lead wire. The resonant frequency and amplitude of turn-on and off waveforms for both high and low side MOSFETs only slightly changed. This phenomenon is even more relevant on the turn-on waveform of Fig. 4.11, where the maximum surge voltage amplitude of the low side MOSFET is increased following the expected impact of the added current measurement wire. The added lead wire increases the parasitic inductance in the switching loop which inevitably results in higher surge voltage. Overall, this method seems to offer minimal perturbations on the general switching behavior of MOSFETs under study, while offering a very reliable methodology to measure the reverse recovery current of the low side MOSFET.

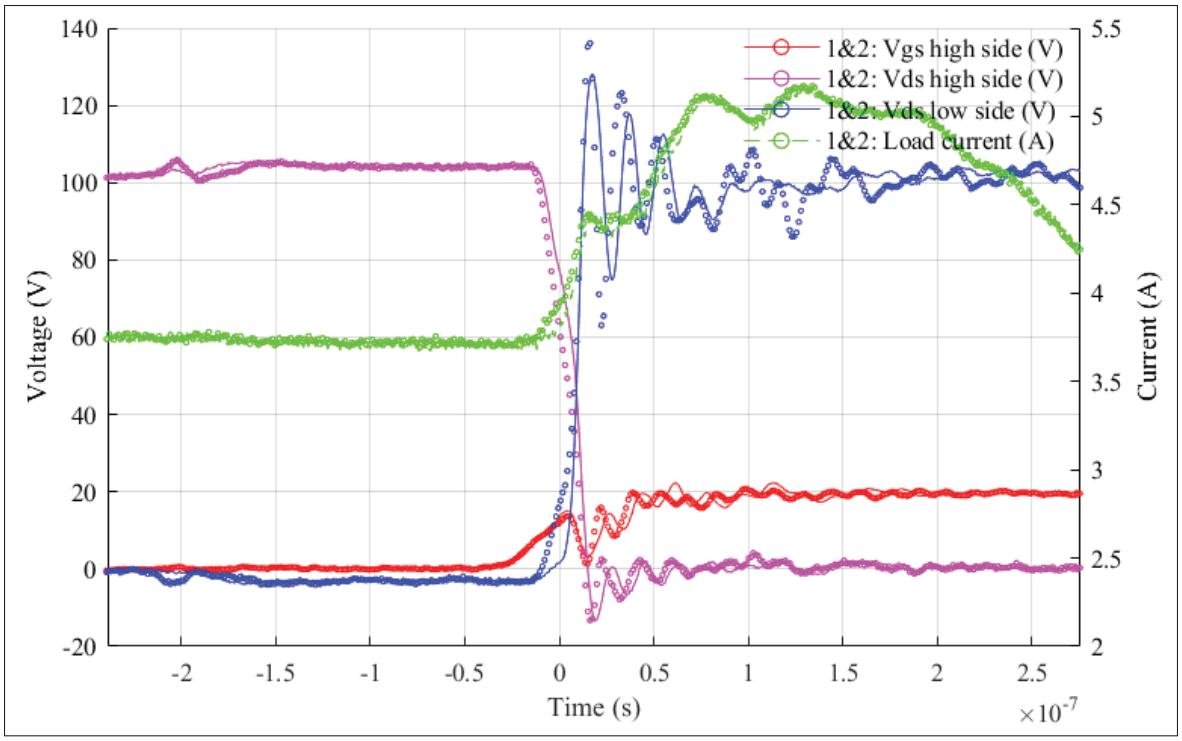

Figure 4.11 Impact of the source lead wire on turn-on waveforms
(rounded results with added source lead wire)

4.2.3.1 Comparison between the Added Lead Wire and the Proximity Magnetic Field

It is interesting to compare the lead wire measurements with the proximity field to validate previous observations. Figs. 4.12 and 4.13 illustrate a comparison between the computed current from the magnetic field and the current measurement with the added wire, respectively on the turn-off and turn-on intervals.

First, the turn-off waveform of Fig. 4.12 shows that the current from the direct Hall effect measurement reaches its final value at the load current even faster than expected with the proximity field methodology, implying that the coupling factor should have been even higher. Moreover, it seems like there is a slight divergence in the lead current measurement for a short period of about 200 ns after the beginning of the turn-off interval, which exactly corresponds to the gate driver delay. This divergence of the lead current measurement from the load current is the result of the low side MOSFET's gate charging through its source lead. As soon as the

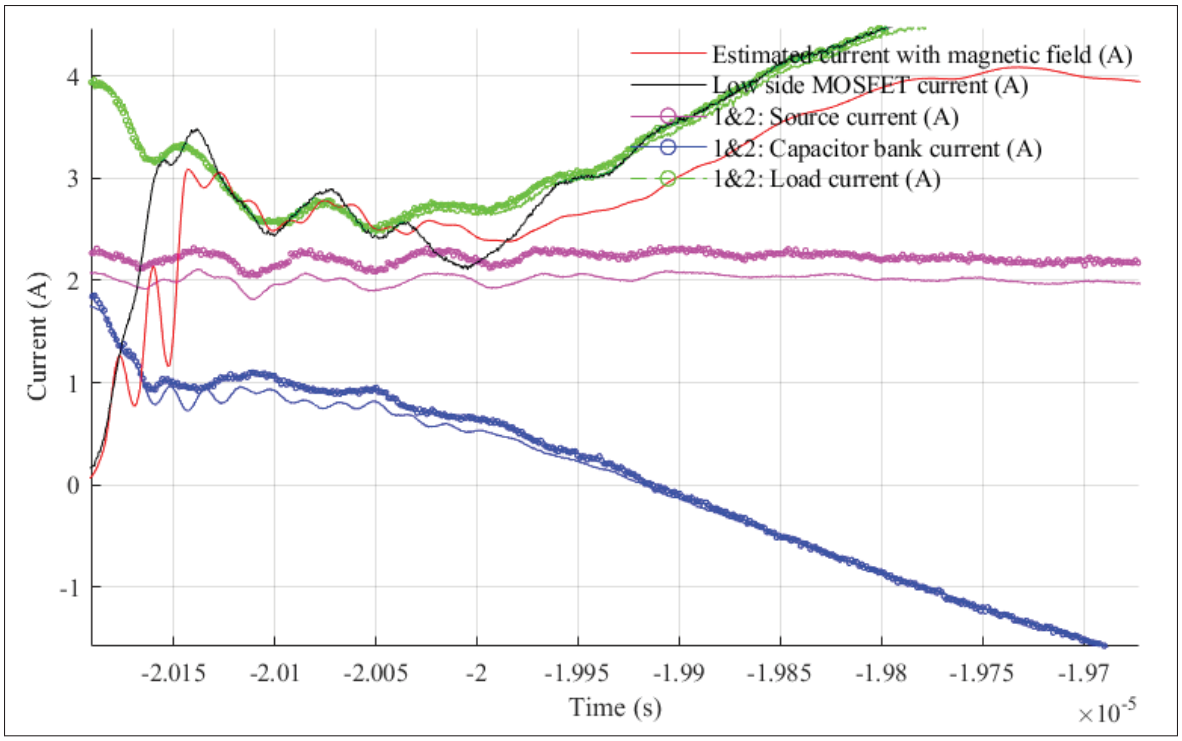

Figure 4.12 Comparison between the proximity field and source lead wire methodologies to extract the low side MOSFET's current on turn-off waveforms (rounded results with lead wire)

measured current of the low side MOSFET reached the load current, the actual internal's diode current can simply be approximated with the load current, resolving the problem of the influence from the gate current measurement.

In contrast, the turn-on waveform presented in Fig. 4.13 shows that the coupling factor of the magnetic field is already too high to offer a precise measurement of the reverse recovery current. Approximating the low side MOSFET's current from the proximity field methodology presented is definitely hardly reliable under semi-controlled conditions despite many efforts to minimize external perturbations. Conversely, the added magnetic wire offers the known precision of a Hall effect current probe CP031 without inducing major perturbations on all switching waveforms during both turn-on and turn-off intervals. In addition, the reverse recovery current extracted from the source lead methodology is not influenced by the low side gate circuit during high side

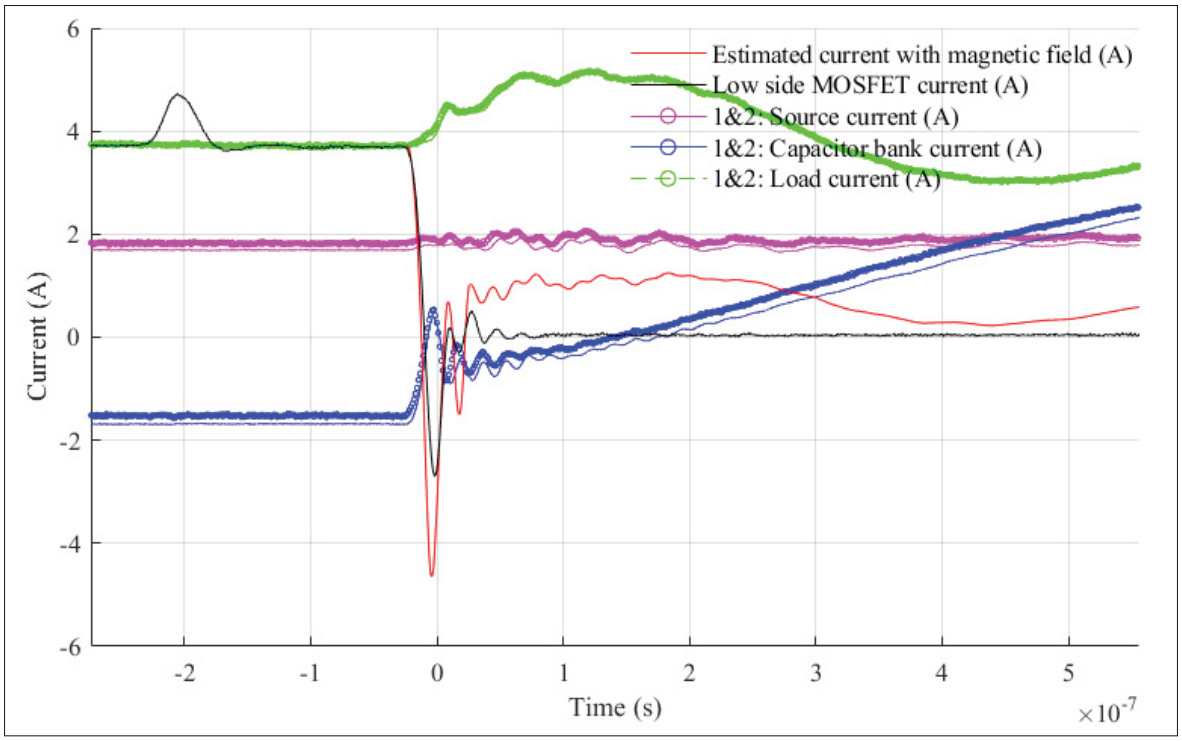

Figure 4.13 Comparison between the proximity field and source lead wire methodologies to extract the low side MOSFET's current on turn-on waveforms (rounded results with lead wire)

turn-on because the discharging of the low side gate circuit happens before the beginning of the turn-on interval, noticeable as a spike current measurement in Fig. 4.13.

4.3 Comparative Methodology of Experimental Waveforms Between MOSFETs

To compare the MOSFETs in the same conditions, the first experimentation consists of adapting the external gate resistance to obtain an equivalent total gate resistance considering the respective internal gate resistance of MOSFETs under study. Due to the very high internal gate resistance of 12 Ω for the SiC MOSFET, and only 0.75 Ω for the Si MOSFET, the equivalent total turn-on and off gate resistance have been fixed to 22 Ω and 15 Ω respectively. To respect the first experimental comparison criterion, the external turn-on and off gate resistance have been adapted at 22 Ω and 15 Ω for the Si MOSFET, resulting in a total equivalent turn-on gate resistance of 22.75 Ω, and 15.75 Ω at turn-off. In contrast, turn-on and off external gate resistance have been

fixed at 10 Ω and 3.3 Ω with the SiC MOSFET to obtain a total equivalent of 22 Ω and 15.3 Ω at turn-on and off. Fig. 4.14 illustrates the experimental turn-on waveform of the Si MOSFET under the specified equivalent gate resistance at a supply voltage of 100 V.

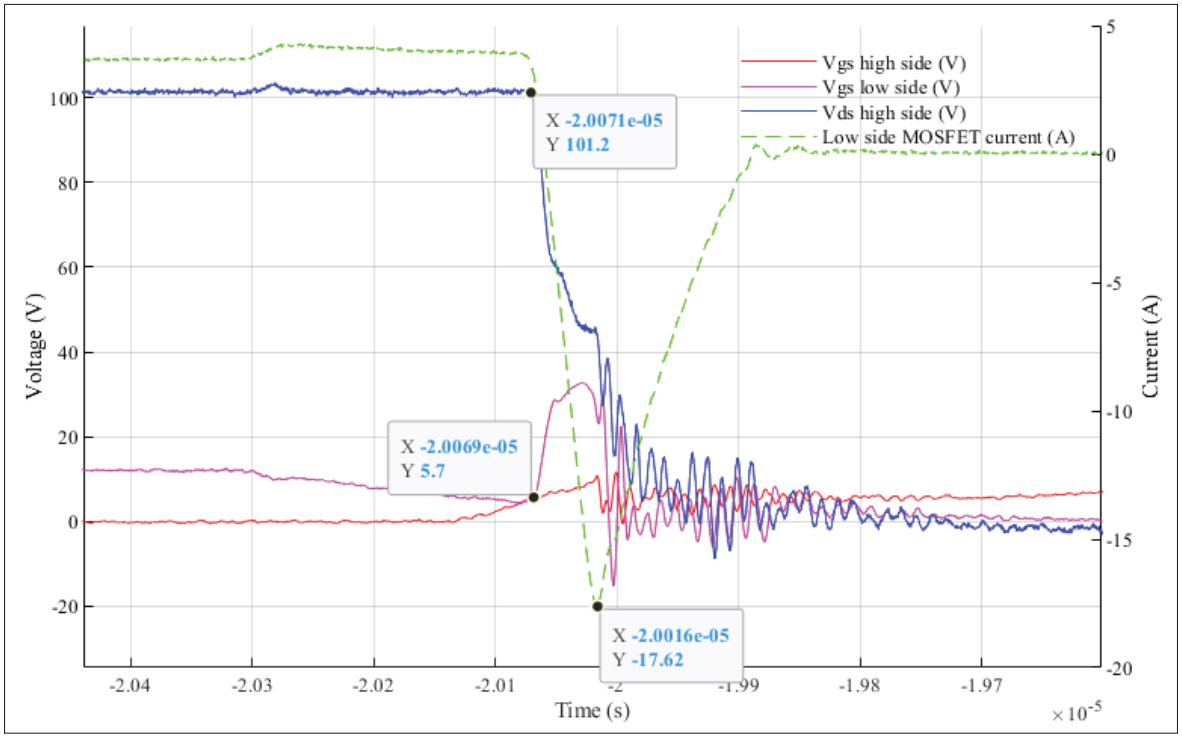

Figure 4.14 Si MOSFET: equivalent total gate resistance (22 Ω On & 15 Ω Off) turn-on waveform gate overlap (with source lead wire)

As shown in Fig. 4.14, a momentary short-circuit occurs during the turn-on process between the high side and low side MOSFET because the low side gate-source voltage is not yet at 0 V when the turn-on process starts. The defined dead time of 200 ns is not sufficient under this configuration with the Si MOSFET. Since the input capacitance of the Si MOSFET is approximately 4 times higher than the SiC MOSFET, it needs around 4 times longer to completely charge and discharge the input capacitance under equivalent gate resistance. Enlarging the dead time between high and low side MOSFET could resolve this problem, but this would require increasing the delay time near the maximum allowed value for the driver at 700 ns. Still, the low side MOSFET gate-source voltage would have barely made it to 0 V under the turn-off equivalent gate configuration.

Fig. 4.14 shows that comparative experimentation between technologies under an equivalent total gate circuit is not possible due to very large disparities in internal gate resistances between technologies. Reducing the equivalent total resistance comparison point to its minimum possible configuration of 12Ω, corresponding to the internal gate resistance of the SiC MOSFET alone, could have possibly been a suitable operating condition for the Si MOSFET. However, completely removing the external gate resistance with the SiC MOSFET resulted in very high surge voltage during transient intervals as shown in Fig. 4.15. The surge voltage on the drain-source measurements is not specifically problematic by itself, but the surge voltage appearing on the gate-source voltage measurement is very critical at its highest point (around 29V.) According to the manufacturer (Rohm Semiconductor, 2017), the maximum gate-source voltage of the SiC MOSFET should not exceed 26V for more than 300 ns. Even if the duration of the surge voltage on the gate circuit is far from 300 ns, this could quickly degrade the SiC MOSFET over time and eventually result in its failure.

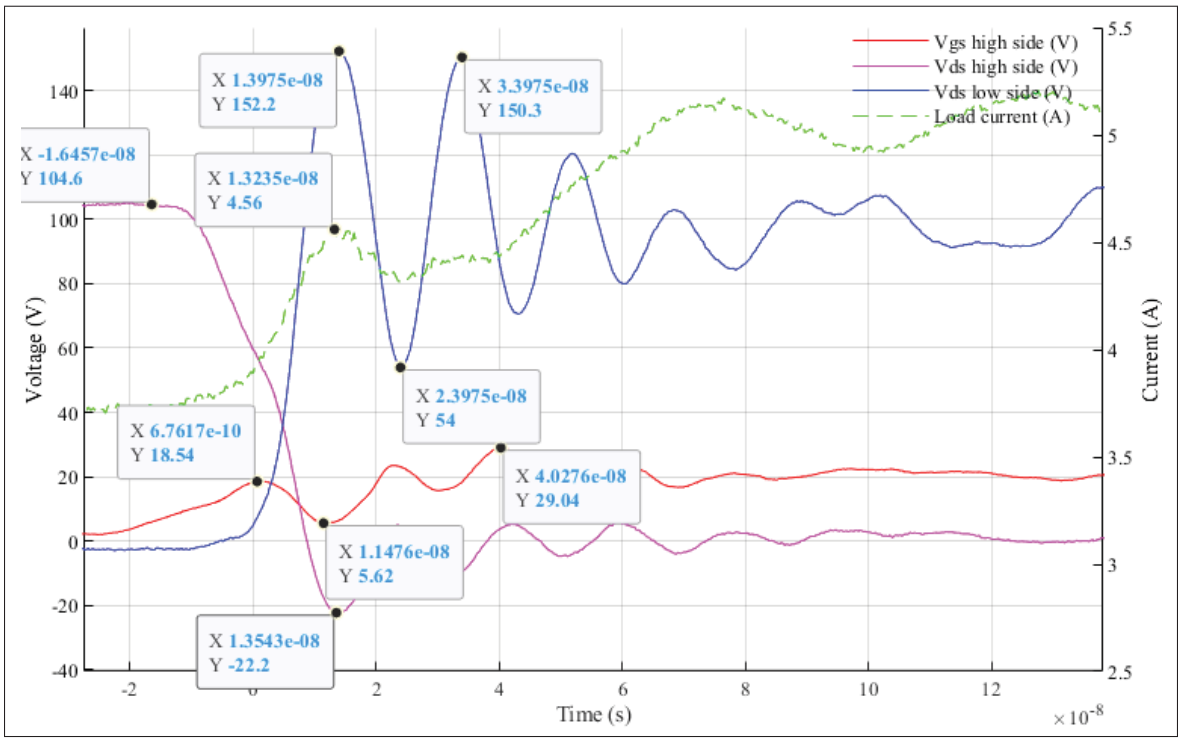

Figure 4.15 SiC MOSFET: equivalent total gate resistance (12 Ω On & 12 Ω Off) turn-on waveform gate overshoot (without source lead wire)

Due to this over voltage higher than the maximum allowed gate-source voltage, an equivalent gate resistance of 12 Ω is unsuitable to be defined as an official comparison configuration between MOSFETs.

Then, a comparison between MOSFETs under study will be done under the same external gate circuit, and the recommended respective driving voltage from manufacturers. This approach considers the MOSFET as a complete entity, including its internal gate resistance and capacitance. Any other elements on the experimental board, except the driving voltage, will stay the same to compute losses and observe the general switching behavior of all technologies under the same external conditions.

4.3.1 Parasitic Turn-On and Mitigation Techniques

Early measurements at 100 V with the Si MOSFET under a turn-on and turn-off external gate resistance of respectively 22 Ω and 3.3 Ω shows gate perturbations during the turn-on process as illustrated in Fig. 4.16. Further experiments showed that a slight increase in the duty cycle resulted in a complete induced false Turn-on issue of the low side Si MOSFET under this configuration. Fig. 4.17 illustrates the turn-on waveforms of the Si MOSFET at 100 V with turn-on and turn-off gate resistance of 22 Ω and 3.3 Ω at a duty cycle of 80 %.

Under the actual gate configuration of both Figs. 4.16 and 4.17, there is a sufficient delay between high and low side gate signals and a very reduced turn-off gate resistance which does not result in gate overlapping. Since the lead wire is not even soldered to the Si MOSFET at this point, it shows that the selected Si MOSFET is possibly highly susceptible to parasitic turn-on under increased voltage and current slope. Moreover, according to the Si MOSFET's datasheet (Infineon Technologies AG, 2012), increasing the device's temperature results in a decrease of the gate threshold voltage, making the MOSFET even more sensitive to parasitic turn-on under higher power switching conditions. To observe the reverse recovery current of the low side MOSFET, Fig. 4.18 illustrates the turn-on waveforms of the Si MOSFET under the same external conditions in Fig. 4.16, including the added lead wire on the low side MOSFET.

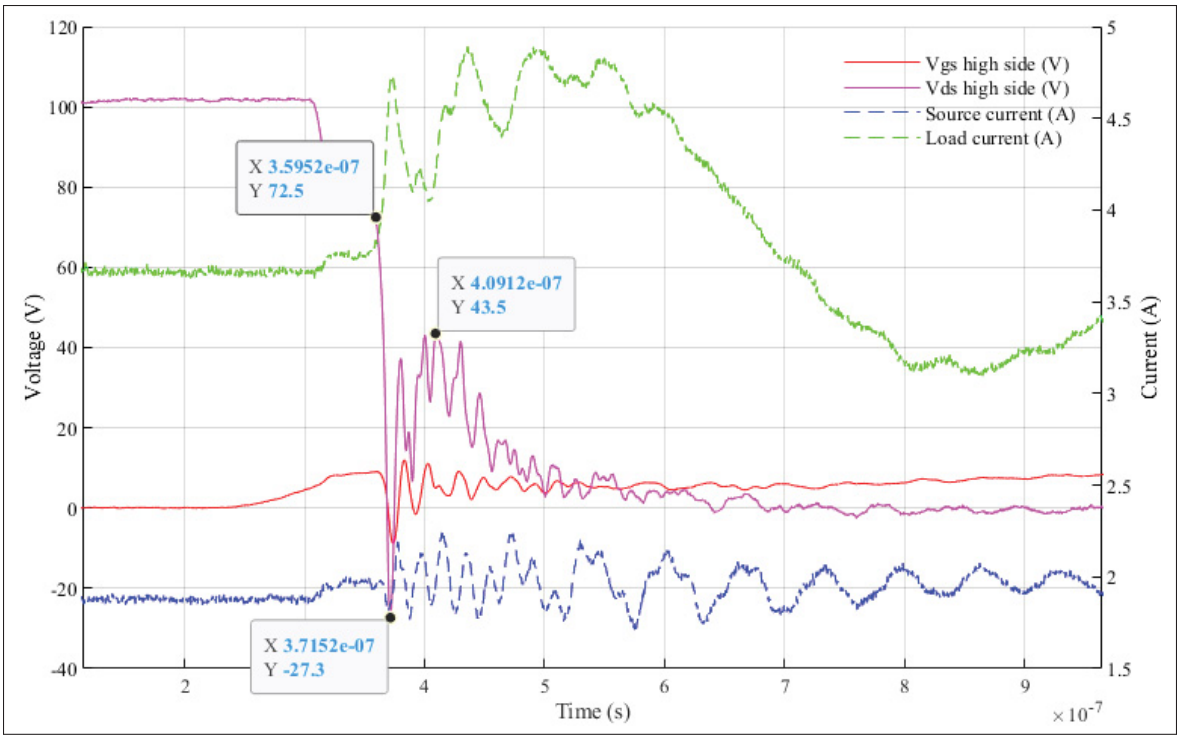

Figure 4.16 Si MOSFET: turn-on waveforms at 100 V without the added source lead wire (22 Ω On & 3.3 Ω Off & DT 50 %)

The added inductance on the switching loop from the lead wire seems to affect even more the gate circuit of the low side MOSFET.This shoot-through is mainly caused by the high dV/dt during the turn-on process, but the increase in parasitic inductance from the added wire and mutual coupling with voltage measurements is also contributing. The impact of dI/dt is highly dependant on the parasitic inductance. The higher its value, the more it contributes to an accidental turn-on (ON Semiconductor, 2016).

Fig. 4.18 shows that the reverse recovery current is repeated during the turn-on process of the high side MOSFET. At the first turn-on attempt, a major surge voltage appears on the low side gate circuit, reaching more than 20V. This evidently leads to an accidental turn-on of the low side MOSFET, resulting in a resistive shoot-through for a short duration between the high side and low side MOSFET. Then, the actual reverse recovery current is occurring right after, when

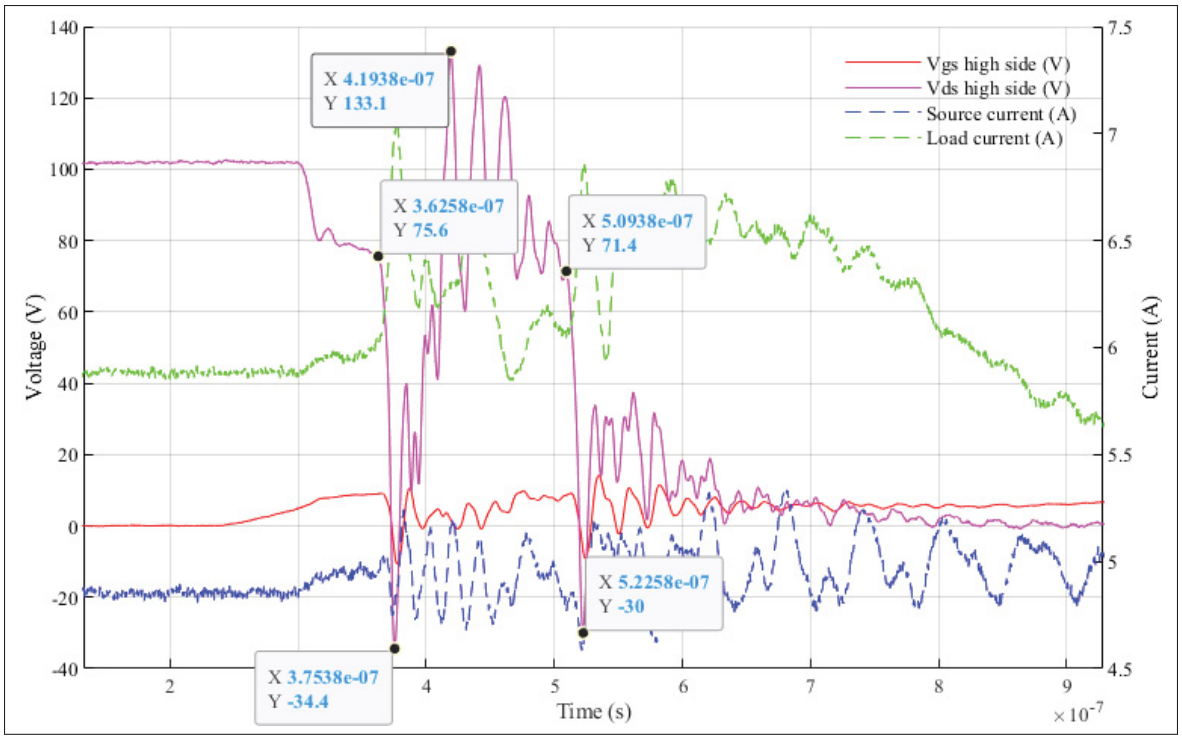

Figure 4.17 Si MOSFET: turn-on waveforms at 100V without the added source lead wire (22Ω On & 3.3Ω Off & DT 80%)

the gate-source voltage of the low side MOSFET went back to 0V. Using such waveform is not a good way to compute losses because it is not representative of a normal switching conditions.

Identifying the exact cause of this parasitic turn-on issue is not as straightforward as it looks, as it is well beyond the impact of just one element. A lot of small details can contribute to creating this problem. However, the most probable cause is the very high dV/dt on the low side MOSFET during high side turn-on, namely high dV/dt false induced accidental turn-on. The high dV/dt during the high side turn-on results in a capacitive voltage divider between the Miller capacitance and the gate-source capacitance which can trigger the low side MOSFET on. Even if the gate circuit is forcing the gate voltage to zero, this capacitive voltage divider induces a current flowing through the gate resistor via the Miller capacitor. However, since the gate resistance offers a high impedance path, most of the current generally go through the gate-source capacitance (ON Semiconductor, 2016). This causes an increase of voltage on the gate-source

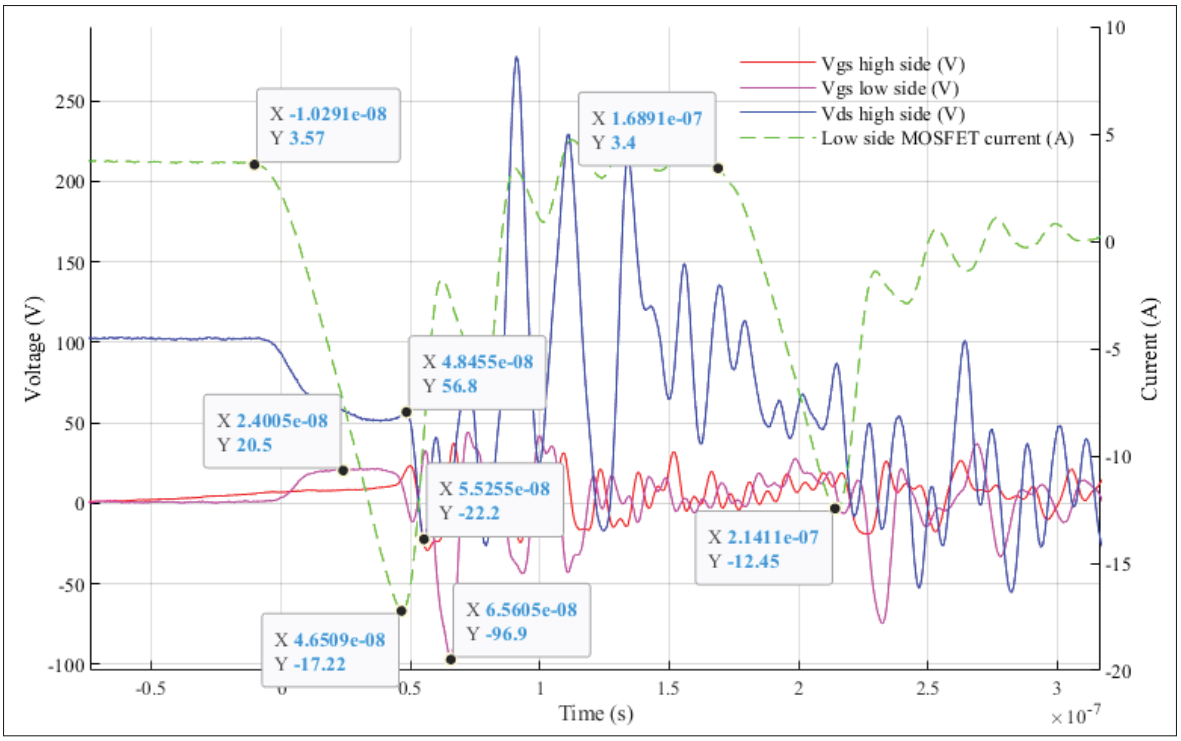

Figure 4.18 Si MOSFET: turn-on waveforms at 100V with the added source lead wire (22 Ω On & 3.3 Ω Off & DT 50 %)

capacitance possibly exceeding the gate threshold and resulting in a self-turn-on event (Graovac, 2008; Toshiba Electronic Devices & Storage Corporation, 2018; ON Semiconductor, 2016). Placing a resistor between the gate and source lead of low side MOSFET could help to mitigate this problem (Graovac, 2008). However, this parasitic turn-on process is the impact combination of parasitic inductances, resistances and capacitances, caused by geometric and designs layout and even dependant on the MOSFET itself (Graovac, 2008; ON Semiconductor, 2016).

The very high dI/dt occurring at the reverse recovery of the low side MOSFET is also responsible for this problem since this inevitably causes high inductive voltage spikes and significant high frequency (HF) ringing in the bridge (Graovac, 2008). In addition, the added lead current measurement wire increases the common source inductance of the low side MOSFET, amplifying the impact of the high dI/dt on the gate circuit during the reverse recovery process (ON Semiconductor, 2016). Combinations of all these different factors can result in a parasitic

turn-on of the low side MOSFET (Graovac, 2008). One of the early solutions to this problem is to choose a power MOSFET with low sensitivity to parasitic turn-on. The ratio between the gate-source capacitance and Miller capacitance has to be as high as possible (Graovac, 2008; Toshiba Electronic Devices & Storage Corporation, 2018), preferably higher than 15, but at least 10 at supply voltage (C_{gs}/C_{gd}) (Graovac, 2008). A capacitor can even be added between the gate-source terminal of the MOSFET to increase even more this ratio, but this will surely slow down the switching speed of the device (Toshiba Electronic Devices & Storage Corporation, 2018). Moreover, increasing the high side gate resistance might be an effective solution to reduce the induced dV/dt on the low side MOSFET, but this also results in a reduction of the high side MOSFET's switching speed (Toshiba Electronic Devices & Storage Corporation, 2018).

Under the specified experimental conditions at a voltage supply of 100 V, the capacitance ratio for the Si MOSFET is as high as 443, around 10 for the SiC MOSFET and around 72 for the GaN MOSFET. Unlike with the Si MOSFET, the SiC and GaN MOSFETs do not exhibit the same parasitic turn-on problem under equivalent external gate resistances. However, the gate-source capacitance is 2 to 4 times smaller, and the internal gate resistance is also higher for both WBG MOSFETs under study. During high side turn-on transients, high dV/dt and voltage change of the low side MOSFET results in a gate current flowing in addition to a non-linear change of the capacitance's value, more particularly the Miller capacitance. Higher gate resistance inevitably causes higher gate voltage and more chance for it to end in a parasitic turn-on. The higher is the parasitic capacitance ratio (C_{gs}/C_{gd}), and the higher is the voltage rise across the Miller capacitance instead than the gate-source capacitance, resulting in less chance to trig an accidental turn-on. Using a negative turn-off voltage and ferrite bead on the gate circuit might further help to mitigate parasitic turn-on issue. Addressing this problem is critical since parasitic turn-on results in increasing power loss and might even cause permanent damage to the device (Toshiba Electronic Devices & Storage Corporation, 2018). The preferable approach is to choose a MOSFET less susceptible to this problem. A high (C_{gs}/C_{gd}) ratio (Graovac, 2008; Toshiba Electronic Devices & Storage Corporation, 2018), small C_{gd} capacitance, a negative turn-off voltage or a gate shunt circuit, a small turn-off resistance (Toshiba Electronic Devices

& Storage Corporation, 2018) and a small input capacitance C_{iss} are the most effective early design approach to avoid self-turn-on phenomenon.

Since the low side MOSFET is considered as the freewheeling diode under the experimental configurations, multiple modifications have been implemented to observe the effect of adding parallel resistance or capacitor to the gate-source capacitance of the low side Si MOSFET to mitigate the parasitic turn-on effect. Also, reduction of the high side switching speed by increasing the turn-on gate resistance or reduction of low side turn-off gate resistance either help to reduce perturbations from high dV/dt. Despite mitigation of the accidental short circuit during high side turn-on, none of the modifications have been satisfying to improve voltage waveform allowing to perform high side losses computation of the Si MOSFET at 100 V due to a very high ringing. Further modifications through parasitic inductance reduction from better board layout or adding ferrite bead on the gate, or simply choosing a Si MOSFET with reduced capacitance and adequate internal capacitance ratio could bring major improvements to avoid false induced turn-on problems. All considered, using a 100 V supply seems to cause too high dV/dt and very bad voltage waveform which makes it impossible to compute losses under such conditions. Then, the voltage supply has been reduced to 50 V in the objective to observe acceptable waveform for losses computation with the Silicon MOSFET under study. Fig. 4.19 illustrates the turn-on waveform of the Silicon MOSFET at a voltage supply of 50 V with turn-on and turn-off gate resistance of respectively 22 Ω and 3.3 Ω.

Decreasing the supply voltage to 50 V also reduces the dV/dt to 2 V/ns instead of 8 V/ns which helps to attenuate the ringing on every voltage waveform, and completely eliminate the parasitic turn-on problem. However, at this early step in the experimentation, multiple voltage measurements were performed with a common measurement point with differential probes to extract voltage waveform. Since major influence from the switching process is perceptible on differential voltage measurements, a pigtail probe has been used to take voltage measurements only one at a time as illustrated in Fig. 4.20. Taking the voltage measurements without other simultaneous voltage measurements resulted in major improvements compared to taking multiple voltage measurements as observed in Fig. 4.19. However, it is impossible to perform high side

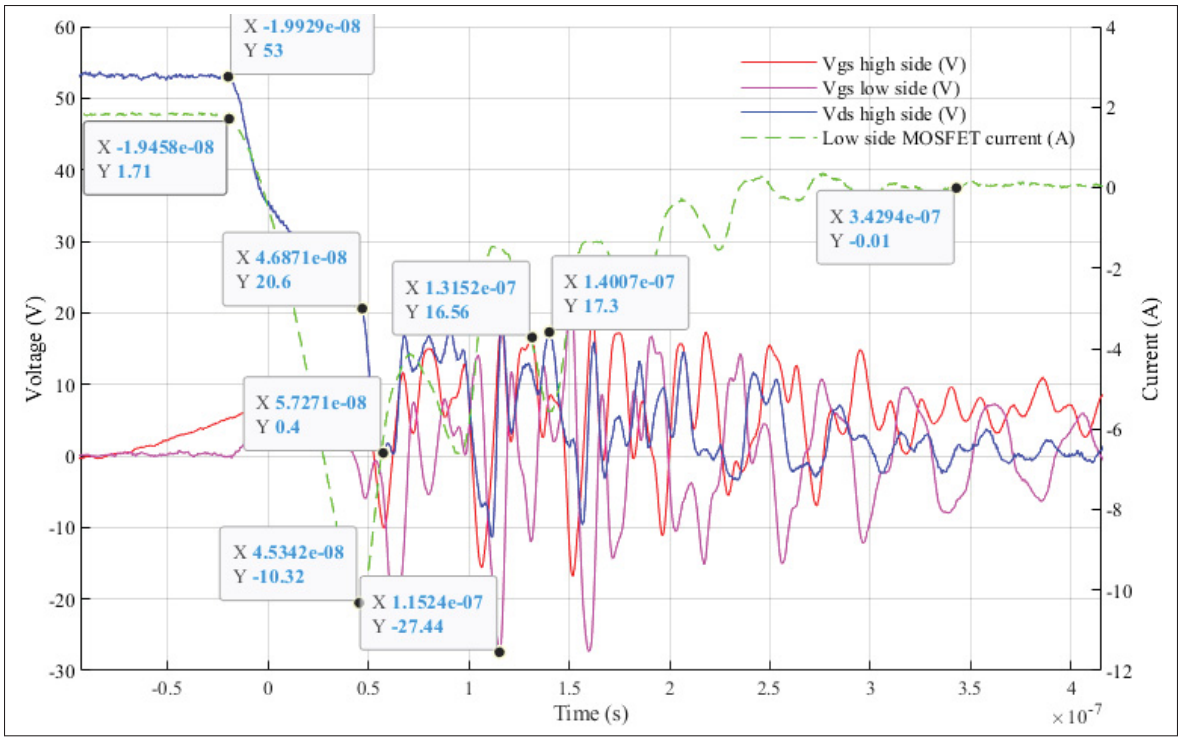

Figure 4.19 Si MOSFET: turn-on waveforms at 50 V with the added source lead wire (22 Ω On & 3.3 Ω Off & DT 50 % with multiple simultaneous differential voltage probes)

voltage measurements with a passive probe due to the absence of complete insulation between the oscilloscope and the power supply ground.

To avoid parasitic turn-on problem, choosing power MOSFETs properly based on application requirements, assessing board layout to reduce parasitic inductance, and respecting the maximum dV/dt are essential steps in the early design stage of a switching application. Yet, taking very reliable voltage and current measurements turn out to be more difficult than expected. Major improvements on voltage waveform from reduced mutual coupling due to reduced measurement surface from a pigtail probe raises major questions about the accuracy of measurement techniques. Then, a review and deeper understanding and development of the experimental measurement technique seems mandatory to obtain high reliability of measurements.

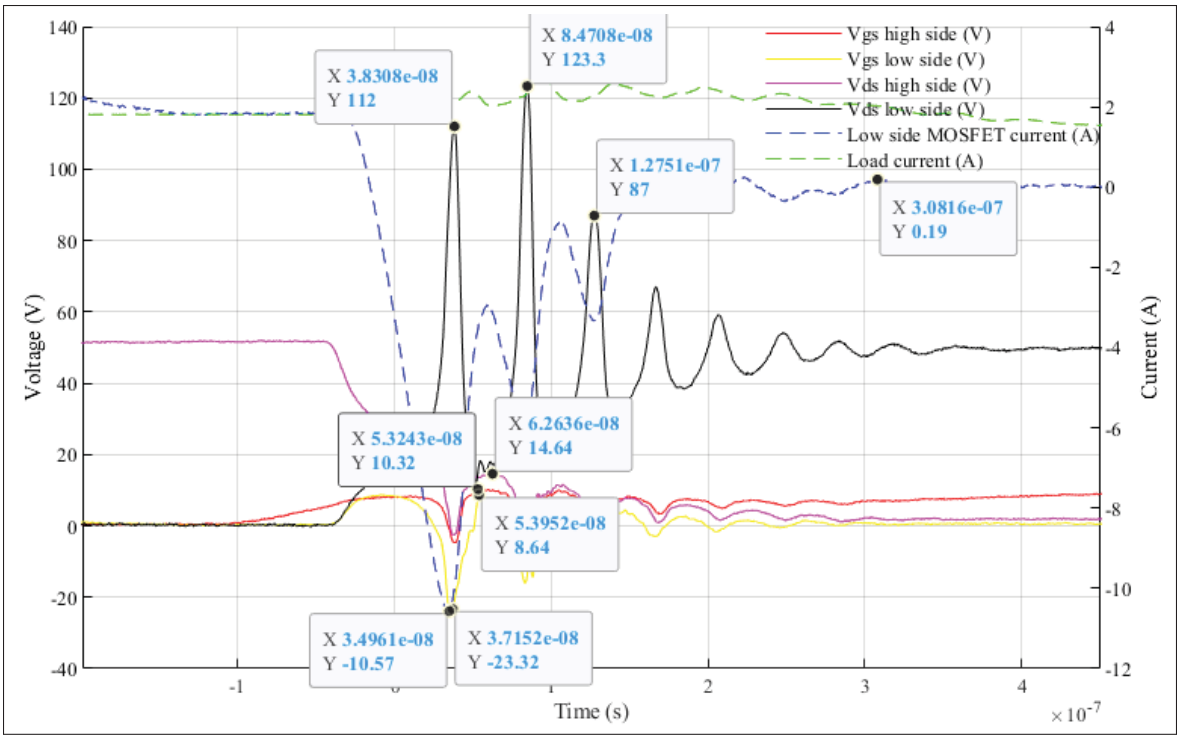

Figure 4.20 Si MOSFET: turn-on waveforms at 50 V with the added source lead wire (22 Ω On & 3.3 Ω Off & DT 50 % with a single passive probe)

4.3.2 Adaptation of Voltage and Current Measurement Techniques

Advanced review of different probing solutions from Lecroy's webinar (Johnson, 2019) and proactive support from highly-skilled Lecroy's engineers helped to determine the most reliable experimental measurement methodology under the half-bridge configuration.

First, taking high side voltage measurements with a non-differential probe can results in a potential short circuit and damages to the oscilloscope's input port during transient if the power supply ground is not insulated from the oscilloscope's ground. Increased common-mode rejection ratio (CMRR) and smaller input capacitance of differential probe makes it perfectly suited for non-isolated high dV/dt voltage measurements. In addition, reducing mutual coupling through measurement surface reduction can further reduce perturbations from high dI/dt, and make differential probe perfectly suited for high side voltage measurements as illustrated in Fig. 4.5.

However, due to the major reduction in the mutual coupling of voltage measurements from passive probes with pigtail observed in Fig. 4.20, it is worth exploring a low side switching configuration to compare general measurements quality for losses computation. Under this new proposed configuration, the high side MOSFET act as the freewheeling diode whilst the low side MOSFET as the switching device referenced to the ground. Thus, it is now possible to use non-differential measurement solutions as passive probes, direct SMA, BNC or optical probes to perform losses computation. Then, individual review of suited probe solutions will allow to define the best way to perform voltage and current measurements under the established half-bridge configuration.

First, passive probes can provide a high CMRR and a direct BNC or SMA connection to the low side MOSFET's lead through the soldering of an adaptor tip. It further reduces the mutual coupling by reducing the measurement surface. Compatible passive probes as PP023/PP0006A are mainly SMA attenuated line with a 10 $M\Omega$ impedance to provide a reduction by a factor of 10. The bandwidth of 500 MHz, the maximum voltage insulation of 500 V RMS and the low input capacitance and short connection options makes it a well-adapted solution to take low side voltage measurement referenced to a common ground.

Then, direct SMA or coaxial line connections are suited for very low voltage measurements like low side gate-source voltage and shunt resistance voltage. Still, non-differential measurements have to be referenced to the ground to avoid a possible short circuit by using a non-insulated power supply. Direct line measurements can provide very high reliability of voltage measurements under a perfect impedance matching between the line and the oscilloscope input port. However, this means low impedance of the oscilloscope input port and very limited voltage measurements under 5V to avoid damaging the oscilloscope. Performing higher, but limited voltage measurements would still be possible with a direct line connection under an increased impedance of the oscilloscope input port. However, bad impedance matching will cause reflection in the line resulting in unreliable voltage measurements. Also, optically isolated differential probes with tip options are suited probes for high and low side measurements with high reliability, high CMRR,

high sensitivity and low mutual coupling. However, such technologies are normally restrained for low voltage measurements as gate signals and current measurement through shunt resistance.

Regardless of the voltage probe technology, avoiding common node voltage measurements is essential to limit the impact of added inductance and capacitance to the switching process while avoiding perturbations from shared measurement points under multiple voltage probes configuration. Then, only one voltage measurement is performed at a time and the Hall effect current measurements CP031 probes are chosen for all current measurements. Also, since the current waveform is stable, it is convenient to use it for the trigger. Fixed trigger position on a common current measurement to all voltage measurements allows providing a good time fit between voltage and current measurements. But in all cases, small time adjustments are often required to provide a logical fit between voltage and current measurements in Matlab to compute losses. Fig. 4.21 presents comparative voltage measurements of drain-source voltage from differential probes ADP305, HVD3106 and passive probe PP006A on the low side MOSFET with the added source lead wire during the blocked state. Due to a lack of room to insert the source lead wire on the freewheeling high side MOSFET, the low side MOSFET is acting as the switching device whilst providing a direct current measurement from the added source lead wire. Then, a steady trigger on the low side MOSFET's current measurement provides a common time reference between voltage measurements. One-by-one, voltage measurements are performed in the shortest possible delay after the experimental board has reached a stable operating temperature.

Fig. 4.21 shows a major difference from the differential probe ADP305 measurements compared to the new generation differential probe HVD3106 and passive probe PP006A with pigtail tip. Compared to differential probe HVD3106, probe ADP305 offers a very low CMRR and lower bandwidth with higher input capacitance which results in less reliable voltage measurement. It is easily perturbed under common mode measurements. This would get even worst under multiple common node voltage measurements due to the higher input capacitance of the ADP305, but this is avoided in this specific scenario. Then, a comparison between the passive probe PP006A and the differential probe HVD3106 does not show much difference under the transients

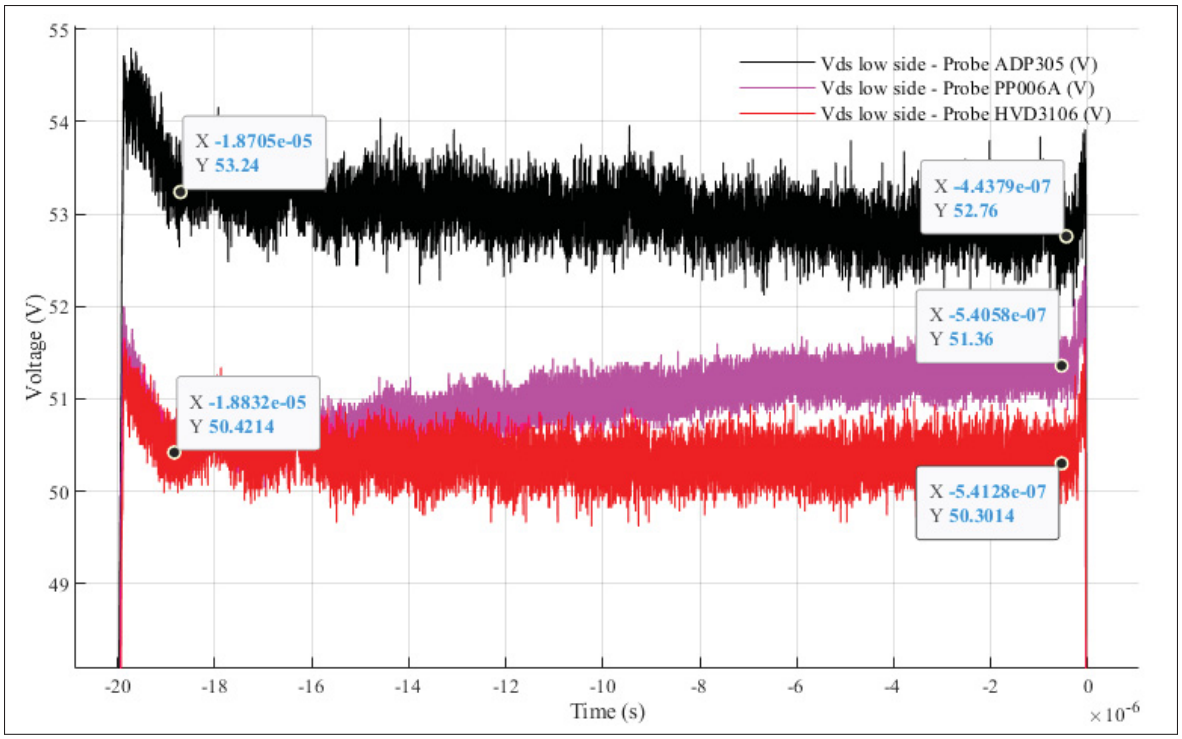

Figure 4.21 Si MOSFET: comparison of low side voltage measurements on turn-off steady state waveforms at 50V with the added source lead wire on low side switching MOSFET (22 Ω On & 3.3 Ω Off & DT 50 %)

measurements. However, the passive probe voltage measurement is drifting away over time whilst the HVD3106 is very steady. Under steady state voltage measurements as presented in Fig. 4.21, differential probe HVD3106 highlights better performance in addition to providing fully insulated voltage measurements also suited for high side measurements unlike for passive probes. Then, Figs. 4.22 and 4.23 illustrate performance comparison between differential and passive probes of the low side drain-source voltage measurements for the turn-on and turn-off switching processes, respectively.

As shown in Figs. 4.22 and 4.23, the differential probe ADP305 once again shows inconsistent voltage measurements compared to PP006A and HVD3106. To avoid offset voltage and current measurements, a complete auto zero procedure is always executed and recommended for both voltage and current probes unconnected from the circuit before each experiment. It also includes degaussing the current probes. Despite following rigorously the measurement procedure, the

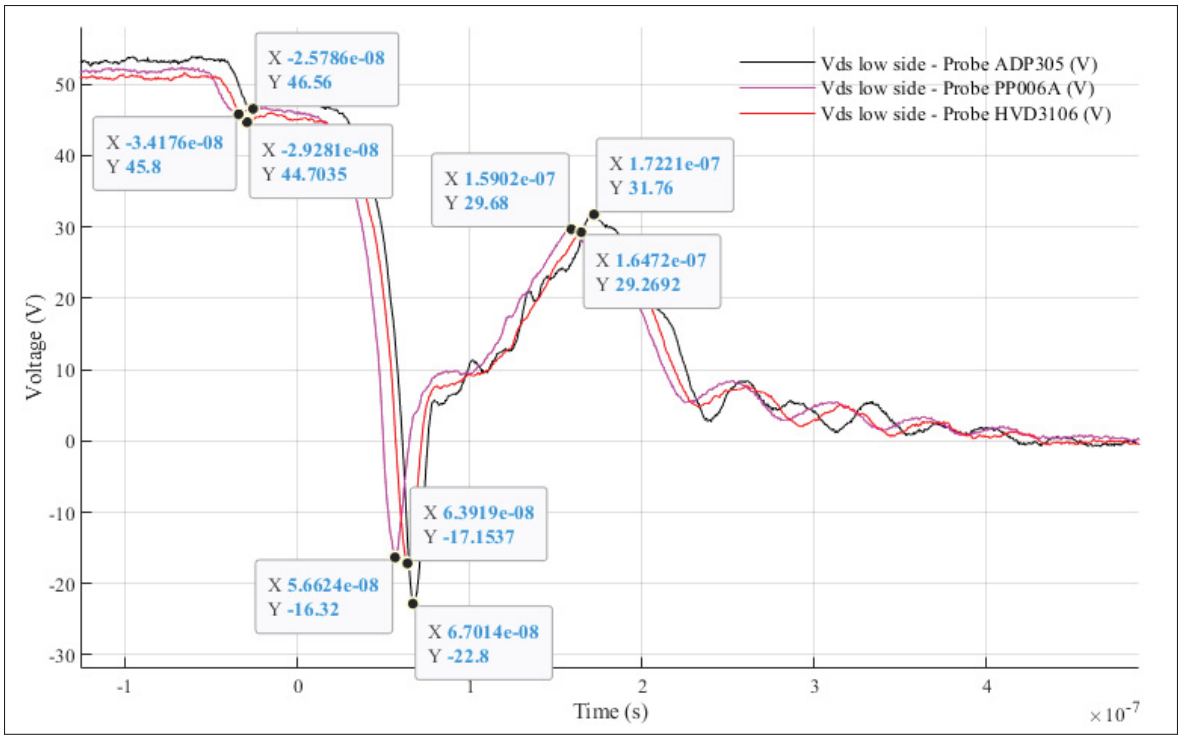

Figure 4.22 Si MOSFET: comparison of low side voltage measurements on turn-on transient waveforms at 50 V with the added source lead wire on low side switching MOSFET (22 Ω On & 3.3 Ω Off & DT 50 %)

differential probe ADP305 exhibits an offset voltage measurement and an increased influence from mutual coupling during fast voltage transient measurements compared to other probing solutions. In addition, the ADP305 voltage measurement is delayed over time and drifts continuously as time goes by partly due to the loading of its increased probe input capacitance on the circuit. In regard to the HVD3106 and PP006A, not significant differences are observable since measurements are very similar. However, the HVD3106 showed more stability for steady state voltage measurement with a complete absence of drifting over time in contrast to the PP006A as illustrated in Fig. 4.21. In addition to offering very reliable transient and steady state voltage measurements similar to what has been obtained with the pigtail passive probe PP006A, the HVD3106 differential probe also offers differential measurements, making it the chosen voltage probe for all experimental measurements. Since only one voltage measurement is performed at a time with a fixed current trigger reference, it is legitimate to question the

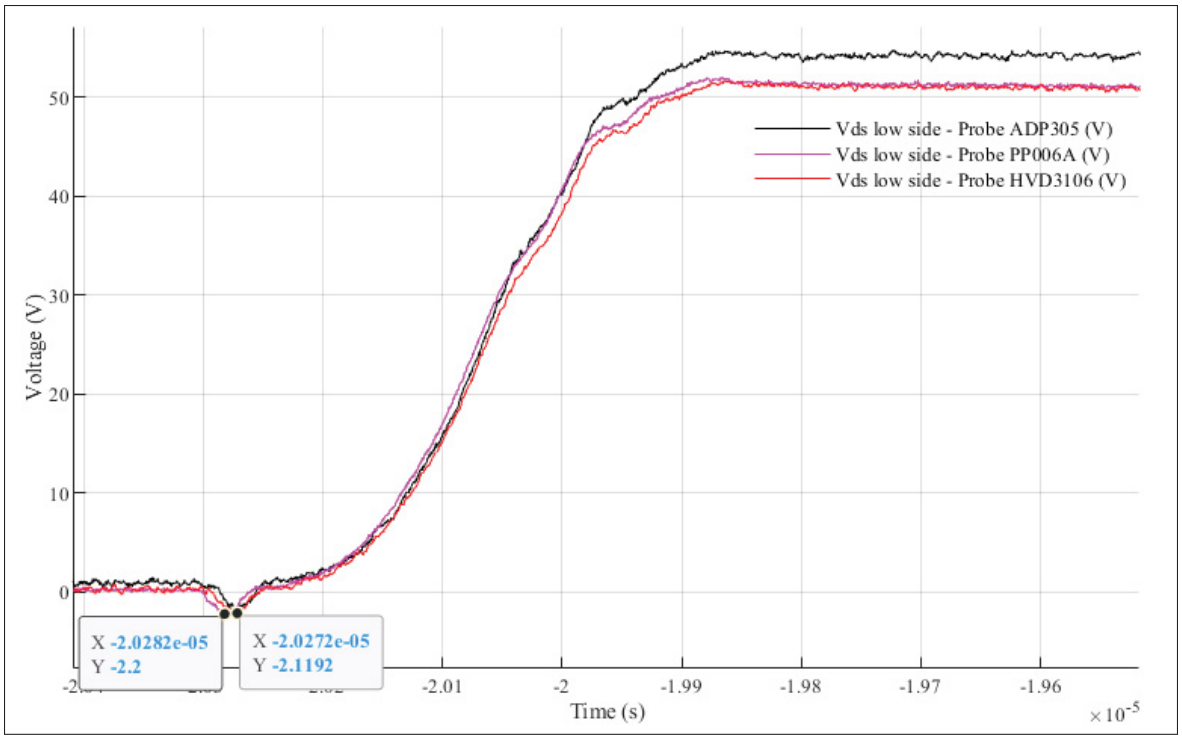

Figure 4.23 Si MOSFET: comparison of low side voltage measurements on turn-off transient waveforms at 50 V with the added source lead wire on low side switching MOSFET (22 Ω On & 3.3 Ω Off & DT 50 %)

stability of the current measurement over time since it could induce false time adjustments between all voltage measurements. To avoid such perturbations, it is essential to wait for the temperature stability of the experimental board before taking any measurements. With each voltage measurement, the current is also measured. Then, comparison under Matlab ensure a perfect time synchronization between all measurements. Fig. 4.24 presents a comparison between load and low side MOSFET current measurements performed for the first and last voltage measurement.

As shown in Fig. 4.24, adequate time synchronization between the first and last current measurement is observable without any time adjustment in Matlab. Then, taking one-by-one voltage measurements under a fixed current trigger reference and a short delay once temperature stability is reached offer adequate time synchronization with minimal perturbations. Even if the

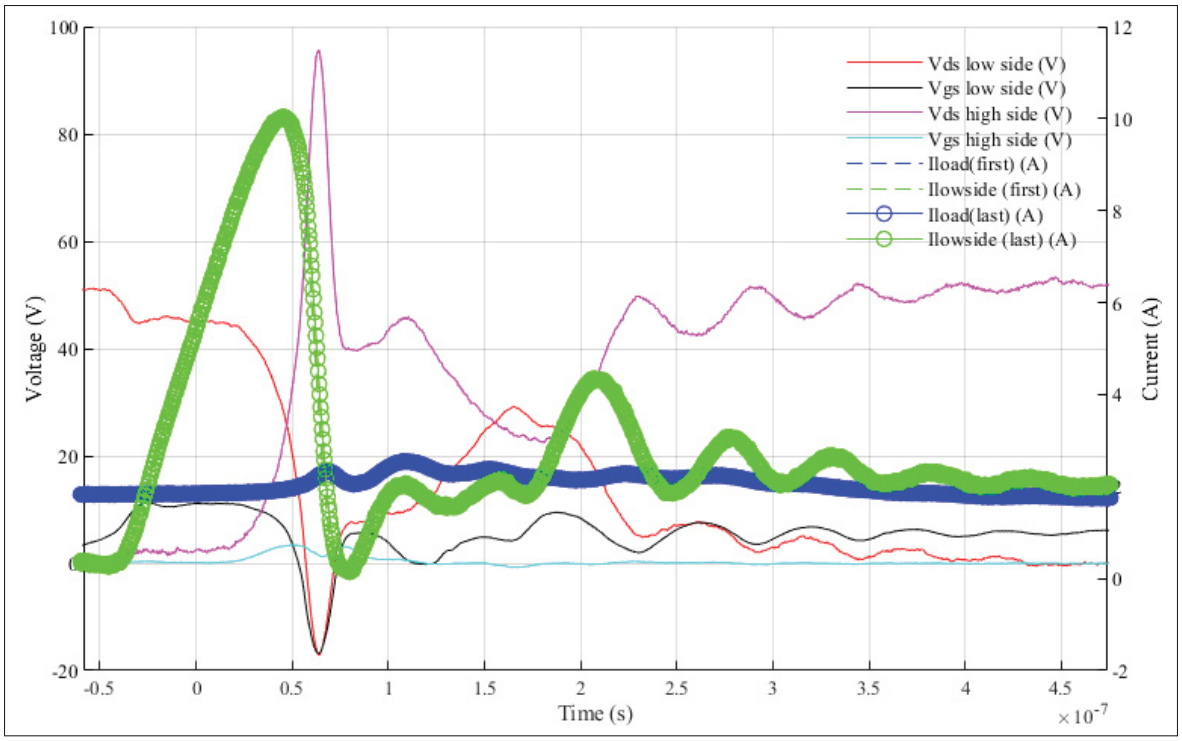

Figure 4.24 Si MOSFET: comparison between first and last CP031 current measurements on transient waveforms at 50 V with the added source lead wire on low side switching MOSFET (22 Ω On & 3.3 Ω Off & DT 50 %)

delay between measurements is of short duration, the temperature of the board increase a little between the first and the last measurements causing a neglectable difference.

4.3.3 Experimental Configuration for Waveform Extraction

Comparison of voltage and current probing solution allowed to define a methodology to extract the waveforms with the least possible disturbance of both the switching process and extracted measurements. Yet, even at a reduced voltage of 50 V, major disturbance on drain-source voltage shows switching waveforms that are not appropriate ones for losses computation. Figs. 4.25 and 4.26 respectively present turn-on and turn-off switching waveforms of the Si MOSFET at 50 V under a low side switching configuration with the added wire placed on the source lead. All recommendations are applied to minimize the disturbance of measurements and the experimental switching behavior.

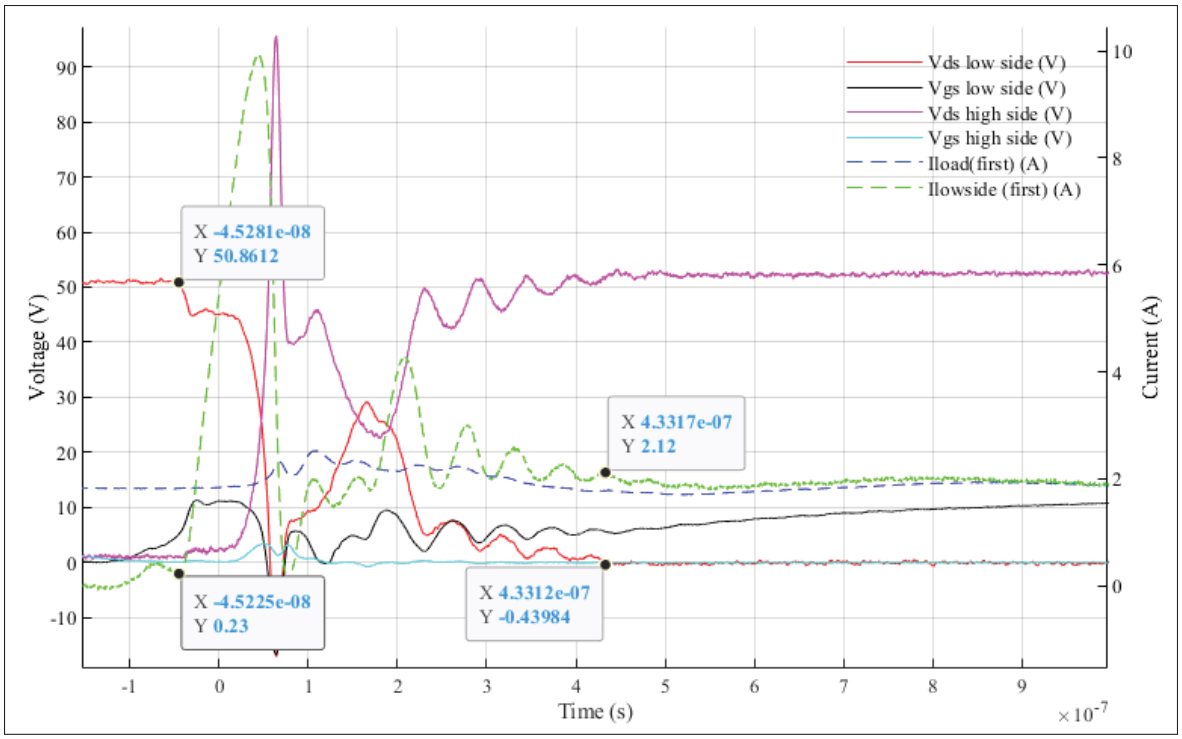

Figure 4.25 Si MOSFET: turn-on waveforms of low side switching MOSFET at 50 V with the added source lead wire (22 Ω On & 3.3 Ω Off & DT 50 %)

As mentioned earlier, major disturbance on low side switching MOSFET drain-source voltage is observable during turn-on process as illustrated in Fig. 4.25. This is unusable for losses computation because voltage waveforms are not compliant with expectations of normal switching waveforms. In addition, turn-off waveforms illustrated in Fig. 4.26 show major influence from the low side gate current on the low side MOSFET current measurement because they share a common connection. Due to the actual configuration of low side switching MOSFET with the added wire, the current measurement also captures the gate current during both turn-on and turn-off intervals which is indistinguishable from the real drain-source switching current. Then, one possibility to resolve this issue is to use the drain lead instead of the source lead of the low side switching MOSFET to obtain an isolated measurement of the switching current. Figs. 4.27 and 4.28 respectively present turn-off and turn-on switching waveforms of the Si MOSFET at 50 V using a low side switching configuration with the added wire placed on the drain lead.

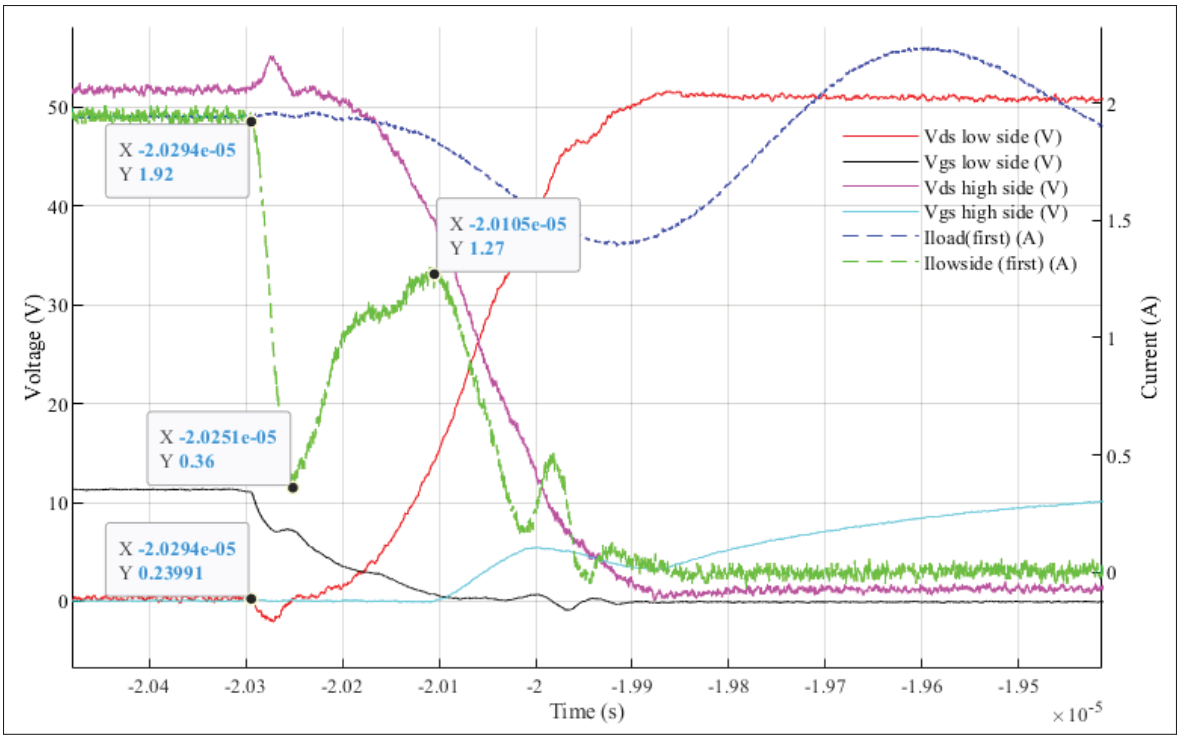

Figure 4.26 Si MOSFET: turn-off waveforms of low side switching MOSFET at 50 V with the added source lead wire (22 Ω On & 3.3 Ω Off & DT 50 %)

Once again, all measurement recommendations are applied to minimize the disturbance of measurements whilst avoiding loading the circuit.

In Fig. 4.27, current and voltage waveforms show compliance with expectations of a normal turn-off switching process with the drain lead wire on the low side MOSFET. However, an evident perturbation on the low side MOSFET switching current is still noticeable when the drain-source voltage gets near the supply voltage value. The internal Miller capacitance of the MOSFET is highly dependent on the drain-source voltage. In this specific case, the Miller capacitance is highly reducing in value as the drain-source voltage increases. It tends to momentarily increase back the current measurement and cause resonance with the parasitic inductance of the switching loop. Quantification of the influence from the Miller capacitance on the switching current is very difficult since its value follows a non-linear relationship with the drain-source voltage. Attempt in characterization of the impact from the Miller capacitance through voltage measurement will

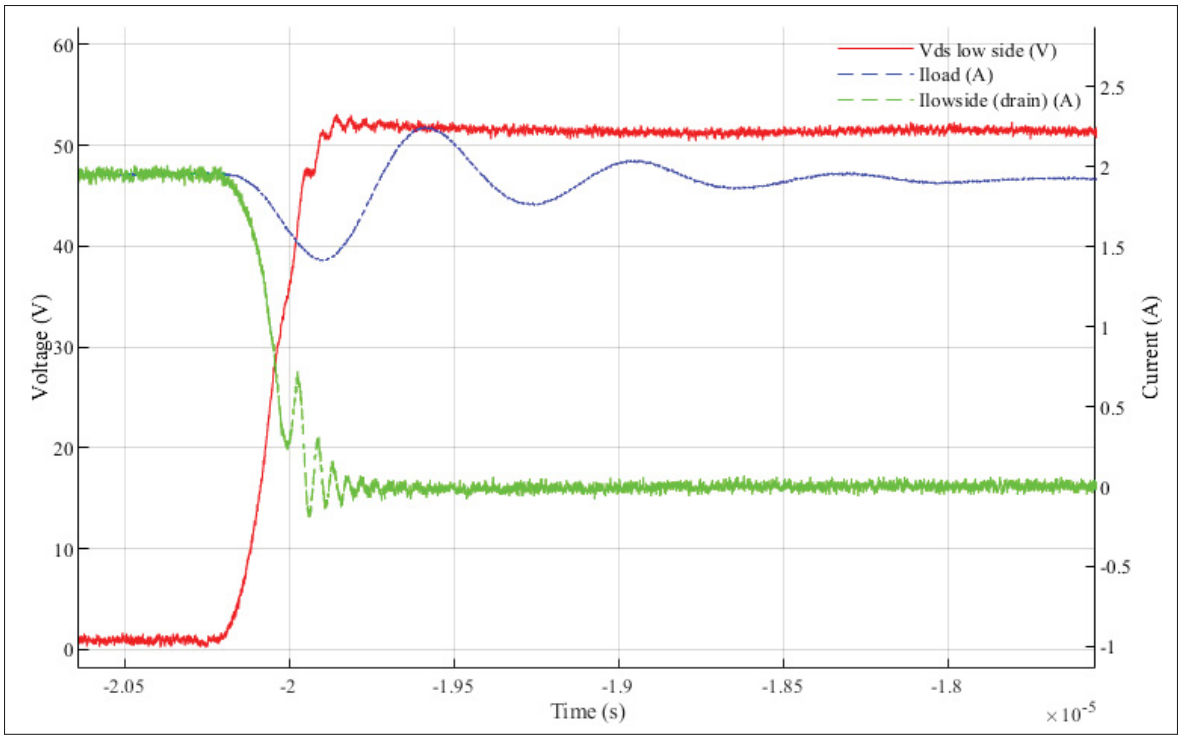

Figure 4.27 Si MOSFET: turn-off waveforms of low side switching MOSFET at 50 V with the added drain lead wire (22 Ω On & 3.3 Ω Off & DT 50 %)

be subjected to the very fast dV/dt and mutual coupling to the board under transients, making this even harder to have a reliable approximation.

Then, despite the absence of influence from the gate-source circuit on the current measurement, high perturbations are observable on both voltage and current measurements of turn-on waveform as illustrated in Fig. 4.28. Similar to turn-off waveforms, the non-linearity of the Miller capacitance subjected to voltage change with fast dV/dt results in largely perturbed current and voltage measurements of the switching MOSFET during transients. Based on observations from Figs. 4.25 to 4.28 under a configuration of low side switching MOSFET, losses computation is not viable due to major perturbations on both current and voltage measurements for both drain and source lead wire current measurements methodologies. Moreover, under a drain lead configuration, the added inductance from the current measurement wire highly

interact and resonate with the Miller capacitance during transients, making voltage waveforms imprecise and consequently unusable.

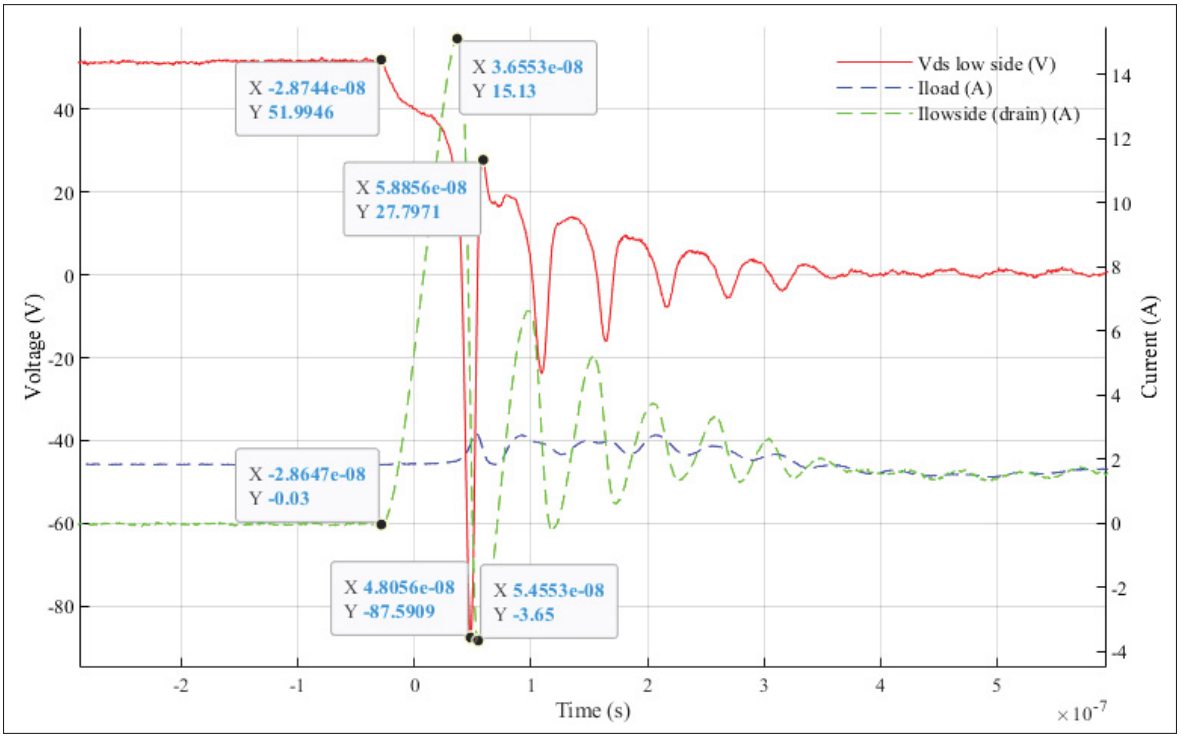

Figure 4.28 Si MOSFET: turn-on waveforms of low side switching MOSFET at 50 V with the added drain lead wire (22 Ω On & 3.3 Ω Off & DT 50 %)

Initially, the purpose of using a low side switching MOSFET configuration was to perform voltage measurements on the switching MOSFET with a pigtail passive probe. However, differential probe HVD3106 turns out to provide even more reliable voltage measurements, which is why it has been defined as the most suitable voltage probe to take further experimental measurements. Then, the best approach would be to go back to a load connected between the middle point of the transistor leg and the ground of the board as initially defined and illustrated in Fig. 4.5. In this configuration, the high side MOSFET is the switching MOSFET whilst the low side device is acting as a freewheeling diode. Since taking voltage measurements with the HVD3106 differential probe is the best approach so far, it is possible to go back to the initial switching configuration without losing measurement precision and reliability. Figures 4.29 and 4.30 respectively present turn-on and turn-off switching waveforms of the Si MOSFET in the

high side switching configuration at 50 V. The switching current is estimated from the load current and low side MOSFET drain lead current measurement.

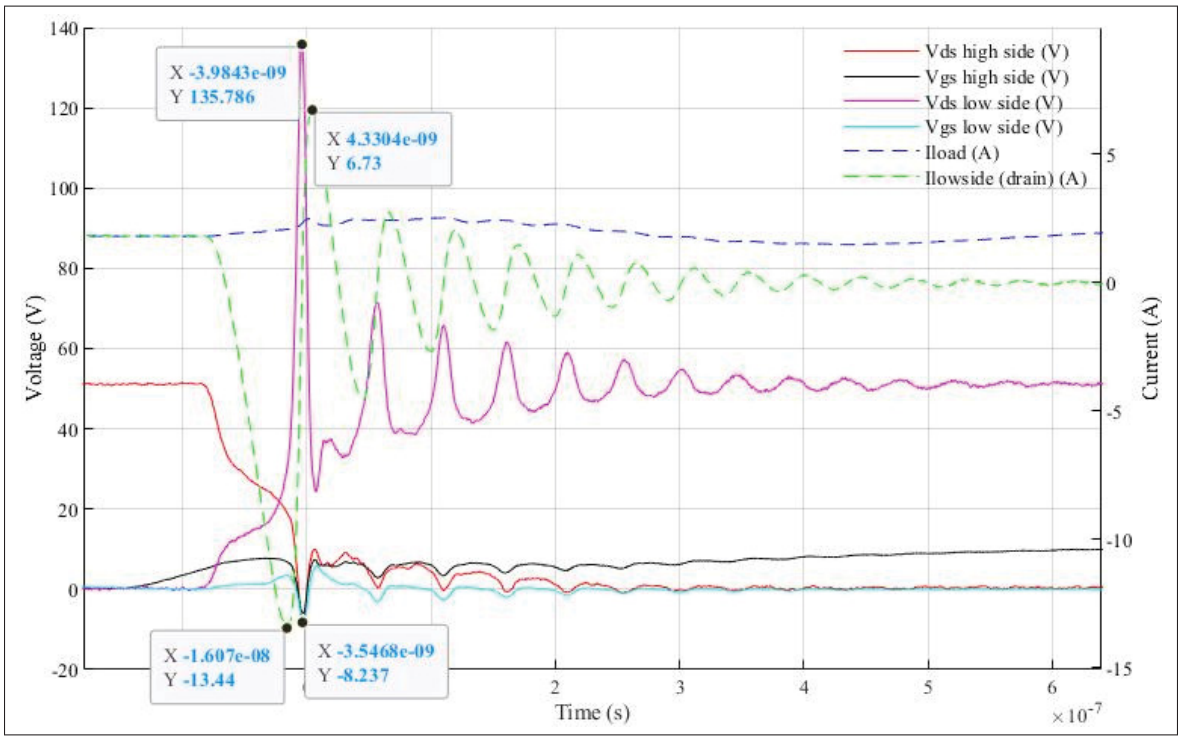

Figure 4.29 Si MOSFET: turn-on waveforms of high side switching MOSFET at 50 V with the added drain lead wire on low side MOSFET (22 Ω On & 3.3 Ω Off & DT 50 %)

Fig. 4.29 illustrates compliant turn-on waveforms suited for turn-on losses computation. Still, resonance is perceptible on voltage and current waveforms, but highly damped compared to the low side switching configuration. Under this arrangement, the added drain lead wire placed on the low side MOSFET is still impacted by the non-linearity of the low side Miller capacitance subjected to high dV/dt. Consequently, increased inductance from the low side added drain lead results in further resonance of voltage and current waveforms under acceptable limits. However, perfect time synchronization between voltage and current waveforms won't result in further computed losses since this is reactive energy. Similarly, Fig.4.30 shows slight resonance in the low side MOSFET current waveform at high side turn-off. For all changes in MOSFET's voltage, there is a change in non-linear capacitances, especially the Miller capacitance which inevitably impacts the current measurement of the drain lead. Nevertheless, the low side MOSFET drain

lead current measurement is not impacted by the gate current since they don't share a common path. In the end, the low side drain lead current extraction methodology allows to obtain suitable waveforms for losses computation under a high side switching configuration.

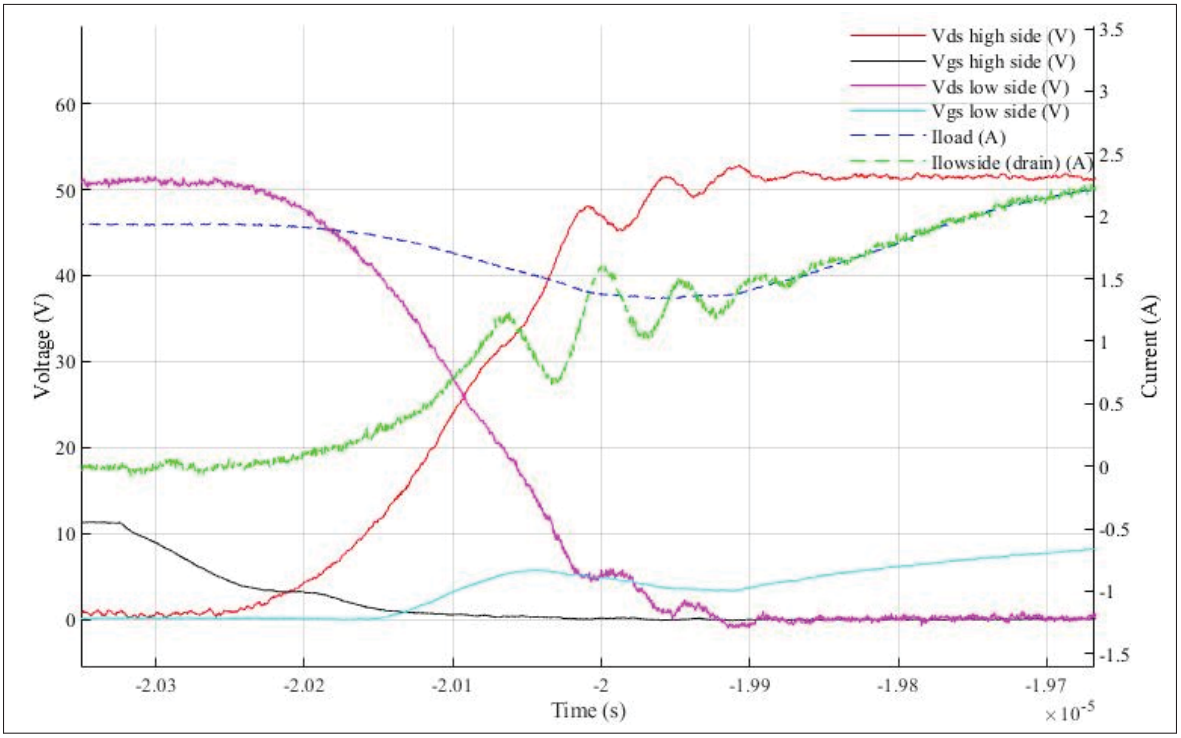

Figure 4.30 Si MOSFET: turn-off waveforms of high side switching MOSFET at 50 V with the added drain lead wire on low side MOSFET (22 Ω On & 3.3 Ω Off & DT 50 %)

Figure 4.31 illustrates the turn-on switching process under a high side switching configuration. The reverse recovery current is measured from the source lead of the low side MOSFET. At first, a small increase in the low side current measurement is noticeable in Fig. 4.31 due to a common path with the low side gate circuit. This current change is attributable to the voltage discharge of the low side MOSFET gate-source capacitance occurring right before the high side turn-on process. Consequently, this does not have any influence on the current measurement during high side turn-on, so neither on turn-on losses computation. In comparison to a low side drain lead configuration as presented in Fig. 4.29, the low side source lead methodology results in less voltage resonance and lower current measurement perturbations, which makes it an even more suited methodology for turn-on losses computations. The Miller capacitance of

the low side MOSFET normally undergoes most of the perturbation from the high dV/dt during high side turn-on. This is mostly the consequence of a lower capacitance value for C_{gd} than C_{gs} capacitance under all supply voltage. High voltage slope and change on the Miller capacitance results in a non-linear change in its value and perturbations of the current measurement when placed on the low side MOSFET's drain lead. Thus, taking the current measurement on the source lead avoids the main perturbations from the very high dV/dt on the Miller capacitance during high side transients. However, placing the measurement wire on the low side MOSFET's source lead shows increased perturbation on gate-source voltage measurement during the high side turn-on. Yet, perturbations on the low side gate circuit do not show a major decrease in performance from the accidental trigger of the low side MOSFET but inevitably make it more susceptible to such problems.

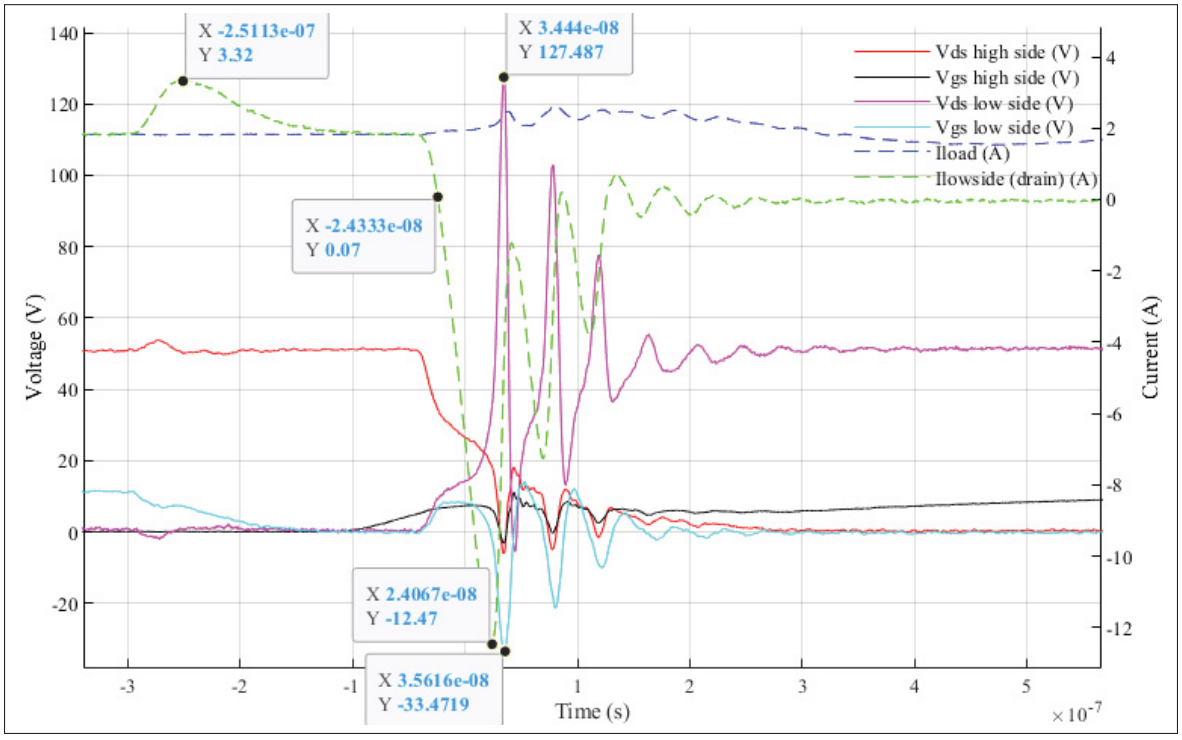

Figure 4.31 Si MOSFET: turn-on waveforms of high side switching MOSFET at 50 V with the added source lead wire on low side MOSFET (22 Ω On & 3.3 Ω Off & DT 50 %)

Figure 4.32 presents turn-off switching waveforms under a high side switching configuration with a low side MOSFET source lead current measurement. As for the low side drain current

methodology, voltage waveforms are without excessive resonance, so considered adequate to compute losses. However, after the high side turn-off follows the low side turn-on, meaning gate-source charging of the low side MOSFET's capacitance. Due to the actual position of the current lead wire on the source lead, the low side gate circuit highly impact the current measurement during turn-off with this configuration. Under the actual configuration, the drain lead current measurement methodology on the low side MOSFET offers the best compliant waveforms for turn-off losses computation, and the source lead methodology offers the best results for high side turn-on losses. However, under a MOSFET packaging solution with a kelvin connection, the low side source lead current measurement path could be independent from the gate circuit and make this methodology also suitable for turn-off measurements.

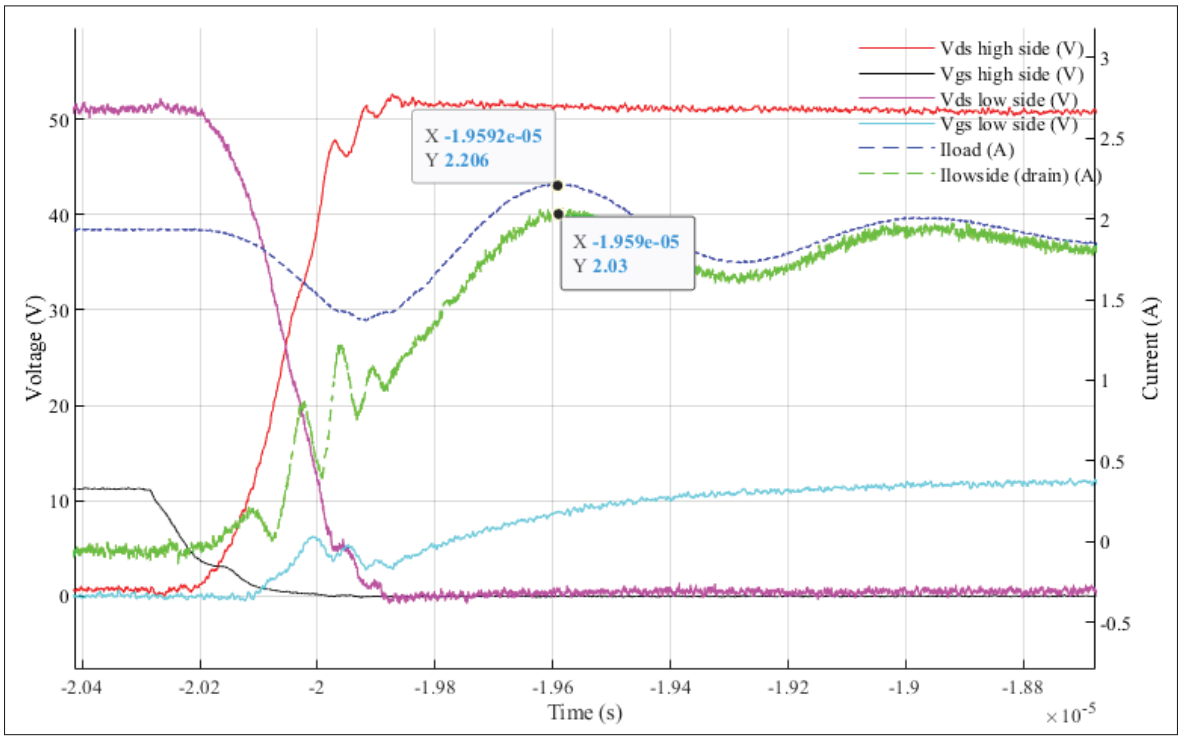

Figure 4.32 Si MOSFET: turn-off waveforms of high side switching MOSFET at 50 V with the added source lead wire on low side MOSFET (22 Ω On & 3.3 Ω Off & DT 50 %)

Therefore, the high side switching configuration provides the best experimental measurements with the lowest perturbations. Both the source and drain lead current measurement methodology on the low side MOSFET offer specific advantages. The fast voltage change across MOSFET's

non-linear capacitances always have an impact on the current measurements taken from any MOSFET's lead, but a kelvin connection could certainly further minimize the impact on the current measurement for the source lead methodology.

4.3.3.1 Losses Computation Methodology

The proposed measurement methodology will surely helps to extract experimental waveforms without inducing avoidable perturbations. However, defining the methodology to compute losses is also critical to ensure reliable experimental observations. Time synchronization between waveforms is crucial to obtain realistic losses computation with a reliable and repetitive methodology. Thus, defining properly the experimental assumptions and the computational methodology to measure losses is essential to get reliable results.

Losses are computed using voltage and current measurements while performing only one voltage measurement at a time to avoid perturbations from common measurement points. Then, high side drain-source voltage, low side MOSFET's current measurement and load current of the same occurrence are used to compute switching and conduction losses. Both the load and low side MOSFET current measurements are required to compute losses because a simple difference between those measurements allows having a proper approximation of the high side switching current. The low side MOSFET current measurement taken on either the drain or source lead is performed in a source-drain direction under a high side switching configuration. Fig. 4.33 presents a general overview of the experimental board ready for waveforms extraction.

Computing losses without adapting the waveforms to provide a good fit between voltage and current measurements will inevitably lead to inaccurate results. Thus, considering voltage and current probe rise time on extracted waveforms is essential. In addition, propagation delay should also be considered if available from the manufacturer's datasheets. Information on propagation delay is not always provided in datasheets which is why an assumption of identical propagation delay has been considered. This is not of major importance because further adjustment on waveforms are often required to observe perfect time synchronization between current and

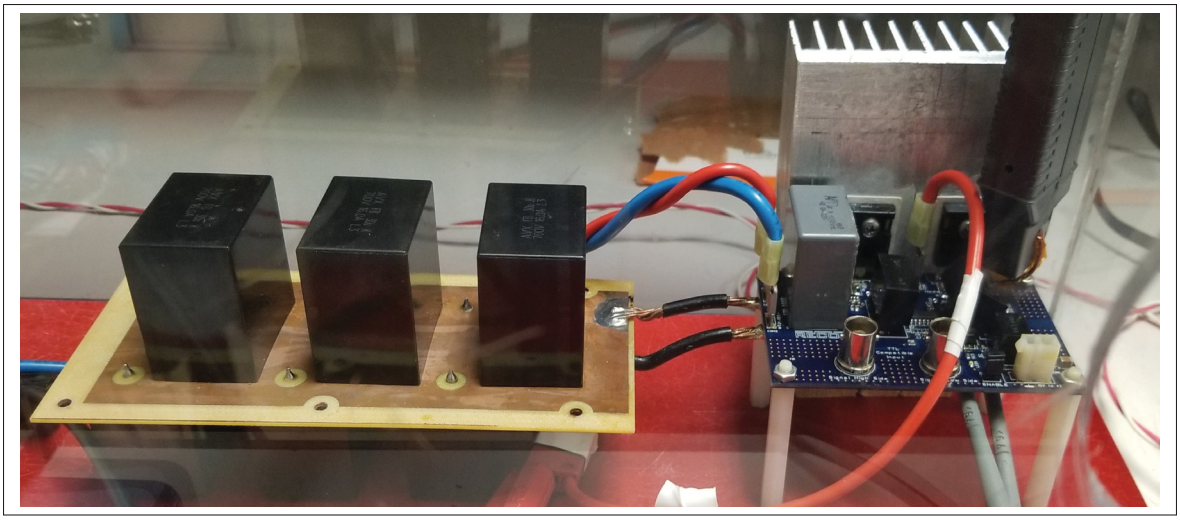

Figure 4.33 Si MOSFET: experimental board ready for measurement extraction under a high side switching MOSFET configuration with the added source lead wire on low side MOSFET

voltage. Also, the rise time provided from datasheets might not be exactly right since it is only a typical value. This further justifies the need for additional adjustments after considering typical rise and propagation delay.

A 1-GHz bandwidth from 12-bit resolution HDO6000 oscilloscope with HVD3106 differential voltage probes and CP031 current probe allow obtaining turn-on and turn-off switching waveforms with high reliability under a single measurement. Multiple measurements extraction focused on transients waveforms as only turn-on or turn-off waveforms did not show significantly different data compared to a single full cycle measurement. Consequently, a unique fine tuning adjustment is performed to observe an adequate time synchronization for all waveforms of the same analysis and cycle. The adjustment is performed identically on current measurements to obtain a perfect time synchronization between voltage and current waveforms based on assumptions of the 2^{nd} turn-on interval as presented in Fig. 2.12. This realistic switching condition implies that as the gate threshold is reached both the voltage and current waveforms of the high side MOSFET change simultaneously. To be more explicit, the start of the estimated current's slope of the high side MOSFET is delayed to match the start of the drain-source voltage slope change of the high

side MOSFET as shown in Fig. 4.34. In all experimental scenarios for all technologies under study, fine-tuning of the time delay adjustment is only between 0.1 ns to 2.3 ns.

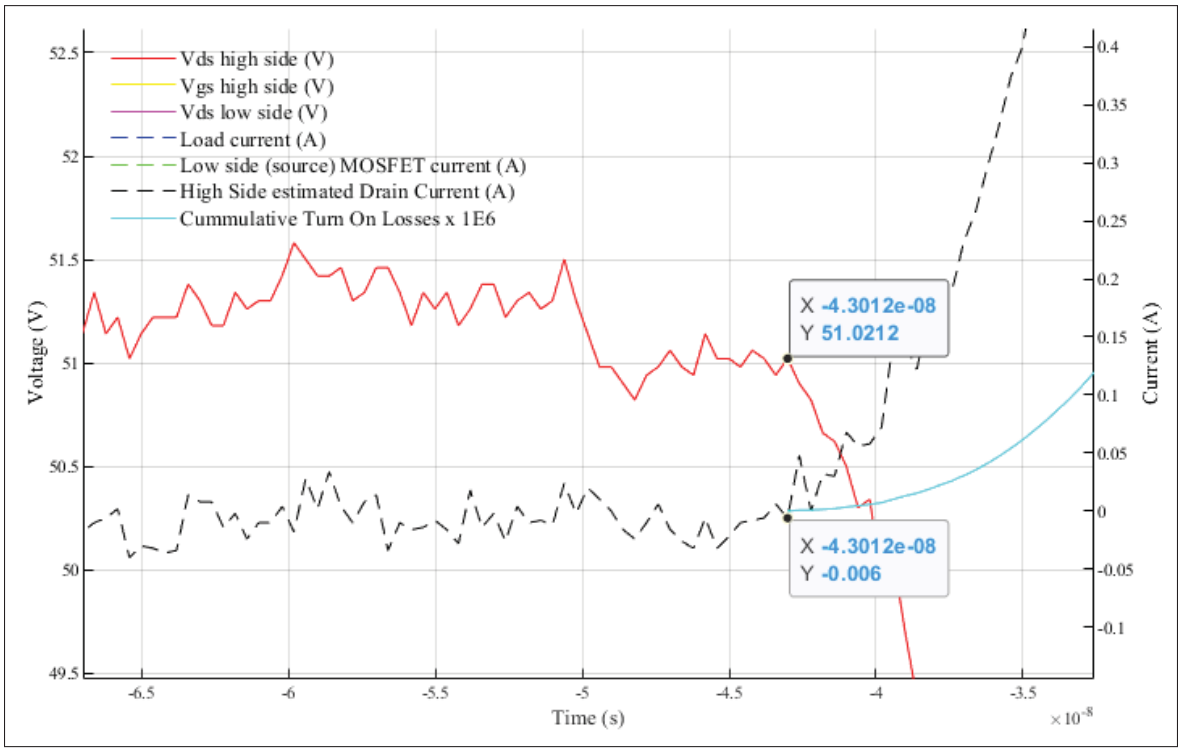

Figure 4.34 High side switching MOSFET: fine adjustment of current waveforms for turn-on losses computation

The matching point between the estimated current slope change and drain-source voltage change is also considered as the beginning of the turn-on interval to compute losses. Loss computation is performed by the integral of the product between the drain-source voltage and the estimated current of the high side MOSFET. Identical time adjustment of turn-on current waveforms is applied for turn-off losses computation. Thus, the same time synchronization defined for turn-on waveforms is kept to assess turn-off-losses from the same measurement. The beginning of the turn-off interval is defined at the beginning of the drain-source voltage slope change as illustrated in Fig. 4.35.

At last, conduction losses are computed for the last 10 μs of the conduction state of the high side MOSFET, ending 1μs before the beginning of the turn-off interval. Due to the very low value of

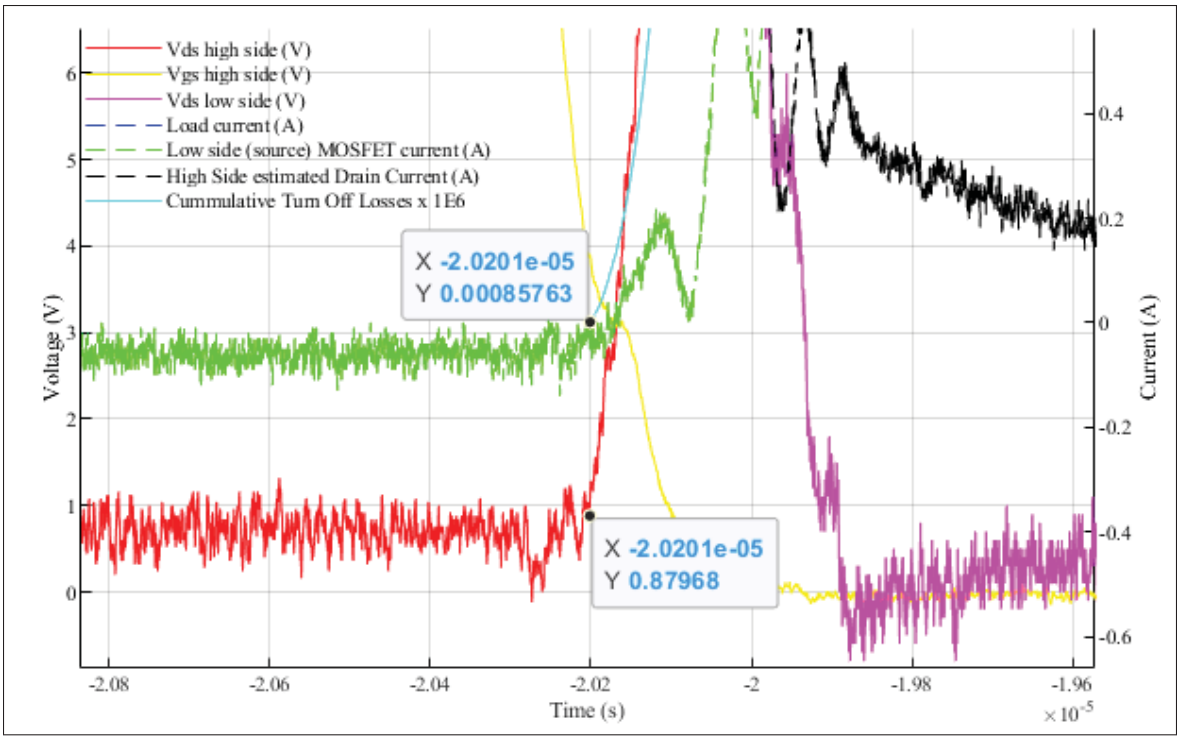

Figure 4.35 High side switching MOSFET: starting point for turn-off losses computation

the voltage measurement and lower SNR during the conduction phase, the absolute value of the drain-source voltage is used to perform losses computation to avoid possible negative voltage measurements. However, it has a very minor effect on the total computed losses.

Defining the exact moment when the turn-on or turn-off intervals ends are highly subjected to interpretation, especially under a very fast switching device resulting in high resonance of waveforms. Based on assumptions defined in Chapter 2, intervals end when the drain-source voltage, drain current and gate-source voltage reached their respective final value. However, multiple losses measurement points have been defined in Chapter 5 for a more precise interpretation of comparative switching performances between MOSFET's technologies under study.

4.3.3.2 Comparison Between the Drain and Source Lead Wire Current Measurement Technique

To have a better understanding of the advantages and drawbacks from both drain and source lead current measurement methodologies, assessing their respective impact on losses computation is essential. Figs. 4.36 and 4.37 respectively present the turn-on losses computation of the Si MOSFET under a high side switching configuration with the source and drain lead methodology. Measurement and calculation of losses are performed while respecting all mentioned considerations of Chapter 4.

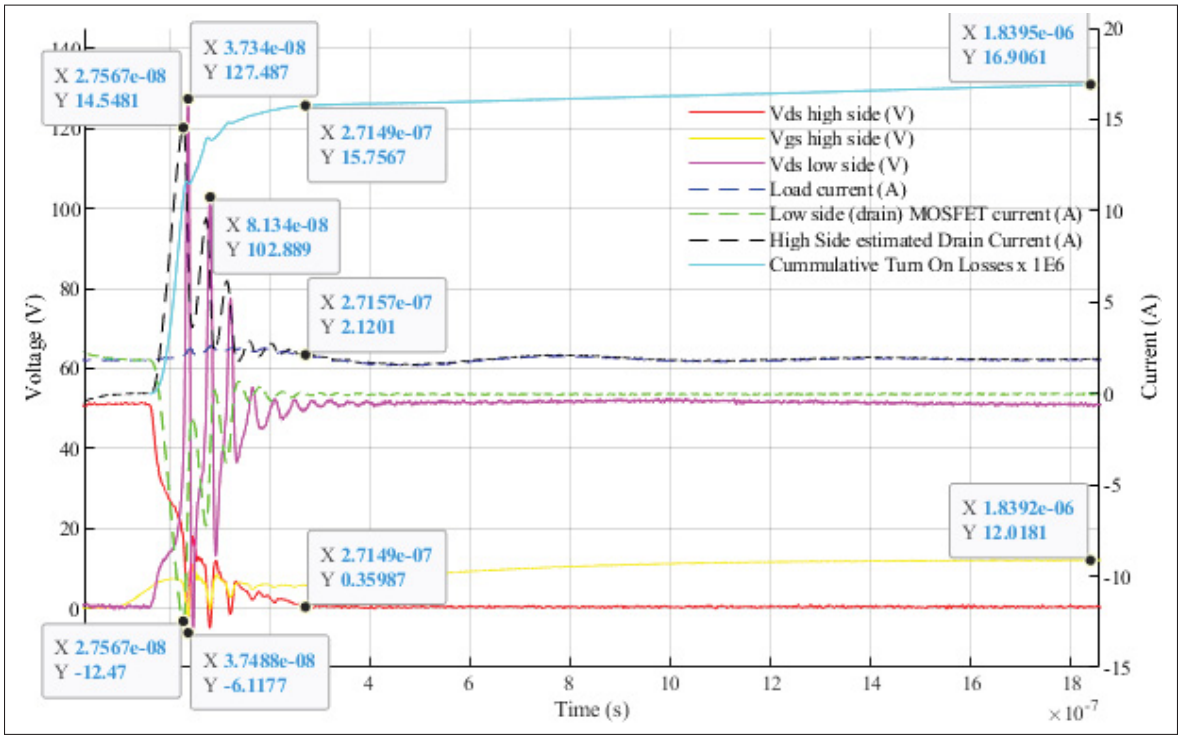

Figure 4.36 High side switching Si MOSFET: turn-on losses computation with the source lead methodology

Despite the increased resonance introduced with the use of the drain methodology, computed turn-on losses are equivalent for both scenarios. Proper time synchronization between voltage and current measurements shows that further resonance is not a part of the active power losses, but results in increased duration of the turn-on switching waveforms. This makes the source lead methodology the preferred configuration to compare turn-on switching losses. However,

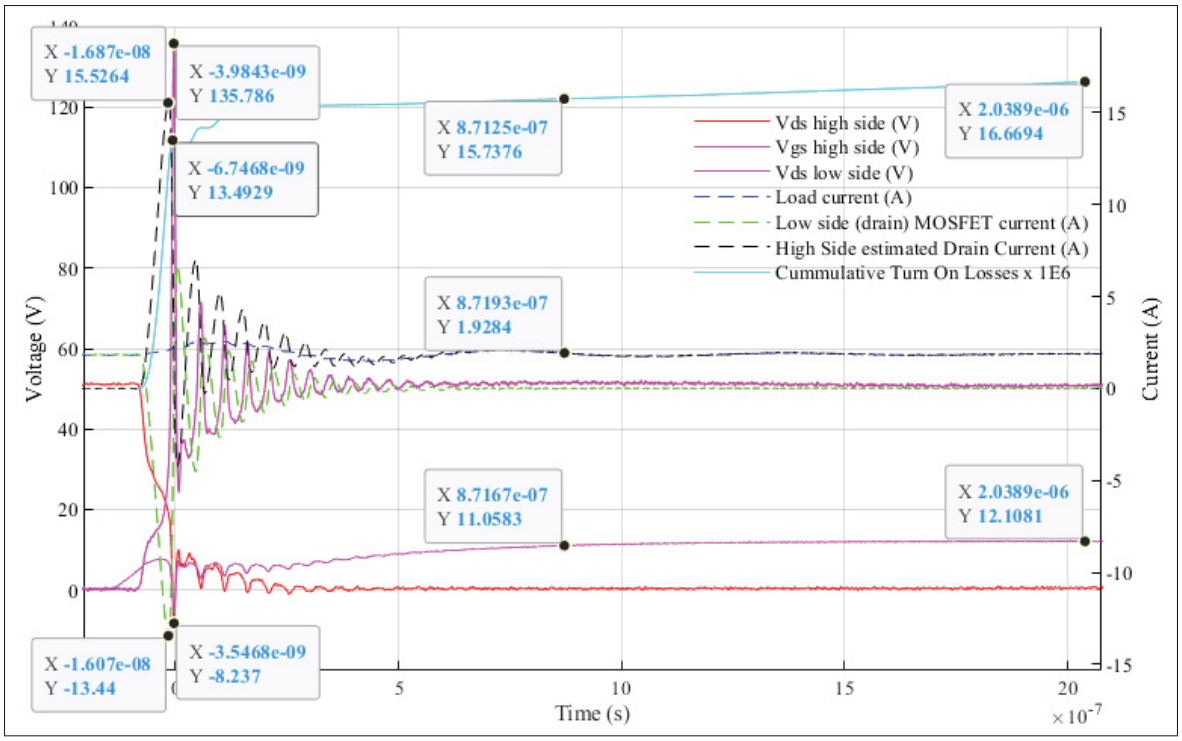

Figure 4.37 High side switching Si MOSFET: turn-on losses computation with the drain lead methodology

the drain methodology can still provide comparative results on losses computation to support calculation under the source methodology. Then, Figs. 4.38 and 4.39 respectively present turn-off losses computation of the Si MOSFET under a high side switching configuration with the source and drain lead methodologies.

Due to the actual position of the current measurement probe in the source-drain direction of the low side MOSFET, the low side MOSFET current measurement is decreased from the gate current during turn-off. Thus, this results in higher estimated high side current during the turn-off switching with the source lead methodology and results in increased losses. Then, without any doubt, the drain lead methodology offers better measurements for turn-off losses computation compared to the source methodology. Moreover, under more aggressive gate voltage and resistance as for the SiC MOSFET, the influence from the gate circuit on the turn-off losses calculation will be even worst with the source lead methodology due to unreal extra

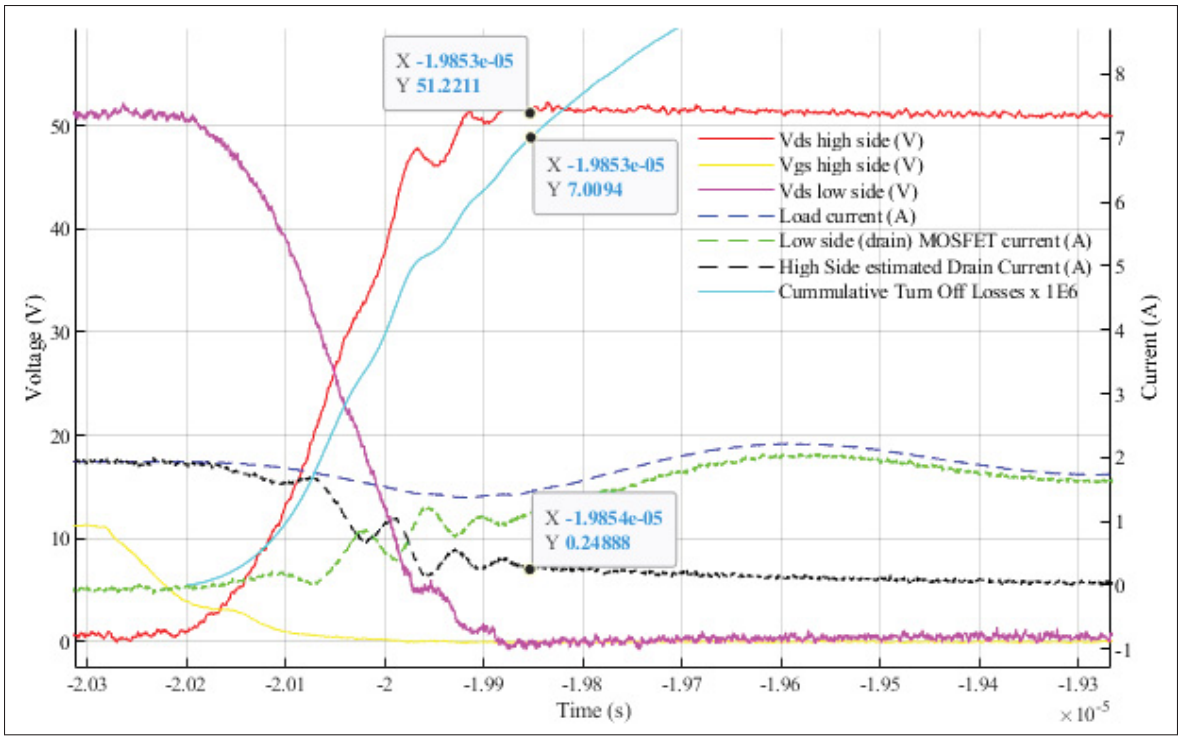

Figure 4.38 High side switching Si MOSFET: turn-off losses computation with the source lead methodology

losses. On the other hand, taking the current measurement with the drain lead inevitably causes much more oscillation on the low side drain-source voltage and extends the turn-on process to an unrealistic value. To determine the best suited current measurement technique, Table 4.3 presents an overview of the advantages and disadvantages of both the drain and source methodologies under a high side switching configuration.

In Table 4.3, a long and steady resonance on the high side drain-source voltage measurement is observable with the drain lead methodology. In contrast, the source lead methodology presents a higher subsequent amplitude of this resonance for a shorter time under the same conditions. Also, increased resonance appears on the high side gate-source voltage, but with much lower impact, and not any marked differences between methodologies.

Based on experimental observations presented in Figs. 4.36 and 4.37, the maximum reverse recovery current is increased when the drain lead methodology is used in comparison with the

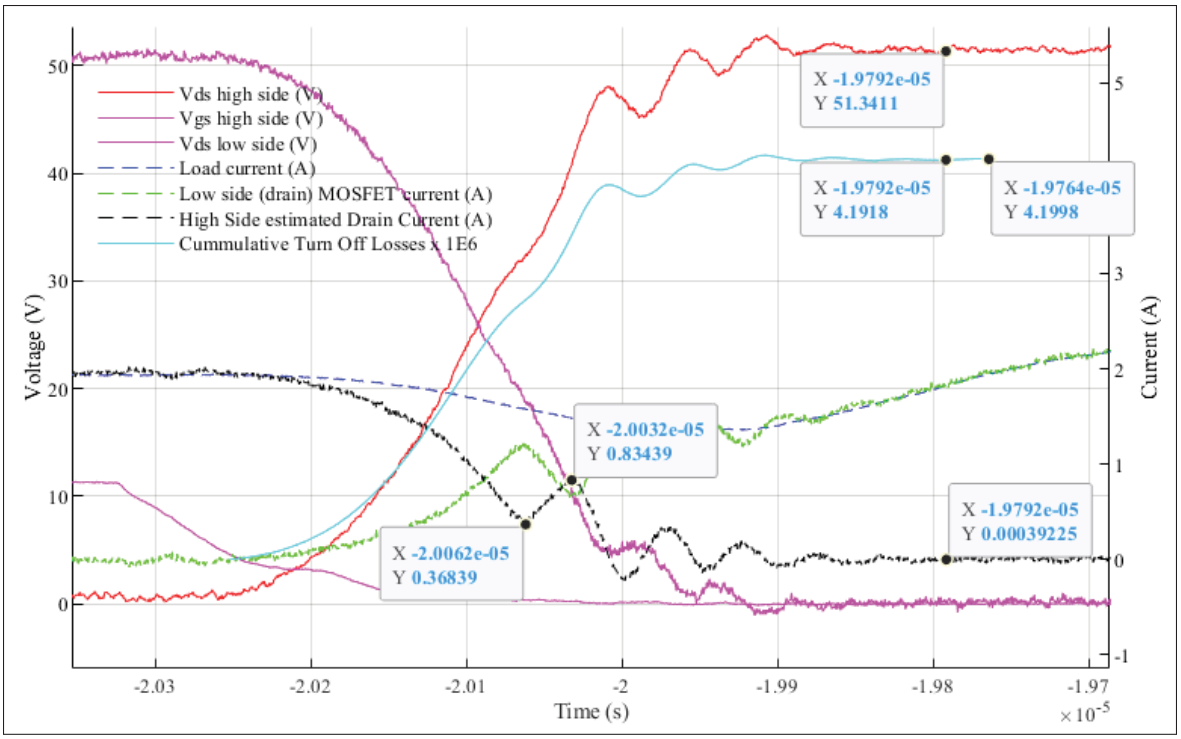

Figure 4.39 High side switching Si MOSFET: turn-off losses computation with the drain lead methodology

source lead measurement technique. Once the freewheeling diode starts blocking during the high side turn-on, a major increase in the low side drain-source voltage is occurring. This inevitably results in a voltage divider on the low side MOSFET's input capacitance. Thus, the increase of voltage across the Miller capacitance causes a decrease of its total capacitance value, resulting in a release of accumulated charges into the circuit. Inversely, the positive voltage variation on the input capacitance tends to increase the accumulated charges into the reduced Miller capacitance value. Thus, this shows that some part of the current from the high side MOSFET is going into the gate-drain capacitance when the high side MOSFET turn-on. This can potentially lead to false turn-on losses computation with the drain lead methodology during the reverse recovery phase, but total turn-on losses are similar between the source and the drain methodologies.

Then, longer resonance on all voltage measurements with the drain lead methodology is explainable with the increased inductance from the added wire and its direct interaction with

Table 4.3 Comparison between the Low Side MOSFET's Drain Lead and Source Lead Current Extraction Methodology

Sequence	Characteristics	Drain Lead Methodology	Source Lead Methodology
High Side Turn-On	V_{ds} High Side	Persistent Resonance of low amplitude	Short Resonance of moderate amplitude
	V_{gs} High Side	Persistent Resonance of low amplitude	Short Resonance of low to moderate amplitude
	V_{ds} Low Side	Higher surge voltage with persistent resonance	High subsequent surge voltage with short resonance
	V_{gs} Low Side	Low to moderate voltage perturbation of long duration	High surge voltage of short duration
	Load Current	Not any marked difference between methodologies	
	Low Side MOSFET's Current	Increased value and resonance from the Miller capacitance (C_{gd})	No observable disturbances
High Side Turn-Off	V_{ds} High Side	Not any marked difference between methodologies	
	V_{gs} High Side	Not any marked difference between methodologies	
	V_{ds} Low Side	Not any marked difference between methodologies	
	V_{gs} Low Side	No observable disturbances	High Resonance and perturbation on the gate circuit
	Load Current	Not any marked difference between methodologies	
	Low Side MOSFET's Current	Increased value and resonance from the Miller capacitance (C_{gd})	Decreased measurement from the gate circuit

the Miller capacitance. The resonance with the drain methodology can be attributed to the accumulated reactive energy resonating between the gate-drain capacitance and the total parasitic inductance. After a little while, this energy is completely dissipated in the parasitic resistance of the circuit. However, it takes much more time with the drain methodology before reaching the final turn-on voltage and current waveforms.

On the other hand, the source lead methodology increases the commonly shared inductance between the drain-source path and gate circuit of the low side MOSFET. This leads to increased perturbations of the gate-source capacitance during the reverse recovery process and puts the low side MOSFET at increased risk of parasitic turn-on as observed in Fig. 4.18. Still, this methodology offers reduced resonance during the high side turn-on with minimal perturbation on the low side current measurement. However, the gate circuit highly influences the low side

MOSFET's current measurement at turn-off and results in increased losses calculation. In contrast, the drain methodology is less likely to cause accidental turn-on, but exhibits increased resonance and increased current measurement during the turn-on process.

It has been possible to observe suited waveforms with the Si MOSFET at 100V with the drain methodology, but further increase in voltage resulted in major resonance with the drain methodology and accidental turn-on with the source methodology for multiple gate configurations. However, GaN MOSFETs exhibits suited waveforms at 100V and over. To compare all technologies with each other, and due to limitations with the chosen Si MOSFET, the maximum voltage under study is fixed at 100V. A probable cause for accidental turn-on only with the Si MOSFET is the very high reverse recovery charge of the Si MOSFET. Based on datasheets, the reverse recovery charge (Q_{rr}) of the Si MOSFET is around 1.2 μC (Infineon Technologies AG, 2012) while this is only 55 nC for the SiC MOSFET (Rohm Semiconductor, 2017) and 136 nC for the GaN MOSFET (Transphorm Inc., 2017). Since the capacitance ratio and turn-on speed are different for all MOSFETs under study, both measurement methodologies will be used to perform experimental comparisons between MOSFETs under a 50 V and 100 V supply for an external turn-on driving resistance of 10 Ω and 22 Ω.

4.4 Review of Final Experimental Comparative Methodology, Measurement Techniques and Computation Methods

Based on experimental observations, reduction in perturbations from mutual coupling, added inductance and capacitance from probes, influence from common node voltage measurements, and considerations of measurement limitations and bandwidth are essential steps in experimental studies. Whether this translates into a simple zero and degauss procedure or more complex devices' internal characteristics and board layout, small details can bring major differences on measurements and switching behavior. Carefully assessing all probing details allowed to perform voltage and current measurements with high reliability, repeatability, and resulted in perfect synchronization for losses computations.

The development of a method for extracting the switching current has proven to be a major challenge. Although measurement of the magnetic field has turned out to be interesting at first to minimize disturbances on the switching behavior. This methodology is very sensitive to the slightest disturbance in an unenclosed environment. In contrast, the lead current extraction methodology on the freewheeling MOSFET turns out as a reliable method with defined limitations, and minimal perturbations on the switching behavior. Both the source and drain methodologies offer some advantages to perform experimental measurements. However, no methods are perfect and there are always room for improvements.

To bring relevant conclusions for each technologies under study, considering the MOSFET as a whole entity brings more logical results due to large disparities in internal gate resistances between technologies. Still, to draw a complete picture of the switching behavior of Si, SiC and GaN MOSFETs, comparison under multiple gate configurations is necessary. Moreover, current extraction from both measurement methodologies can highlight further disparities in their respective switching characteristics.

CHAPTER 5

EXPERIMENTS AND INTERPRETATION OF RESULTS

This chapter presents all established measurement points along with experimental illustrations. Interdependency of established measurement points with internal characteristics and switching behavior of MOSFETs provides a guideline to interpreting experimental results. Then, statistical analysis of relative comparison between MOSFET's technologies highlights the major trend in the switching process for Si, SiC and GaN MOSFETs under study.

In the previous chapters, switching waveforms have been assessed on all technologies under study for four distinct configurations in a hard commutation half-bridge board. Experimental configurations consist of a turn-on gate resistance of 22 Ω and 10 Ω for both high and low sides under a voltage supply of 50 V and 100V. For all experiments, measurement techniques, computation methods, and waveforms adjustments as defined in Chapter 4 are applied to minimize perturbations of measurements, optimize losses computation accuracy and define the beginning and end of the switching intervals. Results have shown very different behaviors for each of the technologies which led to multiple adaptations of the established measurement points in order to compare the MOSFETs under study with a "tooth for tooth" approach. This comparison approach define the MOSFET as a complete entity including all its parasitic components, meaning that only the driving voltage is allowed to change between comparisons to accommodate specific requirements from technologies. Even if the same board and configurations are used to compare MOSFET's experimental results, major differences regarding the general switching waveforms can be observed due to high disparities of intrinsic characteristics between Si, SiC and GaN MOSFETs. Consequently, it is necessary to examine every result obtained based on well-defined measurement points to show potential specific differences in the switching behavior. The following section (5.1) presents a general overview and definition of the measurement points established to compare MOSFET's switching performances.

5.1 Measurements to Compare MOSFET's Switching Performances

Since the interest is to highlight the major differences regarding the switching process between MOSFET's technologies under study, most of the measurement points are focused to show specific information about the switching performance rather than steady-state conditions (i.e. conduction mode). GaN switching waveforms at a voltage supply of 100V with a turn-on gate resistance of 10Ω is used as the reference model to give visual representations of established measurement points. This specific experimental configuration exhibits important resonances and the fastest current rates justifying the requirement of multiple measurement points. The necessity to have multiple turn-on measurement is mainly required to isolate the impact of the resonance on the computation of turn-on switching losses. The following list presents a general overview of all established measurement points to compare the switching performance of MOSFETs.

- Turn-on losses and duration (1^{st} peak);
- Turn-on losses and duration (Slope Stabilized);
- Turn-on losses and duration (v_{gs} Final & Slope Stabilized);
- Maximum positive and negative High Side Estimated Current (HS-EC) slope (dI_F/dt) & (dI_R/dt), respectively;
- Maximum HS-EC value;
- Maximum positive and negative Low Side Drain-Source Voltage (LS-Vds) slope (dv_{ds}/dt);
- Maximum LS-Vds value;
- LS-Vds resonant frequency (ω);
- Turn-off losses and duration;
- Maximum Turn-Off HS-EC slope (dI/dt);
- Conduction losses (10μs).

5.1.1 Turn-On Losses and Duration

As shown in 5.1, three turn-on losses and duration measurement points were established. The first one named "Turn-on losses and duration (1^{st} peak)" mainly indicates the switching

losses accumulated during the reverse recovery process of the low side MOSFET. The high side estimated current reaches its maximum value while the high side drain-source voltage is decreasing quickly which results in the period with the fastest increase in switching losses. For slow switching configurations with low resonance, this measurement point is very close to the actual total turn-on switching losses. However, transient voltage waveforms often show lots of resonance leading to extended turn-on duration and long-term turn-on losses, especially with the drain lead current measurement methodology. The resonance itself does not necessarily add up extra losses because the time delay between current and voltage measurements has been carefully adjusted. However, it tends to influence the capacitance charges such as the gate-source charge. Then, it leads to extra time before the MOSFET gets to a steady conduction state, so indirect extra losses are accounted as part of the turn-on losses. This phenomenon is characterized by a fast increase in switching losses followed by a slow decrease in losses over time as the MOSFET gets closer to the full conduction state.

Fig. 5.1 illustrates a close view of the beginning of GaN's turn-on interval at 100V using the drain methodology with a 10Ω turn-on resistance. Datapoints of the beginning of the interval and first turn-on losses measurement point are highlighted. In addition, Fig. 5.2 provides a complete overview of GaN's turn-on switching waveforms including highlighted measurement points.

As shown in Figs. 5.1 and 5.2, measurement points are identified from left to right as follow: the starting point of the turn-on interval, the first turn-on losses measurement point (known as the first peak). Then, only in Fig. 5.2, the second measurement point is followed by the third measurement point representing the second turn-on losses when the slope in computed cumulative losses is stabilized, named "Turn-on losses (Slope Stabilized)". Finally when both the gate-source voltage (v_{gs}) and the slope in cumulative losses seems to be stabilized, the final turn-on losses measurement point is reached, named "Turn-on losses (v_{gs} Final & Slope Stabilized)".

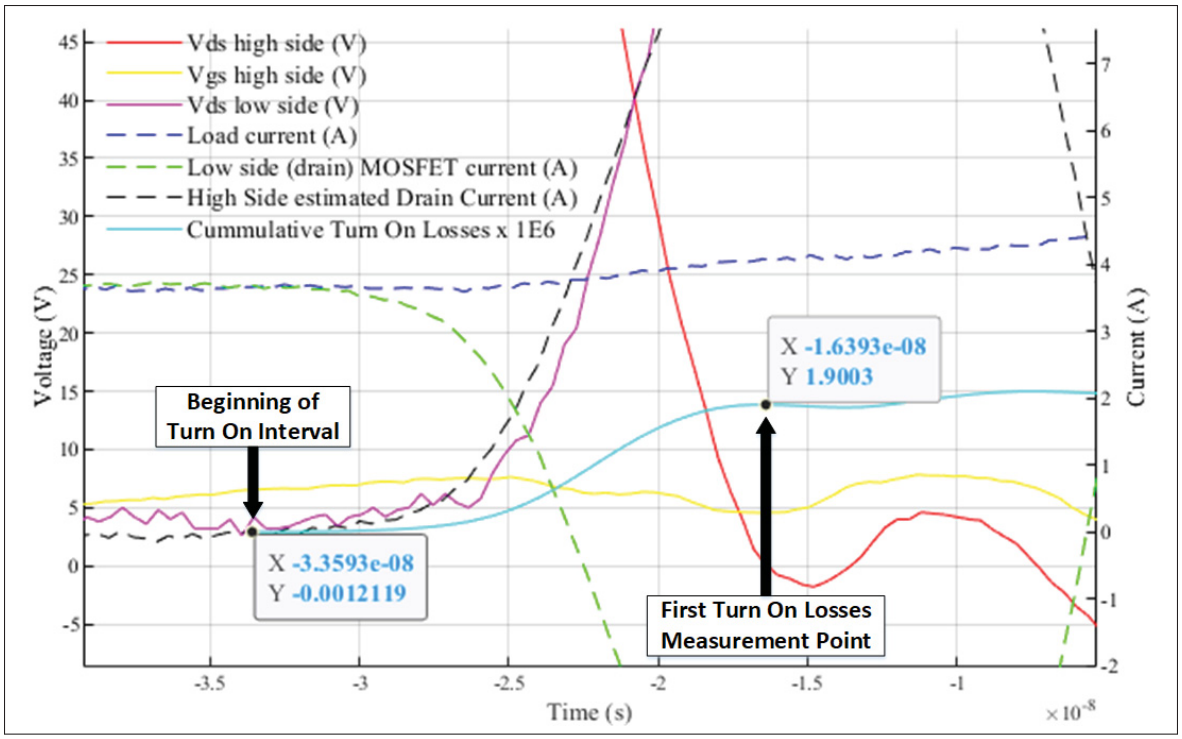

Figure 5.1 Close view of high side GaN turn-on switching waveforms and losses at 100 V with low side drain lead (both high and low side R_{on} = 10 Ω & R_{off} = 3.3 Ω)

At first, the increase in losses is mainly due to the transient in the turn-on process which is assessed from the first turn-on measurement point (the first peak).

Then, the second part is highly dependent on the resonance between the capacitances and inductances of the board, like the Miller capacitance and the parasitic inductances. In experimental observation with high resonance, the slope in cumulative losses reach the steady condition of the conduction state before the resonance ends. Occurring between the second and the last turn-on measurement point, this indicates that the MOSFET have reached its nominal voltage and current. Then, the second turn-on losses measurement point is defined as the moment where the positive slope of cumulative losses is steady as if the full conduction state has been reached. Finally, the last turn-on measurement point is defined as the moment when the slope in cumulative losses is steady in addition to a gate-source voltage stable around its final value.

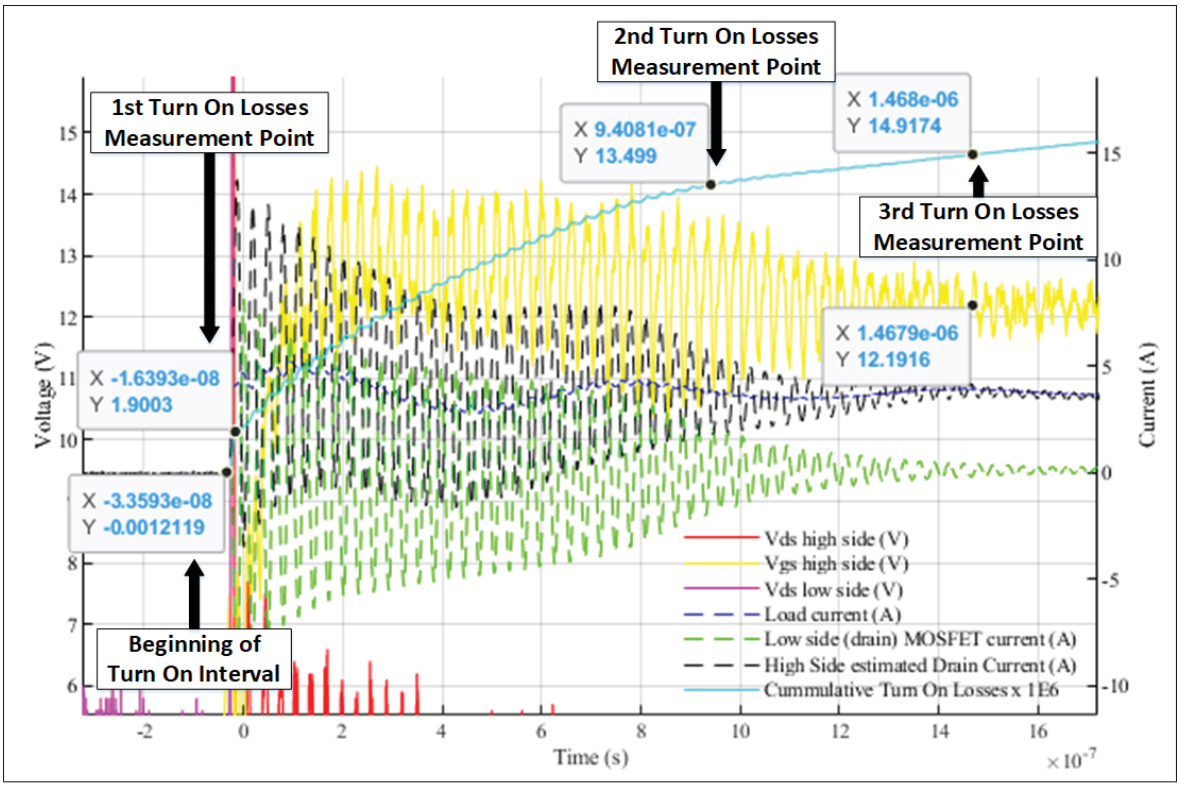

Figure 5.2 General view of high side GaN turn-on switching waveforms and losses at 100 V with low side drain lead (both high and low side R_{on} = 10 Ω & R_{off} = 3.3 Ω)

Moreover, Fig. 5.2 shows that even with a very careful adjustment of the delay between current and voltage measurements, a decrease in the slope of cumulative turn-on losses is still noticeable during the resonant period between the first and second turn-on measurement point. As the resonance tends to decrease over time, the decrease in the resonance on the gate-source voltage eventually leads to a stabilized slope in cumulative losses over time. At a certain point, the slope of cumulative losses is stable around what is observed in the conduction phase even if the resonance is still important, showing that the MOSFET already reached full conduction. This moment might be associated with the real value of the turn-on switching losses, including the resonance, characterized as the second turn-on losses measurement point. This measurement point gets all its importance in the process of comparing experimental results with very low resonance to very high resonance. For experimental results showing low resonance, this second measurement point is very close to the third turn-on losses measurement point since the slope

in cumulative losses tends to stabilize quickly after the gate-source voltage reaches its final value. As shown in Fig. 5.3, a close view of SiC's turn-on waveforms at 100V using the drain methodology with a 10Ω turn-on resistance illustrates an example of a fast switching process with low resonance.

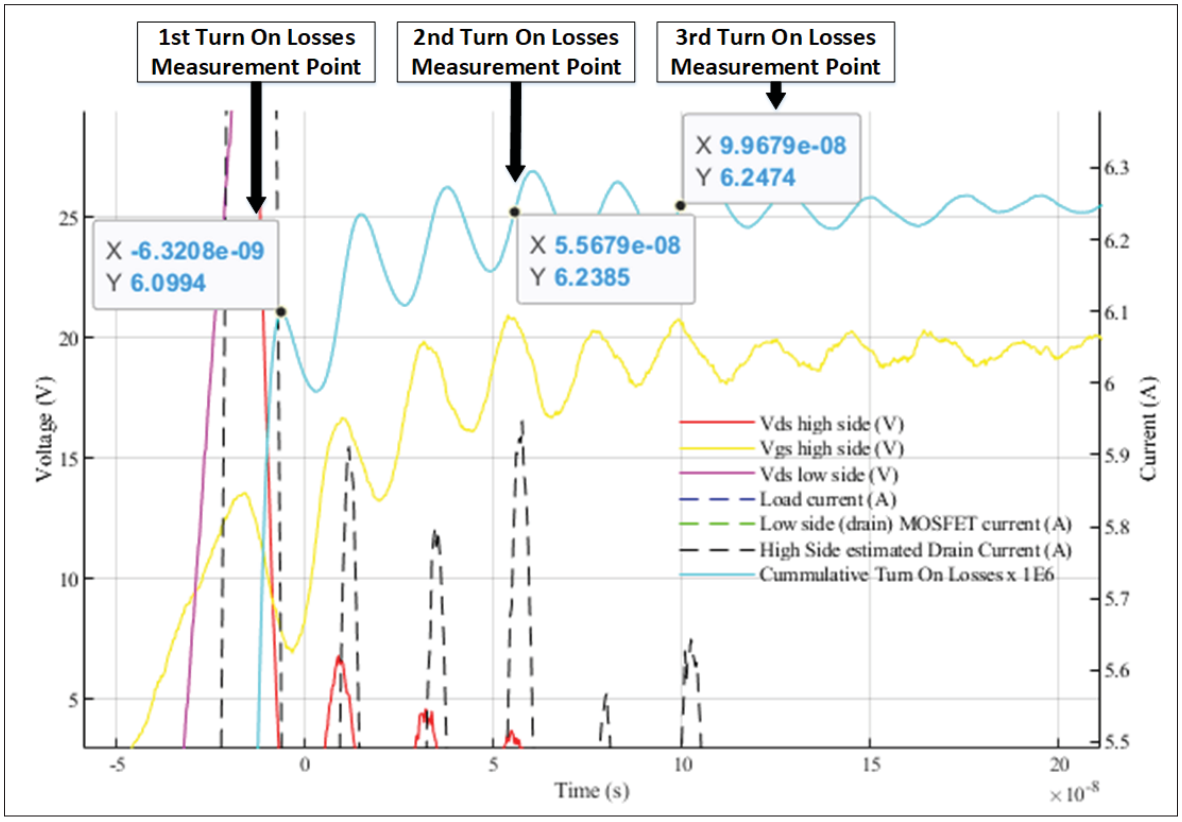

Figure 5.3 Close view of high side SiC turn-on switching waveforms and losses at 100V with low side drain lead (both high and low side R_{on} = 10Ω & R_{off} = 3.3Ω)

However, as mentioned previously, using the drain methodology introduces extra parasitic inductance resonating with the internal parasitic capacitances and inductances of the switching loop during the reverse recovery process of the low side MOSFET. Depending on device switching speed and reverse recovery current slope, the drain methodology might have a mild or very severe effect on the surge voltage and resonance during the turn-on switching process. Then, it is preferable to consider the source methodology instead of the drain methodology to assess and compare turn-on losses. Discussion on experimental results will take into account the

stiffness of the reverse recovery process and the impact of the selected measurement techniques on observations.

5.1.2 High Side Estimated Current (HS-EC) and Reverse Recovery Process

To compute the losses of a switching device, a measurement of the actual current going through the high side switching MOSFET in the half-bridge configuration is required. The near magnetic field was initially explored to take an isolated measurement of the low side MOSFET's current by using the geometry of the PCB layout. However, obtaining a reliable current measurement with repeatability from the integral of the magnetic field was not possible under the experimental conditions and methodology, as discussed previously.

Then, another approach has been used to extract the low side MOSFET's current directly from a Hall effect current measurement probe, referenced as the lead wire methodology in section 4.2.3. The probe is placed either on the drain lead or source lead of the low side MOSFET, as presented in Chapter 4 and illustrated in Fig. 4.9. This current measurement technique has been defined as the selected current measurement technique to extract experimental data. With this solution, highly reliable current measurements were obtained from the low side MOSFET without too much influence on the switching process, allowing to compute the high side MOSFET's estimated current (HS-EC) from the difference between the load current and the low side MOSFET's current.

The first measurement point of the HS-EC is the maximum positive slope (dI_f/dt) occurring during the reverse recovery process of the low side MOSFET's parasitic internal diode. This first measurement point is highly dependent on the external circuit conditions such as the supply voltage and the turn-on speed of the high side MOSFET under a specific gate configuration (Toshiba, 2018). Then, the potential maximum switching speed of the device while considering both the internal and external gate resistance can be assessed with this criterion. This measurement is taken when the body diode of the low side MOSFET is kept in a conduction state due to thermodynamic balance until all the carriers are swept out of the n^- drift layer, commonly known

as the reverse recovery process (Toshiba, 2018). A sharper current slope will lead to a faster recovery process, but an increased maximum reverse recovery current (I_{rrm}) (Toshiba, 2018). However, this is highly dependent on the amount of charge to recover in the body diode, known as the reverse recovery charge (Q_{rr}).

The intrinsic diode known as the parasitic diode is a critical parameter for the MOSFET. A complete analysis of the body diode parameters is required to have a good understanding of how the recovery process characteristics (softness, speed) will influence the efficiency of a hard commutation switching topology (Khersonsky, Robinson & Gutierrez, 1992; Huang, 2014). Properly choosing the MOSFET considering its intrinsic diode is an advantage because it provides the freewheeling capability at no extra component cost and might even eliminate the need for external snubber circuits by reducing voltage spikes, RFI and, EMI from bad designs with snappy diodes (Khersonsky *et al.*, 1992; Huang, 2014).

To properly understand how to interpret the current slope during the reverse recovery process of the low side MOSFET, it is important to understand well the reverse recovery process itself and the principle of charge restoration during this process. PN junction diodes store charges as excess minority carriers in the conduction phase. Since PN diodes work under conductivity modulation principles, this results in lower forward voltage (V_F) and lower conduction losses (Khersonsky *et al.*, 1992; Huang, 2014). The longer the diode stays in conduction, the more it accumulates charges (Q_o). This process continues until it quickly reaches saturation. However, the accumulation process strongly depends on the current value and slope in the conduction state (Khersonsky *et al.*, 1992; Huang, 2014). When the current switch from the conduction to the blocking state, partial charges are quickly neutralized from internal recombination, and the remaining reverse recovery charges (Q_{rr}) are reduced by recombination via the reverse current going through the diode (Khersonsky *et al.*, 1992). Figure 5.4 presents a general overview of the reverse recovery process of MOSFET's parasitic PN junction diode divided into four subsequent intervals. Since MOSFET's voltage is normally referenced as the drain-source voltage (v_{ds}), this nomenclature is kept for the analysis of the MOSFET's parasitic internal diode during the reverse recovery process of the low side MOSFET under the experimental application.

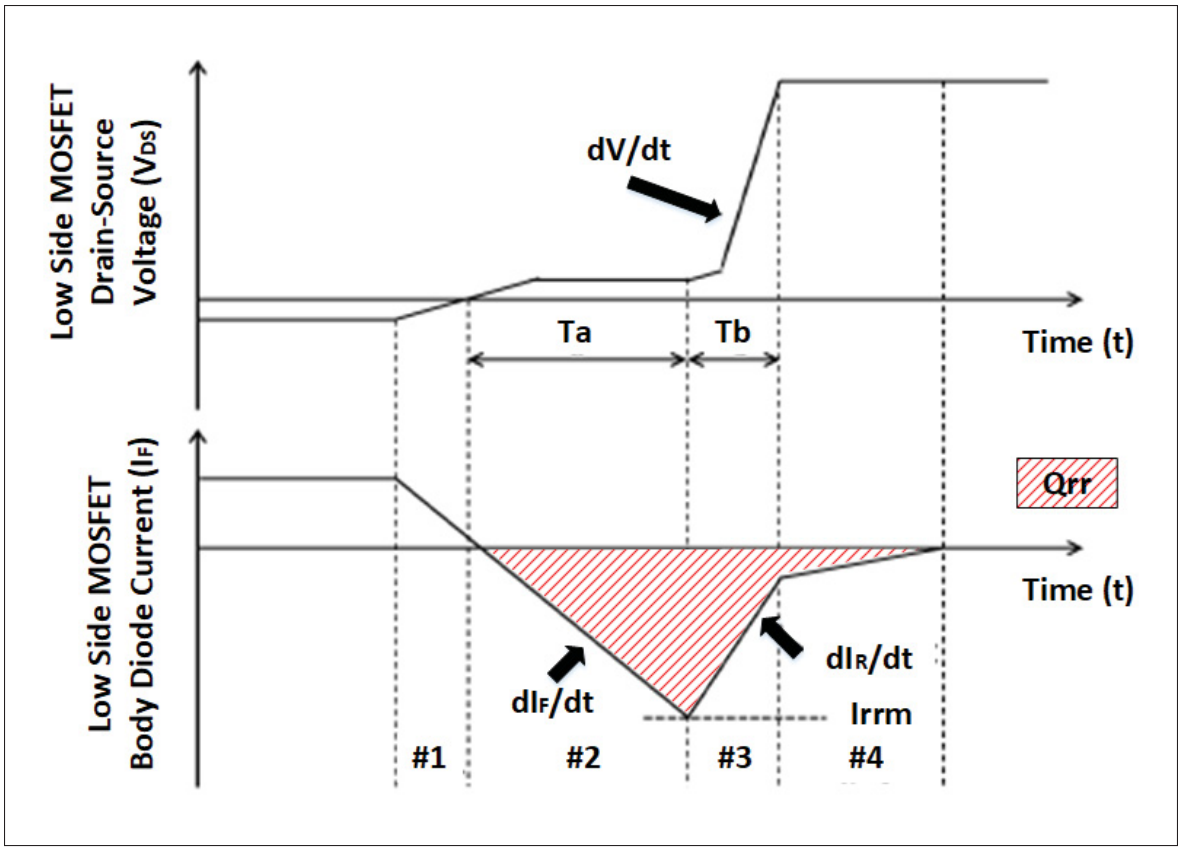

Figure 5.4 Overview of MOSFET reverse recovery process divided into four sub-intervals Adapted from Toshiba (2018)

1. At first, the load current is in a freewheeling phase with the internal body diode of the low side MOSFET, keeping the body diode in the forward conduction mode. As the high side MOSFET turn-on, the current go through the low side MOSFET's body diode. At this point, the body diode switches to the reverse-biased state as the drain-source voltage (v_{ds}) of the low side MOSFET slightly increases, and its current start decreasing sharply with a slope of (di_F/dt) determined by external conditions such as the applied voltage, the commutation loop inductance and the turn-on speed of the switching device without any influence of the diode characteristics. Injection of minority carriers is still in process in the parasitic diode until its current reaches zero (Toshiba, 2018).
2. As the current crosses zero and starts increasing in the reverse direction of the body diode, the recombination process starts as holes and electrons are moved back to the source and drain

electrode respectively. A sharper current slope will inevitably cause a faster recombination process and an increased peak reverse recovery current. Until the recombination process is not completed, the low side MOSFET's body diode is kept in a thermodynamic imbalance, providing a low impedance path and keeping the drain-source voltage of the low side MOSFET low (Toshiba, 2018).

3. When the internal body diode reaches thermodynamic equilibrium along the PN junction, meaning that almost all carriers are swept out, the low side MOSFET's body diode starts blocking by exhibiting a high impedance path, sustaining gradually the drain-source voltage (Toshiba, 2018). This results in a fast decrease of the reverse recovery current with a slope equivalent to (di_R/dt) which induces a high voltage slope in an inverse proportion to the depletion layer's capacitance (C_{ds}) (Toshiba, 2018).
4. Finally, according to (Toshiba, 2018), even after almost all the carriers are swept out and that the drain-source voltage has increased, a small current might still go through the low side MOSFET to move back the remaining carriers, but this is not always observable.

Considered as the main carriers recombination phase, the 2nd interval of the reverse recovery process presented in Fig. 5.4 starts when the current crosses zero and ends when the reverse recovery current reaches its maximum value I_{rrm}. Then, the 3rd interval can be considered as the blocking phase of the body diode, starting from thermodynamic equilibrium at I_{rrm} and ending with a very high impedance path when the low side MOSFET drain-source voltage reached the supply voltage. The duration of both 2nd and 3rd intervals are important parameters to assess the stiffness of the reverse recovery process, respectively referenced as (T_a) and (T_b) in Fig 5.4. A large ratio of (T_b/T_a) is an indication of a soft reverse recovery process with a slow (di_R/dt), resulting in a low (dv_{ds}/dt) and low recovery noise when the diode starts blocking. However, the reverse recovery current slope during the recombination phase (di_F/dt) has a considerable impact on the maximum reverse recovery current reached (I_{rrm}) and the softness ratio (T_b/T_a). Then, the reverse recovery charge (Q_{rr}) is defined as the integration of the time-current curve during the recombination phase (Toshiba, 2018; Khersonsky *et al.*, 1992), which represents the

dissipated energy in the power switching side during the reverse recovery process (Khersonsky *et al.*, 1992).

The final lead methodology presented in Chapter 4 provides a direct current measurement of the low side MOSFET. From the reverse recovery current and the load current, estimation of the high side MOSFET's current is possible with a simple substraction. During the reverse recovery phase of the low side MOSFET, the change in the load current is very negligible in comparison to the change in the low side MOSFET's current. This is due to the presence of a very high inductive and resistive path of the load in comparison to the low side MOSFET during the recombination phase. Consequently, the absolute value of the high side estimated current is slightly higher than the recombination current of the low side MOSFET during the reverse recovery process. Since the current measurement from the lead methodology is taken in the forward direction of the low side MOSFET's body diode, the estimated high side current is of opposite polarity. Then, the high side estimated current positive slope can be referenced as the inverse of the recombination current of the low side MOSFET (dI_F/dt) as presented in Fig. 5.4, in addition to the slight change in the load current during the reverse recovery process. This first established current measurement of the high side positive estimated current slope provides relevant information on the high side MOSFET's switching speed under a specific gate configuration.

Then, the second current measurement taken into account in the experimental analysis is the maximum negative slope (dI/dt) of the HS-EC after the maximum current has been reached. Since the change in the load current is very low during the reverse conduction of the low side MOSFET's body diode, the estimated current is close to the parasitic diode's current during the reverse recovery process. Then, the second current measurement of the maximum negative slope of the high side estimated current is mainly the inverse of the equivalent (di_R/dt) of the low side MOSFET's body diode during the blocking phase as presented in Fig. 5.4. This second measurement provides an idea of the ruggedness of the body diode, but this is highly dependent on the total charges to recover and the switching speed of the high side device during the first two intervals of the reverse recovery process (Toshiba, 2018).

Then, the last current measurement is defined as the maximum current value of the high side MOSFET's estimated current. This measurement is the maximum shoot through current of the high side MOSFET during the reverse recovery process, responsible for a high increase in turn-on losses. This current value is very close to the maximum reverse recovery current (I_{rrm}) of the low side MOSFET's body diode during the second interval of the reverse recovery process. Fig. 5.5 presents a close view of HS-EC measurements for the GaN MOSFET at 100V. Maximum current slope measurements are taken between 20% and 80% of total variations under an approximated steady current slope as shown in Fig. 5.5. The absolute difference in current slope measurements between the HS-EC and low side MOSFET current measurement is less than 5% referenced on the HS-EC slope measurements.

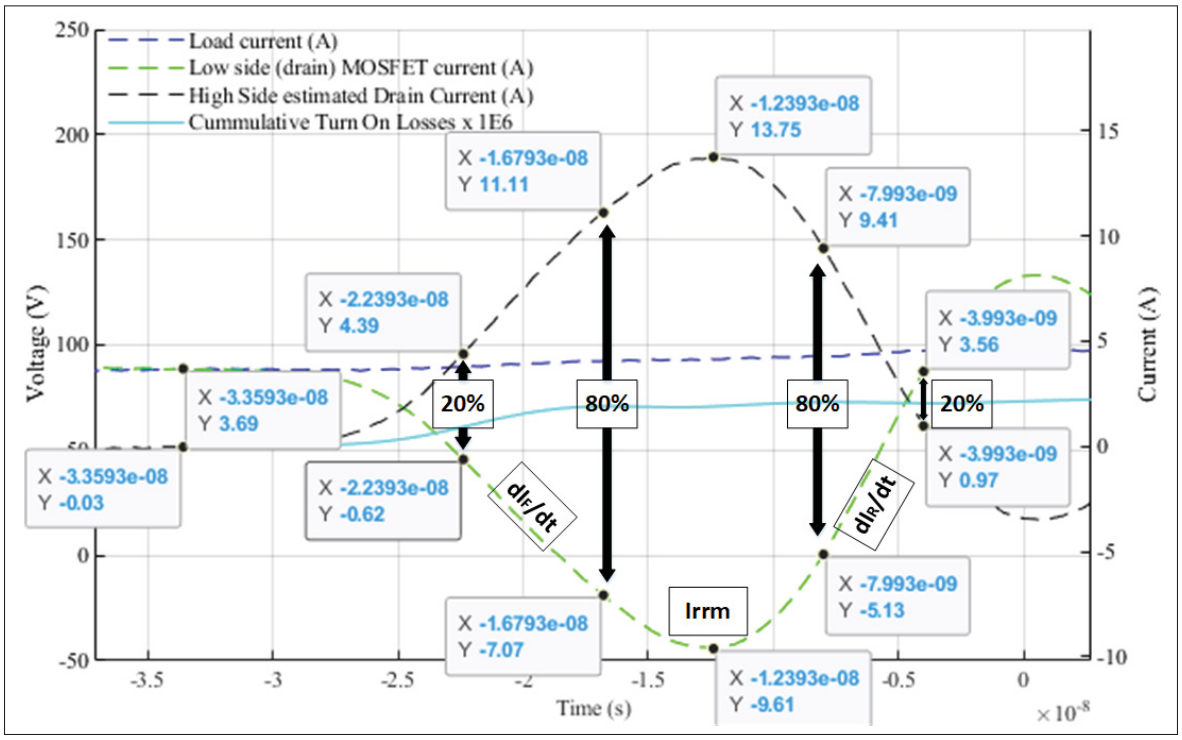

Figure 5.5 Close view of high side GaN turn-on switching waveforms: HS-EC maximum value (I_{rrm}), positive (dI_F/dt) and negative maximum slope ($-dI_R/dt$) at 100V with low side drain lead (both high and low side R_{on} = 10Ω & R_{off} = 3.3Ω)

For experiments under study, MOSFET's switching losses in a hard switching topology are the data of interest. This is the reason why the established measurement points mainly focus

to provide information on the high side MOSFET losses rather than on the low side MOSFET parasitic diode's losses and behavior even if they indirectly affect the switching losses. When the reverse recovery current reaches its maximum value (I_{rrm}) and the diode starts to exhibit a high impedance path, the decreasing current slope (di_R/dt) is dependent on the diode's total reverse recovery charge which inevitably affects the switching losses of the high side device. Moreover, if the change in the diode's current is too aggressive and the amount of recovery charges is high, this will cause a high voltage surge that could result in perturbations on gate circuits, EMI issues, accelerated device's degradation, potentially bring the low side device into avalanche (Huang, 2014), and requiring the addition of a snubber circuit. In another word, it results in increased cost, losses, space and weight on the experimental board as well as lower reliability. Then, a MOSFET with an intrinsic diode with a lower reverse recovery current and lower reverse recovery charge can reduce switching losses and result in lower heat dissipation (Khersonsky *et al.*, 1992).

The reverse recovery charge (Q_{rr}) causes voltage overshoot, possible device failure. Moreover, the higher it is and more susceptible the device is to have a hard commutation (Huang, 2014). The time-current integration during the recombination phase as indicated in Fig. 5.4 also includes the drain-source capacitance charge (Q_{oss}), and there is no physical indication to differentiate their impacts on the reverse recovery process (Huang, 2014). According to (Huang, 2014), one way to determine the real value of the (Q_{rr}) is to subtract the value of (Q_{oss}) (specified in the datasheet) from the (Q_{rr}). Since a high reverse recovery charge can have a major negative impact on the switching performances, it is important to understand which parameters influence its value. To reduce the total reverse recovery charge of the low side MOSFET, decreasing the body diode conduction time, the diode current, and the hard commutation current slope (di_F/dt) directly reduce the value of Q_{rr} since they reduce the amount of accumulated charge during the conduction phase of the body diode (Huang, 2014). However, only reducing the conduction time of the body diode without reducing the maximum forward conduction current will have a minimal effect on the total reverse recovery charge since saturation of accumulated charges tends to be attained very quickly in the body diode. Moreover, it is not always possible to change any

of those parameters since they are defined by the application. Consequently, the best approach to have the greatest minimizing effect of Q_{rr} would be to choose a device with a reduced Q_{rr} when subject to hard commutation topology (Huang, 2014).

For the present experiments, identical power package MOSFETs TO-247-3 have been chosen for every technology under comparison with very similar ratings. In terms of GaN, power devices under the TO-247-3 package are exclusively under a cascade configuration with a low voltage Si MOSFET. Often referenced as the cascode GaN, this consists of a normally-on high voltage GaN High Electron Mobility Transistor (HEMT) in series with a normally-off low voltage (LV) Si MOSFET (Recht, Huang & Wu, 2021). Together, they form a complete normally-off MOSFET as the external drain lead is provided by the GaN HEMT, the source and gate of the GaN MOSFET are respectively connected to the drain and source of the LV Si MOSFET, and the external gate and source are provided by the LV Si MOSFET (Recht *et al.*, 2021). During forward voltage polarization of the cascode GaN, the GaN HEMT self-turned off as the voltage increases over the LV Si MOSFET because it decreases the voltage of the internal gate-source of the HV GaN HEMT (Recht *et al.*, 2021). In this configuration, the GaN HEMT doesn't exhibit a parasitic diode behavior when the MOSFET is in the third quadrant, but still offers a reverse conduction path. However, the Si MOSFET inherently adds a reverse recovery process in this conduction quadrant because of its parasitic body diode in series with the GaN HEMT (Recht *et al.*, 2021). Since the Si MOSFET is a LV device, it only adds a small amount of reverse recovery charge (Q_{rr}) to the device in comparison to standard HV Si MOSFET with higher reverse recovery charge (Recht *et al.*, 2021). However, during the reverse conduction phase, the current has to go through the body diode of the LV MOSFET then into the HV GaN HEMT drain-source on resistance, resulting in increased reverse voltage during 3rd quadrant conduction (Recht *et al.*, 2021). As for other MOSFET technologies, it is possible to reduce the reverse voltage during 3rd quadrant operation by turning on the MOSFET with the appropriate gate voltage (Recht *et al.*, 2021). Figure 5.6 presents the schematic symbol and the internal device structure of a GaN MOSFET in a cascode configuration under the TO-247-3 package from TPH3205WSBQA GaN MOSFET's datasheet (Transphorm Inc., 2017).

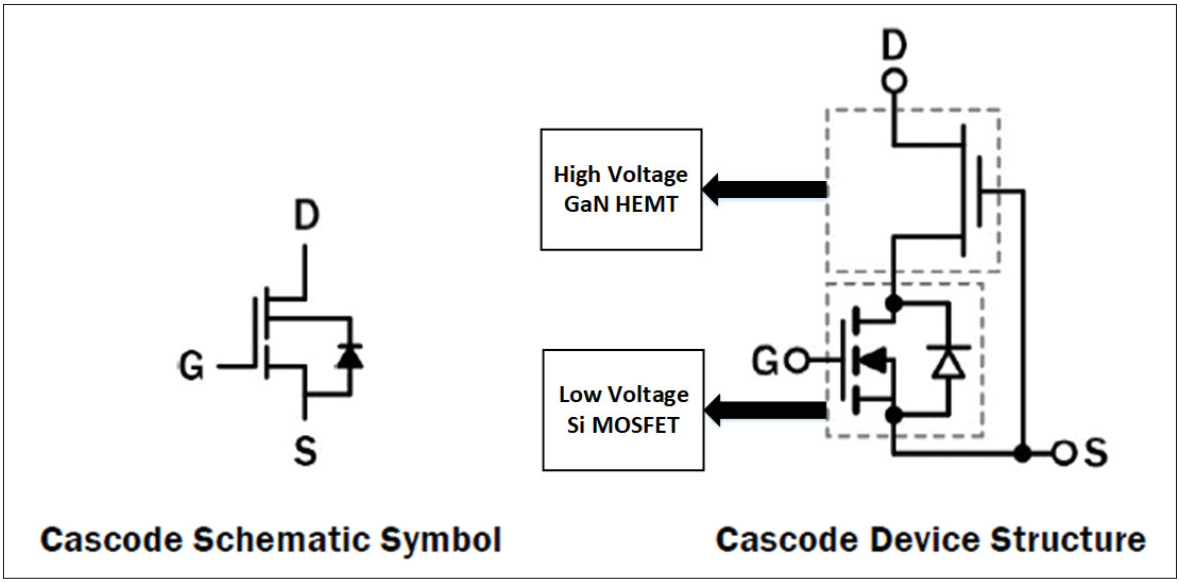

Figure 5.6 Cascode schematic symbol and internal cascode device structure of GaN MOSFETs under TO-247-3 package
Adapted from Transphorm Inc. (2017)

Nowadays, lateral majority carriers GaN HEMT are not accessible under through-hole power packages as TO-247, except under cascode configuration. Since this high voltage configuration consists of an HV GaN device with an LV Si MOSFET, it is important to understand the behavior of this majority carrier itself in the third quadrant operation. One of the most common claims about GaN HEMT is the absence of the body diode, but with the benefits of the reverse conduction. Yet, there is not any accumulated reverse recovery charge since this is a majority carrier even under the 3rd quadrant configuration (Sun, 2019). GaN HEMT has no body diode, but the symmetry of the channel region induces a third quadrant diode-like behavior without the PN junction but without the reverse recovery charge (Q_{rr}) (Sun, 2019). The drain source structure of the lateral GaN HEMT is connected through a two-dimensional electron gas (2DEG) with a conductivity modulation controlled by the applied gate voltage (Sun, 2019). In the third quadrant configuration, the source and drain are swapped and as the drain voltage is lower than the gate voltage, the device turns on and allows the reverse conduction through conductivity modulation (Sun, 2019). Then, in the 1st quadrant, the gate-source voltage has to be over the threshold voltage to allow conduction, but under the third quadrant, this is not necessary,

exhibiting a diode-like behavior. However, allowing the 3rd quadrant conduction require the gate-drain voltage to be over the threshold voltage, which is the addition of the gate-source voltage with the source-drain voltage, so it naturally turns on as the (v_{sd}) increases. Since reverse conduction is allowed without gate polarization, the source-drain voltage is typically higher than with a PN junction diode in Si MOSFETs. Since gate polarization during reverse conduction can highly reduce reverse conduction losses, minimizing the dead time between high side and low side lateral GaN HEMT is necessary to reduce 3rd quadrant conduction losses (Sun, 2019). In hard commutation topologies, such as the half-bridge configuration, a large part of high side turn-on losses are due to the reverse recovery current. Since HV lateral GaN HEMT lacks the PN junction, they can significantly reduce switching losses in hard switching topologies without requiring an additional parallel diode. However, special considerations regarding gate synchronization are required to minimize 3rd quadrant conduction losses (Sun, 2019).

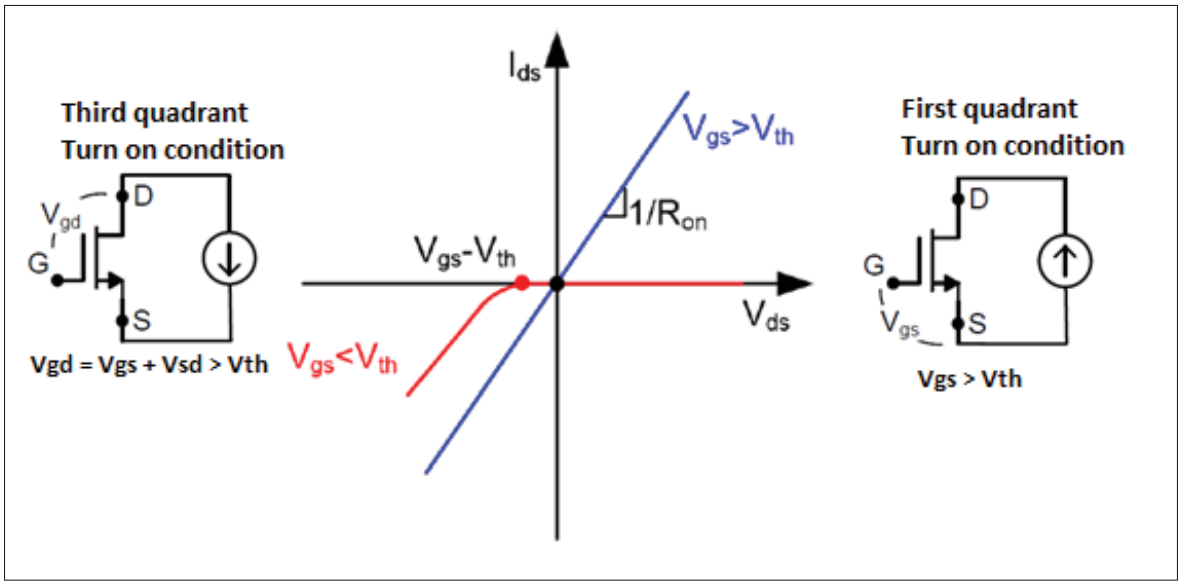

Figure 5.7 Simplified GaN behavior and turn-on conditions in the first and third quadrant
Adapted from Sun (2019)

To recap, the first current measurement of the positive current slope of the high side MOSFET is an equivalent measurement of the inverse of the low side MOSFET's decreasing current (di_F/dt) during the early stage of the reverse recovery process. This current slope is an indication of the switching speed of the high side device under a specific external gate configuration and gate

voltage. However, taking into account the internal gate resistance to determine the equivalent total gate resistance is a better evaluation to determine the absolute maximum switching speed of the device under an equivalent total gate resistance and gate voltage. As explained in Chapter 4, due to high disparities in internal gate resistance between devices under study, it is not possible to compare MOSFET's switching performances under equivalent total gate resistance. Also, faster is the switching speed and faster the low side MOSFET's parasitic diode release the accumulated charges and exhibit a high impedance path. This lead to a higher maximum reverse recovery current (I_{rrm}), which is the third current measurement taken into this analysis. A higher maximum reverse recovery current will lead to a faster current slope during the blocking phase of the low side MOSFET (di_R/dt) leading to higher surge voltage in the commutation path. The inverse of this current slope is the second equivalent current slope measurement of the high side MOSFET. Then, the reverse recovery charge of the low side MOSFET's body diode will have a major influence on the maximum reverse recovery current (I_{rrm}) as well as the surge voltage during the blocking phase.

5.1.3 Low Side Drain-Source Voltage (LS-VDS)

The following established measurement points are voltage measurements and voltage slopes of the low side drain-source voltage (v_{ds}) when the parasitic diode starts blocking the current during the reverse recovery process. The first measurement is the maximum positive voltage slope of the low side MOSFET (dv_{ds}/dt) when the body diode starts to exhibit a high impedance path. Since the impedance of the body diode increases during this phase of the reverse recovery process, the supply voltage quickly appear on the low side MOSFET. In addition, the reverse recovery current of the low side body diode is quickly decreasing, leading to a very fast increase in voltage and a potential surge voltage in the switching loop. Consequently, the second measurement point is the maximum surge voltage appearing across the low side MOSFET (maximum LS-v_{ds} value) at the end of the reverse recovery process. At last, measurements of the maximum negative voltage slope over the low side MOSFET (dv_{ds}/dt) and the resonance frequency (ω) provides some indications about the interaction between MOSFET's internal capacitances and parasitic

inductances of the circuit during the switching process. The maximum surge voltage value and resonant frequency for a chosen configuration can lead to proper snubber configurations. Fig. 5.8 illustrates low side drain-source voltage measurements of the GaN MOSFET using the drain methodology at 100V. It will be used as an example. Maximum voltage slope measurements are taken between 20% and 80% of total variations under an approximated steady voltage slope as shown in Fig. 5.8. As already specified in Chapter 4, under fast switching configurations, the source methodology is preferred to assess turn-on switching waveforms since the drain methodology exhibits extended resonance with parasitic components of the switching path.

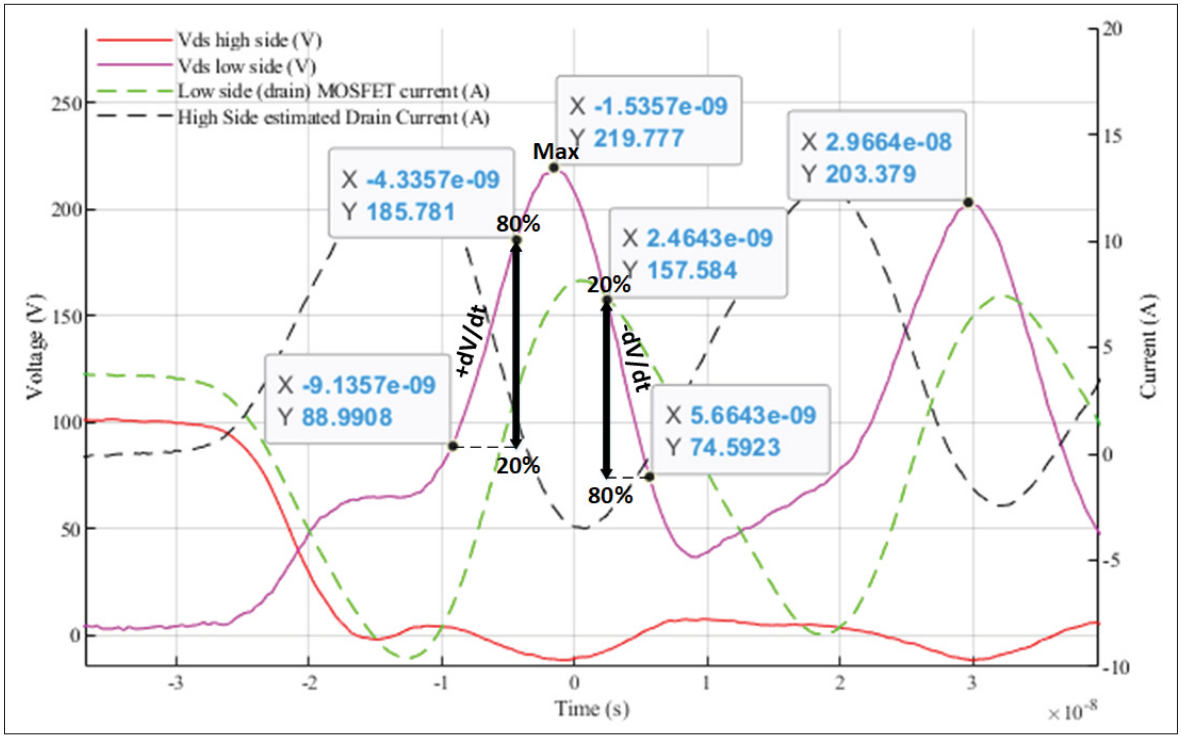

Figure 5.8 Close view of high side and low side GaN turn-on switching waveforms: LS-v_{ds} maximum positive slope ($+dv_{ds}/dt$), maximum value and maximum negative slope ($-dv_{ds}/dt$) at 100V with low side drain lead (both high and low side R_{on} = 10Ω & R_{off} = 3.3Ω)

5.1.4 Turn-Off losses, Duration and Maximum Turn-off High Side Estimated Current (HS-EC) Slope

As for the turn-on process, the difference in the load current measurement and low side MOSFET's current allows evaluating turn-off switching losses of the high side MOSFET. In contrast to turn-on losses measurements, it is preferable to use the drain methodology to evaluate and compare turn-off losses since the source lead measurement is influenced by the gate circuit. To evaluate the low side parasitic diode's performances under the freewheeling period, the low side MOSFET is turned on after the high side turns off to reduce the body diode's forward voltage. Consequently, the source lead methodology captures the gate current at low-side turn-on which results in incorrect estimation of the high side MOSFET's turn-off current.

Since the low side MOSFET is under a low voltage when it turns on during the freewheeling phase, there is no major resonance occurring between the parasitic component of the commutation loop, the added wire on the drain lead and the internal parasitic capacitances of the MOSFET at this moment. However, there is still some resonance between the output capacitance of the high side MOSFET and the added drain lead wire during the turn-off interval. However, it remains acceptable conditions. Thus, the drain methodology offers a current measurement method with minimal perturbations during the turn-off switching process.

However, since the gate driving time delay is high enough to allow the high side MOSFET to completely turn-off before the low side MOSFET turn-on, the current of the high side MOSFET reaches zero before capturing the gate current of the low side MOSFET with the source lead methodology. Then, once the HS-EC reaches zero, further increase in current captured with the source methodology from the gate circuit can be ignored. Still, both methodologies will be considered, but different total gate resistance (internal and external) and different gate voltage exhibit a variable perturbation on measurements with the source methodology during the turn-off interval. Consequently, the drain methodology is considered the primary method to compare turn-off switching losses of the high side device. As for the turn-on process, the delay between voltage and current probes has been adjusted carefully in addition to taking into account the propagation delay and rise time. In addition to the turn-off duration, the maximum decreasing

current slope of the high side estimated current is assessed to evaluate the maximum turn-off switching speed of the high side MOSFET under a specific gate configuration. Fig. 5.9 illustrates an example of turn-off losses computation, duration, and maximum current slope of the GaN MOSFET under the specified 100V configuration.

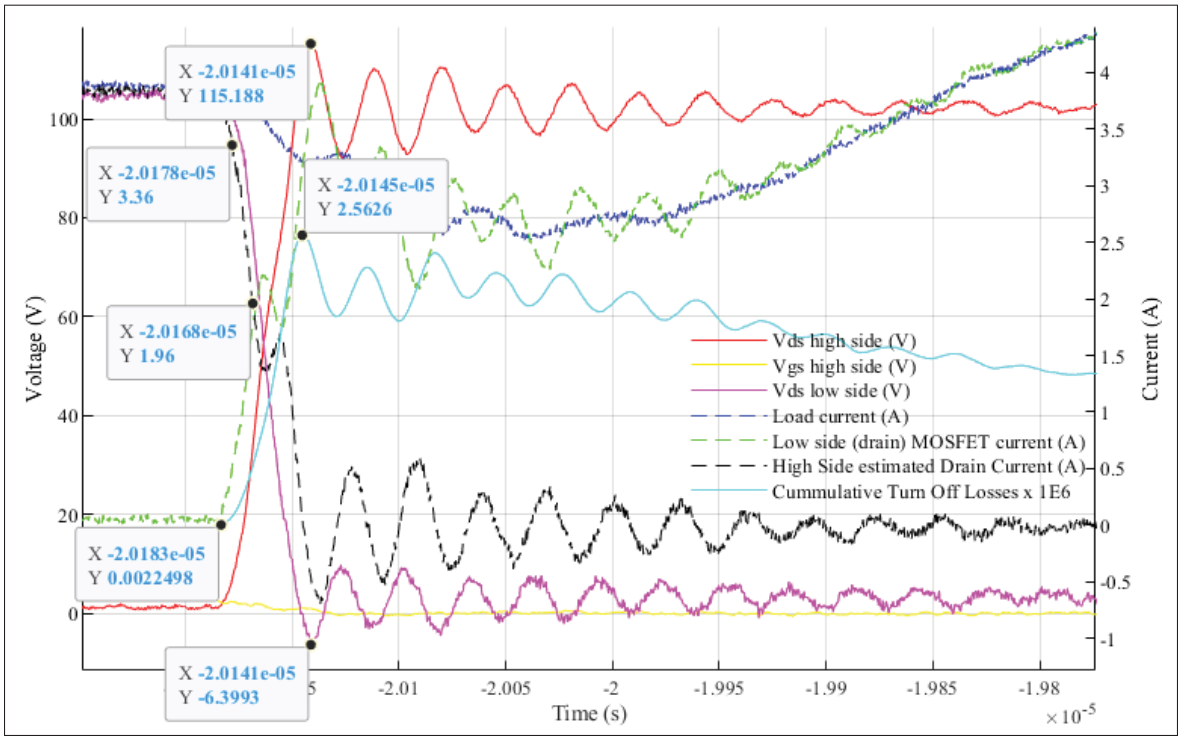

Figure 5.9 Close view of high side and low side GaN turn-off switching waveforms: turn-off losses, duration and maximum value of decreasing slope at 100V with low side drain lead (both high and low side R_{on} = 10Ω & R_{off} = 3.3Ω)

5.1.5 Conduction Losses (10 μs)

Finally, the conduction time is measured over a 10 μs duration ending 1 μs before the beginning of the high side MOSFET turn-off interval. Both current measurement methodologies offer an adequate and equivalent estimation of the high side current during the conduction phase. To make sure that the high side MOSFET is in full conduction state, only the last 10 μs of the conduction phase are considered to compute and compare conduction losses. Fig. 5.10 presents an example of conduction losses waveforms of the GaN MOSFET at 100V. As shown

in Fig. 5.10, oscilloscope waveforms were not scaled around the conduction voltage to increase the accuracy of the voltage measurement during the conduction phase. Then, drain-source voltage measurement during the conduction interval exhibits worse SNR compared to switching voltage measurements due to large voltage variation during switching intervals, resulting in less accuracy of computed losses during the conduction phase. To avoid sporadic perturbations on voltage measurement during the conduction interval, conduction losses are computed and compared at the end of the conduction interval, and for a conduction time of 10 μs. It would be possible to only take a resistance measurement between the drain-source connections while applying a positive gate voltage to obtain an accurate value of $R_{ds(on)}$ to estimate the conduction losses. Moreover, a simple estimate of the conduction resistance with a specific gate voltage from datasheet could be done to compare conduction losses. However, the voltage-current measurement methodology defined in the experiment allow to consider the temperature effect on the value of the MOSFET $R_{ds(on)}$. Then, it is not about comparing conduction resistance under a specific driving voltage, it is more about comparing conduction losses for a specific application. This second approach inherently considers that if the device exhibit higher switching losses, increasing the junction temperature, this might also results in increased conduction losses that would not have been observable with a simple resistance measurement.

5.2 Comparison of Experimental Results

This section presents the comparative results for each technologies under study. Raw data of all experimental results under all configurations are available in Appendix III. Absolute value measurements, computed results and relative comparison of results are all presented with both measurement techniques under all experimentation configurations as follow:

- Si, SiC and GaN at 50V supply, 22Ω external gate resistance.
- Si, SiC and GaN at 50V supply, 10Ω external gate resistance.
- Si, SiC and GaN at 100V supply, 22Ω external gate resistance.
- Si, SiC and GaN at 100V supply, 10Ω external gate resistance.

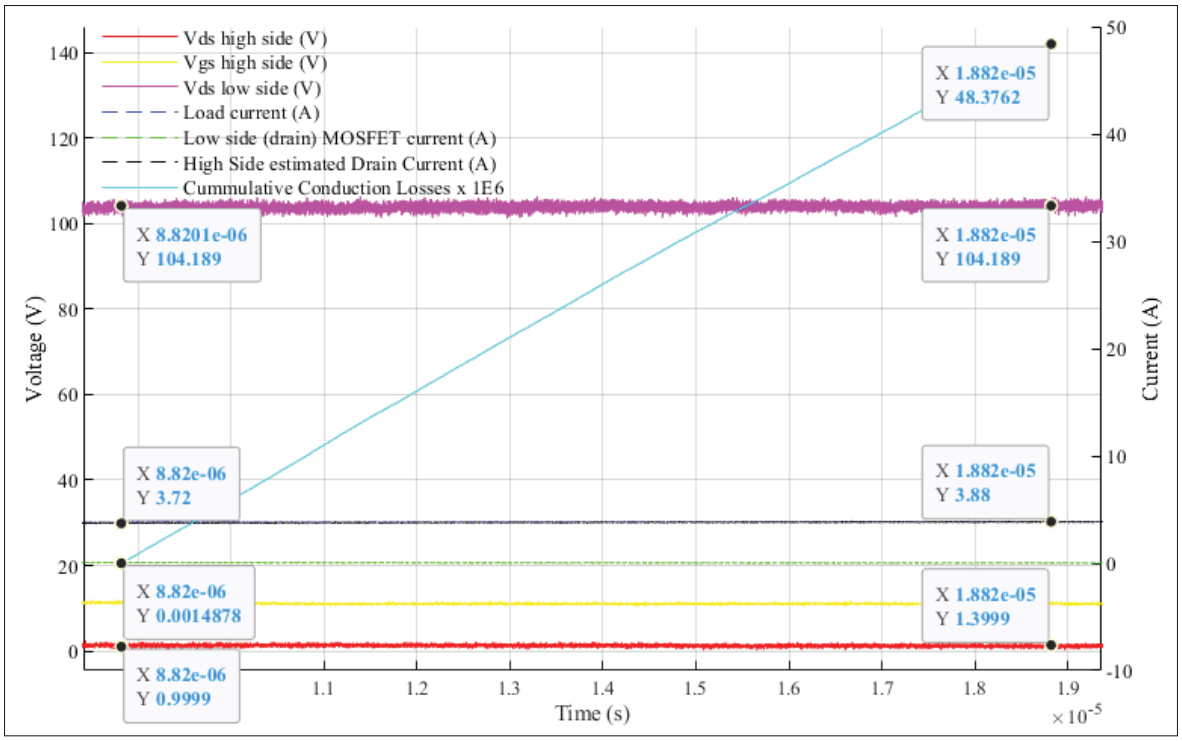

Figure 5.10 Close view of GaN conduction waveforms: computation of conduction losses at 100V with low side drain lead (both high and low side R_{on} = 10Ω & R_{off} = 3.3Ω)

In order to compare MOSFETs altogether, experimental data are expressed under the per-unit system (pu) referenced to the SiC MOSFET's results for all measurement points. With this approach, it is possible to observe relative comparison of established measurement points between different technologies under identical experimental configurations. Relative comparison based on multiple comparable experimental configurations, such as external gate resistance, switching frequency, duty cycle and voltage supply allow to observe repeatability and consistency in relative results between technologies. The only difference in experimental configurations of compared devices is the gate driving voltage of the SiC MOSFET, which is of 18V instead of 12V for other technologies.

Understanding the methodology employed to observe tendencies between relative comparisons of experimental results is critical to its interpretation. Consequently, an example on how to compute the relative comparison of turn-on losses (1st peak) between the Si MOSFET

(IPW65R080CFDA) and the SiC MOSFET (SCT3060ALFR) as presented on Table 5.1 of next section is defined as follow.

In Table III-1 of appendix III, Si MOSFET's turn-on losses (1st peak) at a supply voltage of 50V with an external gate resistance of 22Ω under the drain methodology shows experimental losses of 14.3 μJ. For the same experimental configuration, SiC MOSFET's turn-on losses (1st peak) are only of 1.5 μJ. Based on those results, the relative comparison between the Si MOSFET and the SiC MOSFET can be computed simply by dividing the result of the Si MOSFET by the result of the SiC MOSFET (14.3/1.5), giving a value of 9.6 pu as presented in Table 5.1. Actually, this shows that under this specific experimental condition, the established measurement point defined as turn-on losses (1st peak) is 9.6 times higher for the Si MOSFET compared to the SiC MOSFET.

This exact same methodology is applied to the computation done on all relative observations of all established measurement points, for all technologies, and under all experimental configurations. In all cases, experimental results obtained with the SiC MOSFET are defined as the reference value to express relative results of both GaN and Si MOSFETs. Relative comparison between technologies are only presented between same established measurement point in exact identical experimental configurations.

5.2.1 Comparative Experimental Results between Si MOSFETs (IPW65R080CFDA) and SiC MOSFETs (SCT3060ALHR) in pu

Table 5.1 shows comparative results between the Si MOSFET and SiC MOSFET under the same experimental configurations, using SiC experimental results as the reference value.

In Table 5.1, the relative comparison for each experimentations between the Si MOSFET and the SiC MOSFET under study is presented. Unfortunately, it was not possible to have suitable stable waveforms with the Si MOSFET at 100V due to high perturbations on the gate circuit as explained in chapter 4, except for the drain methodology at a reduced gate resistance of 10 Ω. Still, comparative results obtained at 100V are quite similar to those at 50V under the same current

Table 5.1 Relative Comparison of Si MOSFET (IPW65R080FDA) to SiC MOSFET (SCR3060ALHR) (pu)

Established Measurement Points	50V Supply				100V Supply			
	$R_{G(on)}$ = 22Ω		$R_{G(on)}$ = 10Ω		$R_{G(on)}$ = 22Ω		$R_{G(on)}$ = 10Ω	
	Drain Method	Source Method	Drain Method	Source Method	Drain Method	Source Method	Drain Method	Source Method
Turn-on losses (1st peak)	9.6	9.6	7.6	10.8	-	-	5.8	-
Turn-on duration (1st peak)	2.4	2.4	2.2	2.3	-	-	1.7	-
Turn-on losses (Slope Stabilized)	**10.6**	**12.7**	**7.9**	**15.4**	-	-	**7.3**	-
Turn-on duration (Slope Stabilized)	1.4	4.3	3.5	3.8	-	-	3.0	-
Turn-on losses (v_{gs} Final & Slope Stabilized)	11.3	12.9	8.0	16.1	-	-	7.4	-
Turn-on duration (v_{gs} Final & Slope Stabilized)	6.6	9.2	5.2	3.1	-	-	7.5	-
Maximum Positive HS-EC (dI_F/dt)	0.9	1.0	1.0	1.0	-	-	1.3	-
Maximum Negative HS-EC (dI_R/dt)	4.3	3.3	4.8	3.8	-	-	6.2	-
Maximum HS-EC Value	3.1	3.5	3.2	3.6	-	-	3.3	-
Maximum Positive LS-v_{ds} (dv_{ds}/dt)	2.7	2.0	3.7	2.2	-	-	4.7	-
Maximum Negative LS-v_{ds} (dv_{ds}/dt)	3.6	6.0	4.3	5.6	-	-	4.6	-
Maximum LS-v_{ds} Value	2.0	1.9	2.1	2.0	-	-	2.0	-
LS-v_{ds} Resonant Frequency (ω)	0.4	0.5	0.5	0.5	-	-	0.9	-
Turn-off losses	5.0	7.5	5.5	7.4	-	-	3.1	-
Turn-off duration	8.5	7.6	8.3	8.0	-	-	5.7	-
Maximum Turn-off HS-EC (dI/dt)	0.2	0.3	0.2	0.3	-	-	1.1	-
Conduction losses (10 μs)	1.3	1.5	1.3	3.2	-	-	1.4	-

measurement technique and gate resistance. Then, Table 5.2 presents a statistical analysis of the relative comparison between the Si MOSFET and SiC MOSFET presented in Table 5.1. In Table 5.2, minimum, maximum, mean, median and standard deviation of all established measurement

points are expressed to have a condensed overview of the relative comparison between the Si MOSFET and the SiC MOSFET for all experimentation's configurations presented in Table 5.1.

Table 5.2 Cummulative Statistical Relative Comparison of Si MOSFETs (IPW65R080FDA) to SiC MOSFETs (SCR3060ALHR) under all Experimental Configurations (pu)

Established Measurement Points	**Minimum**	**Maximum**	**Mean**	**Median**	**Standard deviation**
Turn-on losses (1^{st} peak)	5.8	10.8	8.7	9.6	2.0
Turn-on duration (1^{st} peak)	1.7	2.4	2.2	2.3	0.3
Turn-on losses (Slope Stabilized)	**7.3**	**15.4**	**10.8**	**10.6**	**3.4**
Turn-on duration (Slope Stabilized)	1.4	4.3	3.2	3.5	1.1
Turn-on losses (v_{gs} Final & Slope Stabilized)	7.4	16.1	11.1	11.3	3.6
Turn-on duration (v_{gs} Final & Slope Stabilized)	3.1	9.2	6.3	6.6	2.3
Maximum Positive HS-EC (dI_F/dt)	0.9	1.3	1.1	1.0	0.1
Maximum Negative HS-EC (dI_R/dt)	3.3	6.2	4.5	4.3	1.1
Maximum HS-EC Value	3.1	3.6	3.3	3.3	0.2
Maximum Positive LS-v_{ds} (dv_{ds}/dt)	2.0	4.7	3.0	2.7	1.1
Maximum Negative LS-v_{ds} (dv_{ds}/dt)	3.6	6.0	4.8	4.6	0.9
Maximum LS-v_{ds} Value	1.9	2.1	2.0	2.0	0.1
LS-v_{ds} Resonant Frequency (ω)	0.4	0.9	0.6	0.5	0.2
Turn-off losses	3.1	7.5	5.7	5.5	1.8
Turn-off duration	5.7	8.5	7.6	8.0	1.1
Maximum Turn-off HS-EC (dI/dt)	0.2	1.1	0.4	0.3	0.4
Conduction losses (10 μs)	1.3	3.2	1.7	1.4	0.8

Statistical analysis of Table 5.2 shows relevant observations on Si turn-on losses and duration in comparison to the SiC MOSFET. For the three turn-on losses measurement points including

all experimental configurations, turn-on losses are in average 8.7 to 11.1 times higher than for the SiC MOSFET in the exact same conditions. Even if the standard deviation is high, the minimum relative comparison of turn-on losses still shows 5.8 times higher losses for the Si MOSFET as observed in turn-on losses (1st peak). Similarly, for all experimental scenarios, the average turn-on duration is between 2.3 to 6.6 times longer in comparison to the SiC MOSFET. In terms of full turn-on duration, the SiC MOSFET need a higher driving voltage to attain full conduction, but the total input capacitance (C_{iss}) is about 3 to 4 times smaller at supply voltage, and the total gate charge is about 3 times smaller compared to the chosen Si MOSFET. Even if the internal gate resistance is way lower for the Si MOSFET (0.75 Ω) (Infineon Technologies AG, 2012) compared to the SiC MOSFET (12 Ω) (Rohm Semiconductor, 2017), the SiC MOSFET still shows faster turn-on process at lower losses. Then, results show strong evidence for multiple experimental configurations that under the same circumstances, longer turn-on duration and higher losses using high voltage Si MOSFETs can be expected compared to similar characteristics' SiC MOSFETs.

Then, next measurement points in Table 5.2 are the maximum and minimum HS-EC slope, and the maximum value of high side Si MOSFET current during the reverse recovery process in comparison to the SiC MOSFET. As explained, the HS-EC (dI_F/dt) is highly dependent on the switching speed of the high side device. Based on experimental results and the statistical analysis presented in Table 5.1 and 5.2, there is not a significant difference between the Si MOSFET and the SiC MOSFET under study regarding the maximum (dI_F/dt) for equivalent external gate resistance with adequate driving voltage. However, the SiC MOSFET exhibits an increased internal gate resistance of 10.75 Ω in comparison to the Si MOSFET under established experimental conditions of equivalent external gate resistance. Still, the SiC MOSFET shows similar current slope with an increased total equivalent gate resistance. Then, under experimental conditions of comparative total equivalent gate resistance, considering both the internal and external gate resistance, faster current slope (dI_F/dt) is expected with the SiC device, but further analysis are required to valid this statement.

Next, the maximum HS-EC value of the Si MOSFET is in average 3.3 times higher compared to the SiC MOSFET under the same experimental conditions. Meaning that the average maximum reverse recovery current (I_{rrm}) of the Si MOSFET is around 3.3 times higher with a standard deviation of only 0.2. The (I_{rrm}) is highly dependent on the current slope of the high side device and the total reverse recovery charge of the low side MOSFET. Since the current slope of the high side MOSFET (dI_F/dt) and the conduction time are identical between the Si and SiC, the reverse recovery charge (Q_{rr}) is mainly responsible for this marked difference.

Unfortunately, Si and SiC's datasheets (Infineon Technologies AG, 2012; Rohm Semiconductor, 2017) only provide information on the reverse recovery charge (Q_{rr}) for a specific configuration without any means to determine the real (Q_{rr}) for the experimental conditions under study. Anyhow, based on Si's datasheet (Infineon Technologies AG, 2012), its Q_{rr} is at 1.2 μC at 400V with a forward diode's current of 26.3A and a reverse recovery current slope of 100A/μs. Similarly, the reverse recovery charge of the SiC MOSFET provided in the datasheet (Rohm Semiconductor, 2017) is only of 55 nC at 300V with a diode current of 13A and a reverse recovery current slope of 1100A/μs. Diode's specifications of the Si MOSFET is at higher diode forward current, leading to extra accumulation of the reverse recovery charge. However, diode's characteristics of the SiC MOSFET are defined under a reverse recovery current slope about 10 times higher, which also increase the reverse recovery charge. For mentioned respective configurations defined in datasheets (Infineon Technologies AG, 2012; Rohm Semiconductor, 2017), the reverse recovery time (t_{rr}) is 180 ns for the Si MOSFET and only 15 ns for the SiC MOSFET. Unfortunately, there is not any way to convert (Q_{rr}) defined in datasheets (Infineon Technologies AG, 2012; Rohm Semiconductor, 2017) of both MOSFET on an identical basis. However, the difference in specified (Q_{rr}) is as high as 20 times higher for the Si MOSFET, giving expectation of higher (Q_{rr}) for the Si MOSFET in equivalent scenarios as supported by results of higher maximum reverse recovery current presented in Table 5.2.

Of course, the higher reverse recovery charge of the Si MOSFET results in higher maximum reverse recovery current (I_{rrm}) and rougher blocking phase of the low side diode. This concretely translate in a maximum negative reverse recovery current slope (diR/dt) averaging 4.5 times

higher with the Si MOSFET compared to the SiC MOSFET, with a standard deviation of only 1.1. This very high current slope (diR/dt) of the Si MOSFET results in very high surge voltage and voltage slope in the switching loop as the fast current slope reacts and resonate with the parasitic inductances and capacitances. Consequently, the maximum surge voltage is in average twice as high for the Si MOSFET with voltage slopes between 3 to 4.8 times higher. Since more energy is released in the switching loop during the reverse recovery process of the Si MOSFET, this tends to results in a longer turn-on process with an extended duration before the resonance ends. Then, this results in higher risk of perturbations on gate circuits because of higher Miller capacitance, higher surge voltage, and higher voltage slope during the blocking phase of the reverse recovery process.

Next, the average resonance frequency is about twice as small for the Si MOSFET compared to the SiC MOSFET. Both MOSFETs are in the exact same configurations, even if the added wire is the same one that has been used between experimentations to minimize any influence from using a slightly longer or shorter added wire on the total parasitic inductance. Then, the only main parameter resulting in different results of the resonance frequency between the Si and SiC MOSFET under study are the parasitic capacitances of the MOSFETs. Based on datasheets (Infineon Technologies AG, 2012; Rohm Semiconductor, 2017), SiC internal output capacitance (C_{oss}) is smaller than the $Coss$ of the Si MOSFET for any voltage supply under study in experiments, resulting in a faster resonance for the SiC, but this is mainly interesting for snubber designs and EMI issues.

Then, turn-off losses, duration and maximum turn-off high side current slope have been observed and compared for all experimentations like one did for the turn-on losses. In average, for all experiments, turn-off losses are 5.7 times higher for the Si MOSFET with a duration 7 times longer and a current slope around 0.4 pu of what is observed with the SiC MOSFET. The switching speed at turn-off is actually a very important parameter to minimize total turn-off losses, and the major parameter of influence for this measurement point is the input capacitance (C_{iss}). Based on their respective datasheets (Infineon Technologies AG, 2012; Rohm Semiconductor, 2017), SiC input capacitance (C_{iss}) is about 4 times smaller in comparison to the Si MOSFET,

which is highly representative of the gate-source capacitance. Even if the driving voltage of the SiC MOSFET is 50% higher than the one used for the Si MOSFET, it still takes way more time to completely discharge the gate-source capacitance of the Si MOSFET with an identical turn-off gate voltage of 0V. Then, experimental measurements result in expected behavior of convincing faster turn-off process for the SiC MOSFET at reduced losses.

At last, as detailed in section 5.1.5, conduction losses could have been measured only with a resistance measurement during forward polarization of the MOSFETs. However, the exact same methodology employed for the switching losses has been used (i.e. losses computation with voltage and current measurements). Based on compared typical on-state resistance ($R_{ds(on)}$) from Si and SiC datasheets (Infineon Technologies AG, 2012; Rohm Semiconductor, 2017), smaller conduction losses were already expected for the SiC MOSFET. Moreover, it would have been even more interesting to observe conduction losses at increased temperature, since SiC MOSFETs normally exhibit a mild increase of the $R_{ds(on)}$ between 0°C and 75°C in comparison to Si MOSFETs. Comparative experimental observations confirm expectations, showing an average increased conduction losses of the Si MOSFET by 1.72 pu, but the standard deviation is very high at 0.8 pu. Then, higher conduction losses of the Si MOSFETs are expected. However, more observations are needed to have a reliable confirmation about relative comparison of conduction losses under exact external configurations between Si MOSFETs and SiC MOSFETs.

All considered, experimental observations between the SiC MOSFET and Si MOSFET under study are all in favor of the SiC MOSFET. Thus, SiC MOSFETs seem like an easy choice when compared to Si MOSFETs to minimize switching losses, conduction losses, increase switching frequency, and possibly reduced strain and EMI issues. However, further observations at different voltage, power rating, and at increased power would be necessary to observe the drawbacks that may come with the SiC MOSFET under more stressful conditions. Relative comparison under multiple experiments of exact identical external configurations gives tendency in switching behavior between two specific devices of different technology. Observations could be slightly different under different devices characteristics.

5.2.2 Comparative Experimental Results between GaN MOSFETs (TPH3205WSBQA) and SiC MOSFETs (SCT3060ALHR) in pu

Table 5.3 shows comparative results between the Si MOSFET and SiC MOSFET under the same experimental configurations, using SiC experimental results as the reference value. Unlike with the Si MOSFET, it was possible to have suitable waveforms with the GaN MOSFETs for all experimental configurations.

In order to analyse comparative results between GaN and SiC MOSFETs, Table 5.4 is illustrating the statistical analysis of the relative comparison presented in Table 5.3. In Table 5.4, it is important to highlight very strong standard deviation for many relative comparison of established measurement points.

More explicitly, important differences in maximum and minimum values are observed for resonance dependant measurement points like stabilized long-term turn-on losses and duration. In addition, Table 5.4 shows that the maximum positive and negative HS-EC slope is in average quite higher for the GaN MOSFET compared to the SiC MOSFET, meaning that the switching speed is higher for the GaN MOSFETs under identical configurations.

Unfortunately, the extreme ruggedness of the blocking phase of the low side parasitic diode seems to cause major problems when taking measurements with the drain methodology on GaN MOSFETs. This faster slew rate results in higher surge voltage and resonance, which highly interacts with the measurement lead wire when placed on the low side MOSFET's drain pin. The same perturbations, on a way less considerable scale, were observed with the Si MOSFETs and SiC MOSFETs during the turn-on process. As presented in chapter 4, due to further influence and resonance from the drain current measurement methodology, the source methodology is more suitable for turn-on switching measurements. Conversely, turn-off observations are less influenced from the drain lead methodology because the absence of a Kelvin connection on chosen MOSFETs does not permit to measure the low side MOSFET's current without also taking a measurement of the gate current.

Table 5.3 Relative Comparison of GaN MOSFETs (TPH3205WSBQA) to SiC MOSFETs (SCR3060ALHR) (pu)

Established Measurement Points	50V Supply				100V Supply			
	$R_{G(on)}$ = 22Ω		$R_{G(on)}$ = 10Ω		$R_{G(on)}$ = 22Ω		$R_{G(on)}$ = 10Ω	
	Drain Method	Source Method	Drain Method	Source Method	Drain Method	Source Method	Drain Method	Source Method
Turn-on losses (1st peak)	0.5	0.5	0.4	0.3	0.2	0.3	0.3	0.5
Turn-on duration (1st peak)	0.8	0.9	0.9	1.0	0.8	0.8	0.6	0.8
Turn-on losses (Slope Stabilized)	**0.9**	**0.5**	**1.1**	**0.4**	**0.7**	**0.3**	**2.2**	**0.7**
Turn-on duration (Slope Stabilized)	1.4	2.3	3.0	2.2	11.6	2.6	10.5	2.1
Turn-on losses (v_{gs} Final & Slope Stabilized)	0.9	0.5	1.3	0.5	0.7	0.4	2.4	0.7
Turn-on duration (v_{gs} Final & Slope Stabilized)	1.3	1.2	4.6	1.2	7.0	1.4	11.0	1.3
Maximum Positive HS-EC (dI_F/dt)	1.6	1.7	1.5	1.6	2.5	2.4	2.0	2.1
Maximum Negative HS-EC (dI_R/dt)	2.4	2.7	2.1	2.7	4.3	4.6	3.3	4.5
Maximum HS-EC Value	1.6	1.8	1.5	1.7	1.7	1.8	1.5	1.7
Maximum Positive LS-v_{ds} (dv_{ds}/dt)	1.8	1.4	1.7	1.0	2.6	1.9	2.2	1.4
Maximum Negative LS-v_{ds} (dv_{ds}/dt)	2.1	2.1	1.9	1.4	5.0	5.3	3.6	2.4
Maximum LS-v_{ds} Value	1.6	1.5	1.4	1.3	1.8	1.9	1.7	1.5
LS-v_{ds} Resonant Frequency (ω)	0.6	0.6	0.7	0.6	0.7	0.7	0.8	0.6
Turn-off losses	1.3	1.2	1.6	1.2	1.4	1.1	1.0	0.9
Turn-off duration	1.8	1.6	1.9	1.7	1.2	0.8	1.1	1.1
Maximum Turn-off HS-EC (dI/dt)	0.5	0.6	0.7	0.7	0.8	0.9	0.7	1.0
Conduction losses (10 μs)	1.3	1.8	1.5	1.4	0.8	0.8	1.3	1.1

However, the influence of the drain methodology was very mild on both Si and SiC MOSFETs in comparison to GaN MOSFETs. Appendix IV presents comparison tables between the drain and source methodology of every established measurement points for all MOSFETs under study. The relative comparison of established measurement points between the drain and source

Table 5.4 Cummulative Statistical Relative Comparison of GaN MOSFETs (TPH3205WSBQA) to SiC MOSFETs (SCR3060ALHR) under all Experimental Configurations (pu)

Established Measurement Points	Minimum	Maximum	Mean	Median	Standard deviation
Turn-on losses (1st peak)	0.2	0.5	0.4	0.4	0.1
Turn-on duration (1st peak)	0.6	1.0	0.8	0.8	0.1
Turn-on losses (Slope Stabilized)	**0.3**	**2.2**	**0.8**	**0.7**	**0.6**
Turn-on duration (Slope Stabilized)	1.4	11.6	4.4	2.4	4.1
Turn-on losses (v_{gs} Final & Slope Stabilized)	0.4	2.4	0.9	0.7	0.7
Turn-on duration (v_{gs} Final & Slope Stabilized)	1.2	10.9	3.6	1.3	3.7
Maximum Positive HS-EC (dI_F/dt)	1.5	2.5	1.9	1.9	0.4
Maximum Negative HS-EC (dI_R/dt)	2.1	4.6	3.3	3.0	1.0
Maximum HS-EC Value	1.5	1.8	1.7	1.7	0.1
Maximum Positive LS-v_{ds} (dv_{ds}/dt)	1.0	2.6	1.7	1.8	0.5
Maximum Negative LS-v_{ds} (dv_{ds}/dt)	1.3	5.3	3.0	2.3	1.5
Maximum LS-v_{ds} Value	1.3	1.9	1.6	1.6	0.2
LS-v_{ds} Resonant Frequency (ω)	0.6	0.8	0.7	0.7	0.1
Turn-off losses	0.9	1.6	1.2	1.2	0.2
Turn-off duration	0.8	1.9	1.4	1.4	0.4
Maximum Turn-off HS-EC (dI/dt)	0.5	1.0	0.7	0.7	0.2
Conduction losses (10 μs)	0.8	1.8	1.2	1.3	0.4

methodologies for the GaN MOSFETs are presented in Table 5.5. The experimental results obtained with the drain methodology are referenced on the results obtained with the source methodology for the same configuration in pu. Moreover, a brief statistical analysis highlight the major information on each data to ease the comparison and interpretation.

Table 5.5 Relative Comparison of GaN's Experimental Results with Drain Methodology to its relative Source Methodology Referenced on the Source Methodology's Results (pu)

Established Measurement Points	**50V Supply**		**100V Supply**		**Mean**	**Median**	**Standard Deviation**
	$R_{G(on)}$ **22Ω**	$R_{G(on)}$ **10Ω**	$R_{G(on)}$ **22Ω**	$R_{G(on)}$ **10Ω**			
Turn-on losses (1st peak)	1.1	1.6	0.9	0.8	1.1	1.0	0.4
Turn-on duration (1st peak)	0.9	1.0	1.1	0.7	0.9	0.9	0.2
Turn-on losses (Slope Stabilized)	2.0	5.0	2.3	3.7	**3.2**	**3.0**	**1.3**
Turn-on duration (Slope Stabilized)	1.7	2.7	6.7	6.8	**4.5**	**4.7**	**2.7**
Turn-on losses (v_{gs} Final & Slope Stabilized)	1.9	4.8	2.1	3.9	**3.2**	**3.0**	**1.4**
Turn-on duration (v_{gs} Final & Slope Stabilized)	1.3	3.3	5.6	6.0	**4.0**	**4.4**	**2.2**
Maximum Positive HS-EC (dI_F/dt)	1.0	1.0	1.1	1.1	1.0	1.1	0.03
Maximum Negative HS-EC (dI_R/dt)	1.2	1.2	1.2	1.3	1.2	1.2	0.05
Maximum HS-EC Value	1.1	1.1	1.1	1.1	1.1	1.1	0.01
Maximum Positive LS-v_{ds} (dv_{ds}/dt)	1.0	1.1	1.1	1.0	1.1	1.1	0.04
Maximum Negative LS-v_{ds} (dv_{ds}/dt)	1.1	1.2	1.0	1.1	1.1	1.1	0.05
Maximum LS-v_{ds} Value	1.1	1.1	1.0	1.1	1.1	1.1	0.02
LS-v_{ds} Resonant Frequency (ω)	0.9	0.9	0.9	0.9	0.9	0.9	0.004
Turn-off losses	0.9	0.9	1.0	1.0	0.9	0.9	0.1
Turn-off duration	1.0	1.0	1.0	1.0	1.0	1.0	0.02
Maximum Turn-off HS-EC (dI/dt)	1.0	1.2	1.0	1.0	1.1	1.0	0.1
Conduction losses (10 μs)	0.8	1.0	0.6	1.0	0.9	0.9	0.2

In Table 5.5, long-term turn-on losses and durations (in bold) show an average difference of 3.2 to 4.5 pu when measured and computed with the drain current methodology. Except for long-term turn-on data point, the drain methodology does not exhibit major influence on any other experimental measurements or computed results. Then, the drain methodology's

experimental measurements will be excluded for long-term turn-on analysis of the GaN MOSFETs to avoid perturbations from the measurement technique on the interpretation of results. For all other experimental data point, both measurement techniques will be included since only small differences in experimental results are observable between the drain and source current methodology. Table 5.6 presents the relative comparison between the GaN MOSFETs and the SiC MOSFETs, observations are referenced on SiC experimental measurements to express the relative difference in pu. Excluded relative observations with the drain methodology are bolded for long-term turn-on losses and durations datapoint.

Then, Table 5.7 shows the statistical analysis of the relative comparison presented in Table 5.6 between the GaN MOSFETs and the SiC MOSFETs. Data are excluding the relative long-term turn-on observations with the drain methodology.

Statistical analysis presented in Table 5.7 shows relevant observations on GaN turn-on losses and duration in comparison to the SiC MOSFET. For all turn-on losses measurement points, including all experimental configurations, turn-on losses are in average 0.4 to 0.5 pu of SiC MOSFETs' losses with a standard deviation from 0.1 to 0.2 pu. Then, there is no doubt that GaN MOSFETs provide lower turn-on losses in comparison to both SiC and Si MOSFETs, since Si MOSFETs showed even higher turn-on losses than the SiC MOSFETs under study, as presented in Table 5.2. However, the average long-term turn-on duration of the GaN MOSFET is between 1.3 to 2.3 times longer in comparison to the SiC MOSFET with a standard deviation ranging between 0.1 to 0.2 pu.

SiC MOSFETs need a higher driving voltage to attain full conduction, but the total input capacitance is about 2 times smaller at supply voltage, and the total gate charge is up to 2 times higher compared to the chosen GaN MOSFETs (Rohm Semiconductor, 2017; Transphorm Inc., 2017). Moreover, the internal gate resistance is way higher for the SiC MOSFET (12 Ω) (Rohm Semiconductor, 2017) in comparison to the GaN MOSFET under study (2.2 Ω) (Transphorm Americas Sales Representative, 2020), but SiC MOSFETS still shows smaller turn-on duration.

Table 5.6 Relative Comparison of GaN MOSFETs (TPH3205WSBQA) to SiC MOSFETs (SCR3060ALHR) (pu)
Long-Term Turn-on relative observations with the drain methodology excluded

Established Measurement Points	50V Supply				100V Supply			
	$R_{G(on)}$ = 22Ω		$R_{G(on)}$ = 10Ω		$R_{G(on)}$ = 22Ω		$R_{G(on)}$ = 10Ω	
	Drain Method	Source Method	Drain Method	Source Method	Drain Method	Source Method	Drain Method	Source Method
Turn-on losses (1st peak)	0.5	0.5	0.4	0.3	0.2	0.3	0.3	0.5
Turn-on duration (1st peak)	0.8	0.9	0.9	1.0	0.8	0.8	0.6	0.8
Turn-on losses (Slope Stabilized)	**0.9**	0.5	**1.1**	0.4	**0.7**	0.3	**2.2**	0.7
Turn-on duration (Slope Stabilized)	**1.4**	2.3	**3.0**	2.2	**11.6**	2.6	**10.5**	2.1
Turn-on losses (v_{gs} Final & Slope Stabilized)	**0.9**	0.5	**1.3**	0.5	**0.7**	0.4	**2.4**	0.7
Turn-on duration (v_{gs} Final & Slope Stabilized)	**1.3**	1.2	**4.6**	1.2	**7.0**	1.4	**11.0**	1.3
Maximum Positive HS-EC (dI_F/dt)	1.6	1.7	1.5	1.6	2.5	2.4	2.0	2.1
Maximum Negative HS-EC (dI_R/dt)	2.4	2.7	2.1	2.7	4.3	4.6	3.3	4.5
Maximum HS-EC Value	1.6	1.8	1.5	1.7	1.7	1.8	1.5	1.7
Maximum Positive LS-v_{ds} (dv_{ds}/dt)	1.8	1.4	1.7	1.0	2.6	1.9	2.2	1.4
Maximum Negative LS-v_{ds} (dv_{ds}/dt)	2.1	2.1	1.9	1.4	5.0	5.3	3.6	2.4
Maximum LS-v_{ds} Value	1.6	1.5	1.4	1.3	1.8	1.9	1.7	1.5
LS-v_{ds} Resonant Frequency (ω)	0.6	0.6	0.7	0.6	0.7	0.7	0.8	0.6
Turn-off losses	1.3	1.2	1.6	1.2	1.4	1.1	1.0	0.9
Turn-off duration	1.8	1.6	1.9	1.7	1.2	0.8	1.1	1.1
Maximum Turn-off HS-EC (dI/dt)	0.5	0.6	0.7	0.7	0.8	0.9	0.7	1.0
Conduction losses (10 μs)	1.3	1.8	1.5	1.4	0.8	0.8	1.3	1.1

Actually, GaN's first peak turn-on duration is in average 0.8 pu of the SiC MOSFETs, mainly meaning that the maximum reverse recovery current (I_{rrm}) is reached faster. Moreover, the maximum positive HS-EC is in average 1.9 times higher with the GaN MOSFETs with a standard deviation of 0.4 p.u.. Then, strong evidences suggest that GaN MOSFETs switch faster in

Table 5.7 Cummulative Statistical Relative Comparison of GaN MOSFETs (TPH3205WSBQA) to SiC MOSFETs (SCR3060ALHR) under all Configurations (pu) Long-Term Turn-on relative observations with the drain methodology excluded

Established Measurement Points	Minimum	Maximum	Mean	Median	Standard deviation
Turn-on losses (1st peak)	0.2	0.5	0.4	0.4	0.1
Turn-on duration (1st peak)	0.6	1.0	0.8	0.8	0.1
Turn-on losses (Slope Stabilized)	**0.3**	**0.7**	**0.5**	**0.4**	**0.2**
Turn-on duration (Slope Stabilized)	2.1	2.6	2.3	2.2	0.2
Turn-on losses (v_{gs} Final & Slope Stabilized)	0.4	0.7	0.5	0.5	0.2
Turn-on duration (v_{gs} Final & Slope Stabilized)	1.2	1.4	1.3	1.3	0.1
Maximum Positive HS-EC (dI_F/dt)	1.5	2.5	1.9	1.9	0.4
Maximum Negative HS-EC (dI_R/dt)	2.1	4.6	3.3	3.0	1.0
Maximum HS-EC Value	1.5	1.8	1.7	1.7	0.1
Maximum Positive LS-v_{ds} (dv_{ds}/dt)	1.0	2.6	1.7	1.8	0.5
Maximum Negative LS-v_{ds} (dv_{ds}/dt)	1.3	5.3	3.0	2.3	1.5
Maximum LS-v_{ds} Value	1.3	1.9	1.6	1.6	0.2
LS-v_{ds} Resonant Frequency (ω)	0.6	0.8	0.7	0.7	0.1
Turn-off losses	0.9	1.6	1.2	1.2	0.2
Turn-off duration	0.8	1.9	1.4	1.4	0.4
Maximum Turn-off HS-EC (dI/dt)	0.5	1.0	0.7	0.7	0.2
Conduction losses (10 μs)	0.8	1.8	1.2	1.3	0.4

average than both SiC MOSFETs and Si MOSFETs under study. However, relative comparisons show longer duration of the turn-on interval for the GaN MOSFET because very high surge voltage and resonance tend to perturb the high side turn-on behavior, resulting in increased duration before stabilization.

The maximum positive HS-EC (dI_F/dt) is highly dependent on the switching speed of the high side device. In Table 5.7, a significant variability of this parameter is observable between the GaN and SiC MOSFETs under study for equivalent external gate resistance with adequate driving voltage, showing higher switching speed for the GaN MOSFETs. However, the total equivalent gate resistance, including the internal and external resistance is way lower for the GaN MOSFET. Under experimental conditions of comparative total equivalent gate resistance, experimental results regarding the switching speed might show something different between GaN and SiC MOSFETs. Unfortunately, this was not subject to the experimental analysis due to major disparities in internal gate resistance between chosen MOSFETs as presented in chapter 4.

Next, mean value of the relative maximum HS-EC is 1.7 times higher for the GaN MOSFET, meaning that the average maximum reverse recovery current (I_{rrm}) is also around 1.7 times higher with a standard deviation of only 0.1. The I_{rrm} is highly dependent on the positive current slope of the high side device and on the total reverse recovery charge of the low side MOSFET. Since the relative switching speed is higher for the GaN MOSFET under identical external parameters, higher I_{rrm} even with identical reverse recovery charge Q_{rr} is expected for the GaN MOSFET. However, based on GaN's datasheets (Transphorm Inc., 2017), its Q_{rr} is about 136 nC at 400V with a forward diode's current of 22A and a current slope of 1000A/μs. Similarly, SiC's datasheet (Rohm Semiconductor, 2017) specify a reverse recovery charge of only 55nC at a decreased voltage and forward current of respectively 300V and 13A. Also, the current slope is specified at 1100A/μs, which again complicates the comparison between GaNs and SiCs. Moreover, for those specific applications as defined in datasheets (Rohm Semiconductor, 2017; Transphorm Inc., 2017), the reverse recovery time t_{rr} is 15 ns for the SiC MOSFET and 40 ns for the GaN MOSFET. Total reverse recovery charge and time are highly dependent on the conduction current of the parasitic diode, and data on Q_{rr} from datasheets are specified at very different configurations which doesn't allow a direct comparison of Q_{rr} between GaNs and SiCs under study.

Based on experimental observations and relative comparisons between GaNs and SiCs as showed by Tables 5.6 and 5.7, the selected GaN MOSFETs exhibit a relevant faster switching speed as

demonstrated by the maximum positive HS-EC dI_F/dt for a relative average value of 1.9 pu with a standard deviation of 0.4 pu. Consequently, this results in an average maximum reverse recovery current of 1.6 pu for the GaN MOSFETs. Based on experimental results, determining if there is a major difference in the total Q_{rr} under equivalent experimental configuration between the chosen SiCs and GaNs is not possible with certainty. However, based on conducted experiments, the faster slew rate of GaNs is clearly not an advantage since the intrinsic parameters of the parasitic diode and the higher I_{rrm} caused by faster switching speed result in a rougher blocking phase of the parasitic diode with a relative slew rate (dI_R/dt) in average of 3.3 pu with a standard deviation of 1 pu. This very high maximum negative current slope (di_R/dt) of the GaN MOSFET results in very high surge voltage and voltage slope in the commutation loop as the fast current slope reacts and resonate with the parasitic inductances and capacitances. Then, in Table 5.7 an average maximum surge voltage of 1.58 pu with a standard deviation of 0.21 pu is observed with the GaN MOSFETs in comparison to the SiC MOSFETs. In addition, the positive and negative voltage slopes (LS-v_{ds} (dv_{ds}/dt)) are also higher with the GaN MOSFET, on average between 1.74 to 3 pu. This higher ruggedness of the GaN MOSFETs results in an extended turn-on interval with an increased duration before the resonance dissipates. In addition, this results in higher risk of perturbations on gate circuits due to the presence of higher surge voltage and voltage slope during the blocking phase of the reverse recovery process. On another side, the lower Miller capacitance (C_{gd}) of the GaN MOSFET in addition to its capacitances ratio (C_{gs}/C_{gd}) makes it less susceptible to parasitic perturbations on the gate circuit under the same voltage slope and surge voltage compared to the SiC MOSFET (Transphorm Inc., 2017; Rohm Semiconductor, 2017). However, experimental observations with Si MOSFET as presented in chapter 4 clearly demonstrate the higher importance of slew rate and reverse recovery ruggedness on gate perturbations compared to favorable capacitance ratio.

Then, turn-off losses, time and maximum high side current slope during turn-off phase have been observed and compared for all experimentations. In average, turn-off losses and duration tend to show increased value of respectively 1.21 pu and 1.39 pu. However, the standard deviation for both values are of 0.20 pu and 0.41 pu, showing that the difference in the turn-off switching

process is similar between GaN and SiC under study. In addition, an average relative maximum current slope of 0.71 pu with a standard deviation of 0.15 pu is observed for GaN MOSFETs during turn-off, confirming the slightly slower turn-off process of the GaN MOSFET under identical external configuration. Based on their respective datasheets (Rohm Semiconductor, 2017; Transphorm Inc., 2017), SiC input capacitance (C_{iss}) is about 2 times smaller in comparison to the GaN MOSFET which is highly representative of the gate-source capacitance (C_{gs}). Even if the driving voltage of the SiC MOSFET is higher, it still takes more time to completely discharge the gate-source capacitance of the GaN MOSFET. Then, experimental measurements result in expected behavior, showing convincing faster turn-off process for the SiC MOSFET.

At last, similar conduction losses between GaN and SiC MOSFETs were expected based on similar $R_{ds(on)}$ from datasheets (Rohm Semiconductor, 2017; Transphorm Inc., 2017). In Table 5.7, results comply with expectations, showing a relative comparison of 1.24 pu with a standard deviation of 0.32 pu between GaN and SiC MOSFETs. This minor difference tends to advantage SiC MOSFETs for conduction losses. However, it would have been even more interesting to observe conduction losses at increased temperature, since SiC MOSFETs normally exhibit a mild increase of the $R_{ds(on)}$ between 0°C and 75°C in comparison to GaN MOSFETs. Based on experimental observations, there is not enough evidence to determine if higher conduction losses should be expected with GaN MOSFETs compared to SiC.

All considered, experimental observations between the SiC MOSFET and GaN MOSFET under study show advantages and inconvenient for each technologies. GaN seems to exhibit faster switching speed, but increased perturbations in the commutation due to higher ruggedness, and potentially higher reverse recovery charge. So, this may lead to lower turn-on losses, but with higher EMI issues, snubber requirements, and gate perturbations. Actually, where GaN MOSFETs show weaknesses, SiC exhibit forces as reverse recovery softness, possibly lower EMI issues, and less chance of gate perturbations. For sure, both technologies have a lot to offer in comparison to standard Si MOSFET and future development of all WBG technologies will bring even more possibilities. Since GaN MOSFETs are exclusively cascade device under typical power package like TO-247-3, they don't exhibit the major interest in using GaN technologies;

the absence of reverse recovery charge and current while still allowing reverse conduction. For now, it seems like a safer bet to proceed with SiC MOSFETs under higher power requirements, and further analysis between high voltage and power lateral GaN MOSFETs and SiC MOSFETs would be required to have a complete comparison between both technologies.

5.3 Recommendations Based On Relative Experimental Comparison Between Si, SiC and GaN MOSFETs

Experimental relative observations between WBG and Si MOSFETs under study show major difference in the switching process. WBG devices might be less mature, but major improvement in switching performances with reduce losses and duration have been presented in comparison to Si MOSFETs. However, faster switching speed of both SiC and GaN have to be assessed to results in acceptable electromagnetic perturbations during the switching process. Although GaN MOSFETs might exhibit even lower switching losses compared with SiC MOSFETs, it shows the most EMI issues with a limited availability as high voltage and power MOSFETs. Further development of lateral GaN MOSFETs as high voltage device under power package might results in a game changer for high voltage and power converters applications due to the absence in the reverse recovery current. For now, SiC MOSFETs allow very low switching losses while undergoing a very smooth switching process under an adequate gate configuration. Based on experimental comparison between all technologies, SiC MOSFETs bring the advantages of a faster switching device with fewer losses while only resulting in mild perturbations from it, which makes it the most suited high voltage WBG MOSFET for now.

CONCLUSION AND RECOMMENDATIONS

WBG semiconductors showed promising results compared to standard Si MOSFETS. They are offering the best compromise between switching speed, reduced losses and EMI issues. Under the analyzed computational and experimental study, SiC step out as the best-suited technology for energy conversion applications. Still, GaNs are interesting for their high switching speed, but their lack of technological maturity makes them a secondary choice for power applications at the time that we wrote this document. GaN's claimed benefit of the absence of reverse recovery current cannot be experimented with the TO-247 power package for now since those are formed from a GaN-Si cascade configuration. The development of lateral GaN MOSFETs as high voltage devices under power packages can be a game-changer for power converters applications. Although this study only presents the results of one technology for each MOSFET type, interpretation of measurements and statistical analysis of multiple experimental configurations revealed clear behavioral tendencies for all MOSFET technologies. In general, both GaN and SiC MOSFETs offer reduced switching and conduction losses in comparison to Si MOSFETs. In addition, WBG MOSFET's reduced internal capacitances make them suited for faster switching application whilst undergoing less susceptibility to parasitic turn-on.

Carrying out experimental studies is an art. The slightest misstep, whether with the measurement, the development of the board, or even the synchronization of the measurements can lead to erroneous results. Whether this translates into a simple zero and degausses procedure or complex attention to device's internal characteristics and board layout, any single action toward reduction in mutual interference brings contribution for more reliable measurements. In general, a direct contact as for most voltage probes with experimental configurations will induce parasitic components perturbing the normal experimental behavior and other measurements. Also, any unnecessary increase in the measurement surface can increase mutual coupling and reduce the precision of measurements, especially for fast switching applications. Inversely, contactless current measurements have less impact on the switching process and are more stable under

harsh conditions. Thus, it is preferable to minimize the number of probes on the experimental board to essential measurements without shared connection points. It brings results as close as possible to experimental observations under unperturbed conditions, even if this is never perfectly attainable.

Most converter designs focus on the ratio of output power to input power to estimate switching losses and naturally do not offer complete switching current measurement methods neither a complete analysis of the switching process. Thus, there was a need for the development of a current extraction methodology to compare the switching behavior between MOSFET's technology under study, not just losses. At first, contactless magnetic field measurements seemed like the best approach to minimize perturbations on the switching process. However, this methodology turns out to be too sensitive to the surrounding magnetic field, making it impossible to recover a precise measurement of the switching current. In contrast, the lead current methodology showed acceptable perturbations on the switching process, making it a suitable solution for losses computation and comparison. Both the source and drain lead methodology turn out to provide respective advantages that can be used accordingly to perform experimental measurements. Still, improvement of this methodology could be done using a Kelvin connection or its initial integration on the switching board without any contact with either the high or low side MOSFET. A small deviation in PCB traces would isolate the switching trace for non-contact current measurement while having only a minor effect on the switching process. In the objective to bring relevant conclusions for each technology under-study, considering the MOSFETs as a whole entity turns out to bring more logical results due to large disparities in internal gate resistances between technologies.

The computational results, in good agreement with the experimental results, showed reduced losses and a faster switching process with WBG MOSFETs, favoring SiCs. However, conducting the experimental analysis is required to observe EMI issues, maximum surge voltage limits,

and susceptibility to parasitic turn-on. The proposed modeling approach from (Clemente *et al.*, 1982) offers a realistic computational model with known assumptions. This model allowed to compare MOSFETs of different technologies based only on internal characteristics from the equivalent model. Surely, a more complete methodology considering the variability of MOSFET's internal characteristics might have resulted in a better approximation. However, uncertainty from experimental parameters as the unclamped inductance, measurement accuracy, and probe perturbations might highly overcompensate the benefits from a precise computational model.

All considered, experimental development should be adapted as a consequence of the choice of the MOSFET meeting the application criteria to optimize the final design. Due to its internal characteristics, low-temperature dependence, availability, and maturity, SiCs are currently better suited for energy conversion applications. Consequently, there is no doubt that WBGs will play a key role in the development of electric vehicles of the future, but SiCs will most likely be at the forefront of GaNs for power applications. Further study to characterize each available WBG semiconductors for parallelism methods, gate slope control and off-state current could be relevant topics to optimize future developments with WBG technologies.

APPENDIX I

TURN-ON INTERVAL 1: COMPLETE MATHEMATICAL ANALYSIS

Development of the complete mathematical equations (without neglecting Ls) for the first turn-on interval.

$$\mathscr{L}\{f(t)\} = (L_s C_{iss})\left[s^2 v_{gs}(s) - s v_{gs}(0) - v'_{gs}(0)\right] + (RC_{iss})\left[s v_{gs}(s) - v_{gs}(0)\right] + v_{gs}(s) - \frac{V_{GH}}{s} = 0$$

With initial conditions stated as follow:

$$\begin{cases} v_{gs}(0) = V_{GL} \\ v'_{gs}(0) = 0 \end{cases}$$

One obtain,

$$v_{gs}(s)[L_s C_{iss} s^2 + RC_{iss} s + 1] = \frac{L_s C_{iss} V_{GL} s^2 + RC_{iss} V_{GL} s + V_{GH}}{s}$$

$$v_{gs}(s) = \frac{L_s C_{iss} V_{GL} s^2 + RC_{iss} V_{GL} s + V_{GH}}{s(L_s C_{iss} s^2 + RC_{iss} s + 1)}$$

With factorization,

$$v_{gs}(s) = \frac{V_{GL} s^2 + \frac{R}{L_s} V_{GL} s + \frac{V_{GH}}{L_s C_{iss}}}{s\left(s + \frac{RC_{iss} + \sqrt{R^2 C_{iss}^2 - 4L_s C_{iss}}}{2L_s C_{iss}}\right)\left(s + \frac{RC_{iss} - \sqrt{R^2 C_{iss}^2 - 4L_s C_{iss}}}{2L_s C_{iss}}\right)}$$

By abbreviating last relation with,

$$\begin{cases} s+a = s + \frac{RC_{iss}+\sqrt{R^2C_{iss}^2-4L_sC_{iss}}}{2L_sC_{iss}} \\ s+b = s + \frac{RC_{iss}-\sqrt{R^2C_{iss}^2-4L_sC_{iss}}}{2L_sC_{iss}} \end{cases}$$

It gives,

$$v_{gs}(s) = \frac{V_{GL}s^2 + \frac{R}{L_s}V_{GL}s + \frac{V_{GH}}{L_sC_{iss}}}{s(s+a)(s+b)} = \frac{k_1}{s} + \frac{k_2}{s+a} + \frac{k_3}{s+b} \qquad \text{(A I-1)}$$

$$V_{GL}s^2 + \frac{R}{L_s}V_{GL}s + \frac{V_{GH}}{L_sC_{iss}} = k_1(s+a)(s+b) + k_2s(s+b) + k_3s(s+a)$$

By solving terms by terms,

$$k_1 + k_2 + k_3 = V_{GL}$$
$$k_1(a+b) + k_2b + k_3a = \frac{R}{L_s}V_{GL}$$
$$k_1ab = \frac{V_{GH}}{L_sC_{iss}}$$

With,

$$a \cdot b = \left(\frac{RC_{iss} + \sqrt{R^2C_{iss}^2 - 4L_sC_{iss}}}{2L_sC_{iss}}\right)\left(\frac{RC_{iss} - \sqrt{R^2C_{iss}^2 - 4L_sC_{iss}}}{2L_sC_{iss}}\right) = \frac{1}{L_sC_{iss}}$$

$$\left[k_1 = \frac{V_{GH}}{L_sC_{iss}ab} = \frac{\frac{V_{GH}}{L_sC_{iss}}}{\left(\frac{RC_{iss}+\sqrt{R^2C_{iss}^2-4L_sC_{iss}}}{2L_sC_{iss}}\right)\left(\frac{RC_{iss}-\sqrt{R^2C_{iss}^2-4L_sC_{iss}}}{2L_sC_{iss}}\right)} = V_{GH}\right] \qquad \text{(A I-2)}$$

Then,

$$k_2 = \frac{R}{bL_s}V_{GL} - \frac{k_1}{b}(a+b) - \frac{k_3 a}{b}$$

With,

$$a+b = \left(\frac{RC_{iss} + \sqrt{R^2C_{iss}^2 - 4L_sC_{iss}}}{2L_sC_{iss}}\right) + \left(\frac{RC_{iss} - \sqrt{R^2C_{iss}^2 - 4L_sC_{iss}}}{2L_sC_{iss}}\right) = \frac{R}{L_s}$$

$$k_2 = \frac{R}{bL_s}V_{GL} - \frac{RV_{GH}}{bL_s} - \frac{k_3 a}{b}$$

$$k_2 = \frac{R(V_{GL} - V_{GH})}{\left(\frac{RC_{iss} - \sqrt{R^2C_{iss}^2 - 4L_sC_{iss}}}{2L_sC_{iss}}\right)L_s} - \frac{k_3 L_s \left(\frac{RC_{iss} + \sqrt{R^2C_{iss}^2 - 4L_sC_{iss}}}{2L_sC_{iss}}\right)}{\left(\frac{RC_{iss} - \sqrt{R^2C_{iss}^2 - 4L_sC_{iss}}}{2L_sC_{iss}}\right)L_s}$$

$$k_2 = \frac{R(V_{GL} - V_{GH}) - k_3 L_s \left(\frac{RC_{iss} + \sqrt{R^2C_{iss}^2 - 4L_sC_{iss}}}{2L_sC_{iss}}\right)}{\left(\frac{RC_{iss} - \sqrt{R^2C_{iss}^2 - 4L_sC_{iss}}}{2L_sC_{iss}}\right)L_s}$$

Finally,

$$k_3 + k_2 = V_{GL} - k_1$$

$$k_3 - k_3\left(\frac{RC_{iss} + \sqrt{R^2C_{iss}^2 - 4L_sC_{iss}}}{2L_sC_{iss}}\right) + \frac{R}{L_s}(V_{GL} - V_{GH}) = V_{GL} - V_{GH}$$

$$k_3 - k_3 a = (V_{GL} - V_{GH})\left(1 - \frac{R}{L_s}\right)$$

$$k_3\left(1-\frac{RC_{iss}+\sqrt{R^2C_{iss}^2-4L_sC_{iss}}}{2L_sC_{iss}}\right)=(V_{GL}-V_{GH})\left(1-\frac{R}{L_s}\right)$$

$$k_3=\frac{(V_{GL}-V_{GH})\left(1-\frac{R}{L_s}\right)}{\left(1-\frac{RC_{iss}+\sqrt{R^2C_{iss}^2-4L_sC_{iss}}}{2L_sC_{iss}}\right)}$$

$$k_3=\frac{(V_{GL}-V_{GH})\left(1-\frac{R}{L_s}\right)}{\left(\frac{RC_{iss}+\sqrt{R^2C_{iss}^2-4L_sC_{iss}}}{2L_sC_{iss}}\right)\left(\frac{2L_sC_{iss}}{RC_{iss}+\sqrt{R^2C_{iss}^2-4L_sC_{iss}}}-1\right)}$$

$$\left[k_3=\frac{(V_{GL}-V_{GH})-(RC_{iss}+\sqrt{R^2C_{iss}^2-4L_sC_{iss}})}{2\sqrt{R^2C_{iss}^2-4L_sC_{iss}}}=\frac{(V_{GL}-V_{GH})-(\tau_g+\sqrt{\tau_g^2-4L_sC_{iss}})}{2\sqrt{\tau_g^2-4L_sC_{iss}}}\right] \quad \text{(A I-3)}$$

With k_3 in k_2, one get,

$$k_2=\frac{R(V_{GL}-V_{GH})-L_s\frac{(V_{GL}-V_{GH})(1-R/L_s)}{\left(\frac{RC_{iss}+\sqrt{R^2C_{iss}^2-4L_sC_{iss}}}{2L_sC_{iss}}\right)\left(\frac{2L_sC_{iss}}{RC_{iss}+\sqrt{R^2C_{iss}^2-4L_sC_{iss}}}-1\right)}\left(\frac{RC_{iss}+\sqrt{R^2C_{iss}^2-4L_sC_{iss}}}{2L_sC_{iss}}\right)}{\left(\frac{RC_{iss}-\sqrt{R^2C_{iss}^2-4L_sC_{iss}}}{2L_sC_{iss}}\right)L_s}$$

$$k_2=\frac{R(V_{GL}-V_{GH})}{\left(\frac{RC_{iss}-\sqrt{R^2C_{iss}^2-4L_sC_{iss}}}{2L_sC_{iss}}\right)L_s}-L_s\frac{(V_{GL}-V_{GH})(1-R/L_s)}{\left(\frac{2L_sC_{iss}}{RC_{iss}+\sqrt{R^2C_{iss}^2-4L_sC_{iss}}}-1\right)\left(\frac{RC_{iss}-\sqrt{R^2C_{iss}^2-4L_sC_{iss}}}{2L_sC_{iss}}\right)L_s}$$

$$k_2 = \frac{R(V_{GL} - V_{GH})}{\left(\frac{RC_{iss} - \sqrt{R^2C_{iss}^2 - 4L_sC_{iss}}}{2L_sC_{iss}}\right)L_s} - \frac{(V_{GL} - V_{GH})(1 - R/L_s)}{\left(\frac{RC_{iss} - \sqrt{R^2C_{iss}^2 - 4L_sC_{iss}}}{RC_{iss} + \sqrt{R^2C_{iss}^2 - 4L_sC_{iss}}} - \frac{RC_{iss} - \sqrt{R^2C_{iss}^2 - 4L_sC_{iss}}}{2L_sC_{iss}}\right)}$$

$$k_2 = \frac{R(V_{GL} - V_{GH})}{\left(\frac{RC_{iss} - \sqrt{R^2C_{iss}^2 - 4L_sC_{iss}}}{2C_{iss}}\right)} - \frac{(V_{GL} - V_{GH})(1 - R/L_s)}{\left(\frac{2L_sC_{iss}\left(RC_{iss} - \sqrt{R^2C_{iss}^2 - 4L_sC_{iss}}\right) - \left(RC_{iss} - \sqrt{R^2C_{iss}^2 - 4L_sC_{iss}}\right)\left(RC_{iss} + \sqrt{R^2C_{iss}^2 - 4L_sC_{iss}}\right)}{2L_sC_{iss}\left(RC_{iss} - \sqrt{R^2C_{iss}^2 - 4L_sC_{iss}}\right)}\right)}$$

$$k_2 = \frac{R(V_{GL} - V_{GH})(2C_{iss})}{\left(RC_{iss} - \sqrt{R^2C_{iss}^2 - 4L_sC_{iss}}\right)} - \frac{(V_{GL} - V_{GH})(1 - R/L_s)\left(2L_sC_{iss}\left(RC_{iss} + \sqrt{R^2C_{iss}^2 - 4L_sC_{iss}}\right)\right)}{\left(2L_sC_{iss}\left(RC_{iss} - \sqrt{R^2C_{iss}^2 - 4L_sC_{iss}}\right) - \left(RC_{iss} - \sqrt{R^2C_{iss}^2 - 4L_sC_{iss}}\right)\left(RC_{iss} + \sqrt{R^2C_{iss}^2 - 4L_sC_{iss}}\right)\right)}$$

$$\left[k_2 = \frac{(V_{GH} - V_{GL})\left(RC_{iss} - \sqrt{R^2C_{iss}^2 - 4L_sC_{iss}}\right)}{2\sqrt{R^2C_{iss}^2 - 4L_sC_{iss}}} = \frac{(V_{GH} - V_{GL})\left(\tau_g - \sqrt{\tau_g^2 - 4L_sC_{iss}}\right)}{2\sqrt{\tau_g^2 - 4L_sC_{iss}}}\right] \quad \text{(A I-4)}$$

Then, the expression of $v_{gs}(s)$ (I) becomes,

$$v_{gs}(s) = \frac{V_{GH}}{s} + \frac{\frac{(V_{GH} - V_{GL})\left(\tau_g - \sqrt{\tau_g^2 - 4L_sC_{iss}}\right)}{2\sqrt{\tau_g^2 - 4L_sC_{iss}}}}{s + \frac{\tau_g + \sqrt{\tau_g^2 - 4L_sC_{iss}}}{2L_sC_{iss}}} + \frac{\frac{(V_{GL} - V_{GH})\left(\tau_g + \sqrt{\tau_g^2 - 4L_sC_{iss}}\right)}{2\sqrt{\tau_g^2 - 4L_sC_{iss}}}}{s + \frac{\tau_g - \sqrt{\tau_g^2 - 4L_sC_{iss}}}{2L_sC_{iss}}}$$

With the inverse Laplace, one get the following final temporal expression of v_{gs} for the first turn-on interval without neglecting the common source inductance,

$$\mathscr{L}^{-1}\{v_{gs}(s)\} = v_{gs}(t) = V_{GH} + \left(\frac{(V_{GH} - V_{GL})\left(\tau_g - \sqrt{\tau_g^2 - 4L_sC_{iss}}\right)}{2\sqrt{\tau_g^2 - 4L_sC_{iss}}}\right) e^{-\left(\frac{\tau_g + \sqrt{\tau_g^2 - 4L_sC_{iss}}}{2L_sC_{iss}}\right)t} + \left(\frac{(V_{GL} - V_{GH})\left(\tau_g + \sqrt{\tau_g^2 - 4L_sC_{iss}}\right)}{2\sqrt{\tau_g^2 - 4L_sC_{iss}}}\right) e^{-\left(\frac{\tau_g - \sqrt{\tau_g^2 - 4L_sC_{iss}}}{2L_sC_{iss}}\right)t} \quad \text{(A I-5)}$$

APPENDIX II

MOSFET'S TEMPERATURE DEPENDENCY

Table-A II-1 Influence of Increasing the Temperature from 25°C to 75°C on MOSFET's $R_{ds(on)}$ and $V_{gs(th)}$ Depending on Voltage and Current Rating, Package and Technology

$V_{(BR)DSS}$	I_D @ 25°C	Technology	Package	$\Delta R_{ds(on)}$	$\Delta V_{gs(th)}$	Manufacturer & Part Number
200 V	15 A	Si	DPAK (TO-252-3)	+45%	-10%	STMicroelectronics STB19NF20
200 V	16 A	Si	DPAK (TO-252-3)	+45%	-	ON Semiconductor FDD18N20LZ
200 V	16 A	Si	DPAK (TO-252-3)	+50%	-10%	ROHM Semiconductor RCJ160N20TL
200 V	17 A	Si	DPAK (TO-252-3)	+45%	-	Infineon Technologies IRFR15N20DTRPBF
200 V	18 A	Si	DPAK (TO-252-3)	+30%	-15%	STMicroelectronics STD25NF20
200 V	18 A	Si	DPAK (TO-252-3)	+45%	-	Vishay Siliconix IRF640STRLPBF
200 V	18 A	Si	DPAK (TO-252-3)	+50%	-	Infineon Technologies IRF640NSTRLPBF
200 V	19 A	Si	DPAK (TO-252-3)	+50%	-	ON Semiconductor FQB19N20C
200 V	19 A	Si	DPAK (TO-252-3)	+50%	-	Vishay Siliconix SUD19N20-90-E3
200 V	20 A	Si	DPAK (TO-252-3)	+50%	-10%	ROHM Semiconductor RCJ200N20TL
200 V	5 A	GaN	DIE (4-solder bar)	+35%	-1%	EPC EPC2012C
200 V	8.5 A	GaN	DIE (BUMPED DIE)	+35%	-1%	EPC EPC2019
200 V	22 A	GaN	DIE (7-solder bar)	+35%	-1%	EPC EPC2010C

$V_{(BR)DSS}$	I_D @ 25°C	Technology	Package	$\Delta R_{ds(on)}$	$\Delta V_{gs(th)}$	Manufacturer & Part Number
200 V	48 A	GaN	DIE (BUMPED DIE)	+35%	-5%	EPC EPC2034C
200 V	48 A	GaN	DIE (BUMPED DIE)	+40%	-5%	EPC EPC2034
650 V	16 A	GaN	TO-220-3	+35%	-	Transphorm TPH3206PSB
650 V	20 A	GaN	TO-220-3	+35%	-	Transphorm TPH3208PS
650 V	24 A	Si	TO-220-3	+45%	-	Infineon Technologies IPP65R095C7XKSA1
650 V	24 A	Si	TO-220-3	+55%	-12%	IXYS IXFP22N65X2
650 V	24 A	Si	TO-220-3	+50%	-	ON Semiconductor FCP125N65S3R0
650 V	24 A	Si	TO-220-3	+50%	-12%	STMicroelectronics STP33N65M2
650 V	24 A	Si	TO-220-3	+50%	-	Vishay Siliconix SIHP24N65E-E3
650 V	25 A	Si	TO-220-3	+55%	-	Alpha & Omega AOT25S65L
650 V	29 A	SiC	TO-220-3	+10%	-15%	ROHM Semiconductor SCT2120AF
650 V	35 A	GaN	TO-247-3	+35%	-	Transphorm TPH3205WSBQA
650 V	36 A	GaN	TO-247-3	+35%	-	Transphorm TP65H050WS
650 V	46.5 A	GaN	TO-247-3	+35%	-	Transphorm TP65H035WS
650 V	47.2 A	GaN	TO-247-3	+35%	-	Transphorm TP65H035WSQA
650 V	43.3 A	Si	TO-247-3	+45%	-	Infineon Technologies IPW60R080CFDA

$V_{(BR)DSS}$	I_D @ 25°C	Technology	Package	$\Delta R_{ds(on)}$	$\Delta V_{gs(th)}$	Manufacturer & Part Number
650 V	34 A	Si	TO-247-3	+55%	-13%	IXYS IXTH34N65X2
650 V	35 A	Si	TO-247-3	+45%	-12%	Toshiba TK35N65WS1F
650 V	36 A	Si	TO-247-3	+40%	-	ON Semiconductor NTHL095N65S3HF
650 V	42 A	Si	TO-247-3	+50%	-10%	STMicroelectronics STWA57N65M5
650 V	46 A	Si	TO-247-3	+50%	-	Vishay Siliconix SIHG44N65EF-GE3
650 V	47 A	Si	TO-247-3	+50%	-11%	Microsemi APT47N65BC3G
650 V	47 A	Si	TO-247-3	+50%	-10%	ROHM Semiconductor R6547KNZ4C13
650 V	21 A	SiC	TO-247-3	+5%	-8%	ROHM Semiconductor SCT3120ALHRC11
650 V	30 A	SiC	TO-247-3	+5%	-8%	ROHM Semiconductor SCT3080ALHRC11
650 V	39 A	SiC	TO-247-3	+5%	-10%	ROHM Semiconductor SCT3060ALHRC11
650 V	119 A	SiC	TO-247-3	+7%	-12%	STMicroelectronics SCTW90N65G2V
650 V	31 A	Si	TO-247-3	+40%	-	Infineon Technologies IPW60R070CFD7XKSA1
900 V	15 A	GaN	TO-220-3	+30%	-	Transphorm TP90H180PS
900 V	11 A	Si	TO-220-3	+50%	-	Infineon Technologies IPA90R500C3XKSA1
900 V	11.4 A	Si	TO-3P-3	+50%	-	ON Semiconductor FQA11N90-F109
900 V	12 A	Si	TO-247-3	+50%	-	IXYS IXFH12N90P

$V_{(BR)DSS}$	I_D @ 25°C	Technology	Package	$\Delta R_{ds(on)}$	$\Delta V_{gs(th)}$	Manufacturer & Part Number
900 V	15 A	Si	TO-247-3	+45%	-14%	STMicroelectronics STW15NK90Z
900 V	11.5 A	SiC	TO-247-3	+10%	-10%	Cree/Wolfspeed E3M0280090D
900 V	22 A	SiC	TO-263-7	+10%	-13%	Cree/Wolfspeed C3M0120090J

APPENDIX III

RAW DATA OF EXPERIMENTAL RESULTS

This section presents all the experimental results of the Si MOSFET (IPW65R080FDA), SiC MOSFET (SCR3060ALHR) and GaN MOSFET (TPH3205WSBQA) under study.

Table-A III-1 Si MOSFET (IPW65R080FDA) Experimental Results

Established Measurement Points	50V Supply				100V Supply			
	$R_{G(on)}$ = 22Ω		$R_{G(on)}$ = 10Ω		$R_{G(on)}$ = 22Ω		$R_{G(on)}$ = 10Ω	
	Drain Method	Source Method	Drain Method	Source Method	Drain Method	Source Method	Drain Method	Source Method
Turn-on losses (1st peak) (μJ)	14.3	12.5	9.9	9.2	-	-	35.2	-
Turn-on duration (1st peak) (ns)	78	74	62	60	-	-	53.2	-
Turn-on losses (Slope Stabilized) (μJ)	16.5	17.0	10.8	12.3	-	-	45.3	-
Turn-on duration (Slope Stabilized) (ns)	314	336	441	238	-	-	277	-
Turn-on losses (v_{gs} Final & Slope Stabilized) (μJ)	17.7	18.3	11.1	13.2	-	-	46.5	-
Turn-on duration (v_{gs} Final & Slope Stabilized) (ns)	1953	2136	913	645	-	-	1023	-
Maximum Positive HS-EC (dI_F/dt) (A/μs)	306	293	409	382	-	-	782	-
Maximum Negative HS-EC (dI_R/dt) (A/μs)	-1900	-1068	-2578	-1344	-	-	-3961	-
Maximum HS-EC Value (A)	15.5	14.5	17.8	16.2	-	-	29.6	-
Maximum Positive LS-v_{ds} (dv_{ds}/dt) (V/ns)	12.7	12.0	19.3	17.2	-	-	43.2	-
Maximum Negative LS-v_{ds} (dv_{ds}/dt) (V/ns)	-16.4	-25.0	-22.7	-36.3	-	-	-33.5	-
Maximum LS-v_{ds} Value (V)	136	128	162	163	-	-	266	-
LS-v_{ds} Resonant Frequency (MHz)	16.4	22.7	18.1	23.0	-	-	39.1	-
Turn-off losses (μJ)	3.9	7.5	3.7	7.3	-	-	8.1	-
Turn-off duration (ns)	324	344	308	326	-	-	217	-
Maximum Turn-off HS-EC (dI/dt) (A/μs)	-17.9	-24.1	-21.4	-26.3	-	-	-235	-
Conduction losses (10 μs) (μJ)	13.8	13.7	12.2	34.4	-	-	52.4	-

Table-A III-2 SiC MOSFET (SCR3060ALHR) Experimental Results

Established Measurement Points	50V Supply				100V Supply			
	$R_{G(on)}$ = 22Ω		$R_{G(on)}$ = 10Ω		$R_{G(on)}$ = 22Ω		$R_{G(on)}$ = 10Ω	
	Drain Method	Source Method	Drain Method	Source Method	Drain Method	Source Method	Drain Method	Source Method
Turn-on losses (1st peak) (μJ)	1.5	1.3	1.3	0.8	7.8	6.8	6.1	5.1
Turn-on duration (1st peak) (ns)	32	31	28	26	35	33	31	30
Turn-on losses (Slope Stabilized) (μJ)	1.6	1.3	1.4	0.8	8.4	7.5	6.2	5.2
Turn-on duration (Slope Stabilized) (ns)	217	78	126	62	95	63	93	69
Turn-on losses (v_{gs} Final & Slope Stabilized) (μJ)	1.6	1.4	1.4	0.8	8.4	8.0	6.2	5.2
Turn-on duration (v_{gs} Final & Slope Stabilized) (ns)	295	232	177	205	270	248	137	196
Maximum Positive HS-EC (dI_F/dt) (A/μs)	325	294	395	369	457	441	597	534
Maximum Negative HS-EC (dI_R/dt) (A/μs)	-438	-323	-536	-351	-457	-353	-643	-365
Maximum HS-EC Value (A)	5.0	4.1	5.5	4.6	8.0	6.8	8.9	7.4
Maximum Positive LS-v_{ds} (dv_{ds}/dt) (V/ns)	4.8	6.1	5.3	8.0	7.6	9.9	9.2	14.0
Maximum Negative LS-v_{ds} (dv_{ds}/dt) (V/ns)	-4.5	-4.2	-5.3	-6.5	-4.5	-4.1	-7.2	-9.7
Maximum LS-v_{ds} Value (V)	68	68	76	81	112	107	131	133
LS-v_{ds} Resonant Frequency (MHz)	38.5	42.4	37.9	45.5	43.1	51.0	42.4	59.5
Turn-off losses (μJ)	0.8	1.0	0.7	1.0	2.3	2.7	2.6	2.8
Turn-off duration (ns)	38	45	37	41	35	50	38	38
Maximum Turn-off HS-EC (dI/dt) (A/μs)	-118	-86	-97	-76	-179	-155	-215	-144
Conduction losses (10 μs) (μJ)	10.9	9.2	9.6	10.9	39.4	61.8	37.0	43.0

Table-A III-3 GaN MOSFET (TPH3205WSBQA) Experimental Results

Established Measurement Points	50V Supply				100V Supply			
	$R_{G(on)}$ = 22Ω		$R_{G(on)}$ = 10Ω		$R_{G(on)}$ = 22Ω		$R_{G(on)}$ = 10Ω	
	Drain Method	Source Method	Drain Method	Source Method	Drain Method	Source Method	Drain Method	Source Method
Turn-on losses (1st peak) (μJ)	0.8	0.7	0.5	0.3	1.9	2.2	1.9	2.3
Turn-on duration (1st peak) (ns)	26	28	25	26	30	27	17	25
Turn-on losses (Slope Stabilized) (μJ)	1.4	0.7	1.5	0.3	5.9	2.6	13.5	3.7
Turn-on duration (Slope Stabilized) (ns)	297	178	372	138	1095	164	974	143
Turn-on losses (v_{gs} Final & Slope Stabilized) (μJ)	1.5	0.8	1.8	0.4	6.1	2.9	14.9	3.9
Turn-on duration (v_{gs} Final & Slope Stabilized) (ns)	370	290	813	250	1875	337	1502	249
Maximum Positive HS-EC (dI_F/dt) (A/μs)	528	504	573	571	1136	1061	1200	1127
Maximum Negative HS-EC (dI_R/dt) (A/μs)	-1039	-874	-1111	-942	-1950	-1616	-2110	-1640
Maximum HS-EC Value (A)	8.0	7.3	8.4	7.7	13.5	12.2	13.8	12.6
Maximum Positive LS-v_{ds} (dv_{ds}/dt) (V/ns)	8.6	8.2	9.0	8.0	19.9	18.8	20.2	19.2
Maximum Negative LS-v_{ds} (dv_{ds}/dt) (V/ns)	-9.6	-8.7	-10.0	-8.6	-22.5	-21.7	-25.9	-23.5
Maximum LS-v_{ds} Value (V)	106	101	108	102	207	202	220	205
LS-v_{ds} Resonant Frequency (MHz)	24.8	26.6	25.0	26.9	32.1	34.7	32.1	34.7
Turn-off losses (μJ)	1.0	1.2	1.1	1.2	3.1	3.0	2.6	2.6
Turn-off duration (ns)	70	70	71	69	41	40	41	41
Maximum Turn-off HS-EC (dI/dt) (A/μs)	-54.2	-53.5	-66.3	-54.0	-140.0	-135.6	-140.0	-141.0
Conduction losses (10 μs) (μJ)	13.8	16.4	14.9	15.5	30.6	48.7	48.4	46.2

APPENDIX IV

RELATIVE EXPERIMENTAL COMPARISON BETWEEN THE SOURCE CURRENT MEASUREMENT AND DRAIN CURRENT MEASUREMENT METHODOLOGIES

Table-A IV-1 Relative Comparison of Si MOSFET's (IPW65R080FDA) Experimental Results with Drain Methodology to its relative Source Methodology Referenced on Source Methodology's Results (pu)

Established Measurement Points	50V Supply		100V Supply		Mean	Median	Standard Deviation
	$R_{G(on)}$ 22Ω	$R_{G(on)}$ 10Ω	$R_{G(on)}$ 22Ω	$R_{G(on)}$ 10Ω			
Turn-on losses (1st peak)	1.1	1.1	-	-	1.1	1.1	0.05
Turn-on duration (1st peak)	1.1	1.0	-	-	1.0	1.0	0.01
Turn-on losses (Slope Stabilized)	1.0	0.9	-	-	0.9	0.9	0.06
Turn-on duration (Slope Stabilized)	0.9	1.9	-	-	1.4	1.4	0.7
Turn-on losses (v_{gs} Final & Slope Stabilized)	1.0	0.8	-	-	0.9	0.9	0.09
Turn-on duration (v_{gs} Final & Slope Stabilized)	0.9	1.4	-	-	1.2	1.2	0.4
Maximum Positive HS-EC (dI_F/dt)	1.0	1.1	-	-	1.1	1.1	0.02
Maximum Negative HS-EC (dI_R/dt)	1.8	1.9	-	-	1.8	1.8	0.1
Maximum HS-EC Value	1.1	1.1	-	-	1.1	1.1	0.02
Maximum Positive LS-v_{ds} (dv_{ds}/dt)	1.1	1.1	-	-	1.1	1.1	0.04
Maximum Negative LS-v_{ds} (dv_{ds}/dt)	0.7	0.6	-	-	0.6	0.6	0.02
Maximum LS-v_{ds} Value	1.1	1.0	-	-	1.0	1.0	0.04
LS-v_{ds} Resonant Frequency (ω)	0.7	0.8	-	-	0.8	0.8	0.04
Turn-off losses	0.5	0.5	-	-	0.5	0.5	0.2
Turn-off duration	0.9	0.9	-	-	0.9	0.9	0.002
Maximum Turn-off HS-EC (dI/dt)	0.7	0.8	-	-	0.8	0.8	0.05
Conduction losses (10 μs)	1.0	0.4	-	-	0.7	0.7	0.5

Table-A IV-2 Relative Comparison of SiC MOSFET's (SCR3060ALHR) Experimental Results with Drain Methodology to its relative Source Methodology Referenced on Source Methodology's Results (pu)

Established Measurement Points	50V Supply		100V Supply		Mean	Median	Standard Deviation
	$R_{G(on)}$ 22Ω	$R_{G(on)}$ 10Ω	$R_{G(on)}$ 22Ω	$R_{G(on)}$ 10Ω			
Turn-on losses (1st peak)	1.1	1.5	1.1	1.2	1.2	1.2	0.17
Turn-on duration (1st peak)	1.0	1.1	1.1	1.0	1.1	1.1	0.02
Turn-on losses (Slope Stabilized)	1.2	1.7	1.1	1.2	1.3	1.2	0.28
Turn-on duration (Slope Stabilized)	2.8	2.0	1.5	1.4	1.9	1.8	0.64
Turn-on losses (v_{gs} Final & Slope Stabilized)	1.1	1.7	1.0	1.2	1.2	1.2	0.29
Turn-on duration (v_{gs} Final & Slope Stabilized)	1.3	0.9	1.1	0.7	1.0	1.0	0.25
Maximum Positive HS-EC (dI_F/dt)	1.1	1.1	1.0	1.1	1.1	1.1	0.04
Maximum Negative HS-EC (dI_R/dt)	1.4	1.5	1.3	1.8	1.5	1.4	0.21
Maximum HS-EC Value	1.2	1.2	1.2	1.2	1.2	1.2	0.02
Maximum Positive LS-v_{ds} (dv_{ds}/dt)	0.8	0.7	0.8	0.7	0.7	0.7	0.07
Maximum Negative LS-v_{ds} (dv_{ds}/dt)	1.1	0.8	1.1	0.7	0.9	0.9	0.18
Maximum LS-v_{ds} Value	1.0	0.9	1.0	1.0	1.0	1.0	0.05
LS-v_{ds} Resonant Frequency (ω)	0.9	0.8	0.8	0.7	0.8	0.8	0.08
Turn-off losses	0.8	0.7	0.9	0.9	0.8	0.8	0.10
Turn-off duration	0.8	0.9	0.7	1.0	0.9	0.9	0.13
Maximum Turn-off HS-EC (dI/dt)	1.4	1.3	1.2	1.5	1.3	1.3	0.15
Conduction losses (10 μs)	1.2	0.9	0.6	0.9	0.9	0.9	0.22

Table-A IV-3 Relative Comparison of GaN MOSFET's (TPH3205WSBQA) Experimental Results with Drain Methodology to its relative Source Methodology Referenced on Source Methodology's Results (pu)

Established Measurement Points	50V Supply		100V Supply		Mean	Median	Standard Deviation
	$R_{G(on)}$ 22Ω	$R_{G(on)}$ 10Ω	$R_{G(on)}$ 22Ω	$R_{G(on)}$ 10Ω			
Turn-on losses (1st peak)	1.1	1.6	0.9	0.8	1.1	1.0	0.4
Turn-on duration (1st peak)	0.9	1.0	1.1	0.7	0.9	0.9	0.2
Turn-on losses (Slope Stabilized)	2.0	5.0	2.3	3.7	3.2	3.0	1.3
Turn-on duration (Slope Stabilized)	1.7	2.7	6.7	6.8	4.5	4.7	2.7
Turn-on losses (v_{gs} Final & Slope Stabilized)	1.9	4.8	2.1	3.9	3.2	3.0	1.4
Turn-on duration (v_{gs} Final & Slope Stabilized)	1.3	3.3	5.6	6.0	4.0	4.4	2.2
Maximum Positive HS-EC (dI_F/dt)	1.0	1.0	1.1	1.1	1.0	1.1	0.03
Maximum Negative HS-EC (dI_R/dt)	1.2	1.2	1.2	1.3	1.2	1.2	0.05
Maximum HS-EC Value	1.1	1.1	1.1	1.1	1.1	1.1	0.01
Maximum Positive LS-v_{ds} (dv_{ds}/dt)	1.0	1.1	1.1	1.0	1.1	1.1	0.04
Maximum Negative LS-v_{ds} (dv_{ds}/dt)	1.1	1.2	1.0	1.1	1.1	1.1	0.05
Maximum LS-v_{ds} Value	1.1	1.1	1.0	1.1	1.1	1.1	0.02
LS-v_{ds} Resonant Frequency (ω)	0.9	0.9	0.9	0.9	0.9	0.9	0.004
Turn-off losses	0.9	0.9	1.0	1.0	0.9	0.9	0.1
Turn-off duration	1.0	1.0	1.0	1.0	1.0	1.0	0.02
Maximum Turn-off HS-EC (dI/dt)	1.0	1.2	1.0	1.0	1.1	1.0	0.1
Conduction losses (10 μs)	0.8	1.0	0.6	1.0	0.9	0.9	0.2

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