Modeling and Simulation of High Speed Semiconductors Used in GaN and SiC Power Converters

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FOREWORD

The following manuscript is dedicated to providing an improved modeling technic for wide-bandgap semiconductor. The turn ON/OFF transient periods of the switching are affected not only by the switches' characteristics but also by the diode type and circuits' parasitic elements. Intertwining these effects results in a complicated phenomenon, which is hard to understand and analyze. Although the main concentration of this thesis is on the modeling technics and deriving the mathematical equations to describe the entire switching period, a chapter is dedicated to describe the switching phenomenon without any emphasis on the mathematical equations. The collected results and modelings will pave the way in understanding the transient behavior of the wide-bandgap switches.

Modélisation et simulation des semi-conducteurs haute vitesse utilisés dans les convertisseurs de puissance GaN et SiC

Ali RAHIMI

RÉSUMÉ

En considérant les avantages de l'augmentation de la fréquence de commutation, par exemple la réduction de la taille des composants passifs, l'utilisation de semi-conducteurs à large bande interdite (WBG) est une partie inévitable des nouvelles générations de convertisseurs de puissance. La conception d'un convertisseur de puissance opérant à ces fréquences élevées nécessite une modélisation précise des semi-conducteurs de puissance. Dans ce mémoire, suite à l'étude de l'état de l'art, une nouvelle approche est proposée pour modéliser et vérifier les performances de ces nouvelles générations de commutateurs à semi-conducteurs. Une nouvelle méthode mathématique a été proposée pour modéliser la dynamique de commutation. Par ailleurs, un circuit équivalent est proposé pour les diodes de puissance PiN, facilitant l'analyse du circuit. Enfin, un ensemble d'équations d'états a été dérivé pour simuler les transitoires de commutation en considérant l'impact des éléments parasites du circuit. Le principal avantage de cet ensemble d'équations est sa validité pendant toute la période de commutation. En d'autres termes, il n'est pas nécessaire de diviser les périodes transitoires de la commutation en segments et d'analyser le circuit dans chaque segment séparément. Les résultats de simulation sont présentés pour deux scénarios différents. La comparaison des résultats avec les fiches techniques des commutateurs montre des performances prometteuses avec la méthode proposée.

Mots-clés: large bande interdite, semi-conducteur, convertisseur de puissance, diode de puissance PiN

Modeling and Simulation of High Speed Semiconductors Used in GaN and SiC Power Converters

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ABSTRACT

By considering the merits of increasing power converters switching frequency, e.g., passive components size reduction, using wide-bandgap (WBG) semiconductors is an inevitable part of new generations of power converters. Designing a power converter in such high frequencies needs accurate modeling of semiconductor switches. In this thesis, after surveying the state-of-the-art, a new approach has been proposed for modeling and verifying the performance of these new generations of semiconductor switches (SiC-MOSFETs and GaN-FETs). A new mathematical method is proposed for modeling the switches' current. Besides, an equivalent circuit is proposed for PiN power diodes, facilitating the circuit analysis of the switching dynamic. Finally, a set of state equations has been derived to simulate the switching transients by considering the impact of parasitic elements of the circuit. The main advantage of this set of equations is its validity during the entire switching period. In other words, it is not needed to divide the switching's transient periods into smaller segments and analyze the circuit in each segment separately. The simulation results have been presented in two different scenarios. Comparing these results with the switches' datasheets shows the promising performance of the proposed method.

Keywords: wide-bandgap, semiconductor, power converter, PiN power diode

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LIST OF ABBREVIATIONS

A	Junction Area
C	Capacitance
C_{gd}	Gait Drain Capacitor
C_{gs}	Gait Source Capacitor
C_{ds}	Drain Source Capacitor
D_a	Ambipolar Diffusion Constant
e	Electron Charge
EMI	Electromagnetic Interference
FET	Field-Effect Transistor
GaN	Gallium Nitride
i	Current
I_{ch}	Channel Current
I_f	Forward Diode Current
I_{RP}	Reverse Recovery Peak
I_s	Saturation Current
I_{SS}	Steady State Current of Diode
L	Inductance
L_d	Drain Stray Inductance
	L_g] Gate Inductance

L_s	Common Mode Inductance
n	Emission Coefficient
R	Resistance
R_g	Gait Resistance
P	Hole Concentration
q	Electrical Charge (Small Signal)
Q	Electrical Charge (Large Signal)
SiC	Silicon Carbide
t	Time
T_m	Diffusion Time
V	Voltage
V_{DR}	Gate Driver Voltage
V_{TH}	
V_T	Thermal Voltage
τ	Recombination Life Time
τ_{rr}	Reverse Recovery Time Constant

INTRODUCTION

Designing power converters can not be accomplished without finding the best limit point for increasing the switching frequency in the first step. On one hand, it is desired to increase the switching frequency, and consequently reduce the passive components' volume. On the other hand, increasing switching frequency leads to higher switching losses, lower efficiency and more bulky and complex cooling system. Therefore, there is always a need to use semiconductor switches capable of handling higher switching frequencies.

Gallium Nitride transistors (GaN-FETs) and Silicon Carbide MOSFETs (SiC-MOSFETs) are the new generations of power switches that show promising performance in high switching frequency applications. Although low switching losses are the main advantage of these types of switches, designing a converter in such high frequencies has faced the engineers with some new challenges which are not easy to deal with. Overcoming these challenges needs a deeper understanding of switching transient and more precise verification techniques. The switches' performance is a function of their characteristics and the circuit's parasitic components. These parasitic components are hard to measure, and in some cases, their nonlinear characteristic increases the complexity of the problem.

Considering the mentioned issues, this thesis is structured as follows:

Chapter 1 is dedicated to a comprehensive literature review. Furthermore, the objectives of this research are explained in this chapter.

In chapter 2, the modeling of a generic PiN power diodes is discussed. A circuit based model is derived, and simulation results are presented. In chapter 3, the method of modeling nonlinear capacitors is presented. A new equation has been introduced to describe the switch's channel current dependency on the gate-source and drain-source voltages.

In chapter 4, a review of switching procedure is provided. Mainly intended to improve the readers understanding about the physic behind the turn ON/OFF switching phenomenon, this chapter does not include formulas. Chapter 5 is dedicated to the verification of the model. A new set of equations is derived from two different scenarios, and simulation results are presented. In the next part of this chapter, the experimental setup used to validate the model is described. The calculation and measurement of the stray inductance is explained, and simulation results are compared with experimental results.

CHAPTER 1

LITERATURE REVIEW AND RESEARCH'S OBJECTIVES

In section 1.1, the literature is surveyed to capture a better understanding of the problem. In section 1.2, the objectives of this research are explained.

1.1 Literature Review

The trend to increase the switching frequency in power electronics converters is an inevitable part of designers' work. Increasing switching frequency leads to the reduction of size and weight of circuit passive components, and consequently a lower cost converter design. Although increasing switching frequency seems to be a great option, at first sight, some critical drawbacks are raising by increasing switching frequency. The first and most important obstacle is the fact that the switching losses will be increased by enhancing the switching frequency. In a poor designed converter the switching losses can result in overheating issue and low efficiency (Erickson & Maksimovic, 2007). The next obstacle is that the switching frequency is limited by the type of the semiconductor switches. As an example, a thyristor, typically used in high power and current application, is not able to handle switching frequency of more than $10kHz$. Conversely, a power MOSFET's switching frequency can be increased up to $100KHz$ in low-power applications.

During recent years, there has been a surge of effort to develop new types of semiconductor switches. Among these new generations of semiconductor switches, Silicon Carbide MOSFETs (SiC-MOSFETs) and Gallium Nitride FETs (GaN-FETs) show a promising level of performance, and applying these kinds of switches is developing day by day (Shenai, Dudley, Garg, Khan & Ma, 2011). These switches can be used in high-frequency applications due to their low switching losses. However, designing a high-frequency converter is not a straightforward task. The reason behind it is that by increasing the switching frequency, the effect of parasitic elements of the circuit is no longer negligible. In fact, the switch performance would be strongly affected by these parameters (Lidow, De Rooij, Strydom, Reusch & Glaser, 2019).

There are different obstacles to overcome in designing high-frequency converters. Electromagnetic Interference (EMI) issues (Ninomiya, Shoyama, Chun-Feng Jin & Ge Li, 2001), high-frequency ringing, and self-sustained oscillations (Lemmon, Mazzola, Gafford & Parker, 2013), and non-synchronized operation of paralleled switches (Lu & Chen, 2017), (Cheng & Chou, 2014) are among major challenges to be addressed by power electronics engineers. With the existence of these obstacles and complication of switching phenomenon, it is vital to have an accurate switch model.

The methods used for semiconductor switches modeling can be divided into the following categories (Mantooth, Peng, Santi & Hudgins, 2014), (Santi, Peng, Mantooth & Hudgins, 2014):

1. The first category is the physics-based models. This modeling method is based on semiconductors' physics equations. This kind of modeling is the most accurate method; however, applying this method requires many physical parameters of the device which are not available in the semiconductors' datasheets.

2. The second category of modeling is the numerical method. Using numerical simulators like SILVACO and TCAD, which are explicitly developed for power devices and circuits analyzers, it would be possible to solve the semiconductor continuity equations which include Gauss Law. This method's results are highly accurate, but it needs data about the physical dimensions of the device and its material properties. The complication and high level of computation are the other drawbacks of this category(Ohashi & Omura, 2013).
3. The third category is behavioral modeling, the most common switch simulation method used. This method is based on proposing an equivalent circuit for the switch to emulate its behavior. Usually, the required data can be extracted from the switches' datasheet, and it has lower computation than the two former methods.

In several researches, the modeling method is a combination of three main methods (Kraus & Castellazzi, 2015), (Tanimoto, Saito, Matsuura, Kikuchihara, Mattausch, Miura-Mattausch & Kawamoto, 2015).

The main focus of this work is on behavioral methods. The behavioral model of a MOSFET consists of three nonlinear capacitors, which are forming a capacitive loop, and a voltage-dependent current source, figure 3.1. Each capacitor is considered to be in between of two switch's terminals, and named after them, the gate-source capacitor C_{gs}, the gate-drain capacitor C_{gd}, and the drain-source capacitor C_{ds}. The value of these capacitors depends on the switch's terminal voltages. The current source connects the switch's drain to source. The current value, named channel current I_{ch}, is a function of gate-source V_{gs} and drain-source V_{ds} voltages. The capacitors and channel current values are depicted in several graphs in the switches' datasheets.

Finding a more accurate mathematical method to describe the channel current and nonlinear capacitors of the model are the primary goals of behavioral modeling (McNutt, Hefner, Mantooth, Berning & Ryu, 2007).

In the basic behavioral models, it has been assumed that the channel current is zero before a specific level of gate-source voltage, named the threshold-voltage V_{TH}. After that, it would be a linear function of gate-source voltage V_{GS}. Also, the switch's parasitic capacitors have been modeled with a constant capacitor (Clemente, Pelly & Isidori, 1993). In several papers, a mathematic formula is proposed to take into account the effect of both V_{gs} and V_{ds} on the channel current. All proposed formula for the channel current have several unknown constants to be extracted.

A multiplication of a quadratic of V_{GS} and a first-order polynomial of V_{ds} has been proposed in (Zhou, Chen & Wang, 1995) for the channel current simulation. The proposed formula is just for the saturation region, and its three constants have been derived using three known points with the same drain-source voltages. A modified version of this formula has been presented in (Wang, Zhou, Li, Zhao, Huang, Callanan, Husna & Agarwal, 2009), and (Wang, Zhao, Li, Huang, Callanan, Husna & Agarwal, 2008) to add the temperature effect to the model. In (McNutt, Hefner, Mantooth, Berning & Sei-Hyung Ryu, 2003) and (McNutt *et al.*, 2007), the current characteristic of SiC-MOSFET has been divided into two regions, linear and saturation. A temperature-dependent formula has been suggested for each region, which is

known as McNutt Model. The channel current formula in each region consists of two equations for high and low current operation. A software named IMPACT has been used to extract the constants in proposed formulas in each region. The McNutt Model has been improved to cover a wide range of temperature variation in (Sun, Wu, Lu, Xing & Huang, 2013). Mudholkar *et al.* has presented a new set of equation to describe the channel current. The model includes the graduate transition of channel current from linear region to saturation in SiC-MOSFETs (Mudholkar, Ahmed, Ericson, Frank, Britton & Mantooth, 2013). Li *et al.* has proposed a non-segmented equation for the channel current. In order to extract the constants of the formula, a curve-fitting software has been used. (Li, Zhao, Su, Sun, You & Zheng, 2017a). In (Sakairi, Yanagi, Otake, Kuroda & Tanigawa, 2017), a measurement based method has been proposed. Although the simulation results seems to be reliable in compare with the experimental results for both steady-state and transient modeling of the switch, the parameters extraction method is complicated, and measurements are costly and time-demanding.

Zelster *et al.* has presented the approach to simulate the nonlinear voltage-dependent capacitors (Zeltser & Ben-Yaakov, 2017). In the majority of papers, it has been tried to model the nonlinear capacitors with a voltage-dependent equation (Ji, Zheng, Wang & Tolbert, 2017), (Duan, Fan, Wen & Zhang, 2017) and (Mukunoki, Konno, Matsuo, Horiguchi, Nishizawa, Kuzumoto, Hagiwara & Akagi, 2018). Using these types of formulas not only does not improve the simulation speed but also results in low accuracy of the model. None of these formulas can accurately follow the capacitance curve, especially in low-voltage operation. A simplified charge-based model has been introduced by Heckel and Frey (Heckel & Frey, 2015). Although the proposed method shows a promising performance, it needs the measurement of gate-drain capacitor vs. the gate-drain voltage because it is not extractable from datasheet diagrams.

In (Costinett, Maksimovic & Zane, 2014) the nonlinear output capacitor of a switch has been replaced with an equivalent linear capacitor. This method is not suitable to simulate the switch's dynamic behavior during the turn ON/OFF procedure (Chen, Zhao, Yuan, Lu & He, 2014).

A verifying step is needed to clarify the performance of any proposed model.In this step, the model's functionality should be investigated as a part of a circuit. The switches' behavior in verification step is not only a function of the switches' model, but also the circuit elements. The drain's stray inductance L_d, the gate circuit's resistor R_g, and the circuit's diode have the most dominant effects on the switch's behavior. The proposed circuit, which is used for the verification step, should contain the circuit's parasitic components and an accurate model for the diode (Clemente *et al.*, 1993), (Reusch & Strydom, 2013).

There are two approaches for the model verification step, simulation-based and analytical-based. In the simulation-based method, the verification step is being done through the simulation, and there is no mathematical model for the circuit (Li *et al.*, 2017a), (Li, Jiang, Huang, Guo, Deng, Zhang & She, 2017b). In the analytical-based methods, the priority is deriving the proposed circuit equations to have a better understanding of the switching procedure. The analytical method has a complicated procedure caused by the circuit's nonlinear elements. In the former works, the authors had to divide the turn ON/OFF time into some subintervals and separately analyze each subinterval (Clemente *et al.*, 1993), (Ahmed, Todd & Forsyth, 2017). Although this type of analysis is very informative and provides a deep understanding about the switching transient, it is not an easy way to simulate switch's behavior, and can not represent the switch as a unified physical system.

Applying a realistic diode model is an inevitable part of the switch's model verification. The PiN power diodes are the most common type of diode used in power electronics applications. The main drawback of these types of diodes is the reverse recovery current. The peak value of this recovery current namely I_{RRM} is directly dependent on the diode's current rate of change dI/dt. In high frequency applications, high value of dI/dt results in a huge peak of recovery current during the turn OFF transient of the diode. This Phenomenon can increase the switching losses significantly as well as electromagnetic interferences. Accurate analysis of the reverse recovery phenomenon has been investigated in (Benda & Spenke, 1967). Lauritzen and Ma considered some assumptions and introduced a simplified model for PiN diode (Lauritzen & Ma, 1991). This model's main advantage is presenting a unified model that can be used for both turning

ON and OFF transient. Also, this model's parameters extraction method is straightforward and has been explained in (Tien & Hu, 1988) and (Roehr, 2001). In this manuscript, this model is considered as the primary diode model. Some developments have been done to extract an equivalent circuit model for the diode, which can be used in verification step.

1.2 Objectives of the Research

Inspired from the above discussions, and shortcoming of the existing literature, this research aims to introduce a new approach to model and analyze the performance of wide-bandgap semiconductors. Having a survey on the former modeling methods and proposing a new modeling approach are the main objectives of this research. Besides, a systematic method has been introduced to verify the wide-bandgap semiconductor switches' performance.

CHAPTER 2

PIN DIODES, MODELING AND SIMULATION

2.1 Overview

Power PiN diodes are fundamental elements of power electronics converters. A diode conducts the electrical current in one direction when it is forward-biased and stop the conduction during the reverse-biased. Although it seems straightforward to use an ideal diode, it is much more complicated in practice especially during switching transients. A real diode characteristic is different in comparison with an ideal diode. Considering the fact that the diodes' conductivity is based on carrier concentration, it is not easy to find a mathematical model that contains all behavioral details. Turning OFF a PiN power diode is a critical process since it comes with the complex reverse recovery process. When the diode current reaches zero during the diode turn OFF, it does not stay on that level. After that point, the current becomes negative and comes back to zero. This reverse recovery current leads to a current overshoot across the switches' and increases the converter's switching losses. In the first section of this chapter, the PiN's diode structure and operation are discussed with an emphasize on the diode's turn OFF behavior. Then, in the second section, a simplified PiN diode model is presented. The equations have been rewritten in a novel form to be more adapted with the circuit analysis method. Also parameters' extraction methods are illustrated in detail. In the third section, the simulation results are depicted and discussed.

2.2 PiN Diodes Structure and Operation

The PiN diode structure consists of a low-doped N-type region (i-region) in the middle of a P-type and an N-type highly doped material. This structure has been designed to tolerate high reverse voltage up to $3kV$. Figure 2.1 (Lauritzen & Ma, 1991) shows the PiN junction structure and carrier concentration in each region during high injection conditions (i.e. high conduction current).

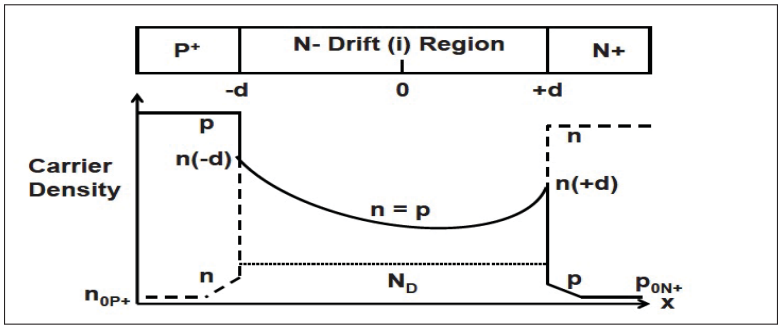


Figure 2.1 PiN diode structure and carrier concentration under High injection condition

Figure 2.2 shows a typical waveform of PiN diode current during turn OFF transient (Lauritzen & Ma, 1991). Considering the carrier concentration in the diode structure, a transient period should be passed before the diode turns OFF. This transient, which includes the reverse recovery period, can be divided into several sub-intervals.

Considering the reverse voltage V_{Off} applied to the diode at time $t = 0$, the first sub-interval after that is the "commutation stage". During this sub-interval, the diode current starts to fall while the diode voltage remains constant. The current change rate in this period is a function of circuit elements, especially the stray inductance of the power loop, the applied voltage (namely a DC source in the loop), and switch's characteristics. This subinterval is finished when the diode current reaches zero.

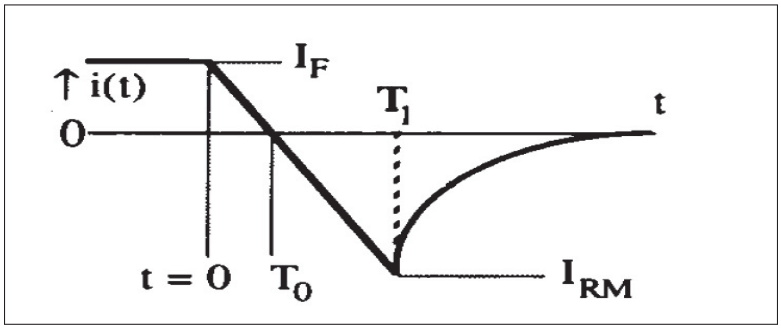


Figure 2.2 PiN diode current waveform during the turn OFF procedure

The next subinterval is named "storage stage". During this subinterval, the diode current changes its direction. Excess carrier concentration continues to reduce up to the time they reach zero on

the boundaries $+d$ and $-d$, as shown in Figure 2.1. At this point, the diode voltage collapses down to zero.

The next phase is the "voltage build-up stage". In this subinterval, which is the beginning of the reverse recovery period, the depletion region starts to develop and sweep out the rest of the excess carrier concentration. This subinterval continues till the current value reaches its negative peak (I_{RRP}). At this point $di_d/dt = 0$. The final phase is the "recovery phase." The diode current gets back to zero, and both current and voltage reach their final values after some oscillations. The frequency and magnitude of these oscillations are depended on the circuit parasitic elements and the intrisic characteristics of the diode. Deriving a set of equations to simulate diode characteristics accurately is a very complicated task to do. Such simulation needs the physical parameters of the diode's structure and its material characteristics which are not available in the diode's datasheet (Kramer & Hitchon, 1997).

In (Lauritzen & Ma, 1991), a simplified set of equations has been introduced.These equations are based on the accumulated charge in the diode's structure, and it is needed to be rewritten in a new format in order to derive an equivalent circuit for the diode. A modified version of these equations will be presented in the next section. The result is a differential equation that shows the relation between the diode current and diode voltage. It is essential to extract the coefficients of this differential equation. The extraction approach is presented in detail.

2.3 Simplified PiN Diode Model

As mentioned before, a new set of simplified equations are introduced in this section. In order to derive these equations, the following assumptions have been taken into account:

1- The drift region is divided into four sub-regions. The excess stored charge in each region (q_1 to q_4) is assumed to be a lumped value in the center of each region, as it is shown in figure 2.3 (Lauritzen & Ma, 1991).

2- It has been considered that the excess carriers concentration is symmetrical in the drift region,. Therefore, it would be possible to confine the analysis of the diode into the first and second region. q_1 and q_2 are the excess stored charge in the first and second region.

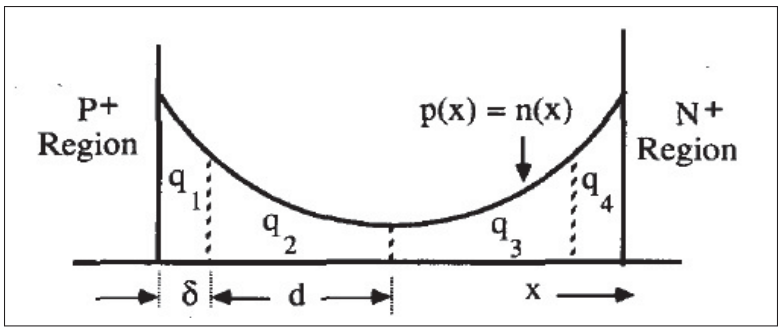


Figure 2.3 Simplified PiN diode carrier concentration under high injection condition

In this scenario, q_1 and q_2 can be calculated by:

$$\begin{aligned} q_1 &= e.A.\delta.(P_1 - P_{i0}) \\ q_2 &= e.A.d.(P_2 - P_{i0}) \end{aligned} \tag{2.1}$$

Where e is a unit electron charge, A is the junction area, δ and d are the first and second region widths, P_1 and P_2 are average hole concentration in the first and second region, and P_{i0} is the equilibrium hole concentration. Considering that the charge redistribution mechanism between the first and second region is diffusion, the current $i(t)$ can be calculated as:

$$i(t) = -e.A.2.D_a \frac{dP}{dt} = \frac{2e.A.D_a.(P_1 - P_2)}{d/2 + \delta/2} \tag{2.2}$$

In equation 2.2, D_a is the ambipolar diffusion constant. To limit the injected current from the first region to the external leads, δ should be considered much smaller than d. If $\delta \rightarrow 0$, the equation of current $i(t)$ can be rewrite as follow:

$$i(t) = \frac{q_0 - q_2}{T} \tag{2.3}$$

Here, the variable q_0 is equal to $e.A.d.(P_1 - P_{i0})$, and the constant $T = d^2/4D_a$ is the diffusion time across of second region.

Writing the charge control continuity equation for the second region, we have:

$$\frac{dq_2}{dt} + \frac{q_2}{\tau} - \frac{q_0 - q_2}{T} = 0 \tag{2.4}$$

Where τ is recombination lifetime. Finally, writing the $p^+ - i$ junction equation, one obtains:

$$P_1 - P_{i0} = P_{n0}(\exp(\frac{V}{nV_T}) - 1) \tag{2.5}$$

In equation 2.5, V_T represents the thermal voltage which is equal to 26mV, and V represents the voltage drop across the $p^+ - i$ junction. Parameter n is dimensionless named ideality factor or emission coefficient. The ideality factor is the parameter that alter the slop of diode's I-V curve. In other word, the ideality factor can be calculated using diode's I-V curve. Furthermore, it should be noted that the ideality factor is a nonlinear parameter. Considering it as constant value can leads to an error in the simulation. Multiplying both side of equation 2.5 by $e.A.d$ results in:

$$q_E = I_s.\tau(\exp(\frac{V}{nV_T}) - 1) \tag{2.6}$$

Here, the q_E is equal to $2q_0$, and $I_s = 2e.A.d.P_{i0}/\tau$ is the diode saturation current. By replacing q_2 and T with $q_M/2$ and $T_M/2$ respectively, in equations 2.3, 2.4, and 2.6, the following set of equations will be obtained. It is used to describe the PiN diode's behavior in terms of macro modelling.

$$i(t) = \frac{q_E - q_M}{T_M} \tag{2.7}$$

$$\frac{dq_M}{dt} + \frac{q_M}{\tau} - \frac{q_E - q_M}{T_M} = 0 \tag{2.8}$$

$$q_E = I_s.\tau(\exp(\frac{v}{nV_T}) - 1) \tag{2.9}$$

Deriving steady-state current equation from this set of equations:

$$I_{SS} = \frac{I_s}{1 + \frac{T_M}{\tau}}(\exp(\frac{v}{nV_T}) - 1) \tag{2.10}$$

Estimating the values of T_M, τ, I_s, and n is a crucial part of the modeling of a diode which will be discussed in detail in the next section. Equations 2.7, 2.8 and 2.9 can be rewritten in a new format to show the direct dependency of the diode voltage and current. Eliminating the variables q_E and q_M in equations 2.7, 2.8, and 2.9 leads to a step of differential equations that shows the relation between the diode current and voltage. This equation is:

$$\frac{di(t)}{dt} + (\frac{1}{T_M} + \frac{1}{\tau})i(t) = \frac{\tau}{T_M}\frac{I_s}{nV_T}e^{v/nV_T}\frac{dv}{dt} + \frac{1}{T_M}I_s(e^{v/nV_T} - 1) \tag{2.11}$$

By replacing 2.10 in 2.11, the following differential equation is obtained:

$$\frac{di(t)}{dt} + \frac{1}{\tau_{rr}}i(t) = \frac{\tau}{\tau_{rr}}\frac{dI_{SS}}{dt} + \frac{1}{\tau_{rr}}I_{SS} \tag{2.12}$$

Where:

$$\frac{1}{\tau_{rr}} = \frac{1}{\tau} + \frac{1}{T_M} \tag{2.13}$$

By estimating the values of n, I_s, T_M, and τ, equations 2.12 and 2.10 can describe a PiN diode behavior. It is important to mention that all these parameters are nonlinear quantities and estimating them with constant values will result in model inaccuracy. On other hand, finding a nonlinear data-set for each nonlinear quantity is not an easy task to do; therefore, in this research, all these four parameters are considered to be constant and the effect of this assumption will be discussed in the future chapters.

As mentioned before, equation 2.12 shows the relation between the diode current and voltage. In the next step, it could be useful if an equivalent circuit can be derived using the differential equation 2.12. To do so, this equation should be compared with the describing differential equation of the circuit presented in 2.4.

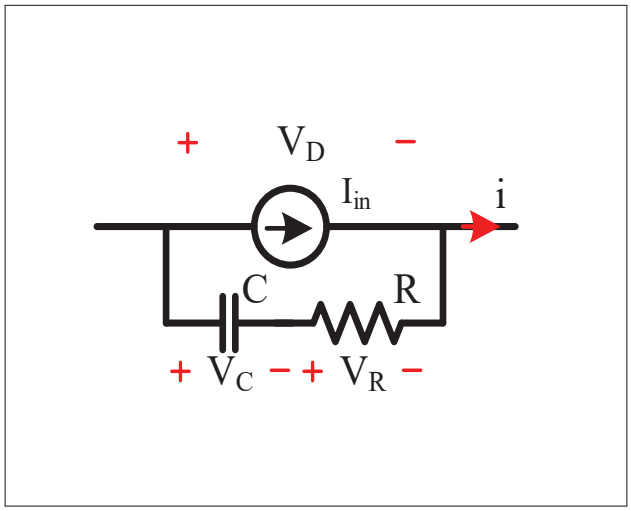


Figure 2.4 Series RC circuit in parallel with the current source I_{in}

By writing the differential equation for the proposed circuit, which relates the circuit voltage V_D to the circuit current i_D, we have:

$$\frac{di(t)}{dt} + \frac{1}{RC}i(t) = (\frac{1}{R} + \frac{dI_{in}}{dV_D})\frac{dV_D}{dt} + \frac{1}{RC}I_{in} \tag{2.14}$$

Comparing equations 2.11 and 2.14, the following formulas can be obtained for R, C, and I_{in}:

$$\begin{aligned} I_{in} &= \frac{1}{1 + T_m/\tau} I_s(\exp(V_D/nV_t) - 1) \\ R &= \frac{T_m}{\tau}(1 + \frac{T_m}{\tau})\frac{nVt}{I_s}\exp(-V_D/nV_t) \\ C &= \frac{\tau}{(1 + \frac{T_m}{\tau})^2}\frac{I_s}{nVt}\exp(V_D/nV_t) \end{aligned} \tag{2.15}$$

Finally, the circuit shown in figure 2.4 in parallel with the diode junction capacitor C_j will represent the diode equivalent circuit, figure 2.5. The values of R, L and C can be computed by set of equations 2.15.

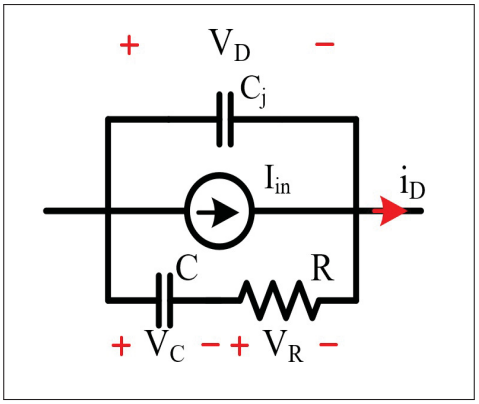


Figure 2.5 PiN diode equivalent circuit

The junction capacitor C_j is nonlinear and voltage-dependent. It should be noted that the reverse recovery period takes around $20ns$ to $50ns$ in fast recovery PiN diodes. This negative time demanding characteristic makes the PiN diodes a questionable candidate for high-frequencies applications.

On the other hand, considering that there is no minority carrier involved in Schottky diodes operation, there is no reverse recovery period. The equivalent circuit will be reduced to a current source in parallel with the junction capacitor (Arribas, Shang, Krishnamurthy & Shenai, 2015).

The switching transient time is significantly lowered than PiN diodes with the same power rating. The main disadvantages of these type of diodes are low reverse voltage and high reverse leakage current. The new generation of Schottky diodes constructed from Silicon-Carbide has a much lower reverse leakage current and low sensitivity to the temperature. The main disadvantage of SiC-Schottky diodes is their high price compared with the PiN and Schottky diodes.

Selecting a diode depends on the application and design priorities. The converter efficiency, weight, and cost are the main factors that should be optimized in the designing procedure. The type of diode can be chosen correctly only if the importance of each factor is clarified.

2.4 PiN Diode's Parameters Extraction

In this section, the extraction approach of parameters n, I_s, T_M, and τ is discussed. The approach to extract n, and I_s is presented in (Roehr, 2001). Estimation approach of T_M, and τ will be explained then. The PiN diode $VS-HFA15PB60-N3$ made by *Vishay Semiconductors* is considered as a sample to verify the model performance.

2.4.1 Three points I-V Method

The Three points $I-V$ Method which is presented in (Roehr, 2001) can be used to find the values of parameters n and I_s. It is needed to have the diode $I-V$ curve, the current axes in logarithmic scale, and the voltage in linear scale as depicted by figure 2.6 (Vishay-Semiconductors, 2019). The next step is selecting three points arbitrary P_1, P_2, and P_3.

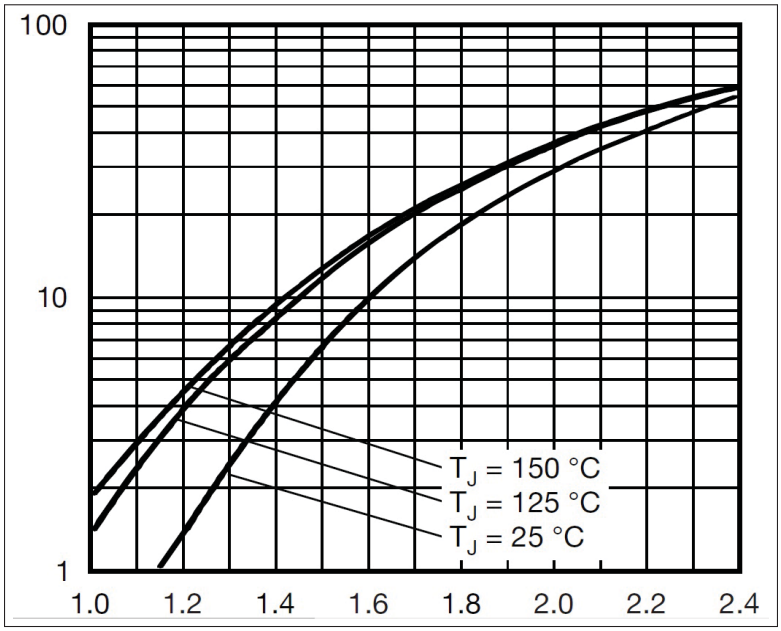


Figure 2.6 Current-Voltage characteristic of the diode $VS - HFA15PB60 - N3$

Having these three points, it would be possible to find the values of n and I_s using the next three formulas:

$$R_s = \frac{(V_2 - V_1) + (V_1 - V_3)\frac{\ln(I_1/I_2)}{Ln(I_1/I_3)}}{(I_2 - I_1) + (I_1 - I_3)\frac{Ln(I_1/I_2)}{\ln(I_1/I_3)}} \tag{2.16}$$

$$n = \frac{(V_1 - V_2) + Rs(I_2 - I_1)}{V_t \ln(I + 1/I_2)} \tag{2.17}$$

$$I_s = \frac{I_1}{\exp(\frac{V_1 - R_s I_1}{n.V_t}) - 1} \tag{2.18}$$

Parameter R_s is the diode's series resistor in the diode spice model (Roehr, 2001), representing the metal contacts resistors and neutral region resistor under high-level injection conditions.

Considering figure 2.6 and using equations 2.16, 2.17 and 2.18, the extracted values for parameters R_s, n, and I_s would be $12.9m\Omega$, 11.45, and $3.7mA$, respectively.

2.4.2 Time Constants T_m and τ Extraction Method

The objective of this subsection is to generalize a new approach to achieve an equation for estimation of τ and T_M. As mentioned before, turning OFF a diode starts with a current decreasing period. During this time $t < T_1$, the current is decreasing almost linearly, and after that $t > T_1$ it approaches zero exponentially, as shown in figure 2.2. Assuming that the slope of the curve in the linear region is $-\alpha$, then:

$$i(t) = I_f - \alpha t, \quad 0 < t < T_1 \tag{2.19}$$

Replacing 2.19 in equation 2.12, the following differential equation can be obtained:

$$\frac{dI_{SS}}{dt} + \frac{1}{\tau} I_{SS} = \frac{1}{\tau}(I_f - \alpha\tau_{rr}) - \frac{1}{\tau}\alpha t \tag{2.20}$$

Solving the differential equation 2.20, one obtains:

$$I_{SS} = (I_f - \alpha t) + (\tau - \tau_{rr})\alpha(1 - \exp(-t/\tau)) \tag{2.21}$$

Taking into account 2.19, equation 2.22 can be written as:

$$I_{SS} = i(t) + (\tau - \tau_{rr})\alpha(1 - \exp(-t/\tau)) \tag{2.22}$$

Equation 2.22 shows the dependency of the diode current and voltage in the linear current descending period. To use this equation, it should be taken into account that at the point T_1,

$i(T_1)$ is equal to $-I_{RRM}$, and the diode voltage is zero; therefore, the variable I_{SS} is zero as well.

$$i_s(T_1) = 0 \tag{2.23}$$

By substituting 2.23 in 2.22 at $t = T_1$, the following fundamental equation is obtained:

$$(1 + \frac{T_m}{\tau}).(I_{RRM}) = \tau\alpha(1 - \exp(-T_1/\tau)) \tag{2.24}$$

Eliminating T_m yields:

$$(\tau - \tau_{rr})\alpha(1 - \exp(-T_1/\tau)) = I_{RRM} \tag{2.25}$$

Solving this equation allows to find the value of τ, and then using 2.13, the coefficient T_m can be computed as well. Using this method for the diode $VS - HFA15PB60 - N3$, the values of τ and T_m would be $39.4ns$ and $18.7ns$, respectively.

In order to evaluate this method's performance, it has been considered that the diode is in series with a resistor R and an inductance L_S. L_S represents the stray inductance of the circuit, figure 2.7.

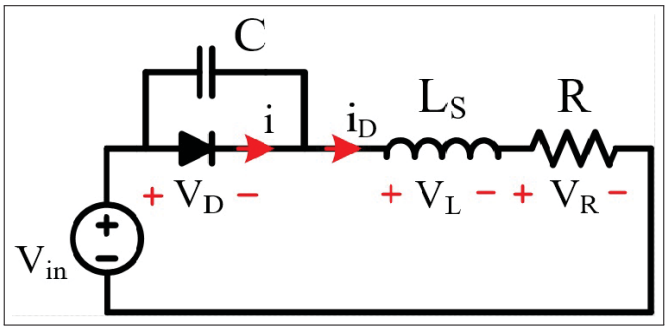


Figure 2.7 Proposed circuit topology for verifying the proposed PiN diode model

Capacitor C shows the junction capacitor of the diode. The values of R, L_S, and C are 10Ω, 200nH, and 25pF, respectively. The relation between the diode voltage V_D and diode current

i is described by equation 2.11. This circuit has been simulated in MATLAB/Simulink. In this simulation, the initial voltage value is $150V$, the diode is ON, and the current i_D is $15A$ (steady-state condition). At the moment $t_0 = 200$ns, the input voltage changes to -200 abruptly.

The diode current waveform is shown in figure 2.8. The dashed curve shows the variable i in figure 2.7, and the other curve shows the summation of this current and the current of the junction capacitor, which is the real diode current i_D.

By comparing the diode's current waveform with the data available in the datasheet, it was expected to have a peak reverse recovery current equal to $15A$. At the same time, the simulation results show a value close to $13A$. The diode voltage waveform is depicted in figure 2.9. As expected, the diode voltage has remained constant up to the time the diode current reaches its negative peak value, and then starts to decrease. The AC component in the diode current and voltage has its root in the resonance phenomenon between the junction capacitor and the circuit's stray inductance.

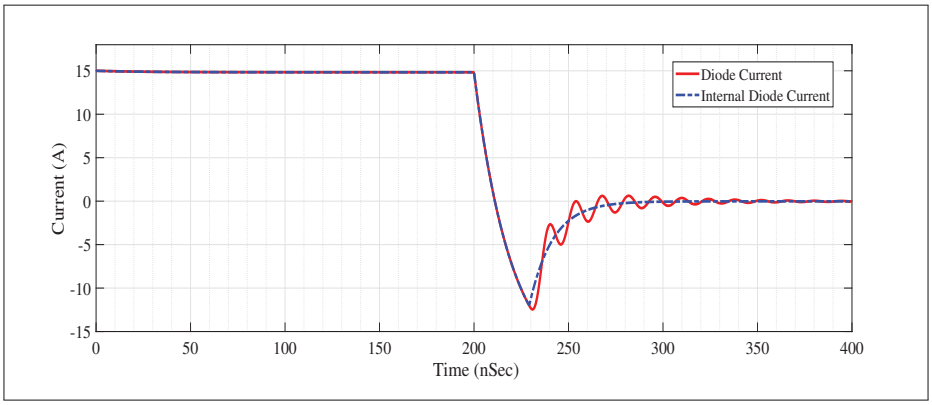


Figure 2.8 Turn OFF diode current

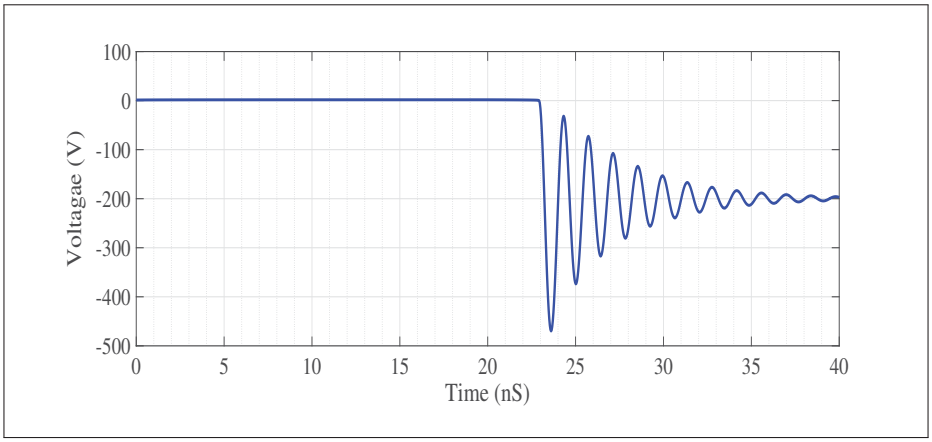


Figure 2.9 Turn OFF diode voltage

CHAPTER 3

FETS MODELING

3.1 Overview

The main focus of this chapter is on deriving a set of differential equations to describe the performance of Wide-Bandgap (WBG) Semiconductor switches, specifically Silicon-Carbide (SiC) MOSFETs and Gallium-Nitride (GaN) FETs. Although the types of materials and structures are different in these two types of WBG semiconductor switches, the basics of modeling are similar. Therefore, this section aims to illustrate the modeling approach regardless to material specifications. The primary circuit suggested for modeling a switch is presented in figure 3.1, (Clemente *et al.*, 1993).

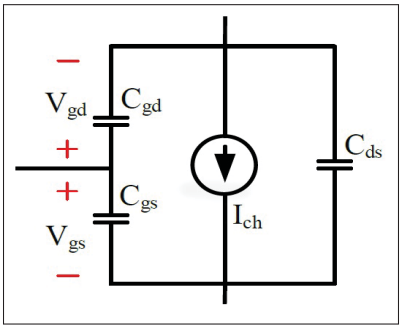


Figure 3.1 WBG semiconductor switch model based on a voltage-controlled current source and the parasitic capacitors

It is important to note that this model's capacitors are nonlinear, and their values depend on the switch's voltages. The switch's transient behavior is extremely affected by these capacitor values, so it is necessary to know how to analyze a nonlinear capacitor's effect in an electrical circuit. Besides that, the current source value I_{ch} (Channel Current) is a function of gate-source and drain-source voltages (V_{gs} and V_{ds}). This dependency is depicted in the switch's datasheet through some charts. So, another goal of this chapter would be to provide an approach to correctly use these sorts of data.

In section 3.2, the concept of nonlinear capacitors will be reviewed. Also, the switch's parasitic capacitors will be discussed. In section 3.3, the dependency of I_{ch} to V_{gs} and V_{ds} will be illustrated, and a new method of modeling will be presented.

3.2 Parasitic Capacitors of a WBG Semiconductor Switch

The nonlinear capacitors of a switch C_{gs}, C_{gd}, and C_{ds} are voltage-dependent capacitors. The capacitances are presented in the switch's datasheet as Input Capacitor C_{iss}, Output Capacitor C_{oss}, and Reverse Transfer Capacitor C_{rss}. The relation between defined capacitors are as follow:

$$\begin{aligned} C_{rss} &= C_{gd} \\ C_{iss} &= C_{gd} + C_{gs} \\ C_{oss} &= C_{gd} + C_{ds} \end{aligned} \tag{3.1}$$

Figure 3.2 shows the capacitances vs. V_{ds} for the GaN-FET model $GS66508P$ manufactured by GaN-Systems.

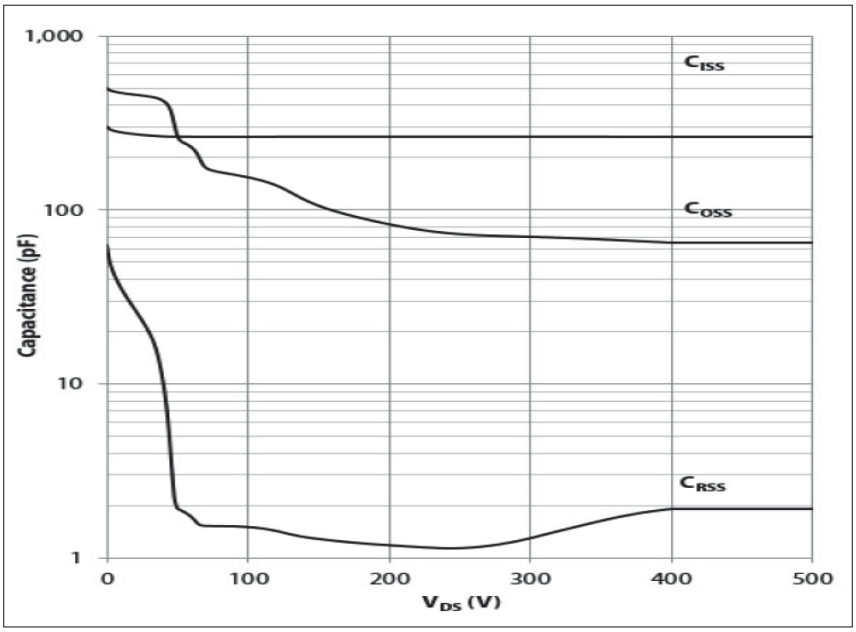


Figure 3.2 Capacitors of GaN-FET $GS66508P$

As shown in this figure 3.2 (GaN-Systems, 2018), C_{gd}, and C_{ds} are extremely nonlinear capacitors, while the variation of C_{gs} with respect to the voltage is almost negligible. This is why in most researches, C_{gs} is considered a voltage-independent capacitor.

In the next step, it would be mandatory to have a better understanding of the nonlinear capacitors and extract the describing formula for both small-signal and large-signal models. In a nonlinear capacitor, the capacitance value will be changed with respect to the voltage value; also, the small-signal model is not the same as the large-signal model which is not took into account in some references (Rahimo & Shammas, 2001). Assuming that figure 3.3 represents a part of the charge vs. voltage curve of a nonlinear capacitor, point (v, q) shows the capacitor's operation point. Based on equation $Q = C.V$, the slope of the line which connects the origin to the point (v, q) (red-line) shows the capacitance value. C_t stands for this slope value of this red line. On the other hand, if $\delta Q/\delta V$ is considered as the definition of the capacitor value, the slope of the tangential blue line in figure 3.3 shows the capacitance value and is denoted by C_S. In other words, C_S is the small signal value of the capacitors.

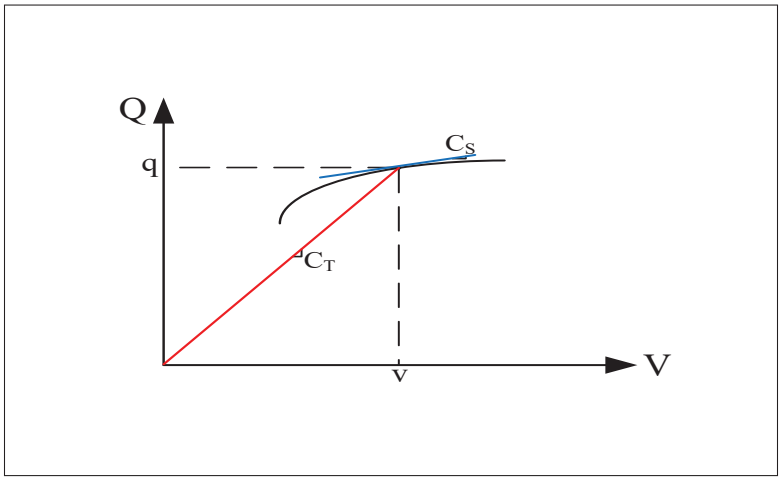


Figure 3.3 Charge vs. Voltage envelope of a nonlinear capacitor

Whether we are measuring C_T or C_S depends on the measurement method. Using an impedance meter is a common way to do this measurement. Since an impedance meter injects a perturbed voltage on top of a dc bias, and measures the current, the measurement results show the C_S

values (Costinett *et al.*, 2014). The current equation using C_T has been presented in equation 3.2. One should note that the current equation consists of two parts, one is related to the derivative of the voltage with respect to time, and the other part is related to the derivative of the capacitance C_T with respect to time.

$$\begin{aligned} Q &= C_T.v \\ \frac{dQ}{dt} &= i(t) \\ i(t) &= C_T.\frac{dv(t)}{dt} + v(t).\frac{dC_T}{dv(t)}\frac{dv(t)}{dt} \end{aligned} \tag{3.2}$$

By using the small signal definition of the capacitor value C_S, the current equation will be as follow:

$$\begin{aligned} dQ &= C_S.dv \\ i(t) &= C_S.\frac{dv(t)}{dt} \end{aligned} \tag{3.3}$$

Using the small signal definition, the capacitor current equation would be similar to the linear capacitors. Equation 3.4 shows the relation between C_T and C_V.

$$C_T(v) = \frac{\int C_S(v).dv}{v} \tag{3.4}$$

Some of the papers that attempt to model the semiconductor switches have tried to present a formula that shows the relation between the capacitance and voltage. Using these types of formulas, neither simplifies the calculations nor increases accuracy; therefore, using a look-up table is a more efficient way to simulate these capacitors.

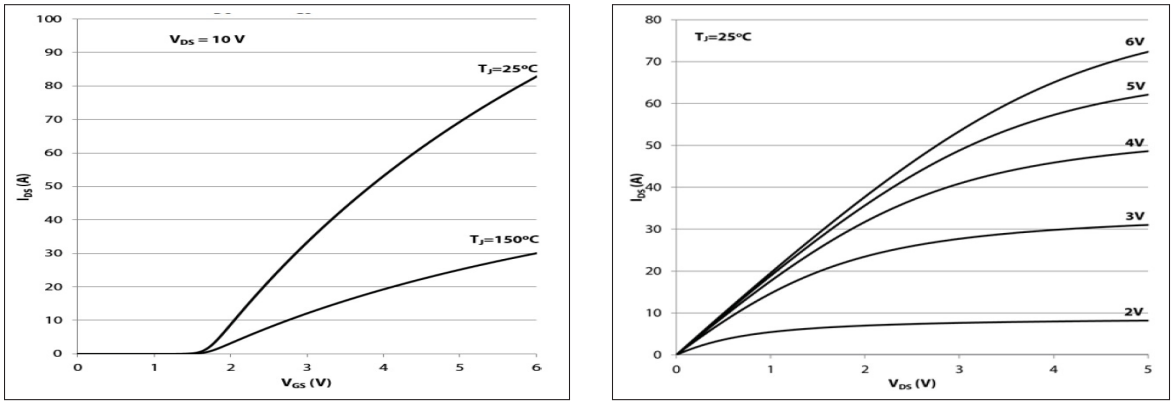
The next point is that the switch's parasitic capacitors are measured using an impedance meter; therefore, the datasheet capacitor values shows a nonlinear capacitor's small-signal definition.

The simulation period should be divided into small subintervals to use these values in a code or simulation. In each subinterval, the capacitance values are considered to be constants. For the next subinterval, these values would be updated with respect to the switch's final voltage in the prior subinterval.

3.3 The Channel Current I_{ch}

The switch model's next nonlinear parameter is the channel current, which is shown with a current source in the switch model, figure 3.1.

The value of the channel's current (I_{ch}) is not only a function of V_{gs} but also V_{ds}. Figure 3.4 shows the dependency of this current to V_{gs}, and V_{ds} of switch $GS66508P$.



a) GaN-FET drain current vs. gate-source voltage b) GaN-FET drain Current vs. drain-source voltage

Figure 3.4 GaN-FET current characteristic

Figure 3.4b (GaN-Systems, 2018) shows the relation between the drain current and drain-source voltage. For a constant value of the gate-source voltage, each curve can be divided into two regions. The first region, named linear region, starts from point $V_{DS} = 0$ to the point at which the drain current loses its dependency to the drain-source voltage variation. At this point, the drain-source voltage V_{DS} is equal to saturation Voltage V_{sat}, and the Channel current I_{ch} is equal to the saturation current I_{sat}. It is important to note that in the saturation region, the current is

just a function of gate-source voltage. For instance, in figure 3.4b, when the gate-source voltage is equal to $3V$, the saturation voltage is equal to $5V$, and the saturation current is $30A$. After this point, by increasing the drain-source voltage, there is no significant change in the drain current. Considering figure 3.4a, V_{DS} is 10V, which is higher than V_{sat}; however, for 3V gate-source voltage the current value is still 30A. On the other hand, in linear region, the drain current is not only a function of V_{GS}, but also a function of V_{DS}.

There are different methods to combine the effect of both voltages on the drain current. A usual method is proposing a mathematical function that consists of exponential and hyperbolical parts. Some iterative methods have been used to fit the constants of these functions. In this research, a new method will be proposed for this estimation. This method is based on the *convex combination* of two vectors. The main advantages of this method are as follow:

1- The resulting formula is of lower complexity compared with the proposed formulas in the literature review. There is no exponential or hyperbolical part involved in the formula.

2- Extraction of unknowns in this method does not need high amount of computation. Even visually extraction of these parameters can leads to an acceptable precision.

The theory of this method is explained in the following section.

3.3.1 Convex Combination of two Vectors

Let's consider two arbitrary vectors in a two-dimensional space, named $\vec{A}$ and $\vec{B}$. $\vec{AB}$ is the vector that connects point A to B. Now Convex Combination of these two points can be defined as:

$$\begin{aligned} l &= A(k-1) + Bk \\ 0 &\leq k \leq 1 \end{aligned} \tag{3.5}$$

Equation 3.5 shows a point which travels through vector $\vec{AB}$, starting from A, by changing the value of k from zero to one.

The next step is the convex combination of two vectors. As it is depicted in figure 3.3.1, vectors $\vec{AC}$ and $\vec{CB}$ connect the points B to C and C to A, respectively. It is possible to write the convex combination of pairs (A, C) and (C, B) using equation 3.6.

$$\begin{aligned} l_1 &= A(k-1) + Ck \\ l_2 &= C(k-1) + Bk \\ 0 &\leq k \leq 1 \end{aligned} \tag{3.6}$$

In this case, when k starts to increase from zero to one, first moving point starts to travel from A to C, and second moving point starts to travel from C to B at the same time. Now, it is possible to write another convex combination for two moving points l_1 and l_2 to derive the equation of one new path l_T. Equation 3.7 shows l_T equation, and it is plotted in figure 3.5 by the blue dashed curve.

$$\begin{aligned} l_T &= l_1(1-k) + l_2 k \\ &= (A(k-1) + Ck)(1-k) + (C(k-1) + Bk)k \\ &= A(1-k)^2 + 2Ck(1-k) + Bk^2 \\ 0 &\leq k \leq 1 \end{aligned} \tag{3.7}$$

It should be noted that by changing parameter k from zero to one, this new curve starts to move from point A and it is tangential to the vector $\vec{AC}$ and ends to point B, while it is tangential to the vector $\vec{CB}$. Therefore, by using vectors $\vec{AC}$ and $\vec{CB}$ the path l_T can be shaped. The start and end point's slope of the path l_T are tuned by the slope of vectors $\vec{AC}$ and $\vec{CB}$, and the path curvature can be affected by the length of these vectors. While equation 3.7 can be a useful equation for estimating a given curve with a function, parameter k is an extra parameter and

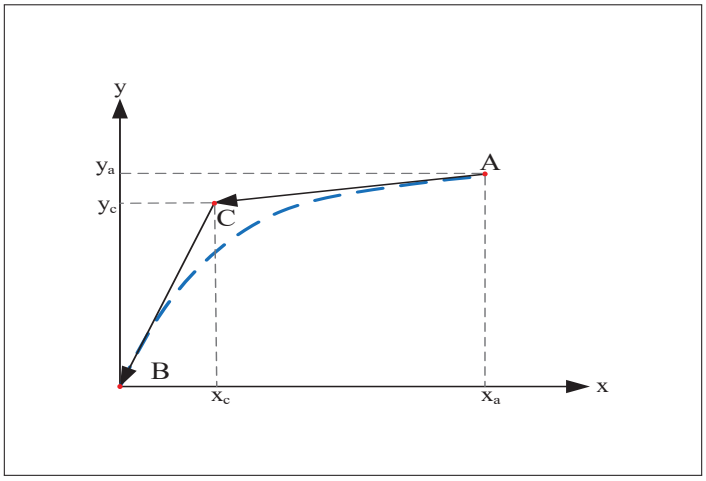


Figure 3.5 Convex combination of two vectors

should be eliminated. To do so, equation 3.7 should be rewritten as follow:

$$
\begin{aligned}
& l_T : l_1(1-k) + l_2 k \\
& \begin{bmatrix} x \\ y \end{bmatrix} = (\begin{bmatrix} x_A \\ y_A \end{bmatrix}(k-1) + \begin{bmatrix} x_C \\ y_C \end{bmatrix} k)(1-k) + (\begin{bmatrix} x_C \\ y_C \end{bmatrix}(k-1) + \begin{bmatrix} x_B \\ y_B \end{bmatrix} k)k \\
& \begin{bmatrix} x \\ y \end{bmatrix} = \begin{bmatrix} x_A \\ y_A \end{bmatrix}(1-k)^2 + 2\begin{bmatrix} x_C \\ y_C \end{bmatrix} k(1-k) + \begin{bmatrix} x_B \\ y_B \end{bmatrix} k^2 \\
& 0 \le k \le 1
\end{aligned}
\tag{3.8}
$$

Equation 3.8 consists of two parts. Replacing point B by $[0, 0]$, and eliminating k results in equation 3.9.

$$
y = \frac{1}{\Delta y_2 - \Delta y_1}[-\Delta y_1^2 + [-\Delta y_2 + \frac{\Delta y_1 - \Delta y_2}{\Delta x_1 - \Delta x_2}(\Delta x_2 - \sqrt{\Delta x_1^2 + (\Delta x_2 - \Delta x_1)x})]^2] \tag{3.9}
$$

Where:

$$\begin{aligned} \Delta x_1 &= x_C - x_B = x_C \\ \Delta x_2 &= x_A - x_C \\ \Delta y_1 &= y_C - y_B = y_C \\ \Delta y_2 &= y_A - y_C \end{aligned} \tag{3.10}$$

Using equation 3.9, it would be possible to estimate the sets of envelopes depicted in figure 3.6.

3.3.2 Channel Current Modeling

To apply equation 3.9 for estimating the curves shown in figure 3.4b, parameters Δx_1, Δx_2, Δy_1, and Δy_2 have been defined as a function of V_{gs} by using interpolation method. Different methods of interpolation examined such as lookup table, Cubic spline data interpolation, and Piecewise Cubic Hermite Interpolating Polynomial (PCHIP). The best results achieved by applying the third method PCHIP. By considering the value of V_{gs}, the correct values of parameters Δx_1, Δx_2, Δy_1, and Δy_2 have been calculated and corresponding curves will be generated. The results of this method is shown in figure 3.6.

To get a better perspective about the interaction of three parameters I_D, V_{ds}, and V_{gs}, the $3D$ figure 3.7 has been presented.

In this figure, the estimated drain current value with respect to the gate-source and drain-source voltages is presented.

Since using a current source in the proposed MOSFET model can impose an unwanted condition to the circuit's states, it would be reasonable to replace it with an equivalent resistor. The resistor value R_{ch} can be obtained by dividing V_{DS} to I_{ch} in the linear region, and in the saturation region, it would be V_{sat}/I_{ch}. The $3D$ surface, depicted in figure 3.8, shows the channel resistance R_{ch} vs. the gate-source and drain-source voltages in the linear region.

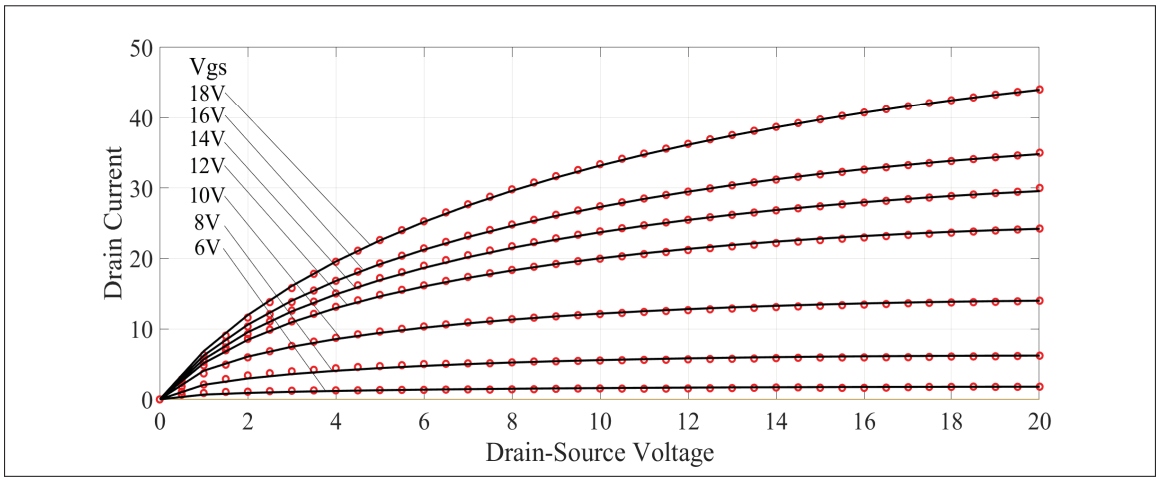


Figure 3.6 Drain current vs drain-source voltage, which is estimated by proposed method. The black lines represent the calculated points using the proposed method and red dots represent the extracted points from the switch datasheet

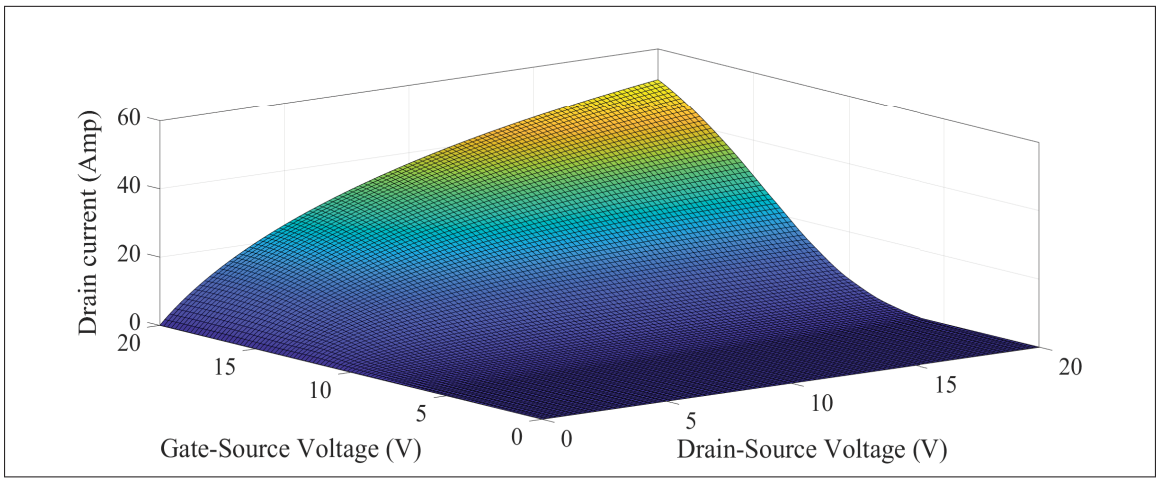


Figure 3.7 Drain current vs drain-source voltage vs gate-source voltage, which estimated by convex combination of vectors

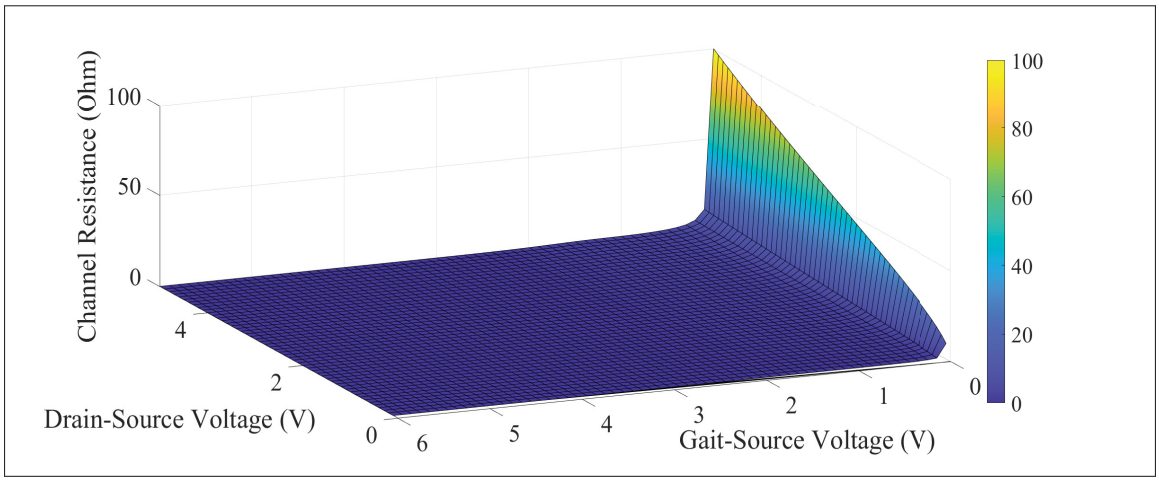


Figure 3.8 The resistance of the channel as a function of the gain-source and drain-source voltage

CHAPTER 4

A REVIEW OF MOSFETS' TURN ON/OFF PROCEDURE

4.1 Overview

This chapter is dedicated to explaining the turn ON/OFF procedure of a MOSFET in its general form. A simplified circuit has been proposed in figure 4.1, and using this circuit, switching transient has been discussed. The proposed circuit does not contain all circuit's parasitic elements to keep the concept as simple as possible. The gate circuit inductance L_g, common mode source inductance L_s and diode junction capacitor C_j are the neglected parasitic components in this circuit. Besides, the mathematical analysis is not presented to have more emphasis on the switching concept itself.

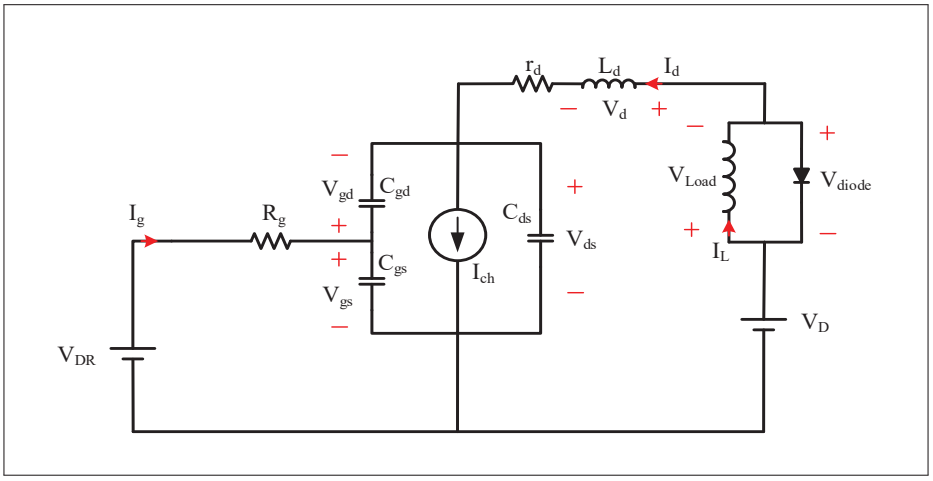


Figure 4.1 Simplified switching circuit

Each transient period of the switching is divided into several subintervals. Each subinterval is discussed in details.

4.2 Switching Transient During the Turn ON Interval

Turning ON/OFF a MOSFET is initiated with a step change of the gate driver voltage from V_{DR_Off} to V_{DR_On}. Figure 4.2 presents a typical gate driver voltage waveform.

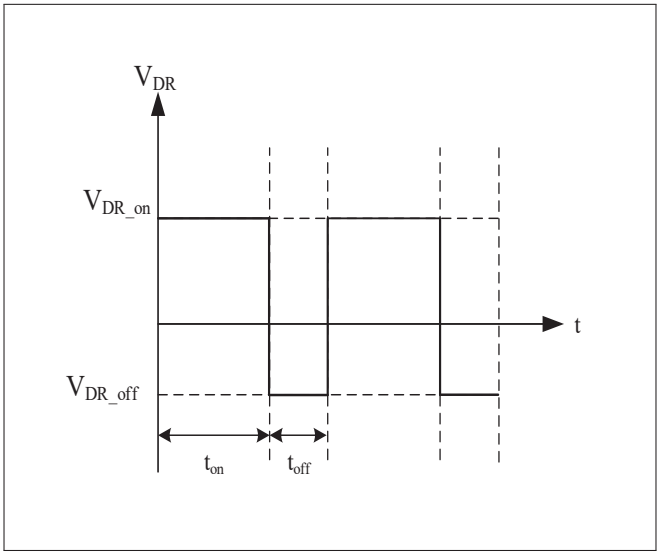


Figure 4.2 Typical Voltage Waveform of the Gate Driver

Figure 4.3 shows a typical drain-source voltage and drain current diagram during turn ON transient. This period can be divided into four main subintervals, i.e., Δt_1 to Δt_4.

The first subinterval starts while the drain-source voltage is almost equal to the output voltage V_D, and the drain current I_d is zero. It has been assumed that the driver voltage V_{DR} rises instantaneously to V_{DR_On} at the beginning of this subinterval. Therefore, the gate-source voltage V_{gs} starts to increase. As long as V_{gs} is less than the MOSFET's threshold voltage V_{TH}, there is no change in V_{ds} and I_d. The first subinterval ends when the gate-source voltage reaches V_{TH}.

The second subinterval Δt_2 starts when V_{gs} value reaches V_{TH}. By increasing V_{gs}, the drain current increases rapidly, and the drain-source voltage falls. During this subinterval, different scenarios can happen, and the mechanisms of increasing the drain current and collapsing the drain-source voltage are intertwined.

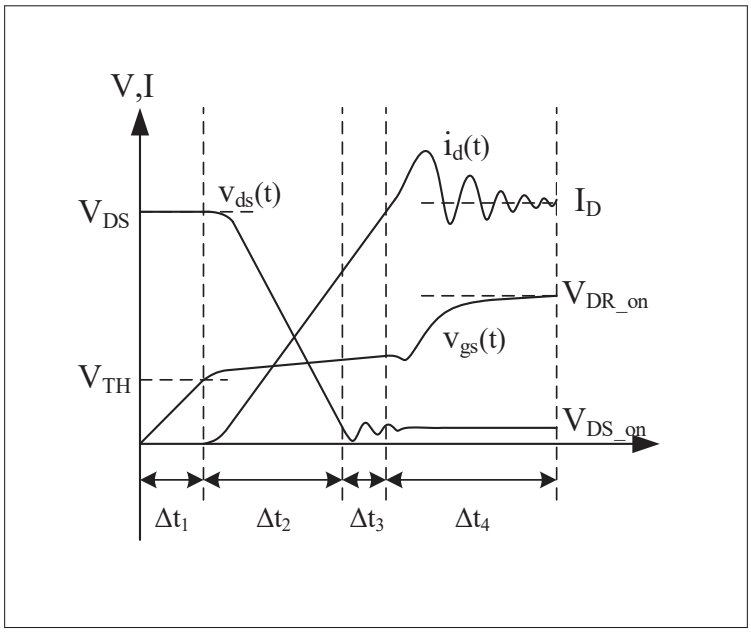


Figure 4.3 Typical waveforms of MOSFETs' turn ON transient

In the first case, the drain stray inductance value L_d is high enough to block the voltage V_D. So, the drain-source voltage can drop down and reach its final value, i.e., V_{ds_On}. The second subinterval ends while the drain current has a value between zero to its final value I_D.

In the second case, the drain stay inductance has a small value. Therefore, the main controlling factor of V_{ds} is the Miller capacitor voltage V_{gd}. This capacitor will be discharged by the gate circuit current namely I_g. The value of the gate resistance R_g has a dominant effect on charging and discharging the MOSFET input capacitors. While C_{gd} is discharging, a Miller plateau can be observed on the gate-source voltage curve. In this case, the subinterval ends while $i_d(t)$ reaches its final value, and $V_{ds}(t)$ has a value between V_D and V_{ds_On}. Therefore, the second subinterval will be ended either when the drain current or the drain-source voltage reaches its final value.

In the third subinterval, again, two scenarios can be observable. If at the end of the second subinterval $V_{ds}(t)$ is equal to V_{ds_on}, during the third subinterval, it remains constant, while the

drain current increases to the load current namely I_D. On the other hand, if at the end of the second subinterval $i_d(t)$ is equal to its final value I_D, the drain-source voltage decreases to V_{ds_On}.

Also, it should be mentioned that after the time in which $i_d(t)$ reaches the final value, there is an overshoot in its waveform. This overshoot is the result of two phenomena. The dominant phenomenon is the diode reverse recovery current I_{RR}. When I_d is equal to I_D, it means that the diode current is equal to zero. After this point, the diode's stored charge should be swept out, leading to a negative current peak in the diode's current waveform. The reverse recovery current passes through the switch, and it is observable as an overshoot in the switch's current waveform.

The other phenomenon is the oscillation of parasitic capacitors and inductances of the circuit.

In the fourth subinterval, $i_d(t)$ and $V_{ds}(t)$ are settled on their final values, and the gate-source voltage increases to reach the gate driver voltage V_{DR_On}.

4.3 Switching Transient during Turn OFF Interval

Figure 4.4 presents a typical waveform of MOSFETs' turn OFF transient. The turn OFF transient starts with a step-change in the gate driver voltage from V_{DR_On} to V_{DR_Off}. During the first subinterval V_{ds} and I_d remains constant and gate-source capacitor discharges. In contrast with the gate-source capacitor, the gate-drain capacitor starts to charge. Considering that the gate-drain capacitor has a negative bias, C_{gd} has a high value. This high capacitance has a direct effect on this subinterval duration. While C_{gs} is discharging, C_{gd} is charging. At the end of the first subinterval, the gate-source voltage reaches a point at which it can still support the drain current.

The second subinterval starts with increasing V_{ds} while the drain current remains constant. The drain current remains constant since as long as V_{ds} is smaller than V_{out}, the free-whiling diode can not turn ON and the drain current can not deviate toward it. Considering the constant level of V_{gs} and the increase of V_{ds}, V_{gd} increases in this subinterval; therefore, the main part of gate circuit current pass through C_{gd} and a Miller plateau region is observable on V_{gs}. The second subinterval ends at the time V_{ds} is equal to V_{out}.

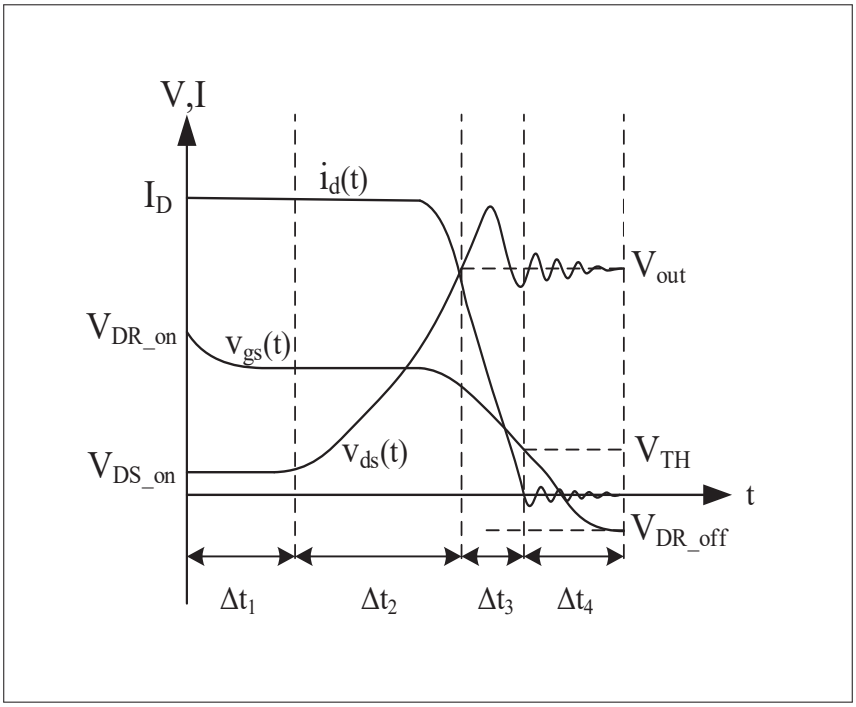


Figure 4.4 Typical waveforms of MOSFETs' turn OFF transient

During the third subinterval, the freewheeling diode starts to conduct the current; therefore, the drain current starts to decrease. di_d/dt results in a negative pick voltage on the drain's stray inductance. So, the drain voltage increase in the third subinterval, and it leads to magnifying the switching loss. The third subinterval terminates at the time which the drain current reaches zero.

In the fourth subinterval, the drain current remains constant, and gate-source voltage reduces to V_{DROff}. C_{ds}, L_d, and R_d form an RLC circuit, and the extra stored energy in C_{ds} will be wasted during the resonance.

In the next chapter, which is dedicated to the simulation of the switch's transients, the simulation results will be compared with the typical waveforms introduced in this chapter to verify if the simulation results are compatible with the expected switching sequences.

CHAPTER 5

WBG SEMICONDUCTOR SWITCHES: SIMULATION AND EXPERIMENTAL VALIDATION OF THE MODEL

5.1 Overview

This section's primary goal is to propose a new method for verifying a switch model and extracting the accurate waveforms of switching transient periods. This proposed method can be modified based on the diode type which has been used in the converter configuration. Using the concepts introduced in section 2 and 3 two scenarios have been taken into account.

In the first scenario, a step-down converter has been designed using a GaN-FET and a SiC-Schottky diode. In the second scenario, a SiC-MOSFET and a PiN power diode are the converter's main elements. For each scenario, all needed data have been extracted from the elements' datasheet accurately.

The first scenario is presented in the next section. An inductive load is being fed through a GaN-FET based converter, and the anti-parallel diode type is a SiC-Schottky. A circuit model is proposed, and the state equation is derived for the simulation purpose. The simulation results are presented and discussed at the end of this section. In section 5.3, the second scenario has been presented. A SiC-MOSFET-based converter combined with a PiN freewheeling diode feeds an inductive load. The proposed circuit and equations have been modified with respect to the diode type, and simulation results.

Section 5.4 is dedicated to the experimental validation. The experiment set up is explained in details and the results are compared with the simulation results.

5.2 First Scenario: Modeling of a GaN-FET switching transient with a SiC-Schottky Freewheeling Diode

As mentioned before, most proposed methods which are used to analyze the switching procedure are suffering from the lack of a *unified system* with a valid time response for all periods of switching transient. The usual approach to solve this issue is dividing the transient periods into some subintervals and proposing a valid system just for each specific subintervals. The next obstacle is that each interval's proposed circuits do not take into account all parasitic elements of the circuit and the power MOSFET.

In this section, a circuit is proposed which contains the effect of all parasitic elements. Using the FET and diode models introduced in chapter 2, and 3, the state equations of this proposed circuit are derived, and the simulation results are presented.

5.2.1 Proposed Circuit for Analyzing Switching Transient

The proposed circuit for analyzing transients of a GAN-FET has been presented in figure 5.1. As it is shown, none of the circuit elements has replaced with a dependent/independent current source. The first component, which is usually replaced by a current source, is the output power inductor L_{out}. If the output inductor represents a highly inductive load, using a current source to model it is a valid assumption. However, in some other applications, it is used as an output filter. In these cases, the inductor current may change between 10% to 20% of the nominal output current of the converter during a switching period; therefore, using a current source to model the inductor results in reducing the model accuracy because of neglecting this change in the output current waveform.

This inductor is in parallel with a freewheeling diode D. Since the type of diode is SiC-Schottky; therefore, the modeling is easier than a PiN power diode. In this case, it has been modeled with a voltage-controlled current source in parallel with the nonlinear junction capacitor C_j. The voltage of the diode is another state of the proposed circuit V_C. Except for the current of the output inductor $i_{L_{out}}$ and voltage of diode capacitor V_C, the next defined state related to the

power loop is the current of the parasitic drain inductor of the power loop I_d, known as the *Drain Inductor*. The switching transient is strongly affected by the drain inductor value L_d (Clemente *et al.*, 1993). The values of r_d and V_D representing the power loop resistor and the output voltage, respectively.

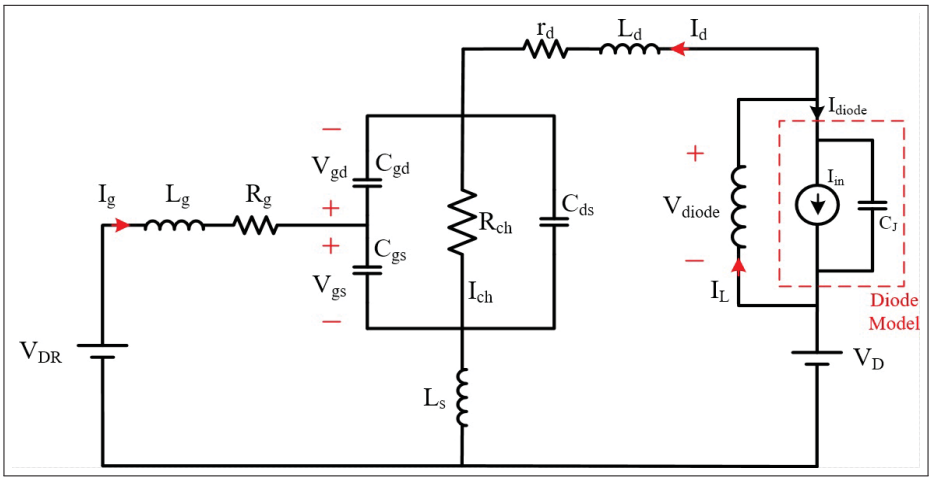


Figure 5.1 Proposed circuit

The next modification is replacing the voltage-dependent current source of the switch model with the channel resistor (R_{ch}) which is represented in figure 3.8. The computation of this resistor has been explained in chapter 3.

In the switch model's capacitive loop, each capacitor's voltage is linearly dependent on the other capacitors' voltages; therefore, the voltage of only two of them can be considered as the state variables. In this case, the gate-source and gate-drain voltages are considered as the state variables, V_{gs}, and V_{gd}.

On the other hand, the current of common mode inductance (I_{L_s}) is linearly dependent on the gate current (I_g) and drain current (I_d). So, I_g and I_d are the next two state variables of the circuit. Finally, the state vector of the circuit X can be defined as:

$$X = \left[I_L, I_d, I_g, V_{diode}, V_{gs}, V_{gd} \right]^T \tag{5.1}$$

Using the Kirchhoff circuit's laws, the state equations of the circuit will be:

$$\begin{bmatrix} 1 & 0 & 0 & 0 & 0 & 0 \\ 0 & L_d + L_S & L_S & 0 & 0 & 0 \\ 0 & L_S & L_g + L_S & 0 & 0 & 0 \\ 0 & 0 & 0 & C_j & 0 & 0 \\ 0 & 0 & 0 & 0 & C_{ds} & -(C_{ds} + C_{gd}) \\ 0 & 0 & 0 & 0 & C_{gs} & C_{gd} \end{bmatrix} \frac{d}{dt} \begin{bmatrix} I_L \\ I_d \\ I_g \\ V_{diode} \\ V_{gs} \\ V_{gd} \end{bmatrix} = \begin{bmatrix} 0 & 0 & 0 & 1/L & 0 & 0 \\ 0 & -r_d & 0 & 1 & -1 & 1 \\ 0 & 0 & -R_g & 0 & -1 & 0 \\ 1 & -1 & 0 & 0 & 0 & 0 \\ 0 & 1 & 0 & 0 & -1/R_{ch} & 1/R_{ch} \\ 0 & 0 & 1 & 0 & 0 & 0 \end{bmatrix} \begin{bmatrix} I_L \\ I_d \\ I_g \\ V_{diode} \\ V_{gs} \\ V_{gd} \end{bmatrix} + \begin{bmatrix} 0 \\ V_D \\ V_{DR} \\ -i_{in} \\ 0 \\ 0 \end{bmatrix} \tag{5.2}$$

The general form of equation 5.2 is:

$$R\frac{dX}{dt} = A.X + U \tag{5.3}$$

Therefore,

$$\frac{dX}{dt} = R^{-1}A.X + R^{-1}U \tag{5.4}$$

5.2.2 Simulation Results of GaN-FET's Switching Transient

As mentioned in chapter 3, the proposed circuit equations are nonlinear and time-varying. In order to solve this set of equations, a code has been written in MATLAB. The approach is

dividing the simulation time into several subintervals (n subintervals). Increasing the number of these subintervals leads to more accurate results. In each subinterval, the time-varying coefficients are considered to be constant. Then, using a numerical method, it would be possible to solve the equations in the specific subinterval i. Computing the final values of state variables in the subinterval i eventuates finding the initial conditions for the next subinterval $i+1$. In other words, the time-varying coefficients will be updated for the next subinterval $i+1$ by considering the final values of subinterval i. To run the simulation, it is essential to set the initial conditions with respect to the former state of the switch and diode. The simulation conditions are shown in the following table:

Table 5.1 GaN-FET and SiC-Schottky Diode Simulation Condition

V_D	I_L	$V_{DR}\ (ON/OFF)$	$R_G\ (ON/OFF)$	L_D	L_G	L_S	L_O
$200V$	$10A$	$5V\ /\ -6V$	$10\Omega\ /\ 5\Omega$	$10nH$	$1nH$	$0.3nH$	$1mH$

5.2.2.1 GaN-FET Turn ON Period

To turn the switch ON, it is assumed that the driver voltage change from zero to $5V$ instantaneously. The turn ON waveforms are presented in figures 5.2 to 5.6 .

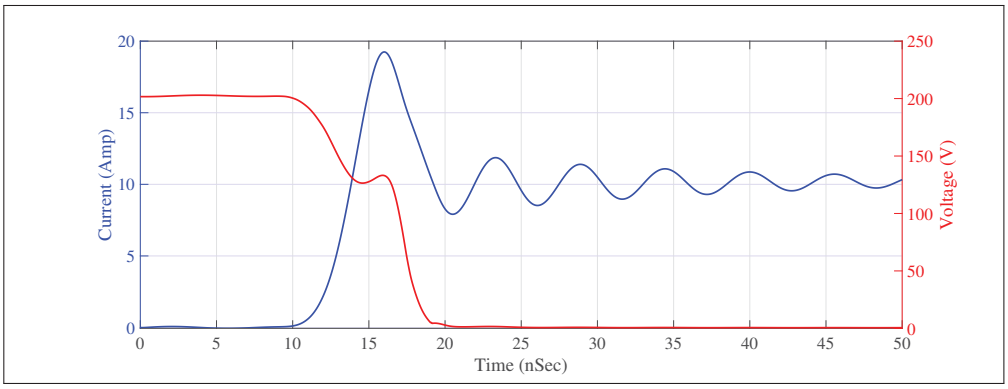


Figure 5.2 Drain-source voltage and drain current of the GaN-FET during turn ON

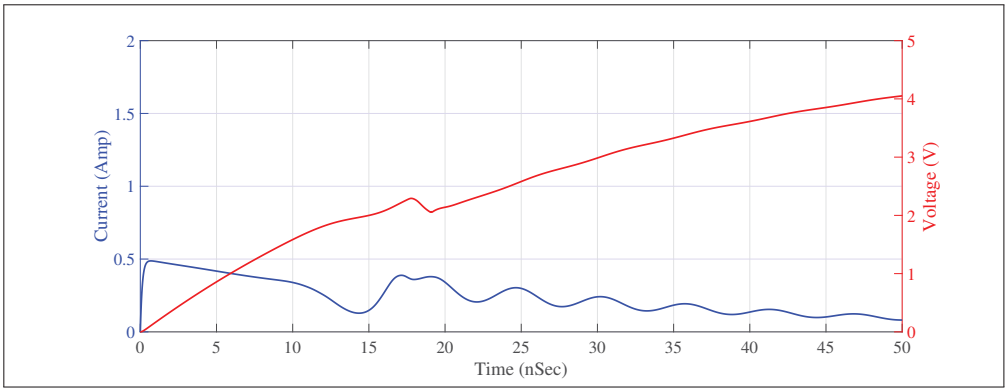


Figure 5.3 Gate-source voltage and gate current of the GaN-FET during turn ON

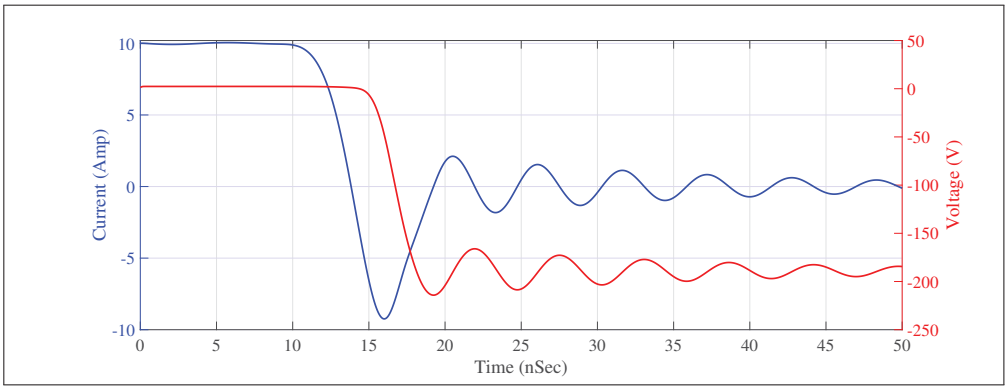


Figure 5.4 SiC Schottky diode voltage and current during the turn OFF period

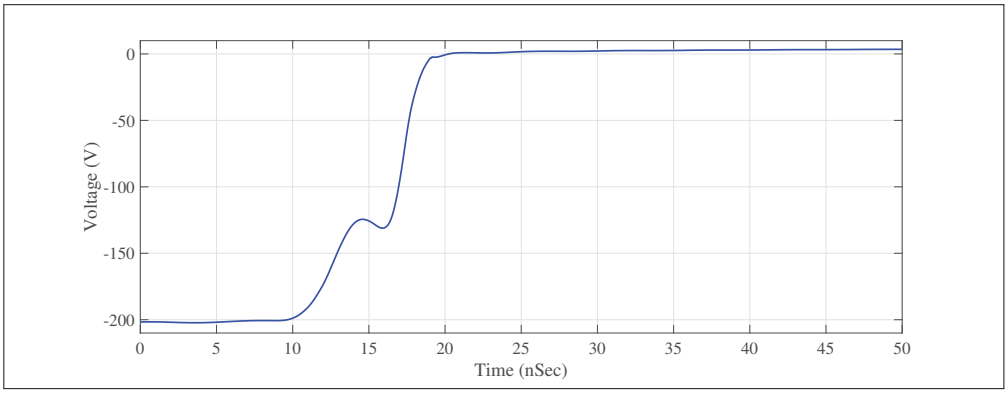


Figure 5.5 Gate-drain voltage of the GaN-FET during turn ON period

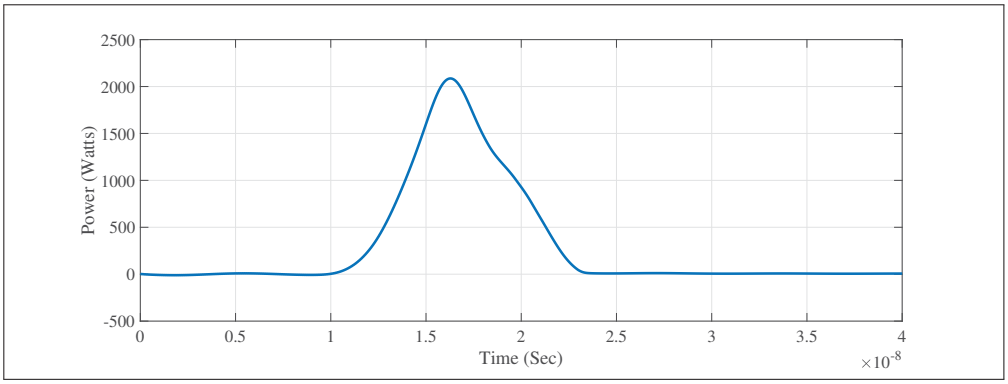


Figure 5.6 Power losses during turn ON transient

Figure 5.3 shows the gate-source voltage of the switch. The first subinterval tooks $10nS$. At $t = 10nS$, V_{gs} is equal to the switch threshold voltage. The current starts to deviate from the freewheeling diode to the drain.

At $t = 14nS$ the drain current reaches its final value, which is $10A$, figure 5.2. Simultaneously, the diode current reaches zero, figure 5.4, and V_{ds} falls to $125V$.

After the point that the diode current reaches zero, there is no reverse recovery period because of the diode type. However, there is an overshoot in the drain current waveform. The reason behind this overshoot is the resonant phenomenon between the drain's stray inductance and GaN-FET output capacitor. This resonant amplitude has been magnified by the low value of the gate circuit resistor (R_g). During this time, the drain-source voltage collapse to its final value $R_{ch}I_d$ namely the ON state voltage.

After the point $t = 20nS$, V_{ds} stay settled on its final value, the drain current has some oscillation before settling on the final value and V_{gs} continues to rise toward the driver ON-voltage V_{DR_On}. Figure 5.6 represents the lost power during this turn ON transient. The total lost energy is $5.1\mu J$.

5.2.2.2 GaN-FET Turn OFF transient Period

The turn OFF period starts with the sudden change of the driver voltage V_{DR} from V_{dsOn} $(5V)$ to V_{dsOff} $(-6V)$. Figures 5.7 to 5.12 are the simulation results for this period of time using the proposed circuit equations 5.2.

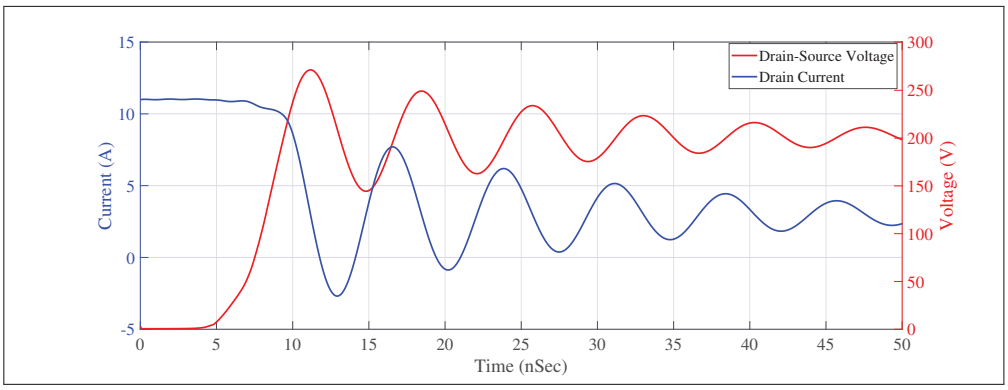


Figure 5.7 Drain-source voltage and drain current of the GaN-FET during turn OFF

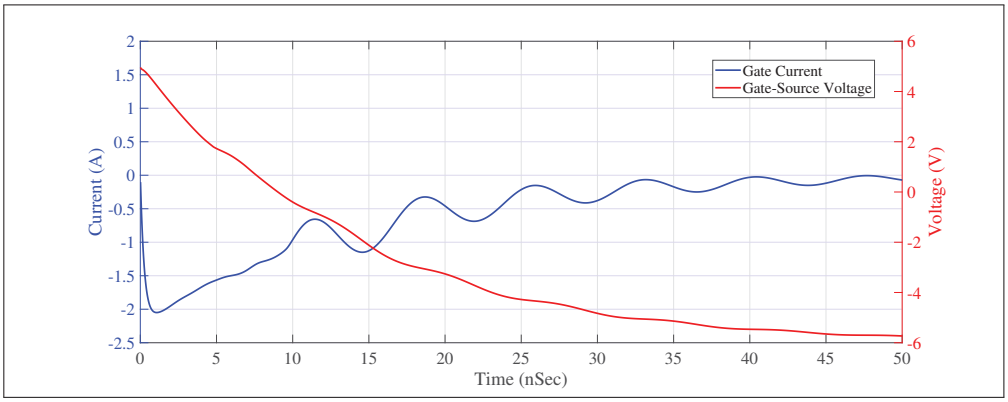


Figure 5.8 Gate-source voltage and gate current of the GaN-FET during turn OFF

In the first subinterval of the turn OFF transient, the gate-source voltage reduces to a level still able to support the drain current as shown in figure 5.8. After $5nS$, the drain current starts to the goes down and V_{ds} starts to increase, as depicted in figure 5.7. Meanwhile, the diode current increases to conduct the load current. Then, both drain current and drain-source voltage reach to zero and V_{out}, respectively, they continue to settle on these final values through some resonances.

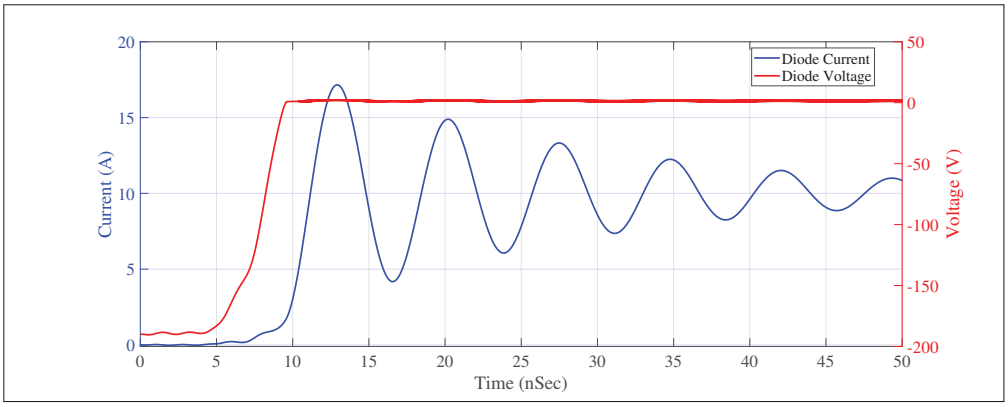


Figure 5.9 SiC Schottky diode voltage and current during the turn ON period

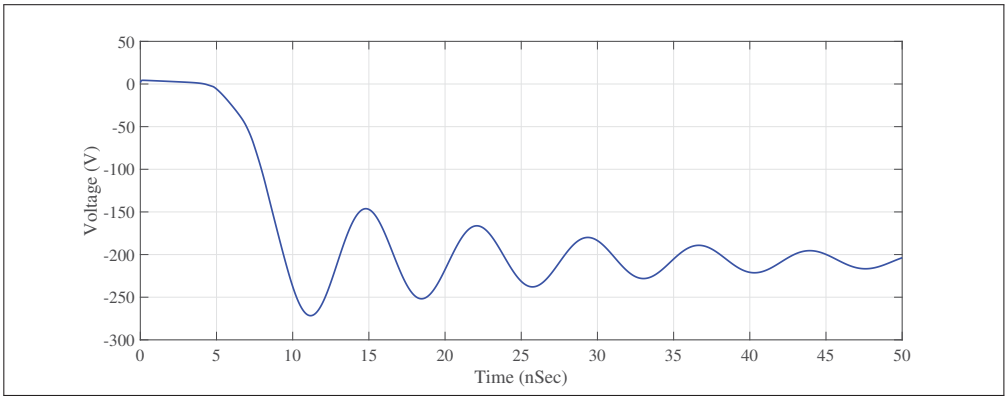


Figure 5.10 Gate-drain voltage of the GaN-FET during turn OFF period

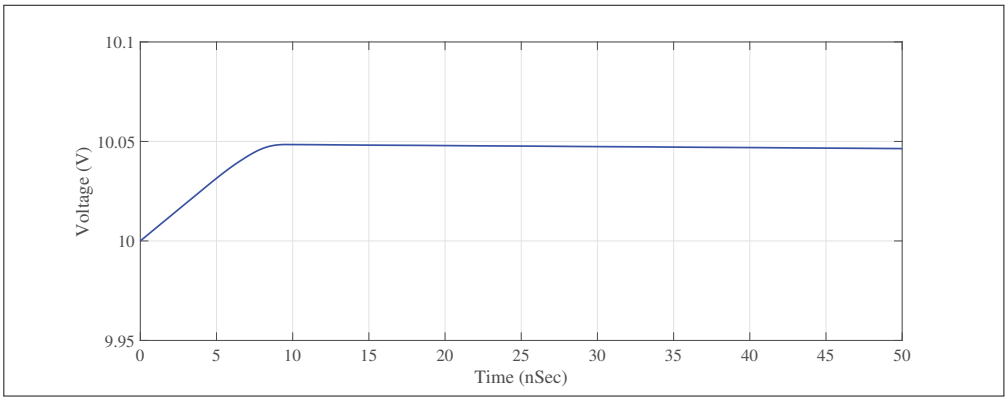


Figure 5.11 Power inductor current during the switch turn OFF transient

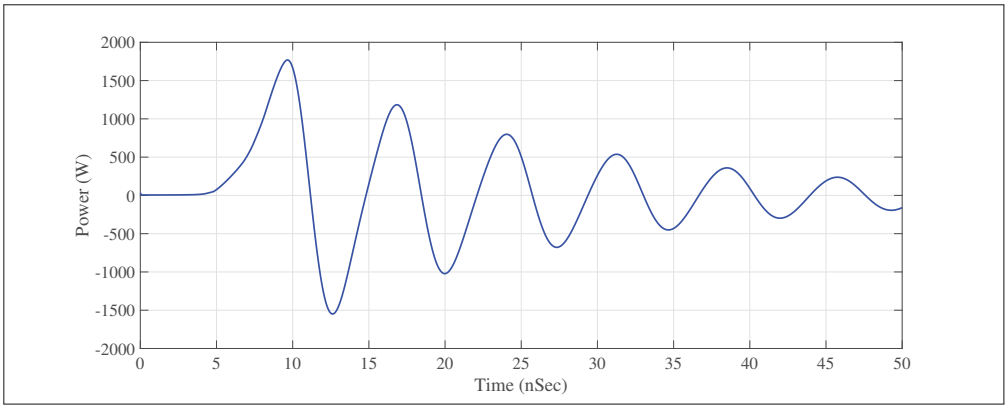


Figure 5.12 Power losses during the GaN-FET turn OFF

The gate-source voltage continues to reduce to $V_{DR_{Off}}$. The value of lost energy during GaN turn OFF is 3.18uj.

5.3 Second Scenario: SiC-MOSFET turn ON transient period with a PiN freewheeling diode

In this section, the switching transient of a SiC-MOSFET with a PiN freewheeling diode has been modeled and simulated. The model introduced in section 5.2.1 should be modified using the PiN power diode model introduced in chapter 2. Using this model, the equivalent circuit model is introduced in figure 5.13.

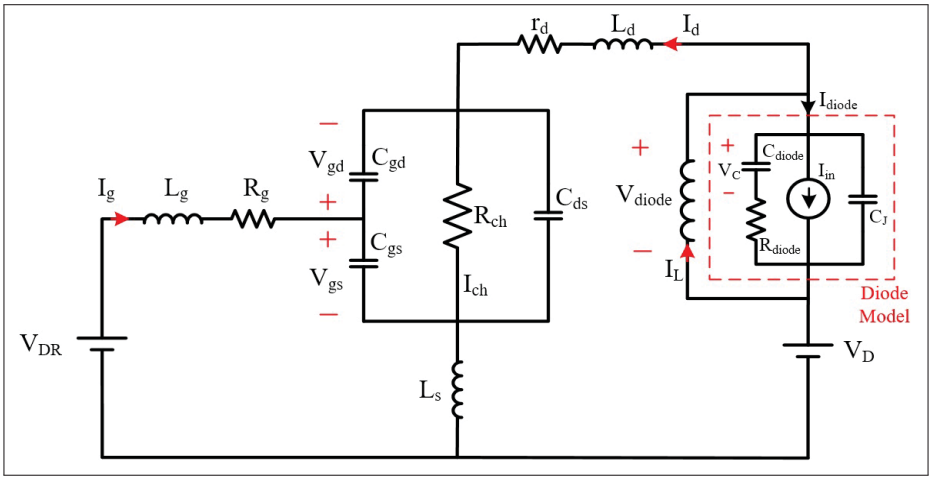


Figure 5.13 Proposed circuit for simulating the switching transients of a SiC-MOSFET and a PiN diode

In this modified model, an *RC* branch has been added to the diode model; therefore, the capacitor's voltage in this branch would be a new state of the circuit. The state vector of the circuit is given by relation 5.5

$$X = \left[V_C, I_L, I_d, I_g, V_{diode}, V_{gs}, V_{gd}\right]^T \tag{5.5}$$

And, the states equations of the circuit will be as follow:

$$\begin{bmatrix} \tau_{rr} & 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & 1 & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & L_d + L_S & L_S & 0 & 0 & 0 \\ 0 & 0 & L_S & L_g + L_S & 0 & 0 & 0 \\ C_{diode} & 0 & 0 & 0 & C_j & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 & C_{ds} & -(C_{ds} + C_{gd}) \\ 0 & 0 & 0 & 0 & 0 & C_{gs} & C_{gd} \end{bmatrix} \frac{d}{dt} \begin{bmatrix} V_C \\ I_L \\ I_d \\ I_g \\ V_{diode} \\ V_{gs} \\ V_{gd} \end{bmatrix} = \begin{bmatrix} -1 & 0 & 0 & 0 & 1 & 0 & 0 \\ 0 & 0 & 0 & 0 & 1/L & 0 & 0 \\ 0 & 0 & -r_d & 0 & 1 & -1 & 1 \\ 0 & 0 & 0 & -R_g & 0 & -1 & 0 \\ 0 & 1 & -1 & 0 & 0 & 0 & 0 \\ 0 & 0 & 1 & 0 & 0 & -1/R_{ch} & 1/R_{ch} \\ 0 & 0 & 0 & 1 & 0 & 0 & 0 \end{bmatrix} \begin{bmatrix} V_C \\ I_L \\ I_d \\ I_g \\ V_{diode} \\ V_{gs} \\ V_{gd} \end{bmatrix} + \begin{bmatrix} 0 \\ 0 \\ V_D \\ V_{DR} \\ -i_{in} \\ 0 \\ 0 \end{bmatrix} \tag{5.6}$$

In this set of equations, parameters I_{in} and C_{diode} have been calculated using equation 2.15.

In section 5.3.1, the simulation results by applying this model are presented. Furthermore, the results are compared with what has been explained in chapter 4 about the switching transient.

5.3.1 Simulation Results of SiC-MOSFET's Switching Transient

By applying the same method introduced in section 5.2.2, it would be possible to solve the set of equations 5.6. The simulation parameters are presented in Table **??**.

Table 5.2 SiC-MOSFET and PiN diode simulation conditions

V_D	I_L	$V_{DR}\ (ON/OFF)$	$R_G\ (ON/OFF)$	L_D	L_G	L_S	L_O
$200V$	$10A$	$20V\ /\ -10V$	$10\Omega\ /\ 5\Omega$	$40nH$	$1nH$	$0.3nH$	$30\mu H$

5.3.1.1 SiC-MOSFET Turn ON Simulation

Again, it is mandatory to set the initial conditions for both turn ON and turn OFF conditions. At $t = 0$, the switch is OFF, and the freewheeling diode conducts the current. Furthermore, all inductors' currents and capacitors' voltages have been considered to be at the steady-state. Considering that, it would be possible to extract the circuit's initial conditions. Table **??** shows the initial conditions for the MOS turn ON.

Table 5.3 SiC-MOSFET turn ON initial conditions

I_L	I_D	I_G	V_C	V_{GS}	V_{GD}
$10A$	$0A$	$0A$	$1.7V$	$0V$	-210

Applying these initial conditions and solving the state equations of the circuit, the turn ON waveforms are presented on figures 5.14 to 5.19.

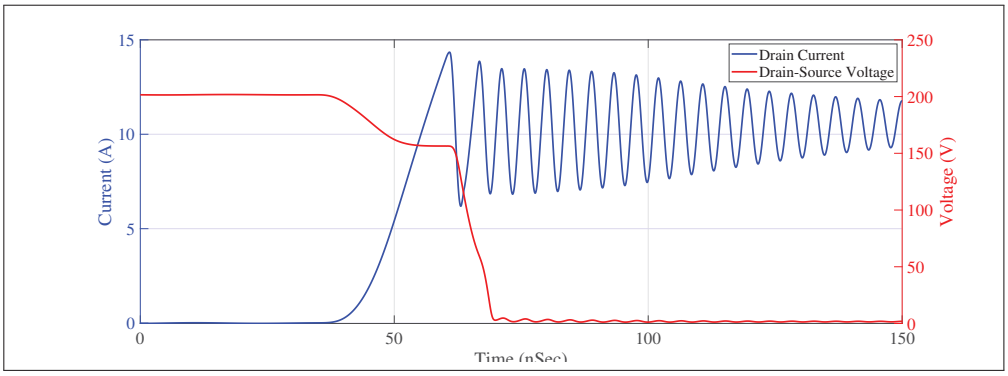


Figure 5.14 Drain-source voltage and drain current of SiC-MOSFET during turing ON transient

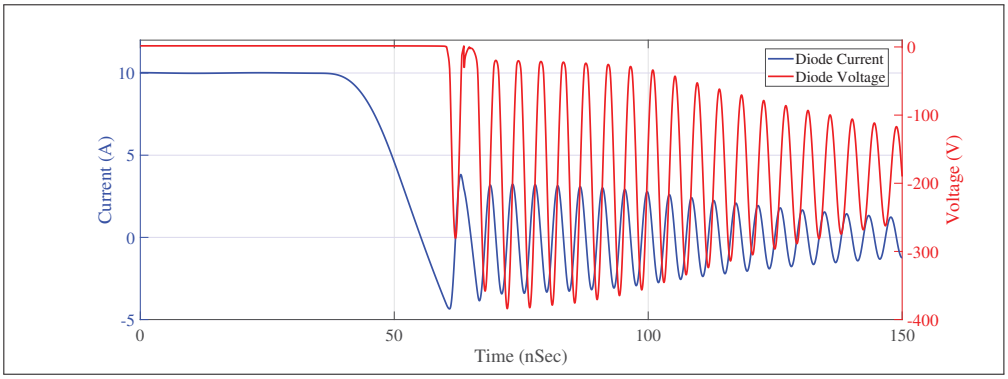


Figure 5.15 PiN diode voltage and current during turn OFF transient (SiC-MOSFET is turning ON)

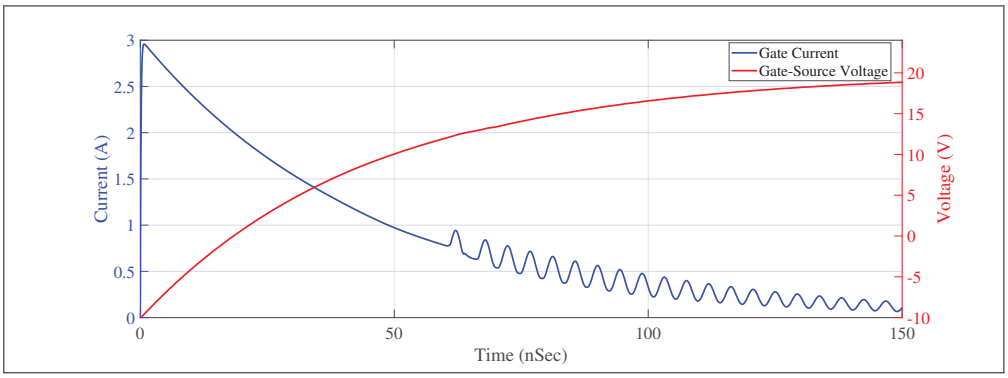


Figure 5.16 SiC-MOSFET gate-source voltage and gate current during turn ON transient

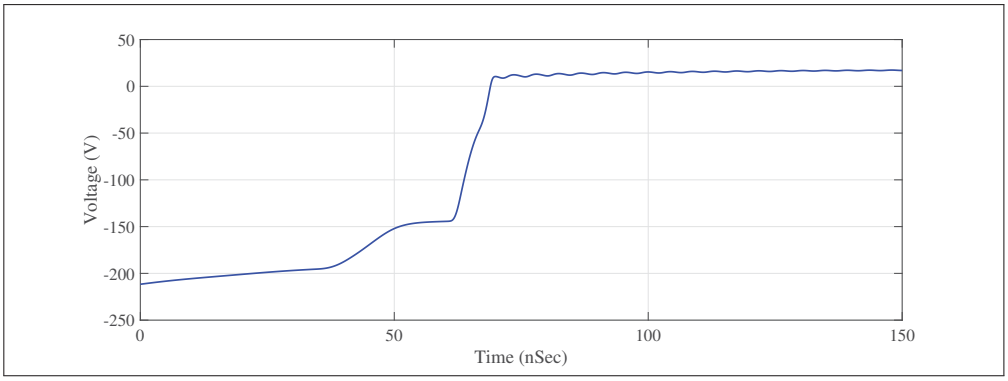


Figure 5.17 SiC-MOSFET gate-drain voltage during the turn ON

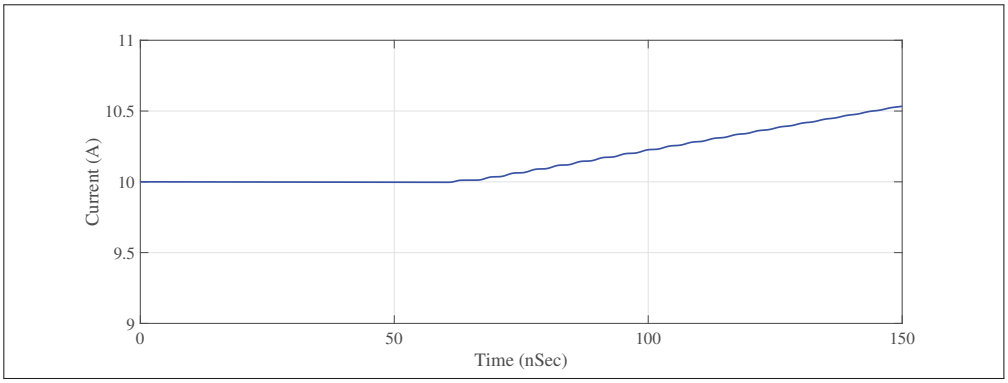


Figure 5.18 Output inductor current during the turn ON

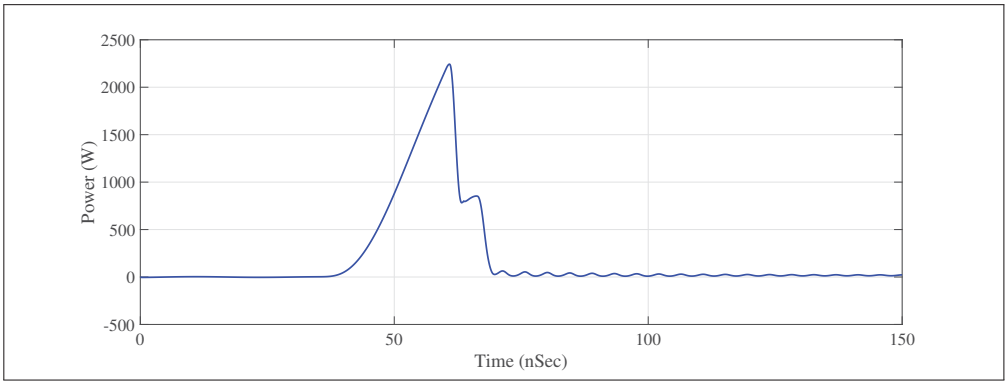


Figure 5.19 SiC-MOSFET's power loss during the turn ON transient

The turn ON transient starts with the delay subinterval which took around 40nS. At the end of this period, V_{gs} reaches the switch's threshold voltage, while I_d and V_{ds} remains constant, as shown in figures 5.14, and 5.16.

During the second subinterval, the load current deviates from the PiN diode into the switch with a high slope. In this subinterval, V_{ds} diminishes around $50V$ and diode voltage remains constant due to the stored charges in its structure, figure. 5.15. The second subinterval ends when I_d is equal to the output inductor current (10A) at t= 55nS. At this point, the freewheeling diode current is zero.

The diode reverse recovery phenomenon dominates the third subinterval. The diode current has a negative peak due to the reverse recovery phenomenon and comes back to zero after that.

During this subinterval, the diode voltage and drain-source voltage remain unchanged. In the fourth subinterval, V_{ds} reduces and settles on its final value $V_{ds_{ON}}$. Also, the drain current reaches I_{out} after some oscillations. The primary source of these oscillations is the resonance of the diode's junction capacitor and the drain's stray inductance. Figure 5.19 represents the lost power during the turn ON transient. The total amount of lost energy during this sequence is $33.8\mu J$.

5.3.1.2 SiC-MOSFET Turn OFF Simulation

Table **??** shows the initial conditions of SiC-MOSFET turn OFF transient simulation. At $t = 0$, the switch is totally ON, and all the output inductor current passes through it. Also, the diode is OFF and its voltage is almost equal to the output voltage. This procedure starts with changing the gate circuit voltage from $V_{DR_{ON}}$ to $V_{DR_{OFF}}$.

Table 5.4 Turn OFF initial conditions

I_L	I_D	I_G	V_{diode}	V_{GS}	V_{GD}
$10A$	$10A$	$0A$	$-180V$	$20V$	-180

The results of simulation are shown in figures 5.20 to 5.25.

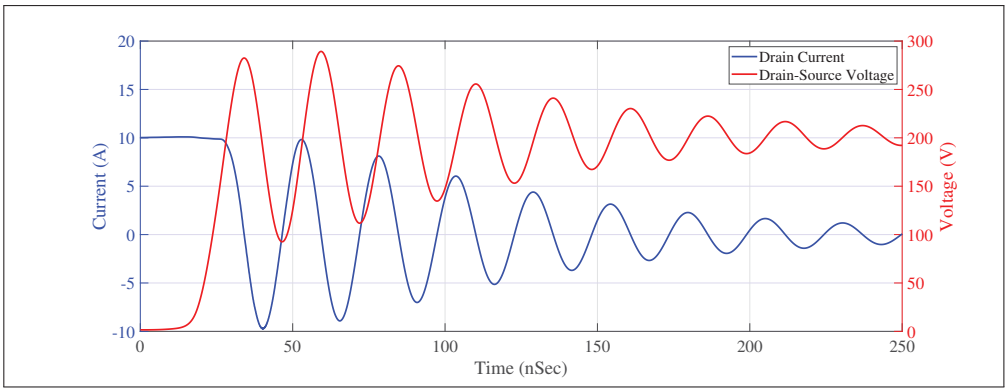


Figure 5.20 Drain-source voltage and drain current of SiC-MOSFET during turning OFF transient

The turn OFF transient begins with the delay subinterval. This subinterval ends after $20nS$. After that, V_{ds} increases rapidly, while the drain current does not change because the freewheeling

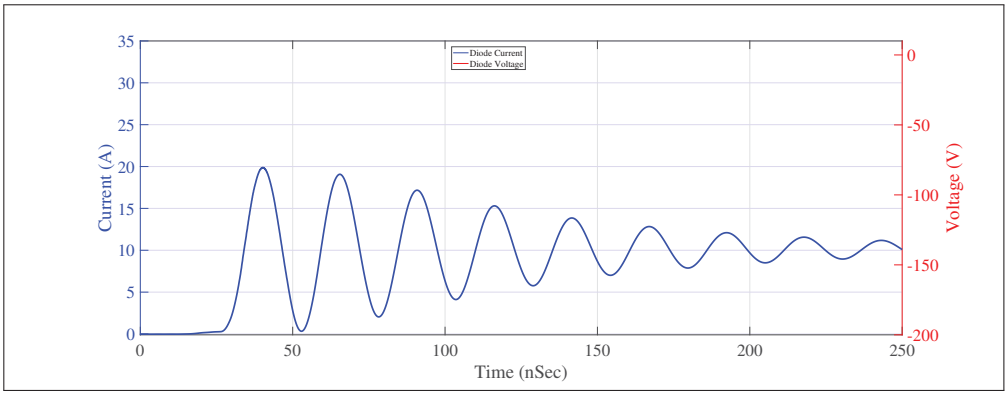


Figure 5.21 PiN diode voltage and current during turn ON transient (SiC-MOSFET is turning OFF)

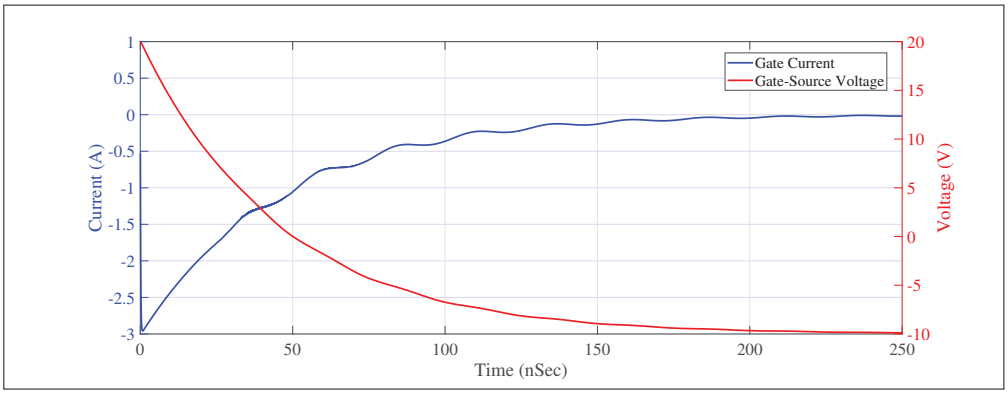


Figure 5.22 SiC-MOSFET gate-source voltage and gate current during turn OFF

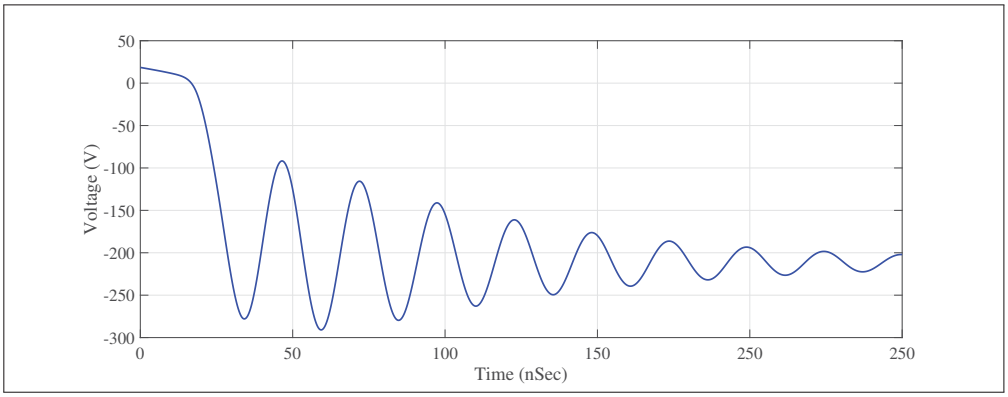


Figure 5.23 SiC-MOSFET gate-drain voltage during the turn OFF

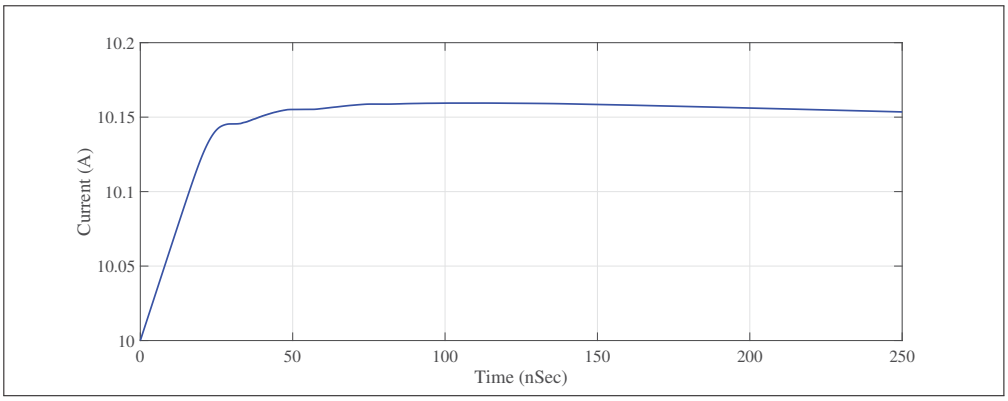


Figure 5.24 Output inductor current during the turn OFF

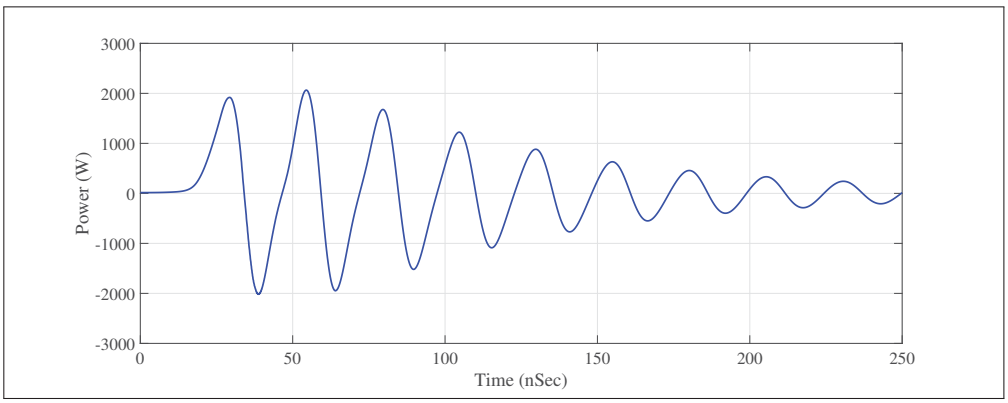


Figure 5.25 SiC-MOSFET's power loss during the turn OFF Transient

diode is reverse biased. When V_{ds} reaches V_{out}, the diode starts to conduct the current, and the drain current starts to decrease. After some oscillations, all parameters reach their final values. The main reason for these oscillations is the resonance between the switch's output capacitor and the drain's stray inductance.

Figure 5.25 shows the lost power during this procedure. The total lost energy is 5.8μJ.

Two mentioned scenarios which have been discussed in this chapter are general forms of the equations. These equations can be revised with respect to the schematic of the circuit. As an example, it is usual to use an isolated ground for the gate driver circuit to eliminate the effect of common mode inductance voltage drop on the gate driver circuit 5.26.

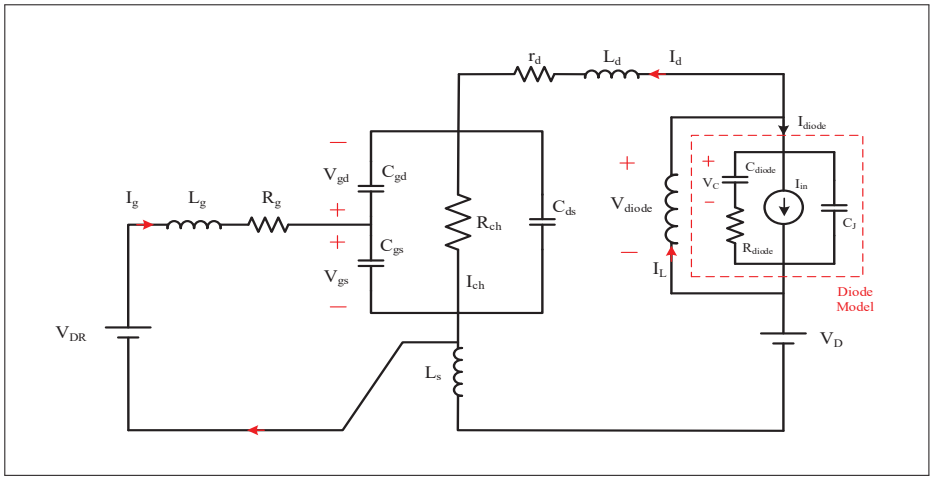


Figure 5.26 Circuit schematic with isolated gate driver ground

In this case the equation should be rewritten based on this change. Therefore, the new set of equation will be as follow:

$$\begin{bmatrix} \tau_{rr} & 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & 1 & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & L_d + L_S & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & L_g & 0 & 0 & 0 \\ C_{diode} & 0 & 0 & 0 & C_j & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 & C_{ds} & -(C_{ds}+C_{gd}) \\ 0 & 0 & 0 & 0 & 0 & C_{gs} & C_{gd} \end{bmatrix} \frac{d}{dt} \begin{bmatrix} V_C \\ I_L \\ I_d \\ I_g \\ V_{diode} \\ V_{gs} \\ V_{gd} \end{bmatrix} =$$

$$\begin{bmatrix} -1 & 0 & 0 & 0 & 1 & 0 & 0 \\ 0 & 0 & 0 & 0 & 1/L & 0 & 0 \\ 0 & 0 & -r_d & 0 & 1 & -1 & 1 \\ 0 & 0 & 0 & -R_g & 0 & -1 & 0 \\ 0 & 1 & -1 & 0 & 0 & 0 & 0 \\ 0 & 0 & 1 & 0 & 0 & -1/R_{ch} & 1/R_{ch} \\ 0 & 0 & 0 & 1 & 0 & 0 & 0 \end{bmatrix} \begin{bmatrix} V_C \\ I_L \\ I_d \\ I_g \\ V_{diode} \\ V_{gs} \\ V_{gd} \end{bmatrix} + \begin{bmatrix} 0 \\ 0 \\ V_D \\ V_{DR} \\ -i_{in} \\ 0 \\ 0 \end{bmatrix} \tag{5.7}$$

The fourth row of this set of equation is related to the gate driver equation. By inspection, one observes that in this new circuit, gate driver dynamic is not a function of L_S. The influence of any other component i.e. diode internal inductance and gate driver capacitors can be taken into account with the same method.

5.4 Experimental Validation

In this section, the simulation results has been compared with the experimental results. The experimental setup is based on the RECOM half-bridge reference design board. By using this half-bridge structure, a 400W buck converter has been designed.

In the subsection 5.4.1, the experimental setup is presented and section 5.4.2 is dedicated to calculation and measurement methods of the stray inductances. In subsection 5.4.3, the simulation results are compared with the experimental waveforms.

5.4.1 Experimental setup

To configure the converter, a RECOM half-bridge reference design board is used. The high side switch is replaced with a PiN power diode (Vishay Semiconductors-VS-HFA15PB60-N3) and the load has connected in parallel with this diode. For the low-side switch a SiC-MOSFET has been used (Infineon-IMZ120R140M1H).

The load is an inductive type consisting of a 13.1Ω resistor in series with a $10mH$ inductor. The input power supply voltage is set to $150V$. The switching frequency and duty-cycle are $50kHz$ and 0.5 respectively. In order to measure the drain current, a trapezoidal-shaped copper wire has been added to the configuration which is called Current Measurement Loop (CML). The CML connects the SiC-MOSFET's source to the ground 5.27. By using a Teledyne LeCroy current prob, the drain current has been measured 5.28.

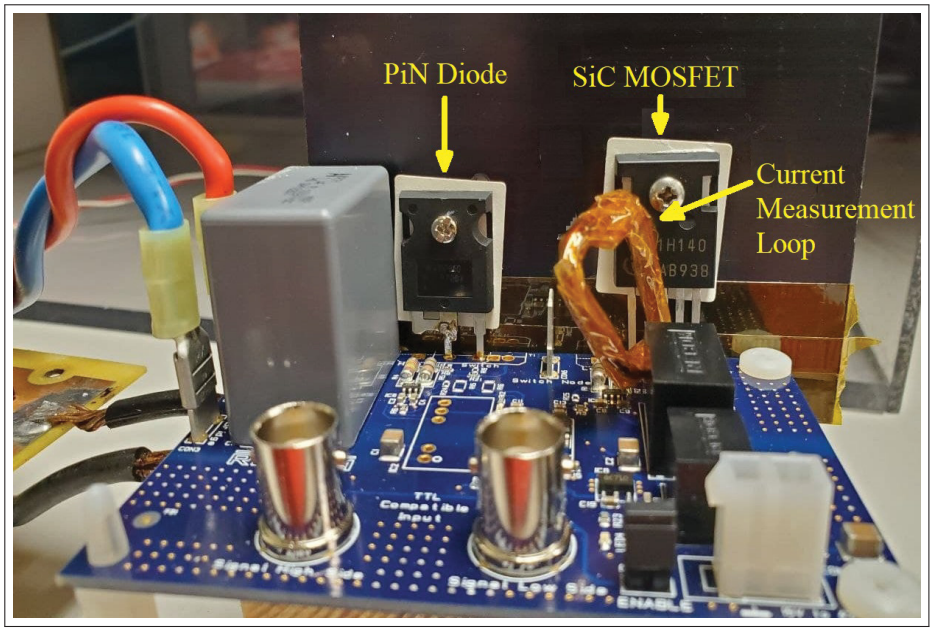


Figure 5.27 Half-bridge configuration with a current measurement loop

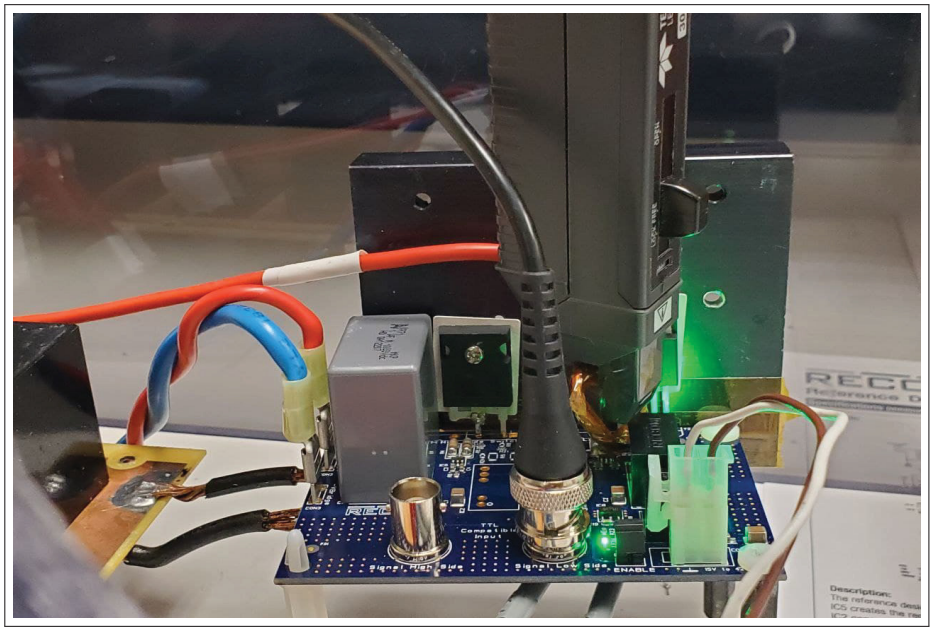


Figure 5.28 Current measurement setup

The isolated DC/DC converter R12P22005D has been used to feed the gate driver IC ZXGD3006E6. The gate driver output voltage levels are $+20V$ for the turn ON and $-5V$ for the turn OFF.

5.4.2 Stray inductance calculation

In order to compare the experimental results with the simulation results, it is needed to find the value of circuit stray inductances. The first method which has been applied is using a Wayne Kerr Precision Magnetics Analyzer 5.29.

Figure 5.29 Wayne Kerr Precision Magnetics Analyzer, series 3260B

This device with Kelvin clips can be used for measurement of very small resistors, inductors and capacitors in a wide frequency range. The measurement has been done for both current loop measurement and PCB power loop. The inductance values are 70.4nH and 49.05nH for CLM and stray inductance of power loop respectively.

The second method, which has been applied is using ANSYS Electronics. ANSYS Electronics provides an environment for electromagnetic/thermal analyze of electro-mechanical systems. Two separate simulations have been run for CMR and PCB, figures 5.30 and 5.31 respectively.

The solver type which is proper for this kind of analyses is EddyCurrent solver and the excitation is solid current type. The maximum mesh elements length is set to be 0.5mm. The obtained values for the CMR inductance are 39nH and 34.6nH for the PCB inductance.

The simulation and measurement values for the inductances have a clear mismatch. It should be noted that finding the exact values for such small parameters always comes with an error. On one hand, it is not possible to add all practical details to the simulation file. On the other hand, the measurement of these parameters contains a percentage of error. Using these techniques can

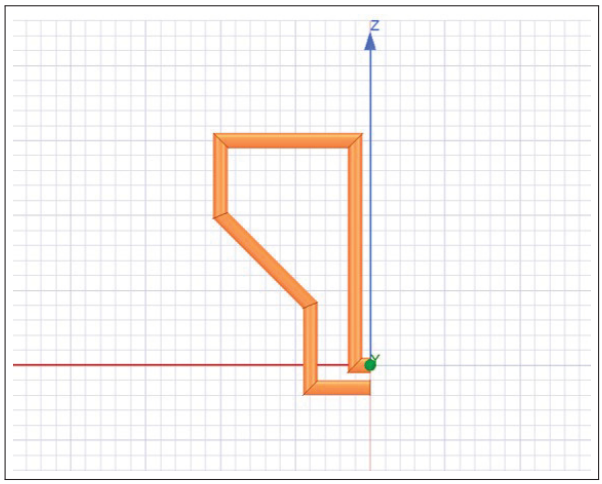


Figure 5.30 Current measurement ring simulation in ANSYS

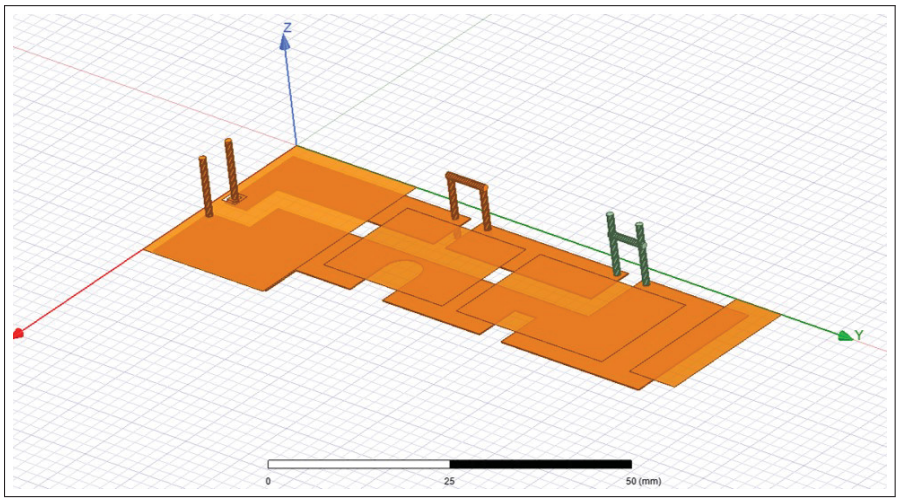


Figure 5.31 PCB simulation in ANSYS

help us to find estimated values for the range of these variables and it is necessary to find the best matched values with some trial and error. In this case, the best achieved values are $70nH$ and $56nH$ for the CMR and PCB inductance respectively.

5.4.3 Comparing Simulation and Experimental Results

The simulation of the converter has been done by using the set of equations A I-14, because of the isolated grounds of gate driver circuits. Figures 5.32 and 5.33 show the drain current and the drain-source voltage for turning ON the switch.

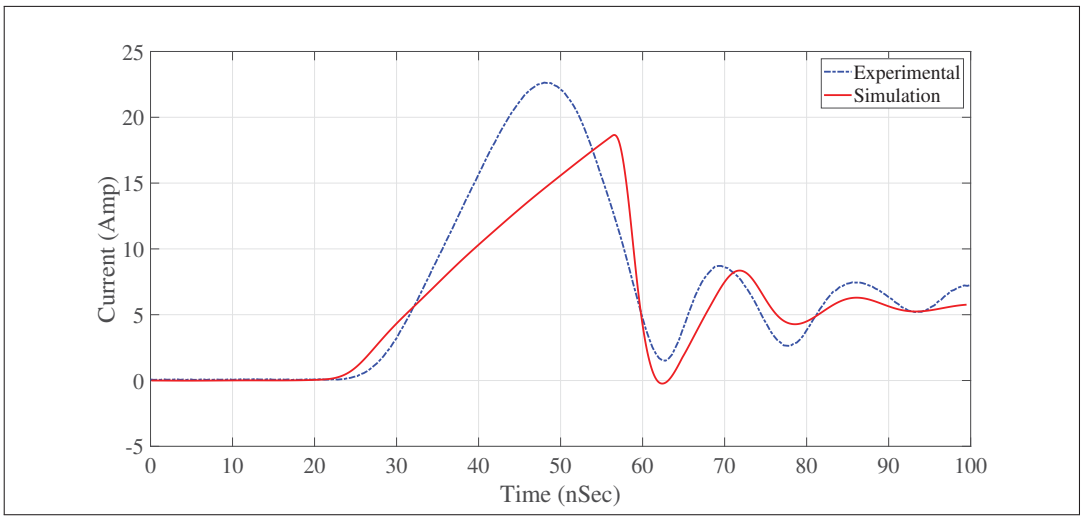


Figure 5.32 SiC-MOSFET drain current during turn ON transient, simulation and experimental results

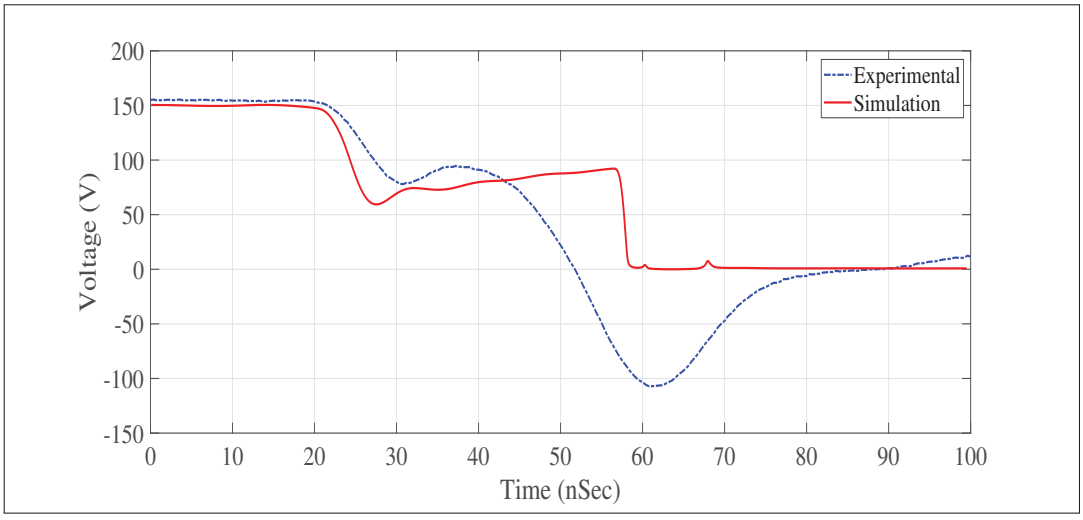


Figure 5.33 SiC-MOSFET drain-source voltage during turn ON transient, simulation and experimental results

The obtained waveforms by the simulation method, which is mentioned in the previous chapter, have an acceptable accuracy in terms of resonant frequency and tracking steady state values. But during the recovery period, there is a difference in between the waveforms. The peak value of the drain current is 15% less than the experimental value. The reason behind these differences can be as follow:

1- The diode model which is used in this simulation is based on some simplifying assumption. These assumption can results in inaccuracy of the model, especially during the recovery period.

2- There is no information in the diode datasheet about the value of the junction capacitor when the diode voltage is between zero to -40V. The junction capacitor is supposed to have a very high values especially when the voltage is close to zero.

Figures 5.34 and 5.35 depicts the drain current and drain-source voltage for both simulation and experimental verification. Considering that there is no recovery period in this interval, the simulation results are very close to the experimental results for both V_{ds} and I_d. The small deviation of these waveforms is attributable to the measurement error of parasitic components.

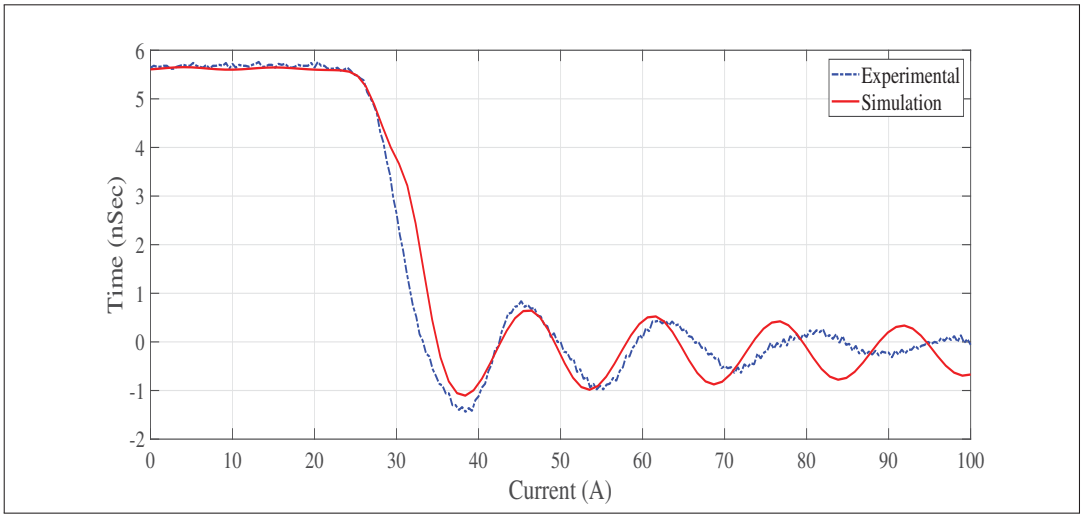


Figure 5.34 SiC-MOSFET drain current during turn OFF transient, simulation and experimental results

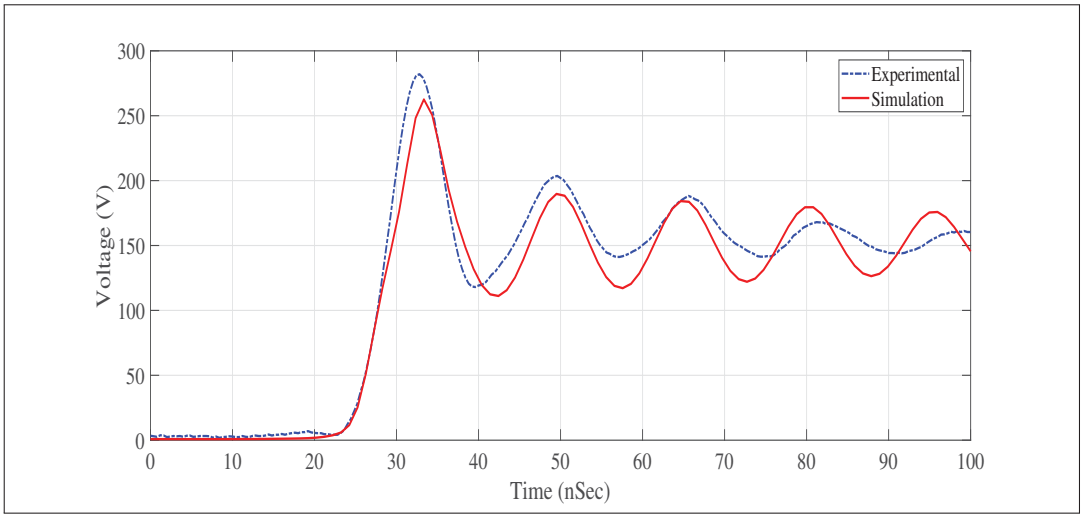


Figure 5.35 SiC-MOSFET drain-source voltage during turn OFF transient, simulation and experimental results

CONCLUSION AND RECOMMENDATIONS

In this research, a new set of equations has been introduced to describe PiN diodes' behavior. The PiN diodes' equivalent circuit has been derived, and its validity checked by simulation. Considering it is a simplified method and some initial assumptions were involved in extracting the equations, the simulation results represented an error compared to the diode's datasheet values. The peak reverse recovery current is 15% less than the value mentioned in the datasheet with the same di/dt value.

In chapter 3 behavioral model is presented for simulation of SiC MOSFETs. The modeling technique, which is based on the convex combination of two vectors, shows excellent compatibility with the datasheet information in steady-state conditions.

A verification method hasbeen developed in chapter 5 by applying the diode and FET's equivalent circuits presented in chapters 2 and 3. The result of using this verification method is a set of time-varying differential equations which can be modified based on the circuit configuration. A lab setup has been designed to compare the simulation results with experimental ones. The results show great similarity between the simulation and experimental results during turn OFF. However, the performance of the model to track the experimental waveforms is degraded during turn ON transient. The main reason behind this accuracy reduction is the diode model performance during the turn OFF.

As mentioned in chapter 2, the equivalent circuit of PiN diode was extracted from some simplified equations, and the nonlinear parameters of these equations were considered constant. These assumptions result in the model's accuracy reduction, especially during the recovery period.

Here are some suggestion for the future works:

Developing a more accurate model for the PiN diodes could be a certain way to increase verification accuracy. The proposed equations do not track the experimental waveforms during

turning ON the switch. As it mentioned, it is because of the simplifying assumption in the process of extracting diode model. Also a more accurate method for extraction of diffusion and recombination coefficients of the diode model could have a great effect on the diode accuracy. Although these coefficient have been considered to be constant in this model, it reality these can be defined with a nonlinear function dependent to the diode instruction and physic.

As the verification method provided a mathematical model for the simulation, investigating on the effect of each circuit parameter on the stability of the system can be other interesting topic. Using such equations, it would be possible to analyse the circuit with a control viewpoint.

Moreover, the proposed method of modeling can be developed for the parallel switches. Quantifying and providing a solution for asynchronous operation of the parallel switches can be a less challenging task to do using this model.

APPENDIX I

DERIVING THE STATES' EQUATIONS FOR VERIFICATION STEP

Figure I-1 depicts the proposed circuit for verification step. As it is mentioned in chapter 5, the states variables are $V_C, I_L, I_d, I_g, V_{diode}, V_{gs}$, and V_{gd}. The states equations can be written by writing the KVL and KCL equations in the loops and nodes specified in the figure I-1.

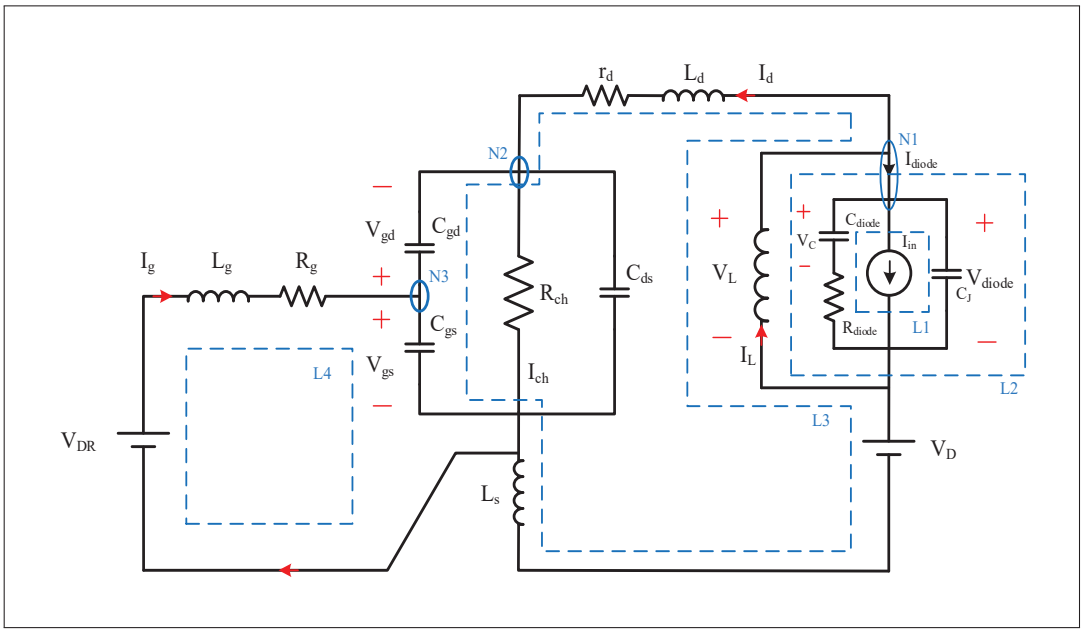


Figure-A I-1 Proposed circuit for verification step containing the loops and nodes presentation

Starting with loop $L1$, we have:

$$V_{diode} = V_C + R_{diode} I_C \tag{A I-1}$$

and

$$I_C = C_{diode} \frac{dV_C}{dt} \tag{A I-2}$$

Considering set of equations 2.15, $R_{diode} C_{diode}$ is equal to τ_{rr} ;therefore, first state equation is:

$$\tau_{rr}\frac{dV_C}{dt} = V_{diode} - V_C \tag{A I-3}$$

Also the output inductor voltage is equal to the diode voltage (Loop L2), so second state equation is:

$$L_O\frac{dI_L}{dt} = V_{diode} \tag{A I-4}$$

writing KVL for the loop L3:

$$-V_D - V_{diode} + L_d\frac{dI_d}{dt} + r_dI_d - V_{gd} + V_{gs} + L_s\frac{dI_d}{dt} = 0 \tag{A I-5}$$

Therefore, third state equation is:

$$(L_d + Ls)\frac{dI_d}{dt} = V_{diode} + V_{gd} - V_{gs} - r_dI_d + V_D \tag{A I-6}$$

Last KVL is in loop L4:

$$-V_{DR} + R_gI_g + L_g\frac{dI_g}{dt} + V_{gs} = 0 \tag{A I-7}$$

And forth state equation is:

$$L_g\frac{dI_g}{dt} = -R_gI_g - V_{gs} + V_{DR} \tag{A I-8}$$

The following equation can be achieved by writing KCL at node N1:

$$I_d - I_L + C_{diode}\frac{dV_C}{dt} + I_{in} + C_j\frac{dV_{diode}}{dt} = 0 \tag{A I-9}$$

The fifth state equation will be:

$$C_{diode}\frac{dV_C}{dt} + C_j\frac{dV_{diode}}{dt} = -I_d + I_L - I_{in} \tag{A I-10}$$

The nodal equation at node N2 is:

$$-I_d - C_{gd}\frac{dV_{gd}}{dt} + \frac{V_{gs} - V_{gd}}{R_{ch}} + C_{ds}\frac{d(V_{gs} - V_{gd})}{dt} = 0 \tag{A I-11}$$

The sixth equation is:

$$C_{ds}\frac{dV_{gs}}{dt} - (C_{gd} + C_{ds})\frac{dV_{gd}}{dt} = I_d - \frac{1}{R_{ch}}V_{gs} + \frac{1}{R_{ch}}V_{gd} \tag{A I-12}$$

And last state equation can be gained by writing KCL at node N3:

$$I_g = C_{gd}\frac{dV_{gd}}{dt} + C_{gs}\frac{dV_{gs}}{dt} \tag{A I-13}$$

By writing these seven state equation in the matrix form, the result will be:

$$\begin{bmatrix} \tau_{rr} & 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & L_o & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & L_d + L_S & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & L_g & 0 & 0 & 0 \\ C_{diode} & 0 & 0 & 0 & C_j & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 & C_{ds} & -(C_{ds} + C_{gd}) \\ 0 & 0 & 0 & 0 & 0 & C_{gs} & C_{gd} \end{bmatrix} \frac{d}{dt} \begin{bmatrix} V_C \\ I_L \\ I_d \\ I_g \\ V_{diode} \\ V_{gs} \\ V_{gd} \end{bmatrix} =$$

$$\begin{bmatrix} -1 & 0 & 0 & 0 & 1 & 0 & 0 \\ 0 & 0 & 0 & 0 & 1 & 0 & 0 \\ 0 & 0 & -r_d & 0 & 1 & -1 & 1 \\ 0 & 0 & 0 & -R_g & 0 & -1 & 0 \\ 0 & 1 & -1 & 0 & 0 & 0 & 0 \\ 0 & 0 & 1 & 0 & 0 & -1/R_{ch} & 1/R_{ch} \\ 0 & 0 & 0 & 1 & 0 & 0 & 0 \end{bmatrix} \begin{bmatrix} V_C \\ I_L \\ I_d \\ I_g \\ V_{diode} \\ V_{gs} \\ V_{gd} \end{bmatrix} + \begin{bmatrix} 0 \\ 0 \\ V_D \\ V_{DR} \\ -i_{in} \\ 0 \\ 0 \end{bmatrix} \quad \text{(A I-14)}$$

The same method can be applied to consider the effect of any changes in the circuit configuration.

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