Harmonic Tuned GaN-based Power Amplifiers with Enhanced Efficiency, Bandwidth and Thermal Management

by

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FOREWORD

This thesis is written as completion to Ph.D. in electrical engineering, at École de technologie supérieure. Author worked on the subject since May 2017 to August 2021. The content is the original work of its author Sina Eskandari.

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Amplificateurs de puissance GaN à réglage d'harmoniques avec une efficacité, une bande passante et une gestion thermique améliorées

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RÉSUMÉ

Les amplificateurs de puissance (PA) à large bande et à haute efficacité sont de plus en plus demandés pour les nouveaux standards de communication sans fil afin de répondre aux exigences d'efficacité spectrale élevée et d'intégration dans les modules frontaux (FEM) et les systèmes d'antennes actives à entrées multiples et sorties multiples (MIMO). Les amplificateurs de puissance modernes sont donc développés pour répondre aux exigences d'une bande passante opérationnelle étendue avec des débits de données de pointe accrus, mais ils souffrent toujours d'inefficacités résultant de réseaux d'adaptation compliqués et d'une grande dissipation de puissance dans les dispositifs actifs. Ces facteurs peuvent dégrader le rendement énergétique et la linéarité et augmenter la densité thermique, en particulier pour les amplificateurs de puissance à puissance élevée (HPA), ce qui affecte les performances et la fiabilité globales des émetteurs. Pour relever ces défis, une approche à deux volets est adoptée dans cette thèse : (i) des nouvelles techniques pour augmenter l'efficacité énergétique et réduire la charge thermique sur de larges bandes passantes sont proposées et (ii) des techniques de gestion thermique efficaces sont étudiées.

Tout d'abord, pour améliorer l'efficacité énergétique tout en augmentant la bande passante, de nouveaux réglages d'impédance harmonique à l'entrée du dispositif sont développés pour deux classes d'opération distinctes : la classe GF inverse en mode continu (CCGF-1) et la classe GF continue (CCGF). Pour le CCGF-1, nous proposons une nouvelle expression du courant de drain à forme fermée pour modéliser les formes d'onde du courant du PA dans le domaine temporel. Nous utilisons ensuite cette expression analytique pour exploiter la manipulation de l'impédance harmonique de la seconde source afin d'étendre l'espace de conception du circuit d'adaptation de sortie de manière résistive. Cette approche permet de réduire la complexité de la conception du réseau d'adaptation de charge aux fréquences fondamentales et harmoniques et d'obtenir une plus grande largeur de bande tout en améliorant simultanément l'efficacité du drain à travers les nouveaux points d'admittance optimaux. Comme preuve de concept, un PA CCGF-1 à large bande est conçu, fabriqué et testé. Les résultats montrent une efficacité de drain de plus de 70% de 3.05 GHz à 3.85GHz, un gain entre 11 et 12.4 dB avec une planéité de gain de ± 0.7 dB et une puissance de sortie à 3-dB de compression de gain entre 39.9 et 41.4 dBm sur la même bande de fréquence. Pour le CCGF, la deuxième harmonique de source est optimisée de manière similaire pour aplanir la réponse en fréquence de l'amplificateur de puissance sur une large gamme de fréquences. De plus, un nouvel espace de conception est exploré en considérant les effets du contrôle de la non-linéarité d'entrée de la capacité grille-source (Cgs) sur les formes d'onde du courant de drain sous des formes d'onde de tension de drain en mode continu. Contrairement au mode CCGF-1 où un dépassement de courant peut se produire, les formes d'onde de courant de drain obtenues en mode CCGF ne dépassent pas le courant de drain maximal. Étant donné que le dépassement de courant peut affecter négativement la fiabilité du dispositif dans le temps tout en augmentant simultanément le

chevauchement avec la forme d'onde de tension en mode continu, évitant le chevauchement en passant au mode CCGF atténuera ces problèmes. Un deuxième prototype de preuve de concept d'un PA CCGF est également conçu, fabriqué et testé. Les mesures montrent une réponse en fréquence plate de 3,3 GHz à 4,3 GHz avec des variations inférieures à ± 0,4 dB pour une puissance de sortie de 40 dBm, et ± 2 % pour une efficacité de drain de 66 %.

La gestion thermique efficace des HPA est entreprise à travers la conception, la fabrication, l'intégration et le test d'un amplificateur en bande C de 40 W. Deux approches alternatives sont étudiées: (i) l'intégration d'une conception de PA à puce unique MMIC (Monolithic Microwave Integrated Circuit) existante, où l'adaptation et la combinaison de puissance sont effectuées sur la puce, sur un boîtier de dissipateur thermique et (ii) la conception de PA hybride où les barres de puissance MMIC de plus faible puissance sont adaptées et combinées hors puce en utilisant la technologie multicouche LTCC (Low Temperature Cofired Ceramics) à faibles pertes et montées dans une structure de gestion thermique optimisée. Il est démontré qu'en utilisant des intercalaires hautement thermoconducteurs avec un coefficient d'expansion thermique correctement adapté, à savoir le cuivre-graphite, ainsi que des cavités dans le LTCC et une base en cuivre, l'approche hybride apporte des améliorations significatives dans la gestion thermique. En effet, les images thermiques de la surface de la puce montrent une amélioration de 10 à 15 °C de la gestion thermique de l'amplificateur de puissance hybride par rapport à l'amplificateur de puissance MMIC au même niveau de puissance de sortie saturée.

Mots-clés : amplificateur de puissance en mode continu, CCGF, CCGF^{-1}, GaN, PA accordé harmonique, haute efficacité, LTCC, manipulation d'harmoniques de deuxième source, gestion thermique.

Harmonic tuned GaN-based power amplifiers with enhanced efficiency, bandwidth and thermal management

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ABSTRACT

High efficiency broadband power amplifiers (PAs) are increasingly in demand for the novel wireless communication standards to meet the high spectral efficiency and integration requirements in front-end modules (FEMs) and massive multiple input multiple output (MIMO) active antenna systems. Modern PAs are therefore developed to address extended operational bandwidth requirement under increased peak data rates but still suffer from inefficiencies resulting from complicated matching networks and large power dissipation in the active devices. These can degrade the power efficiency and linearity performance and increase the heat density, particularly for high power PAs (HPAs), which in turn affects the overall performance and reliability of transmitters. To address these challenges, a two-pronged approach is taken in this thesis: (i) novel techniques to increase power efficiency and reduce the thermal load over wide bandwidths are proposed and (ii) efficient thermal management techniques are investigated.

First, to enhance power efficiency while increasing bandwidth novel harmonic impedance tuning at the device input are developed for two distinct classes of operation: continuous-mode inverse class GF ($CCGF^{-1}$) and the continuous class GF (CCGF). For the $CCGF^{-1}$, we propose new closed-form drain current expression to model the PA current waveforms in the time domain. We then use this analytical expression to exploit second source harmonic impedance manipulation in order to expand the design space of the output matching circuit resistively. This approach allows to diminish the complexity of the design of the load matching network at the fundamental and harmonic frequencies and to achieve wider bandwidth while simultaneously improving drain efficiency across the new optimum admittance points. As a proof of concept, a wideband $CCGF^{-1}$ PA is designed, fabricated and tested. Results show a drain efficiency of more than 70% from 3.05 GHz to 3.85GHz, a gain between 11 and 12.4 dB with a gain flatness of ± 0.7 dB and an output power at 3-dB gain compression between 39.9 and 41.4 dBm over the same frequency band. For the CCGF, the second source harmonic in CCGF is similarly optimized to flatten the power amplifier's frequency response over a wideband range. Moreover, a new design space is explored by considering the effects of controlling the input nonlinearity of the gate-source capacitance (C_{gs}) on the drain current waveforms under continuous mode drain voltage waveforms. Unlike the $CCGF^{-1}$ mode where current overshoot can occur, the obtained drain current waveforms in the CCGF mode do not exceed the maximum drain current. Since the current overshoot can negatively affect the reliability of the device over time while simultaneously increasing the overlap with the voltage waveform in continuous mode, avoiding it by going to the CCGF mode will alleviate these problems. A second proof of concept prototype of a CCGF PA is also designed, fabricated and tested. Measurements show a flat frequency response from 3.3 GHz to 4.3 GHz with variations less than ± 0.4 dB for 40 dBm output power, and ± 2% for 66% drain efficiency.

The efficient thermal management of HPAs is undertaken through the design, fabrication, integration and testing of a 40 W C-band amplifier. Two alternative approaches are investigated: (i) the integration of an existing single MMIC (Monolithic Microwave Integrated Circuit) chip PA design, where matching and power combining are carried out on-chip, on a heat-sink housing and (ii) the hybrid PA design where lower power MMIC power-bars are matched and combined off-chip using low-loss multi-layer LTCC (Low Temperature Cofired Ceramics) technology and mounted in an optimized thermal management structure. It is shown that by using highly thermally conductive interposers with properly matched thermal expansion coefficient, namely copper-graphite, along with cavities in the LTCC and a copper base, the hybrid approach yields significant improvements in thermal management. Indeed, thermal images from the chip surface show 10-15 °C better thermal management of the hybrid HPA compared to MMIC HPA at the same saturated output power level.

Keywords: continuous-mode power amplifier, CCGF, $CCGF^{-1}$, GaN, harmonic tuned PA, high efficiency, LTCC, second source harmonic manipulation, thermal management.

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LIST OF ABREVIATIONS

2DEG	Two-dimensional electron gas
3D	Three dimensional
4G	Fourth generation
5G	Fifth generation
ACPR	Adjacent channel power Ratio
ADS	Advanced design system
AM/AM	Amplitude to amplitude modulation
AM/PM	Amplitude to phase modulation
CCF	Continuous-mode class F
CCF^{-1}	Continuous-mode inverse class F
CCGF	Continuous-mode class GF
$CCGF^{-1}$	Continuous-mode inverse class GF
CW	Continuous wave
DC	Direct current
DE	Drain efficiency
ÉTS	École de technologie supérieure
EM	Electromagnetic
FEM	Front-end modules
FET	Field effect transistor
GaAs	Gallium arsenide
GaN	Gallium nitride
HEMT	High electron mobility transistors

HFSS	High frequency structure simulator
IEEE	Institute of electrical and electronics engineers
HPA	High power amplifier
IMN	Input matching network
LACIME	Laboratoire de communications et d'Intgration de la microlectronique
LTCC	Low temperature co-fired ceramic technology
LTE	Long-term evolution
MIMO	Massive multiple input multiple output
MMIC	Monolithic microwave integrated circuit
PA	Power amplifier
PCB	Printed circuit bord
RF	Radio frequency
RFPA	Radio frequency power amplifier
SiC	Silicon carbide
UMS	United monolithic semiconductors

LIST OF SYMBOLS

α	Conduction angle
β	Zero-crossing cutoff angle
γ	Ratio of second harmonic to fundamental voltage at device input
δ	Continuous mode factor
f_c	Cut-off frequency
f_0	Center frequency
ω	Angular frequency

INTRODUCTION

0.1 Motivation and Context

Wireless communication technologies have transformed many of aspects of our daily lives and now touch virtually all economic sectors. Their spectacular growth over the last couple of decades is set to continue into the foreseeable future. However, this growth comes with several significant challenges two of which, spectral and power efficiencies, are critical for economic, but more importantly sustainability, considerations. Indeed, the need for improving spectral efficiency is easily understood given the fact that the electromagnetic spectrum is a limited non-renewable resource while the amount of data to be transferred continues to grow. Power efficiency, on the other hand, is directly linked to energy consumption and consequently to the cost of operating wireless devices and networks and to their growing impact on the environment. In this context, power amplifiers (PAs), which are key components in all transmitters, are typically responsible for 40% or more of the power consumption in all fixed and mobile terminals. This issue is compounded by the sheer number of PAs need as massive multiple input multiple output (MIMO) active antenna systems are increasingly deployed to provide greater capacity enhancement of data traffic in wireless networks. Providing energy and spectrally efficient communications therefore requires power amplifiers that are both wideband and power-efficient. These needs make it necessary to incorporate efficiency enhancement techniques that reduce dissipated power in the design of broadband PAs. Furthermore, it is important to note that the overall performance and reliability of wireless transmitters can be significantly affected by the heat dissipated from radio frequency power amplifiers (RFPAs). Therefore, to reduce heat generation and improve power efficiency, it is critical for wideband PAs in 4G/5G systems to efficiently generate the required power by using low complexity matching networks in combination with low-loss transmission line technologies.

There are different efforts being deployed in the literature to address these challenges with varying degrees of success. One can name Doherty with DPD, linear amplification using

nonlinear components (LINC), envelope elimination and restoration (EER) etc. Among these techniques, engineering harmonic waveforms has shown good promise to be able to provide good efficiency performance by shaping the drain current and voltage waveforms. This technique reduces power dissipation by minimizing the overlap between the current and voltage waveforms. However, the theory of harmonic tuning is based on precise open and short impedance values at harmonic frequencies, which makes them inherently narrow band, hence not suitable to meet the 4G/5G efficiency and bandwidth requirements. In this context, emerging continuous mode power amplifiers have provided multiple solutions for simplifying the design of wideband matching networks and expanding the operational bandwidth in PA design. On the other hand, in continuous mode PAs, the imaginary part of the optimum fundamental load impedance can be variable on the constant resistive circles of the Smith chart and the second harmonic load is tuned on the edge of Smith chart instead of the fixed shorted or opened circuits. This can offer wider bandwidth performance with comparable efficiency by providing more flexibility with respect to the harmonic impedances. Such a flexibility of harmonic tuning in the theory of continuous mode PAs was limited to output matching networks including the phase variations for the fundamental and second harmonics along constant resistance circles in the Smith chart. While the optimum load trajectory at the output of device varies resistively and there is need to explore more flexibility in this area to simplify the output matching network and improve efficiency performance over the operational band width.

Moving to higher frequency in order to expand operational bandwidth is inevitable in the novel front-end transceivers. Although, at higher frequencies we need to overcome more severe propagation challenges such as path loss between transmitting and receiving antennas, penetration loss and diffraction loss. Therefore, the new generation front-end chains must be able to produce the required electromagnetic power at sub 6 GHz and millimeter wave frequency ranges to deliver the minimum detectable signal power to the enormous numbers of connected devices. The communication links and their massive MIMO antennas should be driven by more front-end chains with each including PA, Mixer, LNA, etc. to have higher performance. Therefore, they need high power signals in small packed area to feed the large

number of antennas elements. This will require a technology which can offer a large level of output power at a small space, efficiently. Before the emerging of the wide bandgap gallium nitride (GaN) transistors, systems suffered from low efficiency of high power amplifiers (HPAs) due to low voltage operating of the semiconductors like gallium arsenide (GaAs) and Silicon (Si) to generate the required power of transmitters. Therefore, there was need to use parallel PAs with larger periphery of gate area which led to consuming more current to generate the required output power and lower output impedance which made the matching networks more complicated and lossy. While the inherent features of GaN technology, such as wide bandgap energy and high breakdown voltage, high charge density and mobility at two-dimensional electron gas (2DEG) channel, high thermal conductivity of Silicon Carbide (SiC), make it appropriate choice to meet the considerable power density requirements of the novel wireless networks.

To realize the wideband PA based on the novel design techniques in this thesis we utilized ceramic technology for implementing the matching networks like low temperature co-fired ceramic (LTCC). This technology provides lower loss at higher frequency and benefits from integration capability with the other components of front-end chain compared to conventional printed circuit bords (PCBs). The combination of relatively high permittivity low-loss dielectrics and high conductivity metals like silver and gold make LTCC a well-suited technology for implementing the high-power transmission lines at input and output matching networks of PA.

The power-hungry transceivers in novel wireless systems have always faced thermal issues, mostly due to the heat generated by the power lost in the PAs within a small space of the front-end chain. This could be more critical using the multi-layer PCB substrates such as FR-4, CEM-1, G-10, Alumina, etc. that need to make cavity holes for mounting chips directly on the circuit ground or the embedded thermal vias to transfer the heat generated underneath of active devices. Furthermore, it is quite important to immediately transfer the heat to the ground layers and keep the chip temperature under the recommended values that released by the fabricant companies. However, realizing efficient thermal transformation systems, either using thermal

vias or cavities, through multilayer fabrication technologies such as LTCC have been challenging and need to be explored for practical solutions.

0.2 Challenges and Problem Statement

As discussed earlier, the design space flexibility offered by the continuous mode theory is limited to phase variations for the fundamental and second harmonics along constant resistance circles in the Smith chart. This limitation leads to degraded performance at the middle or edges of the bandwidth due to impedance mismatch caused by the variation of resistive part of the optimum fundamental impedance with frequency. In literature, a mathematical framework has been presented to quantify: (i) the variation of the real part of the optimum fundamental and second harmonic impedances with frequency and (ii) the degradation in power performance due to these variations for continuous class F/F^{-1} PAs. These works focused on the output matching circuits only and did not consider the impact of input impedance harmonic tuning on the PA performance and, in particular, if such tuning can counter-act the observed degradation. This was due to lack of a closed-form drain current expression to model the effects of input nonlinearity on the drain current waveforms, comprehensively. Furthermore, it is important to note that, the second source harmonic is supposed to be short-circuit in continuous mode theory when providing such a short circuit for the second harmonic at the intrinsic gate plane in wideband operations and continuous modes is almost impossible. Neglecting this point in choosing the optimum load impedance and output matching network design can lead to emerging unexpected results in frequency response of wideband PAs. Therefore, there is a need to investigate: (i) how input impedance tuning, coupled to standard output harmonic matching, can effect on continuous mode of class F/F^{-1} PAs, (ii) what is the role of input nonlinearity in expanding the optimum design space to reduce the complexity of the output matching network design and realization, (iii) how this second source harmonic optimization can effect on frequency response of drain efficiency, output power, gain and linearity performance of wideband PAs.

Additionally, in RFPAs a considerable percentage of DC power is dissipated due to high drain current density and its overlaps with voltage waveforms. Furthermore, RFPAs still suffer from losing the generated power through complicated matching networks from linearity degradation due to harmonic impedance manipulation. Hence, accumulating the lost energy below of monolithic chips can heat up the circuit and degrade the power performance. The heat density within the active devices can be significantly challenging in HPAs as a larger power is dissipated by increasing the output power. This not only effects on the PA performance but also can degrade the circuit mechanical strength. Therefore, there is need to explore: (i) how practical solutions can prevent from accumulating the lost power within small area and (ii) which materials can properly match with the chips and ground base to reduce the thermal resistivity below of the high power chips.

0.3 Objectives

To tackle the challenges discussed in section 0.2, the harmonic tuning techniques in the literature have been investigated to present novel solutions to design and realization of high-efficient wideband power amplifiers in continuous mode of class F/F^{-1}. This requires a comprehensive analysis of the drain current, and the correlation between the input and output harmonic conditions that can result in reducing the complexity of output matching networks' design over a wide range frequency. In this thesis, we will focus on using the emerging GaN semiconductor technology coupled with LTCC technology to design, prototype and test such novel circuits at sub 6 GHz applications. The specific research objectives to this end are as follows:

- Investigate the impact of tuning the second source harmonic on the drain current and PA performance, instead of simply supposing a short circuit.

- Develop the drain current expressions in continuous mode of class F/F^{-1} considering the nonlinearity of the gate-source capacitance (C_{gs}) in generating the second harmonic component at the device input.

- Explore a new design space that provides higher drain efficiency over a larger impedance area on the Smith chart for terminating the fundamental and second load harmonic impedances. This reduces the complexity of output matching circuits design and helps to achieve a flat frequency response.

- Investigate practical solutions for efficient thermal management in high power amplifiers using a single large chip or a hybrid multi-chip implementation.

0.4 Methodology

The methodology deployed throughout this thesis is based on a combination of analytical modeling, circuit, electromagnetic and multi-physics simulations using well-established software tools, and physical prototyping and testing of all designed PAs. All fabrications are done in LTCC technology using commercial GaN transistor chips while testing is carried out in our laboratory at the LACIME group. In the following subsections we provide more detail of these methodology steps:

0.4.1 Active Device and the Equivalent Model

The first step in PA design is choosing the appropriate active device to meet the requirements for implementation of the proposed solutions and project aspects. Then, we need a reliable and measurement base model or physical design kit (PDK) of the active device based on the available size and physical layers. The equivalent nonlinear model must represent the DC and RF characteristics accurately and consider the parasitic components, self-heating and thermal effects on transistor performance. Moreover, it is required that the commercial models support different gate width and fingers to reduce test and measurement costs in reach the optimum results for critical parameters such an output power, power density and DC to RF efficiency. To design and fabricate the PAs in this thesis, the AlGaN/GaN HEMT semiconductors are chosen which the die models can be provided from the leader Electronics Companies and

organizations such as Wolfspeed (Cree), Qorvo, the United Monolithic Semiconductors (UMS). At this stage, the device characteristics should be measured and verified according to the released equivalent model by the company. Thereby, the process of PA design can be done based on the specific characteristics of the available device; and the obtained results from circuit design at the simulation environment can be realized in practical circuits at the laboratory.

0.4.2 PA Design and Simulation

In this stage, the DC and AC characteristics of the chosen GaN device are analyzed under different bias conditions at the ADS (Advanced Design System) software. The load pull characteristics and S-parameters have been extracted to select the optimum load and source matched points based on the expressed theory in each design. Then, the appropriate matching networks have been designed based on the low loss substrates in LTCC technology to evaluate the power performance and stability of the PA in simulation environment. To provide a precise model of PAs the designed circuits have been investigated and optimized in electromagnetic environment of ADS and ANSYS HFSS software. These have been done with considering the electromagnetic scattering effects including coupling and parasitic problems on the compact transmission lines and transistor performance and each component optimized to provide the best possible results. The linearity performance of the designed PAs was tested with driving the LTE and 5G networks modulated signal through the MATLAB and ADS software. The last but not the least step in finalizing the designed PA in this thesis was assessment of the thermal and mechanical performance of the proposed circuit at different output power level, using ANSYS Icepak and Mechanical design environments.

0.4.3 PA Fabrication

The first step was fabrication of the matching networks and passive circuits for the proposed PAs, using the low loss substrates in LTCC technology. This step has been done at the LTCC

laboratory of the École de technologie supérieure (ÉTS). Then, the passive components were soldered on the LTCC substrate, and the active devices were mounted within cavities or on top of thermal vias, which the process have been described for each project in this thesis. The circuits were packaged in aluminum box, fabricated in mechanical department of ÉTS, and mounted on heatsink as a part of cooling system for optimal performance.

0.4.4 PA Test and Validation

In order to validate the expressed theories and simulation results of the designed PAs in comparison with the measured power characteristics, different circuit tests have been done during the fabrication process and final prototypes. For each PA the S-parameters of matching networks and passive circuits were measured using Keysight PNA-X and compared to the EM simulation results to modify them for optimum results or verify them for the next steps.

The power characteristics of fabricated PAs, such as power added efficiency (PAE), output power and gain were measured under continuous wave (CW) input power injection. In addition, the linearity performance of the PAs were assessed under LTE and 5G wideband signals with measuring the adjacent channel power ratio (ACPR). The tests setup for doing these measurements are shown in Fig. 0.1.

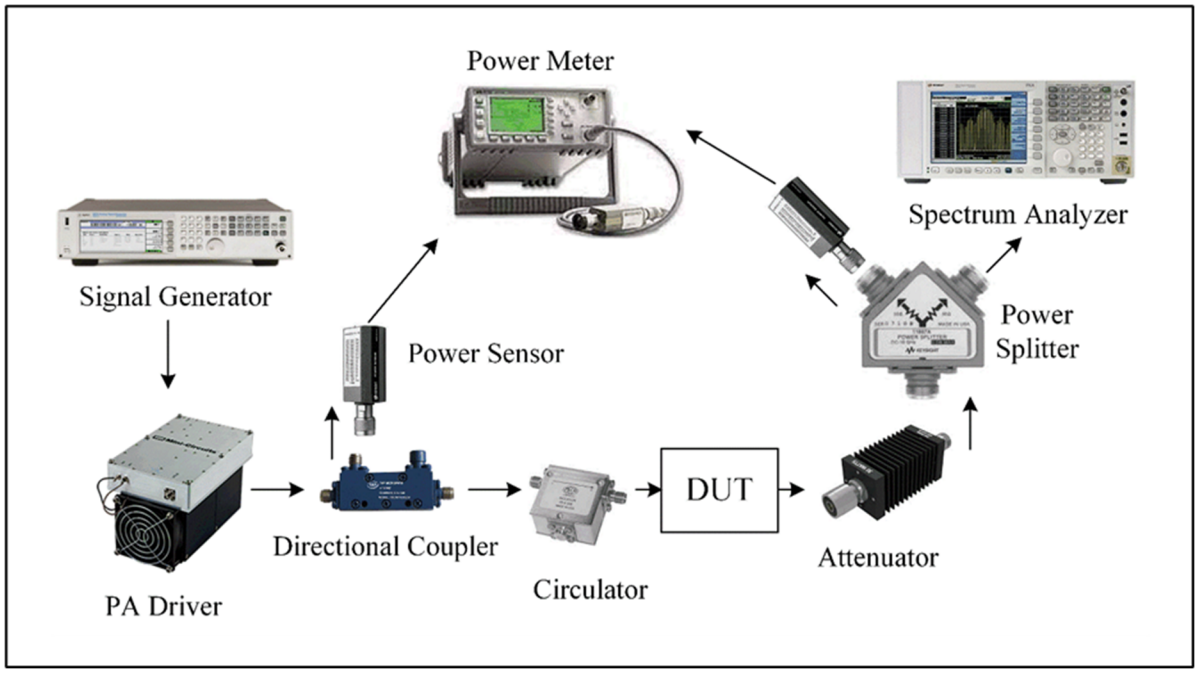

Figure 0. 1 The test setup to measure the power characteristics of PAs when are driven by the CW or modulation signal at the device input

0.5 Thesis Contributions

This thesis is presented in the paper-based format of ÉTS dissertation. The main contributions of this thesis are summarized as follows:

a. In chapter 1, a new closed-form drain current expression is proposed for the continuous-mode inverse class GF ($CCGF^{-1}$) PA to model the current waveforms in the time domain. In addition to taking into account the odd harmonics at the output, this closed-form expression captures the impact of the second-harmonic tuning at the input on the second output harmonic component in continuous mode. Moreover, it presents a new design space is generated for $CCGF^{-1}$ PAs that provide higher drain efficiency over a larger impedance area on the Smith chart. This reduces the complexity of output matching circuits design and helps to achieve a flat frequency response while simultaneously controlling the fundamental and second-harmonic frequencies. The reduction in matching circuit complexity also reduces losses, especially in circuits design at higher frequency ranges. Measurement results

for a prototype CCGF^{-1} PA shows above 70% drain efficiency and 39.9–41.4-dBm output power at 3-dB gain compression from 3.05 GHz to 3.85 GHz.

b. In chapter 2, the presented theory in chapter 1 is extend to the case of continuous class GF (CCGF) and demonstrate the impact of tuning the second source harmonic on the drain current and PA performance, instead of simply supposing a short circuit. In this chapter, the second source harmonic in continuous mode class GF (CCGF) is optimized to flatten the power amplifier's frequency response over a wideband range. Moreover, a new design space is explored by considering the effects of controlling the input nonlinearity of the gate-source capacitance (C_{gs}) on the drain current waveforms under continuous mode drain voltage waveforms. Unlike the CCGF^{-1} mode where current overshoot can occur, the obtained drain current waveforms in the CCGF mode do not exceed the maximum drain current. Since the current overshoot can negatively affect the reliability of the device over time while simultaneously increasing the overlap with the voltage waveform in continuous mode, avoiding it by going to the CCGF mode will alleviate these problems. The measurement results for a prototype CCGF PA show a flat frequency response from 3.3 GHz to 4.3 GHz with variations less than ± 0.4 dB for 40 dBm output power, and 17 dB large signal gain at 3-dB compression point. A drain efficiency of 66% ± 2% is achieved over the entire bandwidth.

c. In Chapter 3, a practical solution to develop thermal transient in high power amplifiers is proposed. The feasibility of the heat transformation underneath of chip has been investigated based on the thermal conductivity and thermal expansion of the interposer between the chip and ground base. It is shown that using the proposed solutions can lead to cool down the chip temperature and keep it below the standard values by transferring the heat generated underneath of the active device, immediately. The main challenge in implementation of such cooling systems is different thermal expansion of the interfaces with high thermal conductivity that should be soldered to transfer the heat to the later layers effectively. A 40W hybrid HPA has been designed and fabricated on multilayer LTCC at c-band frequency, using commercially available GaN transistor provided by the UMS

Company at the LACIME group of the ÉTS. The thermal tests of HPA shows better heat transformation compared to a 40 W MMIC HPA, designed and fabricated at C-band frequency and mounted using the die attach adhesive at the iRadio laboratory of university of Calgary.

0.6 Content

This thesis is in the by articles format including:

a. Chapter 1 introduces a continuous-mode inverse class GF power amplifier based on a new closed-form expression for the drain current. A wideband CCGF^{-1} PA is designed and fabricated, using a commercially available 10-W GaN Cree device in LTCC technology and based on load-pull and source-pull techniques presented in this chapter. The related paper has been published in IEEE Transactions on Microwave Theory and Techniques.

b. Chapter 2 investigates the performance of continuous-mode class GF PA by considering the effects of controlling the input nonlinearity of the gate-source capacitance (C_{gs}) on the drain current waveforms under continuous mode drain voltage waveforms. A wideband CCGF PA is designed and fabricated with flat frequency response and using a commercially available 10-W GaN Qorvo device in LTCC technology. The related paper has been accepted by IEEE Microwave and Wireless Components Letters.

c. Chapter 3 describes a practical solution to cool down the chip temperature and keep it below the standard values. A c-band 40 W hybrid HPA was designed and fabricated to evaluate the thermal management of using the described cooling system in this chapter. The related paper has been submitted to IEEE Transactions on Components, Packaging and Manufacturing Technology.

d. The conclusions and recommendations of this thesis are presented at the end of this document which summarized the achievements in this PhD research and provides several directions as the possibilities of future studies.

CHAPTER 1

CONTINUOUS MODE INVERSE CLASS-GF POWER AMPLIFIER WITH SECOND HARMONIC IMPEDANCE OPTIMIZATION AT DEVICE INPUT

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Abstract

In this paper a continuous inverse class GF ($CCGF^{-1}$) mode of power amplifier operation is introduced based on a new closed-form expression for the drain current. This analytical expression is utilized to exploit second source harmonic impedance manipulation in order to expand the design space of the output matching circuit resistively. This approach allows to diminish the complexity of the design of the load matching network at the fundamental and harmonic frequencies and to achieve wider bandwidth while simultaneously improving drain efficiency across the new optimum admittance points. Using the nonlinear model of a commercially available 10-Watt Gallium Nitride (GaN) device, load-pull and source-pull techniques are used to design a wideband $CCGF^{-1}$. The designed amplifier is fabricated using the selected transistor in low temperature co-fired ceramic (LTCC) technology. Measurement results show that, over the frequency band between 3.05 and 3.85 GHz, a drain efficiency of more than 70%, 11-12.4 dB gain and 39.9-41.4 dBm output power at 3-dB gain compression have been achieved. Although not designed for linearity, the fabricated amplifier shows an adjacent channel power ratio better than 26 dBc under a 20 MHz LTE signal having a 10.45 dB peak to average power ratio.

Introduction

High-efficiency broadband power amplifiers (PAs) are increasingly in demand for the fifth generation (5G) wireless communication standards. This is because of the high spectral efficiency and integration requirements in front-end modules (FEMs) and massive multiple input multiple output (MIMO) active antenna systems to provide greater capacity for the dramatic enhancement of data traffic in wireless networks (Miller, 2017). The overall performance and reliability of transmitters can be significantly affected by the heat dissipated from radio frequency power amplifiers (RFPAs) (Raab *et al.,* 2002; Ghannouchi *et al.*, 2013). Therefore, to reduce heat generation and improve power efficiency, it is critical for wideband PAs in 5G systems to efficiently generate the required power by using low complexity matching networks in combination with low-loss transmission line technologies. In addition to high efficiency, these PAs must also meet stringent linearity requirements that can be achieved by such techniques digital predistortion (Sun *et al.*, 2019; Yu *et al.*, 2020). This paper focuses on the efficiency enhancement through circuit design only and does not explicitly address linearization of the PA.

Harmonics engineering has been well known solution for shaping the drain current and voltage waveforms among the efficiency enhancement techniques. This technique reduces power dissipation by minimizing the overlap between the current and voltage waveforms. The waveform shaping can be applied to the output (Raab *et al.*, 1997; Cripps *et al.*, 2006; Colantonio *et al.*, 2009; Tasker *et al.*, 2009; Kim *et al.*, 2011; Kim *et al.*, 2011), input and output (White *et al.*, 1998; Colantonio *et al.*, 2003; Canning *et al.*, 2013; Sharma *et al.*, 2018) at single frequency and multiple frequencies (Cripps *et al.*, 2009; Wright *et al.*, 2009; Carrubba *et al.*, 2010; Carrubba *et al.*, 2011; Tuffy *et al.*, 2012; Rezaei *et al.*, 2014; Saxena *et al.*, 2017). The approaches in (Raab *et al.*, 1997; Cripps *et al.*, 2006; Colantonio *et al.*, 2009; Tasker *et al.*, 2009; Kim *et al.*, 2011; Kim *et al.*, 2011; White *et al.*, 1998; Colantonio *et al.*, 2003; Canning *et al.*, 2013; Sharma *et al.*, 2018) rely on precise open and short impedance values at harmonic frequencies which makes them inherently narrow band, hence not suitable to meet the 5G efficiency and bandwidth requirements. On the other hand, emerging continuous mode

PAs (Cripps *et al.*, 2009; Wright *et al.*, 2009; Carrubba *et al.*, 2010; Carrubba *et al.*, 2011; Tuffy *et al.*, 2012; Rezaei *et al.*, 2014; Saxena *et al.*, 2017) offer wider bandwidth performance with comparable efficiency by providing more flexibility with respect to the harmonic impedances. However, this flexibility is limited to phase variations for the fundamental and second harmonics along constant resistance circles in the Smith chart. This limitation leads to degraded performance at the middle or edges of the bandwidth due to impedance mismatch caused by the variation of resistive part of the optimum fundamental impedance with frequency (Chen *et al.*, 2012; Carrubba *et al.*, 2011; Carrubba *et al.*, 2012; Lu *et al.*, 2013; Tang *et al.*, 2016; Zheng *et al.*, 2018). In (Carrubba *et al.*, 2011) and (Carrubba *et al.*, 2012), a mathematical framework was presented to quantify: (i) the variation of the real part of the optimum fundamental and second harmonic impedances with frequency and (ii) the degradation in power performance due to these variations for continuous class F/F^{-1} PAs. These works focused on the output matching circuits only and did not consider the impact of input impedance harmonic tuning on the PA performance and, in particular, if such tuning can counter-act the observed degradation. Therefore, there is a need to investigate how input impedance tuning, coupled to standard output harmonic matching, can improve PA performance and how it can expand the optimum design space with improved drain efficiency while reducing the complexity of the output matching network design and realization.

The correlation between input and output harmonic conditions was investigated for Class GF and Class GF^{-1} amplifiers in (Sharma *et al.*, 2018). This was done with drain current expressions that consider the nonlinear behavior of gate–source capacitance (C_{gs}) and a modified conduction angle for a single frequency. In a more recent work (Dhar *et al.*, 2019), this concept of input harmonic tuning was investigated for continuous mode class F^{-1} amplifiers where the drain current expression was based on the first three terms of the current's Fourier series in single frequency class F^{-1}. This approach does not capture the impact of the 2^{nd} harmonic manipulation at the input on the second harmonic component of the current waveform at the output. In the same work, a flexible source second-harmonic design space was also proposed to simplify the input matching network. However, the output matching network

was still quite complicated for controlling harmonic impedances. Furthermore, the problem of lack of frequency response flatness over the bandwidth was still present.

In this paper, a new closed-form drain current expression is proposed for the continuous mode inverse class GF ($CCGF^{-1}$) PA to model the current waveforms in the time domain. In addition to taking into account the odd-harmonics at the output, this closed-form expression captures the impact of the second harmonic tuning at the input on the second output harmonic component in continuous mode. It is shown that, a new design space is generated for $CCGF^{-1}$ PAs that provides higher drain efficiency over a larger impedance area on the Smith chart. This reduces the complexity of output matching circuits design and helps to achieve a flat frequency response while simultaneously controlling the fundamental and second harmonic frequencies. The reduction in matching circuit complexity also reduces losses, especially in circuits design at higher frequency ranges.

The remainder of this paper is organized as follows. In section II, the theory of continuous mode class GF^{-1} is presented and analyzed using the newly proposed closed-form current expression. In section III, the expanded design space in $CCGF^{-1}$ is illustrated. The $CCGF^{-1}$ theory is validated through load/source pull simulations with a 10-Watt GaN Cree model in section IV. In section V, a prototype PA is designed based on the proposed theory and built using LTCC technology. Measurement results and PA performance are also reported in this section.

1.1 Theory of Continuous Mode Class GF^{-1} PAs Under Second Source Harmonic Manipulation

1.1.1 Conventional Class F^{-1} and GF^{-1}

The normalized drain voltage and current waveforms in class F^{-1} are defined by the following equations (Colantonio *et al.*, 2009):

$$V_{ds,F^{-1}}(\theta) = 1 - \sqrt{2}\cos\theta + \frac{1}{2}\cos 2\theta \tag{1.1}$$

$$i_{ds,F^{-1}}(\theta) = i_{DC} - i_1 \cos\theta + i_3 \cos 3\theta \quad (1.2)$$

which represent the standard half-wave rectified sinusoidal for drain voltage and square wave for drain current at the device's current generator plane. i_{DC}, i_1 and i_3 are harmonic components of the drain current, which is generated by terminating the second and third harmonics to open and short circuits, respectively, while terminating the fundamental frequency with the optimum load-pull impedance. Supposing that the second harmonic impedance is shorted at device input, a general equation which models the class F^{-1} drain current waveforms for different bias conditions and conduction angles is given by (Colantonio *et al.*, 2009):

$$i_{ds,F^{-1}}(\theta) = \begin{cases} \left[I_m \left(\dfrac{\cos\theta - \cos\frac{\alpha}{2}}{1 - \cos\frac{\alpha}{2}} \right) - i_{r2} \cos 2\theta \right], & -\dfrac{\alpha}{2} < \theta < \dfrac{\alpha}{2} \\ 0, & -\pi < \theta < \dfrac{\alpha}{2}, \quad \dfrac{\alpha}{2} < \theta < \pi \end{cases} \quad (1.3)$$

Where I_m is the peak current of the device, α and θ are conduction angle and angular frequency, respectively. i_{r2} is the real part of second harmonic drain current that can be extracted by applying the boundary condition of standard class F^{-1} (Cripps *et al.*, 2006).

The role of the nonlinear gate-source capacitor C_{gs} in generating harmonic components at the device input, and consequently its contribution in drain current variations in class F/F^{-1}, have been analyzed as the class GF/GF^{-1} (Sharma *et al.*, 2018). Specifically, in class GF^{-1}, the second source harmonic is tuned to control the nonlinear behavior of C_{gs} in generating the second harmonic voltage at the intrinsic gate point of device. Unlike class F^{-1}, that the second source harmonic is shorted, shaping the gate voltage waveform is used for modifying the drain current components that are generated in opened second harmonic and shorted third harmonic load at the current plane of the device. In order to represent the waveforms of gate–source voltage (V_{gs}) at different bias conditions and considering the second harmonic voltage generated by nonlinear C_{gs}, V_{gs} is defined as (Sharma *et al.*, 2018):

$$V_{gs}\,(\theta,\alpha) = V_{gso} + V_1\left(\frac{\cos\theta - \cos\frac{\alpha}{2}}{1-\cos\frac{\alpha}{2}}\right) + V_2\,\cos 2\theta \tag{1.4}$$

By normalizing this equation to V_1, V_{gs} can be written as:

$$\overline{V_{gs}\,(\theta,\alpha,\gamma)} = \frac{V_{gso}}{V_1} + \left(\frac{\cos\theta - \cos\frac{\alpha}{2}}{1-\cos\frac{\alpha}{2}}\right) + \gamma\,\cos 2\theta \tag{1.5}$$

where, $\gamma = V_1 / V_2$ indicates the voltage ratio of the second harmonic and fundamental voltage component at input. V_1 and V_2 are intrinsically generated out of phase, however, V_2 can be shifted to in-phase with V_1, manipulating the second harmonic at device input. The gate-source voltage is depicted in Fig. 1.1 supposing $V_{gso} = 0$ for class B bias condition ($\alpha = 180$) and γ between -0.4 and 0.4. It can be seen that, for $-0.4 \leq \gamma < 0$ the second out of phase harmonic is flatting or making a valley at the peak of V_{gs} waveform which raises conduction angle for the smaller amplitude of voltage, while for $0 < \gamma \leq 0.4$ the in-phase second harmonic is boosting the maximum of V_{gs} and reducing the conduction angle. For $\gamma = 0$ the ideal sinusoidal waveform happens as it is expected in class B for short-circuit second harmonic at input.

The gate voltage is transformed through the nonlinear transconductance (g_m) of device that the drain current in class GF^{-1} is formulated as:

$$i_{GF^{-1}}(\theta,\alpha,\gamma,I_m) \tag{1.6}$$
$$= \begin{cases} I_m\left(\dfrac{cos\,\theta - cos\frac{\alpha}{2}}{1-cos\frac{\alpha}{2}} + \gamma\ cos\,2\theta\right) - i_{r2}(\beta,\alpha,\gamma,I_m)\ cos\,2\theta, & -\beta < \theta < \beta \\ 0\,, & -\pi < \theta < \beta\ ,\quad \beta < \theta < \pi \end{cases}$$

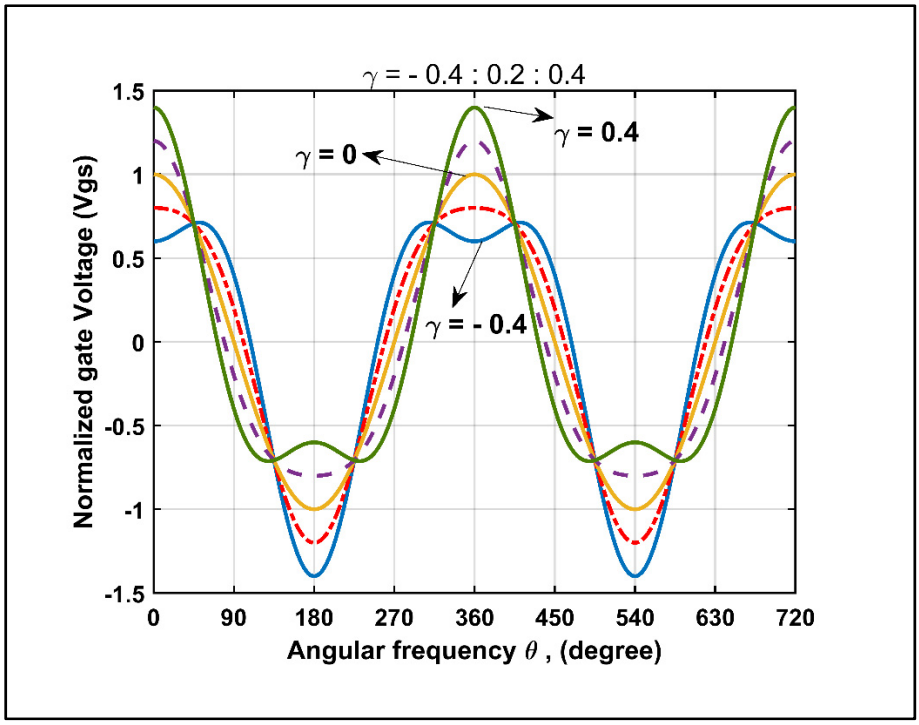


Figure 1.1 Normalized input voltage (V_{gs}) to the fundamental component of gate voltage (V_1), supposing V_{gso}= 0 in class B bias condition (α = 180) and -0.4 ≤ γ ≤ 0.4 in step of 0.2

where, $i_{r2}(\beta, \alpha, \gamma, I_m)$ is the real part of second harmonic drain current and can be computed by imposing the class GF^{-1} boundary condition and β is the device output conduction angle for the drain current. This is actually the zero-crossing cut-off angle which can be extracted by zeroing the normalized V_{gs} as a function of conduction angle and input voltage nonlinear parameter (γ) as following:

$$\beta(\alpha, \gamma) \tag{1.7}$$

$$= \begin{cases} cos^{-1}\left(\dfrac{\dfrac{-1}{1-cos\frac{\alpha}{2}} + \sqrt{\left(\dfrac{-1}{1-cos\frac{\alpha}{2}}\right)^2 + 8\gamma\left(\gamma + \dfrac{cos\frac{\alpha}{2}}{1-cos\frac{\alpha}{2}}\right)}}{4\gamma}\right), & -0.5 < \gamma < 0.5, \quad \gamma \neq 0 \\ \dfrac{\alpha}{2}, & \gamma = 0 \end{cases}$$

In Fig. 1.2, it is shown that the zero-crossing cut-off angle (β) is decreasing when γ varies from -0.5 to 0.5, which means that the device is conducting signal in on-state for a smaller portion of period. Therefore, as mentioned earlier, it is expected that for a certain amount of input power, by increasing the γ factor a larger gate voltage is generated in a shorter period of time that leads to pulling more drain current up to the device's maximum current at the output, instead of having smaller drain current over a longer time. In other words, shaping the gate voltage at input, drain current can be controlled to reduce the overlap between drain current and voltage waveforms on the load line, which leads to increasing the device's drain efficiency. This is investigated in next parts by analyzing the drain current harmonics in continuous mode of class GF^{-1} PAs.

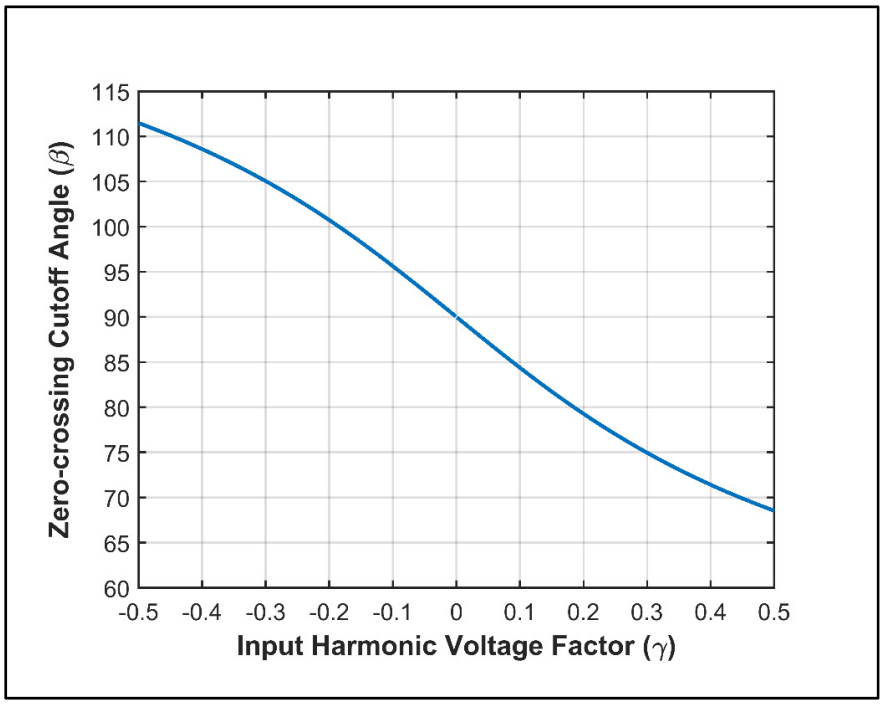


Figure 1.2 Output conduction angle β for class B bias condition ($\alpha = 180$) and $-0.5 \leq \gamma \leq 0.5$

1.1.2 Continuous Mode of Class GF^{-1}with Closed-Form Current Expression

In order to analyze the impact of input impedance tuning on the output matching design space in a manner that maintains and even improves performance, a new closed-form expression of drain current in continuous class GF^{-1} is needed and hereby proposed:

$$i_{CCGF^{-1}}(\theta,\alpha,\gamma,I_m,\delta)= \tag{1.8}$$

$$\begin{cases} \left[I_m\left(\dfrac{\cos\theta-\cos\frac{\alpha}{2}}{1-\cos\frac{\alpha}{2}}+\gamma\cos 2\theta\right)-i_{r2}(\beta,\alpha,\gamma,I_m)\cos 2\theta\right].(1-\delta\sin\theta), & -\beta<\theta<\beta \\ 0\ , & -\pi<\theta<\beta,\quad \beta<\theta<\pi \end{cases}$$

where δ is varied between -1 and 1 to generate a family of waveforms of drain current representing continuous mode operation. Therefore, for δ = 0 the second harmonic at the current plane of the device is open-circuited to generate the required drain current square waveform for standard class F^{-1}. Furthermore, while the real part of the second harmonic is excluded, its imaginary part is kept. This expands the design space allowing for wideband matching while maintaining the impact of second source harmonic manipulation on the second harmonic component of output current in continuous mode. In addition, the term $(1-\delta sin\theta)$ does not affect the expression of $i_{r2}(\beta,\alpha,\gamma,I_m)$ obtained from:

$$\tfrac{1}{\pi}\int_{-\beta}^{\beta} i_{CCGF^{-1}}(\theta,\alpha,\gamma,I_m,\delta).\ \mathrm{Cos}\,2\theta\ d\theta = 0 \tag{1.9}$$

which yields:

$$i_{r2}(\beta,\alpha,\gamma,I_m)= \tag{1.10}$$

$$I_m\left(\frac{\gamma\left(\beta+\frac{\sin 4\beta}{4}\right)\left(1-\cos\frac{\alpha}{2}\right)-\cos\frac{\alpha}{2}\ \sin 2\beta-\left(\frac{4}{3}\sin^3\beta-\ 2\sin\beta\right)}{\left(1-\cos\frac{\alpha}{2}\right)\left(\beta+\frac{\sin 4\beta}{4}\right)}\right)$$

1.1.2.1 Performance Analysis: Current Waveforms

The new drain current equation (1.8) allows us to examine multiple current waveforms that result from various combinations of the parameters γ and δ. These combinations provide insight into the impact of 2nd harmonic source impedance manipulation on the current waveforms in continuous mode of class GF^{-1}. Fig. 1.3 shows the obtained waveforms for $-0.4 \leq \gamma \leq 0.4$ and $-1 \leq \delta \leq 1$. Here, the half-sinusoidal-wave voltage is plotted to minimize the common area with the drain current waveforms and power loss at device. It can be seen that, for $\gamma = 0$ and $-1 \leq \delta \leq 1$, Fig. 1.3(b), the obtained waveforms correspond to the standard continuous mode class F^{-1} as expected. For $-0.4 \leq \gamma \leq 0.4$ and $\delta = 0$, the resulting drain current waveforms are those of single mode class GF^{-1}, Fig. 1.3©. Comparing Figs. 1.3(a) and (b), it is clear that the growth of drain currents for $\gamma = -0.4$ and 0 is negligible for different δ values. However, when γ becomes positive, Fig. 1.3(c), the current growth is much more substantial. This is explained with Considering Fig. 1.1, where for the positive γ a stronger second harmonic voltage is generated in-phase with the fundamental harmonic that rises the peak of V_{gs}, instead of making valley for negative γ or sinusoidal waveform for $\gamma = 0$.

By transferring this peak waveform through the nonlinear g_m to the output of device, a larger drain current is generated. This can be seen in Figs. 1.3(d)-(f) that overshooting of the drain current is considerable for $\gamma = 0.4, 0.2$ in comparison with $\gamma = 0, -0.2, -0.4$ at different amounts of δ. In practice, the drain current is limited by the maximum drain current of the device which should be considered in choosing the proper amounts of γ and δ factors appropriate with the physical characteristics of device. Also, the peak drain voltage is raised to 2.9 V_{DD} according to the standard class F^{-1} voltage equation (1.1) to increase the output power, which should be tolerable by device breaking voltage.

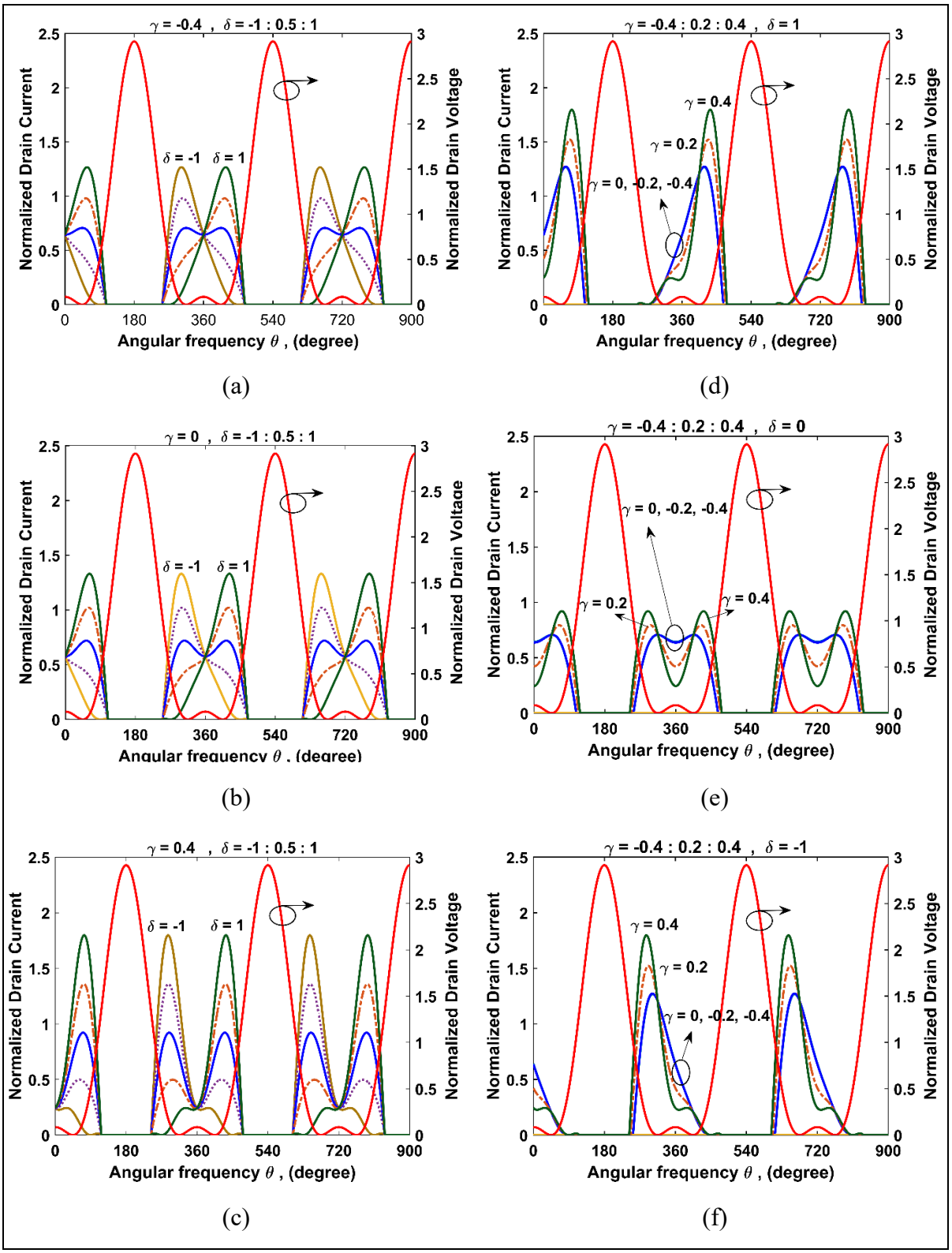


Figure 1.3 Family waveforms of drain current and half-sinusoidal voltage in continues class GF^{-1} for $-0.4 \leq \gamma \leq 0.4$ and $-1 \leq \delta \leq 1$

1.1.2.2 Performance Analysis: Efficiency

To assess the efficiency based on the new drain current expression, (1.8), we extract its Fourier series components up to the third harmonic. By using equation (1.8), we again capture the impact of the second harmonic tuning at the input on the resulting efficiency. The DC, $i_{CCGF^{-1},dc}$, the real and imaginary parts of the three first harmonics, $i_{CCGF^{-1},h,real}$, $i_{CCGF^{-1},h,img}$, with h being the harmonic order, are given by:

$$i_{CCGF^{-1},dc} = \frac{I_m}{2\pi}\left[\frac{-2\beta\cos\frac{\alpha}{2} + 2\sin\beta}{1-\cos\frac{\alpha}{2}} - \left(\frac{i_{r2}}{I_m} - \gamma\right)\sin 2\beta\right] \tag{1.11}$$

$$i_{CCGF^{-1},1,real} = \frac{I_m}{\pi}\left[\frac{-2\ \sin\beta\ \cos\frac{\alpha}{2} + \left(\beta + \frac{\sin 2\beta}{2}\right)}{\left(1-\cos\frac{\alpha}{2}\right)} + \left(\frac{i_{r2}}{I_m} - \gamma\right)\left(\frac{4}{3}\ sin^3\beta - 2\sin\beta\ \right)\right] \tag{1.12}$$

$$i_{CCGF^{-1},1,img} = \frac{\delta I_m}{\pi}\left[\frac{\cos\frac{\alpha}{2}\left(\beta - \frac{\sin 2\beta}{2}\right) - \frac{2}{3}\ sin^3\beta}{\left(1-\cos\frac{\alpha}{2}\right)} - \frac{1}{2}\left(\frac{i_{r2}}{I_m} - \gamma\right)\left(\left(\beta - \frac{\sin 2\beta}{2}\right) + 2sin^3\beta\ \left(2sin^2\frac{\beta}{2} - 1\right)\right)\right] \tag{1.13}$$

$$i_{CCGF^{-1},2,real} = \frac{I_m}{\pi}\left[\frac{-\cos\frac{\alpha}{2}\sin 2\beta\ + 2\sin\beta - \frac{4}{3}\ sin^3\beta}{\left(1-\cos\frac{\alpha}{2}\right)} - \left(\frac{i_{r2}}{I_m} - \gamma\right)\ (\beta + \frac{1}{4}\ \sin 4\beta\ )\right] \tag{1.14}$$

$$i_{CCGF^{-1},2,img} = \frac{\delta I_m}{\pi}\left[\left(\frac{\frac{4}{3}\cos\frac{\alpha}{2}\ sin^3\beta - \frac{1}{2}\left(\beta - \frac{\sin 4\beta}{4}\right)}{\left(1-\cos\frac{\alpha}{2}\right)}\right) - \frac{1}{2}\left(\frac{i_{r2}}{I_m} - \gamma\right)\left(\frac{4}{3}\ sin^3\beta + \frac{1}{5}\left(4sin^3\beta\ (4sin^2\beta - 5)\right)\right)\right] \tag{1.15}$$

$$i_{CCGF^{-1},3,real} = \frac{2I_m}{\pi}\left[\frac{-\frac{1}{3}\sin 3\beta\ \cos\frac{\alpha}{2} + cos^3\beta\ \sin\beta}{\left(1-\cos\frac{\alpha}{2}\right)} - \left(\frac{i_{r2}}{I_m} - \gamma\right)\left(\sin\beta - 2sin^3\beta + \frac{8}{5}\ sin^5\beta\right)\right] \tag{1.16}$$

$$i_{CCGF^{-1},3,img} = \frac{\delta I_m}{\pi}\left[\frac{-10\ \cos\frac{\alpha}{2}\ sin^3\beta\ \left(2sin^2\frac{\beta}{2} - 1\right) + 2sin^3\beta\ (4sin^2\beta - 5)}{5\ \left(1-\cos\frac{\alpha}{2}\right)} + \frac{1}{2}\left(\frac{i_{r2}}{I_m} - \gamma\right)\left(\beta - \frac{1}{6}\sin 6\beta + 2sin^3\beta\ \left(2sin^2\frac{\beta}{2} - 1\right)\right)\right] \tag{1.17}$$

Fig. 1.4 presents the DC component and the real part of the three harmonic components of the drain current; normalized to I_m, as a function of γ. It also plots the ratio of the real part of the fundamental component to DC. This figure show that the variations of the fundamental and DC component are insignificant for $-0.5 \leq \gamma < 0$ whereas they become considerable when $0 \leq \gamma \leq 0.5$. This is due to fact that when $\gamma \geq 0$, the device source is terminated such that the second harmonic voltage shifts in-phase with the fundamental harmonic voltage at input. In this case, the ratio of fundamental to DC drain current increases, which leads to improving the drain efficiency. The theoretically achievable drain efficiency of the continuous class GF^{-1} for zero knee voltage is obtained using (1.11) and (1.12):

$$\eta_{CCGF^{-1}} = \frac{P_{out_{CCGF^{-1}}}}{P_{dc_{CCGF^{-1}}}} = \frac{\frac{1}{\sqrt{2}}\,(V_{dc} - V_k)\; i_{CCGF^{-1},1}(\theta, \alpha, \gamma, I_{m,\delta})}{V_{dc}\;\; i_{CCGF^{-1},dc}(\theta, \alpha, \gamma, I_m)} \tag{1.18}$$

$$= \frac{\sqrt{2}\left[\dfrac{-2\sin\beta\;\cos\frac{\alpha}{2} + \beta + \frac{\sin 2\beta}{2}}{\left(1 - \cos\frac{\alpha}{2}\right)} + \left(\frac{i_{r2}}{I_m} - \gamma\right)\left(\frac{4}{3}\,sin^3\beta - \;2\sin\beta\;\right)\right]}{\left[\dfrac{-2\beta\,\cos\frac{\alpha}{2} + 2\sin\beta}{1 - \cos\frac{\alpha}{2}} - \left(\frac{i_{r2}}{I_m} - \gamma\right)\sin 2\beta\right]}$$

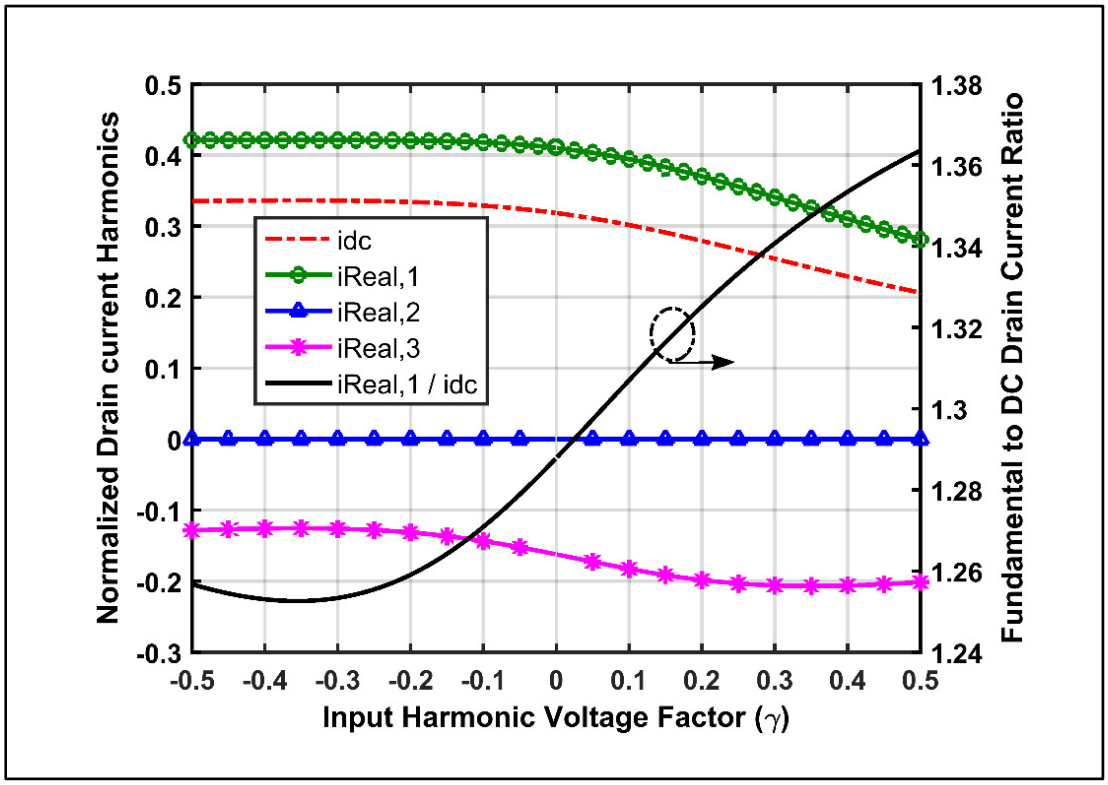


Figure 1.4 Real components of drain current harmonics normalized to the I_m in the continuous mode class GF^{-1} for $-0.5 \leq \gamma \leq 0.5$

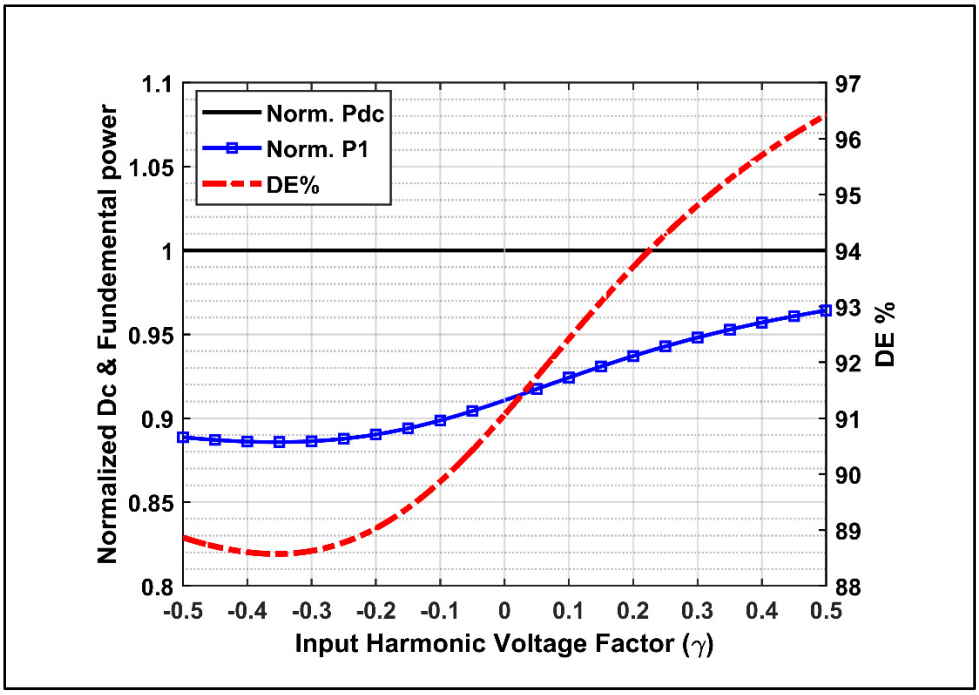


Figure 1.5 Theoretical drain efficiency (DE %), normalized fundamental and DC power to DC power consumption for -0.5 ≤ γ ≤ 0.5

As depicted in Fig. 1.5, the achievable drain efficiency, at the intrinsic plane of a lossless device under ideal waveforms, increases from 89% to 97% when the nonlinear factor at input (γ) moves from -0.5 to 0.5. This can be explained by considering the normalized fundamental power ratio to dc power consumption (square-blue line, Fig. 1.5), which grows for $-0.2 \leq \gamma <$ 0.5. The drain efficiency at $\gamma = 0$ is 91% as it is predicted in standard class F^{-1} without manipulating the second harmonic at device input. However, the use of real devices and matching networks will incur some loss and therefore reduce further the PA efficiency.

It worth noting that, by open-circuiting the second harmonic at the output ($\delta = 0$) no second harmonic component will be present in the drain current directly. However, the effect of manipulating the second harmonic at the input is slightly visible on DC, fundamental and third harmonics through the extracted parameter i_{r2}. Furthermore, the second reactive component of drain current is depending on the input nonlinearity factor γ for $\delta \neq 0$. These can be deduced from the harmonic components of drain current (1.11) - (1.17), as well as the drain current waveforms illustrated in Fig. 1.3. In the next section, we will see how optimum design space

for terminating the fundamental load impedance can be expanded by controlling the second source harmonic in continuous mode ($\delta \neq 0$) of class GF^{-1}.

1.2 New Design Space for Output Matching Network in Continuous Class GF^{-1}

In section II, it is shown that how input nonlinearity factor can affect on conduction angle of truncated drain current in class B bias condition and modify the drain current waveforms generated for various δ factors in continuous class F^{-1}. As a result, a new design space can be described based on the new drain current waveforms, including contribution of controlling the second harmonic at input in continuous class GF^{-1}, while the drain voltage is supposed to have half-wave rectified sinusoidal waveform. Hence, the real and imaginary components of the output admittances are obtained as follows:

$$Y_{CCGF^{-1},nf} = -\frac{I_{ds,n}}{V_{ds,n}} \tag{1.19}$$

$$Y_{CCGF^{-1},f,real} = \frac{I_m}{\pi\sqrt{2}}\left[\frac{\beta - 2\sin\beta\cos\frac{\alpha}{2} + \frac{\sin 2\beta}{2}}{\left(1-\cos\frac{\alpha}{2}\right)} + \left(\frac{i_{r2}}{I_m} - \gamma\right)\left(\frac{4}{3}sin^3\beta - 2\sin\beta\right)\right] \tag{1.20}$$

$$Y_{CCGF^{-1},f,img} = \frac{\delta I_m}{\pi\sqrt{2}}\left[\frac{\cos\frac{\alpha}{2}\left(\beta - \frac{\sin 2\beta}{2}\right) - \frac{2}{3}sin^3\beta}{\left(1-\cos\frac{\alpha}{2}\right)} - \frac{1}{2}\left(\frac{i_{r2}}{I_m} - \gamma\right)\left(\left(\beta - \frac{\sin 2\beta}{2}\right) + 2sin^3\beta\left(2sin^2\frac{\beta}{2} - 1\right)\right)\right] \tag{1.21}$$

$$Y_{CCGF^{-1},2f,real} = \frac{I_m}{\pi}\left[\frac{\left(2-\cos\frac{\alpha}{2}\right)\sin 2\beta \ + \frac{4}{3}\ sin^3\beta)}{\left(1-\cos\frac{\alpha}{2}\right)} - \left(\frac{i_{r2}}{I_m}-\gamma\right)\left(\beta+\frac{1}{4}\ \sin 4\beta\ \right)\right] \tag{1.22}$$

$$Y_{CCGF^{-1},2f,img} = \frac{-2\delta I_m}{\pi}\left[\left(\frac{\frac{4}{3}\cos\frac{\alpha}{2}\ sin^3\beta - \frac{1}{2}\left(\beta-\frac{\sin 4\beta}{4}\right)}{(1-\cos\frac{\alpha}{2})}\right) - \frac{1}{2}\left(\frac{i_{r2}}{I_m}-\gamma\right)\left(\frac{4}{3}\ sin^3\beta + \frac{1}{5}\left(4sin^3\beta\ (4sin^2\beta-5)\right)\right)\right] \tag{1.23}$$

Based on (1.20) to (1.23), the output admittance for the fundamental and second harmonics can be expressed as functions of γ and δ:

$$Y_{CCGF^{-1},f} = \xi_1(\gamma) + j\ \delta\chi_1\ (\gamma) \tag{1.24}$$

$$Y_{CCGF^{-1},2\,f} = j\ \delta\ \chi_2\ (\gamma) \tag{1.25}$$

Here, the real part of fundamental output admittance, $\xi_1(\gamma)$, varies proper with the input nonlinear factor γ in conductance direction and its imaginary part, $\delta\chi_1\ (\gamma)$, varies through δ and γ, reactively. The real part of second harmonic drain current has been excluded while its imaginary part, $\delta\ \chi_2\ (\gamma)$ varies in terms of δ and γ; this moves the second harmonic susceptance on the edge of Smith chart from its open circuit condition. Consequently, a new design space is defined in $CCGF^{-1}$ to relax matching network circuit for terminating fundamental and second harmonic load impedances and achieve a predetermined drain efficiency over wider frequency band. The design space is depicted in Fig. 1.6, sweeping γ from -0.5 to 0.5 and δ from -1 to 1

to avoid from zero-crossing current waveforms. As indicated by arrows in Fig. 1.6, the fundamental conductance varies considerably for positive amounts of γ compared to the negative values, which is consistent with the analysis of drain current waveforms in section 1.1.2.1 Also, the susceptance variation of the load admittance harmonics are mainly dependent on δ, while it is negligible for γ factor.

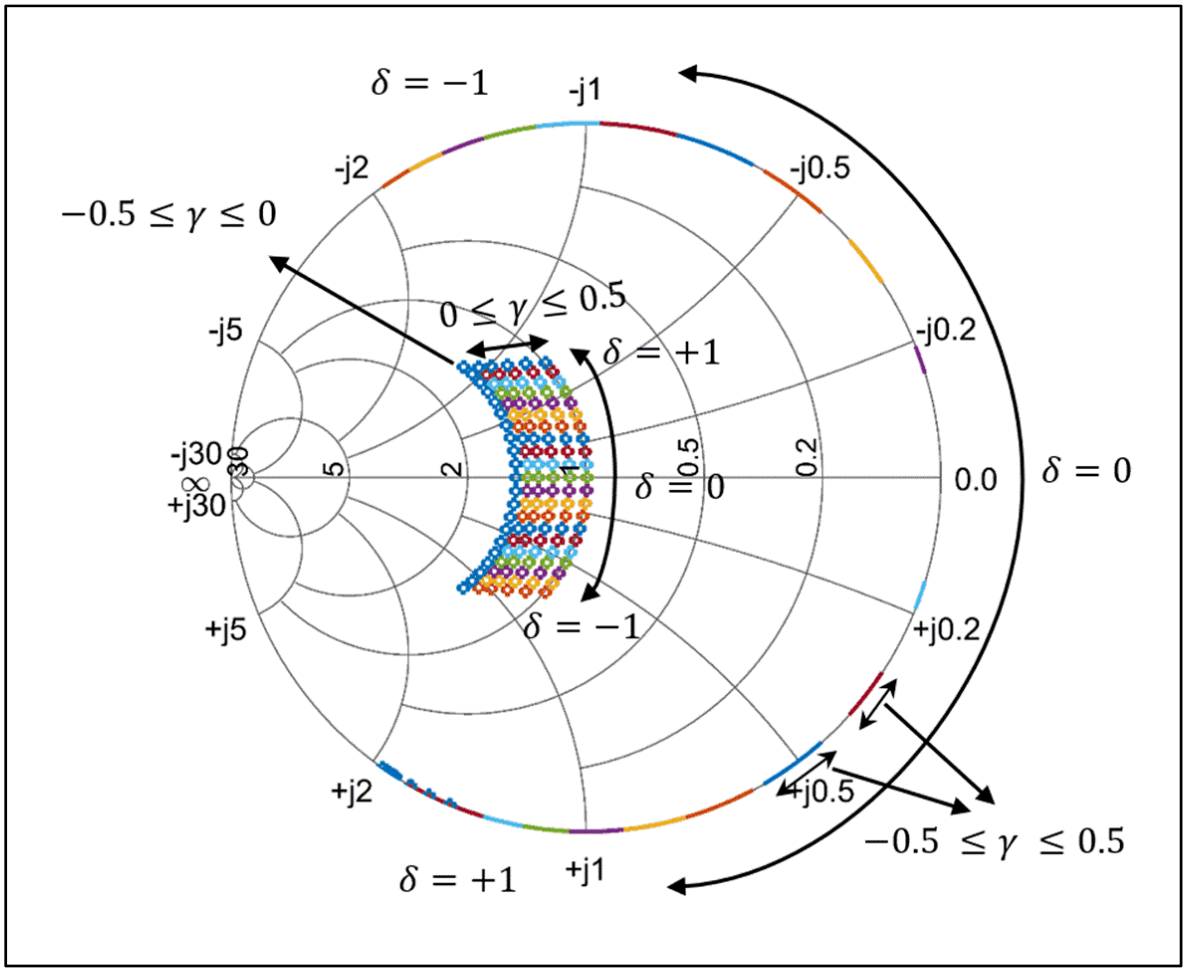


Figure 1.6 New design space for fundamental (inside the Smith chart) and second harmonic (on the edge of the Smith chart) admittances in output matching network of continuous class GF^{-1}; where δ is varying from -1 to 1 and γ is varying from -0.5 to 0.5, the third harmonic is terminated with short circuit

In order to explore the advantages of the new design space, drain efficiency (1.18) and susceptance of the fundamental and second harmonic admittances (1.21), (1.23) normalized to the fundamental conductance G_1 (1.20) are illustrated in Fig. 1.7 as functions of γ and δ factors. It can be seen that, for each value of γ, the normalized susceptances of the output fundamental (B_1/G_1 – red curves) and the second harmonic (B_2/G_1 – blue curves) vary in opposite ways when δ increases. At this condition, the amplitude of the fundamental drain current and voltage are fixed which theoretically leads to constant drain efficiency and output power over the operational frequency band. When $\gamma = 0$, this is consistent with the theory of standard CCF^{-1} (Carrubba *et al.*, 2011) that gives a drain efficiency of 91%.

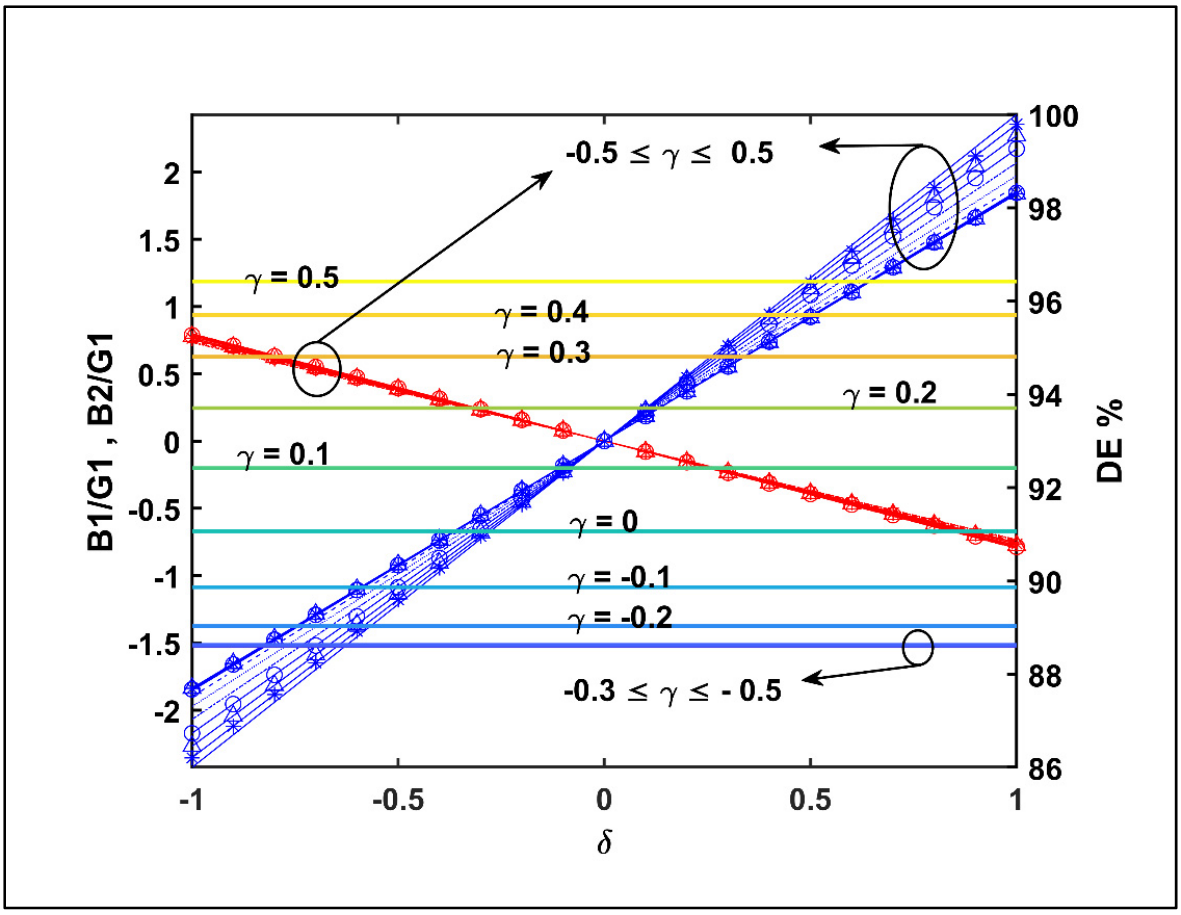


Figure 1.7 Drain efficiency variation in continuous class GF^{-1}, Normalized susceptances (B_1 & B_2) to the fundamental conductance (G_1) for the first and second harmonics of output admittance in terms of $-0.5 \leq \gamma \leq 0.5$ and $-1 \leq \delta \leq 1$; red lines: B_1/G_1, blue lines: B_2/G_1

However, in practice since the real part of the load trajectory in matching networks changes with frequency, mismatch will occur in the middle or at the edges of the bandwidth. Therefore, the flat frequency response predicted in theory cannot be achieved in practice. Furthermore, in extended continuous class F^{-1} (Carrubba *et al.*, 2012) , power performance degradation is estimated when the real part of optimum impedance points for the output fundamental and second harmonics are swept. This is computed through multiplying an extra term of $(1+\sigma \cos\theta)$ into the drain current equation at CCF^{-1}, which explains the drop in frequency response of broadband PAs (Carrubba *et al.*, 2012). While in $CCGF^{-1}$, as illustrated in Fig. 1.6 and 7, tuning the second harmonic at device input not only increases the number of optimum points to provide multiple solutions for terminating the fundamental harmonic at device output, but also it can be controlled to achieve higher drain efficiency to compensate the drop in frequency response in comparison with the shorted second source harmonic in CCF^{-1}.

1.3 PA Design Methodology

In this section, the design space for the output matching network that was theoretically defined in section 1.2 by manipulating the second source harmonic is explored through load-pull and source-pull simulation in Keysight's ADS software. In addition, input and output matching networks are designed to realize the expected theoretical waveforms of $CCGF^{-1}$ PA in the 3.1 to 3.9 GHz frequency range. For this investigation, we chose the commercially available CG2H40010F packed GaN HEMT from CREE Inc., with 10-Watt output power at 28 V drain bias. The complete ADS device model is provided by the supplier and includes the intrinsic and parasitic elements, shown in Fig. 1.8. While the model gives access to the voltage and current at the intrinsic plane on the drain side, it does not do so on the gate side. Therefore, an additional extraction step was used, as proposed in (Tasker *et al.*, 2011) and experimentally verified in (Li *et al.*, 2016), to access the gate voltage at the intrinsic gate plane.

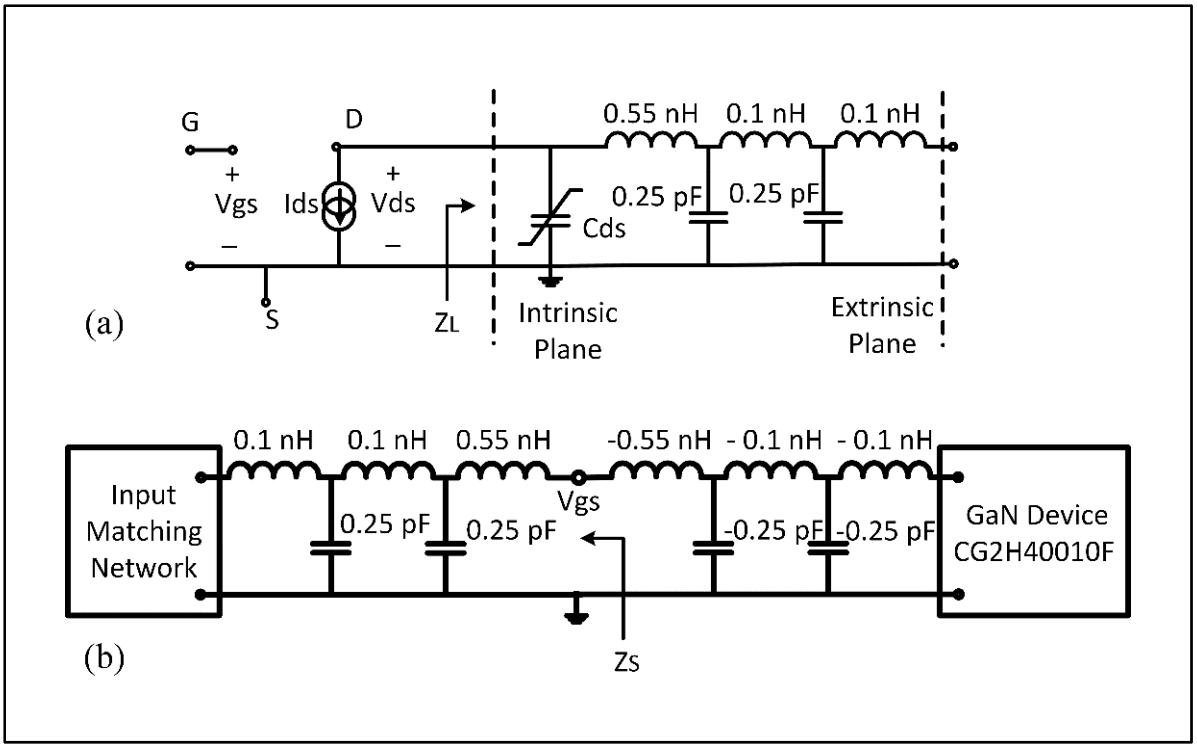


Figure 1.8 Equivalent components for modeling bounding wires and nonlinear drain capacitor in CG2H40010F packed GaN (b) Circuit setup for probing the intrinsic V_{gs} at the packaged device model

1.3.1 Load-pull and Source-pull Methodology

In order to generate the new design space for the fundamental harmonic load impedance through manipulating the second source harmonic in CCGF^{-1}, we start with a load-pull test for the 10-Watt Cree GaN model in class B bias condition at 3.5 GHz center frequency. First, the optimal fundamental output impedance for maximum efficiency is extracted in standard class F^{-1}, with the second harmonic open-circuited and the third harmonic shorted. Under this condition, the power added efficiency (PAE) contours at the packaged device's output plane are computed and shown in Fig. 1.9 (red lines) for the area near maximum. The optimum fundamental load impedance at the center of these contours is then transformed to the drain current generator plane and shown with crossed red sign in Fig. 1.9. The values of these along with their PAE and power performance are given in Table 1.1, class F^{-1}.

Next, keeping the optimal impedance found in the first step, the second harmonic source-pull test is carried out by sweeping the source reflection coefficient Γ_s close to the edge of the Smith chart over 360 degree phase. It was found that by terminating the second source harmonic at 1.2 + j100 Ω higher PAE was achieved. With this new impedance at the source, a second load-pull shows that the PAE contours move from the red to the blue curves and that the corresponding optimum fundamental impedance at the drain current generator plane (Fig. 1.9, red cross) moves towards lower conductance on the Smith chart (Fig. 1.9, blue dot). This movement of the PAE contours, drawn in 2% steps, is in such a way that higher PAE is achieved over a wide range of fundamental load impedances (green points). The resulting PAE contours are between 80% and 89%, which are larger than the maximum 76% PAE achievable with the strand class F^{-1} approach. Therefore, by terminating the second harmonic at the device input properly, not only higher drain efficiency is achievable, but also the optimum fundamental impedance is moved resistively on the Smith chart. Based on Fig. 1.6, utilizing this feature in continuous mode leads to expanding the design space with more constant resistance circles in addition of the phase variation inherent to class CCF^{-1}.This consequently reduces the insertion loss in the output matching network design since: (i) the expanded optimum area simplifies the design of the output matching network by avoiding multiple stubs and transmission lines for controlling the fundamental load trajectory for broadband coverage (ii) choosing higher optimum load impedance reduces the impedance transformation ratio to 50 Ω load.

The final step in the load-pull methodology is to perform a second harmonic tuning at the output fundamental and input second harmonic impedances fixed. Therefore, the second harmonic at output can be exploited for δ between -1 and 1 to generate the design space for fundamental and second harmonic in reactive directions of smith chart. This design space is realized by designing a wideband PA in continuous mode of class GF^{-1} in the next part.

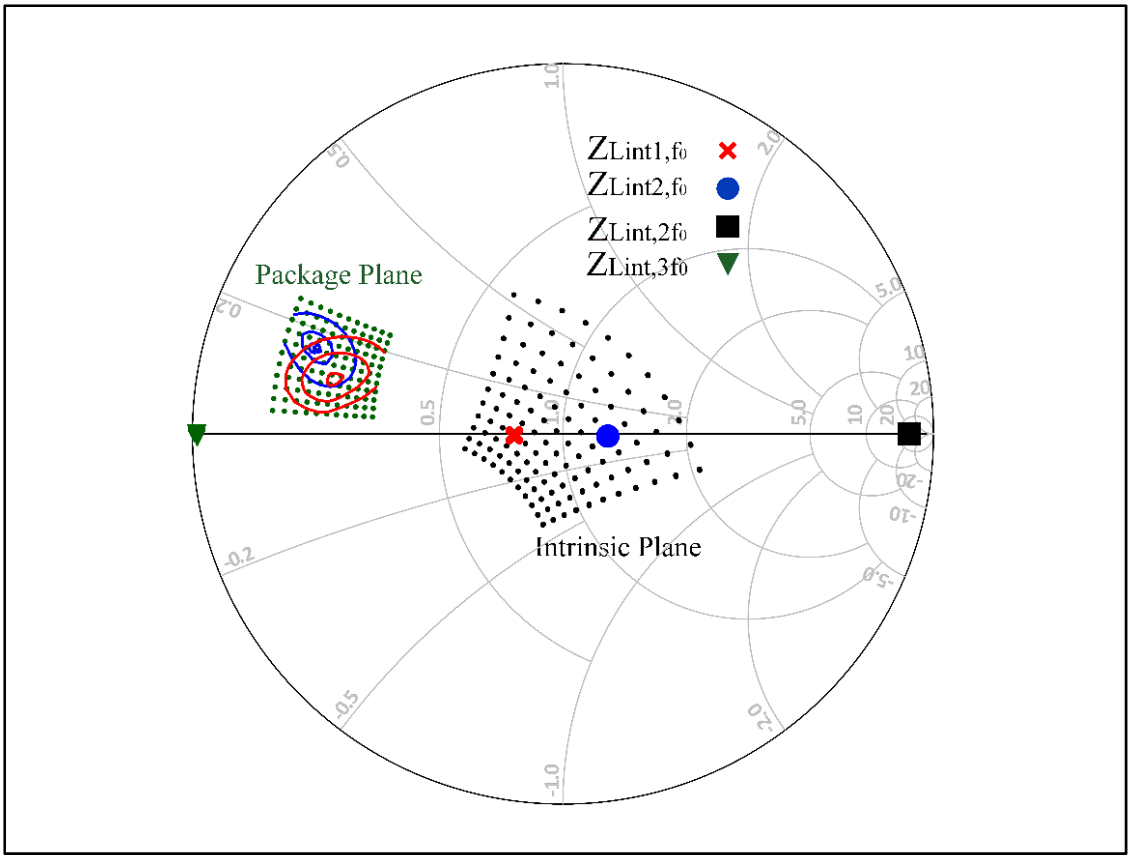


Figure 1.9 Load-pull Smith chart, terminating the second harmonic impedance at the device input in (i) class F^{-1}: PAE contours at package plane (red contours), Z_{Lint1,f_0}: optimum fundamental load impedance at intrinsic plane (red cross), and (ii) class GF^{-1}: PAE contours at package plane (blue contours), Z_{Lint2,f_0}: optimum fundamental load impedance at intrinsic plane (blue dot). In both conditions: $Z_{Lint,2f_0}$: second open circuit (black square), $Z_{Lint,3f_0}$: third short circuit (green triangle), swept impedances at package plane (green dots), and swept impedances at intrinsic plane (black dots)

Table 1.1 Second source and fundamental load harmonic impedance at 3.5 GHz source-pull/load-pull test

Second Harmonic Source Impedance		**Fundamental Harmonic Load Impedance**		**At the Center of Contours**	
Intrinsic plane		Package Plane, Z_{Lpac}	Intrinsic Plane, Z_{Lint}	PAE	Output Power
Class F^{-1}	0.25+j0	13+j5	38+j0.5	76 %	43 dBm
Class GF^{-1}	1.2+j100	9+j9	64−j0.7	89 %	41 dBm

It is noticeable that, with the described source/load-pull procedure, we were able to move the optimal fundamental load impedance into the higher impedance direction on the Smith chart for a fixed voltage waveform. This leads to a decrease of the fundamental drain current as predicted theoretically in Fig. 1.4. Accordingly, the output power is expected to decrease. This can be seen in Table 1.1 where the fundamental output power drops to 41 dBm in class GF^{-1}, from 43 dBm in class F^{-1}, when the input nonlinearity factor is tuned to reach maximum drain efficiency.

1.3.2 PA Circuit Design and Waveforms Analysis

The methodology described in the previous subsection is used to design a wideband $CCGF^{-1}$ PA using the selected GaN device. We seek to achieve a drain efficiency above 70% over the frequency range of 3.1 to 3.9 GHz while maintaining a flat frequency response using simplified matching networks. The Dupont 9K7 substrate with a dielectric constant of 7.2 and a loss tangent of 0.0009 at 10 GHz is used for the PA design. Fig. 1.10 (a) and (b) show schematic diagram of the proposed PA, using ideal transmission lines. The input matching network is made of varying impedance transmission lines (TL_1-TL_5) that in transformation to real microstrip lines, it is necessary to tune the length of the lines to compensate for large discontinuities between high and low characteristic impedances. The layout of the optimized input and output matching networks is illustrated in Fig. 1.10 (c). The corresponding impedance trajectories at the intrinsic reference planes of the input and output (indicated with Z_L and Z_S in Fig. 1.8) for the fundamental and second harmonic frequencies are illustrated in Fig. 1.11.

At the input, the fundamental and second source harmonics are terminated to generate the second harmonic source voltage out-phase with the fundamental harmonic voltage, when $\gamma < 0$, and in-phase, when $\gamma > 0$, at the device gate point. This can be seen by comparing the intrinsic gate-voltage waveforms shown in Figs. 1.12 (a)-(c) with those calculated theoretically and shown in Fig.1.1 for different values of γ. It is important to note that in order to flatten the frequency response, the input matching circuit shown in Fig.1.10 (a) was designed to present a second harmonic source impedance that tracks the gamma factor variation starting from a

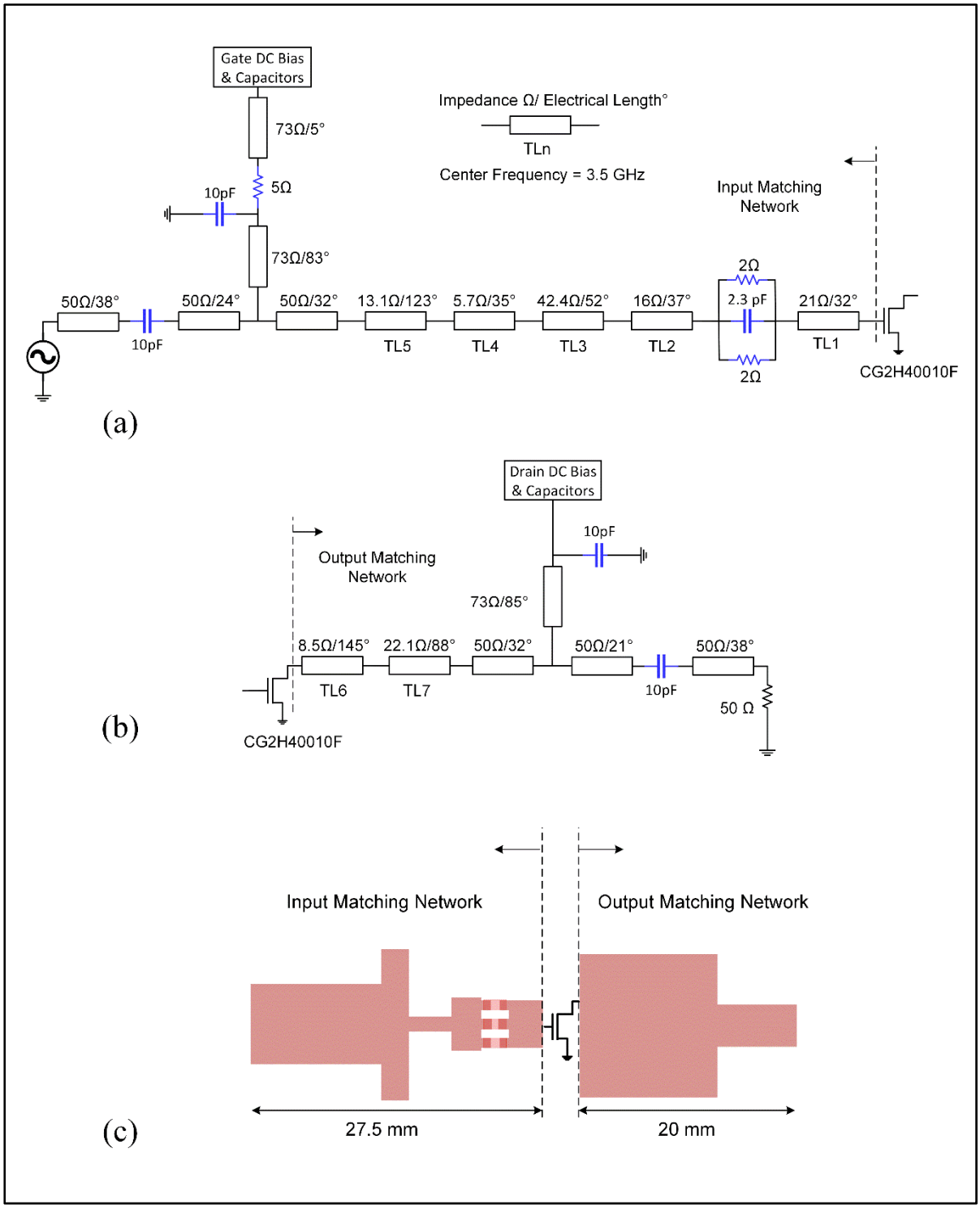


Figure 1.10 PA designed in CCGF^{-1} from 3.1 GHz to 3.9 GHz frequency band, Schematic diagram of designed circuit with ideal components: (a) Input matching network (b) Output matching network; the electrical length of lines are based on the canter frequency at 3.5 GHz. (c) Layout of matching networks

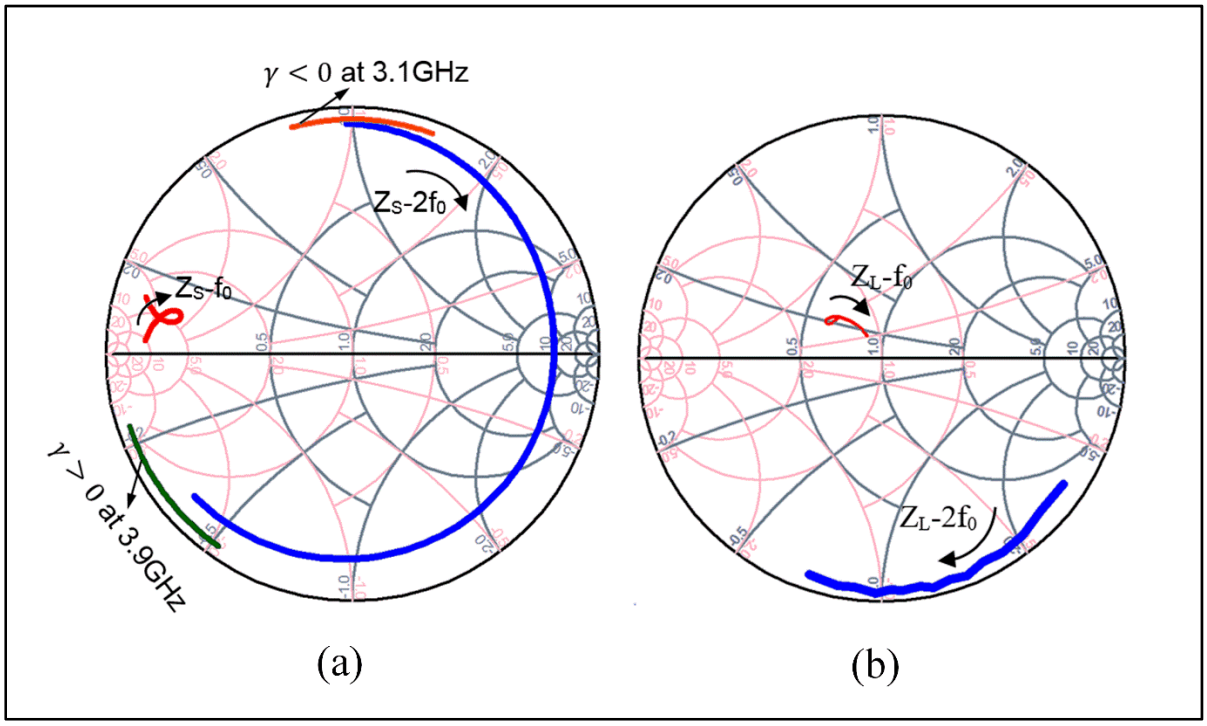


Figure 1.11 PA designed in CCGF^{-1} from 3.1 GHz to 3.9 GHz frequency band (a) Intrinsic trajectory of the source matching network Z_S, with optimum areas at 3.1 GHz (orange line) and 3.9 GHz (green line), (b) Load matching network trajectory at drain current generator plane Z_L; (arrows show the direction of frequency increment)

negative value around 3.1 GHz and increasing with frequency to reach a large positive value at 3.9 GHz. Specifically, at 3.1 GHz the matching circuit gives a second harmonic source impedance of 5+j60 Ω which is very close to the optimal target value of 3+j60 Ω while at 3.9 GHz the circuit presents 4-j10 Ω which is again close to the optimal target of 1.5-j10 Ω. As discussed earlier, this provides higher drain efficiency over an expanded impedance area on the Smith chart (Fig. 1.6) for terminating the output fundamental load.

As a result, the output matching network is designed using two transmission line sections (TL_6 and TL_7) to simultaneously control the fundamental and second harmonics at the intrinsic drain node, as depicted in Fig. 1.10 (a) and (b). It should be noted that, considering the large capacitor at the drain-source intrinsic plane (C_{ds}) and the package parasitic elements, Fig. 1.8 (a), the third harmonic is approximately shorted in this design and not additional matching was needed.

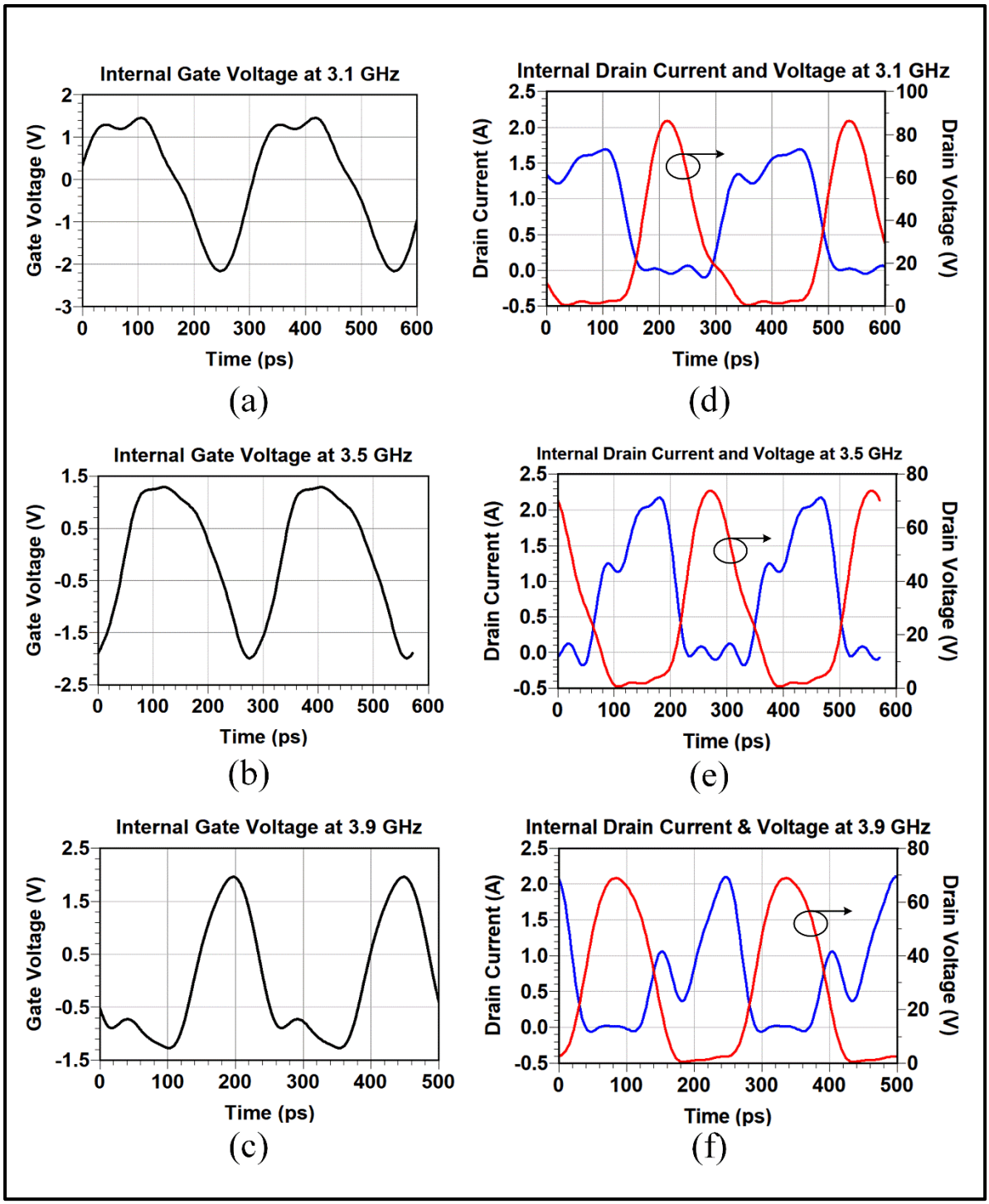


Figure 1.12 Intrinsic waveforms for the designed continuous mode of class GF^{-1} at 3.1 GHz, 3.5GHz ,3.9 GHz: (a)-(c) Gate voltage, (d)-(f) Drain current (blue line) and voltage (red line)

Such a simple and small matching network reduces the output power loss in comparison with conventional CCF^{-1} PA designs, which use multiple stubs and transmission lines in the output matching network to control the load impedance trajectory proper to their design space (Chen *et al.*, 2012), (Yang *et al.*, 2016), (Dhar *et al.*, 2019), (Sun *et al.*, 2015). In other words, we simplified the output matching complexity by adding input matching network for controlling the second source harmonic.

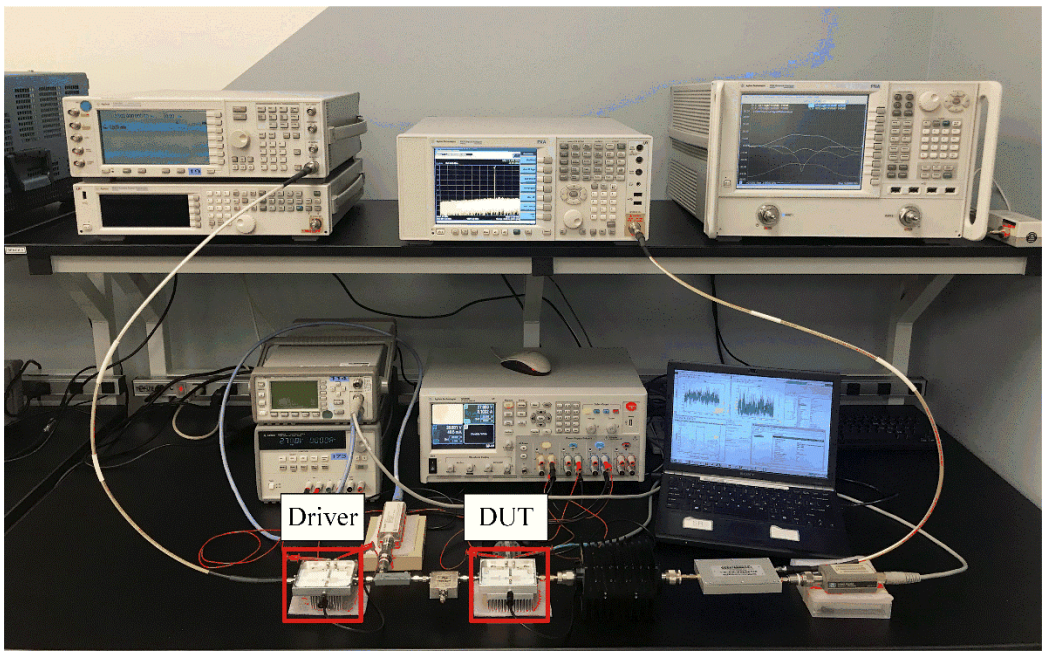
At the output, comparing the load trajectories of Fig. 1.11 (b) with the design space defined in Fig. 1.6 it can be seen that: (i) the δ factor varies between 0 and 1 for the fundamental and second harmonics and (ii) the real part of the fundamental load trajectory varies with increasing frequency. This latter point could lead to degradation in power performance as computed in the extended continuous mode of class F^{-1} (Carrubba *et al.*, 2012). Whereas in the designed CCGF^{-1} PA, by tuning the second harmonic impedance at the device input the optimal fundamental load impedances are expanded radially for the upper half of the desired bandwidth (3.5 GHz to 3.9 GHz). This not only reduces mismatching over the band but also improves drain efficiency to compensate for power performance degradation, which happens inherently with increasing frequency.

The drain current and the half sinusoidal voltage waveforms of the designed CCGF^{-1} PA are shown in Figs. 12(d)-(f) at three frequencies within the bandwidth. These figures show that, by increasing the frequency, the peak of the drain current waveforms increases asymmetrically for positive amounts of δ, which is consistent with the predicted waveforms in theory as shown in Figs. 1.3(c) and 1.3(d). It should also be noted that moving toward higher γ and δ factors over the frequency band leads to generating a larger component of second harmonic drain current in continuous mode, which compensates the fall in fundamental drain current and, consequently, the level of total current is maintained almost constant at the output.

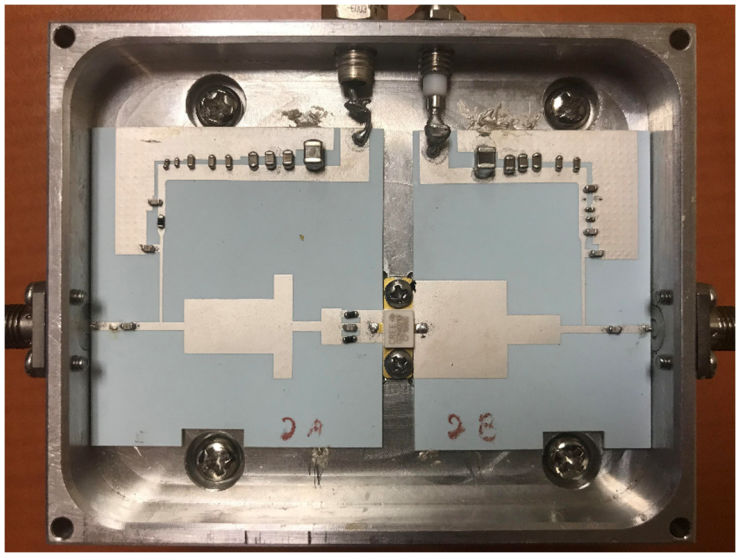
1.4 PA Fabrication and Measurement Results

In section 1.3, it was shown that by controlling the second harmonic at the input of a GaN device, we can generate a felexiable large area for terminateing the fundamental output harmonic. This led to designing a very simple output matching network that simultaneously controls the fundamental and second harmonics over a wide frequency range. A prototype of the designed CCGF^{-1} PA is implemented utilizing the proposed theory and using a packaged 10-Watt GaN Cree device and the low-loss Dupont 9K7 substrate at the in-house LTCC laboratory. The assembled PA as well as the measurment setup for continuouse wave (CW) and modulated signal measurements are shown in Fig 1.13.

The measured power performance of the CCGF^{-1} PA is depicted in Fig. 1.14 and compared to the simulated results when the PA is biased in deep class AB at quiescent drain current of I_{DS}= 25 mA and 28 V drain voltage. At this bias point the variations of β factor is less than 2° compared to the class B bias point, which is negligible for the predicted design space of the fundamental load impedance in theory. Fig. 1.14 (a) shows that the measured results give above 70 % drain efficiency and 65 % PAE from 3.05 GHz to 3.85 GHz at 3-dB gain compression point and are in good agreement with simulations, with a slight shift observed due to fabrication tolerances. The same figure also shows measured and simulated values for the 3-dB saturated output power, between 39.9 dBm and 41.4 dBm, and gain, between 11 dB and 12.4 dB, over the entire frequency bandwidth. In addition, Fig. 1.14 (b) illustrates the PA performance versus input power at 4 frequencies within the bandwidth. It can be seen that, the frequency response variation due to mismatch at the middle or edges of the PAs bandwidth is minimized with this design. This was achieved by the proper tuning of the second source harmonic in the upper half of the desired bandwidth to expand the optimum design area for terminating the fundamental load harmonic. It is worth noting that the gain variations is kept to less than ± 0.7 dB over the desired bandwidth, despite the inherent downward trend of the maximum available gain of the GaN device, which drops about 5 dB from 3 GHz to 4 GHz. Table 1.2 shows the performance of the designed PA compared to that in the reported literature for similar frequencies or continuous modes operation.



(a)



(b)

Figure 1.13 Measurement setup for CW and modulation signal tests, (b) Prototype wideband CCGF^{-1} PA

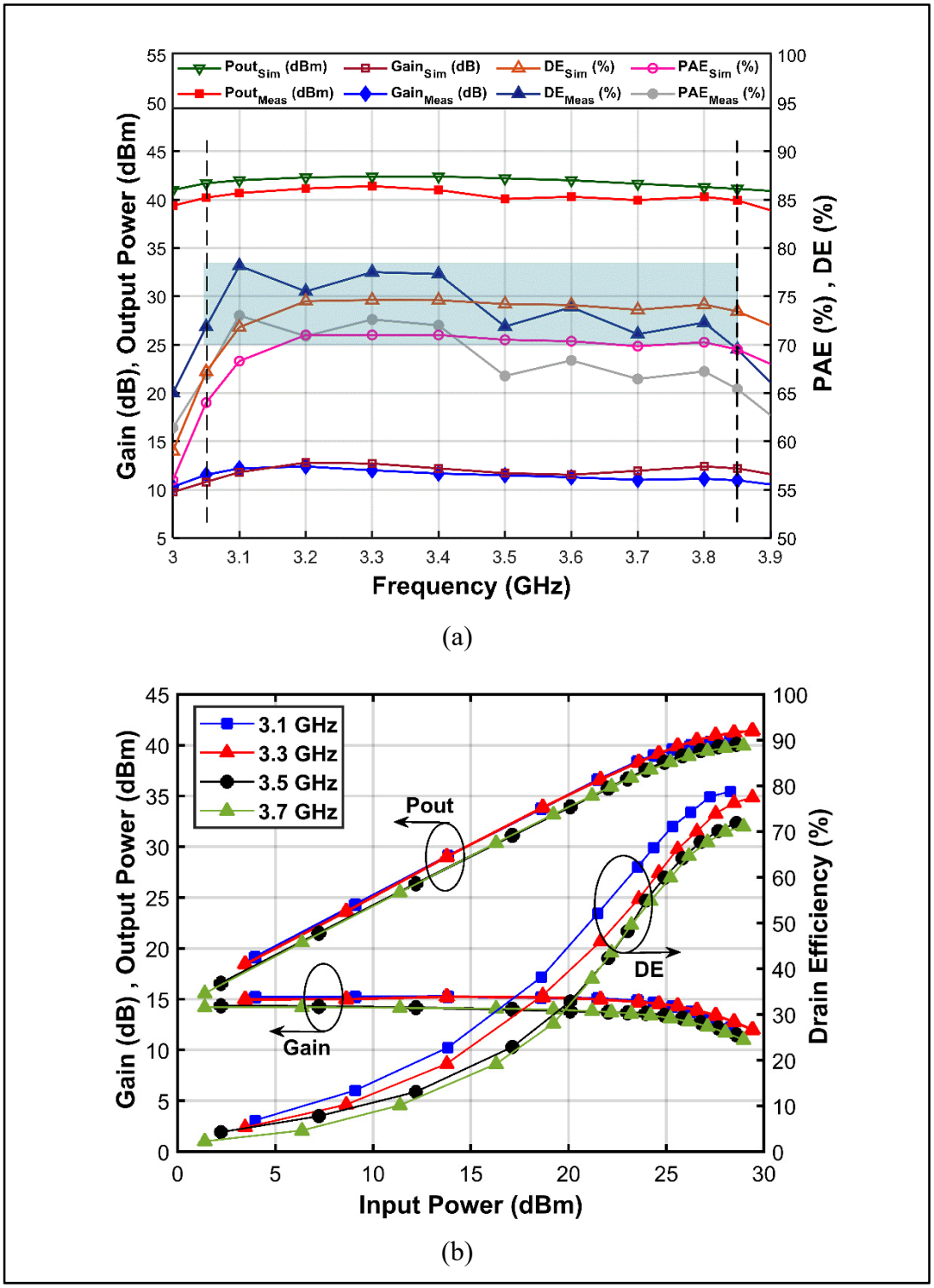


Figure 1.14 Measured and simulated results for output power (dBm), drain efficiency (%), power added efficiency (%) and gain (dB). (a) Frequency response of the CCGF^{-1} PA power performance at 3-dB gain compression from 3 GHz to 3.9 GHz. (b) CW measured power sweep at four frequency points over the bandwidth

Table 1.2 Performance comparison of high-efficiency PAs operating at similar frequencies or designed in continuous mode

Ref	**Frequency (GHz)**	**Pout (dBm)**	**Gain (dB)**	**DE (%)**	**PAE (%)**	**Class***
Pang *et al.*, 2016	0.8-3.6	39.5-42.1	10-13	56-74	N/A	CCJ
Shi *et al.*, 2016	2.4-3.9	39.6-41.4	10.7-12.5	62-75	58-69	CCF^{-1}
Li *et al.*, 2016	3.2-3.7	40.2-42	9.9-11.6	70-83	63-78	HCIMPA
Saxena *et al.*, 2017	1.3-2.4	40.1-41.2	11.4-14.3	63-72	N/A	CCB/J
Li *et al.*, 2018	1.24-2.42	37-39.9	9-12	70-86	N/A	X
Huang *et al.*, 2018	1.2-3.6	40-42.2	10.5-12.5	60-72	N/A	CCJ/F
Dhar et al., 2019	0.8-1.4	38-42.3	9-13	75-93	73-82	$ICCF^{-1}$
Zhou et al., 2020	3.4-3.6	38.5-40	9.4-11.5	N/A	63 -67	$DM\text{-}F^{-1}$
	3.5-3.75	≤ 38.5	9-11.8	N/A	60-66	$QM\text{-}F^{-1}$
This Work	3.05-3.85	39.9-41.4	11 -12.4	70-78	65-73	$CCGF^{-1}$

The linearity performance of the PA is assessed with measuring the adjacent channel power ratio (ACPR) at four frequency points over the bandwidth, without applying any linearization techniques. In this test, we used a standard 20 MHz LTE OFDM signal with 10.45 dB peak-to-average power ratio (PAPR) and sampling rate of 96.5 MHz. The test results are illustrated in Fig. 1.15, which shows an ACPR of better than 26 dBc up to 32 dBm average output power, i.e., at 8 dB back-off.

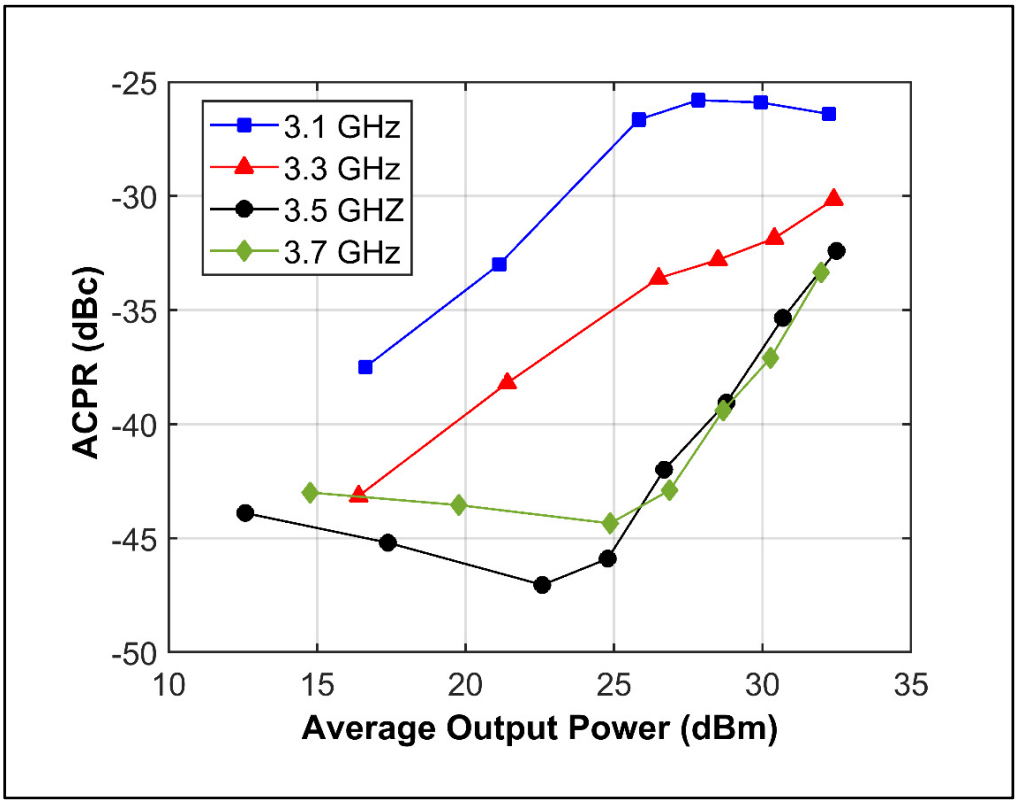


Figure 1.15 Linearity performance of the wideband PA at four frequency points over the bandwidth, using 20 MHz standard LTE signal with 10.45 dB PAPR

1.5 Conclusion

In this paper a comprehensive analysis of continuous inverse class GF ($CCGF^{-1}$) was presented based on a new closed-form expression for the drain current. Unlike the conventional continuous mode class F^{-1} approach where the input second harmonic is shorted, it was shown that controlling the second source harmonic impedance contribute to: (i) improving PA efficiency and (ii) expanding the design space for the fundamental output matching impedance. With the second harmonic properly matched at the input, the output matching network design is simplified. As a result, losses are reduced at the output, leading to increased efficiency, while making it easier to achieve better flatness and bandwidth coverage. This approach was validated through the design, fabrication and measurement of a $CCGF^{-1}$ PA using a packaged 10-Watt GaN device on an LTCC substrate. The measured results show a drain efficiency of more than 70% from 3.05 GHz to 3.85GHz, a gain between 11 and 12.4 dB with a gain flatness of ± 0.7 dB and an output power at 3-dB gain compression between 39.9 and 41.4 dBm. It was also shown that the fabricated amplifier displayed an ACPR level better than 26 dBc over the entire band under a 20 MHz LTE signal having a PAPR of 10.45 dB, without any linearization.

CHAPTER 2

THE SECOND SOURCE HARMONIC OPTIMIZATION IN CONTINUOUS CLASS-GF POWER AMPLIFIERS

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Abstract

In this paper, the theory of continuous mode class GF (CCGF) power amplifier (PA) is introduced and applied to flatten the PA's frequency response over a wideband. The effects of controlling the input nonlinearity of the gate-source capacitance (C_{gs}) on the drain current waveforms are analyzed under continuous mode drain voltage waveforms. A wideband CCGF PA is designed and fabricated using a commercial 10-Watt Gallium Nitride (GaN) device and low temperature co-fired ceramic (LTCC) technology. Results of measurement show a flat frequency response from 3.3 GHz to 4.3 GHz with variations less than ± 0.4 dB for 40 dBm output power, and 17 dB large signal gain at 3-dB compression point. A drain efficiency of 66% ± 2% is achieved over the entire bandwidth. The fabricated PA has a measured adjacent channel power ratio of 24 dBc or better under a 20 MHz LTE signal over the entire bandwidth.

Introduction

High-Efficiency wideband power amplifiers (PAs) are in widespread demand in novel wireless transceivers to increase data transfer rates and to address network-wide spectral and power efficiencies, particularly with the increasing number of users and connected devices. These needs make it necessary to incorporate efficiency enhancement techniques that reduce dissipated power in the design of broadband PAs. In this regard, emerging continuous mode

power amplifiers have provided multiple solutions for simplifying the design of wideband matching networks and expanding the operational bandwidth in PA design (Sharma *et al.*, 2016; Saxena *et al.*, 2017; Lu *et al.*, 2013).

In continuous mode PAs, the imaginary part of the optimum fundamental load impedance can be variable on the constant resistive circles of the Smith chart while the second harmonic load is tuned on the edge of Smith chart instead of the fixed shorted or opened circuits (Wright *et al.*, 2009; Carrubba *et al.*, 2010; Carrubba *et al.*, 2011; Rezaei *et al.*, 2014). Specifically, in continuous class F (CCF), the design space is generated from extracting the family of drain voltage waveforms for a half-sinusoidal current waveform while the second source harmonic is shorted (Carrubba *et al.*, 2010). However, providing a short circuit for the second harmonic at the gate plane in wideband operations and continuous modes is almost impossible.

In (Sharma *et al.*, 2018), the effects of controlling the input nonlinearity by tuning the second source harmonic on PA performance were analyzed in class GF/GF^{-1} at a single frequency. A recent research investigated these effects on continuous mode of invers class GF (CCGF^{-1}) based on a new drain current expression and waveforms (Eskandari *et al.*, 2021). In this paper, we extend to work of (Eskandari *et al.*, 2021) to the case of continuous class GF (CCGF) and demonstrate the impact of tuning the second source harmonic on the drain current and PA performance, instead of simply supposing a short circuit. Unlike the CCGF^{-1} mode where current overshoot can occur, the obtained drain current waveforms in the CCGF mode do not exceed the maximum drain current. Since the current overshoot can negatively affect the reliability of the device over time while simultaneously increasing the overlap with the voltage waveform in continuous mode, avoiding it by going to the CCGF mode will alleviate these problems. Furthermore, a new design space can be explored by combining of the input nonlinear factor, γ, with the continuous mode factor, δ, in CCGF mode.

2.1 Continuous Mode Class-GF Theory

2.1.1 Input Nonlinearity

The voltage waveform at the intrinsic gate plane of device is supposed to be an ideal sinusoidal in standard class F (Raab *et al.*, 1997). Considering the nonlinearity of the gate-source capacitance (C_{gs}) in generating the second harmonic component at the device input (Sharma *et al.*, 2018) the ideal sinusoidal waveform can be altered to half-sinusoidal shape. Hence, the modified gate–source voltage (V_{gs}) in the presence of the second harmonic voltage component (V_2) at different bias conditions can be expressed as:

$$V_{gs}\,(\theta,\alpha) = V_{gso} + V_1\left(\frac{\cos\theta - \cos\frac{\alpha}{2}}{1-\cos\frac{\alpha}{2}}\right) + V_2\,\cos 2\theta \tag{2.1}$$

Normalizing this equation to the fundamental harmonic voltage (V_1), the normalized gate-source voltage $\overline{Vgs}$ is given by:

$$\overline{V_{gs}\,(\theta,\alpha,\gamma)} = \frac{V_{gso}}{V_1} + \left(\frac{\cos\theta - \cos\frac{\alpha}{2}}{1-\cos\frac{\alpha}{2}}\right) + \gamma\,\cos 2\theta \tag{2.2}$$

where, $\gamma = V_2 / V_1$ is the ratio of second harmonic to fundamental voltage components at the input, α and θ are conduction angle and angular frequency, respectively. Using (2.2), the modified input voltage waveforms for zero gate bias voltage (V_{gso}= 0) and class B bias condition are computed and plotted in Fig.2.1.

It can be seen that the fire angle (2β) at the pinch-off gate voltage varies significantly as a function of the γ factor, from 144^o to 224^o. This changes the device switching speed and consequently the conduction angle for the drain current. In Fig. 2.2 it is shown that, the conduction angle is reduced by increasing the γ value from -0.5 to 0.5 in class B bias condition. Considering the non-linear transconductance of device, these variations are transformed to the

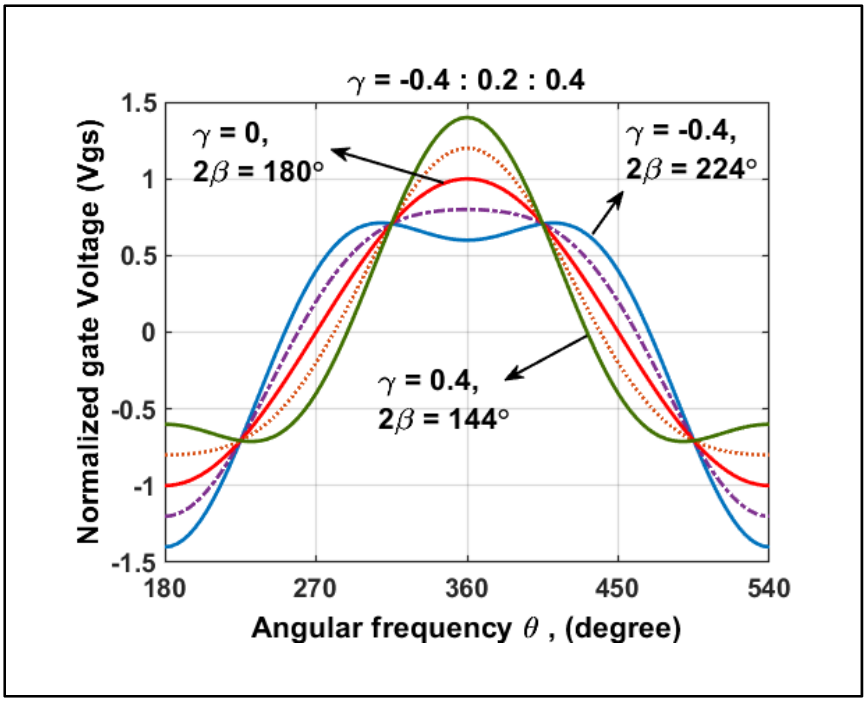

Figure 2.1 Gate-source voltage (V_{gs}) normalized to the fundamental harmonic (V_1) for $-0.4 \leq \gamma \leq 0.4$ in step of 0.2

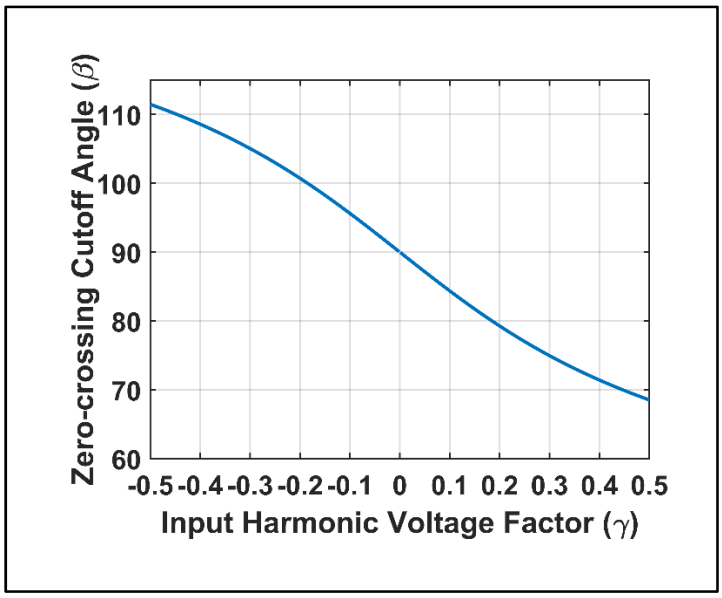

Figure 2.2 Zero-crossing cutoff angle (β) in class B bias condition

drain current and impact on its waveforms, which are investigated in next section. In fact, by zeroing the normalized V_{gs} of (1.2), the new zero crossing angle (β) can be obtained as follows:

$$\beta(\alpha,\gamma) = \begin{cases} \cos^{-1}\left(\dfrac{\dfrac{-1}{1-\cos\frac{\alpha}{2}} + \sqrt{\left(\dfrac{-1}{1-\cos\frac{\alpha}{2}}\right)^2 + 8\gamma\left(\gamma + \dfrac{\cos\frac{\alpha}{2}}{1-\cos\frac{\alpha}{2}}\right)}}{4\gamma}\right), & -0.5 < \gamma < 0.5, \quad \gamma \neq 0 \\ \dfrac{\alpha}{2}, & \gamma = 0 \end{cases} \tag{2.3}$$

2.2 Voltage and Current Waveforms in CCGF

The normalized drain voltage waveforms of the fundamental harmonic, V_1, in continuous mode class F is obtained by multiplying the voltage waveform of standard class F by (1-$\delta \sin\theta$) and is given as (Carrubba *et al.*, 2010):

$$V_{ds,CCF} = \left(1 - \frac{2}{\sqrt{3}}\cos\theta + \frac{1}{3\sqrt{3}}\cos 3\theta\right) \times (1 - \delta \sin\theta) \tag{2.4}$$

Where δ is the continuous mode factor. Since the family waveforms of the drain voltage for $\delta \neq 0$ can be asymmetrically moved to the sides of an ideal square wave ($\delta = 0$), the overlap area between the voltage and the drain current waveforms for each value of δ is variable. This is more critical in the design of wideband PAs given that the drain current waveforms can be varied from the ideal half sinusoidal shape when the second source harmonic is terminated by impedances other than the short circuit. In order to investigate the impact of tuning the second harmonic at the input on the drain current waveforms in continuous mode operation and the resulting modified conduction angle variation, the drain current can be expressed based on the input nonlinearity factor, γ, as:

$$i_{CCGF}(\theta,\alpha,\gamma,I_m) = \tag{2.5}$$

$$\begin{cases} \dfrac{I_m + i_{r3}(\alpha,\beta,\gamma,I_m)}{1+\gamma} \times \left(\dfrac{\cos\theta - \cos\frac{\alpha}{2}}{1-\cos\frac{\alpha}{2}} + \gamma\ \cos 2\theta \right) \\ \qquad -i_{r3}(\beta,\alpha,\gamma,I_m)\ \cos 3\theta \qquad -\beta < \theta < \beta \\ 0\ , \qquad\qquad -\pi < \theta < \beta\ , \qquad \beta < \theta < \pi \end{cases}$$

where, $i_{r3}\ (\alpha,\beta,\gamma,I_m)$ is the real part of the third harmonic drain current and by applying the boundary condition in class GF can be obtained as follows:

$$\frac{1}{\pi}\int_{-\beta}^{\beta} i_{CCGF}(\theta,\alpha,\gamma,I_m)\ .\ \cos 3\theta\ d\theta = 0 \tag{2.6}$$

$$i_{r3}(\alpha,\beta,\gamma,I_m) = \tag{2.7}$$

$$\frac{\frac{I_m}{1+\gamma}\left[\gamma\left(\sin\beta + \frac{\sin 5\beta}{5}\right) + \frac{2\cos\frac{\alpha}{2}\sin 3\beta}{3\left(\cos\frac{\alpha}{2}-1\right)} - \frac{2\sin\beta\ \cos^3\beta}{\left(\cos\frac{\alpha}{2}-1\right)}\right]}{\beta + \frac{\sin 6\beta}{6} - \frac{I_m}{1+\gamma}\left[\gamma\left(\sin\beta + \frac{\sin 5\beta}{5}\right) + \frac{2\cos\frac{\alpha}{2}\sin 3\beta}{3\left(\cos\frac{\alpha}{2}-1\right)} - \frac{2\sin\beta\ \cos^3\beta}{\left(\cos\frac{\alpha}{2}-1\right)}\right]}$$

Using (1.4) and (1.5), the current and voltage waveforms in class CCGF are computed and shown in Fig. 2.3 for -0.5 ≤ γ ≤ 0.5 and -1 ≤ δ ≤ 1. It can be seen that, for γ < 0 the family of drain current waveforms are no longer ideal half-sinusoids, as shown in Fig. 2.3 (a), whereas for γ > 0 these waveforms become quasi-square shaped as depicted in Fig. 2.3 (b). Fig. 2.3 also shows the superposed voltage waveforms as a function of the continuous mode factor, δ, and clearly demonstrates that tuning the second source harmonic with negative γ increases the overlap between the voltage and drain current waveforms thereby increasing the internal power dissipation. On the other hand, positive γ values clearly lead to reduce overlap and decrease power dissipation, which result in improved efficiency. To quantify this, the theoretical drain efficiency, η_{CCGF}, can be obtained by:

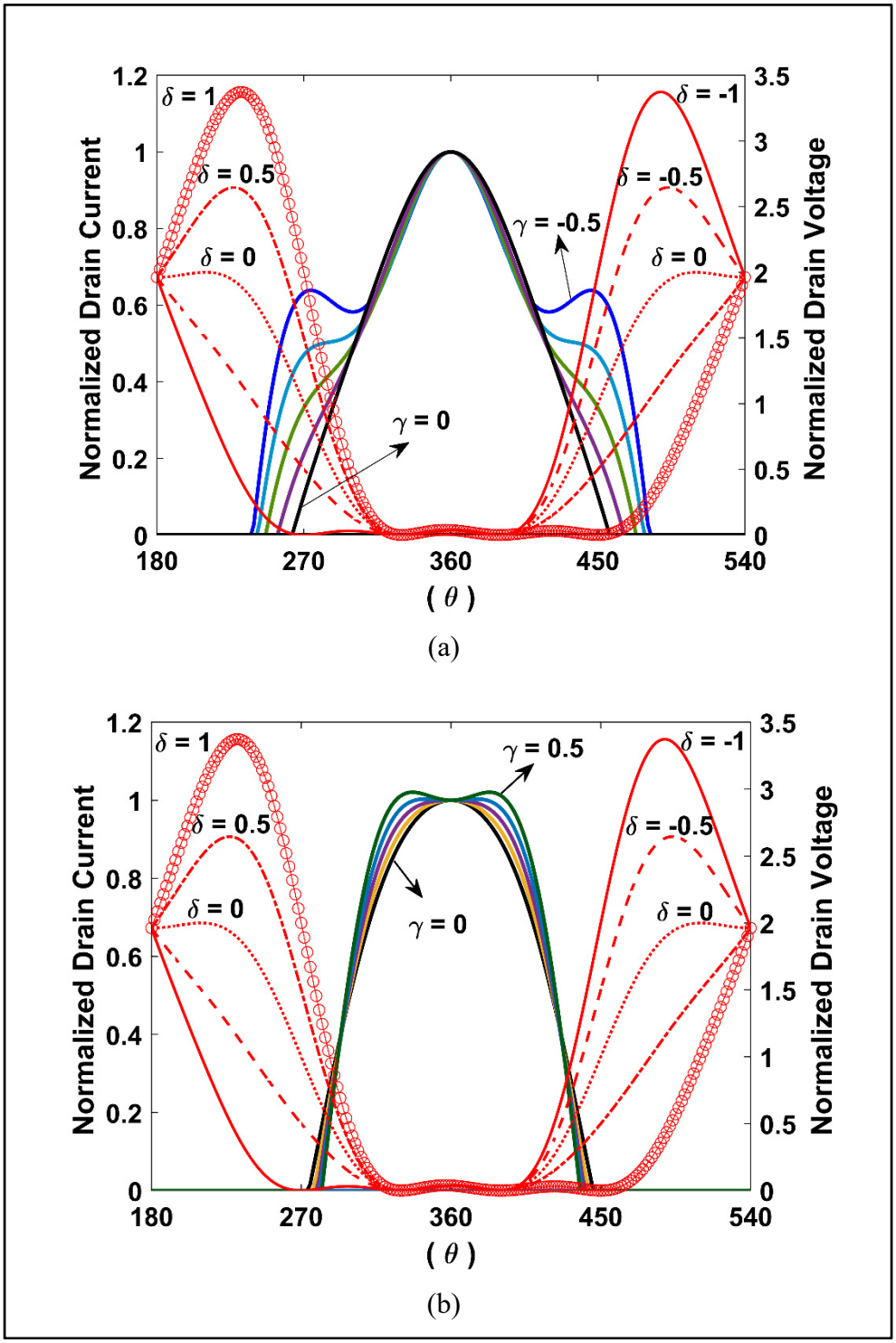

Figure 2.3 Drain voltage (red lines) and current waveforms in CCGF for $-1 \le \delta \le 1$ in step of 0.5, (a) $-0.5 \le \gamma \le 0$, (b) $0 \le \gamma \le 0.5$ in step of 0.1

$$\eta_{CCGF} = \frac{P_{out\_CCGF}}{P_{dc\_CCGF}} = \frac{\frac{1}{\sqrt{3}}\,(V_{dc} - V_k)\; i_{CCGF,1}(\theta, \alpha, \gamma, I_m)}{V_{dc}\;\; i_{CCGF,dc}(\theta, \alpha, \gamma, I_m)} \tag{2.8}$$

where V_{dc} and V_k are the DC voltage and device knee voltage, respectively, and the DC component, $i_{CCGF,dc}$, the first and second harmonics of drain current, $i_{CCGF,1}$ and $i_{CCGF,2}$, are given by:

$$i_{CCGF,dc}(\theta, \alpha, \gamma, I_m) = \tag{2.9}$$
$$\frac{I_m + i_{r3}(\alpha, \beta, \gamma, I_m)}{2\pi\,(1+\gamma)} \times \left(\frac{2\beta\;\cos\frac{\alpha}{2} - 2\;\sin\beta}{\cos\frac{\alpha}{2} - 1} + \gamma\;\sin 2\beta \right)$$
$$- \frac{i_{r3}(\alpha, \beta, \gamma, I_m)\sin 3\beta}{3\pi}$$

$$i_{CCGF,1}(\theta, \alpha, \gamma, I_m) = \tag{2.10}$$
$$\frac{I_m + i_{r3}(\alpha, \beta, \gamma, I_m)}{\pi\,(1+\gamma)}$$
$$\times \left(2\gamma\;\sin\beta - \frac{4}{3}\,\gamma\sin^3\beta + \frac{2\sin\beta\;\cos\frac{\alpha}{2} - \left(\beta + \frac{\sin 2\beta}{2}\right)}{\cos\frac{\alpha}{2} - 1} \right)$$
$$- \frac{2\;i_{r3}(\alpha, \beta, \gamma, I_m)\sin\beta\;\cos^3\beta}{\pi}$$

$$i_{CCGF,2}(\theta, \alpha, \gamma, I_m) = \tag{2.11}$$
$$\frac{I_m + i_{r3}(\alpha, \beta, \gamma, I_m)}{\pi\,(1+\gamma)}$$
$$\times \left(\gamma\left(\beta + \frac{\sin 4\beta}{4}\right) \frac{2\sin\beta\;\cos\frac{\alpha}{2} - 2\sin\beta + \frac{4}{3}\sin^3\beta}{\cos\frac{\alpha}{2} - 1} \right)$$
$$- \frac{i_{r3}(\alpha, \beta, \gamma, I_m)}{\pi}\left(\sin\beta + \frac{\sin 5\beta}{5}\right)$$

In order to analyze the power performance in CCGF versus the γ factor, the normalized values of the DC and fundamental components of the drain current, (1.9-1.10), along with the drain efficiency, (1.8), are shown in Fig. 2.4. It should be noted that the knee voltage is neglected in these calculations given that $V_{dc} >> V_k$ in GaN devices. It can be seen that, the drain efficiency increases significantly when the γ factor varies from – 0.5 to 0. This is due more to the reduction of the DC power consumption, i.e., DC drain current, rather than the increase in the fundamental output power, i.e., fundamental drain current. This can be explained by considering the larger conduction angle β in the drain current waveform for the negative values of γ in Fig. 2.2 which leads to a larger DC component in (1.9). The extra DC power is dissipated in the active device, which is consistent with the increasing overlap between the drain voltage and current waveforms for negative γ as shown in Fig. 2.2. On the other hand, the DC current consumption is almost constant for the positive values of γ whereas the fundamental output current and drain efficiency are increasing slightly. Therefore, it is expected that tuning the second source harmonic in the positive range of γ can lead to reducing the internal power dissipation and flattening the frequency response.

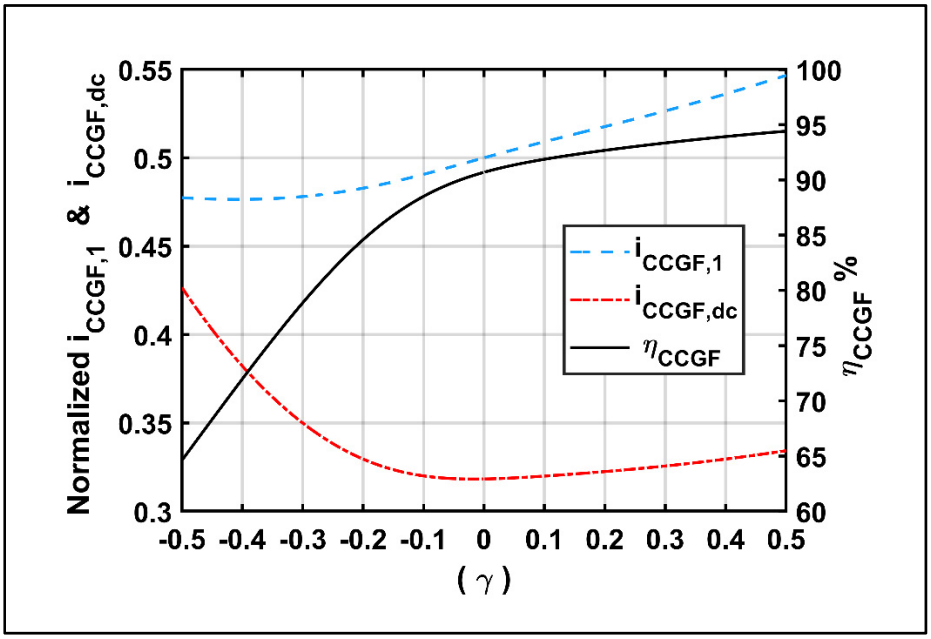

Figure 2.4 Theoretical drain efficiency in CCGF PA (η_{CCGF} %), Normalized DC and fundamental current to I_m for -0.5 ≤ γ ≤ 0.5

2.3 Load Design Space in CCGF

Since the control of the second harmonic at the input in continuous class GF leads to a family of modified drain current harmonics, a new load design space can be established. Using (1.4), (1.10) and (1.11) the harmonic components of the output impedance are given as follows:

$$Z_{CCGF,1}(\theta, \alpha, \gamma, I_m, \delta) = \frac{2}{\sqrt{3}\, i_{CCGF,1}} + j\, \frac{\delta}{i_{CCGF,1}} \tag{2.12}$$

$$Z_{CCGF,2}(\theta, \alpha, \gamma, I_m, \delta) = j \frac{-7\delta}{6\sqrt{3}\, i_{CCGF,2}} \tag{2.13}$$

$$Z_{CCGF,3}(\theta, \alpha, \gamma, I_m, \delta) = \infty \tag{2.14}$$

The design space for CCGF is determined by the ranges of the γ and δ factors. Fig. 2.5 shows this space when γ is swept from -0.5 to 0.5 and δ from -1 to 1 to prevent from crossing the zero-current axis. The real part of fundamental output impedance varies with γ, while its imaginary part varies as a function of both δ and γ. This provides a new design space in CCGF for terminating the fundamental load impedance in the resistive direction of the Smith chart by contrast with the conventional CCF that predicts only the phase variation on constant resistive circles with sweeping the δ factor. The second load harmonic, that only includes the imaginary part, is varying on the edge of the Smith chart for different combinations of the δ and γ factors.

2.4 Wideband PA Design and Fabrication in Continuous Mode of Class GF

The described theory in the previous section and the expanded design space are applied to the design and fabrication of a wideband PA in continuous mode of class GF. The goal is to achieve a flat frequency response with minimal degradation of drain efficiency and output power from 3.3 GHz to 4.3 GHz. A commercially available 10-Watt Qorvo QPD1022 GaN packaged device is chosen to this end. Low-loss Dupont 9K7 LTCC substrate is used for prototyping using an in-house process.

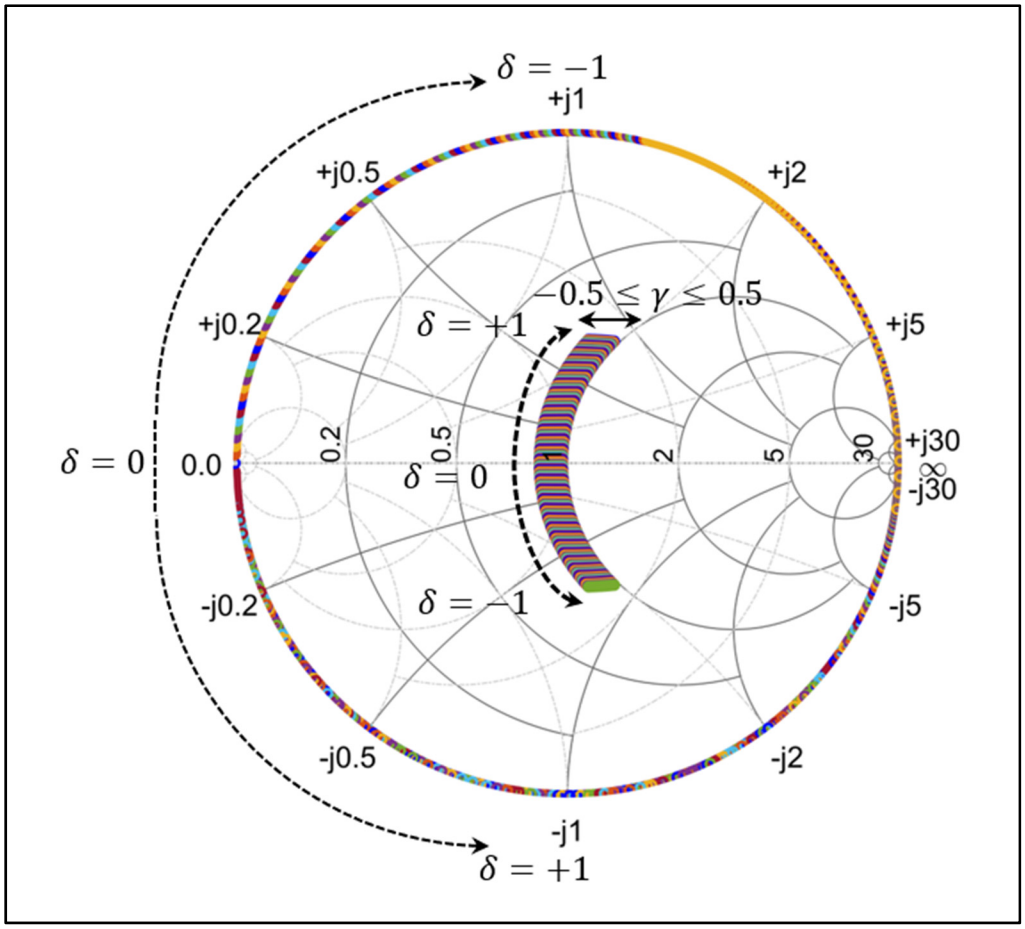

Figure 2.5 New design space in CCGF for terminating the fundamental and second harmonics in output matching network

2.4.1 Circuit Design and Waveform Analysis of CCGF PA

A nonlinear circuit model for the selected QPD1022 device is provided by Modelithics, Inc. and is available in Keysight ADS, with access to the current and voltage waveforms at the internal reference planes of the gate and drain. Using this model and standard multi-harmonic load-pull simulation, we start by determining the optimal fundamental load impedance while the second source harmonic is shorted at each frequency. Next, with the load impedance fixed, we sweep the second source harmonic impedance near the edge of the Smith chart to extract the optimum impedance for achieving the desired gate-source voltage waveform at the device input for each selected frequency. Thereafter, the input matching network, depicted in Fig. 2.6, is designed to provide the optimal impedances found, keeping $\gamma \geq 0$ to prevent from drain

efficiency degradation within the desired bandwidth. At this point, the design space predicted in Fig. 2.5 can be generated and used to extract the optimum fundamental and second harmonic load impedances. These impedances are used to design the output matching network as shown in Fig. 2.6.

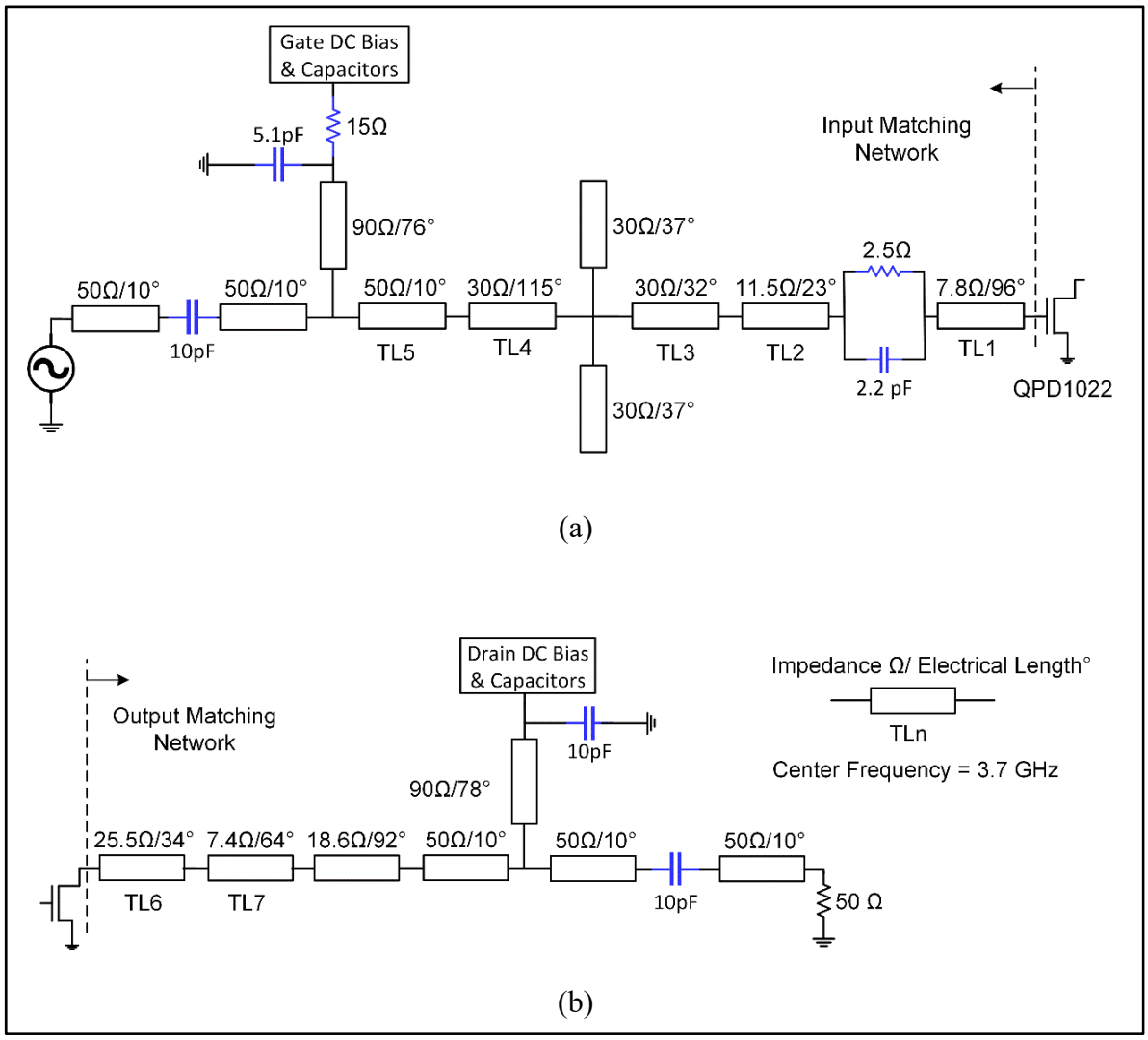

Figure 2.6 Schematic diagram of designed circuit with ideal components. (a) Input matching network, (b) Output matching Network

The voltage and drain current waveforms at the internal reference plane of the device and their corresponding voltage waveforms at the internal gate point are shown in Fig. 2.6 for three frequencies. It can be seen that, at 3.2 GHz where $\gamma = 0$, the drain current has a half-sinusoidal shape while at 3.7 GHz and 4.3 GHz, where $\gamma > 0$, it has quasi-square waveforms with reduced

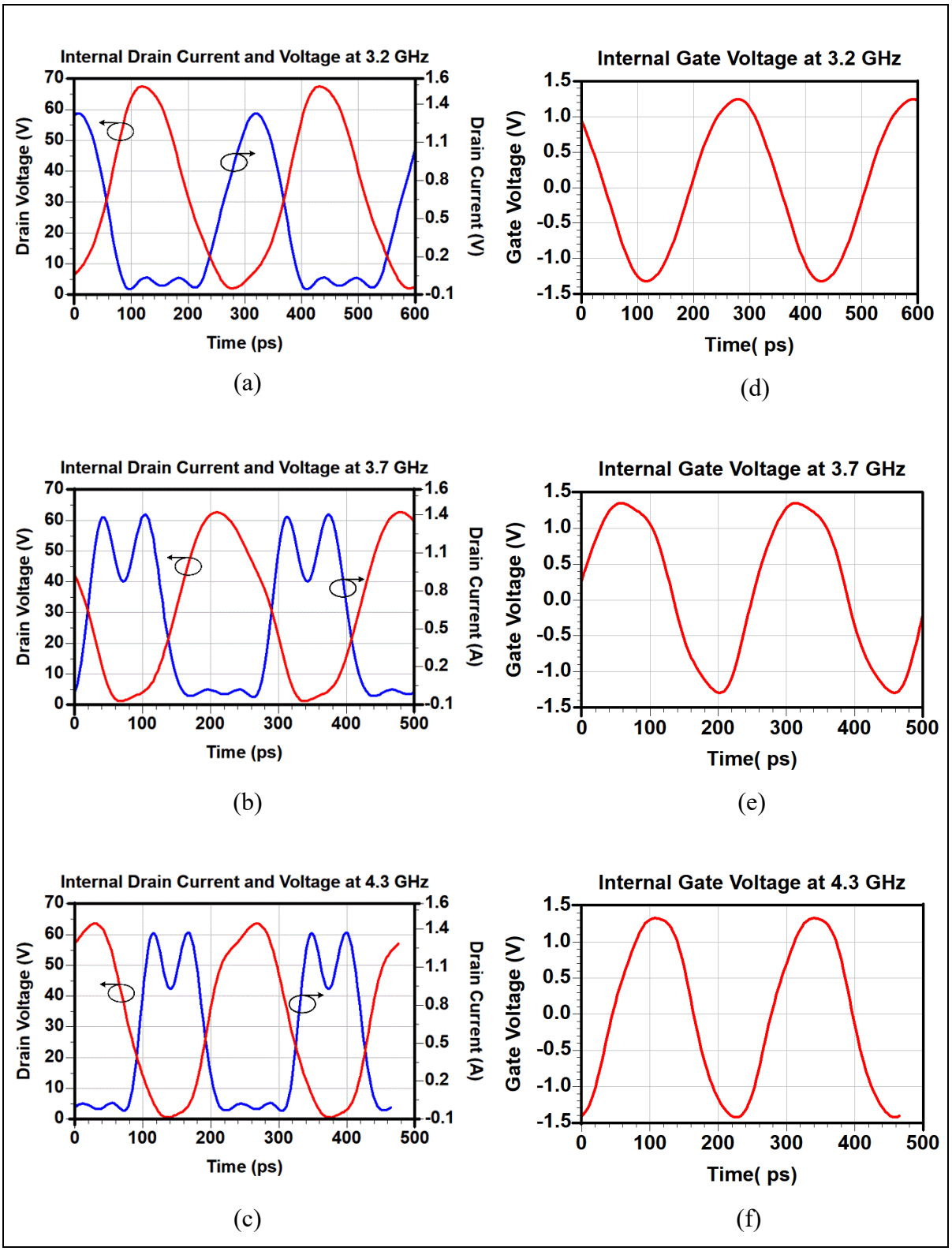

Figure 2.7 Internal waveforms of the designed continuous class GF at 3.2 GHz, 3.7 GHz, 4.3 GHz: (a)-(c) Voltage (red line) and drain current (blue line), (d)-(f) Gate voltage

overlap between the voltage and drain current waveforms in continuous mode operation. This is consistent with the waveforms obtained in the CCGF theory and can be verified by comparing the waveforms illustrated in Fig. 2.7 with the predicted ones in Fig. 2.1, for the gate voltage, and Fig. 2.3 for the drain voltage and current waveforms.

2.4.2 PA Fabrication in CCGF and Measurement Results

The designed matching networks are realized using the Dupont 9K7 substrate with 0.0009 loss tangent at 10 GHz and a dielectric constant of 7.2. The prototype CCGF PA is implemented by mounting the QPD1022 GaN device on the LTCC substrate as shown in Fig. 2.8. We used 25 thermal vias with 150 um diameter, embedded in the LTCC substrate, underneath of the surface mount packaged transistor to properly sink the heat generated at different power levels.

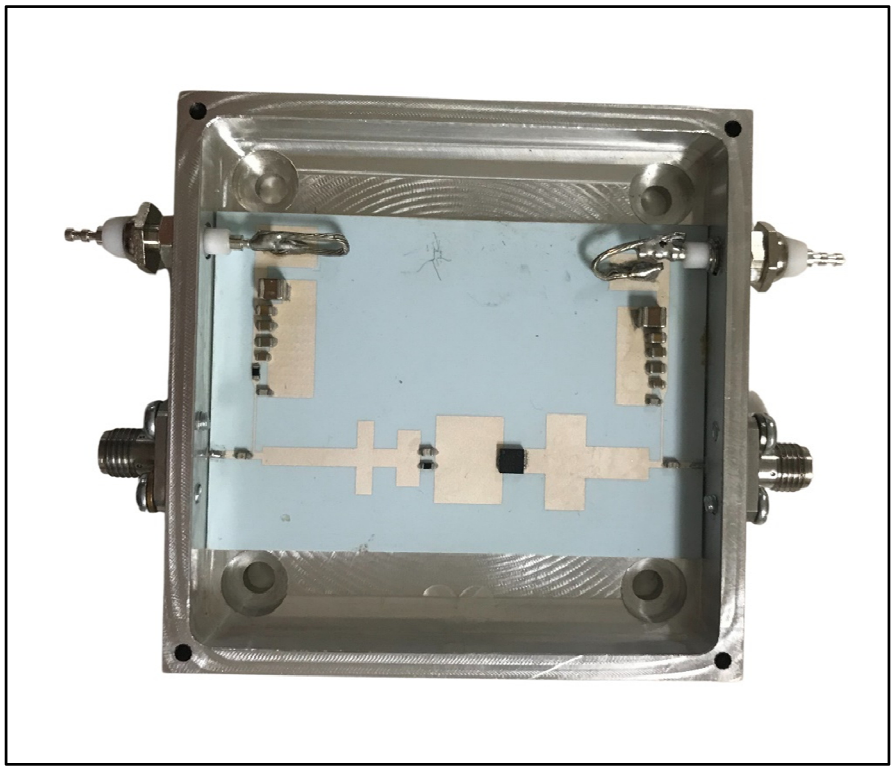

Figure 2.8 Prototype of wideband CCGF in LTCC technology

The power characteristics of the PA are measured with driving continuous wave (CW) and modulated signals while it is biased in deep class AB at quiescent drain current of I_{DS}= 8 mA and 32 V drain voltage. The measured results are shown in Fig. 6 in comparison with the simulated result. The 3dB saturated output power varies from 39.5 dBm to 40.2 dBm with large signal gain of 16.9 ± 0.4 dB and drain efficiency of 66 ± 2 % from 3.3 GHz to 4.3 GHz frequency. The measured results for the proposed CCGF design are compared to the recent published works in continues mode PAs in Table I and shows the best flatness in the PA's characteristics over the considered bandwidth.

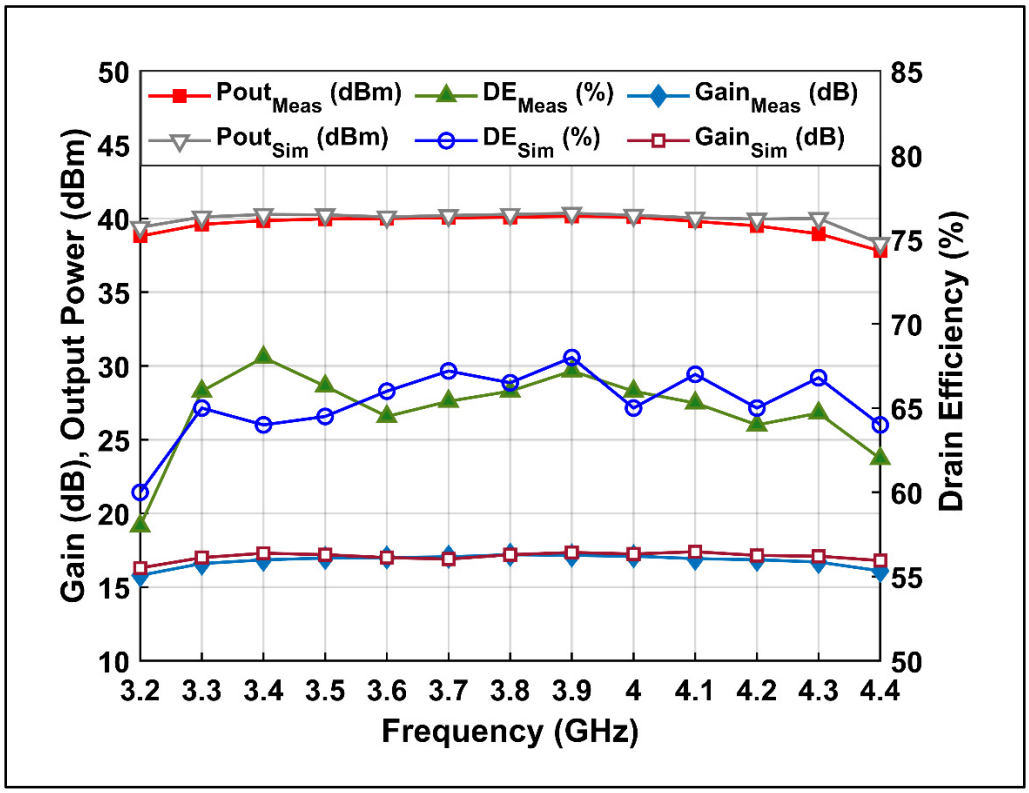

Figure 2.9 Measured and simulated power performance of the CCGF PA at 3-dB gain compression from 3.2 GHz to 4.4 GHz

In order to assess the linearity performance in the fabricated CCGF PA, we measured the ACPR under a modulated signal excitation and without applying any linearization techniques. Here, we utilized a standard 20 MHz LTE OFDM signal with 7.5 dB peak-to-average power ratio (PAPR) and a sampling rate of 96.5 MHz. The measured results are plotted in Fig. 2.10

at four carrier frequencies over the operational bandwidth. Where, the ACPR performance is better than 24 dBc all the way up to 33 dBm of output power, i.e., about 7-8 dB back-off. Consequently, this technique does not degrade the linearity performance of the PA and the desired results can be achieved in practice, using standard DPD techniques.

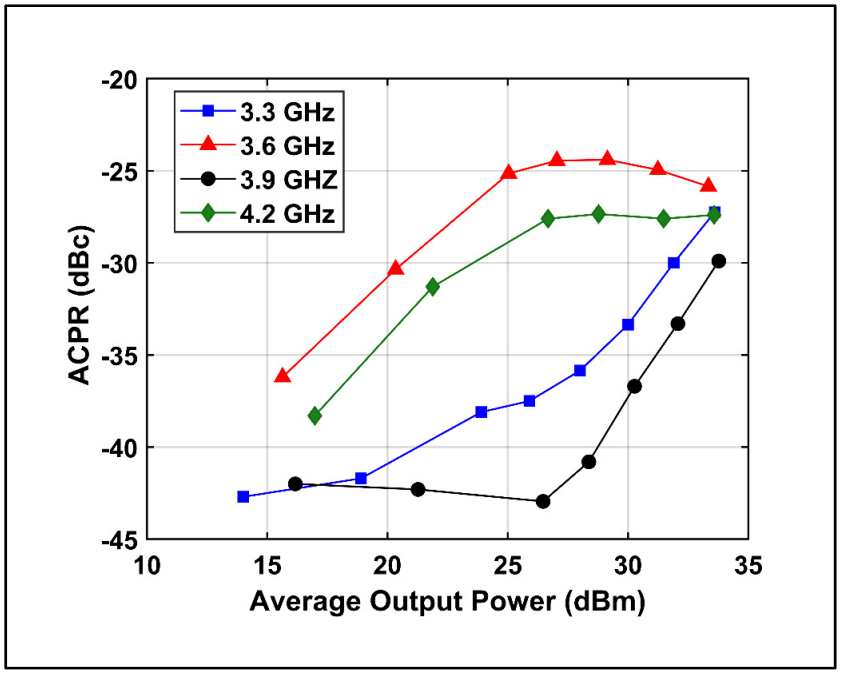

Figure 2.10 The measured ACPR characteristic of the designed CCGF PA under 20 MHz standard LTE signal with 7.5 dB PAPR at four carrier frequencies within the bandwidth

Table 2.1 Comparison with recently reported wideband PAs

Ref.	F (GHz)	Pout (dBm)	Gain (dB)	DE (%)	Class
[16]	2.4 – 3.9	40.5 ± 0.9	11.6 ± 0.9	69 ± 6	CCF^{-1}
[11]	1.2 – 3.6	41.1 ± 1.1	11.5 ± 1	66 ± 6	CCF
[12]	0.5 – 2.3	40.2 ± 1	18.5 ± 6.8	70 ± 10	CCF
[13]	3.05 - 3.85	40.6 ± 0.7	11.7 ± 0.7	74 ± 4	$CCGF^{-1}$
This work	3.3 - 4.3	39.9 ± 0.4	16.9 ± 0.4	66 ± 2	CCGF

2.5 Conclusion

In this paper a comprehensive analysis of continuous mode class GF (CCGF) PA has been presented based on tuning the second source harmonic and its effects on the drain current waveforms in broadband performance. It was shown that, the drain current waveforms can be modified by controlling the input nonlinearity to reduce their overlap with the drain voltage waveforms in continuous mode. This led to keeping the power performance above a desired level over the entire bandwidth and preventing from sever degradation at the frequency response. As a proof of concept, a CCGF PA was designed and fabricated with flat frequency response of its power characteristics between 3.3 GHz and 4.3 GHz. The measurement results show an output power of 40 dBm, a large signal gain of 17 dB and a drain efficient of 66%. The gain and output power flatness was within ±0.4 dB while drain efficiency variation was within ±2%.

CHAPTER 3

THERMAL MANAGEMENT IMPROVEMENT IN HYBRID HIGH POWER GaN AMPLIFIERS WITH COPPER-GRAPHITE INTERPOSERS

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Abstract

A practical solution is proposed to develop thermal management in hybrid high power amplifiers (HPAs) with multilayer substrates. The feasibility of using conductive interposers in implementation of hybrid HPAs has been investigated based on the thermal expansion coefficients of the interposers between the chips and ground base. Thermal management of the proposed structure is analysed based on the finite elements of the physical model in Ansys Icepak, using a C-band 40 W hybrid HPA. The HPA is designed and fabricated with combining 16 commercially available Gallium Nitride (GaN) transistors and the matching networks are implemented by the low temperature co-fired ceramic (LTCC) technology. The simulation and measurement results for thermal performance of the hybrid HPA are compared to a C-band 40 W MMIC HPA, which used electrically conductive adhesives as the interposer. Thermal images from the surface of HPAs show 10-15 °C better thermal management at the hybrid HPA compared to the MMIC HPA at the same saturated output power level.

Introduction

The power-hungry transceivers in novel wireless systems have been facing important thermal issues mainly due to the heat generated by the power lost in radio frequency power amplifiers (RFPAs) within a small space (Quesnel *et al.*, 2021). The higher the power rating of the RFPA, the more heat is generated resulting in a more significant impact on performance and a challenging thermal management problem. Indeed, high power dissipation can raise the chip's temperature and lead to signal distortion, degraded RFPA performance (Florian *et al.*, 2013; Cappello *et al.*, 2018; Florian *et al.*, 2018) and even reduced mechanical integrity (Gonda *et al.*, 2004; Liu *et al.*, 2015). The signal distortion due to such thermal issues can be quantified using a multistage thermal-resistor thermal-capacitor (R_{th} C_{th}) ladder circuit as an equivalent thermal circuit (Florian *et al.*, 2013). Therefore, it is important to efficiently evacuate the heat away from the RFPA's transistor chips towards heat skinning structures so that the chips' temperature is maintained below a recommended values for safe and prolonged operation.

In the literature (Mazeau *et al.*, 2007; Lu *et al.*, 2017; Sodan *et al.*, 2018; Tadjer *et al.*, 2019; Chatterjee *et al.*, 2019; Al-Saman *et al.*, 2020; Shoemaker *et al.*, 2021). the thermal management has been performed mainly at the devices' semiconductor level such as spacing the device fingers, reducing size of gate fingers and using semiconductors with high thermal conductivity at the GaN substrate layers to improve the power dissipation. Additionally, it is shown that the most sensitive region of the field-effect transistors that can be affected by thermal issues is the gate contact, especially when they are based on silicon (Si) which has a low thermal conductivity (Temcamani *et al.*, 2016). However, by replacing the Si substrate layer with the silicon carbide (SiC) (Moore *et al.*, 2015; Bagnall *et al.*, 2018) or polycrystalline synthetic diamond (Chu *et al.*, 2013; Chu *et al.*, 2015, Cheng *et al.*, 2020) the heat evacuation in GaN devices has been improved for high-performance RF applications. In (Yu *et al.*, 2015; Yu *et al.*, 2017) the thermal management for GaN transistors was investigated in wafer-level packaging (WLP). The measurement results showed that, using ceramic substrates in WLPs achieved better thermal performance and reduced parasitic inductances in GaN devices compared to the printed circuit boards (PCBs).

Beyond the device's semiconductor level, thermal management has also been investigated at the circuit and mechanical assembly levels (Chiriac *et al.*, 2004; Ziabari *et al.*, 2012; Kearney *et al.*, 2016; Buttay *et al.*, 2018; Caillaud *et al.*, 2020; Jagt *et al.*, 1998; Lewis *et al.*, 2008; Mach *et al.*, 2019; Inoue *et al.*, 2009; Inoue *et al.*, 2011; Liao *et al.*, 2012; Fu *et al.*, 2003; Inoue *et al.*, 2008; Yu *et al.*, 2019; Li *et al.*, 2004; Moller *et al.*, 2015). For HPAs in particular, two alternative options are typically considered. One option is to integrate a single HPA chip, where matching and power combining are carried out on-chip, in the mechanical housing while the second is to employ a hybrid design approach where lower-power chips are matched and combined off-chip using multilayer PCBs and custom housings. While using the single chip approach yields overall smaller HPAs, it can lead to the accumulation of heat generation within a small area which poses significant challenges for thermal management. Alternatively, using a hybrid design approach benefits from larger spacing which can be leveraged to reduce the heat density underneath the lower-power chips. However, the proposed solutions to improve the thermal management in hybrid design (Chiriac *et al.*, 2004; Ziabari *et al.*, 2012; Kearney *et al.*, 2016; Buttay *et al.*, 2018; Caillaud *et al.*, 2020) have been inefficient in practice. This is due to the low thermal conductivity of substrates used, such as FR-4, CEM-1, G-10, Alumina, etc. Attempts to address these issues include reducing the thermal resistivity through embedding thermal vias (Ziabari *et al.*, 2012), reducing the thickness of low conductivity substrates underneath of the amplifiers' chips or making cavities for mounting chips directly on the circuit ground (Kearney *et al.*, 2016; Caillaud *et al.*, 2020). Electrically conductive adhesives (ECAs) have been used for mounting the transistors to the board or the carrier (Jagt *et al.*, 1998; Lewis *et al.*, 2008; Mach *et al.*, 2019; Inoue *et al.*, 2009; Inoue *et al.*, 2011; Liao *et al.*, 2012). However, such the various solutions and materials are not optimal in that they have relatively low thermal conductivity and their thermal expansion coefficients do not match well those of the transistors resulting in performance degradation with time (Inoue *et al.*, 2009; Inoue *et al.*, 2011; Liao *et al.*, 2012; Fu *et al.*, 2003; Inoue *et al.*, 2008; Yu *et al.*, 2019; Li *et al.*, 2004; Moller *et al.*, 2015).

In this paper, we explore practical solutions that can address the above-mentioned issues. This is done through a comparative study of two proposed thermal management solutions for a 40W

C-band HPA realized with (i) a single chip design mounted with ECA on copper base and (ii) a hybrid design in multilayer LTCC (Low Temperature Cofired Ceramics) technology using 4 power bars mounted on the copper base through copper-graphite interposers. Both designs use the same commercially available GaN MMIC process and produce the same output power. Physics-based finite-element analysis as well thermal imaging are used for validation of the proposed solutions and the relative performance. The remainder of this paper is organized as follows. In section II, we describe the hybrid HPA design steps and section III presents the results of thermal simulation for the HPAs. In section IV, the fabrication process for the prototype HPA along with the results of power performance and thermal measurements are reported.

3.1 HPA Circuit Design and Simulation

3.1.1 UMS GaN Device

The commercially available GH25NHF_10 GaN transistor is provided by the United Monolithic Semiconductors (UMS) Company. In this paper, we used the GH25-10 nonlinear hot-FET model to design and simulation the HPA in the Keysight Advanced Design System (ADS) software. To generate the required output power at the C band frequency we selected the transistor topology with 8 fingers and 125 μm gate width (8 × 125 μm). The breakdown voltage is more than 100 V and transition frequency (f_t) is 25 GHz. The typical performance of the transistor is shown in Table 1 at V_{ds} = 30 V and I_{ds} = 100 mA/mm.

Table 3.1 Typical performance of GH25NHF_10 GaN with 8 × 125 μm gate periphery.

Maximum output power operation at F = 9 GHz	
Pout at 6 dB of compression	4.4 W/mm
Gain at low level	15 dB
Peak power added efficiency (Pout-Pin) / Pdc	42 %

3.1.2 Power-bar MMIC

Each power-bar includes three cells, and each cell is made by combining of two transistors on the MMIC chip. Fig. 3.1 shows the power-bar chip and the load-pull test with the second harmonics tuned. At 5.4 GHz, when each transistor is biased in deep class AB at 13 mA and V_{ds} = 28 V, the phase of second harmonic impedances are swept at the input and output of each cell to select the optimum point. As shown in Figs. 3.1 (b) and (c), the output power and PAE are almost constant for sweeping the second harmonics on the edge of Smith chart except from 150° to 270°. It should be note that, sweeping the second harmonic impedances start at the open-circuit point from 0 to 360° in counter clockwise direction. It can be seen that, the power characteristics are constant when the second harmonics at the input and output of each cell are terminated around the open-circuit point. At this condition, by terminating the fundamental load impedance at Z_{Lopt}= 9+j*2, about 38 dBm saturated output power can be achieved at 2-dB compression gain with 48% PAE.

In order to design a HPA with 40 W output power and above 40% PAE performance, we need to combine 8 cells through 3 stages of combiners. Based on the load-pull results, to achieve this goal the total power loss through the output passive circuit including the matching networks and combiners must be less than 1 dB.

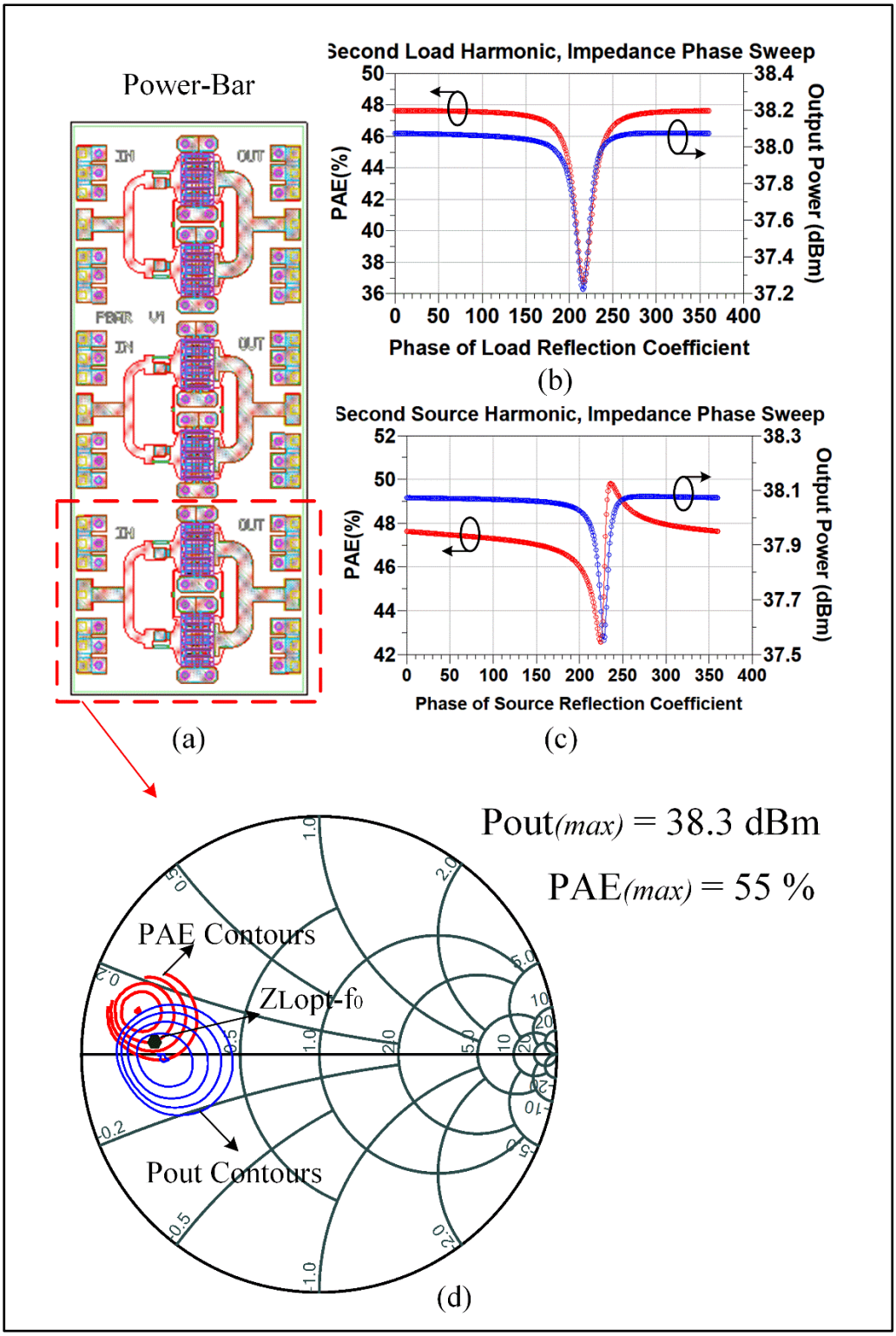


Figure 3.1 (a) UMS Power-Bar MMIC; including 3 cells and 6 transistors, (b) Impedance phase sweep for the second load harmonic, (c) Impedance phase sweep for the second source harmonic, (d) Fundamental load-pull test for one cell

3.1.3 Design of Matching Networks and Combiners in HPA

One of the critical challenges in this design is combining the 8 cells with considering the high power dissipated through each of them. Based on the design aspect and load-pull test, about 6 W can be dissipated in each cell when it works at its saturated output power. Hence, there should be enough space in combining the cells and mounting the power-bars to be able transform the generated heat through the heatsink system. To address this issue, we used two cells in each power-bars to be combined through 3-stage combining networks. This also provides more physical space for using stubs and transmission lines in matching networks. However, there is not enough space for tuning the fundamental and second harmonics just before the first combined stage. Therefore, the input and output matching networks are distributed in the first and second combined stages.

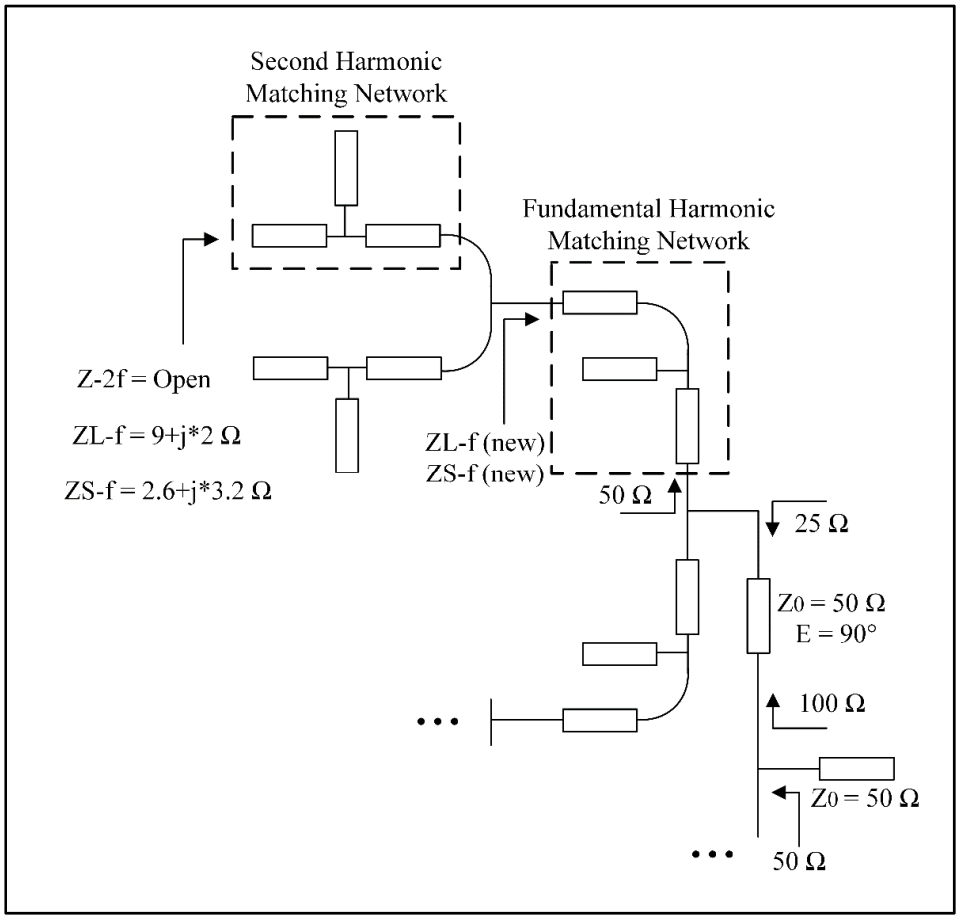


Figure 3.2 Circuit diagram of passive networks in designed HPA

The circuit diagram of the designed passive networks is shown in Fig. 3.2. The input and output matching networks at the first stage are designed using a transmission line along with open stub to block the second harmonics at the input and output ports of each cell. The second stage combiners at the input and output are designed to transform the new optimum fundamental impedances seen after the first stage combiner to 50 Ω impedance. At the last stage, each branch of the combiner includes a quarter wave transformation line with 50 Ω characteristic impedance to transform the 25 Ω impedance, seen from combining two 50 Ωs at the second stage, to 100 Ω.

3.1.4 Full HPA Simulation Result

The designed matching networks and combiners for the HPA were described in section C based on the ideal microstrip lines in schematic environment. In order to evaluate the precise performance of the passive circuits and calculate the impedance transformation loss under electromagnetic effects, the circuits were transformed to the layout environment of ADS software based on real line characteristics. To do this, we used the low loss Ferro A6M substrate with a dielectric constant of 5.7 and a loss tangent of 0.001 at 10 GHz. In order to reduce the passive circuit size, a 10-mil thickness was used as the main dielectric substrate. Such a thin and fragile thickness was mounted on 30 mil dummy substrate layers to maintain the physical strength of the passive circuit.

Fig. 3.3 shows layout of the full HPA including the matching networks, combiners and DC bias circuits, which are tuned for the optimum power performance. It is important to note that circuit design in LTCC technology provides this feature to use multiple thickness of layers proper with the required line widths at each part of circuits. Hence, the DC bias circuits are designed with 40 mil substrate thickness to provide the required width of line for passing the high DC drain current through the quarter-wave impedance transformer line. In addition, by increasing the substrate thickness, characteristics impedance increases for the desired line width and provides high impedance at the DC bias connection point to block the RF signal.

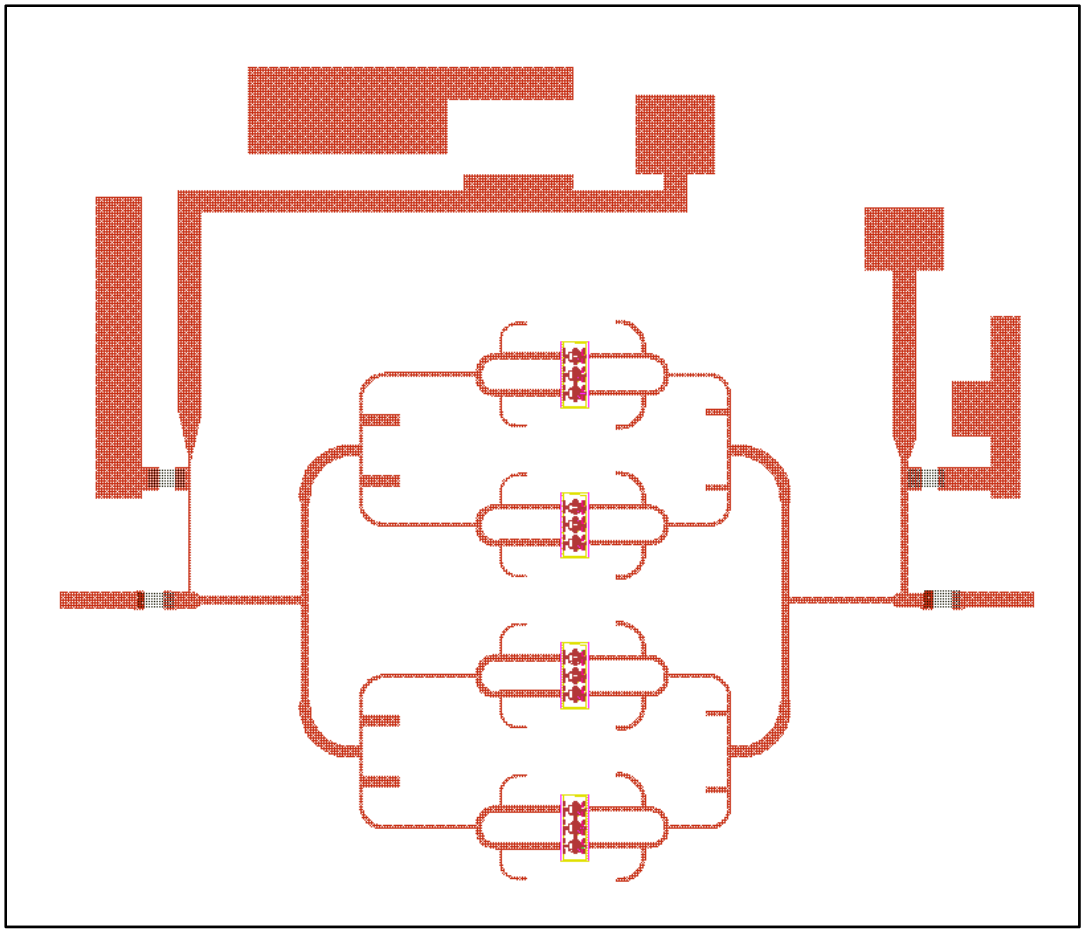


Figure 3.3 Layout of circuit designed on LTCC technology for the HPA

The trajectory of load and source impedances at the fundamental and second harmonics along with the passive circuit loss are shown in Fig. 3.4. It can be seen that, the matching network trajectories are passing from the optimum load and source impedances were described earlier in Fig. 3.1. In addition, Fig. 3.4 (a) depicts the input and output S-parameters of the full HPA from 5.2 GHz to 5.6 GHz that shows how the HPA is matched with the 50 Ω load when the cells are terminated with the optimum impedances. The power loss at the input and output passive circuits are shown in Fig.3.4 (b) at the frequency band. The output power loss is obtained about 0.5 dB at 5.4 GHz which leads to achieve the required output power expected at this design. It should be noted that, the higher loss at the input passive circuit in comparison with the output passive circuit is due to the higher impedance rate of matching the optimum fundamental source impedance to the 50 Ω.

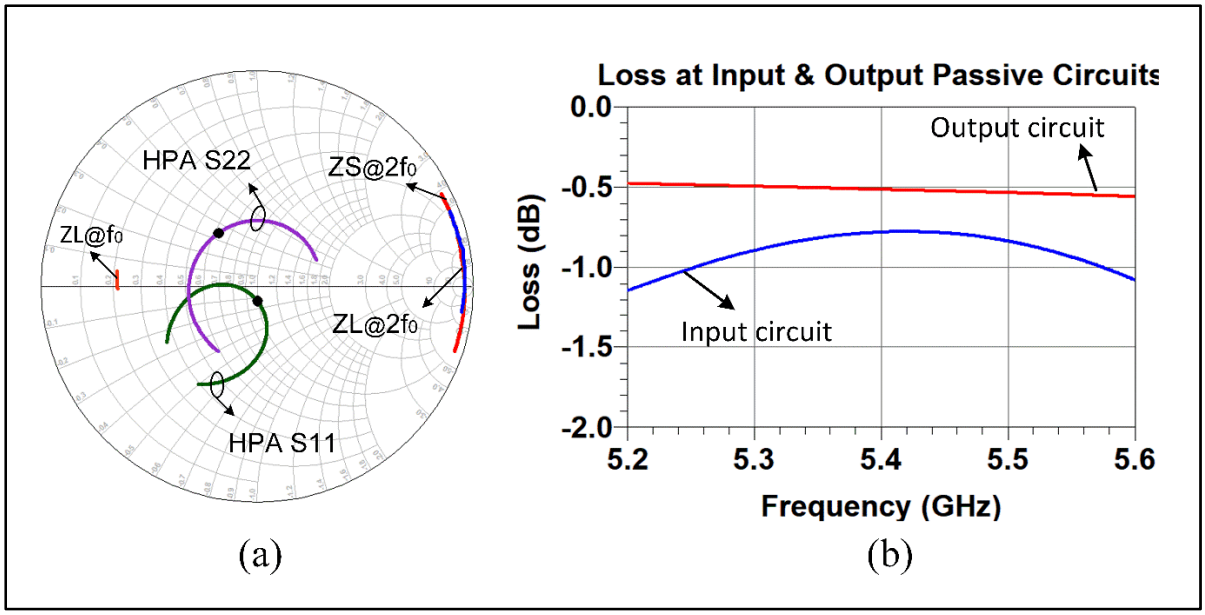


Figure 3.4 (a) The load and source trajectories of each cell along with S_{11} and S_{22} parameters of HPA; ZL@f_0: fundamental load impedance, ZL@$2f_0$: second harmonic load impedance, ZS@$2f_0$: second harmonic source impedance. (b) Loss at the input and output passive circuits

Fig. 3.5 illustrates the power performance of each cell and the full HPA versus input power at 5.4 GHz. It can be seen that, the cells have similar power characteristics that shows the matching networks and combiners are designed symmetrically. For each cell, about 38 dBm saturated output power obtained at 2-dB compression gain with 47% PAE. Considering the passive circuit loss, this provides about 46.5 dBm saturated power at the output of the HPA with 43% PAE at 2-dB compression gain.

The frequency response of output power and PAE for the designed HPA are shown in Fig. 3.6. It can be seen that the 2-dB output power above 40 W with PAE between 40 – 44 % are achieved from 5.28 GHz to 5.58 GHz.

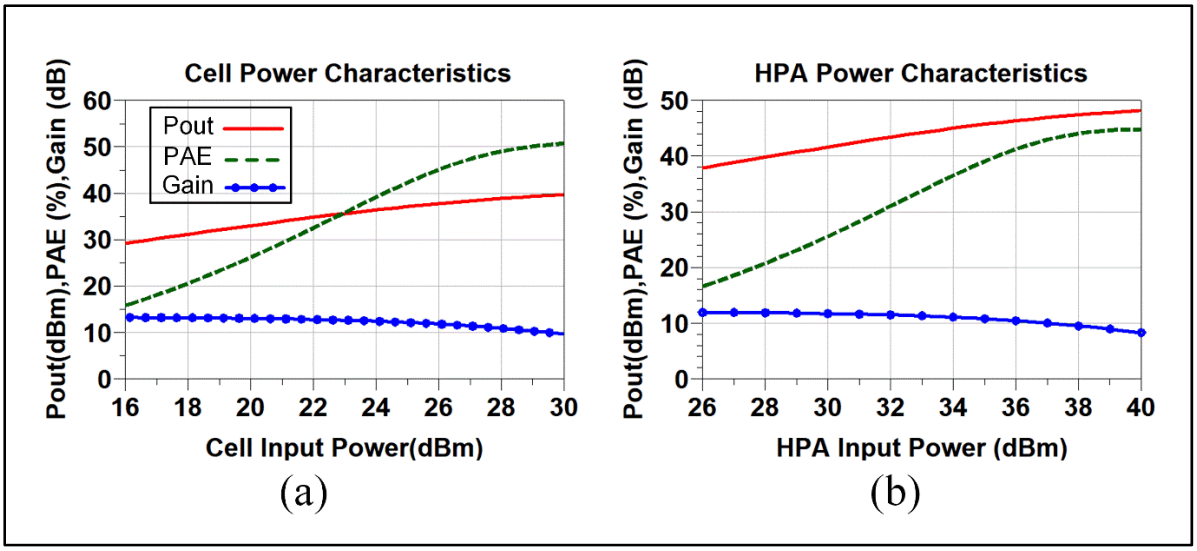


Figure 3.5 Power characteristics: (a) for each cell (b) for HPA

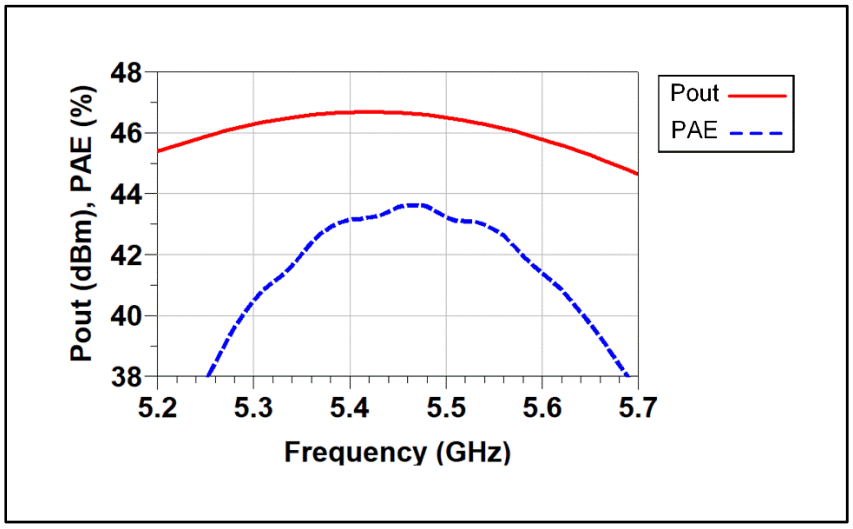


Figure 3.6 Frequency response of Output power and PAE of HPA

3.2 Thermal Management in Designed HPA

In this section, we describe the coolant system to immediately transfer the heat generated underneath of each power bars in the designed HPA. According to the power characteristics of the design HPA in section II, the power dissipated through each cell can be computed as 6 W considering a drain efficiency of 45% and 5 W saturated output power. Therefore, the cooling

system must be able to handle the heat sources up to 48 W RF power loss which can be dissipated at 3-dB output power of the HPA. Hence, the power bars were soldered on a high thermal conductivity copper base connected to an aluminum heatsink and fan to provide the forced-air cooling condition.

The main challenge in design of such a coolant system is choosing the appropriate interfaces to make feasible soldering of the power bar chip on the copper base. This interface must have: (i) high thermal conductivity to immediately transfer the heat flow and (ii) a suitable thermal expansion proper with the upper and lower layers to avoid cracking the chip in soldering process. For example, the linear thermal expansion coefficient (α) of GaN chip with SiC substrate is about 2.77 µm/m°C whereas this characteristic for the copper base is 16-16.7 µm/m°C. The considerable difference can lead to crack the die chip while cooling down after soldering. In order to address this issue, we used the copper-graphite interposer with a thermal expansion coefficient close to the GaN die (4-8 µm/m°C), and thermal conductivity of 360-400 W/mK.

To evaluate the quality of heat transition through the suggested structure its performance was evaluated under transient thermal analysis in Icepack environment of Ansys Electronics Desktop 2021 software in comparison with MMIC HPA designed in iRadio Lab at the University of Calgary. Where, the die attach adhesive ATROX 800HT2V with a thermal conductivity of 130 W/mK was used for mounting the chip on the copper base. The layout of HPA is shown in Fig. 3.7 which is designed with combining of 16 UMS GaN devices (8 cells) and provides 40 W output power with 40 % PAE in simulation results.

To provide a valid condition for comparing the heat transition and considering the matching network loss in the MMIC HPA design, it is supposed that 3W RF power is dissipated through each transistor in generating 2.5 W output power with 45% drain efficiency. This means up to 48 W RF power is dissipated through the power bar shown in Fig. 3.7. Also, the same heatsink and fan are used for cooling the system.

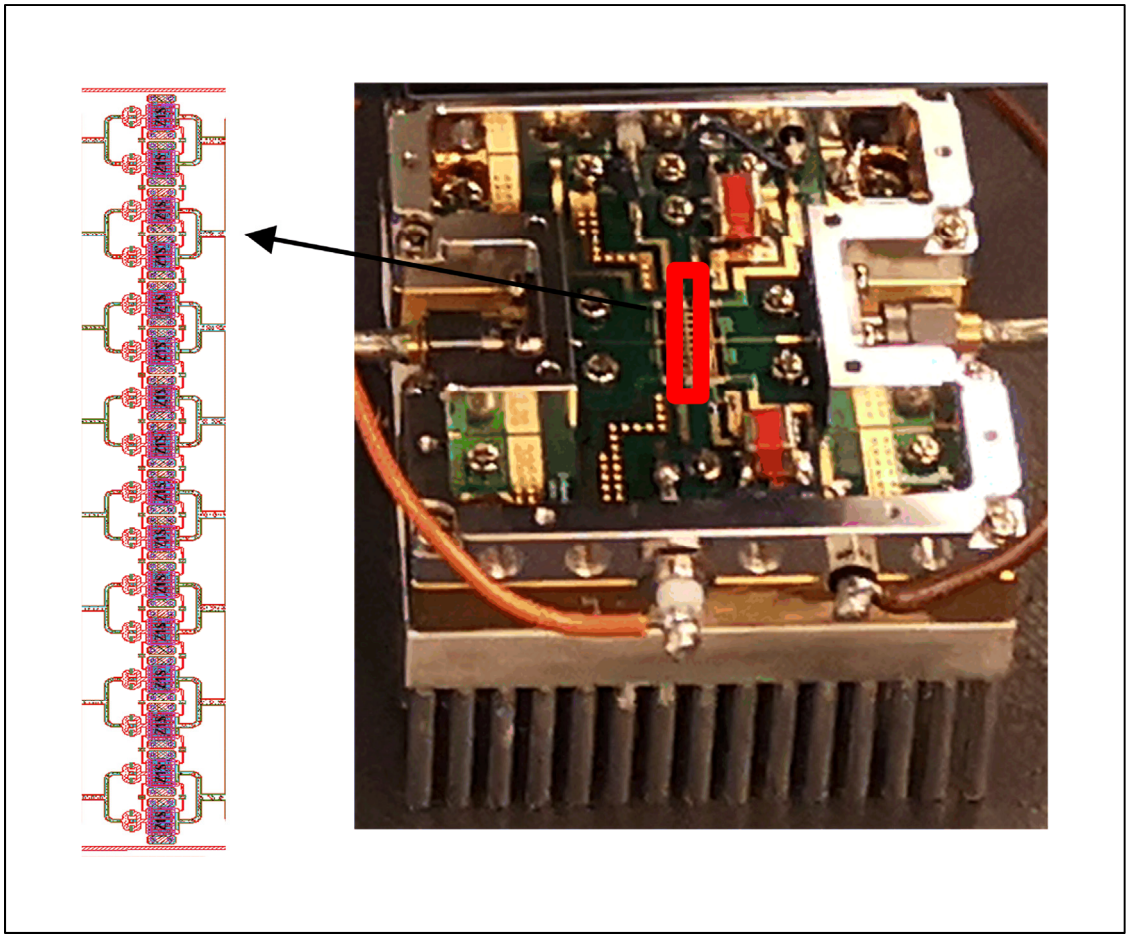


Figure 3.7 MMIC HPA designed in iRadio lab, using 16 UMS GaN devices

The thermal simulation results for the hybrid LTCC HPA and MMIC HPA are shown in Fig. 3.8. It can be seen that, when the power bars are mounted on the copper-graphite interposer in hybrid HPA, the maximum temperature under neath of each power bar reaches to 54 °C and immediately transfer to the copper base which is cooled down by the heat snick and fan (Fig. 3.8 (a)). This is about 9 °C lower than the obtained temperature in the MMIC HPA in simulation results which was mounted on copper base directly, using the die attach adhesive (Fig. 3.8 (b)). Therefore, it is expected to achieve a lower temperature at the gate channel of device in measurement results. This makes the HPA more reliable under CW signal operation and maintain the mechanical strength by working in lower temperature.

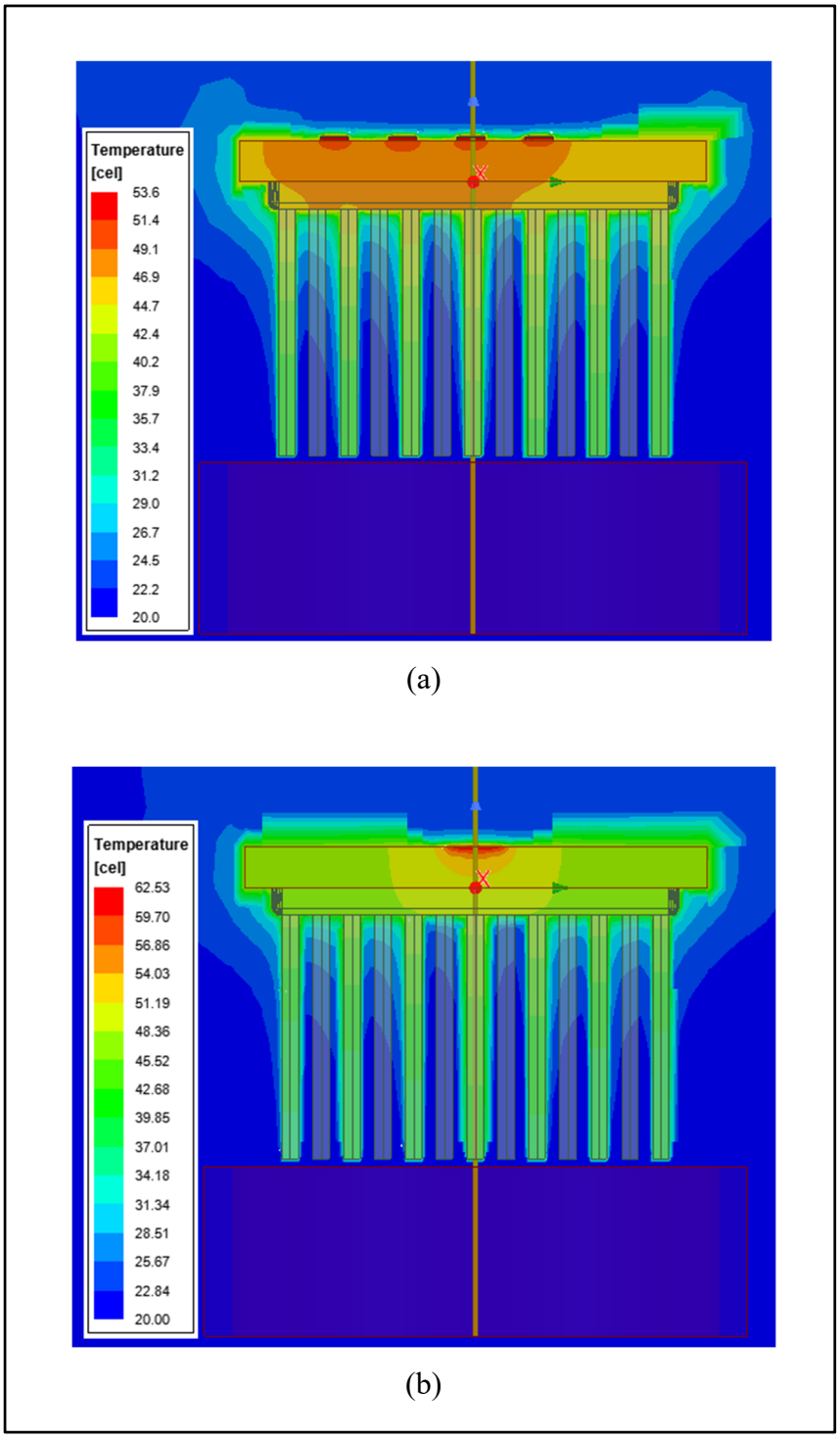


Figure 3.8 Transient thermal analysis in Icepack environment of Ansys Electronics Desktop 2021. (a) 40W Hybrid HPA LTCC mounted on copper-graphite interposer (b) 40W MMIC HPA mounted on copper base using die attach adhesive.

3.3 C-band HPA Implementation and Measurement Result

The HPA circuit described in section II was fabricated and assembled at the in-house LTCC laboratory. The passive circuits were implemented by the low-loss Ferro A6M substrate and silver paste metal in LTCC technology. In this section we describe the steps of assembling the HPA in mounting the power bars on the copper-graphite interposer and soldering them on the copper base. In addition, the measured RF power characteristics and thermal test results of the prototype HPA are illustrated. under continuous wave (CW) signal.

3.3.1 Assembling the HPA

To assemble the HPA we used different solder pastes proper to the passive circuits, power bars, copper-graphite, capacitors and resistor through several steps. Considering the different temperature melt points of the solder pastes the mounting process were done in sequence as following:

1- **Soldering Power-bar on Copper-graphite Interposer**: The power-bars were soldered individually on copper-graphite interposers using gold-tin (80Au20Sn) eutectic solder sheet with 1 mil thick at 280 °C. This was done with the Finetech Pico MA hot air welding/pick and place machine with the 1mm diameter metal tip as depicted in Fig. 3.9 (a). The AuSn preform is picked and dropped by the vacuum tip over the copper-graphite interposer, which is placed on the heating plate, as shown in Fig. 3.9 (b). Using the heating plate x/y Vernier and the rail camera, that shows around the part, this can be precisely aligned to the copper-graphite interposer. Similarly, the GaN die is picked and mounted on top of the gold-tin solder sheet. Then the heating plate should be raised until it touches the AuSn preform.

The soldering process was completed based on the heat pattern for the heating plate as shown in Fig. 3.10 (a) and simultaneously projecting hot air around the vacuum tip, that holds the GaN die, as shown on Fig. 3.10 (b). Melting the solder paste moves down the chip and reduces the vacuum tip pressure on top. It may help to gently tap the heating plate to create vibrations and make sure that the solder sticks well everywhere. Fig. 3.10 (c) shows the GaN die soldered

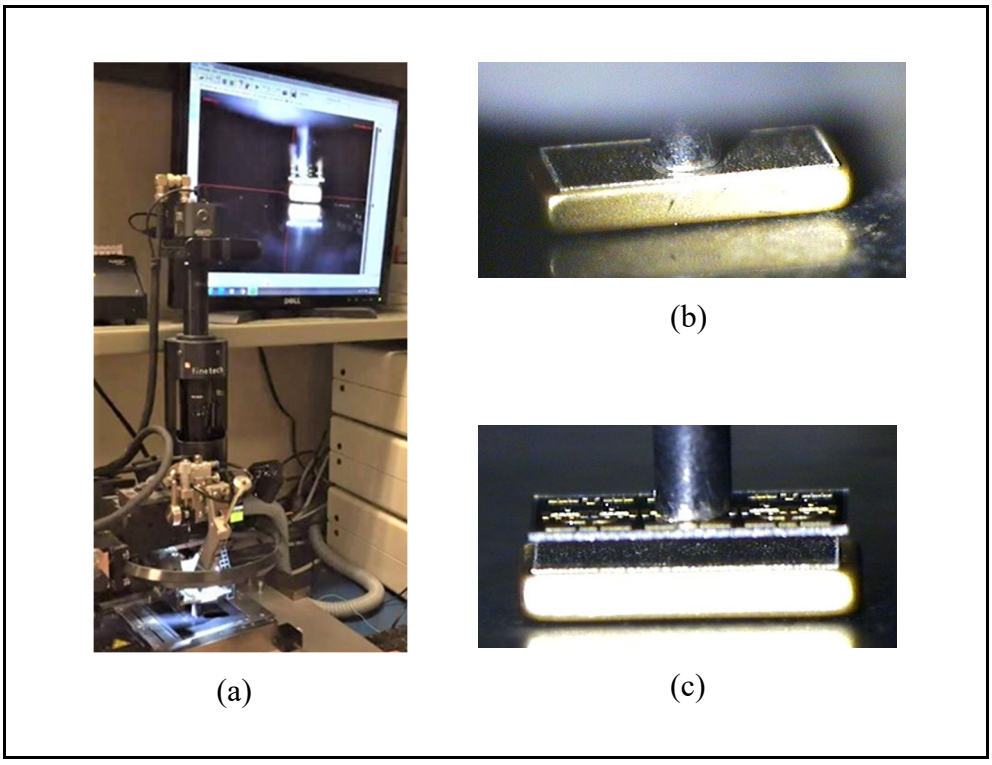


Figure 3.9 (a) Finetech Pico MA hot air welding/pick and place machine. (b) Mounting gold thin on copper-graphite (c) Mounting power bar on copper-graphite

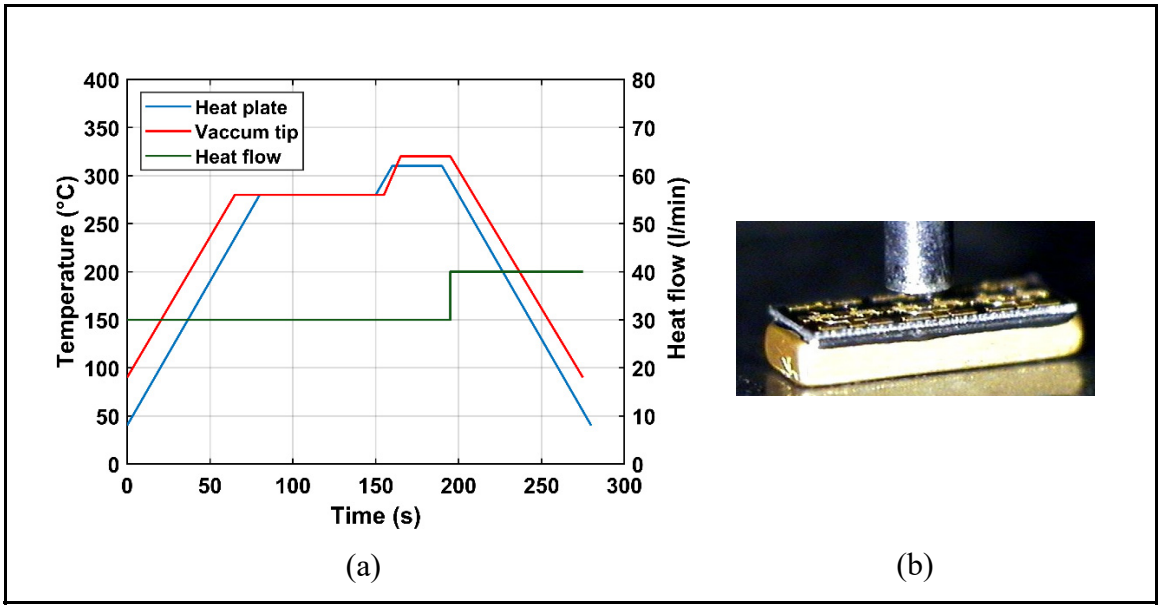


Figure 3.10 The heat patterns for soldering power-bar on copper graphite interposer: (a) for heat plate (b) for vacuum tip, (c) GaN die soldered on the copper-graphite interposer with melted AuSn

on the copper-graphite interposer with melted AuSn.

The GaN die soldered on the copper-graphite interposer was inspected through Xray imaging system as shown in Fig. 3.11. In Fig. 3.11(b) it is visible that a solder bubble (the big black structure) formed after heating on the bottom right of the die. This usually happens due to large solder perform and can be removed by laser machine.

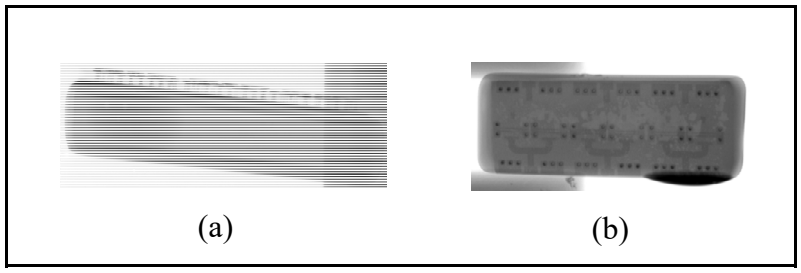
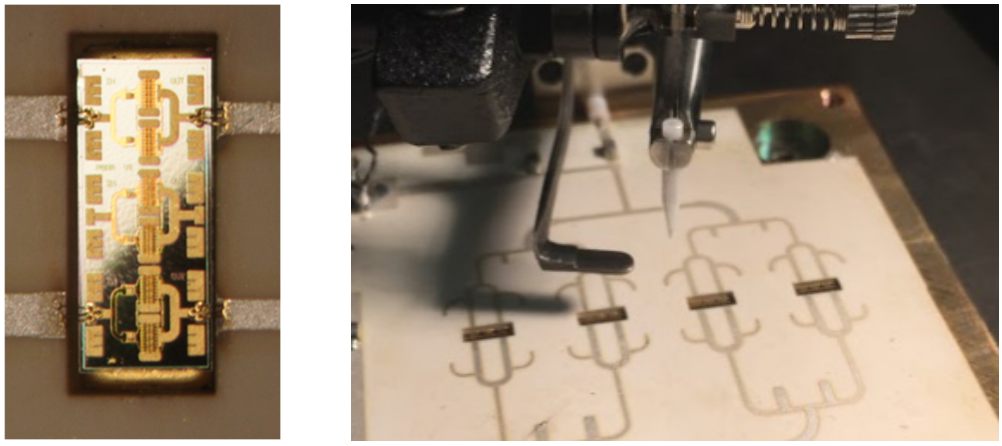


Figure 3.11 Xray image of the GaN die soldered on the copper-graphite interposer

2- **Soldering the Passsive Components:** The capacitors, resistors, DC bias and SMA connectors were soldered on the LTCC PCB using Chip-quick SMD291 AX250T5 solder paste that melt at 183 °C. It is important to note that, the thermal expansion of the LTCC is different with the copper base. Therefore, to avid breaking the LTCC substrated during the soldering process we used silver epoxy paste to fix the LTCC on the copper base within the aluminum wall.

3-**Mounting the Chip on Copper-graphite in LTCC Cavities:** In this step, we used Chip-quick SMDLTLFP250T4 solder paste which melts at 138 °C; with a lower melting point temperature than the other solder pastes were used in this prototype. It is important to note that adding too much solder paste may lead to short circuit the GaN die due to rise the paste around the copper-graphite interposer. Furthermore, to perform bounding wires with same length and shape that was supposed in simulation step, the GaN die top should be close to the same height as the top of the LTCC. Hence, the amount of the solder paste must be choosing to meet these requirements. The bounding wires in this project were done by K&S 4522 gold ball wire bonder to connect the GaN die to input/output matching networks on the LTCC. In order to support the high-power performance and high current density at each branch of the HPA we

used three bounding wires at each cell of the power-bars. This helps to reduce the parasitic effects and RF loss as predicted in simulation results. A power-bar including two cells wire bounded to the LTCC lines are shown in Fig. 3.12.

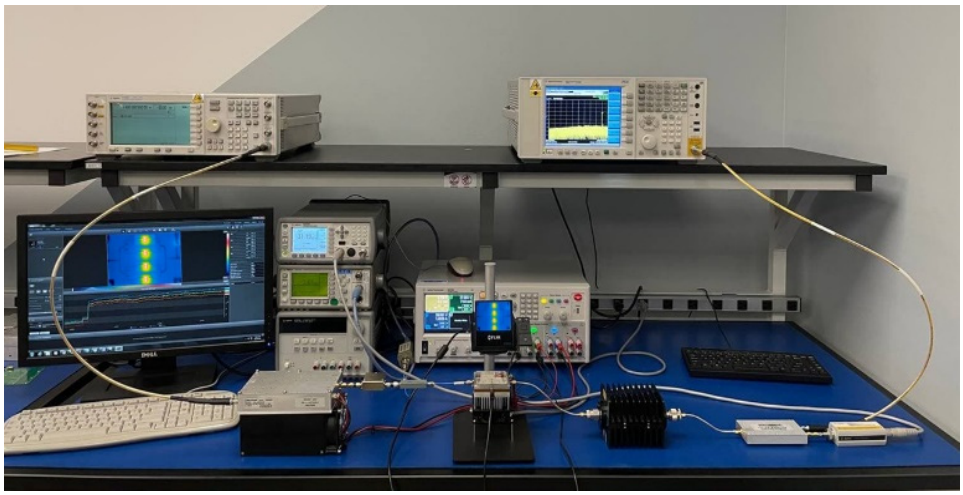


(a) (b)

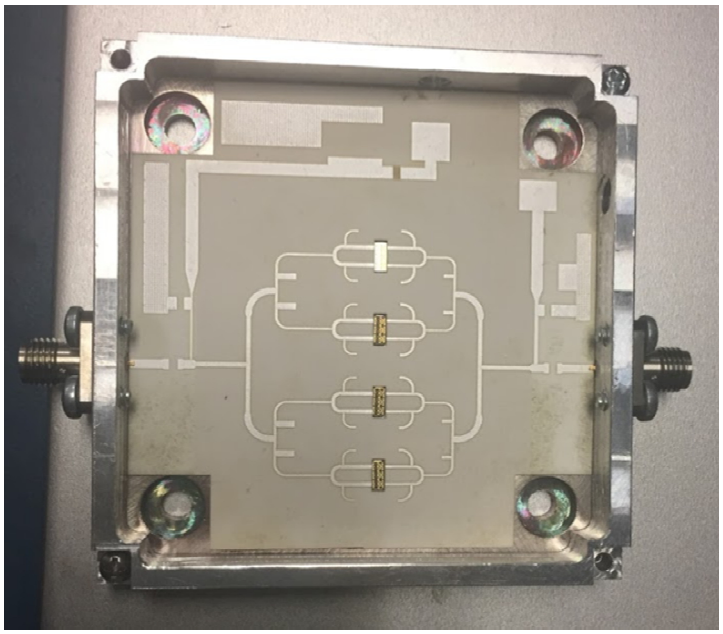
Figure 3.12 Wire bounded power-bars to the silver line on LTCC

3.3.2 Measurement

The power characteristics of the HPA were measured with driving continuous wave at the HPA input while it was biased at quiescent drain current of 20 mA and 32 V drain voltage for each transistor. The measurement setup is shown in Fig. 3.13. Amplifier ZHL-5W-63X-S+ was used to drive the HPA up to its saturated output power. To precisely measure the power performance the average input and output power of HPA were monitored by power meter and spectrum analyser at the same time. During the test, the prototype HPA was mounted on the same heat sink and fan, as their equivalent models were used in simulation setup, to cool down the power-bars at high power performance. The channel temperature of power-bars were measured by FLIR thermal camera. Due to not access to the underneath of each power-bars, directly we used thermocouple to measure the same area in the heat sink to be compared with the simulation results.



(a)



(b)

Figure 3.13 Measurement setup for CW and modulation signal tests, (b) Prototype C-band HPA

The power characteristics of the HPA are shown in Fig. 3.14 in comparison with the simulation results in section I. It can be seen that, 40 W output power was achieved at 2-dB compression point with 43% PAE which are in constant with the simulation results. At this condition the temperature of each chip was measured at the saturated output power which the thermal pictures are shown in Fig. 3.15.

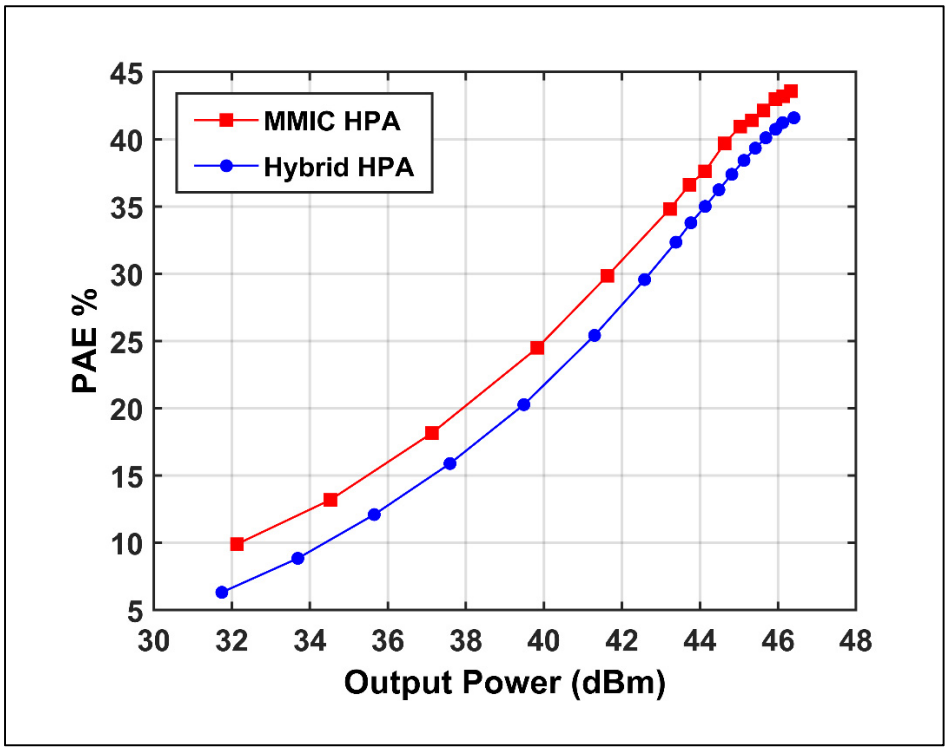


Figure 3.14 The power characteristics of the HPA

In order to evaluate the thermal management for the hybrid HPA mounted on the copper graphite in comparison with the MMIC HPA, the chip temperature was measured in 1 dB power steps which the measured results are shown in Fig. 3.16.

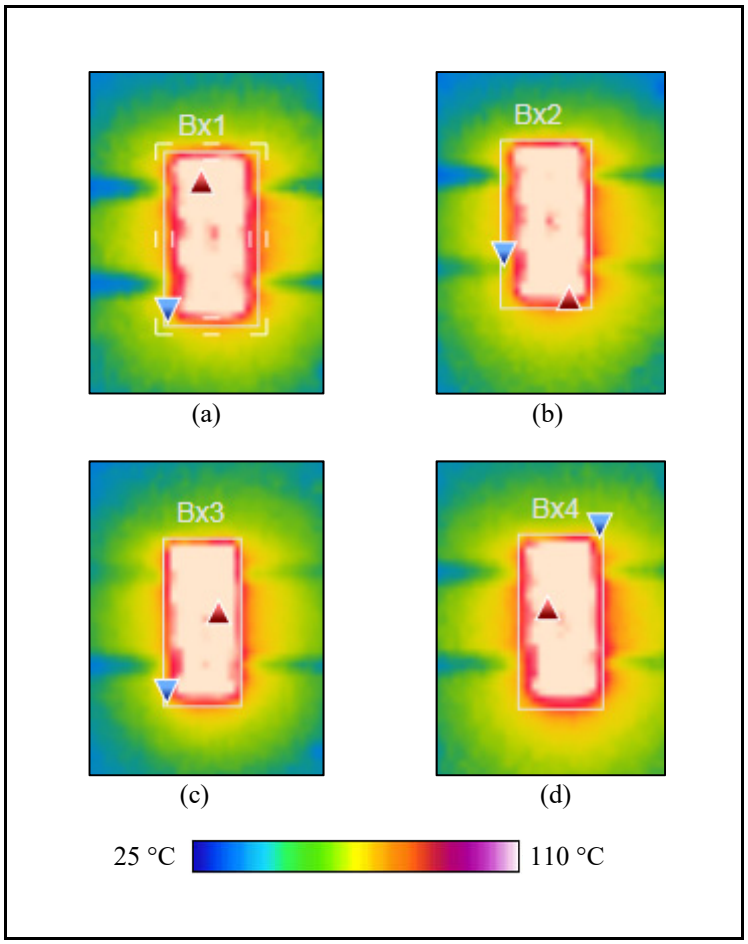


Figure 3.15 Temperature of each chip was measured at the saturated output power

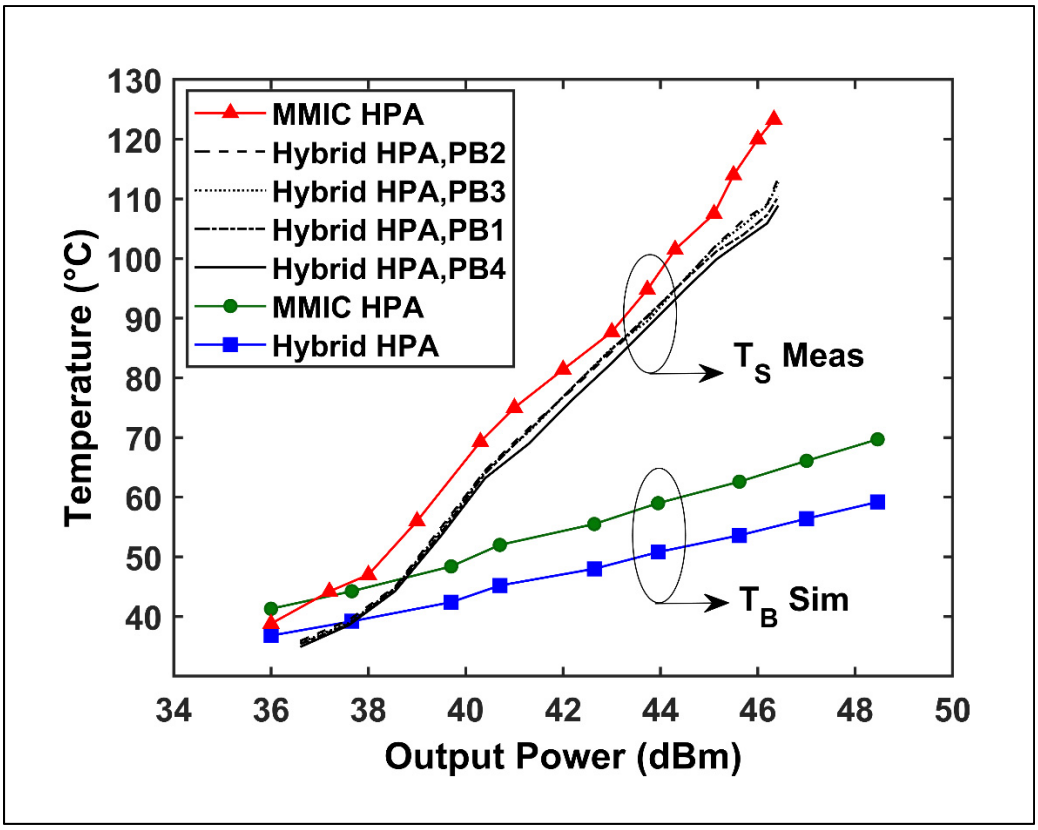


Figure 3.16 Chip temperature measured in 1 dB power steps

3.4 Conclusion

In this paper, we investigated the usage of copper-graphite as the interposers in design of HPAs. It was shown that using the high thermal conductive interposers with appropriate matched thermal expansion coefficient makes possible the soldering of high power chips directly to the coolant system and prevents from cracking the chip in soldering process. This consequently reduces the thermal impedance below of the high power chips to avoid from accumulating energy due to using ECAs and improves the thermal management. As a proof of concept, a C-band 40 W hybrid HPA was designed and fabricated, where 4 MMIC power bars are matched and combined off-chip using low-loss multilayer LTCC technology and mounted using copper-graphite interposers. In comparison with thermal performance in a C-band 40 W MMIC HPA, the simulation and measurement results for the hybrid HPA shows 10-15 °C better thermal management at the base and surface of the power chips.

CONCLUSION AND RECOMMENDATIONS

In this thesis we proposed and investigated novel solutions to improve power characteristics of PAs in wideband operation. Particularly, this thesis focused on broad band harmonic tuned power amplifiers with extended design space for terminating the load harmonics. This led to reduce the complexity of matching networks circuit design over wide frequency range and enhance the drain efficiency performance to meet the novel radio system requirements. Furthermore, a practical solution was proposed to improve thermal management in HPA using properly matched thermal interposers between the chip and copper base. The emerging gallium nitride (GaN) semiconductor technology coupled with LTCC technology were used to design, prototypes and test such novel circuits.

In the first part of thesis, a comprehensive analysis of continuous inverse class GF ($CCGF^{-1}$) was presented based on a new closed-form expression for the drain current. Unlike the conventional continuous mode class F^{-1} approach where the input second harmonic is shorted, it was shown that controlling the second source harmonic impedance contribute to: (i) improving PA efficiency and (ii) expanding the design space for the fundamental output matching impedance. With the second harmonic properly matched at the input, the output matching network design is simplified. As a result, losses are reduced at the output, leading to increased efficiency, while making it easier to achieve better flatness and bandwidth coverage. This approach was validated through the design, fabrication and measurement of a $CCGF^{-1}$ PA using a packaged 10-Watt GaN device on a LTCC substrate. The measured results show a drain efficiency of more than 70% from 3.05 GHz to 3.85GHz, a gain between 11 and 12.4 dB with a gain flatness of ± 0.7 dB and an output power at 3-dB gain compression between 39.9 and 41.4 dBm. It was also shown that the fabricated amplifier displayed an ACPR level better than 26 dBc over the entire band under a 20 MHz LTE signal having a PAPR of 10.45 dB, without any linearization.

In the second part of the thesis, we investigated the effects of controlling the input nonlinearity of the gate-source capacitance (C_{gs}) on the drain efficiency performance and design space for

terminating the load impedances in continuous mode of class GF. It was shown that, the drain current waveforms can be modified by tuning the second source harmonic to reduce their overlap with the drain voltage waveforms in continuous mode and extend the design space for the fundamental load harmonic, resistively. This can be used to maintain the power performance above a desired level over the entire bandwidth as was shown with a proof-of-concept design and fabrication of a CCGF PA that yielded a flat frequency response of its power characteristics between 3.3 GHz and 4.3 GHz. The measurement results show an output power of 40 dBm, a large signal gain of 17 dB and a drain efficient of 66%. The gain and output power flatness was within ±0.4 dB while drain efficiency variation was within ±2%.

In the third part, we investigated the usage of copper-graphite as the interposers in design of HPAs. It was shown that using the high thermal conductive interposers with appropriate matched thermal expansion coefficient makes feasible the soldering of high power chips directly to the coolant system and prevents from cracking the chip in soldering process. This consequently reduces the thermal impedance below of the high power chips to avoid from accumulating energy due to using ECAs and improves the thermal management. As a proof of concept, a C-band 40 W hybrid HPA was designed and fabricated, where 4 MMIC power-bars are matched and combined off-chip using low-loss multilayer LTCC technology and mounted using copper-graphite interposers. In comparison with thermal performance in a C-band 40 W MMIC HPA, the simulation and measurement results for the hybrid HPA shows 10-15 °C better thermal management at the base and surface of the power chips.

The research results presented in this thesis can be extended to address the PA's requirements in the latest generation of wireless transceivers. It is known that the complicated signal modulations in the 5th generation of wireless networks results in higher peak-to-average power ratios over wideband frequency range. Hence, it is necessary to develop the PAs performance in back-off efficiency and improve the linearity. While, keeping the efficient performance in back-off power requires a wide range of optimum load points on Smith chart that can lead to complicated and bulky matching circuit networks, limit the operational bandwidth, and degrade the linearity performance. Therefore, extending the proposed theory in this thesis to

the well-known PAs topology with high back-off performance such as Doherty power amplifier (DPA) can lead to flexible and small matching networks and provide wider band width and better linearity performance. Moreover, implementation of PAs at millimeter wave frequency ranges have been challenging due to the sensitivity of the matching networks to the length of transformation lines. Therefore, the proposed solutions to expand optimum design space for terminating the fundamental and second load harmonic impedances can be used to meet the requirements and reduces the negative effects of fabrication tolerance on PAs' performance.

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