# Highly linear RF amplifying transmitarray unit-cell with varactor-based reconfigurable phase and amplitude

by

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**Cellule RF hautement linéaire pour matrice d'antennes en transmission avec reconfiguration de la phase et de l'amplitude basée sur des réseaux de varacteurs**

David BERTHIAUME

## RÉSUMÉ

Ce travail de recherche propose une solution innovante comme cellule RF pour une matrice d'antennes en transmission reconfigurable (RTA) incluant une fonction d'amplification et des contrôles basés sur des réseaux de varacteurs pour ajuster la phase et l'amplitude indépendamment. Un aspect important de cette cellule pour RTA est sa capacité à délivrer des signaux RF hautement linéaires à des niveaux de puissances relativement élevés pour des émetteurs. De plus, la consommation de courant DC et le nombre de composantes sont minimisés afin de maximiser l'efficacité énergétique ainsi que la fiabilité. Ces fonctionnalités innovatrices sont rendues possible grâce à l'introduction de nouvelles solutions pour améliorer les performances des blocs de circuit et des réseaux de varacteurs, qui sont des éléments clés dans la cellule RF proposée pour les RTA. Ces circuits clés sont un réseau d'impédance accordable (TIN) à base de varacteurs permettant la reconfiguration des deux réseaux suivants : un réseau contrôlant la phase et un réseau incluant un contrôle de l'amplitude ainsi qu'une fonction d'amplification.

Le TIN proposé dans ce travail consiste en une nouvelle technique de circuit basée sur des varacteurs avec une linéarité améliorée en présence de capacités parasites et d'inductances parasites. Le mécanisme causant la dégradation de la linéarité dans des réseaux de varacteurs en configuration anti-séries en présence d'éléments parasites – un aspect clé qui, à notre connaissance, n'a jamais été abordé dans la littérature – est d'abord étudié à l'aide d'une approche analytique basée sur une excitation à fréquences multiples (multi-tone). Il est démontré de façon analytique pour la première fois que simplement optimiser le rapport de dimensions entre les diodes est insuffisant pour contourner cette dégradation de linéarité. La compréhension du mécanisme de dégradation de la linéarité sert de base pour l'introduction d'une nouvelle topologie de varacteurs en configuration anti-séries modifiée (c.-à-d. le TIN proposé) qui génère un minimum de distorsions en présence d'éléments parasites.

Dans la cellule pour RTA proposée, le réseau contrôlant la phase sur 360° et à faibles pertes est un déphaseur à base de varacteurs de type réflexion (V-B RTPS). Les performances en linéarité de ce V-B RTPS sont améliorées par rapport à l'état de l'art tout en considérant les pertes d'insertion (IL), la fréquence d'opération et la plage de déphasage ($\Delta\phi$). L'autre réseau reconfigurable impliqué dans la cellule RTA proposée est un amplificateur GaN RF d'un seul étage incluant des mécanismes de contrôle de l'amplitude sur une grande plage.

Des résultats expérimentaux à une fréquence de 3.6GHz sur les deux réseaux contrôlables et sur un prototype d'une cellule pour RTA démontrent un déphasage jusqu'à 360°, une variation de l'amplitude de 10dB, et un comportement hautement linéaire à une puissance maximale de sortie allant de 14.1dBm à 19.1dBm, en réponse à une excitation à 2 tonalités. Par conséquent, la cellule pour RTA proposée et ses réseaux contrôlables avec de telles capacités de

reconfigurations, tout en atteignant des performances hautement linéaires à des niveaux de puissance adéquats pour émetteurs, constituent une amélioration significative de l'état de l'art dans les domaines des TINs, des déphaseurs et des RTAs.

En plus d'améliorer l'état de l'art en atteignant des performances inégalées, cette cellule pour RTA offre plusieurs opportunités pour de nouvelles fonctionnalités au niveau d'un système d'antenne RTA. Ceci est soutenu par des analyses de systèmes RTA basées sur des performances mesurées. Ces analyses révèlent que notre cellule pour RTA a le potentiel 1) d'améliorer considérablement les performances de linéarité à des niveaux de puissances élevés, contrairement à la plupart des solutions basées sur des varacteurs qui sont limités à des applications utilisant de faibles puissances, 2) de compenser la variation de la perte d'insertion ($\Delta$IL) du déphaseur pour une meilleure qualité du faisceau de champ électromagnétique transmis, 3) d'améliorer considérablement l'efficacité d'une antenne planaire, ce qui n'a jamais été démontré à l'aide de performances mesurées et 4) de réduire l'influence négative de toutes les sources de pertes situées en amont de ces amplificateurs sur l'efficacité énergétique globale d'un système d'antennes RTA. Un aspect qui est rarement considéré dans la littérature, même pour des solutions employant des fonctions d'amplification.

**Mots-clés**: Ajustable, Amplitude, Cellule d'une matrice, Contrôlable, Déphaseur de type réflexion (RTPS), Diode, Distorsion, Distorsion d'intermodulation (IMD), Fréquences multiples (multi-tone), Linéarité, Matrice d'antenne à alimentation spatiale, Matrice d'antenne en transmission, Parasite, Phase, Perte d'insertion (IL), Rapport de puissance de canal adjacent (ACPR), Reconfigurable, Technique de linéarisation, Varacteur.

**Highly linear RF amplifying transmitarray unit-cell with varactor-based reconfigurable phase and amplitude**

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## ABSTRACT

This research proposes a novel reconfigurable transmitarray (RTA) RF unit-cell including varactor-based magnitude and phase control capabilities and an amplifying function while delivering highly linear RF signals at transmitters' power levels. Moreover, the DC current consumption and the components count are minimized for maximum energy efficiency and maximum reliability. These novel features are made possible by proposing solutions to improve the performances of the key circuit blocks and networks involved in this RTA unit-cell. These key circuit blocks are a varactor-based tunable impedance network (TIN) enabling the reconfiguration capabilities within both the following networks: a network controlling the phase and a network including a control of the magnitude and an amplification function.

The proposed TIN in this work consists of a novel varactor-based circuit technique with improved linearity in the presence of parasitic capacitances and parasitic inductances. The mechanism causing linearity degradation in an anti-series varactor network that includes significant parasitic elements – a key aspect that, to our knowledge, has never been reported – is first studied using an analytical approach based on a multi-tone excitation. It is demonstrated analytically that simply optimizing the ratio of diode sizes is insufficient to circumvent this linearity degradation. The underlying linearity degradation concept serves as the basis for introducing a modified anti-series controllable capacitance (i.e., the proposed TIN) generating minimum distortions in the presence of parasitics.

In the proposed RTA unit-cell, the network controlling the phase is a low-loss 360° varactor-based reflection-type phase shifter (V-B RTPS) network with improved linearity performances over the state-of-the-art when considering power, insertion loss (IL), frequency, and relative phase shift ($\Delta\phi$) range. The other reconfigurable network involved in the proposed RTA unit-cell is a single-stage GaN RF amplifier including mechanisms to tune the gain over a wide range.

Measured performances on both fabricated RF controllable networks and on a prototype RTA unit-cell at a carrier frequency of 3.6GHz demonstrate a relative phase shift up to 360°, a magnitude variation up to 10dB, and a delivered highly linear output power level ranging from 14.1dBm to 19.1dBm in response to a multi-tone excitation. Hence, the proposed amplifying RTA unit-cell and its controllable networks with such reconfiguration capabilities while achieving highly linear performances at transmitter-like power levels constitute a significant improvement with respect to the state-of-the-art in the fields of TINs, phase-shifters, and RTAs.

In addition to improving the state-of-the-art by achieving unequaled performances, this RTA unit-cell provides many opportunities for new system-level functionalities. This is supported by measured-performance -based analyzes on RTA antenna systems. These analyses reveal that our proposed RTA unit-cell has the potential of 1) significantly enhancing the linearity performances at large power levels, in contrast with most reported varactor-based solutions limited to low-power applications, 2) compensating the insertion loss variation (ΔIL) of the phase shifter for a better quality of the scattered field, 3) significantly improving the antenna efficiency of a planar aperture, an aspect that was never demonstrated based on measured performances, and 4) reducing the negative impact of all the losses located upstream these RF amplifiers on the global system energy efficiency, an aspect that is not considered in most reported RTA systems, even for RTA systems employing amplifying functions.

**Keywords:** Adjacent channel power ratio (ACPR), Amplitude, Anti-series, Controllable, Diode, Distortion, Intermodulation distortion (IMD), Insertion loss (IL), Linearity, Linearization techniques, Multi-tone, Parasitic, Phase, Reflection-type phase shifter (RTPS), Reconfigurable, Spatially-fed array antenna, Transmitarray, Tunable, Unit-cell, Varactor.

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| | |
|---|---|
| $\Delta\phi_{MAX}$ | Maximum relative phase shift |
| $\Delta G$ | Gain variation |
| $\Delta IL$ | Insertion loss variation |
| $\phi$ | Phase |
| $\eta_a$ | Antenna efficiency |
| $\eta_i$ | Illumination efficiency |
| $\eta_s$ | Spillover efficiency |
| $\eta_{SYS}$ | System energy efficiency |
| A | Amplitude (or magnitude) |
| AC | Alternating current |
| ACPR | Adjacent channel power ratio |
| APS | Amplifying and phase shifting |
| DC | Direct current |
| DUT | Device under test |
| $f_0$ | Fundamental frequency |
| EM | Electromagnetic |
| FET | Field-effect transistor |
| FoM | Figure of merit |
| $FoM_{LIN}$ | Linearity figure of merit |
| $FoM_{PS}$ | Phase shifter Figure of merit |
| GEO | Geostationary orbit |
| IL | Insertion loss |

| | |
|---|---|
| $IL_{MAX}$ | Maximum insertion loss |
| IM | Intermodulation |
| IMD | Intermodulation distortion |
| $IMD_{2f2-f1}$ | Intermodulation distortion product at the frequency $2f_2 - f_1$ |
| IMD3 | 3rd order intermodulation distortion |
| L-C | Inductance and capacitance (or inductive and capacitive) |
| LEO | Low Earth orbit |
| MEMS | Micro-electro-mechanical systems |
| MEO | Medium Earth orbit |
| MMIC | Monolithic microwave integrated circuit |
| PA | Power amplifier |
| PAE | Power added efficiency |
| $P_C$ | Power of the carrier |
| PCB | Printed circuit boards |
| $P_{IN}$ | Input power |
| $P_{OUT}$ | Output power |
| $P_{USB}$ | Power of the upper sideband |
| QAM | Quadrature amplitude modulation |
| RA | Fixe (or non-reconfigurable) reflectarray |
| RF | Radio frequency |
| RRA | Reconfigurable reflectarray |
| RRTA | Reconfigurable reflectarray and transmitarray (or spatially-fed antenna) |
| RTA | Reconfigurable transmitarray |

| | |
|---|---|
| Rx | Receiver |
| SLL | Side lobe level |
| SoG | Silicon on Glass |
| SMA (component) | Surface mount assembly |
| SMA (connector) | Sub-Miniature Version A |
| RWG | Rectangular waveguide |
| TA | Fixe (or non-reconfigurable) transmitarray |
| TBD | To be determined |
| TIN | Tunable impedance network |
| TRL | Technology readiness levels |
| Tx | Transmitter |
| USB | Upper sideband |
| V-B RTPS | Varactor-based reflection-type phase shifter |
| VNA | Vector network analyzer |

# LIST OF SYMBOLS

**LENGTH**

| | |
|---|---|
| m | meter |
| mil | thousandth of an inch |

**PHASE**

| | |
|---|---|
| Deg | degrees |

**TEMPERATURE**

| | |
|---|---|
| °C | degree celsius |

**FREQUENCY**

| | |
|---|---|
| Hz | hertz |
| kHz | kilohertz |
| MHz | megahertz |
| GHz | gigahertz |

**ELECTRIC**

| | |
|---|---|
| A | ampere |
| V | volt |

**CHEMICAL ELEMENT SYMBOL**

| | |
|---|---|
| GaAs | gallium arsenide |
| GaN | gallium nitride |
| Si | silicon |

**TIME**

| | |
|---|---|
| µsec | microsecond |
| msec | millisecond |
| min | minute |

**GAIN and POWER**

| | |
|---|---|
| W | watt |
| dB | Decibel |
| dBc | decibels relative to the carrier |
| dBm | decibel relative to one milliwatt |

**ELECTRIC COMPONENTS**

| | |
|---|---|
| Ω | ohm |
| kΩ | kiloohm |
| MΩ | megaohm |
| F | farad |
| fF | femtofarad |
| pF | picofarad |
| H | henry |
| mH | millihenry |
| µH | microhenry |
| pH | picohenry |

# INTRODUCTION

The aerospace industry is showing increasing interest in reconfigurable antenna systems. This type of system provides opportunities for advanced functionalities (e.g., beam steering and beamforming capabilities) that would ultimately facilitate the adaptation of satellites to the evolving market. However, the needs for fast switching speed and reliable reconfigurations are not yet answered by the actual state-of-the-art. For instance, mechanically-based solutions (e.g., parabolic antenna systems) have a *very* slow scanning speed relative to electronically-based solutions and are generally incapable of producing beamforming functions (Hum & Perruisseau-Carrier, 2014). This thesis shows that electronically reconfigurable, spatially-fed antenna systems are interesting candidates for such required features. Spatially-fed antenna systems include reconfigurable reflectarrays (RRAs) and reconfigurable transmitarrays (RTAs) (or array lenses) (Hum & Perruisseau-Carrier, 2014). This document uses the acronym RRTA (reconfigurable reflectarray and transmitarray) when referring to spatially-fed antennas in general. Also, fixed reflectarray and transmitarray systems (non-reconfigurable) are referred to as RA and TA, respectively.

For electronically-based solutions (e.g., phased arrays and RRTAs), one fundamental element that dictates, and thus limits, the achievable performances is the technology enabling the reconfigurability within the RF controllable networks (control of the phase or magnitude or both). The literature proposes many technologies: MEMS switches, MEMS variable capacitors, solid-state devices (e.g., PIN diodes and varactor diodes), etc. A survey of all available technologies detailed in CHAPTER 1 reveals that solid-state varactor diodes are well-suited for most performances pursued in this research work. Unfortunately, varactors are also associated with poor linearity performances and limited power handling. For these reasons, the authors reviewing RRTA solutions in (Hum & Perruisseau-Carrier, 2014) stipulate that varactor solutions are mostly limited to low-power receiver applications. Therefore, one of the focuses of this work is to propose innovative circuit techniques and novel architectures to demonstrate that it is possible *to operate RTA varactor-based solutions at typical transmitters' power levels* when considering telecommunication's *linearity* requirements.

The global research efforts of this work are oriented towards proposing, by significantly improving the state-of-the-art of the *controllable RF networks* and the *architecture involved in the unit-cells* of an RTA antenna system, solutions aiming at improving the performances of:

1) the controllable networks when considering:
   - linearity at typical satellite transmission power levels,
   - range of tunability,
   - energy efficiency,
   - minimal losses and maximal gain,
   - reliability,
   - network physical area on a PCB,
2) the RTA antenna system when considering:
   - maximal delivered linear power,
   - antenna efficiency,
   - quality of the scattered field (e.g., side lobe levels),
   - global system energy efficiency.

## 0.1 Key contributions of this Ph.D. to significantly improve the state-of-the-art

This research project proposes:

1) an innovative anti-series varactor topology with improved linearity in the presence of parasitics surrounding the diodes and minimal usage of solid-state components (CHAPTER 3),
2) a 360° phase shifter with low and constant insertion loss with improved linearity at high power levels (CHAPTER 4),
3) a GaN-based amplifying RTA unit-cell including varactor-based controls of the magnitude and phase with improved linearity allowing operations at transmitters' power levels and minimum DC consumptions (CHAPTER 6),
4) analysis of potential system-level improvements and novel features associated with the proposed RTA unit-cell (CHAPTER 6).

## 0.2 Organization of the thesis

This thesis has six chapters. CHAPTER 1 summarises fundamental basic notions related to RRTA systems, presents the system under investigation, lists the system-level major stakes, and gives the critical circuit-level characteristics that are pursued. CHAPTER 2 is a literature review, considering the pursued characteristics, of reported spatially-fed antenna systems and controllable networks. Based on this review, CHAPTER 2 is concluded by briefly presenting all the innovative concepts proposed in this work.

CHAPTER 3 presents the proposed varactor-based tunable impedance network (TIN) which is implemented in a novel network controlling the phase proposed in CHAPTER 4 and a controllable gain RF amplifier presented in CHAPTER 5. Finally, CHAPTER 6 proposes a novel RTA unit-cell and analyses its potential for improvements at a system-level.

# CHAPTER 1

# RTA SYSTEM UNDER INVESTIGATION AND IDENTIFIED MAJOR STAKES

This chapter presents the antenna system under investigation as well as the major stakes considered in this work, and is organized as follows.

Section 1.1 and Section 1.2 identify the type of antenna system and the technology enabling the controllability that have the most promising characteristics concerning the pursued objectives in this work.

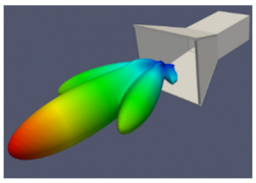
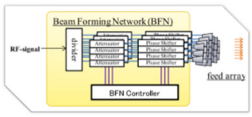
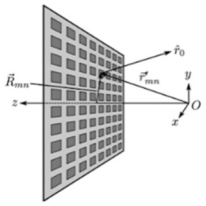
Based on the conclusions drawn in Section 1.1 and Section 1.2, Section 1.3 describes the antenna system under investigation and lists a set of specifications associated with this system.

Finally, the circuit-level and system-level major stakes are described in Section 1.4.

## 1.1 Type of antenna system: Reconfigurable transmitarrays (RTA)

Table 1.1 identifies the key characteristics of the existing type of antenna systems. It is possible to conclude from Table 1.1 that the RA and TA systems are interesting hybrids between aperture antennas and phased arrays since they use only a single RF front end at the feed source. In contrast, the phased arrays use one RF front end for each unit-cell. Therefore, RRTAs reduce the complexity and the global cost, but more importantly, they avoid excessive losses within the phased array's power distribution network.

Table 1.1 Classification of most common antenna systems
Taken from Hum & Perruisseau-Carrier (2014)

| | **Aperture antennas** | **Phased arrays** | **RRTAs** |
|---|---|---|---|
| **Illustration** |  Taken from openEMS, s.d. |   Taken from Nakazawa, Nagasaka, Kamei, Tanaka, & Ikeda, (2014) |  Taken from Hum & Perruisseau-Carrier (2014) |
| **Main advantage** | • Low-cost<br>• High antenna gain (no loss in bulk or *long* transmission lines) | • Allow electronic-based beam steering | • Only one transceiver<br>• Overall promising as high-gain antenna alternative |
| **Main downside** | • Limited to mechanical-based scanning (slow and no beamforming) | • One transceiver for each unit-cell yielding high cost<br>• The feeding network become lossy at high frequencies. | • Difficult to simultaneously obtain compactness and linearity<br>• Difficult to achieve high bandwidth |

### 1.1.1 RRTA basic theory

Figure 1.1 presents the architecture of RRAs and RTAs. The basic idea of RRTAs is to apply a phase correction between the incident wave from a nearby feeding source and the scattered wave of each element on the RRTA surface, in order to obtain a constant phase of the scattered field in a plane normal to the direction of the desired pencil beam (Hum & Perruisseau-Carrier, 2014). It is also possible to produce other beam profiles at the cost of more complex phase correction profiles. For the case of an RRTA with a feed centred on the aperture (i.e., at the origin "O" Figure 1.1), the equation (1.1) (Hum & Perruisseau-Carrier, 2014) is used to solve the necessary phase correction ($\Delta\phi_{mn}$) of each element for a given desired beam direction ($\hat{r}_0$).

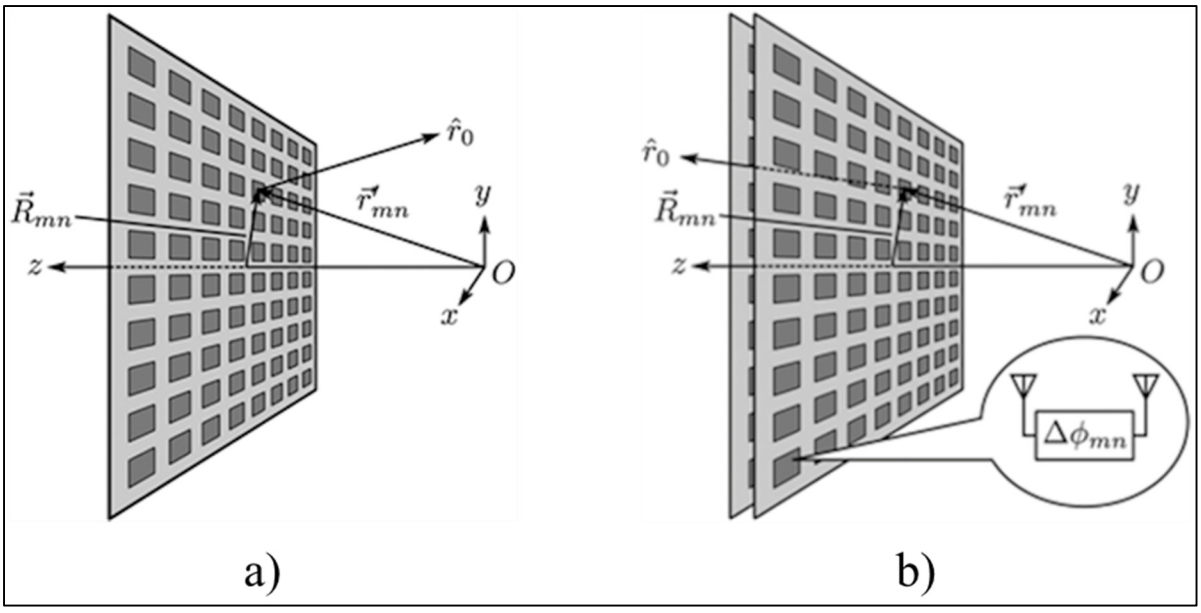



Figure 1.1 Spatially-fed array architectures. (a) Reflectarray (b) Transmitarray
Taken from Hum & Perruisseau-Carrier (2014)

$$k_0\left(r'_{mn} - \vec{R}_{mn} \cdot \hat{r}_0\right) - \Delta\phi_{mn} = 2\pi N \tag{1.1}$$

The main difference between the RRAs and RTAs is the side of the aperture where the feed is located relative to the transmitted field. In RRAs, the feed and scattered field are on the same side of the aperture, whereas they are on opposite sides in RTAs. As explained in the next section, even though these two architectures share many similarities, the RTA architecture is selected over the RRA because it demonstrates a higher potential for improvement concerning the proposed innovative concepts.

### 1.1.2 Trade-off between RRA and RTA antenna systems

Regarding antenna global performances and practicality, it appears that RRAs inherently have some benefits over RTAs. e.g., the authors in (Benet, Perkons, Wong, & Zaman, 1993), an amplifying fixed phase RA for spatial power combiner applications, point out that the RA's non-radiating surface may give opportunities to design the DC bias networks and to dissipate the heat produced by the amplifiers. Also, the antenna efficiency of RRAs is generally higher than RTAs since the undesired reflections on the reflector are re-radiated in the same semi-

sphere than the scattered field, hence contributing to its power as opposed to the RTA where the undesired reflections on the aperture are inherently wasted. Nonetheless, many TAs and RTAs have been reported (Lau & Hum, 2012a; Lau & Hum, 2012b; Nicholls & Hum, 2016; Pan, Huang, Ma, & Luo, 2014), demonstrating excellent global performances.

On the other hand, Section 2.1.1 of the literature review reveals that amplifying solutions give many opportunities for innovations to answer the needs of the targeted application. Amplifying solutions is the *dominating aspect that influences the choice of RTAs over RRAs* in this work. This is because RRA antenna systems inherently allow a mutual coupling between the output and the input of the amplifier, thus creating a feedback loop that limits the maximum gain of the amplifier for stability reasons.

Reported RA and RRA solutions allow mitigating the mutual coupling between the Rx and Tx ports. This is achieved, for instance, by using a dual-polarized orthogonal solution (refer to Figure 1.2) (Kishor & Hum, 2012) or “U-shape” slots with one close to the center of the patch antenna to increase the isolation between both slots (Bialkowski, Robinson, & Song, 2002). However, the authors of (Pan et al., 2014) mention that TA solutions inherently achieve higher isolation between the Rx and Tx ports than any reported RA or RRA solutions without additional complexity in the patch antenna design.

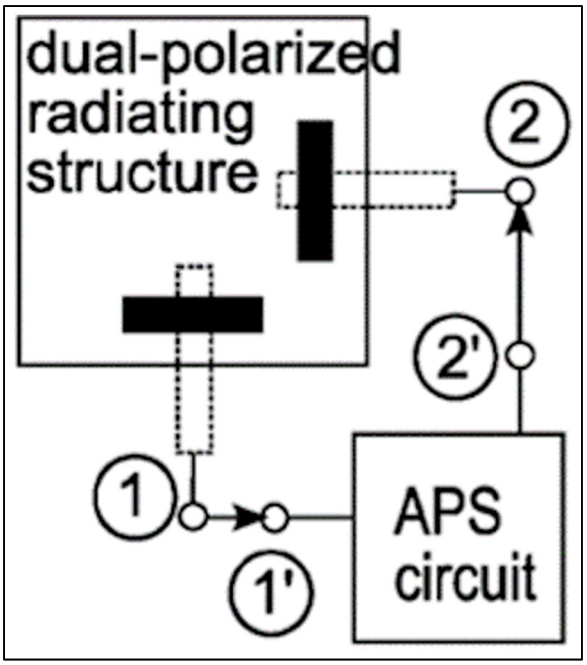



Figure 1.2 A cross-polarized RRA unit-cell where APS (amplifying and phase shifting) is an amplifying-based controllable RF network
Taken from Kishor & Hum (2012)

## 1.2 Technology to enable controllability: Solid-state varactors

Table 1.2 compares all the major available enabling technologies for the design of RRAs and RTAs. Here "*enabling technologies*" is the device allowing to control the phase or amplitude of the scattered wave of each unit-cell of an aperture. It will be presented in section 1.3.2, section 1.4, and section 1.5 that fast switching speed. High energy efficiency, compactness, reliability and linearity at large power levels are key criteria regarding the choice of the enabling technology.

Table 1.2 Enabling technologies qualitative comparison
Taken from Hum & Perruisseau-Carrier (2014) and Nayeri, Yang, & Elsherbeni (2015)

| Enabling technology | | Advantages | Limitations |
|---|---|---|---|
| **Mechanical translation** | | ✓ High power handling<br>✓ Low-IL | ✗ Slow scanning speed<br>✗ High level bias<br>✗ Low reliability |
| **Electronic-based** | **Trends for all electronic-based** | ✓ Fast scanning speed<br>✓ Low-moderate DC consumption | ✗ Low to moderate power handling<br>✗ Difficult at mm-waves |
| | **p-i-n diodes** | ✓ Discrete control<br>✓ Lower IL (than FET switches) | ✗ DC current when ON |
| | **FET switch** | ✓ Discrete control<br>✓ Low DC consumption | ✗ Higher IL at RF |
| | **MEMS** | ✓ Discrete & continuous control<br>✓ Low IL<br>✓ High linearity & power handling<br>✓ ~No DC consumption | ✗ Slower (than solid-state)<br>✗ High bias voltage<br>✗ High cost<br>✗ Low reliability |
| | **Varactors** | ✓ Continuous control<br>✓ Fast scanning speed<br>✓ Low bias voltage<br>✓ High reliability<br>✓ ~No DC consumption | ✗ Low linearity & power handling |
| **Functional materials** | | ✓ Continuous control<br>✓ Potential at mm-waves | ✗ Technology not mature<br>✗ High cost |

Because the targeted application aims for sub-6GHz applications and that "*Functional Materials*" are attractive at much higher frequencies, they are not considered in this work. The following subsection further details the justification of the selection of solid-state varactors in this work.

### 1.2.1 Important considerations for the enabling technology

Two distinct approaches exist:

1) the discrete approach enabled mainly with p-i-n diodes (Carrasco, Barba & Encinar, 2012; Clemente, Dussopt, Sauleau, Potier, & Pouliguen, 2012) or MEMS switches (Rajagopalan, Rahmat-Samii, & Imbriale, 2008; Salti, Fourn, Gillard, & Legay, 2010),
2) the continuous approach using solid-state varactors (Kishor & Hum, 2012; Lau & Hum, 2012a; Riel & Laurin, 2007) or variable MEMS capacitors (Hum, Okoniewski, & Davies, 2007).

The trade-off between these two approaches is the following. The higher the quantization of each discrete element phase is large (i.e., larger step between possible phase values and corresponding to lower resolution), the further its performances diverge (being worse) from those of a design using a continuous approach (i.e., *best* performances) (Nayeri et al., 2015). This is supported by the results presented in Figure 1.3, where higher side lobes are observed for discrete designs. It is worth mentioning that the impact of phase error (due to a discrete solution) on the side lobes tends to be less significant as the aperture size is increased. On the other hand, the main benefit of discrete designs is the lower complexity of the calibration process and lower cost, especially for lower bit phase shifter designs (Nayeri et al., 2015).

Moreover, solid-state varactors are mature and widespread due to their ease to control, fast switching speed, high reliability, small profile, high energy efficiency, etc. Therefore, they are more attractive than MEMS technologies which are prone to lower reliability, an essential issue for satellite applications (Huang et al., 2008b).

It is therefore possible to conclude that continuous approaches are more attractive since this project targets satellite applications where performances and reliability are more important than cost and calibration complexity.

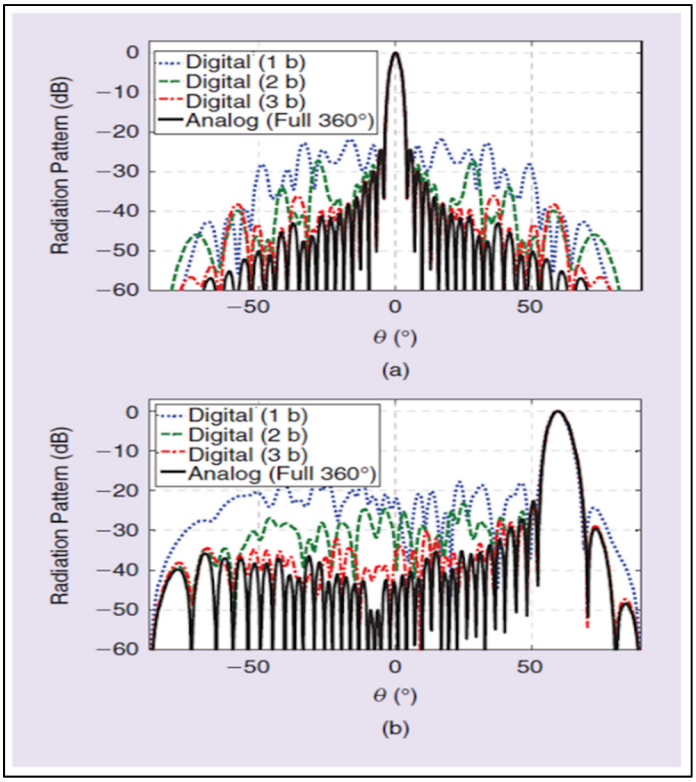



Figure 1.3 A comparison of RAs radiation pattern with digital and analog phase controls. (a) The broadside beam, and (b) the scanned beam Taken from Nayeri et al (2015) and originally published in Nayeri (2012)

However, the main drawbacks of solid-state varactors are their limited linearity performances at high power levels and limited power handling. Hence, this research project focuses, in part, on circumventing these drawbacks by improving the linearity performances of varactor-based RTA antenna systems.

## 1.3 RTA antenna system under investigation

This section presents the RTA antenna system under investigation (also referred to as the targeted application) and lists the specifications related to this system.

### 1.3.1 Schematic of the system under investigation

Figure 1.4 is a block diagram describing the highest hierarchy level of the RTA antenna system under investigation with electronic-based beam steering and beamforming capabilities.

In this system, the feed antenna irradiates an aperture. This aperture is an array of m×n unit-cells. Each unit-cell includes a receiving (Rx) antenna structure, RF networks controlling the phase or the amplitude (or both) of the RF signal, and a transmitting (Tx) antenna structure. By properly tuning the RF signal within each unit-cell, the transmitted signals by the Tx antennas generate a scattered field with the desired characteristics (beam direction, beam shape, etc.).

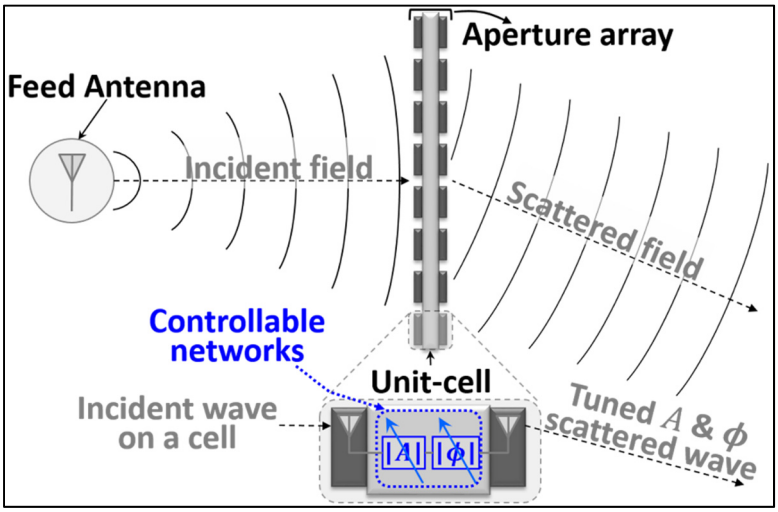



Figure 1.4 Schematic of the electronically controllable RTA system under investigation

### 1.3.2 Antenna system specifications

Table 1.3 lists the system-level specifications that our industrial partners proposed. These specifications are described for different applications and three different types of orbits; geostationary orbit (GEO), medium Earth orbit (MEO) and low Earth orbit (LEO). This work

focuses on tracking applications at lower Earth orbits because they require less power while needing fast switching speed capabilities.

Since this research work's technology readiness level (TRL) is low, these specifications are thus general guidelines for innovations. Nonetheless, they influence many aspects of this project, e.g., the selected type of antenna systems (i.e., RTAs in Section 1.1) and the technology enabling the reconfigurability functions (i.e., solid-state varactors in Section 1.2). Moreover, this list of system-level specifications translates into future chapters on requirements specific to each proposed controllable RF network.

Table 1.3 Antenna system specifications given by our industrial research partners

| **Orbit** | | | **GEO** | | **LEO** | **MEO** |
|---|---|---|---|---|---|---|
| **Sub-type** | | | Shaped coverage of the Earth | Beam hopping | Tracking | Tracking |
| **Frequency band** | **Downlink** | **(GHz)** | 3.4-4.2 | | | |
| | **Uplink** | | 5.85-6.725 | | | |
| **Switching speed** | | | Several min. | ~µsec | ~msec | ~msec |
| **Earth surfaced covered by a conical sector of:** | | **(Deg)** | 17 | | 52 | 126 |
| **Polarization** | | | Fixed for whole mission (linear or circular) | | | |
| **9th order IM[*1]** | | **(dBc)** | <-135 | | | |
| **Operating temperature** | | **(ºC)** | -120 to 120 | | -80 to 120 | -50 to 70 |
| **Aperture diameter[*2]** | | **(m)** | >1.5 | | | |

[*1]Must be measured with carriers of 50W each
[*2]Possible to prototype using smaller dimensions and scale power for a ~1.5m aperture

It is worth mentioning that a carrier frequency of $f_0 = 3.6GHz$ is considered for this work.

## 1.4 Major antenna system stakes

This section details the major antenna system stakes that are taken into consideration in this research project.

### 1.4.1 Metric to characterize linearity performances and maximal delivered linear power by an RTA unit-cell

The maximum power level delivered by an RTA unit-cell while meeting a linearity specification is a key aspect of this research. The linearity specified in Table 1.3 uses the 9th order intermodulation (IM) product and corresponds to very low and often unmeasurable power levels. Based on simulation, the 9th order IM <-135dBc in response to a 2-equal tone is converted into a requirement on a 3rd order IM product which needs to be lower than -40dBc. This value is a realistic simulation-based estimation between the correspondence of a 9th and a 3rd order nonlinearity in varactor-based phase control circuitry.

The metric to evaluate the 3rd order intermodulation distortion (IMD) (illustrated in Figure 1.5a) for a 2-equal tone RF excitation at $\omega_1$ and $\omega_2$, is the ratio of the power $P_{USB}$ at the IMD product at the angular frequency $2\omega_2 - \omega_1$ (or equivalently at $2f_2 - f_1$) over the power $P_C$ at $\omega_2$ (i.e., $IMD_{2f_2-f_1} = \frac{P_{USB}}{P_C}$). This metric is expressed in dBc (Maas, 2003). $IMD_{2f_2-f_1}$ is preferred over the standard IMD3 notation since multiple IM products contribute to the level of distortion at $2f_2 - f_1$ in simulation due to different orders of nonlinearity in a polynomial model and in experimental results. Also, most linearity measurements in this work are characterized at a specific output power level.

Moreover, the highest (i.e., worst) $IMD_{2f_2-f_1}$ level over a considered range of DC bias voltage (e.g., the linearity being evaluated over the full range of the phase shifter's relative phase shift) is used to characterize the linearity performances. For easy comparison and reference, a linearity Figure of Merit ($FoM_{LIN}$) is defined as the highest $IMD_{2f_2-f_1}$ level over the full considered DC bias range and is also expressed in dBc. This $FoM_{LIN}$ is illustrated in Figure 1.5b on a hypothetical $IMD_{2f_2-f_1}$ curve.

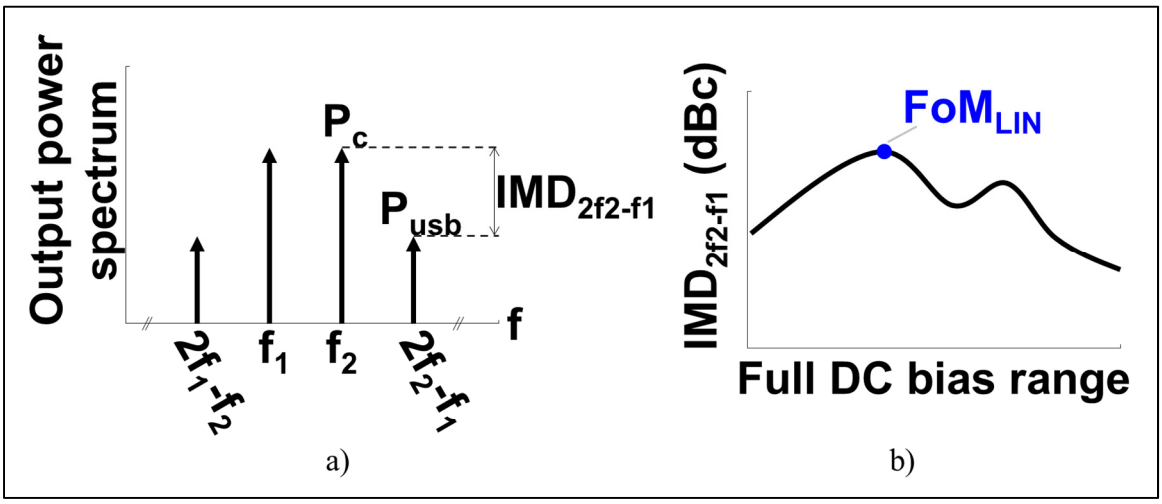



Figure 1.5 a) Considered metric to measure the linearity of a 2-tone RF signal. b) Identification of the $FoM_{LIN}$ on a hypothetical $IMD_{2f2-f1}$ curve

### 1.4.2 Radiation pattern and quality of the scattered field

The radiation pattern of an antenna system comprises several types of lobes. A radiation lobe is a "*portion of the radiation pattern bounded by regions of relatively weak radiation intensity*" (Cited from (Balanis, 2016)). They may be sub-classified into main lobe (or main beam), minor lobes, side lobes and grating lobes. All these lobes are illustrated in Figure 1.6.

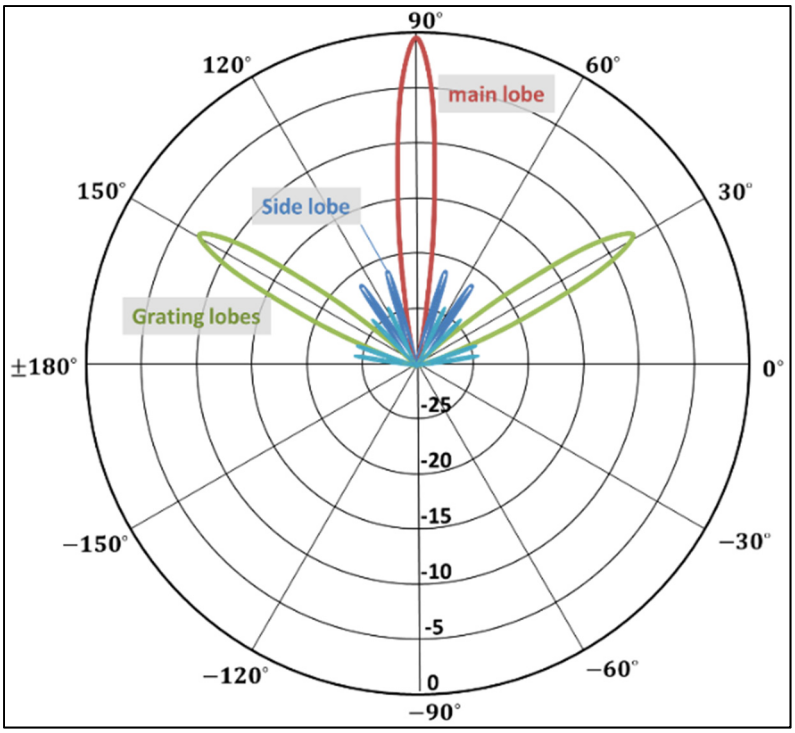



Figure 1.6 Antenna radiation pattern identifying the main lobe, the side lobes, and the grating lobes

Minor lobes usually represent radiation in undesired directions and should be minimized. The power in undesired lobes is referred to as the *quality of the scattered field* in this document. Side lobes are usually the largest of the minor lobes. The level of a side lobe is expressed as the ratio of its power density to the power density of the main lobe. This ratio is referred to as sidelobe level (SLL). Many phenomena contribute to SLL. However, (Lau & Hum, 2012a) highlight that minimizing the insertion loss variations (ΔIL) over the full range of phase shifts of the network controlling the phase helps minimize SLLs.

Grating lobes are specific to arrays and appear due to a diffraction phenomenon occurring for array cell pitch greater than $\frac{\lambda}{2}$. Since it is a diffraction phenomenon, the grating lobes are replicas of the main lobe with an intensity in the same order as illustrated in Figure 1.6. The angles at which the grating lobes appear depend on the pitch between array cells. Grating lobes are detrimental to global performances as they can produce important interferences and significantly reduce the energy radiated in the desired direction (Carrasco et al., 2012). If possible, these lobes are suppressed by using a unit-cell pitch smaller than $\frac{\lambda}{2}$.

### 1.4.3 Limited antenna efficiency of planar aperture

Equation (1.2) defines the antenna efficiency ($\eta_a$) as the product of the spillover efficiency ($\eta_s$) and illumination efficiency ($\eta_i$). $\eta_s$ is the percentage of the radiated power from the feed intercepted by the aperture and is defined in (6) of (Yu, Yang, Elsherbeni, Huang, & Rahmat-Samii, 2010). $\eta_i$ is a measure of the non-uniformity of the scattered field across the aperture and is defined in (19) of (Yu et al., 2010).

$$\eta_a = \eta_s \cdot \eta_i \tag{1.2}$$

The work in (Yu et al., 2010) derives equations (Table 3 of (Yu et al., 2010)) using the coordinate system illustrated in Figure 2 of (Yu et al., 2010) to compute the $\eta_a$ of a center-feed circular aperture system as depicted in Figure 1.7a. In this figure, $\alpha$ is the half aperture angle, D is the diameter of the circular aperture, and H is the feed–aperture distance. These computations use a feed and unit-cells radiation patterns in the form of $\cos^{2\cdot q}\theta$, where $q$ dictates the directivity. It is set to $q = 6$ for the feed and $q = 1$ for each unit-cell of the aperture.

Because RRTAs use planar geometry apertures, one challenge compared to parabolic apertures is the antenna efficiency. The limited $\eta_a$ of RRTAs is supported with Figure 1.7b plotting computed antenna efficiencies of the system in Figure 1.7a reported in (Yu et al., 2010), where the maximal $\eta_a$ is only ~77%. In contrast, theoretical parabolic apertures may achieve 100%.

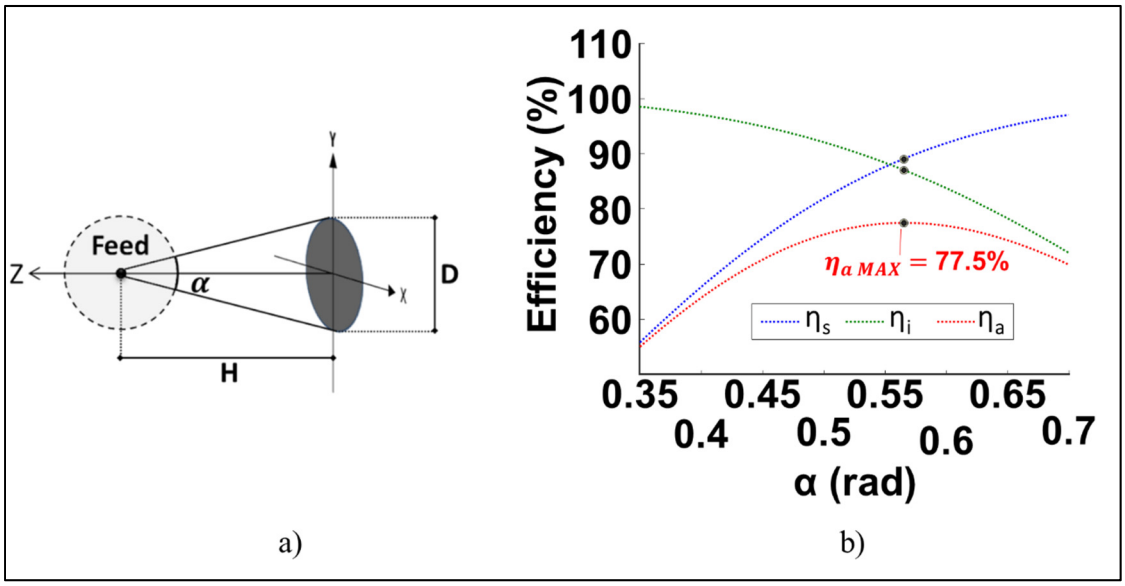



Figure 1.7 Planer circular aperture antenna efficiency as a function of the feed-aperture half aperture angle ($\alpha$) a) Center-feed circular aperture system schematic. Adapted from Yu et al. (2010) b) Computed $\eta_i$, $\eta_s$, and $\eta_a$
Adapted from Yu et al. (2010)

### 1.4.4 Antenna system energy efficiency

The global antenna system energy efficiency ($\eta_{SYS}$) of an RRTA system is rarely discussed in the literature. This is explained because no amplifier function is involved in most proposed RRTA solutions. However, it is considered as a major stake in this work.

$\eta_{SYS}$ is analyzed with the system schematized in Figure 1.8. This system is constituted with:

1) a power amplifier (PA) delivering the RF signal to the feed antenna with an energy efficiency of $\eta_{PA}$,

2) a "PA-A losses" block modelling the losses occurring between the node $P_{Feed}$ and the node $\sum P_{[m,n]_{IN}}$ (resistive losses in the feed antenna, spillover, mismatch, etc.),

3) an array of $m \times n$ unit-cells, and

4) unit-cells composed of an Rx with a loss of $IL_{ANT\ I}$, a network controlling the phase with an insertion loss of $IL_{PS}$, an amplification function with a gain of $G_{GS}$ consuming the DC power $P_{DC\ GS}$, and a Tx antenna with a loss of $IL_{ANT\ O}$.

All the components involved in 4) dictate the relationship between $P_{[m,n]_{OUT}}$ and $P_{[m,n]_{IN}}$. Also, for computation simplifications, the incoming power on each unit-cell ($P_{[m,n]_{IN}}$) is considered uniform, thus $P_{[m,n]_{IN}} = \frac{\sum P_{[m,n]_{IN}}}{[m \times n]_{unit-cells}}$. Similarly, the total output power is approximated to the sum of the delivered power by each unit-cell yielding $\sum P_{[m,n]_{OUT}} = P_{[m,n]_{OUT}} \cdot [m \times n]_{unit-cells}$.

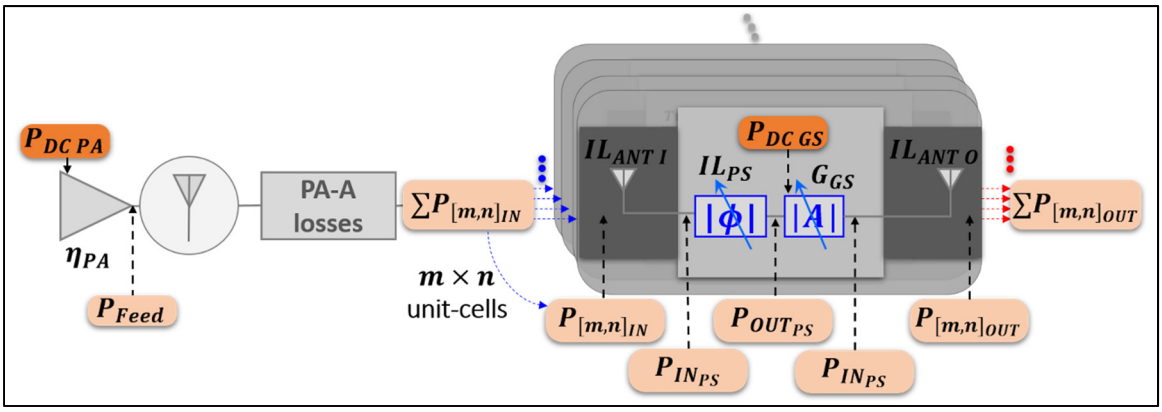



Figure 1.8 Considered antenna system to compute the global system energy efficiency ($\eta_{SYS}$)

Considering the system in Figure 1.8, $\eta_{sys}$ is computed with (1.3). The development of (1.3) is available in ANNEX I.

$$\eta_{SYS} = \frac{\sum P_{[m,n]_{OUT}}}{\sum P_{DC}} = \frac{P_{[m,n]_{OUT}}}{\frac{P_{[m,n]_{IN}}}{IL_{F-A\ Loss} \cdot \eta_{PA}} + P_{DC\ GS}} \tag{1.3}$$

In spite of the simplifications (e.g., uniform illumination) involved in the considered system (Figure 1.8) and that some parameters used in this system may vary for other RTA antenna systems (e.g., $\eta_{PA}$, multiple IL sources, etc.); nonetheless, this method of computing $\eta_{sys}$ allows extracting important tendencies on the impact of the innovative concepts proposed in this project on the global system energy efficiency.

### 1.4.5 Antenna directivity and gain

Antenna gain and directivity are typical figure of merits for antennas. The directivity is described as: "*the directivity of a nonisotropic source is equal to the ratio of its radiation intensity in a given direction over that of an isotropic source*" (cited from (Balanis, 2016)) as defined with (1.4).

$$D_0 = 4\pi \frac{U_{MAX}}{P_{rad}} \tag{1.4}$$

In (1.4), $D_0$ is the maximum directivity (dimensionless) usually expressed in dB, $U_{MAX}$ is the maximum radiation intensity in $W/unit\ solid\ angle$, and $P_{RAD}$ is the total radiated power in W.

The antenna gain ($G_{ant}$) is closely related to the directivity. It is a measure that accounts for the resistive losses that exist in practical antennas as well as its directional capabilities (Balanis, 2016; Pozar, 2009) and is defined with

$$G_{ant} = \eta_{rad} \cdot D_0, \tag{1.5}$$

where $\eta_{rad}$ is the radiation efficiency and is defined with (1.6) (Pozar, 2009).

$$\eta_{rad} = \frac{P_{rad}}{P_{in}} = \frac{P_{in} - P_{loss}}{P_{in}} = 1 - \frac{P_{loss}}{P_{in}} \tag{1.6}$$

In (1.6), $P_{in}$ is the power supplied to the antenna's input, and $P_{loss}$ is the power loss in the antenna.

## 1.5 Key characteristics pursued for controllable RF networks

The system-level specifications (Section 1.3.2) and the major antenna stakes (Section 1.4) dictate the key characteristics pursued for the controllable networks involved in the proposed RTA unit-cell.

This work proposes in CHAPTER 6 an RTA unit-cell architecture built with two novel controllable networks that are introduced in this work: a tunable phase network (CHAPTER 4) and a controllable gain amplifier (CHAPTER 5). This section lists the key features of both controllable networks and their influences on the performances of the RTA antenna system under investigation (Figure 1.4).

These key features are used to evaluate the performances of the reported solutions in the literature. Furthermore, the innovative concepts proposed in this work are oriented towards improving these features.

### 1.5.1 Tunable phase network

The network controlling the phase must achieve a maximal relative phase shift ($\Delta\phi_{MAX}$) greater than 360° for maximal control of the scattered field while minimizing the controllable network insertion loss (IL), in order to optimize the antenna's gain and the global system energy efficiency. The figure of merit ($FoM_{PS}$) defined in (1.7) identifies a key trade-off between these two features and needs to be maximized.

$$FoM_{PS} = \frac{Total\ relative\ phase\ shift}{Maximal\ IL\ over\ full\ \Delta\phi_{MAX}\ range} = \frac{\Delta\phi_{MAX}}{IL_{MAX}}\left(in\frac{°}{dB}\right) \quad (1.7)$$

The variation of the insertion loss (ΔIL) over the full range of $\Delta\phi_{MAX}$ must also be minimized for a better quality of the scattered field (e.g., reduced SLL (Lau & Hum, 2012a)).

As mentioned in Section 1.4.1, the controllable networks must generate minimal distortions at high power levels so that $FoM_{LIN} < -40dBc$. This $FoM_{LIN}$ is measured at a power level of 10dBm at the phase shifter output. Because an amplification function follows the phase shifter in the proposed RTA unit-cell, it significantly increases the power delivered by each unit-cell. Also, the power delivered by the RTA antenna system is scaled up by all the unit-cell (e.g., a circular aperture of a diameter of 1.5m contains ~283 unit-cells of $\frac{\lambda}{2} \times \frac{\lambda}{2}$). Therefore, a 10dBm power level at the output of the phase shifter is consistent with a transmitter application onboard a satellite on an LEO or MEO.

Other important considerations are best possible reliability (hence, minimum components) and a network area smaller than the typical size of $\sim \lambda/2$ by $\sim \lambda/2$ (in free space) of a unit-cell of the aperture in Figure 1.4. Table 1.4 lists the key required features of the network controlling the phase for easy reference and facilitating the comparison of phase shifters among each other.

Table 1.4 Required characteristics for the tunable phase network

| Index | Parameter | Requirement |
|---|---|---|
| **1** | $\boldsymbol{FoM_{LIN}}$ | $\leq -40dBc$ @ $P_{OUT} = 10dBm$ |
| **2** | $\boldsymbol{\Delta\phi_{MAX}}$ | $> 360°$ |
| **2** | $\boldsymbol{FoM_{PS}}$ | Highest value while meeting goals on $\Delta\phi_{MAX}$ and $FoM_{LIN}$ |
| **3** | $\boldsymbol{\Delta IL}$ | Lowest value while meeting goals on $\Delta\phi_{MAX}$ and $FoM_{LIN}$ |
| **5** | **Circuit area** | Smaller than $\frac{\lambda}{2}$ by $\frac{\lambda}{2}$ (In free space) |
| **6** | **Component counts** | Minimum for maximum reliability |

### 1.5.2 Controllable-gain RF amplification

As mentioned in Section 1.1.2, this work uses an amplifying solution. The main characteristics of the network amplifying the RF signal are:

1) a tunable magnitude over a wide range,
2) ability to deliver a modulated signal with $FoM_{LIN} < -40dBc$ at large power levels,
3) high reliability and a circuit area smaller than $\frac{\lambda}{2}$ by $\frac{\lambda}{2}$, which translate into integrating the control and gain functions into a single-stage design,
4) minimum DC power consumption for optimum system energy efficiency, and
5) a return loss $< -10dB$.

## 1.6 Summary of this chapter

This chapter identifies critical circuit-level and system-level considerations of this research project. It identifies the spatially-fed type antenna system, the solid-state varactor technology to enable reconfiguring the antenna, all the major stakes that are the basis for the proposed innovative concepts such as the maximal linear delivered power, etc.

In particular, the antenna system under investigation presented in Section 1.3 is often referred to in the following chapters.

# CHAPTER 2

# LITERATURE REVIEW AND PROPOSED CONCEPTS FOR INNOVATIONS

This chapter identifies the most relevant solutions proposed in the literature in the areas of i) spacially-fed antenna systems (Section 2.1), ii) RF networks controlling the phase (Section 2.2), and iii) the varactor-based tunable impedance networks (Section 2.3) enabling phase and amplitude reconfigurability functions.

Based on this evaluation of the prior-art, this chapter is concluded by presenting in Section 2.4 all the proposed novel concepts that allow this work to significantly improve the actual state-of-the-art. These novel concepts are made possible thanks to the proposed circuit-level innovations and the measured performances in this research and which are presented in CHAPTER 3 to CHAPTER 6.

## 2.1 Literature review: system-level innovations in RRTAs for global high performances and novel features

This section is a literature review of the reported spatially-fed antenna system solutions by focusing on proposed techniques that allow improvements with regard to the major antenna stakes identified in Section 1.4. i.e., maximum delivered output power, system energy efficiency, antenna efficiency, quality of the scattered field, and antenna gain.

It is shown in this section that the prior-art of spatially-fed antenna systems (RAs, TAs, and RRTAs) introduce many advanced features. However, in part due to the complexity of realizing highly linear controllable networks based on solid-state varactors (discussed in Section 2.2), the need for good linearity performances at transmitters' power levels is not yet answered. This is an important aspect that is dealt with in this work.

### 2.1.1 Amplifying solutions

Many fixed (not reconfigurable) spatially-fed antenna solutions include amplifying functions (e.g., (Benet et al., 1993; Bialkowski et al., 2002)). However, to our knowledge, very few RTA amplifying solutions have been proposed. Nevertheless, the work in Pan et al., 2014) demonstrates (illustrated in Figure 2.1) the feasibility of incorporating an amplifying function in an RTA unit-cell to increase the global gain of the antenna system by compensating the insertion loss (IL) of the RF network controlling the phase.

However, as in most fixed and reconfigurable amplifying spatially-fed antenna systems, the work in (Pan et al., 2014) uses a commercially available fixed-bias amplifier device, which risks yielding an excessive DC consumption, and does not report any linearity performance. In other words, most reported amplifying RRTA solutions (e.g., (Kishor & Hum, 2012; Pan et al., 2014)) do not *fully* take advantage of the presence of an amplifier in each unit-cell.

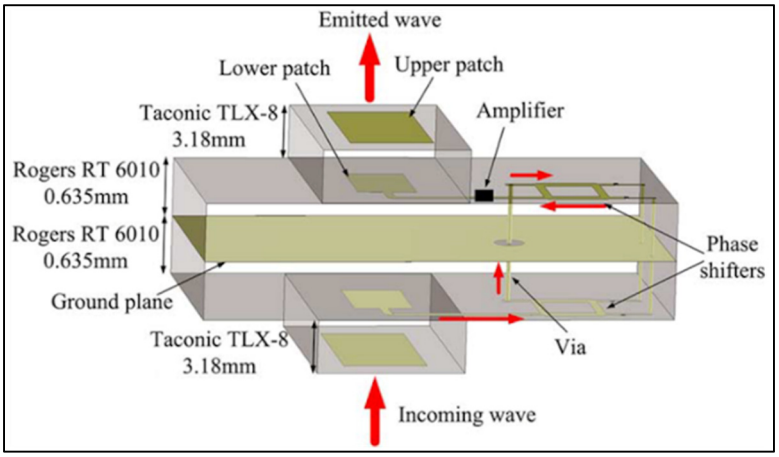



Figure 2.1 An amplifying RTA unit-cell
Taken from Pan et al. (2014)

### 2.1.2 Simultaneous control of the phase and magnitude

Section 1.1.1, describing the basic theory of spatially-fed antenna systems, shows that tuning only the phase is sufficient to achieve beam steering capabilities. It is worth mentioning that

most reported RRTA solutions are only controlling the phase (e.g., (Lau & Hum, 2012b; Riel & Laurin, 2007)).

However, in addition to tuning the phase of the transmitted RF signal within each unit-cell, some works propose to adjust the amplitude (i.e., the magnitude). This additional degree of controllability translates into many novel system-level features for RRTA systems:

1) it allows improving the overall antenna efficiency ($\eta_a$) by compensating the illumination taper of the incident field,
2) it allows better control on the SLL by optimizing the amplitude pattern across the aperture as reported in (Khalaj-Amirhosseini, 2019), and
3) it allows producing more complex antenna radiation patterns, as mentioned in (Yang et al., 2017).

Note that all the works mentioned above use circuit techniques that are not electronically tunable (i.e., without beam steering capabilities), and therefore do not answer the pursued characteristics of this work.

Because the antenna efficiency is a metric used in this work to demonstrate the potential of the proposed RTA unit-cell, feature i) is further detailed in Section 2.1.2.1.

#### 2.1.2.1 Antenna efficiency enhancement using magnitude gradient

The work in (Garcia-Vigueras, DeLara-Guarch, Gómez-Tornero, Guzman-Quiros, & Goussetis, 2012) is oriented towards leaky-wave antenna systems, i.e., a TA, but with the feed integrated inside the aperture. Even though such a system is not considered here, (Garcia-Vigueras et al., 2012) investigated an interesting concept: a tapered leaky-wave leakage rate, consisting of optimizing the amount of energy transmitted from the feed to each unit-cell, to improve $\eta_a$.

This concept is illustrated in Figure 2.2, where the feed is positioned (red dot) in the center of a 1D aperture. In system (a) and system (b), the leakage rate ($\alpha$) is constant for all unit-cells. In system (a), $\alpha$ is optimized for maximum $\eta_S$ (i.e., minimum energy is wasted at both ends of the aperture) and for optimum $\eta_i$ in system (b) (i.e., a more uniform scattered field). System (c) uses a tapered $\alpha$ from the center to the edge of the aperture to optimize $\eta_S$ and $\eta_i$ simultaneously. Simulation results in (Garcia-Vigueras et al., 2012) demonstrate a significant improvement of $\eta_a$ (defined in (1.2)) of the system (c) compared to the systems (a) and (b).

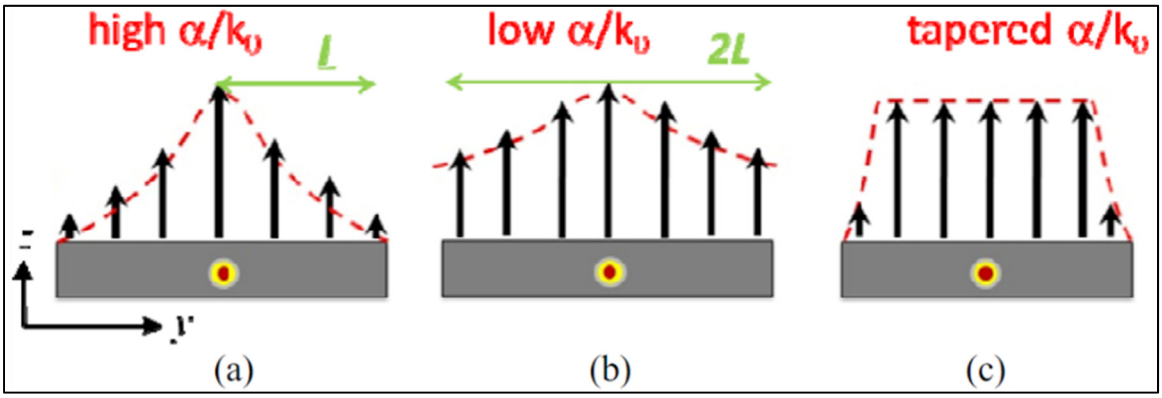



Figure 2.2 Aperture illumination profile for a 1D leaky-wave antenna a) a high attenuation leaky-wave for maximum $\eta_s$ b) a low attenuation profile leaky-wave for higher $\eta_i$, and c) a compensated leaky-wave for optimum $\eta_a$
Taken from Garcia-Vigueras et al. (2012)

The latter concept is applicable in RRTAs by controlling the magnitude of each unit-cell. However, implementing such variable magnitude function based only on attenuation functions worsens the antenna's gain. As seen next, amplifying solutions may be used to circumvent this problem.

The work in (Hosseini & Rahmat-Samii, 2015) investigates the potential of an amplification function in each unit-cell, but this investigation is limited to simulated results. In these simulations, hypothetical negative resistances are modelling a reflection coefficient of the reflector with a magnitude higher than 1 ($|S_{11}| > 1$). The three systems illustrated in Figure 2.3 are compared in (Hosseini & Rahmat-Samii, 2015). This comparison shows that system [C.], i.e., a tapered $|S_{11}|$ as opposed to a constant $|S_{11}|$ in systems [A.] and [B.], compensates

the feed taper yielding improved $\eta_i$, thus improved $\eta_a$. Moreover, the antenna gain of system [C.] is significantly higher than system [A.] (i.e., a non-amplifying system).

The work in (Hosseini & Rahmat-Samii, 2015) is limited to simulations and does not evaluate the impact of using a gain stage in each unit-cell on other key characteristics, e.g., global system energy efficiency, power handling, and maximal delivered linear power.

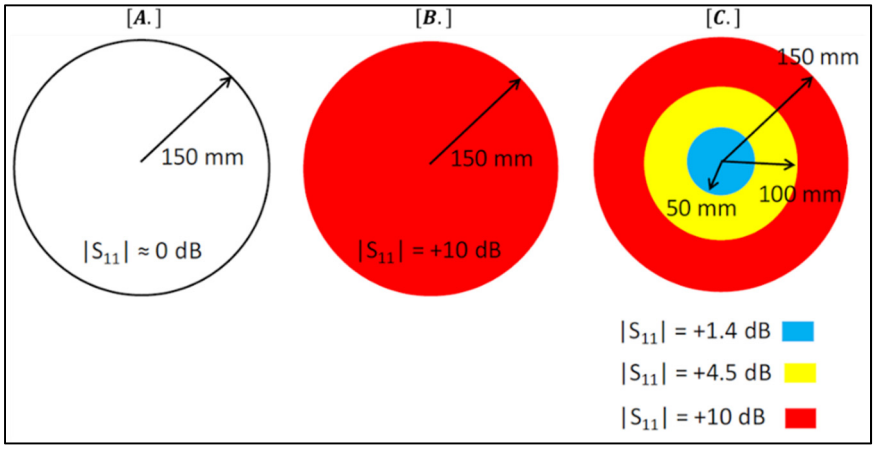



Figure 2.3 Three RA systems with different |S11| profiles
Taken from Hosseini & Rahmat-Samii (2015)

### 2.1.3 RRTA including amplifying function while controlling the phase and magnitude

It is worth mentioning that only a few reported works on spatially-fed antenna systems – one is described next – include simultaneously electronic control functions of the phase and amplitude with an amplifying function.

In the RRA unit-cell proposed in (Cabria, García, Gutiérrez-Ríos, Tazón, & Vassal'lo, 2009) presented in Figure 2.4, a dual-mixer approach controls separately the amplitude of two orthogonal vectors, resulting in a summed vector that is controllable in phase and amplitude. Also, amplification functions are added upstream and downstream (not shown in Figure 2.4) of this mixer-based control circuit.

Unfortunately, the benefits of using an amplifying solution are not discussed in (Cabria et al., 2009). Moreover, the results are demonstrated at low power operations. Therefore, the linearity performances and power handling capabilities of this amplifying mixer-based approach are not provided. Besides, the many active RF devices involved in this solution suggests it is not best suited for highly reliable antenna systems.

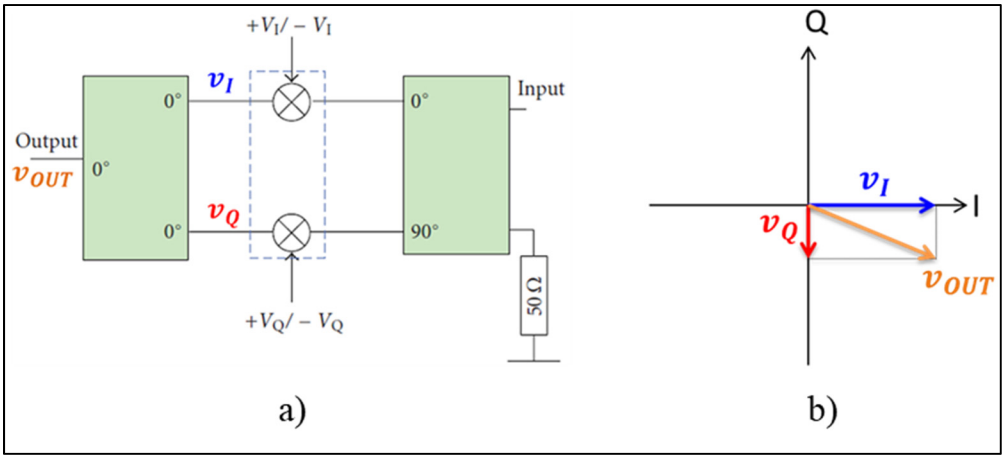



Figure 2.4 An RRA based on an IQ modulator architecture to control the amplitude and the phase (Cabria et al., 2009). a) Circuit schematic taken from Cabria et al. (2009)) b) Vector summation on the IQ plane Adapted from Cabria et al. (2009)

## 2.2 Literature review: Varactor-based phase shifter solutions

The reported varactor-based phase shifter solutions described in this section show that solid-state varactor-based architectures are suitable for most of the required characteristics listed in Table 1.4. However, most reported varactor-based solutions in the literature do not answer the need for good linearity performances at large power levels, an important aspect that is dealt with in this research work.

In the varactor-based reflective-type phase shifter (V-B RTPS) architecture depicted in Figure 2.5, the coupler, typically a 3dB hybrid coupler, equally divides the incoming power (red arrows) towards the reflective loads. Varactor-based tunable impedance networks (TINs) within these loads enable reconfigurability of the reflective loads' input impedance ($Z_{RL}$), which translates into the tuning of the phase of the reflected signals (blue arrows) that are recombined at the output port $RF_{OUT}$ of the V-B RTPS network.

To the best of the author's knowledge, the $FoM_{PS} \approx 247 \circ/dB$ ($FoM_{PS}$ is defined in section 1.5.1) demonstrated in (Burdin, Iskandar, Podevin, & Ferrari, 2015) is among the highest reported for a varactor-based phase shifter network while achieving $\Delta\phi_{MAX} > 360°$. This high $FoM_{PS}$ is made possible by reducing the V-B RTPS IL by using the hybrid coupler as an impedance transformer to optimize the impedance seen by the reflective loads ($Z_T$ in Figure 2.5). Moreover, optimizing the value of $Z_T$ also allows minimizing the ΔIL of the V-B RTPS network, as demonstrated in (Lin, Chang & Hsiao, 2008; Singh & Mandal, 2019).

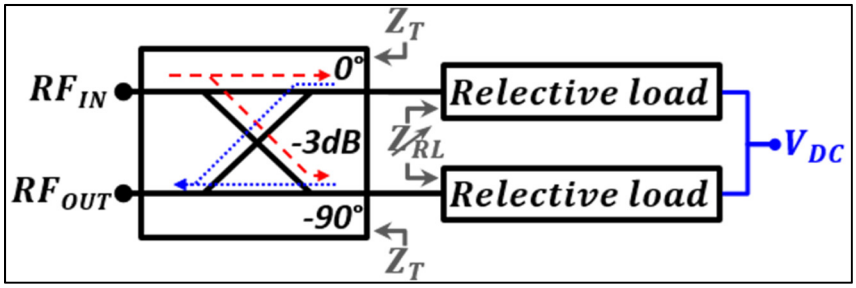



Figure 2.5 State-of-the-art V-B RTPS architecture

The work in (Burdin et al., 2015) also demonstrates it is possible to reduce the circuit area by proposing a reflective load network designed with reduced electrical length transmission lines relative to the typically used quarter wavelength. However, the proposed reflective-load network in (Burdin et al., 2015) uses three TINs, thus is not best suited for high-reliability applications.

Published varactor-based solutions (e.g., (Burdin et al., 2015; Lin et al., 2008; Singh & Mandal, 2019)) show that solid-state varactor-based architectures are suitable for the characteristics 2 to 6 identified in Table 1.4. However, most reported varactor-based solutions implement the TIN with a single varactor topology (e.g., (Burdin et al., 2015; Liu, Zheng, Pan, Li, & Long, 2017)) yielding high level of distortions at large power levels.

Some published phase shifters aim at achieving high linearity performances with multi-varactor topology (e.g., (Kim, Qureshi, Buisman, Larson, & de Vreede, 2008; Qureshi et al., 2007). However, it is demonstrated in CHAPTER 3, with the analysis of a multi-stack varactor topology only (i.e., a TIN), that such a topology suffers from severe linearity degradation when there are significant parasitics surrounding the diodes. Moreover, the $\Delta\phi_{MAX}$ reported in (Kim et al., 2008; Qureshi et al., 2007) are much lower than 360°, a key characteristic for the system under investigation in this work. Besides, (Kim et al., 2008; Qureshi et al., 2007) use significantly more TINs than the proposed solutions in this thesis, which is detrimental to reliability.

Consequently, in part explained by the complexity of realizing highly linear TINs, the prior-art of varactor-based phase shifter fails to fulfill altogether the required characteristics listed in Table 1.4.

## 2.3 Literature review: Highly linear varactor-based tunable impedance network

With regard to improving the linearity and power handling capability of varactor-based tunable impedance networks (TINs), (Meyer & Stephens, 1975) introduces the concept of stacking two identical varactors of size $D_A$ in an anti-series configuration by proposing the abrupt varactor-based topology in Figure 2.6a. This topology significantly improves circuit linearity by enabling a distortion-cancellation mechanism. Moreover, such series stacking of two varactors inherently enhances the power handling capability by sharing the RF voltage between two varactors. In the work of (Buisman et al., 2005), the network's capacitance tuning range is broadened by using hyper-abrupt varactors, while the distortion-cancellation mechanism is

made possible by using the anti-series/anti-parallel topology in Figure 2.6b and by optimizing the ratio ($s$) between the diode sizes, hence the ratio between their junction capacitances.

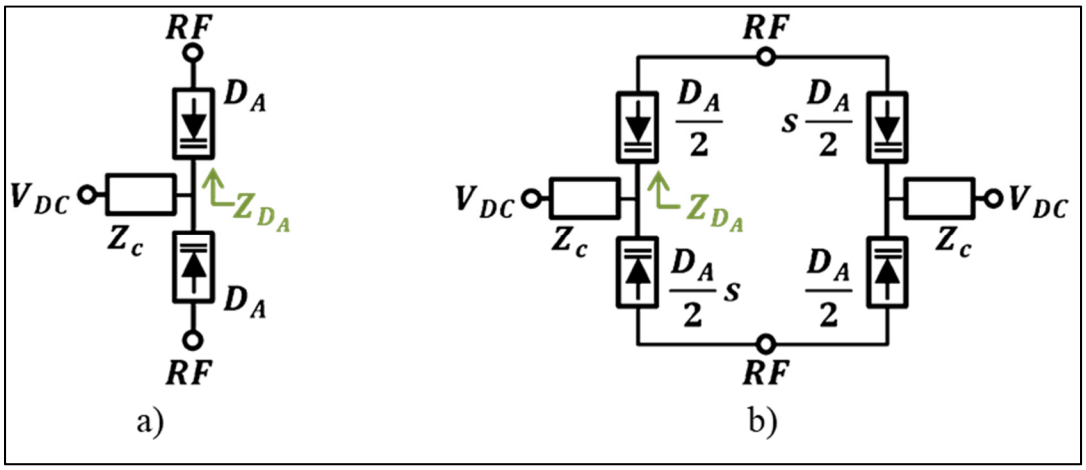



Figure 2.6 State-of-the-art highly linear varactor-based controllable impedance network where $D_A$ is the varactor size. a) Matched anti-series-only topology b) Unmatched anti-series/anti-parallel topology

In the topologies proposed in (Buisman et al., 2005; Meyer & Stephens, 1975), the effectiveness of the distortion-cancellation mechanism relies on a center-tap impedance ($Z_C$ in Figure 2.6), typically implemented with a resistor, higher than the diode's AC impedance ($Z_{D_A}$ in Figure 2.6) for all frequency components (i.e., $Z_C \gg Z_{D_A}$ at all frequencies). The key factor dictating the required value of $Z_C$ is the high value of $Z_{D_A}$ at baseband frequencies, which are at significantly lower frequencies than the fundamental and harmonic frequencies ($f_0, 2f_0, 3f_0, \cdots$). Since the condition on $Z_C$ is alleviated as the tone spacing is widened, (Buisman et al., 2005; Meyer & Stephens, 1975) topologies suit large-bandwidth RF applications and are referred as "wide tone-spacing varactor stacks" in the literature. On the other hand, for near-zero tone spacing (or modulation schemes including very low frequencies), the required infinitely high value of $Z_C$ to comply with $Z_C \gg Z_{D_A}$ at baseband frequency is an important limiting factor, particularly for MMIC-only designs. With regard to increasing the value of $Z_C$ at low frequencies, (Buisman et al., 2005) implements $Z_C$ using an anti-parallel diodes network which maintains the effectiveness of the distortion-cancellation mechanism for a simulated tone spacing as low as ~100Hz. However, because of the possible

current leakages through the diode-based $Z_C$ network, yielding degraded linearity performances, this latter solution adds significant design complexities.

Whereas (Buisman et al., 2005; Meyer & Stephens, 1975) require high $Z_C$ values at tone spacing near 0Hz, the topologies proposed in (Huang et al., 2008b; Huang et al., 2010) require $Z_C \ll Z_{D_A}$ at baseband frequencies and $Z_C \gg Z_{D_A}$ at the fundamental and harmonic frequencies. These center-tap impedance conditions, which are fulfilled by implementing $Z_C$ with an inductance, makes (Huang et al., 2008b; Huang et al., 2010) topologies best suited for modulated signals including content near 0Hz. This shift on the conditions on $Z_C$ is made possible by designing the topology in Figure 2.6a using exponentially doped diodes produced in Silicon on Glass (SoG) (Huang et al., 2008b) and Gallium arsenide (GaAs) Monolithic microwave integrated circuit (MMIC) (Huang et al., 2010) processes. However, the condition $Z_C \ll Z_{D_A}$ at baseband frequencies restricts (Huang et al., 2008b; Huang et al., 2010) topologies to smaller bandwidth applications (e.g., (Huang et al., 2008b) is limited to a tone spacing of ~10MHz).

The work in (Huang et al., 2009) extends the use of exponentially doped diode technologies to a larger variety of RF applications by proposing a wide tone-spacing varactor stack based on the topology in Figure 2.6b. Note that this work is restricted by the same center-tap conditions as in (Buisman et al., 2005; Meyer & Stephens, 1975).

References (Buisman et al., 2007; Huang et al., 2008a) further improve the power handling capability of anti-series topologies by sharing the RF voltage between an increased number of varactors. This is made possible by using multiple series-stacking of the topologies proposed in (Buisman et al., 2005; Meyer & Stephens, 1975). The drawbacks with the topologies in (Buisman et al., 2007; Huang et al., 2008a) are the use of an increased number of components or chip area, and a lower Q factor for the same targeted capacitance value. The works in (Amirpour, Schwantuschke, Brueckner, Quay, & Ambacher, 2019; (Lu, Wang, Gu, Asbeck, & Yu, 2012) also improve power capability by implementing the topology of Figure 2.6a in a gallium nitride (GaN) technology with a focus on the Q factor.

The key characteristics associated to the above works and that are demonstrated in the gigahertz frequency range (≥1GHz) are summarized in Table 2.1 and compared with our work, while taking into consideration the important aspect of L-C parasitics.

All the solutions in Table 2.1 are demonstrated at ~2.15GHz or lower and are implemented either on SoG MMIC (Nanver et al., 2009), GaAs MMIC or GaN MMIC technologies. The limited frequency of operation and MMIC integration aspects in these works are of particular importance. In these conditions, the ideal distortion-free behavior of anti-series topologies is made possible, in part because the effects of parasitics surrounding the diodes are negligible. In fact, the effects of parasitics on the linearity of anti-series varactor networks, to our knowledge, have never been reported.

The discrete-package varactors approach in this work translates into added constraints due to larger parasitics compared to MMIC technologies. As demonstrated in this work, the parasitics in discrete designs at 3.6GHz degrade significantly the linearity of anti-series varactor networks.

Table 2.1 Comparison of existing varactor-based anti-series topologies in the context of significant L-C parasitics

| Ref | Technology / Doping / Topology | Demonstrated with L-C parasitics | $f_0$ (GHz) | Diode count | Linearity/Power at min and max demonstrated TS | | | | Key aspects not demonstrated |
|---|---|---|---|---|---|---|---|---|---|
| | | | | | Measurement type | Linearity level | Power or Voltage | TS (Hz) | |
| Buisman & al., 2005 | SoG MMIC / H-A / AS-AP (Fig.1b in Ref.) | NO✕ | 2 | 4✕ | 2-tone IMD3 | ~-60dBc | 3V | 100M | - Performances for a range of bias<br>- Performances for a range of TS<br>- Experimental linearity performances |
| Huang & al., 2008b | SoG MMIC / EXP / AS Only | NO✕ | 2.14 | 2 | 2-tone IMD3 | ~-63dBc | 16dBm | 10k✕ | - Performances for a range of bias<br>- Linearity with complex modulation |
| | | | | | | ~-33dBc✕ | | 99M | |
| Huang & al., 2010 | GaAs MMIC / EXP / AS Only | NO✕ | 2 | 2 | 2-tone IMD3 | ~-59dBc | 24dBm | 2k | - Performances for a range of bias<br>- Linearity with complex modulation |
| | | | | | | ~-40dBc✕ | | 100M | |
| Huang et al., 2009 | SoG MMIC / EXP / AS-AP / (Fig.3a-b in Ref.) | NO✕ | 2 | 4✕ | 2-tone IMD3 | ~-35dBc✕ | 15dBm | 5k | - Performances for a range of bias<br>- Linearity with complex modulation |
| | | | | | | ~-94dBc | | 80M | |
| Buisman et al., 2007 | SoG MMIC / A / M-AS Only (Fig.3 in Ref) | NO✕ | 2.14 | 4✕ | 2-tone IMD3 | ~-97dBc | 21dBm | 10k✕ | - Performances for a range of bias<br>- Linearity with complex modulation |
| | | | | | | ~-86dBc | | 100M | |
| Huang & al., 2008a | SoG MMIC / EXP / M-AS Only | NO✕ | 2.14 | 4✕ | 2-tone IMD3 | ~-76dBc | 26dBm | 10k✕ | - Performances for a range of bias<br>- Linearity with complex modulation |
| | | | | | | ~-47dBc | | 80M | |
| Lu et &., 2012 | GaN MMIC / A / AS Only | NO✕ | 1 | 2 | 2-tone IMD3 | ~-56dBc | 27dBm | 15M | - Performances for a range of bias<br>- Performances for a range of TS<br>- Linearity with complex modulation |
| Amirpour & al., 2019 | GaN MMIC / A / AS Only | NO✕ | 1-2 | 2 | CW✕ (3rd harm.) | Harmonics only ✕ | | N/A | - 2-tone linearity performances<br>- Experimental linearity performances |
| This work | Discrete / Using AS Only with H-A* | YES* (1st to demonstrate) | 3.6* | 2* | 2-tone IMD3 | -63dBc* | 10dBm | 1k | **Demonstrated in this work** |
| | | | | | | -62dBc | | 120M | - Evaluated over full bias range<br>- Linearity with complex modulation |
| | | | | | | -54dBc | 18dBm | 10M | |
| | | | | | 16QAM* | -56dBc | 18dBm | 10M | |

| Acronyms | | Symbols for a qualitative comparison |
|---|---|---|
| A – Abrupt doping profile | $f_0$ – Frequency of operation | ✕ Disadvantage with respect to this work |
| ACPR – Adjacent channel power ratio | GaAs – Gallium arsenide | * Key improvements or new metrics in this work |
| AS Only – Anti-series-only topology | H-A – Hyper-abrupt doping profile | ~ Data estimated from a graphic |
| AS-AP – Anti-series/anti-parallel topology | M-AS Only – Multi-stack of AS Only | |
| BW – Bandwidth | Ref. – Refer to the reference of same row | |
| CW – Continuous wave | SoG – Silicon on glass | |
| EXP – Exponential doping profile | TS – Tone spacing | |

## 2.4 Innovative concepts proposed in this work to circumvent the shortcomings and limitations of the current state-of-the-art

This section presents the innovative concepts proposed in this work and that circumvent the shortcomings and limitations of the state-of-the-art, as identified in the literature review of Section 2.1 to Section 2.3. These shortcomings include i) inefficiency of varactor-based TINs and varactor-based controllable networks to achieve high linearity performances at large power levels in the presence of significant parasitics, ii) poor energy efficiency of amplifying RRTA solutions, and iii) low reliability of the circuit techniques achieving simultaneous reconfigurability of the magnitude and the phase.

In addition to circumventing these shortcomings, the innovative concepts presented in this section give opportunities for several novel system-level features, and will be analyzed in CHAPTER 6.

### 2.4.1 Varactor-based tunable impedance network with improved linearity in the presence of significant parasitics

The work presented in CHAPTER 3 investigates the linearity performance optimization of the varactor-based discrete design needed for the controllable network in the system illustrated in Figure 1.4. The analyses presented make use of the electrical characteristics of an off-the-shelf GaAs flip-chip varactor device only as numerical example and to allow experimental validation with a practical design using the same varactor. However, the proposed linearity improvement technique is not limited to this specific varactor and may be implemented using other hyper-abrupt varactors in flip-chip and discrete packages.

It is demonstrated, using multi-tone-based equations, that the linearity performance enhancement expected from the distortion-cancellation mechanism inherent to the anti-series networks in Figure 2.6, is severely degraded by the passive parasitics surrounding the varactors. Note that recent articles (e.g., (Anjos, Schreurs, Vandenbosch, & Geurts, 2020; Barrak et al., 2018; Moloudi & Eslamipour, 2021)) employ varactor-based anti-series networks

in various RF systems, which highlights their importance. However, they do not address the linearity degradation mechanism due to L-C parasitics in anti-series networks.

Moreover, it is shown that optimizing the ratio of diode sizes is insufficient to circumvent the linearity degradation due to parasitics.

1) Understanding the degradation of this distortion-cancellation mechanism in an anti-series-only network is the basis for the introduction of a modified anti-series network in CHAPTER 3. The complete hyper-abrupt varactor-based circuit topology pursued here yields many key improvements over the works listed in Table 2.1 and, to our knowledge, over all reported varactor-based anti-series topologies in the literature.
2) It enhances the linearity performances despite the presence of parasitics surrounding the diodes. This allows operating varactor topologies at higher frequencies and is highlighted in Table 2.1 by $f_0 = 3.6GHz$ in our work using discrete components as opposed to the reported $f_0 \leq 2.14GHz$ in previous works based on MMIC approaches.
3) It offers an alternative to the anti-series/anti-parallel topology (Figure 2.6b) with the benefit of reducing by 2 the number of diodes. This is relevant in regards to cost and size for high volume products (e.g., wireless communication systems), and also for high-reliability systems (e.g., on-board satellite RF circuitry as in Figure 1.4).
4) It circumvents the linearity degradation that stems from the inductive effect of series transmission lines between the varactor-based network and external circuits. This facilitates the implementation of anti-series networks in various RF systems (e.g., phase-shifters, tunable filters, configurable amplifiers, etc.).

### 2.4.2 A 360° V-B RTPS with improved linearity with low and constant insertion loss

The complete phase shifter solution proposed in CHAPTER 4 builds on the TIN introduced in CHAPTER 3 to address the linearity shortcoming in most reported V-B RTPS (e.g., (Burdin et al., 2015; Kim et al., 2008; Liu et al., 2017; Qureshi et al., 2007)) while achieving a

$\Delta\phi_{MAX} > 360°$, a low $IL$, a small $\Delta IL$, and minimizing the number of TINs, which is favorable to cost, size and reliability.

### 2.4.3 Novel amplifying RTA unit-cell for improved system-level performances

CHAPTER 6 proposes a varactor-based amplifying RTA unit-cell including compact circuit techniques to simultaneously control the phase and magnitude while answering the need for high linearity performances at transmitters' power level while minimizing the DC consumption. Therefore, it constitutes a significant improvement of the state-of-the-art. The novel characteristics of the proposed RTA unit-cell are:

1) amplification capabilities to compensate the IL of the phase shifter and for high antenna gain,
2) linear operation at large power levels for telecommunication applications,
3) simultaneous dynamic phase and magnitude control capabilities allowing many novel features in advanced systems,
4) a novel circuit technique to control the magnitude is implemented as a part of the gain stage for maximum compactness and minimum components usage, and
5) minimum DC consumption for maximum energy efficiency and minimum heat dissipation.

These innovative characteristics are realized by using a unit-cell architecture built with two rectangular patch antennas, a highly linear and low loss 360° V-B RTPS proposed in CHAPTER 4, and a novel 10dB controllable gain amplifier stage presented in CHAPTER 5.

CHAPTER 6 also investigates potential system-level improvements using systems based on *measured* performances to support the proposed RTA unit-cell novelty. The analyzed system-level improvements are i) maximization of the linear power level of the transmitted scattered wave, ii) compensation of the phase shifter ΔIL for better control of the scattered field, iii) enhancement of the antenna efficiency, and iv) reduction of the negative impact of power losses (e.g., spillover) on the global energy efficiency.

### 2.4.4 Summary and organization of the innovative concepts proposed in this research work

Figure 2.7 illustrates how the different innovative concepts are linked together and which chapter they are associated with, helping to understand the flow of ideas for the remainder of this thesis.

The TIN presented in CHAPTER 3 is implemented into the two controllable networks proposed in CHAPTER 4 and CHAPTER 5. These two controllable networks are the key blocks of the RTA unit-cell presented in CHAPTER 6, the chapter that also analyzes the impact of the RTA unit-cell on the performances at a system level.

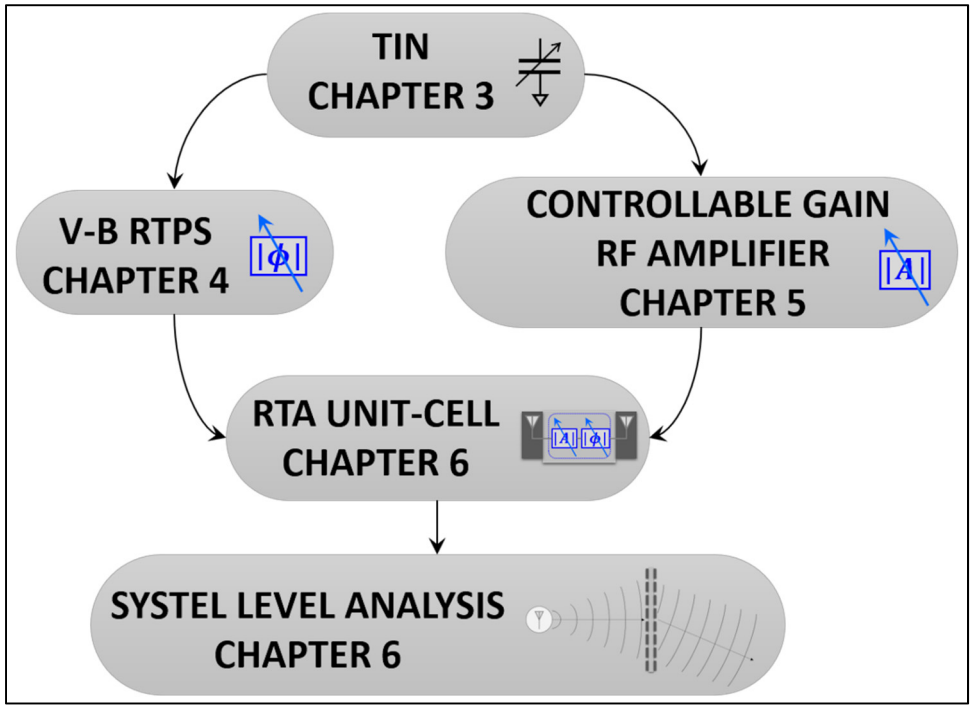



Figure 2.7 Schematic of the organization of the innovative concepts proposed in this research work

# CHAPTER 3

# ANTI-SERIES VARACTOR NETWORK WITH IMPROVED LINEARITY PERFORMANCES IN THE PRESENCE OF INDUCTIVE AND CAPACITIVE PARASITICS

This chapter, which is related to the innovative concept of Section 2.4.1, is organized as follows. Section 3.1 begins with a summary of the theory behind the state-of-the-art anti-series topology. An analytical study is then presented in the same Section 3.1 to explain the mechanism of linearity degradation in an anti-series topology due to capacitive and inductive parasitics. Section 3.2 presents the modified anti-series network that stems from this research work and that allows improving the linearity performances despite the presence of parasitics, followed by the complete varactor-based topology that is introduced in this work. Formulations associated with this modified network and that allow theoretically predicting the possible linearity improvement, are also given. Section 3.3 presents experimental results validating the linearity enhancement achieved with the complete varactor-based topology proposed in this paper, under 2-tone and 16QAM excitation schemes.

## 3.1 Nonlinearities in anti-series varactor in the presence of parasitic elements

Varactor models commonly used by manufacturers include a series parasitic inductance ($L_S$) and a parallel parasitic capacitance ($C_P$). These components were not included in the state-of-the-art formulations presented in (Buisman et al., 2005; Buisman et al., 2007; Huang, Buisman, Zampardi, Larson, & de Vreede, 2012; Huang et al., 2008b; Meyer & Stephens, 1975) to predict the nonlinearities generated by anti-series varactor networks. This constitutes a limitation under certain conditions.

Section 3.1.1 summarizes the theory in (Buisman et al., 2005) predicting the nonlinearities generated by parasitic-free anti-series varactor networks. Section 3.1.2 then extends this theory by introducing new formulations to describe the generation of additional nonlinearities in the presence of significant $C_P$ and $L_S$.

### 3.1.1 Nonlinearities in parasitic-free anti-series topology

In this subsection, we analyze the distortion mechanism in the parasitic-free anti-series-only circuits of (Buisman et al., 2005; Huang et al., 2009). The analysis builds on the formulations presented in (Buisman et al., 2005), to further highlight the nonlinear current generation mechanism for better clarity. This is necessary since frequent references to these currents will be made throughout the remainder of this paper and will be used for various numerical calculations.

#### 3.1.1.1 Assumptions made for analysis

It is worthwhile to explicitly mention the assumptions considered in the theory proposed in (Buisman et al., 2005) and in this chapter.

First, the analyses in (Buisman et al., 2005) as well as in this paper are limited to a quasi-static representation of the weakly nonlinear function that describes the capacitance (in Farads) vs voltage: $C(V) = \frac{dQ}{dV}$ (Maas, 2003; Meyer & Stephens, 1975). This allows using a power series with scalar coefficients to define a nonlinear capacitance function $C(v_S)$ (Maas, 2003; Meyer & Stephens, 1975) that represents the variation of the capacitance value with the instantaneous voltage defined by a time-dependent AC signal $v_s(t)$ (without DC) applied to it. For a given controllable nonlinear capacitance, any new DC bias voltage value or any increase in the amplitude of $v_s(t)$ requires a different $C(v_S)$ nonlinear function. Note that quasi-static representations of weakly non-linear capacitances have been demonstrated to properly predict the nonlinearities at large signal power levels (e.g., (Buisman, Huang, Zampardi, & de Vreede, 2012)).

Second, the nonlinear capacitance $C(v_S)$ is analyzed using the circuit in Figure 3.1 where the ideal $0\Omega$ voltage source is given by (3.1). It is a two equal-tone signal of amplitude A and at angular frequencies $\omega_1$ and $\omega_2$.

$$v_S(t) = A \cdot \cos(\omega_1 t) + A \cdot cos(\omega_2 t) \tag{3.1}$$

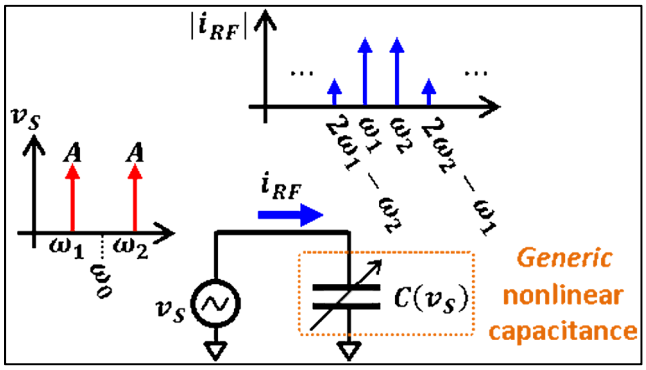



Figure 3.1 Circuit to analyze the nonlinear RF current ($i_{RF}$) generated by a nonlinear capacitance ($C(v_S)$)

In Figure 3.1, $v_S = 0V$ at all frequencies other than $\omega_1$ and $\omega_2$. In this ideal context, the only contributor to harmonics and intermodulation distortion (IMD) products in the RF current $i_{RF}$ is the intrinsic nonlinear behavior of the capacitance $C(v_S)$ as no other component influences the distortions in $i_{RF}$. In a practical implementation, the non-zero external impedances have an important effect on circuit linearity, an aspect that will be dealt with in Section 3.2.2.

### 3.1.1.2 Nonlinearities of a generic nonlinear capacitance

This subsection analyzes the nonlinear behavior of a *generic* nonlinear capacitance $C(v_S)$. In subsequent subsections, this generic $C(v_S)$ is appropriately substituted by specific varactor-based topologies under study. This allows analyzing the nonlinear behavior associated to a specific topology. The nonlinear capacitance $C(v_S)$ in Figure 3.1 is modeled with the power series given by (3.2):

$$C(v_S) = C_0 + C_1 \cdot v_S + C_2 \cdot [v_S]^2 + \cdots + C_n[v_S]^n \tag{3.2}$$

As stated earlier, a new set of scalar coefficients $C_0$ to $C_n$ is required with any new DC bias voltage or any increase in the amplitude of $v_s(t)$.

The nonlinear behavior of $C(v_S)$ within the circuit in Figure 3.1 is analyzed using nonlinearities of the RF current $i_{RF}$, which is calculated using (3.3) (Maas, 2003; Meyer & Stephens, 1975).

$$i_{RF}(t) = C(v_S) \cdot \frac{d[v_s(t)]}{dt} \tag{3.3}$$

Substituting $C(v_s)$ given by (3.2) in (3.3) gives (3.4) (Maas, 2003).

$$i_{RF}(t) = [C_0 + C_1 \cdot v_S + C_2 \cdot [v_S]^2 + \cdots] \cdot \frac{d[v_s(t)]}{dt} \tag{3.4}$$

By substituting $v_S(t)$ with its value in (3.1), (3.4) becomes (3.5).

$$i_{RF}(t) = \begin{bmatrix} C_0 + \\ C_1 \cdot [A \cdot \cos(\omega_1 t) + A \cdot cos(\omega_2 t)] + \\ C_2 \cdot [A \cdot \cos(\omega_1 t) + A \cdot cos(\omega_2 t)]^2 + \cdots \end{bmatrix} \cdot \frac{d[A \cdot \cos(\omega_1 t) + A \cdot cos(\omega_2 t)]}{dt} \tag{3.5}$$

A 3rd order expansion of (3.5) allows associating each capacitor coefficients ($C_0$, $C_1$, and $C_2$ of the power series in (3.2)) with the various frequency components in $i_{RF}$ generated by $C(v_S)$. While higher-order contributors greater than the 3rd order are present in (3.5), their values are not considered in this paper for compactness of the equations. Besides, such higher-order terms have a significantly smaller effect on the overall circuit linearity.

After a 3rd order expansion of (3.5), the $IMD_{2f_2-f_1}$ levels in $i_{RF}$, which stem from the product of the 2nd degree term and the derivative term, are found to be:

$$IMD_{2f_2-f_1} = \frac{i_{RF}(2\omega_2 - \omega_1)}{i_{RF}(\omega_2)} = \frac{A^2 C_2 (2\omega_2 - \omega_1)}{\omega_2 (3A^2 C_2 + 4C_0)} \tag{3.6}$$

As can be seen in the numerator of (3.6), $C_2$ may be used to reduce or cancel the distortion at $2f_2 - f_1$ in a varactor-based controllable impedance network. The remainder of the analyses presented in this paper discusses various methods of minimizing the coefficient $C_2$ associated to tunable-capacitor elements that are built in the form of varactor-based networks. This will allow the study of $IMD_{2f_2-f_1}$ level reduction, depending on the parasitics included in the different embodiments that will be presented.

#### 3.1.1.3 Expression for selected off-the-shelf varactor capacitance

For the targeted application illustrated in Figure 1.4, this work uses the off-the-shelf GaAs flip-chip varactor MA46H120 (MACOM, 2020) because of its wide capacitance tuning range and its low series parasitic resistance ($R_S$). Equation (3.7) is the expression of the nonlinear capacitance to voltage relationship given by the manufacturer and widely used in the literature. In (3.7), $C_{j0}$ is the zero-bias junction capacitance, $V_{DC}$ is the bias voltage of the varactor, $v$ is the RF voltage across the varactor, $V_J$ is the junction potential, and $M$ is the grading coefficient.

$$C(V_{DC}, v) = \frac{C_{j0}}{\left(1 + \frac{V_{DC} + v}{V_J}\right)^M} \tag{3.7}$$

The coefficients $C_n = C_0,\ C_1,\ C_2, \cdots$ are extracted by applying a 3rd order Taylor series expansion to (3.7) as a function of $v$ to reformulate (3.7) to the power series given by (3.2). The resulting $C_0$, $C_1$, and $C_2$ are given by (3.8) (Meyer & Stephens, 1975). This expansion will be used in later sections.

$$C_0 = \frac{C_{j0}}{\left(\frac{V_j + V_{DC}}{V_J}\right)^M}$$
$$C_1 = -C_0 \frac{M}{(V_J + V_{DC})} \tag{3.8}$$
$$C_2 = \frac{1}{2} C_0 \frac{M(M+1)}{(V_J + V_{DC})^2}$$

#### 3.1.1.4 Formulation for parasitic-free anti-series nonlinear

This subsection analyzes the nonlinear behavior of the parasitic-free anti-series varactor topology shown in Figure 3.2.

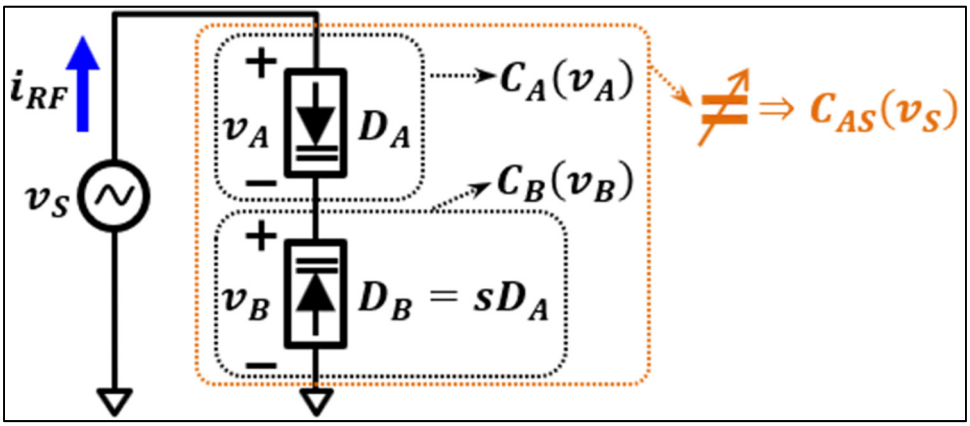



Figure 3.2 Circuit to analyze $i_{RF}$ generated by the parasitic-free anti-series topology. As in Figure 2.6, varactors are biased at $V_{DC}$ through a high impedance network $Z_C$ (not shown for simplification)

The equivalent capacitance $C_{AS}(v_S)$ in Figure 3.2 is a stack of two nonlinear capacitances $C_A(v_A)$ and $C_B(v_B)$ with $v_S = v_A + v_B$, where $v_A$ and $v_B$ are the AC voltages across the capacitances $C_A$ and $C_B$, respectively. The only circuit elements present in $C_A(v_A)$ and $C_B(v_B)$ are the two varactors which are defined, respectively, by their different sizes $D_A$ and $D_B$. Also, $D_A$ and $D_B$ are related through the ratio $s$ of their sizes, i.e., $D_B = sD_A$. $C_A(v_A)$ and $C_B(v_B)$ may be expressed with the power series given in (3.9) where $C_{An} = C_{A0,}C_{A1}, C_{A2}$ and

$C_{Bn} = C_{B0,}C_{B1}, C_{B2}$ are dependent on the nonlinearities associated to $C_A(v_A)$ and $C_B(v_B)$, respectively.

$$C_A(v_A) = C_{A0} + C_{A1} \cdot v_A + C_{A2} \cdot v_A^2 + \cdots$$
$$C_B(v_B) = C_{B0} - C_{B1} \cdot v_B + C_{B2} \cdot v_B^2 + \cdots$$

With $C_{A0}$, $C_{B0}$ determined from (3.7) as:

$$C_{A0} = C_0 \qquad C_{B0} = sC_0$$
$$C_{A1} = C_1 \qquad C_{B1} = sC_1$$
$$C_{A2} = C_2 \qquad C_{B2} = sC_2 \tag{3.9}$$

The varactor associated to $C_A$ is modeled with (3.7) and the coefficients $C_{An} = C_{A0}, C_{A1}, C_{A2}, \cdots$ are obtained with a Taylor series as in (3.8). The coefficients $C_{Bn}$, assuming the same type of varactor, are subsequently derived from $C_{An}$ considering the scaling relationship $D_B = sD_A$ . The values of $C_{An}$ and $C_{Bn}$ are given in (3.9).

Starting from the values of $C_{An}$ and $C_{Bn}$ in (3.9), the power series $C_{AS}(v_S)$ that describes the intrinsic nonlinear behavior of the topology in Figure 3.2 (in orange) is formulated with (3.10) (equivalent to (3) to (5) in (Buisman et al., 2005). ANNEX II details the derivation of the coefficients $C_{ASn} = C_{AS0}, C_{AS1}, C_{AS2}$ in (3.10). Note that $C_0$ is left unexpanded in (3.10) for conciseness.

$$C_{AS}(v_S) = C_{AS0} + C_{AS1} \cdot v_S + C_{AS2} \cdot v_S^2 + \cdots$$

where

$$C_{AS0} = \left[\frac{s}{s+1}\right] C_0$$

$$C_{AS1} = -\left[\frac{s(s-1)}{(s+1)^2}\right] C_0 \frac{M}{(V_J + V_{DC})} \tag{3.10}$$

$$C_{AS2} = \left[\frac{1}{2}\frac{\alpha_2}{(s+1)^3}\right] C_0 \frac{M}{(V_J + V_{DC})^2}$$

with

$$\alpha_2 = s\big((M+1)s^2 + (-4M-1)s + M + 1\big)$$

Equation (3.10) allows computing the resulting $i_{RF}\ IMD_{2f_2-f_1}$ levels in the circuit of Figure 3.2. Equation (3.6) is used for this computation by substituting the coefficients $C_n = C_0, C_1, C_2$ with $C_{ASn} = C_{AS0}, C_{AS1}, C_{AS2}$.

In (Buisman et al., 2005), the use of hyper-abrupt ($M \geq 1$) varactors is made possible by introducing the diode-size scaling parameter $s$ (unmatched varactors) which allows designing for $\alpha_2 = 0$ in (3.10) to cancel $C_{AS2}$. By associating $C_{AS2}$ to $C_2$ in the numerator of (3.6), it can be seen that this results in lower 3rd order distortions. Designing for $\alpha_2 = 0$ is achieved by solving for the required value of the diode-size ratio ($s$) with (3.11), as a function of the value $M$ dictated by the choice of varactor.

$$s_{IDEAL} = \frac{1}{2} \cdot \frac{4M + 1 + \sqrt{12M^2 - 3}}{(M+1)} \tag{3.11}$$

However, unlike the technique in (Meyer & Stephens, 1975) which uses matched ($s = 1$) abrupt ($M = 0.5$) anti-series varactors and where *all* distortion components (i.e., related to $C_{AS1}, C_{AS2}, C_{AS3}$, etc.) are canceled, the technique using unmatched-size and hyper-abrupt varactors in (Buisman et al., 2005) does *not* allow for a cancellation of all even-order and all higher odd-order (greater than 3rd order) distortion components. Moreover, the very presence

of even-order distortion components in the varactor currents ($i_{RF}$ in Figure 3.2) yields degraded linearity performances due to a secondary mixing mechanism caused by the presence of a non-zero source impedance connected to the anti-series network. In (Buisman et al., 2005), this problem is overcome by introducing the anti-series/anti-parallel network (Figure 2.6b) to cancel all even-order as well as the 3rd order nonlinearities.

However, in practical implementations relying on hyper-abrupt varactor-based anti-series-*only* topologies, the non-cancellation of even-order distortion components constitutes a limiting factor. In that regard, a solution to minimize the effects of the secondary mixing mechanism in the presence of a non-zero source impedance, when using hyper-abrupt anti-series-*only* topologies has not been proposed. This work proposes a technique to address this in Section 3.2.2.

### 3.1.2 Nonlinearities of anti-series topology in the presence of significant parasitics

The formulations in the literature so far (e.g., (Buisman et al., 2005; Huang et al., 2009)) are limited to parasitic-free varactors, and to the best of the authors' knowledge, the negative impact of parasitic capacitances and inductances on linearity in anti-series varactor topologies has never been reported.

In the Subsection 3.1.2.1, we demonstrate the detrimental effect of parallel parasitic capacitances in the distortion mechanism of unmatched hyper-abrupt varactor-based anti-series topologies by extending the preceding equations. Moreover, in Subsection 3.1.2.2, the negative impact of series inductances on linearity is analyzed.

Figure 3.3 is the model of the GaAs flip-chip varactor MA46H120 considered in this paper (MACOM, 2020). This model includes three parasitic elements: a series resistance ($R_S$), a parallel linear capacitance ($C_P$), and a series linear inductance ($L_S$). The parameters listed in Table 3.1 MA46H120 varactor parameters are considered in the analyses that follow. Note that

the parasitic capacitance $C_P$ is expressed also as a normalized value with respect to $C_{j0}$ (i.e., $N_{CP}$ in %). Also note that, given $M = 2.256$, (3.11) yields $s_{IDEAL} \approx 2.71$.

Table 3.1 MA46H120 varactor parameters

| Parameter | Value |
|---|---|
| $C_{j0}$ | $1.09pF^{*1}$ |
| $V_J$ | $4.445V^{*1}$ |
| $M$ | $2.256*1$ |
| $C_P \,/\, \left[N_{CP} = \frac{C_P}{C_{j0}}(in\ \%)\right]$ | $139fF^{*1}$ / $[12.8\%]^{*2}$ |
| $R_S$ | $0\Omega^{*3}$ |
| $L_S$ | $\sim 300pH^{*4}$ |
| $s_{IDEAL}$ | $2.71^{*5}$ |
| $V_{Turn-on}$ | $0.5V^{*1}$ |
| $V_{Breakdown}$ | $-27.4V^{*1}$ |

[*1]Data provided in (MACOM, 2020). [*2] Highlights the significance of $C_P$ relative to $C_{j0}$ [*3]Identified as 0.88Ω in (MACOM, 2020) but is neglected in analytical analysis. [*4]Estimated from experimental measurements. [*5]Computed with (3.11).

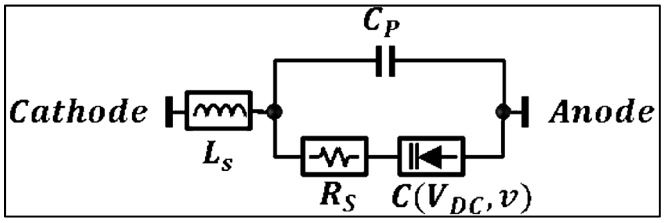



Figure 3.3 Model of the varactor MA46H120 including parasitics
Taken from MACOM (2020)

### 3.1.2.1 Effect of parallel parasitic capacitance on linearity

This subsection describes the intrinsic nonlinear behavior of an unmatched ($s > 1$) anti-series-only topology including parasitic capacitances ($C_P$). For the purpose of focusing on the effects of $C_P$ on linearity, the varactor model in Figure 3.3 is considered with $C_P \neq 0F$, $L_S = 0H$ and $R_S = 0\Omega$.

Individually-packaged varactor components are considered in this work. Therefore, the size ratio $s$ between the two varactors in Figure 3.4 is accounted for by using a first diode of size $D_A$ connected in anti-series with a set of identical diodes in parallel (of size $D_B = s \cdot D_A$). As seen in Figure 3.33, the parasitic linear capacitance $C_P$ is in parallel with the diode. Thus, paralleling $s$ diodes also increases $C_P$ by $s$. The resulting circuit for the analysis of the intrinsic nonlinear behavior of an anti-series-only topology including $C_P$ is shown in Figure 3.4. The nonlinear capacitance $C_A(v_A)$ includes the nonlinear capacitance of the varactor of size $D_A$ and its associated parasitic $C_P$, while $C_B(v_B)$ includes the circuit elements associated to $C_A(v_A)$, but scaled by $s$.

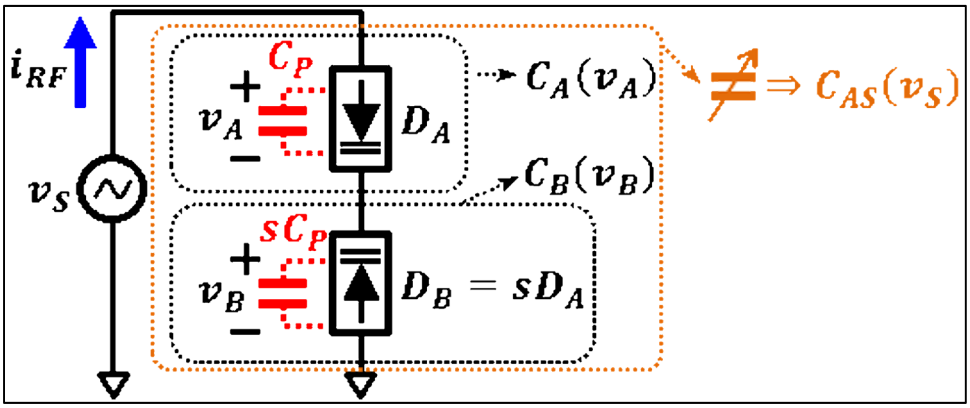



Figure 3.4 Anti-series-only topology including parallel parasitic capacitances ($C_P$). As in Figure 2.6, varactors are biased at $V_{DC}$ through a high impedance network $Z_C$ (not shown for simplification)

$C_A(v_A)$ and $C_B(v_B)$ are formulated with power series, this time including $C_P$, as in (3.12). The values of $C_{An} = C_{A0}, C_{A1}, C_{A2}$ and $C_{Bn} = C_{B0}, C_{B1}, C_{B2}$ in (3.12) are dependent on the circuit elements associated to $C_A(v_A)$ and $C_B(v_B)$, respectively, in Figure 3.4.

$$C_A(v_A) = C_{A0} + C_{A1} \cdot v_A + C_{A2} \cdot v_A^2 + \cdots$$
$$C_B(v_B) = C_{B0} - C_{B1} \cdot v_B + C_{B2} \cdot v_B^2 + \cdots$$

With

$$C_{A0} = C_0 + C_P \qquad C_{B0} = s(C_0 + C_P)$$
$$C_{A1} = C_1 \qquad C_{B1} = sC_1$$
$$C_{A2} = C_2 \qquad C_{B2} = sC_2 \tag{3.12}$$

In Figure 3.4, the resulting equivalent nonlinear capacitance $C_{AS}(v_s)$ (orange rectangle) is expressed by the power series (3.13), with coefficients $C_{ASn} = C_{AS0}, C_{AS1}, C_{AS2}$ that are derived in ANNEX II, starting from the values of $C_{An}$ and $C_{Bn}$ in (3.12).

$$C_{AS}(v_S) = C_{AS0} + C_{AS1} \cdot v_S + C_{AS2} \cdot v_S^2 + \cdots$$

where

$$C_{AS0} = \left[\frac{s}{s+1}\right](C_0 + C_P)$$
$$C_{AS1} = -\left[\frac{s(s-1)}{(s+1)^2}\right] C_0 \frac{M}{(V_J + V_{DC})}$$
$$C_{AS2} = \left[\frac{1}{2}\frac{\alpha_2}{(s+1)^3}\right] C_0 \frac{M}{(V_J + V_{DC})^2} \tag{3.13}$$

with

$$\alpha_2 = s\left((M+1)s^2 + Ks + M + 1\right)$$
$$K = M\frac{(-4C_0 - C_P)}{C_0 + C_P} - 1$$

We now focus on the $IMD_{2f_2-f_1}$ levels of RF current $i_{RF}$ shown in Figure 3.4, which are computed with the help of (3.12) and ANNEX II. It will be shown that these $IMD_{2f_2-f_1}$ levels are severely degraded due to the presence of parasitic $C_P$.

The computation of the $i_{RF}$ $IMD_{2f_2-f_1}$ levels takes into account all the MA46H120 varactor parameters (Table 3.1 MA46H120 varactor parameters), all the other circuit variables (Table 3.2) and a variable $C_P$ value normalized with respect to $C_{j0}$ ($N_{CP} = C_P/C_{j0}$ in %). The results are shown in Figure 3.5 for $N_{CP}$ varying from $0.1\%$ to $12.8\%$.

At an available power of $P_{AVS} = 18dBm$, the worst case $IMD_{2f_2-f_1}$ level in $i_{RF}$ is about $-45dBc$ and corresponds to the case $N_{CP} = 12.8\%$ with $V_{DC} = 0V$. However, for the purpose of simplifying comparisons between $IMD_{2f_2-f_1}$ performances in multiple conditions (ratio $s$, bias voltage $V_{DC}$, parasitics, etc.), all levels in Figure 3.5 are normalized such that the worst case with $N_{CP} = 12.8\%$ and $V_{DC} = 0V$ translates into $IMD_{2f_2-f_1} = 0dBc$. This allows using the Figure of Merit ($FoM_{LIN}$ defined in Section 1.4.1) for linearity performance and which will be used throughout this CHAPTER 3, defined as the worst case linearity in $dBc$ over the full range of the bias voltage $V_{DC}$. In Figure 3.5, it implies an $FoM_{LIN}$ of $0dBc$ for $N_{CP} = 12.8\%$ (marker *(3)*), of $-13.9dBc$ for $N_{CP} = 2\%$ (marker *(2)*) and of $-37dBc$ for $N_{CP} = 0.1\%$ (marker *(1)*).

Table 3.2 Default circuit parameters to compute $i_{RF}$ $IMD_{2f2-f1}$

| | |
|---|---|
| **Varactor's parameters** | Parameters listed in Table 3.1 MA46H120 varactor parameters including $s = s_{IDEAL} \approx 2.71$ [*1] |
| **RF voltage source** | 2-tone signal in (3.1) with:<br>$A = 1V$<br>$f_1$ and $f_2 = f_0 \pm f_{ENV}$<br>$f_0 = 3.6GHz$<br>$f_{ENV} = 5MHz$ (spacing of 10MHz) |
| **$V_{DC}$ values** | 0V to 25V with steps of 0.1V |
| **$C_{An}$ and $C_{Bn}$** | According to the topology analyzed |

[*1] $s_{IDEAL} \approx 2.71$ computed with (3.11) is used since it remains a near-optimal value, and it allows evaluating the effect of a change in $C_P$ only.

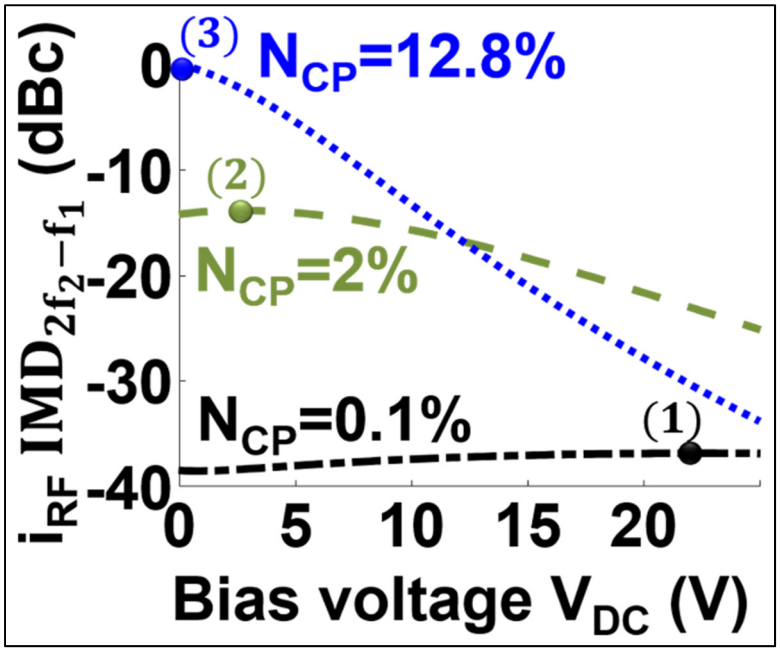



Figure 3.5 Computed $i_{RF}$ $IMD_{2f2-f1}$ levels as a function of $V_{DC}$ of the circuit in Figure 3.4. Note that markers (1) to (3) identify the $FoM_{LIN}$ of each case of $N_{CP}$

Note that $N_{CP} = 12.8\%$ stems from the choice of the varactor MA46H120 (Table 3.1 MA46H120 varactor parameters). The linearity performances of the topology in Figure 3.4 implemented with this varactor is used for benchmarking purposes in this CHAPTER 3.

As can be seen in Figure 3.5, even when considering a hypothetical case with $N_{CP}$ as low as 2%, the $FoM_{LIN}$ improvement relative to the case $N_{CP} = 12.8\%$ is reduced by only $13.9dB$ (marker *(2)* with respect to marker *(3)*), which is a marginal improvement compared to the nearly-ideal case of $N_{CP} = 0.1\%$ (marker *(1)*). Therefore, in our applications where packaged varactors with $N_{CP} \approx 12.8\%$ are typical, relying on lower $N_{CP}$ to improve linearity is not a solution.

This justifies the need for linearity improvement techniques for applications such as ours, to compensate the linearity degradation due to capacitive parasitics ($C_P$).

Next, the potential of compensating the linearity degradation due to $C_P$ by varying $s$ is evaluated.

The computations with $N_{CP} = 12.8\%$ show an $FoM_{LIN}$ improvement of only $\sim 8.4dB$ relative to marker *(3)* (i.e., still significantly higher that marker *(2)*) when the scaling factor $s$ is swept. This points to the inefficacity of simply adjusting the ratio of diode sizes $s$ in the anti-series topology to compensate the negative effect of $C_P$ on linearity. It is attributed to the dependence of $\alpha_2$ on $C_0$ in (3.13), when $C_P$ is present. While $\alpha_2$ in (3.10) ($C_P$-free case) may be cancelled over the full range of the bias voltage $V_{DC}$ with the proper scaling factor $s$, $\alpha_2$ in (3.13) may only be cancelled over a narrow range of $V_{DC}$ with a specific value of $s$, given the presence of $C_0$ in (3.13) and its dependence on $V_{DC}$. This is a serious limitation in this type of anti-series implementation, when a highly linear and controllable capacitance network with a wide tunable range is desired.

The above considerations demonstrate that the existing distortion cancellation technique applied to two unmatched series-connected hyper-abrupt varactors is *not effective* in the presence of significant parasitic capacitance $C_P$. This justifies the need for linearity improvement techniques. An improved anti-series-only network that allows improving the linearity performances in the presence of $C_P$ is proposed in Section 3.2.1.

### 3.1.2.2 Effect of series parasitic inductance on linearity

We now analyze the nonlinear behavior of an anti-series topology in the presence of series parasitic inductances. This analysis uses the varactor model in Figure 3.3 with $L_S \neq 0$, $C_P = 139fF$ ($N_{CP} = 12.8\%$) and $R_S = 0.88\Omega$.

Considering identical diodes in parallel for $D_B = s \cdot D_A$ (Figure 3.4), each represented by the network of Figure 3.3, the inductances in these networks may be combined in parallel using the symmetry principle to determine the equivalent inductance associated with the entire network of diodes. Moreover, this network of parallel diodes resulting representing the diode $sD_A$ is augmented with an additional diode of size $D_A$ to represent the anti-series topology of Figure 3.4, and the inductances in the resulting network may be summed as an equivalent series inductance $L_{EQ}$. The expression of $L_{EQ}$ is given by (3.14). Note that (3.14) neglects any mutual inductance phenomena for simplification purposes but still adequately captures the negative impact of $L_S$ on linearity.

$$L_{EQ} = L_S\left(\frac{s+1}{s}\right) \tag{3.14}$$

A single series equivalent inductance allows analyzing the effect of $L_S$ on linearity in $i_{RF}$ with the circuit in Figure 3.6 by substituting the non-zero series impedance $Z_L$ with $L_{EQ}$. In Figure 3.6, the impedance seen by the voltage source $v_s$ is identified as $Z_{TOT} = Z_L + Z_{C_{AS}(v_{AS})}$ where $Z_{C_{AS}(v_{AS})}$ is the impedance of $C_{AS}(v_{AS})$. Due to the presence of $Z_L$, the nonlinear capacitance $C_{AS}(v_{AS})$ expressed in (3.13) is no longer a function of the ideal source voltage $v_S$, but varies as a function of the AC voltage $v_{AS}$. This means that the analysis given in Section 3.1.2.1, which includes the effect of parasitic capacitance $C_P$ only, is not sufficient when $Z_L \neq 0$.

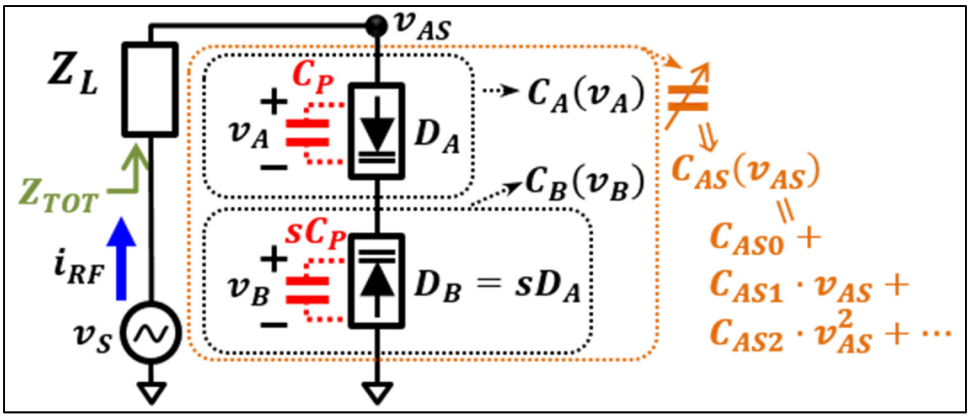



Figure 3.6 Anti-series-only topology including $C_P$ driven by a non-zero source impedance $Z_L$. As in Figure 2.6, varactors are biased at $V_{DC}$ through a high impedance network $Z_C$ (not shown for simplification)

In the circuit of Figure 3.6, two mechanisms generate nonlinearities at the voltage node $v_{AS}$: (i) the intrinsic nonlinear behavior of the anti-series topology (Section 3.1.2.1) and (ii) a secondary mixing mechanism, due to the presence of $Z_L$. This latter mechanism is mentioned in the literature (e.g., (Buisman et al., 2005)), but only for an undefined non-zero source impedance $Z_L$.

Next, the secondary mixing mechanism in the presence of inductive $Z_L$ is explained and its severe negative impact on linearity is demonstrated.

The intrinsic nonlinear behavior of the anti-series circuit generates nonlinear current components in $i_{RF}$ in Figure 3.6, where $v_S$ is the 2-tone excitation centered at $f_0$ defined by (3.1). These nonlinear $i_{RF}$ current components, in turn, generate nonlinear voltage components at the node $v_{AS}$ through the ohmic interaction between $i_{RF}$ and $Z_L$. As a result, secondary mixing products occur, given the nonlinear voltage content of $v_{AS}$ that is now present across the nonlinear capacitance ($C_{AS}(v_{AS})$). In our context, a key mixing product is the one between the fundamental voltage tones centered at $f_0$ (i.e., $f_1$, $f_2$) and voltage components in the vicinity of $2f_0$ (e.g., $2f_1$, $f_1 + f_2$, $2f_2$) within $v_{AS}$. This yields additional contributors to $IMD_{2f_2-f_1}$ products (one example being the mixing product $2[f_2 + f_1] - f_1 = 2f_2 - f_1$). The simulations presented next will show that this secondary mixing mechanism is detrimental to linearity. The worst-case is when $L_{EQ}$ and the capacitance network $C_{AS}$ allow a series resonance in the vicinity

of $2f_0$. This corresponds to $|Z_{TOT}|@2f_0 \rightarrow 0\Omega$ which allows significantly higher $i_{RF}$ and $v_{AS}$ components in the vicinity of $2f_0$. As a result, the contributors due to this secondary mixing mechanism further degrade the $IMD_{2f_2-f_1}$ levels.

The aforementioned explanation stating that the presence of inductive series parasitics ($L_S$) yields linearity degradation is confirmed by results from the simulation of the circuit in Figure 3.6 with $Z_L$ substituted by $L_{EQ}$. In these harmonic balance simulations using ADS™, all the varactor parameters in Table 3.1 MA46H120 varactor parameters and all the circuit variables in Table 3.2 are considered, except for $A = 0.01V$ and a variable $L_S$ (i.e., $L_{EQ}$ is swept). Figure 3.7 presents conclusive results regarding $L_S$.

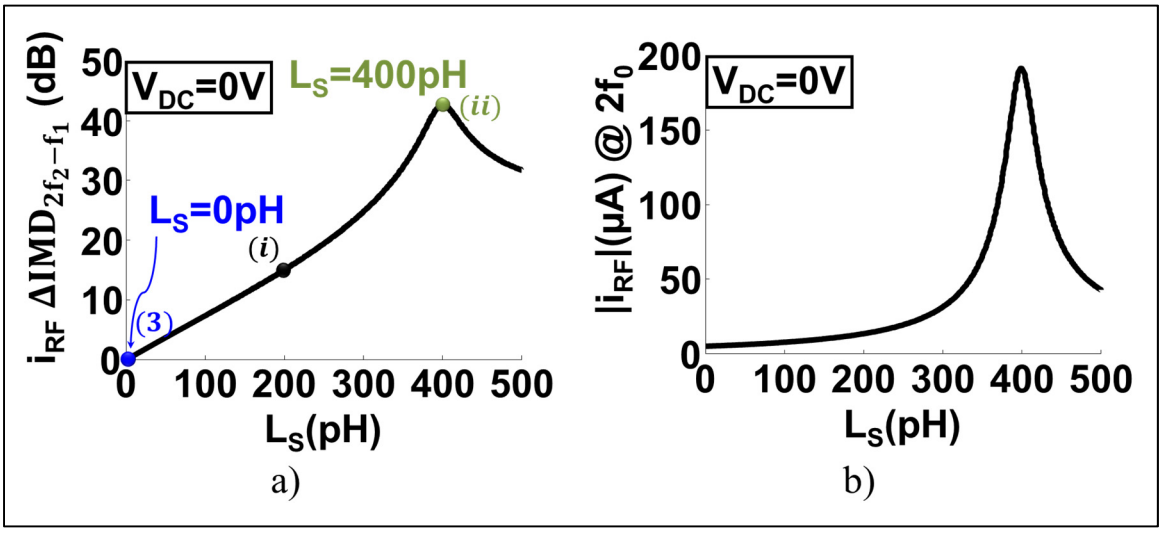



Figure 3.7 a) Increase of $i_{RF}$ $IMD_{2f2-f1}$ level with $L_S$ at a bias voltage of $V_{DC} = 0V$
b) $|i_{RF}|$ at $2f_0$ as a function of $L_S$ at a bias voltage of $V_{DC} = 0V$

For performance evaluation, the highest $IMD_{2f_2-f_1}$ level obtained across the $V_{DC}$ bias voltage range is considered as the linearity Figure of Merit (as defined in Section 3.1.2.1).

All $IMD_{2f_2-f_1}$ levels in Figure 3.7 are normalized such that the case $L_S = 0pH$ with $V_{DC} = 0V$ (marker *(3)*) translates into $0dBc$. This also means that any linearity degradation compared to marker *(3)* is attributed to the presence of $L_S$.

Figure 3.7a plots the increase of $i_{RF}$ $IMD_{2f_2-f_1}$ levels as a function of $L_S$ with $V_{DC} = 0V$. It shows a significant degradation of $IMD_{2f_2-f_1}$ with an increasing $L_S$ between $0pH$ and ~$300pH$. This is because an increasing $L_S$ (and $L_{EQ}$ according to (3.14) in series with $C_{AS}(v_{AS})$ translates into a decreasing resulting reactance seen by $v_S$, hence an increasing $i_{RF}$, which in turn translates into an increasing RF voltage across each nonlinear junction capacitance within the varactor and consequently higher $IMD_{2f_2-f_1}$. The peak at $L_S \approx 400pH$ results from $L_{EQ} \approx 550pH$ (3.14) resonating at the frequency $2f_0$ with $C_{AS0} \approx 0.9$pF (computed with (3.13)) when $V_{DC} = 0V$. Figure 3.7b supports the above explanation. It shows that $|i_{RF}|$ at $2f_0$ reach a peak at the same $L_S$ value as for the curve of Figure 3.7a, i.e., when resonance at $2f_0$ occurs.

The overall $IMD_{2f_2-f_1} - L_S$ relationship in Figure 3.7a demonstrates that the $L_S$ associated to diode's technology and assembly (semiconductor technology, wire-bond or flip-chip connectivity, discrete diode devices or MMIC designs, etc.) has the potential of severely degrading circuit linearity and is a limiting factor in regards with the maximum frequency of operation of a given technology.

Moreover, the above analysis may be extended to series interconnect transmission lines presenting significant electrical lengths and which have a similar negative impact on linearity as with $L_S$. As a case example illustrated in Figure 3.8, a connection network used with the anti-series/anti-parallel topology (Figure 2.6b) inherently adds series parasitics between the two anti-series branches. If the electrical length of this connection network is significant (e.g., in a $3.6GHz$ design requiring discrete components on a PCB), the above analysis shows that this topology inevitably yield degraded linearity performances. As a solution to minimize the effect of such connectivity network, an alternative to the anti-series/anti-parallel topology is proposed in Section 3.2.2.

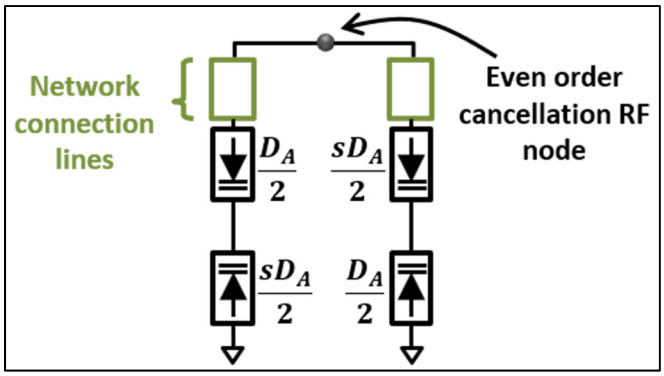



Figure 3.8 Anti-series/anti-parallel topology including significant series parasitics within the network connection lines

## 3.2 Proposed modified anti-series topology for improved linearity in the presence of parasitics

This section presents an improved anti-series-only topology introducing two major innovations. (i) It enhances circuit linearity of hyper-abrupt varactor-based controllable networks in the presence of significant parasitic parallel capacitance ($C_P$), and (ii) it desensitizes its linearity performances from source impedance loading effects without the necessity of doubling the number of required varactors as required in the state-of-the-art anti-series/anti-parallel topology (Figure 2.6b). Moreover, (ii) offers the additional advantage of minimizing the linearity degradation due to the connection network compared to the circuit in Figure 3.8. These two innovative concepts are presented in Section 3.2.1 and Section 3.2.2, respectively.

### 3.2.1 Anti-series-only topology with enhanced linearity performances in the presence of $C_P$

The linearity enhancement of a varactor-based anti-series topology, as reported in the literature so far, is achieved through the optimization of the ratio between the diode sizes ($s$) to enable a 3rd order distortion cancellation. This was shown in Section 3.1.1.4 by designing for $\alpha_2 = 0$ in (3.10), hence $C_{AS2} = 0$, yielding the ideal ratio $s = s_{IDEAL}$ as in (3.11). However, as demonstrated in Section 3.1.2.1, this nonlinearity-cancellation mechanism is significantly

impaired by the parasitic $C_P$, yielding poor overall linearity performances. The negative impact of $C_P$ on linearity is significantly reduced with the *modified* anti-series network proposed here.

We first examine the underlying concept with the help of the circuit in Figure 3.9. It will be demonstrated that the linearity degradation due to $C_P$ may be minimized with a compensation technique that allows adjusting the capacitance ratio between $C_A$ and $C_B$, independently of $s$.

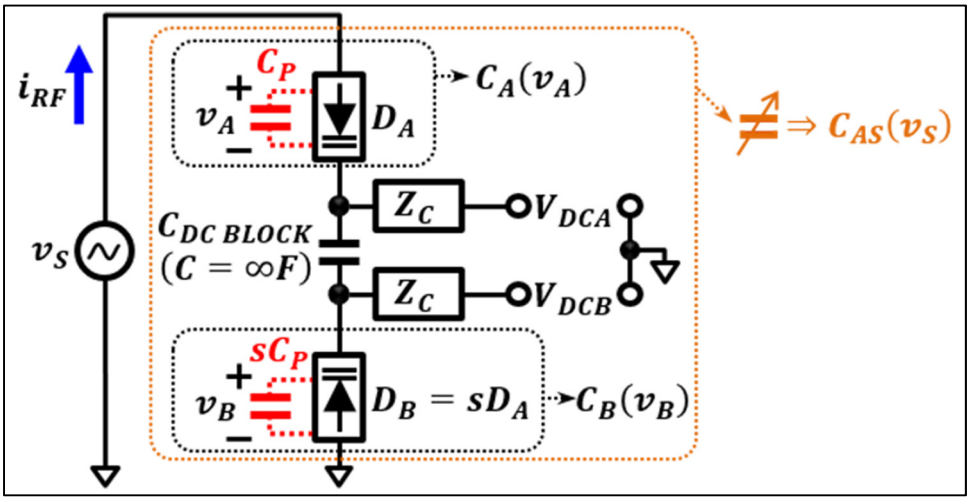



Figure 3.9 Dual-biased anti-series topology in the presence of $C_P$. $D_A$ and $D_B$ are biased at $V_{DCA}$ and $V_{DCB}$, respectively, through a high impedance network $Z_C$. $V_{DCA}$ and $V_{DCB}$ are decoupled with $C_{BLOCK}$ which has an ideal infinite impedance at DC and 0Ω at all other frequencies

For the purpose of this demonstration, Figure 3.9 includes nonlinear capacitances $C_A(v_A)$ and $C_B(v_B)$ that may be tuned *independently*, thanks to the biasing of $D_A$ and $D_B$ with separated bias voltages ($V_{DCA}$ and $V_{DCB}$). The ideal decoupling capacitance ($C_{DC\ BLOCK}$ in Figure 3.9) is necessary in this analysis to maintain an infinite impedance at DC and an ideal 0Ω at all other frequencies, including down to baseband frequencies ($f_{ENV}$). These hypothetical conditions allow maintaining an optimal capacitance ratio between $C_A$ and $C_B$ even in the presence of significant parasitics $C_P$, yielding enhanced linearity performances. This is shown next.

$$C_A(v_A) = C_{A0} + C_{A1} \cdot v_A + C_{A2} \cdot v_A^2 + \cdots \tag{3.15}$$

$$C_B(v_B) = C_{B0} - C_{B1} \cdot v_B + C_{B2} \cdot v_B^2 + \cdots$$

With

$$C_{A0} = C_{0\alpha} + C_P \qquad C_{B0} = s(C_{0\beta} + C_P)$$
$$C_{A1} = C_{1\alpha} \qquad C_{B1} = sC_{1\beta}$$
$$C_{A2} = C_{2\alpha} \qquad C_{B2} = sC_{2\beta}$$

With the help of (3.15) and ANNEX II, while considering the varactor parameters in Table 3.1 MA46H120 varactor parameters and all the other circuit variables in Table 3.2, the $IMD_{2f_2-f_1}$ levels of the RF current $i_{RF}$ are computed. The objective of these computations is to minimize the distortions by optimizing the value of $V_{DCB}$ for every given value of $V_{DCA}$ over its full range. Figure 3.10a presents the optimal $V_{DCB}$ bias voltage profile applied to the diode $D_B$ as a function of $V_{DCA}$.

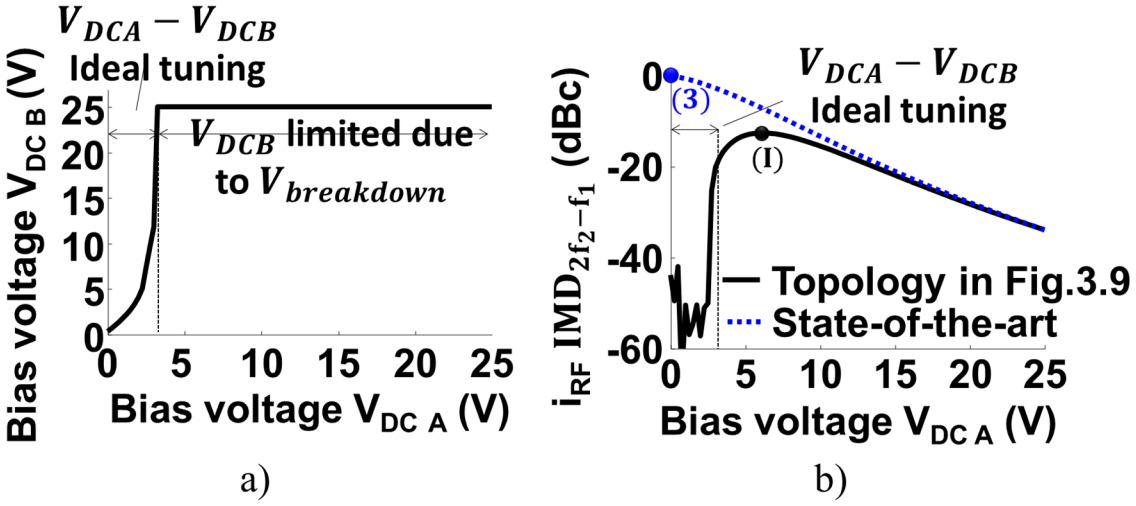



Figure 3.10 a) $V_{DCA}$ vs $V_{DCB}$ bias profile which optimizes circuit linearity b) $i_{RF}$ $IMD_{2f2-f1}$ level (solid curve) of the circuit in Figure 3.9 when using the $V_{DCA}$ vs $V_{DCB}$ bias profile of a) benchmarked against the $IMD_{2f2-f1}$ level of the topology including $C_P$ with $N_{CP} = 12.8\%$ (blue curve). Markers *(3)* and *(I)* identify the $FoM_{LIN}$ of each curve

Over the range of $V_{DCA}$ values from $0V$ to $3.25V$ (identified as "$V_{DCA} - V_{DCB}$ ideal tuning" in Figure 3.10a), it is possible to select the optimal value of $V_{DCB}$ to achieve maximal linearity

improvement. Above $V_{DCA} = 3.25V$, the value of $V_{DCB}$ that would enable optimal $IMD_{2f_2-f_1}$ cancellation is higher than the diode's breakdown voltage. Therefore $V_{DCB}$ is kept fixed at $25V$ for $V_{DCA} \geq 3.25V$.

To evaluate the linearity improvement from the use of independent bias as in Figure 3.9 in the presence of $C_P = 139fF$ ($N_{CP} = 12.8\%$), the linearity performance (black curve in Figure 3.10b) associated with the optimal $V_{DCB}$ vs $V_{DCA}$ bias profile of Figure 3.10a is computed using the same normalization as in Figure 3.5 (i.e., marker (3) equal $0dBc$). Figure 3.10b therefore allows benchmarking the linearity $FoM_{LIN}$ (as defined earlier) of the topology in Figure 3.9 against the $FoM_{LIN}$ of the anti-series topology in Figure 3.4 with identical $C_P = 139fF$ (the blue curves in Figure 3.5 and Figure 3.10b are the same).

It can be seen that in the range "$V_{DCA} - V_{DCB}$ ideal tuning", the $IMD_{2f_2-f_1}$ levels are improved by more than $\sim 40dB$. This demonstrates the feasibility of achieving excellent linearity improvement despite the presence of $C_P$, assuming the hypothetical case where a dual (separate) bias scheme as in Figure 3.9 is used. Above this ideal tuning range, the linearity improvement being less significant is due to the voltage breakdown limitation, which does not allow maintaining an optimal $V_{DCA} - V_{DCB}$ profile.

The topology in Figure 3.9 adds circuit complexities that make it prohibitive for a practical implementation (e.g., requiring $C_{DC\,BLOCK} = \infty$). However, the above analysis based on Figure 3.9 allows drawing an important conclusion.

The linearity improvement shown in Figure 3.10b is achieved with the $V_{DCB}$ vs $V_{DCA}$ bias profile of Figure 3.10a, which shows that the condition $V_{DCA} < V_{DCB}$ is required. Hence, a bias condition in Figure 3.9 where $V_{DCB}$ is set at some DC voltage $V_1$, while $V_{DCA}$ is set at a DC voltage $V_2 < V_1$ translates necessarily into $C_A|_{V_2} > \left[\frac{C_B|_{V_1}}{s} = \frac{sC_A|_{V_1}}{s} = C_A|_{V_1}\right]$ according to (3.7). It can be concluded then that the linearity degradation due to $C_P$ may be reduced by increasing the capacitance of $C_A$ relative to the capacitance of $C_B$. This must be achieved independently

of the capacitance $C_P$, which does not vary with the bias voltage, and thus may not be achieved by adjusting the size ratio $s$. Moreover, in a practical implementation restricted to a unique bias voltage, it cannot be accomplished neither by setting $V_{DCA} \leq V_{DCB}$. Therefore, the solution proposed in this paper is to add a lumped capacitance in parallel with $C_A$.

It is worth recalling also that, although modifying the diode-size ratio $s$ allows adjusting the ratio between $C_A$ and $C_B$, the $FoM_{LIN}$ improvement in the presence of $C_P$ as a function of $s$ can only be of limited value, as explained in Section 3.1.2.1, hence does not substitute the proposed method of adding a lumped capacitance.

Based on the above conclusion, we propose in Figure 3.11 a modified anti-series-only network that improves significantly the linearity performances despite the presence of $C_P$, by providing a new degree of freedom to reach a greater range of $C_A/C_B$ ratios, compared to only adjusting the ratio $s$. This is achieved by adding a lumped capacitance ($C_{LIN}$) in parallel with the smaller nonlinear capacitance $C_A$.

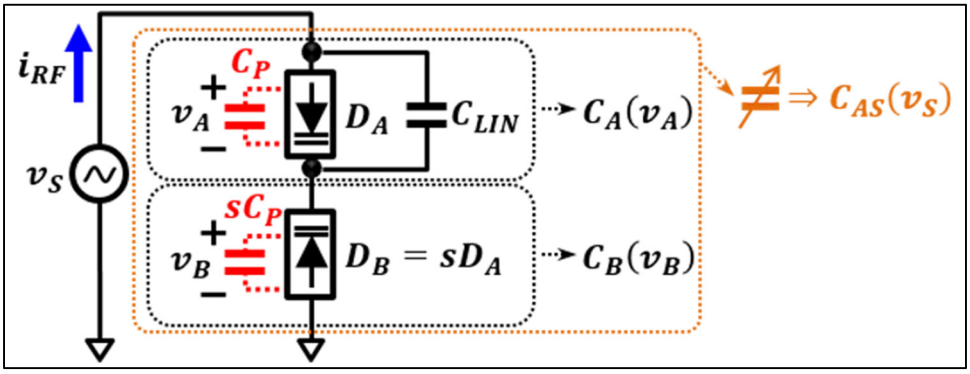



Figure 3.11 Proposed improved anti-series network. As in Figure 2.6, varactors are biased at $V_{DC}$ through a high impedance network $Z_C$ (not shown for simplification)

Next, we demonstrate through computations and simulations the linearity improvement with the addition of $C_{LIN}$. First, the power series $C_A(v_A)$ and $C_B(v_B)$ associated with the topology in Figure 3.11 is derived by adding $C_{LIN}$ to the coefficient $C_{A0}$ in (3.12), yielding (3.16).

$$C_A(v_A) = C_{A0} + C_{A1} \cdot v_A + C_{A2} \cdot v_A^2 + \cdots$$
$$C_B(v_B) = C_{B0} - C_{B1} \cdot v_B + C_{B2} \cdot v_B^2 + \cdots$$

With

$$C_{A0} = C_0 + C_P + C_{LIN} \qquad C_{B0} = s(C_0 + C_P)$$
$$C_{A1} = C_1 \qquad C_{B1} = sC_1$$
$$C_{A2} = C_2 \qquad C_{B2} = sC_2 \tag{3.16}$$

$IMD_{2f_2-f_1}$ levels are now used to demonstrate the linearity improvement of the proposed topology in the presence of $C_P$ compared to the well-known topology of Figure 3.4. The $i_{RF}$ $IMD_{2f_2-f_1}$ levels of the circuit in Figure 3.11 are computed with ANNEX II using the $C_{An}$ and $C_{Bn}$ coefficients given in (3.16) while considering the varactor parameters in Table 3.1 MA46H120 varactor parameters, all the circuit parameters in Table 3.2, and a variable $C_{LIN}$.

Figure 3.12 plots the $FoM_{LIN}$, i.e., the highest $IMD_{2f_2-f_1}$ level over the full range of bias voltages, as a function of $C_{LIN}$ for two scaling factor $s$: (i) for $s \approx s_{IDEAL} = 2.71$ as per Table 3.1 MA46H120 varactor parameters (black solid curve) and (ii) for $s = 3$ (green dashed curve). The case $s = 3$ reflects the diode ratio in the designs used for experimental implementation (Section 3.3.2).

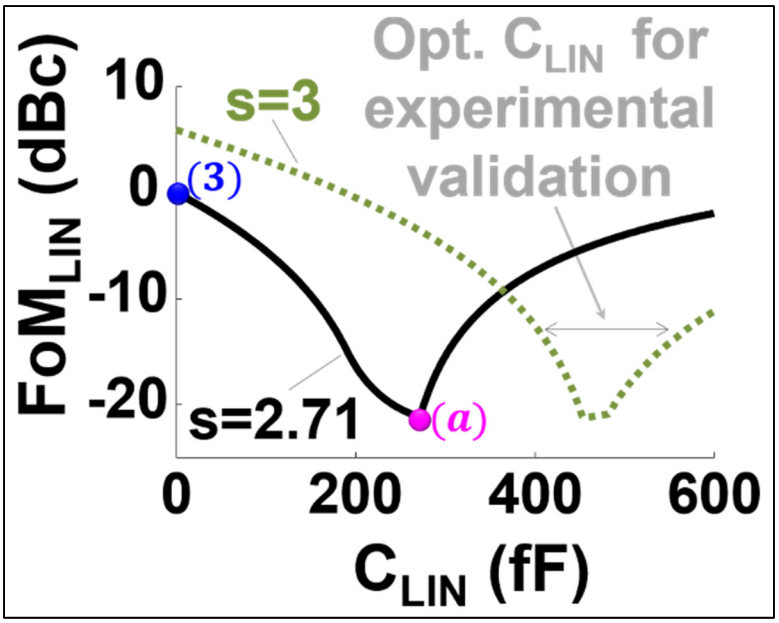



Figure 3.12 Computed FoMLIN levels of the circuit in Figure 3.11 as a function of CLIN for $s = s_{IDEAL} = 2.71$ (black curve) and for $s = 3$ (green curve). Markers *(3)* and *(a)* identify key FoMLIN values

In Figure 3.12, all plotted $FoM_{LIN}$ values on both curves are normalized such that the case $C_{LIN} = 0fF$ for $s = 2.71$ (marker *(3)*), which corresponds to the regular topology in Figure 3.4, translates into $0dBc$. Accordingly, any negative $dBc$ value on these $FoM_{LIN}$ curves represents an improvement attributed to our proposed technique over the state-of-the-art.

For the case of $s = 2.71$, the optimal value of $C_{LIN}$ is $\sim 270fF$ (marker *(a)*) and corresponds to a $\sim 21dB$ improvement of the $FoM_{LIN}$ compared to marker *(3)*. Therefore, the proposed modified network in Figure 3.11 brings a significant improvement of linearity in the presence of $C_P$.

Moreover, the case $s = 3$ in Figure 3.12 demonstrates that similar linearity performances to the case $s = 2.71$ may be achieved by properly adjusting $C_{LIN}$. Therefore, unlike in the topology in Figure 3.4, where linearity inevitably degrades as the value of the scaling factor differs from $s_{IDEAL}$, the topology proposed here offers greater flexibility on the value of $s$. This

is of particular interest in a discrete component approach where the size ratio $s$ is set by paralleling multiple diodes.

It is also worth mentioning that the proposed linearization technique is effective on a wide range of $N_{CP}$ values and thus is applicable to other hyper-abrupt varactors. For instance, when the circuit in Figure 3.11 is implemented with the SMV2019 varactor from Skyworks™ ($N_{CP} = 3.1\%$ and $S_{IDEAL} = 2.32$ due to a $M = 1.4$), the same numerical computations applied earlier yield an improvement of the $FoM_{LIN}$ by $28dBc$ for $C_{LIN} = 120fF$. Similarly, with the SMV1231 varactor from Skyworks™ ($N_{CP} = 23.4\%$ and $S_{IDEAL} = 3.19$ due to a $M = 5$), the same computations yield a $FoM_{LIN}$ improved by $18dBc$ for $C_{LIN} = 980fF$.

### 3.2.2 Desensitization of linearity against external impedance in anti-series-only topologies

It was shown in Section 3.1.2.2 that linearity in an anti-series-only topology using hyper-abrupt varactors is significantly degraded when driven by a non-zero source impedance $Z_L$.

The complete varactor-based circuit topology proposed here circumvents this shortcoming, with key advantages over the state-of-the-art anti-series/anti-parallel topology (Figure 3.8) used for the same purpose. Our solution consists of cancelling all the even-order harmonics at the voltage $v_{AS}$ (i.e., $v_{AS} = 0V$ around $2f_0$, $4f_0$, $\cdots$) with a quarter-wave shorted stub as illustrated with "$2f_0$ trap" in Figure 3.13a. This circumvents the linearity degradation due to the well-known secondary mixing mechanism caused by a non-zero $Z_L$ (Section 3.1.2.2), when voltage exists at even-order harmonics.

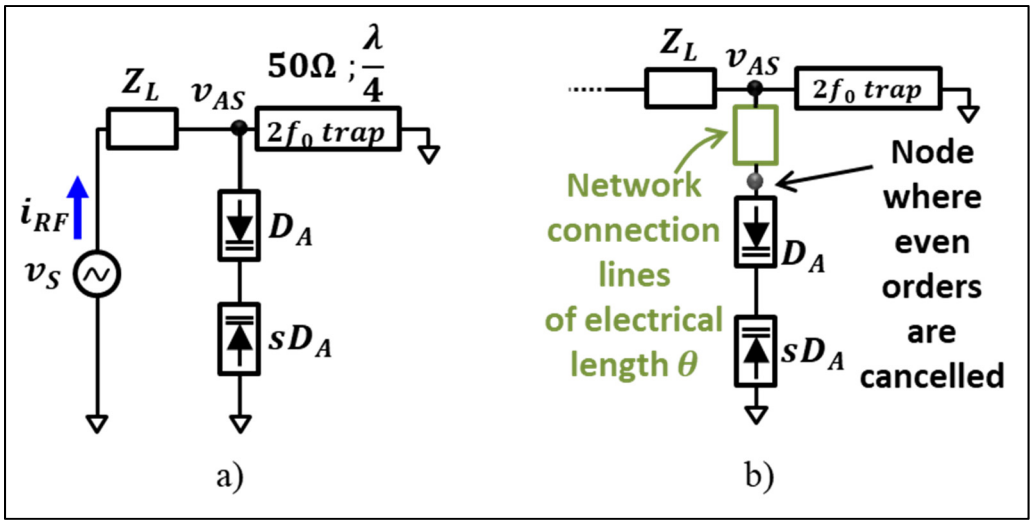



Figure 3.13 a) Anti-series topology including an even-order filter trap.
b) Possible design optimization that allows mitigating the effect of series parasitics for better overall circuit linearity performances

Our proposed technique has two benefits over the anti-series/anti-parallel topology. (i) It reduces the number of varactors by a factor of two and (ii) whereas in the anti-series/anti-parallel topology the linearity is inevitably degraded due to series-parasitics in the network connection lines (Figure 3.8 in Section 3.1.2.2), our technique circumvents this problem. Figure 3.13b illustrates the underlying concept where the cancellation of even-order harmonics takes place at the node connected to the varactor. This is made possible by adjusting the dimensions of the transmission line-based filter ("$2f_0\ trap$") to account for the electrical length $\theta$ of the network connection lines and the loading effects of $Z_L$, thereby allowing to force $v_{2f_0} \approx 0V$ at this node.

### 3.2.3 Complete proposed varactor-based anti-series topology

The proposed varactor-based anti-series topology, which is introduced for the first time in this work, is shown in Figure 3.14. It combines both the novel circuit techniques presented in Section 3.2.1 and Section 3.2.2. i.e., the addition of $C_{LIN}$ for improved linearity despite the presence of the parasitic $C_P$, and the "$2f_0$ trap" to avoid linearity degradation due to loading effects.

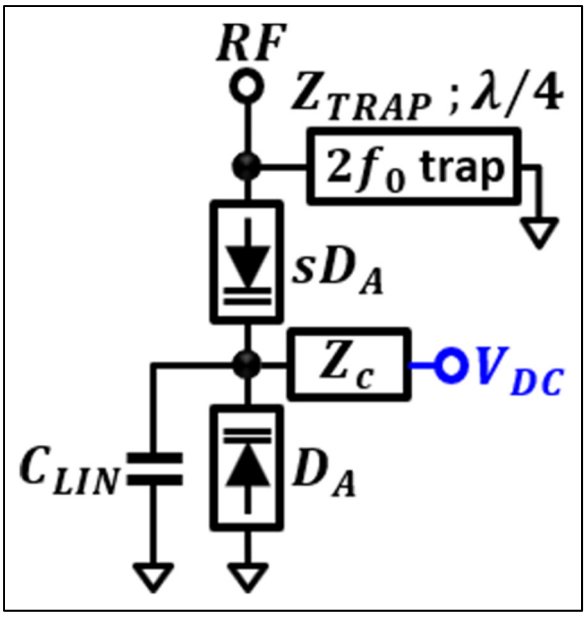



Figure 3.14 Complete anti-series topology including both proposed circuit techniques in Section 3.2.1 and Section 3.2.2

The complete topology in Figure 3.14 consists of a varactor-based tunable impedance network (TIN) implemented in controllable RF networks: a highly linear phase shifter presented in CHAPTER 4 and a controllable gain RF amplifier presented in CHAPTER 5.

## 3.3 Experimental implementation and results

This section presents results from experimental measurements i) validating the improved linearity of the proposed anti-series topology in Section 3.2.1 when benchmarked against a topology that does not use the proposed linearization technique (i.e., Figure 3.14 without $C_{LIN}$) and ii) validating the complete varactor-based circuit topology proposed here, which makes use of an even-order harmonic trap.

### 3.3.1 Description of fabricated circuits

This subsection describes the circuits fabricated for the linearity characterization of the anti-series-only topologies.

In the previous sections, the linearity is analyzed based on the currents $i_{RF}$ (Figure 3.1). Given the difficulty of measuring $i_{RF}$, the distortions are accurately measured here using a hybrid coupler.

In part .3.3.1.1 of this subsection, the fabricated anti-series topologies are detailed. Then the devices under test ($DUTs$), each one comprising an anti-series network and a hybrid coupler, are described in part 3.3.1.2.

#### 3.3.1.1 Fabricated anti-series topologies

To demonstrate the linearity improvement of the proposed anti-series topology that includes $C_{LIN}$ (referred to as $C_{AS\,NEW}$), it is benchmarked against an identical topology, but *without* $C_{LIN}$ (referred to as $C_{AS\,REF}$). $C_{AS\,REF}$ and $C_{AS\,NEW}$ are designed with the following features and their schematics and photos are presented in Figure 3.15a, Figure 3.135c and Figure 3.135b Figure 3.135d, respectively.

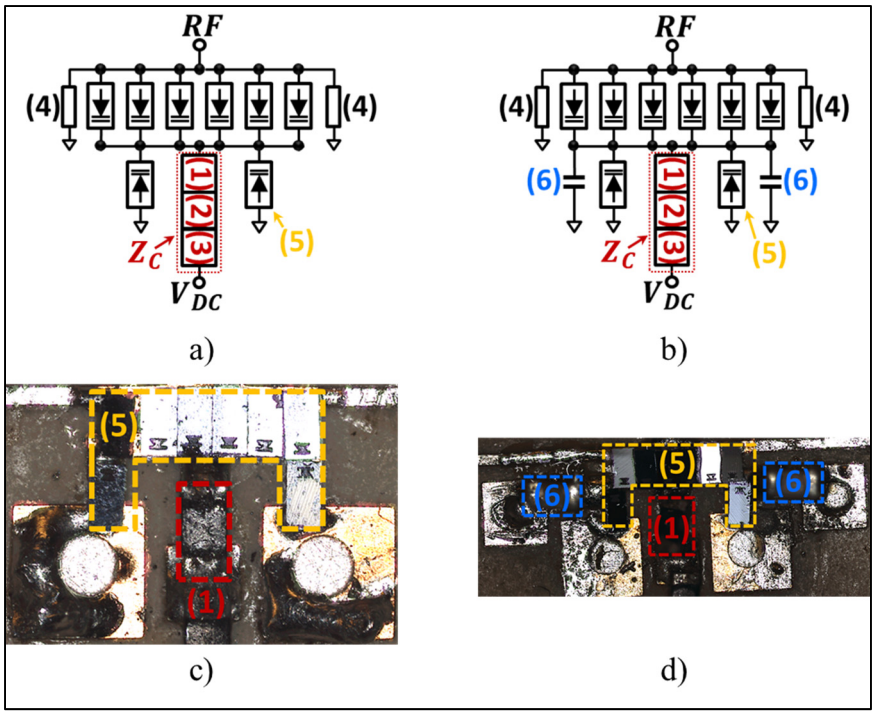



Figure 3.15 a) Schematic of $C_{AS\ REF}$ b) Schematic of $C_{AS\ NEW}$ c) photo of the fabricated network $C_{AS\ REF}$ showing a close-up of the diodes d) photo of the fabricated network $C_{AS\ NEW}$ showing a close-up of the diodes. Components: (1) 100kΩ 0402 resistor (2) 20MΩ 0402 resistor (3) 200MΩ 0805 resistor (4)~100Ω ; λ/4 transmission line (5) MA46H120 varactor model from MACOM (MACOM, 2020) (6) $C_{LIN}$ 0402 capacitance

1) All varactor used are MA46H120 (MACOM, 2020) (marker *(5)*).
2) A 6:2 discrete varactor configuration is used so that the impedance tuning range meets the requirement in our application (Figure 1.4). At the same time it corresponds to a diode-size ratio (i.e., $s = 3$) in the vicinity of $s_{IDEAL} \approx 2.71$, as dictated by the choice of varactor and according to (3.11) and Table 3.1 MA46H120 varactor parameters.
3) Unlike in other works that use twice the number of varactors (Figure 2.6b) to cancel even-order voltage harmonics, here we use our proposed technique (Section 3.2.2) with quarter-wave $2f_0$ $traps$ (marker (4)).
4) The DC feed network ($Z_C$) is a line-up of a $100k\Omega$, a $22M\Omega$, and a $200M\Omega$ resistors (markers (1), (2) and (3)). Moreover, the ground plane is slotted below the $Z_C$ network to minimize the shunt capacitive parasitics.

5) The linearity improvement technique proposed in Section 3.2.1 is implemented in $C_{AS\,NEW}$ with lumped capacitances $C_{LIN}$ (marker (6)). The two identical $C_{LIN}$ account for the ratio of $6:2$ $(i.e.\,2x3:1)$ such that a comparison may be drawn between the experimental linearity performances and the computed results presented in Figure 3.12.

#### 3.3.1.2 Fabricated DUTs

Figure 3.16a presents the schematic of the $DUTs$ used to measure the linearity performances of $C_{AS\,REF}$ and $C_{AS\,NEW}$. In this network, the $50\Omega$-$90°$ hybrid coupler equally divides the incoming RF power (red arrows) towards two identical anti-series topologies ($C_{AS}$), both of them implemented as $C_{AS\,REF}$ in one distinct $DUT$, and as $C_{AS\,NEW}$ in another distinct $DUT$. The distortions in the reflected signals (blue arrows) measured at the $RF_{OUT}$ port are generated strictly by $C_{AS}$.

$C_{AS\,REF}$ and $C_{AS\,NEW}$ are implemented on the same 10mils CLTE ($\varepsilon_r = 2.98$) substrate. $C_{AS\,REF}$ implemented in $DUT_{REF}$ (Figure 3.16b) serves as the reference linearity performance from the state-of-the-art, and $C_{AS\,NEW}$ implemented in $DUT_{NEW}$ (Figure 3.16c) demonstrates the linearity improvement brought by the technique proposed here.

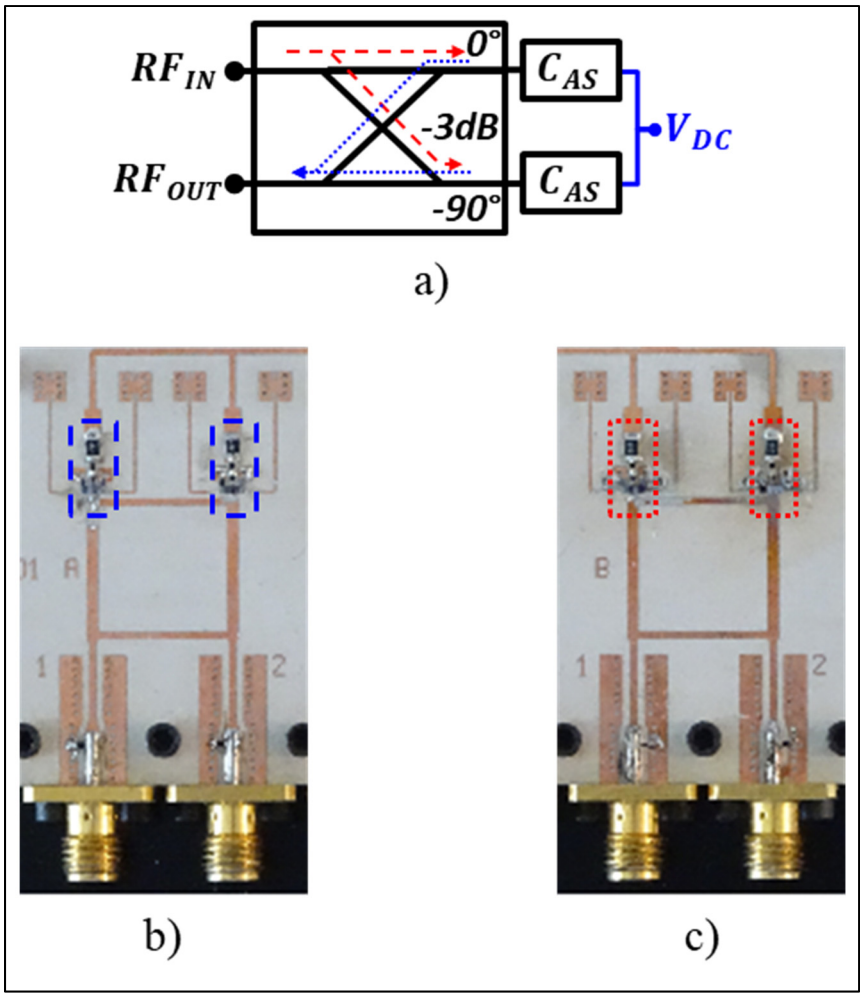



Figure 3.16 a) Schematic of the DUT b) Photo of the fabricated network $DUT_{REF}$ where the blue line identifies $C_{AS\ REF}$ c) Photo of the fabricated network $DUT_{NEW}$ where the red line identifies $C_{AS\ NEW}$

### 3.3.2 Experimental results

The linearity performances of $DUT_{REF}$ and $DUT_{NEW}$ are evaluated using two metrics. (i) $IMD_{2f_2-f_1}$ levels with a two equal-tone RF signal at frequencies $f_0 \pm f_{ENV}$ (Table 3.2) and (ii) Adjacent Channel Power Ratio (ACPR) levels with a $10MHz$ $16QAM$ RF signal centered at $f_0$ (Table 3.2) and a raised-cosine filter using a roll-off factor of 0.22. Results from these measurements are discussed in part Section 3.3.2.1 and Section 3.3.2.2.

It is worth mentioning that VNA-based S-parameters measurements show that $S_{11} < -15dB$ and that $S_{21} < 1.2dB$ for both $DUTs$, over a large bandwidth, and for any bias voltage. This demonstrates that the mismatch and transmission losses are maintained very low, thereby guarantying an accurate measurement of the anti-series networks linearity based on the signals coupled to the $RF_{OUT}$ port.

#### 3.3.2.1 $IMD_{2f2-f1}$ levels

The measured $IMD_{2f_2-f_1}$ levels at an output power ($P_{OUT}$) of $10dBm$ and at $P_{OUT} = 18dBm$ are shown in Figure 3.17a and Figure 3.17b, respectively. In Figure 3.17, the blue curves correspond to $DUT_{REF}$ and the black curves correspond to $DUT_{NEW}$. Also, to avoid any uncertainty, all levels lying below the minimum measurable level (light gray curve) are set equal to $-75dBc$.

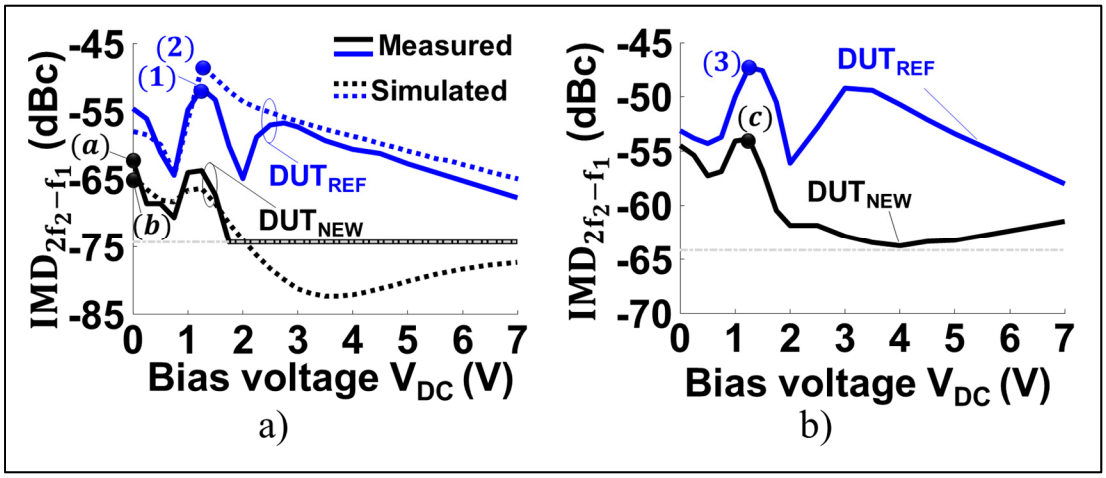



Figure 3.17 Simulated and measured $IMD_{2f2-f1}$ levels for $DUT_{REF}$ (Figure 3.15a and Figure 3.16b) and $DUT_{NEW}$ (Figure 3.15b and Figure 3.16c) for a tone spacing of 10MHz, a) at $P_{OUT} = 10dBm$ and b) at $P_{OUT} = 18dBm$. The light gray line identifies the minimum measurable level with the test setup

Using the same $FoM_{LIN}$ as for the computations and simulations, i.e., the worst-case $IMD_{2f_2-f_1}$ level over the full range of bias voltages, $DUT_{NEW}$ demonstrates an improvement by $10.6dB$ at $P_{OUT} = 10dBm$ (difference between markers *(1)* and *(a)*) and an improvement of $6.6dB$ at $P_{OUT} = 18dBm$ (difference between markers *(3)* and *(c)*).

These levels for $DUT_{NEW}$ were obtained for an experimentally optimized value of $C_{LIN} = 500fF$, which is in agreement with the range "Opt. $C_{LIN}$" identified in Figure 3.12. Moreover, the dashed curves in Figure 3.17a result from harmonic balance simulations performed in ADS™ at $P_{OUT} = 10dBm$ with the same 2-tone RF signal using the nonlinear model (Figure 3.3) of the varactor MA46H120 implemented in the same two DUT designs, including electromagnetic simulations performed in Momentum™ for the modelling of passive structures, i.e., the hybrid coupler, the transmission lines, and the components pads. Linearity optimization by simulation is reached with $C_{LIN} = 450fF$. Such excellent correlations between theory, simulations and measurements validate that the linearity improvements observed in Figure 3.17 are attributed to the proposed linearity improvement technique (Section 3.2.1) and also validate the proposed even-order cancellation technique (Section 3.2.2).

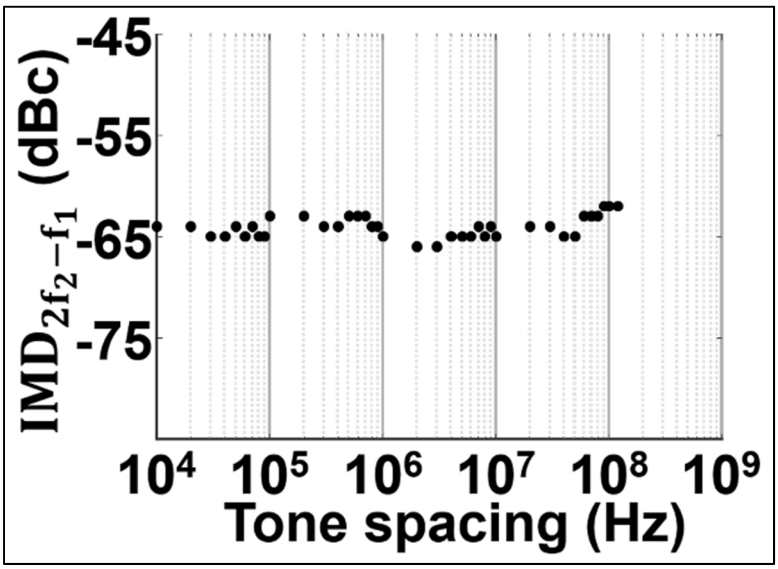



Figure 3.18 Measured $IMD_{2f2-f1}$ levels vs the tone spacing for $DUT_{NEW}$ (Figure 3.15b and Figure 3.16c) at $P_{OUT} = 10dBm$ and $V_{DC} = 1V$

Figure 3.18 presents $IMD_{2f_2-f_1}$ levels over a tone spacing ranging from $1kHz$ to $120MHz$, measured on $DUT_{NEW}$ at $P_{OUT} = 10dBm$ and for $V_{DC} = 1V$. The absence of linearity degradation over the full tone spacing range demonstrates: i) that the DC feed network $Z_C$ does

not degrade linearity performances at a tone spacing as low as $1kHz$ and ii) that the proposed distortion-cancellation technique in the presence of L-C parasitics with the use of $C_{LIN}$, as well as the proposed "$2f_0$ trap" as an alternative to the anti-series/anti-parallel topology, are both effective at a tone spacing as wide as $120MHz$.

#### 3.3.2.2 ACPR levels

Figure 3.19a plots the ACPR levels measured at $P_{OUT} = 18dBm$ where the blue and black curves correspond to $DUT_{REF}$ and $DUT_{NEW}$, respectively. Using the same $FoM_{LIN}$, $C_{AS\ NEW}$ demonstrates an improvement of the $FoM$ by $3.9dB$ (difference between markers *(4)* and *(d)*).

Figure 3.19b is a screenshot of an ACPR measurement example for $V_{DC} = 0.5V$, where the yellow power spectrum corresponds to $DUT_{REF}$ and the blue spectrum corresponds to $DUT_{NEW}$.

In Figure 3.19b, the displayed values $-51.9dBc$ and $-52.2dBc$ are related to $DUT_{REF}$ and the blue curve represent an ACPR improvement by ~7dB, which is comparable to the ~5dB improvement identified in Figure 3.19a at $V_{DC} = 0.5V$.

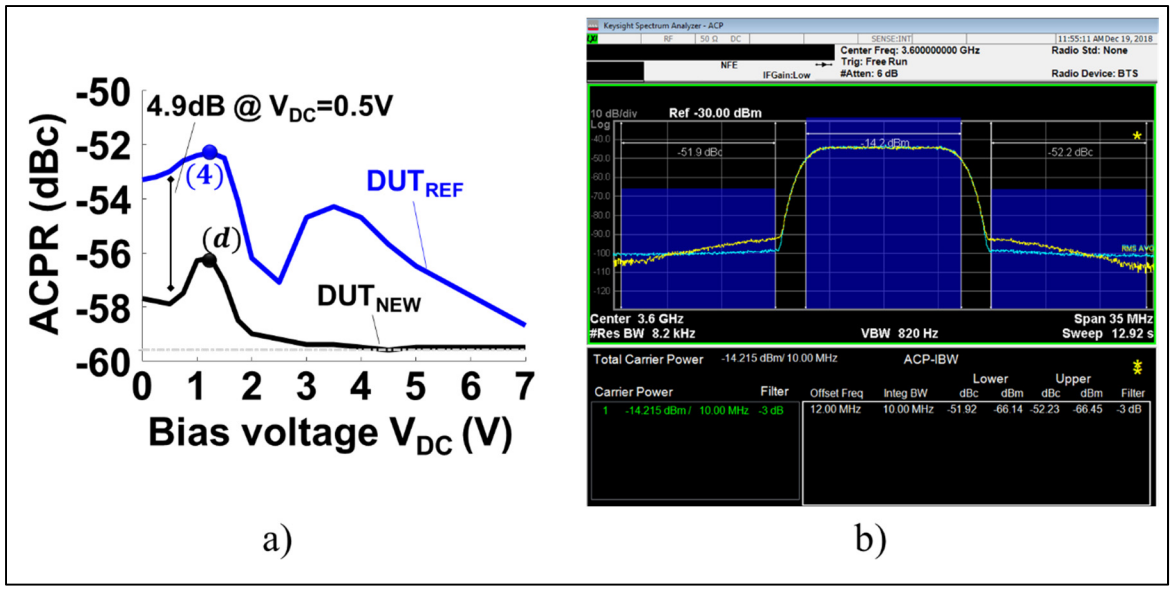



Figure 3.19 a) Measured ACPR levels for $DUT_{REF}$ (Figure 3.15a and Figure 3.16b) and $DUT_{NEW}$ (Figure 3.15b and Figure 3.16c) at $P_{OUT} = 18dBm$. The light gray line identifies the minimum measurable level. b) Screenshot of measured output spectrums at $V_{DC} = 0.5V$ where the yellow and blue curves correspond to $DUT_{REF}$ and $DUT_{NEW}$, respectively. The signal is attenuated for equipment protection explaining that the power being shown is lower than 18dBm

To the best of our knowledge, ACPR measurements have never been performed on hyper-abrupt anti-series topologies. This is relevant since it is difficult to comply with the condition $Z_C \gg Z_{D_A}$ (refer to Figure 2.6) for the content at low frequencies in such modulation schemes. It is thus interesting that i) the high resistance $Z_C$ network does not degrade significantly the linearity with such a modulation scheme and ii) that the proposed anti-series topology combined with the proposed even-order cancellation technique improves performances with such complex modulated signals.

#### 3.3.2.3 Summary of the measured performances

The key results demonstrating improved linearity by the proposed topology are summarized in Table 3.3. Note that these performances are compared favourably with other varactor-based topology solutions in Table 2.1.

Table 3.3 Summary of key measurement results

| | $IMD_{2f_2-f_1}$ @ $P_{OUT}$ =10dBm | $IMD_{2f_2-f_1}$ @ $P_{OUT}$ =18dBm | ACPR @ $P_{OUT}$ =18dBm | Demonstrated bandwidth |
|---|---|---|---|---|
| $FoM$ with linearization technique ($C_{LIN}$) | -62.2dBc | -47.3dBc | -56.2dBc | 1kHz to 120MHz |
| $FoM$ without $C_{LIN}$ | -51.6dBc | -53.9dBc | -52.3dBc | N/A |
| Improvement | 10.6dB | 6.6dB | 3.9dB | N/A |

## 3.4 Conclusion of this chapter

This chapter studies the linearity performances of hyper-abrupt varactor-based anti-series-only topologies by focusing on the effect of the parasitics surrounding the varactors. First, the mechanisms causing linearity degradation due to the presence of parallel capacitance ($C_P$) and series inductance ($L_S$) parasitics – an aspect that to the best of the authors' knowledge has never been addressed in the literature – are demonstrated analytically using a multi-tone excitation. It is shown that this degradation may not be avoided simply by adjusting the diode-size ratio. Based on these analyses, we propose an improved anti-series-only network compensating the linearity degradation due to these parasitics, thereby significantly improving linearity performances compared to the state-of-the-art. Furthermore, the complete varactor-based topology introduced in this work reduces the number of diodes by a factor of 2 compared to prior work by proposing an even-order harmonic filter, and is an attractive alternative to the well-known anti-series/anti-parallel topology. The proposed topology improves the $IMD_{2f_2-f_1}$ levels by 10.6dB and 6.6dB at output power levels of 10dBm and 18dBm, respectively, and also improves ACPR levels by 3.9dB in response to a 16QAM modulated signal at an output power level of 18dBm. The large signal linearity performances demonstrated at 3.6GHz in this paper constitute a significant improvement over the state-of-the-art. This is especially important for designs using discrete components, where parasitics are more predominant than in a MMIC approach. Although not shown here, simulations and experimental validations show that these results have only minimal impact on the tuning range of the reactance, hence the proposed techniques are suitable for applications such as Figure 2.6.

# CHAPTER 4

# HIGHLY LINEAR, 360° RF VARACTOR-BASED PHASE SHIFTER WITH LOW AND CONSTANT INSERTION LOSS

This chapter is organized as follows and relates to the innovative concept presented in Section 2.4.2 as well as the characteristics listed in Table 1.4. Section 4.1 presents the proposed V-B RTPS network demonstrating significant linearity improvement over the entire tuning range with respect to the state-of-the-art while achieving a $\Delta\phi_{MAX} > 360°$, a low IL, and a small ΔIL. These performances are validated with experimental results at 3.6GHz and at an output power of 10dBm in Section 4.2 and compared favourably with the prior-art in Section 4.3.

## 4.1 Proposed varactor-based reflective-type phase shifter

### 4.1.1 Highly linear varactor-based tunable impedance network

The proposed V-B RTPS in this work and presented in this chapter uses the TIN of Figure 4.1a, implemented by paralleling two branches of the anti-series topologies proposed in CHAPTER 3 (Figure 3.14) with $s = 3$, for maximal capacitance range and improved linearity.

In Section 4.1.2.1, a small-signal analytical approach is used to compute $\Delta\phi_{MAX}$ of our V-B RTPS network. The nominal capacitance (without RF excitation) of the TIN and the series inductive parasitic $L_S$ associated to each diode are two parameters that need to be considered for this computation and are detailed next. The expression of these two parameters is calculated with the network in Figure 4.1b.

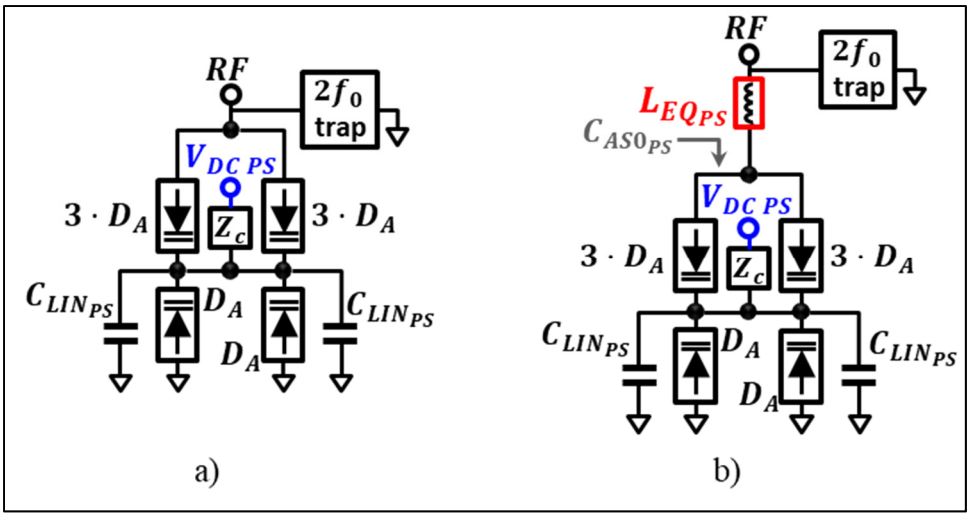



Figure 4.1 a) TIN used in the proposed V-B RTPS network with $s = 3$. b) Network used to theoretically analyze the topology in a) where the diodes are modeled with the circuit in Figure 3.3 with $R_S = 0\Omega$, $C_P = 139fF$, and all the $L_S$ are simplified into a single series-equivalent inductance $L_{EQ_{PS}}$

The nominal capacitance of the varactor-based TIN ($C_{AS0_{PS}}$ identified in Figure 4.1b) is computed with (4.1), where $C_0$ is the nominal capacitance of a single varactor (i.e., (3.7) with $v = 0$). The calculation of (4.1) is made with ANNEX II and the factor "2" accounts for the use of two anti-series topologies in parallel.

$$C_{AS0_{PS}} = \{2\} \cdot \left[\frac{(C_0 + C_P + C_{LIN})(C_0 + C_P)}{C_{LIN} + (C_0 + C_P)(s+1)}\right] s \quad \text{where } C_0 = \frac{C_{j0}}{\left(\frac{V_j + V_{DC}}{V_J}\right)^M}. \tag{4.1}$$

For equation compactness, all $L_S$ components included in each varactor of the topology in Figure 4.1b are simplified into a single series-equivalent inductance $L_{EQ_{PS}}$ using (4.2) (same simplification as in (3.14) of Section 3.1.2.2, but with a factor "½" accounting for the two paralleled anti-series topologies). Note that even though the precision of (4.2) is slightly altered by the presence of $C_{LIN_{PS}}$ and by neglecting any mutual inductance phenomena, it still adequately captures the effect of $L_S$ on $\Delta\phi_{MAX}$.

$$L_{EQ_{PS}} = \left\{\frac{1}{2}\right\} \cdot L_S \left(\frac{s+1}{s}\right) \tag{4.2}$$

### 4.1.2 Schematic and design of the proposed V-B RTPS

The V-B RTPS network is presented in Figure 4.2a. It is built with a hybrid coupler loaded with a novel, highly linear reflective load network (illustrated in Figure 4.2b). The coupler transforms the impedance $Z_0$ at ports $RF_{IN}$ and $RF_{OUT}$ to an impedance $Z_T$ seen from the reflective loads. This requires specific characteristic impedances in the coupler lines, e.g., $Z_A = \sqrt{Z_0 \cdot Z_T/2}$ (Burdin et al., 2015; Lin et al., 2008).

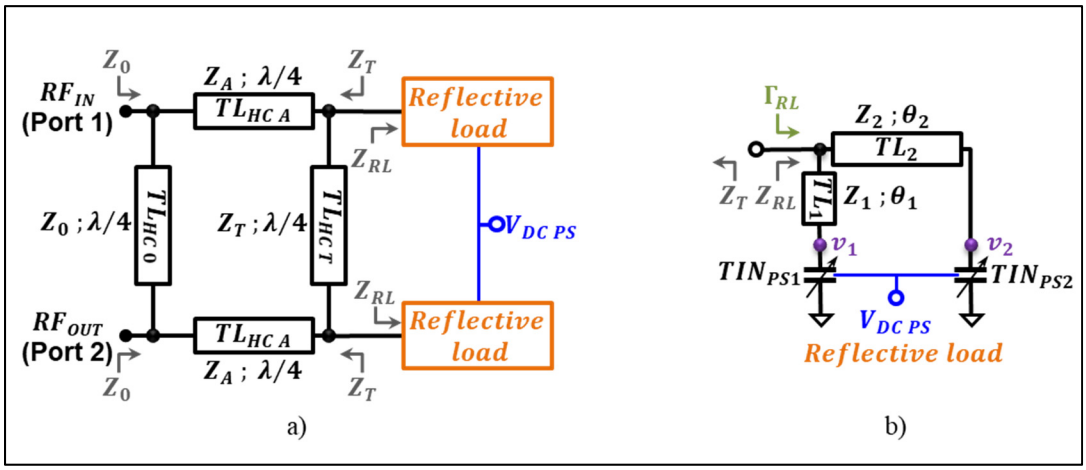



Figure 4.2 a) Proposed V-B RTPS. b) Proposed reflective load network where $TIN_{PS1}$ and $TIN_{PS2}$ are implemented with the anti-series topology of Figure 4.1a

#### 4.1.2.1 Proposed reflective load network

The reflective load proposed in this work (Figure 4.2b) offers two key improvements compared to the prior-art. i) In addition to minimizing the circuit area with the setting of $Z_1, Z_2$ and $\theta_1, \theta_2$ to other values than $50\Omega$ and $90°$ (demonstrated in (Burdin et al., 2015)), the technique proposed here makes use of $TL_1$, resulting in only two TINs as opposed to three in (Burdin et al., 2015), which is favorable for cost and reliability. ii) High linearity performances at large power levels are achieved by implementing the TINs with the anti-series-only topology of

Figure 4.1b, which overcomes the linearity degradation due to L-C parasitics. Note that $C_{LIN\,PS}$ associated to $TIN_{PS1}$ and $TIN_{PS2}$ are referred to as $C_{LIN\,PS1}$ and $C_{LIN\,PS2}$, respectively.

Next, analytical equations to compute $\Delta\phi$ are given. Section 4.1.2.2 and Section 4.2 refer to these equations for explanation and validation purposes.

The tuning of $\Delta\phi$ is enabled by $TIN_{PS1}$ and $TIN_{PS2}$ (Figure 4.2b). The reconfigurability of $TIN_{PS1}$ and $TIN_{PS2}$ as a function of the bias voltage $V_{DC\,PS}$ allows controlling the reflective load network's input impedance ($Z_{RL}$). This impedance is computed with (4.3) when $TIN_{PS1}$ and $TIN_{PS2}$ are modelled with the network in Figure 4.1b and for lossless transmission lines of electrical lengths $\theta \leq 90°$ (i.e., $\tan(\theta_1) > 0$ and $\tan(\theta_2) > 0$). In equation (4.3), $C_{01}$ and $C_{02}$ are computed with (4.1) and are the nominal capacitances of $TIN_{PS1}$ and $TIN_{PS2}$, respectively.

$$Z_{RL} = \frac{-j \cdot K_{N1} \cdot K_{N2}}{K_{12}\tan(\theta_1)\tan(\theta_2) + K_1\tan(\theta_1) + K_2\tan(\theta_2) - K_0}$$

With

$$\begin{aligned} K_{N1} &= \left[Z_1 C_{01} L_{EQ_{PS}} \omega^2 + Z_1^2 C_{01}\omega\tan(\theta_1) - Z_1\right] \\ K_{N2} &= \left[Z_2 C_{02} L_{EQ_{PS}} \omega^2 + Z_2^2 C_{02}\omega\tan(\theta_2) - Z_2\right] \end{aligned} \tag{4.3}$$

$$\begin{aligned} K_{12} &= \left(Z_1^2 C_{01} C_{02} L_{EQ_{PS}} + Z_2^2 C_{01} C_{02} L_{EQ_{PS}}\right)\omega^3 - (Z_1^2 C_{01} + Z_2^2 C_{02})\omega \\ K_1 &= \left[C_{01} C_{02} L_{EQ_{PS}}^2 \omega^4 - \left(C_{01} L_{EQ_{PS}} + C_{02} L_{EQ_{PS}} + Z_1^2 C_{01} C_{02}\right)\omega^2 + 1\right] Z_2 \\ K_2 &= \left[C_{01} C_{02} L_{EQ_{PS}}^2 \omega^4 - \left(C_{01} L_{EQ_{PS}} + C_{02} L_{EQ_{PS}} + Z_2^2 C_{01} C_{02}\right)\omega^2 + 1\right] Z_1 \\ K_0 &= 2Z_1 Z_2 C_{01} C_{02} L_{EQ_{PS}} \omega^3 - (Z_1 Z_2 C_{01} + Z_1 Z_2 C_{02})\omega \end{aligned}$$

As well-known in the literature, the maximum relative phase shift ($\Delta\phi_{MAX}$) is computed with (4.4), which is calculated from the reflection coefficient $\Gamma_{RL} = (Z_{RL} - Z_T)/(Z_{RL} + Z_T)$ at the input port of the reflective load network. In (4.4), $Z_{RL\,MIN}$ and $Z_{RL\,MAX}$ are computed with (4.3) for $V_{DC\,PS_{MIN}} = 0.5V$ and $V_{DC\,PS_{MAX}} = 20V$, respectively.

$$\Delta\phi_{MAX} = 2\left[tan^{-1}\left(\frac{Z_{RL\,MAX}}{Z_T}\right) - tan^{-1}\left(\frac{Z_{RL\,MIN}}{Z_T}\right)\right] \quad (4.4)$$

#### 4.1.2.2 Effect of key elements in the V-B RTPS on the phase shifter global performances

Here, explanations of the effect of key elements in the V-B RTPS on the phase shifter global performances are given. This is useful since the numerous design parameters involved, together with the challenge of meeting linearity performances at high power, translate into increased design complexity.

Properly adjusting $Z_T$ allows centering the circular locus of the reflection coefficient ($\Gamma_{RL} = \frac{Z_{RL}-Z_T}{Z_{RL}+Z_T}$ in Figure 4.2b), yielding improved $IL_{MAX}$ and $\Delta IL$ (Burdin et al., 2015; Lin et al., 2008). Also, $Z_T$ significantly influences $\Delta\phi_{MAX}$ through (4.4) (Burdin et al., 2015; Lin et al., 2008). The optimization of $Z_2$ and $\theta_2$ ($TL_2$) allows achieving low $IL$, low $\Delta IL$ and $\Delta\phi_{MAX} > 360°$, while using minimal circuit area (demonstrated in (Burdin et al., 2015)).

The design parameters introduced in this work are now considered. $TL_1$ and $C_{LIN\,PS}$ are explained based on simulations performed in ADS™ and plotted in Figure 4.3. Note that $FoM_{LIN}$ and $FoM_{PS}$ are defined in Section 1.4.1 and Section 1.5.1, respectively. These simulations based on S-parameters and harmonic balance include a 2-equal-tone excitation at frequencies $f_1$ and $f_2$ with a spacing of $10MHz$ and a total average input power ($P_{IN}$) of $10dBm$, as well as: i) the networks in Figure 4.2, ii) the varactor parameters of Table 3-1, iii) accounting for losses in transmission lines with electromagnetic (EM) simulations in Momentum™.

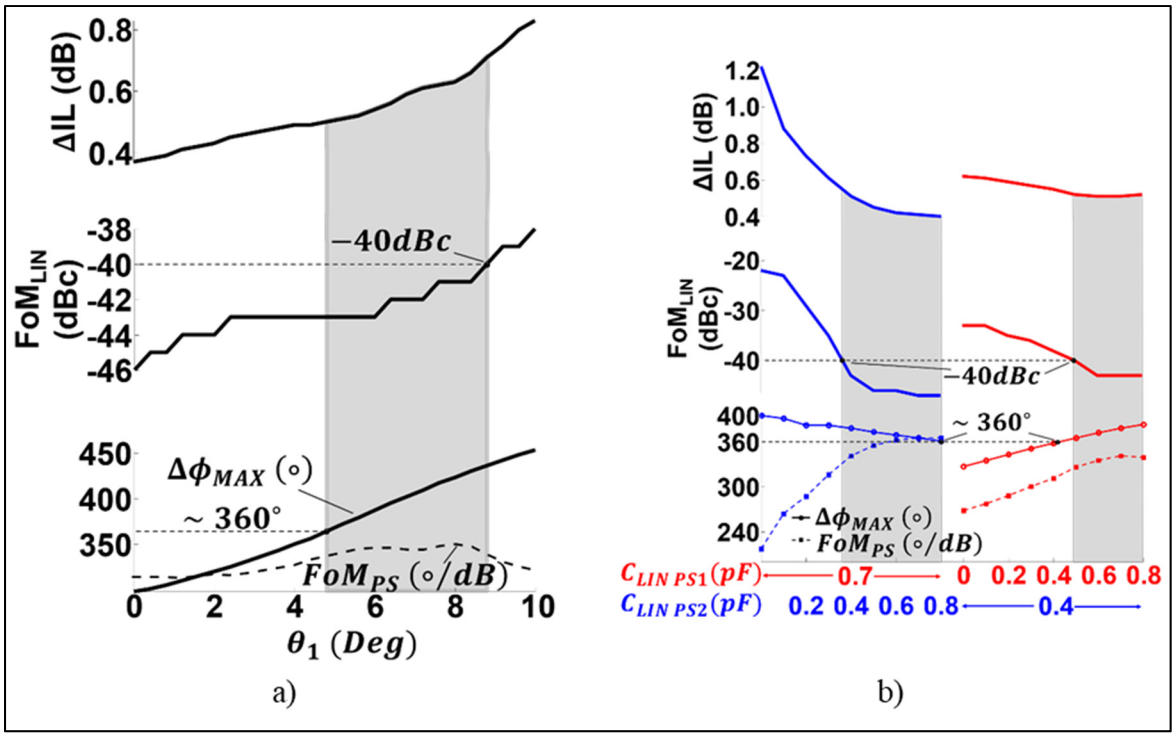



Figure 4.3 Simulation results of $\Delta\phi_{MAX}$, $FoM_{PS}$, $FoM_{LIN}$, and $\Delta IL$ a) as a function $\theta_1$ and b) as a function of $C_{LIN\ PS1}$ and $C_{LIN\ PS2}$

In Figure 4.3, the performances are plotted as a function $\theta_1$ (Figure 4.3a) and $C_{LIN\ PS1}$, $C_{LIN\ PS2}$ (Figure 4.3b) with a specific set of values for other parameters listed in Table 4.1.

Note in Figure 4.3a that $\Delta\phi_{MAX}$ increases with $\theta_1$ and $\Delta\phi_{MAX} > 360°$ is reached with $\theta_1 > 4.8°$. This justifies the addition of $TL_1$ in our technique to reach $\Delta\phi_{MAX} > 360°$ with the use of only two TINs. However, increasing $\theta_1$ has also the negative effect of increasing $FoM_{LIN}$ and $\Delta IL$. Hence, when $\theta_1$ is set within the range identified with the gray area, $FoM_{LIN} < -40dBc$ and $\Delta\phi_{MAX} \geq 360°$. The impact of $\theta_1$ on linearity stems from its influence on the magnitude of the voltage across $TIN_{PS1}$ ($v_1$ in Figure 4.2b) which in turns impacts the distortions generated by the varactor-based $TIN_{PS1}$ as demonstrated in CHAPTER 3 and (Carey-Smith & Warr, 2006).

Table 4.1 Set of design parameters for simulations of the proposed V-B RTPS network

| Parameters | Design value |
|---|---|
| $\boldsymbol{TL_{HC\,0}}$ | $Z_0 = 50\Omega$ |
| | $\theta = 90°$ |
| $\boldsymbol{TL_{HC\,A}}$ | $Z_A = 20\Omega$ |
| | $\theta = 90°$ |
| $\boldsymbol{TL_{HC\,T}}$ | $Z_T = 16\Omega$ |
| | $\theta = 90°$ |
| $\boldsymbol{TL_1}$ | $Z_1 = 103\Omega$ |
| | $\theta_1 = 5.2°$ |
| $\boldsymbol{TL_2}$ | $Z_2 = 103\Omega$ |
| | $\theta_2 = 23°$ |
| $\boldsymbol{TL_{2f0\,trap}}$ | $Z_{TRAP} \approx 95\Omega$ |
| | $\theta_{TRAP} \approx 90°$ |
| $\boldsymbol{C_{LIN\,PS1}}$ | $700fF$ |
| $\boldsymbol{C_{LIN\,PS2}}$ | $400fF$ |
| $\boldsymbol{TIN_{PS}}$ | Network of Figure 4.1 |
| **Varactors' parameters** | Table 3-1 |
| $\boldsymbol{Z_C}$ | A line-up of a 100kΩ, a 22MΩ, and a 200MΩ resistors |
| $\boldsymbol{V_{DC\,PS}}$ **range** | $0.5V\ to\ 20V$ |

The results plotted in Figure 4.3b are function of $C_{LIN\,PS1}$ (in red, with $C_{LIN\,PS2} = 0.4pF$) and $C_{LIN\,PS2}$ (in blue, with $C_{LIN\,PS1} = 0.7pF$). These results highlight the necessity of $C_{LIN\,PS1}$ and $C_{LIN\,PS2}$ in the V-B RTPS to achieve low distortion levels in the presence of L and C parasitics. Also, it is possible to demonstrate with (4.3) and (4.4) and with $\theta_1 \ll \theta_2$, that the ratio of the capacitance of $TIN_{PS1}$ (which depends on $C_{LIN\,PS1}$) over the capacitance of $TIN_{PS2}$ (which depends on $C_{LIN\,PS2}$) increases $\Delta\phi_{MAX}$. This explains why $\Delta\phi_{MAX}$ increases with $C_{LIN\,PS1}$ and decreases with $C_{LIN\,PS2}$ in Figure 4.3b.

The series parasitic $L_S$ (Figure 3.3) has similar effects as with $\theta_1$ and $\theta_2$, i.e., improving $\Delta\phi_{MAX}$ and degrading $FoM_{LIN}$ as $L_S$ increases. It is thus necessary to take into account the parasitics surrounding the diodes, since building a V-B RTPS network without considering $L_S$ risks yielding unnecessarily high $\Delta\phi_{MAX}$ and unacceptable levels of distortions.

To enhance the validity of these simulations, $\Delta\phi_{MAX}$ is computed with (4.4) using the parameters listed in Table 4.1, where $Z_{RL\ MIN}$ and $Z_{RL\ MAX}$ are calculated with (4.3). This computation yields $\Delta\phi_{MAX} = 399°$, which agrees with simulation results yielding $\Delta\phi_{MAX} = 378°$ when using the same set of parameters (Table 4.1). The difference between the computed and the simulated $\Delta\phi_{MAX}$ stems from $L_S$ being simplified with a single-equivalent $L_{EQ_{PS}}$ in the analytical analysis.

## 4.2 Experimental implementations and results

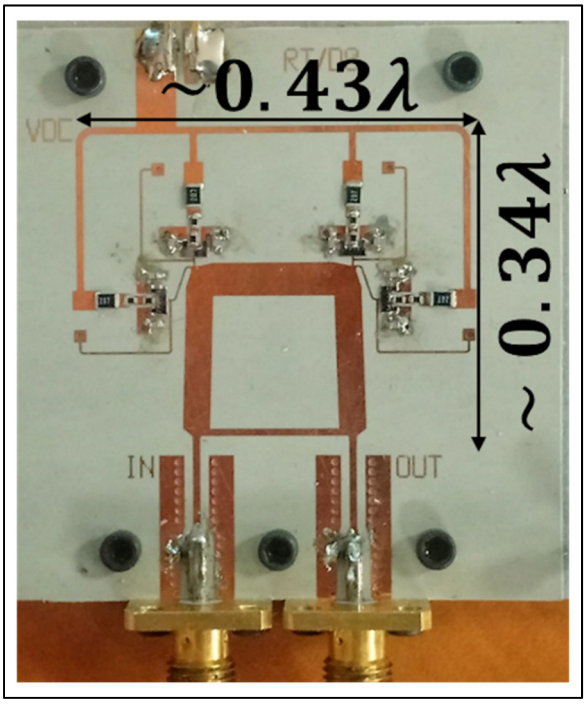



Figure 4.4 Experimentally implemented V-B RTPS network

Figure 4.4 presents the V-B RTPS network fabricated with the parameters listed in Table 4.2 on a 10mils CLTE substrate ($\varepsilon_r = 2.98$) (Roger corporation, 2020). Note that the length of all transmission lines having a large range of characteristic impedances are optimized with EM simulations in Momentum™. This explains the trapezoidal shape of the coupler as opposed to a rectangle in (Burdin et al., 2015; Lin et al., 2008). Moreover, the measured performances presented next have an excellent correlation with the simulated results of the same design in ADS™.

Table 4.2 Parameters of the fabricated V-B RTPS network

| Parameters | Physical dimensions | Electric equivalence |
|---|---|---|
| $\boldsymbol{TL_{HC\,0}}$ | $W = 26mil$ | $Z_0 = 50\Omega$ |
| | $l \approx 530mil$ | $\theta = 90°$ |
| $\boldsymbol{TL_{HC\,A}}$ | $W = 96mil$ | $Z_A = 19\Omega$ |
| | $l \approx 504mil$ | $\theta = 90°$ |
| $\boldsymbol{TL_{HC\,T}}$ | $W = 116mil$ | $Z_T = 16\Omega$ |
| | $l \approx 501mil$[*1] | $\theta = 90°$ |
| $\boldsymbol{TL_1}$ | $W = 6mil$ | $Z_1 = 103\Omega$ |
| | $l = 32mil$ | $\theta_1 = 5.2°$ |
| $\boldsymbol{TL_2}$ | $W = 6mil$ | $Z_2 = 103\Omega$ |
| | $l = 148mil$ | $\theta_2 = 23°$ |
| $\boldsymbol{TL_{2f0\,trap}}$ | $W = 8mil$ | $Z_{TRAP} \approx 94\Omega$ |
| | $l = 530mil$ | $\theta_{TRAP} \approx 87°$ |
| $\boldsymbol{C_{LIN\,PS1}}$ | $500fF$ | |
| $\boldsymbol{C_{LIN\,PS2}}$ | $200fF$ | |
| $\boldsymbol{TIN_{PS}}$ | Network of Figure 4.1a | |
| **Varactors' parameters** | Table 3-1 | |
| $\boldsymbol{Z_C}$ | A line-up of a 100kΩ, a 22MΩ, and a 200MΩ resistors | |
| $\boldsymbol{V_{DC\,PS}}$ **range** | $1V\ to\ 18V$ | |

[*1]Reduced length compared to $TL_{HC\,0}$ to account for the dependency of the transmission line electrical length as a function of its width (Gonzalez, 1996).

Figure 4.5 and Figure 4.6 presents measured and simulated $S_{11}$ and $S_{21}$, respectively, for the bias voltage $V_{DC\,PS}$ ranging from 1V to 18V. These results demonstrate that the proposed V-B RTPS achieves low $IL$ and low $\Delta IL$ at $f_0 = 3.6GHz$ and a bandwidth of 440MHz (range with $S_{11} < -10dB$).

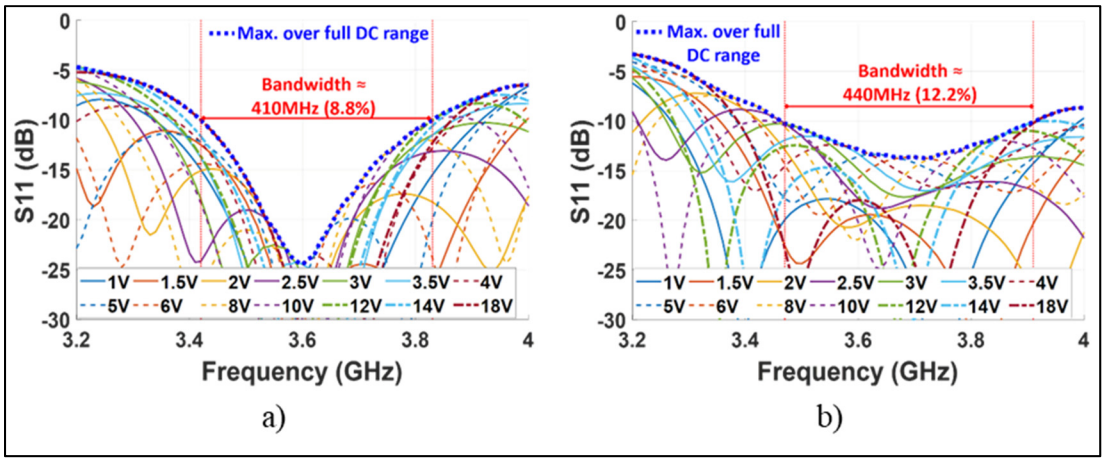



Figure 4.5 $S_{11}$ in dB as a function of frequency for values of $V_{DC\,PS}$ from 1V to 18V a) Simulated $S_{11}$ b) Measured $S_{11}$. The red vertical lines delimit the frequency bandwidth and the blue bold curve corresponds to the highest $S_{11}$ value over the full range of $V_{DC\,PS}$

Figure 4.7 plots the simulated and measured relative phase shift ($\Delta\phi$) (i.e., the phase of $S_{21}$) at $f_0$ and Figure 4.8 the $IMD_{2f2-f1}$ levels in response to a 2-equal tone signal at $f_0 \pm 5MHz$ over the full bias range. As can be seen, $\Delta\phi_{MAX} > 360°$ and that $FoM_{LIN} \leq -40dBc$ for an output power ($P_{OUT}$) of $10dBm$.`

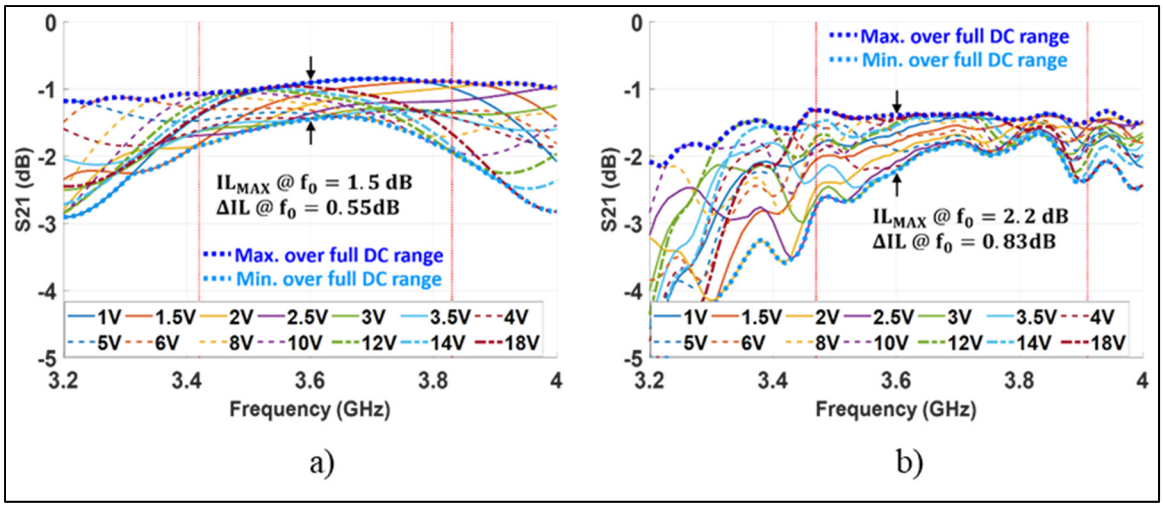



Figure 4.6 $S_{21}$ in dB as a function of frequency for values of $V_{DC\ PS}$ from 1V to 18V a) Simulated $S_{21}$ b) Measured $S_{21}$. The red vertical lines in a) and b) correspond to the bandwidth identified in Figure 4.5a and Figure 4.5b, respectively. The bold blue and bold light blue curves correspond to the highest and lowest $S_{21}$ value over the full range of $V_{DC\ PS}$, respectively

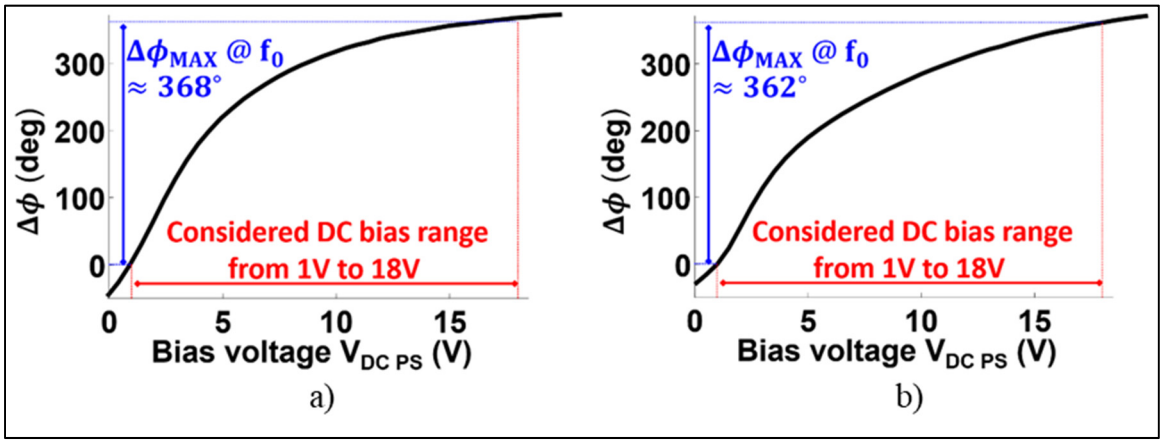



Figure 4.7 Relative phase shift (i.e., phase of $S_{21}$) at the frequency $f_0 = 3.6GHz$ as a function of the bias voltage $V_{DC\ PS}$. a) Simulated. b) Measured

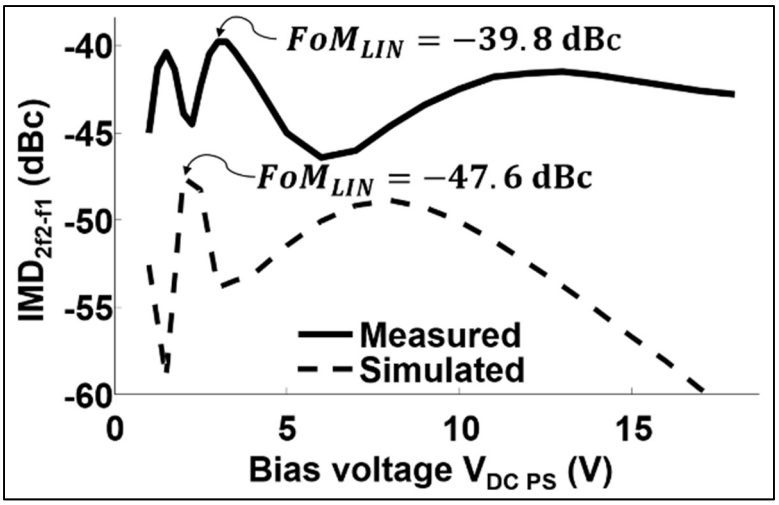



Figure 4.8 Simulated and measured $IMD_{2f2-f1}$ level over the full range of $V_{DC\ PS}$ in response to a two equal-tone signal at 3.6GHz ± 5GHz while $P_{OUT} = 10dBm$

## 4.3 Summary of performances and comparison with prior-art

The performances of the proposed V-B RTPS are summarized in Table 4.3 and compared with solutions from the literature. The single varactor topology used in (Burdin et al., 2015; Lin et al., 2008; Liu et al., 2017; Vilenskiy, Makurin, Poshisholina, & Lee, 2018) (as in most varactor-based reported solutions) implies poor linearity performances as demonstrated in the literature (e.g., (Buisman et al., 2005) for TIN only) and (Lin et al., 2008; Vilenskiy et al., 2018) are associated to high $IL$. In (Kim et al., 2008; Qureshi et al., 2007), higher linearity performances than the solutions using a single varactor topology (e.g., (Burdin et al., 2015; Liu et al., 2017)) are demonstrated at 1GHz and 2GHz in a MMIC implementation, however: i) linearity demonstrated at a single bias voltage only, ii) it uses TINs without any consideration of parasitics surrounding the diodes, hence prone to linearity degradation in discrete designs at $f_0 \geq 3.6GHz$ as demonstrated in CHAPTER 3, iii) it uses a large number of TINs, iv) $\Delta\phi_{MAX}$ is limited to 200°, and v) $IL_{MAX}$ is high. In contrast, the proposed V-B RTPS network demonstrates high linearity performances at $P_{OUT} = 10dBm$ despite the presence of significant parasitics, together with a low $IL_{MAX}$, a small $\Delta IL$, and a $\Delta\phi_{MAX} > 360°$, while minimizing the number of TINs and circuit area. This constitutes a significant improvement of the state-of-the-art.

Table 4.3 Performances of our proposed V-B RTPS and prior-art

| Ref | Technology or varactor device / TIN-T | Phase shifter topology | Goal | $f_0$ (GHz) | BW (MHz) / (%) | $\Delta\phi_{MAX}$ @ $f_0$ (°) | $IL_{MAX}$ @ $f_0$ / $\Delta IL$ @ $f_0$ (dB) / (dB) | Linearity with multi-tone signal | |
|---|---|---|---|---|---|---|---|---|---|
| | | | | | | | | Measured linearity | Bias range |
| **Burdin & al., 2015** | Discrete MA46H071 / Single varactor ✕ | RTPS IT-HC | FoM ΔIL Size | 2 ✕ | 200 / 10 | 385 | 1.56 / 1.16 | Not provided; limited to low power ✕✕ | |
| **Lin & al., 2008** | Discrete SMD Si HAV / Single varactor ✕ | RTPS IT-HC | ΔIL | 2 ✕ | 200 / 10 | 407 | ≈4.4 ✕ / ≈0.4 | Not provided; limited to low power ✕✕ | |
| **Liu & al., 2017** | Discrete BB833 / Single varactor ✕ | RTPS V-CL | BW FoM | 1.5 ✕ | 1000 / 67 | 350 | 2.6 / ≈1.8 | Not provided; limited to low power ✕✕ | |
| **Vilenskiy & al., 2018** | Discrete SMV2201 / Single varactor ✕ | RTPS HC DUAL BIAS | ΔIL | 5.8 | 600 / 10 | 360 | ≈4,6 ✕ / ≈0,6 | Not provided; limited to low power ✕✕ | |
| **Qureshi & al., Jun. 2007** | In-house MMIC SoG / Anti-series | TR-ALL-PASS | Linearity | 1 ✕ | | 30 ✕ | 0.2 / ≈0.1 | IMD3 < -56dBc @ $P_{OUT}$ = 19dBm | Measured at single bias ✕ |
| **Kim & al., 2008** | In-house MMIC SoG / Anti-series | TR-ALL-PASS | $\Delta\phi_{MAX}$ Linearity | 2 ✕ | 700 / 35 | ≈200 ✕ | 3.7 ✕ / ≈1.4 | IMD3 = -70dBc @ $P_{IN}$ = 10dBm | Measured at single bias ✕ |
| **This work** | Discrete MA46H120 / Anti-series compensated for L-C parasitics | RTPS IT-HC | Linearity FoM ΔIL Size | 3.6 | 440 / 12 | 362 | 2.2 / 0.8 | $FoM_{LIN}$ = -40dBc @ $P_{OUT}$ = 10dBm | Full bias range |

| Acronyms | | Symbols for a qualitative comparison | |
|---|---|---|---|
| BW – Bandwidth | SoG - Silicon on glass | ≈ | Data estimated from a graphic |
| HAV – Hyper abrupt varactor | TIN-T – Tunable impedance network topology | ✕ | Disadvantage with respect to this work |
| IL – Insertion loss | TR-ALL PASS - Transmission/All pass topology | ✕ | Poor linearity of single diode TIN demonstrated in (Buisman et al., 2005) |
| IT-HC - Impedance transforming hybrid coupler | V-CL - Vertical coupled line coupler | | |
| RTPS - Reflection-type phase shifter | | | |

## 4.4 Conclusion of this chapter

The proposed phase shifter in this chapter allows achieving high linearity at large power levels despite the presence of significant parasitics surrounding the diodes. The other key features ($IL_{MAX}$, $\Delta IL$, $\Delta\phi_{MAX}$) are comparable to those prior varactor-based solutions that give best performances for these features. Moreover, these prior solutions, while achieving good $IL_{MAX}$, $\Delta IL$, and $\Delta\phi_{MAX}$, are limited to poor linearity due to their single-varactor topology. Hence, the high linearity combined with good $IL_{MAX}$, $\Delta IL$, and $\Delta\phi_{MAX}$ in this work constitute a significant improvement in phase shifter techniques.

# CHAPTER 5

# VARACTOR-BASED CONTROLLABLE-GAIN GAN RF AMPLIFIER

This chapter is associated with the innovative concept of Section 2.4.3 and the required characteristics reported in Section 1.5, and it is organized as follows. Section 5.1 details the working principle of the mechanism enabling tunability of the gain over a wide range and presents the proposed controllable-gain RF amplifier. Section 5.2 presents experimental results validating the wide range of achievable gain variation and the achievement of other key required characteristics of the RF amplifier.

## 5.1 Controllable gain RF amplifier network

The proposed controllable gain RF amplifier uses the architecture presented in Figure 5.1. The reconfigurable magnitude is enabled by integrating a TIN as part of the input matching ($Z_{MATCH\ I}$) and the output matching ($Z_{MATCH\ O}$) networks and by controlling the transistor's gate bias voltage $V_G$. Both complementary mechanisms controlling the gain are detailed next.

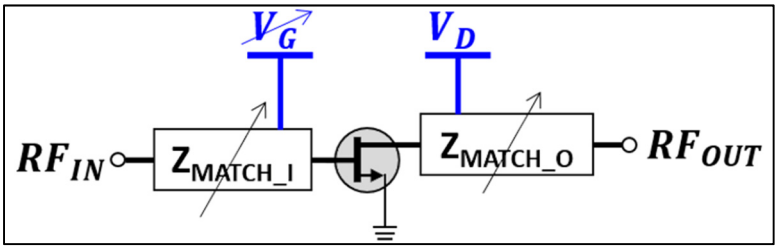



Figure 5.1 Architecture of the controllable gain RF amplifier

### 5.1.1 Controllable gain mechanism

The working principle of the first mechanism enabling control on the gain is schematized in Figure 5.2a. An ideal switch is used only for explanation purposes and is substituted with a TIN in the *real* implementation in Figure 5.2b. In Figure 5.2a, setting the switch in the ON state (short-circuit) allows power to be dissipated through a shunt lumped resistor $R_{GAIN}$, thus

increases the insertion loss between the ports $RF_1$ and $RF_2$. On the other hand, setting the switch in the OFF state (open circuit) minimizes the IL by preventing any loss through $R_{GAIN}$. In the tunable gain network in Figure 5.2b, the ideal switch is substituted by the TIN of Figure 3.14, with its capacitance being tuned with the bias voltage $V_{DC\ GS}$. A lumped capacitance ($C_{GAIN}$) is also added to adjust the capacitance range for optimal gain variation of the RF amplifier. The network in Figure 5.2b thus corresponds to an analog control of the IL between the ports $RF_1$ and $RF_2$. Setting $TIN_{GS}$ to its minimum capacitance yields minimum IL (and thus maximum gain) and vice-versa.

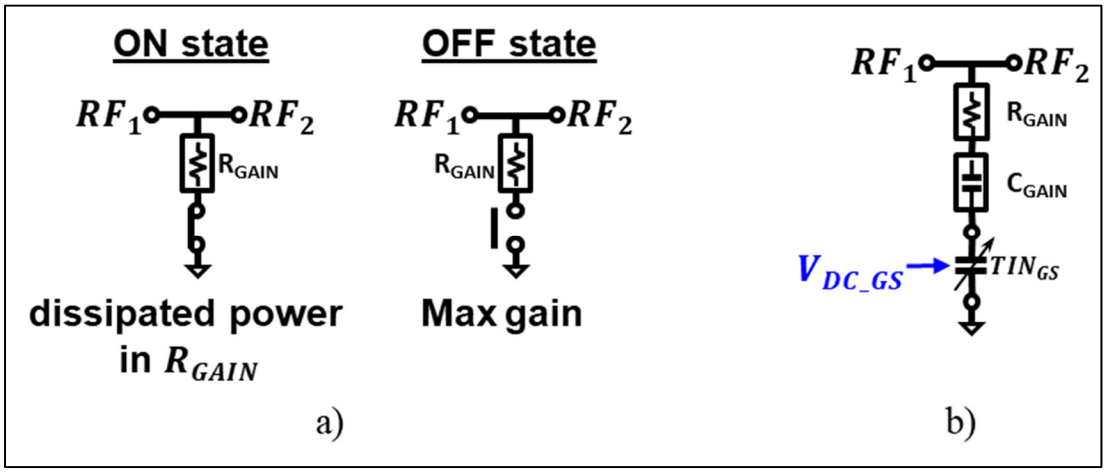



Figure 5.2 a) Schematized underlying concept of the tunable gain network. b) Real implementation of the tunable gain network

Many aspects must be carefully considered when incorporating this circuit technique into the matching networks of an amplifier to control its gain. i) The impedance matching networks must be designed so that optimum gain and maximum linear output power are obtained when the tunable gain networks are set to their minimum capacitance values, ii) $S_{11} < -10dB$ must be achieved over the full range of the bias voltage $V_{DC\ GS}$, which is an important limiting factor concerning the range of gain variation (ΔG), and iii) the TINs must not worsen the linearity performances of the RF amplifier. Aspect iii) is especially critical at maximum gain since the larger swing of the voltage RF signal across the TIN in $Z_{MATCH\_O}$ (output) risks yielding unacceptable distortion levels.

However, the $IMD_{2f_2-f_1}$-to-$V_{DC}$ relationship of the varactor-based TIN (refer to Figure 3.17b) helps in that regard since the TINs tend to intrinsically generate less nonlinearities in the bias range required to configure the RF amplifier for higher gain. This tendency is explained as follows. Observe from Figure 3.17b measured at a power as high as 18dBm, that the worst linearity (highest $IMD_{2f2-f1}$) occurs at lower bias voltages (i.e., worst linearity performances in Figure 3.17b are in the range $V_{DC} < \sim 1.5V$). On the other hand, this same bias voltage range ($V_{DC} <\sim 1.5V$) corresponds to the highest capacitance values of the TINs and thus to lower gain of the RF amplifier (i.e., to lower voltage swings across the TIN located at the output node). This tendency may also be expressed as follows: for higher gain configurations where the voltage swing across the TIN downstream the transistor tends to increase, which leads to *increased* nonlinearities generated by this TIN, corresponds to bias voltages where the TIN intrinsically tends to generate *less* nonlinearities. These two opposed tendencies avoid the situation where there is a cumulation of linearity degradation for the same bias voltage excursion.

Another important design parameter regarding aspect iii) is the value of the resistor in series with the TINs ($R_{GAIN}$). Decreasing the value of $R_{GAIN}$ simultaneously tends to *increase* (improve) the range of achievable gain variation (ΔG) and to *increase* the voltage swing across the TINs (i.e., *worsen* linearity performances). In conclusion, an optimal compromise exists between achievable ΔG and the nonlinearities generated by the TINs when selecting the value of $R_{GAIN}$.

The second mechanism consists of adjusting the RF transistor's gate bias voltage $V_G$ accordingly to the level of attenuations generated by the 1st mechanism described above (i.e., $V_G$ is set as a function of $V_{DC\,GS}$). It will be shown that properly adjusting $V_G$ vs $V_{DC\,GS}$ allows optimizing the linearity-efficiency compromise and to broaden the ΔG achieved by the 1st mechanism. The schematic of Figure 5.3 is used to explain how $V_G$ is adjusted, where the total voltage (DC plus RF) at the gate node ($v_{GATE}$) is drawn for both extreme states of maximum and minimum attenuation at a given input power level. In the minimum attenuation state, the total voltage excursion at $v_{GATE}$ is at its maximum. In this case, $V_G$ is set so that it corresponds

to the bias level (a *relatively* high value) resulting in the targeted acceptable limit of distortion level ($IMD_{MAX}$ in Figure 5.3) at the output $v_{RF_{OUT}}$, but without unnecessarily further increasing $V_G$, so as to minimize the DC consumption at the drain ($I_{DRAIN}$). This optimum linearity-efficiency compromise is schematized in Figure 5.3 with $v_{GATE}$ just reaching the threshold voltage ($V_{TH}$) of the transistor. As the attenuation within each matching network is increased with $V_{DC\ GS}$, $V_G$ is appropriately reduced so that the excursion of the total voltage (DC plus RF) at $v_{GATE}$ reaches ~exactly $V_{TH}$, thus allowing the distortion level of $v_{RF_{OUT}}$ to be maintained to ~$IMD_{MAX}$. Therefore, a quasi-optimal linearity–efficiency compromise is achieved for any value within the predetermined range of $V_{DC\ GS}$. Moreover, the reduction of $V_G$ at lower gain configurations has the additional benefit of lowering the transconductance of the transistor, which translates into a larger ΔG of the RF amplifier.

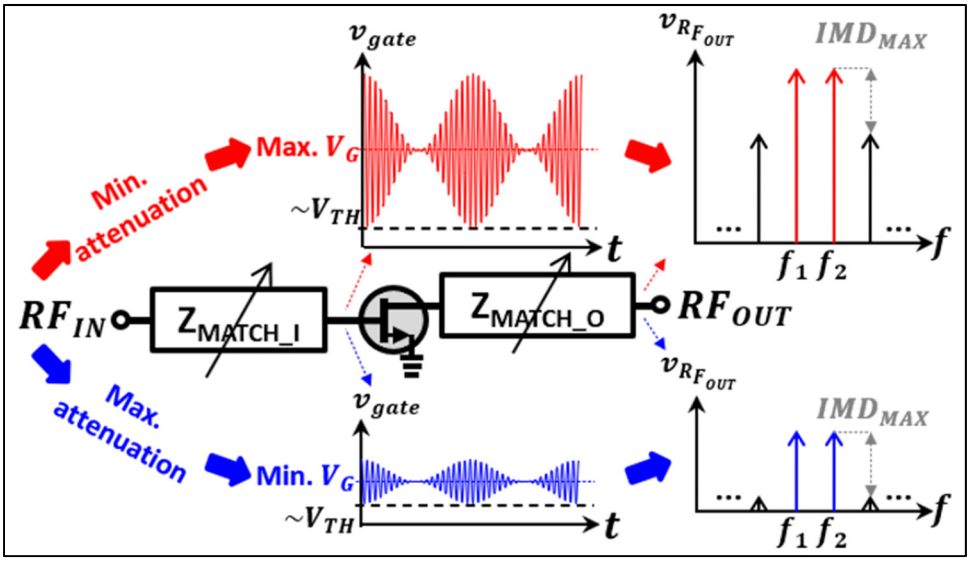



Figure 5.3 Schematic illustrating the concept of tuning the gate bias voltage $V_G$ vs $V_{DC\ GS}$ for a broadened ΔG range and optimum linearity–efficiency compromise. In red and blue are the maximum and minimum gain states, respectively

### 5.1.2 Design of the RF amplifier

The controllable gain RF amplifier and its impedance matching networks (Figure 5.4) are built with the following characteristics.

1) The transistor is a GaN HEMT CGH40006S from Cree™/Wolfspeed™ (Wolfspeed, 2021) because of its large current density capability.
2) The input and output impedances are matched with L-configuration LC networks for minimum component usage and circuit area.
3) An RLC trap filter, a series RC high pass filter, and a series resistor ($R_{STAB}$) are used in the input matching network to ensure the amplifier's stability.
4) Both DC feeds consist of a quarter-wave transmission line ended with a shunt capacitor. A resistor ($R_{CHOKE}$) is added in series of this DC feed for the biasing of the gate.
5) A tunable gain network (Figure 5.2b) controlled with the bias voltage $V_{DC\,GS}$ is included in both matching networks, where $TIN_{GS1}$ and $TIN_{GS2}$ are implemented with the TIN of Figure 3.14 with $s = 3$. Components $C_{LIN}$ associated with $TIN_{GS1}$ and $TIN_{GS2}$ are referred to as $C_{LIN\,GS1}$ and $C_{LIN\,GS2}$, respectively.
6) The bias voltage at the drain is set to $V_D = 10V$ to ensure an operation in the saturated region.

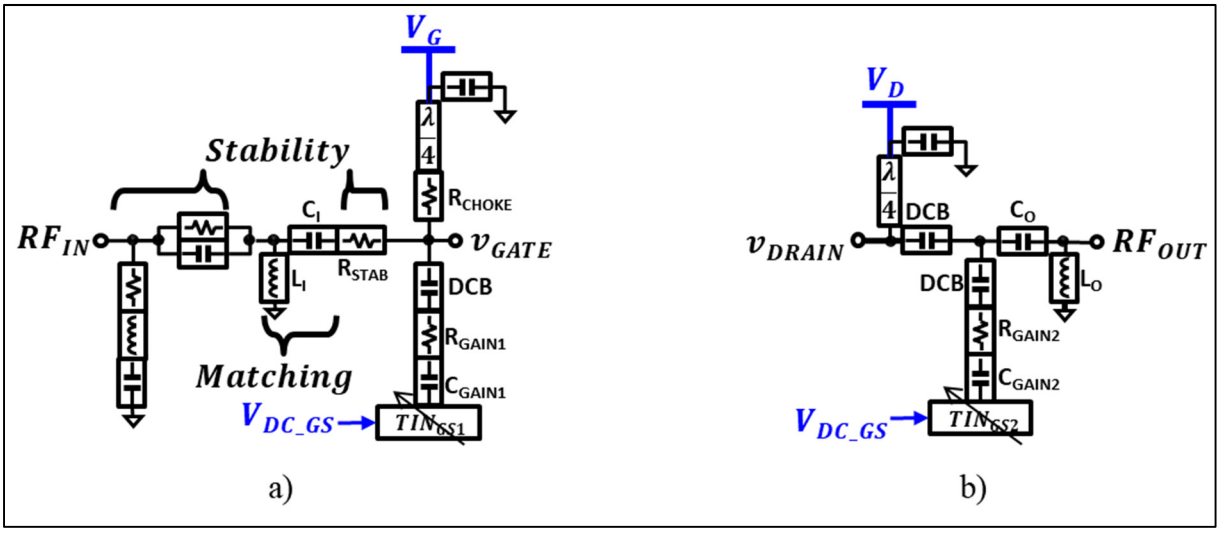



Figure 5.4 Schematics of a) the input matching network and b) the output matching network

## 5.2 Experimental implementation and results

The controllable-gain RF amplifier is fabricated on a 10mils CLTE ($\varepsilon_r = 2.98$) substrate (Roger corporation, 2020) with the parameters listed in Table 5.1. A photo of this network is presented in Figure 5.5, where the identified dimensions show it can be implemented into a $\lambda/2 \times \lambda/2$ RTA unit-cell.

Table 5.1 Electronic parameters of the fabricated RF amplifier

| Parameter | Value | Parameter | Value |
|---|---|---|---|
| $R_{CHOKE}$ | $75\Omega$ | $R_{GAIN1}$ | $10\Omega$ |
| $R_{STAB}$ | $3\Omega$ | $R_{GAIN2}$ | $5.1\Omega$ |
| $L_I$ | $2.2nH$ | $C_{GAIN1}$ | $2pF$ |
| $C_I$ | $0.9pF$ | $C_{GAIN2}$ | $0.3pF$ |
| $L_O$ | $3.9nH$ | $C_{LIN\ GS1}$ | $0.4pF$ |
| $C_O$ | $3pF$ | $C_{LIN\ GS2}$ | $0.4pF$ |

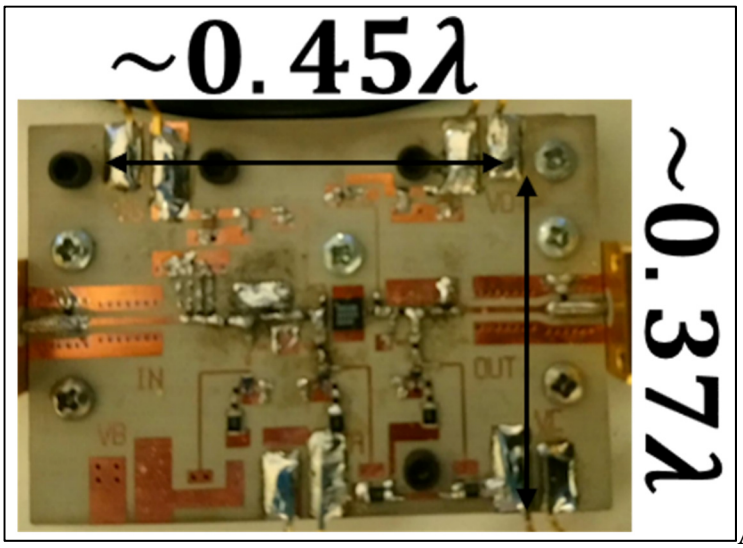



Figure 5.5 Experimentally implemented controllable-gain RF amplifier

The key performances of the fabricated RF amplifier presented next are measured in the condition where $V_G$ is set to the value that optimizes the linearity–efficiency (i.e., minimum $I_{DRAIN}$) compromise for every given value of $V_{DC\ GS}$. Here, these optimum values correspond to the lowest $V_G$ value that allows $IMD_{2f2-f1} < -40dBc$. The $V_G$–$V_{DC\ GS}$ profile for optimum linearity–efficiency is plotted in Figure 5.6 over a range of $V_{DC\ GS}$ from 0V to 20V. As mentioned in Section 5.1.1, this $V_G$–$V_{DC\ GS}$ profile also broadens the range of gain variation.

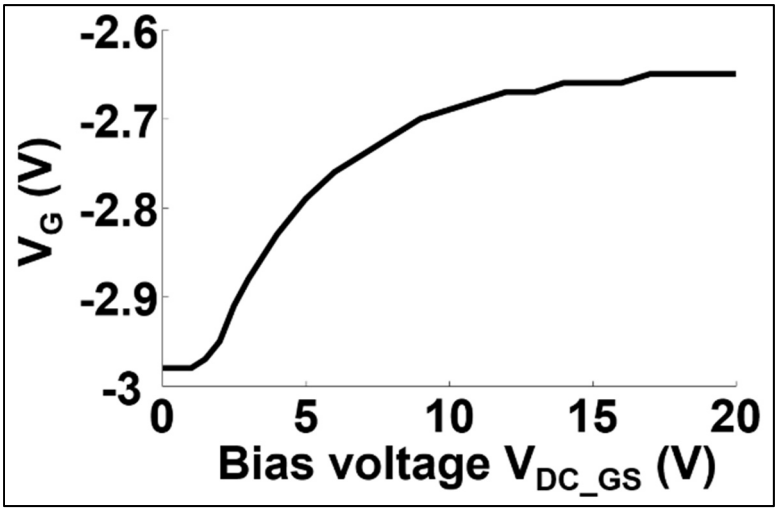



Figure 5.6 Gate bias voltage $V_G$ profile as a function of the bias voltage $V_{DC\ GS}$ to maintain the optimum linearity–energy efficiency compromise

Figure 5.7 presents the S-parameters over a wide range of frequencies and a bias voltage $V_{DC\ GS}$ ranging from 1V to 20V. These results demonstrate that at $f_0 = 3.6GHz$ i) $S_{11} < -10dB$ over the full range of $V_{DC\ GS}$, ii) the maximum small-signal gain is $S_{21\ MAX} = 8.1dB$, and iii) the range of gain variation (ΔG) at low power is $\Delta S_{21} = 9.9dB$.

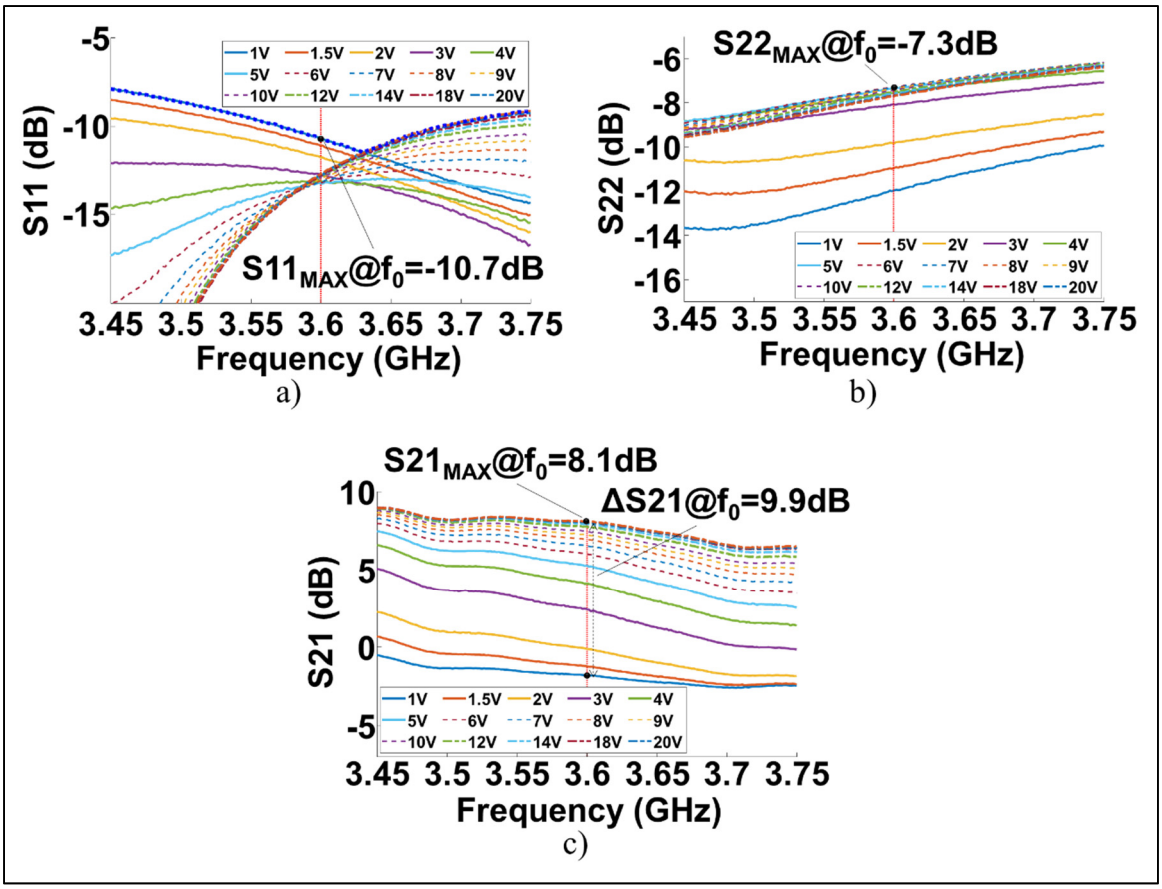



Figure 5.7 Measured s-parameters in dB for a range of bias voltage $V_{DC\,GS}$ from 1V to 20V when using the profile of $V_G$ given in Figure 5.6. a) $S_{11}$, b) $S_{22}$, and c) $S_{21}$

The measured $IMD_{2f2-f1}$ over $V_{DC\,GS}$ plotted in Figure 5.8b confirms that the $V_G$–$V_{DC\,GS}$ profile in Figure 5.6 is adequately adjusted, since $IMD_{2f2-f1}$ is maintained in the vicinity of $-40dBc$ over the full range of $V_{DC\,GS}$.

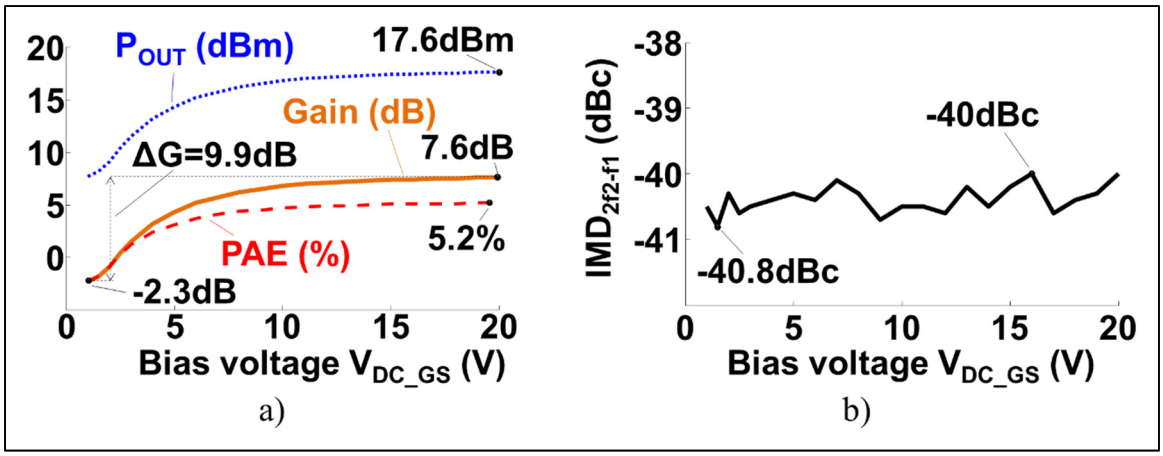



Figure 5.8 Measured a) gain, $P_{OUT}$, and PAE, and b) $IMD_{2f2\text{-}f1}$ level at a fixed input power of 10dBm as a function of the bias voltage $V_{DC\ GS}$ when using the profile of $V_G$ given in Figure 5.6

## 5.3 Summary of measured performances

The proposed RTA unit-cell in the next chapter takes advantage of the innovative performances achieved by the controllable-gain RF amplifier proposed in this chapter. The demonstrated measured performances associated with this novel amplifier are summarized in Table 5.2 and show the capability of delivering a linear RF signal at an output power as high as 17.6dBm, while achieving a gain variation over a range as wide as 9.9dB.

Table 5.2 Measured performances of the controllable gain RF amplifier at $f_0 = 3.6GHz$

| Type of measurement | Performance | Measured |
|---|---|---|
| Small signal S-parameters | $S_{11\ MAX}$ | $-10.7dB$ |
| | $S_{22\ MAX}$ | -7.3dB |
| | $S_{21\ MAX}$ | $8.1dB$ |
| | $\Delta S_{21}$ | $9.9dB$ |
| Two equal-tone RF excitation with $IMD_{2f2-f1} \leq -40dBc$ @ $P_{IN} = 10dBm$ | $P_{LIN\ MAX}$ | $17.6dBm$ |
| | $Gain_{MAX}$ | $7.6dB$ |
| | $\Delta G$ | $9.9dB$ |
| | $PAE\ @\ Gain_{MAX}$ | 5.2% |

# CHAPTER 6

# PROPOSED RTA UNIT-CELL AND OPPORTUNITIES FOR NOVEL RTA ANTENNA SYSTEM FEATURES

This chapter, associated with the innovative concept of Section 2.4.3, proposes an RTA unit-cell using the architecture described in Section 6.1. Then, based on experimental results measured with the test bench detailed in Section 6.2, Section 6.3 analyses potential system-level benefits of implementing our proposed unit-cell in an RTA antenna system.

## 6.1 RTA unit-cell architecture

The architecture of the proposed RTA unit-cell presented in Figure 6.1 consists of two novel controllable RF networks, one controlling the phase followed by another amplifying the signal and controlling the magnitude, enclosed between two standard rectangular patches behaving as the receiving and the transmitting antennas. It is shown in this chapter that this proposed unit-cell consists of a significant improvement of the state-of-the-art.

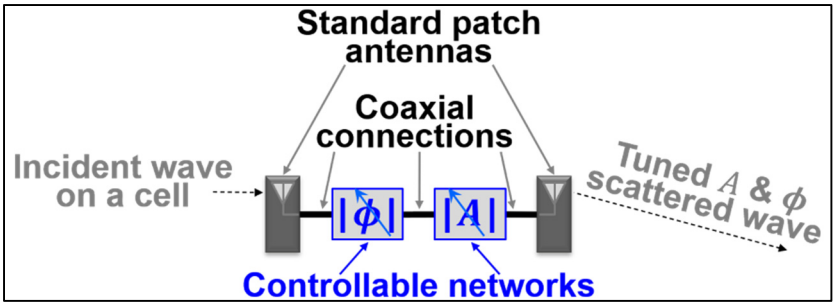



Figure 6.1 Architecture of the proposed RTA unit-cell

## 6.2 Experimental implementation and measurement test bench

The proposed RTA unit-cell using the architecture in Figure 6.1 is at a prototype development stage and is built by series-stacking individual circuit blocs linked with SMA connections. The patch antennas have dimensions of 1060mils×1327mils and are fabricated on an RT/Duroid

6002 ($\varepsilon_R = 1.99$) substrate and both controllable networks are implemented with the V-B RTPS of CHAPTER 4 and the controllable-gain RF amplifier of CHAPTER 5.

To measure the achievable performances by our proposed RTA unit-cell, the Rx and Tx patch antennas are mounted at the end of two rectangular waveguides (RWG), as shown in the test bench depicted in Figure 6.2a. In this test bench, RW-I and A-I are the RWG and the patch antenna upstream of the controllable networks, respectively, while the RWG RW-O and the patch antenna A-O are downstream of the controllable networks. Moreover, a waveguide-to-SMA adapter is mounted at the other end of both RWGs to excite the unit-cell at the port $RF_{IN}$ and measure the transmitted signal at the port $RF_{OUT}$. Such RWG-based test bench method emulates the impedance and boundary conditions of a unit-cell positioned in the center of an infinite aperture (Lau & Hum, 2012a).

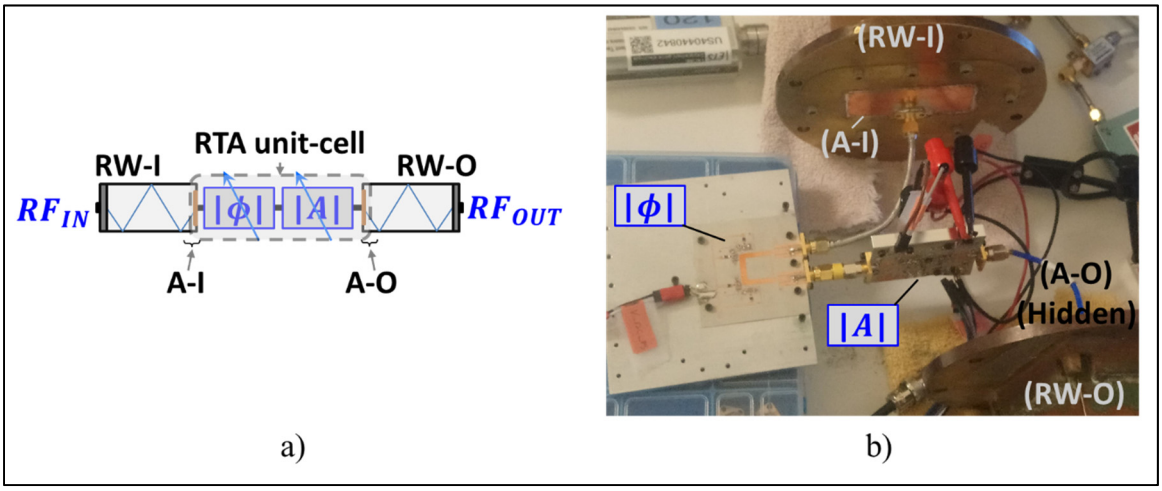



Figure 6.2 Test bench to measure the performances of the proposed RTA unit-cell.
a) Schematic b) Photo of the fabricated test bench

Figure 6.2b presents a photo of the experimental implementation of this test bench, where the key parts are identified.

## 6.3 Measured performances and opportunities for novel RTA antenna system features

The proposed RTA unit-cell (Figure 6.1) achieves performances that provide numerous opportunities for novel features at the level of an RTA antenna system, e.g., complex patterns of the scattered field, improve antenna efficiency, lower SLL, etc. Four examples of such novel features are analyzed in this section and quantified based on measured performances demonstrating that the proposed RTA unit-cell is highly relevant for RTA systems design. In addition, this section is concluded by summarizing achieved performances by the proposed RTA unit-cell, supporting that it constitutes a significant improvement of the state-of-the-art.

### 6.3.1 Enhanced maximum delivered linear power

Here, the maximum delivered linear power ($P_{LIN\ MAX}$) by the proposed unit-cell is quantified when measured in the test bench of Figure 6.2 in the condition where the RF amplifier is set to its maximum gain with $V_{DC\ GS} = 20V$ and $V_G = -2.65V$. $P_{LIN\ MAX}$ is defined as the maximum output power level at which $IMD_{2f2-f1} < -40dBc$ in response to a 2-equal tone excitation centred at 3.6GHz and with a 10MHz spacing between the tones.

Figure 6.3 plots measured $P_{LIN\ MAX}$ levels over the full range of the bias voltage $V_{DC\ PS}$, thus over a range of $\Delta\phi \approx 360°$, where $P_{LIN\ MAX}$ is between 13.7dBm and 19.1dBm depending on $V_{DC\ PS}$. Such high delivered linear output power levels constitute a significant improvement of the state-of-the-art for a varactor-based reconfigurable RTA unit-cell, extending the use of varactor-based RTA antenna systems to transmitter applications. In contrast, most reported solutions are restricted to low-power applications.

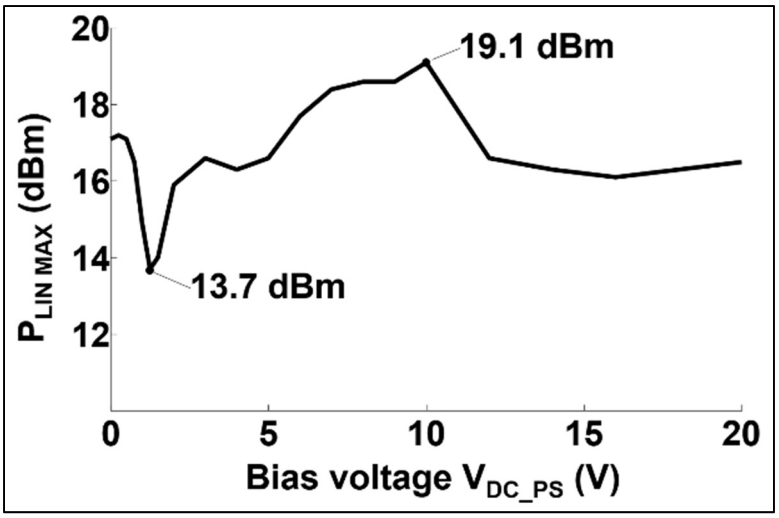



Figure 6.3 Maximum delivered linear power ($P_{LIN\ MAX}$) over the full range of the bias voltage $V_{DC\ PS}$

In Figure 6.3, $P_{LIN\ MAX}$ varies significantly due to the V-B RTPS IL and distortion level being dependent on $V_{DC\ PS}$ (refer to Figure 4.6 and Figure 4.8 in CHAPTER 4).

### 6.3.2 Constant output power by compensating the ΔIL of the V-B RTPS

Authors in (Lau & Hum, 2012a) mention that minimizing the phase shifter ΔIL allows reducing the magnitude of the undesired side lodes generated by a reconfigurable specially-fed antenna system. Here, the controllable-gain amplifier gives the opportunity of a ~*constant* power at the output of a unit-cell over the full range of $\Delta\phi_{MAX}$. This is possible by adjusting the bias voltage $V_{DC\ GS}$ so that the controllable gain of the RF amplifier cancels out the ΔIL of the V-B RTPS.

Figure 6.4 presents the highest and lowest achievable *constant* output power for a given input power of 10.5dBm, where $V_G = -2.55V$ and $V_G = -2.73V$ for both extreme cases, respectively. The curves $V_{DC\ GS\ MAX}$ and $V_{DC\ GS\ MIN}$ illustrate how $V_{DC\ GS}$ is tuned as a function of $V_{DC\ PS}$, in order to compensate the V-B RTPS ΔIL, yielding the maximum ($P_{OUT\ MAX}$) or minimum ($P_{OUT\ MIN}$) constant output power. Moreover, because the RF amplifier ΔG (~9.9dB reported in Table 5.2) is greater than the small V-B RTPS ΔIL (~0.8dB reported in Table 4.3), our proposed RTA unit-cell allows a range of gain variation of $\Delta G = 6.2dB$. This ΔG is

therefore achieved while maintaining a constant output power (minimum or maximum) and a high level of linearity.

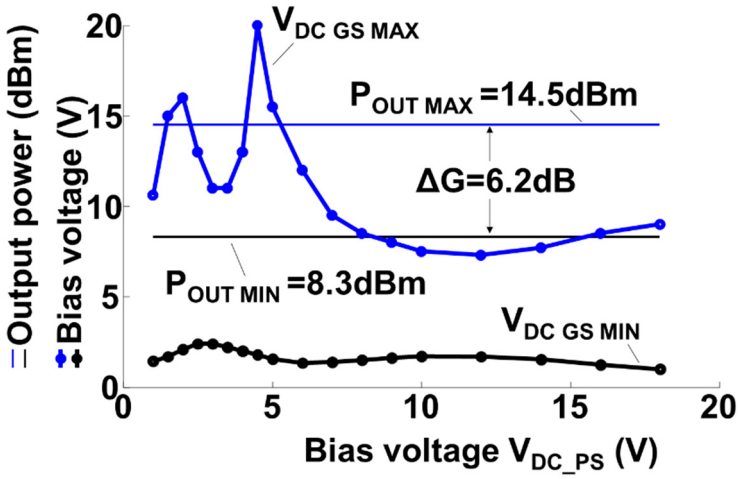



Figure 6.4 Maximum and minimum achievable constant output power levels of the proposed RTA unit-cell for a given input power of 10.5dBm

To the best of the author's knowledge, the performances reported in Figure 6.4, achieved while delivering a highly linear output signal, were never demonstrated in the literature for a reconfigurable RTA unit-cell.

### 6.3.3 Improved antenna efficiency

This section demonstrates, with computations based on measured performances, that implementing a tapered gain from the unit-cells at the center of an aperture to those at the edge of the same aperture, with use of the controllable-gain amplifier design presented above, allows mitigating the well-known problem of limited antenna efficiency ($\eta_a$) associated with planar apertures. Note that the expression (1.2) defining $\eta_a$ is given in Section 1.4.2.

The analysis presented next uses a gain taper of 6.2dB from the center to the edge of a circular aperture. This gain taper corresponds to the available tunable gain for all unit-cells while maintaining a constant output power *for any phase shift* (Section 6.3.2). In other words,

$\Delta G = 6.2dB$ is available for all unit-cells without influencing its delivered power even though each cell requires a different $\Delta\phi$ depending on its position on the aperture (deduced from the theory described in Section 1.1.1).

Moreover, even though a normalization is used in the following analysis so that the maximum incoming power on the aperture is equalled to 0dBm, it is, in fact, valid as long as the power at the input of all unit-cells is 10.5dBm or lower. Also, this analysis considers that the gain of each cell does not depends on the power level at its input port. This is because $\Delta G = 6.2dB$ is demonstrated at $P_{IN} = 10.5dBm$ (i.e., the power at the amplifier's input is $10.5dBm - IL_{ANT\,I} - IL_{PS}$), a power that is at a significant back-off level from the amplifier's $P_{1dB}$ to achieve high linearity, i.e., in a power region where the gain is ~flat. This approximation is supported by the results in Table 5.2 where $\Delta S_{21} \approx \Delta G_{@P_{IN}=10dBm}$.

Figure 6.5 illustrates the effect of implementing a tapered gain in the center-feed circular aperture system depicted in Figure 1.7a, where the feed and the cells use the radiation patterns described in Section 1.4.3. In Figure 6.5, $\alpha = 0.6186rad$ because it optimizes $\eta_a$ when considering a gain taper of 6.2dB.

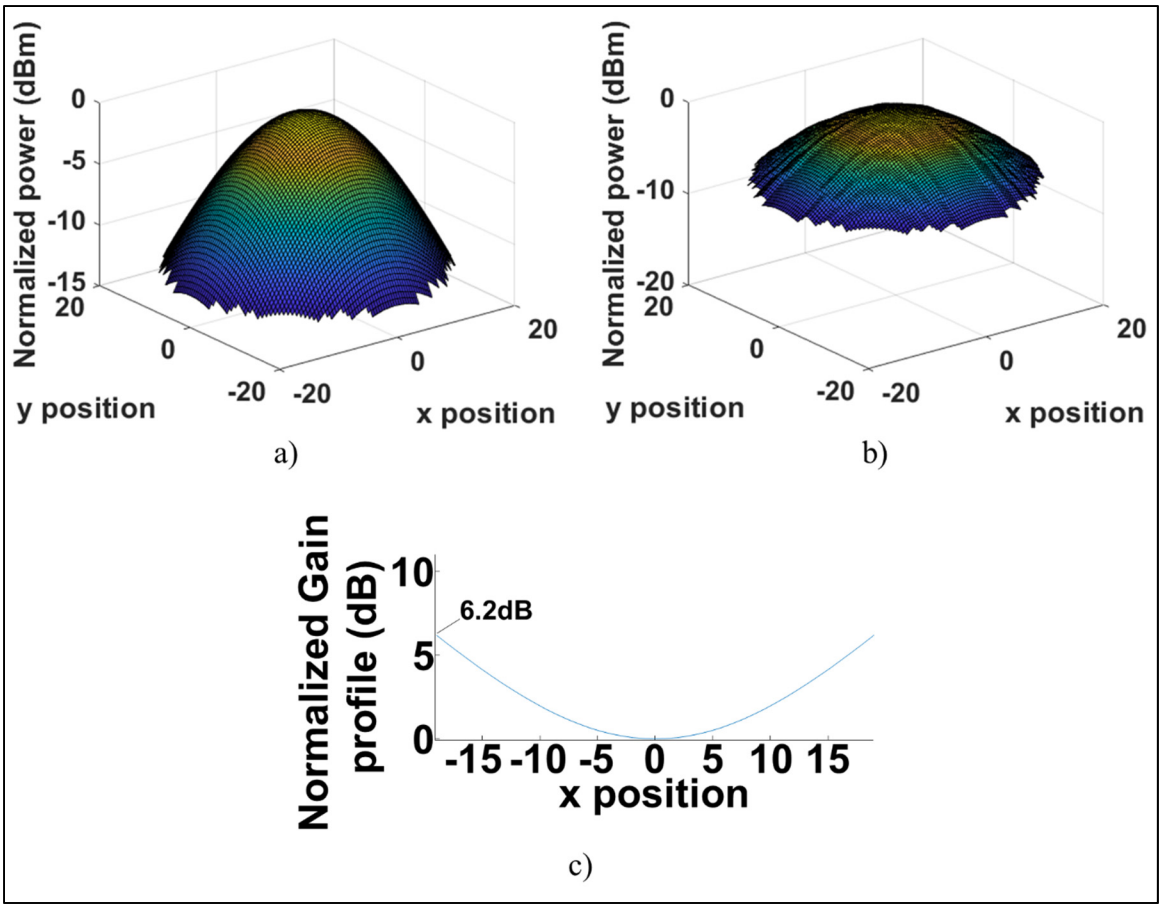



Figure 6.5 Illustration of the implementation of a gain profile while considering $\alpha = 0.6186rad$. a) Incident power on the circular aperture, b) 2D cut of the applied gain profile, and c) resulting compensated scattered field

Figure 6.5a is the incoming field on the circular aperture. Observe that the center-edge taper of the incoming field is ~13.7dB as a result, in part, of $\alpha = 0.6186rad$. Figure 6.5b is a 2D cut of the gain taper implemented across the aperture. Figure 6.5c is the resulting compensated scattered field transmitted by the RTA antenna system. The gain taper profile is the same as the incoming field but in opposition and limited to a taper of 6.2dB. Consequently, it enhances the $\eta_i$ of the transmitted field, yielding improved $\eta_a$. It is worth mentioning that these 3D curves are plotted with MATLAB™ based on the equations given in (Yu et al., 2010).

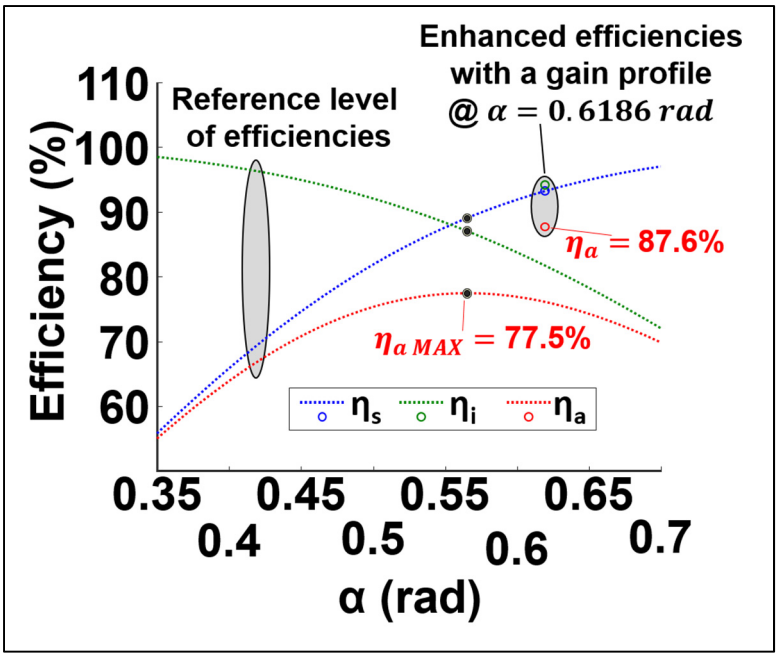



Figure 6.6 $\eta_i$, $\eta_s$, and $\eta_a$ over the half angle $\alpha$.
Results plotted with dotted curves are
taken from Yu et al. (2010)

The computed efficiencies presented in (Yu et al., 2010) (also described in Section 1.4.3) based on lossless non-amplifying unit-cells, are here used as a reference. Figure 6.6 plots the efficiencies reported in (Yu et al., 2010) (dashed curves) over a range of $\alpha$ from 0.35rad to 0.7rad and the resulting efficiencies when applying the gain profile described above (Figure 6.5). The results in Figure 6.6 demonstrates that the compensated system improves $\eta_a$ by ~10%, thanks to the opportunity of a tunable magnitude by our proposed RTA unit-cell. To the best of our knowledge, it is the first time an improvement of $\eta_a$ of a reconfigurable planar aperture is demonstrated through system-level simulations that are based on measured performances of the unit cells.

### 6.3.4 Optimized antenna energy efficiency

The impact of including a gain stage in each unit-cell on the energy efficiency ($\eta_{SYS}$ computed with (1.3)) is investigated here. This investigation considers the system in Figure 6.7, which is the same system as in Figure 1.8 (section 1.4.4), but with i) $\eta_{PA} = 20\%$, ii) the block "PA-A

losses" swept from 0 to -7dB, iii) $[m \times n] = 283$ unit-cells corresponding to a ~1.5m diameter circular aperture for a pitch of $\frac{\lambda}{2}$ between each unit-cell at 3.6GHz, and iv) the unit-cell modelled with the architecture of Figure 6.1 based on measured performances with the test bench of Figure 6.2, including the losses $IL_{ANT\ I}$, $IL_{ANT\ O}$, and $IL_{PS}$ of both antennas and the V-B RTPS, respectively, and an amplification function with a gain of $G_{GS}$ consuming the DC power $P_{DC\ GS}$. Note that these losses and this $G_{GS}$ involved in iv) dictate the gain between the powers $P_{[m,n]_{OUT}}$ and $P_{[m,n]_{IN}}$ involved in (1.3), thus have a significant influence on $\eta_A$.

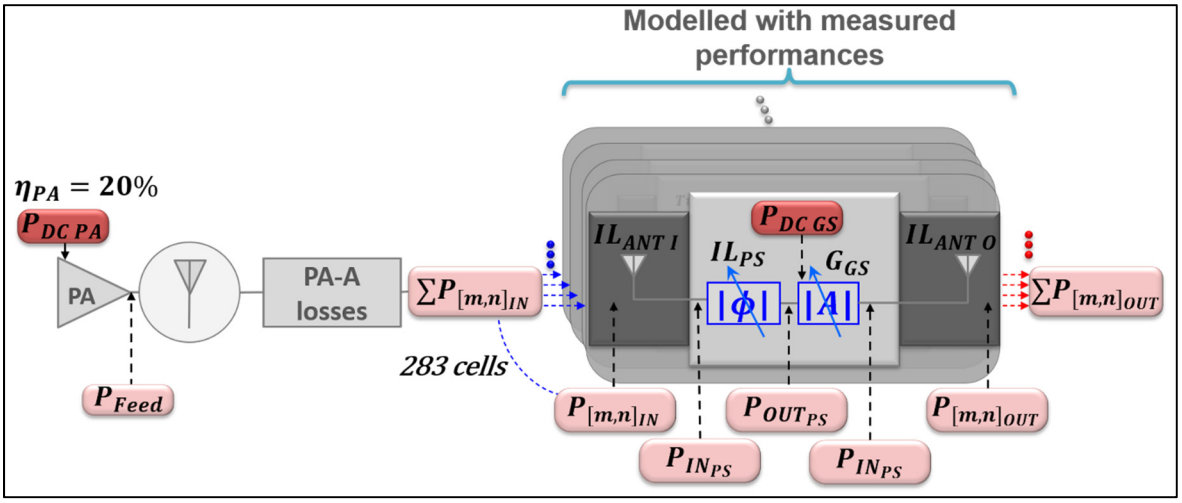



Figure 6.7 Considered antenna system to compute $\eta_{SYS}$

The impact of the amplifier stage is evaluated by comparing the computed $\eta_{SYS}$ of a "Case 1" using Figure 6.7 with the amplifier's gain set to its maximum (i.e., $V_{DC\ GS} = 20V$ for all measured performances), to the computed $\eta_{SYS}$ of a "Case 2" also using Figure 6.7, but with $G_{GS} = 0dB$ and $P_{DC\ GS} = 0W$. This configuration means that "Case 2" uses the same measured performances as "Case 1", but with the gain stage removed. Moreover, for a fair comparison, the total output power ($\sum P_{[m,n]_{OUT}}$) is equal for both cases.

"Case 1" and "Case 2" are analyzed for the lowest and highest levels of $IL_{PS}$ (i.e., two sets of measurements are used, one with $V_{DC\ PS}$ adjusted so that $IL_{PS} = IL_{PS_{MIN}}$ and the other with $V_{DC\ PS}$ adjusted so that $IL_{PS} = IL_{PS_{MAX}}$). Performances measured with the test bench of

Figure 6.2 for $IL_{PS_{MIN}}$ and $IL_{PS_{MAX}}$ are given in Table 6.1. The input power level is maximized to the extent of satisfying $IMD_{2f2-f1} < -40dBc$, thus corresponding to $P_{LIN\ MAX}$ as defined in Section 6.3.1. The screenshots of measured power spectrums at the output of the RTA unit-cell in Figure 6.8 support the fact that these performances correspond to $P_{LIN\ MAX}$ since $IMD_{2f2-f1} \approx -40dBc$.

Table 6.1 Measured performances of the RTA unit-cell to evaluate $\eta_{SYS}$

| **Parameter** | **Measured performances for lowest *IL* of the V-B RTPS** | **Measured performances for highest *IL* of the V-B RTPS** |
|---|---|---|
| $V_{DC\ PS}$ | 10V | 4V |
| $V_{DC\ GS}$ | 20V (Max gain) | 20V (Max gain) |
| $P_{DC\ GS}$ | 1.29W | 1.26W |
| $IL_{A-I}$ | - 0.4dB | - 0.4dB |
| $IL_{PS}$ | - 1.3dB (i.e., $IL_{PS_{MIN}}$) | - 2.5dB (i.e., $IL_{PS_{MAX}}$) |
| $G_{GS}$ | 8dB | 7.7dB |
| $PAE_{G_{GS}}$ | 1.8%* | 1.3%* |
| $IL_{ANT\ O}$ | - 1dB | - 0.7dB |
| $P_{[m,n]_{IN}}$ | 9.9dBm | 12.1dBm |
| $P_{[m,n]_{OUT}}$ | 15.2dBm | 16.2dBm |
| $IMD_{2f2-f1}$ | -40.1dBc | -40.3dBc |

* Lower values than reported in Figure 5.8a due to a lower power level at the gain stage input.

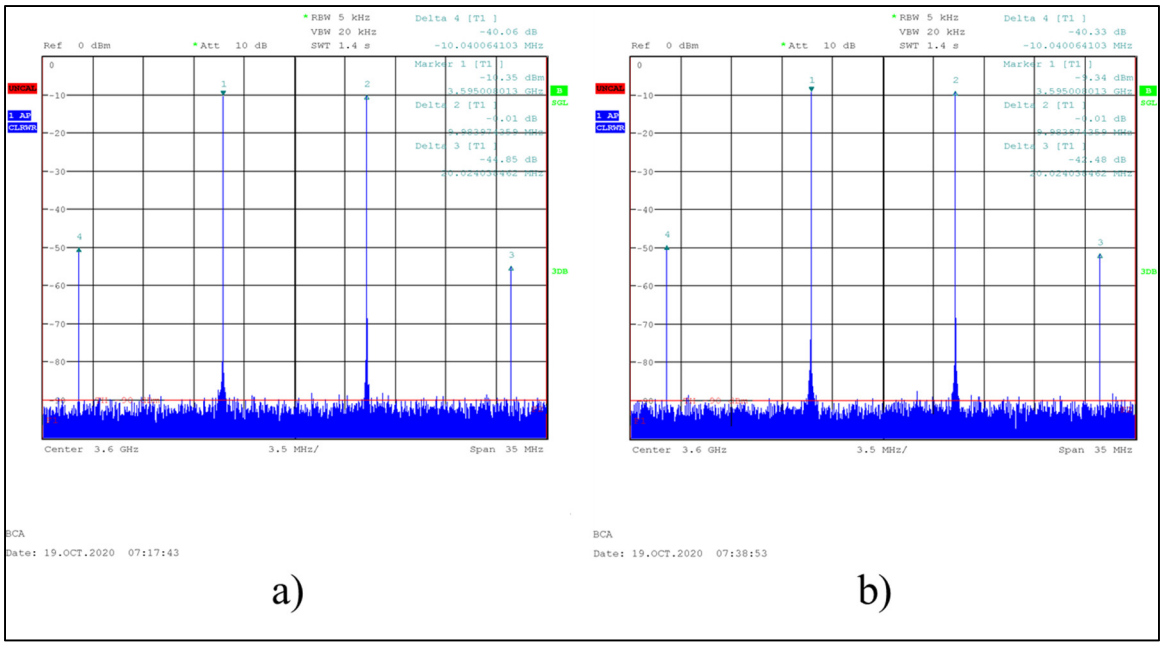



Figure 6.8 Screenshots of the measured power spectrum at the output of the proposed RTA unit-cell. a) Case 1 – Lowest IL of the V-B RTPS. b) Case 2 – Highest IL of the V-B RTPS. The measured total power is lower due to attenuators used for protection of the spectrum analyzer

Figure 6.9 plots the resulting $\eta_{SYS}$ for "Case 1" and "Case 2" computed with (1.3) for "PA-A Loss" swept from 0dB to -7dB when considering the measured performances listed in Table 6.1 for both extreme levels of $IL_{PS}$.

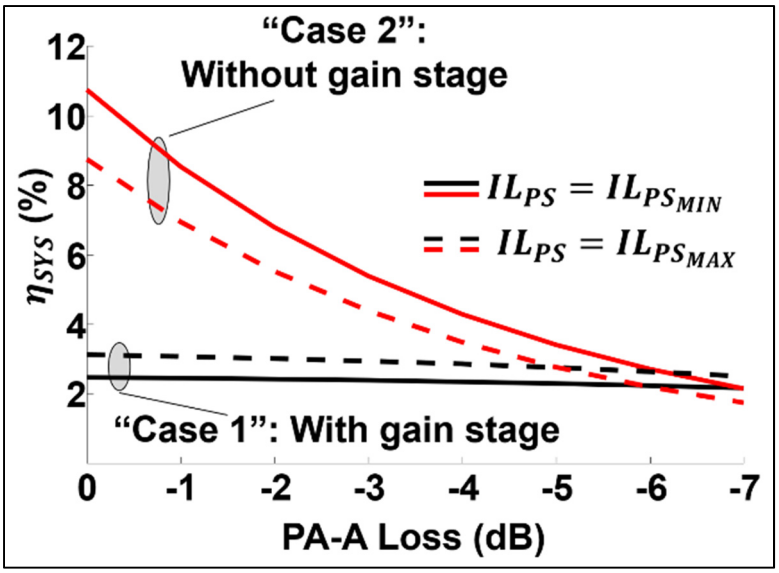



Figure 6.9 Computed $\eta_{SYS}$ for both cases under investigation (with and without gain stages) based on the measured performances given in Table 6.1

These computed $\eta_{SYS}$ use a system including simplifications (e.g., uniform illumination) and depends on many factors and parameters (e.g., $\eta_{PA} = 20\%$, maximum gain state, etc.) that vary significantly from an RTA antenna system to another. Nonetheless, it shows that in the conditions where the losses upstream the gain stage are large (e.g., -5dB to -7dB in Figure 6.9), that $\eta_{SYS}$ of both systems becomes ~equivalent (in Figure 6.9, the $\eta_{SYS}$ of "Case 1" is even higher than the $\eta_{SYS}$ of "Case 2" for $IL_{PS_{MAX}}$). This is despite the fact that the gain stage PAE is only ~1.8% or lower (Table 6.1). The limited impact of using amplifiers in each RTA unit-cell stems mainly from the reduced linear losses of the blocks preceding (upstream) the gain stages (V-B RTPS, A-I, and "PA-A losses"). These results also suggest that linear amplifier design techniques with improved efficiencies would benefit to the type of amplifying RTA systems considered here, rendering the amplifying RTA systems even more attractive.

Moreover, the "PA-A losses" range where "Case 1" compares less favourably with "Case 2" (e.g., from 0dB to ~ -3dB) corresponds to systems that are assumed to have extremely low losses, hence that are difficult, or even impossible, to realize. Consequently, this demonstrates

that amplifying-based RTA antenna systems have the benefit of reducing significantly the negative impact on $\eta_{SYS}$ of all the losses upstream of the RF amplifier in each unit-cell.

### 6.3.5 Summary of achievable performances by the proposed RTA unit-cell

The key performances of the proposed RTA unit-cell reported in this chapter are summarized in Table 6.2. Such an innovative set of performances demonstrating possible operations at large power levels while controlling the phase over a range of 360° and the magnitude over a range of 6.2dB, together with a compensation of the V-B RTPS ΔIL, constitutes a significant improvement of the state-of-the-art.

Table 6.2 Summary of the reported measured performances of the proposed RTA unit-cell

| Parameter | Performance | Source |
|---|---|---|
| Maximum relative phase shift ($\Delta\phi_{MAX}$) | $> 360°$ | Table 4.3 |
| $P_{LIN\ MAX}$ | $13.7dBm$ to $19.1dBm$ | Figure 6.3 |
| Maximum constant output power over the full range of $\Delta\phi$ | $14.5dBm$ | Figure 6.4 |
| Range of gain variation while maintaining a constant output power over the full range of $\Delta\phi$ | $6.2dB$ | Figure 6.4 |
| Maximum gain of the RTA unit-cell over the full range of $\Delta\phi$ | $4.1dB$ to $5.3dB$ | $P_{[m,n]_{OUT}} - P_{[m,n]_{IN}}$ in Table 6.2 |

# CONCLUSION

This research proposes a highly linear reconfigurable transmitarray (RTA) unit-cell with the capability of simultaneously reconfiguring the phase and magnitude while delivering a linear RF signal at power levels for transmitter applications. Such innovative functionalities constitute a significant improvement of the state-of-the-art. The RF networks of this RTA unit-cell are implemented with a highly linear varactor-based reflective-type phase shifter (V-B RTPS) with low and constant insertion loss (proposed in CHAPTER 4) followed by a GaN RF amplifier including a varactor-based controllable gain mechanism as part of its matching networks (presented in CHAPTER 5).

The highly linear behaviour of these two controllable networks is made possible by enabling the electronically reconfigurable functions with the modified anti-series hyper-abrupt varactor-based tunable impedance network (TIN) proposed in CHAPTER 3. This TIN includes a novel and compact compensation technique to circumvent the linearity degradation due to the parasitics surrounding the diodes, which severely deteriorate the linearity performances of other reported anti-series-based TINs in the literature. This work demonstrates this linearity degradation due to parasitics using an analytical approach based on a multi-tone excitation. An important conclusion of this analysis is that simply optimizing the ratio of diode sizes is insufficient to circumvent this problem. Therefore, the solution proposed in this work consists of a major improvement of the state-of-the-art of varactor-based TINs.

Measured performances at a carrier frequency of 3.6GHz demonstrate that a prototype of the proposed RTA unit-cell can simultaneously reconfigure the phase of the transmitted signal over a range of 360° and its magnitude over a range of ~10dB. Moreover, multi-tone-based measurements demonstrate that the proposed RTA unit-cell generates minimum distortions at power levels as high as 14.1dBm to 19.1dBm depending on the phase. To the best of the author's knowledge, such demonstrated highly linear behaviour with dual dynamic control capability was never demonstrated in the literature.

In addition to achieving improved performances compared to the previous solutions, the proposed RTA unit-cell gives numerous opportunities for new system-level functionalities demonstrating its high relevance at an antenna system level. CHAPTER 6 analysis examples of such functionalities using RTA antenna systems based on measured performances. These analyses show that our proposed RTA unit-cell has the potential of i) significantly improve the antenna system efficiency compared to a non-amplifying RTA system, ii) cancelling the insertion loss variation of the phase shifter for better control of the scattered field, and iii) significantly reducing the negative impact on the system energy efficiency of all the losses upstream the RF amplifier in each unit-cell.

**Communications, declared invention, and publications**

The communications, declared invention, and publications related to this research work are:

- paper under preparation for the IEEE Transactions on Antennas and Propagation (Berthiaume, Laurin et Constantin, TBD-a),
- submitted letter in the IEEE Microwave and Wireless Components Letters (journal) (Berthiaume, Laurin et Constantin, TBD-b),
- published journal paper in the IEEE Access journal (Berthiaume, Laurin, & Constantin, 2021),
- declaration of an invention at the Office of the Dean of Research of the ÉTS: Novel varactor-based electronically controllable phase shifter functions intended for wireless telecommunication systems employing MIMO architectures (2019),
- poster communication at STARaCom annual meeting 2019 (Berthiaume, Laurin, & Constantin, 2019).

**Future works and possible improvements**

This section briefly presents additional opportunities for innovation identified during this research.

1) Implementation in the proposed RTA unit-cell into a full RTA antenna system

The next step of this project is to implement a complete RTA system based on the amplifying RTA unit-cell proposed in CHAPTER 6. However, several challenges have been identified regarding such a system-level implementation.

- Implement the proposed RTA unit-cell in this work, but in a single substrate stackup for more *compactness.* (Both antennas, the phase shifter, and the variable gain amplifier are integrated into the same assembly.)
- In an RTA system, mutual coupling between adjacent Tx antennas can cause significant changes in the impedance seen by the variable gain stage ($Z_{GS\,OUT}$) of each unit-cell. The negative impact on the performances of the gain stage due to degraded $Z_{GS\,OUT}$ needs to be characterized. Furthermore, potential innovative techniques could be researched to mitigate this effect.
- The space environment is prone to large temperature fluctuations. Although this research could not focus on this aspect, it is of great importance for the system under investigation (Figure 1.4). In particular, the effects of temperature on the distortion cancellation mechanism (CHAPTER 3) have never been studied. This is relevant in that the two diodes are of different sizes, which may yield different temperature gradians of both diode and thus to a possible degradation of linearity performances. Again, this aspect however opens up opportunities for innovation. Among others, improvement of the anti-series topology's linearity over a wide temperature range and an innovative method of dissipating the heat from the unit-cells when implemented in a complete RTA antenna system.

2) Bandwidth: Analysis and potential improvements

Even though the targeted application considered in this work does not target LTE or 5G-like bandwidths, the distortion cancellation mechanism and the phase shifter demonstrate 120MHz (Figure 3.18) and 440MHz (Figure 4.5b) bandwidths, respectively. It is therefore interesting to note the potential of such varactor-based networks for very large bandwidth telecommunication applications. The potential innovations regarding the bandwidth are to further analyze the compatibility of the proposed circuit technique in this work with modern

telecommunication technologies (e.g., 5G) and to further improve the bandwidth performances of the proposed anti-series topology.

3) MMIC implementation: for potential operation at millimeter wave frequencies

Even though the parasitics are *smaller* in MMIC technologies, the other MMIC-based state-of-the-art varactor-based tunable impedance networks (Table 2.1) are still limited to frequencies of operation of $\leq 2.4GHz$. The proposed discrete component-based anti-series topology (CHAPTER 3) focuses on mitigating the negative impacts of parasitics surrounding varactors in tunable impedance networks. The implementation of the proposed anti-series topology, but in an MMIC technology, therefore has the potential for operation at millimeter wave bands used in 5G applications (e.g., ~24GHz). This needs to be investigated.

## ANNEX I

## EXPRESSION OF THE GLOBAL SYSTEM ENERGY EFFICIENCY

This annex gives the development of the expression to compute the system energy efficiency ($\eta_{SYS}$) of Section 1.4.4. For easy reference, the antenna system detailed in Section 1.4.4 is reproduced here in Figure-A I-1.

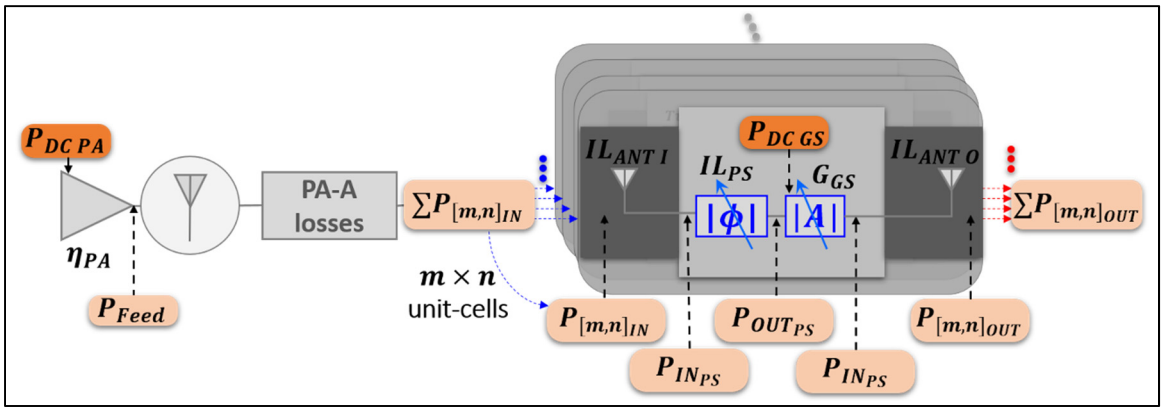



Figure-A I-1 Antenna system to compute the global system energy efficiency ($\eta_{SYS}$)

As mentioned in Section 1.4.4, uniform illumination on each unit-cell and identical unit-cells are considered such that:

$$P_{[m,n]_{IN}} = \frac{\sum P_{[m,n]_{IN}}}{[m \times n]_{unit-cell}} \tag{A I-1}$$

and

$$\sum P_{[m,n]_{OUT}} = P_{[m,n]_{OUT}} \cdot [m \times n]_{unit-cell}. \tag{A I-2}$$

Also, the total consumed DC power is defined as:

$$\sum P_{DC} = P_{DC\,PA} + \sum P_{DC\,GS}$$

with

$$P_{DC\,PA} = \frac{P_{Feed}}{\eta_{PA}} = \frac{P_{[m,n]_{IN}} \cdot [m \times n]_{unit-cell}}{IL_{F-A\,Loss} \cdot \eta_{PA}} \tag{A I-3}$$

and

$$\sum P_{DC\,GS} = P_{DC\,GS} \cdot [m \times n]_{unit-cell}.$$

Knowing that $\eta_{SYS}$ is the total power delivered over the total consumed DC power as expressed in (A I-4).

$$\eta_{SYS} = \frac{\sum P_{[m,n]_{OUT}}}{\sum P_{DC}} \tag{A I-4}$$

$\eta_{SYS}$ of the system in Figure-A I-1 is computed with (A I-5) by substituting $\sum P_{[m,n]_{OUT}}$ and $\sum P_{DC}$ in (A I-4) with (A I-2) and (A I-3), respectively.

$$\eta_{SYS} = \frac{P_{[m,n]_{OUT}} \cdot [m \times n]_{unit-cell}}{\frac{P_{[m,n]_{IN}} \cdot [m \times n]_{unit-cell}}{IL_{F-A\,Loss} \cdot \eta_{PA}} + P_{DC\,GS} \cdot [m \times n]_{unit-cell}}$$

$$\eta_{SYS} = \frac{P_{[m,n]_{OUT}}}{\frac{P_{[m,n]_{IN}}}{IL_{F-A\,Loss} \cdot \eta_{PA}} + P_{DC\,GS}} \tag{A I-5}$$

## ANNEX II

## COMPUTATION OF THE NONLINEAR COEFFICIENTS OF ANTI-SERIES TOPOLOGIES

This annex gives the details to derive the coefficients $C_{ASn} = C_{AS0}, C_{AS1}, C_{AS2}$ of the nonlinear capacitance $C_{AS}(v_S)$ in power series (3.10) and (3.13) and to compute the coefficients in the power series (3.15) and (3.16). Equation (3.10) defines the intrinsic nonlinear behavior of the parasitic-free anti-series-only varactor topology in Figure 3.4. Equation (3.13) also defines the nonlinear behavior of the anti-series-only varactor topology, but this time including parallel parasitic capacitances $C_P$ as shown in Figure 3.6. Equations (3.15) and (3.16) define the power series associated to the anti-series network using a dual bias scheme (Figure 3.9) and the improved anti-series network including $C_{LIN}$ (Figure 3.11), respectively.

Figure-A II-1 represents a generic topology consisting of two series-stacked nonlinear capacitance $C_A(v_A)$ and $C_B(v_B)$. The small-signal voltage $v_s$ of the ideal source is shared between $C_A$ and $C_B$ such that $v_S = v_A + v_B$. The instantaneous nonlinear capacitance variations of $C_A(v_A)$ and $C_B(v_B)$ are, respectively, formulated with the power series given in (A II-1) where the constant scalar coefficients $C_{An} = C_{A0}, C_{A1}, C_{A2}$ and $C_{Bn} = C_{B0}, C_{B1}, C_{B2}$ are independent of $v_S$, consistent with the varactor model considered throughout this paper.

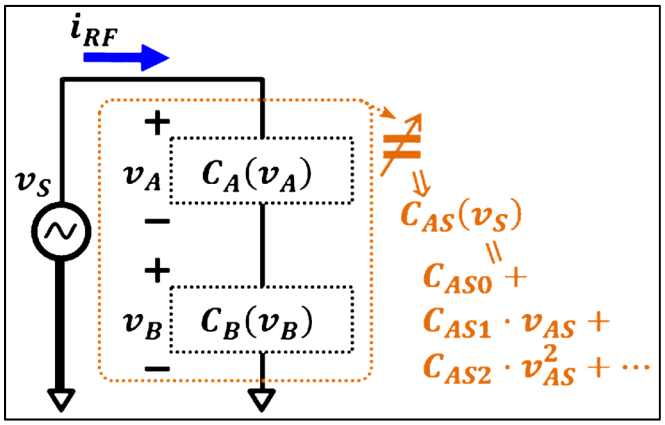



Figure-A II-1 A generic anti-series topology showing all network's elements on the form of a power series for calculation purposes

$$C_A(v_A) = C_{A0} + C_{A1} \cdot v_A + C_{A2} \cdot v_A^2 + \cdots$$
$$C_B(v_B) = C_{B0} - C_{B1} \cdot v_B + C_{B2} \cdot v_B^2 + \cdots \quad \text{(A II-1)}$$

Reference (Meyer & Stephens, 1975) demonstrates the series-combination of $C_A(v_A)$ and $C_B(v_B)$ in Figure-A II-1, resulting in (A II-2) and is repeated here for convenience, consistent with the terminology in the formulations of this paper. Equation (A II-2) includes the $C_{ASn}$ coefficients of power series $C_{AS}(v_S)$ (in orange in Figure-A II-1).

$$C_{AS}(v_S) = C_{AS0} + C_{AS1} \cdot v_S + C_{AS2} \cdot v_S^2 + \cdots$$

$$C_{AS0} = \frac{1}{P_0} \qquad C_{AS1} = -\frac{2P_1}{P_0^3} \qquad C_{AS2} = \frac{3}{P_0^5}(2P_1^2 - P_0P_2)$$

Where (A II-2)

$$P_0 = \frac{1}{C_{A0}} + \frac{1}{C_{B0}} \qquad P_1 = -\frac{C_{A1}}{2C_{A0}^3} + \frac{C_{B1}}{2C_{B0}^3}$$
$$P_2 = \frac{\frac{C_{A1}^2}{2} - \frac{C_{A0}C_{A2}}{3}}{C_{A0}^5} + \frac{\frac{C_{B1}^2}{2} - \frac{C_{B0}C_{B2}}{3}}{C_{B0}^5}$$

In (A II-2), the coefficients $C_{ASn} = C_{AS0}, C_{AS1}, C_{AS2}$ of power series $C_{AS}(v_S)$ are function of the terms $P_0$, $P_1$, and $P_2$, which themselves are function of coefficients $C_{An}$ and $C_{Bn}$ in (A II-1).

In this work, hyper-abrupt varactors ($M > 1$) and unmatched varactors ($s > 1$) including parasitics are considered. Accordingly, the $C_{ASn}$ coefficients defining $C_{AS}(v_S)$ here are obtained simply through the substitution of $C_{An}$ and $C_{Bn}$ in (A II-2) by the appropriate capacitance terms.

For the cases of the parasitic-free anti-series varactor topology (Section 3.1.1.4) and of the anti-series varactor topology including $C_P$ (Section 3.1.2.1), $C_{A0}, C_{A1}, C_{A2}$ and $C_{B0}, C_{B1}, C_{B2}$ are substituted as in (3.9) and (3.12), respectively.

For the cases of the dual biased scheme anti-series network and of the improved anti-series network including $C_{LIN}$ (Section 3.2.1), $C_{A0}, C_{A1}, C_{A2}$ and $C_{B0}, C_{B1}, C_{B2}$ are substituted as in (3.15) and (3.16), respectively.

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