Low-Power Wideband Receiver Front-End Design for Short-Range IoT Applications

by

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MANUSCRIPT-BASED THESIS PRESENTED TO ÉCOLE DE TECHNOLOGIE SUPÉRIEURE
IN PARTIAL FULFILLMENT FOR THE DEGREE OF
DOCTOR OF PHILOSOPHY
Ph.D.

MONTREAL, DECEMBER 9, 2022

ÉCOLE DE TECHNOLOGIE SUPÉRIEURE
UNIVERSITÉ DU QUÉBEC

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ACKNOWLEDGEMENTS

First of all, I would like to express my sincere gratitude to my thesis supervisor, Professor Frédéric Nabki. I would particularly like to thank him for the freedom he gave me in choosing the direction to give to my research project, his advice and ideas which made this doctorate what it is today and lots of kind supports during the hard time of COVID-19 pandemic.

I would like to thank Norm, Jackson, Mark, Lorenzo, Eric, Matthew, Thomas, Peter, Ali, Miranda... at Sequans communications for their enthusiasm to the project, technical supports and encouragements. Special Thanks to Luke Parker for his kind support for PCB modifications.

I would also like to thank all those who contributed to this thesis. I must mention here in particular the company CMC Microsystems, which provided the design tools and allowed the manufacture of chips designed during this doctorate.

Thank to my lovely friends, Anousha, Mehran, Bahador, Ehsan, Ali and Amir to strike a balance with life outside the dark depths of the lab and office. Special thanks to Mathieu for IT supports and logistics.

And finally, I would also like to thank my parents, my sister and my brother for their support throughout my life and my studies. Dad, Mom, Golnaz and Amir thank you! Without you, none of this would have been possible.

Conception de récepteur RF large bande à basse consommation pour les applications IoT à courte portée

Arash ABBASI

RÉSUMÉ

La croissance rapide de l'internet des objets (IoT) promet la mise en place d'un environnement intelligent, y compris la domotique. Des milliards d'appareils IoT sont nécessaires pour atteindre cet objectif. En conséquence, la réduction d'une fraction de la consommation d'énergie de chaque appareil IoT peut entraîner une importante réduction globale de la consommation d'énergie à l'échelle mondiale. Sans aucun doute, l'émetteur-récepteur RF joue un rôle important pour définir la consommation électrique globale des modules IoT.

L'objectif de ce travail est de développer un récepteur RF à faible consommation d'énergie et à large bande pour les applications IoT. Pour ce faire, dans un premier temps, une revue de la littérature est présentée. Elle se concentre sur les techniques de conception de récepteurs à faible puissance et examine les circuits en détail.

À la suite de la revue de littérature, un tutoriel de conception détaillé comprenant la procédure de conception et la caractérisation est présenté pour fournir une approche de conception systématique du récepteur RF à réutilisation du courant proposé.

Un récepteur RF à faible puissance et à réutilisation de courant utilisant une inductance active et des techniques d'annulation de bruit $1/f$ pour les applications en bande L est présenté. L'inductance active améliore le facteur de bruit du récepteur à des fréquences plus élevées et les techniques d'annulation de bruit suppriment le bruit à basses fréquences.

Une comparaison d'un balun différentiel hors puce et d'un balun LC utilisant le même récepteur RF à réutilisation de courant avec et sans inductance sur puce est présentée pour évaluer les performances en utilisant différents réseaux d'adaptation et bandes de fréquences.

En somme, cette thèse décrit l'étude, la conception et la caractérisation d'un récepteur RF à faible puissance et à large bande à réutilisation du courant qui peut être conçu dans plusieurs bandes fréquentielles pour utilisation dans différentes applications IoT.

Mots-clés: IoT, current-reuse receiver,low noise amplifier, wideband, low-power

Low-Power Wideband Receiver Front-End Design for Short-Range IoT Applications

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ABSTRACT

The fast growth of the internet-of-things (IoT) promises the establishment of a smart environment including home automation, health monitoring, location tracking etc. Billions of IoT devices are needed to achieve this goal and connect the objects around us. This introduces a need to develop low-power IoT devices. Accordingly, reducing by a fraction of the power consumption in each IoT device can lead to an important overall energy use reduction globally. undoubtedly, the RF transceiver plays a significant role to define the overall power consumption of the IoT module.

The aim of this work is to develop a low-power and wideband current-reuse receiver front-end for IoT applications. The wideband feature covers several frequency bands to reduce the number of receivers required. To do this, first, a literature review is presented. It focuses on the low-power receiver design techniques and discusses the circuits in detail.

Following the literature review, A detailed design tutorial including the design procedures and characterization results is presented to provide a systematic design approach of the current-reuse receiver front-end to breakdown the circuit to sub-blocks and perform the design as a conventional receiver architecture.

A low-power RF-to-BB current-reuse receiver front-end using an active-inductor and $1/f$ noise-cancellation techniques for L-band applications is presented. The active-inductor improves the receiver noise-figure at higher frequencies and the noise-cancellation technique suppresses the low frequency noise. Both active-inductor and $1/f$ noise-cancellation techniques help enhance the receiver noise figure. The effect of the metal fill on the performance is studied in measurements that shows the notable improvement in the noise figure performance.

A comparison of an off-chip differential and an LC Balun employing the same current-reuse receiver front-end with and without an on-chip inductor is presented to evaluate the performance using different matching networks and frequencies. This demonstrates that the receiver can be tuned to any frequency band by adjusting the matching network.

Overall, this thesis describes the study, design and characterization of low-power and wideband current-reuse receiver front-ends that can be tuned for any frequency band to be used for different IoT applications. The active-inductor and $1/f$ noise-cancellation techniques introduced in this work improve the performance of the receiver and allow it to maintain its performance at higher frequencies even in a relatively large 130 nm CMOS process.

Keywords: IoT, current-reuse receiver,low noise amplifier, wideband, low-power

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LIST OF ABBREVIATIONS

ADC	Analog to Digital Converter
ETS	Ecole de Technologie Superieure
FFT	Fast Fourrier Transform
FOM	Figure Of Merit
IC	Integrated Circuit
IoT	Internet of things
IEEE	Institute of Electrical and Electronics
TCAS	Transaction on Circuit and System
MDPI	Multidisciplinary Digital Publishing Institute
VCO	Voltage Controlled Oscillator
VNA	Vectorial Network Analyzer
LNTA	Low Noise Transconductance Amplifier
LNA	Low Noise Amplifier
TIA	Transimpedance Amplifier
AI	Active-Inductor
NC	Noise-Cancellation
CRR	Current-Reuse Receiver
BB	Baseband
GPS	Global Positioning System

GNSS	Global Navigation Satellite System
NF	Noise Figure
DSB	Double Side-band
IIP3	Third-order Input Intercept Point
IM3	Third-order Intermodulation Product
CG	Conversion-Gain
LO	Local-oscillator
RF	Radio Frequency
IF	Intermediate Frequency
CMOS	Complementary metal–oxide–semiconductor
DC	Direct Current
AC	Alternating Current
PCB	Printed Circuit Board
CML	Current-mode Logic
LDO	Low-dropout Regulator
EDA	Electronic Design Automation
VCCS	Voltage Controlled Current Source
V_{TH}	Voltage-Threshold
PDK	Process Design Kit
CS	Common-source

CG	Common-gate
P1dB	1-dB compression point

LIST OF SYMBOLS AND UNITS OF MEASUREMENTS

Ω	Ohm
F	Farad
Hz	Hertz
m	Meter
Q	Quality Factor
s	Seconde
V	Volt
W	Watt
λ	Lambda
dB	Decibel
dBm	Decibel Milliwatt
g_m	Transconductance

INTRODUCTION

Context of the Study and Problems

As the proliferation of the internet of things (IoT) occurs, many are expecting the gradual establishment of a ubiquitous smart environment, including home automation, health monitoring, traffic control, transportation, etc, as shown in figure 0.1, an improvement in the wireless connectivity is a top priority Liu & Niknejad (2019); Kim *et al.* (2019); Karim (2018).

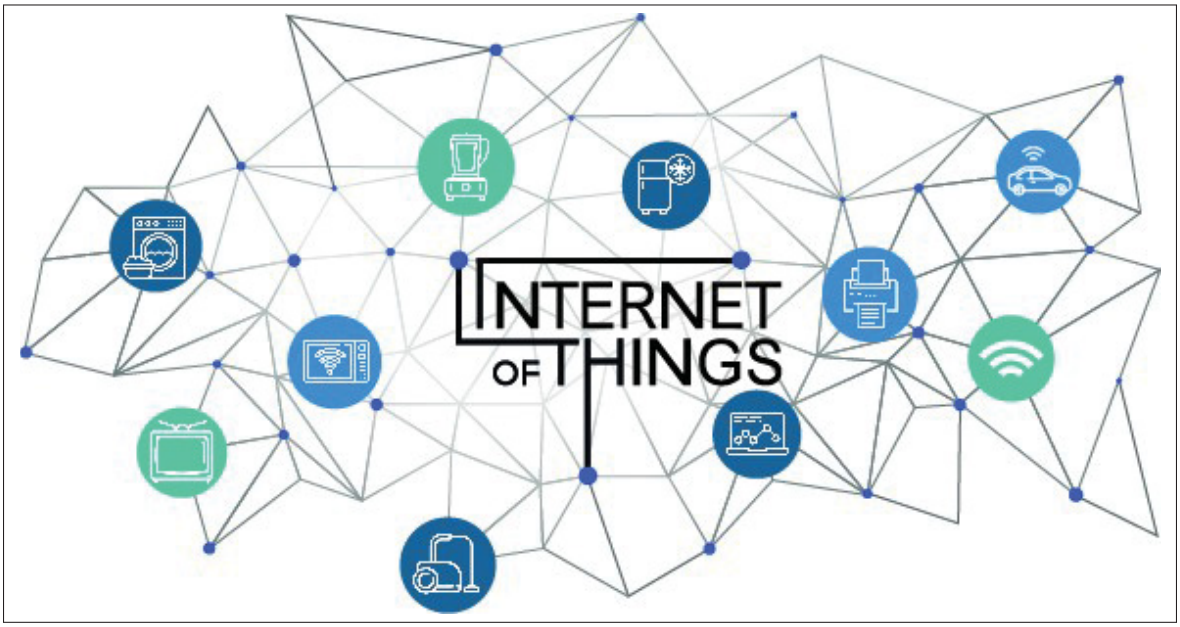

Figure 0.1 Applications of IoT.
Taken from plopdo.com.

The smart city is one of the most important applications of the IoT, in which a broad number of ultra-low power sensors connect wirelessly to monitor the environment and provide monolithic communication between humans and things. In healthcare, the IoT enables continuous monitoring of patients by professionals and doctors to reduce the risk of any incidents. IoT devices are also utilized widely for location tracking and positioning in different applications such as vehicles for navigation, health for patient tracking, military for soldier localization, shipping to track goods,

etc. For instance, car insurance companies provide special discount for costumers willing to install tracking devices that provide useful information such as millage and speed to the insurer; Pascual Pelayo (2018); Petäjäjärvi (2018).

In recent years, there has been a significant change in wireless communications. At the beginning of the history of communication, a radio or television station employed a very high power transmitter for video and audio broadcasting to several receivers. A few decades ago, a dramatic change was observed and today the number of cordless and wireless devices, like wireless internet and cellular telephones, are growing everyday with vastly proliferating wireless links. As wireless applications have been increasing in all sectors, there will be a new opportunity for more use cases requiring devices to be wirelessly connected and networked together. There has been a wide range of research and development on IoT applications, where every objects such as our home appliances are to be connected to a network to enhance monitoring and control. It is undeniable, today, that a great number of human beings are carrying a laptop, smartwatch or smartphone in everyday life which are powerful computing platforms. Thus, this is a unique chance to increase the number of sensors to connect and monitor the world around us (and us) through mobile devices married to wireless technology. These sensors can be used for wide range of purposes like continuous life signs monitoring or dynamically locating patients in hospitals.

As a part of any wireless application, the wireless transceiver plays a key role to determine a wireless system's specifications such as performance and power. In a transceiver, a radio frequency (RF) front-end consumes most of the power. Moreover, it determines the key specifications of the receiver and transmitter performance, such as linearity and noise figure (NF), which has led to a broad number of research works on RF front-end circuit design (Jeong, Lee, Lee & Kim (2016); Liu *et al.* (2018); Niitsu *et al.* (2018); Ture, Devos, Maloberti & Dehollain (2018)). The transceiver includes the receiver and the transmitter blocks. The receiver, which is

the main interest of this work, receive a low-power wanted signal that needs to be amplified and differentiated from interference and noise. Thus, it need to have very low NF with sufficient linearity while consuming minimum power. Therefore, careful consideration and effort should be taken in designing an RF front-end to achieve the highest performance with the minimum power consumption, requiring specific circuit design techniques and architectures. We can think of a few major requirements for transceivers such as NF, gain,linearity and power Tam (2016); Ali Niknejad (2019).

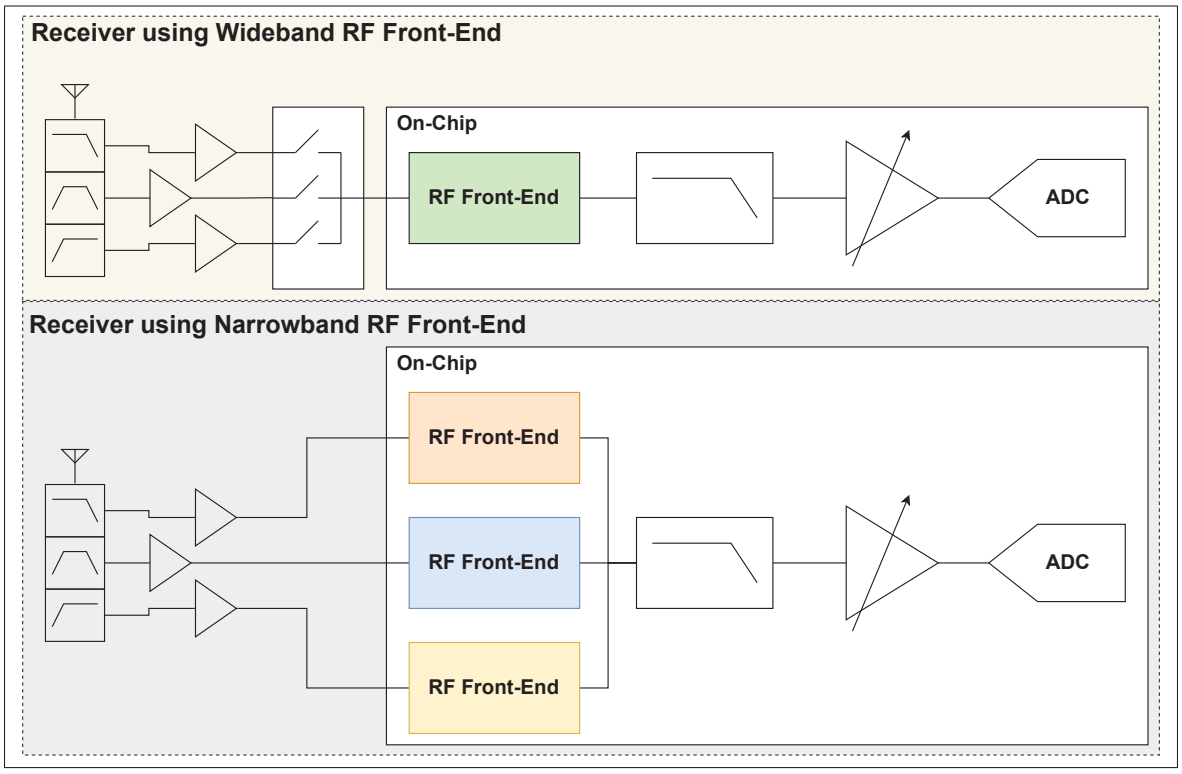

Figure 0.2 Wideband and narrowband RF front-end.

As the number of wireless devices for IoT is expected to increase to the tens of billions by 2025, saving even a fraction of the power on every wireless device is crucial to save significant amounts of aggregate power. As mentioned earlier, most of the power in wireless applications is consumed by the RF transceiver to process the RF signals. There has been a wide range

of research and articles in both academia and industry that propose circuit design techniques and receiver architectures to reduce the power consumption of the RF transceiver front-end while maintaining the other performance metrics such as gain, noise and linearity Thijssen, Klumperink, Quinlan & Nauta (2020); Elsayed *et al.* (2019); Neeraja, Moganti & Md (2021); Chen *et al.* (2019); Vijayalakshmi & Nagarajan (2019); Forno, Moio, Schenatti, Macii & Urgese (2020). However, they still need improvement that need to be taken into account and will be discussed in this work. In addition, it is crucial to maintain the performances of transceiver over a wide frequency range to meet the requirements of several wireless standards. In this way, a single transceiver to meet the requirements of several wireless standards becomes possible and cost and power consumption of the RF subsystem can be substantially reduced. Figure 0.2 shows receiver front-ends using a narrowband and a wideband RF front-end. It shows that the wideband RF front-end can cover several wireless standards using external switches that switch different frequency bands. In this way, a low power, low cost and agile RF receiver can be achieved to support several wireless protocols without requiring multiple font-ends.

Research Objectives

Low power and high performance receivers have attracted great interest in the research community, as they provide a potential to extend the battery life of wireless devices. In recent years, attempts have been made to reduce power consumption of the RF receiver front-end as it is consuming most of the power in the receiver circuits. In low-power receivers, attaining the low noise figure (NF) and the high blocker tolerability is of the great importance, though very challenging in wideband implementations which are sought after, as they reduce the number of RF front-ends required in a given wireless device that needs to support multiple wireless standards.

The selection process of the wideband RF front-end structure is a difficult, challenging and time-consuming task that directly affects the performance of the entire receiver. It is important

to manage the challenges and properties related to each building blocks. To this end, a number of parameters need to be taken into account.

A conventional receiver architectures contain a low noise amplifier (LNA) or a low noise transconductance amplifier (LNTA), a down-conversion mixer, an local oscillator (LO) and integrated analog filters. However, the low-power design requires the new receiver design techniques to reduce the power consumption while the overall performances are not affected, notably over a wide frequency range. After architecture selection, performance enhancing and low-power techniques are required to design each of the sub-blocks.

The goal of this work is to:

1. **propose a wideband low-power receiver front-end using current-reuse architecture to reduce static power consumption**
2. **propose an active-inductor technique to enhance the performance of the current-reuse receiver at high radio frequencies**
3. **propose a $1/f$ noise-cancellation technique to enhance the noise performance at a low intermediate-frequency**
4. **fabricate and test the proposed current-reuse circuits with different matching circuits to outline circuit reliability and input matching options**

The main contributions of the research work are as follows:

1. **It gives a unique perspective on low-power and wideband RF-to-Baseband current-reuse receivers (CRRs) including the related architectural choices, characterization and analysis that are involved in the design methodology.**
2. **It presents the design and fabrication of a wideband low-power RF-to-BB current-reuse receiver using an active inductor and $1/f$ noise-cancellation for L-band applications in order to validate the proposed methodology and architecture**

3. **It provides a comparison of the impact of an off-chip differential balun and an LC Balun with or without using an on-chip inductor in a wideband low-power RF-to-BB CRR front-end to provide design insights into the impact of the input matching strategy of such a front-end structure**

Structure of the Thesis

- The CHAPITRE 1 presents the state-of-the-art. Its main objective is to give an overview of the low-power receiver architectures. It also discuss the weakness of the prior art and potential future developments.
- The CHAPITRE 2 is a paper published in the special issue "Design of Mixed Analog/Digital Circuits", section "Circuit and Signal Processing", Electronics, MDPI. It presents the design procedure and characterization of ideband current-reuse receiver front-ends for low-power applications.
- The CHAPITRE 3 is a paper published in the IEEE Access journal. It presents the design and measurement results of a CRR front-end employing an active-inductor and $1/f$ noise-cancellation techniques. It also shows the effect of a metal fill in the measurement results.
- The CHAPITRE 4 is an article submitted to the special issue "Design of Mixed Analog/Digital Circuits, Volume 2", section "Circuit and Signal Processing", Electronics, MDPI. It presents the design and measurement comparison of an off-chip differential balun and an LC balun in a low-power RF-to-BB current-reuse receiver front-end.

CHAPTER 1

LITERATURE REVIEW

Overview

In wireless communications, a very weak wanted signal arrives at the receiver input. This received wanted signal need to be amplified with minimum added noise. The RF signal should be down-converted to a low intermediate-frequency (IF) or base-band (BB) signal by local oscillator (LO) and then filtered before analog to digital conversion (ADC) and digital signal processing (DSP) to remove interference and noise. This chapter studies and analyses the recent published works on low-power receiver architectures and a critical analysis of the drawbacks and benefits of each work is given.

1.1 Current reuse receiver

It is challenging to reduce the power consumption of the RF front-end while maintaining performance metrics such as linearity and NF. Various methods and techniques have been studied to address these challenges. Among them, a widespread method to reduce the power consumption is current-reuse. Usually, current-reuse has been employed within individual blocks such as a low noise transconductance amplifier (LNTA), Shams, Abbasi & Nabki (2020). By scaling down the CMOS technology, one may increase the operating frequency and reduce the threshold voltage such that new transceiver design techniques have emerged. The idea of current-reuse focused on stacking different circuits and sharing the same supply. Several recent published current-reuse receivers are discussed in this section.

1.1.1 Current-Reuse Receiver with Stacked LNTA, Mixer and VCO

A stacked LNTA, Mixer and Voltage controlled oscillator (VCO) (LMV) is proposed by Tedeschi, Liscidini & Castello (2010) to reduce power consumption by sharing a single supply and biasing current shown in Figure 1.1. Transistor M_0 defines the VCO current while at the same time

performs as LNTA to amplify and convert the RF signal to RF current. Stacking the VCO may cause injection locking issue of the VCO due to the large blocker. Moreover, it reported very high NF of 10 dB.

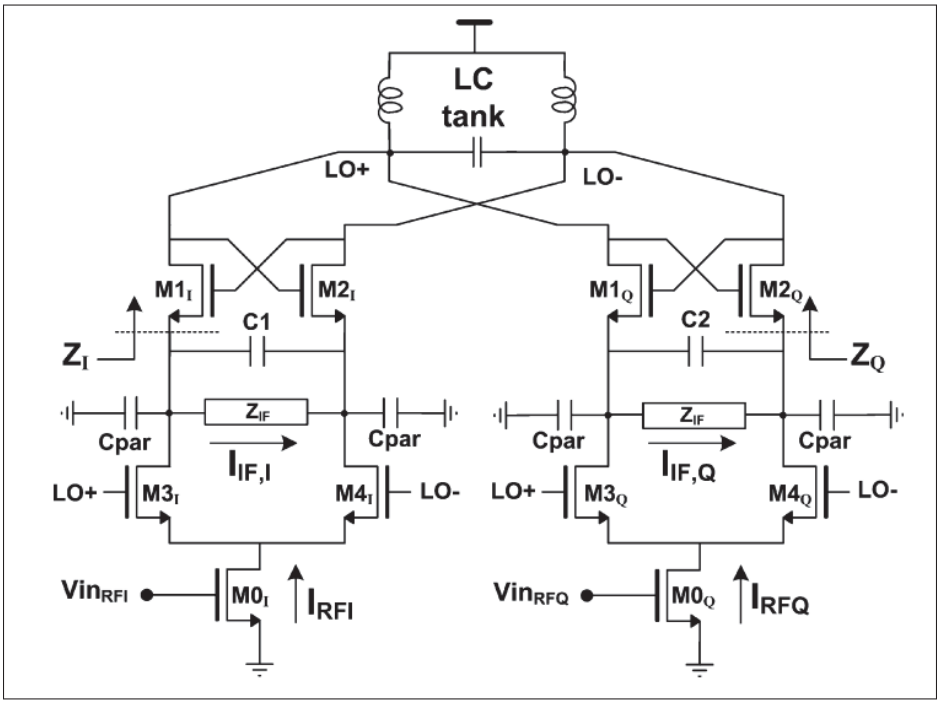

Figure 1.1 LMV circuit diagram.
Taken from Tedeschi *et al.* (2010)

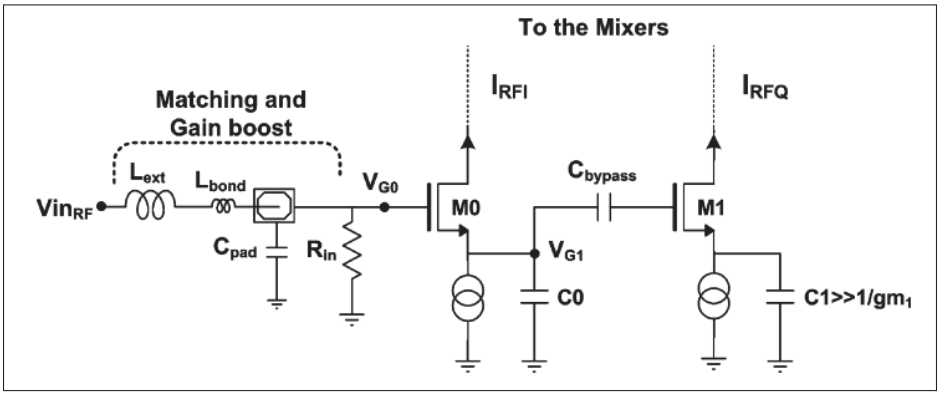

Figure 1.2 LNTA circuit using quadrature generation through capacitor.
Taken from Tedeschi *et al.* (2010)

The I and Q generation can be achieved through LNTA using capacitive generation, shown in Figure 1.2. This may cause unbalance output of LNTA which is only suitable for narrowband applications such as ZigBee standard. In addition, the LNTA may suffer stability issue where certain criteria need to be met to avoid instability.

Although very low-power consumption is achieved by Tedeschi *et al.* (2010), It still suffers from several issues like high NF and instability that makes this work not suitable to many applications. Next, a current-reuse receiver is proposed where the VCO is not stacked to avoid the problems related to the injection locking of the VCO.

1.1.2 Current-Reuse Receiver with Balun-LNA

Figure 1.3 shows the current-reuse receiver front-end proposed by Lin, Mak & Martins (2014b).

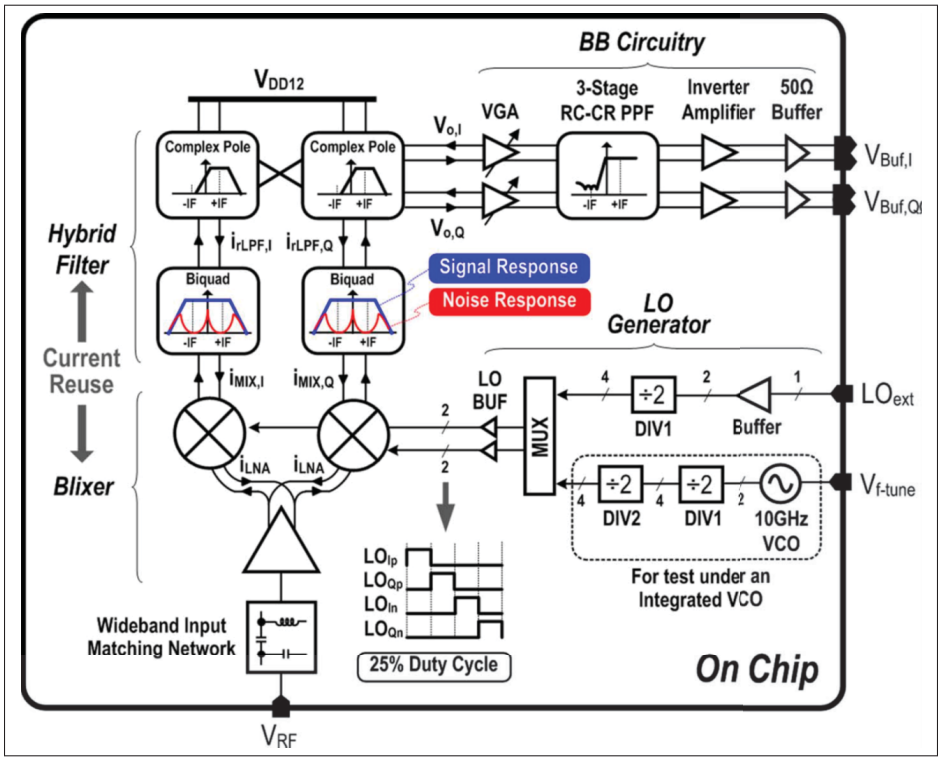

Figure 1.3 System overview of single-input current-reuse architecture.
Taken from Lin *et al.* (2014b)

The receiver cascodes Balun-LNA, mixer, biquad filter and a complex filter to enhance image rejection in the initial stage. The current-reuse receiver followed by VGA and RC-CR complex filter offers additional gain programmability and extra image rejection. The proposed Balun-LNA illustrates in Figure 1.4. It converts the single-ended signal to a differential current through a common-source and common-gate noise-cancelling LNTA topology. Although the A_{GB} inverter based amplifier reduces the imbalance, such a design is always susceptible to mismatch. Moreover, extra components at the input increase NF and power consumption. Figure 1.5 shows the biquad filter that helps for channel selection and filtering.

The active inductor shapes the noise at the IF frequency; however, the NF is reduced only by 0.5 dB at the cost of the oscillation risk due to the positive feedback.

The proposed complex filter circuit shown in Figure 1.6 obtains the real part from diode connected transistor M_L and the imaginary part from I/Q cross connected M_C. In this way, the image is slightly rejected, 5 dB, while NF is degraded.

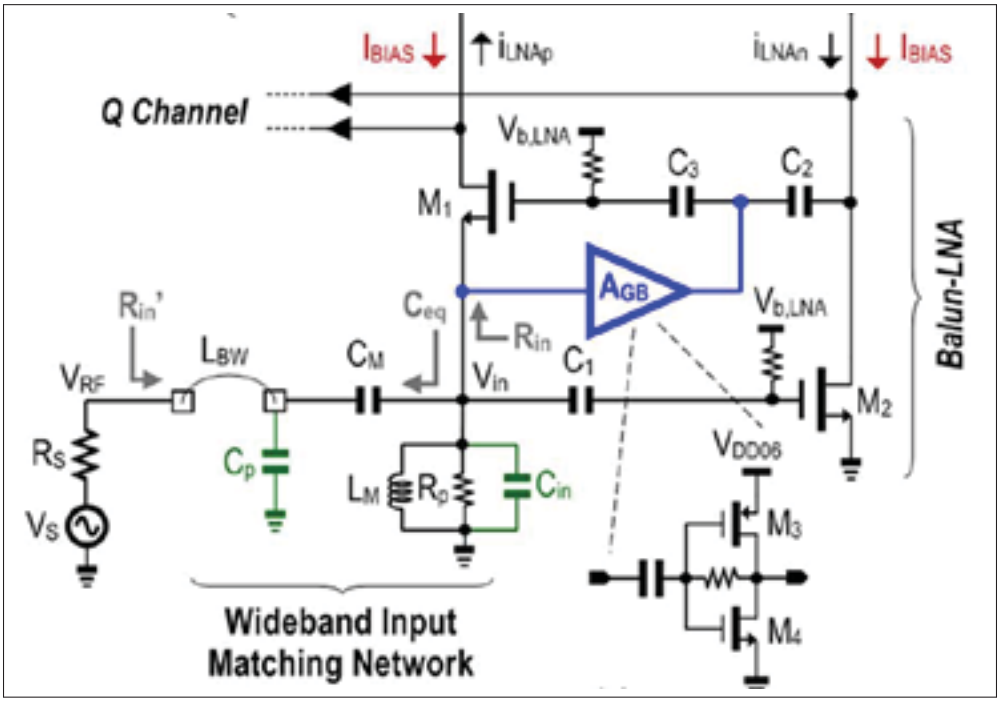

Figure 1.4 Single input Balun-LNA.
Taken from Lin *et al.* (2014b)

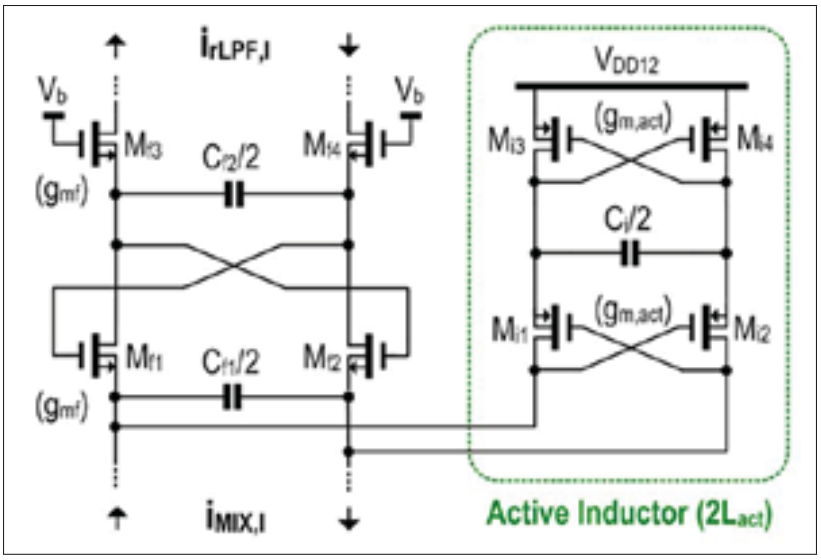

Figure 1.5 Proposed IF-noise-shaping Biquad.
Taken from Lin *et al.* (2014b)

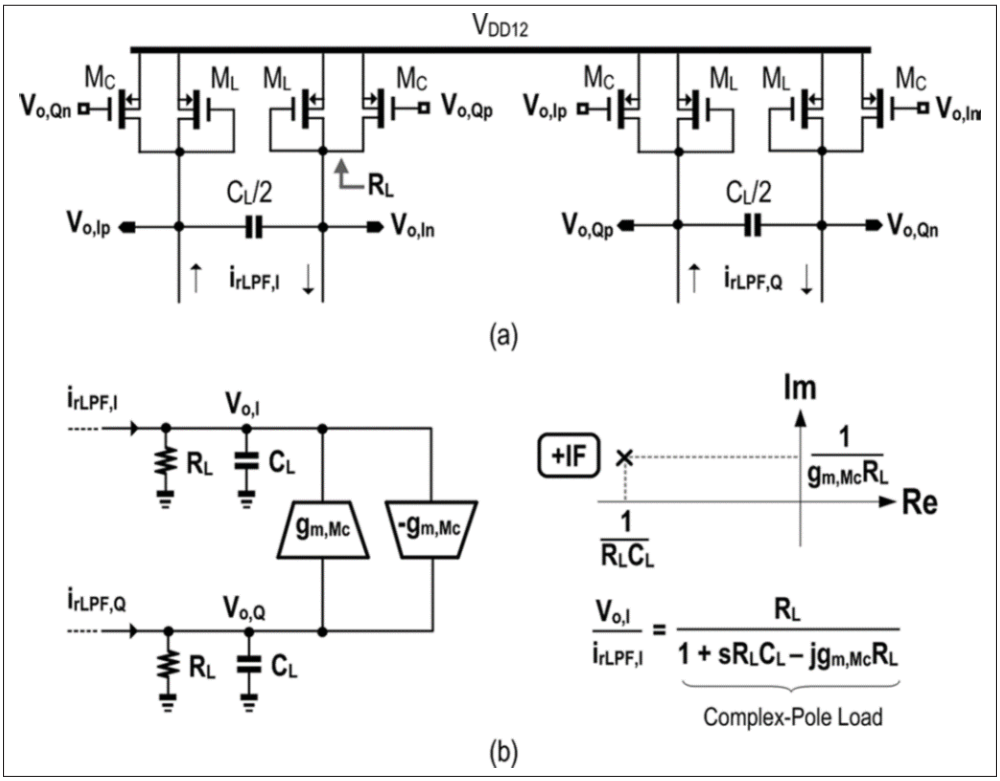

Figure 1.6 (a) Proposed complex-pole load and (b) its small-signal equivalent circuit.
Taken from Lin *et al.* (2014b)

Lin *et al.* (2014b) proposed a receiver front-end for the ZigBee wireless standard. There are both advantages and disadvantages in this approach. The complex pole attenuates the image signal by 5 dB; however, it is not sufficient, which led to the use of an additional complex filter at the cost of higher NF and supply voltage that increases power consumption. The better solution here is to use a programmable gain complex filter instead of VGA, RC-CR filter and complex pole as a current reuse architecture separately. Moreover, an additional active-inductor to reduce NF by 0.5 dB from 9 dB to 8.5 dB is not efficient where it increases the risk of oscillation due to the positive feedback. In addition, cascoding several blocks requires a higher supply voltage that increases power consumption. In the next section, another approach is introduced with an N-path configuration.

1.1.3 Current-Reuse Receiver with an N-path Configuration

Figure 1.7 shows the current-reuse receiver proposed by Lin, Mak & Martins (2014a) where the structure takes advantage of the N-path configuration to enhance the overall performance. The receiver is proposed for TV-band (0.15 to 0.85 GHz) applications.

The receiver uses a single input common-source configuration without any extra components for external matching. An 8-path passive mixer feedback realizes input impedance matching, RF filtering and noise cancelling. It also takes advantage of harmonic recombination; 8-phase BB signals can combine in a way to remove the 3rd and 5th order harmonics at the output.

The current-reuse technique combined with an N-path down-conversion mixer could enhance the performance as reported by Lin *et al.* (2014a) while consuming a lot of current 16 mW. The feedback N-path passive mixer is not recommended due to the risk of oscillation. Another drawback is additional circuits to combine the N-path at the output that is power consuming, shown in Figure 1.8. To reduce the voltage headroom requirement, an active mixer can be replaced with a current driven passive mixer. Next, a current-reuse receiver using a passive mixer is shown where the I and Q path are stacked.

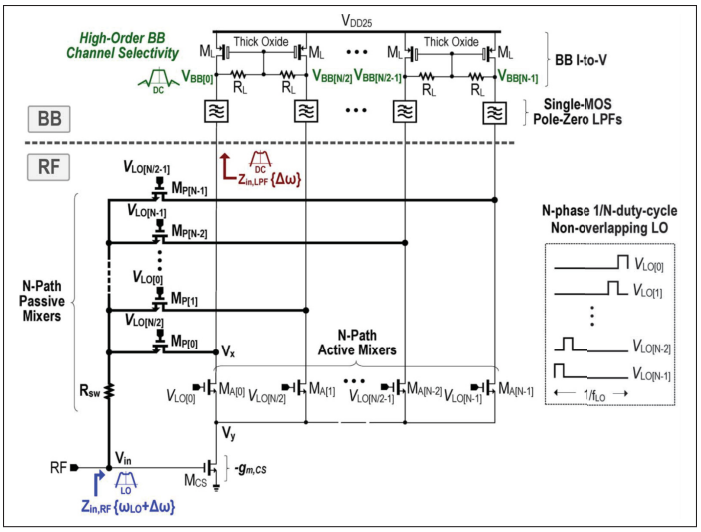

Figure 1.7 Current-reuse receiver with N-path configuration.
Taken from Lin *et al.* (2014a)

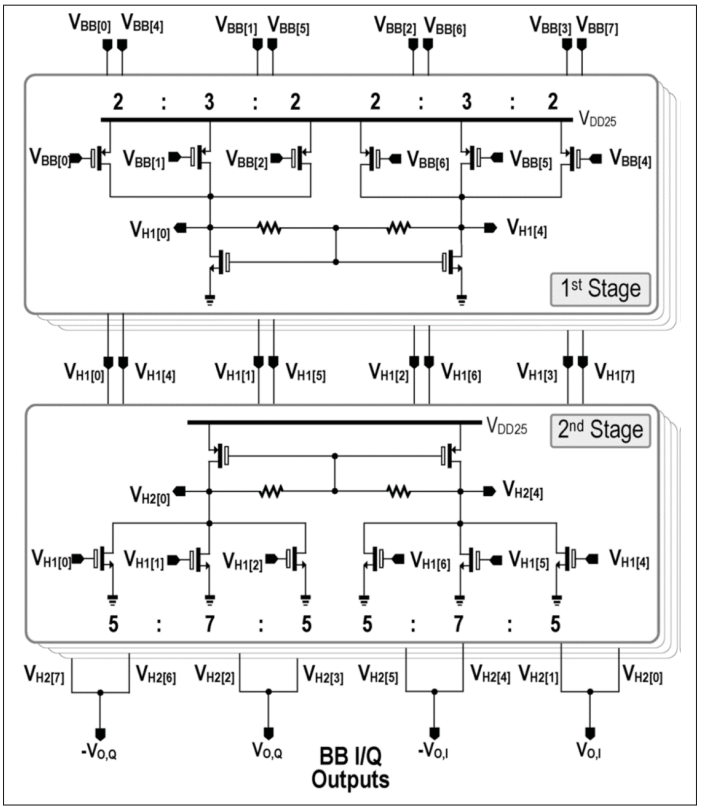

Figure 1.8 8-path combiner circuit.
Taken from Lin *et al.* (2014a)

1.1.4 Current-Reuse Receiver with Stacked I/Q Paths

Figure 1.9 shows a current-reuse receiver circuit proposed by Ramella, Fabiano, Manstretta & Castello (2017). In this architecture, both I and Q paths are cascoded and share the same supply voltage. A single to differential transformer followed by common-gate amplifier to convert voltage to current employed at the input illustrated in Figure 1.10. The cross-coupled technique at the input boosts the transconductance where it reduces NF and enhances gain.

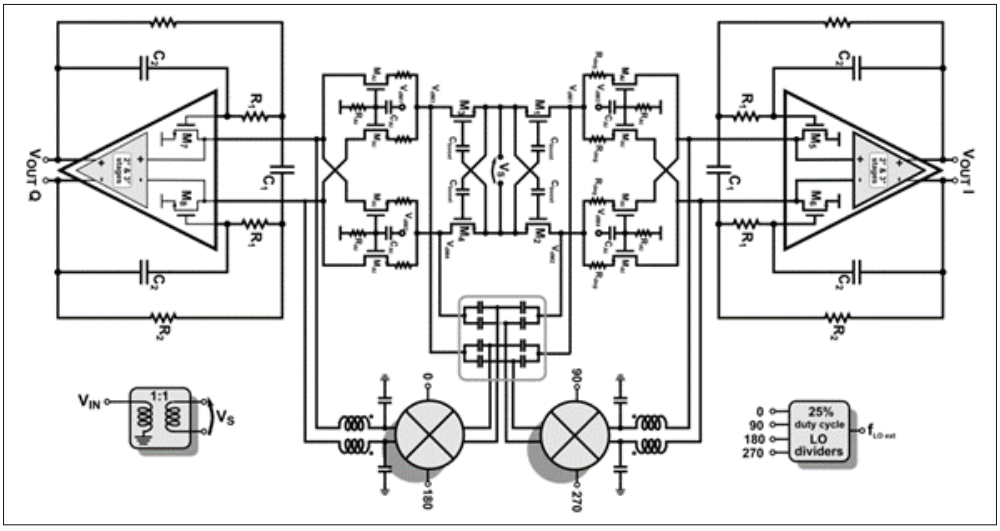

Figure 1.9 Block diagram of the current-reuse receiver.
Taken from Ramella *et al.* (2017)

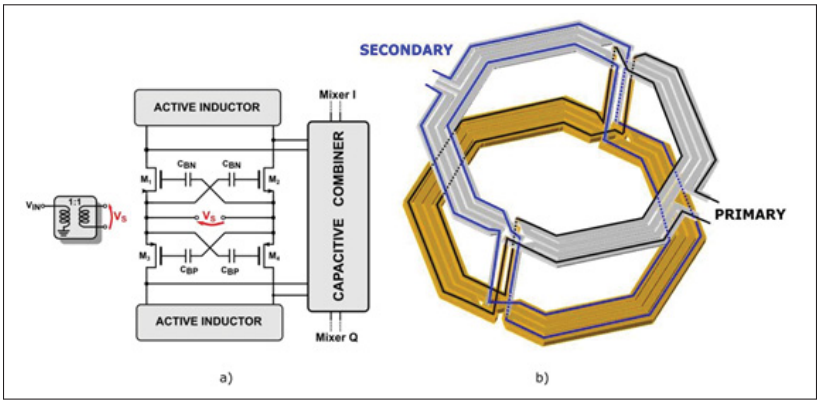

Figure 1.10 (a) Cross-coupled common-gate LNTA. (b) Single to differential transformer.
Taken from Ramella *et al.* (2017)

A schematic of the I path is shown in Figure 1.11. The active-inductor boosts the Z_{RF} at high frequency. In this way, the RF current is routed towards the mixer input. However, it shows low impedance at low frequency where M_{AI} acts like a cascode stage for the baseband (BB) output stage to boost the output impedance. However, this degrades the linearity that limits the IIP3 and curtails the circuit's applicability to a wide range of use cases.

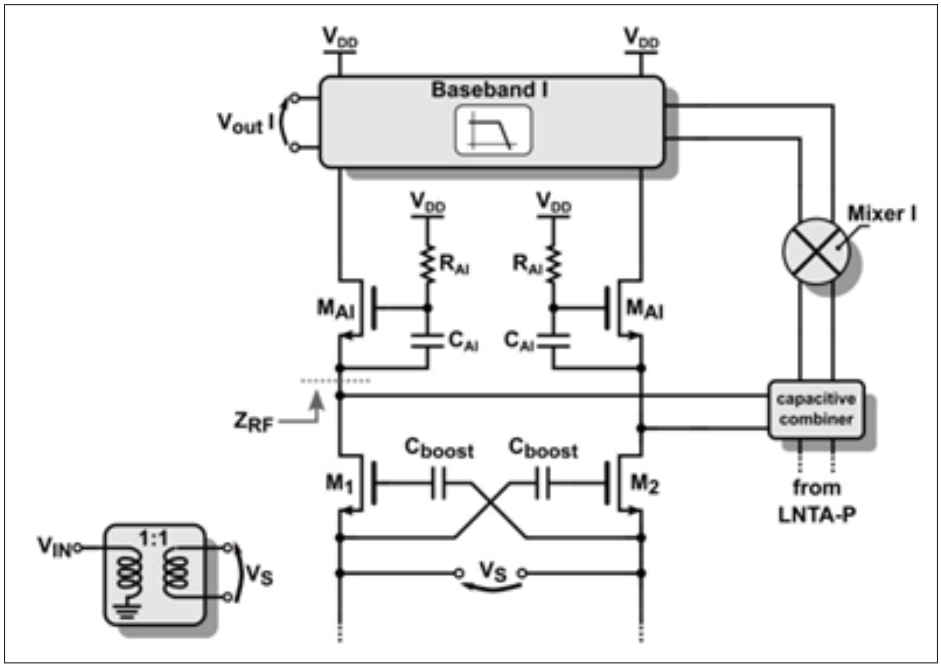

Figure 1.11 Receiver I path circuit.
Taken from Ramella *et al.* (2017)

The solution to improve the linearity is shown in Figure 1.12. Cross-coupling reduces the common mode impedance to $\frac{1}{2g_{m,AI}}$ at higher frequencies, thus improving linearity.

Although the reported circuit by Ramella *et al.* (2017) shows good linearity and NF results, high power is consumed in this architecture. By stacking the I and Q paths, a high voltage headroom is required. Moreover, keeping all transistors in saturation across process, voltage and temperature corners is complex and potentially non-viable. The circuit proposed by Ramella *et al.* (2017) has the advantage of featuring a parallel passive mixer over the circuit in Lin *et al.* (2014b) and Lin *et al.* (2014a) where significant voltage headroom is saved.

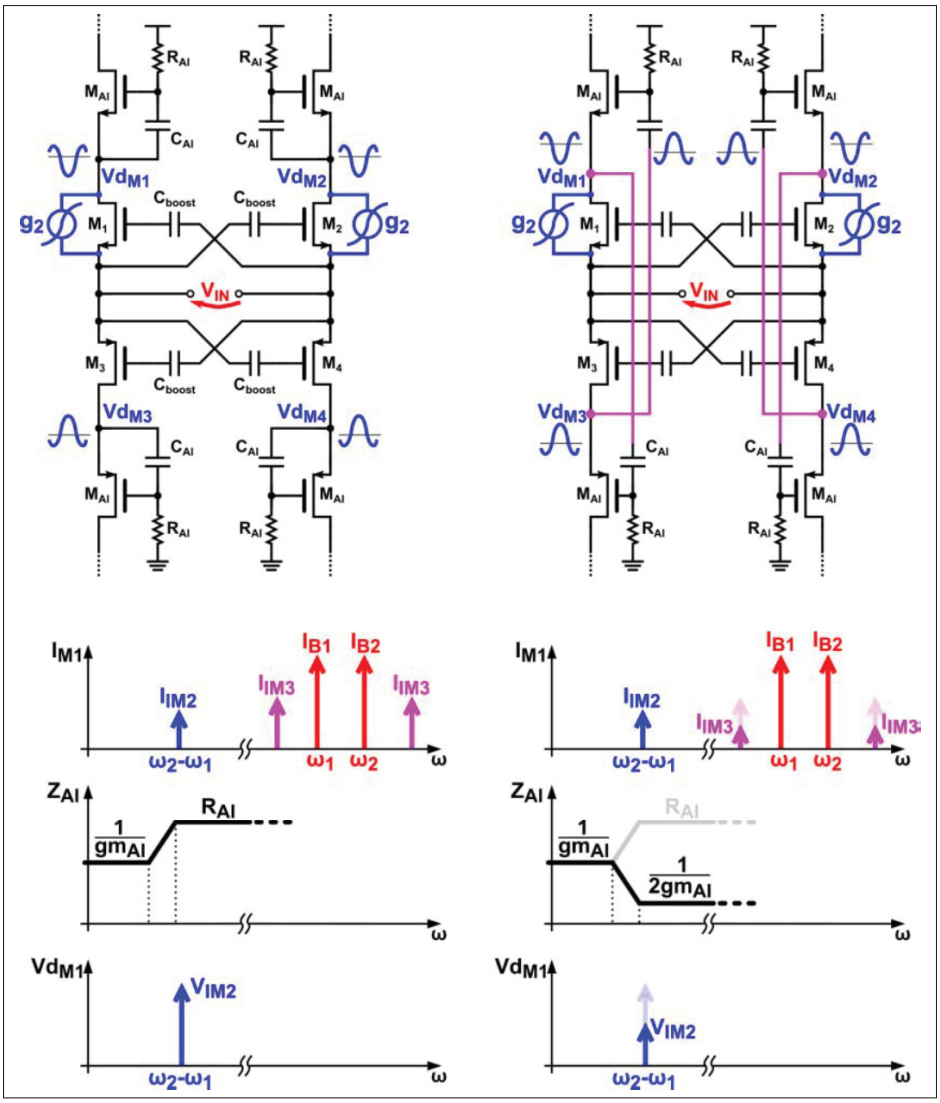

Figure 1.12 Front-end with conventional AI (left) and adopted solution (right).
Taken from Ramella *et al.* (2017)

1.1.5 Source-Degenerated Current-Reuse Receiver with 1/f Reduction

Figure 1.13 shows current-reuse architecture proposed by Kim & Kwon (2019). It offers better performance in terms of NF in comparison to earlier mentioned architectures while consuming 3.6 mW power. A common-source input stage with a source-degeneration inductor is used for input matching. R_S employed to minimize the $1/f$ noise. Cascode transistors provide better

isolation between input and output. Moreover, it boosts the output impedance that increases the gain and current driving to the next stage. The passive mixer is followed by transimpedance amplifier (TIA) that converts the RF current to a BB voltage at the output. By increasing the feedback resistor, R_F, the conversion gain increases.

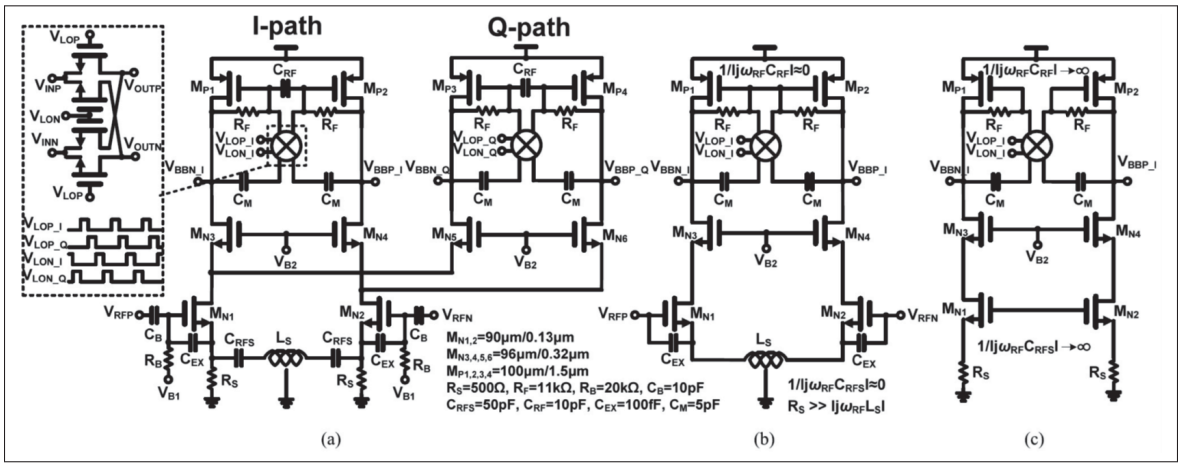

Figure 1.13 (a) Proposed current-reuse. (b) I path model in RF domain. (c) I path model in BB domain.
Taken from Kim & Kwon (2019)

The circuit proposed by Kim & Kwon (2019) shows interesting NF and linearity results while input matching is degraded after fabrication due to the susceptible behaviour of the common-source configuration, which is very sensitive to bond-wires and parasitics. To enhance the input matching result, a common-gate amplifier using a cross-coupled technique can be used by slightly sacrificing NF, which is acceptable for several wireless standards. Moreover, a programmable R_F resistor to be employed to program the receiver gain and increase circuit reliability when the input RF is high.

1.1.6 Quadrature RF-to-Baseband-Current-Reuse Architecture

Park & Kwon (2021) extended the work proposed by Kim & Kwon (2019) which employed simultaneous input matching and $1/f$ noise cancellation technique, but modified the cascode circuit to perform as an I/Q generator, shown in Figure 1.14.

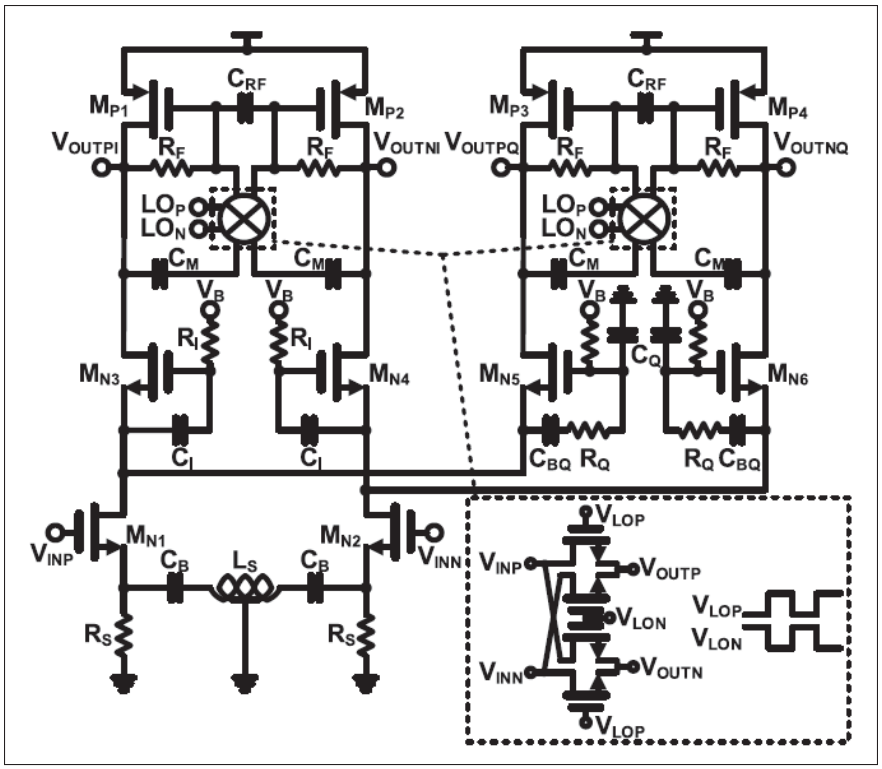

Figure 1.14 Quadrature RF-to-BB-CR receiver architecture. Taken from Park & Kwon (2021)

Although power consumption of 1.13 mW is very low, this approach is only suitable for the applications where receiver sensitivity is not important since it reported a high NF of 13.2 dB. The high NF is due to the active-inductor that blocks the RF signal in the I path to achieve the quadrature signal at the output. In addition, the performance of the quadrature generation is very sensitive to the parasitic capacitances and resistances of the transistors (M_{N3}-M_{N6}), increasing circuit variability .

1.2 Function-Reuse Architecture

One of the low-power receiver design techniques is function-reuse of the current consuming blocks. The circuit shown in Figure 1.15 is proposed by Lin, Mak & Martins (2014c). The green colour shows the RF path where the RF signal is amplified and converted to a current through the G_m stage.

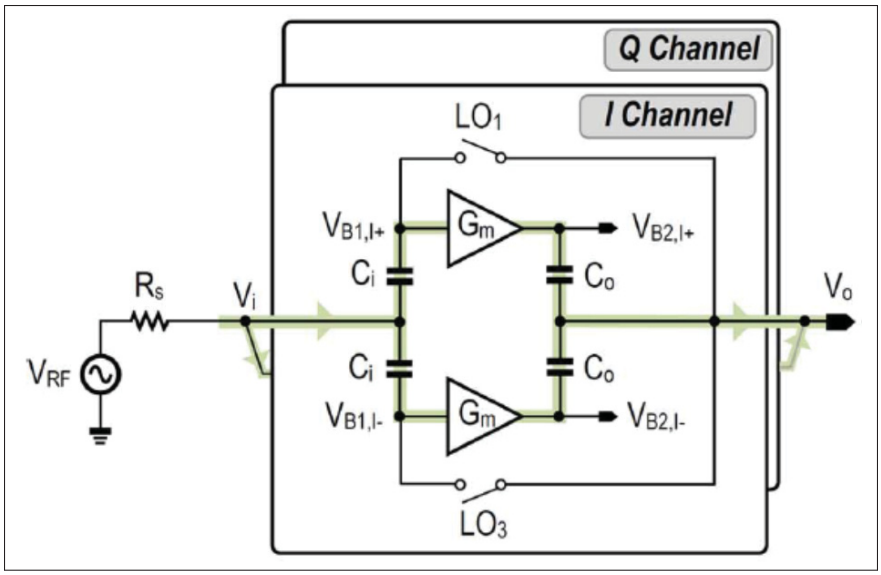

Figure 1.15 Function-reuse receiver with highlighted RF path.
Taken from Lin *et al.* (2014c)

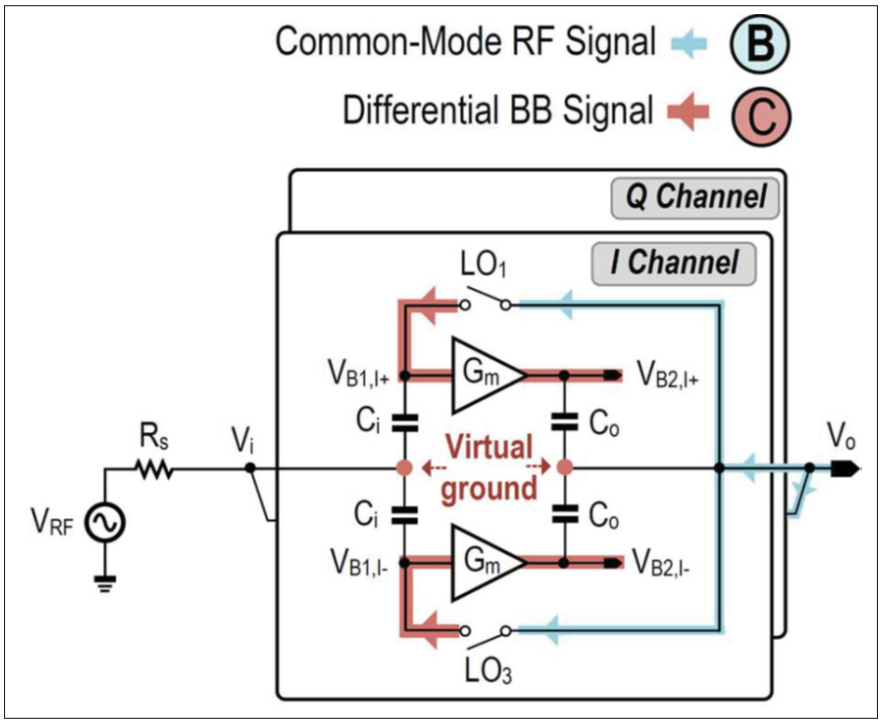

Figure 1.16 Baseband signal path.
Taken from Lin *et al.* (2014c)

The RF current is down-converted to a BB signal through LO switches and amplified with the G_m stage that is shown with a red colour in Figure 1.16. In this way, the G_m stage is employed for both RF and BB signal amplification. The output BB signal is separated from the RF signal with C_o.

Although this architecture consumes very low power, it still has several drawbacks. A feedback loop in the RF path increases the risk of oscillation. Moreover, the design suffers from limited bandwidth and it is only suitable for narrowband designs, and it is susceptible to clock jitter. In addition, reported results show poor linearity. Like the current-reuse technique, the function-reuse technique is also not suitable for a zero-IF receiver. A low IF is recommended by utilizing an image rejection filter.

Next, ultra-low power techniques are discussed and their issues are mentioned.

1.3 Ultra-Low Power Receivers

Recently several ultra-low power (ULP) receiver topologies have been published and proposed circuits with less than 1 mW of power consumtion. In this section, we detail and analyse the drawbacks and benefits of each one.

1.3.1 ULP Receiver for MedRadio Standard using a New Mixing Technique

The circuit shown in Figure 1.17 is proposed for MedRadio applications in the 400 MHz band. The inverter based LNA is used at the input with external inductor for the matching purpose.

A novel active current-reuse inverter based down-conversion mixer enhances gain and reduces NF. When the local oscillator (LO) is ON, the input shorts to the output and attenuates the BB signal. On the other hand, when the LO is off, amplification takes place. In this way, a higher gain and lower NF are achieved in the mixer compared with the conventional passive mixer. The mixer functionality is shown in Figure 1.18. Due to the single balanced configuration of the mixer, linearity degrades to the certain extent. The circuit performance over frequency is

relative to the current consumption. Thus, to work at higher frequencies, a higher current needs to be consumed to achieve sufficient operating bandwidth.

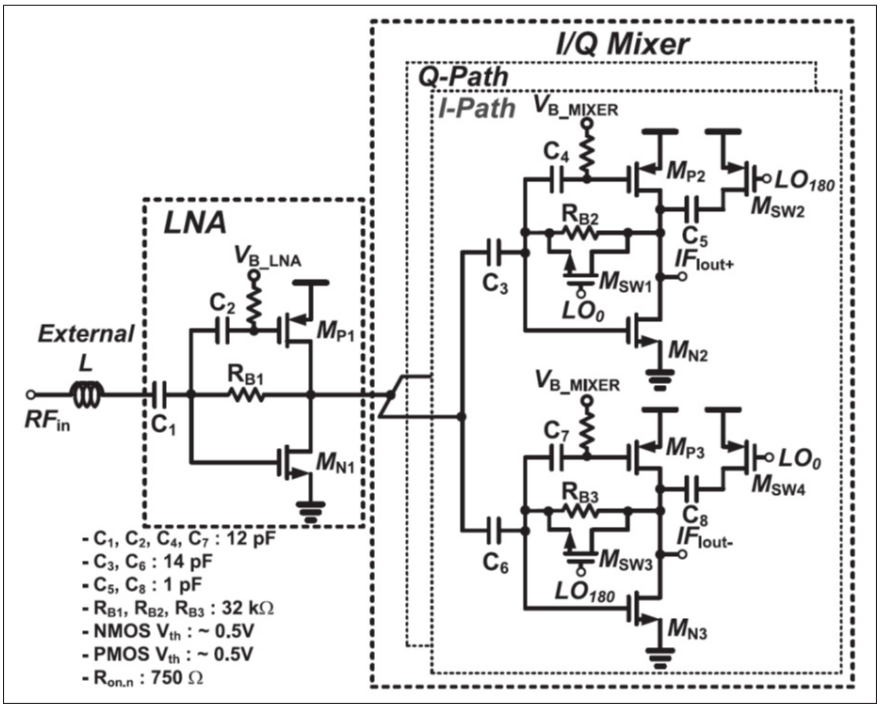

Figure 1.17 Ultra-low power receiver for MedRadio application.
Taken from Choi *et al.* (2015)

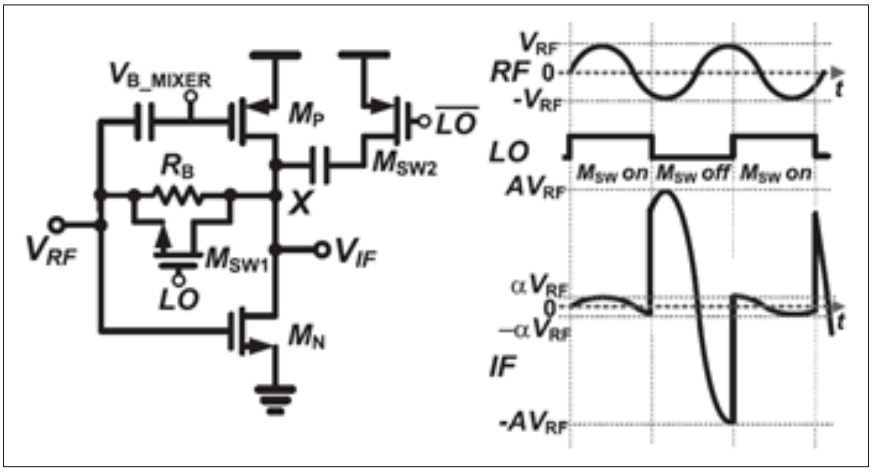

Figure 1.18 Mixer functionality diagram.
Taken from Choi *et al.* (2015)

1.3.2 ULP Receiver using Novel g_m-Boosted Common-Gate LNA

The ircuit proposed in Wang, Li, Cheng, Luo & Gao (2016) employed a common-gate configuration amplifier with an additional novel G_m-boosting technique that is shown in Figure 1.19. G_m-boosting is achieved through a feedforward amplifier. The input voltage is converted to a current and down-converted to BB through double balanced switches. Finally, the current is converted toa voltage through the output resistor.

The proposed circuit consumes very low-power of 0.8 mW in sub-GHz applications. The NF performance is degraded due to the additional components at the input. To reduce NF and increase gain bandwidth at higher frequencies, higher power needs to be consumed. The circuit performance with a conventional cross-coupling capacitor technique is still preferred over the proposed architecture to boost the g_m which enhances the gain and reduces NF.

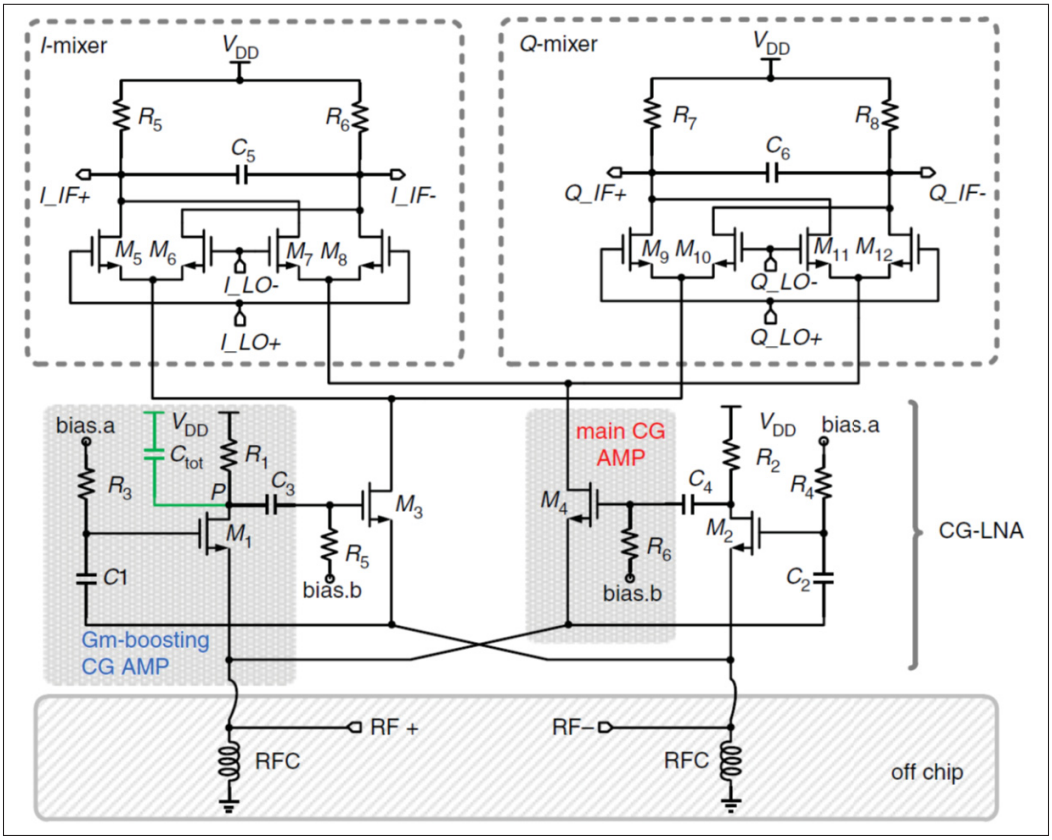

Figure 1.19 Common-gate doubly balanced I/Q receiver front-end.
Taken from Wang *et al.* (2016)

1.3.3 Receiver Employing an LNTA and Current-Reuse Image Rejection Filter

Another ultra-low power approach was proposed by Kargaran, Guo, Manstretta & Castello (2019). The front-end architecture including LNTA and current driven passive mixer is followed by a novel image rejection filter, as shown in Figure 1.20.

The conventional LNTA circuit is shown in Figure 1.21(a) that uses an external LC network matching and on-chip transformer to boost the g_m to improve input matching for low-power designs. The proposed LNTA circuit by Kargaran *et al.* (2019) is shown in Figure 1.21(c) that utilizes the bondwire and additional C_2 without using an extra inductor to improve matching and reduce chip area. The effect of the bondwire variation is shown in Figure 1.21(b) that is acceptable thanks to the reliable common-gate topology which is relative to the effective g_m.

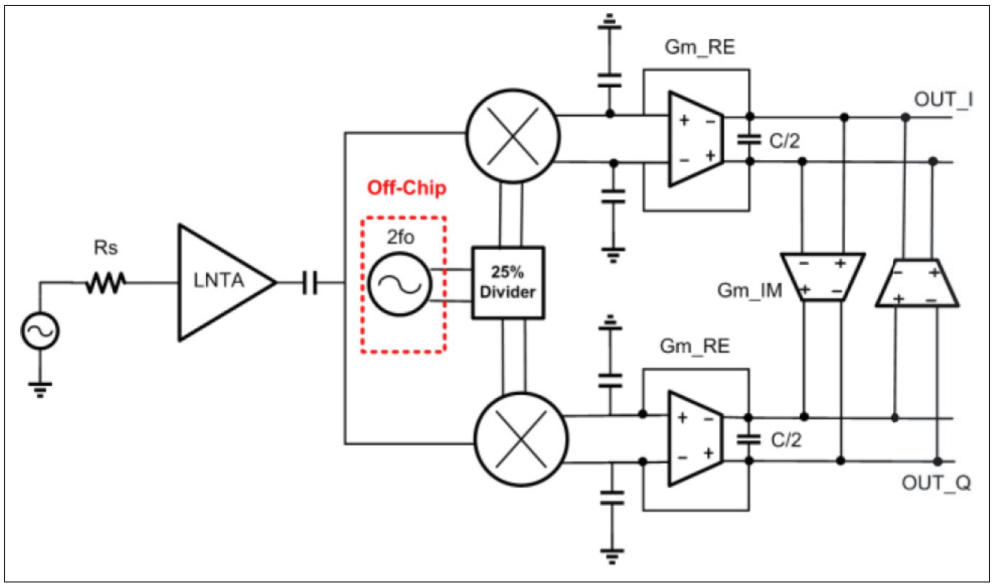

Figure 1.20 RF receiver front-end architecture.
Taken from Kargaran *et al.* (2019)

The circuit shown in Figure 1.22 uses a g_m-boosted input stage to enhance the NF result and complex pole load to improve image rejection for a low-IF receiver. A complex pole is achieved by cross connecting the M_{IM} transistors. To minimize the mismatch effect of the passive mixer, the M_5 transistor with negative feedback is used.

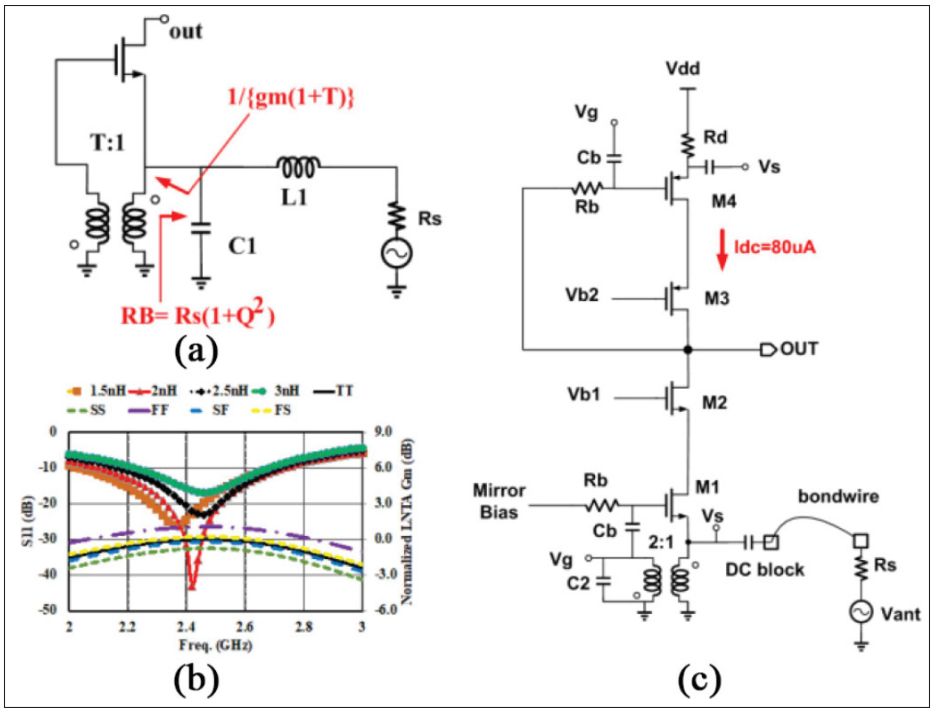

Figure 1.21 (a) Conventional input matching; (b) Simulated bonding effect on S_{11}; (c) LNTA circuit diagram.
Taken from Kargaran *et al.* (2019)

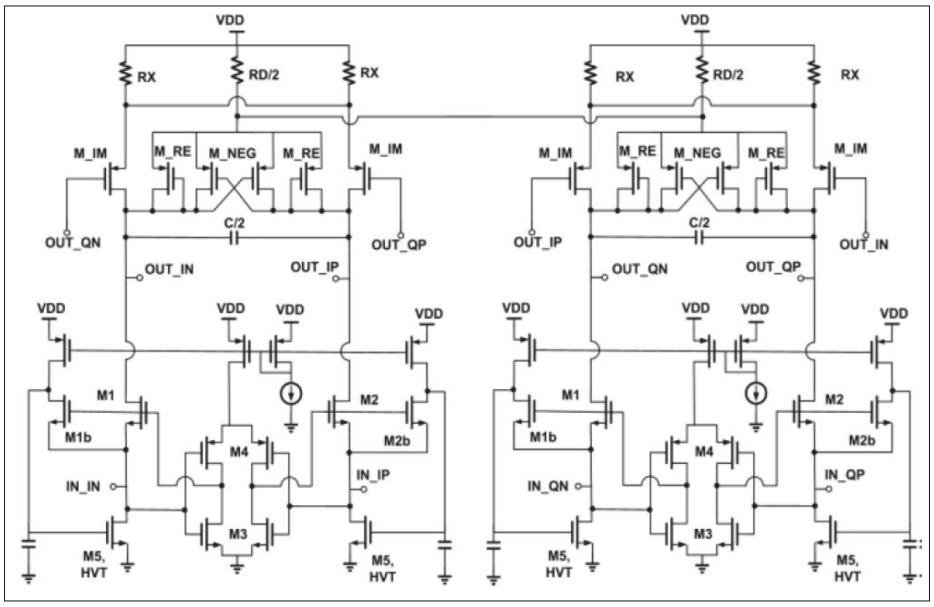

Figure 1.22 I/Q image rejection circuit.
Taken from Kargaran *et al.* (2019)

The mentioned circuit is designed at 2.4 GHz and shows good linearity performance while consuming very low power below 500 µW. An image rejection of 15 dB at 2 MHz IF is reported which required an additional image rejection filter that increases the power consumption. Moreover, Monte-Carlo simulation needs to be performed to make sure image rejection is sufficient when considering process-induced mismatches.

Notably, most of the current-reuse image rejection techniques proposed in the previous sections does not generally provide enough image rejection. It is preferred to include image rejection circuitry separately to achieve better overall performance in the RF front-end.

1.4 Conclusion

Among various receiver architectures studied in this section, the current-reuse architecture is a promising candidate for low-power applications. However, this technique suffers several problems that need to be improved. It suffers from direct leakage of the low frequency noise into the BB that should be improved to make it suitable for a Zero-IF receiver architecture. Better isolation of the RF signal to improve the NF at higher RF needs to be taken into account to make it suitable for large technology nodes such as 130 nm CMOS process and enable low cost implementations that are amenable to IoT-driven applications.

CHAPTER 2

A DESIGN METHODOLOGY FOR WIDEBAND CURRENT-REUSE RECEIVER FRONT-ENDS AIMED AT LOW-POWER APPLICATIONS

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Article published in *MDPI Electronics*, August 2022.
https://doi.org/10.3390/electronics11091493

Abstract: This work gives a design perspective on low-power and wideband RF-to-Baseband current-reuse receivers (CRR). The proposed CRR architecture design shares a single supply and biasing current among both LNTA and baseband circuits to reduce power consumption. The work discusses topology selection and a suitable design procedure of the low noise transconductance amplifier (LNTA), down-conversion passive-mixer, active-inductor (AI) and TIA circuits. Layout considerations are also discussed. The receiver was simulated in 130 nm CMOS technology and occupies an active area of 0.025 mm^2. It achieves a wideband input matching of less than -10 dB from 0.8 GHz to 3.4 GHz. A conversion-gain of 39.5 dB, IIP3 of -28 dBm and a double-sideband (DSB) NF of 5.6 dB is simulated at a local-oscillator (LO) frequency of 2.4 GHz and an intermediate frequency (IF) of 10 MHz, while consuming 1.92 mA from a 1.2 V supply.

Keywords: current-reuse receiver; common gate; common source; low power; current sharing; low noise.

2.1 Introduction

The fast growing Internet of Things (IoT) is creating smart environments that have the potential to significantly improve our quality of life. This includes IoT systems used in location tracking and positioning, such as vehicles or drones for navigation, home automation, in the health industry to monitor patients and in agriculture to optimize and control watering systems, etc. This requires IoT devices with low power consumption, which will translate into billions of IoT devices that will require significant aggregate power consumption to operate. Accordingly, reducing the power consumption in each IoT device by a fraction can lead to an important overall energy use reduction globally.

Notably, in a typical IoT module, the RF transceiver plays a significant role in defining the overall power consumption of a given system. This work thus aims at giving insights regarding how to reduce the power consumption of RF transceivers. There are several techniques to reduce the power consumption of RF transceivers, including current sharing of the baseband and RF front-end by stacking a transimpedance amplifier (TIA) on top of the low transconductance amplifier (LNTA) and mixer, which is very effective compared to the conventional technique that cascades the LNTA, mixer and TIA.

There have been a wide range of studies into current-reuse techniques for RF receivers, leading to the introduction of the current-reuse receiver (CRR) architecture. Conventionally, in such receivers, current-reuse is employed in the LNTA design to boost the transconductance by stacking both PMOS and NMOS transistors and sharing their current bias through a single supply (Shams *et al.* (2020)). Recently, the current-reuse technique has been applied to receiver design by stacking several blocks such as the LNTA, mixer and TIA and sharing the biasing current among all of these circuits. In this fashion, power consumption can be reduced significantly. In Tedeschi *et al.* (2010), a voltage-controlled oscillator (VCO), mixer and LNTA are stacked to share the biasing current from a single supply. This reduces the overall power consumption significantly, but the design suffers from a high noise figure (NF) and VCO injection locking. Similarly, in Cai, Shi, Hu & Wang (2020), VCO and LNA are stacked, thus reducing the

power consumption at the price of narrowing the bandwidth, potentially becoming prone to VCO injection locking as in Tedeschi *et al.* (2010). A balun LNA, active mixer and hybrid baseband filter are stacked in Lin *et al.* (2014b) to form a current-reuse topology to reduce power consumption. However, the active-mixer consumes voltage headroom, which reduces linearity. Another approach is the function-reuse technique employed in Lin *et al.* (2014c), where a push–pull amplifier is used to function as both the LNTA and TIA. However, a poor linearity of -50 dBm due to the low supply voltage is reported. Moreover, this approach is suitable for sub-GHz applications only. In Lin *et al.* (2014a), a current-reuse receiver using an N-path passive mixer for input matching and an active mixer for down-conversion is used. This topology needs additional voltage headroom for its active mixer, increasing its supply voltage requirement. Moreover, it requires an additional circuit to combine the N paths, consuming additional power. Another approach introduces the $1/f$ noise-cancellation (NC) technique. However, it consume a high power of 8 mW Ghosh & Gharpurey (2011). Another alternative in Kim & Kwon (2019) utilizes both input matching and a $1/f$ NC technique and reports a low NF of 1.94 dB at the cost of very narrow bandwidth. The same current-reuse receiver architecture is employed in Abbasi, Shams, Kakhki & Nabki (2020a) but utilizes a cross-coupled common-gate (CCCG) LNTA topology to enhance the operating bandwidth. However, both Kim & Kwon (2019); Abbasi *et al.* (2020a) suffer from the loading effect on the RF signal due to the sharing of the passive mixer input and receiver output nodes. A quadrature RF-to-BB current-reuse receiver is proposed in Park & Kwon (2021), which comprises the architecture from Kim & Kwon (2019). It reports a very high NF of 13.2 dB despite using a common-source LNTA topology with a low noise contribution and narrow bandwidth. In Ramella *et al.* (2017), the concept of an active-inductor (AI) was introduced, and this was used in our earlier works Abbasi, Shams & Nabki (2020b) to overcome the issues mentioned above.

In order to provide design insights into low-power CRR circuits, this work provides a design procedure, characterization and more depth into the design methodology behind the circuit proposed in our earlier work Abbasi *et al.* (2020b). It includes the topology selection and design of the LNTA, down-conversion mixer and active-inductor (AI). The concept and design of the

TIA is described as well. The paper provides all of the design steps and test benches required, along with the mathematical calculations necessary for the design. The paper is structured as follows. Section 2.2 overviews the design steps and test benches of the circuit implementation, Section 2.3 presents system integration considerations, Section 2.4 discusses circuit layout aspects, and Section 2.5 presents the post-layout simulation results of the resulting design and discusses them.

2.2 RF-to-BB Current-Reuse Receiver Front-End Circuit Level Design

Thanks to the CMOS scaling, which reduces the threshold voltage of the transistors, V_{TH}, and increases their frequency of operation (i.e., transition frequency ω_T or f_T), the stacking of several circuits sharing a single supply is possible. However, this introduces design challenges, which are discussed in Abbasi *et al.* (2020b). The current-reuse receiver (CRR) block diagram proposed in Abbasi *et al.* (2020b) is shown in Figure 2.1. In this section, the detailed design steps, test benches and topology selections are discussed.

2.2.1 Low Noise Transconductance Amplifier

In CRR front-ends, the LNTA plays a significant role in defining the overall performance of the CRR, such as its sensitivity, input matching and power consumption. There are two well-known LNTA topologies that can be employed: common-source (CS) and common-gate (CG). The common-source topology is suitable for very low-noise applications, where the noise-figure (NF) is given by Razavi (2013)

$$NF_{CS} = 1 + g_m R_S \gamma \left(\frac{\omega_o}{\omega_T}\right)^2, \tag{2.1}$$

where g_m is the transconductance, R_S is the source impedance, γ is the channel effect, ω_o is the operating frequency, and ω_T is related to the maximum frequency at which that transistor can operate effectively (i.e. transition frequency). Equation (2.1) shows that a higher ω_T results in a very low NF in the CS LNTA topology. The NF in CG topology is given by

$$NF_{CG} = 1 + \frac{\gamma}{g_m R_s}. \tag{2.2}$$

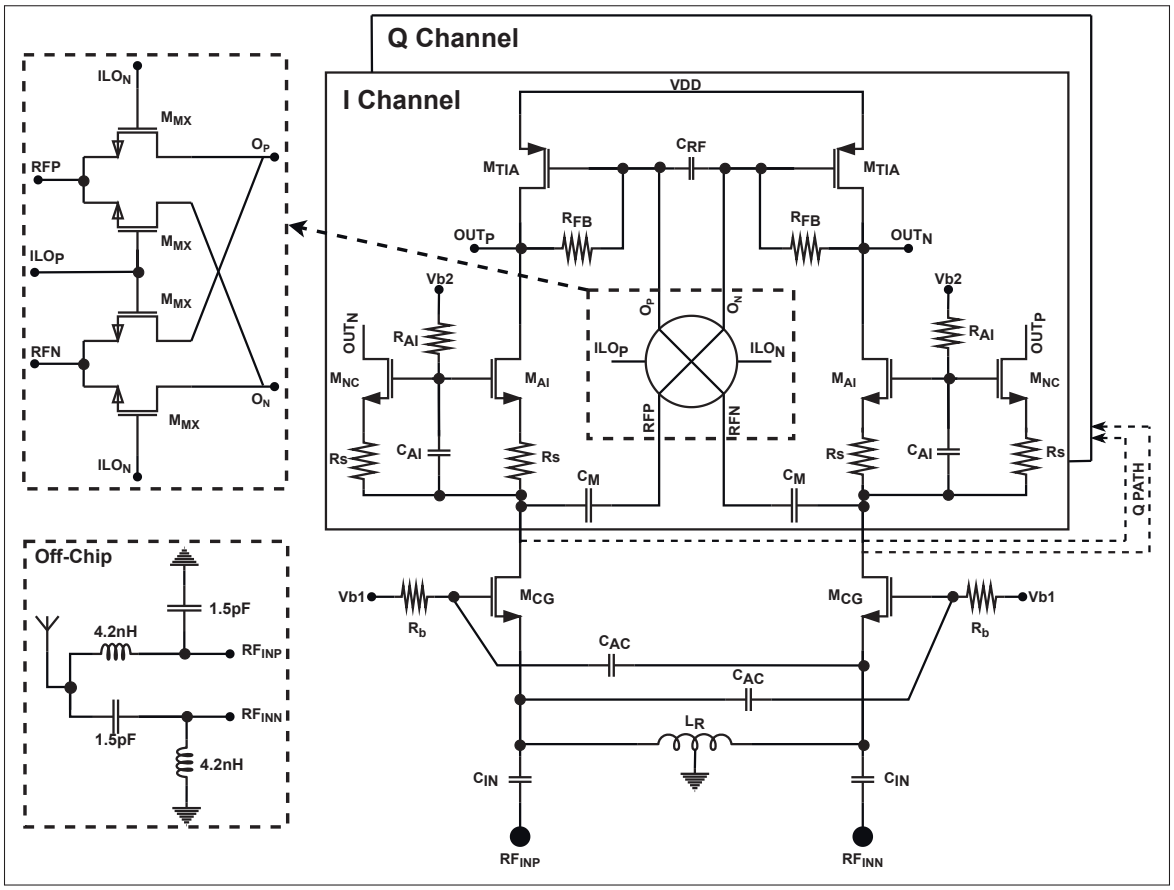

Figure 2.1 Block diagram of the proposed current-reuse receiver.
Taken from Abbasi *et al.* (2020b)

It is undeniable that the CG topology achieves much higher NF (>3 dB) than the CS topology since the second term in Equation (2.1) is suppressed by ω_T when $\omega_T \gg \omega_o$. On the other hand, the CG topology is more suitable for wideband applications, while the CS topology results in narrow-band input impedance matching. The input impedance considering the CS LNTA is given by

$$Z_{CS} = s\left(L_g + L_s\right) + \frac{1}{s(C_{gs} \parallel C_{par})} + \omega_T L_s, \tag{2.3}$$

where L_g is a series gate inductor, L_s is an source-degeneration inductor, C_{gs} is the gate to source capacitance, and C_{par} is the parasitic capacitance considering the input of the LNTA, such as the pad and ESD cell capacitance. Equation (2.3) shows that the CS topology is suitable for narrow-band applications. On the other hand, the input impedance considering the CG LNTA is calculated by $1/g_m$ which is a real impedance. Hence, the CG LNTA topology is very suitable for wideband applications as it can be readily matched to the antenna (e.g., 50 Ω). Thus, topology selection for the LNTA depends on the application requirements. The receiver in Abbasi *et al.* (2020b) requires a wideband operation to cover a wide range of frequencies for several wireless standards; hence, the CG topology is suitable for this goal at the cost of a higher NF compared with the CS topology.

The LNTA design begins with an optimization of g_m and f_T. Figure 2.2a shows a test bench utilized to optimize and characterize g_m and f_T. Less than half of the supply voltage is applied to the drain terminal, which is close to the voltage that is expected after the receiver integration. The simulation is performed by sweeping the biasing current (I_{ds}) while the width over length ratio (W/L) is maintained at constant value. To observe the channel-length effect, W and L are increased with a scaling coefficient from W/L to 5W/5L, resulting in the plots shown in Figure 2.2b,c. This shows that, by increasing the current for a given W/L, both g_m and f_T increase to a certain value until they flatten. The short channel effect can be reduced by increasing L. Thus, by increasing both W and L by the same scaling factor, g_m improves. However, f_T reduces due to the increase in gate-source and gate-drain capacitance. In the CG topology, f_T is not the main contributor in the NF equation, but it is preferred to maintain it to be at least 10 times higher than the operating frequency to avoid any non-idealities such as oscillations. In this case, a scaling factor of 2 (i.e., 2W/2L) is selected. To achieve the required g_m for input matching, both the width and the current need to increase. This can lead the circuit to consume high power. One approach to reduce the power consumption is to use the capacitive cross-coupling technique to boost the transconductance by a factor of 2. In this way, half of the current is required to achieve

the required g_m. The LNTA requires a current path to ground, and this can be achieved using either a resistor or inductor. In Abbasi *et al.* (2020b), an inductor is used to reduce the voltage headroom requirement and the RF signal loss by resonating with the parasitic capacitance. Note that further device optimization will need to be performed after receiver integration.

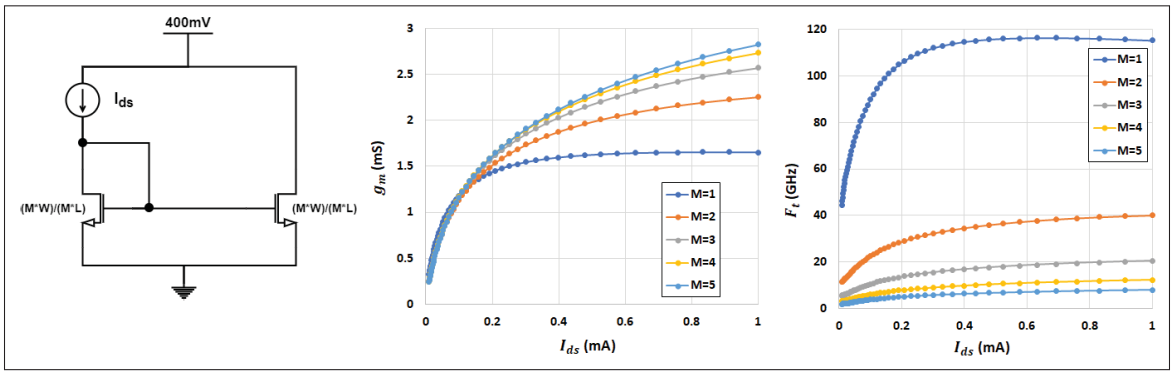

Figure 2.2 (**a**) Test bench to optimize and characterize g_m and f_T, (**b**) resulting g_m plots, and (**c**) resulting f_T plots.

A single-ended antenna input needs to be converted to a differential signal at the input of the receiver. Both single to differential and LC baluns can be used. An LC-balun achieves a lower NF than a differential balun at the cost of a narrower bandwidth, but its combination with a CG LNTA topology provides wide bandwidth. Moreover, an LC-balun is able to convert the antenna impedance to any impedance considering the LNTA by adjusting the L and C values. This gives more flexibility to the design and allows it to operate at higher g_m.

2.2.2 Down-Conversion Mixer

There are two choices of down-conversion mixers: active and passive. A passive mixer is preferred over an active mixer since active mixers require voltage headroom, which is not desirable due to the resulting poor linearity performance. Moreover, low-frequency noise can be filtered out using an AC-coupling capacitor at the input of the passive mixer. Thus, in Abbasi *et al.* (2020b), a passive mixer is used to down-convert the RF signal to the IF. A double-balanced passive mixer, as shown in Figure 2.1, is used. To design the mixer switches and optimize the

W/L ratio, where L is minimum, a test bench that models the receiver front-end is employed as shown in Figure 2.3. In this test bench, the LNA and TIA are ideal macro-models. A voltage controlled current source (VCCS) is used to convert the RF voltage to the RF current to perform as an LNTA. The LNTA output impedance is modeled by R and C. R_1, C_1 and an OpAmp model define the TIA macromodel. The design of the mixer switches is performed by sweeping the value of the W/L ratio and the gate voltage of the mixer switches concurrently in order to achieve the best NF and linearity. Figure 2.4 shows the NF and 1 dB compression point (P1dB) performance versus the W/L ratio and the gate voltage of the switches, VCM. The best integrated double side band noise figure (DSBNF), from 1 MHz to 10 MHz, is achieved at a VCM of 800 mV, while the P1dB at 600 mV is 1.4 dB higher than at a VCM of 800 mV. Very large mixer switches need to be avoided to minimize large parasitic capacitors at the input of the mixer that attenuate the RF signal and cause LO to RF leakage. Thus, a W/L ratio of 35 µm/130 nm is selected as a suitable trade-off value. Moreover, the gate voltage should be below the breakdown of the transistors when the LO signal switches high or low. Final optimization is needed after receiver integration.

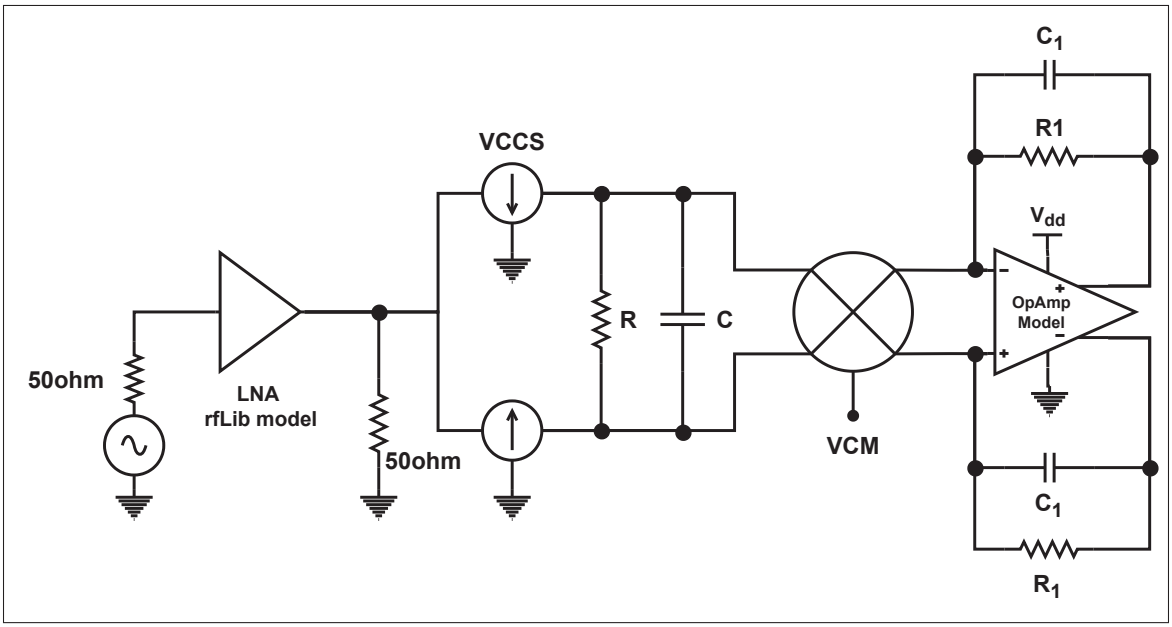

Figure 2.3 Test bench to design and optimize the down-conversion mixer switches.

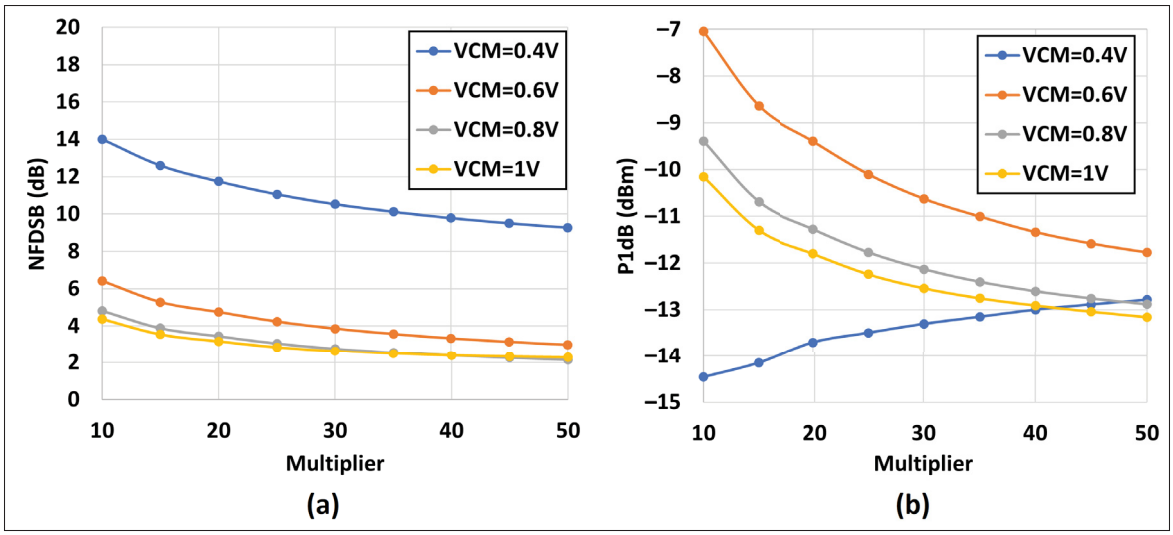

Figure 2.4 (**a**) The noise figure and (**b**) the 1 dB compression point versus the W/L ratio for different gate voltages of the input transistors.

2.2.3 Active Inductor and Noise Cancellation

In Kim & Kwon (2019), the mixer input and receiver output share the same node, which causes RF signal losses. As a result, the design is not able to operate at very high frequency and is more suitable to sub-GHz applications. In our earlier works Abbasi *et al.* (2020b), the concept of an AI was introduced. In this design, cascoded devices are used to boost the output impedance, as shown in Figure 2.1 (M_{AI}). The impedance considering the AI circuit, Z_{AI}, by ignoring M_{NC} since it is in parallel, is summarized and given by

$$Z_{AI}(s) \cong \frac{g_{m,AI}R_S(R_{AI}C_{AI}s+1)+R_{AI}C_{AI}s}{g_{m,AI}R_SC_{AI}s+g_{m,AI}+C_{AI}s} \,||\, \frac{1}{sC_{par}}, \tag{2.4}$$

where C_{par} is the parasitic capacitance at the mixer input and is related to the technology node.

The impedance from the LNTA to the AI is very small at lower frequencies and increases at higher frequencies. This helps to isolate the RF signal from the output node. In this case, the mixer input connects to the LNTA output directly, where the majority of the RF signal flows through the mixer input due to the lower input impedance compared to that of the AI.

Figure 2.5a shows the test bench to design the AI circuit. The AI circuit includes M_{AI}, R_{AI} and C_{AI}. R_S is used to boost the impedance at higher frequencies. A small value is considered to avoid excessive voltage headroom usage. M_{TIA} and R_{FB} are used to model the TIA circuit. R_{AI} and C_{AI} should be optimized to define the cut-off frequency. The transconductance of M_{AI} defines the impedance of the AI at DC and low frequencies. A small signal, I_{AC}, is applied to the input of the AI circuit, and V_{AC}/I_{AC} is calculated to extract the input impedance of the AI circuit, Z_{AI}. Figure 2.5b illustrates the magnitude of Z_{AI} versus the frequency with and without R_S being considered. It is obvious that R_S helps to boost the AI input impedance at the cost of voltage headroom. Thus, there is a trade-off between the NF and linearity when the value of R_S is defined. The gate terminal of M_{AI} needs to be biased with a voltage, V_b, of 800 mV to keep it in saturation.

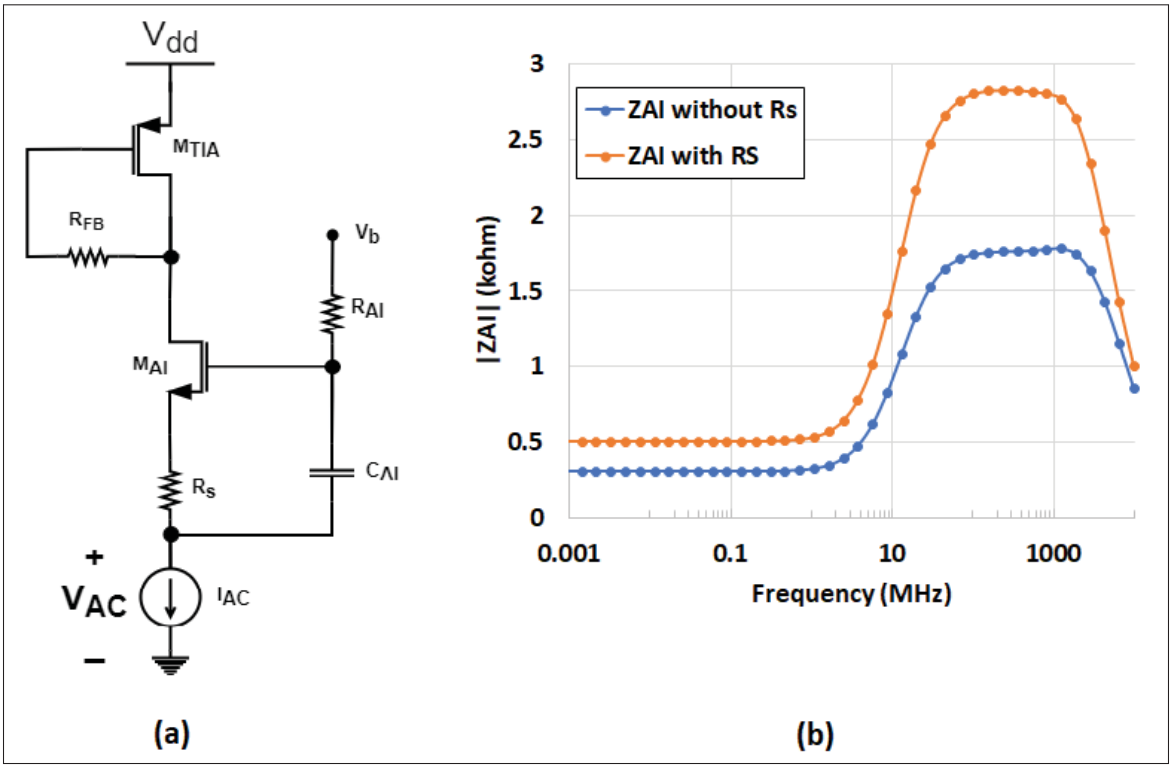

Figure 2.5 (**a**) Test bench to design the active inductor and (**b**) its impedance magnitude over frequency with and without R_S considered.

The magnitude of Z_{AI} is shown for different C_{AI} values in Figure 2.6. This illustrates that a higher C_{AI} value pushes the cutoff frequency of Z_{AI} to a lower frequency and increases its magnitude at high frequency, while it remains constant at lower frequencies. A value for C_{AI} of 1 pF shows a good trade-off value between the frequency cutoff and maximal impedance magnitude. Another step in the design of the AI circuit is to select the best W/L ratio of M_{AI}. Figure 2.7 shows that increasing the W/L ratio of M_{AI} with the multiplier from 2 to 8 leads to a higher g_m and a lower Z_{AI} magnitude at lower frequencies. A W/L ratio of M×10 µm/260 nm, where M is equal to 4, is selected as a good trade-off between low-frequency and high-frequency impedance behavior.

Final component value fine tuning can be performed after receiver integration.

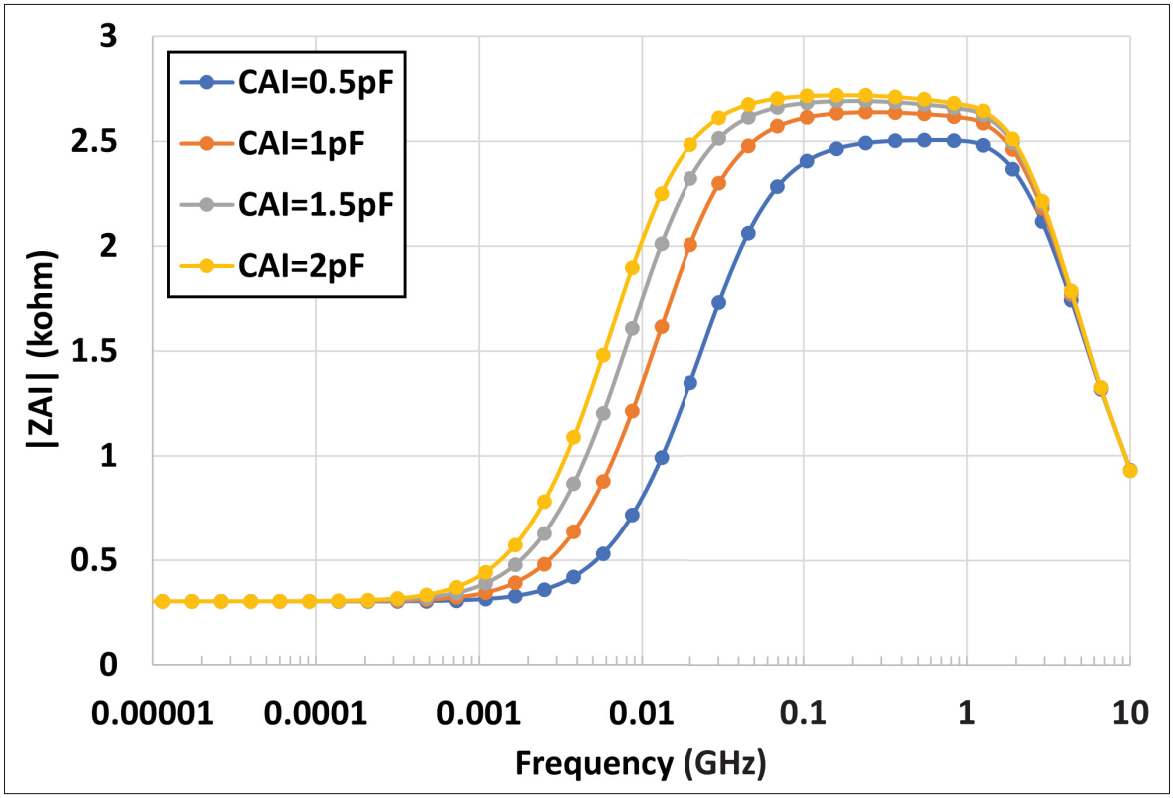

Figure 2.6 Magnitude of Z_{AI} for different values of C_{AI}.

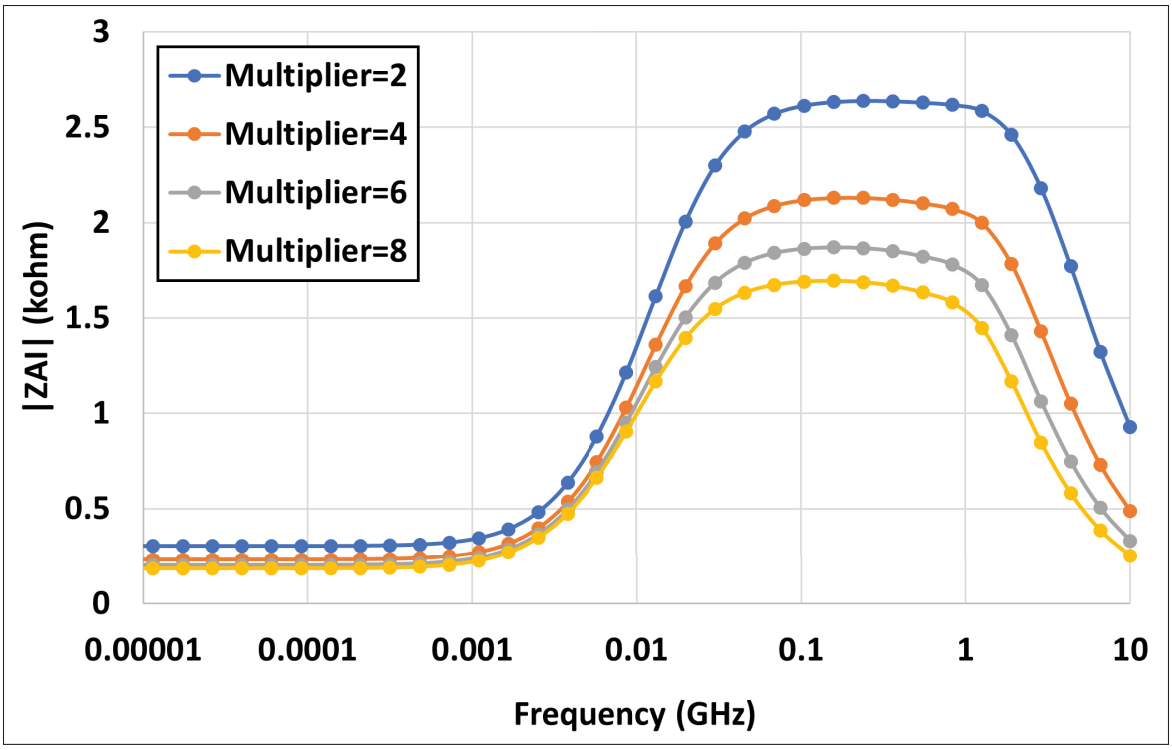

Figure 2.7 Magnitude of Z_{AI} for different W/L ratio multipliers of transistor M_{AI}. The unit W/L ratio is 10 µm/260 nm.

2.2.4 Transimpedance Amplifier

The final step is to design the baseband (BB) circuit in the CRR front-end where the BB current needs to be converted to a BB voltage at the output. In Kim & Kwon (2019); Abbasi *et al.* (2020b), a TIA is designed using a single transistor with a feedback resistor, R_{FB}, shown in Figure 2.1. A large channel-length value should be used to enhance the TIA output impedance. The impedance considering the TIA is defined by $1/g_m$ of M_{TIA}. The conversion gain is approximately calculated through the following relation:

$$Conv.Gain \cong \frac{2\sqrt{2}}{\pi} g_{m,eff} R_{FB}. \tag{2.5}$$

where $g_{m,eff}$ is $2 \times g_m$ of transistor M_{CG} thanks to the capacitive cross-coupling technique, which boosts the g_m by almost two times. R_{FB} should be large enough to achieve the required conversion gain. The output common-mode voltage can be slightly higher than half of the supply voltage in order to provide more voltage headroom for the AI and LNTA circuits. A value for C_{RF} of 1 pF is used to remove high-frequency components at the output of the mixer right before the TIA input.

After all of the aforementioned circuits are integrated within the CRR structure, an optimization needs to be performed by small adjustments to the component values in order to achieve the best possible performance.

2.3 System Integration

CRR Front-End

The design of each circuit part of the CRR has been discussed in Section 2.2, which covered the design choices, theoretical analysis, design flow and test benches. The sub-blocks need to be integrated as shown in Figure 2.1 to form the CRR front-end. This includes the LNTA with external LC-balun to convert RF voltage to current, a passive mixer to convert the RF signal to a baseband current, a TIA to convert the baseband current to a voltage at the output and finally the AI circuit to isolate the RF signal from the output in order to reduce the RF signal loss.

The TIA, AI and LNTA are cascoded to share a single supply of 1.2 V. The performance of the CRR front-end should be verified through simulations versus several design metrics such as biasing voltages to make sure the design is robust. This begins with the NF and CG performance versus the gate voltage biasing of the LNTA, as shown in Figure 2.8. This illustrates that a voltage bias of 365–375 mV achieves almost a constant conversion gain and NF performance. The performance starts to degrade at higher biasing voltages due to the resulting poor input matching, as shown in Figure 2.9 and voltage headroom limitation. The S_{11} starts degrading at

biasing voltages above 380 mV since g_m increases due to the larger device current stemming from the increase in V_{GS}.

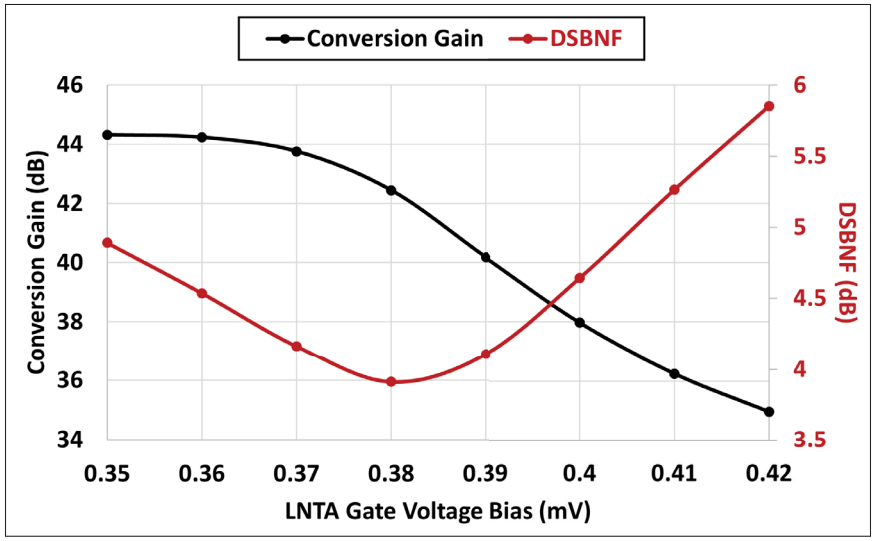

Figure 2.8 The NF and conversion gain versus the gate bias voltage of the LNTA.

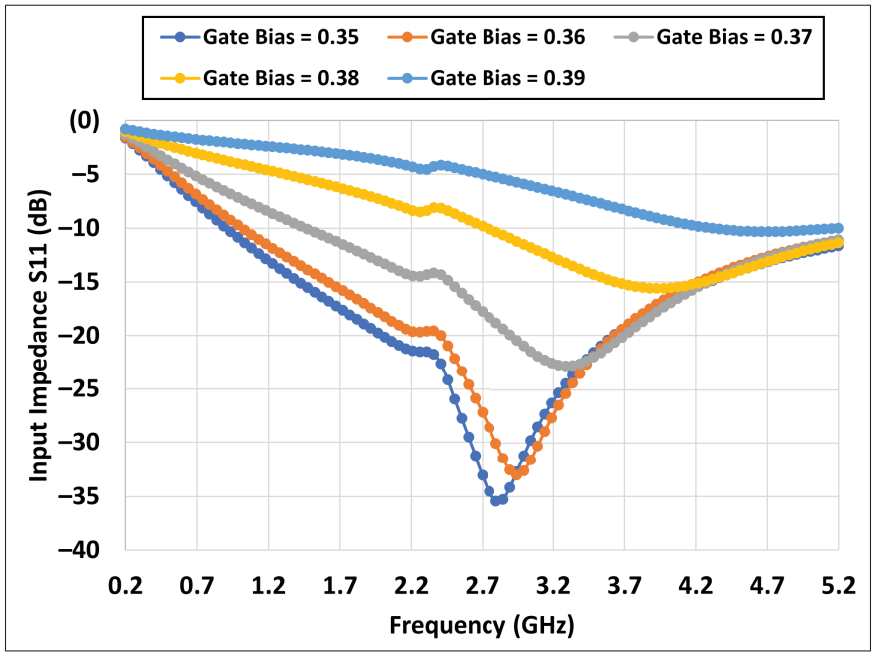

Figure 2.9 The input matching (S_{11}) versus frequency for several gate bias voltages of LNTA.

It is important to optimize the gate biasing voltage of the mixer switches. Figure 2.10 shows the NF and conversion gain of the CRR front-end versus the gate biasing of the mixer switches. It shows a flat conversion gain and NF performance versus a wide rage of biasing from 0.6 V to 0.9 V, which is beneficial to compensate for bias variations.

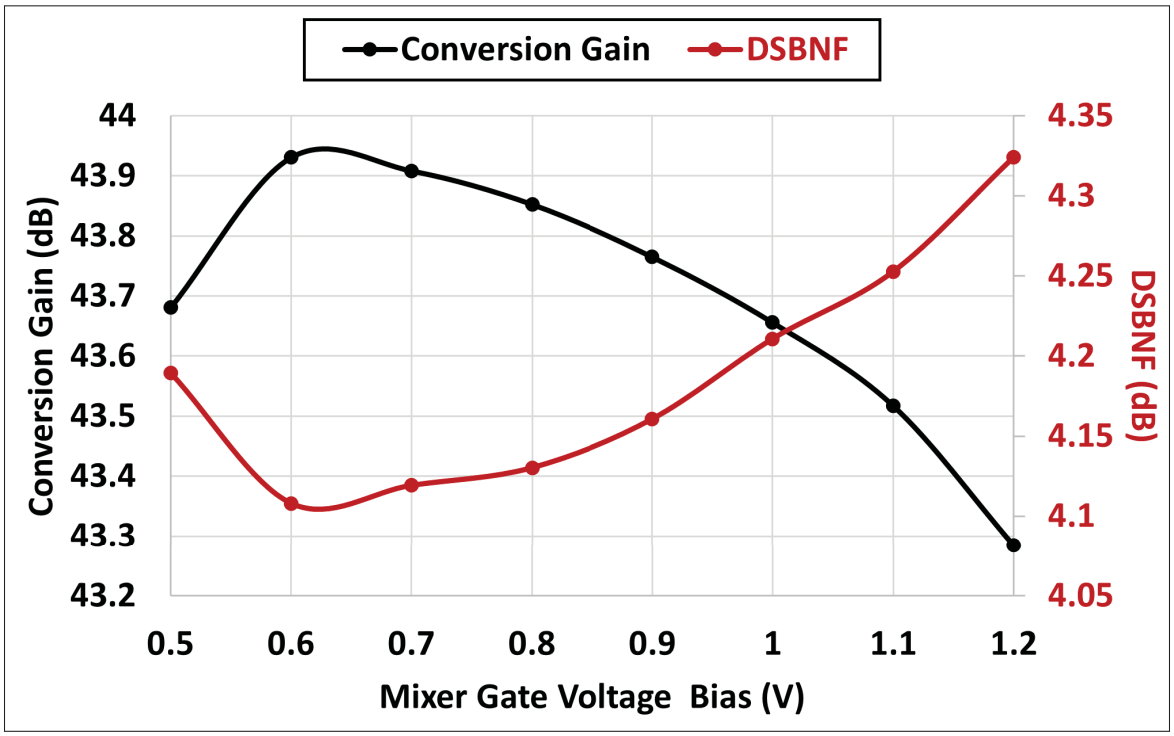

Figure 2.10 The NF and conversion gain versus the gate bias voltage of the mixer.

The performance of the CRR front-end needs to be verified across a wide supply voltage range since the current-reuse architecture depends on the available voltage headroom. Figure 2.11 shows the NF and conversion gain performance versus the supply voltage sweep from 1 V to 1.5 V. It shows a very stable performance versus the supply variations. The conversion gain changes by almost 3 dB from a supply going from 1.1 V to 1.3 V, and the NF is almost constant at 4.1 dB.

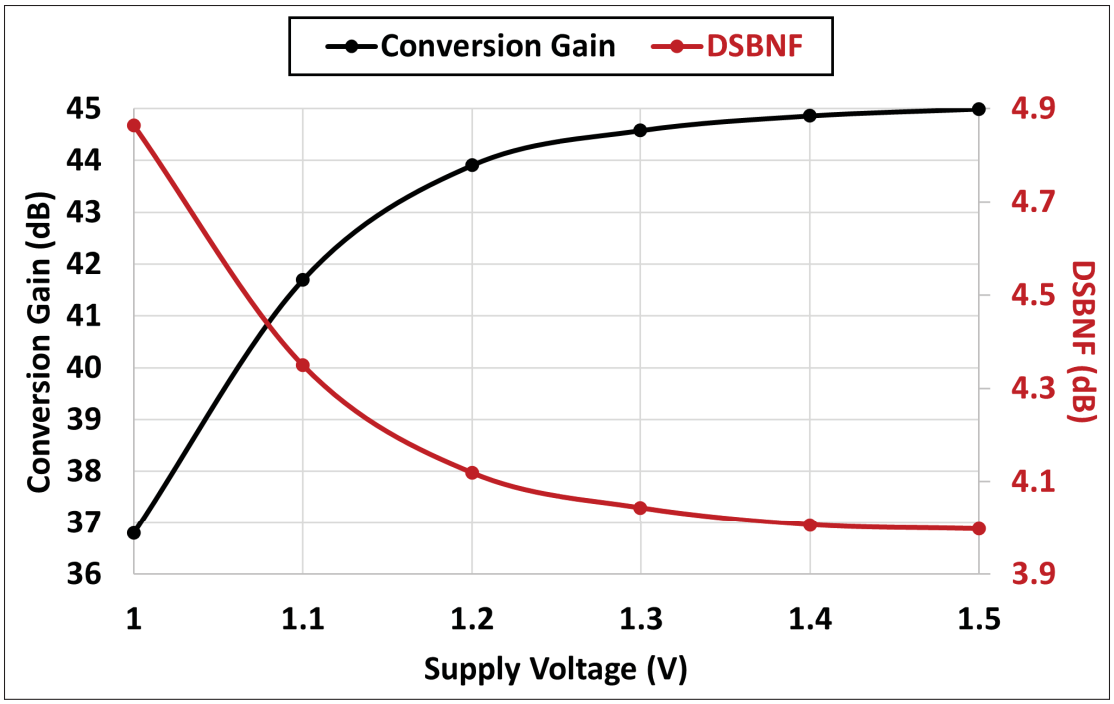

Figure 2.11 The NF and conversion gain versus supply variations.

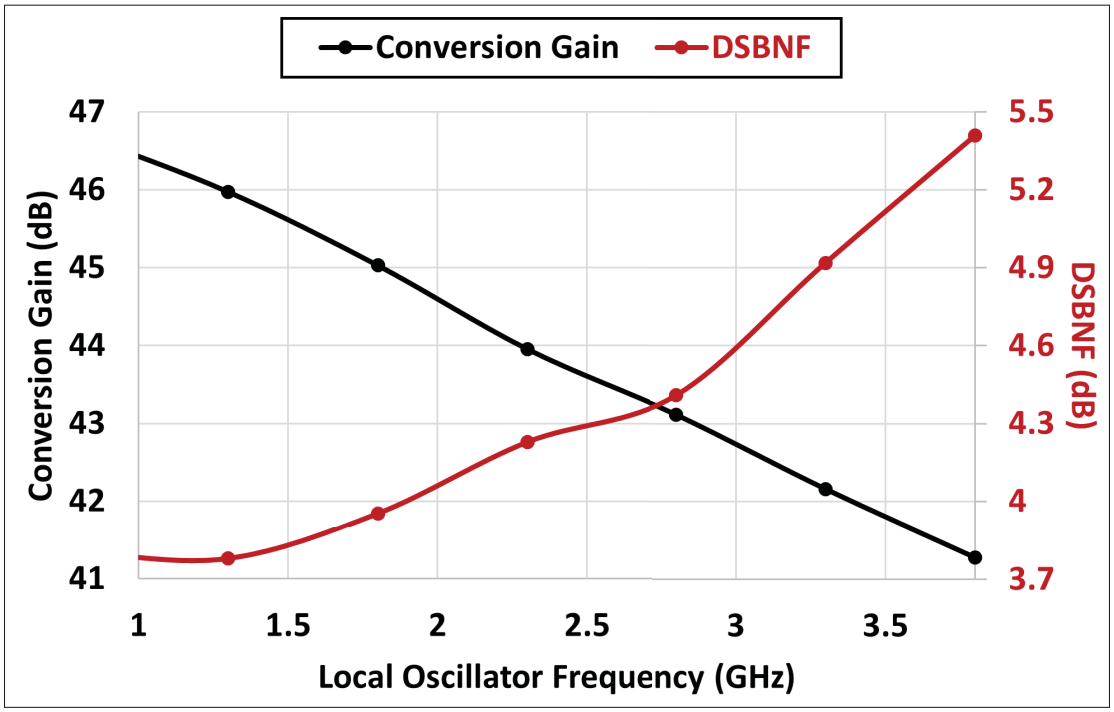

Figure 2.12 The NF and conversion gain versus the LO frequency.

Finally, the performance needs to be verified over the RF bandwidth from 1 GHz to 3.8 GHz in order to cover the wideband operation of the studied receiver. Figure 2.12 shows the NF and CG performance versus the LO frequency. It shows that the conversion gain reduces while NF increases versus the LO frequency sweep due to the losses of the parasitic capacitors after the LNTA.

The linearity performance of the CRR front-end is verified through post-layout simulations in Section 2.5.

2.4 Layout Considerations

Analog circuit design is always challenging since many design metrics need to be considered while designing a circuit. This can be more complex when designing RF circuits. It is always crucial to think of the impact of the layout on the performance during the schematic level design. Thanks to the evolution of process design kits (PDKs), many layout non-idealities such as gate resistance and terminal-to-terminal capacitance are modeled in the RF device models. However, the routing effects and substrate leakage are not modeled at the schematic level. Hence, the layout considerations are discussed here in order to ensure the performance of the CRR front-end after post-layout simulations and ultimately after fabrication.

2.4.1 LNTA Layout

The LNTA is the first circuit in the receiver front-end that receives the weak signal. Routing to the LNTA input and output needs to have the minimum parasitic resistance to avoid the degradation of NF and S_{11} and to ensure a minimum parasitic capacitance. In this case, top metal layers are preferred to reduce metal resistance and substrate leakage, but it is preferred to reserve the topmost metal layer for supply and ground routing. It is very important to keep routing resistance and capacitance low where the RF signal path passes through in areas such as the capacitive cross-coupling, which is used to enhance the transconductance. In the LNTA layout, it is beneficial to maintain the layout symmetry but avoid using any conventional analog

matching techniques since these increase the parasitic capacitance. The capacitive loading effect on the inductor may change the resonant frequency. In this case, a capacitor of 1 pF should be added to the schematic during the schematic design phase, which can be reduced after post-layout simulation is performed. Vias always have high resistance; hence, it is preferred to increase the number of vias to reduce the resistance. This can worsen with the scaling down of the CMOS node.

2.4.2 Mixer Layout

The mixer layout is also important as it is paramount to maintain the symmetry in the mixer layout to avoid any non-idealities related to the even-order harmonics. It is also important to keep the parasitics at the gate and the source of the switches equal to avoid LO-RF and LO-IF feed-through. This can be done by carefully drawing the input, output and LO routes. While routing the LO path, it is essential to isolate it with ground routing underneath the LO routing to avoid the substrate leakage of the high-power LO signal that may degrade the performance of the entire chip. In this case, the LO signal can be routed with metal five while it is shielded by metal four, which is connected to ground. While designing the mixer, it should not be made very large to avoid parasitic loading on the RF ports.

2.4.3 Baseband Circuits

Layout considerations are more relaxed when it comes to the BB circuits. Nonetheless, the routing and circuits after the mixer should keep both symmetry and ensure matching, while parasitic capacitances are not as critical to minimize. While sizing the BB transistors, a sufficient number of fingers and multipliers needs to be used to match the components appropriately. Two well-known layout techniques can be used to perform the matching of baseband circuits: common-centroid and inter-digitization. In this work, inter-digitization is used to create the layout of the AI and TIA circuits. In BB circuits, parasitic resistance is important. Thus, low-resistance metal with sufficient width should be used.

2.4.4 Floor Plan

The complete integration of the sub-circuits requires routing from the pads to the LNTA input. The parasitic capacitance needs to be minimized as much as possible to reduce RF signal losses. It is essential to use high metal layers to draw routing to the LNTA input. Sensitive nets can use several pads to reduce the effect of wire bonding. It is suggested to employ high metal layers while connecting the sub-circuits as well. High metal layers can be used to connect the LNTA output to the mixer input, while lower metals can connect the BB and AI circuit. To avoid RF signal loss, the parasitic capacitance at the LNTA output needs to be reduced, as indicated in (2.6).

2.5 Post-Layout Simulation Results and Discussion

The wideband and low-power RF-to-baseband CRR front-end was implemented with TSMC 130 nm CMOS technology. The layout is shown in Figure 2.13. The CRR front-end only occupies an active area of 0.025 mm^2. It consumes a very low current of 1.92 mA from a supply voltage of 1.2 V.

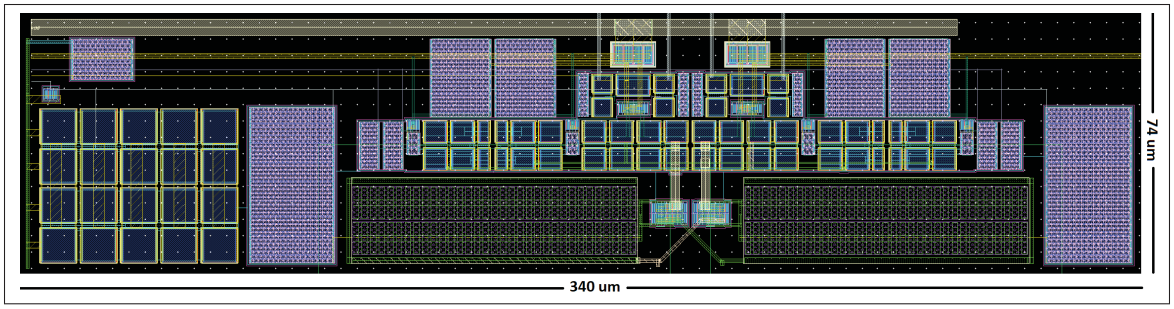

Figure 2.13 The layout of CRR front-end .
Taken from Abbasi *et al.* (2020b)

The NF and conversion gain are post-layout simulated versus the IF, while the LO frequency is constant at 2.4 GHz, as shown in Figure 2.14. At frequencies above 10 MHz, a flat NF of 4.5 dB is achieved, while an integrated DSB NF of 5.6 dB from 0.5 MHz to 20 MHz is attained.

A high low-frequency noise contribution comes from the direct coupling of the LNTA flicker noise to the baseband due to the low impedance path through the AI circuit at low frequencies. The receiver exhibits a conversion gain of 39.5 dB over a wide IF 3dB-bandwidth of 40 MHz. Although the conversion gain drops at high IF, the NF remains below 5 dB at up to 100 MHz.

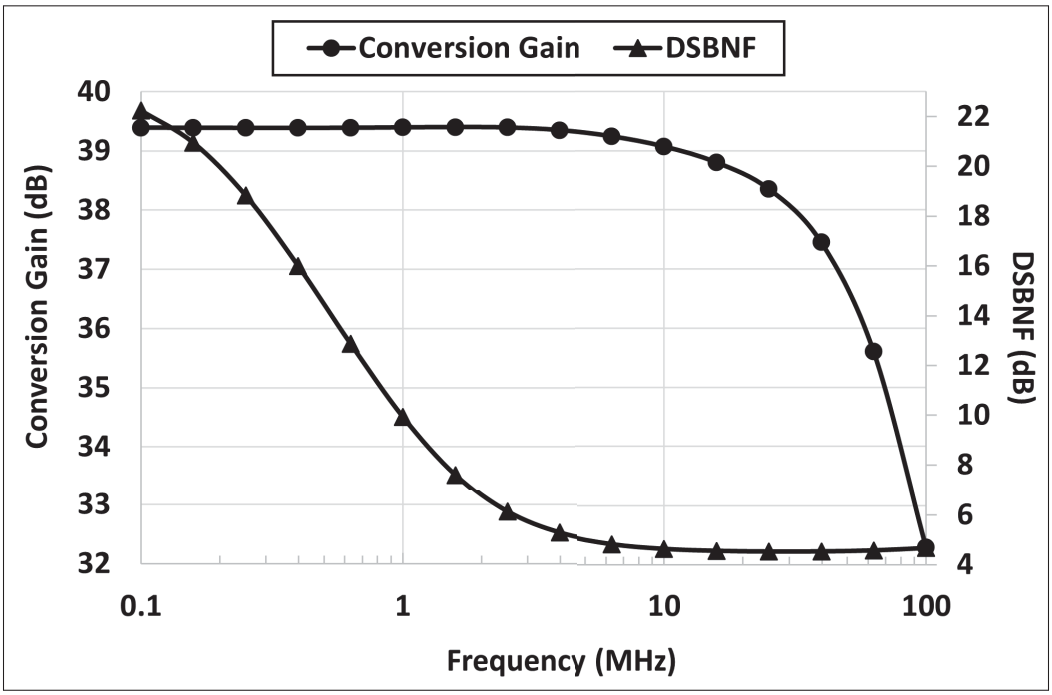

Figure 2.14 The post-layout simulated NF versus the IF.

The linearity performance is verified by applying two tones of 2.41 GHz and 2.411 GHz at the input. This is performed while the LO frequency remains at 2.4 GHz. This generates fundamental tones of 10 MHz and 11 MHz and third-order intermodulation products of 9 MHz and 12 MHz at the output. The output power of the fundamental tone and third-order intermodulation products versus the input power are shown in Figure 2.15. An IIP3 of -28 dBm is achieved.

The receiver performance is verified with an RF input signal varying from 0.75 GHz to 3.4 GHz while the IF remains constant at 10 MHz, as shown in Figure 2.16. The front-end exhibits an S_{11} of less than -10 dB over the entire RF range of interest. As the RF increases, the conversion gain reduces from 44.7 dB to 36 dB, and the DSB NF increases from 4.1 dB to 7.9 dB. On the

other hand, the IIP3 result improves from −34.5 dBm to −25 dBm due to the conversion gain reduction.

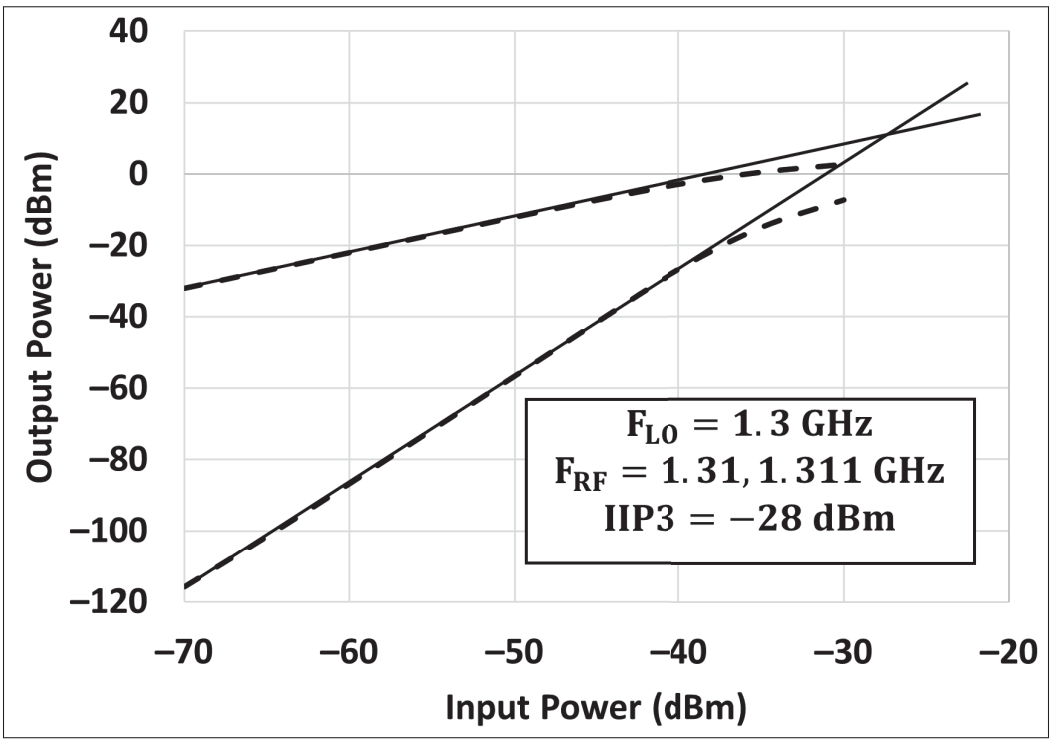

Figure 2.15 The post-layout simulated fundamental and third-order intermodulation products versus the input power.

The design's capabilities and its overall performance are compared to prior works using the following figure of merit (FoM) used in Bozorg & Staszewski (2020) and given by

$$FoM = \frac{Gain[abs] \times (F_H - F_L)(GHz) \times IIP3[mW]}{(F-1) \times F_L(GHz) \times P_{dc}[mW]}, \tag{2.6}$$

where F_H and F_L are the highest and lowest RF operating frequencies, respectively, F is the noise factor, IIP3 is the in-band IIP3 performance in mW, and P_{dc} is the power consumption. The results are shown in Figure 2.17, where the FoM for the proposed design and other references is plotted versus the power consumption. The FoM compares well considering the power consumption.

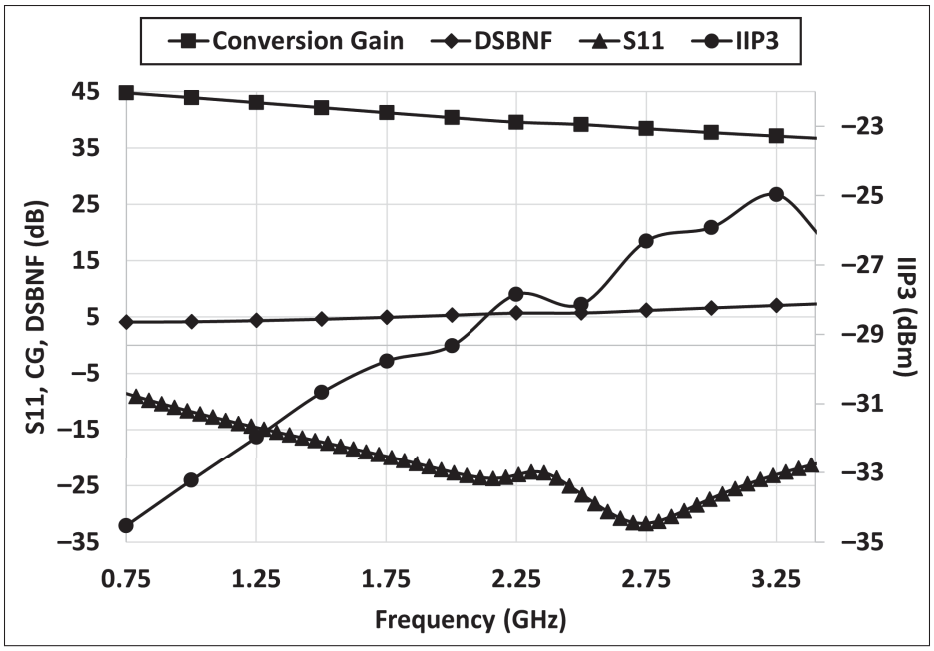

Figure 2.16 Receiver post-layout simulated performance versus the RF signal.

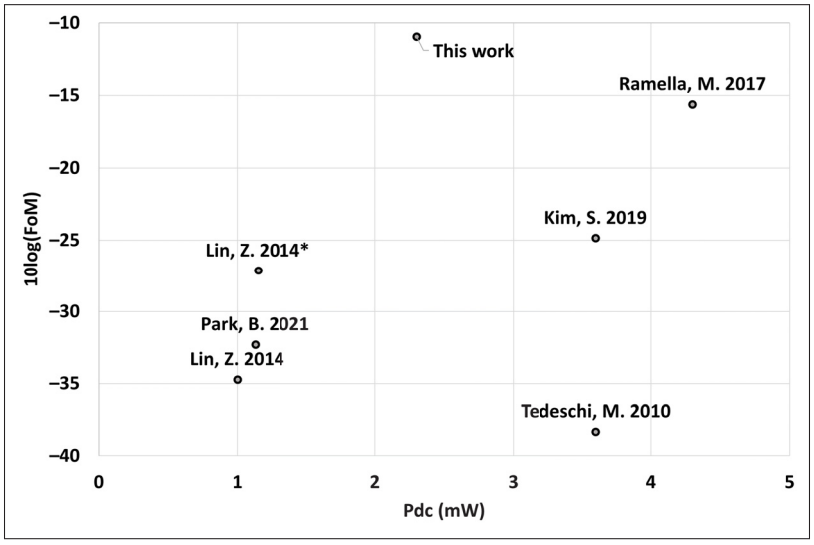

Figure 2.17 Comparison of the FoM to prior works versus the power consumption. Tedeschi, M. 2010 (Tedeschi *et al.* (2010)). Lin, Z. 2014 (Lin *et al.* (2014b)). Lin, Z. 2014* (Lin *et al.* (2014c)). Kim, S. 2019 (Kim & Kwon (2019)). Ramella, M. 2017 (Ramella *et al.* (2017)). Park, B. 2021 (Park & Kwon (2021)).

Table 2.1 compares and summarizes the performance of the proposed receiver simulated here from the circuit proposed in Abbasi *et al.* (2020b) with the latest literature. This work compares well in terms of bandwidth and NF considering its technology node and power consumption.

Table 2.1 Performance Summary and Comparison.

Parameters	**This Work ****	**JSSC 2010 [1]**	**JSSC 2014 [2]**	**JSSC 2014 [3]**	**MWCL 2019 [4]**	**JSSC 2017 [5]**	**IEEE 2021 [6]**
Application	IoT	ZigBee	ZigBee	ZigBee	IoT	Bluetooth	BLE
Process node	130 nm CMOS	90 nm CMOS	65 nm CMOS	65 nm CMOS	65 nm CMOS	28 nm CMOS	65 nm CMOS
Freq. (GHz)	0.8–3.4	2.4	2.4	0.433–0.96	0.91	2.4	2.4–2.48
S11 (dB)	<−10	<−10	<−10	<−10	<−10	<−10	<−10
Gain (dB)	39.5	75	57	50	40.7	43.4	42
NF (dB)	5.6	9	8.5	8.1	1.94	7.8	13.2
IIP3 (dBm)	−28 *	−12.5 †	−6 †	−20.5 †	−25.6 *	−20 *	−25 *
P_{DC}@V_{DD} (mW)	2.3@1.2	3.6@1.2	1@1.2	1.15@0.5	3.6@1.8	4.3@1.8	1.13@0.8
Active Area (mm^2)	0.025	0.35	0.3	0.2	0.559	0.4	0.85
FoM	−11	−38.3	−34.7	−27.1	−24.8	−15.6	−32.3

* In-band IIP3; † Out-of-band IIP3; ** Post-layout simulation.

References:[1]Tedeschi *et al.* (2010), [2]Lin *et al.* (2014b), [3]Lin *et al.* (2014c), [4]Kim & Kwon (2019), [5]Ramella *et al.* (2017), [6]Park & Kwon (2021)

2.6 Conclusions

This work provided a design tutorial for the low-power and wideband RF-to-baseband CRR that was proposed in Abbasi *et al.* (2020b). It discussed topology selection, design considerations

and layout aspects for the LNTA, down-conversion mixer, AI circuit and TIA. The receiver is able to perform over the wide frequency band from 0.8 GHz to 3.4 GHz.

The proposed receiver in Abbasi *et al.* (2020b) was divided into four individual sub-circuits—LNTA, mixer, AI circuit and TIA—to be designed individually before integration. The design of each circuit was detailed through equations and simulations. Two well-known LNTA topologies, the CG and CS, were studied to make sure that the best topology was selected to provide wideband performance. The AI circuit in Abbasi *et al.* (2020b) enhances the RF performance and addresses the issues raised in the literature. The TIA design used a single transistor, and design constraints and metrics were studied. Then, the test bench models to design and simulate each sub-circuit were also included. Finally, post-layout simulation results after the integration were presented, outlining the potential of the receiver and the viable design procedure described in this paper.

Author Contributions

Conceptualization, A.A. and F.N.; methodology, A.A.; software, A.A.; validation, A.A.; formal analysis, A.A.; investigation, A.A.; resources, A.A.; data curation, A.A.; writing—original draft preparation, A.A.; writing—review and editing, A.A. and F.N.; visualization, A.A.; supervision, A.A. and F.N.; project administration, A.A.; funding acquisition, F.N. All authors have read and agreed to the published version of the manuscript.

Acknowledgments

The author would like to thank CMC Microsystems for chip fabrication and for providing the EDA tool.

CHAPTER 3

A WIDEBAND LOW-POWER RF-TO-BB CURRENT-REUSE RECEIVER USING AN ACTIVE INDUCTOR AND $1/f$ NOISE-CANCELLATION FOR L-BAND APPLICATIONS

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Article published in *IEEEAccess*, September 2022.
https://doi.org/10.1109/ACCESS.2022.3205110

Abstract: A low-power and wideband RF-to-baseband (BB) current-reuse receiver (CRR) front-end utilizing both a $1/f$ noise cancellation (NC) technique and an active inductor (AI) is proposed tuned to operate from 1 GHz to 1.7 GHz for L-Band applications, including those that require high modulation bandwidths. The CRR front-end employs a single supply and shares the bias current of the low noise transconductance amplifier (LNTA) with the BB circuits to reduce the power consumption. To minimize the losses of the radio frequency (RF) signal right before down-conversion, a high impedance AI circuit isolates the mixer input from the CRR output node. The $1/f$ NC circuit suppresses the low frequency noise of the LNTA that leaks to the output. A common-gate LNTA with g_m-boosting, along with a single-to-differential LC-balun are used to enhance the input matching, conversion gain and noise figure (NF). The proposed receiver is fabricated in a TSMC 130 nm CMOS process and occupies an active area of 0.54mm^2. The input matching (S_{11}) is below -10 dB from 1 GHz to 1.7 GHz. At a local-oscilator (LO) frequency of 1.3 GHz, intermediate-frequency (IF) of 10 MHz and default current settings, the CRR achieves a conversion gain of 41.5 dB, a double-sideband (DSB) NF of 6.5 dB, and an IIP3 of -28.2 dBm while consuming 1.66 mA from a 1.2 V supply.

Keywords: current-reuse receiver (CRR), cross-coupled common-gate low noise transconductance amplifier (LNTA), wideband, low-power, wide modulation bandwidth, L-Band.

3.1 Introduction

The internet of things (IoT) aims to connect trillions of devices for various applications. Today, both academia and industry are investigating how to employ the IoT to manage, locate, monitor, identify and track within different sectors such as automotive, agriculture, manufacturing, education, smart buildings, military and others. IoT applications operate in different frequency bands. One of the important bands is the L-Band that includes several applications and wireless standards such as various global navigation satellite systems (GNSS), cellular communication, aircraft surveillance, digital video/audio broadcasting, etc. Marks, Lavender, Wongsaroj & Hogg (2015); Abularach *et al.* (2015); Beresik, Sotak, Nebus & Puttera (2011); Zhang, Liu & Jiang (2012); Penttinen (2015); Chen *et al.* (2012); Li *et al.* (2014). For instance, among the various features of the IoT, location tracking is important, and can be used in different applications such as vehicles for navigation, health for patient tracking, military for soldier localization, shipping to track goods, etc Zhang *et al.* (2012).

As the L-Band includes several wireless standards and applications within the $1-2$ GHz band, a wideband RF front-end that covers a wide frequency range is suitable as it mitigates the need of multiple RF front-ends. In addition, a wide modulation bandwidth is required in the front-end to not limit the receiver bandwidth to address the requirements of different wireless standards.

However, while wideband RF front-ends are attractive, as they provide system agility and compactness, reducing the power consumption of the RF front-end while maintaining performance metrics such as linearity and noise figure (NF) is a challenge. Various methods and techniques have been studied to address this challenge. Among them, a widespread method to reduce power consumption is current-reuse. Usually, current-reuse has been employed within individual blocks such as the low noise transconductance amplifier (LNTA) Shams *et al.* (2020). In Thijssen *et al.* (2020), a current-reuse power-optimized LNTA was used in a conventional cascaded receiver architecture. It reports good 1-dB compression out-of-band linearity, but a poor in-band 1-dB compression of -56 dBm is achieved at a maximum gain setting of 61 dB. Another approach Purushothaman, Klumperink, Plompen & Nauta (2021) employed a current-reuse baseband

amplifier in a mixer-first receiver architecture. It achieves very good performance consuming a low-power of 0.38 mW. However, the receiver architecture is not suitable for wideband modulations as it reports a very low baseband bandwidth of 2 MHz that is not suitable for wider modulation bandwidth applications. In Park & Kwon (2020), a quadrature low noise amplifier (LNA) and active-type poly-phase filter (PPF) were used to reduce power consumption. However, the receiver has a narrow RF bandwidth due to the common-source LNA topology, and high NF because of the quadrature technique used in the LNA. In Silva-Pereira, de Sousa, Freire & Vaz (2018), alternatively, an inverter-based LNA with an LC-balun and passive PPF are used to generate the quadrature signal before the down conversion. This reduces the LO dynamic power for Bluetooth low-energy (BLE), but using an LC-balun and passive PPF is not suitable for wideband applications. In addition, a phase-locked loop (PLL) free receiver architecture is proposed in Wang, Qiu, Koo, Ruby & Otis (2018) at the cost of a high NF. Recently, current sharing of RF and BB blocks using a single supply voltage has been actively studied. Conventionally, receiver front-ends cascade circuits to receive and amplify a weak RF signal with a LNTA, down-convert it to BB through a mixer and finally convert the current signal to a voltage signal using a transimpedance amplifier (TIA), as shown in Figure 3.1. On the other hand, by scaling down the CMOS technology node where the voltage threshold is reduced and transition frequency (f_T) is increased, stacked architectures that reduce power consumption by sharing the current of the RF circuits with the BB circuits are now possible.

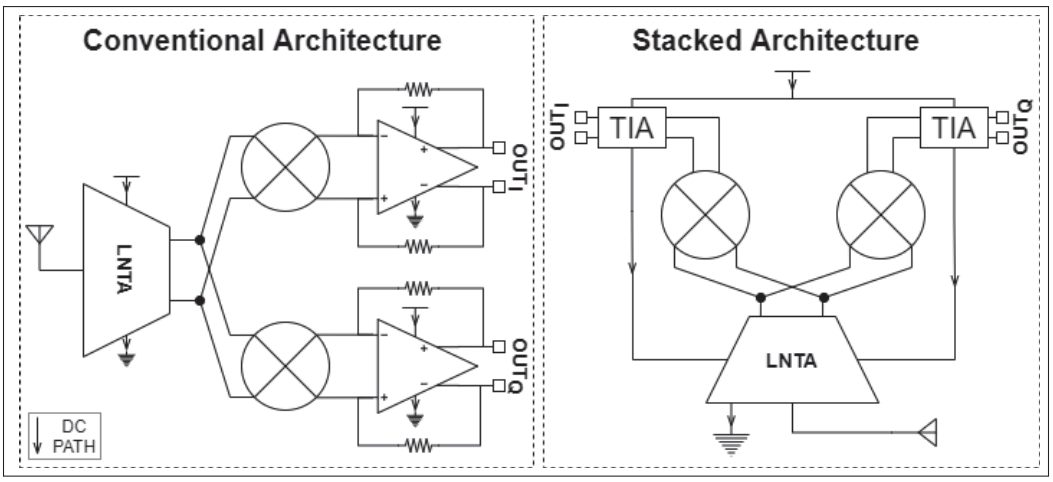

Figure 3.1 Conventional and stacked receiver front-end architectures.

Although the stacked architecture reduces power consumption significantly, it has shortcomings. In Tedeschi *et al.* (2010), LNTA, mixer and voltage-controlled oscillator (VCO) blocks are stacked to share a single supply, reducing the power consumption. However, the front-end suffers from VCO injection locking and a high NF of 9 dB. In addition, the common-source LNTA used limits the RF bandwidth, which is not suitable to cover wide RF bandwidth with a single receiver module. Another approach with cascoded LNTA, active mixer and BB filter was proposed in Lin *et al.* (2014b). It still suffers from high NF. Moreover, the use of an active mixer reduces the linearity and increases voltage headroom requirements. A function-reuse RF front-end is an interesting method which employs a push-pull amplifier to function as both LNTA and TIA. However, it reported poor P_{1dB} of -50 dBm due to the low supply voltage Lin *et al.* (2014c). This approach is only suitable for sub-GHz applications. A current-reuse architecture using an N-path passive mixer for input matching is another sub-GHz alternative which reports good NF performance Lin *et al.* (2014a). However, one of its bottlenecks is the use of an active mixer for down-conversion that requires a higher supply voltage. It also suffers LO to RF leakage due to the N-path passive mixer used for input matching. Moreover, it requires additional circuits to combine the N paths at the output which increases the overall power consumption. In Ghosh & Gharpurey (2011), a $1/f$ noise-cancellation (NC) technique and linearity enhancement method is used, but its power consumption is high at 8 mW. A current-reuse receiver (CRR) proposed in Kim & Kwon (2019) employed input matching and a $1/f$ noise reduction technique that results in a low NF of 1.94 dB at the cost of limited RF bandwidth. Moreover, both Kim & Kwon (2019) and Abbasi *et al.* (2020a) suffer from losses of the RF signal due to the sharing of the BB output and passive mixer input. To overcome this issue, our earlier work in Abbasi *et al.* (2020b), applied the concept of an active inductor (AI) from Ramella *et al.* (2017); Razavi (2020) to isolate the mixer input from the BB output, thus reducing the losses of the RF signal before the down conversion. This allows the receiver to maintain its performance at higher frequencies even in a relatively large 130 nm CMOS process. However, it still suffers from a high NF at low IF due to the direct injection of the low frequency noise of the LNTA into the BB.

This work is the continuation and extension of our earlier published conference paper in Abbasi *et al.* (2020b) that presented simulation results. Notably, this work improves the circuit architecture of our prior work with a 1/f noise cancellation technique and an integrated on-chip input inductor. In Abbasi *et al.* (2020b), a high quality off-chip input inductor model was used in simulation, while in this work, this inductor is integrated on-chip. Importantly, measurement results are now presented, thus experimentally validating our prior work, along with the aforementioned improvements.

Accordingly, this work proposes a quadrature (I/Q) low-power and wideband RF-to-BB CRR front-end uniquely employing both an AI and $1/f$ NC technique in order to overcome the aforementioned issues. It utilizes a wideband LNTA stage to convert the RF voltage to an RF current, a current driven passive mixer to down-convert the RF signal to an IF signal, and a TIA to convert the IF current to an IF voltage using a single transistor. The proposed CRR front-end achieves good NF and linearity performance along with low power consumption. The paper is structured as follows. Section 3.2 provides a receiver architecture overview, Section 3.3 details the different circuits required in the design, and Section 3.4 presents the measurement results and discusses them.

3.2 Receiver Overview

Through the scaling down of CMOS technology nodes, the implementation of high frequency circuits is readily possible with reduced trade-offs thanks to the reduced parasitic. However, the fabrication cost increases sharply for smaller technology nodes. Thus, in order to implement such circuits in cost efficient CMOS such as 130 nm CMOS technology, design techniques are required to maintain the performance of the design. For instance, in Kim & Kwon (2019), while a very low NF is reported, the RF bandwidth is limited. This is due to the fact that the input of the down-conversion mixer is shared with the receiver output node causing loading from the following stage and output circuit. Ultimately, this degrades the performance of the receiver at higher frequencies and limits it to sub-GHz applications. To mitigate this issue, this work

uniquely applies both an AI and $1/f$ NC technique from Abbasi *et al.* (2020b); Ramella *et al.* (2017); Razavi (2020) to the CRR front-end.

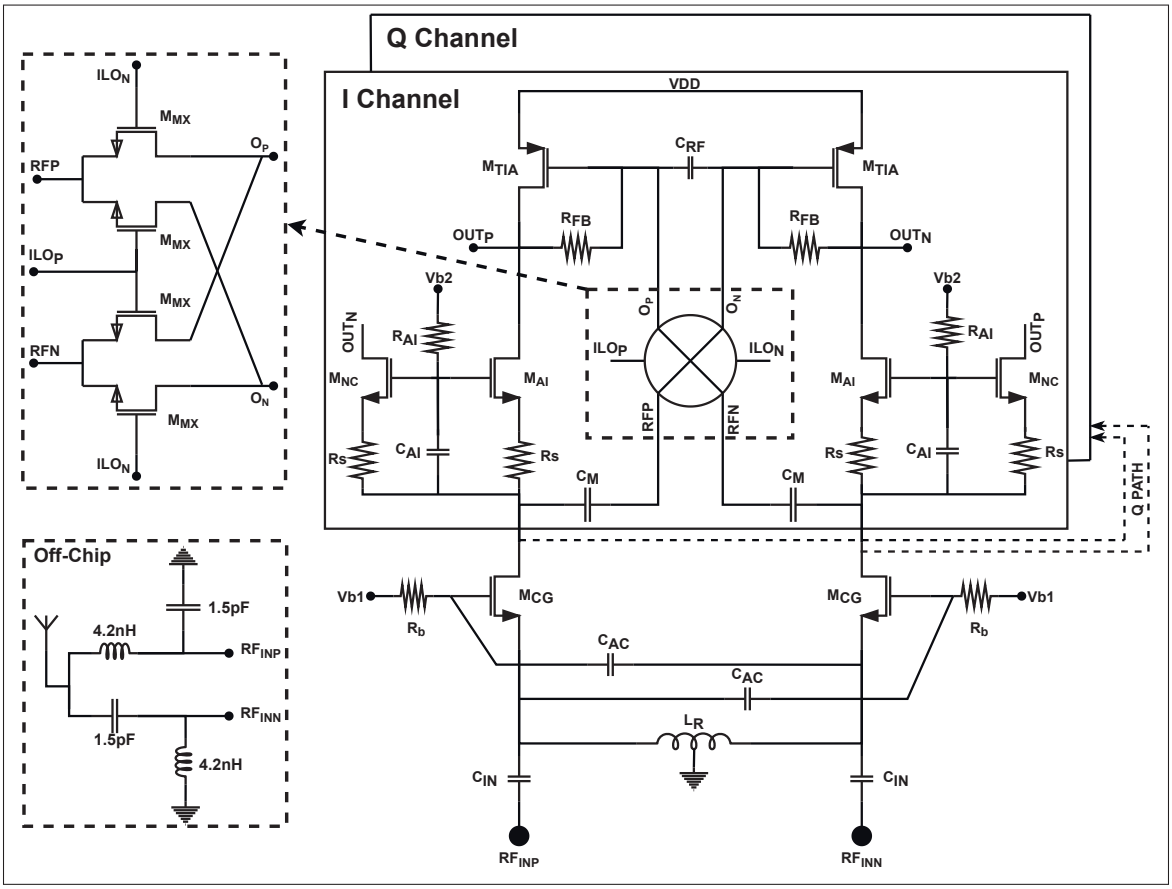

Figure 3.2 Block diagram of the proposed CRR front-end.

The block diagram of the proposed CRR front-end is shown in Fig 3.2. It includes an LNTA to convert the RF voltage to a current. Transistors M_{CG}, inductor L_R and cross-coupled capacitors C_{AC} form the LNTA circuit. The LNTA sets the receiver sensitivity, linearity and input impedance matching. Thus, it is designed to attain the required performance metrics, and it defines the overall current consumption. The CRR employs a passive mixer shown on the top left of the figure, and includes transistors M_{MX} that do not consume DC current. As previously mentioned, the CRR uses both an AI and $1/f$ NC circuit in order to improve the receiver sensitivity. These are implemented by M_{AI}, R_{AI}, C_{AI}, M_{NC} and R_S. The single supply current

divides equally between the TIA blocks, each formed by a single transistor, M_{TIA}, and feedback resistor, R_{FB}. The TIA feeds the LNTA and AI current. Moreover, the receiver employs a quadrature (I/Q) architecture using a 25% LO duty-cycle and single LNTA. In this way, the power consumption is significantly reduced by the reuse of the supply current. Details pertaining to each circuit composing the CRR front-end are discussed in the next section.

3.3 Circuit Design

3.3.1 LNTA with LC-Balun Matching Network

The LNTA plays an important role for input matching and receiver sensitivity. Two well-known typologies can be used to provide input matching: the common-source and the common-gate. In Kim & Kwon (2019), the common-source topology along with a $1/f$ NC technique is employed. Although the noise performance is very good, it has a narrow-band response, and is sensitive to package parasitics and non-idealities related to the printed circuit board (PCB). In this work, a common-gate topology is used instead, and provides wideband input matching at the cost of a higher NF. In Figure 3.2, M_{CG} forms the common-gate topology which is differentially applied in this design. The gate terminal of M_{CG} connects to a bias voltage, V_{b1}. Center tap inductor L_R provides the DC current path to the ground and resonates with parasitic capacitors at the input to reduce input losses. C_{IN} is an AC-coupling capacitor. To reduce the power consumption and NF of the LNTA, cross-coupled capacitors C_{AC} are used to boost the transconductance of M_{CG} by approximately a factor of two, yielding an effective transconductance of $g_{meff} = 2 \times g_m$. This assumes that the short channel effect is negligible for the input transistors. Moreover, this increased transconductance helps achieve the required input impedance, $1/g_{meff}$, and a better NF with less current. The noise factor of the LNTA is calculated by using the following:

$$F \cong 1 + \frac{\gamma}{4\alpha} \cdot \frac{1}{R_S g_m} + \frac{R_{Balun}}{R_S}, \tag{3.1}$$

where α and γ are the bias-dependent noise parameters and R_S is the source resistance. The balun losses can be modeled by series resistor R_{Balun}. γ/α is reduced by increasing the channel-length slightly while maintaining the transition frequency, f_T, at least ten times higher than the frequency of operation.

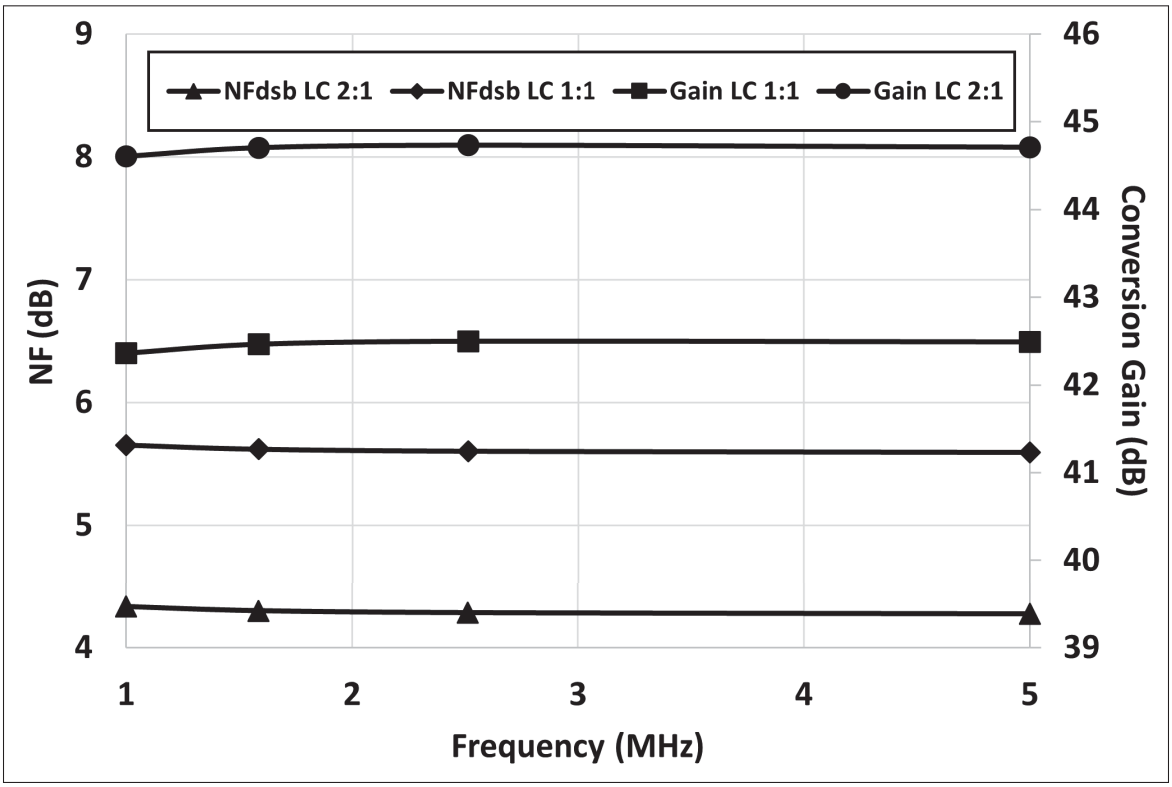

Figure 3.3 Simulated conversion-gain and DSB NF of the CRR using a 1:1 LC-balun or a 2:1 LC-balun.

Earlier works used a 1:1 balun to convert the single ended signal to a differential one Ramella *et al.* (2017); Park & Kwon (2021); Jeong, Sun, Han & Lee (2014). To perform input matching, the LNTA input impedance should be designed to $R_S = 1/2g_m$. This degrades the NF by increasing the second term in equation (3.1) by two times. The noise factor is then given by

$$F \cong 1 + \frac{\gamma}{2\alpha} + \frac{R_{Balun}}{R_S}. \tag{3.2}$$

In this work, a 2:1 LC-balun, shown at the bottom left of Figure 3.2, is used to convert the single ended input signal to a differential one at the input of the LNTA. It can convert the 50 Ω antenna impedance to any impedance required (in this work 25 Ω) on the differential side by choosing proper inductor and capacitor values. This gives the advantage to design the LNTA with higher $g_{m,eff}$ (in this work $2\times g_{m,eff}$) to achieve lower NF while maintaining the input matching performance. In this way, the LNTA noise is given by

$$F \cong 1 + \frac{\gamma}{4\alpha} + \frac{R_{Balun}}{R_S}. \tag{3.3}$$

In this fashion, the good input matching is maintained and the second term in (3.3) is halved in comparison to (3.2) that involves a 1:1 balun. An W/L of $50\mu/140n$ is chosen for M_{CG} to achieve the best NF and g_m/g_{ds} performance, where g_{ds} is the admittance of M_{CG}.

To outline the benefit of the matching technique proposed, the simulated NF and conversion-gain of the CRR is compared using a 1:1 or a 2:1 LC-balun employing $g_{m,eff}$ and almost $2 \times g_{m,eff}$, respectively. The results are shown in Figure 3.3, outlining that the conversion-gain is improved by about 2.5 dB and the NF is reduced by more than 1 dB.

The LNTA and LC-Balun were tuned to the L-band in this work, but this tuning could have been applied to other bands such as the 2.4 GHz ISM band (e.g., Bluetooth Low Energy) or the 900 MHz ISM band (e.g., Zigbee).

3.3.2 Active Inductor and $1/f$ Noise-Cancellation Technique

Conventionally, a cascode circuit is used to boost the output impedance and enhance isolation. Figure 3.4(a) shows the conventional CRR using a cascode circuit after the LNTA. The input of the down-conversion mixer and receiver output share the same node, causing RF signal attenuation from both parasitic capacitors and the large loading of the next stage at the output. This limits the operating frequency of the circuit. Moreover, it renders the architecture impractical for modern applications if designed in a large technology node such as 130 nm CMOS. To

overcome this issue, this work proposes an AI in Figure 3.4(b) using M_{AI}, C_{AI} and R_{AI}. The impedance looking into the AI circuit, Z_{AI}, is low at DC but keeps increasing with frequency Razavi (2020). In this way, the AI circuit isolates the mixer input from the output node at higher frequencies, while the DC current passes through the AI circuit. To boost the impedance further, R_S is added to the source of M_{AI}. The impedance looking into the AI circuit, Z_{AI}, by ignoring M_{NC} since it is in parallel is given by

$$Z_{AI}(s) \cong \frac{g_{m,AI}R_S(R_{AI}C_{AI}s+1)+R_{AI}C_{AI}s}{g_{m,AI}R_SC_{AI}s+g_{m,AI}+C_{AI}s} \,||\, \frac{1}{sC_{par}}, \tag{3.4}$$

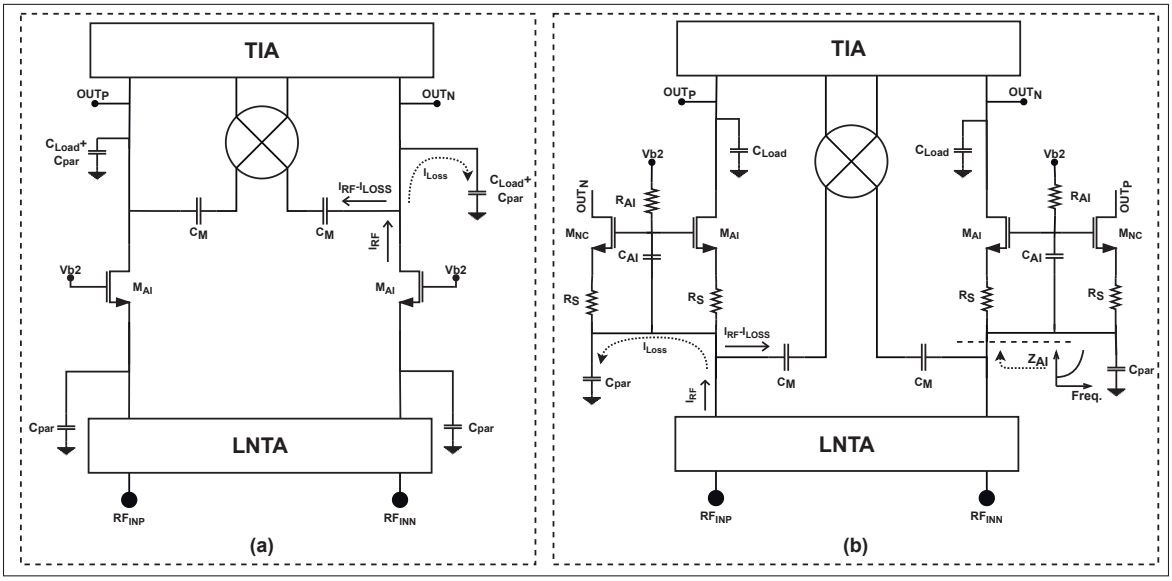

Figure 3.4 (a) Convectional CRR with cascoded transistor. (b) Proposed architecture introducing an AI and $1/f$ NC technique.

where C_{par} is the parasitic capacitance at the mixer input. The C_{par} depends on the technology node. Figure 3.5 shows the mathematical model of the magnitude of Z_{AI} versus the frequency using (3.4) for different parasitic capacitance values and compares it with simulation results. To model this, a $g_{m,AI}$ of 3.5 mS, C_{AI} of 1 pF, R_{AI} of 50 kΩ and R_S of 200 Ω are used. Two scenarios are considered for C_{par}. Firstly, C_{par} is ignored, showing that Z_{AI} increases linearly with frequency. Then, C_{par} values of 30 fF are considered to compare with the simulation results.

This shows that as a result of increasing the parasitic capacitor at the input of the AI circuit, Z_{AI} reduces faster at higher frequencies and limits the operating frequency of the AI.

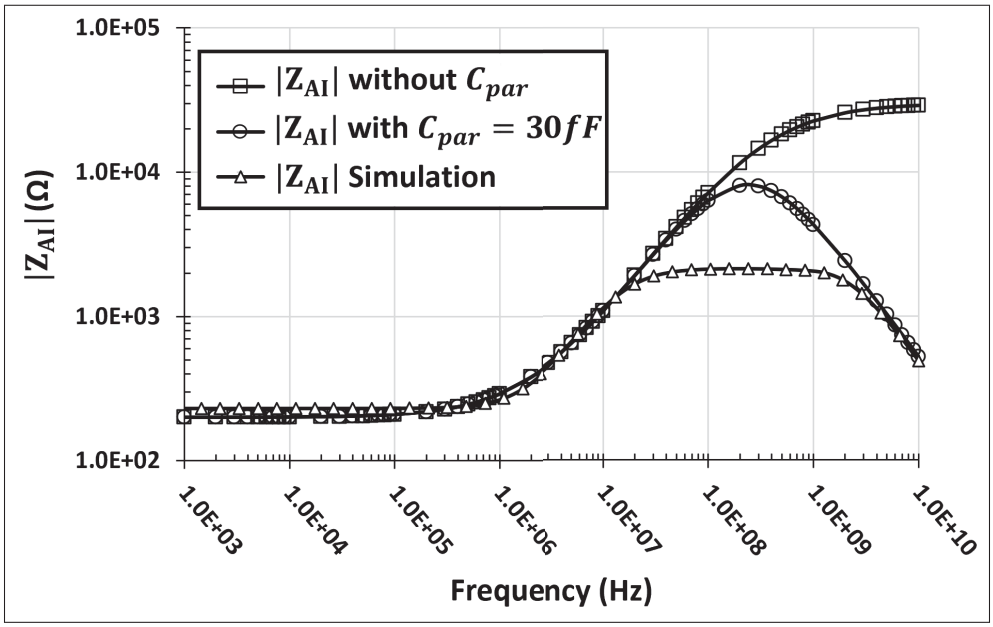

Figure 3.5 Mathematical model, with and without C_{par}, and simulation of the magnitude of Z_{AI} versus frequency.

The AI circuit injects noise into the LNTA output at RF as well as at low frequencies at BB. The noise factor considering the AI circuit is then given by

$$F \cong 1 + \frac{\gamma}{4\alpha} + \frac{R_{Balun}}{R_S} + 4R_S\left(\gamma g_{m,AI} + \frac{1}{R_{AI}}\right)\left(1 + \frac{R_{Balun}}{2R_S}\right) + K_1\frac{V_{fk\_LNA}^2}{4kTR_S} + K_2\frac{V_{fk\_AI}^2}{4kTR_S}. \quad (3.5)$$

Another problem of the conventional CRR shown in Figure 3.4(a) is the direct coupling of the LNTA $1/f$ noise to the output. This also can affect the structure with the AI since the AI circuit is not blocking the low frequency components. To overcome this issue, M_{NC}, added in Figure 3.4(b), creates a low frequency path to the output with the opposite polarity. This makes the $1/f$ noise common-mode for the next stage such that it can be rejected with a differential

architecture ($K_1 \sim 0$). The $1/f$ noise of the AI circuit is still contributing to the output. The source-degeneration resistor, R_s, helps reduce the $1/f$ noise of M_{NC} and M_{AI} as well as boost Z_{AI}. In (3.5), $g_{m,AI}$ is replaced with $g_{m,AI}/(1 + g_{m,AI}R_s)$ where R_s is a degeneration resistor and $K_2 << 1$. The simulation results of the CRR front-end with the NC circuit activated or deactivated is shown in Figure 3.6. As can be seen, while the thermal noise remains the same, the $1/f$ noise is suppressed by the NC circuit. This allows the CRR front-end to operate at low IF in a direct-conversion architecture.

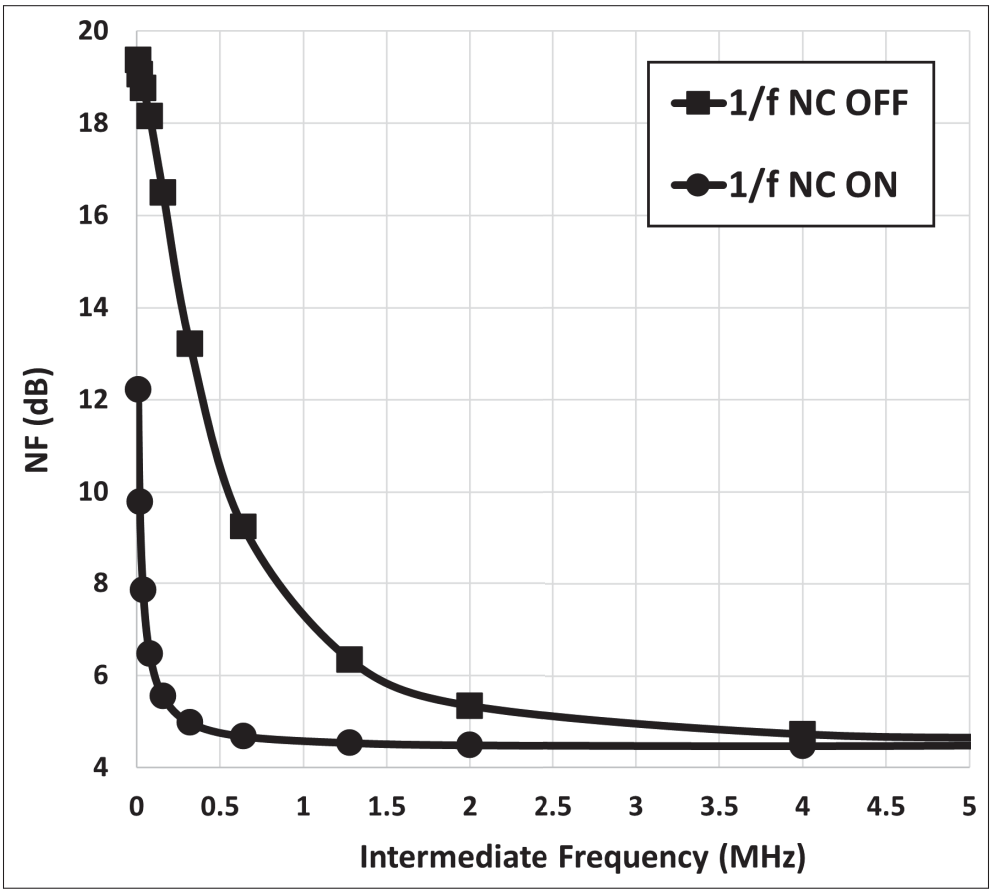

Figure 3.6 The simulated NF with the NC circuit activated or deactivated.

The straightforward way to design the NC circuit is to half the W/L ratio of M_{AI} and double the value of R_S in the AI circuit. Then, the same device values can be used in the NC circuit Ramella *et al.* (2017).

3.3.3 Passive Down-conversion Mixer

A conventional current driven double-balanced passive mixer is employed to convert the RF current to the BB current, as shown in Figure 3.2. It operates with a 25% duty cycle LO signal to enhance both NF and conversion gain Razavi (2013). The clock generation circuit is shown in Figure 3.7 Shams & Nabki (2022). The AC-coupling capacitors, C_M, separate the DC biasing of the mixer. Moreover, this blocks the low frequency noise of the LNTA. The source and drain biasing of the mixer switches is provided by the TIA to be half of the supply (600 mV). The gate bias voltage of the mixer switches is chosen to ensure that the LO signals are able to toggle the switches properly, while maintaining the V_{GS} and V_{GD} values in the safe operating region to avoid breakdown.

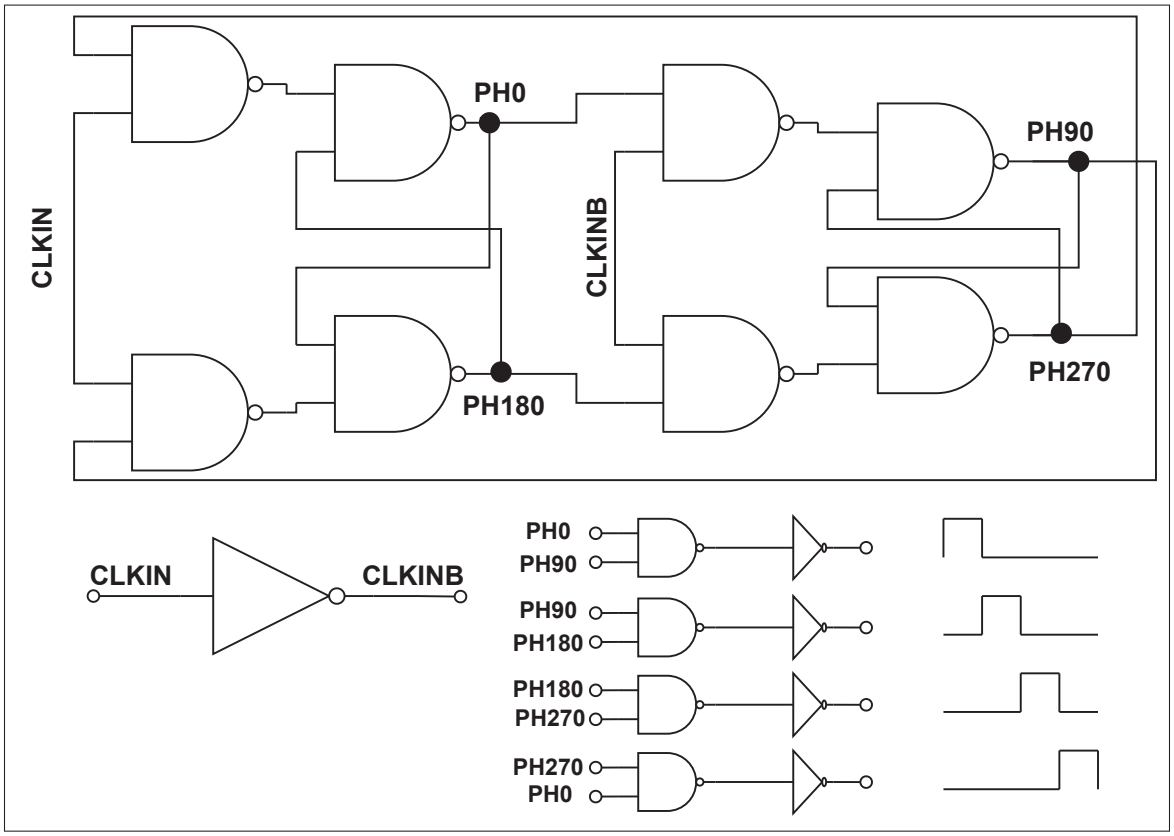

Figure 3.7 Schematic of the clock generation circuit generating 25% duty cycle phases.

3.3.4 Transimpedance Amplifier

The BB current generated by the down-conversion mixer is converted to a BB voltage using a TIA at the output node. The TIA circuit is formed by M_{TIA} and feedback resistors, R_{FB}. M_{TIA} needs to provide sufficient g_m to maintain the impedance low enough at the output of the mixer in order to keep the voltage swing at that node small, and thus avoid a degradation of the linearity. To enhance the output impedance and reduce the short-channel effect, a large channel length of 500 nm is used for M_{TIA}.

Overall, the conversion gain of the proposed receiver is approximately calculated as

$$Gain_{CRR} \cong \frac{2\sqrt{2}}{\pi} g_{m,eff} R_{FB} \tag{3.6}$$

3.3.5 Output Buffer

An output buffer is required to allow for measurement of the CRR using off-chip laboratory equipment such as a spectrum analyzer, high-speed oscilloscope or any similar instrument with a 50 Ω input impedance. This output buffer ensures that the output impedance of the CRR is well matched to the impedance of the testing equipment. For this purpose, a fully differential current-mode logic (CML) circuit is used and shown in Figure 3.8. The gain of the CML circuit is designed to be of 0 dB and is given by

$$Gain_{CML} = g_{m1} \cdot R_L, \tag{3.7}$$

where R_L is the output load. This load is chosen to be 50 Ω in order to avoid a very high value for $g_{m,M1}$ that would results in high current and large W/L ratio, reducing the bandwidth of the buffer. A 2:1 balun can be used off-chip at the output to convert the 100 Ω differential output to a single ended 50 Ω output. Cascode transistors, M_2, are used to enhance the bandwidth of the

CML circuit. The input of the CML circuit is AC-coupled to separate its biasing voltage with that of the CRR front-end. The cascode transistors are directly biased with the supply voltage.

Both the CML and CRR front-end each utilize a 1.2 V supply. The CML circuit consumes a high current of 40 mA to maintain high linearity and low NF performance for testing proposes.

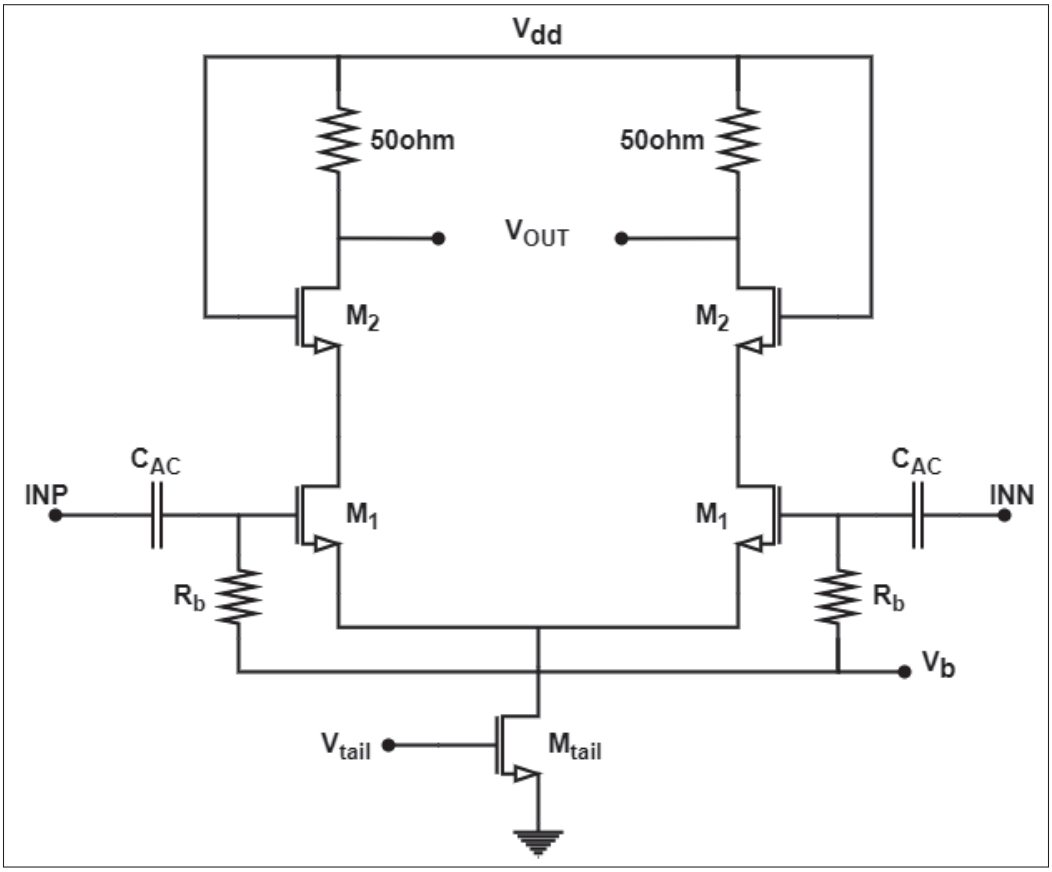

Figure 3.8 Output buffer circuit used in the measurements.

3.4 Experimental Results and Discussion

The low-power and wideband RF-to-BB current-reuse receiver front-end was fabricated in TSMC 130 nm CMOS technology. Both CRR front-end and CML output buffer were implemented on-chip and the die micrograph is shown in Figure 3.9. The design was fabricated under two conditions, one is covered with metal fill at sensitive nodes (Chip1), shown in Figure 3.9(a), and

another reduced the metal fill on sensitive RF nodes and blocks (Chip2), shown in Figure 3.9(b). Metal fill reduction was done manually through an iterative process to make sure the metal fill is optimized on the sensitive paths. The CRR front-end occupies an active area of 0.54mm^2, excluding the output buffer and bond pads. It consumes 1.66 mA from the 1.2 V supply. Both chips were measured under the same biasing conditions, PCB and test setup.

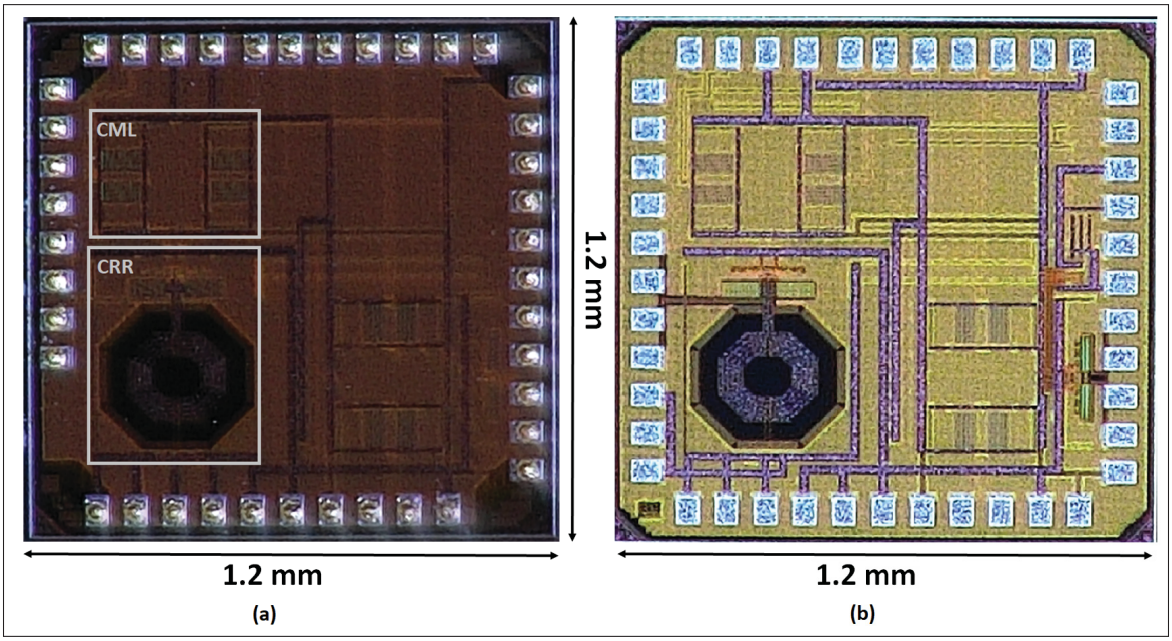

Figure 3.9 Die micrograph of the fabricated die (a) fully covered with metal fill (Chip1), and (b) with reduced metal fill on the sensitive nodes (Chip2). Note that the circuitry on the right half of the dies is not related to this work.

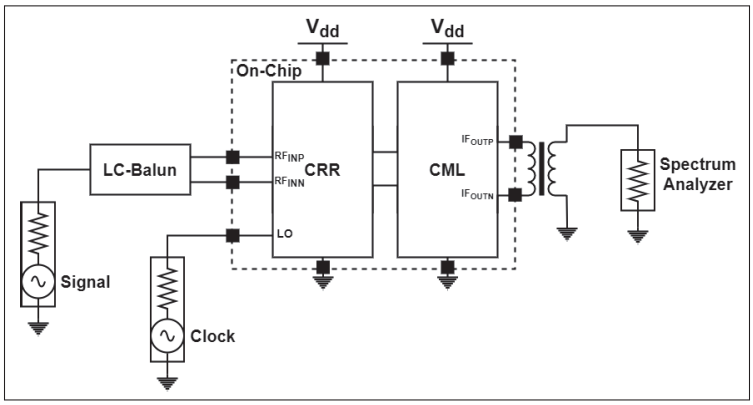

Figure 3.10 Diagram of the measurement setup.

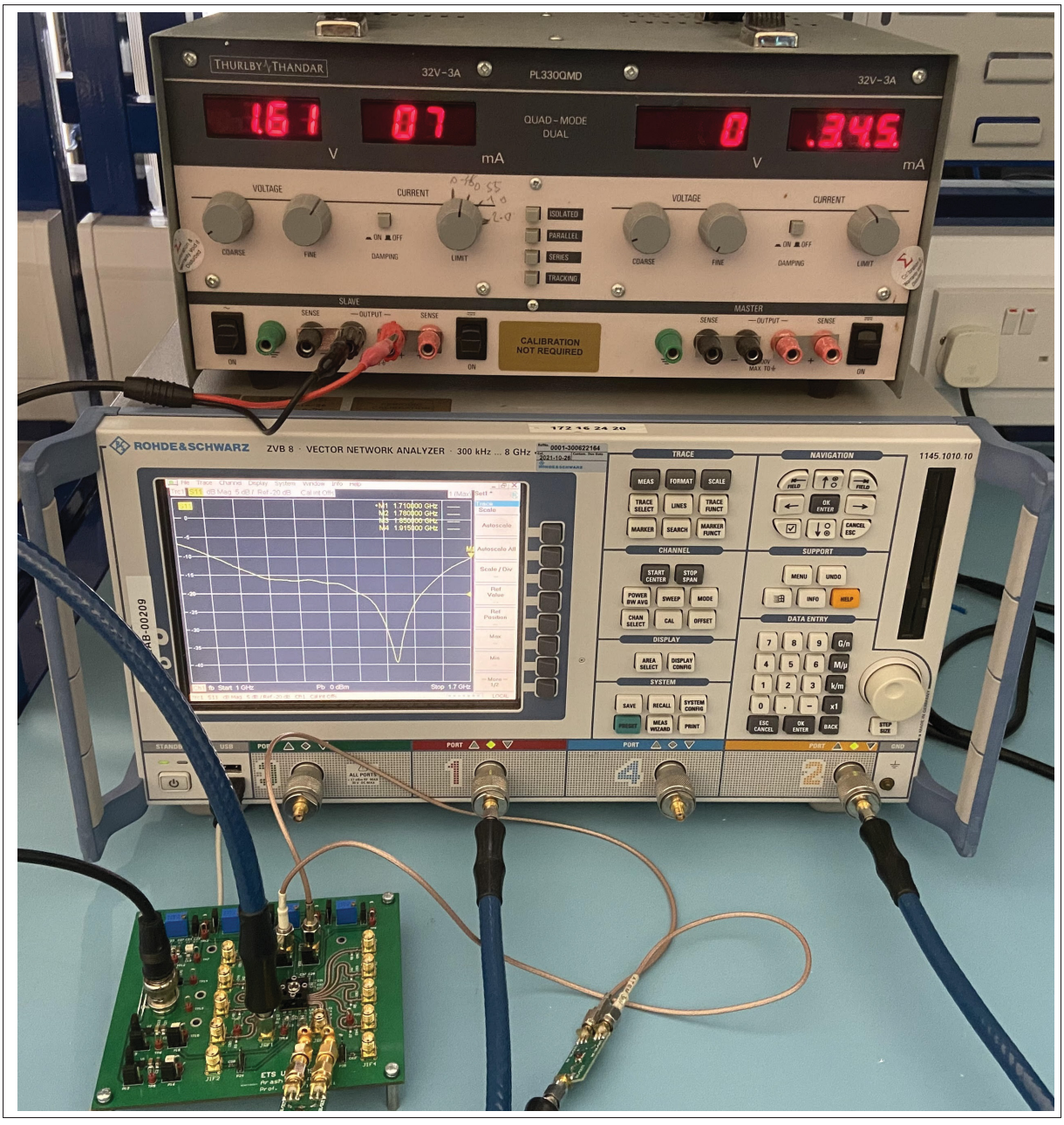

Figure 3.11 Picture of the measurement setup.

The diagram and picture of the measurement setup is shown in Fig 3.10 and 3.11, respectively. The CRR front-end and output buffer supply and ground are separated on the PCB. The chip is packaged into a QFN48 package, and is connected to the PCB with an RF socket (SG-MLF-7006). To extract the actual performance of the CRR front-end, the non-idealities due to the

socket, cables and external baluns should be taken into account. To this end, the S-parameter characteristics of the cables and baluns are extracted using a 4-port vector network analyzer (VNA), Rohde and Schwarz ZVB 8. The socket losses are provided by the manufacturers' datasheet. The single-ended input from the signal generator (Agilent N5182a MXG) is converted to a differential input using an external LC-balun shown at the bottom left of Figure 3.2. A second signal generator(Agilent N5182a MXG) provides the clock signal for the mixer switches. The differential output of the output buffer is converted to a single-ended signal using a 2:1 balun (TRS2-32-75+) and this signal drives the measurement equipment.

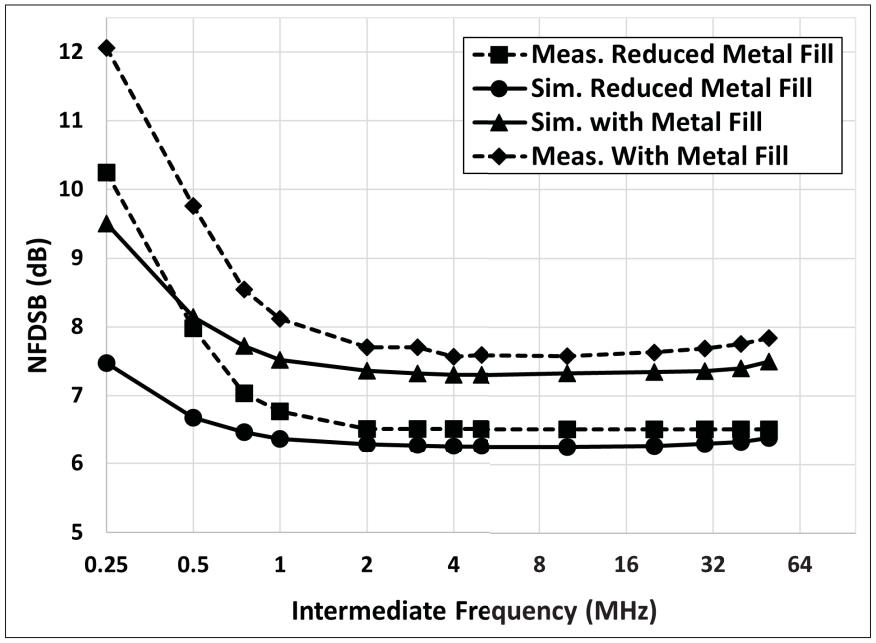

Figure 3.12 The simulated and measured NF versus the IF.

The Y-factor method using a noise source is employed to measure the NF performance. Figure 3.12 illustrates the measured and simulated double side-band (DSB) NF versus the IF while the LO frequency is at 1.3 GHz. A flat measured NF of 7.5 dB is achieved using Chip1 and is close to the simulation results above an IF of 1 MHz.The measured and simulated NF of Chip2 with reduced metal fill lowers by about 1 dB to 6.5 dB above an IF of 1 MHz. The $1/f$ NF is slightly increased for both simulation and measurement at low frequencies due to the AC-coupling between the CRR front-end and the output buffer circuit. This effect is not important as the buffer

would not be required in a receiver implementation including the BB circuits. The measured $1/f$ noise corner frequency is very close to the simulation results. This shows the $1/f$ NC circuit operates well.

The measured and simulated conversion gain versus the IF is shown in Figure 3.13 while an LO frequency of 1.3 GHz is used. The circuit achieves a flat conversion gain of 40.5 dB with Chip1. The figure also shows using Chip2 the impact of the metal fill effect on the conversion gain simulation and measurement results due to the parasitic loading. The conversion gain of 41.5 dB of Chip2 represents a 1 dB improvement over Chip1. A wide IF bandwidth of 90 MHz is achieved. The conversion gain results are reduced at low frequency due to the AC-coupling at the input of the output buffer, but again this would not be an issue in an implementation of the receiver without the buffer.

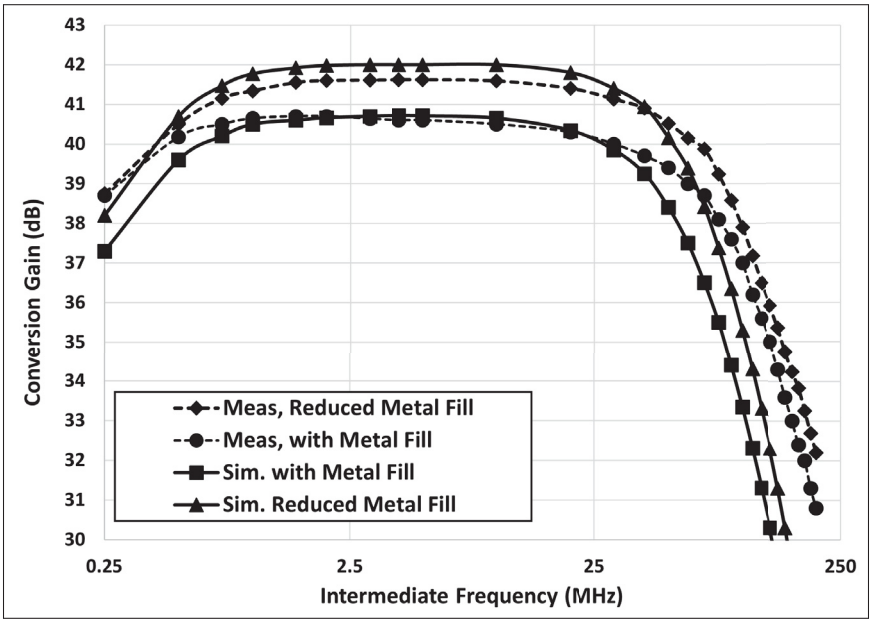

Figure 3.13 The simulated and measured conversion gain versus the IF.

A two-tone test with 1.31 GHz and 1.311 GHz input signals is performed to measure the in-band IIP3 performance of the CRR front-end. An LO frequency of 1.3 GHz is applied to the mixer switches. This generates two tones at 10 MHz and 11 MHz at the IF, along with third-order

intermodulation products at 9 MHz and 12 MHz that appear above the noise floor by increasing the input power. Figure 3.14 shows the output power of the fundamental tone and third-order intermodulation product versus an input power sweep where an in-band IIP3 of −28.2 dBm is achieved for both Chip1 and Chip2. There may be a few dB uncertainty in the IIP3 results since the CML circuit might limit the linearity. To confirm this, under the same biasing condition and test scenario, the CML voltage was increased by 0.2 V. This improved the IIP3 result of Chip1 to −26.5 dBm and Chip2 to −27.5 dBm.

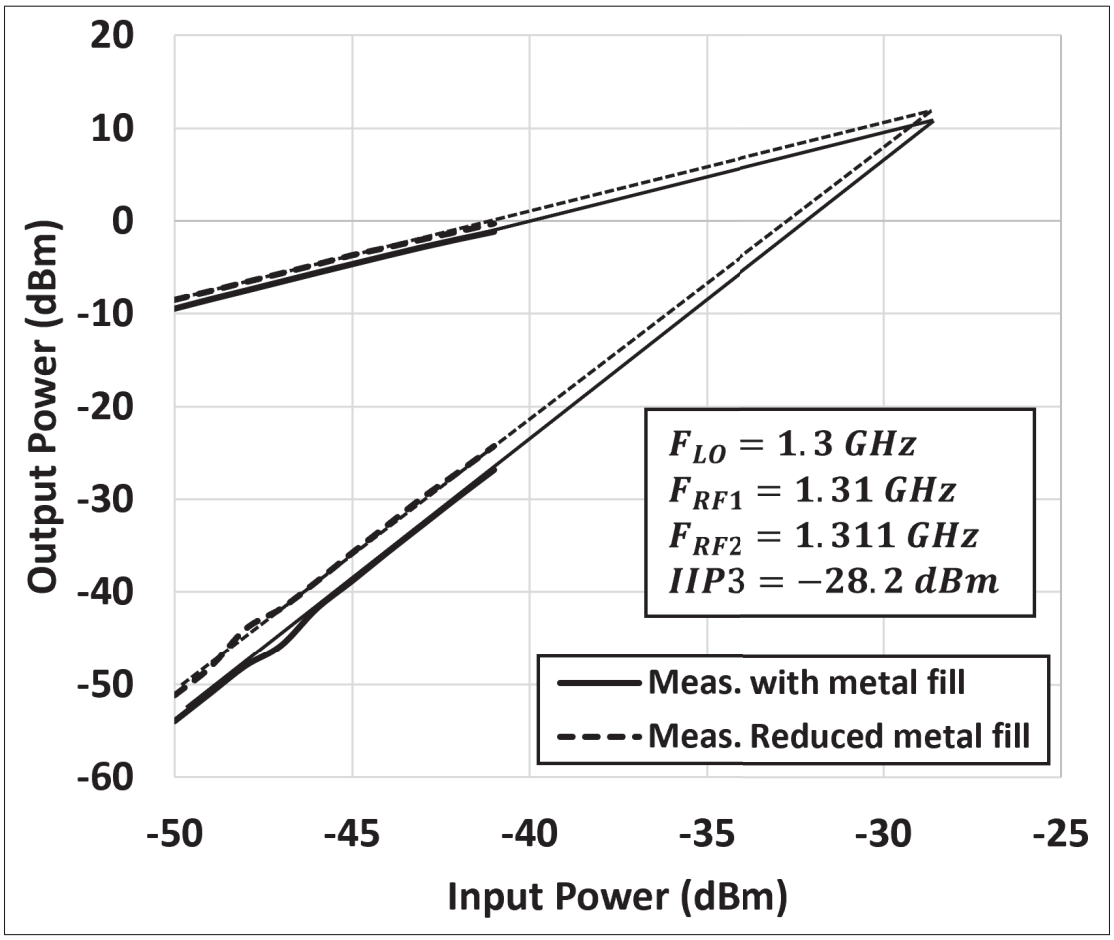

Figure 3.14 Measured fundamental and third-order intermodulation products versus the input power sweep. The resulting in-band IIP3 is shown.

The in-band IIP3 performance is verified across the IF by using a two-tone RF signal (1 MHz offset between tones) and an LO frequency that remains constant at 1.3 G. The input tones

are swept and the IIP3 extracted for multiple IF values. The result is shown in Figure 3.15. It illustrates that the in-band IIP3 performance of Chip1 increases from −28.2 dBm to −25.2 dBm by increasing the IF from 3 MHz to 95 MHz. The IIP3 performance of Chip2 increases from −29 dBm to −26.5 dBm by increasing the IF from 3 MHz to 95 MHz.

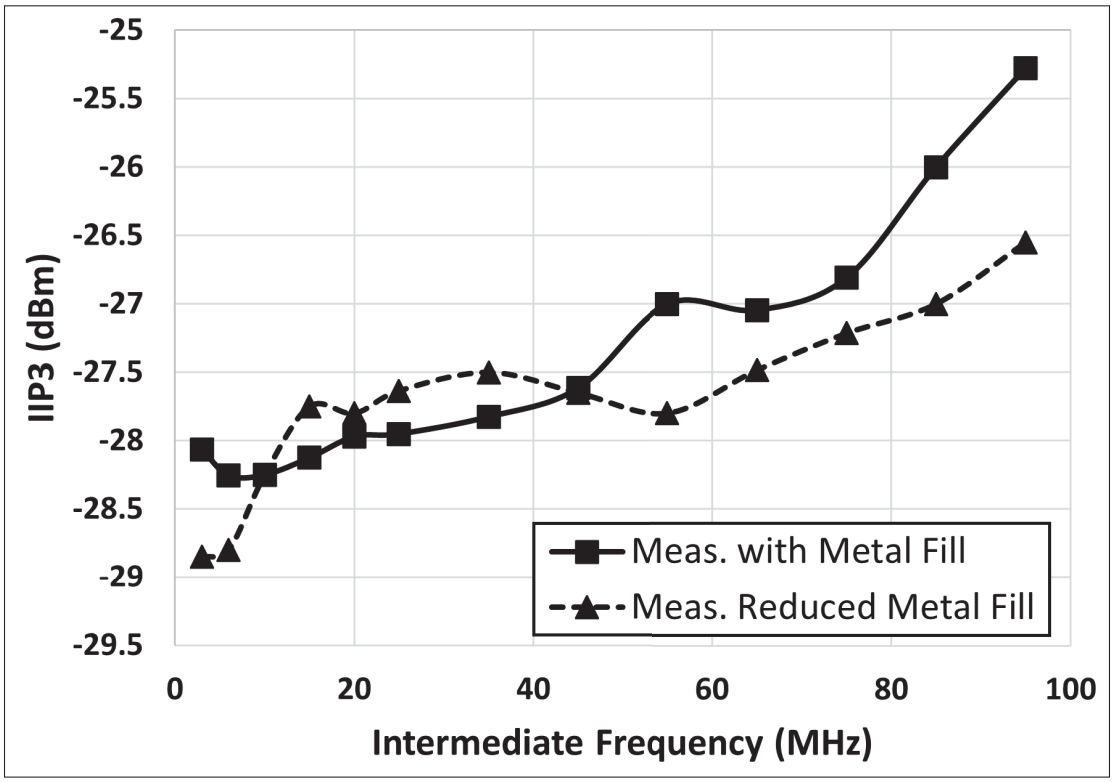

Figure 3.15 Measured in-band IIP3 performance versus the IF.

The out-of-band (OOB) IIP3 performance is verified across the IF by using a two-tone RF signal (1 MHz offset between tones) and an LO frequency that remains constant at 1.3 GHz. The input tones are swept and the IIP3 extracted for multiple IF values. The result is shown in Figure 3.16. It illustrates that the OOB IIP3 performance of Chip1 increases from −24.1 dBm to −16.9 dBm by increasing the IF from 120 MHz to 280 MHz. The OOB IIP3 performance of Chip2 increases from −25 dBm to −16.2 dBm by increasing the IF from 120 MHz to 280 MHz.

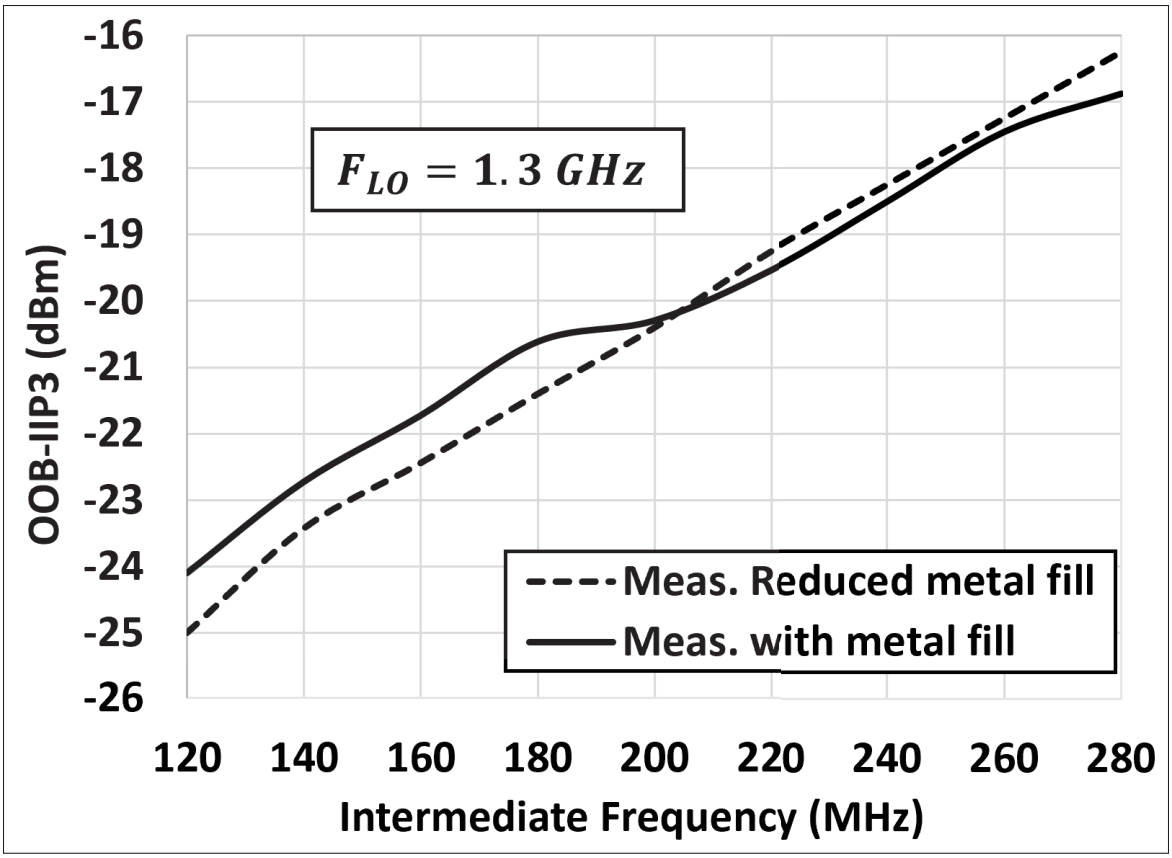

Figure 3.16 Measured OOB IIP3 performance versus the IF.

Figure 3.17 shows the receiver performance across the RF range from 1 GHz to 1.7 GHz while the IF remains constant at 10 MHz. It shows the S_{11} remains below −10 dB over the entire RF range with Chip1. The S_{11} of Chip2 moved slightly to higher frequencies due to the parasitic capacitor reduction on the input nets. Both conversion gain and NF of Chip1 remain almost constant at 40.5 dB and 7.5 dB, respectively. The conversion gain and NF of Chip2 also remain almost constant at 41.5 dB and 6.5 dB, respectively. The NF of Chip2 remains constant at the RF band edge while it degrades slightly for Chip1. The IIP3 result of Chip1 improves for the frequencies above 1.3 GHz from −28.2 dBm to −22.5 dBm due to the RF signal losses at higher frequencies and reduced conversion gain. The IIP3 result of Chip2 follows the same trend and it improves for the frequencies above 1.3 GHz from −29 dBm to −24 dBm.

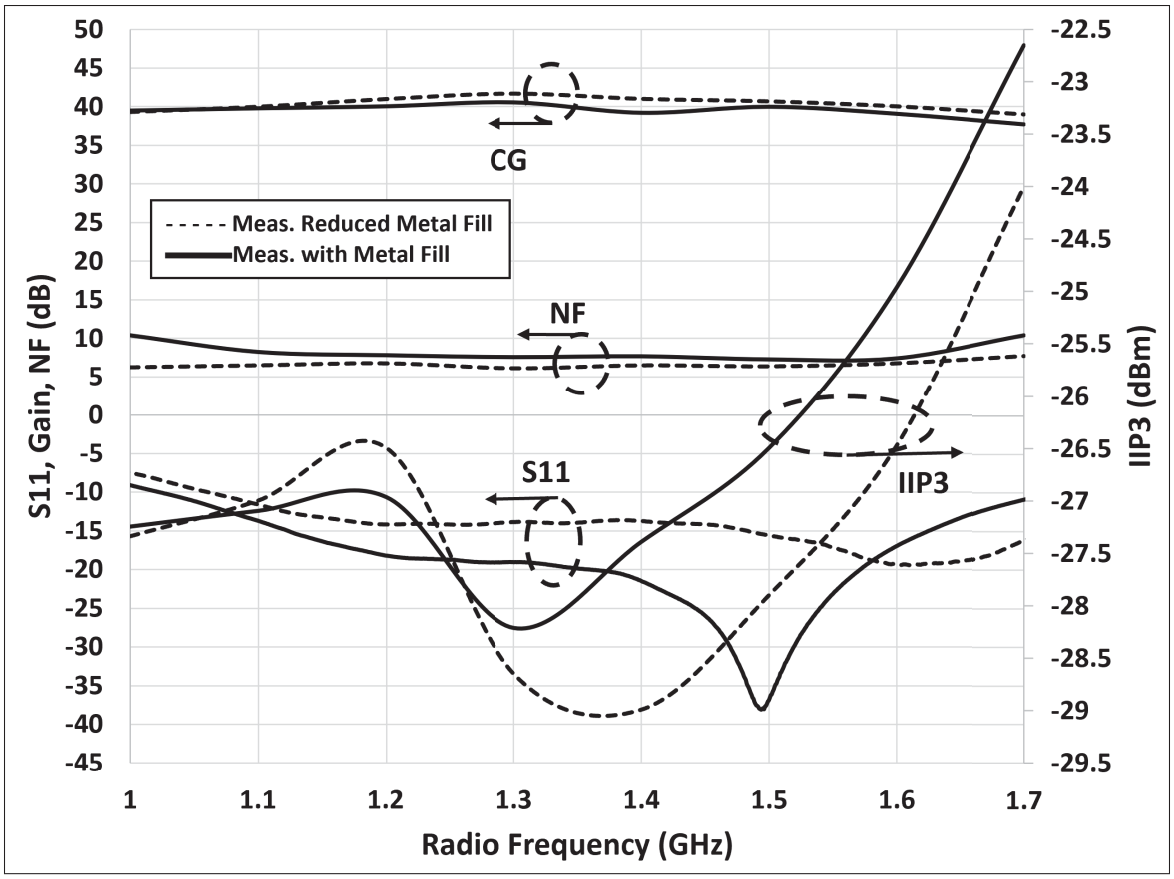

Figure 3.17 Measured receiver performance versus the RF input signal frequency.

The performance comparison and summary of the proposed receiver with the recent literature is reported in Table 4.2. Note that the majority of the other designs in the table are implemented in smaller CMOS technology nodes ranging from 28 nm to 90 nm and have relatively narrow baseband bandwidths (i.e., modulation bandwidth), providing inherent advantages. This work compares well in terms of bandwidth and NF considering its technology node and power consumption. It supports a significantly wider baseband bandwidth of 90 MHz and a wide RF band of operation from 1 GHz to 1.7 GHz (i.e., in the L-band). Its area, considering the technology node utilized, also compares well with the other works. Moreover, its projected low-cost of implementation is well suited to IoT applications, while supporting large modulation bandwidths for applications such as GNSS.

Table 3.1 Performance Summary and Comparison

Parameters	This Work	This Work★	TMTT 2020[1]	JSSC 2014[2]	JSSC 2014[3]	MWCL 2019[4]	JSSC 2017[5]	IEEE 2021[6]	JSSC 2021[7]	JSSC 2021[8]	JSSC 2018[9]	TMTT 2019[10]
Application	IoT	IoT	IoT	ZigBee	ZigBee	IoT	Bluetooth	BLE	IoT	IoT	ZigBee	BLE
Process node	130nm CMOS	130nm CMOS	65nm CMOS	65nm CMOS	65nm CMOS	65nm CMOS	28nm CMOS	65nm CMOS	28nm CMOS	28nm CMOS	65nm CMOS	130nm CMOS
F_{High} (GHz)	1.7	1.7	2.48	3.55	0.96	0.92	2.8	2.48	2.9	2.8	2.48	2.48
F_{Low} (GHz)	1	1	2.4	2.25	0.433	0.9	2	2.4	2.2	1.8	2.4	2.4
BB (MHz)	90	90	2	2	2	20	1.5	2	2	2	2	2
S11 (dB)	<-10	<-10	<-10	<-10	<-10	<-10	<-10	<-10	<-10	<-10	<-10	<-10
Gain (dB)	40.5	41.5	49.5	57	50	40.7	43.4	42	61	45	57.8	42
NF (dB)	7.5	6.5	8.2	8.5	8.1	1.94	7.8	13.2	5.5	6	15.7	7.2
IIP3 (dBm)	-28.2	-28.2	–25.75	-53	-45	-25.6	-20	-25	-46	-13	-18.5	-17
OOB IIP3 (dBm)	-24.1_-16.9	-25_-16.2	N/A	-6	-20.5	N/A	6	N/A	-7.5	5	N/A	N/A
$P_{DC}@V_{DD}$ (mW)	2@1.2	2@1.2	2.16@1.2	1@1.2	1.15@0.5	3.6@1.8	4.3@1.8	1.13@0.8	0.37@0.7	0.38@0.8	1.78@1	1.7@1.2
Area (mm^2)	0.54	0.54	1.16	0.3	0.2	0.559	0.4	0.85	0.5	0.2	0.45	0.7

★ This work with reduced metal fill in the vicinity of sensitive RF nodes. References: [1] Park & Kwon (2020), [2] Lin *et al.* (2014b), [3] Lin *et al.* (2014c), [4] Kim & Kwon (2019), [5] Ramella *et al.* (2017), [6] Park & Kwon (2021), [7] Thijssen *et al.* (2020), [8] Purushothaman *et al.* (2021), [9] Wang *et al.* (2018), [10] Silva-Pereira *et al.* (2018).

Very good performance is achieved in Purushothaman *et al.* (2021), but the receiver architecture is not suitable for wide bandwidth applications due to the sharp frequency response having a 2 MHz bandwidth at the LO frequency. Many of the other receiver architectures are not able to achieve wideband RF matching due to the LNTA topology, making them unsuitable for wideband wireless standards. Note that in some of the references, instead of in-band IIP3, only the 1-dB compression point (P1dB) is reported and it is assumed that in-band IIP3 is 10 dB higher than P1dB.

3.5 Conclusion

A low-power and wideband RF-to-BB CRR front-end was fabricated in TSMC 130 nm CMOS technology. The design was fabricated under two conditions: one is covered with metal fill at sensitive nodes (Chip1), and another has reduced metal fill on the sensitive RF nodes and blocks (Chip2). The results show almost 1 dB improvement in conversion gain and NF when the metal fill is reduced on the sensitive RF nodes and blocks. It uniquely incorporated an AI and NC

circuit to the conventional CRR front-end architecture to enhance the NF performance and RF bandwidth of the receiver. The current sharing of the LNTA, AI and TIA reduced the power consumption significantly. In addition, a cross-coupled technique with a common-gate topology in the LNTA reduces the power consumption further while maintaining the receiver performance. The LNTA uses the LC-Balun to convert the single ended 50 Ω input from the antenna to a differential port with slightly lower impedance in order to allow for the LNTA to be designed with a higher transconductance, thus improving the NF and conversion gain performance.

The proposed wideband receiver front-end can be used for L-band frequency ranging from 1 GHz to 1.7 GHz. This can simplify multi-band receiver modules and lower their integration cost and overall power consumption. For instance, this receiver can be used to support the various global navigation satellite systems. In this work, the LNTA and LC-Balun were tuned to the L-band, but the design could be re-tuned to other applications.

Fundamentally, the proposed CRR front-end architecture allows relatively large CMOS technology nodes to extend their performance capabilities to higher RF operating frequencies at low-power and good NF, which can significantly reduce the implementation cost of wideband RF receivers.

Acknowledgment

The author would like to thank CMC Microsystems for enabling chip fabrication and providing access to the EDA tools. Also, the authors thank Sequans Communications and its supportive team in both hardware platform and RFIC departments for providing laboratory equipment and technical support during the measurements.

Appendix: RF bandwidth reduction mentioned in Chapter 3 compared to that in Chapter 2

This work is indeed the evolution and extension of our earlier published paper in Chapter 2 that only provided simulation results. Moreover, the paper presented in Chapter 3 uses an on-chip

inductor (L_R). Importantly, measurement results are now presented validating experimentally our prior work. In Chapter 2, a model of a high quality off-chip inductor was used in the simulations instead of L_R . In this Chapter, the input inductor which is L_R in figure 3.2 is integrated on-chip. It has a low quality factor compared with an off-chip inductor. In addition, in work presented in Chapter 2, the effect of the extracted PCB model is not included. The figure below shows the effect of the extracted PCB model on the simulated S11 performance that shows that after adding the PCB model, the simulated S11 (i.e., S11 considering the PCB) is very close to the measurement result reported in figure 3.17 in this Chapter.

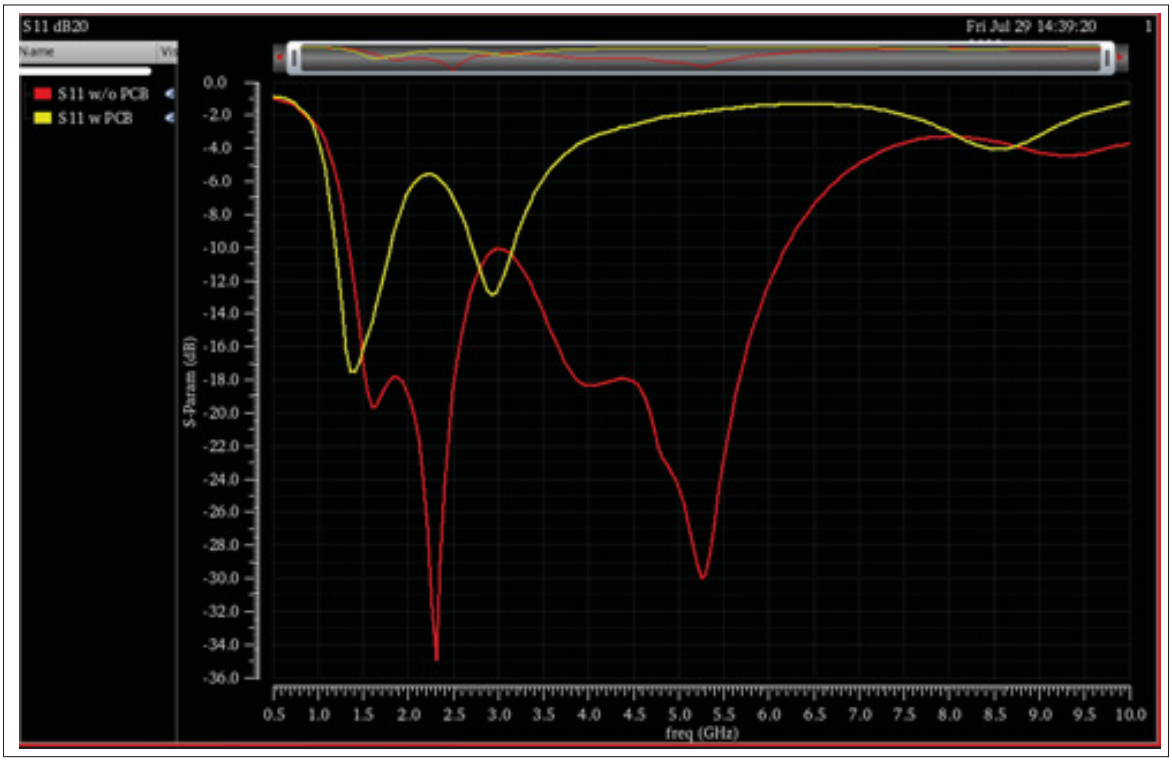

Figure 3.18 Effect of PCB model on S11 performance.

CHAPTER 4

A COMPARISON OF OFF-CHIP DIFFERENTIAL AND LC INPUT MATCHING BALUNS IN A WIDEBAND AND LOW-POWER RF-TO-BB CURRENT-REUSE RECEIVER FRONT-END

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Article Published in *MDPI Electronics*, October 2022.
https://doi.org/10.3390/electronics11213527

Abstract: A wideband and low-power RF-to-baseband (BB) current-reuse receiver (CRR) front-end is proposed and the performance is verified using two matching networks, one with with an LC balun and on-chip biasing inductor, CRR1, and another with a differential balun and without on-chip biasing inductor, CRR2, requiring less area. The transimpedance amplifier (TIA) and low noise transconductance amplifier (LNTA) share the bias current from a single supply to reduce the power consumption. It employs both an active-inductor (AI) and a $1/f$ noise-cancellation technique to improve the NF and RF bandwidth performance. A passive mixer is utilized for RF to BB conversion which does not require any DC power and voltage headroom. Both CRR1 and CRR2 are fabricated in TSMC 130 nm CMOS technology on a single die and packaged using a QFN48. CRR1 occupies an active area of 0.54mm^2. From 1 to 1.7 GHz, it achieves a conversion-gain of 41.5 dB, a double-sideband (DSB) NF of 6.5 dB, S_{11} <-10 dB and an IIP3 of -28.2 dBm while the local-oscillator (LO) frequency is at 1.3 GHz. CRR2 occupies an active area of 0.025mm^2. From 0.2 to 1 GHz, it achieves an average conversion-gain of 37 dB, an average DSB NF of 8 dB and an IIP3 of -21.5 dBm while the LO frequency is at 0.7 GHz. Both CRR1 and CRR2 consume 1.66 mA from a 1.2 V supply voltage.

Keywords: LC balun, differential balun, current-reuse receiver (CRR), cross-coupled common-gate (CCCG) low noise transconductance amplifier (LNTA), wideband, low-power, matching network.

4.1 Introduction

Growth in the internet-of-things (IoT) market led both academia and industry to invest on developing low-power and wideband transceivers to cover a wide RF spectrum and several wireless standards with minimum power consumption. One of the challenges is to design a receiver front-end that can cover several RF bands by minor modification on the input matching network. In this way, design time, cost and verification time can be reduced. However, designing a receiver front-end with low-power consumption and wideband RF coverage is an added challenge.

A well-known method to design low-power circuits is the current-reuse technique which is conventionally used to design low noise transconductance amplifiers (LNTA) Shams *et al.* (2020). In Thijssen *et al.* (2020), a push-pull LNTA is used in a cascaded receiver to reduce the power consumption. However, it reports a poor 1 dB compression point (P1dB) of -56 dBm. A stacked baseband amplifier is employed in a mixer first receiver architecture in Purushothaman *et al.* (2021) that achieves very low power consumption. However, it has limited bandwidth due to the mixer first architecture that makes it not suitable for wideband modulation schemes. A quadrature low noise amplifier (LNA) followed by poly-phase filter (PPF) is employed in Park & Kwon (2020) to improve the power efficiency. However, it suffers form a narrow RF bandwidth due to the common-source LNA topology. Another approach in Silva-Pereira *et al.* (2018), employs a current-reuse LNA followed by an on-chip LC-balun and a passive PPF to reduce the dynamic power consumption in the LO signal path. However, the combination of the on-chip LC balun followed by PPF limits the bandwidth which is not suitable for wideband applications. In Wang *et al.* (2018), a free phase-locked loop (PLL) receiver architecture is proposed, but the reported NF of 15.7 dB is very high. Recently, thanks to the scaling down in CMOS technology, where the voltage-threshold (V_{TH}) is reduced and the transition frequency (f_T) is increased, the current-reuse technique is employed to design a receiver front-end by stacking different blocks and share the bias current from a single supply to reduce the overall power consumption in comparison to the conventional approach in which circuits are cascaded with separate supply currents, as shown in figure 4.1.

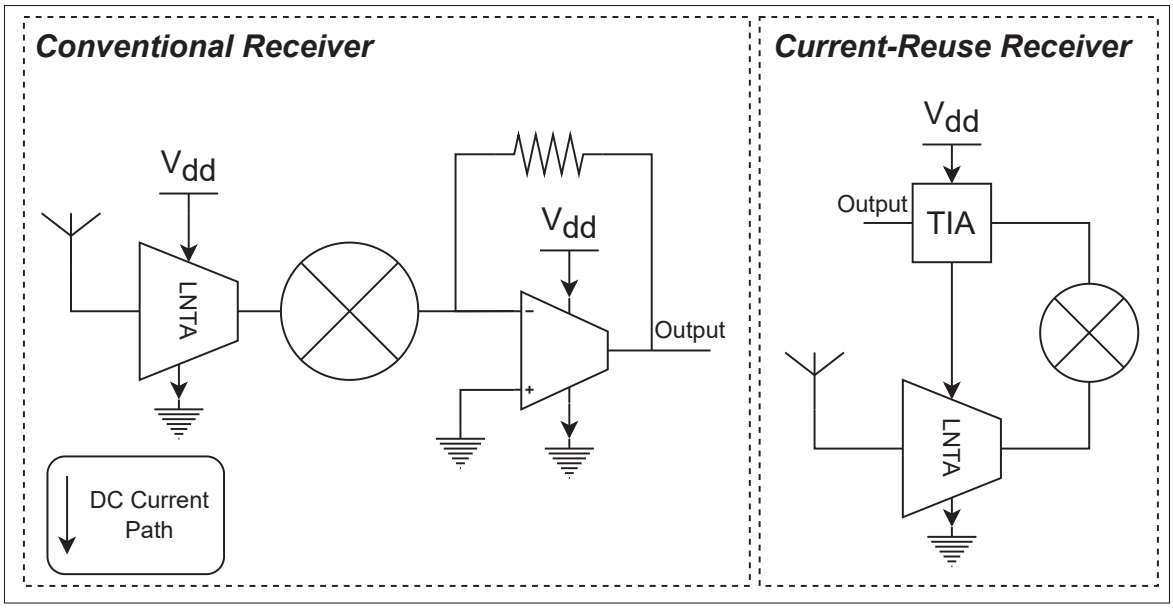

Figure 4.1 Conventional (left) and current-reuse (right) receiver architectures.

A wide range of studies has been done on designing low-power receivers using the current-reuse technique. The low noise amplifier (LNA), down-conversion mixer and voltage controlled oscillator (VCO) are stacked in Tedeschi *et al.* (2010) to share a single supply and bias current which achieves very low power consumption. However, the reported NF of 10 dB is high. Moreover, it may suffer injection locking of the VCO. In Lin *et al.* (2014b), the LNTA, active-mixer and baseband (BB) filter are cascoded. Its choice of an active-mixer increases the voltage headroom requirement to achieve high linearity. In Lin *et al.* (2014c), a function-reuse method is employed where a push-pull amplifier functions as both LNTA and TIA. However, a low supply voltage results in poor 1 dB compression (P1dB) performance of -50 dBm. Moreover, the circuit is mainly suitable for sub-GHz applications due to the limited RF bandwidth. An N-path current-reuse receiver is another alternative which is also suitable for sub-GHz applications Lin *et al.* (2014a). One of the issues in N-path receivers is the requirement for additional circuitry to combine the N paths which requires additional power consumption and area. Moreover, the active-mixer used requires more voltage headroom. A $1/f$ noise-cancellation (NC) technique and linearity enhancement method is utilized by Ghosh & Gharpurey (2011), but it consumes a relatively high 8 mW. A current-reuse technique is used in Cai *et al.* (2020) by sharing the

VCO current with the LNA and PA. Moreover, a function-reuse mixer is employed that reduces the overall power consumption. However, the stacking of the VCO on the LNA and PA may cause problems with VCO locking. Another approach is to employ a method of simultaneous input matching and a $1/f$ NC technique which results a very low NF of 1.94 dB Kim & Kwon (2019) at the cost of very limited RF bandwidth. Both current-reuse receiver (CRR) circuits proposed in Kim & Kwon (2019) and Abbasi *et al.* (2020a) share the output node with the down-conversion mixer input, which causes loading and the loss of the RF signal. In our earlier works Abbasi *et al.* (2020b); Abbasi & Nabki (2022); Abbasi, Moshrefi & Nabki (2022b,a), the concept of an active-inductor (AI) and a $1/f$ NC technique was introduced to overcome the problems mentioned above. The AI circuit helps to isolate the output node from the mixer input. In addition, the $1/f$ NC technique pushes the $1/f$ noise corner below 1 MHz.

This work mainly employs the quadrature (I/Q) low-power and wideband RF-to-BB CRR front-end proposed in Abbasi *et al.* (2022b) to assess its functionality with different matching circuits over a wide frequency range. It evaluates the performance of the LNTA using both a differential balun without an on-chip biasing inductor and an LC balun with an on-chip biasing inductor. The RF-to-BB CRR employs both an AI and $1/f$ NC to improve the gain and NF performance by isolating the RF signal from the output node and removing the common-mode low frequency noise. It utilizes a wideband cross-coupled common-gate (CCCG) topology to convert the RF voltage to an RF current, a 25% down-conversion passive mixer is used to convert the RF current to a BB current without consuming DC current. Finally, it converts the BB current to the BB voltage using a TIA circuit that shares the DC current with the LNTA to reduce power consumption.

This study shows that the proposed CRR is well-suited to different matching circuits over a wide RF range, and discusses both input matching methods and their impact on performance. Notably, a structure with a differential balun and without an on-chip biasing inductor is studied, having reduced area in comparison to what was proposed in Abbasi *et al.* (2022b).

The paper is structured as follows. Section 4.2 overviews the receiver front-end architecture and provides a detailed description of the front-end circuitry, and Section 4.3 presents the measurement results. This is followed by a conclusion.

4.2 RF-to-BB-Current-Reuse Receiver Front-End Circuit-Level Considerations

Scaling down the CMOS technology node improves the frequency of operation and reduces the V_{TH} of the transistors. This allows for the stacking of circuits to share the bias current using a single supply. This introduces several design challenges to maintain the overall performance which was studied in our earlier work Abbasi *et al.* (2022b). In reality, designing a receiver front-end requires time and cost. It would be very efficient to design a receiver front-end that can be used for several frequency bands with minor adjustment in the input matching network. Moreover, a receiver compatible with different matching networks helps to reuse the receiver for applications having different requirements.

The block diagram of the circuit proposed in Abbasi *et al.* (2022b), CRR1, and the block diagram of the proposed circuit in this work, CRR2, are shown in Figure 4.2. CRR2 does not include an internal biasing inductor for the DC current path and uses an external differential balun. Both circuits include the LNTA which mainly defines the receiver performance, the down-conversion passive mixer to reduce the DC power consumption and the voltage headroom required, the AI and $1/f$ NC circuits that are used to improve the NF performance, and the TIA that converts the BB current to the BB voltage at the output. The TIA shares the current with the LNTA to reduce the power consumption.

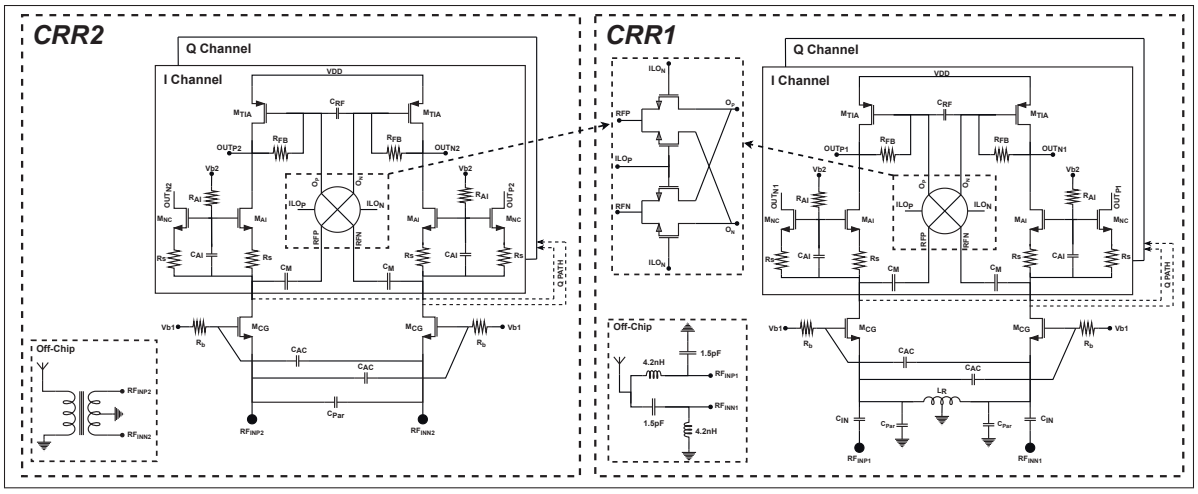

Figure 4.2 CRR1 proposed in Abbasi *et al.* (2022b) (right), CRR2 proposed in this work (left).

4.2.1 LNTA Design with Differential Balun and LC Balun Input Matching Network

The LNTA is the first stage in the receiver front-end which defines the sensitivity and amplifies the weak input signal before down-conversion. There are two well-know topologies to design the LNTA circuit: the common-gate (CG) and the common-source (CS). In Kim & Kwon (2019), a common-source topology was used which results a very low NF at the cost of narrow bandwidth. However, the CS topology is very sensitive to non-idealities such as wire-bonding, reducing the design robustness of the LNTA. On the other hand, the CG topology is well-known for its design robustness and wideband operation, but higher NF. It provides the input matching through $1/g_m$ that can be achieved by optimizing the current and the W/L ratio Razavi (2013). However, the CG topology requires a high current to achieve the required g_m. To overcome this issue, a cross-coupled technique is employed to boost the effective g_m by two times without consuming extra DC current. This results in achieving the required input matching, NF and gain. Moreover, this cross-coupling avoids using large transistors to achieve the required g_m, which results in less parasitics that reduce the RF signal losses and improve NF. In this work, a CCCG LNTA is used with wideband input matching and allows for higher robustness at the cost of higher NF.

In Figure 4.2, the CCCG LNTA is formed by M_{CG} and the cross-coupled connection of C_{AC}. The NF is given by

$$F \cong 1 + \frac{\gamma}{4\alpha} \cdot \frac{1}{R_S g_m} + \frac{R_{Balun}}{R_S}, \tag{4.1}$$

where α and γ are the bias-dependent noise parameters and R_S is the source resistance. The balun losses can be modeled by series resistor R_{Balun}. The γ/α is reduced by increasing the channel-length slightly but maintaining an f_T of at least ten times higher than the frequency of operation.

To perform input matching using a 1:1 differential balun, $R_S = 1/2g_m$ is designed for. Then the second term in (4.1) increases by two times. The noise factor is then given by

$$F \cong 1 + \frac{\gamma}{2\alpha} + \frac{R_{Balun}}{R_S}. \tag{4.2}$$

Compared to the differential balun, the LC balun converts the 50 Ω antenna impedance to the required impedance (in this work 25 Ω) on the differential side. In this way, the LNTA can be designed with a higher g_m while maintaining the input matching performance and reducing the NF. In this way, the LNTA noise is given by

$$F \cong 1 + \frac{\gamma}{4\alpha} + \frac{R_{Balun}}{R_S}. \tag{4.3}$$

The LNTA with differential balun can be designed with a 25 Ω input impedance, but at the cost of poor input matching.

In this work, the LNTA is designed using an LC balun and a differential balun at its input in CRR1 and CRR2, respectively.

The single-ended antenna input needs to convert to a differential signal at the input of the LNTA. CRR1 employs an off-chip LC balun to convert the single-ended signal to a differential one.

Moreover, an on-chip inductor, L_R, is used to provide the DC current path, and resonates with the large parasitic capacitors, C_{Par}, at the input of the LNTA. L_R helps reduce RF signal losses, and allows the receiver to operate at higher frequencies, as will be later shown in the measurements. Although the LC balun is well-known for its narrow band operation, its combination with the CG LNTA topology provides wideband input impedance matching Abbasi *et al.* (2020b). Alternatively in CRR2, an off-chip single to differential balun is utilized. The balun provides the DC current path that removes the need for the on-chip inductor that requires significant die area. However, it suffers from high RF signal losses due to the parasitic capacitances that are not resonated out as in CRR1, reducing its operating frequency range capabilities.

The LC balun and LNTA in CRR1 are tuned to operate from 1 GHz to 1.7 GHz. CRR2 is designed over a similar frequency range to compare with CRR1, but its input matching strategy will nonetheless reduce its operating frequency range.

4.2.2 Active-Inductor and $1/f$ Noise-Cancellation Technique

Conventionally, CRRs use cascode devices to boost the output impedance and isolate the I/Q paths Abbasi *et al.* (2020b); Kim & Kwon (2019). However, they suffer from RF signal loss due to the sharing of the mixer input with the output node that has large capacitive loading. Moreover, the 1/f noise from the LNTA is directly coupled to the output through the cascode transistor; despite the conventional receiver architecture that uses an AC-coupling capacitor before the mixer to remove low frequency components. To overcome the issues mentioned above, our earlier works Abbasi *et al.* (2020a); Abbasi & Nabki (2022); Abbasi *et al.* (2022b) proposed the AI and 1/f NC circuits.

The AI circuit helps isolate the passive mixer input from the output node to avoid RF losses due to the loading of the output node which helps improve the NF and gain at higher frequencies even in a relatively large technology node such as 130 nm CMOS.

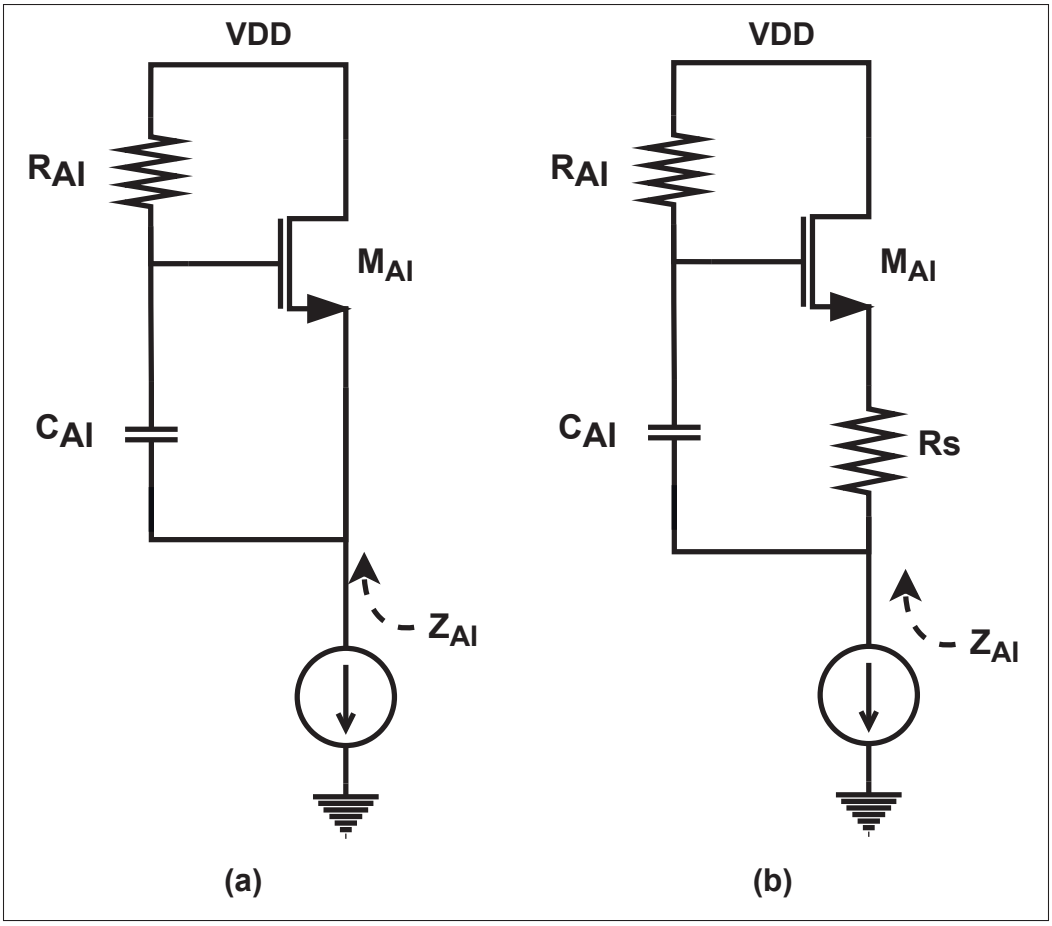

Figure 4.3 (a) Conventional and (b) active-inductor with R_s.

Figure 4.3(a) shows the conventional AI proposed in Razavi (2020). The AI is formed by M_{AI}, R_{AI} and C_{AI}. The impedance looking into the AI circuit is small at low frequencies to pass the DC current while it keep increasing moving towards high frequencies. The impedance looking into the circuit shown in Figure 4.3(a) is given by

$$Z_{AI}(s) \cong \frac{R_{AI}C_{AI}s + 1}{g_{m,AI} + C_{AI}s} \,||\, \frac{1}{sC_{par}}, \tag{4.4}$$

where C_{par} is the parasitic capacitance at the mixer input. C_{par} is dependant on the technology node.

A small resistor, R_S, is added to boost the impedance looking into the AI circuit at the cost of voltage headroom, as shown in Figure 4.3(b). The impedance looking into the AI circuit, Z_{AI} is then calculated by

$$Z_{AI}(s) \cong \frac{g_{m,AI}R_S(R_{AI}C_{AI}s+1)+R_{AI}C_{AI}s}{g_{m,AI}R_SC_{AI}s+g_{m,AI}+C_{AI}s} \,||\, \frac{1}{sC_{par}}, \tag{4.5}$$

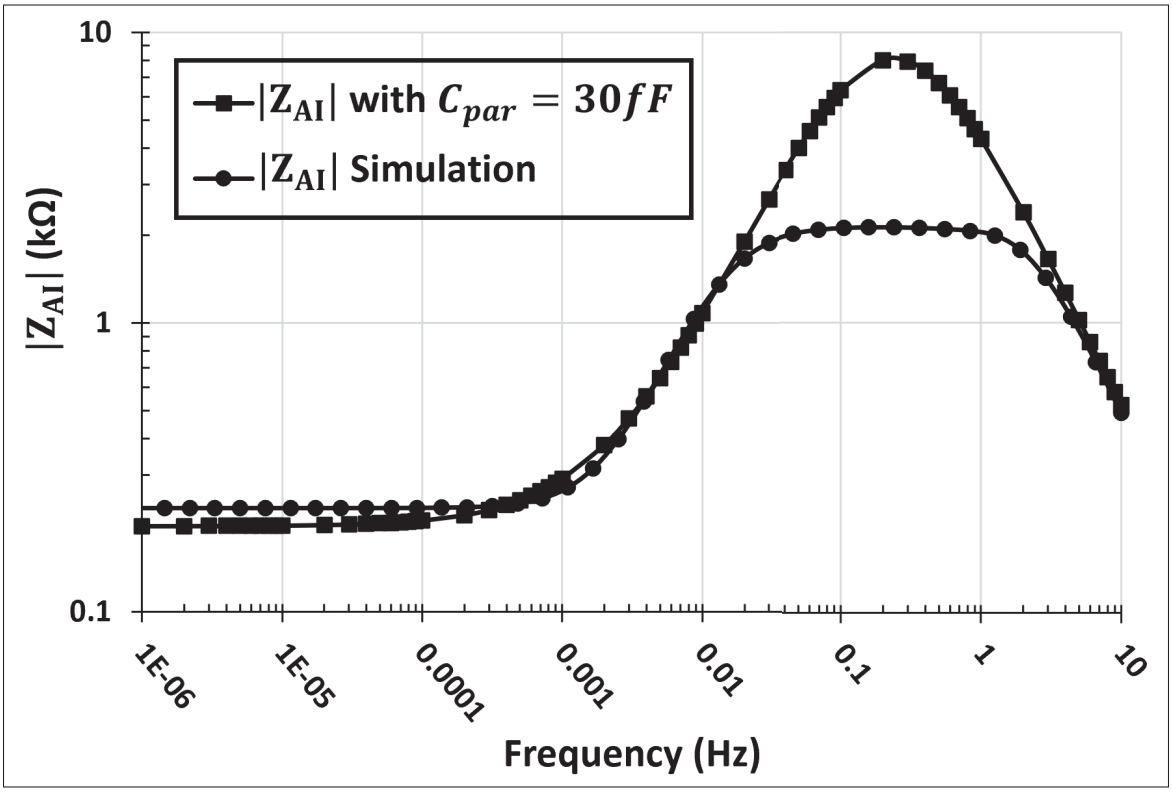

Figure 4.4 Mathematical model of Z_{AI} looking into the active-inductor with R_S included and C_{par} of 30 fF along with circuit simulation results.

Appendix A derives (4.5). The mathematical model of $|Z_{AI}|$ from (4.5) with a C_{par} value of 30 fF is plotted versus the frequency along with simulation results in Figure 4.4, where g_m is of 3.5 mS, C_{AI} is of 1 pF, R_{AI} is of 30 kΩ and R_S is of 200 Ω. For high values of g_m, the low frequency impedance in (4.5) is equal to R_S if channel-length modulation is ignored.

As mentioned previously, the LNTA $1/f$ noise is directly coupled into the CRR output since the AI circuit is not blocking low frequencies. To suppress the resulting low frequency noise, a $1/f$ NC circuit is used. M_{NC} provides the signal path to the output with the opposite sign to cancel the low frequency noise and push the $1/f$ corner to a lower frequency.

4.2.3 Passive Mixer

The RF current from the LNTA needs to be down-converted to the BB current before the TIA and BB circuits. To this end, both active and passive mixer structures can be employed. Usually, the passive mixer is preferred over the active mixer since the active mixer suffers from both a voltage headroom issue and a direct coupling of low frequency noise.

Accordingly, a 25% double balanced passive mixer is employed to down-convert the RF current from the LNTA to a BB current without DC power consumption and no voltage headroom limitation. The mixer should have an input impedance that is much smaller than that of the LNTA output impedance in order to ensure lower NF and higher gain. Moreover, a low input impedance reduces the voltage gain at the input of the mixer which improves linearity. Thus, it is important to optimise the switch sizes in a way to achieve low input impedance, while maintaining the parasitic capacitance sufficiently small to avoid RF signal loss. The gate of the mixer switches need to be biased such that the LO signal turns on and off the mixer switches completely. The voltage bias of the source and drain terminal of the mixer switches is provided by the TIA. The rail-to-rail voltage of the LO signal should not exceed the transistor breakdown, and a voltage that is similar to the supply or lower is preferred.

4.2.4 Transimpedance Amplifier

The TIA is formed by a single transistor, M_{TIA}, and feedback resistor, R_{FB}. It converts the BB current to the BB voltage at the output. A large channel-length is preferred for M_{TIA} to enhance the output impedance. The simplified equation of the conversion-gain is given by

$$gain \cong \frac{2\sqrt{2}}{\pi} g_{m,eff} R_{FB}, \tag{4.6}$$

where $g_{m,eff}$ is two times the transconductance of transistor M_{CG}.

4.3 Experimental Results and Discussions

The wideband and low-power current-reuse receiver front-end was fabricated in a TSMC 130 nm CMOS process, and the die micrograph is shown in Fig 4.6, occupying a total area of 1.2 mm × 1.2 mm. The on-chip current-mode logic (CML) buffer provides output matching to measure the performance of the CRR using a spectrum analyzer (Agilent N9020A), as shown in Fig. 4.5. The CML buffer needs to consume a high power of 48 mW so that the CRR performance is maintained, notably its linearity. The current bias needs to be adjusted to achieve a transconductance for M_1 that yields a 0 dB gain given by $g_{m1} \times 50\Omega$. The required transconductance can be reduced by half if the output impedance is doubled. This helps to reduce the effect of parasitic capacitors and increases the bandwidth of the CML buffer. In this way, to match the 100 Ω output impedance of the CML buffer with the spectrum analyzer, a 2:1 differential to single-ended balun is required and the losses need to be taken into account during the measurements. In addition, the cascode transistor, M_2, enhances the output impedance and reduces the miller effect to increase the bandwidth. The large AC-coupling capacitor, C_{AC}, is used to separate the CML buffer biasing from the CRR output voltage. Both the CRR and the CML buffer utilize a 1.2 V supply.

As was previously discussed, the performance of the circuit is characterized using two different input matching networks: i) a Differential balun (TCM1-63AX-2+), and ii) a custom-designed LC balun. This outlines the robustness of the circuit, along with its operation over a wide RF band with the two input matching methods utilized.

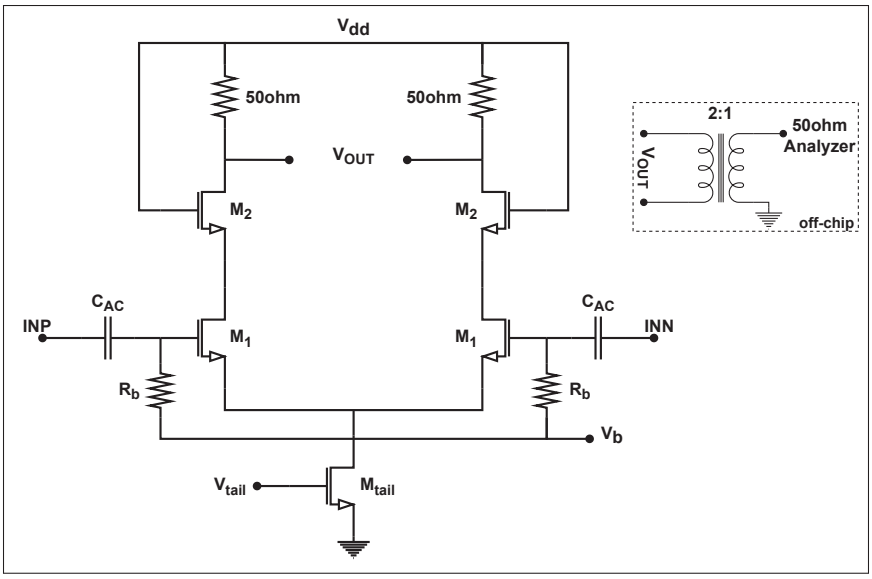

Figure 4.5 The CML buffer circuit used to drive the measurement equipment in matched state.

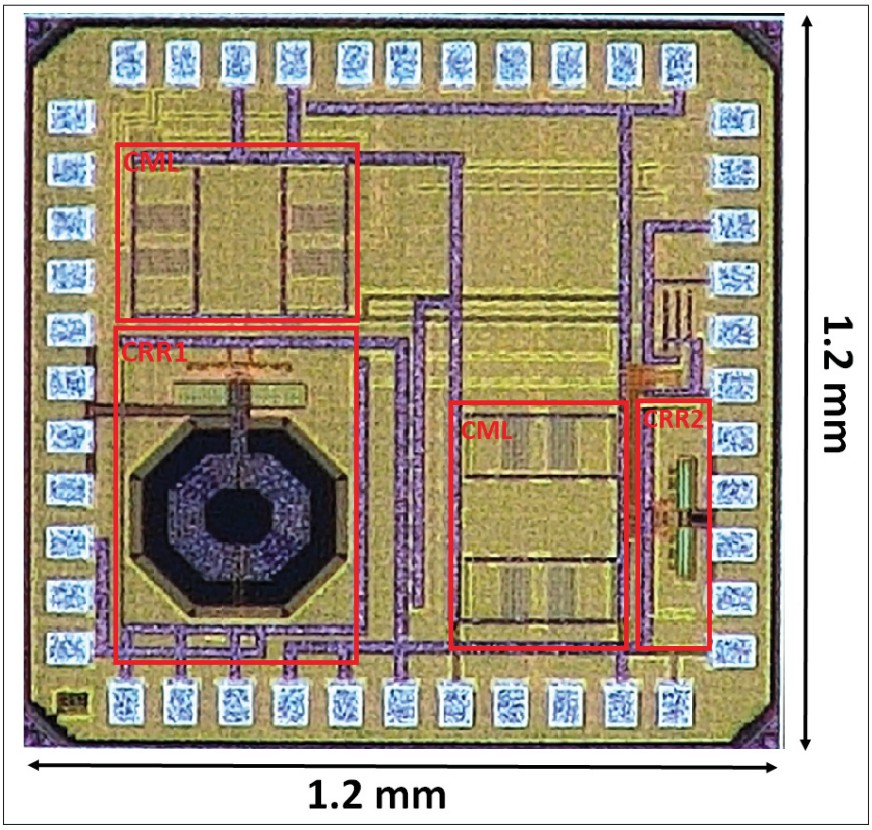

Figure 4.6 Die micrograph.

Figure 4.7 Measurement setup using a VNA to evaluate the S_{11} performance of CRR1 and CRR2. The voltage shown on the power supply is applied to the LDO on the PCB that in turn provides the 1.2V supply to the chip.

For this purpose, as was shown on Figure 4.2, two CRR topologies were implemented in this work: one with an on-chip inductor, CRR1, which occupies an active area of 0.54mm^2 and is measured using an LC balun at its input, and the other without an on-chip inductor, CRR2, that occupies a much smaller active area of 0.025mm^2 and is measured with a differential balun at its input. These active areas exclude the CML buffer and bond pads. Both CRR1 and CRR2 consume 1.66 mA from the 1.2 V supply. This identical current biasing is selected to provide a representative comparison of both presented circuits.

The chip is packaged in a QFN48, and it is connected to the PCB using a socket (SG-MLF-7006). Non-idealities related to the cable, socket and external output balun are carefully considered. To

this end, the S-parameter characteristics of the cables and baluns are extracted using a 4-port vector network analyzer (VNA) (Rohde and Schwarz ZVB-8). The socket losses are provided by the manufacturers' datasheet. Two signal generators (Agilent N5182a MXG) were used to generate the input signal and the clock signal for the down-conversion mixer switches. For the measurement, the differential output of the CML buffer is converted to a single-ended output to the spectrum analyzer using an external 2:1 balun. Figure 4.7 shows the measurement setup using a VNA to measure the S_{11} performance of CRR1 and CRR2. The power supply shows that both CRR1 and CRR2 consume together 3 mA while their CML buffers are powered down.

There are several methods to measure the NF performance of the receiver. In this work, the Y-factor method which utilizes a noise source is employed with high accuracy. The NF performance of CRR1 and CRR2 is measured across the RF input and is shown in Figure 4.8. The NF remains below 8 dB over the RF from 1 to 1.7 GHz in CRR1. However, the NF is increasing from 6 to 10.5 dB with the RF going from 0.2 to 1 GHz in CRR2. This is thanks to the on-chip inductor used in CRR1 that resonates with C_{Par} at the frequency of operation which reduces RF signal losses and allows CRR1 to maintain its NF performance at higher frequencies. However, this comes at the cost of a larger chip area for CRR1 due to its on-chip inductor. The performance of both CRR1 and CRR2 is verified across the IF while the LO frequency is constant at 1.3 GHz and 0.7 GHz, respectively, and the results are shown in Figure 4.9. The low frequency noise is suppressed and the $1/f$ corner noise is pushed to a low frequency of less than 1 MHz thanks to the $1/f$ NC circuit.

A low-power RF signal with a 5 MHz frequency spacing from the LO frequency is applied to the input to calculate the conversion-gain from the output signal power at BB (in dBm) minus the power of the input signal at RF. The measured conversion-gain performance versus the RF input is shown in Figure 4.10. Relative to the NF performance shown in Figure 4.8, the conversion gain in CRR2 reduces from 39.5 to 33 dB over the RF input range from 0.2 to 1 GHz while CRR1 maintain its conversion-gain performance of about 40 dB over the entire RF band from 1 to 1.7 GHz.

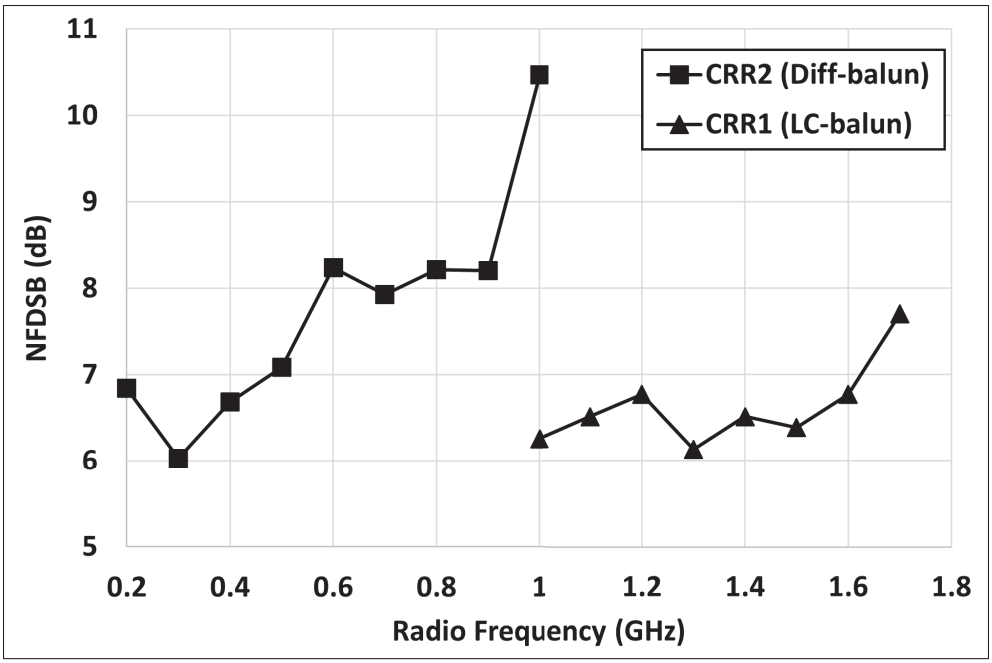

Figure 4.8 The NF performance CRR1 and CRR2 versus the RF input.

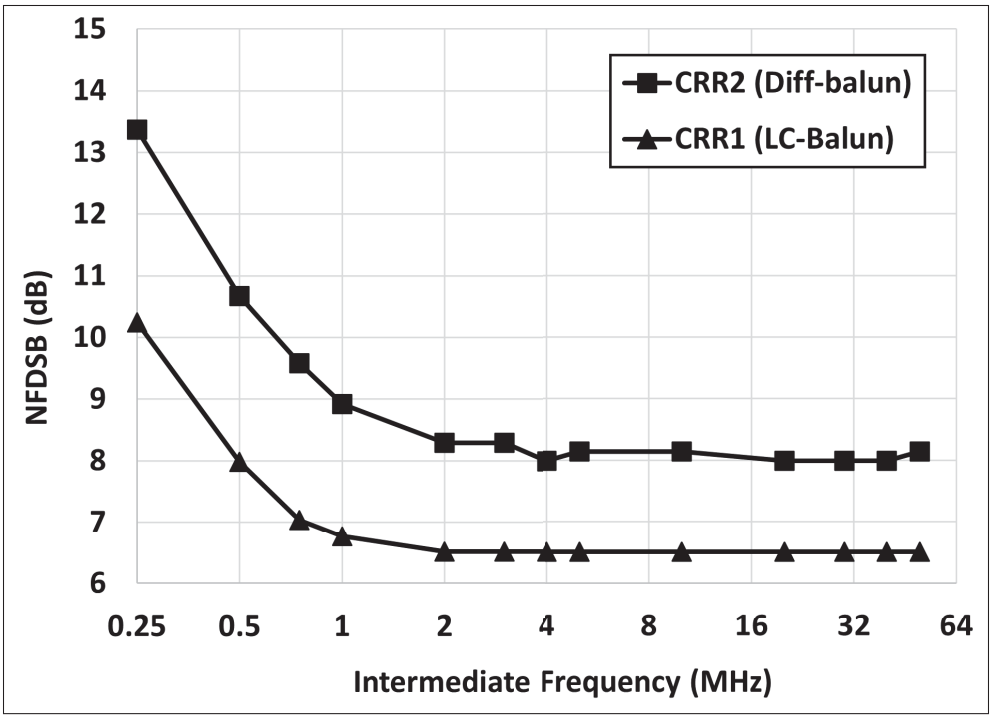

Figure 4.9 The NF performance of CRR1 and CRR2 versus the IF.

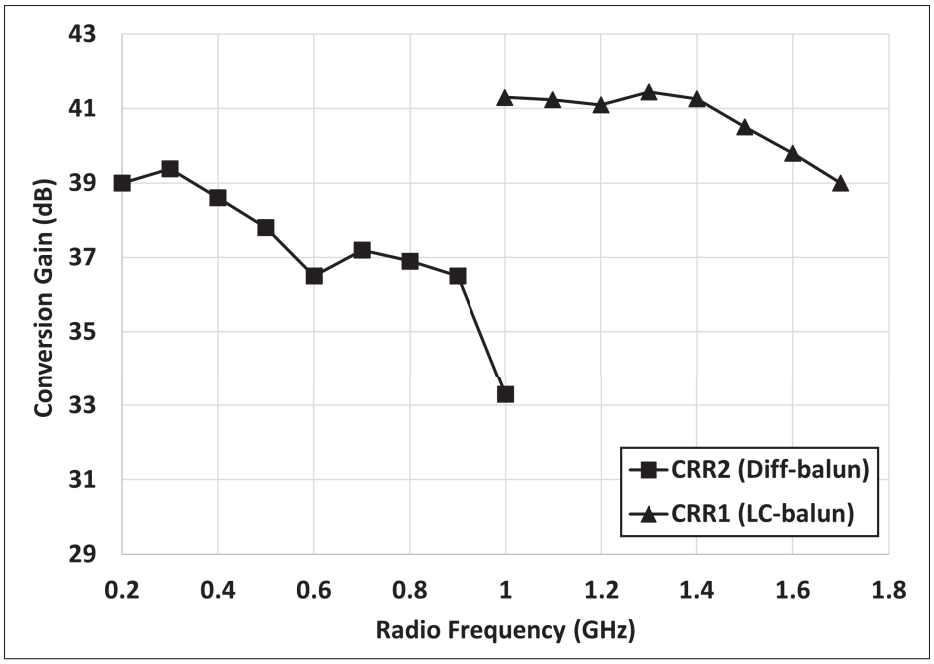

Figure 4.10 The conversion-gain performance of CRR1 and CRR2 versus the RF input.

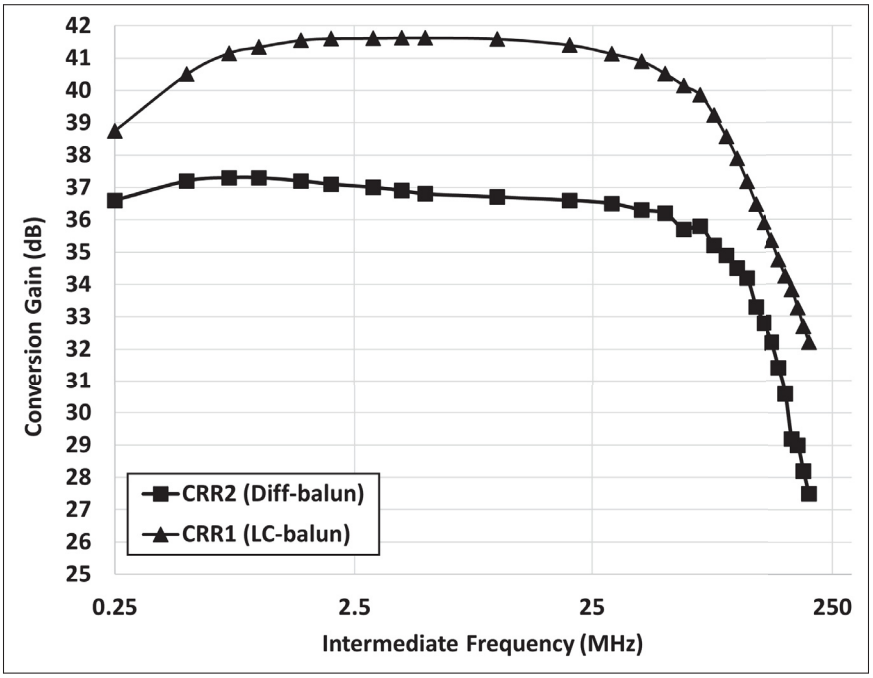

Figure 4.11 The conversion-gain performance of CRR1 and CRR2 versus the IF.

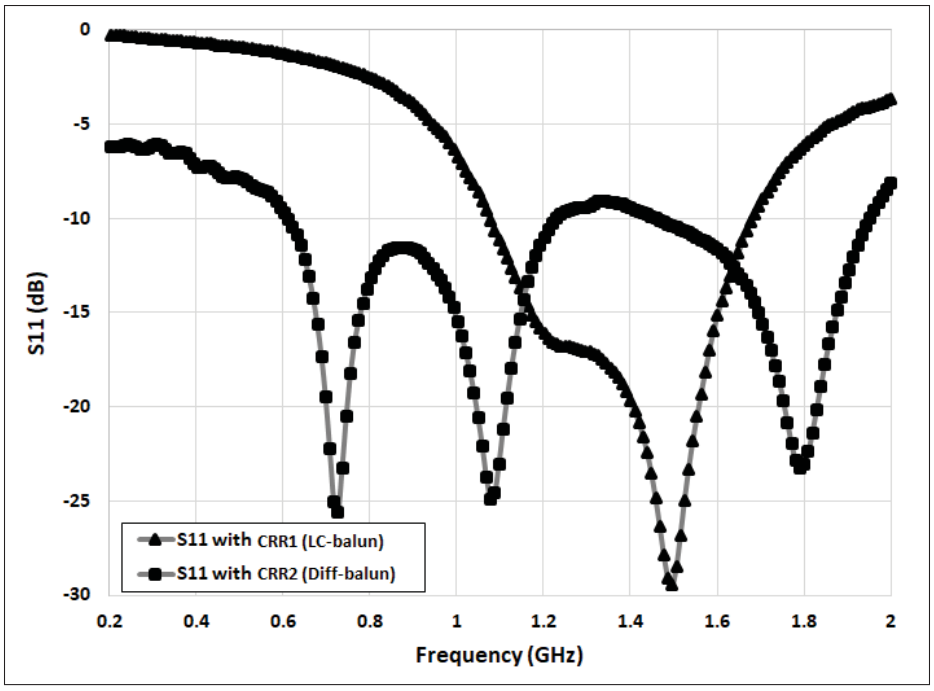

Figure 4.12 The S11 performance of CRR1 and CRR2 versus the RF input.

The conversion-gain performance is also measured across the IF while the LO is constant at 1.3 GHz in CRR1 and 0.7 GHz in CRR2. The resulting conversion gain curves are plotted in Figure 4.11. The bandwidths of both CRR1 and CRR2 remain almost the same since they use the same AI, $1/f$ NC, passive mixer, TIA and CML buffer. In this figure, CRR1 achieves almost 4.5 dB higher gain than CRR2 due to the higher loss of the differential balun and the lack of on-chip inductor to resonate with the paracitic capacitors at the input of the receiver.

The S_{11} performance of both CRR1 and CRR2 is measured versus the RF input using a VNA, and the results are shown in Figure 4.12. It illustrates that CRR1 with the LC balun achieves an $S_{11}<-10$ dB over a wide RF bandwidth from 1.1 to 1.7 GHz. CRR2 achieves an $S_{11}<-10$ dB over a band of 0.6 to 1.2 GHz. Although the S_{11} is higher than -10 dB for frequencies below 0.6 GHz in CRR2, due to the reduced parasitic capacitor contribution at lower frequencies, resulting in reduced RF loss, it could nonetheless maintain a good NF and conversion-gain. At 0.2 GHz the S_{11} is -6.2 dB which is equivalent to the a mismatch-induced loss of 1.2 dB.

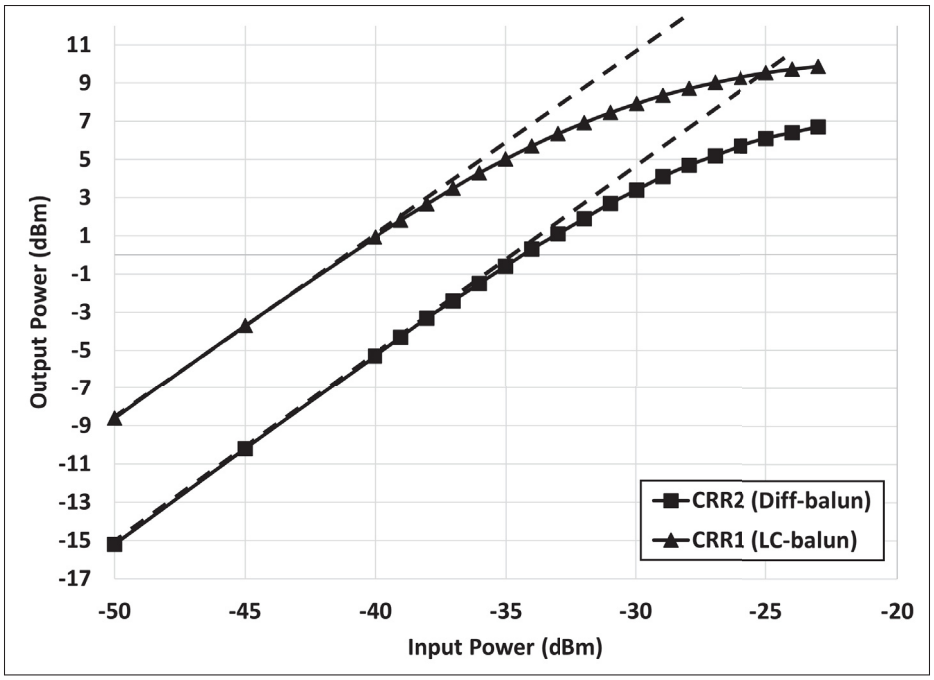

Figure 4.13 The measured output signal power of CRR1 and CRR2 versus a single-tone input power sweep.

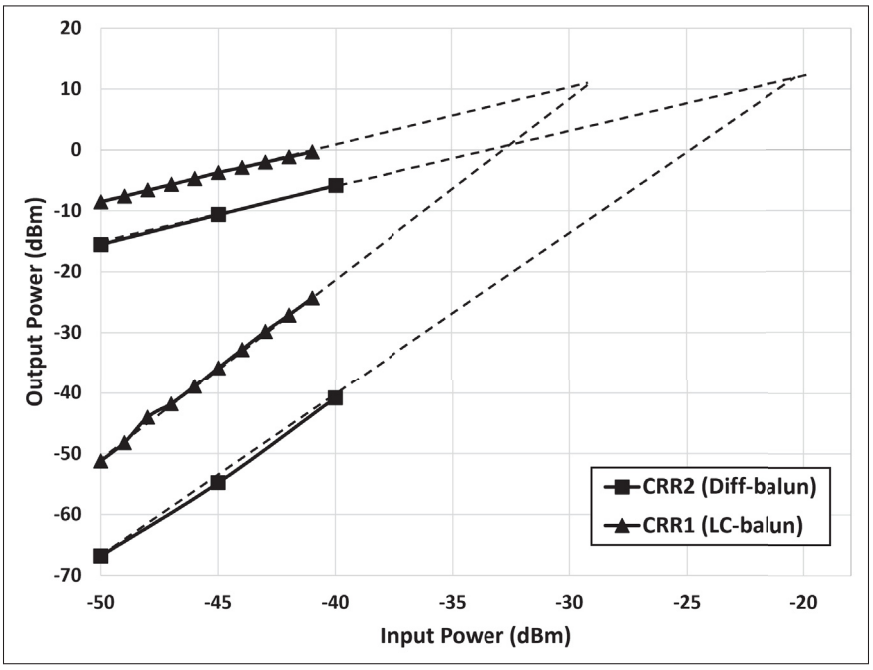

Figure 4.14 The measured third-order intercept points of CRR1 and CRR2 versus a two-tone input power sweep.

The linearity performance of CRR1 and CRR2 is characterized using P1dB and the in-band third-order intercept point (IIP3). The P1dB measurement is performed by applying a single input tone that is 5 MHz offset from the LO signal, where the signal power is swept from −50 to −20 dBm. This is done while the LO signal is at 1.3 GHz in CRR1 and 0.7 GHz in CRR2. The resulting output power versus the input power is plotted in Figure 4.13. It shows that CRR1 achieves an input P1dB of −35.5 dBm, while CRR2 achieves a higher input P1dB of −31 dBm, which is relative to the gain difference reported above.

The IIP3 performance is evaluated using a two-tone test applied to the input with 10 MHz and 11 MHz offsets from the LO signal, while the LO frequency is at 1.3 GHz in CRR1 and 0.7 GHz in CRR2. The input power swept from −50 to −35 dBm. This generates two fundamental tones of 10 MHz and 11 MHz along with two intermodulation products of 9 MHz and 12 MHz at the output. The output fundamental tone and the third-order intermodulation products are plotted versus the input power in Figure 4.14. It illustrates that CCR1 achieves an IIP3 of −28.2 dBm, while CRR2 achieves an IIP3 of −21.5 dBm. Note that there may be a few dB of uncertainty in the IIP3 results since the CML buffer may limit the linearity.

The overall performance summary of CRR1 and CRR2 along with a comparison to other works using a current-reuse topology is reported in Table 4.1. The results show that CRR2 operates at lower frequency compared to CRR1, our earlier work. Otherwise, the overall performance remains similar. Notably, in CRR2, the conversion gain is reduced and the NF increased, but linearity is improved. Moreover, CRR2 achieves higher bandwidth of 110 MHz compared to CRR1 (90 MHz).

Overall, this circuit topology, in either of the forms presented, achieved a high BB bandwidth, making it suitable to wide modulation bandwidth applications. The NF, IIP3 and bandwidth performance compare well with the state-of-the-art considering the power consumption and technology node of the presented receivers.

The presented architecture shows that it can provide good performance metrics regardless of the input network selected for impedance matching. An LC balun input matching strategy (CRR1)

Table 4.1 Performance Summary and Comparison to Other Works

Parameters	This Work CRR2 (Diff. balun)	This Work CRR1 (LC Balun)	TMTT 2020[1]	JSSC 2014[2]	Elec. 2020[3]	MWCL 2019[4]	JSSC 2017[5]	IEEE 2021[6]	JSSC 2021[7]	JSSC 2018[8]	TMTT 2019[9]
Application	IoT	L-band	IoT	ZigBee	ZigBee	IoT	Bluetooth	BLE	IoT	ZigBee	BLE
Process node	130nm CMOS	130nm CMOS	65nm CMOS	65nm CMOS	130nm CMOS	65nm CMOS	28nm CMOS	65nm CMOS	28nm CMOS	65nm CMOS	130nm CMOS
Freq. (GHz)	0.2-1	1-1.7	2.4-2.4	2.4	2.4	0.91	2.4	2.4-2.48	1.8-2.8	2.4	2.4
Bandwidth (MHz)	110	90	2	2	2	20	1.5	2	2	2	2
S11 (dB	<-10	<-10	<-10	<-10	<-10	<-10	<-10	<-10	<-10	<-10	<-10
Gain (dB)	33-39.5	41.5	49.5	57	45	40.7	43.4	42	45	57.8	42
NF (dB)	6-10.5	6.5	8.2	8.5	3.5	1.94	7.8	13.2	6	15.7	7.2
IIP3 (dBm)	-21.5*	-28.2*	-25.75*	-6†	N/A	-25.6*	-20*	-25*	-13*	-18.5*	-17*
P_{DC}@VDD (mW)	2@1.2	2@1.2	2.16@1.2	1@1.2	2.9@1	3.6@1.8	4.3@1.8	1.13@0.8	0.38@0.8	1.78@1	1.7@1.2
Active Area (mm^2)	0.025	0.54	1.16	0.3	0.7	0.559	0.4	0.85	0.2	0.45	0.7

* In-band IIP3 † Out-of-band IIP3
References:[1]Park & Kwon (2020), [2]Lin *et al.* (2014b), [3]Cai *et al.* (2020), [4]Kim & Kwon (2019), [5]Ramella *et al.* (2017), [6]Park & Kwon (2021), [7]Purushothaman *et al.* (2021), [8]Wang *et al.* (2018), [9]Silva-Pereira *et al.* (2018).

shows that a more uniform gain and NF can be obtained at the cost of added inductor die area. CRR2 exhibits more conversion gain and NF variations over its operating frequency range, and it has a lower frequency of operation, but it requires significantly reduced active area (the lowest reported in the table) which can be an advantage in some applications.

4.4 Conclusion

A low-power and wideband RF-to-BB current-reuse receiver front-end was fabricated in TSMC 130 nm CMOS technology. The current sharing of the TIA and LNTA reduces the power consumption significantly. Moreover, a CCCG LNTA topology boosts the transconductance without consuming extra power. An AI and $1/f$ NC technique enhances the receiver NF performance and RF bandwidth. The performance of the receiver front-end is verified with both an input differential balun without an on-chip inductor and an input LC balun with an on-chip inductor to demonstrate the robustness of the architecture. In fact, the receiver may be tuned for

different RF bands by changing the components of the matching network. The results show the receiver covers an RF band from 0.2 to 1 GHz and from 1 to 1.7 GHz with a differential balun and LC balun, respectively. This work shows that the proposed CRR is well-suited to different matching circuits over a wide RF range.

Author Contributions

Conceptualization, A.A. and F.N.; methodology, A.A.; software, A.A.; validation, A.A.; formal analysis, A.A.; investigation, A.A.; resources, A.A.; data curation, A.A.; writing—original draft preparation, A.A.; writing—review and editing, A.A. and F.N.; visualization, A.A.; supervision, A.A. and F.N.; project administration, A.A.; funding acquisition, F.N. All authors have read and agreed to the published version of the manuscript.

Acknowledgment

The author would like to thank CMC Microsystems for enabling chip fabrication and providing access to the EDA tools. Also, the authors thank Sequans Communications and its supportive team in both hardware platform and RFIC departments for providing laboratory equipment and technical support during the measurements.

Appendix: Proof of the AI Input Impedance

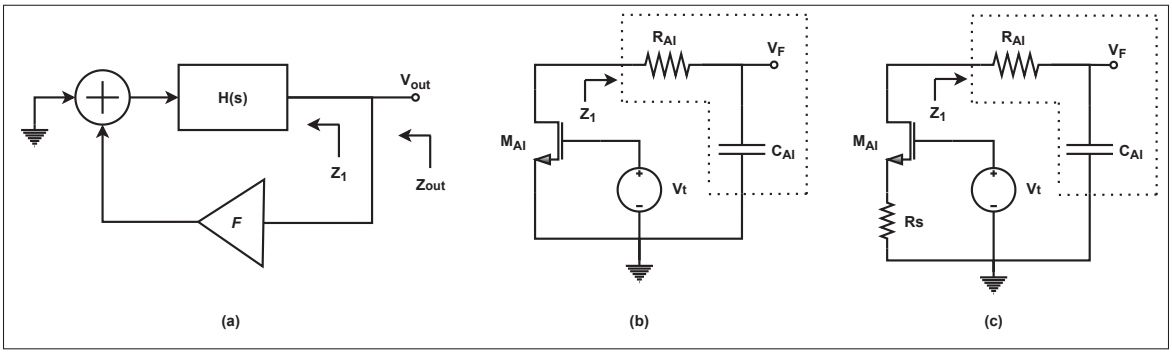

Figure 4.15 (a) Output impedance of a negative-feedback system. The open-loop circuit of (b) Figure 4.3(a) and (c) Figure 4.3(b).

The block diagram of a negative-feedback system when calculating the output impedance is shown in Figure 4.15(a). The feedback network, F, reduces the output impedance of Z_1 such that

$$Z_{out}(s) = \frac{Z_1}{1 + FH(s)}. \tag{4.7}$$

Hence, Z_{out} increases if $KH(s)$ reduces. This means $KH(s)$ with a low pass transfer function results an inductive output impedance.

The open-loop circuit of Figure 4.3(a) can be modeled as Figure 4.15(b). $H(s)$ is realized by first-order low-pass $R_{AI}C_{AI}$ filter and F by transistor M_{AI}. The impedance looking into the $R_{AI}C_{AI}$ filter, Z_1, is given by

$$Z_1(s) = R_{AI} + \frac{1}{C_{AI}s}. \tag{4.8}$$

Moreover, the loop-gain is calculated by

$$FH(s) = -\frac{V_F}{V_t} = \frac{g_m}{C_{AI}s}. \tag{4.9}$$

Finally, referring to (4.7), the output impedance, Z_{out}, is given by

$$Z_{out}(s) \cong \frac{\frac{R_{AI}C_{AI}s+1}{C_{AI}s}}{1 + \frac{g_m}{C_{AI}s}} = \frac{R_{AI}C_{AI}s + 1}{C_{AI}s + g_m}. \tag{4.10}$$

Accordingly, the inductive behavior of the active-inductor circuit is thus demonstrated, where at low frequency, the output impedance is $1/g_m$ and it increases with frequency to R_{AI} if $R_{AI} >> 1/g_m$.

Now, adding the source-degeneration resistor, R_s, to transistor M_{AI}, which is shown in Figure 4.15(c). The loop-gain is then calculated by

$$FH(s) = -\frac{V_F}{V_t} = \frac{g_m \frac{1}{C_{AI}s}}{1 + g_m R_s}. \tag{4.11}$$

Again from (4.7), the closed loop output impedance is calculated such that

$$Z_{out(withR_S)}(s) \cong \frac{g_{m,AI}R_S(R_{AI}C_{AI}s + 1) + R_{AI}C_{AI}s}{g_{m,AI}R_S C_{AI}s + g_{m,AI} + C_{AI}s}. \tag{4.12}$$

Appendix: Extension of Table 4.1

Table 4.2 shows more details in the performance comparison of the front-ends summarized previously in Table 4.1.

Table 4.2 Performance Summary and Comparison

Parameters	This Work CRR2 (Diff. balun)	This Work CRR1 (LC Balun)	TMTT 2020[1]	JSSC 2014[2]	JSSC 2014[3]	MWCL 2019[4]	JSSC 2017[5]	IEEE 2021[6]	JSSC 2021[7]	JSSC 2021[8]	JSSC 2018[9]	TMTT 2019[10]
Application	IoT	IoT	IoT	ZigBee	ZigBee	IoT	Bluetooth	BLE	IoT	IoT	ZigBee	BLE
Process node	130nm CMOS	130nm CMOS	65nm CMOS	65nm CMOS	65nm CMOS	65nm CMOS	28nm CMOS	65nm CMOS	28nm CMOS	28nm CMOS	65nm CMOS	130nm CMOS
F_{High} (GHz)	1	1.7	2.48	3.55	0.96	0.92	2.8	2.48	2.9	2.8	2.48	2.48
F_{Low} (GHz)	0.2	1	2.4	2.25	0.433	0.9	2	2.4	2.2	1.8	2.4	2.4
BB (MHz)	110	90	2	2	2	20	1.5	2	2	2	2	2
S11 (dB)	<-10	<-10	<-10	<-10	<-10	<-10	<-10	<-10	<-10	<-10	<-10	<-10
Gain (dB)	33-39.5	41.5	49.5	57	50	40.7	43.4	42	61	45	57.8	42
NF (dB)	6-10.5	6.5	8.2	8.5	8.1	1.94	7.8	13.2	5.5	6	15.7	7.2
IIP3 (dBm)	-21.5	-28.2	–25.75	-53	-45	-25.6	-20	-25	-46	-13	-18.5	-17
P_{DC}@V_{DD} (mW)	2@1.2	2@1.2	2.16@1.2	1@1.2	1.15@0.5	3.6@1.8	4.3@1.8	1.13@0.8	0.37@0.7	0.38@0.8	1.78@1	1.7@1.2
Area (mm^2)	0.025	0.54	1.16	0.3	0.2	0.559	0.4	0.85	0.5	0.2	0.45	0.7

References: [1] Park & Kwon (2020), [2] Lin *et al.* (2014b), [3] Lin *et al.* (2014c), [4] Kim & Kwon (2019), [5] Ramella *et al.* (2017), [6] Park & Kwon (2021), [7] Thijssen *et al.* (2020), [8] Purushothaman *et al.* (2021), [9] Wang *et al.* (2018), [10] Silva-Pereira *et al.* (2018).

CONCLUSION AND RECOMMENDATIONS

Summary

The objectives of this thesis were to study, design and characterize a low-power wideband receiver front-end and contribute a versatile design methodology. The first contribution of this work is a detailed design methodology that provides mathematical analysis, procedures and characterization of the proposed current-reuse receiver structure. In addition, layout design concerns are discussed. The second contribution, is the presentation of a wideband current-reuse receiver front-end design, along with its fabrication and experimental characterization. It features, for the first time, an active-inductor and $1/f$ noise-cancellation technique to allow the receiver to operate at higher frequencies despite the large technology node of 130 nm CMOS. The receiver includes a common-gate LNTA topology to provide wideband operation. The low-power consumption is achieved thanks to the current-reuse topology that allows current sharing of the TIA and LNTA circuits from a single supply. In addition, a cross-coupled technique used in the LNTA design boosts the transconductance by almost two times without consuming extra power. Finally, The third contribution is the presentation of the comparison between an off-chip differential balun and an LC balun for input matching, employing the same current-reuse receiver front-end with and without an on-chip inductor. This comparisons allows for the evaluation of the robustness and performance of the proposed front-end structure using different input matching networks and frequencies.

Contributions

The main contributions of the research work carried out and presented in this thesis by articles are as follows:

A Design Methodology for Wideband Current-Reuse Receiver Front-Ends Aimed at Low-Power Applications

This First contribution was published in a scientific journal: special issue "Design of Mixed Analog/Digital Circuits", section "Circuit and Signal Processing", Electronics, MDPI was presented in CHAPTER 2. It presents a design perspective on low-power and wideband RF-to-Baseband current-reuse receivers (CRRs) including design procedure, characterization and more depth into the design methodology.

A Wideband Low-Power RF-to-BB Current-Reuse Receiver using an Active Inductor and 1/f Noise-Cancellation for L-Band Applications

This second contribution was published in a scientific journal: IEEE Access was presented in CHAPTER 3. This work presents the design and fabrication of a novel wideband low-power RF-to-BB current-reuse receiver using an active inductor and 1/f noise-cancellation for L-band applications. Co-author Amirhossein Moshrefi contributed in the first chip validation check and logistics required to carry out follow-on validation required to complete this manuscript.

A Comparison of off-chip Differential and LC input matching balun in a wideband and Low-Power RF-to-BB Current-Reuse Receiver Front-End

This third contribution was published in a scientific journal: Electronics, MDPI was presented in CHAPTER 4. This work provides a comparison of off-chip differential balun and LC-Balun using an on-chip inductor in a widenabd and low-power RF-to-BB current-reuse receiver front-end.

Recommendations

In order to continue the work started during this thesis, several recommendations can be made. This can notably allow the design to attain an even wider bandwidth of operation.

There are several performance metrics such as noise figure, power consumption, bandwidth, linearity and integration of external components that need to be addressed. The main focus of this work leading to its contributions was to design a low-power and wideband receiver that was achieved by the current-reuse topology that stacks TIA and LNTA to share biasing current from a single supply. In addition, the cross-coupled common-gate LNTA helps to reduce power consumption by half. The overall NF performance was improved using an active-inductor and $1/f$ noise-cancellation technique. The first set of recommendations is to design the proposed circuit using a smaller technology node to compare the performance and determine the technology scaling benefit of the proposed architecture. In fact, one of the reasons that degrades the NF is large parasitic contribution at the output of the LNTA that is due to the technology node. Moreover, metal-insulator-metal and MOSFET capacitors are used instead of metal-oxide-metal capacitors since these were not available in the design kit of this technology node. This increased area and reduced the overall performance achievable. A more modern node can give access to these capacitor structures to enhance performance.

The second set of recommendations is related to the input matching circuits and LNTA topology employed in this work. It is very important to reduce the number of external components by utilizing an on-chip balun to convert the single-ended signal to a differential signal. This may consume more chip area however. To reduce the area consumption of added on-chip matching elements, a common-gate and common-source LNTA topology can be used at the cost of an imbalanced output.

The third set of recommendations relates to the out-of-band linearity performance that is significant if a blocker signal's frequency is close to the wanted signal frequency. The current-reuse receiver proposed in this work operates in current-mode. A current-mode filter may help to suppress the out-of-band blockers right after the passive mixer output. The usage

of current-mode filter was proposed in conventional receiver architectures Silva-Pereira *et al.* (2018); Abdulaziz, Klumperink, Nauta & Sjöland (2018).

Finally, the fourth set of recommendations relates to the measurement setup. An on-chip CML buffer circuit and differential to single-ended balun were used to provide the output matching to the spectrum analyzer. In fact, the on-chip CML buffer circuit may contribute to the non-idealities pertaining to metrics such as linearity. This effect is not easy to distinguish from the overall performance of the actual receiver front-end. Another way to provide the output matching would be to design a buffer on the PCB with 50 Ω single-ended output and high impedance input where the receiver output can be connected directly. This helps to characterize the circuit more accurately.

Academic Publications

During this doctorate, several academic publications were obtained. They are listed below.

1. "A low-power wideband receiver front-end for NB-IoT applications" by Abbasi, A., Shams, N.,& Nabki, F. Presented at 18th IEEE International New Circuits and Systems Conference (NEWCAS) 2020.
2. "A 6 GHz 130 nm cmos harmonic recombination rf receiver front-end using n-path filtering" by Shams, N., Abbasi, A., & Nabki, F. Presented at 18th IEEE International New Circuits and Systems Conference (NEWCAS) 2020. (**Invited to publish the extended version in IEEE TCAS I**)
3. "A 3.5 GHz to 7 GHz wideband differential LNA with gm-enhancement for 5G applications" by Shams, N., Abbasi, A., & Nabki, F. Presented at 18th IEEE International New Circuits and Systems Conference (NEWCAS) 2020.
4. "A 0.8-3.4 GHz, low-power and low-noise RF-to-BB-Current-Reuse receiver front-end for wideband local and wide-area IoT applications" by Abbasi, A., Shams, N.,& Nabki,

F. Presented at 27th IEEE International Conference on Electronics, Circuits and Systems (ICECS) 2020.

5. "A Wideband Low-Power Current-Reuse RF-to-BB Receiver Using a Clock Strategy Technique" by Abbasi, A., Moshrefi, A.,& Nabki, F. Presented at 20th IEEE International New Circuits and Systems Conference (NEWCAS) 2022. (**Invited to publish the extended version in IEEE TCAS I**)
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7. "A Wideband Low-Power RF-to-BB Current-Reuse Receiver using an Active Inductor and 1/f Noise-Cancellation for L-Band Applications" by Abbasi, A., Moshrefi, A. & Nabki, F. Published in special issue "Design of Mixed Analog/Digital Circuits", section "Circuit and Signal Processing", IEEEAccess, IEEE 2022.
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