Low Power Agile Wideband RF CMOS Front-Ends for 5G, Wi-Fi 6E and Impulse Radio Applications

by

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Circuits CMOS RF large bande agiles à faible consommation pour les applications de la 5G, du Wi-Fi 6E et de la radio impulsionnelle.

Nakisa SHAMS

RÉSUMÉ

Les années 2020 appartiennent à la cinquième génération, la 5G, c'est-à-dire une nouvelle norme radio (NR), qui est considérée comme une évolution remarquable par rapport aux systèmes de communication actuels et qui peut être configurée de manière flexible pour divers scénarios d'application. Ainsi, nos vies seront affectées par la 5G de manière plus spectaculaire que tout autre changement technologique, car elle nous mène vers un monde entièrement connecté. La 5G, qui utilise la bande de fréquences sub-6 GHz et le spectre des ondes millimétriques (mm-Wave) avec d'autres technologies RF comme les radios à bande ultra-large (UWB), fournira de multiples services.

Alors que la 5G NR est passée de l'état de concept à celui de réalité, la norme Wi-Fi s'est développée en parallèle pour rester au niveau de la norme cellulaire et offrir de meilleures performances et un débit plus élevé. Récemment, l'organisation IEEE a créé un nouveau groupe de travail, le Wi-Fi 6E ou IEEE 802.11ax, pour étudier et réaliser les technologies Wi-Fi de nouvelle génération. Wi-Fi 6E fait référence à l'ensemble des dispositifs Wi-Fi, fournit des débits gigabit avec des performances plus élevées, des débits de données plus rapides et une latence plus faible, et complète le déploiement des réseaux 5G pour fournir une connectivité à l'intérieur, où la 5G NR est beaucoup moins efficace. Le Wi-Fi 6E a été étendu à la bande 6 GHz, offrant une augmentation considérable de la bande passante disponible. Cependant, sa dissipation d'énergie relativement élevée pose des problèmes à l'adoption du Wi-Fi pour les plateformes à faible consommation, telles que les dispositifs de l'Internet des objets (IoT) et les nœuds de capteurs sans fil. Les prévisions d'un grand nombre d'appareils connectés d'ici 2030 et la réalisation de la 5G et de la Wi-Fi 6E entraînent le besoin de techniques au niveau des circuits pour atténuer les interférences croissantes liées à ce nombre croissant d'appareils.

À cette fin, ce travail se concentre sur les techniques de conception pour fournir des architectures frontales de récepteur RF hautement résistantes aux interférences, de manière économe en énergie et fonctionnant dans une large gamme de fréquences RF d'entrée. Tout d'abord, une revue de la littérature est présentée. Elle se concentre sur les circuits frontaux des récepteurs RF, leurs circuits au niveau des transistors et leurs spécifications. Dans la deuxième partie de cette thèse, nous démontrons trois récepteurs RF utilisant une configuration de commutation à 4, 8 et 16 chemins qui permettent la sélection de la troisième harmonique de la fréquence de l'oscillateur local (LO), et qui suppriment efficacement les autres harmoniques afin de réduire la fréquence d'entrée et la consommation d'énergie du générateur d'horloge multiphase dans des bandes de fréquences RF plus élevées.

En considérant les défis de conception liés au filtre de commutation à N chemins, y compris le nombre de commutateurs, la consommation énergétique du circuit de génération des phases du LO et la performance de bruit, il est démontré qu'un système de filtre de commutation à 8

chemins est préférable pour fournir un compromis approprié entre les effets de repli harmonique, la mesuresbruit, la surface du circuit et la consommation d'énergie. Ainsi, la troisième partie de cette thèse démontre un récepteur RF à sélection d'harmoniques tolérant aux bloqueurs qui peut être reconfiguré pour sélectionner les premières et troisièmes harmoniques de la fréquence de commutation dans les bandes de fréquences basses et hautes, respectivement. Nous présentons un circuit intégré de preuve de concept en technologie CMOS 130 nm. Nous présentons un circuit intégré de preuve de concept dans un processus de technologie CMOS et nous présentons les résultats de mesures.

De fortes interférences hors bande (OOB) ou des bloqueurs indésirables peuvent désensibiliser un récepteur. Pour améliorer la résilience aux bloqueurs, le circuit frontal RF doit éviter l'amplification aux fréquences des bloqueurs au niveau du nœud d'entrée du récepteur. Pour ce faire, deux architectures différentes de récepteurs RF à large bande et antibruit sont présentées. Elles sont capables de tolérer les bloqueurs d'harmoniques LO sans sacrifier les performances en matière de bruit et en éliminant les pré-filtres SAW tout en consommant peu d'énergie d'horloge. Les résultats de mesure des prototypes de circuits intégrés en CMOS 65 nm confirment les avantages de nos techniques.

La dissipation d'énergie étant toujours importante pour les dispositifs de communication à large bande, il est possible d'économiser davantage d'énergie en exploitant une architecture IR-UWB à conversion directe auto-démodulante. À cette fin, cette thèse décrit l'étude, la conception, la fabrication et la caractérisation d'une électronique frontale IR-UWB non cohérent à double bande reconfigurable. Le récepteur IR-UWB multi-bandes proposé peut être reconfiguré numériquement dans différents modes de fréquence de fonctionnement, et est capable de supporter des données modulées en modulation par déplacement de fréquence binaire (FSK) en plus de la modulation tout-ou-rien (OOK), et permet de tirer parti de la signalisation ternaire en combinant les modulations OOK et FSK. Enfin, une méthodologie de conception détaillée est proposée, les résultats de mesure du récepteur fabriqué en technologie CMOS TSMC 130 nm et des discussions sont présentées.

Les techniques présentées permettront sans aucun doute le développement de nouvelles applications et contribueront ainsi à l'avancement des connaissances scientifiques sur les récepteurs frontaux à large bande RF.

Mots-clés: Récepteur, sélection des harmoniques, suppression du bruit, IR-UWB, reconfigurable.

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ABSTRACT

The 2020s belong to the fifth generation, 5G, that is a new radio (NR) standard, which is considered an outstanding evolution over the current communication systems and can be flexibly configured for various application scenarios. Thus, our lives will be affected by 5G more dramatically than any other technology shift since it will lead us to a fully connected world. 5G using sub-6 GHz frequency band and millimeter wave (mm-Wave) spectrum together with other RF technologies like ultra-wideband (UWB) will provide multiple services.

As 5G NR transitioned from concept to reality, Wi-Fi has been the developing standard in parallel to keep it at par with the cellular standard providing better performance and higher throughput. Recently, the IEEE introduced a new task group, i.e., the Wi-Fi 6E or IEEE 802.11ax, to investigate and realize next-generation Wi-Fi technologies. Wi-Fi 6E refers to the set of Wi-Fi devices, provides gigabit throughputs with higher performance, faster data rates, and lower latency, and complements the deployment of 5G networks to provide connectivity indoors, where 5G NR is far less effective. Wi-Fi 6E was extended into the 6 GHz band, offering considerable increases in available bandwidth. However, its relatively high power dissipation poses challenges for Wi-Fi being adopted for low power platforms, such as Internet-of-Things (IoT) devices and wireless sensor nodes. Forecasts of numerous connected devices by 2030 and the realization of 5G and Wi-Fi 6E drive the need for circuit-level techniques to alleviate the increasing interference coming with this growing number of devices.

To this end, this work focuses on design techniques to provide highly interference resilient RF receiver front-end architectures in a power efficient manner and operating in a wide range of input RF frequencies. First, a literature review is presented. It focuses on the RF receiver front-ends, their transistor-level circuit, and their specifications. In the second part of this dissertation, we demonstrate three wideband RF receivers using a 4-, 8-, and 16-path switching configuration that allows for the selection of the third harmonic of the local oscillator (LO) frequency, and that effectively suppresses other harmonics to reduce the input frequency and power consumption of the multi-phase clock generator at higher RF frequency bands of operation.

When considering the design challenges related to the N-path switching filter, including the number of switches, power consumption of the LO phases generation circuitry, and noise performance, it is shown that an 8-path switching filter system is preferred to provide a suitable trade-off between the harmonic fold back effects, noise figure, circuit area, and power consumption. Thus, the third part of this dissertation demonstrates a blocker-tolerant harmonic selection wideband RF receiver that can be reconfigured to select the first and third harmonics of the switching frequency at the low and high frequency bands, respectively. We present a proof of concept integrated circuit in 130 nm CMOS technology process and present the measurement results.

Strong out-of-band (OOB) interference or undesired blockers can desensitize a receiver. To enhance resilience to the blockers, the RF front-end must avoid amplification at blocker frequencies at the input node of the receiver. To do this, two different wideband noise-cancelling wideband RF receiver architectures are then presented that have the capability of tolerating the LO harmonic blockers without sacrificing noise performance and alleviating the SAW pre-filters requirement while consuming low clocking power consumption. Measurement results from the integrated circuit prototypes in 65 nm CMOS confirm our techniques' benefits.

Since power dissipation is always important for wideband communication devices, more power can be saved by exploiting a self-demodulating direct conversion impulse radio UWB (IR-UWB) architecture. To this end, this dissertation describes the study, design, fabrication, and characterization of a reconfigurable dual-band non-coherent wideband IR-UWB front-end. The proposed multi-band IR-UWB receiver can be digitally reconfigured in different operating frequency modes, and is able to support data modulated in binary frequency shift keying (FSK) in addition to on-off keying (OOK), and allows for the leveraging of ternary signaling by combining both OOK and FSK modulations. Ultimately, a detailed design methodology and measurement results of the fabricated receiver in TSMC 130 nm CMOS technology are presented.

The presented techniques will undoubtedly allow the development of new applications, and will thus contribute to the scientific knowledge advancement on RF wideband receiver front-ends.

Keywords: Wideband, Wireless, Receiver, Harmonic Selection, Noise-Cancelling, Ultra wideband, Impulse radio, Reconfigurable.

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LIST OF ABREVIATIONS

ADC	Analog to Digital Converter
AWG	Arbitrary Waveform Generator
BB	Baseband
BER	Bit Error Rate
BPF	Band-Pass Filter
CCC	Capacitive Cross Coupling
CCD	Critical Current Detection
CG	Common Gate
CS	Common source
D-MPPM	Digitalized Multi-pulse Position Modulation
FCC	Federal Communications Commission
FSK	Frequency Shift Keying
IIP3	Input Third Order Intercept Point
IM3	Third Order Intermodulation
IR	Image Rejection
IoT	Internet of Things
IR-UWB	Impulse Radio Ultra Wide Band
HRM	Harmonic-Rejection Mixer
HRR	Harmonic Rejection Ratio

LNA	Low Noise Amplifier
LO	Local Oscillator
LVDS	Low Voltage Differential Signaling
LPF	Low Pass Filter
NF	Noise Figure
OOB	Out-Of-Band
OOK	On-Off Keying
PCB	Printed-Circuit-Board
PLL	Phase-Locked Loop
PVD	Peak Voltage Detector
PHY	Physical Layer
PGA	Programmable Gain Amplifier
PPM	Pulse Position Modulation
PVT	Process-Voltage-Temperature
RF AMP	Radio Frequency Amplifier
SAW	Surface-Acoustic-Wave
SRO	Super Regenerative Oscillator
SRR	Super Regenerative Receiver
TCA	Transconductance Amplifier
TDC	Time-to-Digital Converter

TIA	Transimpedance Amplifier
VCO	Voltage Controlled Oscillator
VNA	Vector Network Analyzer

LIST OF SYMBOLS AND UNITS OF MEASUREMENTS

Ω	Ohm
F	Farad
Hz	Hertz
m	meter
Q	Quality factor
s	second
V	Volt
W	Watt

INTRODUCTION

The 2020s belong to 5G radio, the fifth generation cellular radio standard, according to the ongoing trend of wireless mobile telecommunications technology that has evolved since the 1980s. It is expected that 5G will provide a various range of services from enhanced mobile broadband at multi-Gb/s, to the massive Internet of Things (IoT) revolution. That is why the new radio (NR) term was coined for 5G as it employs denser modulation schemes and pairs with current technologies to meet the ever-increasing demand for communication networks. A 5G system can support large bandwidth, wide connectivity, low latency, and support the IoT paradigm that has expended in recent years. The transition to 5G from LTE is much faster than the transition to 4G from 3G as technologies have rapidly advanced, (Fig. 0.1 illustrates this). All generations up to 4G are used below the 3 GHz frequency spectrum, while 5G is expected to support a wide spectrum range, ranging from low-bands from 0.45 −6 GHz and millimeter wave (mm-Wave) bands greater than 24 GHz.

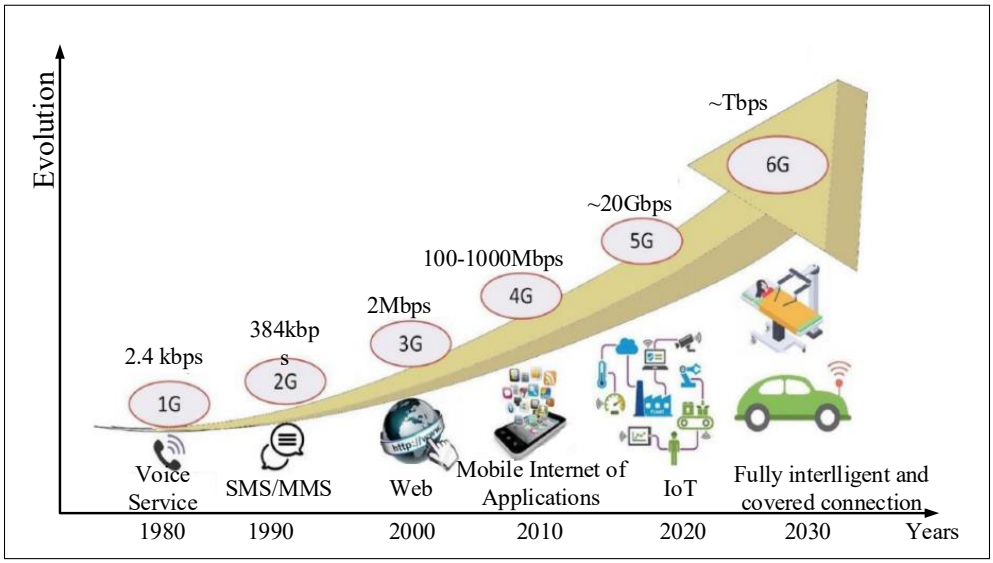

Figure 0.1 Evolution of communication systems
Extracted from Lin & Lee (2021); Sheikh & Babul (2020)

The sub-6 GHz and millimeter wave (mm-Wave) bands aim in part to solve spectrum congestion in 5G wireless systems that are low in cost, highly reliable, and compact (Lee, Han, Lee, Kang, Bae, Jang, Oh, Chang, Kang, Son et al. (2019b)). As the sub-6 GHz frequency band allows for power efficient and simpler designs to implement 5G systems, as opposed to the mm-Wave band, this puts a strain on developing the RF front-end designs that leverage new architectures to meet the 5G specifications within a wide band.

In addition to mobile telecommunications technology, Wi-Fi (IEEE 802.11 a/g/n/ac/ax) is the most common Internet access technology and has had considerable success in deploying IoT networks in outdoor and indoor environments during the last decade. This evolution has led to many different standards depicted in Fig. 0.2. Wi-Fi can operate on an unlicensed spectrum, as opposed to 5G. Despite achieving great success in mobile, business, research, daily usage, etc, the existing Wi-Fi standard does not provide enough network access performance for all IoT devices with different service requirements. Thus recently, the IEEE introduced a new task group, i.e., Wi-Fi 6 or IEEE 802.11ax, to investigate and realize next-generation Wi-Fi technologies for dense IoT networks' scenarios with large data traffic (Chen, Li, Balasubramaniam, Wu, Zhang & Wan (2020); López-Pérez, Garcia-Rodriguez, Galati-Giordano, Kasslin & Doppler (2019); Maldonado, Karstensen, Pocovi, Esswie, Rosa, Alanen, Kasslin & Kolding (2021)). In addition for the first time in several years, the FCC proposed several rules to provide more spectrum available for unlicensed usage in the $5.925-7.125$ GHz band (a.k.a. 6 GHz band). This spectrum was deemed suitable for Wi-Fi expansion because of its proximity to the existing Wi-Fi bands (2.4 GHz and 5 GHz). Moreover, this new opportunity offers wider channels that enable higher throuput and latency properties for new Wi-Fi 6 (802.11ax standard). Moreover, it ensures that licensed services and devices operating in the band continue on thriving.

The introduction of the 5G NR standard has imposed several challenges in the sub-6GHz receivers' design. The maximum channel bandwidth increases to 100 MHz, while a -15 dBm

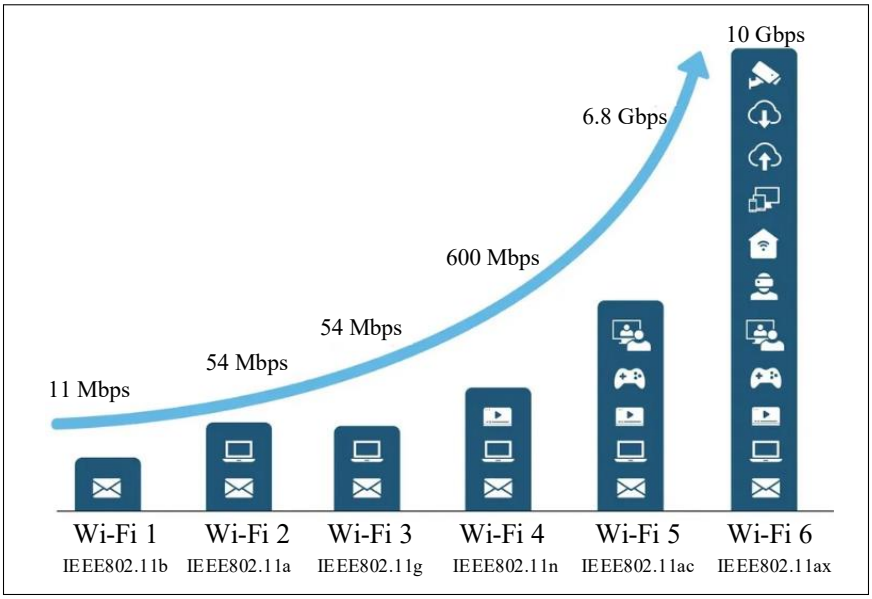

Figure 0.2 The evolution of Wi-Fi Standards
Taken from Chauhan *et al.* (2021); Sun *et al.* (2014)

continuous-wave blocker can only be placed $\Delta f = 85\,\text{MHz}$ away from the desired band edge. A small $\frac{\Delta_f}{BW}$ places a stringent linearity requirement on a receiver, thus demanding higher-order filtering. Moreover, a low noise figure is required to achieve the highest possible sensitivity and link budget, allowing to maximize data rates and range, along with spectral efficiency. In addition, since the desired band may contain many signals resulting from the digital beam-forming operation and carrier aggregation, in-band (IB) linearity also becomes critical.

Moreover, the demand for highly integrated receivers has driven the development of blocker-tolerant systems based on widely tunable filters. The recent CMOS receivers employ bulk acoustic wave (BAW) filters and high-Q surface acoustic wave (SAW) to suppress large out-of-band (OOB) blockers in a conventional narrow-band receiver design (Hasan, Gu & Liu (2016)). To cover different frequency bands, multiple BAW/SAW filters are necessary, which increases the form factor and cost. The RF filtering elimination is challenging because of the reciprocal mixing and gain compression. To reduce the size and cost of the transceiver, multiple narrow-band receivers can be replaced by a widely tunable receiver or wideband receiver. On the other

hand, a wideband receiver passes the desired signal and undesired blockers/OOB interference since it has no selectivity. The blockers might be placed very close to the desired frequency channels, thus it is difficult to maintain a high dynamic range in the presence of large blockers (Bu, Hameed & Pamarti (2020); Han & Kinget (2021); Murphy, Darabi & Xu (2015); Wu, Mikhemar, Murphy, Darabi & Chang (2015)). In addition, a 0-dBm blocker can clip the low noise amplifier (LNA) due to the low supply voltage in the modern CMOS process (e.g., 1 V). As a result, the wideband receiver, while sought after to simplify the radio system architecture, experiences high noise and distortion, leading to deteriorated performance. Therefore, the challenge lies in designing a wideband receiver architecture to improve its blocker-tolerance without sacrificing area and power consumption.

Accordingly, this dissertation attempts to provide some solutions for several of the problems described thus far by exploiting N-path switching filter based blocker tolerant wideband RF receiver front-ends to enhance resilience to undesired blockers and out of band (OOB) interference. The three different receiver front-end integrated circuits (ICs) demonstrated in this dissertation target sub-6 GHz applications that cover 5G, Wi-Fi and IR-UWB. The implemented RF wideband receivers employ fully-differential architectures that are able to tolerate harmonic local oscillator (LO) blockers without sacrificing noise performance and to alleviate the SAW pre-filters requirement while allowing for low-power LO clock generation.

Note that N-path switching filters used in the proposed RF wideband receivers are driven by an N-phase LO clock generator. As the number of paths, N, in the N-path switching filter and/or the operating frequency increases, the dynamic power consumption of the LO clock generation increases in a linear fashion. Since driving the switches of the 8-phase mixer beyond 3 GHz significantly increases the dynamic power consumption, even in smaller CMOS technologies, there is a need to design a receiver architecture to save the dynamic power by relaxing the requirements of the clock generator, phase-locked loop (PLL) and oscillator. Thus, this dissertation

also presents a more agile design through a differential reconfigurable multi-band non-coherent impulse radio ultra-wideband (IR-UWB) receiver. Since the proposed IR-UWB architecture employs a self-demodulating direct conversion RF front-end structure, it avoids using frequency translation blocks like a down-conversion mixer, a PLL and an oscillator. Among all techniques and architectures employed for multi-standard wireless systems, IR-UWB has gained much attention because of its potential for low power implementations. The use of IR-UWB technology in designing and implementing energy efficient RF receiver front-end for short range communications is another main subject of this dissertation.

Research objectives

This doctoral thesis aims to present the work carried out over the past five years. This work focuses on the design and characterization of wideband RF receiver structures for next generation radio, 6 GHz Wi-Fi and IR-UWB. This research will enable future RF and analog designers to have a better understanding of these RF receivers, and therefore to improve the performance of tomorrow's wideband RF front-ends. To achieve this objective and with the aim of building a complete receiver front-end, different sub-objectives have been identified, which are:

- establish clear and simple receiver design methods at the system and transistor levels,
- propose design methods or structures for wideband RF receivers supporting higher frequency RF inputs beyond 3 GHz, while consuming low LO power compared to the conventional architectures,
- propose design methods or structures that increase the performance of wideband receivers over the entire frequency band of operation,
- design an IR-UWB architecture supporting data modulated in binary frequency shift keying (FSK) in addition to on-off keying (OOK) modulation scheme, for enhanced robustness, and

- propose design methods or structures providing robustness to process variations and mismatches.

The main contributions of the research work are as follows:

1. **A new architecture for wideband RF receiver operating at third order harmonic of the switching frequency rather than the fundamental to reduce the input frequency and power consumption of the multi-phase clock generator by a factor of three**

2. **A harmonic selective RF receiver to select a first and third harmonic of switching frequency and to efficiently suppress blockers at LO harmonics together with suppressing near-band blockers**

3. **A new filtering characteristic at the RF input node of the front-end by using differential first and third harmonic selection N-path filters (HS-NPF) to prevent the blockers from experiencing significant voltage gain**

4. **A new RF receiver structure exploiting a noise-canceling technique and** 1^{st} **and** 3^{rd}**-order LO harmonic selection at low and high frequency bands, respectively**

5. **A multi-band IR-UWB non-coherent receiver that can be digitally reconfigured in different operating frequency modes. This receiver includes a self-demodulating direct conversion front-end architecture supporting an on-off keying (OOK) modulation scheme, in addition to data modulated in binary frequency shift keying (FSK) for enhanced robustness, and supporting ternary signaling**

While the four different RF receiver front-ends presented in this thesis contribute key innovations towards greater front-end integration, they obviously provide only a small portion of the possible research areas in the broader space of wideband receivers.

Thesis Organization

This dissertation attempts to provide some solutions to several of the problems described, by building a reconfigurable dual-band non-coherent IR-UWB receiver, in addition to N-path filter based blocker tolerant inductor-less harmonic selection RF receiver front-ends. The four different RF receiver front-end ICs demonstrated in this dissertation target three different application thrusts: one front-end targeting sub-6 GHz 5G applications, two front-ends for sub-6 GHz 5G and 6 GHz Wi-Fi applications, and one targeting IR-UWB systems.

Chapter 1 presents a literature review of wideband receiver architectures. Its main objective is to give an overview of what a wideband RF receiver front-end is and to describe some of the recent reported structures: a wideband RF receiver using discrete-time analog filtering, a receiver using switching mixers, receivers based on N-path filtering, and IR-UWB receiver architectures including coherent and non-coherent architectures.

Chapter 2 presents the proposed RF front-end receiver configuration that allows for the selection of the third harmonic of the LO frequency, and that effectively suppresses other harmonics to reduce clocking power consumption at higher RF frequency bands of operation. Notably, the use of an N-path switching filter is mathematically analyzed to demonstrate how the harmonic recombination stage is reconfigured at the baseband to select the third harmonic of the LO switching frequency rather than the fundamental to reduce the input frequency and power consumption of the multi-phase clock generator by a factor of three. Moreover, the chapter further expands on three RF receiver front-ends using a 4-, 8-, and 16-path switching configuration and harmonic recombination at the baseband. Post-layout simulation results of these front-ends in TSMC 65 nm CMOS technology are used to fully expose the trade-offs of the proposed architecture. In addition, the simulated post-layout performance of the 4-, 8-, and 16-path third harmonic selection receivers is compared to a conventional architecture to provide a fair comparison to the performance metrics of the proposed architecture.

Chapter 3 presents the fabricated harmonic selection receiver front-end to support the $5G$ sub-6 GHz band. A $0.5-6$ GHz harmonic selective RF receiver front-end exploiting wideband inductor-less LNA, 8-path switching filter and BB 1^{st} and 3^{rd} harmonic recombination blocks has been designed and verified in 130 nm TSMC CMOS technology. It is demonstrated how the baseband harmonic recombination stage can be reconfigured to select the first harmonic of the switching frequency at the low frequency band ($0.5-1.9$ GHz) and the third LO harmonic at the high frequency band ($1.95-6$ GHz). Based on harmonic selectivity, the proposed wideband receiver achieves blocker tolerance and harmonic rejection while consuming substantially less power, compared to the existing architectures operating at such high frequencies.

Chapter 4 extends the work on the harmonic selection receiver of Chapter 3 by demonstrating two wideband harmonic selection noise-canceling (HS-NC) RF receiver front-ends for 5G and Wi-Fi 6. Two proposed RF receiver architectures employ two harmonic rejection N-path filters with resistive coefficients and frequency translational noise cancellation (FTNC) technique to enhance resilience to the harmonic LO blockers and to achieve low noise. Since driving the switches of the N-path switching system beyond 3 GHz increases the power consumption significantly, the proposed HS-NC architectures are configured to select the 1^{st} and 3^{rd}-order LO harmonic at the low frequency band ($0.5-2.4$ GHz) and high frequency band ($2.4-7.2$ GHz), respectively. An IC prototype of both front-ends is fabricated in TSMC 65 nm CMOS as a proof-of-concept and it is characterized. The front-ends, capable of operation from $0.5-7.2$ GHz, show a minimum in-band NF of 3.4 dB at a 80 MHz BB frequency.

Finally, Chapter 5 focuses on building an OOK and binary FSK reconfigurable dual-band non-coherent IR-UWB receiver supporting ternary signaling. It can be digitally reconfigured in different operating frequency modes, including two single-band modes and one concurrent dual-band mode. The proposed receiver employs a self-demodulating direct conversion RF front-end architecture with OOK modulation scheme. Moreover, the proposed reconfigurable receiver

architecture supports data modulated in binary FSK in addition to OOK for enhanced robustness. It also uniquely supports ternary signaling by combining both OOK and FSK modulations. The receiver was fabricated in TSMC 130 nm CMOS technology and is characterized. The proposed receiver has the capability of decoding the frequency information of the received pulse at a 100 Mbps data rate in OOK or binary FSK, or 150 Mbps by leveraging ternary signaling in the concurrent dual-band mode, hence improving power efficiency.

Finally, this manuscript ends with a conclusion covering the whole of this thesis and summarizes the key contributions of this dissertation. It also presents different avenues for future research to build on the work done in the course of this doctorate.

CHAPTER 1

LITERATURE REVIEW

This chapter presents a brief review of the work done by various researchers on wideband RF front-end architectures. The receivers have been analysed based on their performances, as well as the benefits and the drawbacks of using these receivers.

1.1 Wideband RF Receiver Front-End Architectures

The narrow-band receiver front-ends invariably use external RF filtering to prevent the large OOB signals from corrupting the desired signal. Since RF filters are almost fixed, multiple receivers are required to support the large number of frequency bands serviced by a modern wireless devices. Compared to narrow-band receivers, wideband receivers that are tunable over the entire frequency band of interest can be employed. Wideband receivers offer great reconfigurability and flexibility. However, since there is no off-chip surface-acoustic-wave (SAW) filtering available, any blocker and interferer along with the desired signal can corrupt the reception. Thus, it has prevented the commercial adoption and wideband structures. To enable a wideband front-end into commercialization, one must improve its tolerance in the presence of blocker signals in order to be competitive with narrow-band receivers. Accordingly, there has been a growing interest in blocker-tolerant wideband receiver architectures without resulting in a significant increase in power consumption or occupied chip area (Murphy, Darabi, Abidi, Hafez, Mirzaei, Mikhemar & Chang (2012); Wu *et al.* (2015)).

1.1.1 Wideband RF receiver using discrete-time analog filtering

Typically, the RF signal can be down-converted to the IF or baseband by using either sampling or mixing. Based on sampling theory, down-conversion can be realized by sampling of an RF signal on a capacitor, as utilized in discrete-time approaches that employ switched-capacitor techniques (Fig. 1.1(a)) (Chen & Hashemi; Tohidian, Madadi & Staszewski (2014)). Down-conversion by using discrete-time mixers provides programmability in the center frequency of

the receiver, while the order of the filters and the bandwidth are controlled by selecting the number of charge sharing phases and proper down-sampling rate, respectively. In addition, there is a need for digital filtering and oversampling to reduce the gain at the harmonics. In the digital domain, high harmonic rejection is achieved by using a high sampling rate (Tohidian *et al.* (2014)). However, discrete-time approaches suffers from the limited linearity caused by the first sampling stage that usually is composed of an LNA.

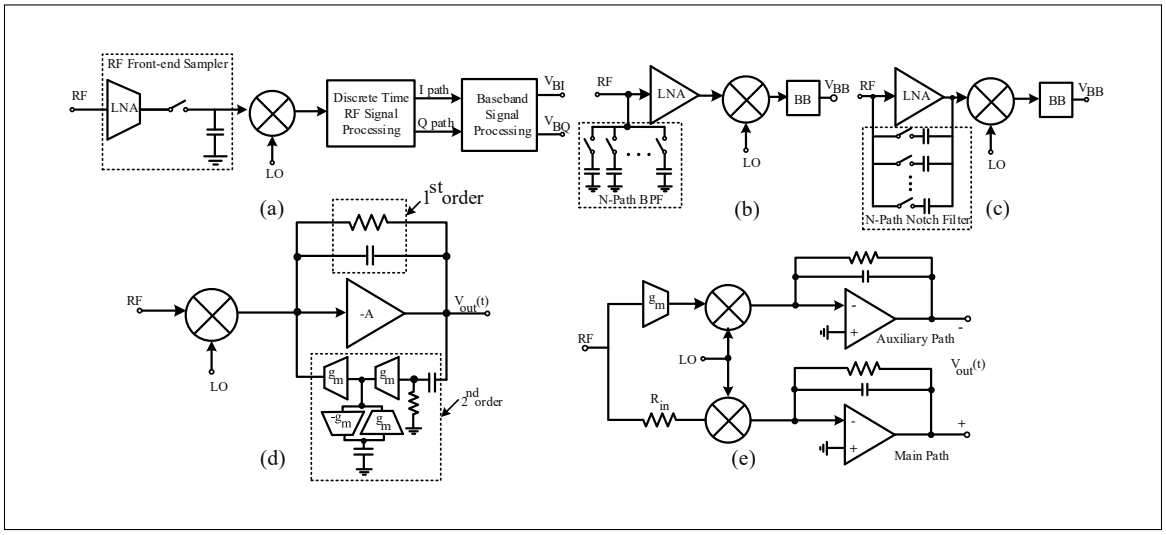

Figure 1.1 Prior art in receivers. (a) Discrete-time (DT) RF signal processing (taken from Chen & Hashemi), (b) receiver based on the N-path band path filters (taken from Darvishi *et al.* (2013a); Luo *et al.* (2016)), (c)receiver based on the notch filters, (d) Mixer-first architectures (taken from Andrews & Molnar (2010); Lin *et al.* (2014)), and (e) Noise cancellation structures (taken from Murphy *et al.* (2012))

1.1.2 Wideband RF receiver using switching mixers

RF signal down-conversion can also be realized by switching mixers (sampling mixers) that multiply the RF signal and a square-wave LO waveform. Since the LO waveform is not a pure sine-wave and contains undesired harmonics, mixing the RF signal with a square wave down-converts both the desired signal located around the LO frequency and the signals located around the LO harmonics. An RF band-selection filter mitigates this harmonic mixing in narrow-band receivers. An alternative approach is to employ harmonic-rejection mixers (HRM) in order

to cancel the need for a discrete IF filter and to limit spurious mixing in receivers. By providing frequency-synthesis, HRMs can be employed in broadband receivers such as proposed in Ho, Singh, Forbes & Gharpurey (2014); Singh, Forbes, Ho, Ko & Gharpurey (2014); Wu, Murphy & Darabi (2019).

The first harmonic-rejection principle proposed in Weldon, Narayanaswami, Rudell, Lin, Otsuka, Dedieu, Tee, Tsai, Lee & Gray (2001) used the gain coefficients at the RF part of the circuit, while the use of the harmonic-rejection coefficients at the baseband analog-domain was described in Molnar, Lu, Lanzisera, Cook & Pister (2004). The proposed HRM in Weldon *et al.* (2001) includes three parallel mixing paths with gain ratios of $1 : \sqrt{2} : 1$. Three weighted current outputs are summed to approximate a sine-wave LO that includes only the $8m \pm 1$ harmonics of the fundamental frequency of f_{LO}, where m is an integer. In this fashion, the 3^{rd} and 5^{th} harmonics can be rejected. Higher harmonic rejection can be achieved by accurately implementing the desired weighting ratio $1 : \sqrt{2}$ on chip. Realizing an accurate ratio and handling the random variations because of circuit mismatches are two challenges of this approach.

To address these issues, an analog two-stage poly-phase harmonic rejection (HR) filter can be implemented on chip (Ru, Moseley, Klumperink & Nauta (2009)). Figure 1.2 shows wideband receiver architecture proposed in Ru *et al.* (2009). For the differential transconductance LNA section, the receiver entails two off-chip inductors and one off-chip transformer. An 8-path passive mixer in current-driven mode is used for down-conversion (Figure 1.2(a)). The 8-phase 12.5 % duty cycle clock generation with a high phase accuracy ($<0.07^o$ at 0.8 GHz) is generated by using a divide-by-8 circuit. Transimpedance amplifiers (TIAs) realize the baseband (BB) low-pass filters (LPFs). This structure acts as a frequency-translated RF-to-BB LNA, with the frequency-translated BB-to-RF virtual ground, which absorbs both the out-band signal and in-of-band interferers. The channel selection and signal amplification are done at BB, thus resulting in high linearity. Although it offers higher HR, well above 60 dB, good out-of-band linearity (16 dBm) and robustness to mismatches, it features a moderate 1-dB compression point and higher power consumption (60 mW from 1.2 V at 0.9 GHz) due to the use of a 7 unit low noise transconductance amplifier in 3 parallel groups and two TIA stages.

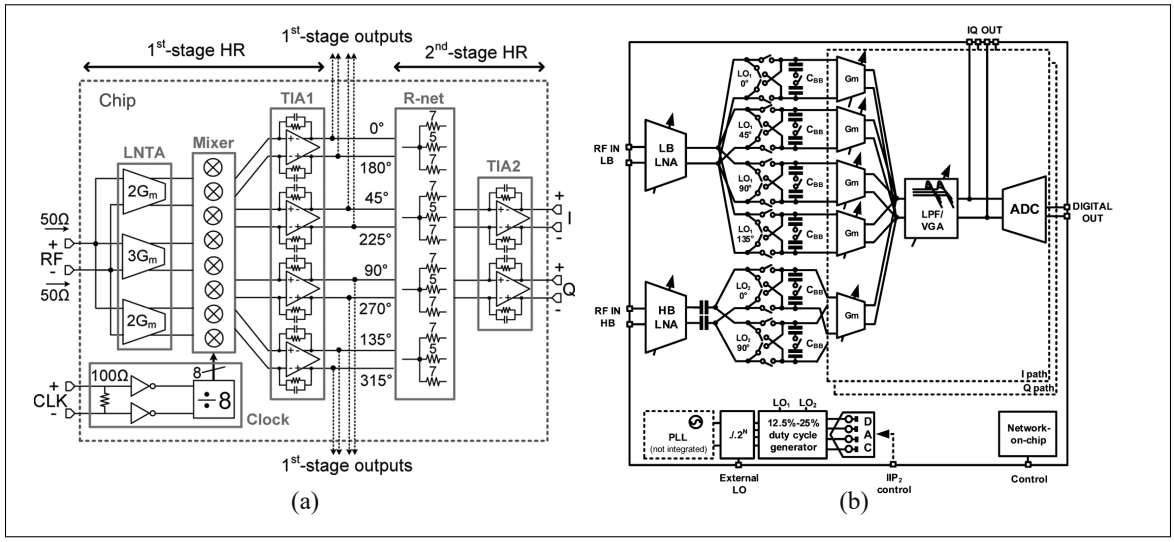

Figure 1.2 (a) The proposed wideband receiver architecture using the two-stage poly-phase HR and the low-pass blocker filtering, and (b) harmonic recombination receiver architecture
Taken from Ru *et al.* (2009) and van Liempd *et al.* (2014), respectively

Another wideband receiver architecture is proposed in van Liempd *et al.* (2014), shown in Figure 1.2(b). This wideband RF receiver operates at up to 6 GHz. The receiver architecture is split into a low-band RF path ($0.4-3$ GHz) and a high-band RF path ($3-6$ GHz) using 8- and 4-phase passive mixers, respectively. It employs two differential LNAs followed by a 4-path and 8-path passive mixers and a set of BB gain stages (G_m) before applying the LPF and gain control. A low-pass RC input impedance is realized by using the power-efficient Gm-C circuitry instead of a virtual ground. A band-pass response at the output of the LNA is frequency translated to a low-pass response at BB. Thus, it suppresses the OBB blockers at RF. Since driving the switches of the 8-phase mixer beyond 3 GHz escalates power consumption significantly, even in 28 nm CMOS technology, conventional 4-phase passive mixers are used for high-band RF signals, precluding from many advantages. Noise figure and the OBB IIP3 of this topology are lower than 3 dB and +3 dBm, respectively, while consuming 35 mW from 0.9 V supply voltage.

1.1.3 Wideband RF receivers using N-path filtering

A promising solution is the impedance transformation that is realized in N-path switching systems that act as passive mixers, as these have no reverse isolation, unlike active mixers. The impedance transformation of a passive mixer can be used to synthesize on-chip high-Q band-pass filtering (BPF) by frequency-translating low-Q baseband impedances to the RF (see Fig. 1.1(b) and Fig. 1.1(c)) (Forbes, Ho & Gharpurey (2013); Lin *et al.* (2014); Xu, Zhu & Kinget (2017)). The center frequencies of the BPF impedances are tuned by the clock frequency, making them very attractive for tunable multi-standard receivers. As these switching systems are only composed of switches and capacitors, the resulting high-Q BPFs provide a high linearity. Moreover, there is no flicker noise issue since the BPF switches are not biased with a DC current (Mirzaei, Darabi & Murphy (2012)).

The proposed receiver in Xu *et al.* (2017) offers higher rejection of the 3^{rd} and 5^{th} LO harmonics. It employs a ratio of 12:17:12 for both the LNA and baseband G_m cells to realize the size ratio of $1 : \sqrt{2} : 1$. However, the approach requires a high current of 24 mA. The switched-capacitor (SC) RF front-end reported in Xu & Kinget (2016) employs N-path RF filters to realize 1) high-linearity and high-order filtering, 2) RF impedance matching by using a programmable SC resistance and 3) harmonic-rejection. For high linearity, Xu & Kinget (2016) employs only passive components, however, this has the cost of a high noise figure (NF) of $6.8 - 9.7$ dB.

1.1.3.1 Mixer-first receivers using N-path filtering

N-path filtering can also be employed in the mixer-first receiver architecture ((Fig. 1.1(d))) that improves linearity by removing the LNA and placing the antenna at the passive mixer input, resulting in impressive out of band IIP3 (Andrews & Molnar (2010); Lin *et al.* (2014)). The proposed RF-to-BB current-reuse architecture in Lin *et al.* (2014) exploits both current-mode active and passive mixers to merge the beneficial properties of both mixers (Figure 1.3). The baseband low-pass part of the passive mixer is up-converted to the RF to realize a band-pass filter centered at the desired receiver frequency that is specified by the LO frequency of the mixer.

The N-path passive mixer realizes the input matching, noise cancelling, input biasing, and OBB filtering, while the full current-reuse structure is achieved by using the N-path active mixer to save power and for strong BB filtering to improve OOB linearity. The current-reuse receiver in Lin *et al.* (2014) optimizes the power consumption (10.6 – 16.2 mW) while achieving the NF of 4.6 ± 0.9 dB, OOB IIP3 of 17.4 dBm and HRR of higher than 51 dB. However, LO leakage is high due to lack of an LNA. LO leakage cancellation helps to achieve some limited suppression while it consumes large area and power (Jayasuriya, Yang & Molnar (2014)). Although mixer-first receivers provide higher linearity without consuming a large power, they experience LO leakage re-radiation.

The LNA usually act as backward isolation, and thus, mixer-first architectures suffer from noise, strong LO signals leaking to the antenna and the limited image rejection (IR) performance because of missing LNA. Thus, high-Q BPFs and inclusion of an LNA help to achieve the desired performance and specifications. An LNA can be added to achieve a better NF, however, at the cost of linearity (Andrews & Molnar (2010)). Similarly, higher order filtering at the baseband (Chen & Hashemi (2015)) is possible, however, the linearity is degraded because of the required active components. Instead, Murphy *et al.* (2012) employs the mixer resistance to provide wideband matching, while achieving high linearity by configuring the baseband in feedback. As shown in Fig. 1.1(e), the noise cancelling receivers in Hedayati, Aparin & Entesari (2014); Murphy *et al.* (2012) achieve low NF by eliminating the thermal noise of the matching resistance. The architecture achieves a high out-of-band IIP3 due to the first-order filtering at the baseband. However, it suffers from LO leakage.

1.2 Ultra-Wideband Impulse Radio Receiver Architectures

Ultra-wideband (UWB) has emerged as an appealing technology for transmitting information for applications requiring either low bit rates over medium-to-long ranges or high bit rates over short ranges. The UWB radio communication systems' approach is based on sharing the occupied spectrum resources by using the overlay principle (Khan (2009); Porcino & Hirt (2003)). UWB provides qualities including wide unlicensed bandwidth, multiple access capability, high

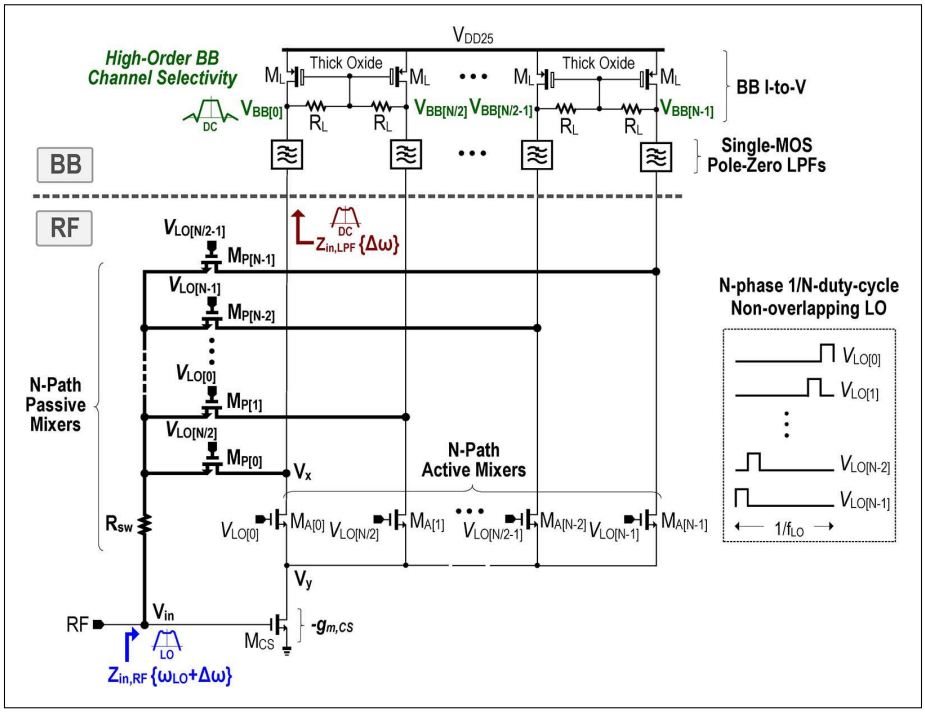

Figure 1.3 Stacked RF-to-BB receiver with parallel N-Path active/passive mixers
Taken from Lin *et al.* (2014)

multi-path resolution, and low power spectral density. Thus, UWB is an attractive physical layer (PHY) for low data-rate wireless sensor networks and high data-rate wireless personal area networks (WPANs).

According to the FCC, UWB is defined as a signal occupying a bandwidth larger than 500 MHz or a fractional bandwidth larger than 20 % Commission et al. (2002). The fractional bandwidth is expressed by

$$f_{\mathrm{BW}} = \frac{f_H - f_L}{f_c}. \tag{1.1}$$

where $f_c = \frac{f_H + f_L}{2}$, f_H and f_L are the upper and lower frequency over the 10-dB bandwidth, respectively. There are two common types of UWB signals classified based on modulation,

carrier-based UWB (CB-UWB) and impulse radio UWB (IR-UWB) (Barras (2010)). This thesis focuses on IR-UWB system, however, an overview of both UWB systems is briefly given.

In a CB-UWB system, the carrier signal is a narrow band signal modulated by different pulse shapes. CB-UWB systems use frequency conversion and provide better spectral control. The major difference with a conventional system is that the modulated signal is transmitted as BB signal with low duty cycle. The controllability and frequency accuracy of CB-UWB signal makes it meet the FCC spectrum mask readily, compared to IR-UWB signals.

IR-UWB, is considered carrier-less. It is generally exploited to describe transceiver systems employing short impulses, typically on the order of 1-2 nanoseconds, with frequencies in the GHz range (Barras (2010)). This system uses RF impulses as a signal carrier to transmit messages. Before transmission, the IR-UWB signal is generally time-modulated. The major challenges in IR-UWB systems is to control the exact impulse shape and its center frequency. However, since the IR-UWB systems digitally generate low power character, they provide a great potential for ultra low power transceiver design.

IR-UWB receivers are generally divided into coherent and non-coherent receivers. The coherent receivers operate based on the comparison of the incoming signal with a generated template pulse locally. The coherent detection provides high robustness against the noise, interference, and multi-path signals. However, there is a need for precise timing in the receiver leading to high power synchronization and complicated schemes that defeat the simplicity enabled by IR-UWB. In addition, this correlation is mainly performed in the digital domain by using a wideband analog to digital converters (ADC) resulting in more power consumption (Parvizi (2016)). In the non-coherent receivers, there is no need to use template pulse. The transmitted bit is determined by using either the peak or the integrated energy of the received impulse. This approach is suitable for low data rate applications and but has lower immunity to interference and noise in comparison to coherent receivers. In the following, the characteristics of the coherent and non-coherent receivers are discussed in detail.

1.2.1 Coherent receivers

As mentioned above, the received impulses are correlated with the locally generated template pulse to demodulate the transmitted bit in the coherent receivers (Abe, Yuan, Ishikuro & Kuroda (2012); Chen, Vinod, McMillan, Yang, Wong & Yang (2022); Siligaris, Chaix, Pelissier, Puyal, Zevallos, Dussopt & Vincent (2013)). If the correlation is greater than a given threshold, the signal is received. Figure 1.4 shows the operating principle of the coherent receiver. As can be seen in Figure 1.4, there is a need for a template pulse generator in the receiver since the transmitted impulse is distorted based on the characteristics of the wireless channel. Thus, to achieve a high-performance transceiver, the channel characteristics should be determined by the template generation block. Then, these characteristics are applied to the template pulse. In the following, the multiple coherent receiver schemes and state-of-the-art designs will briefly be reviewed.

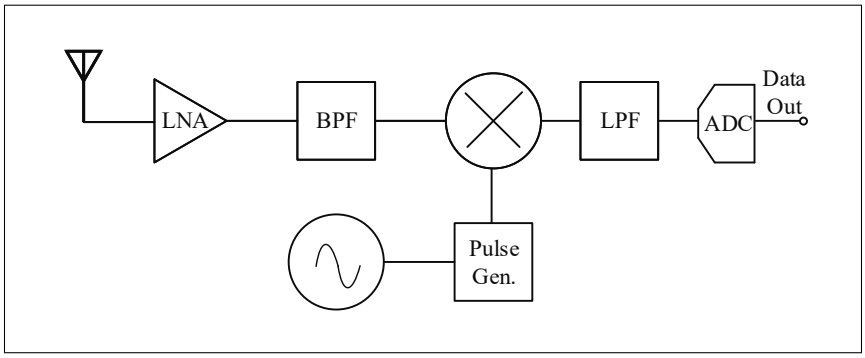

Figure 1.4 Operating principle of a coherent receiver

The quadrature analog correlation receiver presented in Ryckaert, Verhelst, Badaroglu, D'Amico, De Heyn, Desset, Nuzzo, Van Poucke, Wambacq, Baschirotto et al. (2007) is implemented by first mixing the incoming signal with in-phase (I) and quadrature (Q) LO signals and then integrating the resulting function (Figure 1.5(a)). A rectangular window is used rather than the ideal analog pulse template to reduce the power consumption and the complexity of the receiver. Since the receiver uses the pulse position modulation (PPM), there is a need for two serially cascaded delay lines to provide the timing in the analog receiver, one for the delays required for

PPM pulses and the other one to provide the timing window for the integrator employed in the quadrature analog correlator. The receiver consumes a total power of 28.8 mW. Note that More than 75 % of the power is dissipated by the RF front-end of the receiver, highlighting the importance of effective duty cycling and low power RF design in the receiver.

The proposed 100 −960 MHz quadrature analog correlation in Van Helleputte, Verhelst, Dehaene & Gielen (2009) has a similar architecture to the one proposed in Ryckaert *et al.* (2007) (Figure 1.5(b)). However, the whole receiver including the digital back-end circuitry and the synchronization block is implemented on-chip. Nevertheless, an off-chip crystal reference is required to generate accurate timing. The receiver supports data rates from 305 kbps to 39 Mbps, and achieves energy efficiency of 108-pJ/bit in the data detection mode.

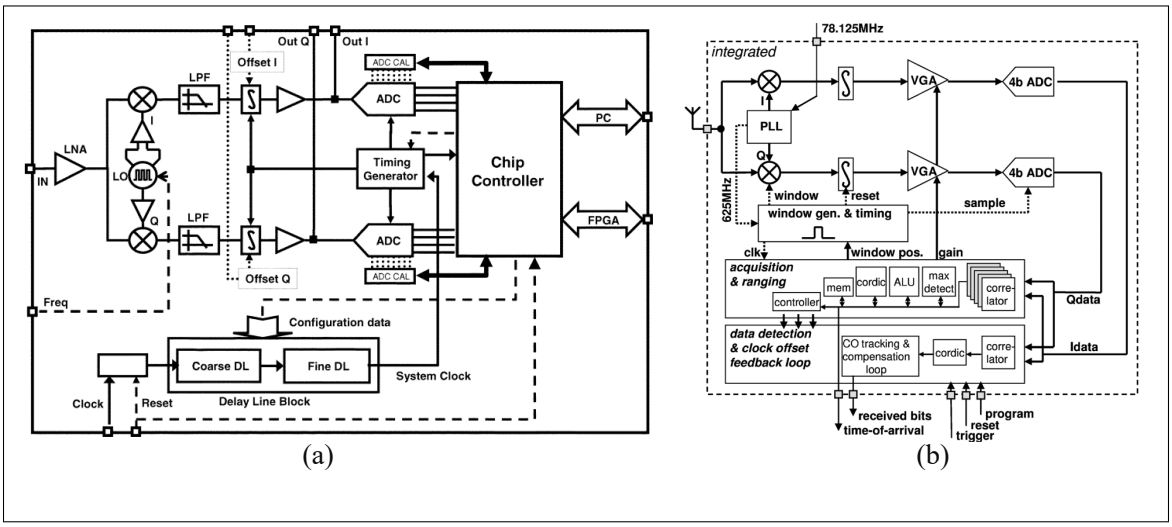

Figure 1.5 Quadrature analog correlating architectures
Taken from Ryckaert *et al.* (2007) and Van Helleputte *et al.* (2009)

The high power consumption and the design complexity of coherent receivers make them impossible to use in low data rate and low power applications. A better solution for these applications is non-coherent receivers with low power consumption (Crepaldi, Angotzi & Berdondini (2019); Geng, Liu, Li, Zhuo, Rhee & Wang (2015); Lee, Park, Jang, Jung & Kim (2019a); Zhang, Li, Mouthaan & Lian (2018b)).

1.2.2 Non-coherent receivers

Non-coherent receivers can generally be divided into three main categories including energy detection, peak detection, and super regenerative detection.

1.2.2.1 Energy detection receiver

The receivers based on energy detector multiply the incoming impulse and integrate the output in a given time window (Crepaldi *et al.* (2019); Ding, Wang, Song, Rhee & Wang (2021); Nikoofard, Zadeh & Mercier (2021)). The integrator output is compared with a threshold to specify the bit received. Thus, the time window duration plays an important role to capture the pulse and/or noise/interferers.

The receiver presented in (Vigraham & Kinget (2014)) uses the OOK modulation in a energy detection based receiver. Figure 1.6 shows the block diagram of the non-coherent receiver composed of an LNA and two RF amplifiers. For energy detection, a self-mixer is fed by the output of the first and the second RF amplifiers. A programmable gain amplifier (PGA) amplifies the baseband signal. Then, the amplified baseband signal enters into a comparator for decision.

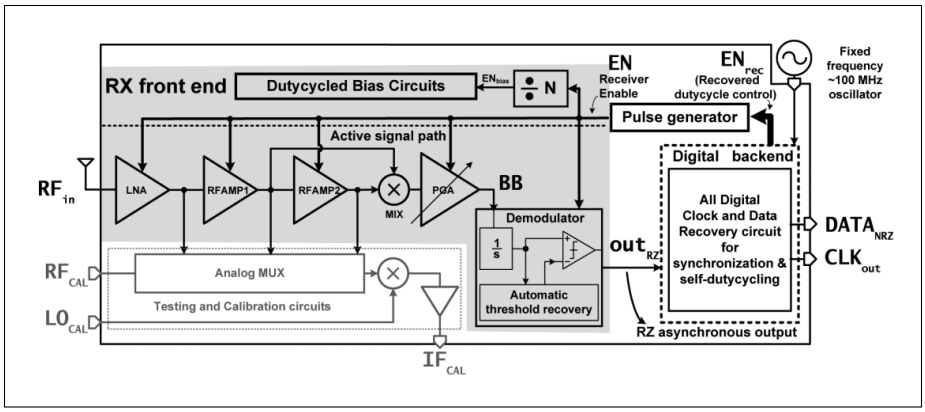

Figure 1.6 Block diagram of an energy detection receiver
Taken from Vigraham & Kinget (2014)

The demodulation scheme used is continuous-time slicing, leading to decoupling of the synchronization and demodulation and thus reduces power consumption and acquisition time, compared

to the conventional gated-integration scheme. To improve the efficiency, the receiver provides self duty cycling and its ON time is of 30 ns. The receiver consumes 11.5 mW without duty cycling. The receiver provides 0.375 nJ/b energy efficiency by employing duty cycling.

The non-coherent energy detection receiver proposed in (Lee *et al.* (2019a)) is divided into analog and digital parts (see Figure 1.7). The analog part is composed of aN LNA, a radio frequency amplifier (RF AMP), an envelope detector, a BB amplifier, and a hysteresis comparator. The digital part is composed of an edge detector, a synchronizer, and 6-bit time-to-digital converter (TDC). The receiver employs the digitized multi-pulse position modulation (D-MPPM) to modulate a number of data bits in a single clock period and thus implement a clock-less receiver. The data rate is improved by a factor of five (500 Mbps), while the receiver consumes the total power of 27.7 mW.

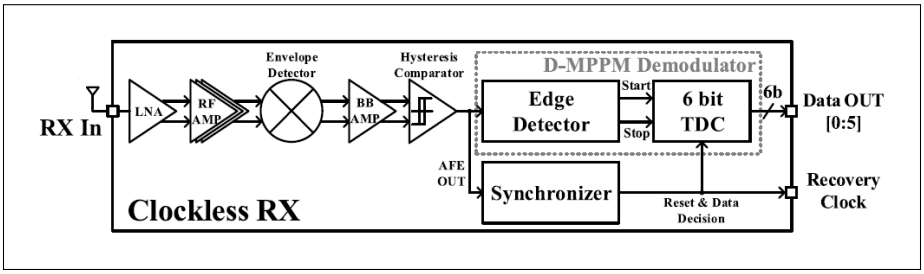

Figure 1.7 Energy detection non-coherent receiver
Taken from Lee *et al.* (2019a)

1.2.2.2 Peak detection receiver

Receivers based on peak detector compare the incoming input signal with a threshold to specify whether a pulse is received or not (Shams, Nabki et al. (2019)). Therefore, these type of receivers do not have sensitivity to the placement and duration of the integration window. The 3.1 −4.9 GHz IR-UWB non-coherent architecture proposed in (Vauche, Muhr, Fourquin, Bourdel, Gaubert, Dehaese, Meillere, Barthelemy & Ouvry (2017)) employs peak voltage detector (PVD) technique. The receiver is composed of a band pass type LNA, driving an asynchronous peak detector based on envelope detection. A short duration BB pulse (1.5 ns) is provided by

the peak detector for each incoming UWB pulse. Then, the numeric single-ended signal is converted into a low voltage differential signaling (LVDS) signal to provide standardized signals to the board interface (see Figure 1.8). The receiver achieves a sensitivity of −85.8 dBm at 1 Mbps data rate. Thus, an input signal with a magnitude of 1.1 mV can be detected, leading to a communication range of 1.9 m. The receiver consumes total power of 30.5 mW at 100 Mbps data rate.

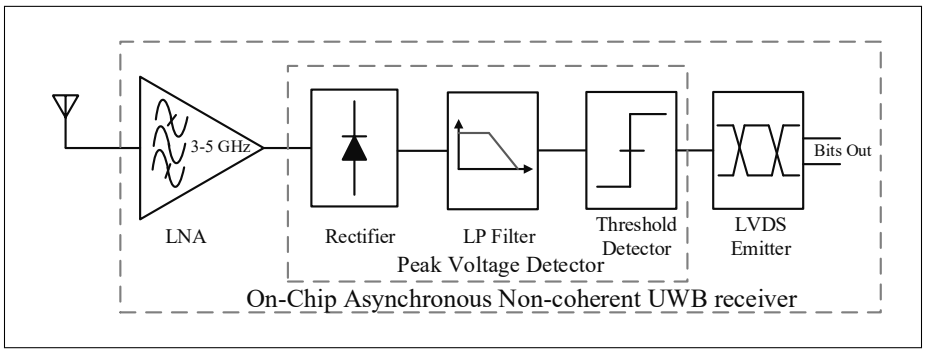

Figure 1.8 An IR-UWB peak detection non-coherent receiver
Taken from Vauche *et al.* (2017)

Note that this scheme suffers from a low theoretical sensitivity since the signal is not collected throughout the symbol duration time, as opposed to the energy detectors. However, the PVD technique can be employed for short-range transceivers and is well suited for burst duty-cycled receivers due to its asynchronous nature.

1.2.2.3 Super regenerative receiver (SRR)

The other non-coherent receivers are based on energy detection and super regenerative amplification (Fu, El-Sankary, Ge, Yin & Truhachev (2022); Raghunathan & Lee (2018); Rezaei & Entesari (2018)). These receivers operate based on triggering an oscillation with the input pulses. The generated oscillation is employed for an envelope detection and the pulses are decoded with respect to the oscillator start-up time. However, any interference or noise can trigger the oscillation and thus reduce the receiver sensitivity.

The 902 −928 MHz SRR, a fully integrated receiver proposed in (Rezaei & Entesari (2018)), shown in Figure 1.9(a), operates in three modes including frequency calibration mode, critical current detection (CCD) mode and receiver mode. It is composed of an input transconductance amplifier (TCA) to isolate the antenna and to couple the incoming signal to the super regenerative oscillator (SRO), an envelope detector extracts the oscillation amplitude, and a comparator discriminates between a 1 or a 0, based on the oscillation amplitude. The receiver achieves excellent energy efficiency. However, the it requires accurate frequency calibration at startup and adjusts its gain only at startup which is not ideal for varying channel conditions.

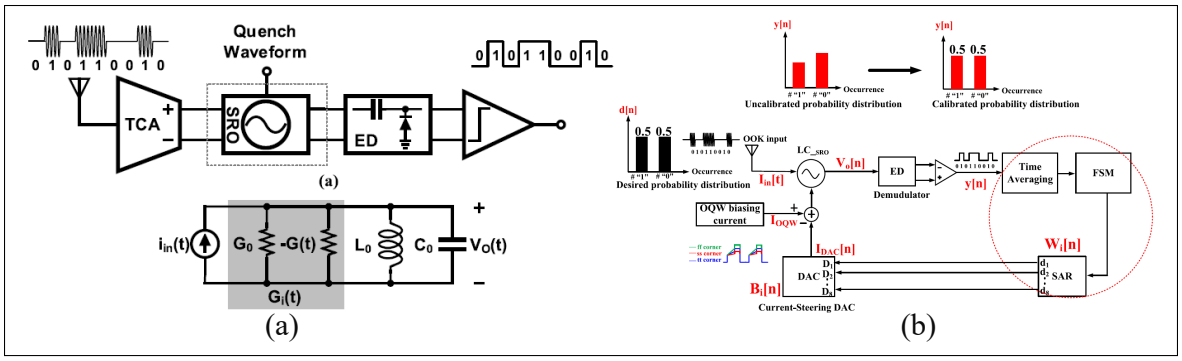

Figure 1.9 (a) Simplified block diagram of the SRR, and (b) SRR system level architecture using a statistics-based time averaging technique
Taken from Rezaei & Entesari (2018) and Fu *et al.* (2022)

The sensitivity of the SRR system can be affected by negative transconductance ($-G_m$) variations of the SRO and center frequency deviations. To overcome the detrimental effect of process-voltage-temperature (PVT) variations, calibration techniques can be employed. These are classified into foreground and background methods. A foreground calibration scheme is proposed in (Rezaei & Entesari (2018)) for center frequency and $-G_m$ variations. However, foreground calibration solutions suffer from interruptions of the input data stream. To overcome this drawback, the recent SRR architecture proposed in Fu *et al.* (2022) introduces a blind background calibration technique, shown in Figure 1.9(b). The proposed scheme helps SRRs to keep their high sensitivity and immunity to $-G_m$ changes under PVT variations. Moreover, it employs input signal statistics, and there is no need for an input bit-stream interruption for extraction of the errors.

1.3 Comparison of the state-of-the-art

Table 1.1 compares the measured performance of the coherent and non-coherent RF receiver architectures. The receiver proposed in (Geng *et al.* (2015)) can operate at frequency range of 7.25 – 9.5 GHz, and achieves a 500 Mbps data rate while consuming 5.9 mW at the cost of lower sensitivity. The proposed architecture in (Lee *et al.* (2019a)) consumes 27.7 mW at a data rate of 500 Mbps. The coherent architecture presented in (Ding *et al.* (2021)) provides a 100 Mbps data rate with a sensitivity of −62 dBm at a power consumption of 23.3 mW. Non-coherent IR-UWB receivers are known to extract good amount of signal energy despite multi-path propagation and distortions. Low cost, low complexity applications, and reduced power consumption give an edge to the non-coherent architectures over their counterpart coherent receivers. However, they usually exhibit reduced sensitivity.

Table 1.1 Comparison of the state-of-the-art

Ref.	Tech. (nm)	Freq. (GHz)	Data Rate (Mbps)	Sensitivity (dBm)	Power (mW)	Area (mm^2)	Architecture
Zhang *et al.* (2018b)	65	3-8	10	-64	6.4	0.01	Non-Coherent
Crepaldi *et al.* (2019)	130	3.5-4.5	1000	$-38^{\star\star}$	12	$0.34^{\star}$	Non-Coherent
Hsieh, Huang, Kuo, Wang & Lu (2016)	180	0.402-0.405	0.05, 0.12	-55	0.352	3.3	Coherent
Ding *et al.* (2021)	65	3.5	100	-62	23.3	0.94	Coherent
Cheng & Chen (2021)	180	0.433	0.2	-80/-78/-77	0.054	0.45	Coherent
Vigraham & Kinget (2014)	65	4.35	2	-76.5	11.66	$0.53^{\star}$	Non-Coherent
Geng *et al.* (2015)	65	7.25–9.5	500	-59	5.9	$2.25^{\diamond}$	Non-Coherent
Lee *et al.* (2019a)	65	3-5	500	-61	27.7	$2.88^{\ddagger}$	Non-Coherent

* Active area. $^{\diamond}$Including the receiver, transmitter and PLL. ** At a 10^{-3} packet error rate.
‡ Including the receiver and transmitter.

1.4 Conclusion

This chapter briefly introduced the concept of wideband receiver front-end, and it summarized the different wideband receiver architectures in the state-of-the-art. It can be seen that there are many architectures for wideband receivers and that their use is set to expand more and more. The relationship between the different RF front-end's specifications were briefly discussed.

The chapter also introduce IR-UWB receivers. Overall, non-coherent IR-UWB receivers are preferred over coherent IR-UWB receivers. However, this comes at the cost of reduced sensitivity. Moreover, non-coherent receivers do not require channel estimation and accurate synchronisation, and are thus attractive due to their simplicity, and consequently lower power dissipation.

CHAPTER 2

ANALYSIS AND COMPARISON OF LOW-POWER 6 GHZ N-PATH FILTER-BASED HARMONIC SELECTION RF RECEIVER FRONT-END ARCHITECTURES

The unlicensed spectrum in the 2.4 and 5 GHz bands has led to the exponential growth of Wi-Fi. The FCC has proposed the widening of the spectrum available for unlicensed Wi-Fi usage in the $5.9-7.2$ GHz band, and a band extension effort is also being coordinated by ETSI in Europe. Accordingly, wireless systems and devices should be able to efficiently support the higher bands and new standards used in upcoming applications. This puts a strain on the RF front-end specifications.

The contribution of this chapter is the analysis, design, and comparison of 4-, 8- and 16-path harmonic selection receiver architectures that allow for the selection of the third harmonic of the LO frequency, and that effectively suppresses other harmonics to reduce clocking power consumption at higher RF frequency bands of operation. In addition, these receiver architectures mitigate the disadvantages stemming from the need for a high clocking frequency in the N-path switching filter and employ a differential structure alleviating the issues related to the even-order LO harmonics.

Analysis and Comparison of Low-Power 6 GHz N-Path Filter-Based Harmonic Selection RF Receiver Front-End Architectures

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Abstract: N-path switching systems employing switched-series-R-C networks are analyzed in the context of RF receiver front-ends, and it is shown that it is possible to mitigate the need to generate an accurate low power clock at high frequencies by operating at higher order harmonics of the switching frequency. For values of N that are an integer factor of 4 (i.e., $N = 4, 8$ and 16), harmonic selection RF receivers architectures are presented using two feed-forward N-path switching filters and harmonic recombination at the baseband. Moreover, it is demonstrated how the harmonic recombination stage at the baseband can be reconfigured to select the third harmonic of the switching frequency rather than the fundamental in order to reduce the input frequency and power consumption of the multi-phase clock generator by a factor of three. In addition, to analyse the performance of the proposed RF receiver architecture, multiple receivers have been designed and post-layout simulated in two CMOS technologies, TSMC 130 nm and TSMC 65 nm. The resulting $5.7-7.2$ GHz RF receiver architectures allow for operation at the third harmonic of the LO frequency (i.e., $1.9-2.4$ GHz), reducing power consumption and allowing for good performance metrics at both studied technology nodes.

Keywords: Receiver front-end, harmonic recombination, N-path filter, harmonic selection, G_m stages, performance analysis

2.1 Introduction

Narrow-band RF receiver front-ends utilize off-chip RF filtering to prevent the wanted signal from being corrupted by large out-of-band (OOB) signals. To support the large number of frequency bands provided by modern wireless technologies, typically multiple narrow-band receivers are required since RF filters are often fixed (Murphy *et al.* (2012)). Compared to narrow-band receivers, wideband RF receiver front-ends offer more flexibility. Typical wide-band receiver architectures are realized by a low noise amplifier (LNA) followed by a down-conversion mixer. The simplest RF signal down-conversion approach is to employ a 4-phase mixer composed of four switches that are driven by four 25 % duty cycle non-overlapping clocks (Mollaalipour & Miar-Naimi (2016)), as shown in Fig. 2.1. Since SAW filtering is not an option in wideband receivers, any unattenuated blocker will appear at the LNA, along with the desired signal (Javadi, Miar-Naimi, Tijani, Manstretta & Castello (2021)). Accordingly, there has been a growing interest in blocker-tolerant wideband receiver architectures without resulting in a significant increase in power consumption or occupied chip area.

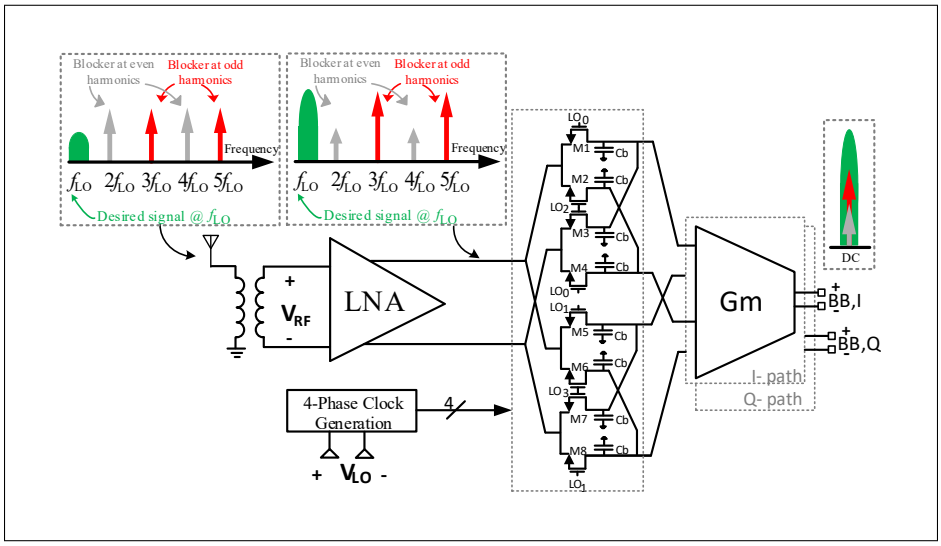

Figure 2.1 Conventional wideband receiver using a 4-phase passive mixer

A promising solution is the impedance transformation that is realized in N-path switching systems that act as passive mixers, as these have no reverse isolation, unlike active mixers (Mirzaei & Darabi (2010)). In N-path switching systems, RF signal down-conversion is realized by multiplying the RF signal and a square-wave LO waveform. Since the LO waveform is not a pure sine-wave and contains undesired harmonics, mixing the RF signal with a square wave down-converts both the desired signal located around the LO frequency and the signals located around the LO harmonics. An RF band-selection filter mitigates this harmonic mixing in narrow-band receivers. An alternative approach is to employ harmonic-rejection mixers (HRM) to cancel the need for a discrete IF filter and to limit spurious mixing in receivers. By providing frequency-synthesis, HRMs can be employed in wideband receivers such as proposed in (Ho *et al.* (2014); Singh *et al.* (2014); Wu *et al.* (2019)). Such harmonic rejection architectures will be studied in this work to establish trade-offs and comparison with conventional architectures. Notably, this work will propose an architecture that can operate at higher RF frequencies with reduced impact on power consumption and operation with larger geometry CMOS technology nodes.

An overview of the prior art is given in Section 2.2. Then, N-path switching systems and harmonic selection techniques are analyzed in Section 2.3. Section 2.4 describes the proposed architectures, and the circuits are detailed in Section 2.5, with post-layout simulation results presented in Section 2.6.

2.2 Prior Art in Harmonic Rejection RF Receivers

The first harmonic-rejection (HR) principle proposed in Weldon *et al.* (2001) used the gain coefficients at the RF section of the circuit, while the use of the HR coefficients at the baseband analog-domain was described in Molnar *et al.* (2004). The proposed HRM in Weldon *et al.* (2001) includes three parallel mixing paths with gain ratios of $1 : \sqrt{2} : 1$. In this fashion, the 3^{rd} and 5^{th} harmonics can be rejected. Higher harmonic rejection can be achieved by accurately implementing the desired weighting ratio $1 : \sqrt{2} : 1$ on chip Ru *et al.* (2009). An alternative HR technique later introduced is based on the N-path filter design (Forbes *et al.* (2013); Karami,

Banaeikashani, Behmanesh & Atarodi (2020); Lu, Hung & Lee (2018)) that can be used in receiver structures to provide more harmonic rejection. The proposed receiver in Xu *et al.* (2017) employs a ratio of $12 : 17 : 12$ for both the LNA and baseband G_m cells to realize the size ratio of $1 : \sqrt{2} : 1$. It offers higher rejection of the 3^{rd} and 5^{th} LO harmonics at the cost of a high current of 24 mA. A 16-path HRM is proposed in Elmi, Tavassoli & Jalali (2018), where the receiver employs a HR 16-path filter using resistive coefficients that results in relatively high power consumption.

Note that in prior works, the 3^{rd} and 5^{th} harmonic rejection are achieved by employing the pseudo-sine wave method, either at a weighted LNA, at a harmonic-rejecting N-Path Filter (HR-NPF) or at a harmonic recombiner at the baseband (van Liempd *et al.* (2014); Xu & Kinget (2016); Zinjanab, Elmi & Jalali (2018)). Employing a HR-NPF increases the number of switches by a factor of $\frac{N}{2} - 1$ that leads to the increased power consumption of the N-phase clock generator (Zinjanab *et al.* (2018)). Using harmonic recombination at the baseband shows a better performance in terms of the harmonic rejection ratio (HRR), compared to harmonic attenuation at the LNA output. The most reported HR architectures operate at an RF input frequency of less than 3 GHz and use an 8-phase passive switching circuit to achieve harmonic rejection. To drive the eight switches, there is a need for 12.5 % duty cycle clock generation, and the LO should operate at a frequency that is four times that of the RF frequency. For example, to support an RF of 3 GHz, the switching frequency is of 3 GHz, and the clock generator requires an LO operating at 12 GHz, consuming considerable power and precluding the use of older technology nodes.

Accordingly, this work aims to mitigate this issue by relaxing the frequency requirement of the N-path filter, as this is key in supporting higher frequency RF inputs beyond 3 GHz. A versatile wideband RF receiver composed of an N-path filter-based architecture that offsets the aforementioned disadvantages is proposed. Three RF receiver front-ends using a 4-, 8- and 16-path switching configuration and harmonic recombination at baseband are presented. Moreover, the performance of 4-, 8- and 16-path HR receivers is compared to the conventional wideband receiver architecture shown in Fig. 2.1. In the proposed N-path HR receivers, the amplifiers

at baseband are decomposed and reconfigured to select the 3^{rd} harmonic of the switching frequency, as opposed to the fundamental harmonic of the LO. As a result, the required N-path filter switching clock frequency is reduced by a factor of three, relaxing the LO frequency requirement. This allows the proposed receiver to have lower complexity and achieve lower power consumption. The proposed RF front-ends operate from 5.7 to 7.2 GHz to cover the upcoming Wi-Fi 6E band that has been proposed by the FCC for unlicensed Wi-Fi usage to overcome an 800 MHz spectrum shortage (Grace).

2.3 Analysis of the Frequency Down-conversion Properties of the N-Path Switching Filter and its Harmonic Selection Properties

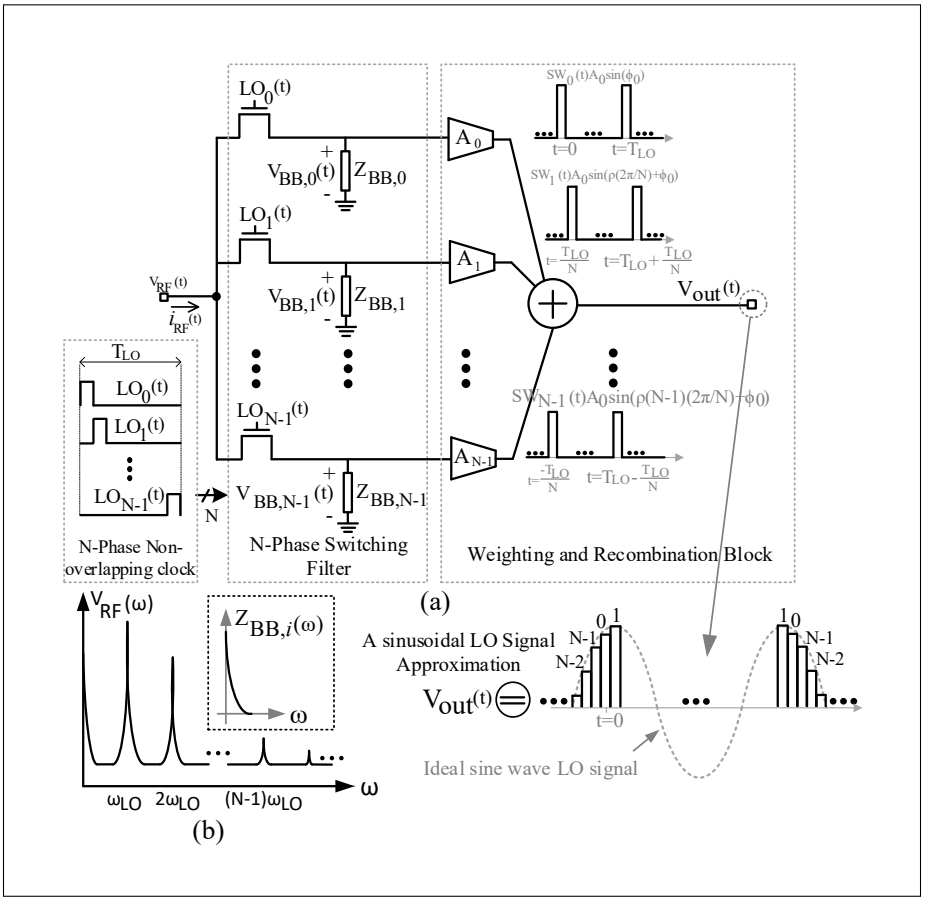

Figure 2.2 (a) N-path switching system using baseband gain coefficients, and (b) RF input voltage of $V_{RF}(\omega)$

Consider an N-path switching system composed of N identical branches as shown in Fig. 2.2(a) and that employs baseband signal recombination (Mirzaei *et al.* (2012); Murphy *et al.* (2015); Zinjanab, Jalali & Farshi (2020)). The MOS switches are driven by a N-phase non-overlapping clock, $LO_0(t), LO_1(t), ..., LO_{N-1}(t)$, with a duty cycle of $1/N$ and pulse width of T_{LO}/N, as shown in Fig. 2.2(a). The periodic function of the N-phase LO clock can be written as

$$SW_0(t) = \begin{cases} 1, & (k - \frac{1}{2N})T_{LO} \leq t \leq (k + \frac{1}{2N})T_{LO} \\ 0, & (k + \frac{1}{2N})T_{LO} \leq t \leq (k + \frac{2N-1}{2N})T_{LO}, \end{cases} \tag{2.1}$$

$$SW_i(t) = SW_0(t - \frac{i}{N}T_{LO}),\ i = 1, 2, ..., N - 1, \tag{2.2}$$

where $SW_i(t)$ represents i^{th} phase of the LO clock and k is an arbitrary integer number. The non-overlapping clock causes only one path of the switching filter to be 'ON' at any given moment. Switches are assumed to be ideal, except for an ON resistance of R_{SW} and an ideal RF current source of $i_{RF}(t)$ that flows into the N-path switching system. If the i^{th} phase of the clock voltage is high, the $i_{RF}(t)$ only flows through the i^{th} branch at any moment. The baseband voltage of $V_{BB,i}(t)$ is given by (Mirzaei *et al.* (2012))

$$V_{BB,i}(t) = [SW_i(t) \times i_{RF}(t)] * Z_{BB,i}(t). \tag{2.3}$$

Accordingly, the current flowing into a baseband impedance of $Z_{BB,i}$ is equal to $i_{RF}(t)$ or equal to zero, when the corresponding MOS switch is ON or OFF, respectively. The Fourier transform of (2.3) is expressed as

$$V_{BB,i}(\omega) = \frac{1}{2\pi}[SW_i(\omega) * I_{RF}(\omega)] \times Z_{BB,i}(\omega). \tag{2.4}$$

To express the Fourier transform of $SW_i(t)$, the Fourier series of $SW_i(t)$ in (2.1) and (2.2) is first expressed as

$$SW_0(t) = \sum_{n=-\infty}^{\infty} a_n e^{jn\omega_{LO}t}, \tag{2.5}$$

$$SW_i(t) = \sum_{n=-\infty}^{\infty} a_n e^{-jin\frac{2\pi}{N}} e^{jn\omega_{LO}t}, \tag{2.6}$$

where a_n represents the Fourier series coefficients and are equal to

$$a_n = \frac{1}{N} sinc(\frac{n\pi}{N}). \tag{2.7}$$

Therefore, the Fourier transform of $SW_i(t)$, $SW_i(\omega)$, is given by

$$SW_i(\omega) = \sum_{n=-\infty}^{\infty} 2\pi a_n e^{-jin\frac{2\pi}{N}} \delta(\omega - n\omega_{LO}). \tag{2.8}$$

It is clear from (2.8) that $SW_i(\omega)$ is non-zero at f_{LO} and its harmonics. Ignoring harmonic foldback effects, the baseband voltage of $V_{BB,i}(t)$ can be expressed as

$$V_{BB,i}(\omega) = \sum_{n=-\infty}^{\infty} a_n e^{-jin\frac{2\pi}{N}} I_{RF}(\omega - n\omega_{LO}) Z_{BB,i}(\omega). \tag{2.9}$$

As such, the input RF current is frequency-translated to the baseband by a shift of $n\omega_{LO}$ to generate the baseband voltage via the baseband impedance.

Note that since only one switch is 'ON' at any given moment, the voltage of $V_{RF}(t)$ at the RF side of the switches is equal to the resistance drop across the corresponding switch plus the baseband voltage, $V_{BB,i}(t)$ (Mirzaei *et al.* (2012)). Thus, the RF voltage of $V_{RF}(\omega)$ in the frequency domain is given by

$$V_{RF}(\omega) = R_{SW} I_{RF}(\omega) + \sum_{i=0}^{N-1} \frac{1}{2\pi} SW_i(\omega) * V_{BB,i}(\omega). \tag{2.10}$$

By replacing $SW_i(\omega)$ and $V_{BB,i}(\omega)$ by (2.8) and (2.9), respectively, then $V_{RF}(\omega)$ can be written as

$$V_{RF}(\omega) = R_{SW} I_{RF}(\omega) + N \sum_{n=-\infty}^{\infty} \sum_{k=-\infty}^{\infty} a_n a_k \times I_{RF}(\omega - (n+k)\omega_{LO}) Z_{BB}(\omega - n\omega_{LO}), \tag{2.11}$$

where $n + k$ is equal to αN, α being integer number. N switches and N baseband impedances provide an impedance transformation from the baseband to f_{LO} and its harmonics at the RF input. In this fashion, a low-Q baseband impedance is transferred to a high-Q RF impedance by the impedance transformation of the N-path switching filter.

The baseband impedances of $Z_{BB,i}$ are low-pass filters composed of large capacitors and the RF input current has a frequency of $m\omega_{LO} + \Delta\omega_0$ ($\Delta\omega_0 \ll \omega_{LO}$), where m ($1 \leq m \leq N-1$) is an arbitrary integer number. Thus, $V_{BB,i}(\omega)$ and $V_{RF}(\omega)$ are defined as

$$V_{BB,i}(\Delta\omega_0) = I_{RF}(m\omega_{LO} + \Delta\omega_0) \times (\frac{1}{N} sinc(\frac{m\pi}{N}) e^{-jim\frac{2\pi}{N}} Z_{BB,0}(\Delta\omega_0)), \tag{2.12}$$

$$V_{RF}(m\omega_{LO} + \Delta\omega_0) = I_{RF}(m\omega_{LO} + \Delta\omega_0) \times \left(R_{SW} + \frac{1}{N} sinc^2(\frac{m\pi}{N}) Z_{BB,0}(\Delta\omega_0) \right). \tag{2.13}$$

Accordingly, the RF-to-BB conversion gain is approximately equal to

$$\frac{|V_{BB,i}(\Delta\omega_0)|}{|V_{RF}(m\omega_{LO} + \Delta\omega_0)|} \cong \frac{\frac{1}{N} sinc(\frac{m\pi}{N}) Z_{BB,0}(\Delta\omega_0)}{R_{SW} + \frac{1}{N} sinc^2(\frac{m\pi}{N}) Z_{BB,0}(\Delta\omega_0)}. \tag{2.14}$$

If $\Delta\omega_0$ is relatively small, then $Z_{BB,0}(\Delta\omega_0)$ has a relatively large value compared to R_{SW}, then the switching resistance in (2.14) can be assumed to be negligible. Thus, (2.14) is simplified to $\frac{1}{sinc(\frac{m\pi}{N})}$ for $|\Delta\omega_0| \ll |\omega_{LO}|$. On the other hand, for large values of $\Delta\omega_0$, $Z_{BB,0}(\Delta\omega_0)$ has relatively small values, and the second term in the denominator of (2.14) can be ignored compared to the value of R_{SW}. Therefore, (2.14) is then approximately equal to zero. As a result,

for $|\Delta\omega_0| \ll |\omega_{LO}|$, we have

$$|V_{BB,i}(\Delta\omega_0)| \cong \frac{|V_{RF}(m\omega_{LO} + \Delta\omega_0)|}{sinc(\frac{m\pi}{N})}. \tag{2.15}$$

Fig. 2.2(b) depicts the RF input voltage of $V_{RF}(\omega)$, obtained in (2.11). The minimum value of $V_{RF}(\omega)$ is limited by the value of R_{SW}. Moreover, Fig. 2.2(b) illustrates the harmonic selectivity of the N-path switching filters and shows that the center frequency of the high-Q N-path switching is controlled by the LO frequency, making them a promising approach for applications that need for tunable high-Q band-pass filters.

To recombine the N baseband voltages of $[V_{BB,0}, V_{BB,1}, ..., V_{BB,N-1}]$ and to achieve an output voltage, a harmonic recombination structure is often used (Murphy *et al.* (2012,1); Xu *et al.* (2017)). According to (2.8), the N-phase clock has non-zero components at the harmonics of f_{LO} in the N-path switching system. To provide the suitable harmonics selectivity, the LO signal must only contain the components at the desired frequency. This can be achieved by a combination of the passive switching system and the amplifiers in the harmonic recombination stage. To equivalently generate a sine LO signal, an ideal LO sine signal of $A_c sin(\rho\omega_{LO}t + \varphi_0)$ is divided into N equal time intervals with pulse widths of $\frac{T_{LO}}{N}$, where A_c and φ_0 are a constant amplitude and an initial phase, respectively. Therefore, the required voltage gain of each corresponding amplifier, $A_{G_m}(i)$, is defined as

$$A_{Gm}(i) = A_c sin(\rho i \frac{2\pi}{N} + \varphi_0), i = (0, 2, ..., N-1), \tag{2.16}$$

where $0 \leqslant \rho < N, \rho \in \mathbb{Z}$. The particular case of $\rho = 1$ is analyzed in recent works such as Murphy *et al.* (2012,1); Park & Razavi (2014); Xu *et al.* (2017), however, the case of $\rho = 3$ is discussed here in order to favor the down-conversion of the third harmonic of the LO frequency in the recombination process.

It is assumed in this analysis that each gain coefficient of $(A_{Gm}(i))$ in Fig. 2.2(a) is realized by an amplifier with an infinite input resistance. This stage converts each baseband voltage to a

baseband current by employing transconductance amplifiers $[A_0, A_1, ..., A_{N-1}]$ configured with the appropriate gain coefficients as defined in (2.16). The total current flowing through the output resistance generates the output voltage given by

$$V_{out}(\omega) = \left[\sum_{i=0}^{N-1} A_{G_m}(i) V_{BB,i}(\omega)\right] R_{out}, \tag{2.17}$$

where R_{out} is the total output resistance of the N parallel amplifiers. The transconductance amplifiers have their gains, $A_{G_m}(i)$, set to obtain harmonic rejection (Park & Razavi (2014)). From (2.9) and (2.16), the Fourier transform of the output voltage can be expressed as

$$V_{out}(\omega) = (\sum_{i=0}^{N-1} \sum_{n=-\infty}^{\infty} a_n A_c sin(3i\frac{2\pi}{N} + \varphi_0) e^{-jin\frac{2\pi}{N}} \times I_{RF}(\omega - n\omega_{LO}) Z_{BB,i}(\omega)) R_{out}. \tag{2.18}$$

If a resistance of R_{RF} is considered to be in parallel with the input current source, $i_{RF}(t)$, it can be shown that (2.9) will become

$$V_{BB,i}(\omega) = \sum_{n=-\infty}^{\infty} a_n e^{-jin\frac{2\pi}{N}} \times \left[\frac{R_{RF} I_{RF}(\omega - n\omega_{LO}) Z_{BB,i}(\omega)}{R_{RF} + R_{SW} + \frac{1}{N}\sum_{k=-\infty}^{\infty} sinc^2(\frac{k\pi}{N}) Z_{BB,i}(\omega - k\omega_{LO})}\right], \tag{2.19}$$

$$\begin{aligned} V_{out}(\omega) = \sum_{i=0}^{N-1} \sum_{n=-\infty}^{\infty} a_n A_c sin(3i\frac{2\pi}{N} + \varphi_0) e^{-jin\frac{2\pi}{N}} R_{out} \times \\ \left[\frac{R_{RF} I_{RF}(\omega - n\omega_{LO}) Z_{BB,i}(\omega)}{R_{RF} + R_{SW} + \frac{1}{N}\sum_{k=-\infty}^{\infty} sinc^2(\frac{k\pi}{N}) Z_{BB,i}(\omega - k\omega_{LO})}\right]. \end{aligned} \tag{2.20}$$

Accordingly, $V_{out}(\omega)$ has a non-zero value if $n = \alpha N$ ($\alpha \in \mathbb{Z}$) and $\varphi_0 \neq 0$. Therefore, the output voltage becomes

$$\begin{aligned} V_{out}(\omega) = \sum_{i=0}^{N-1} \sum_{\alpha=-\infty}^{\infty} \frac{1}{N} A_c sinc(\alpha\pi) sin(3i\frac{2\pi}{N} + \varphi_0) R_{out} \times \\ \left[\frac{R_{RF} I_{RF}(\omega - \alpha N\omega_{LO}) Z_{BB,i}(\omega)}{R_{RF} + R_{SW} + \frac{1}{N}\sum_{k=-\infty}^{\infty} sinc^2(\frac{k\pi}{N}) Z_{BB,i}(\omega - k\omega_{LO})}\right]. \end{aligned} \tag{2.21}$$

As $sinc(\alpha\pi)$ is equal to unity when α is equal to zero, and is equal to zero when $\alpha \neq 0$, $V_{out}(\omega)$ in (2.21) indicates rejection at all harmonics, excluding the baseband. The output voltage of $V_{out}(\omega)$ around the baseband can be given as

$$V_{out}(\omega) \approx \sum_{i=0}^{N-1} sin(3i\frac{2\pi}{N} + \varphi_0) \times \left[\frac{R_{RF} Z_{BB,i}(\omega) R_{out}}{R_{RF} + R_{SW} + \frac{1}{N} Z_{BB,i}(\omega)} \right] I_{RF}(\omega). \tag{2.22}$$

If $Z_{BB,i}(\omega)$ is implemented by large capacitors, then only the third harmonic of f_{LO} is amplified at the output, and other frequency components are rejected.

Accordingly, the N-path switching architecture allows for the RF input signal to be down-converted to the baseband through the third harmonic of the LO frequency, and thus allows to relax the LO frequency requirements for a targeted RF band.

2.4 Proposed Harmonic Selection RF Front-end Architectures

The HR principle leveraged in the proposed receiver is illustrated in Fig. 2.3. The architecture consists of an off-chip balun for the single-to-differential conversion, a differential wideband LNA, two N-path filters implementing an RF band-pass filter (BPF), and baseband harmonic-recombination transconductors (G_m stages). The proposed HR receiver, being fully differential, rejects the even LO harmonics, and as such there is no need to put in parallel a notch filter with the LNA, yielding advantages in area and power consumption. The LNA amplifies the RF signal, and as shown in Fig. 2.3. The amplified RF signal at the differential outputs of the LNA is down-converted to the baseband signal across the capacitors in the N-path filter, such that the circuit can be considered as an RF down-conversion receiver. All the switches in the N-path filter are driven by a 1/N duty-cycle non-overlapping LO signal at f_{LO}.

Since multiplication with a square wave, or equivalently linear time-variant behavior in a N-path switching filter down-converts both wanted and unwanted signals around the LO harmonics, selecting higher harmonics rather than fundamental harmonics helps to reduce the required multi-phase clock frequency. As depicted in Fig. 2.3, while the switches in the N-path filtering

are driven at f_{LO} (as opposed to $3f_{LO}$), the down-converted voltages across the $C_{B,N}$ capacitors at baseband [$V_{BB,1}$, $V_{BB,2}$, … $V_{BB,N}$] are recombined to reject the unwanted harmonics and to retain the desired RF signal around $3f_{LO}$. In this fashion, the fundamental harmonic of the LO is rejected while selecting the third harmonic of the square-wave. There is a conversion gain reduction in the relative amplitude of the third harmonic of the LO that can be compensated at the baseband stages.

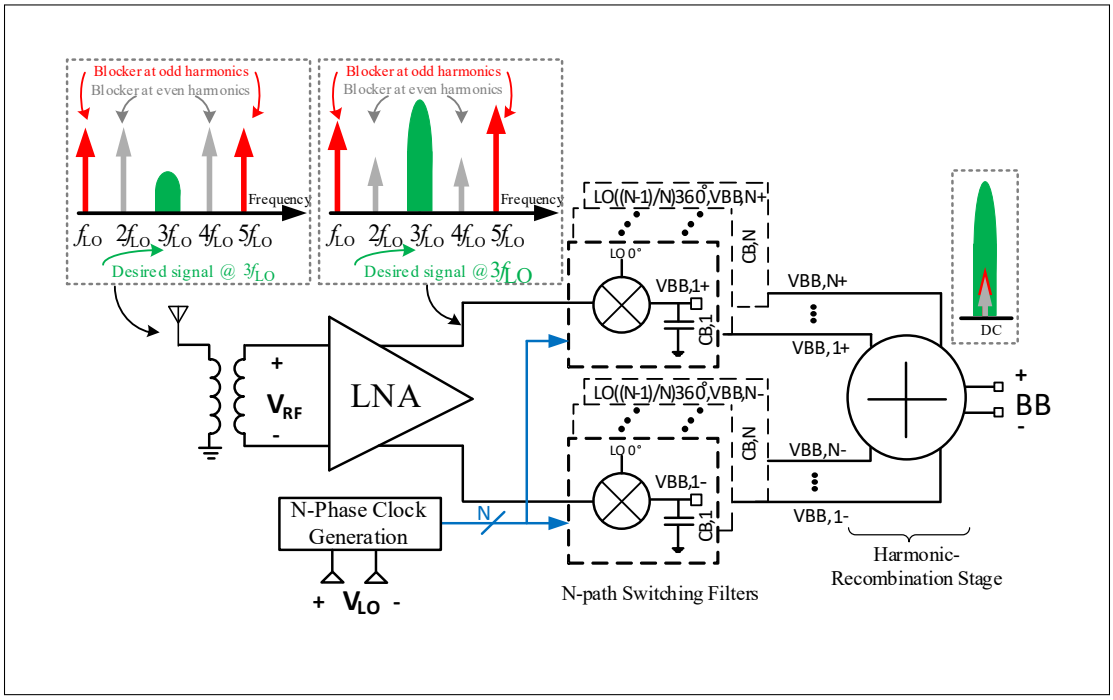

Figure 2.3 Operating principle of the proposed harmonic recombination RF receiver

Fig. 2.4 shows three architectures of the proposed 5.7 – 7.2 GHz RF receiver front-end employing an 4-path, 8-path and 16-path switching filters, and the harmonic recombination implementation at baseband. The required LO frequency ranges from 1.9 to 2.4 GHz to support the aforementioned operating RF band. The weighed baseband harmonic recombination G_m stages appropriately combine the baseband signals to equivalently generate an approximation of $A_c \times sin(\rho\omega_{LO}t + \varphi_0)$, where ρ is equal to 3. Because of the use of an N-path switching filter, the LO signal is divided into N equal time intervals with pulse widths of $1/Nf_{LO}$. Thus, the

voltage gain of each corresponding G_m stage is achieved by (2.16), as discussed before. The combination of the N-path filters and mixing of the baseband ratioed G_m outputs allow for the selection of the third harmonic of f_{LO} and rejection of the fundamental harmonic.

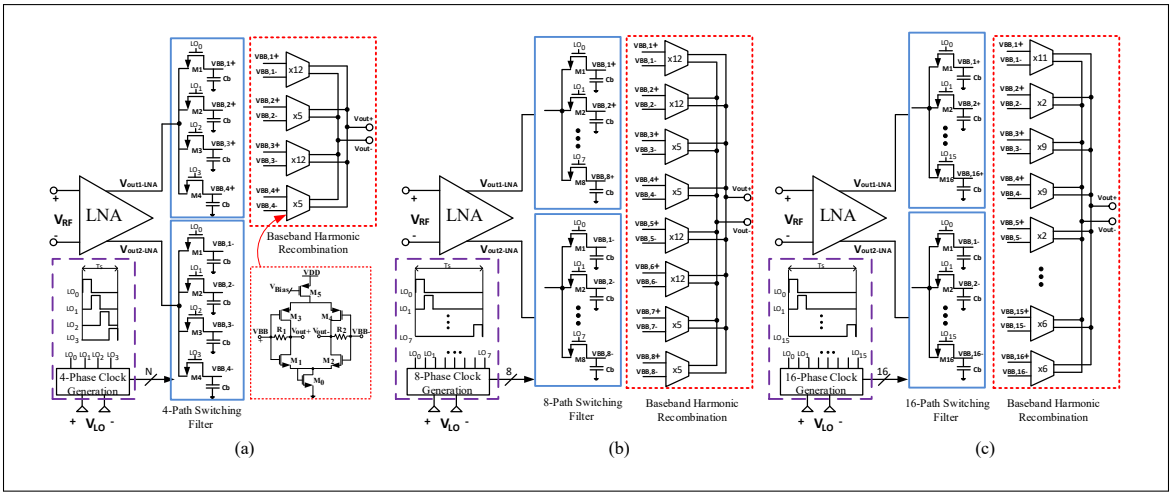

Figure 2.4 Architecture of the harmonic recombination RF receiver front-end using a (a) 4-path switching system, (b) 8-path switching system, and (c) 16-path switching system

Fig. 2.5 illustrates the third harmonic selection with phasor diagrams, along with the first and fifth harmonic rejection at the output of the baseband harmonic recombination circuit for the 8-path HR receiver. This assumes $[GM_1, GM_2, ..., GM_8]$ are weighed baseband harmonic recombination G_m stages (Fig. 2.4 (b)) so that $GM_1 = 12G_m$, $GM_2 = -12G_m$, $GM_3 = 5G_m$, etc. As shown in Fig. 2.5, the first and fifth order harmonics are cancelled, while the third harmonic signal vectors constructively add. Note that since the vectors of $[GM_5, ..., GM_8]$ with respect to their amplitude and phase are identical to vectors of $[GM_1, ..., GM_4]$, the phasor diagrams only show the $[GM_1, ..., GM_4]$ vectors.

2.4.1 Comparison of the RF front-ends using 4-path, 8-path and 16-path mixing

Typically, 4-path switching mixers are employed in the state-of-the-art in both software-defined radios (SDRs) and RFICs to enable frequency-flexible receivers (Borremans, Mandal, Giannini, Debaillie, Ingels, Sano, Verbruggen & Craninckx (2011); Wu, Chang, Chen, Chiu, Lai, Wang,

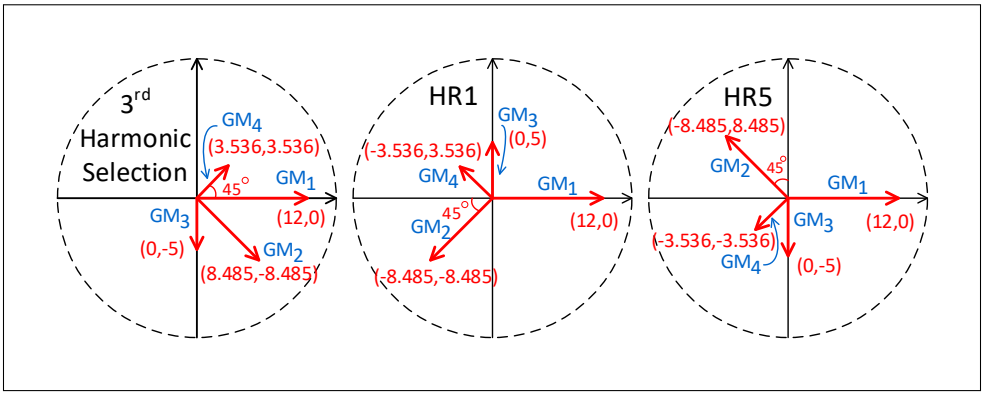

Figure 2.5 Phasor diagrams of the 3^{rd} harmonic selection, along with the 1^{st} and 5^{th} harmonic rejection for the 8-path HR receiver

Yang, Lin, Chen, Tsai et al. (2013)). However, 4-path mixers intrinsically show non-negligible response at higher harmonics of the switching frequency (Molnar & Andrews (2012)). Thus, when there is a blocker at such frequencies, the front-end is inevitably desensitized.

High-order (e.g., 8-path or 16-path) switching filter-based circuits achieve higher HR (Murphy *et al.* (2012)) or higher OOB-IIP3 (Darvishi, van der Zee & Nauta (2013b)) at the cost of more complexity compared to 4-path filters. Additionally, N-path switching filters suffer from harmonic foldback which is due to their time-variant nature (Hemati & Jannesari (2017)). These folding products can be suppressed either by employing a low-pass pre-filter in front of the N-path filter or by increasing the number of paths, N, thus widening the distance between f_{LO} and $(N-1)f_{LO}$, the first folding harmonic (Ghaffari, Klumperink, Soer & Nauta (2011)). The former approach precludes the receiver from having a tunable RF frequency. The latter approach makes the design more complex and increases the power consumption significantly in the multi-phase clock generator, especially when operating at higher RF frequencies.

Increasing the number of paths, N, more accurately approximates a sinusoidal LO. It thus increases the HR ratios, reduces the harmonic foldback and reduces the NF. This is at the cost of higher power consumption due to the increased number of paths. Thus, there is a trade-off between the NF performance and the power consumption or the circuit complexity. In order to

outline this trade-off, three harmonic rejection receivers front-ends are designed using 4-path, 8-path and 16-path switching filters.

Fig. 2.4(a) shows the block diagram of the receiver using a 4-path filter. Two 4-path switching filters are connected to the output of the LNA. The harmonic recombination at the baseband recombines the four differential baseband voltages ($V_{BB,1+}$, …, $V_{BB,4+}$ and $V_{BB,1-}$, …, $V_{BB,4-}$) from the RF front-end, and provides the differential baseband outputs of V_{out+} and V_{out-}. Fig. 2.4(b) and Fig. 2.4(c) illustrate the harmonic selection RF receiver employing 8-path and 16-path switching filters with 8 and 16 differential G_m cells for harmonic recombination, respectively. The weighting ratios of the G_m cells are calculated by using (2.16) with $N = 4, 8$ and 16. The NMOS switches in the 4-, 8- and 16-path filters are derived by a set of 25 %, 12.5 % and 6.25 % duty-cycle non-overlapping clocks, respectively.

Clearly, driving the switches of the 16-path filter beyond 3 GHz increases power consumption significantly, even in smaller geometry CMOS technologies. As a result, when considering the design challenges related to the N-path filter, including the number of switches, power consumption of the LO phases generation circuitry and NF performance, an 8-path switching filter system is preferred to provide a trade-off between the harmonic folding back effects, NF, complexity and power consumption. This will be demonstrated in the section 2.5.

2.5 Circuit Implementation

The HR receiver front-end based on the proposed architecture has been designed in TSMC 65 nm CMOS technology ($N = 4, 8, 16$) and in TSMC 130 nm CMOS technology ($N = 8$) to illustrate the impact of larger transistor geometries on the proposed architecture. The signal path consists of a differential wideband LNA, two N-path switching filters and harmonic recombination-weighting via G_m cells (Fig. 2.4). The N-phase clock is generated by employing flip-flops and is derived by an off-chip differential signal. The following subsections describe the key blocks in more detail.

2.5.1 Differential wideband low noise amplifier

The LNA is implemented as a push-pull capacitive cross coupling (CCC)-common-gate (CG) configuration, and is shown in Fig. 2.6(a). It operates in the 5 to 8 GHz frequency range. The core of the differential wideband LNA is composed of the combination of shunt feedback (SFB) (Pan, Qin, Ye & Wang (2016); Wang, Niknejad & Brodersen (2006)), CG (Khurram & Hasan (2011)), current reuse (Li, Cheng & Wang (2018); Li *et al.* (2018)) and CCC (Belmas, Hameau & Fournier (2012)) topologies. Transistors M_{1A} and M_{1B} in one branch are cross-connected with M_{2A} and M_{2B} in the other branch. This capacitive cross-coupled common gate topology doubles the effective transconductance g_m, reducing the NF. In addition, using the push-pull architecture of M_{1A} and M_{1B} (M_{2A} and M_{2B}) further increases the effective g_m without requiring extra current. Low threshold voltage transistors are used in the design of the LNA.

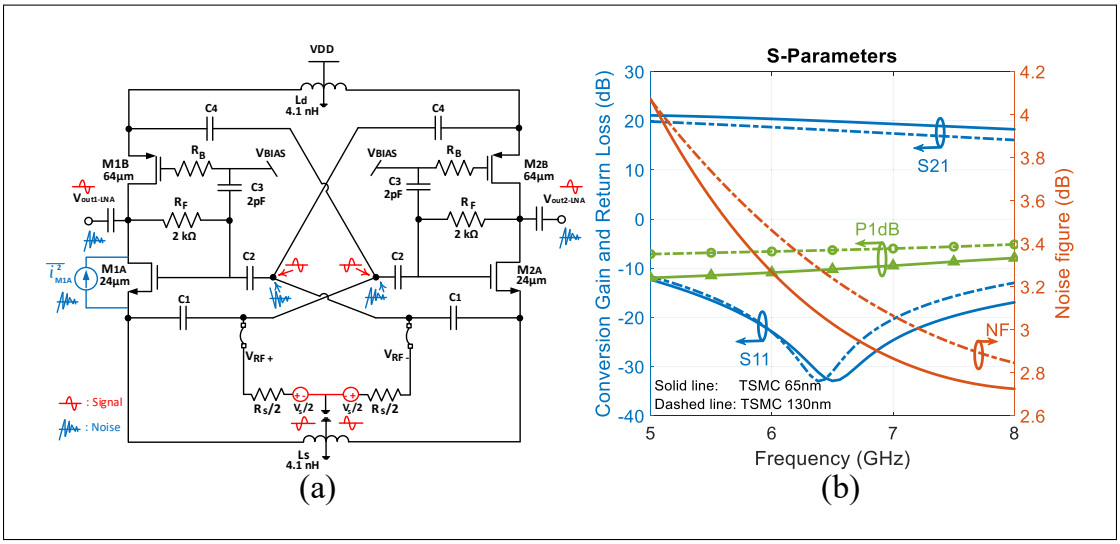

Figure 2.6 (a) Differential wideband LNA, and (b) its Gain (S21), return loss (S11), NF and 1-dB compression point (P1dB)

To provide the bias current paths for the LNA, and also to benefit from the symmetric structure, two center-tapped on-chip inductors, L_s and L_d, are connected to the source of the NMOS and PMOS transistors. The values of these inductors are chosen to resonate with the transistors'

C_{gs} and also with the input parasitic capacitance extracted from the layout at the frequency of interest. Moreover, shunt feedback resistors R_F provide the input impedance matching. At low frequencies, the differential input impedance using small signal equivalent circuit is given by

$$Z_{in} = \frac{R_F + r_{o_{M1A}} || r_{o_{M1B}}}{2(1 + (g_{m_{M1A}} + g_{m_{M1B}}) r_{o_{M1A}} || r_{o_{M1B}})}. \tag{2.23}$$

The input matching ($Z_{in} = R_s$) is achieved by

$$r_o + R_F = 2(1 + (g_{m_{M1A}} + g_{m_{M1B}}) r_o) R_s, \tag{2.24}$$

where the output resistance of r_o is $r_{o_{M1A}} || r_{o_{M1B}}$.

The bias separation of M_{1A} and M_{1B} (M_{2A} and M_{2B}) and their sizing optimization enables the wide bandwidth operation. In addition, the output noise of M_{1A} and M_{1B} (M_{2A} and M_{2B}) is partially cancelled by using the cross connection and differential outputs, while the amplitudes are doubled.

The generated noise by the transistors that affect the noise factor are modeled as a parallel current source with the transistors. To simplify the noise factor analysis, all capacitive effects are ignored. The transfer functions of transistor noise currents i_{M1A} and i_{M1B} to $V_{out1_{LNA}}$ and i_{M1A} and i_{M1B} to $V_{out2_{LNA}}$ are derived as

$$TF_{i_{M1AB,out1}} = \frac{1}{2}\left(\frac{R_F r_o}{r_o + R_F} + \frac{(R_F + R_s) r_o}{2R_s(1 + (g_{m_{M1A}} + g_{m_{M1B}}) r_o) + r_o + R_F}\right), \tag{2.25}$$

$$TF_{i_{M1AB,out2}} = \frac{1}{2}\left(-\frac{R_F r_o}{r_o + R_F} + \frac{(R_F + R_s) r_o}{2R_s(1 + (g_{m_{M1A}} + g_{m_{M1B}}) r_o) + r_o + R_F}\right), \tag{2.26}$$

By considering input matching conditions of (2.24) and the following conditions

$$(g_{m_{M1A}} + g_{m_{M1B}}) r_o \gg 1, \tag{2.27}$$

$$(g_{m_{M1A}} + g_{m_{M1B}}) R_F \gg 1, \tag{2.28}$$

(2.25) and (2.26) can be simplified as

$$TF_{i_{M1AB,out1}} \approx \frac{3R_F}{8(g_{m_{M1A}} + g_{m_{M1B}})R_s}, \tag{2.29}$$

$$TF_{i_{M1AB,out2}} \approx \frac{R_F}{8(g_{m_{M1A}} + g_{m_{M1B}})R_s}. \tag{2.30}$$

From (2.29) and (2.30), the noise generated by $M1A$ and $M1B$ has the same polarity at nodes $V_{out1,LNA}$ and $V_{out2,LNA}$. Thus, the noise with the ratio of $TF_{i_{M1AB,out2}}/TF_{i_{M1AB,out1}} = 1/3$ is partially cancelled. The transfer function of i_{M1A} to $V_{out1,LNA} - V_{out2,LNA}$ is given by

$$T_{i_{M1AB}} = TF_{i_{MAB,out1}} - TF_{i_{MAB,out2}} = \frac{R_F}{4(g_{m_{M1A}} + g_{m_{M1B}})R_s}. \tag{2.31}$$

Using the same method, the transfer functions for the noise currents of i_{R_s} and i_{R_F} to the differential outputs are given by

$$TF_{i_{R_s}} = TF_{i_{R_s,out1}} - TF_{i_{R_s,out2}} = \frac{R_s}{4} - \frac{-R_s}{4} = \frac{R_s}{2}, \tag{2.32}$$

$$TF_{i_{R_F}} = TF_{i_{R_F,out1}} - TF_{i_{R_F,out2}} = \frac{R_F(2r_o + R_F)}{2(r_o + R_F)}. \tag{2.33}$$

While there is no cancellation for the generated noise by the source resistor and shunt feedback resistors, the noise currents of M_{1A} and M_{1B} (and M_{2A} and M_{2B}) are partially cancelled, leading to an improved noise factor, as M_{1A} and M_{1B} (M_{2A} and M_{2B}) are important noise contributors.

Finally, by considering the major noise components including thermal noise of the resistors and thermal channel noise of the transistors, the total noise factor can be expressed as (Shams, Abbasi & Nabki (2020))

$$F \approx 1 + \frac{\gamma}{2(g_{m_{MA}} + g_{m_{MB}})R_s} + \frac{2R_s}{R_F} \times \left(1 + \frac{r_{o_{MA}} || r_{o_{MB}}}{r_{o_{MA}} || r_{o_{MB}} + R_F}\right)^2, \tag{2.34}$$

where $g_{m_{MA}}$ and $g_{m_{MB}}$ and γ represent $g_{m_{M1A}} + g_{m_{M2A}}$, $g_{m_{M1B}} + g_{m_{M2B}}$ and the channel length modulation, respectively. The noise contributed by M_{1A} and M_{1B} (M_{2A} and M_{2B}) is one-fourth

of the generated noise by the main transistors in a typical differential SFB LNA (i.e., $\frac{2\gamma}{g_{m_M} R_s}$). The last term is due to the feedback resistance R_F. While it experiences no noise cancellation, it can have a minor impact on the overall NF when increasing R_F. In this fashion, the overall NF of the LNA is reduced.

Fig. 2.6(b) shows the flat voltage gain (i.e., S21) of 20 dB over the desired frequency band from 5 −8 GHz. The input return loss (i.e., S11) and NF are less than −10 dB and 4 dB over the entire frequency band of interest, respectively. Moreover, Fig. 2.6(b) shows the 1-dB compression point, P1dB, at different frequency inputs with a −40 dBm input amplitude. The P1dB variation is small over the entire frequency band and is higher than −12 dBm.

The LO frequency range in the third harmonic selection receiver varies from 1.9 to 2.4 GHz, which is one of the busiest spectrum that carries majority of the LTE and ISM traffic. It should be mentioned that when an input RF signal operating at 1.9 −2.4 GHz is applied to the LNA, it experiences less than 4 dB amplification, while the LNA amplifies the targeted input RF signal operating at 5.7 −7.2 GHz by up to 20 dB. Moreover, the input matching of the LNA in the 1.9 −2.4 GHz range is mistuned and will result in significant reflection of interferers in that range.

2.5.2 N-path switching filter

Two N-path switching filters are connected to the output of the LNA (Fig. 2.4). The baseband capacitors ($C_{BB,1}$, $C_{BB,2}$, …, $C_{BB,N}$, $N = 4, 8, 16$) are realized with MIM capacitors to ground. The NMOS switches are derived by a set of 1/N duty-cycle non-overlapping clocks. For example, the gate of the 16 NMOS switches in the 16-path HR receiver are capacitively coupled to the 16 LO clock phases. The switches are biased at a 600 mV DC voltage in order to set a 1.2 V swing on their gate-source. This swing provides the maximum achievable linearity for the fixed-size switches. The switches in the N-path filter are realized by low threshold voltage transistors. Increasing switch size reduces the switch resistance and will improve linearity. However, the resulting larger switches exhibit larger parasitic capacitance, causing clock leakage, reduced operating frequency range and increased power consumption for the clock generator to drive

the switches. Thus, the W/L ratio of the switch transistors in the switching filter is chosen to be 4 µm / 60 nm in the 65 nm implementation, and the equivalent switch resistance is equal to 56.9 Ω (g_{ds} = 17.56 mS).

In the proposed HR receiver, the LO clock generator was designed to operate properly for the worst process corner (i.e., SS corner). The generated LO signals are sharp enough to mitigate the different threshold voltage effects for different corners. However, in future work, a variable bias voltage could be designed by employing a replica transistor to track the switching transistors.

Note that the bandwidth of the N-path filter is a function of the filter's time constant. In each path of an N-Path switching filter, the RC network performs integration on the input signal, when the corresponding NMOS switch is turned on. During a given on-time of the switch, there is no need for the voltage to be settled, as opposed to what is required in a sampling system. Thus, the size of the baseband capacitor is independent of the LO frequency and can be specified based on the desired bandwidth. The switches do not dissipate dynamic power since they will be statically driven. The size of the switches can be larger than that of the main clocked switches in the N-path filter since the parasitic capacitances of the switches can be absorbed in the desired capacitance. However, the maximum achievable bandwidth of the N-path filter is limited by the capacitive load of the subsequent stage. Thus, the IF bandwidth of the 16-path HR receiver is lower than that of the 4- and 8-path HR receivers due to the 16 G_m cells in the following stage.

2.5.3 Baseband harmonic recombination transconductors

The harmonic recombination at the baseband, as shown in Fig. 2.4, recombines the differential baseband voltages ($V_{BB,1+}$, $V_{BB,2+}$, … $V_{BB,N+}$ and $V_{BB,1-}$, $V_{BB,2-}$, … $V_{BB,N-}$) from the RF front-end, and provides the differential baseband outputs of V_{out+} and V_{out-}. In the 4- and 8-path HR receivers, the differential 4- and 8-phase outputs are converted into currents by 4 and 8 differential G_m cells with a weighting ratio of 12 : 5 calculated using (2.16) with $\varphi_0 = 22.5^o$ and N = 4 and 8, respectively (Fig. 2.4(a) and (b)). However, the 16 G_m cells in the 16-path HR receiver are weighted with the ratios of 11 : 2 : 9 : 6 calculated with (2.16).

Fig. 2.4(a) also depicts the self-biased G_m circuit, where each G_m unit cell contains two resistive common-mode feedback resistors, R_1 and R_2. The harmonic recombination used in N. Shams & Nabki (2020) employs $12G_m$ and $5G_m$ unit cells composed of 12 R_1 (R_2) and 5 R_1 (R_2) resistors configured in parallel. Thus, there is a need of 68 R_1 resistors (and 68 R_2 resistors). This would occupy a relatively large area. Accordingly, in order to reduce this area, an alternative approach is to share the R_1 and R_2 resistors for the $12G_m$ unit cells. In other words, instead of using 12 R_1 and 12 R_2 resistors in the $12G_m$ unit cells, one R_1 resistor and one R_2 resistor are employed in the $12G_m$ unit cells. This resistor sharing approach reduces the required number of R_1 and R_2 resistors to 17 rather than 68 in the 8-path HR receiver. Resistors R_1 and R_2 were set to 50 kΩ, and the transconductance of the G_m cell is equal to 80 μS. Similar resistor sharing is also applied in the 4- and 16-path HR receivers. Each G_m unit cell consumes 156 µW from a 1.2 V supply in the 65 nm implementation.

2.5.4 N-phase non-overlapping clock generation

The use of two N-path switching filters (as shown in Fig. 2.4) complicates the design of the LO clock signal. The multi-phase non-overlapping clock generation with $1/N$ duty cycle consumes considerable amount of power.

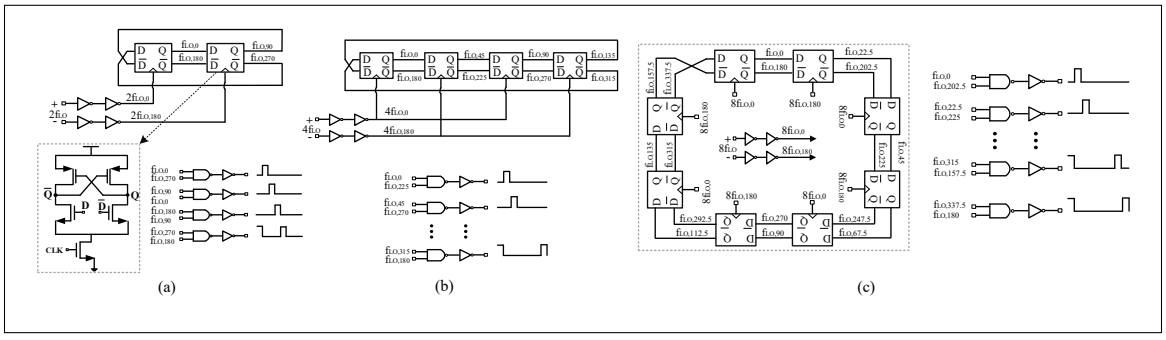

Figure 2.7 4-phase clock generation circuit, (b) 8-phase clock generation circuit, (c) 16-phase clock generation circuit

Fig. 2.7 depicts the structure of the 4-, 8- and 16-phase clock generators that is used in this work. For an 8-phase LO clock, the required input signal of the LO operates at four times of

the switching frequency. The 8-phase LO generation shown in Fig. 2.7(b) consists of a ring flip-flop based divider consisting of four latches to generate eight phases with 50 % duty cycle at the switching frequency. Then, these eight clocks are AND'ed together to convert the clocks from a 50 % to a 12.5 % duty cycle, and to ensure non-overlapping clocks. The divider can operate from 80 MHz up to 3 GHz in 65 nm, limited by the capacitive load of the 8-path switching system. In a similar fashion, the 4-phase and 16-phase non-overlapping clocks are achieved by employing two flip-flops in a ring (see Fig. 2.7(a)) and a ring of eight flip-flops (Fig. 2.7(c)), respectively.

During start-up, the first flip-flop output is set to VDD and the other flip-flops' outputs are set to ground. Then, a clock activates the flip-flop-based ring divider and multiphase clocks with $1/N$ duty cycle are generated at the flip-flops' output. It should be mentioned that the flip-flops are buffered with minimum loads to prevent output signals for potentially going into a metastable state. Moreover, as can be seen in Fig. 2.7, the input signals are buffered before connecting to the flip-flops in order to ensure an input amplitude of 1.2 V_{pk-pk}, and avoid metastability due to intermediate voltages.

2.6 Post-layout Simulations Results

The three proposed harmonic selection RF receiver front-end architectures are implemented in TSMC 65 nm CMOS. Moreover, the 8-path architecture is also implemented in TSMC 130 nm CMOS in order to outline the impact of technology scaling on the proposed architecture. Post-layout simulation results, along with process corner analyses, are presented. Moreover the 4-phase mixer conventional receiver shown in Fig. 2.1 is also implemented in TSMC 65 nm CMOS in order to outline the advantages of the proposed HR receivers.

Fig. 2.8 shows the respective layouts of RF receiver using 4-path (Fig. 2.8(a)), 8-path (Fig. 2.8(b)) and 16-path (Fig. 2.8(c)) switching systems, outlining their active areas of 0.19 mm^2, 0.25 mm^2 and 0.38 mm^2, respectively. As can be seen, more area is occupied as the number of paths, N, is increased. Note that the conventional receiver shown in Fig. 2.1 was also laid out. While the baseband paths between the conventional receiver and the 4-path HR receivers

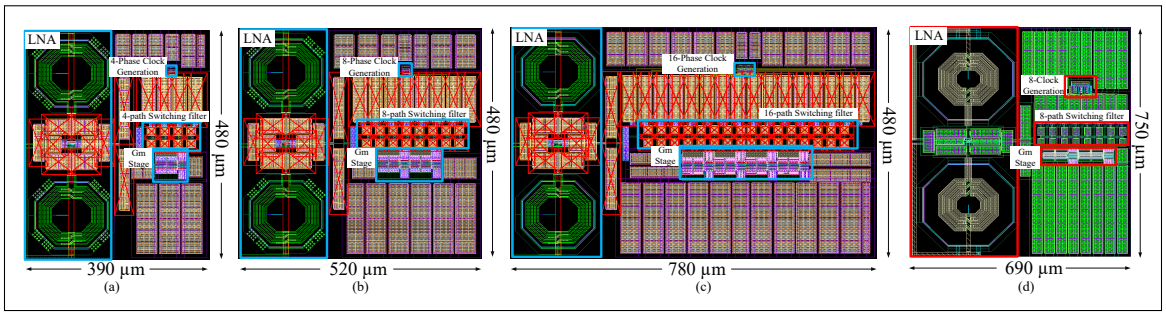

Figure 2.8 Layout of the proposed harmonic recombination receiver using a (a) 4-path switching filter, (b) 8-path switching filter, (c) 16-path switching filter in TSMC 65 nm CMOS having dimensions of 390 µm × 480 µm, 520 µm × 480 µm and 780 µm × 480 µm, respectively, and (d) layout of the proposed harmonic recombination receiver using an 8-path filter in TSMC 130 nm CMOS having dimensions of 690 µm × 750 µm

are different (i.e., G_m stages), there is no significant difference in terms or area required to implement both architectures. Thus, Fig. 2.8 does not show the conventional receiver's layout. Fig. 2.8(d) shows the 8-path architecture implemented in 130 nm CMOS, having an area of 0.52 mm^2, which is approximately twice the size of the 65 nm CMOS comparable implementation. Post-layout simulations include all of the extracted resistive and capacitive parasitics and the RF models of the inductors.

In addition, a bond-wire packaging model, shown in Fig. 2.9(a) and (b), is considered in the post-layout simulations. A differential model shown in Fig. 2.9(a) is used for the LNA, and a single-ended model is used for other pins, as shown in Fig. 2.9(b). Note that $Z_{In,LNA}$ in Fig. 2.9(a) is the input of the LNA before connecting to the bond-wire model, and is equal to $100 + 13.72j\ \Omega$ at frequency of 6 GHz in 65 nm CMOS. Consider the equivalent half-circuit bond-wire model. Then, after connecting the bond-wire to the input of the LNA ($Z_{In,LNA}$), the input impedance of Z_{IN} can be calculated by

$$Z_{\text{IN,half-circuit}} = ((\frac{Z_{In,LNA}}{2} || \frac{1}{j\omega C_3}) + j\omega L + R) || \frac{1}{j\omega(C_2 + 2C_1)} = 50.203 + 6.8j\Omega, \qquad (2.35)$$

Thus, Z_{IN} is equal to $100.4 + 13.74j\Omega$. The post-layout simulation results are presented in subsections of 2.6.1-2.6.6.

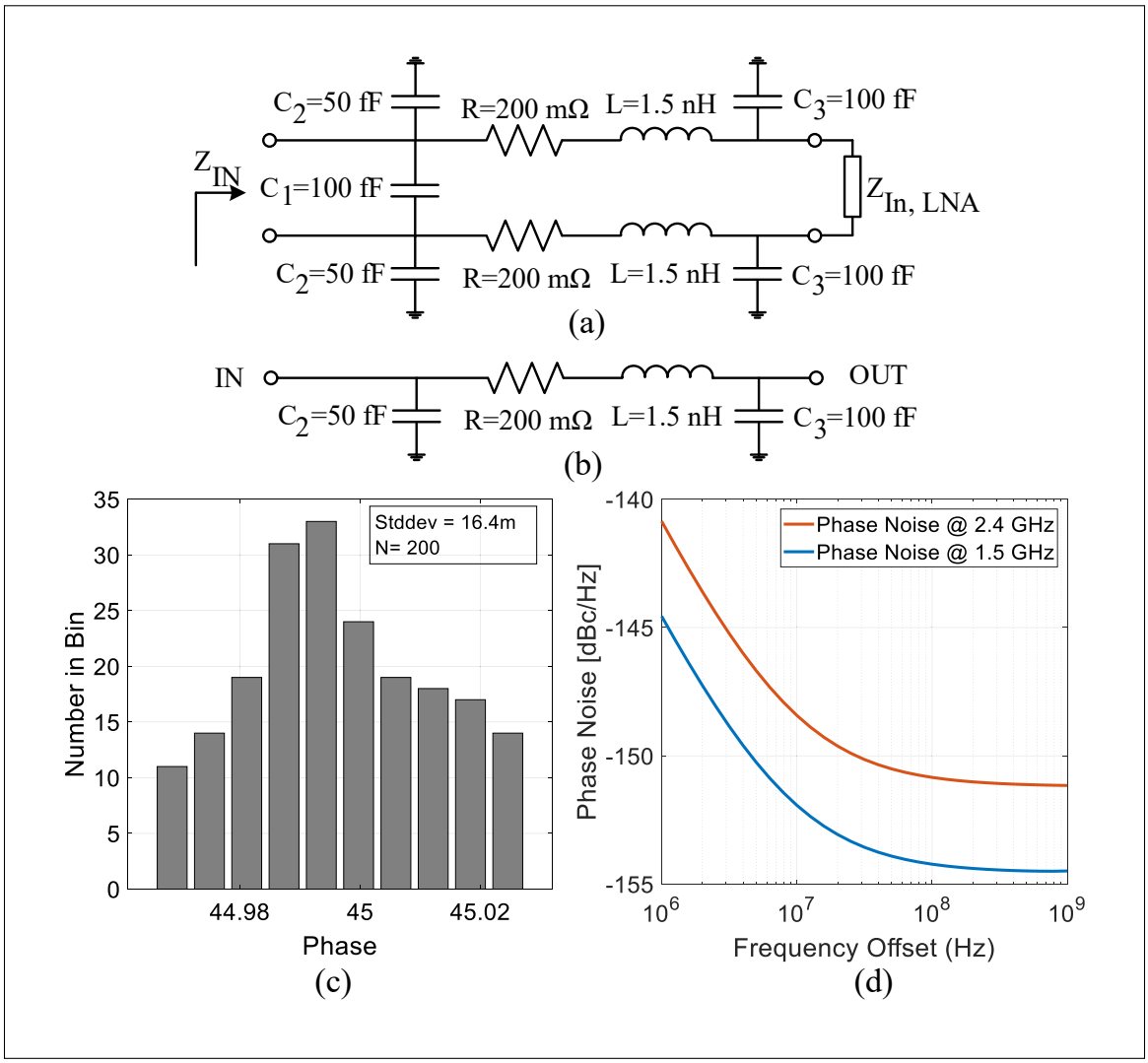

Figure 2.9 Bond-wire packaging model for (a) differential LNA input, and (b) single-ended pins, (c) post-layout simulated histogram of the phase deviation from 45^o between two adjacent 2.4 GHz LO clocks and (d) the output phase noise of the 8-phase LO clock generator vs. frequency offset

2.6.1 LO performance

Dynamic switching power for the LO is calculated as

$$P_{\text{LO}} = \eta f_{LO} C_{eff} V_{dd}^2, \tag{2.36}$$

where η, f_{LO}, C_{eff} and V_{dd} are the activity factor, switching frequency, the internal and load capacitances, and the supply voltage, respectively.

Fig. 2.9(c) presents the phase difference from Monte Carlo simulations at 45^o between two adjacent clocks due to mismatch in 65 nm CMOS. The histogram illustrates a maximum phase error of only 0.03^o and it achieves $\sigma = 0.0164^o$ for 2.4 GHz. Moreover, the maximum phase error of the 4- and 16-phase clock generators are of 0.02^o at 90^o with $\sigma = 0.0125^o$ and 0.07^o at 22.5^o with $\sigma = 0.024^o$, respectively.

Fig. 2.9(d) shows the output phase noise of the 8-phase LO clock generator. Since the latches are derived with a master clock, the phase noise is low. For 6 GHz and 9.6 GHz input signals ($f_{LO} = 6\,GHz/4 = 1.5\,GHz$ or $f_{LO} = 9.6\,GHz/4 = 2.4\,GHz$), the post-layout simulated phase noise of the 8-phase LO generator is less than -154.1 dBc/Hz and -150.8 dBc/Hz, respectively, at an 80 MHz offset. Assuming that the receiver is free from gain compression and benefits from a perfectly linear down-conversion mixer, there is still a significant amount of noise due to the reciprocal mixing in the receive band. Under reciprocal mixing, the NF derived by the receiver's blocker can be calculated by

$$\mathrm{NF_{blocker}} \approx 174 \left[\frac{dBm}{Hz}\right]^{-1} + P_d\,[dBm] + L_\omega\,[\Delta\omega] \left[\frac{dBc}{Hz}\right], \tag{2.37}$$

where P_d and $L_\omega[\Delta\omega]$ are the blocker power and the LO phase noise at the blocker offset $\Delta\omega$, respectively. The NF of the receiver in the presence of a 0 dBm blocker and the phase noise of -150.8 dBc/Hz is predicted to be 23.2 dB. This noise degradation is due to the reciprocal mixing of the phase noise in the presence of a 0 dBm blocker.

Accordingly, the clock generation relaxes the phase noise of the divider while consuming low power. The post-layout simulation results shows that the 8-phase LO generation circuit consumes between 2.5 and 3.3 mW from a 1.2 V supply in 65 nm technology, depending on the LO frequency. When the LO frequency is set to 1.9 GHz, the LO generation consumes 2.5 mW, while dissipating 3.3 mW at $f_{LO} = 2.4$ GHz. The 4-phase and 16-phase LO clock generators consume up to 2.1 mW and 12.5 mW, respectively. This is significantly lower than what would

be required using a conventional implementation operating at a much higher LO (e.g., 6 GHz). As such, in the proposed receiver architecture, the dynamic power consumption is reduced by a factor of three because of the selection by the HR-NPF of the third harmonic of the LO frequency in order to operate over the higher operation frequencies targeted ($3f_{LO}$ = 5.7 −7.2 GHz).

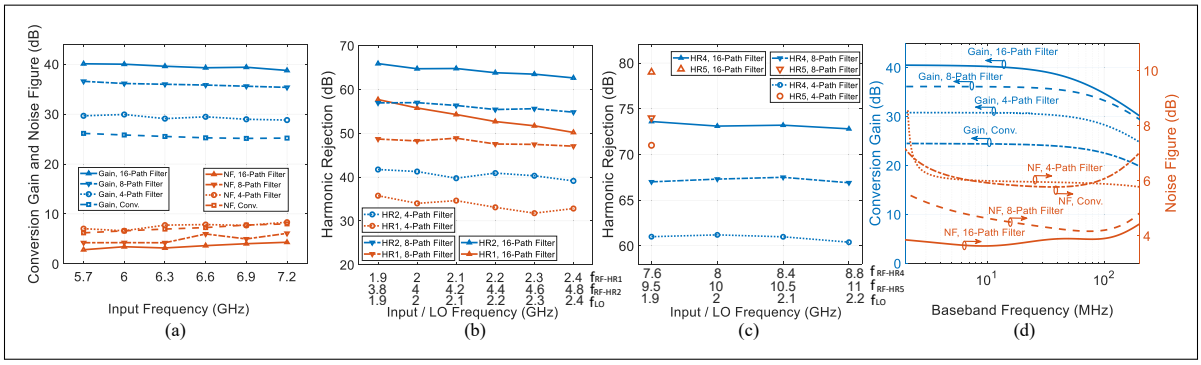

Figure 2.10 Post-layout simulation performance of the conventional receiver along with that of the proposed RF receivers using 4-, 8- and 16-path switching systems: (a) Conversion gain and NF vs. input frequency at baseband frequency of 40 MHz (LO frequency is 5.7 −7.2 GHz for conventional receiver and 1.9 −2.4 GHz for HR receivers), (b) 1^{st} and 2^{nd} HRRs (HR1 and HR2) vs. Input/LO frequency, (c) 4^{th} and 5^{th} HRRs (HR4 and HR5) vs. Input/LO frequency, and (d) conversion gain and NF for a 6 GHz RF input (f_{LO} = 2 GHz in the proposed architectures) vs. the baseband frequency

2.6.2 Performance comparison of the conventional and the proposed HR receivers

Fig. 2.10 shows the performance of the conventional receiver (shown in Fig. 2.1) along with that of the proposed RF receivers using 4-, 8- and 16-path switching systems. The N-path filter structures benefits from frequency tunability that can be achieved by changing the LO clock frequency. By varying the LO input frequency from 1.9 to 2.4 GHz, the RF receiver covers the entire RF frequency band of interest (i.e., 5.7 −7.2 GHz), since the proposed harmonic selection RF receiver front-end operates at the third harmonic of the LO frequency, as previously discussed. Consequently, in the conventional receiver, the LO input frequency varies from 5.7 −7.2 GHz since it operates at the fundamental LO frequency. In the proposed RF receiver architectures, the set of G_m stages and the two feed-forward N-path switching filters provide a conversion gain from RF to baseband.

The RF to baseband conversion gain and double-side band (DSB) NF vs. LO frequency at a baseband frequency of 40 MHz are shown in Fig. 2.10(a) in 65 nm CMOS. The conventional receiver, 4-, 8- and 16-path HR receivers achieve a conversion gain of 24.8 dB, 29.9 dB, 36.4 dB and 38.9 dB, respectively. The achieved NF of the conventional receiver, 4-, 8- and 16-path HR receivers is of 5.8 dB, 5.9 dB, 4.4 dB and 3.8 dB, respectively, at an LO frequency of 6 GHz in the conventional receiver and 2 GHz in the proposed receivers. Fig. 2.10(a) shows a relatively flat gain and NF up to a 7.2 GHz RF input frequency (i.e., the third harmonic of a 2.4 GHz LO in the proposed HR receivers and the fundamental of the LO in the conventional receiver).

Compared to the conventional receiver, the proposed HR receivers provide higher gain due the set of G_m stages. Note that in the proposed architectures, the switching filter conversion gain reduces when selecting an LO factor larger than 1 because of the sinc roll-off that results from the zero-order hold. For example, in a 16-path switching filter, the conversion gain at $3f_{LO}$ is smaller than the gain at f_{LO}. However, this small attenuation is compensated in the baseband by employing 16 weighted G_m cell stages. Therefore, the 16-path HR receiver having 16 weighted G_m stages provides higher gain, compared to the conventional receiver having one G_m stage. More importantly, the NF is reduced by increasing the number of paths due to a more accurately approximated sinusoidal LO, allowing for a lower NF to that of the conventional receiver for the 8-path and 16-path receivers.

The 1^{st} and 2^{nd} harmonic rejection ratios (HRR) vs. LO frequency are post-layout simulated and plotted in Fig. 2.10(b). The HRR is generally defined as the ratio of the conversion gain at the selected effective LO nf_{LO} to the gain at any other attenuated harmonic of f_{LO}. For example for the proposed architecture, when the switching frequency is of 2.3 GHz, the first HRR for this LO frequency is calculated by dividing the gain at 2.3 GHz by the gain at 6.9 GHz, which is the 3^{rd} harmonic frequency and the desired RF signal. The 1^{st} and 2^{nd} HRRs (HR1 and HR2) are both higher than 47 dB at any LO frequency for both 8- and 16-path filters. Note that the conventional receiver operates at the fundamental harmonic of its LO (i.e., 5.7 −7.2 GHz) and its 2^{nd}, 3^{rd}, 4^{th} and 5^{th} harmonic frequencies are higher than 10 GHz, and thus they are not plotted in Fig. 2.10(b) and Fig. 2.10(c).

Since the RF receiver operates from 5.7 to 7.2 GHz, it is designed to suppress the LO harmonics up to 8 GHz to guarantee proper operation. Thus, HRRs are plotted for input RF frequencies of up to 7.2 GHz for the 1^{st} and 2^{nd} LO harmonics (Fig. 2.10(b)). In addition, Fig. 2.10(c) shows the harmonic rejection ratio when injecting an input at 4 and 5 times of the LO frequency, and the receiver provides higher than 60 dB rejection. In these cases, the HR receiver achieves a high harmonic rejection ratio as these harmonics are beyond the LNA amplification range.

Fig. 2.10(d) depicts the overall NF and conversion gain of the compared receivers vs. the baseband frequency for $f_{LO} = 2$ GHz (i.e., $f_{RF} = 3 \times f_{LO} = 6$ GHz) for the HR receivers and for $f_{LO} = 6$ GHz for the conventional receiver. The 3-dB bandwidth achieved by the conventional receiver, 4-, 8-, and 16-path HR receivers at baseband are of 142 MHz, 120 MHz, 100 MHz and 54 MHz, respectively. As the HR receiver using a 16-path filter generates a LO signal approximation more similar to a pure sine-wave, it shows the lower NF thanks to the noise folding reduction, but has lower baseband bandwidth due to the added parasitics of its more numerous G_m cell stages.

Table 2.1 Post-layout simulation results overview for the conventional and the three proposed receivers (65 nm CMOS)

Parameters	Conv. RX	4-Path HR RX	8-Path HR RX	16-Path HR RX
LO Freq. (GHz)	5.7- 7.2	1.9-2.4	1.9-2.4	1.9-2.4
RF Freq. (GHz)	5.7-7.2	5.7-7.2	5.7-7.2	5.7-7.2
HR1 (dB)*	N/A	34.4	47.6	65
HR2 (dB)*	N/A	42	56.8	51
NF (dB) ‡	5.8	5.9	4.4	3.8
BW (MHz)	142	120	100	54
P_{LNA} (mW)	2.4	2.4	2.4	2.4
$P_{Baseband}$ (mW)	0.310	5.3	10.6	17.4
P_{LO} (mW)	14.7-19.6	1.6-2.1	2.5-3.3	8.4-12.5
P_{Total} (mW)	17.4-22.3	9.3-9.8	15.5-16.3	28.2-32.3
Area (mm^2)	0.19	0.19	0.25	0.38

‡ NF at a 40 MHz baseband frequency. * HR1 and HR2 at $f_{LO} = 2$ GHz

A detailed performance comparison of the HR RF receivers using 4-, 8- and 16-path switching systems to that of the conventional receiver composed of the 4-phase mixer (Fig. 2.1) is shown in Table 2.1. Since the 4-, 8-, and 16-path HR receivers exploit the third harmonic selection architecture, their LO clock frequencies varies from 1.9 to 2.4 GHz to cover the entire RF frequency band of interest (i.e., 5.7 −7.2 GHz), compared to the typical receiver architecture. Thus, power dissipation of the multi-phase LO generator in the third harmonic selection receivers is less than that of in the conventional receiver due to the direct relation of dynamic power with f_{LO}. As previously discussed, it is desired to increase the number of paths, N, to reduce the NF and harmonic foldback effect and increase the HRR. Therefore, if the 5.7 −7.2 GHz conventional receiver was to employ a 16-path switching filter, the oscillator would have to provide a frequency of $8f_{LO}$ (i.e., 45.6 −57.6 GHz), leading to an extremely high power dissipation or to a design that would require a smaller geometry CMOS technology and thus a higher cost. However, the third harmonic selection architecture proposed here helps mitigate this issue and the required frequency of the 16-phase clock generator reduces by a factor of three (i.e., 15.2 −19.2 GHz). However, use of the 16-path switching system in the HR receiver requires more area (see Fig. 2.8(c)) and power consumption, and has narrower bandwidth due to the 16 weighted G_m stages at the baseband.

It should be mentioned that the total power consumption (P_{total}) in Table 2.1 is divided into two parts, analog and digital power consumption. The former includes the LNA and G_m cells blocks (P_{LNA} and $P_{Baseband}$), and the latter is composed of the LO clock generator (P_{LO}). While the DC power consumption is calculated by multiplying the supply voltage and DC current drawn from it, dynamic switching power for the LO is calculated using (36).

The baseband harmonic recombination in the 4-, 8-, and 16-path HR receivers consumes 5.3 mW, 10.6 mW and 17.4 mW from a 1.2 V supply, respectively. The LNA is the same in the all receivers, and consumes 2.4 mW from a 1.2 V supply. As a result, the third harmonic selection receiver using 8-path filter achieves the better trade-off between the NF, BW, area and power consumption, while providing harmonic rejection.

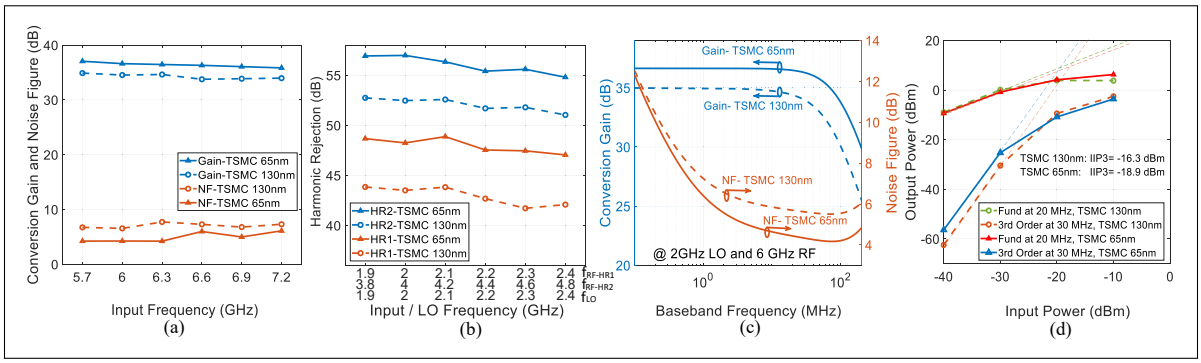

Figure 2.11 Post-layout simulation performance of the proposed 8-path HR receiver implemented in 65 nm and 130 nm CMOS: (a) Conversion gain and NF vs. input frequency (LO frequency is 1.9 −2.4 GHz), (b) 1^{st} and 2^{nd} harmonic rejection ratios (HR1 and HR2) vs. Input/LO frequency and (c) conversion gain and NF for a 6 GHz RF input (f_{LO} = 2 GHz) vs. the baseband frequency, and (d) IIP3 performance

2.6.3 8-path HR receiver performance in two CMOS technologies

Fig. 2.11 compares two 8-path HR receivers designed in 130 nm and 65 nm in terms of conversion gain, NF and 1^{st} and 2^{nd} HRRs. Note that the receivers designed in both technologies are using a 1.2 V supply voltage.

As shown in in Fig. 2.11(a), the 8-path HR receiver implemented in 130 nm achieves a conversion gain of 35 dB and NF of 5.6 dB for an LO frequency of 2 GHz (i.e., RF of 6 GHz), while the receiver designed in 65 nm provides a conversion gain and NF of 36.4 dB and 4.4 dB, respectively at a similar LO frequency. The 1^{st} and 2^{nd} HRRs are both higher than 42 dB at any LO frequency are shown in Fig. 2.11(b). Fig. 2.11(c) depicts the NF and conversion gain of the receiver vs. the baseband frequency for f_{LO} = 2 GHz. At lower baseband frequencies, the NF is significantly affected by the flicker noise. Larger technology nodes however will have considerable parasitic capacitance connected to the filter output, which will limit the achievable baseband bandwidth, as can be seen in the 130 nm implementation.

Both implementations in-band IIP3 performance is plotted in Fig. 2.11(d), and is of −16.3 dBm in 130 nm and −18.9 dBm in 65 nm when injecting two input tones at f_1 = 10 MHz and f_2 = 20 MHz offsets from the 6 GHz RF input (i.e., with f_{LO} = 2 GHz). The input power of the two

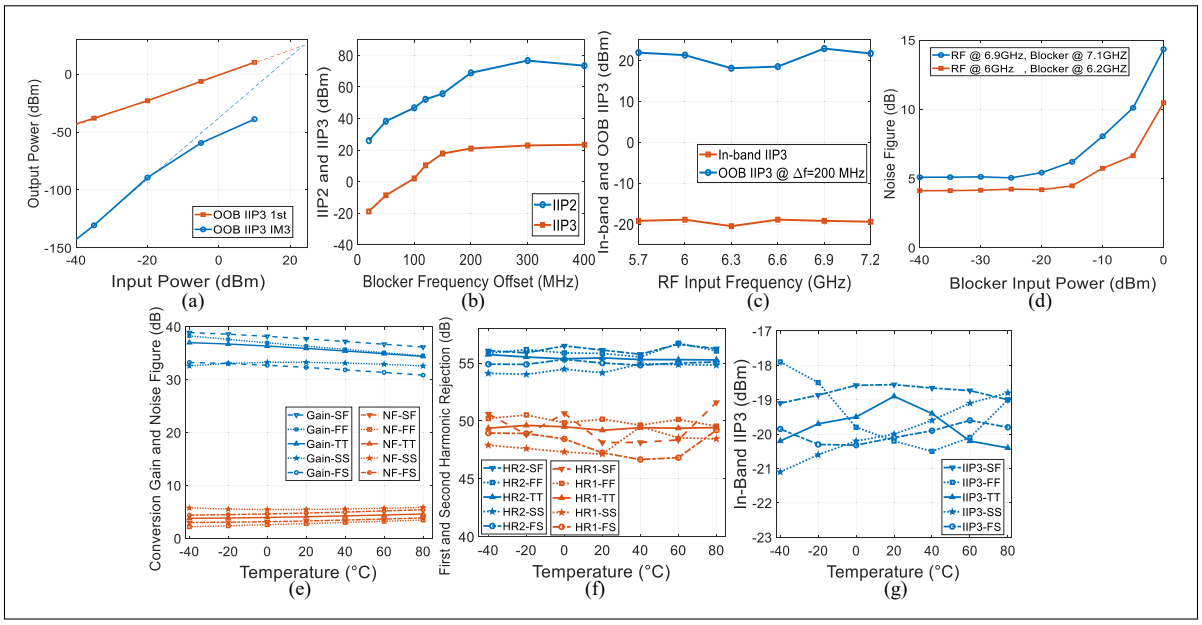

Figure 2.12 Post-layout simulated (a) OOB IIP3 vs. input power for OOB blocker located at a 200 MHz offset, (b) IIP2 and IIP3 vs. blocker offset frequency, and (c) in-band and OOB IIP3 vs. RF input frequency, (d) NF in the presence of a blocker at an offset frequency of 200 MHz for f_{RF} = 6 GHz and f_{RF} = 6.9 GHz, (e) variations of conversion gain and NF (6 GHz RF input), (f) variations of 1^{st} and 2^{nd} HRRs (HR1 and HR2) (6 GHz RF input) and (g) variations of in-band IIP3 due to temperature and process corners (NMOS/PMOS; FF=fast/fast, SS=slow/slow, TT=typical/typical, SF=slow/fast and FS=fast/slow)

tones is swept from −40 to −10 dBm and the fundamental and third-intermodulation power are plotted. Both the third-intermodulation tones at $2f_1 - f_2$ and $2f_2 - f_1$ are in-band and are not filtered at the baseband in order to extract an accurate IIP3.

The implementation in two diffident technologies shows that the architecture scales well to older technologies nodes due to its relaxed LO frequency requirements. Nonetheless it can also yield improved performance at smaller geometry nodes.

2.6.4 Linearity

The N-path switching filter improves the OOB linearity of the HR receivers due to the low OOB gain before the baseband harmonic recombination circuit. For the in-band linearity, the base-

band harmonic recombination is the bottleneck because of the LNA gain. Since the baseband structure rejects the unwanted LO harmonics, the OOB linearity is not limited by the baseband circuit, so that the linearity of the LNA becomes the bottleneck. Note that the low OOB impedance of the N-path switching filter helps improve the output linearity of the LNA.

Fig. 2.12(a) shows the OOB linearity performance of the 8-Path HR receiver architecture vs. input power. The OOB IIP3 is post-layout simulated with a two tones test with frequency at $[f_{RF} + \Delta f, f_{RF} + 2\Delta f - 1\ MHz]$ located out of the desired band so that the third order intermodulation (IM3) is in band. This allows the evaluation of the impact of OOB blockers on the desired signals. Δf indicates the blocker frequency offset from the RF input frequency. At a 6 GHz RF input signal with Δf = 200 MHz, OOB IIP3 is 21.3 dBm. The OOB IIP3 as a function of offset frequency at f_{RF} = 6 GHz is shown in Fig. 2.12(b). OOB IIP3 for 120 MHz and 400 MHz offset blockers are of 11.8 dBm and 23 dBm, respectively. Moreover, to evaluate the linearity behavior of the 8-Path HR receiver across the operating RF frequency, the post-layout simulated in-band and OOB IIP3 vs. RF input frequency is plotted in Fig. 2.12(c). While the in-band IIP3 is around $-18\ dBm$, OOB IIP3 at Δf = 200 MHz is better than $+18\ dBm$. The distortion originating from a non-zero voltage swing at the output of the LNA limits the OOB linearity while distortion in the baseband harmonic recombination degrades the in-band IIP3.

Moreover, a two tone test at $[f_{RF} + \Delta f, f_{RF} + \Delta f + 1\ MHz]$ was applied to the LNA to measure the IIP2 (see Fig. 2.12(b)). At a 6 GHz RF, the in-band IIP2 with two tones at 6.05 GHz and 6.051 GHz (i.e., 50 MHz blocker offset frequency) and the OOB IIP2 with two tones at 6.2 GHz and 6.21 GHz (i.e., 200 MHz blocker offset frequency) are $+38.3\ dBm$ and $+68.9\ dBm$, respectively.

2.6.5 Blocker Tolerability

To analyze the resilience of the receiver in the presence of a blocker, a desired signal was overlapped with a blocker at a 200 MHz offset. Then, the blocker power was swept from −40 dBm to 0 dBm. Fig. 2.12(d) shows the post-layout simulated NF vs. blocker power for a 6 GHz and a 6.9 GHz RF, while the blocker is located 200 MHz away. At low blocker powers, the NF of

the receiver dominates the in-band noise. In the presence of the blocker with sufficiently large power, reciprocal mixing of the blocker with OOB noise or with LO phase noise dominates the in-band interference at baseband. The NF in the presence of a −15 dBm blocker increases to only 4.7 dB at a 6 GHz RF frequency. The NF for a 0 dBm blocker degrades to 14.3 dB and 10.4 dB for f_{RF} = 6 GHz and f_{RF} = 6.9 GHz, respectively. Note that the sharp deterioration in NF for a 0 dBm blocker is because of the compression of the receiver gain in addition to the dominant effect of the reciprocal mixing of the blocker with OOB noise and phase noise of the LO.

To address the reciprocal mixing performance of the receiver, phase noise vs. offset frequency (see Fig. 2.9(d)) and NF vs. blocker input power (see Fig. 2.12(d)) are plotted. The low phase noise of the divider minimizes the detrimental effect of reciprocal mixing. However, the NF in the presence of a large blocker power increases due to the reciprocal mixing which is proportional to the LO phase noise. The design of a low phase noise LO clock generator can reduce reciprocal mixing, and could be addressed in future work as discussed in Wu *et al.* (2015).

Table 2.2 Post-layout simulation performance summary and comparison to recently published RF receivers, illustrating the potential of the proposed architecture to achieve high frequency operation and low power consumption, including in larger geometry nodes

Parameters	Lin *et al.* (2014) JSSC' 14	Park & Razavi (2014) JSSC' 14	Murphy *et al.* (2015) JSSC' 15	Xu *et al.* (2017) JSSC' 17	Lien, *et al.* (2018b) JSSC' 19	Wu *et al.* (2019) JSSC' 19	This work♮	This work♮
Topology Description	Current-reuse RF Front-End +Passive Mixer	HRM Miller BPF	FTNC- RX-HBT	HR-NPF	Mixer-first RX + N-Path Filters	Harmonic Selective + Noise Canc.	Third Harmonic Selection	Third Harmonic Selection
No. Phases Paths	8	8	8	8	4	32	8	8
Tech. (nm)	65	65	28	65	28	28	130	65
RF Input	Single-ended	Single-ended	Differential	Differential	Differential	Single-ended	Differential	Differential
RF Bands (GHz)	0.15 - 0.85	0.5 - 2.5	0.1 - 3.3	0.2 - 1	0.1 - 2	0.5 - 3	5.7 - 7.2	5.7 - 7.2
IF BW (MHz)	9	0.5 - 20	0.2 - 3	2	6.5	49	60	100
Gain (dB)	51 ± 1	38	NR	36 - 32	16	42	35	36.4
S11 (dB)	<-12.5	<-10	NR	<-10	-25 @ 1GHz	<-10	<-10	<-10
NF (dB)	4.6 ± 0.9	2.9	1.7	5.4 - 6	4.1 - 10.3	2.4 - 5	5.6	4.4
OOB IIP3 (dBm)	+17.4 at 150 MHz	+10 at 100 MHz	+11.5	+9 at 20 MHz	+44 ($\Delta f/BW$=12.3)	+4 at 50 MHz	+24.5 at 200 MHz	+21.3 at 200 MHz
In-band IIP3 (dBm)	-12	-	-	-	-	-	-16.3	-18.9
Active area (mm^2)	0.55	0.82	5.2	0.29	0.8	1.2	0.52	0.25
Power Consumption (mW)	10.6 - 16.2	20 @ 2GHz	36.8-62.4	26-32‡	34 - 96◇	21⋆	20.3-22.2+	15.5-16.3⋆⋆

♮ Post-layout simulation results. ‡ 26 −32 mA from 1.2/2.5 V supply voltage, 24 mA for analog circuit and 2 −8 mA for clock. ◇ 33 mW/GHz for LO and 30 mW for baseband amplifier. ⋆ 21 mW for analog circuit and 7 −10 mW for LO. + 9.6 mW LNA and G_m cells, 10.7 −12.6 mW LO. ⋆⋆ 13 mW LNA and G_m cells, 2.5 −3.3 mW LO.

2.6.6 8-path HR receiver robustness to process variations

The robustness of the 8-Path HR receiver architecture to process variations is evaluated. Fig. 2.12(e), (f) and (g) depict the sensitivity of the conversion gain, NF, the 1^{st} and 2^{nd} HRRs and linearity in response to temperature variations and process corners. As seen in Fig. 2.12(e), when varying the temperature from $-40\,C^o$ to $80\,C^o$, the conversion gain and DSB NF are higher than 31 dB and less than 6.5 dB for a $f_{LO} = 2$ GHz, respectively. The 1^{st} and 2^{nd} HRRs are higher than 46 dB over the wide temperature variations, as shown in Fig. 2.12(f). As shown in in Fig. 2.12(g), the in-band IIP3 is $-21.1dBm$ at $-40\,C^o$ in the worst case, which is degraded by 2.2 dB compared to the results at $27\,C^o$. Accordingly, it is expected that the architecture presented is well-suited to operation in different temperature conditions and is likely to be robust to process variations.

2.7 Discussion

Table 2.2 illustrates that most reported HR receivers in the state-of-the-art exploit an 8-phase passive switching circuit to achieve the acceptable HRR and operate at an RF input frequency of less than 3 GHz. The proposed third harmonic selection architecture is key in supporting higher frequency RF inputs beyond 3 GHz while consuming low LO power compared to the conventional and other HR architectures. When considering the operating frequency, the bandwidth and LO power, the proposed architecture is desirable to mitigate the power consumption increases typical of operation at higher RF bands, while offering the benefits of a fully differential structure and harmonic rejection. It is also well-suited to relatively large geometry low-cost CMOS technologies.

To attain the desired specifications of the proposed front-end, several factors should be considered. First, there may be a phase mismatch in the LO clocks due to the clock signal paths or mismatch in the clock generator. This can slightly degrade the HRR and NF performance because any overlap between the LO phases will cause charge sharing between the baseband capacitors, resulting in self-corruption of the signal. To resolve this, the LO generator should be placed as close as possible to the switches and dummy paths metals need to be used to en-

sure a more symmetry LO layout. Thus, the N-phase LO signal can appropriately drive the corresponding switches at a given time. Second, there may be coefficient mismatches in the harmonic recombination stage. This can degrade the gain, HRR and NF performance of the receiver. However, duplicating the G_m units as is done where rather than changing the width and number of fingers of the transistors implementing the stages mitigates this issue.

2.8 Conclusion

In this paper, a conventional N-path high-Q switching filter was analyzed and demonstrated how the combination of the N-path filter and baseband harmonic recombination helps to reduce clocking power consumption by selecting higher harmonics of the LO frequency. At higher RF frequency bands, the third harmonic selective configuration mitigates the disadvantages stemming from the need for a high clocking frequency in N-path switching systems. This allows for lower power consumption of the multi-phase clock generation circuitry. In addition, using a differential structure mitigates the issues related to the even-order LO harmonics.

HR receiver architectures leveraging the third harmonic of the LO with $N = 4, 8, 16$ were presented using two feed-forward switching filters with a multi-phase non-overlapping LO clock generator and a baseband harmonic recombination scheme to reject the 1^{st}, 2^{nd}, 4^{th} and 5^{th} harmonics. The required primary clock frequency and dynamic power consumption of the N-phase LO generator is significantly reduced compared to the conventional receivers, thanks to the third harmonic selection structure.

Moreover, the proposed architecture using an 8-path filter yielded a good trade-off between performance and power consumption and area, and it was presented in both TSMC 130 nm and 65 nm CMOS technologies, showing that it is well-suited to older technology nodes and can scale well with smaller geometries. This work has presented post-simulation results. As such, in future work to further validate the concepts presented, the HR receiver using an 8-path switching filter will be fabricated in TSMC 65 nm CMOS technology. Ultimately, this architecture is potentially applicable for battery-powered wireless devices supporting multiple

communication bands as it has the potential of achieving high frequencies of operation and low power consumption.

CHAPTER 3

BLOCKER-TOLERANT INDUCTOR-LESS HARMONIC SELECTION WIDEBAND RECEIVER FRONT-END FOR 5G APPLICATIONS

The harmonic selection RF receiver architecture presented in Chapter 2 can operate at the frequency band of $5.9-7.2$ GHz for unlicensed Wi-Fi usage. In this chapter, a harmonic selection RF receiver is proposed to support the low band frequencies in addition to the higher frequency bands. The ever-increasing demand for wireless data traffic and the number of bands with the introduction of sub-6 GHz 5G calls for wideband blocker-tolerant RF receiver front-ends.

Thus, the main contribution of this chapter is the design, fabrication, and measurement of the RF receiver front-end that is able to select the 1^{st} and 3^{rd}-order harmonics of the switching frequency of the N-path filter. The main advantages of this receiver architecture are to efficiently suppress blockers at LO harmonics together with suppressing near-band blockers, reduce input frequency and dynamic power consumption of multi-phase clock generation by a factor of three, support higher frequencies with RF bandwidth of up to 6.5 GHz ($0.5-6$ GHz), and consume substantially less power, compared to the existing architectures operating at such high frequencies.

Blocker-Tolerant Inductor-Less Harmonic Selection Wideband Receiver Front-End for 5G Applications

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Abstract: A blocker-tolerant harmonic selection receiver front-end with RF bandwidth of 6.5 GHz to support the 5*G* sub-6 GHz band is presented. The proposed N-path switching filter-based receiver employs harmonic recombination blocks at the baseband to select the desired local oscillator (LO) harmonics and suppress blockers. It is demonstrated how the configuration of two feed-forward N-path switching filters and baseband harmonic recombination stage can be reconfigured to select the first harmonic of the switching frequency at the low frequency band (0.5 −1.9 GHz) and the third LO harmonic at the high frequency band (1.95 −6 GHz). Thus, the proposed architecture has the capability of supporting an RF input frequency of up to 6 GHz while the switching frequency operates up to 2 GHz. Higher harmonic selection in addition to the fundamental helps to reduce the power consumption and required input frequency of the multi-phase LO clock generator. An RF receiver prototype is fabricated in a TSMC 130 nm CMOS technology. It achieves a 5 dB noise figure (NF), −16.6 dBm in-band input-referred third order intercept point (IIP3), and 9 dBm out-of-band (OOB) IIP3, respectively, at the low frequency band (0.5 −1.9 GHz). The 2^{nd}-5^{th} harmonic rejection ratios (HRR) are higher than 44 dB without any calibration. The receiver can tolerate a 0 dBm blocker at a 180 MHz offset from a 1 GHz switching frequency with an NF of 9.4 dB. Over the high frequency band (1.95 −6 GHz), the receiver's NF is less than 7.1 dB. Moreover, in-band IIP3, OOB IIP3 and first HRR are higher than −21 dBm, 7 dBm, and 39 dB, respectively. The receiver achieves an S11 better than −10 dB over 0.5 −6 GHz, and has a total power consumption of 17 −22.5 mW from a 1.2-V supply.

Keywords: Wideband receiver, N-path switching filter, harmonic recombination, blocker suppression, non-overlapping clocks, harmonic rejection, sub-6 GHz band

3.1 Introduction

Fifth generation (5G) wireless systems aim at solving spectrum congestion by providing larger channel bandwidth. A 5G system can support large bandwidth, wide connectivity and low latency. 5G is specified for both the sub-6 GHz and millimetre wave (mm-Wave) bands. The sub-6 GHz frequency band allows for longer range, simpler and more power efficient 5G systems, as opposed to the mm-Wave band. At present, the maximum carrier bandwidth of 5G is 100 MHz in the sub-6 GHz frequency band, and 400 MHz in the mm-Wave band, which is much larger than the carrier bandwidth of LTE (i.e., 20 MHz Shen & Zhao (2022); Xie, Oliaei, Rakers, Fernandez, Xiang, Parkes, Riches, Verellen, Rahman, Bhan et al. (2012)), and many core bands can support a typical 100 MHz carrier bandwidth (Equipment (2018); Su, Shen, Liu & Guo (2022)). This lays a strong foundation for 5G systems to support ultrahigh throughput and large bandwidth. The advantage of this large carrier bandwidth is that high transmission rates can be supported.

Since 5G applications require the processing of large amounts of data and need larger bandwidth for effective signal processing, more power is typically consumed by the RF blocks (Gupta & Jha (2015)). Therefore, a crucial challenge is to develop RF circuits providing the required performance with the lowest power consumption and widest carrier bandwidth. Accordingly, this work aims to build an RF front-end design that leverages novel structures to meet the sub-6 GHz band 5G specifications within a wide band and with stringent power consumption metrics, while using relatively low-cost 130 nm CMOS technology.

The key specification of wideband RF front-ends is to provide high OOB and harmonic blockers tolerance without employing off-chip surface acoustic wave (SAW) filters (Javadi *et al.* (2021); Zhang, Chen, Gao, Ma, Hao, Zhu & Chi (2017)). Thus, the primary challenge in such a wideband receiver design is to suppress strong blocker signals while preserving the desired signal. To suppress the blockers, an on-chip high-order Q-enhanced LC filter proposed in (Amin, Raman & Koh (2019)) can be used. However, at sub-GHz frequencies, the large chip area is a limiting factor. Alternatively, integrated G_m-C band-pass filters (BPF) can be used as in (Le-Thai,

Nguyen, Nguyen, Cho, Lee & Lee (2010); Xu, Venkatachala, Hu, Leuenberger, Temes & Moon (2019)), but suffer from inherent non-linearity. Moreover, a big challenge in the LC and G_m-C BPFs is to implement tuning schemes, while preserving the pass-band shape and tracking the carrier frequency. Other options that do not rely on BPFs such as active blocker rejection techniques for receiver front-ends proposed in (Calderin, Ramakrishnan, Puglielli, Alon, Nikolić & Niknejad (2017); Rasekh & Bakhtiar (2019)) can be used, but suffer from high power dissipation (40 mW and 80 mW, respectively).

Alternatively, N-path switching band-pass filters are widely used for RF filtering (Ghaffari *et al.* (2011)). The N-path filters translate the baseband (BB) low-pass response by employing passive switches that are driven by an N-phase local oscillator (LO), and achieve a high-Q band-pass response with a center frequency set by the LO switching frequency (f_{LO}). However, harmonic selectivity is one of the imperfections of N-path switching filters. This causes blockers located at the LO harmonic frequencies to affect the wideband RF receiver resulting in receiver desensitization or gain compression. To mitigate large blockers, several harmonic rejection mixing (HRM) techniques used in RF receivers have leveraged the concept of N-path filtering. This includes a BPF structure (Poursaadati Zinjanab, Elmi & Jalali (2018)), notch filter structure (Shams & Nabki (2021b)), mixer-first topology (Purushothaman, Klumperink, Plompen & Nauta (2021); Sharma & Nallam (2020)), and noise cancellation scheme (Javadi *et al.* (2021); Wu *et al.* (2015)).

Harmonic rejection schemes relax the required RF and IF filter by suppressing blockers located around the LO harmonics, and thus, improve the OOB IIP3. Since the LO signal does not contain certain harmonics, the harmonic rejection is achieved by synthesizing the LO signal and then summing multiple LO paths with weighted amplitudes. Typically, the amplitude scaling is realized by weighting transconductors (G_m-cells) in the RF, N-path switching or IF paths (Forbes *et al.* (2013); Lin *et al.* (2014); Murphy *et al.* (2015); N. Shams & Nabki (2020); Wu, Ng, Zheng, Leung, Chao, Li & Luong (2017); Xu *et al.* (2017)). The $0.6-3$ GHz noise-canceling receiver in (Wu *et al.* (2019)) employs 32-phase non-overlapping clocks, harmonic-selective transimpedance amplifiers (TIAs) and harmonic recombination blocks to achieve a HRR of

45 dB while consuming 30 mW. At higher frequencies, 32-phase non-overlapping LO clocks draw considerable power consumption. Thus, another drawback of N-path switching filters is the inaccessibility of accurate low-power N-phase LO signal generators at high frequencies. An LO clock generator with an input frequency of $N \times f_{LO}$ generates the sampling signals with a 1/N duty-cycle. Therefore, the dynamic switching power of the LO clock signal is calculated as

$$P_{\mathrm{LO}} = \eta C_{eff} f_{LO} V_{dd}^2, \tag{3.1}$$

where η, C_{eff}, f_{LO}, and V_{dd} are the activity factor, the internal and load capacitances, the switching frequency, and the supply voltage, respectively.

As the number of paths, N, in the N-path switching filter and/or the operating frequency increases, the power consumption of the LO clock generation increases in a linear fashion. The proposed $0.4-3.3$ GHz single-ended receiver architecture in (Elmi *et al.* (2018)) employs a 16-path HRM technique by using resistive coefficients and combines the baseband (BB) signals with 65, 55, 37 and 13 G_m unit cells to adjust the center frequency at the desired LO harmonic and to reduce power consumption. However, this results in relatively high complexity due to the number of parallel BB recombiners, the large number of switches, and the required 16-phase clock generator. The proposed wideband RF receivers in (van Liempd *et al.* (2014)) and (Razavi & Razavi (2022)) operate up to 6 GHz. The receiver architecture in van Liempd *et al.* (2014) is split into a low-band RF path ($0.4-3$ GHz) and a high-band RF path ($3-6$ GHz) using 8- and 4-phase passive mixers, respectively. Since driving the switches of the 8-phase mixer beyond 3 GHz increases the power consumption significantly, even in 28 nm CMOS technology, conventional 4-phase passive mixers are used for high-band RF, and consume 35 mW. The receiver in (Razavi & Razavi (2022)) employs a multi-loop 8-path structure to ease the trade-off between linearity and noise, and a "divide-and-conquer" principle for harmonic rejection to afford robustness against gain and phase mismatches at the cost of a $23-49$ mW power consumption.

There is thus a need for a structure that can leverage the benefits of N-path filters, while mitigating their harmonic rejection limits and allowing for low-power LO clock generation. Accordingly, this paper presents a blocker tolerant harmonic selection differential wideband RF receiver that addresses all of the aforementioned challenges simultaneously. To cover the RF frequency range of 0.5 −6 GHz, the input RF frequency is split into a low band (LB) frequency range, from 0.5 −1.9 GHz, and a high band (HB) frequency range, from 1.95 −6 GHz. This results in a relaxed trade-off between OOB filtering at lower frequencies and low-power LO clock generation at higher frequencies. The proposed wideband RF receiver architecture is composed of a differential LNA, a two feed-forward N-path switching filter configuration, 1^{st} and 3^{rd} harmonic recombination blocks at baseband, and variable gain BB amplifiers. In the proposed N-path harmonic selection receiver architecture, two feed-forward N-path switching systems and BB harmonic recombination blocks are configured to select the 1^{st} harmonic of the switching frequency at the LB frequency, and the 3^{rd} LO harmonic at the HB frequency. Moreover, by selecting the higher harmonic of the LO clock frequency in addition to the fundamental one, the proposed architecture is able to cover higher frequencies of up to 6 GHz, and to reduce the input frequency requirement and dynamic power consumption of the LO generation block by a factor of three according to (3.1).

It should be mentioned that to provide a wideband RF front-end for 5G applications in the sub-6 GHz band and to support an RF operating range of up to 6 GHz, the conventional 8-path filter-based receiver structure that is often utilized to provide harmonic rejection should operate from 0.5 GHz to 6 GHz. Consequently, the required clock generator driving the 8-path structure requires an input LO operating at up to 24 GHz, which is not readily achievable and not compatible with low-cost CMOS processes and low-power operation. Indeed, creating an accurate low power multi-phase LO signal at such high frequencies requires significant dynamic power consumption and high-speed transistors. Accordingly, this work aims to alleviate this issue by relaxing the N-path filter's frequency requirement while supporting RF input signals from 0.5 GHz to 6 GHz. The required input clock frequency of the proposed wideband 8-path filter based receiver architecture ranges from 2 GHz to 8 GHz, as opposed to the conventional

RF receivers operating at up to 24 GHz. Thus, the proposed receiver can support RF inputs beyond 3 GHz without dissipating high power or sacrificing the NF and the harmonic rejection performance. It can also reduce the implementation cost as the resulting lower clock frequency is suited to larger geometry technology nodes.

This paper is organized as follows. Section 3.2 describes the proposed blocker tolerant 1^{st} and 3^{rd} harmonic selection receiver architecture. The transistor-level circuit implementation is detailed in Section 3.3. Section 3.4 presents the measurement results and discusses the performance metrics of the proposed architecture in comparison to the conventional architecture. This is followed by a discussion and conclusion.

3.2 Proposed Harmonic Selection Receiver Architecture

The differential architecture of a blocker tolerant first and third harmonic selection receiver is illustrated in Fig. 3.1. The proposed receiver consists of a wideband differential inductorless LNA, two feed-forward N-path switching filters, BB first and third harmonic recombination blocks, variable gain BB amplifiers, and a multi-phase LO clock generator. All switches in the N-path switching system are driven by N-phase non-overlapping LO clocks.

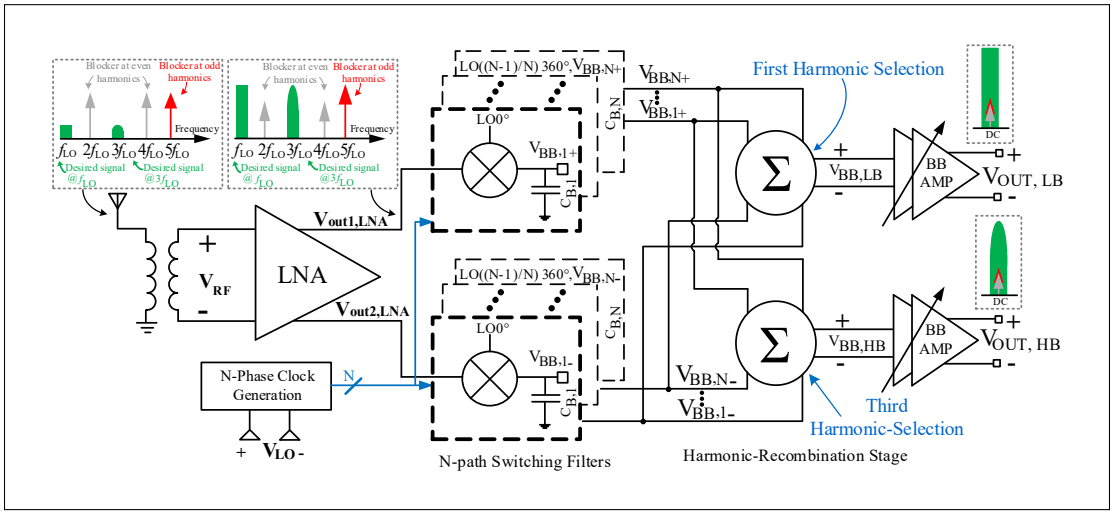

Figure 3.1 Diagram of the proposed harmonic recombination RF receiver

The 0.5 −6 GHz RF input signals are amplified by the wideband LNA, as shown in Fig. 3.1. The even-order harmonics of the switching frequency (f_{LO}) are attenuated due to the fully differential structure, and as such it removes the need for a notch filter in parallel with the LNA, yielding advantages in power consumption and area. The amplified RF signal at the LNA outputs ($V_{out1,LNA}$ and $V_{out1,LNA}$) is down-converted to the baseband signal by employing two feed-forward N-path filters. The N-path switching systems are loaded with a BB capacitor ($C_{BB,1}$, $C_{BB,2}$, …, $C_{BB,N}$), providing high in-band impedance for low NF and voltage gain. At the differential output of the LNA, the N-path switching filter up-converts this BB capacitor impedance to the RF to provide the in-band voltage gain and the out-of-band filtering.

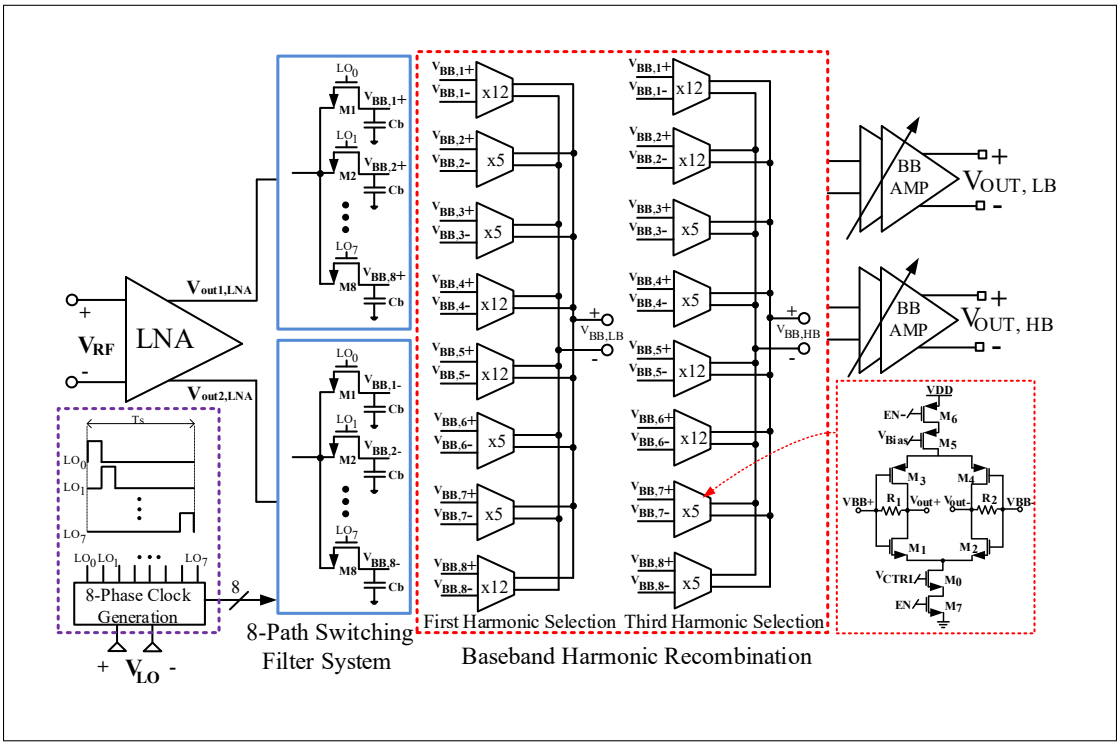

Figure 3.2 Architecture of the 1^{st} and 3^{rd} harmonic selection receiver front-end

As the frequency of operation increases, the power consumption of the LO clock generator increases. Thus, in the proposed sub-6 GHz receiver, the RF input frequency is split into the LB frequency (0.5 −1.9 GHz) and the HB frequency (1.95 −6 GHz). When the input RF signal operates in the range of 0.5 −1.9 GHz, the amplified RF signal from the LNA is down-converted by

employing two N-path switching filters. Then, the proposed architecture selects the fundamental harmonic of the f_{LO} by using the BB first harmonic recombination circuit, and suppresses the other harmonics. Fig. 3.1 shows how a harmonic blocker located at $3f_{LO}$ is rejected through the BB first harmonic recombination block. However, in the HB frequency range, the BB harmonic selection block is configured to select the third LO harmonic while rejecting the other harmonics, especially the first one (see Fig. 3.1). Note that the BB first and third harmonic recombination blocks include enable and disable pins. At the HB frequency, the recombination circuit selecting the first LO harmonic is disabled. This helps reduce the DC power consumption along with the dynamic power consumption. Thanks to the harmonic selection system, the trade-off between improved OOB filtering at lower frequency and low-power N-path filter operation at higher frequency is mitigated, as the receiver at the LB and the HB frequencies operates at the first and third LO harmonic, respectively.

Note that the conversion gain reduces when an LO harmonic larger than 1 is selected. For example, in a 16-phase switching filter, the conversion gain at $5f_{LO}$ is smaller than the gain at f_{LO}. This small attenuation can be compensated by using the BB amplifiers (see Fig. 3.1).

3.3 Circuit Design

The harmonic selection RF receiver is composed of the differential inductorless LNA, two feed-forward 8-path switching filters, BB 1^{st} and 3^{rd} harmonic recombination blocks and BB amplifiers. Fig. 3.2 illustrates the circuit of the harmonic selection RF receiver and its main building blocks. Due to the split RF input frequency and 1^{st} and 3^{rd} LO harmonic selection at the LB and HB frequency ranges, respectively, the LO frequency requirement ranges from 0.5 GHz to 2 GHz to support the aforementioned operating RF band. In the N-path switching filter, the multi-phase LO clock has non-zero components at the harmonics of f_{LO}. The harmonics selectivity is achieved when the LO signal contains the desired frequency components. The N-path switching system divides an ideal LO sine signal of $A_c sin(\rho\omega_{LO}t + \varphi_0)$ into N equal time intervals, where the pulse widths are $1/Nf_{LO}$ and A_c and φ_0 are a constant amplitude and an initial phase, respectively. Then, the amplifiers in the BB harmonic recombination stage are

combined to equivalently generate a sine LO signal. The voltage gain of each corresponding amplifier, $A_{G_m}(i)$, is defined as (Shams & Nabki (2022)):

$$A_{Gm}(i) = A_c sin(\rho i \frac{2\pi}{N} + \varphi_0), i = (0, 2, ..., N-1), \tag{3.2}$$

where $0 \leqslant \rho < N, \rho \in \mathbb{Z}$. The particular cases of $\rho = 1$ and $\rho = 3$ are used here in order to favor the down-conversion of the 1^{st} and 3^{rd} harmonic of the LO frequency in the BB recombination process, respectively. Therefore, two harmonic recombination blocks at the baseband are employed to recombine the down-converted voltages across the BB capacitors ($[V_{BB,1}, V_{BB,2}, \ldots, V_{BB,N}]$) (see Fig. 3.2). Note that the weighting ratio of each G_m stage in both the 1^{st} and 3^{rd} harmonic recombination blocks is achieved by (3.2).

Moreover, the harmonic selectivity of the BB 1^{st} and 3^{rd} harmonic recombination blocks is illustrated as phasor diagrams in Fig. 3.3. The BB 1^{st} and 3^{rd} harmonic recombination circuits constructively add the 1^{st} and 3^{rd} harmonic signal vectors, while cancelling the odd-order harmonics (see Fig. 3.3(a) and (b)). Note that $[GM_1, GM_2, ..., GM_8]$ are the weighed G_m stages in the BB harmonic recombination blocks such that their coefficients are equal to $[12G_m, 5G_m, ..., 12G_m]$ and $[12G_m, -12G_m, ..., -5G_m]$ for the LB and HB frequency ranges, respectively.

N-path switching filters are highly linear due to their passive nature and can provide a high Q characteristic. However, one important drawback of N-path switching filters is the harmonic fold back (HFB) in the frequency response because of the sampling that occurs. Indeed, HFB implies that the filter translates interferers and noise around frequencies of $(Nk \pm 1)f_{LO}, k = 1, 2, 3,$ into its passband, where N and f_{LO} are the number of paths and the switching frequency, respectively. It can be shown that the first and strongest HFB occurs at the $(N \pm 1)f_{LO}$. For example, the HFB in the 8-path switching filter appears at $7f_{LO}$. The harmonic fold back rejection ratio (HFBRR) is the ratio of the gain at the desired RF signal to the gain at the signal folded from the LO harmonics and can be calculated by

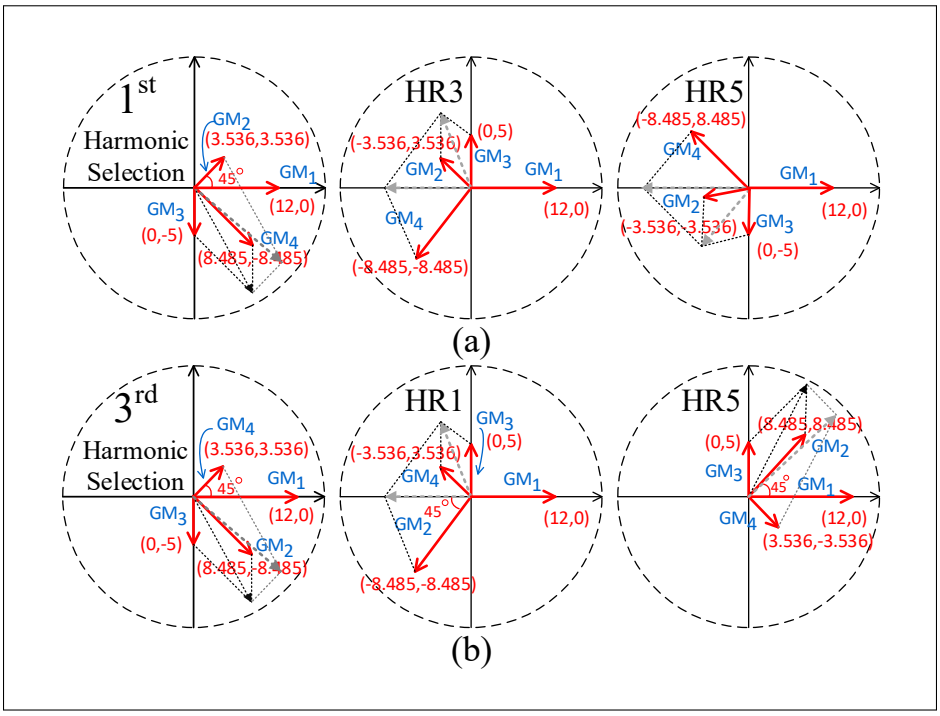

Figure 3.3 Phasor diagrams of (a) the 1^{st} harmonic selection, along with the 3^{rd} and 5^{th} harmonic rejection, and (b) the 3rd harmonic selection, along with the 1^{st} harmonic rejection for the 8-path HR receiver

$$HFBRR_i = \frac{sinc(\frac{\pi}{N})}{sinc(i\frac{\pi}{N})}, (i = kN - 1, k \in), \tag{3.3}$$

Fig. 3.4 shows the HFB attenuation for a conventional N-path filter. Thus, increasing number of paths, N, helps to reduce the HFB effect by pushing the strongest HFB to higher frequencies. However, it requires a higher input frequency to the LO generator, more dynamic power consumption, higher speed circuits and potentially the use of higher cost CMOS nodes.

In the third harmonic selection technique proposed, the strongest HFB of the N-path switching filter occurs at $(kN \pm \rho)f_{LO}$, where ρ is the ρ^{th} order LO harmonic selected. For example, the HFB in the 8-path filter appears at $5f_{LO}$ when the third harmonic of the switching filter is selected (i.e, $\rho = 3$). Thus, the HFB attenuation in the third harmonic selection path is less than that of the first harmonic selection path. To provide the high fifth LO harmonic suppression at

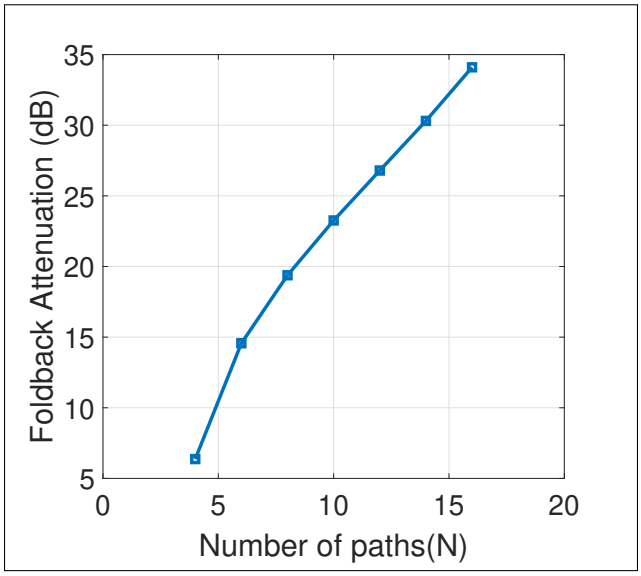

Figure 3.4 Fold-back attenuation versus the number of paths

the HB path, an off-chip adjustable notch filter was employed to avoid amplification at the HFB frequencies.

Compared to the structure proposed in N. Shams & Nabki (2020), the distinguishing features are the use of the inductorless LNA to reduce chip area, the use of the first harmonic selection as well as the third harmonic selection at the baseband, and importantly, supporting a wide range of RF inputs (i.e., 0.5 GHz to 6 GHz).

3.3.1 Differential Wideband LNA

The LNA architecture is depicted in Fig. 3.5(a). The core of the LNA architecture is similar with the structure proposed in Shams *et al.* (2020), and consists of the combination of common gate (CG), shunt-feedback (SFB), current reuse, and capacitive cross coupling (CCC) topologies. The LNA in Shams *et al.* (2020) employs two center-tapped inductors to resonate with parasitic capacitances and provide the bias current paths for the LNA. However, to avoid the biasing based on inductors and to save silicon area, the current sources implemented with M_{nb1} and M_{pb1} (M_{nb2} and M_{pb2} in the second branch) are used to provide high resistance for AC signals.

Thus, the total noise factor analyzed in Shams & Nabki (2022) is modified and can be expressed as

$$F \approx 1 + \frac{\gamma}{2(g_{m_{M_A}} + g_{m_{M_B}})R_s} + \frac{2R_s}{R_F} \times \left(1 + \frac{r_{o_{M_A}} || r_{o_{M_B}}}{r_{o_{M_A}} || r_{o_{M_B}} + R_F}\right)^2 + \frac{R_s}{2} \times (\gamma_n g_{m_{nb}} + \gamma_p g_{m_{pb}}), \tag{3.4}$$

where γ, R_s, R_F, $g_{m_{M_A}}$, $g_{m_{M_B}}$, $g_{m_{nb}}$, and $g_{m_{pb}}$ represent the channel length modulation, source resistance, shunt feedback resistors, $g_{m_{M_{1A}}} + g_{m_{M_{2A}}}$, $g_{m_{M_{1B}}} + g_{m_{M_{2B}}}$, $g_{m_{M_{nb1}}} + g_{m_{M_{nb2}}}$, and $g_{m_{M_{pb1}}} + g_{m_{M_{pb2}}}$, respectively. The second term is due to M_{1A} and M_{1B} (M_{2A} and M_{2B} in the second branch), while the third term is the noise contributed by feedback resistance R_F. The last term is due to current sources M_{nb1} and M_{pb1} (M_{nb2} and M_{pb2}), indicating that $g_{m_{nb}}$ and $g_{m_{pb}}$ should be minimized. The inductor-less LNA used in the proposed receiver reduces the power consumption (i.e., 1.1 mW) and area (i.e., 0.036 mm^2), and provides a wide RF bandwidth (i.e., 6.5 GHz), compared to the LNA proposed in Shams *et al.* (2020).

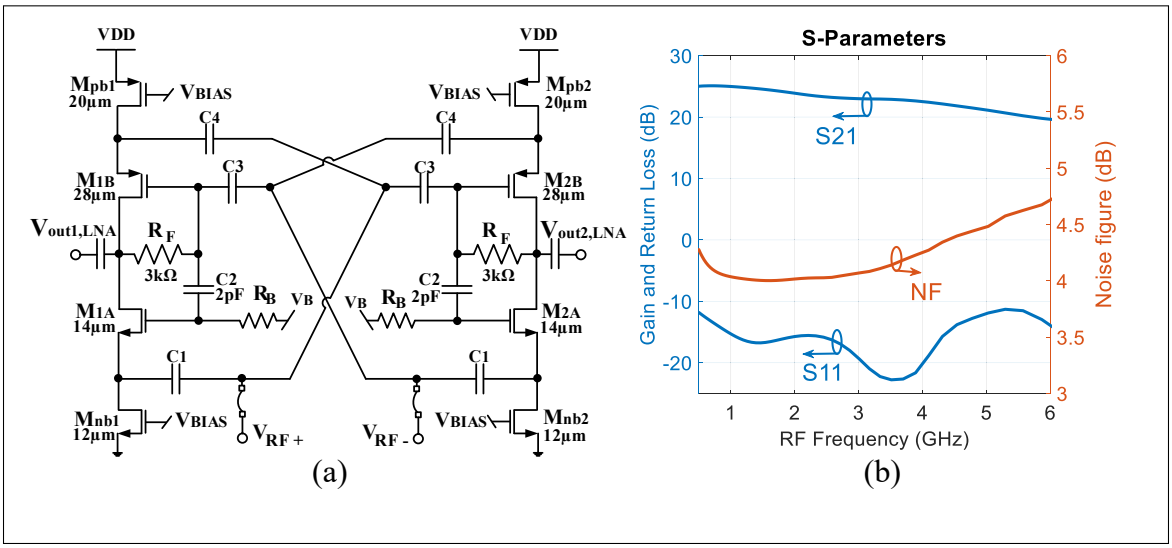

Figure 3.5 (a) Differential wideband LNA, and (b) its post-layout simulated gain (S21), return loss (S11) and NF.

Moreover, the major source of LNA non-linearity originates from M_{1A} and M_{1B} (M_{2A} and M_{2B}). The third-order intermodulation product (IM3) current of M_A and M_B can be modeled by a current source across M_A and M_B. The IM3 current cancellation is the same as the noise cancellation analyzed in Shams & Nabki (2022) due to the same current-source modeling method, and is analysed in more detail in Appendix A.

The post-layout simulated voltage gain, S11 and NF of the wideband differential LNA is plotted in Fig. 3.5(b). The inductorless LNA achieves an S11 below -10 dB and a voltage gain higher than 20 dB from 0.5 GHz to 6 GHz. The NF is below 4.6 dB and increases at high frequency due to the reduced gain.

Note that a high load impedance over the wide frequency range can help to achieve a flatter gain. The shunt-feedback topology used in the LNA is a well-known topology in wideband amplifiers, where an increase of R_F increases gain at the cost of higher NF, while lower NF can be achieved by reducing R_F. Nevertheless, it is difficult to satisfy noise and gain performance simultaneously and in the proposed work, a trade-off was selected. If a lower LNA gain can be accepted, then a design with a gain of less than 20 dB will reduce the gain variation over the low and high frequency bands.

3.3.2 8-Path Switching Filter

The design of the N-path switching filter is critical to the performance of the receiver. The RF receivers presented in Shams & Nabki (2022) employ 4-, 8-, and 16-path switching systems and harmonic recombination blocks at the baseband. The post-layout simulation performance reported in Shams & Nabki (2022) demonstrates that increasing the number of paths, N, more accurately approximates a sinusoidal LO, and thus increases the HRRs and reduces the NF at the cost of more circuit complexity and higher LO power consumption. According to Shams & Nabki (2022), the harmonic selection receiver using an 8-path filter achieves an acceptable trade-off between NF, BW, area, and power consumption, while providing harmonic rejection. Thus, this work employs the switching filter with $N = 8$ as shown in Fig. 3.2.

Two 8-path switching filters are employed to down-covert the amplified RF signals to the BB. The 8 switches and BB capacitors ($C_{BB,1}$, $C_{BB,2}$, …, $C_{BB,8}$) are realized with low threshold voltage transistors with W/L = 4 μm / 130 nm, and 200 fF MIM capacitors. The NMOS switches are driven by 12.5 % duty-cycle non-overlapping clocks and are capacitively coupled to the 8-phase LO clock. In addition, to provide the maximum achievable HRR, the size of switches should be increased to reduce their ON resistance, resulting in larger parasitic capacitance, clock leakage, and higher LO power consumption to drive them. Thus, fixed-size switches are biased at a 600 mV DC voltage to provide a 1.2 V supply swing on the switches' gate-source and thus improve linearity.

3.3.3 First and Third Harmonic Recombination Paths

The BB 1^{st} and 3^{rd} harmonic recombination paths make the effective BB signals of [$V_{BB,1}$, $V_{BB,2}$, …, $V_{BB,8}$] more closely resemble a sine wave. To do this, the 8 differential down-converted signal pairs ($V_{BB,1+}$, $V_{BB,2+}$, …, $V_{BB,N+}$ and $V_{BB,1-}$, $V_{BB,2-}$, …, $V_{BB,N-}$) are weighted and recombined to generate signals of $V_{BB,LB}$ for the LB frequencies and $V_{BB,HB}$ for the HB frequencies (see Fig. 3.2). The $8G_m$ cells in the proposed receiver using the 8-path filter are weighted with ratios of 12 : 5 calculated with (3.2), where $\varphi_0 = 22.5^o$ and $N = 8$. In the ideal case, when the first harmonic is selected ($\rho = 1$), the $8G_m$ cells of $[GM_1, GM_2, ..., GM_8] = [0.9239, 0.3827, -0.3827, ..., 0.9239]$ are recombined. In the third harmonic selection path, where ($\rho = 3$), the $8G_m$ cells of $[GM_1, GM_2, ..., GM_8] = [0.9239, -0.9239, 0.3827, ..., -0.3827]$ are recombined. Note that higher harmonic rejection can be achieved by accurately implementing the desired weighting factor $1 + \sqrt{2}$. The weighting ratio of $0.9239/0.3827 = 2.4142$ more accurately approximates the weighting factor of $1 + \sqrt{2}$, compared to the weighting ratio of $12/5 = 2.4$. To provide suitable transistor matching and to achieve robustness to amplitude mismatches in the layout post-fabrication, the G_m cell coefficients are implemented through duplicating 12 (i.e., $0.9239A_c$) and 5 (i.e., $0.3827A_c$) G_m stages, rather than changing the size and fingers of the transistors.

At LB frequencies, the output of the 8 weighted G_m cells are combined and configured to select the 1^{st}-order LO harmonic. The Fourier analysis of such a waveform can be expressed as

$$V_{BB,LB}(t) = \begin{cases} 12, & 0 < t < \frac{T_{LO}}{8} \\ 5, & \frac{T_{LO}}{8} < t < \frac{T_{LO}}{4} \\ -5, & \frac{T_{LO}}{4} < t < \frac{3T_{LO}}{8} \\ -12, & \frac{3T_{LO}}{8} < t < \frac{T_{LO}}{2} \\ -12, & \frac{T_{LO}}{2} < t < \frac{5T_{LO}}{8} \\ -5, & \frac{5T_{LO}}{8} < t < \frac{3T_{LO}}{4} \\ 5, & \frac{3T_{LO}}{4} < t < \frac{7T_{LO}}{8} \\ 12, & \frac{7T_{LO}}{8} < t < T_{LO} \end{cases} \tag{3.5}$$

$$\begin{aligned} a_n = & \frac{7}{n\pi} sin(\frac{n\pi}{8}) + \frac{10}{n\pi} sin(\frac{n\pi}{4}) + \frac{7}{n\pi} sin(\frac{3n\pi}{8}) \\ & - \frac{7}{n\pi} sin(\frac{5n\pi}{8}) - \frac{10}{n\pi} sin(\frac{3n\pi}{4}) - \frac{7}{n\pi} sin(\frac{7n\pi}{8}), \end{aligned} \tag{3.6}$$

$$\begin{aligned} b_n = & -\frac{7}{n\pi} cos(\frac{n\pi}{8}) + \frac{12}{n\pi} - \frac{10}{n\pi} cos(\frac{n\pi}{4}) - \\ & \frac{7}{n\pi} cos(\frac{3n\pi}{8}) + \frac{7}{n\pi} cos(\frac{5n\pi}{8}) + \frac{10}{n\pi} cos(\frac{3n\pi}{4}) + \\ & \frac{7}{n\pi} cos(\frac{7n\pi}{8}) - \frac{12}{n\pi} cos(n\pi), \end{aligned} \tag{3.7}$$

where n is an integer. Fig. 3.6(a) plots the harmonic content according to the Fourier coefficients and $V_{BB,LB}(t) = a_0 + \sum_{n=1}^{\infty} a_n cos(n\omega_{LO}t) + \sum_{n=1}^{\infty} b_n sin(n\omega_{LO}t)$. Ideally, there is no 3^{rd}-order harmonic content in the effective LO. However, complete suppression of the 3^{rd} harmonic is not achieved due to LO non-idealities and device mismatches.

In the HB frequency range, the output of the 8 weighted G_m cells of $[12, -12, 5, 5, -12, 12, -5, -5]$ are combined to equivalently generate a sine LO signal of $A_c sin(3\omega_{LO}t + \varphi_0)$ at the $V_{BB,HB}$ output, and to select the 3^{rd} harmonic of the switching frequency. The Fourier coefficients of the

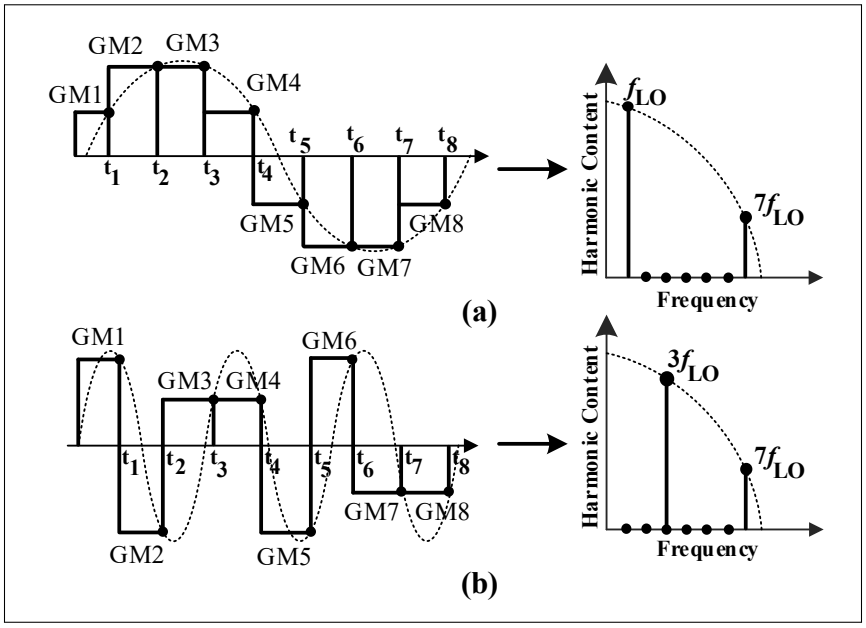

Figure 3.6 Effective LO waveform and harmonic content from the Fourier analysis at (a) the $V_{BB,LB}$ output, and at (b) the $V_{BB,HB}$ output

resulting effective LO are given by

$$V_{BB,HB}(t) = \begin{cases} 12, & 0 < t < \frac{T_{LO}}{8} \\ -12, & \frac{T_{LO}}{8} < t < \frac{T_{LO}}{4} \\ 5, & \frac{T_{LO}}{4} < t < \frac{3T_{LO}}{8} \\ 5, & \frac{3T_{LO}}{8} < t < \frac{T_{LO}}{2} \\ -12, & \frac{T_{LO}}{2} < t < \frac{5T_{LO}}{8} \\ 12, & \frac{5T_{LO}}{8} < t < \frac{3T_{LO}}{4} \\ -5, & \frac{3T_{LO}}{4} < t < \frac{7T_{LO}}{8} \\ -5, & \frac{7T_{LO}}{8} < t < T_{LO} \end{cases} \tag{3.8}$$

$$\begin{aligned} a_n = {} & \frac{24}{n\pi} sin(\frac{n\pi}{8}) - \frac{17}{n\pi} sin(\frac{n\pi}{4}) + \frac{17}{n\pi} sin(\frac{n\pi}{2}) \\ & - \frac{24}{n\pi} sin(\frac{5n\pi}{8}) + \frac{17}{n\pi} sin(\frac{3n\pi}{4}) - \frac{5}{n\pi} sin(n\pi), \end{aligned} \tag{3.9}$$

$$b_n = -\frac{24}{n\pi}cos(\frac{n\pi}{8}) + \frac{12}{n\pi} + \frac{17}{n\pi}cos(\frac{n\pi}{4}) - \frac{17}{n\pi}cos(\frac{n\pi}{2}) + \frac{24}{n\pi}cos(\frac{5n\pi}{8}) - \frac{17}{n\pi}cos(\frac{3n\pi}{4}) + \frac{5}{n\pi}cos(n\pi), \tag{3.10}$$

Fig. 3.6(b) depicts the effective LO waveform at the $V_{BB,HB}$ output and harmonic content from the Fourier analysis. The harmonic content achieved from the Fourier analysis demonstrates that the proposed architecture is able to select at the third LO harmonic.

The robustness of the receiver design is investigated through Monte Carlo analysis. Over 200 runs, both the process variations and device mismatches were considered. Fig. 3.7 depicts the post-layout simulated results of the 3^{rd} and 1^{st} HRRs for the LB and HB frequency ranges, respectively, when the LO frequency is set to 1 GHz. The average 3^{rd} HRR is 48.0 dB when the first LO harmonic is selected. The average 1^{st} HRR is 42.6 dB at the third harmonic of the LO frequency.

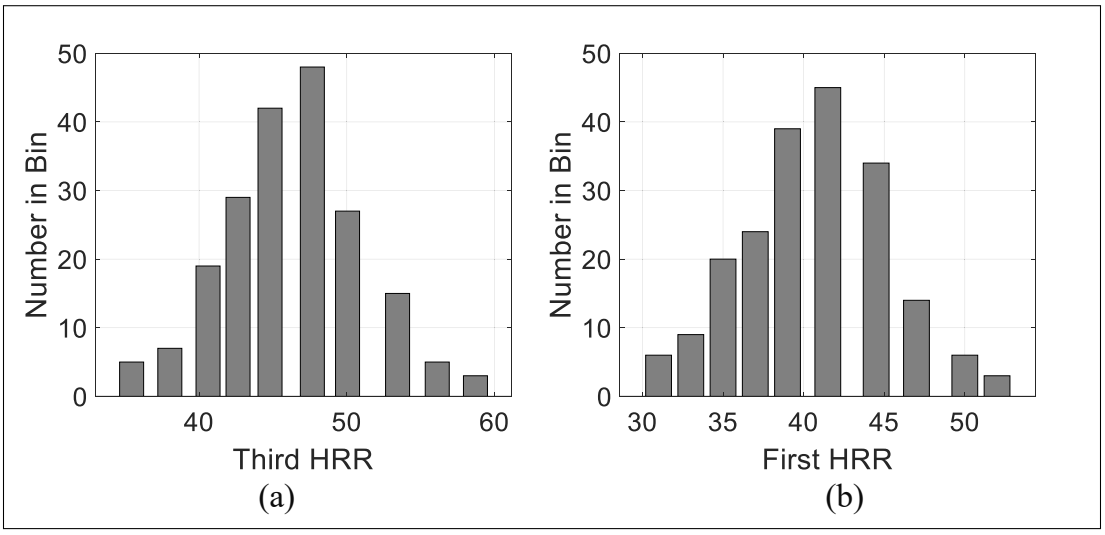

Figure 3.7 Post-layout Monte Carlo simulation histograms of the HRR for a 1 GHz LO with 200 runs: (a) 3^{rd} HRR for the LB frequency range and (b) 1^{st} HRR for the HB frequency range

Fig. 3.2 also depicts the self-biased G_m circuit, where each G_m unit cell contains two resistive common-mode feedback resistors, R_1 and R_2, and control voltages V_{Bias} and V_{CTRL}. These control voltages in the Gm cell are used to provide DC biasing. However, the value of the transconductance may change due to PVT variations, leading to shifts in bandwidth, gain, and harmonic rejection performance. Thus, tuning V_{Bias} and V_{CTRL} can help to overcome PVT variations.

The self-biased G_m circuit used in the harmonic recombination blocks contains two resistive common-mode feedback resistors, R_1 and R_2. One R_1 resistor and one R_2 resistor were shared for the $12G_m$ ($5G_m$) unit cells, instead of using twelve R_1 (five R_1) and twelve R_2 (five R_2) resistors in the $12G_m$ ($5G_m$) unit cells. This resistor sharing approach reduces the required number of R_1 and R_2 resistors to 17 rather than 68 ($(12+5)\times4$) in the 8-path harmonic selection receiver, and helps reduce mismatches in the layout.

3.3.4 Variable Gain BB Amplifier and LO Clock Generator

Fig. 3.8(a) shows the implemented dynamically biased BB amplifier circuit. The biased BB amplifier consists of the differential pair M_1-M_4 that is biased by transistors M_5, M_6, M_9, and M_{10}. M_5 and M_6 are used to increase the differential pair's bias current to allow for a larger input signal. The BB amplifier employs M_{16} and M_{17} as switches to add or remove resistance R1 in order to control the gain by varying the output resistance. The gain can be varied between 12 dB and 15 dB. The differential amplifier's outputs are set at the desired common-mode voltage by using common-mode feedback through M_{11}-M_{14}. Note that the BB amplifiers employed for the LB and HB paths have the same configuration with a bias current of 650 µA.

The proposed receiver architecture relies on an 8-phase LO clock with a duty cycle of 12.5 % to perform the harmonic rejection, blocker rejection and down-conversion. Fig. 3.8(b) shows the 8-phase clock generator used, consisting of four latches in a ring flip-flop-based divider (Shams & Nabki (2021a)). Each latch is realized as depicted in Fig. 3.8(b). Following the divider, 8 AND gates convert the LO signals from a 50 % to a 12.5 % duty cycle, and to provide

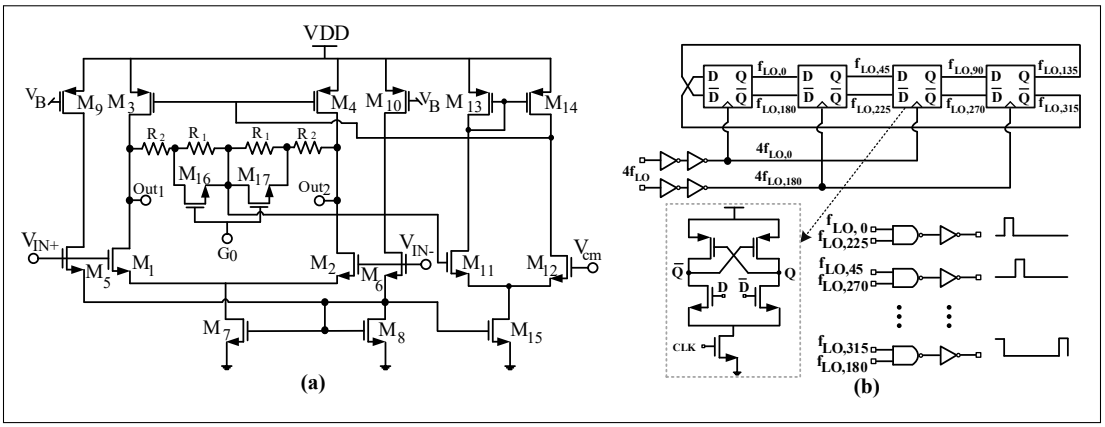

Figure 3.8 (a) Variable gain BB amplifier, and (b) 8-phase non-overlapping LO clock generator

8-phase non-overlapping LO clocks. Note that 4 times of the switching frequency (i.e., $4f_{LO}$) is required for the 8-phase LO input and the $4f_{LO}$ signal is inputted off-chip. Thus, the input frequency of the LO generator varies from $2-8$ GHz to generate the desired switching frequency of $0.5-2$ GHz, while consuming $5.8-11$ mW.

It should be mentioned that the input signals are buffered before applying them to the four latches, as shown in Fig. 3.8(b). This buffer is composed of two cascaded inverters with high threshold voltage NMOS and PMOS transistors. Thus, even if the input signal level applied to the LO clock generator were to be lower than that desired (i.e., between $0.3-1\ V$ rather than $0-1.2\ V$), the high threshold voltage transistors would shift the input signal level to the desired level.

Any overlap between the eight LO phases results in charge sharing between the BB capacitors and in turn leads to the self-corruption of the signal. Thus, this degrade the HRRs and NF performance. To alleviate this issue, since the LO clock consists of a ring flip-flop based divider consisting of four latches to generate eight phases, the layout of the one latch was drawn and it was repeated four times to create the ring flip-flop based divider and to minimize the mismatch. In addition, dummy paths have been added in the layout design such that the eight LO signals are applied to the corresponding eight NMOS switches at almost the same time. Moreover, the

LO generator is placed as close as possible to the switches to reduce the parasitic capacitance and resistance of the associated interconnect routing.

3.4 Measurement Results

The proposed receiver was fabricated in a 130 nm CMOS technology from TSMC and operates from 0.5 GHz to 6 GHz. Fig. 3.9(b) shows the die micrograph, having an active area of 0.48 mm^2 (0.76 mm × 0.64 mm). The total area including bond-pads is 1 mm^2.

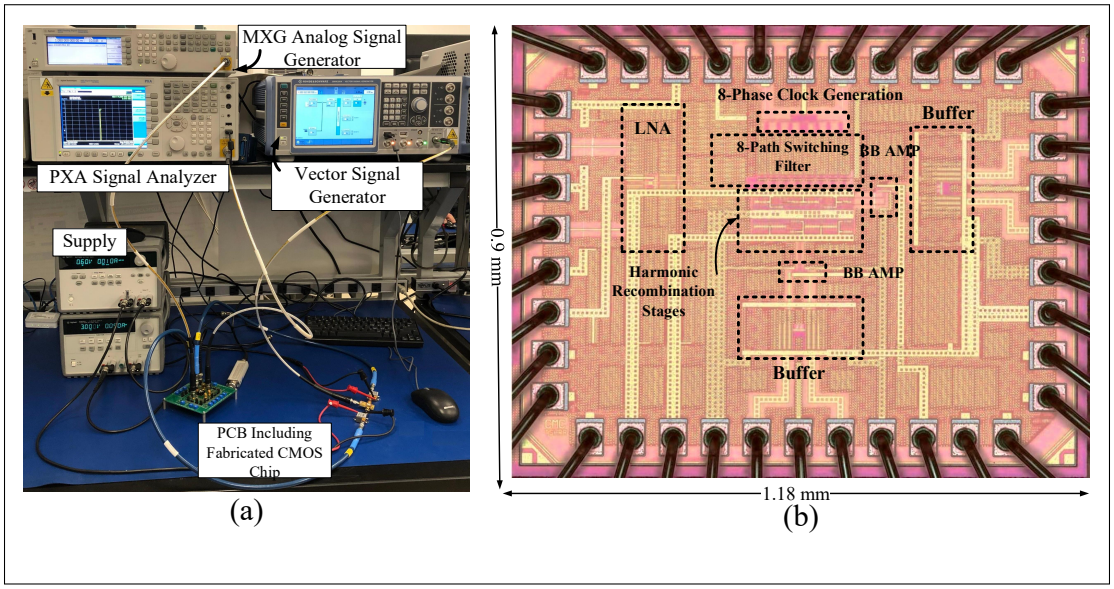

Figure 3.9 (a) Micrograph of the harmonic selection receiver occupying an active area of 0.76 mm × 0.64 mm in 130 nm CMOS, and (b) the measurement setup

The chip was packaged in a 48-pin QFN package and mounted on a PCB for measurements. The measurement setup is shown in Fig. 3.9(a). As the inputs of the receiver and the 8-phase clock generator are differential, wideband RF baluns (MABA-011108) are used to interface to the single-ended 50 Ω signal generator (Rohde & Schwarz SMW200A). The input reflection coefficient (S11), or input return loss, of the receiver was measured by employing a network analyzer (Keysight PNA N5225A). Fig. 3.10(a) depicts the measured and the post-layout simulated results of the input return loss (S11). Note that the discrepancies between the measured

and post-layout simulated results are mainly due to the bond pad parasitics, packaging traces, bond wire, and the use of the external balun. Despite these aspects affecting the return loss, it remains below −10 dB within the operating frequency band, spanning from 0.5 GHz to 6 GHz, and indicating acceptable input matching.

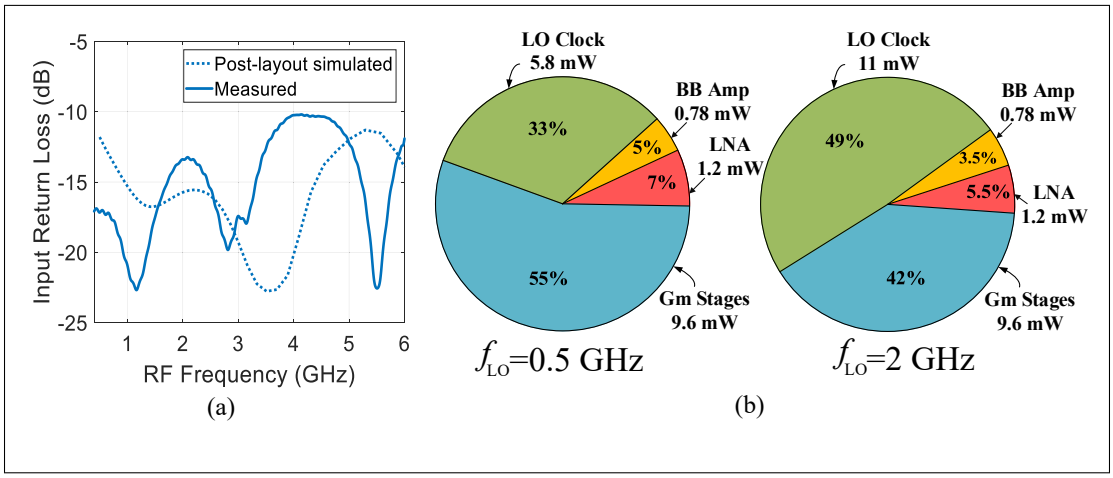

Figure 3.10 a) The post-layout simulated and measured input return loss, and (b) the power consumption breakdown at a 0.5 GHz and 2 GHz switching frequency

The analog circuits (i.e., LNA, BB harmonic recombination circuits and BB amplifier) consume 1.2 mW, 9.6 mW and 0.78 mW from a 1.2 V supply, respectively. This results in total static power (i.e., RF + BB sections) of 11.48 mW. The entire 8-phase LO clock generator block consumes 5.8 −11 mW across the desired operating frequency range of 0.5 GHz to 2 GHz. Fig. 3.10(b) presents the power consumption breakdown at a switching frequency of 0.5 GHz and 2 GHz. The power consumption, especially dynamic power, can be significantly scaled down by implementing the system in a smaller geometry CMOS technology. The post-layout simulation results reported in Shams & Nabki (2022) project a 4× reduction in power consumption if the circuit was implemented in 65 nm CMOS.

As discussed in Section 3.2, the proposed receiver supports low and high frequency bands. In the LB frequency range (i.e., 0.5 −1.9 GHz), the first harmonic of the 8-path switching filter response is selected at the BB frequency, while in the HB frequency range (i.e., 1.95 −6 GHz)

the third harmonic of f_{LO} (i.e., $f_{RF} = 3f_{LO}$) is selected. Several metrics were measured at both the LB and HB frequency ranges in order to verify the operation of the receiver.

3.4.1 Receiver Characterization in the LB Frequency Range

Over the LB frequency range ($f_{RF} = 0.5-1.9$ GHz), where the first LO harmonic is selected, the input RF frequency (f_{RF}) is equal to the f_{LO} ($f_{RF} = f_{LO}$). The measured RF to BB gain and NF over an RF input frequency of $0.5-1.9$ GHz is plotted in Fig. 3.11(a) for a baseband frequency of 80 MHz. The gain response is relatively flat, demonstrating the wide RF bandwidth achieved. The measured voltage conversion gain from the balun input to the differential outputs of the receiver is above 30 dB over the RF range.

The NF was measured by employing a signal analyzer (Keysight N9030A PXA) and a noise source (Keysight 346C). An amplifier (Mini-Circuits ZX60-6013E-S+) was used before the signal analyzer to mitigate the effect of the signal analyzer's noise. When the first LO harmonic is selected, the measured NF varies from 5 dB to 6.4 dB over an LO frequency range of $0.5-1.9$ GHz, as seen in Fig. 3.11(a).

To guarantee proper operation, the proposed receiver is designed to suppress the LO harmonics at up to 9 GHz. The HRR in the first harmonic selection scenario was measured as follows. A -30 dBm input signal was applied to the harmonic selection receiver at a 80 MHz offset from the desired down-conversion frequency (i.e., f_{LO}) to measure the conversion gain. The same input power was applied at the integer harmonics of f_{LO} ($2f_{LO}, ..., 5f_{LO}$), which are attenuated. The HRR is calculated by the ratio of the conversion gain to BB at these LO harmonic frequencies relative to the conversion gain of the desired frequency. Without any calibration, Fig. 3.11(b) shows that the measured 2^{nd}, 3^{rd}, 4^{th}, and 5^{th} HRRs are higher than 53 dB, 44 dB, 62 dB, and 69 dB at a 80 MHz BB frequency, respectively. Note that high HRRs are achieved, as the LO harmonic frequencies are beyond the LNA amplification range. Moreover, Fig. 3.11(c) and (d) plots the measured conversion gain and NF as a function of the BB frequency at the LO frequencies of 1 GHz and 1.8 GHz, showing that the flicker noise can considerably affect the NF

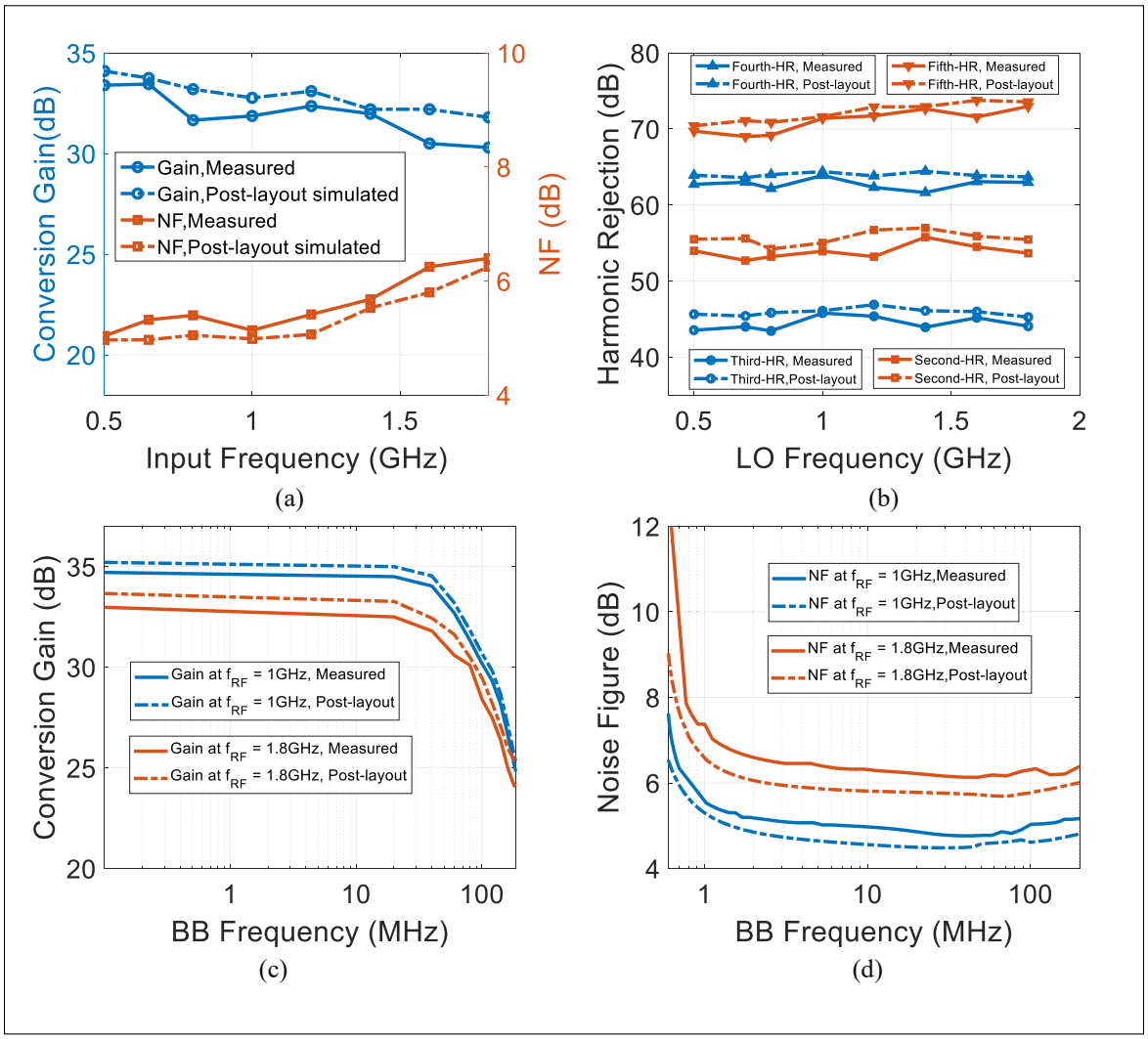

Figure 3.11 Measured and post-layout simulated performance of the proposed receiver operating in the LB frequency range (1^{st} harmonic selection): (a) conversion gain and NF vs. RF frequency at an 80 MHz BB frequency (LO frequency range of 0.5 –1.9 GHz), (b) 2^{nd}, 3^{rd}, 4^{th} and 5^{th} harmonic rejection ratios vs. LO frequency, (c) conversion gain for a 1 GHz and 1.8 GHz RF input vs. the baseband frequency, (d) NF for a 1 GHz and 1.8 GHz RF input vs. the baseband frequency

at BB frequencies under 1 MHz, while a flat NF of 5 dB is achieved at higher BB frequencies. The BB bandwidth is measured to be 80 MHz, which can accommodate the sub-6 GHz 5G standards.

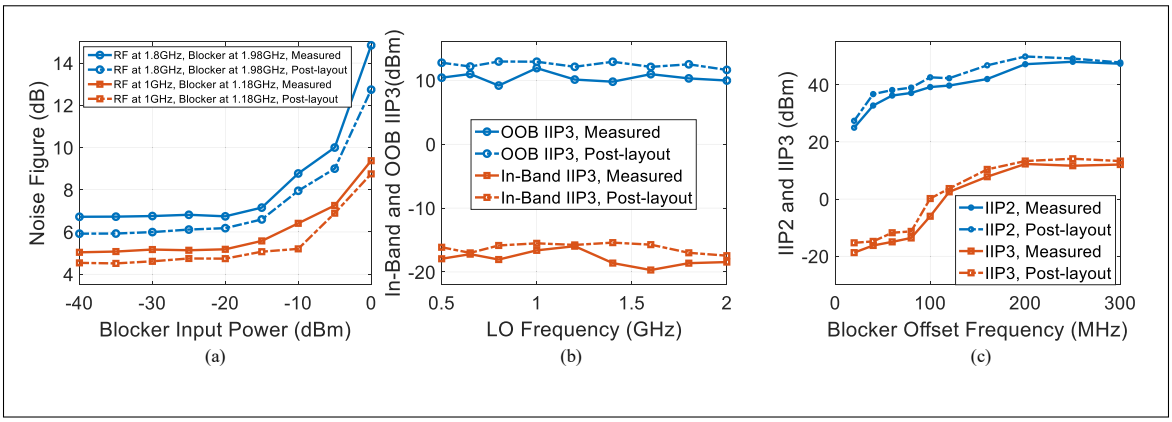

Figure 3.12 Measured and post-layout simulated performance of the proposed receiver operating in the LB frequency range (1^{st} harmonic selection): (a) NF versus blocker power at a blocker offset frequency of 180 MHz for f_{RF} = 1 GHz and f_{RF} = 1.8 GHz, (b) in-band and OOB IIP3 vs. LO frequency and (c) IIP2 and IIP3 vs. blocker offset frequency for a 1 GHz LO frequency

A key specifications for wideband RF receivers is blocker tolerance. The blocker resilience of the proposed receiver is measured by evaluating the NF in the presence of a blocker. A small desired signal at f_{RF} is accompanied by a continues-wave blocker located 180 MHz away (f_{RF} + 180 MHz). This blocker is generated using a signal generator (Keysight E8267D). Then, the blocker amplitude is swept. Fig. 3.12(a) plots the measured NF vs. the blocker input power for an 1 GHz and 1.8 GHz RF desired signal. The proposed RF receiver can tolerate blockers of up to −15 dBm before exhibiting a noise figure deterioration due to gain reduction. For an 1 GHz RF desired signal, the NF degrades to 6.4 dB in the the presence of a −10 dBm blocker. The NF increases to 9.5 dB in the presence of a strong 0 dBm blocker due to gain compression and reciprocal mixing.

To evaluate the linearity performance of the proposed architecture in the LB frequency range, both in-band and OOB IIP3 were measured as a function of the LO frequency and blocker offset frequency, Δf. A two-tone test with frequencies at $[f_{RF} + \Delta f, f_{RF} + 2\Delta f - 1\ MHz]$ was carried-out to measure the IIP3. The in-band and OOB IIP3 were measured at a frequency offset of 40 MHz ([f_{RF}+40 MHz, f_{RF}+79 MHz]) and 200 MHz ([f_{RF}+200 MHz, f_{RF}+399 MHz]), respectively.

The resulting LB frequency range in-band and OOB IIP3 are plotted in Fig. 3.12(b). The in-band IIP3 is seen to be −16.6 dBm at Δf = 40 MHz for a 1 GHz LO frequency, while the OOB IIP3 is better than 9 dBm at Δf = 200 MHz. Note that both in-band and OOB IIP3 are nearly constant over different LO frequencies. To further evaluate the linearity, the IIP3 was measured vs. different blocker frequency offsets at a f_{RF} = 1 GHz when the blocker power is set to −30 dBm, and is shown in Fig. 3.12(c). For a blocker offset frequency under 80 MHz, the in-band IIP3 is dominated by the LNA, 8-path switching filter, and BB harmonic recombination stage. When the blocker offset frequency is above 80 MHz, both tones are OOB. Thus, the harmonic recombination stage and BB amplifier play a minor role in the receiver linearity, and the OOB IIP3 is dictated by the LNA and 8-path switching filter. Since the LNA achieves higher IIP3 by increasing the frequency spacing between the two tones, it determines the maximum achievable receiver linearity. Moreover, Fig. 3.12(c) plots the IIP2 as a function of the blocker frequency offset. To measure IIP2, a two-tone test at $[f_{RF}+\Delta f_{blocker}, f_{RF}+\Delta f_{blocker}+1\ MHz]$ was carried-out. At a 1 GHz RF, the in-band IIP2 with two tones at 1.08 GHz and 1.081 GHz (i.e., blocker offset frequency of 80 MHz) and the OOB IIP2 with two tones at 1.2 GHz and 1.201 GHz (i.e., blocker offset frequency of 200 MHz) are 37 dBm and 48 dBm, respectively.

3.4.2 Receiver Characterization in the HB Frequency Range

Over the HB frequencies, the proposed receiver allows for higher frequency operation by selecting the third harmonic of the LO frequency (i.e., $f_{RF} = 3f_{LO}$). By sweeping the LO switching frequency from 0.65 GHz to 2 GHz, the RF receiver covers the desired HB frequency range (i.e., RF of 1.95 GHz to 6 GHz). This is due to the operation at the third harmonic of the LO frequency to cover the HB frequency range, as previously discussed. In this scenario, the measurement procedure is similar to that of the LB frequency. The measured conversion gain and NF as a function of RF input frequency at a 80 MHz BB frequency are shown in Fig. 3.13(a). The gain varies over the 1.95 −6 GHz frequency range from 27.8 dB to 31.2 dB, and the NF varies from 5.3 dB to 7.1 dB. A better NF performance can be achieved by minimizing the 8-phase LO clocks' overlap to avoid a low-ohmic path between G_m cells' inputs. In addition,

large switches followed by lower noise BB amplifiers can help to alleviate the NF of the receiver, albeit not significantly. Alternatively, frequency translational noise cancellation techniques can be employed to achieve lower noise and higher linearity (Bu *et al.* (2020); Murphy *et al.* (2015)).

Moreover, an RF input at 1, 2, 4 and 5 times of the LO frequency is injected into the receiver to measure the HRRs. Fig. 3.13(b) plots the HRRs vs. LO frequency. The minimum first and second order HR are 38.4 dB and 50 dB, respectively, while the receiver provides an HRR higher than 62 dB for the fourth and fifth harmonics. It should be mentioned that an off-chip adjustable notch filter was employed to provide the high fifth LO harmonic suppression at the HB path.

In Fig. 3.13(c) and Fig. 3.13(d), the measured and post-layout simulated conversion gain and NF are plotted vs. the BB frequency at $f_{RF} = 3f_{LO} = 3$ GHz and 5.4 GHz. The conversion gain drops by 3 dB at a BB frequency of 92 MHz when then input RF is at 3 GHz. Note that the noise from the LO clock generator and buffers at $3f_{LO}$ is coupled to the RF through the 8-path switching system. Thus, the NF degrades after being down-converted to BB by the 8-path switching filter, as discussed in (Murphy *et al.* (2012)). This effect is reflected as a flicker noise. A corner frequency at around 6 MHz is observed.

Fig. 3.14(a) plots the measured and post-layout simulated NF in the presence of a OOB blocker vs. blocker input power. Small desired signals at $f_{RF} = 3$ GHz and $f_{RF} = 5.4$ GHz were accompanied by a single tone blocker at a 180 MHz offset. The blocker amplitude was then swept. The NF is relatively constant up to a -15 dBm and -20 dBm blocker power for a blocker located at 3.18 GHz and 5.58 GHz, respectively. The NF degrades to 15.6 dB when a 0 dBm blocker was present at a 180 MHz offset from the 5.4 GHz RF signal. This added noise mainly originates from reciprocal mixing with the phase noise of the LO. This phase noise is due to the noise of the frequency divider and external input.

At the HB frequency range, the measured and post-layout simulated linearity performance of the third harmonic selection receiver is plotted in Fig. 3.14. Both in-band and OOB IIP3 remain almost flat over the different LO frequencies (see Fig. 3.14(b)). The measured IIP3 and IIP2

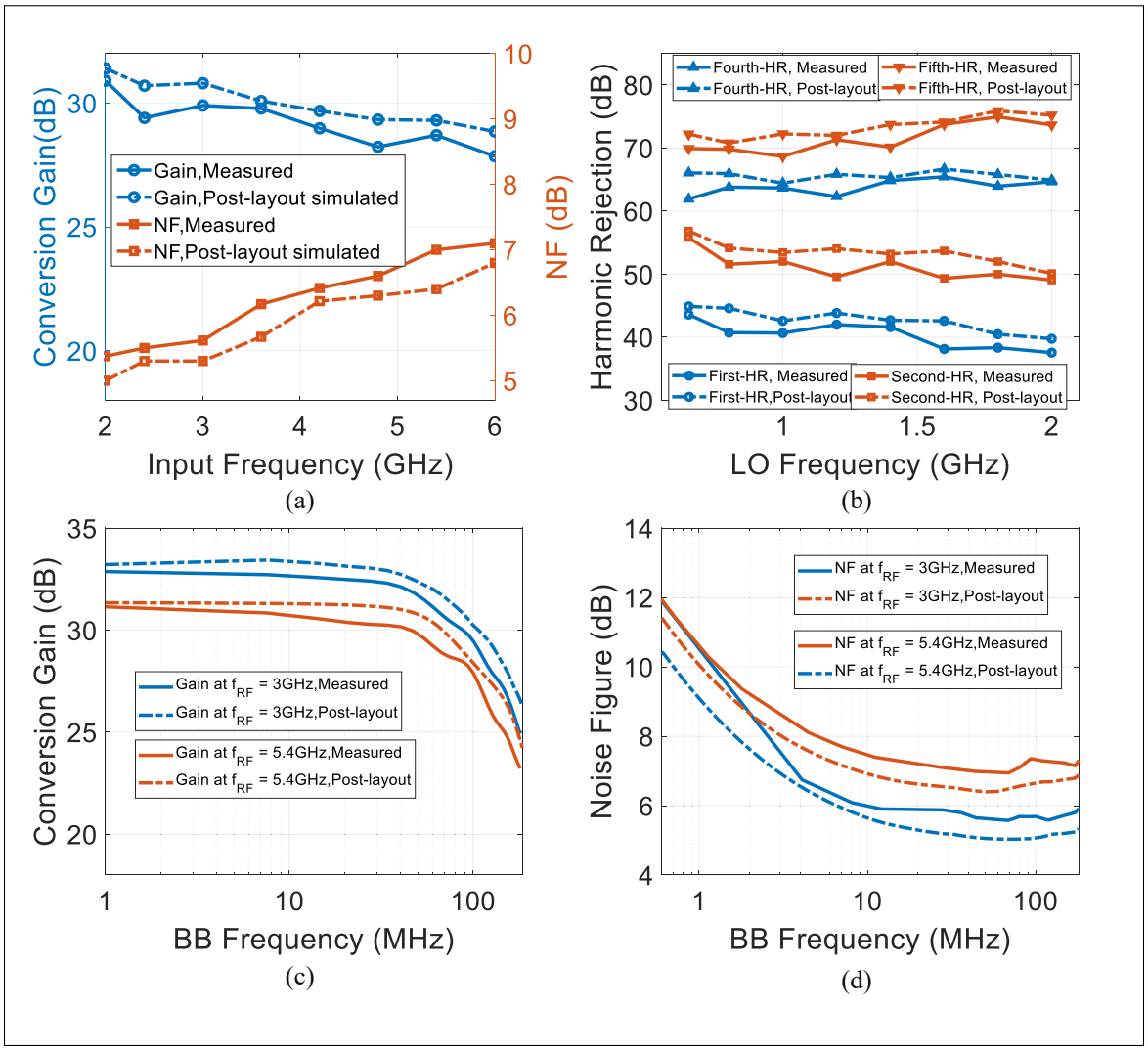

Figure 3.13 Measured and post-layout simulated performance of the proposed receiver operating in the HB frequency range (3^{rd} harmonic selection): (a) conversion gain and NF vs. RF frequency at an 80 MHz BB frequency (LO frequency range of 0.65 −2 GHz), (b) 1^{st}, 2^{nd}, 4^{th} and 5^{th} harmonic rejection ratios vs. LO frequency, (c) conversion gain for a 3 GHz and 5.4 GHz RF input vs. the baseband frequency (f_{LO} = 1 GHz and 1.8 GHz, respectively), (d) NF for a 3 GHz and 5.4 GHz RF input vs. the baseband frequency (f_{LO} = 1 GHz and 1.8 GHz, respectively)

as a function of a blocker of varying offset frequency are plotted for a 1 GHz LO frequency (f_{RF} = 3 GHz) in Fig. 3.14(c). At a blocker offset of 80 MHz, the in-band IIP3 was measured to be about −18 dBm, while the OOB IIP3 and IIP2 are better than 7.8 dBm and 46 dBm at a blocker offset of 200 MHz, respectively.

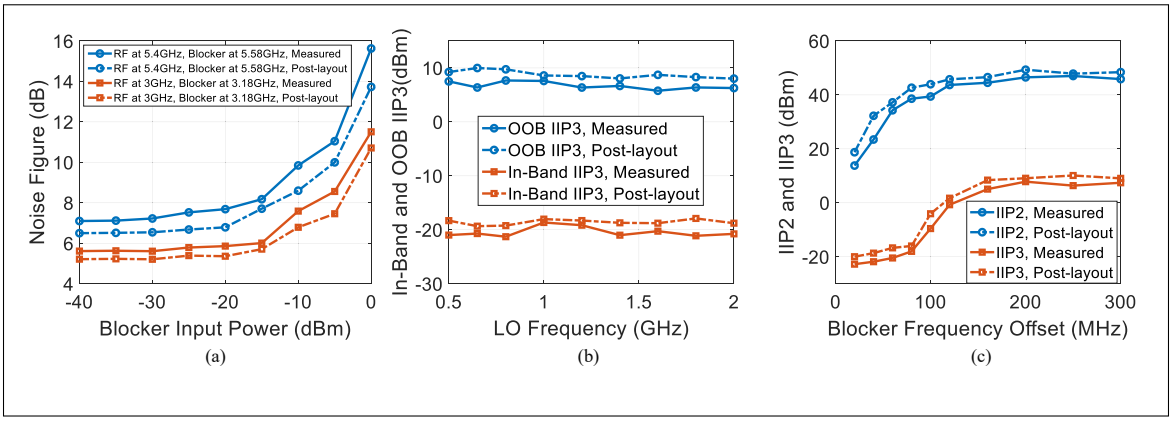

Figure 3.14 Measured and post-layout simulated performance of the proposed receiver operating in the HB frequency range (3^{rd} harmonic selection):(a) NF versus blocker power at a blocker offset frequency of 180 MHz for f_{RF} = 3 GHz and f_{RF} = 5.4 GHz, (b) in-band and OOB IIP3 vs. LO frequency at a frequency offset of 40 MHz and 200 MHz, respectively, and (c) IIP2 and IIP3 vs. blocker offset frequency for a 1 GHz LO frequency

It should be mentioned that the harmonic selection receiver is able to more accurately approximate a sinusoidal LO by using an 8-path switching system, compared to the typical receiver architecture composed of a 4-phase passive mixer. This allows it to achieve a lower NF, higher gain and better HRRs. In addition, since the N-path switching filter employs the BB capacitors and the G_m cells at the harmonic recombination blocks that are fed with the BB signals across the BB capacitors, the circuit behaves as a highly linear multiphase passive mixer. The integrated N-path filters thus provide high linearity and selectivity to mitigate large OOB blockers.

Moreover, the required LO switching frequency ranges from 0.5 −2 GHz to cover the entire RF frequency band of interest (i.e., 0.5 −6 GHz). The input frequency of the LO generator varies from 2 −8 GHz to generate the desired LO switching frequency range. However, the typical receiver architecture operating over an RF frequency band of 0.5 −6 GHz requires an LO switching frequency that varies from 0.5 −6 GHz. Note that two times of the switching frequency (i.e., $2f_{LO}$) is required for the 4-phase LO input in that architecture. Thus, the required LO clock generator driving the 4-phase structure requires an input frequency of 1 to 12 GHz. Designing an LO clock generator operating at a frequency of up to 8 GHz is easier to achieve

than at up to 12 GHz with the conventional structure. As a result, the dynamic power dissipation of the multi-phase LO generator in the proposed harmonic selection receiver is less than that of a conventional receiver thanks to the reduced input frequency of the LO generator.

As seen in Fig. 3.11, Fig. 3.12, Fig. 3.13, and Fig. 3.14, although the post-layout simulation results show slightly different performance than the measured results, there is relatively good agreement between the measurements and simulations. Differences are mostly attributed due to circuits' non-idealities, mismatches, package parasitics and the PCB losses, all of which are expected to degrade performance from that predicted by simulations.

3.4.3 Summary and Comparison to the State-of-the-Art

A performance summary of the proposed blocker tolerant receiver prototype and a comparison to other recently published wideband receivers are shown in Table 3.1. This prototype achieves a comparable power consumption, OOB IIP3, BB bandwidth and area. The proposed architectures in Krishnamurthy & Niknejad (2019); Lien, Klumperink, Tenbroek, Strange & Nauta (2018b); Shao, Qi, Mak & Martins (2021); Xu *et al.* (2017) achieve low NF, high linearity and support an RF input frequency of up to 2 GHz while dissipating more power. The wideband receivers reported in Wu *et al.* (2019) and Razavi & Razavi (2022) operate in the $0.5-3$ GHz and $0.4-6$ GHz frequency range at the cost of $31-38$ mW and $23-49$ mW power consumption, respectively, even though they leverage a smaller geometry technology node. When compared to the recent reported receivers, the proposed blocker tolerant receiver succeeds in significantly reducing the total DC and dynamic power consumption and in supporting a wide RF input frequency band of 3 GHz ($0.5-6$ GHz) without sacrificing OOB linearity, NF and HRR, thanks to the 1^{st} and 3^{rd} harmonic selection architecture. This is notably achieved in a larger geometry technology node than the other works, reducing the implementation cost of the structure. This work thus compares favorably When considering the operating frequency range, LO power, BB bandwidth and area. It also features a fully differential structure and harmonic rejection.

Overall, the fabricated receiver architecture in 130 nm CMOS exhibits performance that compares well to the state-of-the-art implemented in more advanced technologies, illustrating the potential of the proposed harmonic selection architecture to enable low power and low cost blocker-tolerant wideband receivers.

3.5 Conclusion

The ever-increasing demand for wireless data traffic favors the deployment of sub-6 GHz 5G networks. These system require wideband blocker-tolerant receiver front-ends that put a strain on low-power design. In this work, a 0.5 −6 GHz blocker-tolerant harmonic selection RF receiver featuring a wideband LNA, 8-path switching filter and BB 1^{st} and 3^{rd} harmonic recombination blocks has been designed and verified in 130 nm CMOS technology. The proposed blocker-tolerant receiver is able to efficiently suppress blockers at the LO harmonics while suppressing near-band blockers. This is achieved by employing two feed-forward 8-path switching filters for frequency down-conversion. The proposed architecture employs two separate harmonic recombination paths at the BB to select the 1^{st}-order harmonic of the LO frequency in the LB frequency range (0.5 −1.9 GHz), and the 3^{rd}-order LO harmonic in the HB frequency range (1.95 −6 GHz). The 3^{rd} harmonic selection in the HB frequency range helps reduce the frequency and dynamic power consumption of the multi-phase clock generator by a factor of three. Thus, the proposed receiver can support higher RF input signals of up to 6 GHz, while the 8-phase LO frequency operates only at up to 2 GHz with an input clock of up to 8 GHz. Based on the harmonic selection, the proposed wideband receiver achieves good blocker tolerance and harmonic rejection, while consuming substantially less power, compared to the existing architectures operating at such high frequencies.

Measurement results from the fabricated prototype verifies the merits of this work in balancing the HRR, linearity and NF with power and area. In the LB frequency range, the fabricated receiver achieves a 32 dB conversion gain, 80 MHz BB bandwidth, 4.9 dB NF, and 46 dB HRR at a 1 GHz LO. In the HB frequency range, the receiver exhibits a conversion gain of 30 dB, 1^{st} HRR of 41 dB, a NF of 5.6 dB at a 87 MHz BB frequency, for a 3 GHz RF input (i.e., 1 GHz LO) and

92 MHz BB bandwidth, without any trimming or calibration. The receiver provides wideband input matching, with S11 better than −10 dB throughout the measured RF range of 0.5 −6 GHz. The RF front-end consumes 11.5 mW and its clock generator only consumes 5.8 −11 mW.

Ultimately, this work demonstrates a blocker-tolerant wideband receiver front-end architecture that provides good performance metrics and low-power operation at high operating frequencies, and that is well-suited to low-cost implementations in larger geometry technology nodes.

3.6 Appendix A

In the proposed architecture, the LNA is driving a low impedance. It is assumed that the output voltage swing is small. Thus, the transistor conductance (g_{ds}) exhibits negligible nonlinear effects. The main source of non-linearity originates from the LNA transconductance. By carrying-out a series expansion of the nonlinear transistor model, the drain current of M_A is given by

$$i_{ds_{M_A}} = g_{m_{M_A}} V_{gs} + \frac{g'_{m_{M_A}}}{2!} V_{gs}^2 + \frac{g''_{m_{M_A}}}{3!} V_{gs}^3 + ..., \tag{3.11}$$

where $g_{m_{M_A}} = \partial i_{D_{M_A}} / \partial v_{GS}$, $g'_{m_{M_A}} = \partial^2 i_{D_{M_A}} / \partial^2 v_{GS}$, and $g''_{m_{M_A}} = \partial^3 i_{D_{M_A}} / \partial^3 v_{GS}$. Note that $g_{m_{M_A}}$ is the linear gain while $g'_{m_{M_A}}$ and $g''_{m_{M_A}}$ are the second-order and third-order non-linearity coefficients, respectively. To achieve a good linearity, the coefficients of the second and third terms in (3.11) should be close to zero, by adjusting the size and gate bias of M_A and M_B. Note that $g'_{m_{M_B}}$ is defined as $\partial i^2_{D_{M_B}} / \partial v^2_{GS}$, where $i_{D_{M_B}}$ is the channel current of the transistor PMOS of M_B flowing from its drain to source. The relation between $i_{D_{M_B}}$ and v_{GS} is expressed as $-i_{D_{M_B}} = K_p(V_{SG_{M_B}} - |V_{th}|^2)$ in the saturation region, where K_p is a positive constant number. Thus, $g'_{m_{M_B}}$ is a negative number, as opposed to the $g'_{m_{M_A}}$. Thus, the total output current from

$v_{out1,LNA}$ is expressed by

$$\begin{aligned} i_{out1,LNA} = i_{ds_{M_A}} - i_{ds_{M_B}} = i_1 + i_2 + i_3 + ... \\ (g_{m_{M_A}} + g_{m_{M_B}})v_{gs} + (g'_{m_{M_A}} - g'_{m_{M_B}})\frac{v_{gs}^2}{2!} \\ +(g''_{m_{M_B}} + g''_{m_{M_A}})\frac{v_{gs}^3}{3!} \end{aligned} \tag{3.12}$$

where i_j is the j^{th} th harmonic current in the current-reuse topology of the LNA. Note that the combination of NMOS and PMOS transistors in the current-reuse topology helps to reduce the even-order distortion coefficients.

However, the output current of the LNA according to (3.12) suffers from third-order non-linearity. To calculate the third-order nonlinear current, a two-tone test input at ω_1 and ω_2 with the same amplitude is assumed. The output IM3 voltage due to M_A is given by

$$V_{out1,LNA_{2\omega_1-\omega_2}} - V_{out2,LNA_{2\omega_1-\omega_2}} = 2i_{2\omega_1-\omega_2} \times \frac{R_F}{4(g_{m_{M_A}} + g_{m_{M_B}})R_s} \tag{3.13}$$

where $i_{2\omega_1-\omega_2}$ is the IM3 current and can be given by

$$i_{2\omega_1-\omega_2} = \frac{3}{4}a_3A^3, a_3 = \frac{1}{3!}\frac{\partial I_{D_{M_A,M_B}}}{\partial V^3_{GS_{M_A,M_B}}} \tag{3.14}$$

where a_3 is the third-order coefficient in $i_{d,M_A,M_B} = a_1V_{gs,M_A,M_B} + a_2V^2_{gs,M_A,M_B} + a_3V^3_{gs,M_A,M_B}$ Zhang & Sánchez-Sinencio (2010) that is derived from the large signal relation between $V_{GS_{M_A,M_B}}$ and $I_{D_{M_A,M_B}}$. Thus, the IIP3 caused by M_{1A} and M_{1B} (M_{2A} and M_{2B}) can be calculated. A lower value of $V_{GS_{M_A}}$ and $V_{GS_{M_B}}$ provides better linearity performance.

3.7 Appendix B

The RF input voltage V_{RF} drives the LNA. The differential RF output signal of the LNA is then down-converted by two 8-path switching filters, and the resulting BB signals are recombined by BB harmonic recombination blocks. It is assumed that the LNA's output impedance is

very large, compared to the up-converted BB impedance and the switch impedance. The noise contributors in the receiver architecture are the antenna ($\overline{V^2_{out_{ANT}}}$), LNA ($\overline{V^2_{out_{LNA}}}$), switches ($\overline{V^2_{out_{R_{SW}}}}$), BB harmonic recombination circuitry ($\overline{V^2_{out_{WHRB}}}$), and BB amplifier's ($\overline{V^2_{out_{AMP}}}$) noise. The noise factor of the receiver is approximately given by

$$F \cong \frac{\overline{V^2_{out_{ANT}}} + \overline{V^2_{out_{LNA}}} + \overline{V^2_{out_{R_{SW}}}} + \overline{V^2_{out_{WHRB}}} + \overline{V^2_{out_{AMP}}}}{|A_{V,RX}|^2 4kTR_S}, \tag{3.15}$$

The noise contributed by the antenna experiences the conversion gain similarly to the input signal. Thus, the output noise due to the antenna ($\overline{V^2_{out_{ANT}}}$) can be given by

$$\overline{V^2_{out_{ANT}}} = \sum_{i=-\infty}^{\infty} \left| A_{v_{[\rho,\rho-iN]_{RX}}}(\omega) \right|^2 \overline{V^2_{n,R_S}}, \tag{3.16}$$

where the subscript ρ corresponds to the ρ^{th} harmonic that is received by the receiver. The receiver is required to down-convert the signals around the fundamental and third harmonic, and thus ρ is equal to 1 and 3, respectively. Equation (3.16) expresses the folding of the noise from all harmonics.

The noise contributed by the LNA ($\overline{V^2_{out_{LNA}}}$), is the significant noise contributor, as expected. The output noise due to the LNA is expressed by

$$\overline{V^2_{out_{LNA}}} = \left| A_{V_{LNA}} A_{V_{WHRB}} A_{V_{BB,AMP}} \right|^2 \overline{V^2_{n,LNA}} \tag{3.17}$$

where $A_{V_{WHRB}}$ and $A_{V_{BB,AMP}}$ are the gain of the harmonic recombination block of the BB circuitry, and the voltage gain of the BB amplifiers, respectively. It is assumed that $\overline{V^2_{n,LNA}} = 4kT\gamma/A_{V_{LNA}}$. To minimize the noise contributed by the LNA, the largest $A_{V_{LNA}}$ practically possible was implemented.

The noise associated with the 8-path switches and BB circuitry will not contribute significantly to the total output noise when the LNA output impedance and the receiver gain are large enough. This is because the BB harmonic recombination circuits are current driven, and since only one switch is turned ON at any given time, the series voltage noise sources cannot generate a noise current.

Table 3.1 Performance summary and comparison to the state-of-the-art

Parameters	Xu *et al.* (2017) JSSC' 17	Lien *et al.* (2018b) JSSC' 18	Wu *et al.* (2019) JSSC' 19	Krishnamurthy & Niknejad (2019) JSSC' 19	Shao *et al.* (2021) TCAS-I' 21	Razavi & Razavi (2022) JSSC' 22	This work	This work
Technology (nm)	65	28	28	28	28	28	130	130
RF Input	Differential	Differential	Single-Ended	Single-Ended	Single-Ended	Single-Ended	Differential	Differential
Receiver Topology	HR-NPF	Bottom Plate Mixing in N-Path Filter	Harmonic Selective Noise Canc.	N-Path Filter Driving Z with 40 dB/dec. Roll -off	N-Path LNA OB Blocker Cancelation+ FA BB Amp.	H-trap technique	First Harmonic Selection	Third Harmonic Selection
RF Freq. (GHz)	0.2-1	0.1-2	0.5-3	0.2-2	0.1 -2	0.4-6	0.5-1.9	1.95-6
BB BW (MHz)	2	6.5	49	18	20	0.2-160	80	92
Gain (dB)	36	16	42	13	24	54	34	30
NF (dB)	5.4-6	4.1-10.3	2.4-5	4.3-7.6	3.1^{+}	2.1-4.42	5	6
OOB IIP3 (dBm)	9 @ 20MHz	+44 $\Delta f/BW$=12.3	4 @ 50MHz	33.3 @80MHz	5.4 @80MHz	9.8	9	7.2
In-Band IIP3 (dBm)	-	15	-	-	0^{Δ}	$-30^{\S}$	-16.6	-18
HRR (dB)	51	-	$45^{\star}$	-	-	62.3	44	38
HR Calibration	N0	-	YES	-	NO	NO	NO	NO
Power (mW)	$26-32^{\natural}$	$38\text{-}96^{\dagger}$	$31\text{-}38^{\diamond}$	$146.6\text{-}179^{\star\star}$	22^{+}	23-49	17-22.5	17-22.5
Active Area mm^2	0.29	0.8	1.2	0.48	0.24	1.9	0.48	0.48

$^{\natural}$ 24 mW for analog circuits and 2 −8 mW for clock. † 30 mW for baseband amplifier and 33 mW/GHz for LO. * HRR of 45 dB without calibration and higher than 80 dB with calibration.$^{\diamond}$ 21 mW for receiver and 7 −10 mW for LO. ** 143 mW for active synthesis of the impedance and TIA and 3.6 −36 mW for LO. $^{+}$ at 2 GHz RF. $^{\Delta}$ at 20 MHz. § at 120 MHz offset from 5 GHz.

CHAPTER 4

A BLOCKER TOLERANT HARMONIC SELECTION NOISE-CANCELLING RF RECEIVER FOR 5G AND WI-FI 6E APPLICATIONS

The presented harmonic selection receiver in Chapter 3 can operate at the frequency range of $0.5-6$ GHz, and achieves a NF of $5-6.4$ dB over the low frequency band ($0.5-1.9$ GHz) and $5.3-7.1$ dB over the high frequency band ($0.5-1.9$ GHz). One potential research direction can be to enhance the noise performance of the proposed RF front-end without sacrificing interference resilience. Among different approaches proposed to enhance the receiver's performance, the noise cancellation technique is one of the most promising.

Thus, the contribution of this chapter is the presentation of two wideband harmonic selection noise-canceling RF receivers exploiting a resistive harmonic selection 8-path filter and noise cancellation technique to achieve optimum performance in terms of HRRs and NF. The architectures employ two steps of harmonic selection, providing more rejection at the undesired harmonic blockers. Moreover, both receivers are able to select the higher-order LO harmonics in addition to the fundamental one. Thus, this reduces the dynamic power consumption and required input frequency of the multi-phase LO clock generator.

A Blocker Tolerant Harmonic Selection Noise-Cancelling RF Receiver for 5G and Wi-Fi 6E Applications

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Abstract: Two wideband harmonic selection noise-cancelling (HS-NC) RF receiver front-ends are presented, which are capable of supporting 5G new radio (NR) and Wi-Fi 6E applications, and operate from 0.5 GHz to 7.2 GHz. Their architecture employs a differential harmonic selection N-path filter (HS-NPF) with resistive coefficients to avoid voltage gain at harmonic blocker frequencies, and exploits baseband (BB) harmonic recombination blocks to select the desired local oscillator (LO) harmonics, in addition to featuring noise cancelling. It is demonstrated how a conventional feed-forward NPF, two separate resistive HS-NPF down-conversion paths, and BB harmonic recombination stages are configured to select the first LO harmonic at the low frequency band (0.5 −2.4 GHz) and the third harmonic of the LO frequency at the high frequency band (2.4 −7.2 GHz). Higher harmonic selection rather than the fundamental helps to reduce the dynamic power consumption and required input frequency of the multi-phase LO clock generator at the high frequency band. The two RF receiver front-ends are fabricated in a TSMC 65 nm CMOS technology. The first receiver (RX1) achieves a harmonic-rejection ratio (HRR) of higher than 44 dB without any calibration, a minimum in-band NF of 3.4 dB at a 80 MHz BB frequency, and OOB IIP3 of higher than 9.2 dBm over the entire frequency band of operation, with a power consumption of 14.5 −20.8 mW, including the LO generation circuit. The second receiver's (RX2) NF is 3.9 −4.8 dB, and in-band IIP3, OOB IIP3, 3^{rd} and 1^{st} HRRs are higher than −21.6 dBm, 6.7 dBm, 42 dB, and 37 dB, respectively. The receiver has a total power consumption of 11.1 −17.4 mW from a 1.2-V supply. The key difference between both receivers is that the harmonic recombination blocks are employed right after the down-conversion in RX1, while a bank of TIAs is used between the down-conversion paths and the

harmonic recombination blocks in RX2. RX1 provides better performance at the cost of higher power consumption in comparison to RX2.

Keywords: Wideband receiver front-end, N-path switching filter, harmonic recombination, noise cancellation, non-overlapping clocks, harmonic rejection, blocker tolerant, Wi-Fi 6E, 5G new radio.

4.1 Introduction

The ever-growing demand for high data rates and wireless data traffic in mobile applications is driving fast adoption of 5G and Wi-Fi 6E. 5G and Wi-Fi are complementary technologies working together to meet businesses' and citizens' connectivity requirements. 5G aims to support a wide range of enhanced services, including self-driving vehicles, factory automation and IoT. Moreover, 5G smartphones need to integrate sub-6 GHz bands initially to provide a monolithic transition from 4G to 5G Balteanu (2019). In addition, 5G new radio (NR) supports a channel bandwidth of up to 100 MHz in the sub-6 GHz frequency band Equipment (2018); Su *et al.* (2022), and requires fast on/off transitions of less than 10 µsec to support the required short transition-time intervals Paek, Kim, Bang, Baek, Choi, Nomiyama, Han, Choo, Youn, Park et al. (2019).

In addition to 5G NR, Wi-Fi achieved remarkable success in the deployment of IoT networks over the last two decades. Recently, the IEEE introduced a new task group, i.e., the Wi-Fi 6 or IEEE 802.11ax, to investigate and realize next-generation Wi-Fi technologies for dense IoT networks having a large number of data links (Chen *et al.* (2020); López-Pérez *et al.* (2019); Maldonado *et al.* (2021)). According to the IEEE 802.11ax standard, the current generation of Wi-Fi, known as Wi-Fi 6, includes devices that can operate in the 6 GHz band (5925 −7125 MHz), referred to as Wi-Fi 6E. With access to a 1200 MHz band, wider channel bandwidths of 160 MHz and 320 MHz, can now be supported Plückebaum, Sörries, Wissner, Elbanna, Strube Martins & Godlovitch (2021).

These wider channel bandwidths enable high data rate applications and increase spectrum efficiency, while keeping the ability to share spectrum with other unlicensed deployments. Moreover, since many 5G NR and Wi-Fi-based devices are battery powered, there is an increasing demand to improve power consumption, form factor and cost. Such enhancements can be achieved by a high level of integration in advanced CMOS processes at the expense of relatively high costs however. A wideband receiver supporting 5G NR and Wi-Fi applications must satisfy the required specifications while maintaining a low NF, proper input matching, and high linearity,

across a wide input frequency range. Ideally, it should also be amenable to implementation in a low-cost CMOS technology node.

While versatile, a wideband receiver is sensitive to both the desired signal and undesired blockers or out of band (OOB) interferers since it has typically weak frequency selectivity. Blockers may appear very close to the desired frequency channels, and thus pose a challenge to maintaining a high dynamic range. At low blocker powers, the noise figure (NF) of the receiver and corresponding thermal noise floor dominate the in-band noise Zhang, Zhu & Kinget (2018a). As the blocker power becomes large, the reciprocal mixing of the blocker with the LO phase noise introduces additional noise in the receive band and desensitizes a receiver Murphy *et al.* (2012). In addition to the reciprocal mixing, the gain compression and intermodulation challenges of wideband receivers are exacerbated without input pre-filtering.

Different approaches, such as N-path switching filters Haq, Englund, Antonov, Tenhunen, Stadius, Kosunen, Östman, Koli & Ryynänen (2020); Xu *et al.* (2017), N-path notch filters Shams & Nabki (2021b), mixer-first receivers Jayasuriya *et al.* (2014); Krishnamurthy & Niknejad (2019), and noise-cancelling receivers Bu *et al.* (2020); Han & Kinget (2021); Murphy *et al.* (2015); Wu *et al.* (2015), have shown the most promising performance in terms of filtering, noise, and linearity, while keeping reasonably good tunability of the bandwidth (BW) and the LO frequency. N-path switching filters are widely used as an integrated RF filtering technique and provide a high-Q factor and large tuning range that is set by the LO frequency (f_{LO}). The N-path switching system translates the BB low-pass response to the RF node through the switches driven by N-phase LO clocks. However, the switches' ON-resistances limit the stop-band rejection characteristics. In addition, the N-path switching system demonstrates limited selectivity and insufficient blockers' suppression at the LO harmonics frequencies. To overcome these limitations, harmonic rejection (HR) receivers based on the N-path switching technique have been proposed by utilizing precise weighting coefficients and more clock phases Forbes *et al.* (2013); N. Shams & Nabki (2020); Nguyen, Kim, Han, Lee, Kim & Lee (2018); van Liempd *et al.* (2014). The harmonic rejection can be achieved either at BB or before the down-conversion (at the RF node).

The trade-off between the NF, linearity, and wideband matching can be enhanced by utilizing the frequency translational noise cancellation (FTNC) technique that has been successfully extended to the mixer-first topology to cancel noise Han & Kinget (2021); Lenka & Banerjee (2019); Murphy *et al.* (2015); Wu *et al.* (2019). Its mixer-first branch (main path) provides tuned RF input matching by translating the BB impedance to its LO frequency. The auxiliary path measures the up-converted noise from the main path at the RF input. The BB outputs of these two signals are combined to cancel out the noise for better receiver sensitivity. The harmonic-selective FTNC receiver proposed in Wu *et al.* (2019) combines 32-phase over-sampling mixers with the FTNC concept to achieve a $2.4-5$ dB NF while consuming $28-31$ mW. Furthermore, the large G_m value in the LNTA limits the OOB IIP3 to 4 dBm. The architecture proposed in Wang, Wang & Heydari (2021) exploits a band-pass common-gate (CG) amplifier with an N-path notch filter feedback loop to provide a low NF of $2.1-2.5$ dB and a moderate channel selection at the receiver input while consuming $68-95$ mW. However, using a passive mixer at the input does not provide sufficient LO harmonic blocker rejection since most of the RF input matching is provided by the switch resistance of the passive mixer.

Therefore, the challenge lies in designing a wideband receiver architecture to improve blocker-tolerance, notably at the LO harmonics, without sacrificing die area and power consumption. Accordingly, this paper presents two fully-differential noise-cancelling RF receiver front-ends with enhanced harmonic blocker tolerance that are able to support both 5G NR and Wi-Fi 6E applications. The architectures are able to tolerate LO harmonic blockers without sacrificing noise performance and to alleviate the need for surface acoustic wave (SAW) pre-filters, while allowing for low-power LO clock generation. The receiver architectures employ two resistive harmonic selection N-path filters (HS-NPF), include a feed-forward NPF, leverage the FTNC technique and perform harmonic recombination at the BB. The two-stage harmonic selection topology helps to improve the receiver linearity for blockers at the LO harmonics. It should be mentioned that the key difference between the two HS-NC architectures is that the harmonic recombination blocks are employed right after the down-conversion in the first front-end (named RX1), while a bank of TIAs is used between the down-conversion paths and the harmonic

recombination blocks in the second front-end (named RX2). It will be demonstrated that in RX1, when the BB signals are appropriately weighted and summed right after the down-conversion, a better rejection at the the LO harmonics is achieved along with a lower NF. This is in contrast to RX2, where the down-converted signals are amplified before the BB harmonic recombination.

Since the proposed architecture exploits three separates down-conversion paths, driving the switches of the N-phase switching filter (i.e. $N = 8, 16, 32, ...$) results in considerable high power dissipation, even in smaller CMOS technologies. Thus, selecting higher order (i.e. 3^{rd}) harmonics of the LO signal in addition to the fundamental one reduces the dynamic LO power consumption and required input frequency of the LO clock generation by a factor of N. Accordingly, for the proposed architecture, the input RF frequency is split at 2.4 GHz into a low band (LB) frequency range, from $0.5 - 2.4$ GHz, and a high band (HB) frequency range, from $2.4 - 7.2$ GHz. Therefore, the proposed HS-NC receiver architecture is able to cover higher frequencies of up to 7.2 GHz by operating at the 3^{rd} order LO harmonic. In the proposed HS-NC receiver architecture, two resistive HR N-path switching filters and BB harmonic recombination blocks are configured to select the 1^{st} harmonic of the LO frequency in the LB frequency range and the 3^{rd} LO harmonic in the HB frequency range. The RF range split results in a relaxed trade-off between low-power LO clock generation at higher frequencies, and OOB filtering at lower frequencies.

Compared to the noise cancelling (NC) architecture proposed in Murphy *et al.* (2012,1); Wu *et al.* (2019), the distinguishing features in the proposed work are the use of differential harmonic selection switching filters with resistive coefficients to select the first and third LO harmonics in the voltage-driven main paths and a wideband LNA followed by conventional N-path switching filter in the auxiliary path, rather than the multiple RF-G_ms used in Murphy *et al.* (2015). Moreover, the proposed HS-NC architecture attenuates the unwanted down-converted harmonics before the BB G_m-cells and reduces the load impedance of the LNA at the LO harmonic frequencies, such that high OOB linearity at the high-order LO harmonics can be achieved.

This paper is organized as follows. Both noise cancelling harmonic selection receiver ftont-ends are described in Section 4.2. The harmonic selection switching filter based on a resistive coefficients technique is presented in Section 4.3. The transistor-level circuit implementation of the receivers is detailed in Section 4.4. Section 4.5 presents the measurement results and discusses the performance metrics of the both receiver front-ends in comparison to the state-of-the-art. This is followed by a discussion and a conclusion.

4.2 Harmonic Selection Noise-Cancelling Architecture of RX1 and RX2

Two wideband HS-NC RF front-ends presented are capable of supporting 5G NR and Wi-Fi 6E applications, and operate from 0.5 GHz to 7.2 GHz. The RX1 and RX2 architectures exploit the noise-cancelling and a resistive HS-NPF techniques to avoid voltage gain at harmonic blocker frequencies, in addition to BB harmonic recombination blocks to select the first LO harmonic at the low frequency band (0.5 −2.4 GHz) and the third harmonic of the LO frequency at the high frequency band (2.4 −7.2 GHz). These techniques help to enhance the receiver's large-signal resilience to LO harmonic blockers. However, two architectures are different in where harmonic blockers' suppression happens and it is investigated how the BB harmonic selection block placement effects on the receiver performance including HRRs, NF and linearity.

The differential architectures of the two HS-NC RF receiver front-ends of RX1 and RX2 are illustrated in Fig. 4.1 and Fig. 4.2, respectively. They both employ a frequency translational noise-cancelling technique and differential 8-path harmonic selection switching system, and they were both fabricated in TSMC 65 nm CMOS technology. The HS-NC receiver front-ends consist of three down-conversion paths, namely a main path for first harmonic selection ($MP-1^{st}HS$), a main path for third harmonic selection ($MP-3^{rd}HS$), and an auxiliary path. In both RX1 and RX2, the two main paths exploit the differential HS-NPFs with resistive coefficients to select the 1^{st} and 3^{rd} harmonic of f_{LO}, while the auxiliary path employs a conventional feed-forward switching filter (see Fig. 4.1 and Fig. 4.2). The auxiliary path provides the voltage measurement required for noise cancellation by using an LNA that is followed by a feed-forward switching filter.

In RX1, the down-converted signals in the auxiliary path are then recombined by employing two harmonic recombination blocks at the BB. The main paths represent a mixer-first receiver, which has a passive mixer and a BB amplifier. The RF current is down-converted to the BB by the 1^{st} HS-NPF and 3^{rd} HS-NPF systems in the main paths, and the in-band current is converted to a voltage by using the BB harmonic recombination blocks, as shown in Fig. 4.1. The HS-NPFs used in the main paths attenuate the undesired harmonic blockers at the RF input node, and up-convert the input impedance of the BB harmonic recombination to provide the input impedance matching.

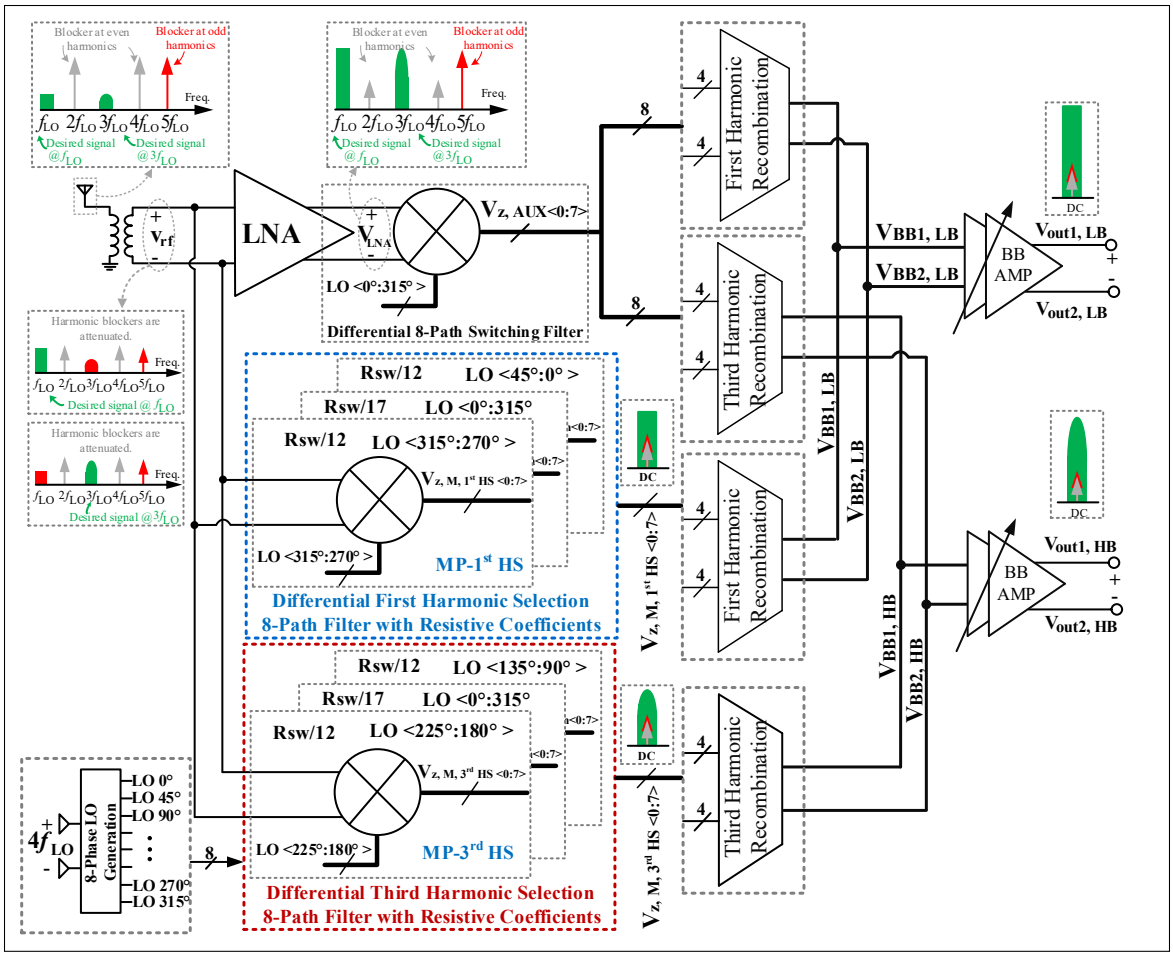

Figure 4.1 Block diagram of the proposed architecture of the HS-NC front-end RX1

The RF input frequency is split into a low band (LB) ranging from 0.5 to 2.4 GHz and a high band (HB) ranging from 2.4 to 7.2 GHz. When the receiver operates in the LB frequency range, the 1^{st} HS-NPFs in the main path and the conventional feed-forward switching filter in the auxiliary path are activated. Note that the 3^{rd} HS-NPF in the other main path and BB 3^{rd} harmonic recombination blocks are powered off. The 1^{st} HS-NPF in the main path selects and down-converts the desired fundamental harmonic of the LO frequency (f_{LO}) to the BB ($V_{Z,M,1^{st}HS<0:7>}$), and suppresses the other LO harmonics. In addition, the auxiliary path simultaneously down-converts the amplified RF signal by employing a feed-forward switching filter ($V_{Z,AUX<0:7>}$). The BB 1^{st} harmonic recombination blocks of the main and auxiliary paths synthesize down-converted signals $V_{Z,M,1^{st}<0:7>}$ and $V_{Z,AUX<0:7>}$, respectively. Then, these are followed by a BB variable gain amplifier to sum the outputs of the BB 1^{st} harmonic recombination blocks ($V_{BB1,LB}, V_{BB2,LB}$). In addition to the signal recombination, this stage provides a desired magnitude and phase shift between the two main and auxiliary down-conversion paths to achieve noise cancelling. Note that the two stages of harmonic selection help to provide more rejection at the undesired harmonic blockers. All of the switches in the conventional switching filter and HS-NPFs are driven by N-phase non-overlapping clocks operating at f_{LO}. Fig. 4.1 with the spectrum annotated at each node shows how a harmonic blocker located at $3f_{LO}$ is suppressed through the 1^{st} HS-NPF and the BB 1^{st} harmonic recombination blocks over the LB frequency range.

Over the HB frequency range of 2.4 to 7.2 GHz, the 3^{rd} HS-NPF in the main path and the BB 3^{rd} harmonic recombination blocks in the main and auxiliary paths are configured to select the 3^{rd} LO harmonic and suppress other harmonic blockers (as shown in Fig. 4.1). Note that the 1^{st} HS-NPF and BB 1^{st} harmonic recombiner in both main and auxiliary paths are powered down. This reduces the DC power consumption and dynamic power consumption. The down-converted signals at the outputs of the conventional 8-path switching filter and 3^{rd} HS-NPF ($V_{Z,AUX<0:7>}$ and $V_{Z,M,3^{rd}HS<0:7>}$) are appropriately weighted and summed in the BB 3^{rd} harmonic recombiners of the main and auxiliary paths, as shown in Fig. 4.1. To cancel the main

path's noise, the outputs of the both BB 3^{rd} harmonic recombiners are fed into the BB amplifier as previously discussed.

In RX1, the signals down-converted by the main and auxiliary paths are recombined by employing the BB 1^{st} and 3^{rd} harmonic recombination blocks right after down-conversion over the LB and HB frequency ranges, respectively. Alternatively, the down-converted signals can be amplified by employing a bank of TIAs right after the down-conversion, and then recombined by exploiting the BB harmonic recombination blocks. This is what is done in RX2.

RX2 aims to investigate the effect of amplifying the down-converted harmonics' before the BB recombination on receiver performance. The conceptual diagram of RX2 is shown in Fig. 4.2. While the LNA, conventional feed-forward switching filter, 1^{st} and 3^{rd} HS-NPFs used in the RX2 are identical to that of the RX1, the two receivers differ in the BB configuration. While RX1 employs BB harmonic recombination blocks right after both conventional and HR down-conversions, RX2 employs a bank of conventional TIAs in the main and auxiliary paths to convert the down-converted currents to voltages and provide amplification. As shown in Fig. 4.2, the TIAs' outputs of the main and auxiliary paths ($V_{Z,M,1^{st}<0:7>}$, $V_{Z,M,3^{rd}<0:7>}$, $V_{Z,AUX<0:7>}$) are appropriately weighted and summed with the BB weighting and recombination blocks ($V_{BB,LB}$ and $V_{BB,HB}$). In addition to signal recombination, this stage adjusts the gains and phases of both paths to cancel the noise of the main path. Moreover, it provides more rejection at the undesired LO harmonic blockers and generates differential outputs at f_{LO} and $3f_{LO}$. In the main paths, the input impedance of the TIAs is up-converted to the RF input through the 1^{st} and 3^{rd} HS-NPFs and thus provides input matching.

Since the down-converted LO harmonics in RX1 at each of the LB and HB frequencies are recombined by employing two BB harmonic recombination blocks at the main and auxiliary paths, as opposed to RX2 that exploits one BB harmonic recombination block after a bank of TIAs, it is expected that RX1 will achieve the better performance in terms of HRRs, gain and NF. However, RX2 is expected to dissipate less power, compared to RX1, as it employs two 1^{st}

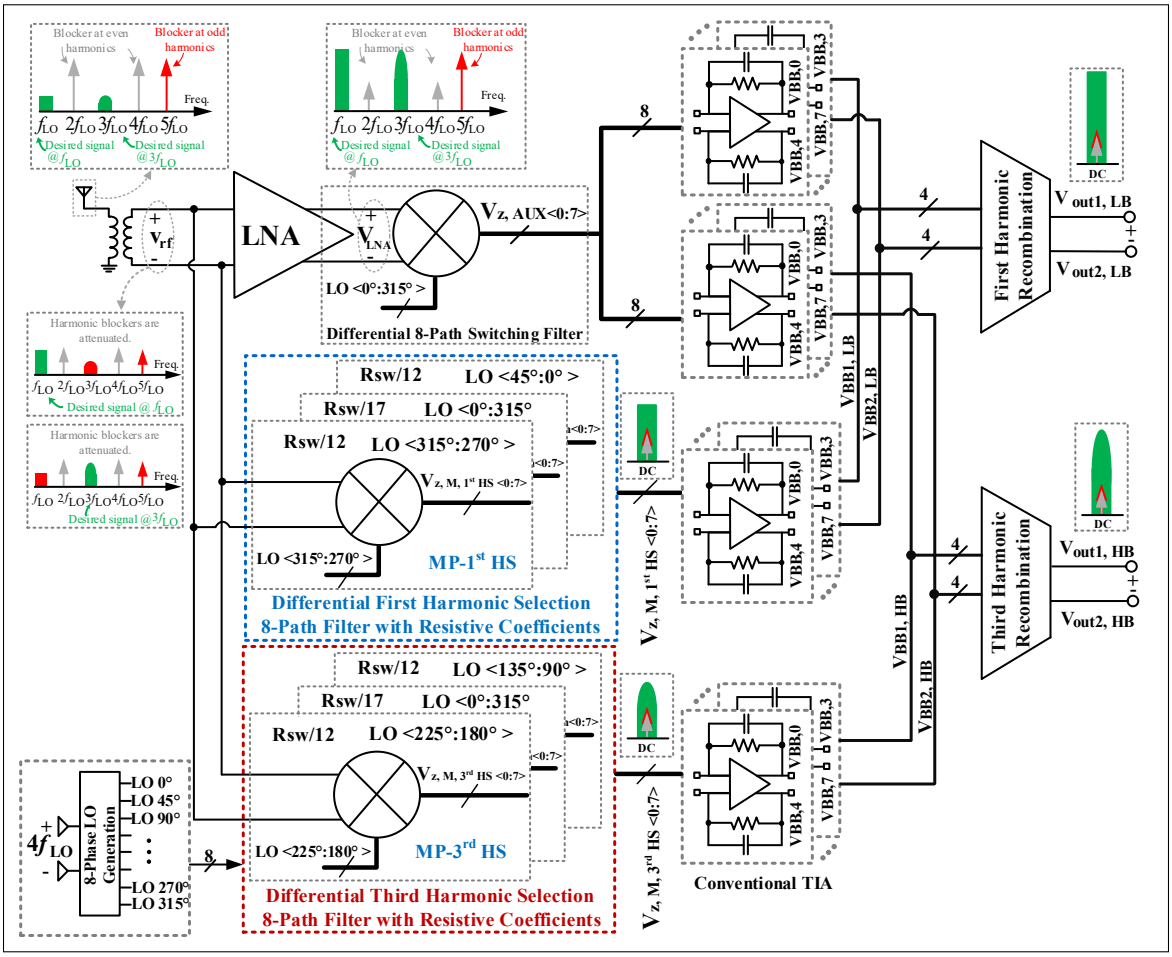

Figure 4.2 Block diagram of the proposed architecture of the HS-NC front-end RX2

and two 3^{rd} BB harmonic recombination blocks. This will be discussed in the measurement results.

4.3 Harmonic Selection Switching Filter Based on Resistive Coefficients

Harmonic blockers in a current-driven switching filter can generate large down-converted currents due to the square wave nature of the LO clocks. In a single-ended design, the BB output current from each switch of the switching filter is obtained by multiplying the RF current with a single clock pulse. Thus, signals around every LO harmonic generate currents that flow into the TIAs and saturate them. In a fully differential switching filter, since the differential switches'

outputs are connected together and the effective LO is a differential waveform, the even-order LO harmonic blocker currents are suppressed at the switching filter's output and do not flow into the TIAs. For this reason, a fully-differential architecture relaxes the requirements for blockers around the even-order LO harmonics.

To suppress blockers around odd-order LO harmonics, the differential RF transconductance amplifiers can be followed by a N-phase switching filter to improve small-signal harmonic rejection Forbes *et al.* (2013); Ru *et al.* (2009). The multiple mixing paths in parallel with the desired weighting ratio of $1 : \sqrt{2} : 1$ make the receiver experience no gain at frequencies around the LO harmonics, and thus blocker signals around the LO harmonics do not generate BB currents flowing into the TIAs. If no current flows into the TIAs, they cannot saturate and this improves the large-signal resilience of the receiver to harmonic blockers.

However, the weighting ratio implementation by the RF amplifiers increases the power consumption. The weighted RF amplifiers can be replaced with resistive attenuators, and the same HRR results can be achieved. Since the use of the resistive attenuators increases the NF, the weighted resistive coefficients network can be employed at the BB nearer to the output Ru *et al.* (2009) to realize the desired weighting ratio and to provide higher HRRs. However, the weighted resistive coefficients can be used at the earlier stages as well. If using resistive coefficients keeps the receiver's NF at an acceptable level, lower power consumption and higher linearity can be achieved.

It should be mentioned that the negative coefficients have no effect on the odd HRRs, and are only important to achieve even HRRs. Thus, half of the coefficients cannot be realized with resistors and the odd harmonics can be rejected by employing positive resistive coefficients, and the even harmonics can be rejected by using a differential architecture. As such, to analyse the harmonic selection N-path switching filter with resistive coefficients, the BB amplifier coefficients used such as in Xu *et al.* (2017) can be replaced with the BB resistive coefficients.

Fig. 4.3 shows the resistive HR N-path switching filter where $R_{sw,r}$ is a reference switching resistance and is equal to $1/A_c$. In this architecture, the resistive coefficients, $R_{SW,i}$, are expressed

by

$$R_{SW,i} = \frac{1}{C(i)}, \tag{4.1}$$

where $C(i) = c_i A_{Gm}(i)$, and c_i is equal to 0 for $A_{Gm}(i) \geq 0$, and is equal to 1 for $A_{Gm}(i) < 0$. If $C(i) = 0$ then $R_{SW,i}$ must be infinite, and the corresponding path is eliminated. Note that the voltage gain of each corresponding amplifier, $A_{G_m}(i)$, is defined as Shams & Nabki (2022)

$$A_{Gm}(i) = A_c cos(\rho i \frac{2\pi}{N} + \varphi_0), i = (0, 2, ..., N-1). \tag{4.2}$$

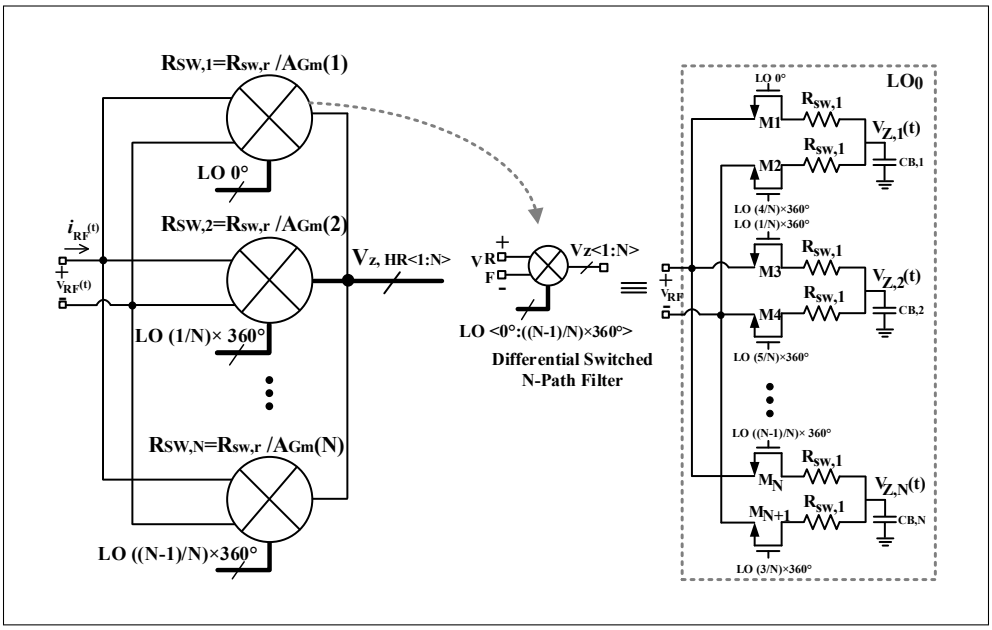

Figure 4.3 Differential harmonic rejection switching system with resistive coefficients

The resistive coefficients of the HR N-path switching filter can be calculated with

$$R_{SW,i} = \frac{R_{sw,r}}{A_0 cos(\rho i \frac{2\pi}{N} + \varphi_0)}, \tag{4.3}$$

where $0 \leq \rho < N, \rho \in \mathbb{Z}$ and $R_{sw,r}$ is a reference switching resistance. For the first path, the BB voltage, $V_{Z,HR,1}(\omega)$, is given by

$$V_{Z,HR,1}(\omega) = \frac{1}{2\pi}\left[\sum_{i=0}^{N-1} C(i)SW_i * V_{RF}(\omega)\right] \times Z_{BB,i}(\omega), \tag{4.4}$$

$$\begin{aligned} V_{Z,HR,1}(\omega) = \sum_{i=0}^{N-1}\sum_{n=-\infty}^{\infty} a_n c(i) A_c sin(\rho i \frac{2\pi}{N} + \varphi_0) e^{-jin\frac{2\pi}{N}} \\ \times V_{RF}(\omega - n\omega_{LO}) Z_{BB,1}(\omega), \end{aligned} \tag{4.5}$$

where N and ρ are an even and an odd number, respectively. Thus, (4.5) can be extended as follows

$$\begin{aligned} V_{Z,HR,1}(\omega) = \frac{1}{2}A_c[\sum_{i=0}^{N-1}\sum_{n=-\infty}^{\infty} c(i)a_n e^{j\varphi_0} e^{-ji(n-\rho)\frac{2\pi}{N}} \\ \times V_{RF}(\omega - n\omega_{LO}) + \sum_{i=0}^{N-1}\sum_{n=-\infty}^{\infty} c(i)a_n e^{j\varphi_0} e^{-ji(n+\rho)\frac{2\pi}{N}} \\ \times V_{RF}(\omega - n\omega_{LO})] Z_{BB,1}(\omega)). \end{aligned} \tag{4.6}$$

$V_{Z,HR,1}(\omega)$ in (4.6) has a non-zero value for $n = kN \pm \rho$. Note that there may be charge sharing between the BB capacitors due to lack of complete isolation, and thus the voltage gain can be lower than that predicted by (4.6). As mentioned above, half of the coefficients are equal to zero, thus (4.6) can be given by

$$\begin{aligned} V_{Z,HR,1}(\omega) = \frac{1}{4}NA_c Z_{BB,1}(\omega)) \\ \left[\sum_{k=0}^{\infty} a_{kN\pm\rho} \times |V_{RF}(\omega - (kN \pm \rho)\omega_{LO})|\right]. \end{aligned} \tag{4.7}$$

According to (4.7), all odd harmonics ($n = 2m + \rho$ and $2m \neq \rho N$ where m is an arbitrary integer number and ρ is an odd number) will be rejected at the BB nodes, except the $(kN \pm \rho)^{th}$ harmonics.

A small value of $R_{sw,r}$ results in charge sharing between the BB capacitors and degrades HRRs and the signal to noise ratio. However, a large value of $R_{sw,r}$ increases the thermal noise. Thus, there is a trade-off between the HRR and the noise performance.

Due to a lack of complete isolation between the paths, a limited rejection is achieved at the input node of the harmonic selection N-path switching filter where the harmonic blockers can be present. The maximum achievable HRR depends on the source resistance (R_s) and the total resistance seen from the input port. The input equivalent resistance of a conventional N-path filter is equal to the switch on-resistance. However, the resistive HS-NPF shown in Fig. 4.3 can be modeled by the equivalent circuit depicted in Fig. 4.4. The input resistance can be expressed by

$$R_{IN_{HR,filter}} = R_{sw,1}||R_{sw,2}...||R_{sw,N}. \tag{4.8}$$

$$R_{IN_{HR,filter}} = \frac{2}{\sum_{i=1}^{N} |A_{Gm}(i))|} = \frac{2R_{sw,r}}{\sum_{i=1}^{N} \left|cos(\rho i \frac{2\pi}{N} + \varphi_0)\right|}. \tag{4.9}$$

For frequencies further away from the LO frequency (f_{LO}), the HS-NPF output can be approximated ($V_{out}(\omega)$) by

$$V_{out}(\omega) = \frac{2R_{sw,r}}{2R_{sw,r} + R_S \sum_{i=1}^{N} \left|cos(\rho i \frac{2\pi}{N} + \varphi_0)\right|} V_{RF}(\omega). \tag{4.10}$$

Thus, the maximum rejection at the input port of the HS-NPF with resistive coefficients inversely depends on the source impedance (R_S). The overall NF can be decreased by increasing the the source impedance. Accordingly, if another stage is placed before the HS-NPF system and provides a 50 Ω matching impedance, a larger source resistance can be employed to increase the maximum rejection at the input port of the HS-NPF system, and to reduce the overall NF.

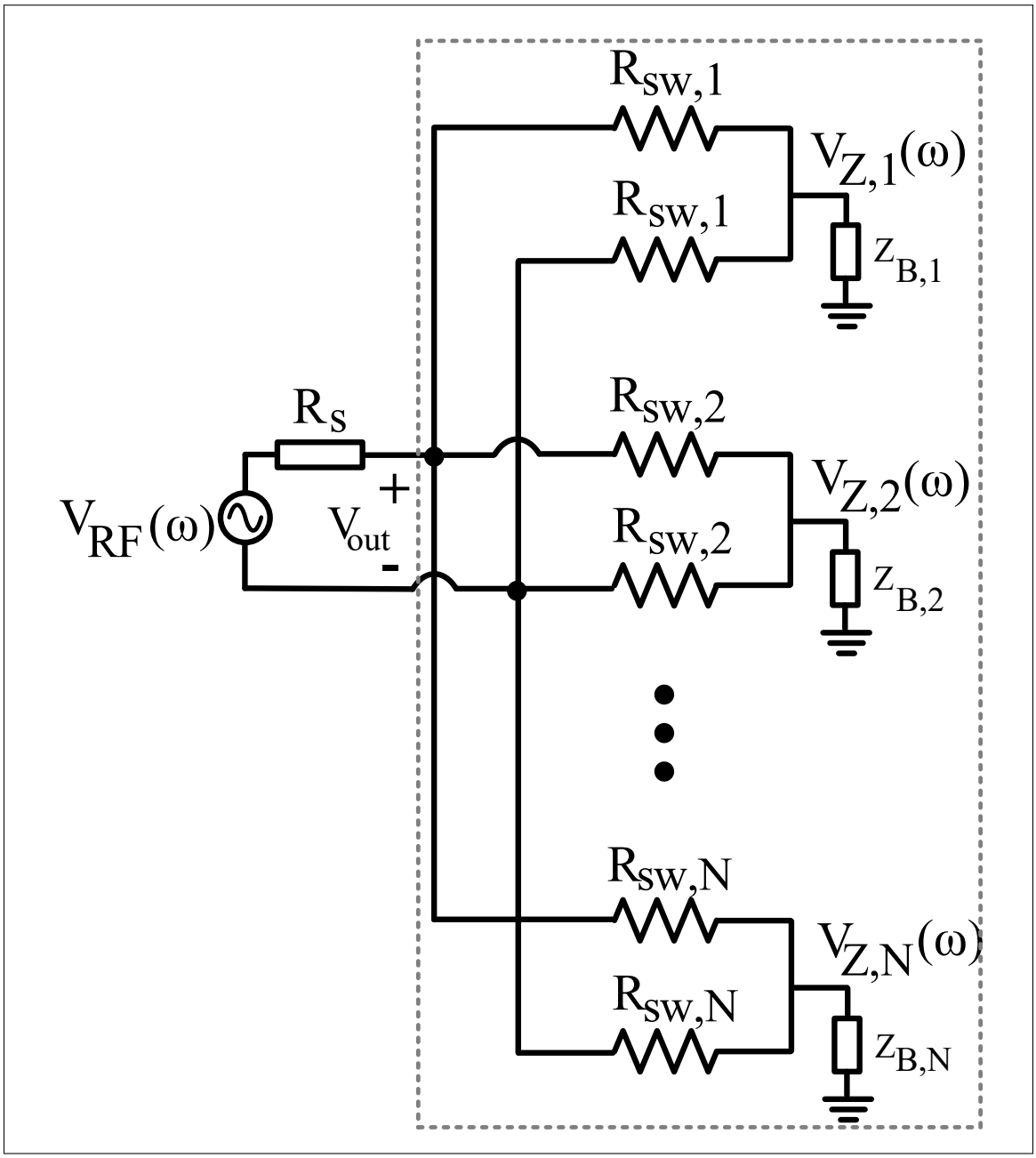

Figure 4.4 The equivalent input impedance seen from the input port of the resistive HS-NPF at any specific time

4.4 Circuit Implementation

The schematics of the building blocks composing the proposed receivers are shown in Fig. 4.5.A differential wideband LNA, differential feed forward 8-path switching filter, 1^{st} and 3^{rd} HS-NPFs, BB 1^{st} and 3^{rd} harmonic recombination blocks, and TIA are detailed below.

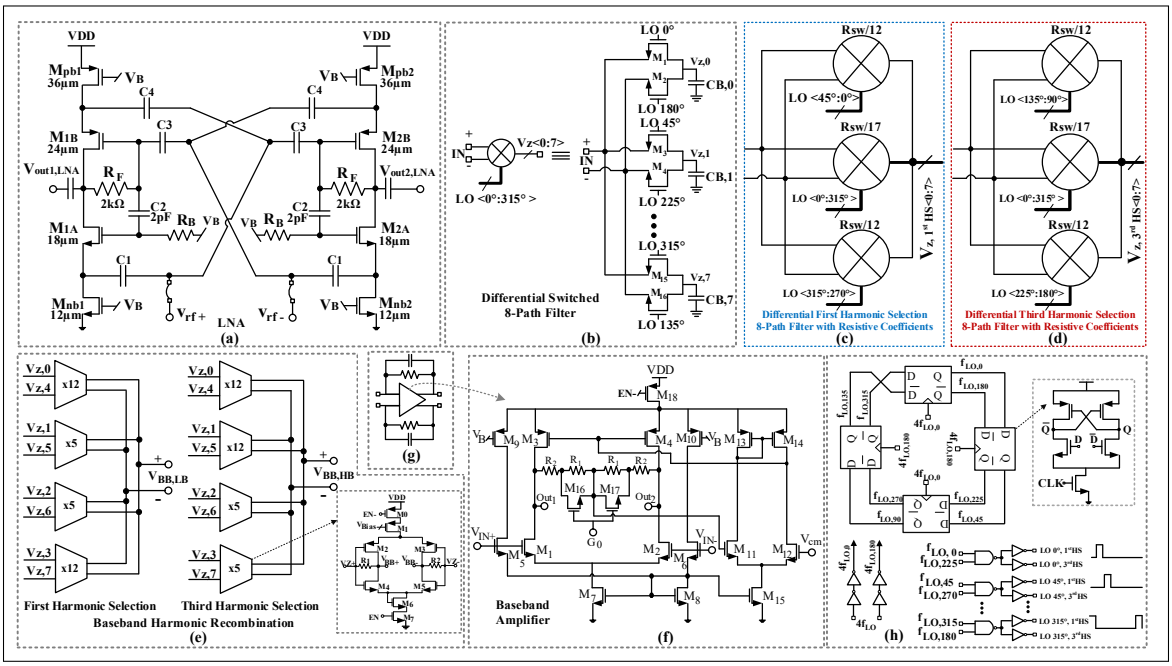

Figure 4.5 Transistor level implementation of the proposed receiver: (a) differential wideband LNA, (b) Differential switched 8-path filter, (c) differential first harmonic selection 8-path filter with resistive coefficients, (d) differential third harmonic selection 8-path filter with resistive coefficients, (e) first and third harmonic selection circuits for BB harmonic recombination, (f) BB amplifier, and (g) multi-phase LO generator

4.4.1 Differential wideband LNA

The LNA architecture used in the RF receivers is depicted in Fig. 4.5(a). The core of the LNA consists of the combination of common gate (CG), common source (CS), current reuse, and capacitive cross coupling (CCC) topologies. The main transistors M_{1A}/M_{1B} in one branch are cross connected with M_{2A}/M_{2B} in the other branch to construct a CCC-CG topology. The ef-

fective g_m can thus be doubled Belmas *et al.* (2012); Shams *et al.* (2020). Transistors M_{1A}/M_{1B} (M_{2A} and M_{2B} in other branch) implement a push-pull structure, increasing the effective g_m without added power consumption. The shunt feedback resistor, R_F, provides the input impedance matching.

The LNA used in Shams *et al.* (2020) uses two center-tapped inductors to resonate with parasitic capacitances and provide the bias current path. However in this work, the current sources of M_{nb1}/M_{pb1} and M_{nb2}/M_{pb2} are used to provide a high resistance for AC signals. This avoids the need for biasing using on-chip inductors, saving on die area. Independent bias branches are applied to M_{1A}/M_{1B} (M_{2A} and M_{2B}) in this LNA. In this fashion, the size and bias of these transistors can be flexibly adjusted to enhance performance. Moreover, the high output impedance of the LNA helps to achieve proper operation of the N-path switching filter, as it affects blocker suppression. In addition, the output noise of M_{1A}/M_{1B} (M_{2A} and M_{2B}) is partially cancelled by using the cross coupled topology. The total noise factor can be expressed as

$$\begin{aligned} F \approx 1 + \frac{\gamma}{2(g_{m_{M_A}} + g_{m_{M_B}})R_s} + \frac{2R_s}{R_F} \times \\ \left(1 + \frac{r_{o_{M_A}} || r_{o_{M_B}}}{r_{o_{M_A}} || r_{o_{M_B}} + R_F}\right)^2 + \frac{R_s}{2} \times (\gamma_n g_{m_{nb}} + \gamma_p g_{m_{pb}}), \end{aligned} \tag{4.11}$$

where γ, R_s, R_F, $g_{m_{M_A}}$, $g_{m_{M_B}}$, $g_{m_{nb}}$, and $g_{m_{pb}}$ represent the channel length modulation, the source resistance, shunt feedback resistance, $g_{m_{M_{1A}}} + g_{m_{M_{2A}}}$, $g_{m_{M_{1B}}} + g_{m_{M_{2B}}}$, $g_{m_{M_{nb1}}} + g_{m_{M_{nb2}}}$, and $g_{m_{M_{pb1}}} + g_{m_{M_{pb2}}}$, respectively. The second term is due to M_{1A}/M_{1B} and M_{2A}/M_{2B}, while the third term is the noise contributed by the feedback resistance, R_F. The last term is due to the current sources composed of M_{nb1}/M_{pb1} and M_{nb2}/M_{pb2}, indicating that $g_{m_{nb}}$ and $g_{m_{pb}}$ should be minimized.

The post-layout simulated results of the inductorless LNA, as plotted in Fig. 4.6, show a voltage gain of more than 20 dB, NF of less than 4.6 dB, and S11 of below −10 dB over the entire desired frequency band of 0.5 −7.2 GHz, while consuming 1.3 mA from a 1.2-V supply. Note

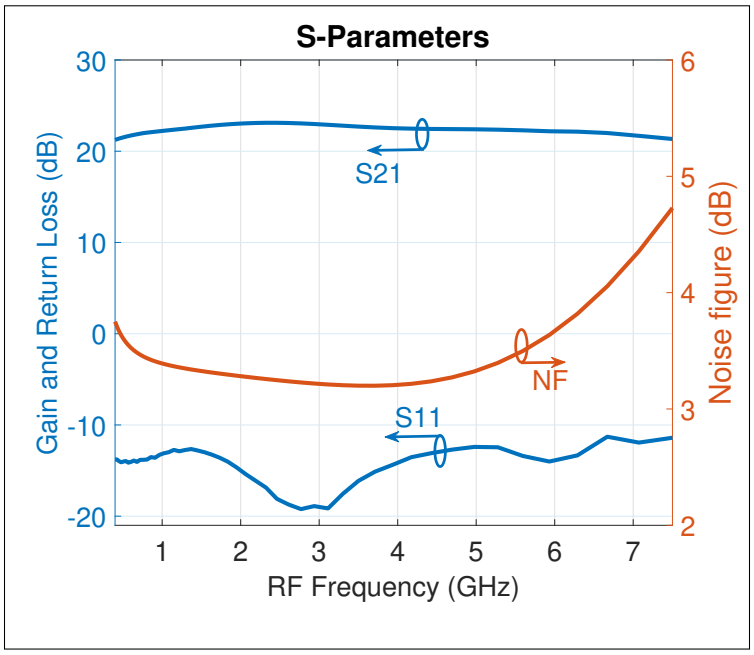

Figure 4.6 The LNA post-layout simulated gain (S21), return loss (S11) and NF

that the input impedance matching of the HS-NC receiver is achieved by up-converting the input impedance of the BB harmonic recombination cells in the main path, and the LNA's input impedance in the auxiliary path.

4.4.2 Differential down-conversion paths

The proposed HS-NC receiver front-ends employ one differential feed-forward 8-path filter in the auxiliary path (see Fig. 4.5(b)), and two resistive 1^{st} and 3^{rd} HS-NPFs in the auxiliary paths, shown in see Fig. 4.5(c) and (d), respectively. In the switching filter, all switches are realized by equally sized NMOS devices to mitigate charge injection and clock feed-through.

In the LB frequency range, the first harmonic of f_{LO} ($\rho = 1$) is selected by employing a 1^{st} HS-NPF, while in the HB frequency range, the 3^{rd} harmonic of f_{LO} ($\rho = 3$) is selected by using a 3^{rd} HS-NPF. In addition, the signals are down-converted to an 8-phase BB signal. The resistive coefficients ($R_{SW,i}$) are calculated with (4.3). Thus, resistive coefficients of [$R_{SW,0}$,

$R_{SW,1}$, $R_{SW,3}$,..., $R_{SW,7}$] are equal to [$R_{sw,r}$, $R_{sw,r}/cos(\frac{\pi}{4})$, ∞, $R_{sw,r}/cos(\frac{3\pi}{4})$, $R_{sw,r}/cos(\pi)$, $R_{sw,r}/cos(\frac{5\pi}{4})$, ∞, $R_{sw,r}/cos(\frac{7\pi}{4})$] when φ_0, N and ρ are equal to zero, 8 and 1, respectively. To select the 3^{rd} LO harmonic ($\rho = 3$), the resistive coefficients of the 8-path switching filter are equal to [$R_{sw,r}$, $R_{sw,r}/cos(\frac{3\pi}{4})$, ∞, $R_{sw,r}/cos(\frac{9\pi}{4})$, $R_{sw,r}/cos(3\pi)$, $R_{sw,r}/cos(\frac{15\pi}{4})$, ∞, $R_{sw,r}/cos(\frac{21\pi}{4})$]. Note that there are only two different resistive values, including $R_{sw,r}$ and $R_{sw,r}/0.7071$. The resistive coefficients are realized by the NMOS transistor switches to reduce the total capacitance seen by the clock generator and chip area. Moreover, this reduces the dynamic power consumption of the LO clock generator. Since the switch resistance is given by

$$R_{SW} = \frac{1}{\mu_n C_{ox} \frac{W}{L}(V_{GS} - V_{TH})}. \tag{4.12}$$

The resistive coefficients can be realized by changing either the W/L ratio or the number of unit transistors. To provide best transistor matching, two resistive coefficients of $R_{sw,r}$ and $R_{sw,r}/0.7071$ are realized by duplicating 17 and 12 unit transistors, respectively. Thus, the harmonic selection 8-path switching systems consist of three differential 8-path filters with coefficients of 12 : 17 : 12. More importantly, the two filters with resistive coefficient of $R_{sw,r}/12$ have a phase difference with respect to the resistive coefficient of $R_{sw,r}/17$ of 45° and 315° in the 1^{st} HS-NPF, and a phase difference of 135° and 225° in the 3^{rd} HS-NPF (see Fig. 4.5(c) and (d)).

Since both conventional 8-path switching and HS-NPFs employ a differential architecture, the effective LO is a differential waveform. Thus, when the differential switches' outputs are connected together, the even-order harmonic blocker currents are suppressed at the switching filter's output, and do not flow into the BB harmonic recombination circuits. Fig. 4.7 illustrates the frequency response of the differential 1^{st} and 3^{rd} harmonic selection 8-path filters at the LO frequency of 2 GHz. Therefore, the proposed differential receivers are resilient to even-order harmonic blockers. Moreover, the leakage from the LO to the RF input is reduced.

4.4.3 Analog baseband circuits

RX1 and RX2 differ in their treatment of the BB signals. In RX1, the BB down-converted outputs in the main and auxiliary paths are differentially connected to the BB 1^{st} and 3^{rd} harmonic recombination circuits that combine $V_{Z,M,1^{st}HS,<0:7>}$, $V_{Z,M,3^{rd}HS,<0:7>}$ and $V_{Z,AUX,<0:7>}$ with the sinusoidal weighted coefficients at the selected harmonic (see Fig. 4.1). The BB harmonic recombination blocks, shown in Fig. 4.5(e), employ four weighted G_m cells to equivalently generate a sine LO signal. The voltage gain of each corresponding amplifier is achieved by

$$A_{Gm}(i) = A_c sin(\rho i \frac{2\pi}{N} + \varphi_0), i = (0, 2, ..., 7). \tag{4.13}$$

To select the 1^{st}-order harmonic of f_{LO} ($\rho = 1$), the BB 1^{st} harmonic recombination block employs four G_m cells with weighting ratios of 12:5:5:12 to equivalently generate a sine LO signal. In contrast, for the 3^{rd} harmonic recombination block, weighting ratios of 12:12:5:5 are used and the outputs of the four weighted G_m cells are reconfigured to select the 3^{rd}-order LO harmonic (($\rho = 3$)). This results in an approximation of $A_c \times sin(3(2\pi f_{LO})t + \varphi_0)$, where A_c and φ_0 are a constant amplitude and an initial phase, respectively.

The weighted outputs of the harmonic recombination blocks in the main and auxiliary paths are summed in the BB amplifier. The BB amplifier provides the desired magnitude and phase shift between the two paths to achieve optimum noise canceling, in addition to signal recombination. The circuit diagram of the implemented biased BB amplifier is shown in Fig. 4.5(f). The differential pair of M_1-M_4 is biased through M_5-M_{10}. For a larger input signal, the bias current of the main differential pair is increased by transistors of M_5 and M_6. A common-mode feedback created by M_{11}-M_{14} is employed to keep the outputs of the differential amplifier at the desired common-mode voltage. For both LB and HB frequency paths, the used BB amplifiers are designed with the same configuration with a bias current of $650\mu A$.

As discussed in Section 4.2, RX2 employs a bank of conventional TIAs placed after the conventional 8-path filter, $1^{st}HS - NPF$ and $3^{rd}HS - NPF$ (i.e., in the three paths). The BB TIAs

are differentially fed with the down-converted signals of $V_{Z,M,1^{st}HS,<0:7>}$, $V_{Z,M,3^{rd}HS,<0:7>}$ and $V_{Z,AUX,<0:7>}$. The desired signals in the main paths are filtered and amplified by the bank of differential TIAs. The TIAs consist of a fully differential BB amplifier along with feedback resistors and capacitors, as shown in Fig. 4.5(g). The BB capacitors of $C_{B,<0:7>}$ in the three paths and feedback components in the TIAs set RX2's bandwidth. Note that when the receiver operates in the LB frequency range, the G_m unit cells and BB amplifiers used in the HB path are powered-down and vise versa.

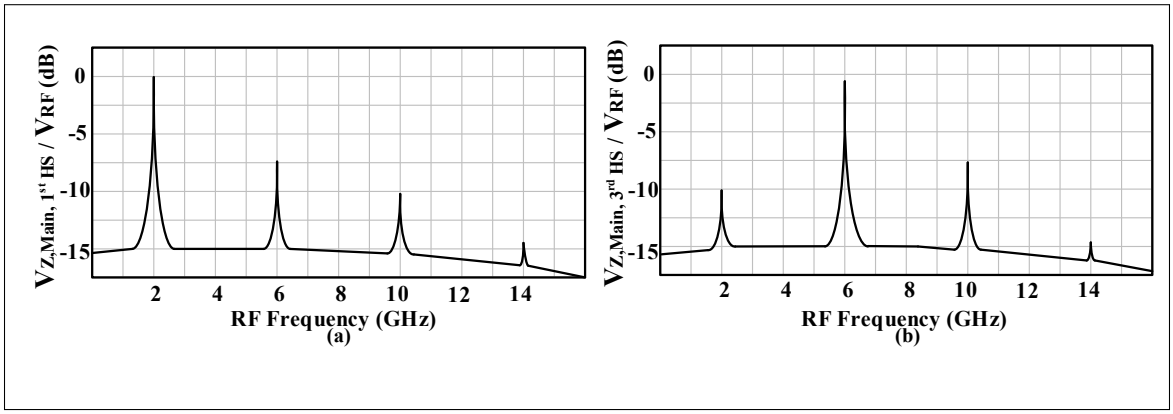

Figure 4.7 Frequency response of the (a) differential 1^{st} harmonic selection 8-path filter, and (b) differential 3^{rd} harmonic selection 8-path filter at a 2 GHz LO frequency

4.4.4 Multi-phase LO generator

Both receivers rely on eight LO phases with 12.5 % duty-cycle non-overlapped LO clocks to perform harmonic blocker rejection and down-conversion. All switches used in the conventional 8-path filter, 1^{st} and 3^{rd} HS-NPFs are driven by 8-phase LO clocks. The clock generator shown in Fig. 4.5(h) consists of four latches forming a ring counter to generate eight phases with 50 % duty cycle at the f_{LO}. To convert the clocks from a 50 % to a 12.5 % duty cycle, and to ensure non-overlapping clocks, the ring flip-flop based divider is followed by AND gates and these eight clocks are AND'ed together. For an 8-phase LO clock, the LO input signal operates at four times f_{LO}. Note that to support an RF of 7.2 GHz, the f_{LO} is of 7.2 GHz, and the 8-phase clock generator requires an input signal operating at 28.8 GHz, which is not readily achievable.

The proposed architectures aims to mitigate this issue by relaxing the frequency requirement of the 8-path filters and HS-NPFs, thanks to the higher order LO harmonic selection when operating in the HB frequency range.

The divider can operate at up to 2.4 GHz in 65 nm CMOS, and its operating frequency is limited by the capacitive load of the conventional 8-path filter, 1^{st} and 3^{rd} HS-NPFs. At 0.5 GHz, it draws 2.1 mW. The power dissipation rises to 8.4 mW at 2.4 GHz. Moreover, for 4 GHz and 8 GHz input signals ($f_{LO} = 4\ GHz/4 = 1\ GHz$ or $f_{LO} = 8\ GHz/4 = 2\ GHz$), the 8-phase LO generator exhibits a post-layout simulated phase noise of less than -156.7 dBc/Hz and -152.4 dBc/Hz, respectively, at an 80 MHz offset (see Fig. 4.8). The phase noise is low because the latches are driven with an off-chip master clock ranging from 2 GHz to 9.6 GHz.

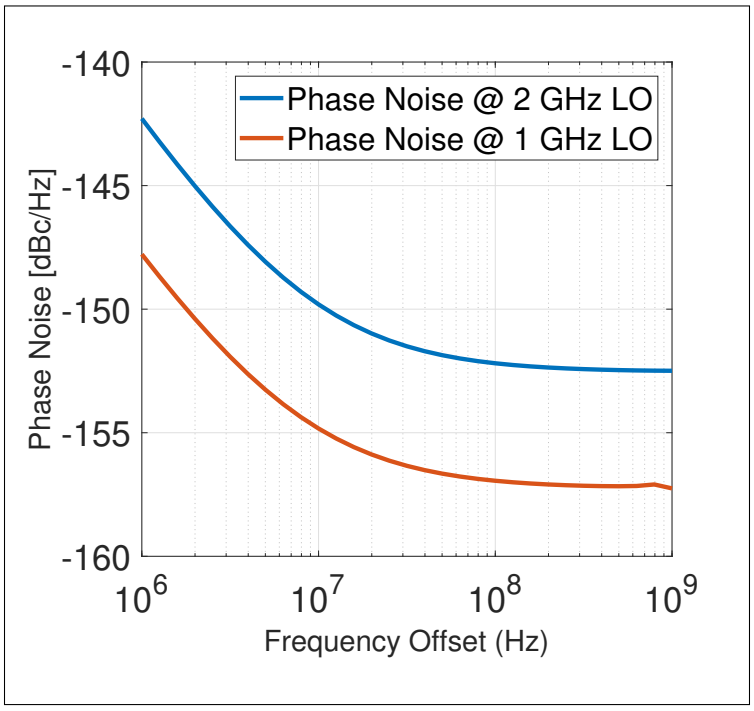

Figure 4.8 The post-layout simulation of the output phase noise of the 8-phase LO signal generator as a function of the frequency offset

4.5 Measurement Results

The proposed receivers were designed and fabricated in TSMC 65 nm CMOS technology for an operating frequency of 0.5 −7.2 GHz. The chip micrograph is shown in Fig. 4.9. The total area including pads is 1.25 mm × 1.44 mm, and the active area is 0.93 mm^2, where 1/3 of the active chip area is occupied by the MIM capacitors. The chip is packaged in a 48-pin QFN and mounted on a four-layer Rogers 4003C PCB. Since the RF inputs and 8-phase clock generator of both receivers are differential, two wideband RF baluns (MABA-011108) are used to provide the differential input signals for the receiver from the single-ended 50 Ω signal generator to facilitate single-ended measurements (e.g. IIP3 and NF). It should be mentioned that the on-chip 8-phase clock generator requires a master clock operating at four times of f_{LO} and that is applied off-chip. Thus, a SMW200A vector signal generator, is employed to generate the required input to drive the LO clock generator. As discussed in Section 4.2, each receiver supports low and high frequency bands. Over the LB frequency range (0.5 −2.4 GHz), the first harmonic of the 8-path switching filter response is selected at the BB frequency, while over the HB frequency range (2.4 −7.2 GHz), the third harmonic of f_{LO} ($f_{RF} = 3f_{LO}$) is selected. Over both LB and HB frequency ranges, the LO generator master clock varies from 2 −9.6 GHz ($4f_{LO}$, where f_{LO} ranges from 0.5 −2.4 GHz).

RX1 and RX2 consume 12.4 mW and 9 mW, respectively, from a 1.2-V power supply, excluding the buffers. The LO generation block consumes 2.1 −8.4 mW depending on the operating frequency. Output buffers were used to drive the testing equipment, and they each consume 14.4 mW from a 1.2-V supply.

The input return loss (S11) of both RX1 and RX2 were measured by employing a network analyzer (Keysight PNA N5225A) and are plotted in Fig. 4.10. These are below −10 dB within the desired frequency band, spanning from 0.5 to 7.2 GHz.

The conversion gain, NF, HRR, in-band and OOB IIP3 were measured over the LB and HB frequency ranges of both RX1 and RX2.

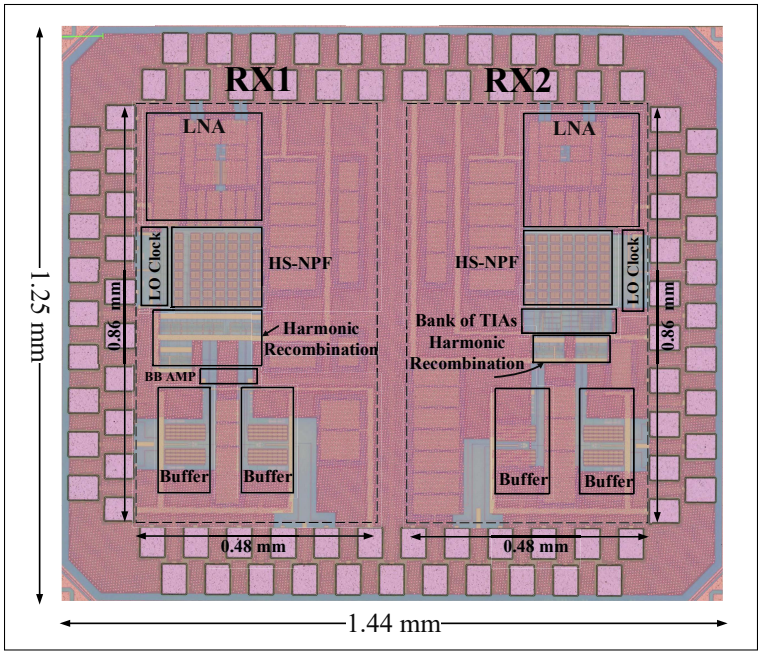

Figure 4.9 Chip micrograph of RX1 and RX2, occupying an active area of 0.88 mm × 1.085 mm in 65 nm CMOS

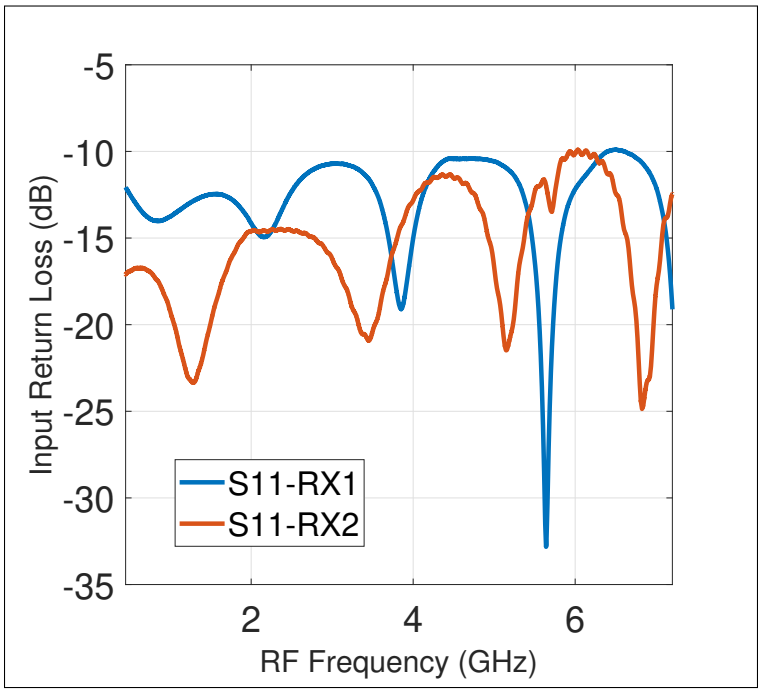

Figure 4.10 Measured input return loss (S11) of RX1 and RX2

4.5.1 Performance of RX1

The conversion (RF-to-BB) gain and DSB NF of RX1 were measured by using An Agilent N9030A PXA signal analyzer and a 346B noise source. It is plotted in Fig. 4.11(a) over an RF input frequency ranging from 0.5 to 7.2 GHz, covering both LB and HB frequency ranges. This demonstrates the wide RF operation bandwidth achieved. The measured conversion gain from the balun input to the differential outputs of the receiver, with BB frequency fixed at 80 MHz, is well above 42 dB, varying from 45.6 −48 dB over the LB frequency range, and 42 −46.2 dB over the HB frequency range.

As seen in Fig. 4.11(a), over the LB frequency range, the NF varied from 3.4 dB to 4.1 dB. NF in the HB frequency range is 3.7 −4.3 dB from 2.4 to 7.2 GHz. The NF at the higher frequencies is higher due to the LO leakage to the receiver input, and results in a DC offset in the BB. This offset leads to an imbalance between the gain experienced in the four BB G_m cells used in the harmonic recombination block. Thus, more noise is folded from the higher LO harmonics onto the desired BB signal. This could be mitigated by employing a BB DC offset cancellation technique to lower the NF at higher frequencies.

Moreover, conversion gain and NF are plotted in Fig. 4.11(b) as a function of the BB frequency for both the LB and HB frequency ranges at an RF frequency of 2 GHz and 6 GHz, respectively. Note that the LO frequency is set at 2 GHz in both cases. A flat NF of 3.7 dB and 4.2 dB is achieved over the LB and HB frequency ranges, respectively, for a BB frequency ranging from 10 MHz to 100 MHz. RX1 achieves a 3 dB BW of the 63 MHz and 97 MHz at the input RF frequency of 2 GHz (LB path) and 6 GHz (HB path), respectively.

RX1 harmonic rejection tests were conducted over LO frequencies from 0.5 GHz to 2.4 GHz as the fourth and fifth LO harmonics can potentially fall into the desired bands. The HRR vs. LO frequency is measured and plotted in Fig. 4.11(c) and (d) for the LB and HB frequency ranges, respectively, at an 80 MHz BB frequency. To measure the HRR, a −30 dBm input signal was applied to the receiver at a small frequency offset from the desired down-conversion frequency (f_{LO}) to measure the RF-to-BB gain of the desired band. For all integer harmonics of f_{LO}

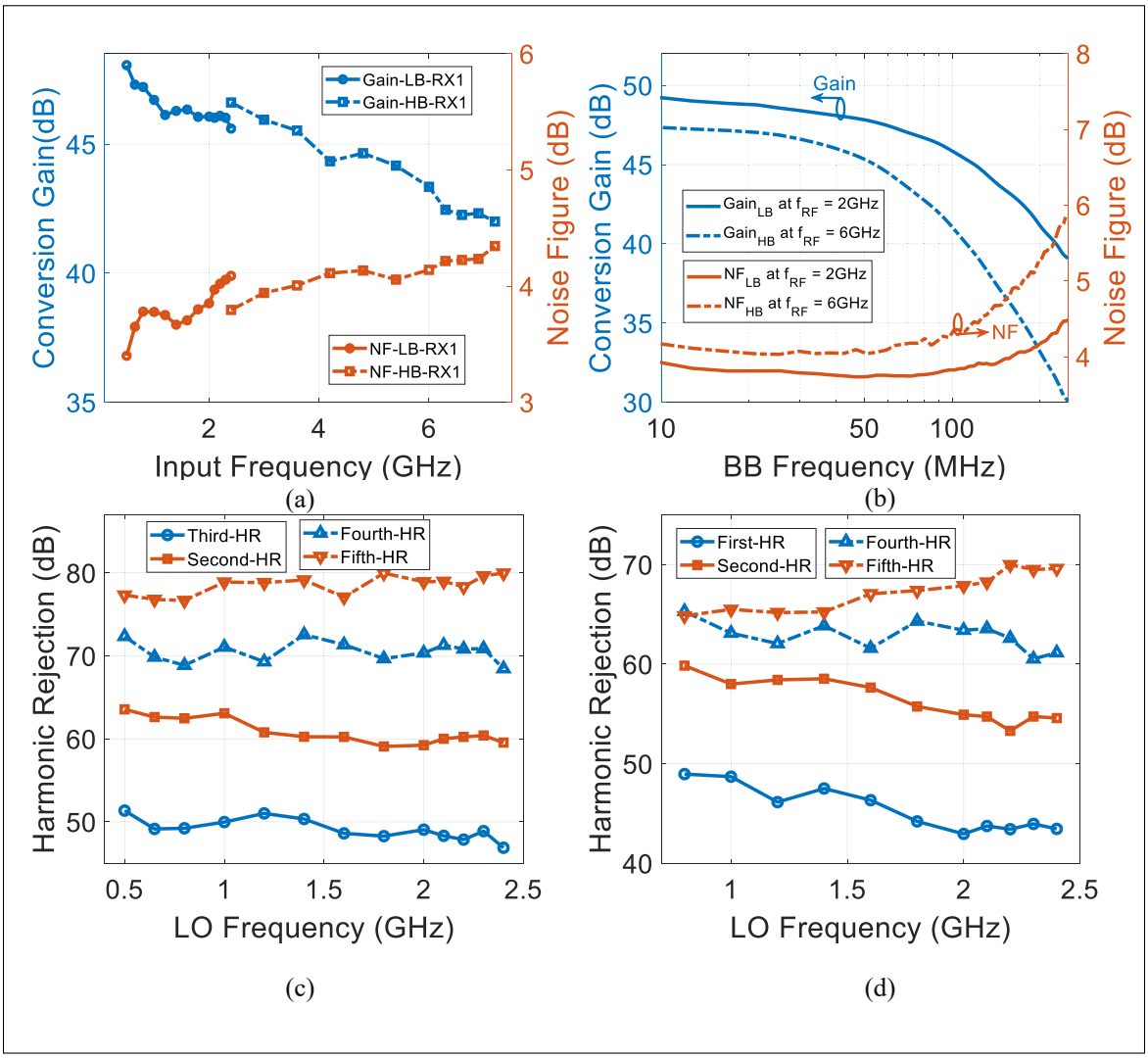

Figure 4.11 Measured performance of RX2 implemented in 65 nm CMOS: (a) Conversion gain and NF vs. input frequency (LO frequency is 0.5 –2.4 GHz) at an 80 MHz BB frequency, (b) conversion gain and NF for a f_{LO} = 2 GHz (f_{RF}=2 GHz and 6 GHz for the LB and HB frequency ranges, respectively) vs. the baseband frequency, (c) 3^{rd}, 2^{nd}, 4^{th}, and 5^{th} HRRs vs. LO frequency for the LB frequency range, and (d) 1^{st}, 2^{nd}, 4^{th}, and 5^{th} HRRs vs. LO frequency for the HB frequency range

$(2f_{LO}, ..., 5f_{LO})$, the same input power was applied to the receiver's input, which should be rejected. The HRR is achieved by dividing the gain at the LO harmonic frequencies by the conversion gain of the desired frequency signal. The measured 3^{rd} and 1^{st} HRRs are higher than 47 dB and 44 dB for both the LB and HB frequency ranges, respectively. Moreover, Fig. 4.11(c)

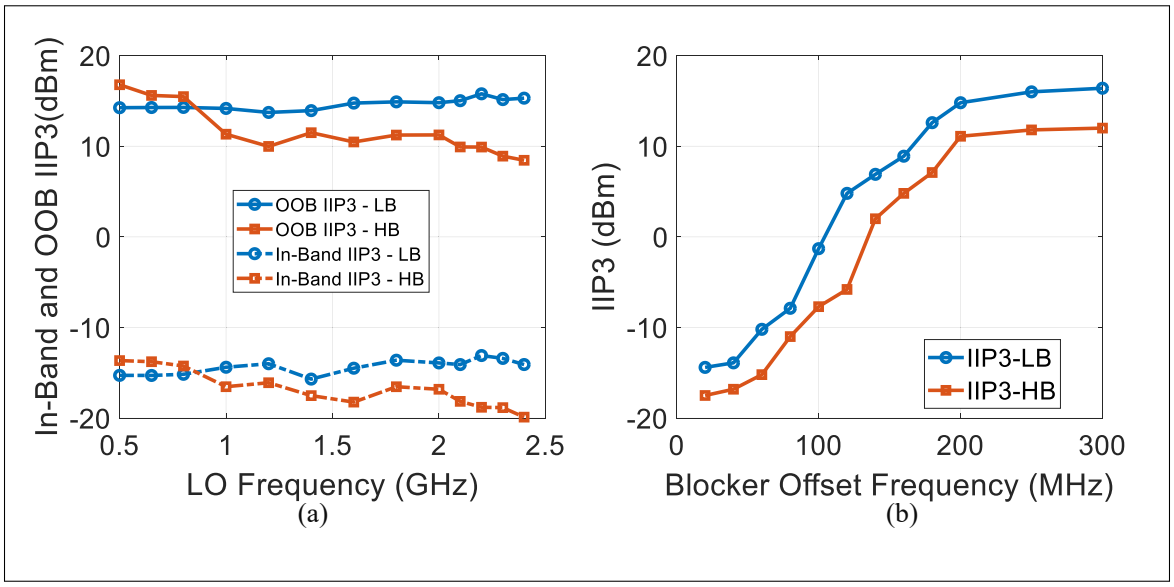

Figure 4.12 Measured RX1 (a) OOB and in-band IIP3 vs. LO frequency, and (b) IIP3 vs. blocker offset frequency

and (d) show the rejection ratio of the 2^{nd}, 4^{th}, and 5^{th} LO harmonics, with rejection in excess of 54 dB for both frequency ranges. As the LO harmonic frequencies lay beyond the range of the LNA amplification, higher HRRs are achieved.

The measurement of the linearity of RX1 is plotted in Fig. 4.12. The IIP3 is achieved by applying two equal-amplitude tones at $[f_{RF}+\Delta f, f_{RF}+2\Delta f-1\ MHz]$. In-band and OOB IIP3 were measured as a function of LO frequency at a frequency offset of 40 MHz and 200 MHz, respectively, and plotted in Fig. 4.12(a). The in-band IIP3 was measured to be better than -15.6 dBm and -19.8 dBm for the LB and HB frequency ranges, respectively. Moreover, the OOB IIP3 was relatively constant at 15 dBm for the LB frequency range, and goes from 16.7 dBm to 9.2 dBm for the HB frequency range. Compared to the in-band IIP3, the OOB IIP3 is significantly enhanced because the linearity of the BB amplifiers dominates the in-band IIP3. To further evaluate the linearity performance, the IIP3 of the LB and HB frequency ranges was measured as a function of Δf, the offset frequency from the RF input signal, at a 2 GHz LO frequency, and is shown in Fig. 4.12(b). Note that the OOB linearity is limited by distortion originating from a non-zero

voltage swing at the output of the auxiliary path, while the degradation at in-band frequencies is due to the non-linearity of the BB circuits.

4.5.2 Performance of RX2

RX2 was characterized in a similar fashion as to RX1. For the LB and HB frequency ranges, Fig. 4.13(a) shows the measured conversion gain and NF as a function of the RF input frequency at a 80 MHz BB frequency. RX2 achieves a conversion gain gain higher than 39 dB/36 dB at the LB and HB frequency ranges, respectively. The measured DSB NF ranges from 3.9 to 4.6 dB over the LB frequency range and from 4.3 to 4.8 dB over the HB frequency range. The receiver NF is less than 4.8 dB across the entire band, thanks to the auxiliary path in the noise-cancelling architecture. Fig. 4.13(b) depicts the measured conversion gain and NF vs. the BB frequency. The NF is of 4.1 dB at 2 GHz in the LB frequency range, and 4.6 dB at 6 GHz in the HB frequency range. RX2 achieves a BB BW of 88 MHz and 103 MHz at the input RF frequency of 2 GHz (LB path) and 6 GHz (HB path), respectively.

Fig. 4.13(c) and (d) illustrate the measured HRRs vs. LO frequency of RX2 for both the LB and HB frequency ranges, respectively. Without RF filtering and calibration, RX2 provides 2^{nd}, 3^{rd}, 4^{th}, and 5^{th} order HRRs that are higher than 50 dB, 42 dB, 63 dB, and 72 dB, respectively, at a 80 MHz BB frequency. For the HB frequency range, the minimum 1^{st} and 2^{nd} order HR are 37 dB and 46.6 dB, respectively, while the 4^{th} and 5^{th} HRRs are higher than 57 dB.

The in-band IIP3 of RX2 is measured by injecting a two-tone input spaced at 40 MHz and 79 MHz offsets from f_{RF}. The OOB IIP3 is measured with an offset of 200 MHz and spacing of 399 MHz for the −30 dBm two-tone input. The measured in-band and OOB linearity performance of RX2 vs. LO frequency are plotted in Fig. 4.14(a). The measured LB in-band IIP3 is −18.3 dBm at a 2 GHz RF, and the HB in-band IIP3 is −21.6 dBm at a 6 GHz RF. The OOB IIP3 for the LB and HB frequency ranges was measured as 11.5 dBm and 6.7 dBm, respectively, at a 2 GHz LO frequency (i.e., f_{RF} = 2 GHz for the LB path and f_{RF} = 6 GHz for the HB path). Note that both in-band and OOB IIP3s of the LB frequency range are almost constant over dif-

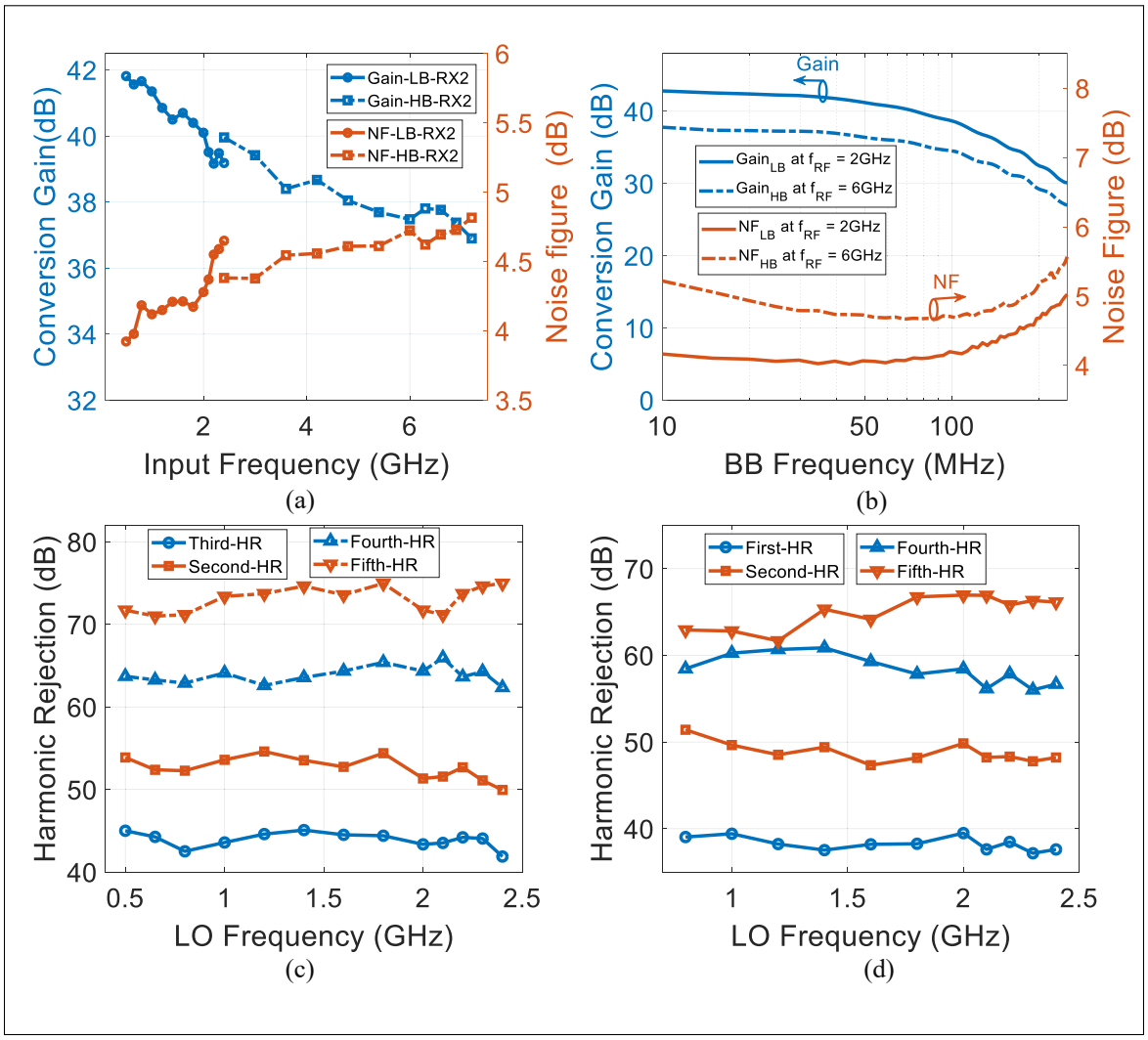

Figure 4.13 Measured performance of RX2 implemented in 65 nm CMOS: (a) Conversion gain and NF vs. input frequency (LO frequency is 0.5 −2.4 GHz) at an 80 MHz BB frequency, (b) conversion gain and NF for a f_{LO} = 2 GHz (f_{RF}=2 GHz and 6 GHz for the LB and HB frequency ranges, respectively) vs. the baseband frequency, (c) 3^{rd}, 2^{nd}, 4^{th}, and 5^{th} HRRs vs. LO frequency for the LB frequency range, and (d) 1^{st}, 2^{nd}, 4^{th}, and 5^{th} HRRs vs. LO frequency for the HB frequency range

ferent LO frequencies (see Fig. 4.14(a)). Fig. 4.14(b) depicts the measured LB and HB IIP3 over different offset frequencies Δf, where f_{LO} is set to 2 GHz. The OOB IIP3 in the LB frequency range reaches 15.6 dBm at a 300 MHz offset frequency, whereas the OOB IIP3 is 10.4 dBm in the HB frequency range.

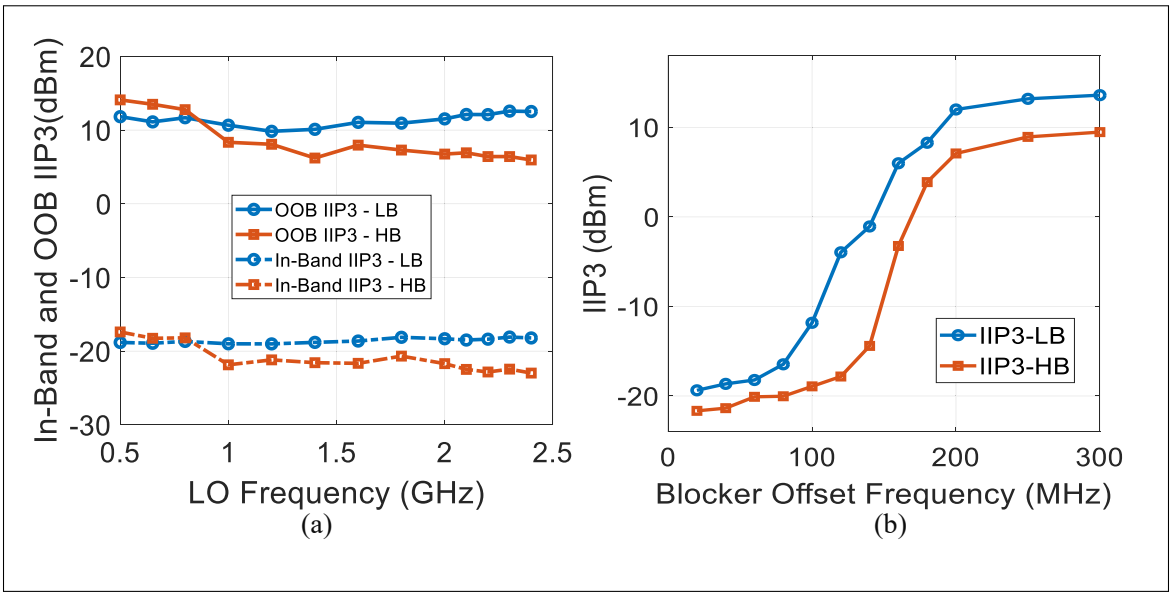

Figure 4.14 Measured RX2 (a) OOB and in-band IIP3 vs. LO frequency, and (b) IIP3 vs. blocker offset frequency

4.5.3 Performance Summary

The performance summary of the two presented HS-NC receivers in the LB and HB frequency ranges, and their comparison with other recently published blocker tolerant wideband receivers are listed in Table 2.1. The designs in Lien, Klumperink, Tenbroek, Strange & Nauta (2018a); Razavi & Razavi (2022) achieve an input bandwidth accommodating the sub-6 GHz cellular band and Wi-Fi signals, similarly to presented here. Measurement results show that the operating frequency of the designs can be up to 7.2 GHz while keeping NF less than 4.8 dB. The receiver designs in Krishnamurthy & Niknejad (2019); Lien *et al.* (2018a) achieve a higher linearity of 39 dBm and 33 dBm at the cost of significantly higher power dissipation of 80 mW and 179 mW, respectively. In addition, the achieved HRRs in Han, Haque, Bajor, Wright & Kinget (2020); Wu *et al.* (2019) appear to rely on calibration and mismatch adjustments post-fabrication. Compared to the prior art, the proposed inductorless architectures achieve high BB BW, wide operating frequency f_{RF}, low power consumption, and small chip area while maintaining comparable NF, gain and OOB IIP3. Moreover, the proposed architectures succeed in operating at a high RF input beyond 3 GHz (0.5 −7.2 GHz), while the 8-phase LO clock generator operates

up to 2.4 GHz (master clock of up to 9.6 GHz). The total DC and dynamic power consumption of the proposed differential architectures is much lower than that of receivers based on noise cancelling and non-linearity cancellation architectures, without sacrificing the NF, HRRs, and OOB linearity. This confirms that the effectiveness of the NC and 1^{st} and 3^{rd} HS-NPF configurations.

In addition, Fig. 4.15 summarises the conversion gain and NF of both proposed receivers vs. the input frequency for both the LB and HB frequency ranges. As discussed in section 4.2, the recombining of the down-converted LO harmonics right after the down-conversion, as done in RX1, helps to achieve a higher harmonic rejection at the unwanted LO harmonics, compared to the use of amplification before the BB harmonic recombination, as done in RX2. Although RX1 employs two BB harmonic recombination blocks for each of the LB and HB frequency ranges, leading to more DC power consumption, it avoids the down-converted LO harmonic blockers experiencing a large on-chip gain. In contrast, in RX2, the down-converted LO harmonic blockers are amplified by the TIAs used before the harmonic recombination, and thus harmonic selection occurs after this amplification. Thus, the blockers can easily desensitize the BB harmonic recombination blocks in addition to the TIAs.

4.6 Conclusion

5G and Wi-Fi 6E are complementary technologies working together to meet the ever growing connectivity needs. Two $0.5-7.2$ GHz wideband and blocker-tolerant RF receiver front-ends exploiting harmonic selection 8-path switching systems with resistive coefficients and noise cancellation have been designed and verified in TSMC 65 nm CMOS technology. Since driving the switches of the conventional 8-path switching system and 1^{st} and 3^{rd} HS-NPFs beyond 3 GHz increases the power consumption significantly, the proposed HS-NC architectures are configured to select the 1^{st} and 3^{rd}-order LO harmonic over a LB frequency range ($0.5-2.4$ GHz) and a HB frequency range ($2.4-7.2$ GHz), respectively. The RF HS-NC receivers employ two harmonic selection stages in order to efficiently tolerate LO blocker harmonics while still keeping a low NF, thanks to the NC technique. RX1 features differential 1^{st} and 3^{rd} HS-NPFs

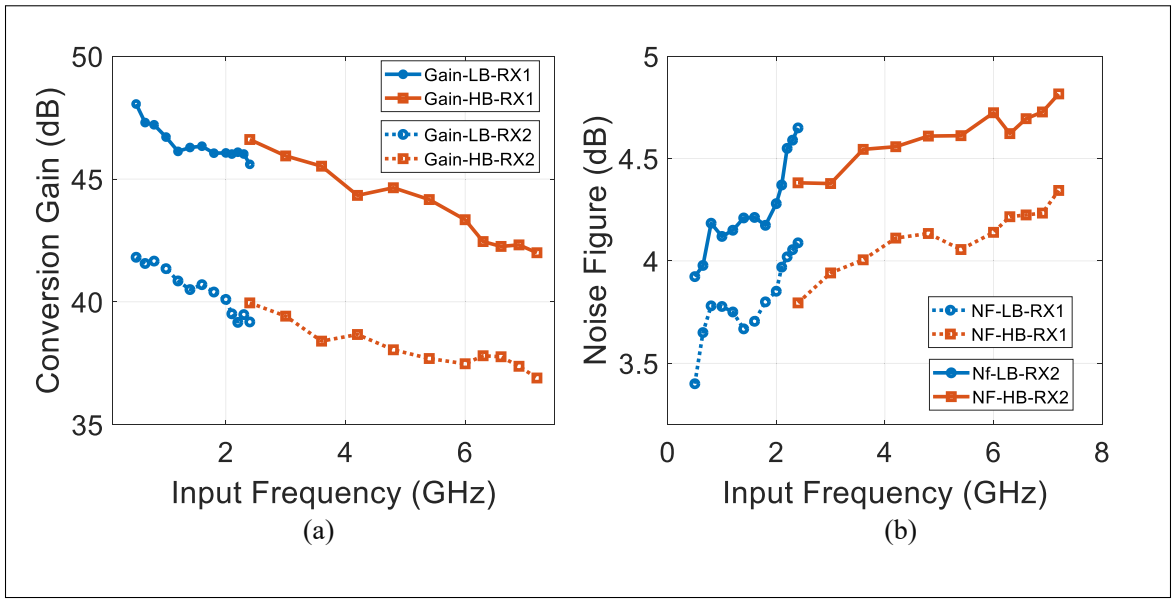

Figure 4.15 Measured (a) conversion gain and (b) NF of RX1 and RX2 over both supported RF ranges

with resistive coefficients to provide high-Q selectivity at the RF input, and is suitable for any voltage-driven passive mixer. RX2 features 1^{st} and 3^{rd} harmonic recombination blocks at the BB after a bank of TIAs to enhance the resilience to LO harmonic blockers.

In addition, 3^{rd} harmonic selection over the HB frequency range in addition to the 1^{st}-order LO harmonic selection over the LB frequency range helps to reduce the required input frequency of the 8-phase clock generator by a factor of three, and consequently significantly reduce its dynamic power consumption. Accordingly, the trade-off between wideband operation, noise, OOB linearity and power consumption is significantly relaxed.

RX1 demonstrates a 46 dB/43.4 dB conversion gain, 63 MHz/97 MHz BB bandwidth, 3.8 dB/4.1 dB NF, and 49 dB/43 dB HRR at a 2 GHz LO for the LB/HB frequency ranges, respectively. High-Q input selectivity facilitates a linear HS-NC receiver design that achieves higher than 13.7 dBm / 9.2 dBm OOB-IIP3 for the LB/HB frequency ranges, respectively. RX2 exhibits a conversion gain of 40 dB/37.4 dB, 3^{rd} and 1^{st} HRRs of 43.3 dB/39.4 dB, NF of 4.3 dB/4.7 dB, OOB-IIP3 of 11.5 dBm/6.7 dBm, and 88 MHz/103 MHz BB bandwidth at a 2 GHz LO frequency for the

Table 4.1 Measurement performance summary and comparison to recently published RF receivers

Parameters	Lien *et al.* (2018a)	Wu *et al.* (2019)	Krishnamurthy & Niknejad (2019)	Han *et al.* (2020)†	Bu *et al.* (2020)	Razavi & Razavi (2022)	This work	
	JSSC' 18	JSSC' 19	JSSC' 19	JSSC' 20	JSSC' 20	JSSC' 22	RX1	RX2
Tech. (nm)	45 SOI	28	28	65 GP	28	28	65	65
RF Input	Differential	Single-ended	Single-ended	Differential	Single-ended	Single-ended	Differential	Differential
Receiver Topology	Mixer first with positive capacitive feedback	Harmonic Selective NC	NPF driving an impedance with 40-dB/decade roll-off	Multi-branch modulated mixer clock	TI-FA +PVT-NC +NPF	Harmonic -trap technique	NC-1st and 3rd HS	NC-1st and 3rd HS
RF Freq. (GHz)	0.2-8	0.5-3	0.2-2	0.3-1.3	0.1-1	0.4-6	0.5-7.2	0.5-7.2
BB BW (MHz)	10	40-98	18	7-33	2.4-40	0.2-160	63-97	88-103
Gain (dB)	21	38-46	13	46.7	30	54	42-48	37-41.8
NF (dB)	2.3-5.4^{+}	2.4-5	4.3-7.6	2.7-4.4	4.1-5.8	2.1-4.42	3.4 -4.3	3.9-4.8
OOB IIP3 (dBm)	+39$^{\natural}$	+4	+33.3$^{\diamond}$	+8§	+18	+9.8	+15 9.2	11.5 6.7
In-Band IIP3 (dBm)	+5	-	+10$^{\diamond}$	-12.1	+9$^{\triangleleft}$	-20$^{\partial}$	-15.6 -19.8	-18.3 -21.6
HRR (dB)	-	+80‡	-	+51.7$^{\natural}$	-	+62.3	>47 >44	>42 >37
Power (mW)**	80	28-31	146.6-179	49.8	48-74	23-49	14.5-20.8	11.1-17.4
Active Area (mm^2)	0.8	1.2	0.48	1.8	3.75	1.9	0.93	0.93

** including the LO clock generator power, $^{+}$ 0.5 −6 GHz, $^{\natural}$ $\Delta f/BW$ = 8, $^{\diamond}$ +33.3 dBm at f_{OS}/BW = 4.4 and +10 dBm at f_{OS} = 10MHz. $^{\triangleleft}$ with calibration, † in the high-sensitivity mode, § $\Delta f/BW$ = 175/7, ‡ Δf =20MHz, $^{\partial}$ 40 MHz channel bandwidth around 5 GHz.

LB/HB frequency ranges, respectively. The RF front-ends of RX1 and RX2 consume 12.4 mW and 9 mW, respectively, and their clock generators consume only 2.1 −8.4 mW.

Thus, RX1 achieves better overall performance in comparison to RX2, but exhibits higher power consumption. The use of the harmonic recombination right after the down-conversion paths in RX1 helps to achieve the higher LO HRRs, lower NF and higher conversion gain, compared to RX2. In addition, RX1 enhances the large-signal resilience of the receiver to the harmonic blockers. However, RX1 consumes more DC power than RX2 due to the two BB harmonic recombination blocks for each of the LB and HB frequency ranges it features, as opposed to one for each frequency range in RX2.

4.7 Appendix A

Fig. 4.16(a) and (b) depicts the measured 3rd and 1st HRRs and OOB IIP3 of the RX1 for a sample of 7 chips at the LO frequency of 2 GHz, respectively, where the gate-bias voltage of M_1 in Fig. 4.5(e) and M_9 in Fig. 4.5(f) is adjusted externally to maintain the desired IIP3

performance. In addition, the 3^{rd} and 1^{st} HRRs and OOB IIP3 of the RX2 were measured for a sample of 7 chips at the LO frequency of 2 GHz, and are shown in Fig. 4.17 (a) and (b).

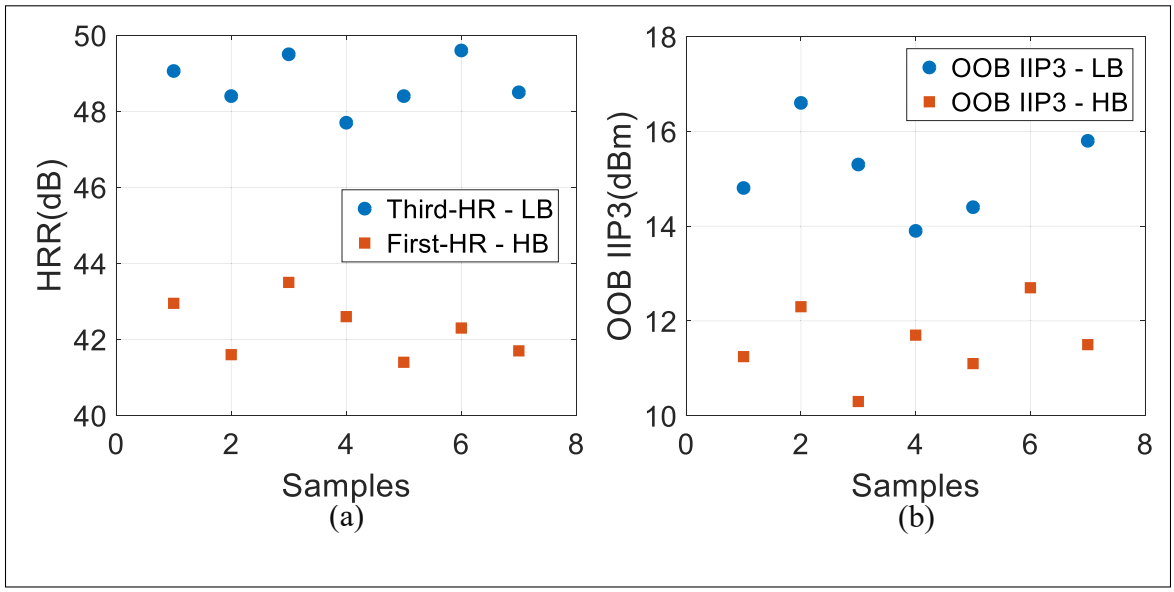

Figure 4.16 Measured (a) 3^{rd} and 1^{st} HRRs and (b) OOB IIP3 at the 2 GHz LO frequency over seven samples for the RX1

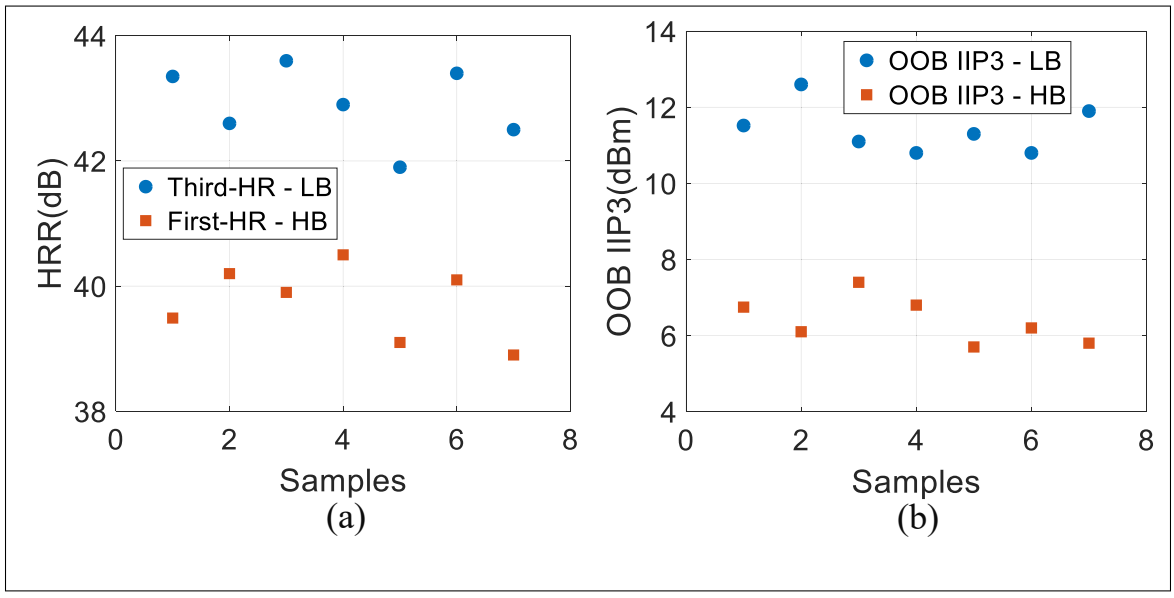

Figure 4.17 Measured (a) 3^{rd} and 1^{st} HRRs and (b) OOB IIP3 at the 2 GHz LO frequency over seven samples for the RX2

CHAPTER 5

AN OOK AND BINARY FSK RECONFIGURABLE DUAL-BAND NON-COHERENT IR-UWB RECEIVER SUPPORTING TERNARY SIGNALING

A portion of the receiver's power consumption is associated with the NMOS switches driving the N-path switching filter-based designs with the N-phase LO clock, as discussed in Chapter 4. This dynamic power consumption can be saved by exploiting a non-coherent IR-UWB architecture. IR-UWB technology is a growing research topic due to its low power consumption, low complexity, high data rate, and low transmission power.

Thus, the contribution of this chapter is the presentation of a multi-band IR-UWB non-coherent receiver that can be digitally reconfigured in different operating frequency modes. The proposed receiver employs a self-demodulating direct conversion RF front-end architecture with an OOK modulation scheme. Moreover, the proposed architecture supports ternary signaling by combining both OOK and FSK modulations. The receiver operates as a conventional non-coherent OOK IR-UWB receiver in the single-band modes. In the concurrent dual-band mode, the receiver has the capability of using binary FSK modulation in addition to OOK modulation and allowing for the leveraging of ternary signaling to enhance its performance.

An OOK and Binary FSK Reconfigurable Dual-Band Non-Coherent IR-UWB Receiver Supporting Ternary Signaling

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Abstract: This paper presents a multi-band low-power and low-complexity impulse radio ultra-wideband (IR-UWB) non-coherent receiver. The proposed receiver can be digitally reconfigured in three different modes of operation, including two single-band modes and one concurrent dual-band mode. In the two single-band modes, the proposed envelope detection architecture is capable of receiving and demodulating an on–off keying (OOK) pulse stream at RF center frequencies of 2.8 GHz or 4.8 GHz. In the concurrent dual-band mode, the proposed architecture is able to demodulate binary frequency shift keying (FSK), in addition to OOK demodulation, at center frequencies of 3 GHz and 5 GHz. The receiver is composed of a reconfigurable low-power differential low noise amplifier (LNA), a fully differential squarer (self-mixer circuit), low-pass filter (LPF) and variable gain baseband (BB) amplifiers. The receiver is fabricated in TSMC 130 nm CMOS process technology. The receiver can operate at up to 150 Mbps with the ternary signaling that is enabled by the binary FSK modulation combined with the OOK modulation in concurrent dual-band mode. At its maximum gain, the receiver achieves a sensitivity of -72 dBm at a bit error rate (BER) of 10^{-3} at a 100 Mbps data rate. It consumes 11.9 mW and 13.2 mW from a 1.2-V supply in the single-band modes and concurrent dual-band mode, respectively.

Keywords: Ultra-wide band, impulse radio, reconfigurable structure, non-coherent architecture, concurrent dual-band, programmable current switching, ternary signaling, on-off keying, binary frequency shift keying.

5.1 Introduction

The growing demand for ubiquitous wireless connectivity has exposed the potential of the Internet of Things (IoT) to fuel the next industrial revolution and become the largest market for electronic devices. To support IoT networks, communication systems have to support multiple standards while achieving good performance without increasing system size and cost. Notably, there is a strong motivation to provide a single radio system that is able to support multi-standards and multi-bands in order to suit as many IoT device types as possible.

Among all techniques used for multi-standard wireless systems, IR-UWB has gained much attention due in part to its potential for low power implementations. In the time domain, the IR-UWB system translates a large bandwidth signal to very narrow pulses. Data bits in IR-UWB systems are modulated on short duration pulses of less than 2 ns that can also provide very accurate localization capabilities (Bao, Zou, Nejad, Qin & Zheng (2018); Zhang *et al.* (2018b)). IR-UWB systems can feature very low power because of their inherent duty cycle advantage at relatively low data rates and because of their suitability to non-coherent detection, which does not require phase information that can typically be complex to extract.

One of the biggest challenges of IR-UWB systems lies in the receiver design. The receiver requires low energy consumption, high sensitivity, and a low-complexity implementations. Moreover, the receiver should have the ability of synchronization and fast acquisition, and be robust to timing mismatches. Coherent IR-UWB receiver architectures use bandwidth more efficiently and achieve a higher sensitivity at the cost of complex phase tracking blocks and added power consumption (Hazra & Tyagi (2014); Ouvry, Masson, Hameau, Gaillard & Caillat (2015); Zou, Mendoza, Wang, Zhou, Mao, Jonsson, Tenhunen & Zheng (2011)). Even a small misalignment in time results in a performance degradation. Alternatively, non-coherent IR-UWB receivers (Crepaldi *et al.* (2019); Fath, Schmickl, Faseth & Pretl (2021); Gimeno, Flandre & Bol (2017); Kim & Green (2016); Tsai, Chen, Wang, Yeh & Lin (2014)) have been widely accepted by low cost low power applications. IR-UWB systems can leverage non-coherent receivers to reduce the hardware complexity.

Moreover, the proper modulation scheme results in the efficient usage of the signal bandwidth, and improved power consumption and data-rate. In the receiver design, On-Off Keying (OOK) modulation is of special interest compared to Pulse Position Modulation (PPM) and Phase-shift keying (PSK), since it involves the detection of the envelope of the received RF signal at low power and cost (Hsieh *et al.* (2016); Im, Kim & Wentzloff (2018); Tsai, Liao & Li (2020)). The IR-UWB non-coherent receiver in (Crepaldi *et al.* (2019)) employs OOK modulation and operates at a 4 GHz center frequency with an overall power consumption of 12 mW, resulting in a 12 pJ/b energy efficiency at a 1 Gbps data rate. A 3.5 GHz receiver using a binary frequency-domain OOK modulation is proposed in (Ding *et al.* (2021)) that achieves a 100 Mb/s data rate and an energy efficiency of 243 pJ/b, while consuming 24.3 mW from a 1-V supply.

Moreover, in order to meet the requirement of low power consumption, frequency-shift keying (FSK) modulation is used in Wi-Fi (Im, Kim & Wentzloff (2017)) and Bluetooth low energy (BLE) (Abdelhamid, Paidimarri & Chandrakasan (2018); Alghaihab, Shi, Breiholz, Kim, Calhoun & Wentzloff (2019)). The FSK scheme provides a high-transmission efficiency, resilience to interference (Hsieh *et al.* (2016)), and is more robust to frequency pulling because of its constant envelope nature (Lee & Kwon (2021); Tang & Culurciello (2011); Zgaren & Sawan (2015)). A 2.4 GHz receiver architecture in (Lee & Kwon (2021)) employs a switched dual-mode demodulator to support both OOK and binary FSK modulations, consuming 1.8 mW at the cost of a 9.9 dB noise figure (NF). The sub-GHz receiver proposed in (Cheng & Chen (2021)) presents an ultra low power (54 µW) architecture compatible with OOK, binary FSK, and differential binary PSK modulations, and operates at 433 MHz with data rate of 200 kb/s. Overall, these works rely on single and static band selection, leading to performance trade-offs that cannot be modified once the designs are tuned to one set of parameters. Moreover, the proposed structures do not support IR-UWB signals.

Reconfigurable and flexible receiver architectures can achieve multi-band operation so that the receiver can be digitally tuned to different bands over a wide frequency range (Shams *et al.* (2019)). This is the approach proposed in this work to design an IR-UWB receiver. In addition to the multi-band design, Since the non-coherent IR-UWB receiver reduces the power

consumption and energy efficiency, we select a non-coherent architecture based on an envelope detector so that no power-hungry blocks such as oscillators are required. Moreover, the non-coherent architecture requires no timing synchronization or channel estimation, leading to a reduced complexity of the radio front-end.

Accordingly, this work aims to provide a more agile design through a differential reconfigurable multi-band non-coherent IR-UWB receiver supporting both OOK and binary FSK signal demodulation, and fabricated in 130 nm TSMC CMOS process technology. The main contribution of this work is the reconfigurable multi-band envelope detection structure that can be digitally reconfigured in order to support different operating frequency modes, including two single-band modes at center frequencies of 2.8 GHz or 4.8 GHz, and one concurrent dual-band mode at center frequencies of 3 GHz and 5 GHz. Moreover, the proposed receiver architecture has the capability of demodulating at the BB binary FSK signals in addition to OOK signals, allowing for versatile operation. It also can support ternary signaling by combining OOK and FSK modulations to increase channel capacity or improve data transport efficiency, and benefit the analog to digital conversion operation (Abdelaziz & Gulliver (2019); De Wit, Zhang & Reynaert (2019); Morozov, Pilipko & Korotkov (2011); Vyawahare, Deshmukh & Chandurkar (2014)). Data recovery at the BB can be classified into two categories: i) pulses detected with the same polarity from OOK demodulation, and ii) pulses detected with bipolar polarities from FSK demodulation. In the proposed reconfigurable IR-UWB envelope detection architecture, when the receiver operates in one of the single-band modes, the low duty cycling OOK IR-UWB signals can be demodulated and distinguished at the BB by pulses having the same polarity. Alternatively, when the receiver operates in concurrent dual-band mode, binary FSK demodulation is carried-out such that the polarity of the demodulated signals is correlated with the center frequency of the input RF signal. Accordingly, in concurrent dual-band mode, a positive polarity detected at the BB indicates an input RF signal in the 3 GHz band, while a negative polarity at the BB indicates an input RF signal centered in the 5 GHz band.

Importantly, since the proposed receiver employs a self-demodulating direct conversion RF front-end structure, it avoids the use of frequency translation blocks like a down-conversion

mixer, a phase-locked loop (PLL) and an oscillator. As opposed to work in (Cheng & Chen (2021); Ding *et al.* (2021); Lee & Kwon (2021); Zgaren & Sawan (2015)), this reduces chip area and power consumption. The system and circuit blocks are designed and optimized to achieve good sensitivity and low power consumption.

The rest of this paper is organized as follows. Section 5.2 presents the system design of the proposed IR-UWB receiver structure for the different modes of operation. The LNA, squarer and BB amplifier are detailed in Section 5.3. Section 5.4 presents the post-layout simulation results along with the measurement results of the fabricated non-coherent IR-UWB receiver and discusses them, and is followed by a conclusion.

5.2 Receiver Architecture

The proposed architecture of the reconfigurable multi-band IR-UWB receiver is depicted in Fig. 5.1. The receiver operates in the $2.8-5$ GHz band with a bandwidth of 500 MHz. The RF front-end architecture starts with a reconfigurable differential wideband LNA amplifying the incoming RF UWB pulses. The reconfigurable multi-mode LNA is able to operate in two single-band modes (mode 1 and 2) and one concurrent dual-band mode (mode 3). As will be detailed in Section 5.3, the proposed LNA employs the programmable current mode switches (SW1 and SW2) to select the operation modes (see Fig. 5.1). The current mode switch configuration for different operation modes is shown in Table 5.1, where f_0 is the band center frequency.

Fig. 5.2 illustrates an overview of the symbol representation and three incoming IR-UWB pulses types: two single-bands pulses centered at 2.8 or 4.8 GHz, and one concurrent dual-band set of pulses at 3 GHz and 5 GHz. A modulated pulse with the width of $t_{pulse} = 2$ ns is toggled to represent '1' and '0' via OOK modulation.

The amplified IR-UWB signals are down-converted by employing either the squarer circuit SQ_{SB} or squarers SQ_{CDBM1} and SQ_{CDBM2}, depending on the receiver's operating mode (see Fig. 5.1, where the blocks related to each mode are outlined in a different color. Then, the envelope of the squared signals is captured by the LPF and amplified by the BB amplifier chain.

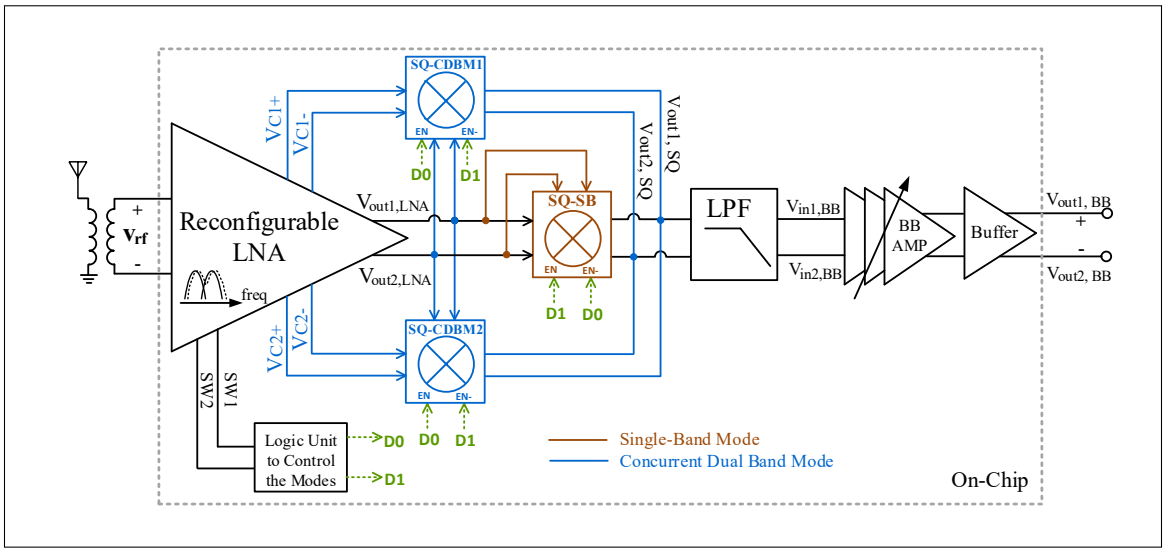

Figure 5.1 Proposed reconfigurable multi-mode non-coherent IR-UWB receiver. Blocks used by each of the modes are outlined in different colors

Note that there is a logic unit that controls which operation mode of the receiver is active, as shown in Fig. 5.1. Squarers SQ_{SB}, SQ_{CDBM1} and SQ_{CDBM2} include enable and disable pins controlled by $D1$ and $D0$. $D1$ and $D0$ with respect to the operating mode of the LNA are used to enable or disable squarers SQ_{SB}, SQ_{CDBM1} and SQ_{CDBM2} as necessary. When the reconfigurable LNA operates in one of the two single-band modes (i.e., SW1=1, SW2=0 or SW1=0, SW2=1), the logic unit outputs $D1$ and $D0$ are '1' and '0', respectively. If the LNA operates in the concurrent dual-band mode (i.e., SW1=1, SW2=1), the outputs of $D1$ and $D0$ are '0' and '1', respectively.

5.2.1 Single-Band Mode

The proposed receiver operates in two single-band modes (mode 1 and 2). In mode 1, when the LNA's programmable switches SW1 and SW2 are set as '1' and '0', respectively (see Table 5.1), only incoming IR-UWB signals centered at 2.8 GHz (see Fig. 5.2) are amplified by the LNA. When in mode 2, the switches are set to SW1=0 and SW2=1, and the LNA only amplifies the IR-UWB signals centered at 4.8 GHz.

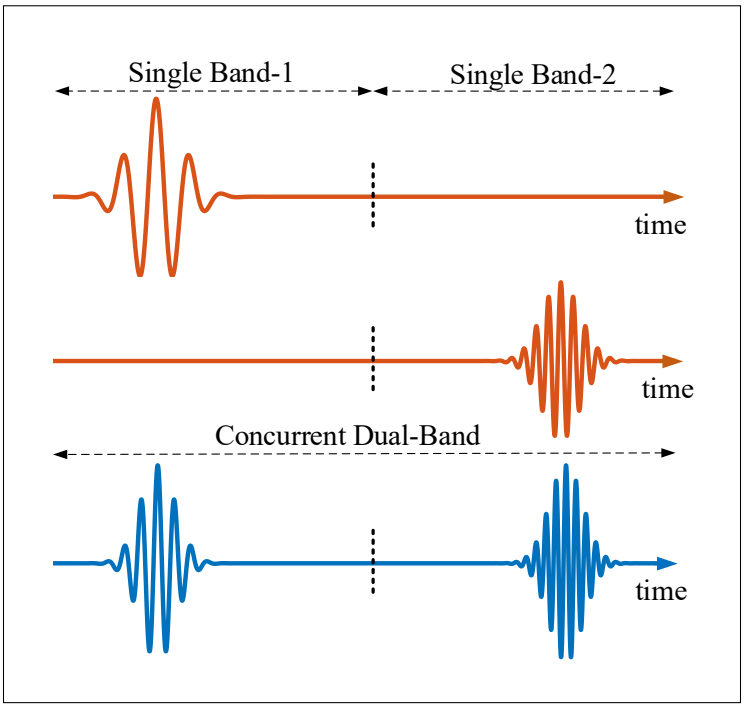

Figure 5.2 Different operation bands of the reconfigurable IR-UWB receiver

Table 5.1 Operation modes supported using the current-mode switches.

Modes	SW1	SW2	f_0 (GHz)	Note
1	1	0	2.8	Single-band
2	0	1	4.8	Single-band
3	1	1	3 and 5	Concurrent dual-band

In the single-band modes, the amplified RF pulse at the output of the LNA ($V_{out1,LNA}$, $V_{out2,LNA}$) is squared (thus down-converted) by squarer circuit SQ_{SB} (see Fig. 5.1) that acts as an envelope detector in order to demodulate the incoming OOK-modulated signal, yielding a self-demodulating structure. Note that the amplified RF pulse can be down-converted by employing either conventional passive and active mixers or squarer (self-mixing) circuit. The former approach requires the generation of a local template pulse using an LO signal at the center frequency of the pulse to be mixed with the incoming signal. This approach is very sensitive to the timing and shape of the template pulse. Thus, there is a need to provide an accurate template and precise synchronization for high performance operation (Allidina (2015)). Alternatively

here, the squarer circuit mixes the incoming RF signal with itself, and since there is no need to generate the template pulse, implementation complexity will be reduced which is desirable for a low power receiver.

In the single-band modes, when squarer SQ_{SB} is enabled, squarers SQ_{CDBM1} and SQ_{CDBM2} are disabled to save power. In order to capture the envelope of the squared signal, a LPF is used at the output of the squarer, as shown in Fig. 5.1. Then, the variable gain BB amplifiers provides enough signal gain to trigger the next digital conversion stages.

5.2.2 Concurrent Dual-band Mode

In the concurrent dual-band mode (mode 3), the incoming RF signal contains two different frequency bands around 3 GHz and 5 GHz (see Fig. 5.2). The two incoming RF input signals are amplified by the LNA concurrently at its outputs ($V_{out1,LNA}$, $V_{out2,LNA}$). In addition, the LNA structure provides two more RF differential outputs: V_{C1+}, V_{C1-} and V_{C2+}, V_{C2-}. V_{C1+} and V_{C1-} contain the amplified RF signal at 3 GHz (i.e., less amplification occurs at the 5 GHz band), and V_{C2+} and V_{C2-} contain the amplified RF signal at 5 GHz (i.e., less amplification occurs at the 3 GHz band).

In the concurrent dual-band mode, two squarers (SQ_{CDBM1} and SQ_{CDBM2}) down-convert the dual-band signal. As can be seen from Fig. 5.1, $V_{out1,LNA}$ and $V_{out2,LNA}$ are multiplied with V_{C1+} and V_{C1-} by using squarer SQ_{CDBM1}. As previously discussed, $V_{out1,LNA}$ and $V_{out2,LNA}$ contain both signals at 3 GHz and 5 GHz, while V_{C1+} and V_{C1-} contain the amplified signal only at the 3 GHz band. Thus, the result of the multiplication is that the pulse envelope in the 3 GHz band is extracted at the SQ_{CDBM1} output, $V_{out1,SQ}$. In a similar fashion, SQ_{CDBM2} is fed with $V_{out1,LNA}$ and $V_{out2,LNA}$ and V_{C2+} and V_{C2-}. As previously discussed, V_{C2+} and V_{C2-} contain the amplified signal only at the 5 GHz band. Thus, $V_{out2,SQ}$ contains the pulse envelope in the 5 GHz band.

Since the BB amplifier $V_{in1,BB}$ input is fed by $V_{out1,SQ}$, and $V_{in2,BB}$ is fed by $V_{out2,SQ}$, the BB amplifier outputs a positive pulse at its differential outputs (i.e., $V_{out2,BB} - V_{out1,BB}$) when $V_{in1,BB}$ is larger than $V_{in2,BB}$. Conversely, it outputs a negative pulse when $V_{in2,BB}$ is larger than $V_{in1,BB}$.

Fig. 5.3 shows the transient post-layout simulation of the concurrent dual-band mode including the LNA output of both-frequency pulses, the outputs of SQ_{CDBM1} and SQ_{CDBM2}, and the BB amplifier differential outputs including their difference $V_{out2,BB} - V_{out1,BB}$. As shown in Fig. 5.3, the output of $V_{out1,SQ}$ at the 3 GHz band has higher amplitude than the output of $V_{out2,SQ}$, and the output of $V_{out2,SQ}$ at the 5 GHz band has a higher amplitude than the output of $V_{out1,SQ}$. The resulting BB amplifier differential output polarity shows the FSK-demodulated dual-band signal.

In this fashion, the reconfigurable IR-UWB receiver is capable of decoding the frequency information of the received pulse through the polarity of the BB output. This translates to a positive BB output signal indicating an input RF pulse at the 3 GHz band, and to a negative BB output signal indicating an RF pulse at the 5 GHz band, as shown in Fig. 5.3. This can be leveraged to operate the receiver in binary FSK demodulation, without employing an additional oscillator and PLL.

It should be mentioned that the LPF and BB amplifiers are shared by the two bands simultaneously, and since two squarers (SQ_{CDBM1} and SQ_{CDBM2}) are active in this mode, the receiver dissipates more power, compared to operation in either of the single-band modes.

5.3 RF Front-end Circuit Design

In this section, the reconfigurable multi-band differential LNA based on programmable current mode switches, the squarer circuit, and the variable gain BB amplifier are presented. All of the circuits are implemented in one chip with a 1.2-V supply.

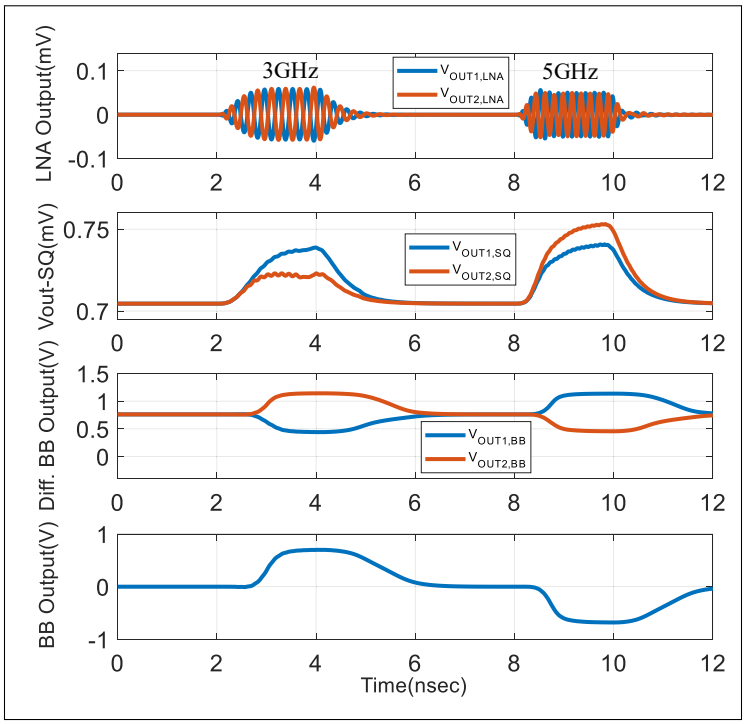

Figure 5.3 Transient post-layout simulation of the proposed receiver in the concurrent dual-band mode

5.3.1 Reconfigurable Multi-band Fully-Differential LNA

A differential UWB multi-band LNA is proposed in this work and shown in Fig. 5.4. As was discussed previously, it can operate in two different single-bands or a concurrent dual-band.

The LNA is composed of two stages. The first stage is a common-gate (CG) topology, used due to its wideband input matching characteristics. The transconductance of the input CG transistor M_0 is set to $g_m = 1/R_s$, where R_s is the source resistance and equal to 50 Ω. Thus, the matching bandwidth can be expressed by

$$f_{BW} = \frac{1}{2\pi C_{gs0}\frac{1}{g_{m,M_0}}}. \tag{5.1}$$

where C_{gs0} is the gate-source capacitance and g_{m,M_0} is the transconductance of transistor M_0, respectively. Therefore, the input impedance at resonance can be matched to 50 Ω by con-

trolling g_{m0}. Although the CG topology shows poorer noise performance compared to the common source (CS) topology, it has become a useful structure at higher frequencies (Shim, Yang & Jeong (2013)).

Note that a symmetrical and balanced architecture is preferred over an unbalanced one because of its robustness to substrate noise, suppression of even order harmonics and resilience to power-supply ripples. Thus, to benefit from a symmetric structure and to provide the bias current paths, two center-tapped on-chip inductors, L_s and L_d are connected to the source of M_0 and the drain of transistors M_3 and M_4. The values of these inductors are chosen to resonate in the desired operation band with the parasitic capacitances of transistors M_0, M_3 and M_4 and the extracted parasitics. Thus, by considering coupling capacitor C_1, the input impedance of the CG amplifier is given by

$$\mathrm{Z_{in}} = \frac{1}{j\omega C_1} + (\frac{1}{j\omega C_s} \parallel j\omega L_s \parallel \frac{1}{g_{m,M_0}}), \tag{5.2}$$

where L_s and g_{m,M_0} are the degeneration inductor and the input transconductance, respectively, and C_s is the total input capacitance of M_0 at the input of the CG. The real part and the imaginary part of Z_{in} are calculated as

$$\mathrm{R[Z_{in}]} = \frac{g_{m,M_0} L_s^2 \omega^2}{(L_s C_s)^2 \omega^4 + L_s(g_{m,M_0}^2 L_s - 2C_s)\omega^2 + 1}, \tag{5.3}$$

and

$$\mathrm{X[Z_{in}]} = -\frac{L_s^2 C_s(C_1 + C_s)\omega^4 + L_s(g_{m,M_0}^2 L_s - 2C_s - C_1)\omega^2 + 1}{C_1[(L_s C_s)^2 \omega^4 + L_s(g_{m,M_0}^2 L_s - 2C_s)\omega^2 + 1]\omega}. \tag{5.4}$$

To keep Z_{in} purely resistive at the resonant frequency ω_0, the imaginary part $X[Z_{in}]$ should be zero. Thus, ω_0 can be calculated as

$$\omega_0 = \sqrt{\frac{C_1 - g_{m,M_0}^2 L_s}{L_s C_1 C_s}}. \tag{5.5}$$

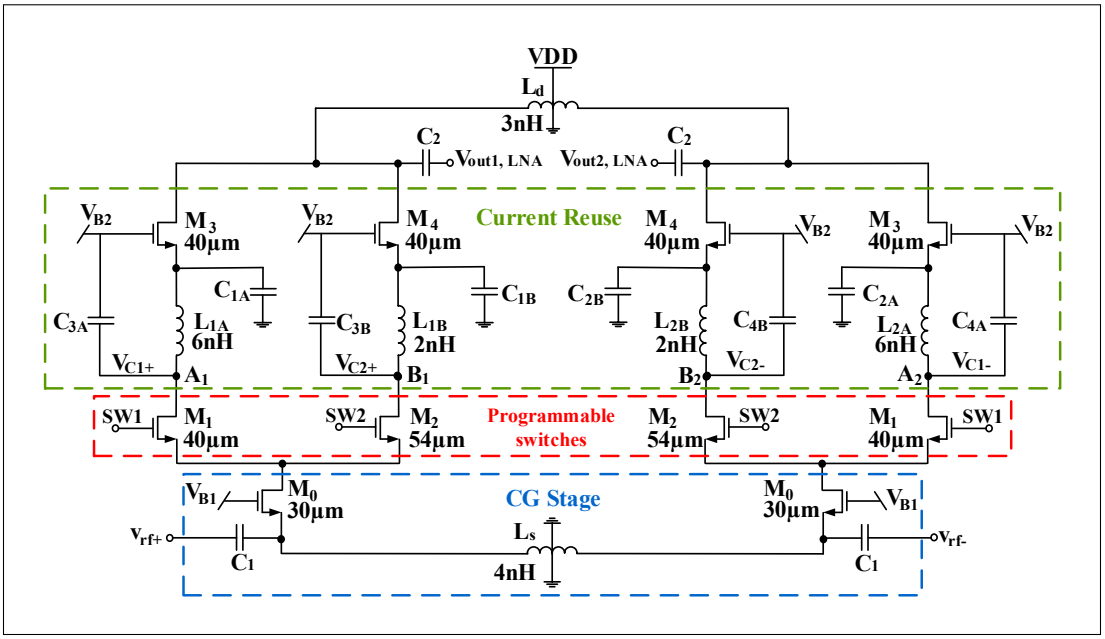

Figure 5.4 Schematic of the reconfigurable fully-differential LNA

By substituting (5.5) into (5.3), the resistive input impedance $R[Z_{in}]$ at ω_0 is expressed as

$$Z_{\text{in}}(\omega_0) = \frac{g_{m,M_0} L_s (C_1 - g_{m,M_0}^2 L_s)}{C_s (C_1 - g_{m,M_0}^2 L_s)^2 + g_{m,M_0}^2 L_s (C_1 - g_{m,M_0}^2 L_s) + C_1 C_s}. \tag{5.6}$$

By substituting the $g_{m,M_0} = 21.6\ mS$, $L_s = 4\ nH$, $C_1 = 1.5\ pF$, and $C_s = 35\ fF$ into (5.6), an input impedance, Z_{in}, of 50.14 Ω is achieved.

The second stage of the LNA is composed of programmable current mode switches M_1 and M_2, as shown in Fig. 5.4. The main function of this stage is to provide band selection. The programmable current switches select the desired operating mode according to Table 5.1, as previously discussed.

The transistor switches M_1 and M_2 are DC control switches, when SW1 and SW2 are set as 'ON' and 'OFF', respectively, a 1-V DC voltage is applied to the gate of transistor M_1. However, when SW2 is set to 'ON', a 1-V DC voltage is applied to the gate of M_2. In the concurrent dual-band mode, both SW1 and SW2 are 'ON' such that a 1-V DC voltage is simultaneously applied to

the gates of M_1 and M_2. As a result, both received RF input signals are amplified since both LNA paths are active.

Moreover, the LNA exploits the current reuse technique to achieve high power gain at a reduced power cost. Transistors M_3 and M_4 are stacked onto switches M_1 and M_2, respectively. When either M_1 or M_2 is ON, the drain current passes through M_3 and M_4 in one of the two branches. The current reuse structure employs some passive components. C_{1A} and C_{1B} (C_{2A} and C_{2B} in the other branch) act as the bypass capacitors at the source of M_3 and M_4 and enhance the gain of the CS stage. These bypass capacitors are selected to be large enough to operate as an AC ground, i.e. 10 pF. RF choke inductors L_{1A} and L_{1B} (L_{2A} and L_{2B} in the other branch) prevent the RF signal from passing from the drain of M_0 to the source of M_3 and M_4. In addition, these inductors act as the loads of the CG stage. C_{3A} and C_{3B} (C_{4A} and C_{4B} in the other branch) act as coupling capacitors to provide an RF signal path between the CG (M_0) and CS (M_3 and M_4) stages. In addition, the coupling capacitors values are chosen so that the C_{gs} parasitic capacitances of M_3 and M_4 resonate with inductors L_{1A} and L_{1B}, respectively (L_{2A} and L_{2B} in the other branch).

In the proposed LNA topology, the noise originating from M_1, M_3 and L_{1A} (M_2, M_4 and L_{1B}) can be reduced by the gain of the first stage. When M_1 is ON and M_2 is OFF, the overall NF of the LNA's equivalent half-circuit can be calculated by

$$\mathrm{F} = \frac{\overline{V^2_{n,out1,LNA}}}{(A_{V_{LNA}})^2} \times \frac{1}{\overline{V^2_{n,S}}}, \tag{5.7}$$

where $\overline{V^2_{n,out1,LNA}}$ represents the output noise of the LNA. $\overline{V^2_{n,S}}$ and $A_{V_{LNA}}$ are thermal noise of the source resistor and the LNA's voltage gain, respectively. The LNA output noise and voltage gain analysis details are derived in Appendix A. According to (5.7) above and (5.28) in Appendix A, the total noise factor can be written as

$$
\begin{aligned}
\mathrm{F} = 1 + [&\frac{g_{m,M_0}(\frac{1}{g_{m,M_1}}||\frac{1}{C_{p1}s})}{1 + g_{m,M0}((\frac{R_S}{2} + \frac{1}{C_1 s})||\frac{L_s}{2}s||\frac{1}{C_{p1}s})}]^2 \times \\
&\frac{1}{A^2_{V_{1st}}} \times \frac{\gamma}{g_{m,M_0}R_S} + \frac{1}{A^2_{V_{1st}}} \times \frac{\gamma}{g_{m,M_1}R_S} + \\
&\frac{1}{(A_{V_{1st}}A_{V_{2nd,3rd}})^2} \times [(\frac{L_d}{2}s||\frac{1}{C_{p4}s})g_{m,M_3}]^2 \times \frac{\gamma}{g_{m,M_3}R_S},
\end{aligned}
\tag{5.8}
$$

where $A_{V_{1st}}$ is the voltage gain of the CG stage and $A_{V_{2nd,3rd}}$ is the second and third stages' voltage gain. $A_{V_{1st}}$ and $A_{V_{2nd,3rd}}$ are given by (5.16) and (5.17) in Appendix A, respectively. The first term in (5.8) is derived from the thermal noise of R_S ($\overline{V^2_{n,S}}$). The other terms are related to the drain current noise of $\overline{i^2_{n,M_0}}$, $\overline{i^2_{n,M_1}}$, and $\overline{i^2_{n,M_3}}$. The total NF depends on transconductances g_{m,M_0} and g_{m,M_1}, as seen in (5.8). Thus, both g_{m,M_0} and g_{m,M_1} should be high enough to obtain a low NF. Accordingly, a high voltage gain can simultaneously be achieved. However, the increase of g_{m,M_0} and g_{m,M_1} results in more power consumption. Therefore, there is a trade-off between the voltage gain, noise performance and power consumption.

5.3.2 Fully Differential Squarer

The squaring operation in the proposed reconfigurable envelope detection receiver is performed by employing a double balanced active mixer and LPF load. The mixer and LPF schematic are shown in Fig. 5.5. All of the transistors are biased in the saturation region and they are sized to yield the lowest attenuation. Differential pairs M_7/M_8, M_9/M_{10} and M_{11}/M_{12} form the core of the squarer circuit. PMOS transistors M_{13} and M_{14} act as an active load to enhance the output voltage swing. To stabilize the output common mode, feedback using resistor R is employed. As shown in Fig. 5.5, two differential RF input signals v_{rf+} and v_{rf-} are connected to the transistors so that the circuit acts as a fully differential squarer.

The biasing current of the squarer is set by using current source transistor M_6. The LPF extracts the envelope of the squared signal at the squarer output. It is realized through the output resistance of the squarer and capacitors C_1 and C_2. Since the proposed receiver architecture shown

in Fig. 5.1 employs three squarer circuits, SQ_{SB} for the two single-band modes, and SQ_{CDBM1} and SQ_{CDBM2} for concurrent dual-band mode, transistors M_5 and M_{15} can enable or disable the squarers in accordance with the operation modes of the receiver described previously. This allows to reduce the power consumption when operating in one of the single-band modes.

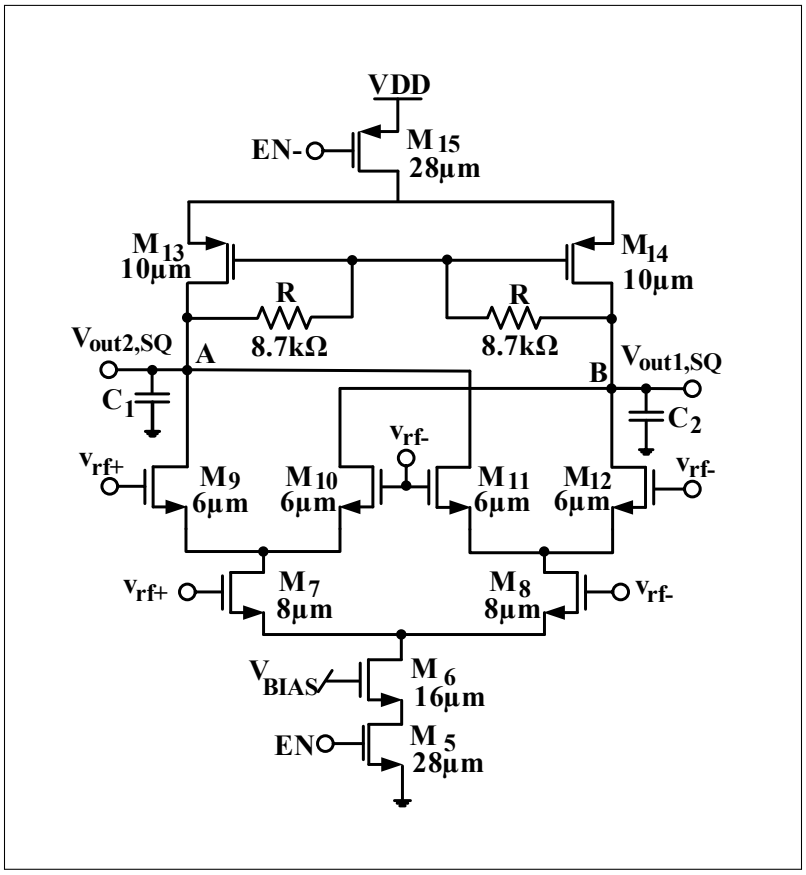

Figure 5.5 Schematic of the squarer circuit integrated with a LPF load

The squaring operation is achieved through the intrinsic characteristics of the MOS transistor. In Fig. 5.5, the small signals of the drain current of M_7 and M_8 (i_{d,M_7} and i_{d,M_8}) are expanded to the Taylor series in terms of small signal v_{gs}. To simplify the analysis, the drain current (i_d) dependence on v_{ds} has been neglected. The resulting expression for the small signal drain current is given by

$$i_d = g_m v_{gs} + g'_m v_{gs}^2 + g''_m v_{gs}^3 + ..., \tag{5.9}$$

where g_m, g'_m, and g''_m are the transistor's transconductance and its derivatives with respect to v_{gs}. A squarer circuit is designed to cancel the terms related to g_m and g''_m in (5.9) to achieve a squaring operation of the small signal voltage. The circuit structure shown in Fig. 5.5 can accomplish this. Drain currents i_{d,M_7} and i_{d,M_8} can be given by

$$i_{d,M_7} = g_{m,M_7} v_{rf+} + g'_{m,M_7} v_{rf+}^2 + g''_{m,M_7} v_{rf+}^3, \tag{5.10}$$

and

$$i_{d,M_8} = g_{m,M_8} v_{rf-} + g'_{m,M_8} v_{rf-}^2 + g''_{m,M_8} v_{rf-}^3. \tag{5.11}$$

Since $v_{rf-} = -v_{rf+}$, (5.11) can be written as

$$i_{d,M_8} = g_{m,M_8}(-v_{rf+}) + g'_{m,M_8}(-v_{rf+})^2 + g''_{m,M_8}(-v_{rf+})^3. \tag{5.12}$$

Considering that M_7 and M_8 have the same size and biasing, and $i_{d,M_9} = \frac{1}{2} i_{d,M_7}$ and $i_{d,M_{11}} = \frac{1}{2} i_{d,M_8}$. The output current,$i_{OUT+}$, can then be written as

$$i_{OUT+} = i_{ds,M_9} + i_{ds,M_{11}} = \frac{1}{2}(i_{d,M_7} + i_{d,M_8}) = g'_{m,M_7}(v_{rf+})^2. \tag{5.13}$$

This shows that i_{OUT+} is ideally dependant on g'_{m,M_7} and on the square of the input RF voltage, v_{rf+}. Increasing the transconductance g_{m,M_7} increases the slope of the transconductance, g'_{m,M_7}, resulting in a higher squarer conversion gain.

Appendix B provides an analysis of the conversion gain of the squarer circuit, yielding the following expression

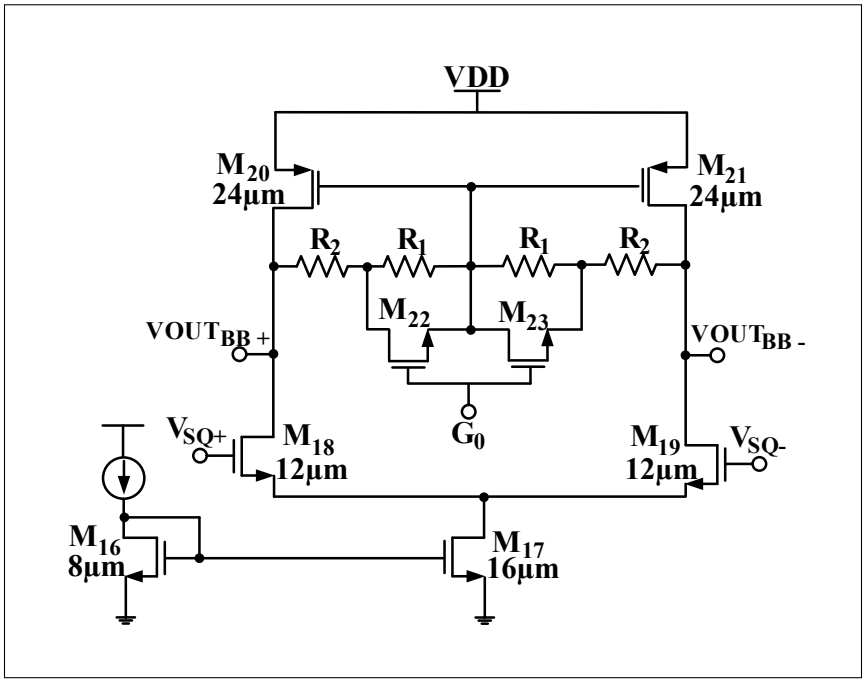

Figure 5.6 Schematic of the variable gain BB amplifier circuit

$$\mathrm{A}_{SQ} = \frac{V_{out1,SQ} - V_{out2,SQ}}{v_{rf+} - v_{rf-}} = 2R_{OUT+} \times 2g_{m,M_9}(1- [r_{o,M_7}||\frac{1}{C_{p0}}||\frac{1}{2}(\frac{r_{o,M_9} + R_A}{1 + g_{m,M_9}r_{o,M_9}})] \times g_{m,M_7}), \tag{5.14}$$

where r_o, R_A, R_B, and C_{p0} are the channel resistance of the transistors, the output resistances seen from node A and B, and the parasitic capacitance caused by M_7, M_9 and M_{10}, respectively. Outputs ($V_{out1,SQ}$ and $V_{out2,SQ}$) are plotted in Fig. 5.3 when the receiver operates in the concurrent dual-band mode.

5.3.3 Differential Variable Gain Baseband Amplifier

The BB output of the squarer suffers from significant gain loss. Thus, the BB amplifier shown in Fig. 5.6 acts as an essential stage in the pulse detection and improves the dynamic range of the receiver. To achieve a high voltage gain, transistors $M_{16} - M_{21}$ are sized and biased

in the saturation region. For this fully differential structure, a common-mode feedback circuit consisting of R_1 and R_2 is employed to stabilize the output common-mode. Gain control is performed by varying the output resistance by using M_{22} and M_{23}. A three-stage amplifier is implemented with this structure to provide enough amplification for the squared signal.

The three variable gain BB amplifiers are cascaded to fulfill the linearity requirement of the receiver, as the linearity of the receiver is dominated by the last stage. Note that the linearity of the BB amplifiers would be degraded by the stacking of transistors and the architecture selected for the BB stages has high linearity due to its reduced stacking. Its fully-differential nature also benefits the non-linearity performance.

5.4 Measurement Results

The reconfigurable IR-UWB receiver front-end is fabricated in TSMC 130 nm CMOS technology and the die has been packaged in a 48-pin 7 mm × 7 mm QFN package. Fig. 5.7(a) shows the measurement setup. The fabricated chip micrograph is shown in Fig. 5.7(b). The die size including the pad frame is of 1.5 mm × 1 mm with an active area of 0.96 mm^2, of which 0.64 mm^2 is occupied by the LNA.

The measurement results of the reconfigurable LNA and of the proposed IR-UWB receiver are presented in the two following subsections.

To characterize the differential multi-band LNA, two external RF baluns were mounted on a printed-circuit-board (PCB) due to its differential nature. The LNA different frequency band modes of operation are managed by using two switches that have been mounted onto the PCB. When the LNA operates in either of the two single-band modes, it consumes a total of 10.4 mW from a 1.2-V supply. In concurrent dual-band mode, it consumes 11.3 mW from the same supply.

The S-parameters were measured by using a network analyzer (Agilent PNA N5225A). Fig. 5.8 compares the measured and post-layout simulation results including S11, S21 and NF for the

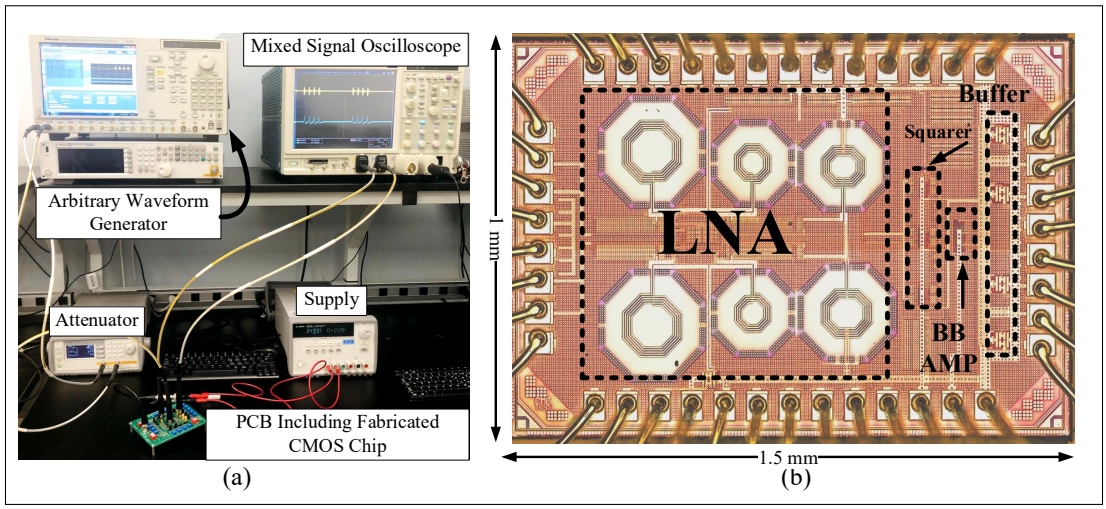

Figure 5.7 (a) Measurement setup used to characterize the proposed design, and (b) micrograph of the reconfigurable IR-UWB receiver front-end, occupying an active area of 1.2 mm × 0.8 mm in 130 nm CMOS

three different operating modes. As can be seen in Fig. 5.8, the input reflection coefficient (S11) of the LNA is well below −10 dB within the operating band, spanning from 2 to 5.5 GHz, in each mode of operation. The measured gains, eliminating the losses in the output buffer and the off-chip baluns, are 14.8 dB and 13.4 dB for the band-1 and band-2 single-band modes, respectively, and 13.7 dB for the concurrent dual-band mode.

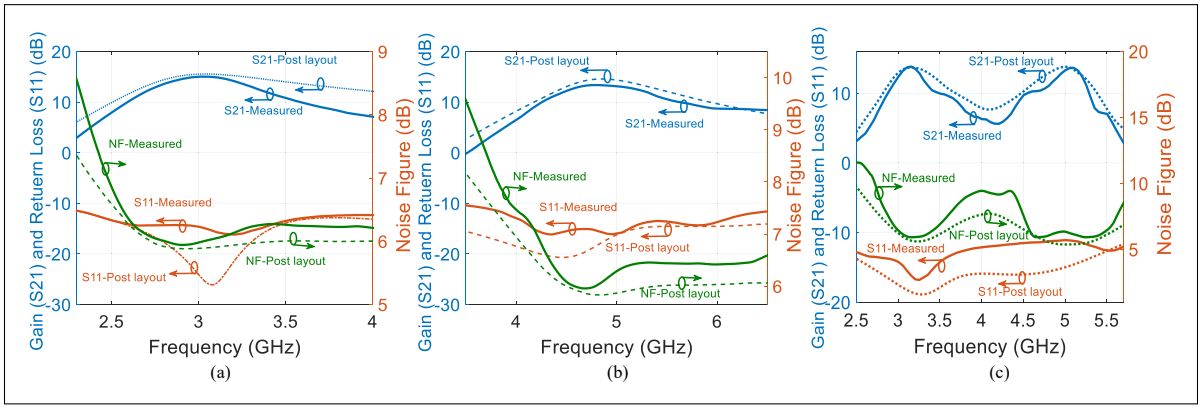

Figure 5.8 Measured and post-layout simulation results of the LNA gain (S21), input return loss (S11) and NF while operating in (a) band-1 mode (mode 1), (b) band-2 mode (mode 2) and (c) concurrent dual-band mode (mode 3)

The NF was measured by using a 346B Noise Source and an Agilent N9030A PXA signal analyzer. A Mini-Circuits ZX60-6013E-S+ amplifier was utilized before the signal analyzer in order to effectively remove the impact of the signal analyzer noise. The NF can be measured up to approximately 8 GHz because of the limited bandwidth of the amplifier. In the single-band modes, the LNA exhibits an NF of 5.9 dB and 6.1 dB at frequencies centered at 2.8 GHz and 4.8 GHz, respectively. In the concurrent dual-band mode, the NF is measured to be 6 dB and 6.3 dB in the low and high bands, respectively. Note that the measured S21 curves follow the shape of the simulated ones, however, the measured results are slightly lower than the post-layout simulated ones. The lower S21 is due to the AC coupling capacitors employed in the signal path and to RF losses at the FR-4 PCB-level. Moreover, the S21 bandwidth limitation is due to the packaging parasitics and PCB. The QFN package and PCB parasitics are attributed to the variations in the input matching and observed. Note that the measured input matching remains below -10 dB nonetheless.

Note that when SW1 and SW2 are set as 'ON' and 'OFF', respectively, M_2 is 'OFF', and thus there is no loading effects on M_1 and M_0 through M_2. Similarly, when SW1 and SW2 are set as 'OFF' and 'ON', respectively, M_1 is 'OFF', and thus there is no loading effects from M_1 on M_2 and M_0. However, when both SW1 and SW2 are 'ON', these cause a loading effect (parasitics resistance and capacitance) from M_2 on M_1 and vice versa. Parasitic resistance of SW1 and SW2 appears in series with L_{1A}, L_{1B},L_{2A}, and L_{2B} in the concurrent dual band mode, thus shifting the frequency. In addition, since both M_1 and M_2 are 'ON', the DC biasing in the concurrent dual- band mode is different from the two single-band modes, when only one of M_1 or M_2 is 'ON'.

The measured performance of the proposed differential LNA is compared to previously published multi-mode LNAs and the results are summarized in Table 5.2. The LNA circuits proposed in Singh, Slovin, Xu, Schlesinger, Bain & Paramesh (2017) and Chen & Wang (2017) operate on three single narrow bands and dual-band frequencies, respectively. Dual narrow-band operation is demonstrated in Singh *et al.* (2017) by employing a multi-tapped transformer

to save circuit area while consuming a peak power of 7.2 mW from a 1.2-V supply for the single-ended architecture. Comparatively, the proposed design features ultra-wide bands.

Table 5.2 Summary of the LNA performance and comparison to other works

Reference	Technology (nm)	Mode	Frequency (GHz)	S11 (dB)	S21 (dB)	NF (dB)	Power (mW)	Area (mm^2)
Singh *et al.* (2017)$^{\diamond}$	130+PC switch	Dual-Band	3 5	-12.5 -13.8	21.2 21.9	2.5 2.7	7.2 3.6	4*
Kumar, Dutta & Sahoo (2019)$^{\diamond}$	180	Three Narrow Bands	1.8	-11	14.1	8.5	2	1.44
			2.1	-12	14.5	8.2		
			2.4	-14	14.1	8.7		
		Wideband	2 - 5	<-10	14.5	8.6	3.8	
Chen & Wang (2017)$^{\diamond}$	180	Three Single-bands	2.4	<-12.5	10.6	4.96	3.6	0.64
			5.2	<-22.7	17.4	5.16		
			5.8	<-25	15.6	5.57		
This Work‡	130	Two Single-bands	2.8	<-10	14.8	5.9	10.4	0.64†
			4.8	<-10	13.4	6.1		
		Concurrent Dual-Band	3 5	<-10 <-10	13.7 13.6	6 6.3	11.3	

* Including two LNAs. $^{\diamond}$ Single-ended structure. ‡ Differential structure. † Active area.

Compared to single-ended LNAs, the design of a ultra-wideband differential LNA structure such as that proposed here is challenging because of the trade-off between power consumption, NF and area. Due to the doubled number of components, the differential structure typically occupies twice the area and dissipates twice the power of a single-ended structure. As can be seen in Table 5.2, the proposed differential multi-band LNA structure exhibits comparable performance in terms of S-parameters, operating frequency, NF, and area with respect to the other LNAs implemented, which are single-ended structures, indicating the potential of the proposed fully-differential LNA architecture. As expected, its differential nature causes it to exhibit higher power consumption.

5.4.1 IR-UWB Receiver Characterization

To verify the fabricated reconfigurable non-coherent IR-UWB receiver, an RF modulated OOK signal is generated with a Tektronix AWG7122C Arbitrary Waveform Generator (AWG), and is applied to the receiver RF input port. The measurement is carried out for the three modes: band-1 mode, band-2 mode and concurrent dual-band mode.

5.4.1.1 Single-Band Modes

In band-1 mode, the receiver operates as a conventional non-coherent IR-UWB receiver. Fig. 5.9 shows the transient measurement results of that mode, including the RF input modulated pulse, output of the LNA, and the BB amplifiers output. In Fig. 5.9(a), an OOK-modulated pulse at 2.8 GHz is applied to the RF input port of the receiver. The generated pulse has an 8 mV amplitude and 2 ns duration. As can be seen, the incoming modulated pulse is amplified by the LNA and the amplified envelope of the pulse is successfully extracted at the output of the BB amplifier.

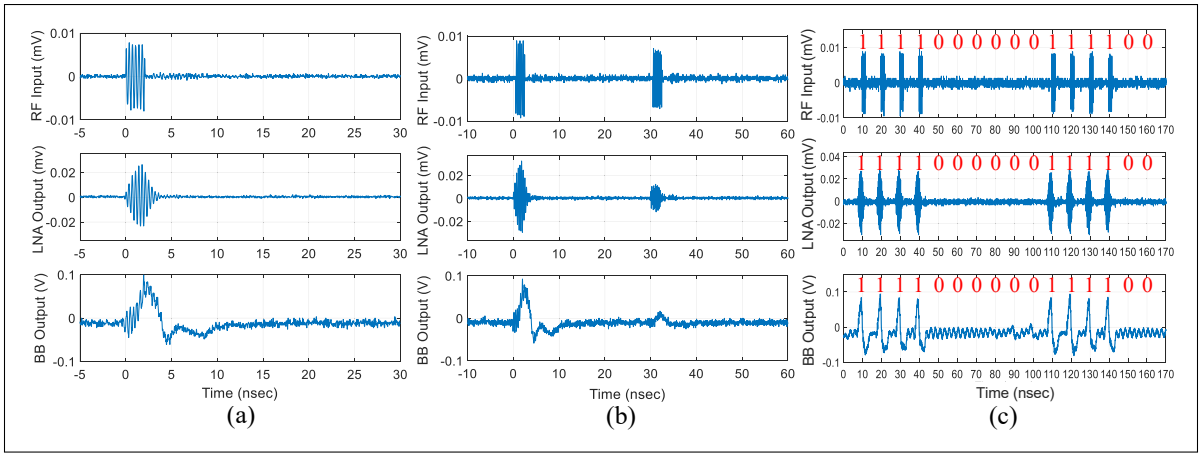

Figure 5.9 Measured operation of the IR-receiver operating in band-1 mode (a) applying one OOK-modulated pulse at 2.8 GHz, (b) applying two pulses at 2.8 GHz (first pulse) and 4.8 GHz (second pulse) and (c) applying a random OOK data stream

In Fig. 5.9(b), the receiver operating in band-1 mode is fed with two pulses, one at band-1 (2.8 GHz) and one at band-2 (4.8 GHz), which is out of the operating band of that mode. As can be seen, only the 2.8 GHz pulse is amplified by the LNA. It is then squared by using the $SQ - SB$ squarer, and its envelope is extracted by the LPF and amplified by the BB amplifiers. The second pulse at 4.8 GHz is suppressed, as expected.

Furthermore, to characterize the maximum achievable pulse rate, a long sequence of an OOK-modulated data stream of '1111000000111100' is applied to the receiver, as shown in Fig. 5.9(c). The '1' and '0' symbols are encoded by the presence and absence of a pulse, respectively. De-

spite the time interval of 10 ns between each incoming pulse (i.e. 100 Mbps, assuming one pulse per bit), the receiver is able to extract the envelope of the amplified squared signal at its output (see Fig. 5.9(c) bottom trace), verifying the capability of distinguishing the presence and absence of the OOK modulated signal.

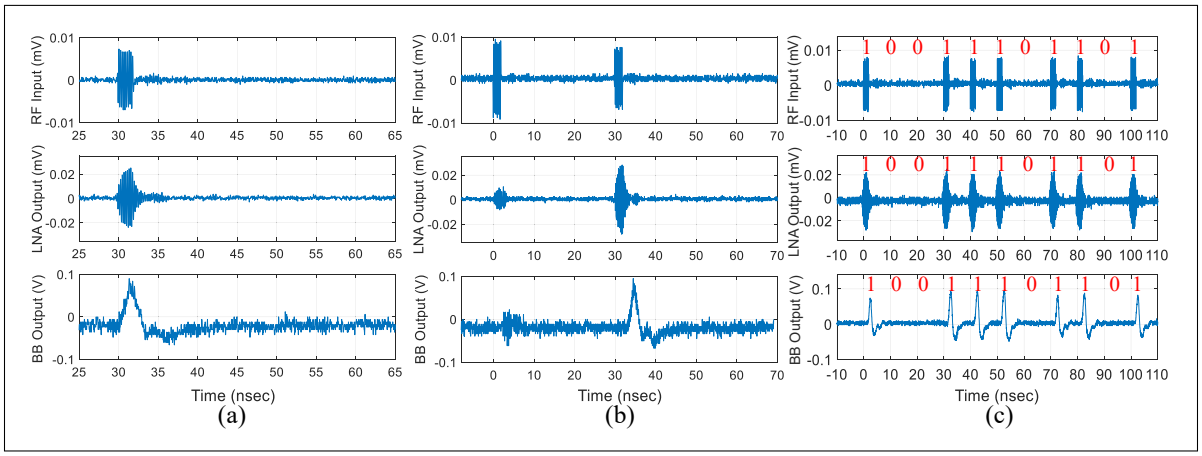

Figure 5.10 Measured operation of the IR-receiver operating in band-2 mode (a) applying one OOK-modulated pulse at 4.8 GHz, (b) applying two pulses at 2.8 GHz (first pulse) and 4.8 GHz (second pulse) and (c) applying a random OOK data stream

A similar scheme is carried-out for band-2 mode applying an OOK modulated pulse at band-2 (4.8 GHz) (Fig. 5.10(a)), feeding the LNA with two pulses at band-1 and band-2 (Fig. 5.10(b)), and applying a 100 Mbps OOK-modulated data sequence (Fig. 5.10(c)). As expected, the behavior is similar to the band-1 mode, with only the pulse at 4.8 GHz being amplified and squared, as seen in Fig. 5.10(a) and (b). Similarly to band-1 mode, Fig. 5.10(c) shows that the incoming data stream of '10011101101' is successfully extracted at the BB output, and it verifies the OOK data can be retrieved and demodulated at the receiver BB output at 100 Mbps.

5.4.1.2 Concurrent Dual-band Mode

In the concurrent dual-band mode, the receiver is able to cover two bands simultaneously. The receiver is fed with two RF pulses each at a different frequency: 3 GHz and 5 GHz. As shown in Fig. 5.11(a), the reconfigurable LNA amplifies the two incoming modulated pulses, simulta-

neously. Two pulse envelopes are extracted by squarers SQ_{CDBM1} and SQ_{CDBM2} and the LPF. The envelope signals are amplified by the BB amplifiers at the output of the receiver. As discussed in Section 5.2.2, if the incoming RF pulse is at 3 GHz, a pulse envelope with positive amplitude is extracted at the output of the receiver. Conversely, a pulse envelope with negative amplitude is extracted at the receiver output when the input RF pulse is at 5 GHz. This shows that the receiver can leverage binary FSK modulation as well as OOK modulation. Binary FSK modulation can provide advantages over OOK modulation with regards to robustness to interference Hsieh *et al.* (2016).

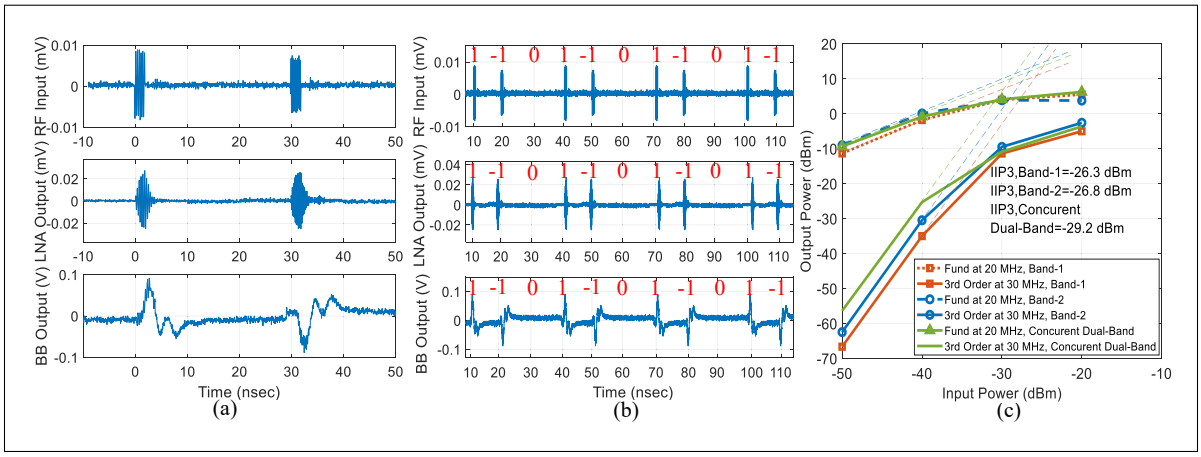

Figure 5.11 Measured waveforms of the IR-UWB receiver operating in the concurrent dual-band mode by (a) applying two RF pulses at 3 GHz and 5 GHz, (b) applying a binary FSK data stream that includes zeros, and (c) measured in-band IIP3 performance of the receiver for the three modes of operation

In addition, an FSK-modulated random data sequence at different frequencies of 3 GHz and 5 GHz is applied to the receiver, as shown in Fig. 5.11(b). There is a time interval of 10 ns between each incoming pulse. It should be mentioned that two RF pulses operating at 3 GHz and 5 GHz are marked by '1' and '-1', respectively. The figure also shows how OOK can be combined with FSK to create '0' symbols. Accordingly, at the baseband, the presence and absence of signal are distinguished by symbols of '1' ('-1') and '0', respectively. A positive BB output signal indicates an input RF pulse at 3 GHz, and a negative BB output signal designates

an RF pulse at 5 GHz (see Fig. 5.11(b)). The output response of the receiver ($V_{out1,BB}, V_{out2,BB}$) is sufficiently fast to preserve the distinctive features of the consecutive pulses.

Moreover, the receiver can operate with ternary signals (i.e., '1', '0' and '-1'), as evident by the added '0' symbols included in Fig. 5.11(b). The ternary signaling can be used using a 3-bit to 2-ternary pair (3B2T) to increase the bitrate by a factor of $1.5X$ ($1.33X$ can also be achieved using a 4B3T code) (De Wit *et al.* (2019); Morozov, Pilipko & Korotkov (2009)). This can also benefit analog to digital conversion of the signal by enhancing its power consumption due to better dynamic range properties of ternary analog to digital converters (Morozov *et al.* (2011)). A ternary sequence based IR-UWB system can be simultaneously used by different types of receivers, namely differential, coherent, and energy detectors such as the one proposed here (Coppens, De Poorter, Shahid, Lemey & Marshall (2022); Lee, Chin, Kwok, Wong & Niu (2009); Lei, Chin & Kwok (2006)). As such, the receiver in concurrent dual-band mode can handle information more densely than the single-band modes that feature binary signal detection. As a result, in the concurrent dual-band mode, the proposed receiver has the capability of decoding the frequency information of the received pulse at a 100 Mbps data rate in binary FSK or at 150 Mbps by leveraging ternary signaling, while operating at the same symbol rate, hence improving power efficiency. This can also be leveraged by reducing the symbol rate to 66.67 MHz in order to achieve 100 Mbps via ternary signalling. The resulting widened symbol time separation can benefit inter symbol interference robustness.

The measurement results demonstrate that the proposed reconfigurable IR-UWB receiver can demodulate pulses that can be modulated in OOK or binary FSK. It can also combine these modulations to enable ternary signaling in order to optimize the data transport efficiency or increase the maximal data rate.

5.4.1.3 Linearity

In-band linearity performance of the receiver is investigated for the two single-band modes and the concurrent dual-band mode at the frequency bands of interest, as shown in Fig. 5.11(c). Two

input tones at $f_1 = 10\,\text{MHz}$ and $f_2 = 20\,\text{MHz}$ offsets from the RF input frequency (depending on the operating mode) are injected to the input of the receiver. For example, when the receiver operates in the single-band mode at center frequencies of 2.8 GHz, the two input tones are located at 2.81 GHz and 2.82 GHz. Then, the input power of the two tones is swept from -50 to $-10\,\text{dBm}$. The IIP3 of the receiver for the three modes of operation is higher than $-30\,\text{dBm}$, as seen in Fig. 5.11(c). The IIP3 is measured to be of $-26.3\,\text{dBm}$, $-26.8\,\text{dBm}$ and $-29.2\,\text{dBm}$ for the band-1, band-2 and concurrent dual-band modes, respectively.

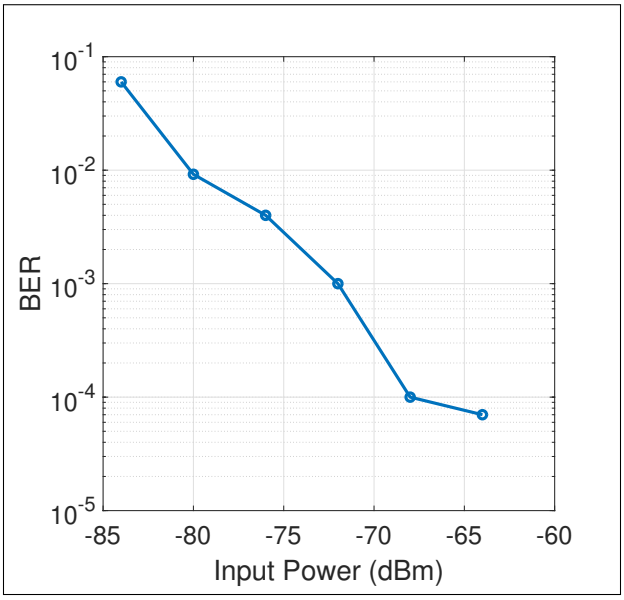

Figure 5.12 The measured BER performance vs receiver input power in the concurrent dual-band mode

To measure the receiver sensitivity, an R&S SMW200A signal generator was employed to set the power and the desired signal frequency. Then, the BER was measured by using an R&S FSW-signal and spectrum analyzer with a pseudorandom data waveform similar to that of Fig. 5.11(b). The input signal power was reduced by using an attenuator, while the BER performance was monitored. Fig. 5.12 depicts the measured BER versus input power in the concurrent dual-band mode. The measured receiver sensitivity at a BER of 10^{-3} was extracted to be of $-72\,\text{dBm}$ at a data rate of 150 Mbps.

5.4.1.4 Performance and Comparisons

In the single-band modes, the proposed receiver consumes 11.9 mW from a 1.2-V supply. The LNA, squarer SQ_{SB}, and BB amplifiers consume 10.4 mW, 0.47 mW and 1 mW (3×0.34 mW), respectively. In the concurrent dual-band mode, since both SW1 and SW2 of the LNA are ON and both squarers (SQ_{CDBM1} and SQ_{CDBM2}) are active, the receiver exhibits a slightly higher power consumption of 13.2 mW. Fig. 5.13 illustrates the power consumption breakdown of each operating mode.

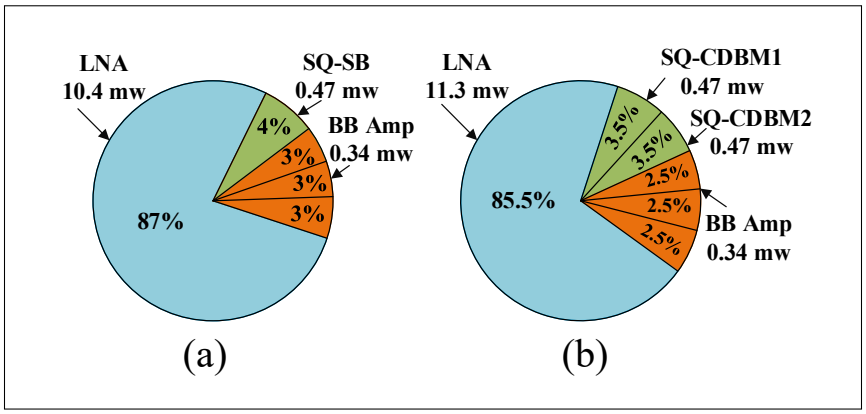

Figure 5.13 Power consumption breakdown in the (a) single-band modes and (b) concurrent dual-band mode

The overall performance of the fabricated multi-mode IR- UWB receiver proposed here is compared to previous published works in Table 5.3 in terms of operating frequency, data rate, sensitivity, power consumption, energy efficiency, and area. The architecture proposed in Geng *et al.* (2015); Vigraham & Kinget (2014) reports a 2 Mbps and 500 Mbps data rate with a power consumption of 11.66 mW and 5.9 mW, while operating at the 4.35 GHz and 7.25 −9.5 GHz, respectively. The proposed receiver in Lee *et al.* (2019a) achieves a −61 dBm sensitivity at 500 Mbps with a $10^{-}3$ BER and an energy efficiency of $55pJ/bit$ while operating over 3 −5 GHz and consuming 27.7 mW. In comparison, the proposed IR-UWB receiver architecture can operate at up to 150 Mbps with a sensitivity of −72 dBm and an energy efficiency of $88pJ/bit$. In this work, the RF incoming frequency information can be extracted according to the polarity of the BB output in the concurrent dual-band mode. Thus, the proposed architecture can achieve

dual mode data demodulation of OOK and binary FSK. This enables operation with ternary signaling by combining both modulations. It can do so without employing an additional oscillator. Ternary signaling can notably be beneficial to increase channel capacity or improve data transport efficiency by using encoding schemes such as 4B3T. It can also benefit analog to digital conversion.

Table 5.3 Summary of the IR-UWB receiver performance and comparison to other works

Ref.	Tech. (nm)	Freq. (GHz)	Data Rate (Mbps)	Modulation	Sensitivity (dBm)	Power (mW)	Area (mm^2)	RF Input	Architecture
Zhang *et al.* (2018b)	65	3-8	10	S-OOK	-64	6.4	0.01	Single-ended	Non-Coherent
Crepaldi *et al.* (2019)	130	3.5-4.5	1000	OOK	$-38^{\star\star}$	12	$0.34^{\star}$	Single-ended	Non-Coherent
Vigraham & Kinget (2014)	65	4.35	2	OOK	-76.5	11.66	$0.53^{\star}$	Single-ended	Non-Coherent
Geng *et al.* (2015)	65	7.25–9.5	500	OOK	-59	5.9	$2.25^{\diamond}$	Single-ended	Non-Coherent
Lee *et al.* (2019a)	65	3-5	500	D-MPPM	-61	27.7	$2.88^{\ddagger}$	Single-ended	Non-Coherent
This work	130	2.8-5	100/150†	OOK/FSK$^{\natural}$	-72	11.9* ,13.2 **	1.5	Differential	Non-Coherent

* Active area. $^{\diamond}$Including the receiver, transmitter and PLL. ** At a 10^{-3} packet error ratio. ‡ Including the receiver and transmitter. † 100 Mb/s data rate in the single-band mode and 150 Mb/s data rate in the concurrent dual-band mode by leveraging ternary signaling. $^{\natural}$ Ternary signaling is supported. * 11.9 mW in the single-band mode. ** 13.2 mW in the concurrent dual-band mode.

5.5 Conclusion

This paper demonstrated a 2.8 −5 GHz non-coherent IR-UWB receiver that supports OOK and binary FSK modulation. The proposed reconfigurable receiver uses an envelope detection architecture and achieves high data rate OOK and FSK demodulation, yielding a self-demodulating structure. The envelope detection architecture precludes the need to maintain the phase of the incoming pulses, reducing circuit complexity and power consumption. The design can be digitally reconfigured in three different modes of operation: two single-band modes and one concurrent dual-band mode. In the two single-band modes, the IR-UWB receiver is able to receive, amplify and demodulate the in-band OOK-modulated pulses, while rejecting the other band's pulses. In the concurrent dual-band mode, the frequency information can be extracted through the polarity of the differential BB output, enabling binary FSK demodulation in addition to OOK demodu-

lation. This enables ternary signaling to either optimize the data transport efficiency or increase the maximal data rate.

The proposed IR-UWB receiver was fabricated in 130 nm CMOS technology. The total power consumption of the receiver at a 100 Mb/s and 150 Mbps data rate is of 11.9 mW and 13.2 mW from a 1.2-V supply when operating in the single-band modes or concurrent dual-band mode by leveraging ternary signaling, respectively. The IR-UWB receiver represents an agile architecture that is able to support multiple pulse frequency ranges and OOK and FSK modulations without the size and complexity disadvantages originating from typical concurrent dual-band front-end architectures, and that benefits from the inherent properties of IR-UWB signals.

5.6 Appendix A

5.6.1 LNA Gain Analysis

The equivalent half-circuit of the proposed LNA is plotted in Fig. 5.14(a) when M_1 is ON and M_2 is OFF. Since the source of M_3 is grounded by C_{1A}, the LNA can be considered as a two-stage cascaded amplifier. The voltage gain of the equivalent half-circuit of the LNA is achieved by

$$\mathrm{A}_{V_{LNA}} = A_{V_{1st}} A_{V_{2nd,3rd}}, \tag{5.15}$$

where $A_{V_{1st}}$ and $A_{V_{2nd,3rd}}$ are the voltage gain of the CG stage and the second and third stages' voltage gain, respectively. $A_{V_{1st}}$ is given by

$$\begin{aligned}\mathrm{A}_{V_{1st}} = \frac{V_{d0}}{\frac{V_s}{2}} = g_{m,M_0}\left(\frac{1}{g_{m,M_1}} \| \frac{1}{C_{p1}s}\right)\times \\ \frac{\frac{1}{g_{m,M_0}} \| \frac{L_s}{2}s \| \frac{1}{C_{p0}s}}{\frac{R_S}{2} + \frac{1}{C_1 s} + \frac{1}{g_{m,M_0}} \| \frac{L_s}{2}s \| \frac{1}{C_{p0}s}},\end{aligned} \tag{5.16}$$

where g_{m,M_0}, g_{m,M_1} ,C_{p0}, C_{p1}, and R_S are the transconductance of M_0, the transconductance of M_1, the source parasitic capacitance generated from M_0, the drain and source parasitic capaci-

tance caused by M_0 and M_1, and the input source resistance of 50 Ω, respectively. Note that the channel resistance of the transistors, r_o, are ignored for simplicity.

$A_{V_{2nd,3rd}}$ can be expressed as

$$\begin{aligned} \mathrm{A}_{V_{2nd,3rd}} &= \frac{V_{out1,LNA}}{V_{g3}}\frac{V_{g3}}{V_{d1}}\frac{V_{d1}}{V_{d0}} = -(\frac{L_d}{2}s||\frac{1}{C_{p4}s})g_{m,M_3}\times \\ &\frac{C_{3A}}{C_{3A}+C_{p3}}\times g_{m,M_1}(L_{1A}||\frac{1}{C_{p2}}||(\frac{1}{C_{3A}}+\frac{1}{C_{p3}})), \end{aligned} \tag{5.17}$$

where g_{m,M_3}, C_{p2}, C_{p3}, and C_{p4} are the transconductance of M_3, the total parasitic capacitance at the drain of M_1, the parasitic capacitance at the gate of M_3, and the drain parasitic capacitance caused by M_3, respectively.

5.6.2 LNA Noise Analysis

This section performs a detailed noise analysis of the proposed LNA. The noise equivalent circuits of the LNA are shown in Fig. 5.14(b) and (c). Note that noise performance is predominantly affected by transistor M_0. In the proposed LNA, the main thermal noise sources generated from the source resistor R_s ($\overline{V_{n,S}^2}$) and the channel noise of M_0, M_1, and M_3 ($\overline{i_{n,M_0}^2}$, $\overline{i_{n,M_1}^2}$, and $\overline{i_{n,M_3}^2}$) are expressed as

$$\overline{\mathrm{V}_{\mathrm{n,S}}^2} = 4kTR_S\Delta f, \tag{5.18}$$

$$\overline{\mathrm{i}_{\mathrm{n,M_i}}^2} = 4kT\gamma g_{m,M_i}\Delta f,\ i = 0, 1, 3, \tag{5.19}$$

where $k = 1.38\times10^{-23}J/K$, T, Δf, and γ denote the Boltzmann constant, the absolute temperature, the noise bandwidth, and the excess noise coefficient that is equal to $\frac{2}{3}$ for long-channel transistors and rises to 2 in short-channel transistors, respectively. Since the operating frequency of the proposed LNA is higher than 2 GHz, the $1/f$ noise can be ignored. In addition, it is assumed $\Delta f = 1$ Hz.

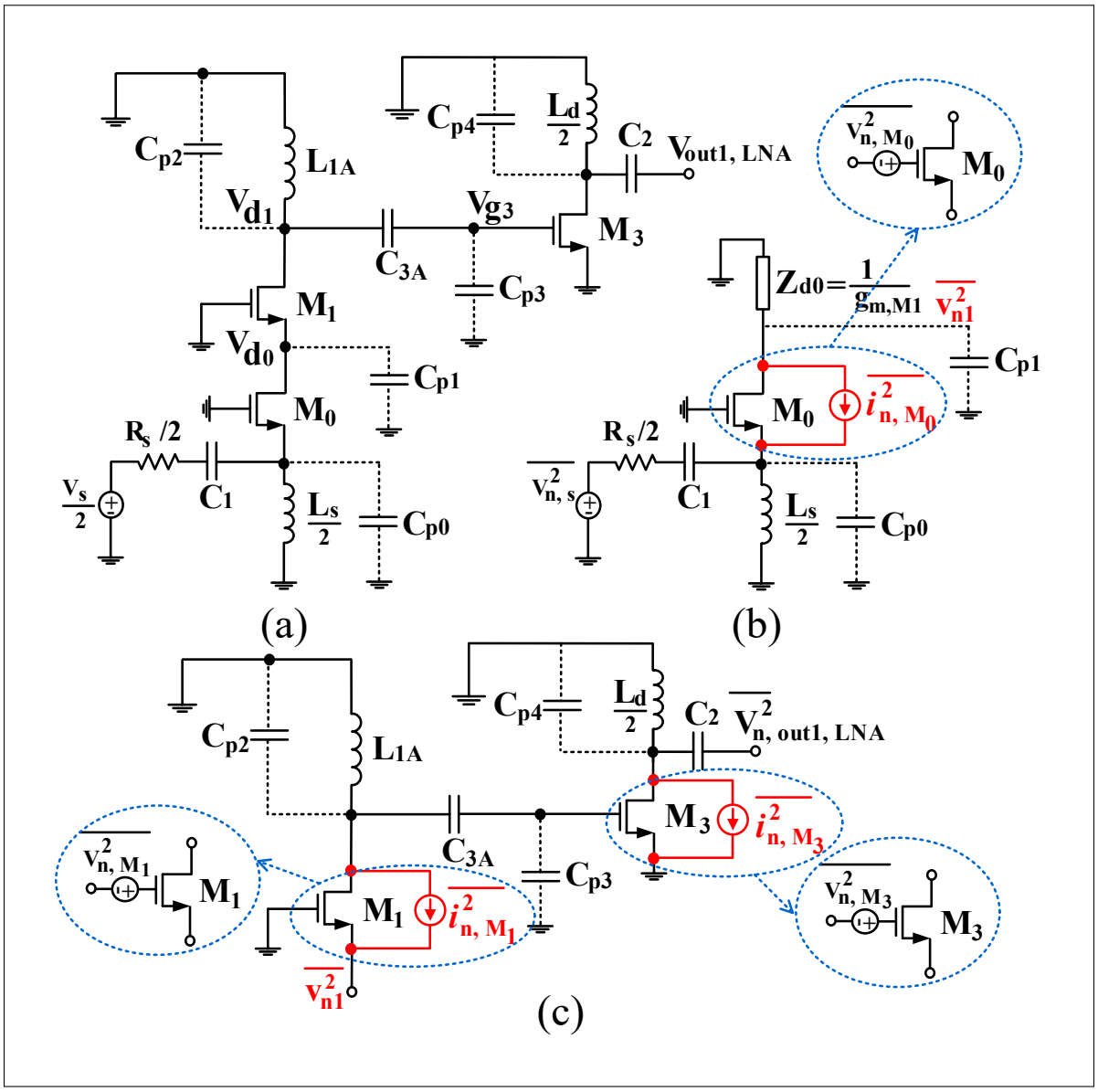

Figure 5.14 (a) Equivalent half-circuit of the proposed LNA, (b) the noise equivalent circuit of the first stage, and (c) the noise equivalent circuit of the second and third stages

As shown in Fig. 5.14(b),the total mean-square noise voltage at the CG stage's output ($\overline{V_{n1}^2}$) can be expressed as

$$\overline{V_{n1}^2} = \overline{V_{n1,R_S}^2} + \overline{V_{n1,M_0}^2}, \tag{5.20}$$

where $\overline{V^2_{n1,R_S}}$ and $\overline{V^2_{n1,M_0}}$ are the generated output noise of the CG stage by $\overline{V^2_{n,S}}$ and $\overline{i^2_{n,M_0}}$, respectively. The first stage's gain ($A_{V_{1st}}$) amplifies the $\overline{V^2_{n,S}}$. Thus, $\overline{V^2_{n1,R_S}}$ is given by

$$\overline{\mathrm{V^2_{n1,R_S}}} = (A_{V_{1st}})^2\overline{V^2_{n,S}}. \tag{5.21}$$

The channel noise of M_0 ($\overline{i^2_{n,M_0}}$) is modeled by a current source (see Fig. 5.14(b)). $\overline{i^2_{n,M_0}}$ can alternatively be modeled by a voltage source in series with the gate ($\overline{V^2_{n,M_0}} = \overline{i^2_{n,M_0}}/g^2_{m,M_0}$) (see Fig. 5.14(b)). Thus, multiplying $\overline{V^2_{n,M_0}}$ by the voltage gain from the gate to the output of M_0 yields $\overline{V^2_{n1,M_0}}$ that is given by

$$\overline{\mathrm{V^2_{n1,M_0}}} = [\frac{g_{m,M_0}(\frac{1}{g_{m,M_1}}||\frac{1}{C_{p1}s})}{1+g_{m,M0}((\frac{R_S}{2}+\frac{1}{C_1 s})||\frac{L_s}{2}s||\frac{1}{C_{p1}s})}]^2\frac{\overline{i^2_{n,M_0}}}{g^2_{m,M_0}}. \tag{5.22}$$

According to (5.20)-(5.22), $\overline{V^2_{n1}}$ can be given by

$$\begin{aligned}\overline{\mathrm{V^2_{n1}}} &= (A_{V_{1st}})^2\overline{V^2_{n,S}}+\\ &[\frac{g_{m,M_0}(\frac{1}{g_{m,M_1}}||\frac{1}{C_{p1}s})}{1+g_{m,M0}((\frac{R_S}{2}+\frac{1}{C_1 s})||\frac{L_s}{2}s||\frac{1}{C_{p1}s})}]^2\frac{\overline{i^2_{n,M_0}}}{g^2_{m,M_0}}.\end{aligned} \tag{5.23}$$

Similarly, the channel noise of M_1 and M_3 is modeled by voltage sources $\overline{V^2_{n,M_1}} = \overline{i^2_{n,M_1}}/g^2_{m,M_1}$ and $\overline{V^2_{n,M_3}} = \overline{i^2_{n,M_3}}/g^2_{m,M_3}$ in series with the gate of M_1 and M_3, respectively (see Fig. 5.14(c)). The total mean-square noise voltage at the third stage's output ($\overline{V^2_{n,out1,LNA}}$) is given by

$$\overline{\mathrm{V^2_{n,out1,LNA}}} = \overline{V^2_{n,1st}} + \overline{V^2_{n,2nd}}, \tag{5.24}$$

where $\overline{V^2_{n,1st}}$ and $\overline{V^2_{n,2nd}}$ are the generated output noise from $\overline{V^2_{n1}}$ and the sum of $\overline{V^2_{n,M_1}}$ and $\overline{V^2_{n,M_3}}$, respectively. $\overline{V^2_{n,1st}}$ is achieved by multiplying $\overline{V^2_{n1}}$ with the second and third stages' gain ($A_{V_{2nd,3rd}}$), which can be expressed by

$$\overline{\mathrm{V}^2_{\mathrm{n,1st}}} = (A_{V_{2nd,3rd}})^2\overline{V^2_{n1}}. \tag{5.25}$$

$\overline{V^2_{n,2nd}}$ is expressed by multiplying $\overline{V^2_{n,M_1}}$ by $A_{V_{2nd,3rd}}$ and multiplying $\overline{V^2_{n,M_3}}$ by the third stage's voltage gain. Thus, $\overline{V^2_{n,2nd}}$ is expressed by

$$\overline{\mathrm{V}^2_{\mathrm{n,2nd}}} = (A_{V_{2nd,3rd}})^2\frac{\overline{i^2_{n,M_1}}}{g^2_{m,M_1}} + [(\frac{L_d}{2}s||\frac{1}{C_{p4}s})g_{m,M_3}]^2\frac{\overline{i^2_{n,M_3}}}{g^2_{m,M_3}}. \tag{5.26}$$

According to (5.24)-(5.26), $\overline{V^2_{n,out1,LNA}}$ is given by

$$\begin{aligned}\overline{\mathrm{V}^2_{\mathrm{n,out1,LNA}}} &= (A_{V_{2nd,3rd}})^2[\overline{V^2_{n1}} + \frac{\overline{i^2_{n,M_1}}}{g^2_{m,M_1}}]+ \\ &[(\frac{L_d}{2}s||\frac{1}{C_{p4}s})g_{m,M_3}]^2\frac{\overline{i^2_{n,M_3}}}{g^2_{m,M_3}}.\end{aligned} \tag{5.27}$$

By substituting (5.23) into (5.27), $\overline{V^2_{n,out1,LNA}}$ can be shown to be given by

$$\begin{aligned}\overline{\mathrm{V}^2_{\mathrm{n,out1,LNA}}} &= (A_{V_{2nd,3rd}})^2[(A_{V_{1st}})^2\overline{V^2_{n,S}}+ \\ &[\frac{g_{m,M_0}(\frac{1}{g_{m,M_1}}||\frac{1}{C_{p1}s})}{1+g_{m,M0}((\frac{R_S}{2}+\frac{1}{C_1 s})||\frac{L_s}{2}s||\frac{1}{C_{p1}s})}]^2\frac{\overline{i^2_{n,M_0}}}{g^2_{m,M_0}} + \frac{\overline{i^2_{n,M_1}}}{g^2_{m,M_1}}]+ \\ &[(\frac{L_d}{2}s||\frac{1}{C_{p4}s})g_{m,M_3}]^2\frac{\overline{i^2_{n,M_3}}}{g^2_{m,M_3}}.\end{aligned} \tag{5.28}$$

By substituting (5.28) into (5.7), the noise factor of the LNA in the single-band modes is derived.

In the concurrent dual-band mode, since both SW1 and SW2 of the LNA are ON, the noise contributed by transistors M_3 and M_4 should be considered in (5.8). Thus, $\overline{V^2_{n,2nd}}$ in (5.24) is the generated output noise from the sum of $\overline{V^2_{n,M_1}}$, $\overline{V^2_{n,M_3}}$, $\overline{V^2_{n,M_2}}$, $\overline{V^2_{n,M_4}}$, and can be expressed by

$$\overline{\mathrm{V}^2_{\mathrm{n,2nd}}} = (A_{V_{2nd,3rd_{SW1}}})^2 \frac{\overline{i^2_{n,M_1}}}{g^2_{m,M_1}} + [(\frac{L_d}{2}s||\frac{1}{C_{p4}s})g_{m,M_3}]^2 \frac{\overline{i^2_{n,M_3}}}{g^2_{m,M_3}} + (A_{V_{2nd,3rd_{SW2}}})^2 \frac{\overline{i^2_{n,M_2}}}{g^2_{m,M_2}} + [(\frac{L_d}{2}s||\frac{1}{C_{p4}s})g_{m,M_4}]^2 \frac{\overline{i^2_{n,M_4}}}{g^2_{m,M_4}}. \tag{5.29}$$

It should be mentioned that C_{p4} in (5.29) is the total parasitic capacitance of the drain of M_3 and M_4. Note that $\overline{V^2_{n,1st}}$ in (5.24) in the concurrent dual-band mode can be achieved by multiplying $\overline{V^2_{n1}}$ with the second and third stages' gain of $A_{V_{2nd,3rd_{SW1}}}$ and $A_{V_{2nd,3rd_{SW2}}}$, which can be expressed by

$$\overline{\mathrm{V}^2_{\mathrm{n,1st}}} = (A_{V_{2nd,3rd_{SW1}}})^2\overline{V^2_{n1}} + (A_{V_{2nd,3rd_{SW2}}})^2\overline{V^2_{n1}}. \tag{5.30}$$

Thus, $\overline{V^2_{n,out1,LNA}}$ in the concurrent dual-band mode is achieved by substituting (5.30) and (5.29) into (5.24).

5.7 Appendix B

5.7.1 Squarer Conversion Gain Analysis

The differential voltage conversion gain of the squarer shown in Fig. 5.5 is given by

$$\mathrm{A}_{SQ} = \frac{V_{out1,SQ} - V_{out2,SQ}}{v_{rf+} - v_{rf-}}. \tag{5.31}$$

To simplify the analysis and due to the fully differential and symmetric architecture, the conversion gain is calculated for the half-circuit of the squarer. Thus, $V_{out1,SQ}$ is expressed as

$$\mathrm{V}_{out1,SQ} = R_{OUT+} \times i_{OUT+}, \tag{5.32}$$

where R_{OUT+} is the output resistance seen from node A. i_{OUT+} in (5.32) is given by

$$\begin{aligned} &i_{OUT+} = i_{ds,M_9} + i_{ds,M_{11}} = \\ &g_{m,M_9}(v_{rf+} - V_{s,M_9}) + g_{m,M_{11}}(v_{rf-} - V_{s,M_{11}}). \end{aligned} \tag{5.33}$$

Since $v_{rf-} = -v_{rf+}$ and $V_{s,M_{11}} = -V_{s,M_9}$, (5.32) can be written as

$$i_{OUT+} = 2g_{m,M_9}(v_{rf+} - V_{s,M_9}), \tag{5.34}$$

where V_{s,M_9} is the source voltage of M_9, and is expressed by

$$\begin{aligned} &\mathrm{V}_{s,M_9} = i_{ds,M_7} \times \\ &[r_{o,M_7} || \frac{1}{C_{p0}} || (\frac{r_{o,M_9} + R_A}{1 + g_{m,M_9} r_{o,M_9}}) || (\frac{r_{o,M_{10}} + R_B}{1 + g_{m,M_{10}} r_{o,M_{10}}})]. \end{aligned} \tag{5.35}$$

Since the squarer employs a fully differential and symmetric architecture, R_A is equal to R_B. In addition, M_9, M_{10}, M_{11}, and M_{12} have the same size and biasing, thus, they have the same g_m ($g_{m,M_9} = g_{m,M_{10}} = g_{m,M_{11}} = g_{m,M_{12}}$) and r_o ($r_{o,M_9} = r_{o,M_{10}} = r_{o,M_{11}} = r_{o,M_{12}}$). Therefore, (5.34) can be written as

$$\mathrm{V}_{s,M_9} = i_{ds,M_7}[r_{o,M_7} || \frac{1}{C_{p0}} || \frac{1}{2} (\frac{r_{o,M_9} + R_A}{1 + g_{m,M_9} r_{o,M_9}})]. \tag{5.36}$$

where i_{ds,M_7} is given by

$$i_{ds,M_7} = g_{m,M_7} v_{rf+}, \tag{5.37}$$

By substituting (5.37) into (5.36) and (5.36) into (5.34), the output current of i_{OUT+} can be shown to be given by

$$
\begin{aligned}
i_{OUT+} &= 2g_{m,M_9}(v_{rf+}- \\
&[r_{o,M_7}||\frac{1}{C_{p0}}||\frac{1}{2}(\frac{r_{o,M_9}+R_A}{1+g_{m,M_9}r_{o,M_9}})] \times g_{m,M_7}v_{rf+}).
\end{aligned}
\tag{5.38}
$$

By substituting (5.38) into (5.32), $V_{out1,SQ}$ can be written as

$$
\begin{aligned}
\mathrm{V}_{out1,SQ} &= R_{OUT+} \times 2g_{m,M_9}(v_{rf+}- \\
&[r_{o,M_7}||\frac{1}{C_{p0}}||\frac{1}{2}(\frac{r_{o,M_9}+R_A}{1+g_{m,M_9}r_{o,M_9}})] \times g_{m,M_7}v_{rf+}),
\end{aligned}
\tag{5.39}
$$

where the output resistance of R_{OUT+} is given by

$$
\begin{aligned}
\mathrm{R}_{OUT+} &= R||\frac{1}{C_{p1}}||\frac{1}{C_1}||(r_{o,M_9}+[r_{o,M_7}||(\frac{r_{o,M_{10}}+R_B}{1+g_{m,M_{10}}r_{o,M_{10}}})] \\
&+ g_{m,M_9}r_{o,M_9}[r_{o,M_7}||(\frac{r_{o,M_{10}}+R_B}{1+g_{m,M_{10}}r_{o,M_{10}}})]).
\end{aligned}
\tag{5.40}
$$

Thus, the conversion gain of squarer, (5.14), is achieved by substituting (5.40) into (5.39).

CONCLUSION AND RECOMMENDATIONS

Research Summary and contributions

This thesis aimed to study, design, and characterize innovative approaches toward the development of four different wideband RF receiver front-ends architectures for various emerging applications at sub-6 GHz frequencies. These touched applications related to 5G NR, Wi-Fi 6E and IR-UWB. To support next-generation communication systems, these innovative RF front-end architectures have overcome many inherent challenges to wideband receivers and provide state-of-the-art performance for emerging wideband applications.

The first contribution of this dissertation was the presentation of the analysis, design, and comparison of 4-, 8- and 16-path filter-based harmonic selection RF receiver front-end architectures, operating at $5.7-7.2$ GHz. When considering the design challenges related to the N-path filter, including the number of switches, power consumption of the LO phases generation circuitry, and NF performance, it is shown that an 8-path switching filter system is preferred to provide a suitable trade-off between the harmonic fold back effects, NF, circuit area and power consumption.

The second contribution of this thesis is the presentation of a blocker-tolerant harmonic selection receiver front-end that can be reconfigured to select the first LO harmonic at the low frequency band ($0.5-1.9$ GHz) and the third harmonic of the switching frequency at the high frequency band ($1.95-6$ GHz). The receiver has been designed and verified in 130 nm TSMC CMOS technology and has been successfully tested.

The third contribution is the presentation of two different wideband noise-canceling harmonic selection RF receiver architectures that are able to tolerate LO harmonic blockers without sacrificing noise performance and alleviate the SAW pre-filters requirement, while the LO clock generator consumes low power. Both receivers have been implemented in TSMC 65 nm CMOS

and measurement results from a fabricated prototype verify the merits of this work in balancing the HRR, linearity, and NF with power and area. Since driving the switches of the conventional 8-path filter and harmonic rejection 8-path switching filter requires to design of the multi-phase clock generator, PLL and oscillator, it increases the dynamic power consumption even in 28 nm CMOS. For these reasons, we also investigated the design a non-coherent IR-UWB receiver that can be amenable to much lower power applications, and thus complement the wideband receivers proposed.

Accordingly, the fourth contribution of this dissertation was the presentation of a low-power reconfigurable dual-band non-coherent IR-UWB receiver that can be digitally reconfigured in different operating frequency modes and employs a self-demodulating direct conversion RF front-end architecture with an OOK modulation scheme in addition to supporting data modulated in binary FSK. It also uniquely supports ternary signaling by combining both OOK and FSK modulations, and thus achieves a higher data rate and improved efficiency.

Discussion and Recommendations

Several recommendations can be made to continue the work started during this doctorate. The recommendations presented here relate both to the harmonic selection receiver designs and the creation of new IR-UWB structures and systems.

In this dissertation, the use of an N-path switching filter is mathematically analyzed to demonstrate how the harmonic recombination stage is reconfigured at the baseband to select the third harmonic of the LO switching frequency in addition to the fundamental in order to reduce the input frequency and power consumption of the multi-phase clock generator by a factor of three. Moreover, it has been demonstrated how the first and third harmonic selection N-path switching filters with resistive coefficients can be reconfigured to suppress the harmonic blockers at the input node of the front-end. The proposed RF receiver architectures allow exploring a high

frequency spectrum over 3 GHz, thanks to the higher order LO harmonic selection scheme. The presented harmonic selection RF receiver and noise-canceling architectures require eight clock phases and a harmonic recombination stage at the G_m-cell baseband. In addition, more than 40 % of DC power consumption of the whole receiver is assigned to the BB harmonic recombination blocks.

The first set of recommendations concerns the design of a low phase noise LO signal generator to reduce reciprocal mixing. The main issue in a wideband RF receiver is the reciprocal mixing of LO phase noise. Assuming that the receiver uses a perfectly linear down-conversion N-path switching filter and is free from gain compression, a significant amount of noise in the receiver band can originate from the reciprocal mixing. To mitigate the reciprocal mixing issue, a phase noise cancellation technique can be investigated in future work Wu *et al.* (2015). In addition, the generated multi-phase LO clocks should be sharp enough to mitigate the different threshold voltage effects for different corners. Therefore, a variable bias voltage can be employed through a replica transistor to track the switching transistors.

The second set of recommendations is to alleviate the requirement for the BB harmonic recombination stages by employing harmonic rejection multi-phase LO signals. To do this, there is a need to design a multi-phase LO clock generation with the given pulse width (PW) and time-delay (T_{delay}). Assuming that a 6-phase LO signal has a time-delay of $T_{delay} = T_s/6$ with respect to the first path clock and the pulse width in each path was equal to $T_s/8$; if these 6-phase clocks are differentially combined together, it is possible to select the third-order LO harmonic and suppress the other unwanted harmonics. This concept is depicted in figure 6.1 for $f_{LO} = 2$ GHz. When the 6-path switching filter is derived by 6-phase LO clocks with a pulse width of $T_s/8$ and time-delay of $T_{delay} = T_s/6$, the output of the 6-path switching filter contains the third-order LO harmonic. The normalized rejection at the even and first harmonics is illustrated in figure 6.1(b).

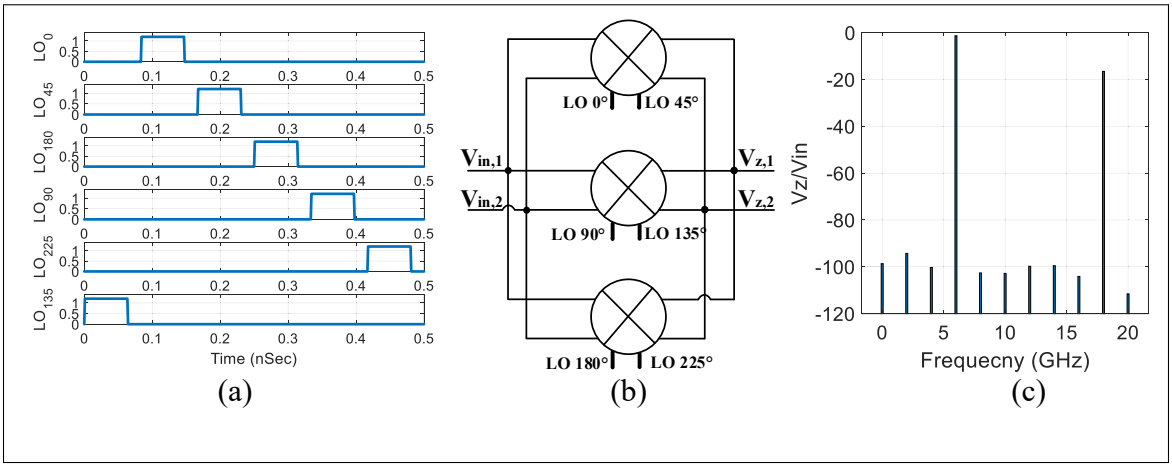

Figure 6.1 (a) 6-phase clock with $PW = T_s/8$ and $T_{delay} = T_s/6$, and (b) LO harmonic of the 6-phase clocks

Note that the LO clock period in this technique is divided by integer numbers (e.g., $PW = T_s/8$ and $T_{delay} = T_s/6$), and it can be accurately generated by employing delay-locked loops (DLL) and delay lines. It should be mentioned that the number of paths in the N-path switching filter, T_{delay}, and PW of LO clocks play an important role in the harmonic rejection ratio and harmonic folding back effects. This technique will help to cancel the need of the BB harmonic recombination blocks. Thus, it considerably saves the DC power consumption and alleviates the complexity of the receiver architecture. Therefore, it would be interesting to study the possibility of harmonic rejection offered by a non-overlapping clocks strategy.

A portion of the power consumption of the N-path switching filter-based designs in this dissertation is coming from driving the NMOS switches. Power consumption is always important for wideband communication devices since the power budget is limited. The power can be saved by employing a self-demodulating direct conversion IR-UWB front-end architecture with an OOK modulation scheme. The presented OOK and binary FSK non-coherent IR-UWB receiver removed the need for a PLL and oscillator, and thus saved more power.

The third set of recommendations concerns the implementation of an ultra low power IR-UWB receiver by employing the wake-up mechanism to reduce power dissipation during idle times. Since the receiver's power consumption at higher frequencies may be high, wake-up receivers can be a solution to save more power. The wake-up architectures continuously monitor the channel for requests to activate the receiver. These receivers can automatically determine whether the RF signal is present or not. Then, the receiver is powered down or up based on the received bit. Moreover, the receiver can achieve multi-mode demodulation schemes according to the sleep and/or wake up modes.

Contributions

The main contributions of the research work carried out and presented in this thesis are as follows:

A new RF receiver front-end architecture based on an N-path switching filter to select the 3^{rd} harmonic of switching frequency

This contribution was published in a scientific journal: *N. Shams and F. Nabki, "Analysis and comparison of low-power 6-GHz N-path-filter-based harmonic selection RF receiver front-end architectures," IEEE Transactions on Very Large Scale Integration (VLSI) Systems, vol. 30, no. 3, pp. 253-266, March 2022.* and was presented in CHAPTER 2.

A blocker-tolerant inductor-Less RF wideband receiver front-end based on the 1^{st} and 3^{rd} harmonic selection scheme

This second contribution was accepted in a scientific journal: *N. Shams and F. Nabki, "A blocker-tolerant inductor-Less RF wideband receiver front-end based on the 1^{st} and 3^{rd} harmonic selection scheme," IEEE Transactions on Very Large Scale Integration (VLSI) Systems*, and was presented in CHAPTER 3.

Two RF wideband receiver architectures using the resistive harmonic selection switching filter and noise-canceling technique

This third contribution was submitted in a scientific journal: *N. Shams and F. Nabki, "Two RF wideband receiver architectures using the resistive harmonic selection switching filter and noise-canceling technique," IEEE Journal of Solid-State Circuits (JSSC)*, and was presented in CHAPTER 4.

A reconfigurable dual-band non-coherent IR-UWB receiver supporting ternary signaling in addition to OOK and Binary FSK modulations schemes

This fourth contribution was submitted in a scientific journal: *N. Shams, A. Pourvali Kakhki, M. Nabavi and F. Nabki, "A reconfigurable dual-band non-coherent IR-UWB receiver supporting ternary signaling in addition to OOK and Binary FSK modulations schemes," IEEE Transactions on Very Large Scale Integration (VLSI) Systems*, and was presented in CHAPTER 5.

Academic achievements

During this doctorate, several academic achievements were obtained. These have been separated into two distinct categories: Peer-reviewed journal articles, and Peer-reviewed conference articles. They are presented below.

Journal articles with peer review:

1. "Analysis and comparison of low-power 6-GHz N-path-filter-based harmonic selection RF receiver front-end architectures," by N. Shams and F. Nabki, IEEE Transactions on Very Large Scale Integration (VLSI) Systems, vol. 30, no. 3, pp. 253-266, March 2022.

2. ”Blocker-Tolerant Inductor-Less Harmonic Selection Wideband Receiver Front-End for 5G Applications,” by N. Shams and F. Nabki, submitted to IEEE Transactions on Very Large Scale Integration (VLSI) Systems, (accepted on the 13^{th} of November 2022).

3. ”A Blocker Tolerant Harmonic Selection Noise-Cancelling RF Receiver for 5G and Wi-Fi 6E Applications,” by N. Shams and F. Nabki, submitted to IEEE Journal of Solid-State Circuits (JSSC) (submitted on the 14^{th} of November 2022).

4. ”An OOK and Binary FSK Reconfigurable Dual-Band Non-Coherent IR-UWB Receiver Supporting Ternary Signaling,” by N. Shams, A. Pourvali Kakhki, M. Nabavi and F. Nabki, submitted in: IEEE Transactions on Very Large Scale Integration (VLSI) Systems (submitted on the 1^{st} of November 2022).

Conference papers with peer review:

1. ”A noise-cancelling harmonic selection receiver using an N-path filter for 5G applications,” by N. Shams and F. Nabki, in 2021 19th IEEE International New Circuits and Systems Conference (NEWCAS), 2021, pp. 1-4: IEEE.

2. ”A wideband RF receiver using a harmonic rejection N-path notch filter for 5G applications,” by N. Shams and F. Nabki, in 2021 19th IEEE International New Circuits and Systems Conference (NEWCAS), 2021, pp. 1-4: IEEE.

3. ”A 6 GHz 130 nm CMOS harmonic recombination RF receiver front-end using n-path filtering,” by N. Shams, A. Abbasi, and F. Nabki, in 2020 18th IEEE International New Circuits and Systems Conference (NEWCAS), 2020, pp. 58-61: IEEE.

4. ”A 3.5 to 7 GHz Wideband Differential LNA with g m Enhancement for 5G Applications,” by N. Shams, A. Abbasi, and F. Nabki, in 2020 18th IEEE International New Circuits and Systems Conference (NEWCAS), 2020, pp. 230-233: IEEE.

5. ”A low-power wideband receiver front-end for NB-IoT applications,” by A. Abbasi, N. Shams, A. P. Kakhki, and F. Nabki, in 2020 18th IEEE International New Circuits and Systems Conference (NEWCAS), 2020, pp. 50-53: IEEE.

6. ”A 0.8-3.4 GHz, low-power and low-noise RF-to-BB-Current-Reuse receiver front-end for wideband local and wide-area IoT applications,” by A. Abbasi, N. Shams, and F. Nabki, in 2020 27th IEEE International Conference on Electronics, Circuits, and Systems (ICECS), 2020, pp. 1-4: IEEE.

7. ”Reconfigurable IR-UWB current mode switched receiver for IoT applications,” by N. Shams, A. P. Kakhki, and F. Nabki, in 2019 26th IEEE International Conference on Electronics, Circuits, and Systems (ICECS), 2019, pp. 9-12: IEEE.

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