An Efficiency-enhanced Power Combining and Recycling Network for LINC Power Amplifiers

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Un réseau de combinaison et de recyclage de puissance à efficacité améliorée pour l'amplificateur de puissance

Jinmei YANG

RÉSUMÉ

L'amplification linéaire à l'aide de composants non linéaires (LINC) est l'une des différentes méthodes permettant d'obtenir une efficacité d'amplificateur de puissance élevée et, en même temps, de présenter une bonne linéarité. Dans cette méthode, deux signaux modulés en phase à amplitude constante, amplifiés respectivement par deux amplificateurs de puissance à haute efficacité identiques, sont additionnés pour obtenir une amplification de puissance. Cependant, lors de la combination des signaux au moyen d'un dispositif telle que le combinateur Wilkinson, l'énergie se dissipe sous forme de chaleur à travers la résistance d'isolement. Ce mémoire étudie la conception et la mise en œuvre d'un combinateur de puissance Wilkinson modifié pour les amplificateurs de puissance LINC. L'objectif est d'augmenter l'efficacité énergétique de l'amplificateur de puissance LINC en recyclant la puissance généralement dissipée sous forme de chaleur dans la résistance.

Le travail comprend des conceptions distinctes pour trois composants; (i) un combineur Wilkinson traditionnel, (ii) un Balun et (iii) un redresseur de recyclage de puissance. Un réseau de sommation de puissance RF et de recyclage de puissance RF est formé en intégrant trois composants, dont les performances globales sont mesures.

La conception et la simulation sont réalisées pour le combinateur Wilkinson avec un Balun LC remplaçant la résistance. Le prototype fabriqué démontre une efficacité de puissance maximale de 93,3 % au port de sommation RF et une efficacité maximale de 91.7 % au port de différence RF.

Un redresseur composé de deux sous-redresseurs et d'un réseau de compression d'impédance est simulé, et les performances sont vérifiées avec le prototype fabriqué. Le redresseur proposé peut atteindre jusqu'à 66,2 % de l'efficacité de redressement maximale avec une puissance de signal d'entrée RF de 20 dBm à 3,5 GHz. On observe également que de 6 dBm à 24 dBm, le circuit conçu présente un rendement de redressement supérieur à 40%.

Les performances globales sont évaluées en mettant en cascade le combinateur Wilkinson conçu, le Balun et le redresseur. 53,5 % de l'efficacité du recyclage de l'alimentation CC est observée à 2,7 GHz avec une puissance de signal d'entrée RF de 20 dBm au port d'entrée Wilkinson. On observe également que de 8 dBm à 20 dBm, le circuit conçu présente un rendement de redressement supérieur à 40 %.

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An efficiency-enhanced power combining and recycling network for LINC power Amplifier

Jinmei YANG

ABSTRACT

Linear amplification using nonlinear components (LINC) is one of the various methods to provide high power amplifier efficiency and, at the same time, present good linearity. In this method, two constant amplitude phase-modulated signals, amplified respectively by two identical high-efficiency power amplifiers, are summed to achieve power amplification. During the summing of the signals using a combiner, like the Wilkinson combiner, energy is lost as heat through the isolation resistor. The design and implementation of a modified Wilkinson power combiner for LINC power amplifiers are investigated in this thesis. The goal is to increase the power efficiency of the LINC power amplifier by recycling the power that would be dissipated as heat in the resistor.

The work includes separate designs for three components: (i) a traditional Wilkinson combiner, (ii) a Balun, and (iii) a power recycling rectifier. An RF power summing and RF power recycling network are formed by integrating the three components. The overall performance is measured.

The design and simulation are conducted for the Wilkinson combiner with an LC Balun replacing the resistor. The fabricated prototype demonstrates a maximum power efficiency of 93.3% at the RF summing port and a maximum efficiency of 91.7% at the RF difference port.

A rectifier composed of two sub-rectifier and one impedance compression network is simulated, and the performance is verified with a fabricated prototype. The proposed rectifier can achieve 66.2% of the maximum rectifying efficiency with 20 dBm RF input signal power at 3.5GHz. It is also observed that from 6 dBm to 24 dBm, the designed circuit presents a rectifying efficiency greater than 40%.

The overall performance is evaluated by cascading the designed Wilkinson combiner, the Balun, and the rectifier. 53.5% of DC power recycling efficiency is observed at 2.7GHz with 20 dBm RF input signal power at the Wilkinson input ports. It is also observed that from 8 dBm to 20 dBm, the designed circuit presents a rectifying efficiency greater than 40%.

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LIST OF ABBREVIATIONS

RF   Radio Frequency

PA   Power Amplifier

PAE   Power Added Efficiency

PAR   Peak-to-Average Ratio

APD   Analog Pre-Distortion

DPD   Digital Pre-Distortion

LINC   Linear Amplification with Nonlinear Components

SCS   Signal Component Separator

RCN   Resistance Compression Network

ICN   Impedance Compression Network

BALUN   differential (**Bal**anced) port to a single-ended (**Un**balanced) port

LIST OF SYMBOLS

Ω Ohm

Z_0 the Characteristic Impedance

Z_{od} the Characteristic impedance for differential port

Z_{oc} the Characteristic impedance for single-ended port

f_o the Operating Frequency

θ_d the phase difference

INTRODUCTION

Power amplifiers in modern wireless telecommunication

In advanced wireless telecommunications systems, a power amplifier (PA) is a critical component to amplify the power of the radio frequency (RF) signal to a level that can be transmitted over long distances to meet the coverage requirement. Such PAs must be designed to meet some strict requirements, such as efficiency, linearity, and output power. As the most power-hungry components, high power efficiency, often referred to as power added efficiency (PAE), is an essential requirement. In portable devices, battery life is mainly affected by PA's efficiency. Similarly, a high-efficiency PA can reduce power consumption, lowering operating costs and reducing the environmental footprint. In advanced wireless systems, higher-order modulation schemes are often used to achieve higher data rates, such as 64-QAM or 256-QAM OFDM modulation [Javier Campos (2016)], [Bob Witte (2020)]. These modulation schemes are more sensitive to nonlinear distortions and nonlinear effects than simpler modulation schemes like BPSK or QPSK due to the higher peak-to-average ratio (PAR). A nonlinear power amplifier can cause distortions in the higher-order modulation schemes, leading to an increased bit error rate and a reduced data throughput. Therefore, in advanced wireless systems, linearity is required for power amplifiers to ensure the highest possible signal quality and data throughput [C. Behrens, R. I. Killey, S. J. Savory, M. Chen and P. Bayvel, (2010)].

The trade-off between linearity and efficiency is a significant challenge in power amplifier design for advanced wireless systems. The desire for high efficiency to extend battery life and reduce operating costs must be balanced with the need for high linearity to maintain signal quality and data throughput.

Power amplifier design techniques for high linearity and high efficiency

Class-A power amplifiers provide good linearity since the transistors work in their linear operation area for the whole signal range. However, due to the high constant current flow,

Class-A power amplifiers are not very efficient in terms of power consumption, making them unsuitable for the final stage of power amplifiers.

The Class-AB amplifier combines the advantages of both Class-A and Class-B amplifiers. It provides a high-quality signal with low distortion and high linearity, like a Class-A amplifier, but with improved efficiency due to the Class-B mode of operation.

A Doherty power amplifier is another good candidate for better linearity and higher efficiency [Bumman KIM, (2018)]. It uses a unique architecture consisting of two parallel amplifier stages. The first stage, called the "carrier amplifier," is a highly efficient Class-B or Class-C amplifier that operates at a constant power level. The second stage, called the "peaking amplifier," is a less efficient Class-A or Class-AB amplifier that operates only when the input signal is at its peak level [R. Pengelly, C. Fager and M. Ozen. (2016).]. A Doherty amplifier can achieve higher efficiency than a conventional power amplifier. The carrier amplifier handles most of the power amplification. In contrast, the peaking amplifier is only used when needed to provide additional power for the signal peaks, reducing the amount of energy dissipated by the amplifier and improving overall efficiency.

The pre-distortion technique is another practical approach to improve the power amplifier's linearity. Pre-distortion in analog (ADP) [Mikyung Cho. (2016)] or digital way (DPD) [R. Branson, C. Steinbeiser, Kim Tran, B. Loran and D. (2012)] is introduced to modify the input signal before the power amplifier amplifies it. The pre-distortion is designed to introduce distortion into the input signal intentionally, however, in such a way that the resulting distortion cancels out the distortion introduced by the power amplifier. The power amplifier can operate more efficiently and with lower distortion using pre-distortion.

In a conventional power amplifier, the power supply voltage is typically set to a fixed value higher than the input signal's peak voltage. Envelope tracking (ET) is a technique used in power amplifiers (PA) to improve their efficiency and linearity by dynamically adjusting the voltage of the PA's power supply in response to changes in the input signal amplitude. [X.

Liu, J. Jiang, C. Huang and P. K. T. Mok, (2022)]. By adjusting the power supply voltage to match the envelope, the PA can operate at a lower voltage when the input signal is low, which improves efficiency [M. Hassan, P. M. Asbeck and L. E. Larson. (2013)]. Implementing ET can be complex and requires careful design and optimization to achieve optimal performance.

In the techniques listed above, the amplifier components must operate in a linear mode to achieve an acceptable linearity. A LINC (Linear amplification with Nonlinear Components) power amplifier provides an option to allow the amplifier components to work in the saturation state, which significantly improves the amplifying components' efficiency. [Cox, (1974)], [Chireix, (1935)]. This is achievable by decomposing an amplitude modulated signal into two phase-only modulated signals, i.e., constant envelop signals, which are then amplified efficiently. However, to obtain the amplified version of the original signal, the two phase-only modulated signals must be combined. The combining structures that guarantee that the output signal is a linear amplified copy of the input signal must be properly terminated by isolated combiners, such as a Wilkinson combiner, which are power lost as heat in the isolation resistor. [L. Sundstrom and M. Johansson.1994], [Philip A. G. (2009)]. Therefore, while the LINC amplifier can be linear with highly efficient amplification components, its overall efficiency will be limited by the power loss of the combiner.

Research Problem

The question that we seek to address in this thesis is how to improve the overall efficiency of LINC amplifiers by improving the power efficiency of isolated combiners. Given that these components must be lossy to ensure linearity, the question therefore centers on how to recover the power that would otherwise be dissipated in the combining structure and use it to reduce the level of required DC power for the amplifier.

Research objective

The objective of this thesis is to achieve power efficiency enhancement for the LINC amplifier architecture by using a modified Wilkinson combiner design. Specifically, the goal is to design, prototype, and test a new Wilkison combiner where the isolation resistor is replaced by an energy harvesting circuit with an RF-to-DC rectifier such that the recovered DC power can be used to bias the LINC amplification components. The new Wilkinson-rectifier circuit will be a four-port component with three RF ports and one DC output port.

Organization of the thesis

The remainder of the thesis is organized as follows. In Chapter 1, we present the fundamental concepts of the LINC amplifier and discuss the relevant state of the art in the literature. Chapter 2 presents the detailed design of the Wilkinson combiner with the addition of a Balun at the conventional resistance terminals. In this chapter, we also present the simulation, the implementation, and the measurement of the design. In Chapter 3, the detailed design of the rectifier is given. Chapter 4 provides the results of the cascading circuit of the Wilkinson power combiner and the rectifier. A study conclusion is given in the Conclusion & Recommendations chapter along with a discussion of possible future work.

CHAPTER 1

LINC PA BASICS AND LITERATURE REVIEW

1.1   LINC Amplifier Basics

The LINC amplifier architecture is depicted in Figure 1.1. In this architecture, a phase and amplitude modulated input signal is separated by a Signal Component Separator (SCS) into two constant amplitude phase-modulated signals. These two components are amplified respectively by two identical high efficiency power amplifiers. The two output signals are subsequently combined to generate an amplified signal of the input signal. [Walid.H.(2010)].
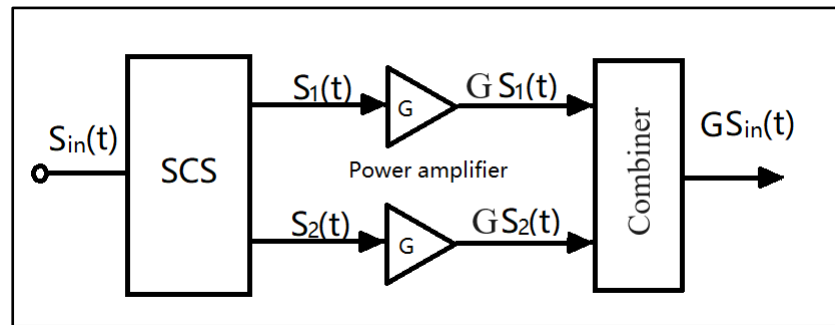
Figure 1.1   Block diagram of LINC PA

The input signal can be expressed as:

$$S_{in}(t) = r(\text{t}) * e^{j\varphi(t)} \qquad 0 \le r(\text{t}) \le r_{max} \qquad (1.1)$$

where $r(t)$ is the amplitude of the input signal $S_{in}(t)$ and $\varphi(t)$ is its phase. $r(t)$ can be further expressed as

$$r(t) = r_{max} * \cos \theta(t) \qquad 0° \le \theta(t) \le 90° \qquad (1.2)$$

where r_{max} represents the signal's peak amplitude.

Through the SCS, the input signal is decomposed into two signals, $S_1(t)$ and $S_2(t)$ as shown in Figure 1.2, with a constant amplitude of $r_{max}/2$:

$$S_1(t) = \frac{r_{max}}{2} e^{j(\varphi(t)+\theta(t))} \tag{1.3}$$

$$S_2(t) = \frac{r_{max}}{2} e^{j(\varphi(t)-\theta(t))} \tag{1.4}$$

Figure 1.2   Vector diagram of signal decomposition in LINC

Since $S_1(t)$ and $S_2(t)$ are constant amplitude, these two signals can be amplified by two identical high-efficiency saturated amplifiers, with a Gain equal to G. The outputs of the two amplifiers are combined using an isolated combiner. The isolated combiner will distribute the two

amplified signals between the summing port (Σ) and the difference port (Δ). At the summing port, the output signal can be expressed as follows:

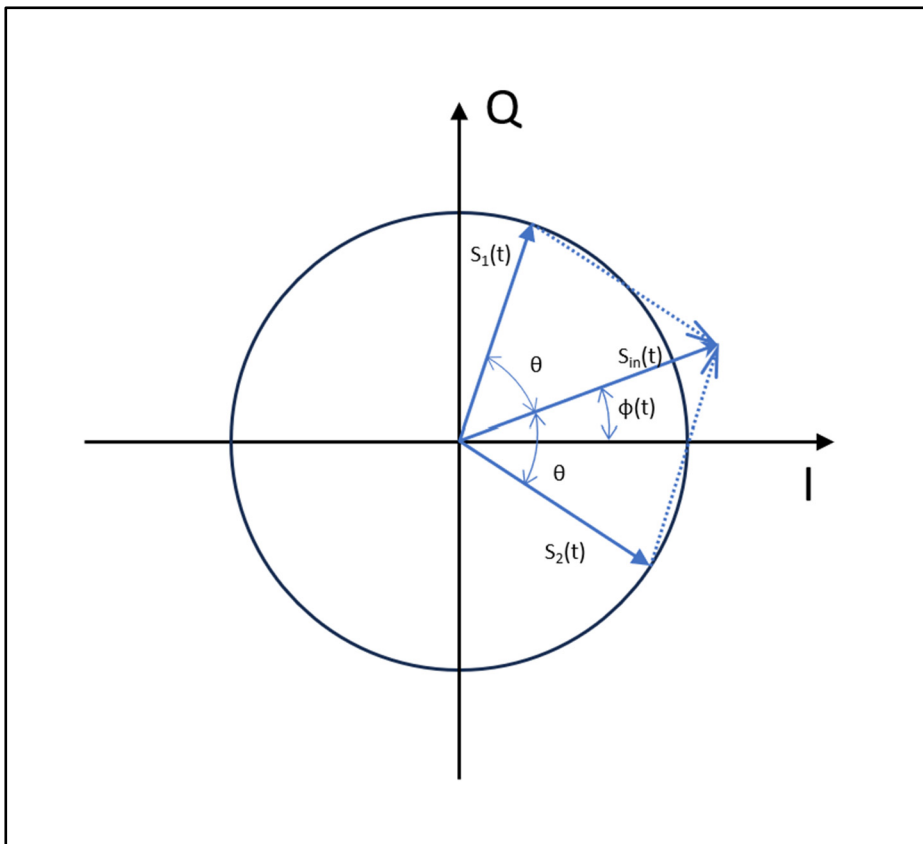$$S_\Sigma(t) = G\big(S_1(t) + S_2(t)\big) = G\left(\frac{r_{max}}{2}e^{j(\varphi(t)+\theta(t))} + \frac{r_{max}}{2}e^{j(\varphi(t)-\theta(t))}\right) \tag{1.5}$$

$$S_\Sigma(t) = Gr_{max}e^{j\varphi(t)}\frac{e^{j\theta(t)}+e^{-j\theta(t)}}{2} = Gr_{max}\cos\theta(t)\,e^{j\varphi(t)} = Gr(t)*e^{j\varphi(t)} \tag{1.6}$$

$$S_\Sigma(t) = GS_{in}(t) \tag{1.7}$$

The equations (1.5-1.7) indicate that, with the ideal combiner, the LINC power amplifier can achieve an amplified signal with perfect linearity by using two identical amplifiers working in a saturation state with high efficiency.

At the difference port, the output signal can be expressed as follows:

$$S_\Delta(t) = G\big(S_1(t) - S_2(t)\big) = G\left(\frac{r_{max}}{2}e^{j(\varphi(t)+\theta(t))} - \frac{r_{max}}{2}e^{j(\varphi(t)-\theta(t))}\right) \tag{1.8}$$

$$S_\Delta(t) = Gr_{max}e^{j\varphi(t)}\frac{e^{j\theta(t)}-e^{-j\theta(t)}}{2} = jGr_{max}\sin\theta(t)\,e^{j\varphi(t)} \tag{1.9}$$

This difference signal is typically dissipated in a resistance that isolates the input ports. There are several options for realizing isolated combiners [Pozar, D. M. (2012)]. A Hybrid Ring Combiner, also known as a rat-race combiner, uses a circular ring structure to combine or divide RF signals. One quadrature coupler associated with one 90-degree phase shifter can achieve the same function. This thesis focuses on a LINC power amplifier with a Wilkinson Combiner, as shown in Figure. 1.3.
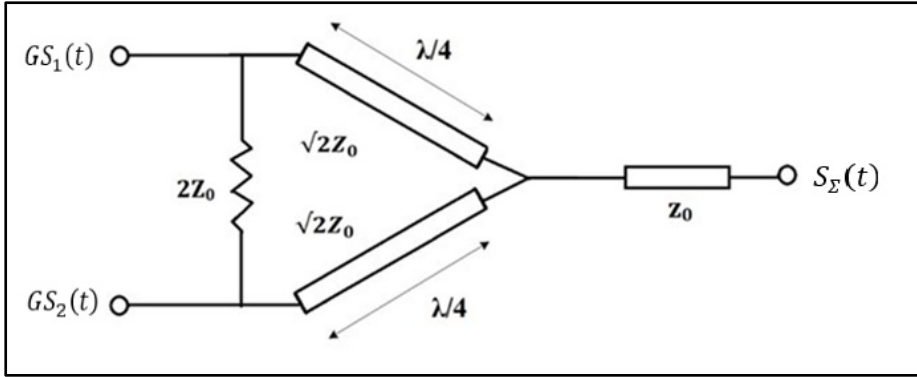
Figure 1.3   Wilkinson power combiner

The scattering parameters for the ideal Wilkinson combiner are:

$$[S] = \frac{-j}{\sqrt{2}} \begin{bmatrix} 0 & 1 & 1 \\ 1 & 0 & 0 \\ 1 & 0 & 0 \end{bmatrix} \tag{1.10}$$

As shown by equations (1.1-1.3), the input signal of Wilkinson can be written as:

$$S_{Wil\_in}(t) = GS_1(t) + GS_2(t) = G\frac{r_{max}}{2}e^{j(\varphi(t)+\theta(t))} + G\frac{r_{max}}{2}e^{j(\varphi(t)-\theta(t))} \tag{1.11}$$

and the input power is:

$$P_{Wil\_in} = P_1 + P_2 = 2 * G^2 \left(\frac{r_{max}}{2}\right)^2 = G^2\frac{r_{max}^2}{2} \tag{1.12}$$

where P_1 is the power of $GS_1(t)$ and P_2 is the power of $GS_2(t)$, $P_1 = P_2$.

The output signal of the Wilkinson combiner is:

$$S_\Sigma(t) = G\left(\frac{-j}{\sqrt{2}}S_1(t) + \frac{-j}{\sqrt{2}}S_2(t)\right) = G\frac{-j}{\sqrt{2}}\left(\frac{r_{max}}{2}e^{j(\varphi(t)+\theta(t))} + \frac{r_{max}}{2}e^{j(\varphi(t)-\theta(t))}\right) \tag{1.13}$$

$$S_{\Sigma}(t) = G \frac{-j}{\sqrt{2}} r_{max} \cos(\theta) \, e^{j\varphi(t)} \tag{1.14}$$

The summing powers can be written as a function of the outphasing angle modulation:

$$P_{\Sigma}(t) = G^2 \left(\frac{1}{\sqrt{2}} r_{max} \cos(\theta(t)) \right)^2 = G^2 \frac{r_{max}^2}{2} \cos^2\theta(t) \tag{1.15}$$

With this result, we can calculate the power efficiency of the summing and difference ports of the Wilkinson combiner. For the output power summing (Σ) port:

$$\eta_{\Sigma}(t) = \frac{P_{\Sigma}(t)}{P_{Wil\_in}} = \frac{G^2 \frac{r_{max}^2}{2} \cos^2\theta}{G^2 \frac{r_{max}^2}{2}} = \cos^2\theta(t) \tag{1.16}$$

For the output power at difference (Δ) port:

$$\eta_{\Delta}(t) = 1 - \cos^2\theta(t) = \sin^2\theta(t) \tag{1.17}$$

Equations (1.15) and (1.16) suggest that the combiner summing port achieves 100% efficiency at maximum output power when $S_1(t)$ and $S_2(t)$ are in phases ($\theta=0°$), So there is no power dissipated through the resistor; On the contrary, the combiner achieves 0% efficiency when $S_1(t)$ and $S_2(t)$ are in the out-of-phases ($\theta=90°$), which means all power is dissipated through the resistor.

1.2   Related Research

Researchers have conducted extensive studies to alleviate the problem of wasted energy on the isolation resistor and to improve the efficiency of the LINC PA.

One approach involves using non-isolating combiners in a study by [Ekta Aggrawal. (2020)], a Chireix combiner was employed to replace the Wilkinson combiner. The Chireix combiner offers a small range of tunable outphase angles. However, when the outphase angles are outside this limited angle, the load impedance presented to the PAs deviates significantly from the nominal value, resulting in distortion and decreased PA efficiency.

To address this issue, adaptive termination was implemented by adding it to a load of each amplifier based on the respective outphase angle [S. Moloudi, K. Takinami, M. Youssef, M. Mikhemar and A. Abidi, 2008.], [P. Roblin and H. -C. Chang,(2018)]. This approach aimed to enlarge the tunable range of outphase angles. Adding adaptive termination leads to increased circuit complexity.

Another approach is maintaining the Wilkinson isolation combiner but incorporating a rectifier that replaces the isolation resistor in the conventional Wilkinson combiner[R. Langridge, T. Thornton, P. Asbeck, and L. Larson. (1999)], [X. Zhang, L. Larson, P. Asbeck, and R. Langridge (2002)], [Philip A. Godoy. (2009)]. The rectifier serves to recycle the energy that would otherwise be dissipated in the form of heat on the isolation resistor. This approach allows for the recovery and utilization of the energy, thereby improving the overall efficiency of the PA. However, one significant disadvantage of employing the rectifier is that the impedance of the rectifier circuit presented to the Wilkinson combiner is not a fixed-value impedance because of the nonlinearity of the diode. Various designs have been proposed to decrease the changes in the presented impedance of the diode.

In the study of [R. Langridge, T. Thornton, P. Asbeck, and L. Larson. (1999)], a second combiner and matching circuit were employed between the diode and the first combiner (Wilkinson combiner). A more detailed analysis of the approach is in [X. Zhang, L. Larson, P. Asbeck, and R. Langridge (2002)], which used an optional isolator, a combiner, and two transformers to solve this problem. It is worth noting that the circuit is complicated.

In the work of [Philip A. Godoy. (2009)], a proposal was made to incorporate Resistance compression networks (RCNs) before the rectifier, connecting them to the transformer that was used to transfer the Wilkinson differential output to a single end. The RCN reduces the impedance variations caused by the rectifier. Consequently, the impedance matching performance can be improved, and the operating power range can be extended. However, it should be noted that in the design of the RCN-based rectifiers, the input impedance of the sub-rectifier should be purely resistive. Otherwise, the efficiency improvement achieved by using the RCN will degrade. This requirement limits the application of this approach.

In this work, a Complex Impedance Compression Network (ICN) [Zhi-Xia Du. (2018)] is used to replace the RCN. The ICNs can compress the variation range of the complex impedance rather than that of the resistance, featuring design flexibility.

CHAPTER 2

DESIGN OF LINC PA COMBINER

2.1 Introduction

As previously stated, for a LINC PA using a conventional Wilkinson combiner, energy will dissipate in the isolation resistor when the two signals are not in phase. To recycle the energy that is supposed to have been dissipated in the resistor and to improve the efficiency of the LINC PA, a combiner, including a Balun and a rectifier, will be designed to recycle the energy. The main idea is to use an energy recycling circuit to replace the isolation resistor. The rectified power can be used as one power supply to the internal PA or other circuits in the system through an additional power management circuit.

This chapter will focus on the Wilkinson combiner and Balun's design, simulation, and implementation. The measured results of the proposed design are also presented. The power rectifier design will be presented in the next chapter.

In a conventional Wilkinson combiner in the LINC PA, as depicted in Figure 1.2 and Figure 2.1, the combiner achieves 100% efficiency at the summing port when the two input signals, $S_a(t)=GS_1(t)$ and $S_b(t)=GS_2(t)$, are in phase with $\theta_d=0°$, and θ_d is the phase different between the $S_a(t)$ and $S_b(t)$. On the contrary, the combiner achieves 0% efficiency when the two phases are opposite with $\theta_d=180°$. When $\theta_d=180°$, all the RF power dissipates as heat through the isolation resistor. In a Zo $=50\Omega$ system, the resistor is 100Ω. This behavior significantly affects the efficiency of the LINC power amplifier. Figure 2.2 illustrates the relationship between the power efficiency collected at the signal-summing port and the phase difference between the two input signals, which follows equation (1.15).
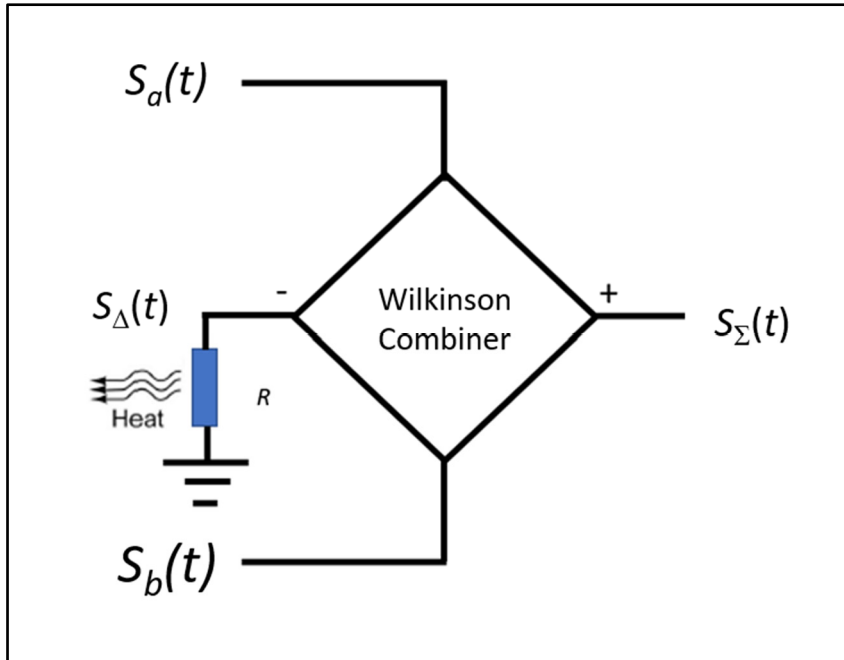.

Figure 2.1   Energy dissipates as heat through the resistor
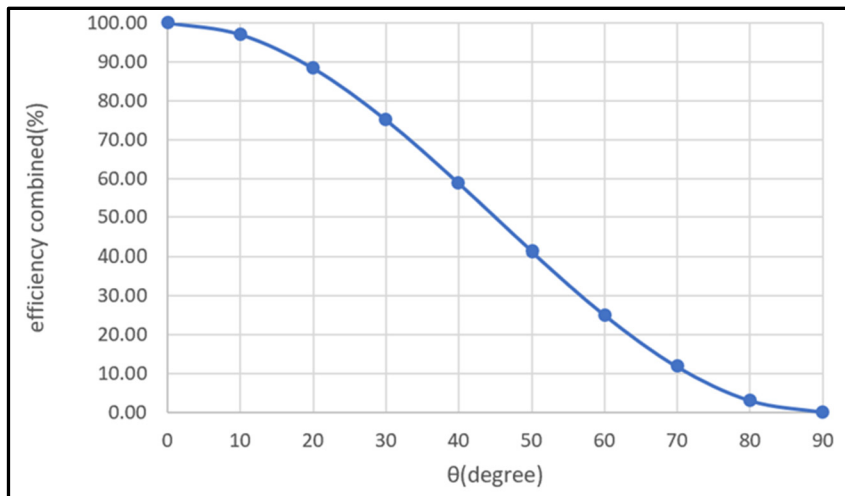in a conventional Wilkinson combiner

Figure 2.2   Summing port efficiency vs. phase difference
between the two signals

An architecture with power recycling at the difference port of the Wilkinson combiner is illustrated in Figure 2.3. According to equation 1.15, if the power at the difference port is collected and recycled, the total system efficiency would be 100%, assuming the loss from the

non-ideal components is neglected. The RF power at the differential port $S_\Delta(t)$ can be transformed to DC by a rectifier circuit. The DC power is then fed back to the power supply of the power amplifier, allowing it to be reused for power consumption. In this design, a Balun is used to transform the differential signal into a single-ended one, and it is connected to a rectifier. The rectifier following the Balun converts the radio frequency (RF) power into direct current (DC) power. Achieving energy recycling for the power amplifier's consumption.
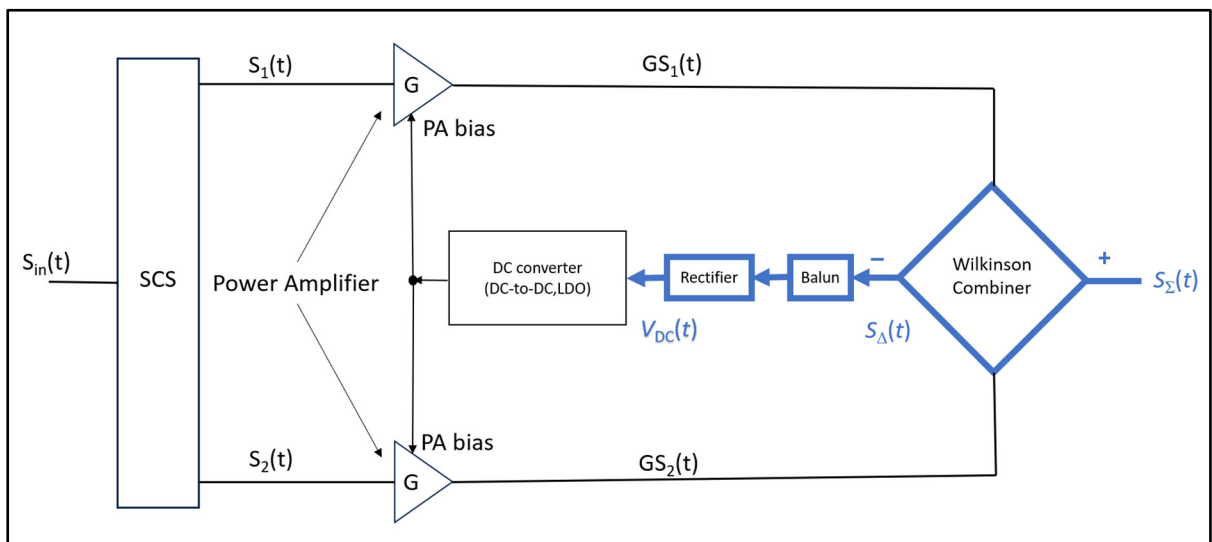

Figure 2.3   Architecture of power recycling of LINC PA

2.2   Wilkinson combiner with a subtraction port

The Wilkinson combiner/divider is a passive lossy three-port component for combining/dividing power. The basic structure is illustrated in Figure 2.4(a). Depending on the application, it can be used for signal combination or division. In the LINC PA application, one can use it not only to combine two saturated PA signals to regenerate the amplified signal at the summation port but also to collect the difference signal of the two signals at the subtraction port (difference port), shown in Figure 2.4b. To express the requirement, one uses a 100Ω difference port to replace the 100Ω resistor in Figure 2.4a to demonstrate the signal transmission, as illustrated in Figure 2.4(b). The S-Parameters matrix of this four-port network, which can be obtained by the even-odd analysis method [Pozar, D. M. (2012)], is given by:

$$[S] = \frac{-j}{\sqrt{2}} \begin{bmatrix} 0 & 1 & 1 & 0 \\ 1 & 0 & 0 & 1 \\ 1 & 0 & 0 & -1 \\ 0 & 1 & -1 & 0 \end{bmatrix} \tag{2.1}$$

(a) A conventional three-port Wilkinson combiner

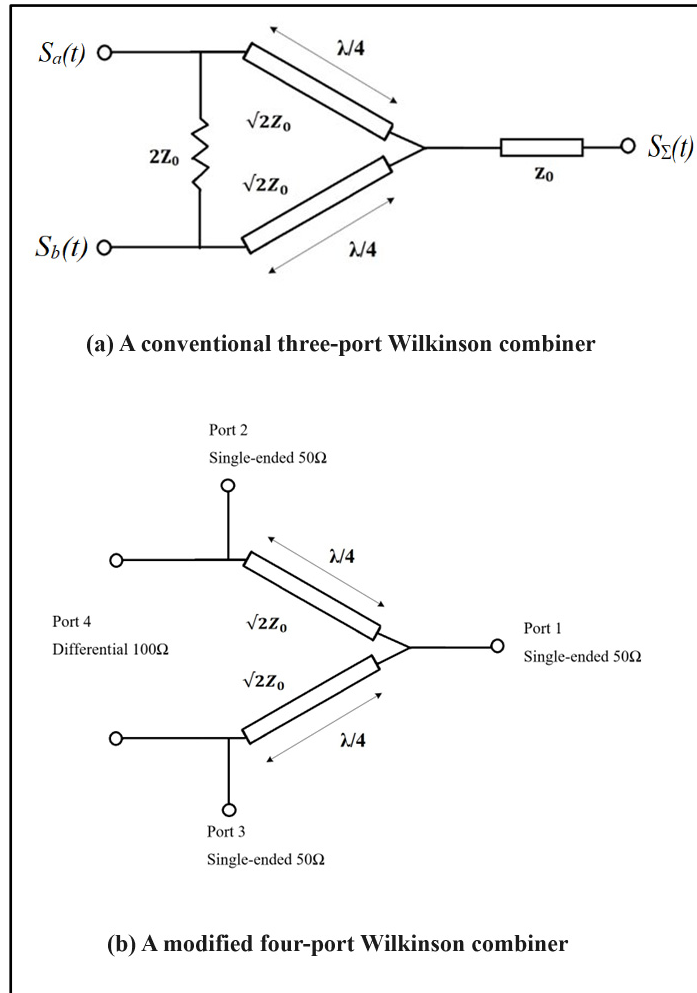**(b) A modified four-port Wilkinson combiner**

Figure 2.4   Wilkinson power combiner

By analyzing the S-parameters in (2.1), it can be determined that the four-port Wilkinson combiner is a lossless network. When the combiner is driven in ports 2 and 3, and the other ports have matching loads, the in phase components of the input signals are summed and directed to the output at port 1, known as the summation port, while simultaneously, the

outphased components between the two input signals create a potential difference between ports 2 and 3, which is then transferred to port 4.

2.2.1   Design of Wilkinson Combiner

The Wilkinson combiner design is conducted in Keysight's Advanced Design System (ADS). Roger's RO3006 material, with 6.15 of the relative dielectric constants and 25 mils of the height, is chosen for the substrate. Based on the substrate characteristics, the microstrip line width for Z_o =50Ω is 36 mil, and the line width for the $\sqrt{2}Z_o$ =70.71Ω is 17.44 mils. The physical transmission line length for quarter wavelength at the frequency of interest, 3GHz, is 485.43 mils.

The schematic for the S-parameter simulation is shown in Figure 2.5. A behavioral model for converting differential mode to single-ended mode, ideal Balun, is used to simulate the signal transmission in the subtraction port.
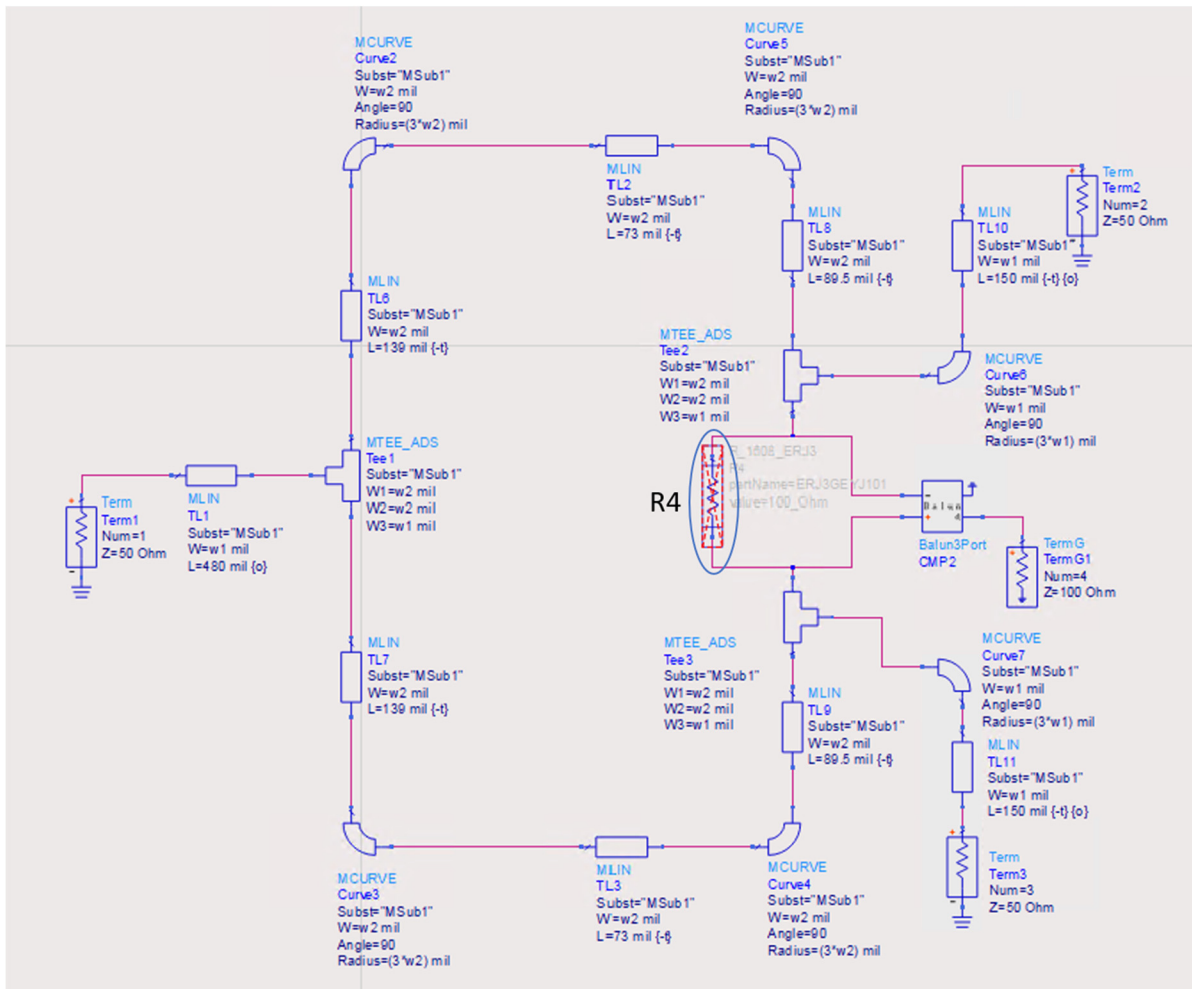
Figure 2.5   Schematic for Wilkinson combiner simulation

The simulated S-parameters are shown in Figure 2.6. It can achieve 33% of relative bandwidth for 20dB return loss at each port.

Because in the actual S-parameter measurement, it is difficult to measure differential port, therefore one 100Ω resister will be placed to measure the combiner's efficiency. A three-port simulation with a physical 100Ω model is conducted. The simulated results are shown in Figure 2.7. It can be observed that by using the physical resistor, S33 and S23 are slightly deteriorated. By looking at the physical resistor model shown in Figure 2.8, it can be discovered that the physical resistor is not a precise 100Ω. Instead, it is a 100Ω in series with an inductor. Although

it is possible to add a capacitor in series to convert the value to a precise 100Ω, we decided not to do so in the actual design, as the measured values of S11= -29.450dB and S23=-29.237dB are within an acceptable range. Furthermore, adding a capacitor can introduce other unknown effects and make the overall design more complex. Therefore, we opted not to include a capacitor in the final design. This finding highlights the importance of considering the practical limitations and deviations that can arise in real-world applications instead of relying solely on idealized theoretical models.
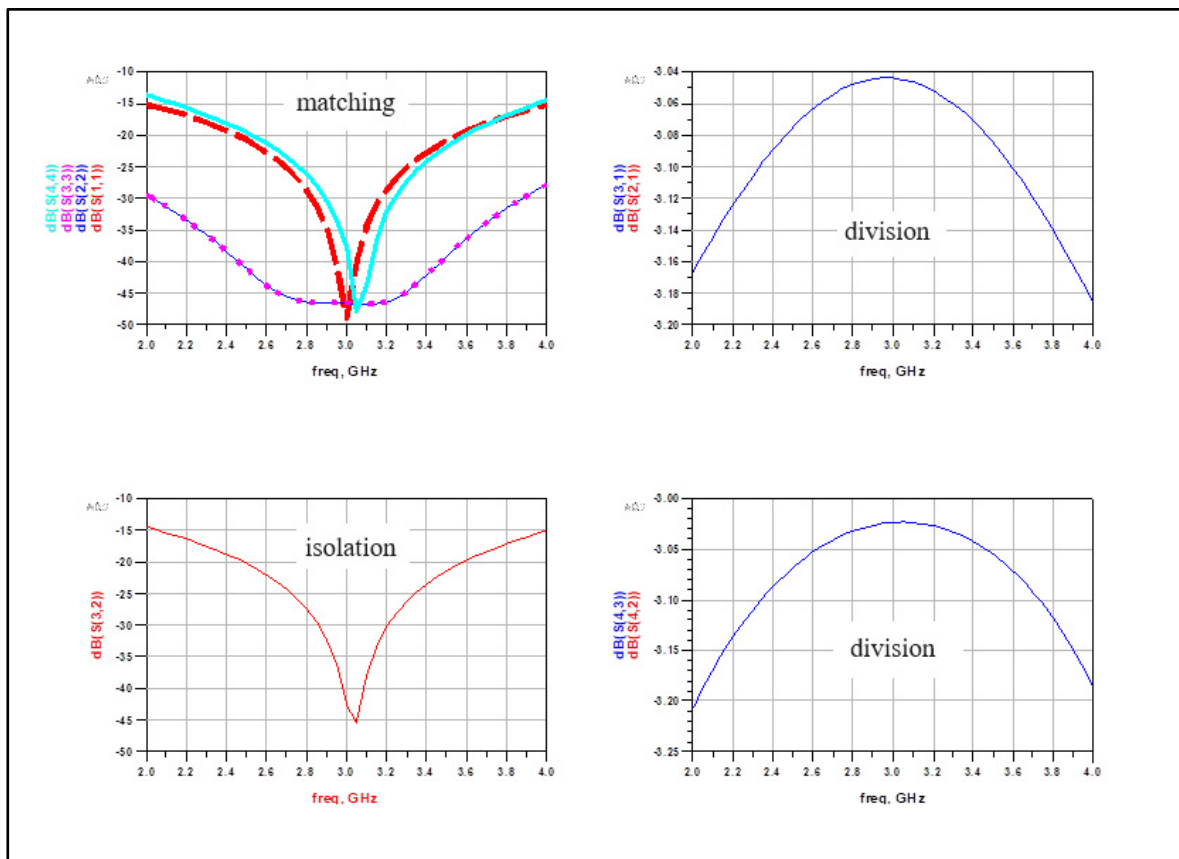

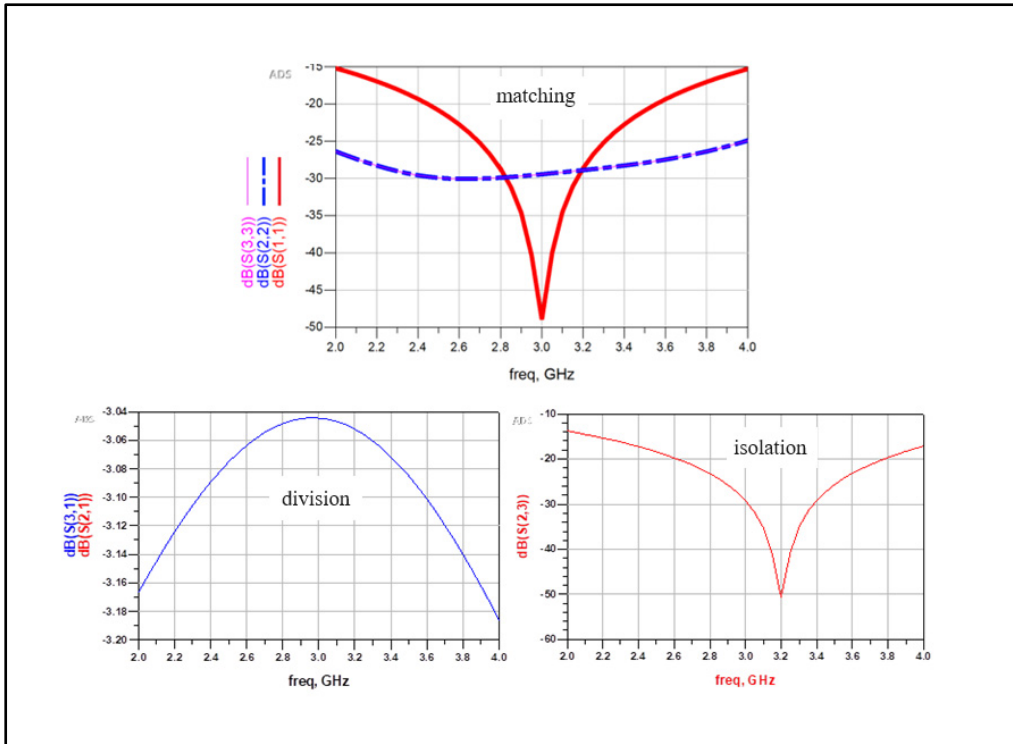Figure 2.6   Simulated S-parameters of four ports Wilkinson combiner

Figure 2.7   Simulated S-parameter of Wilkinson when
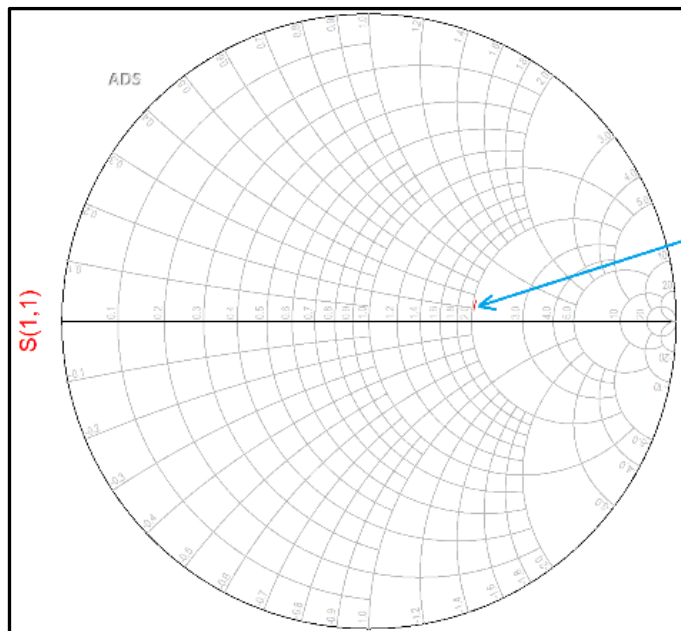actual 100Ω model is used

Figure 2.8   S11 of the physical 100Ω resistance

2.2.2   Implementation and Measurement

A prototype was fabricated to verify the simulated combiner's performance, as shown in Figure 2.9. 100Ω resistor is placed in the subtraction port.
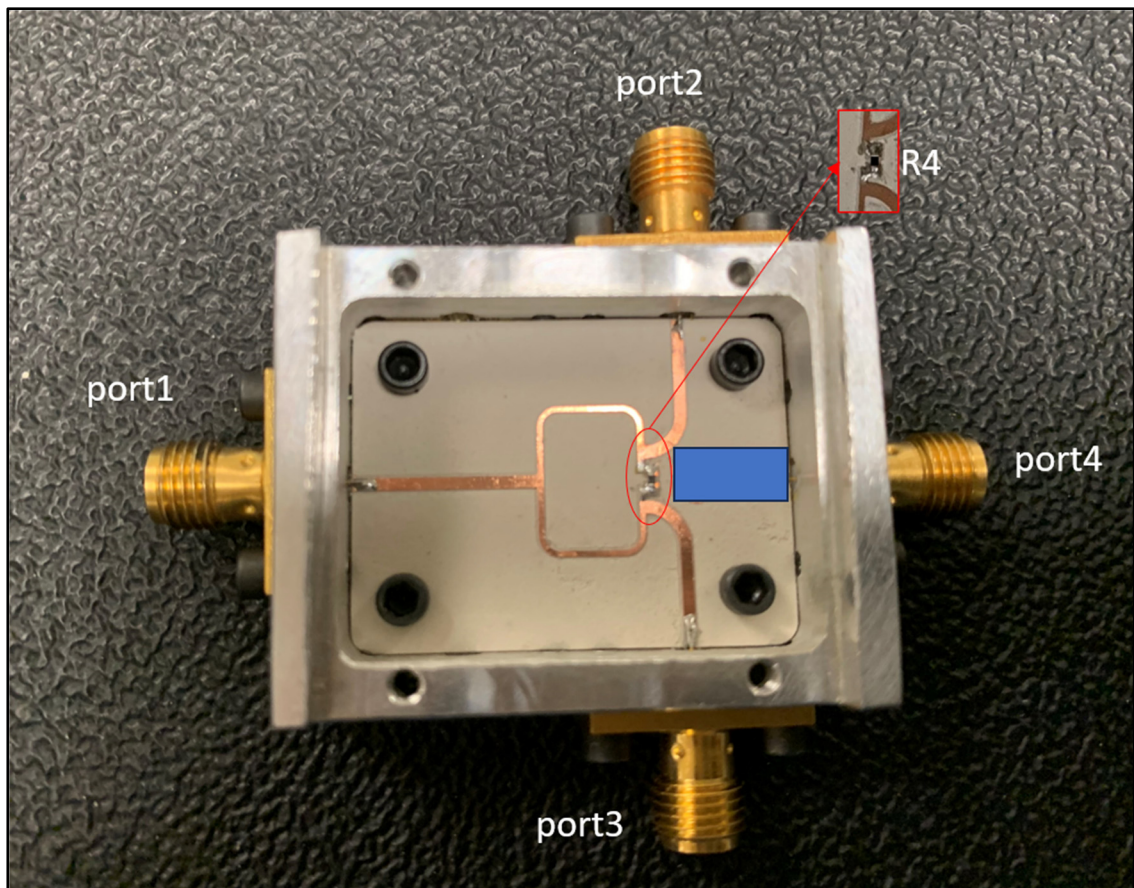

Figure 2.9   Fabricated prototype of Wilkinson combiner

The Wilkinson combiner's S-parameters are measured by using a vector network analyzer. These measurements are crucial in determining the circuit performance and serve as a baseline for further analysis and optimization. The measured S-parameters are presented in Figure 2.10.
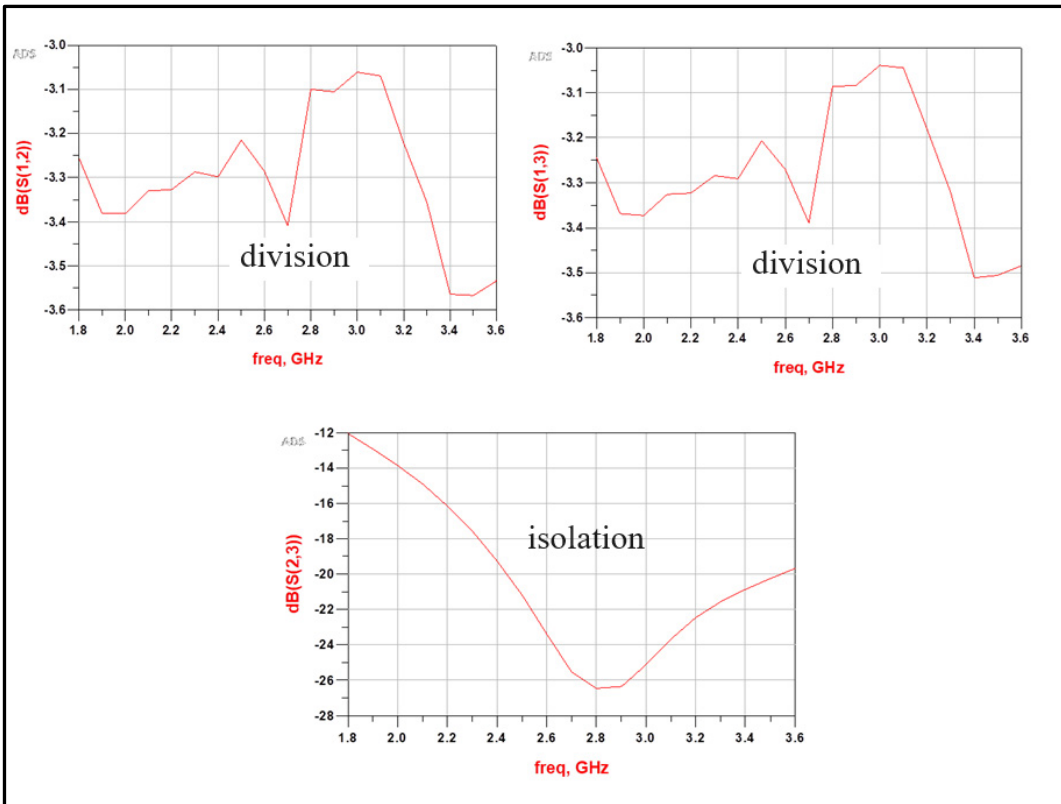
Figure 2.10   Measured S-parameters of Wilkinson combiner

Compared to the simulation results, the measured isolation between ports 2 and 3 has around 200MHz offset from the designed center frequency but is still around 25dB at 3GHz.

2.3   Balun

Balun stands for "BALanced-to-UNbalanced" impedance transformation. It is a three-port component used to converts differential signals into single-ended signals and vice versa. Along with balanced and unbalanced transformation, Balun can also perform another important function: impedance matching.

As discussed in the previous section, a Balun will replace the 100 Ω resistance that is supposed to be connected between the two input signals of the Wilkinson combiner. The differential port should match to 100Ω while the single-ended port should match to 50 Ω. The unbalanced output is to be connected to the following part circuit, which is the rectifier circuit. The Balun

serves as a critical intermediary in this process, facilitating the transformation of the differential signals into a single-ended output signals and maintaining the Wilkinson combiner in symmetry.

2.3.1   Simulation of an LC Balun

An LC Balun composed of four components is illustrated in Figure 2.11. The inductors and capacitors' values can be calculated by the following equations below:

$$L = \frac{\sqrt{Z_{od}Z_{oc}}}{2\pi f_o} \tag{2.2}$$

$$C = \frac{1}{2\pi f_o\sqrt{Z_{od}Z_{oc}}} \tag{2.3}$$

where Z_{od} and Z_{oc} are the characteristic impedance for differential and single-ended ports, respectively, and f_o is the operating frequency. In this work, $f_o = 3$ GHz, $Z_{od} = 100$ Ω, and $Z_{oc} = 50$ Ω. Therefore, the components value can be obtained with L=3.75 nH and C=0.75 pF.
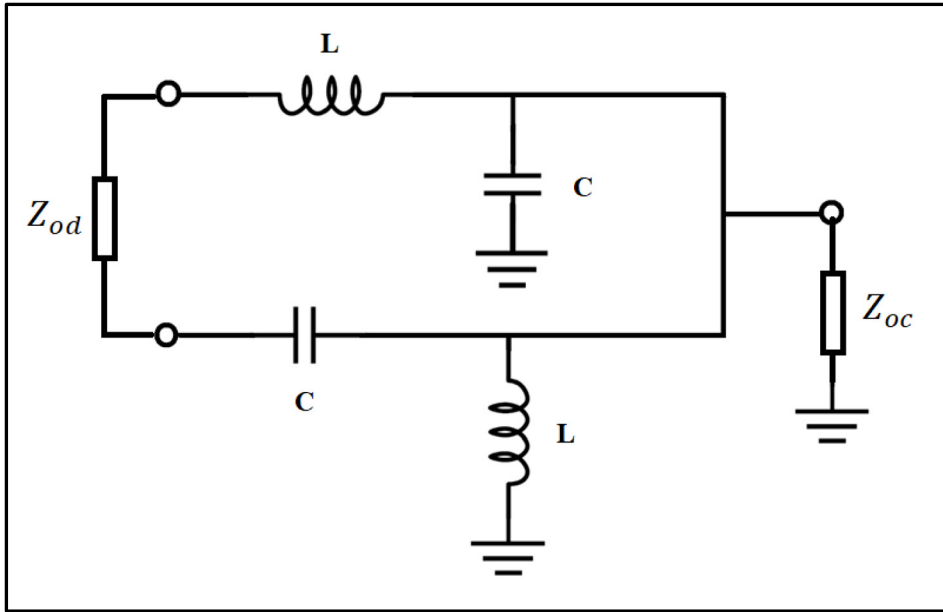
Figure 2.11   Circuit of an LC Balun

The S-parameter simulation is conducted in ADS, as shown in Figure 2.12. To better predict the actual situation, all transmission line segments and Vias necessary for constructing the Balun are also included in the simulation, and accurate S-parameter-based models for inductors and capacitors are used instead of ideal component values. The simulated S-parameters are presented in Figure 2.13. The Balun can achieve better than 20 dB of return loss for both ports. Around 0.3 dB insertion loss at 3GHz is caused by the parasitic loss in the actual component model.

Figure 2.12   Schematic of the LC Balun design

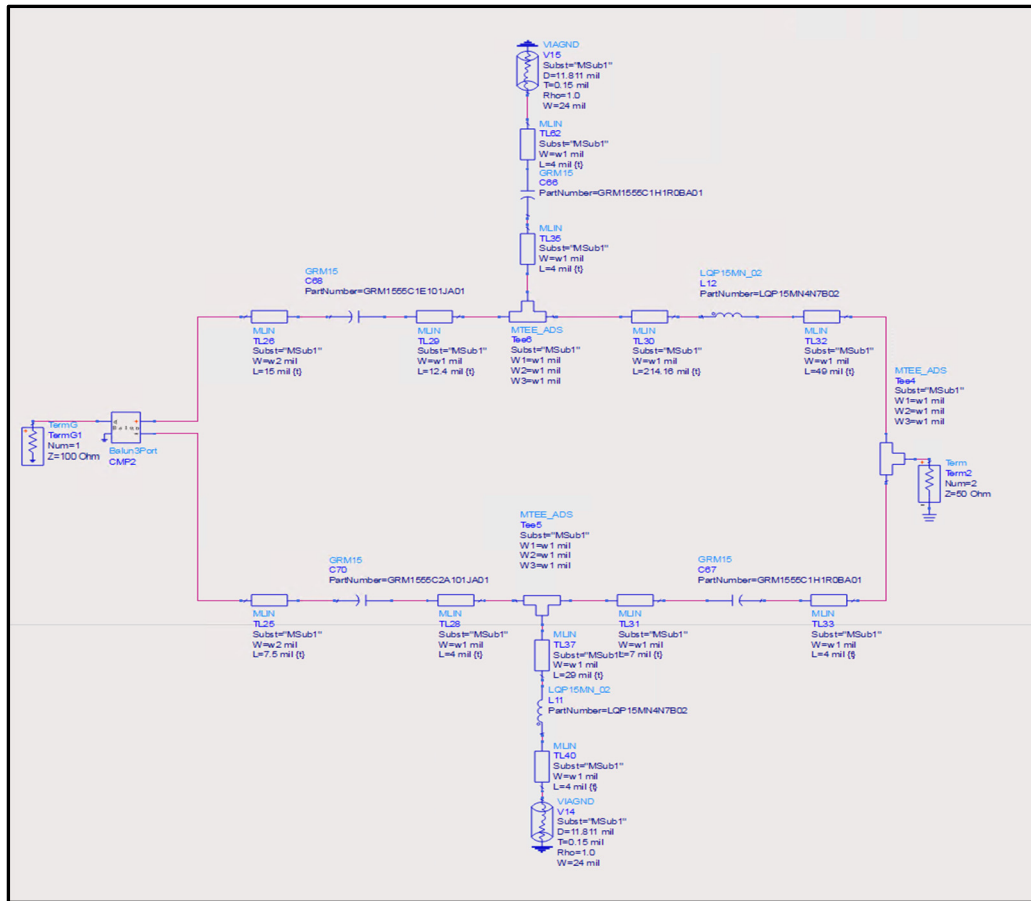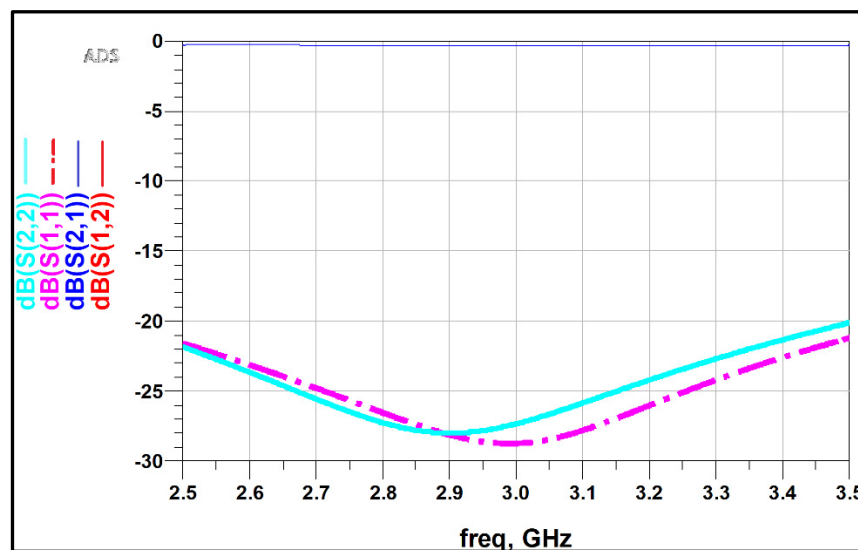Figure 2.13   S-parameters of LC Balun

2.4   Cascading of the Wilkinson Combiner and Balun

So far, we have completed the design of the regular Wilkinson combiner and the LC Balun. In this section, we aim to make a cascaded circuit of the regular Wilkinson combiner and the LC Balun components into a single circuit. The objective is to replace the 100Ω resistor typically used in the regular Wilkinson circuit with the Balun component. By doing so, we can analyze the performance of this modified Wilkinson power circuit and compare it with the traditional Wilkinson combiner design.

2.4.1   Simulation of Wilkinson Combiner Connected to an LC Balun

As depicted in Figure 2.14, by connecting the Wilkinson combiner's 100 Ω differential output to the Balun's 100 Ω differential input, the vector difference between $S_a(t)$ and $S_b(t)$ can be transmitted to the Balun's output, $S_{Balun\_out}(t)$.
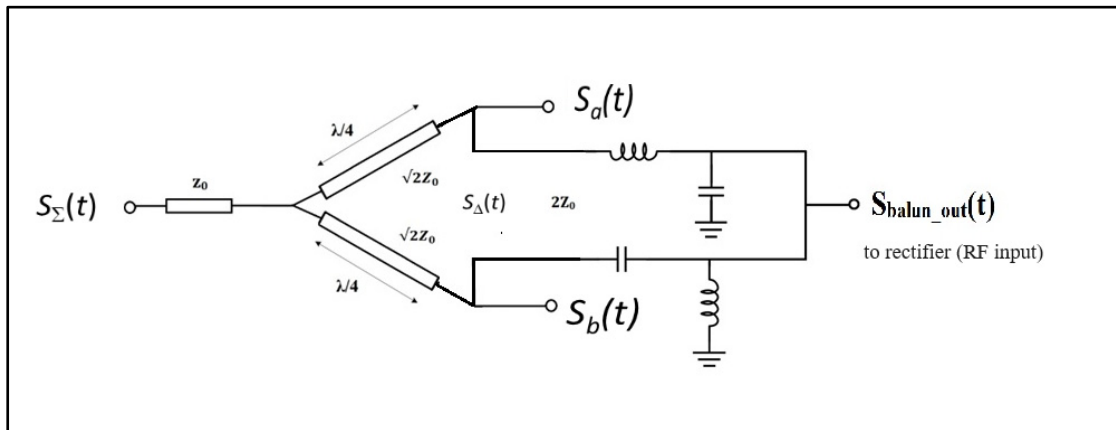
Figure 2.14 Schematic block diagram of the modified
Wilkinson power combiner measurement

The detailed simulation schematic in ADS, with the transmission line segments and the ground vias, is presented in Figure 2.15. The simulated S-parameters are shown in Figure 2.16. It can be observed that at the frequency of interest,

(a) the return loss at the four ports is less than 17dB;

(b) the insertion loss between two output ports and the two input ports is less than 3.25dB;

(c) the isolation between the two input and the two output ports is greater than 20dB.

Figure 2.15   Schematic of the modified Wilkinson power combiner in ADS

Figure 2.16   Simulated results of the modified Wilkinson power combiner/Balun

2.4.2   Implementation and measurement of the cascade design of the Wilkinson combiner and Balun

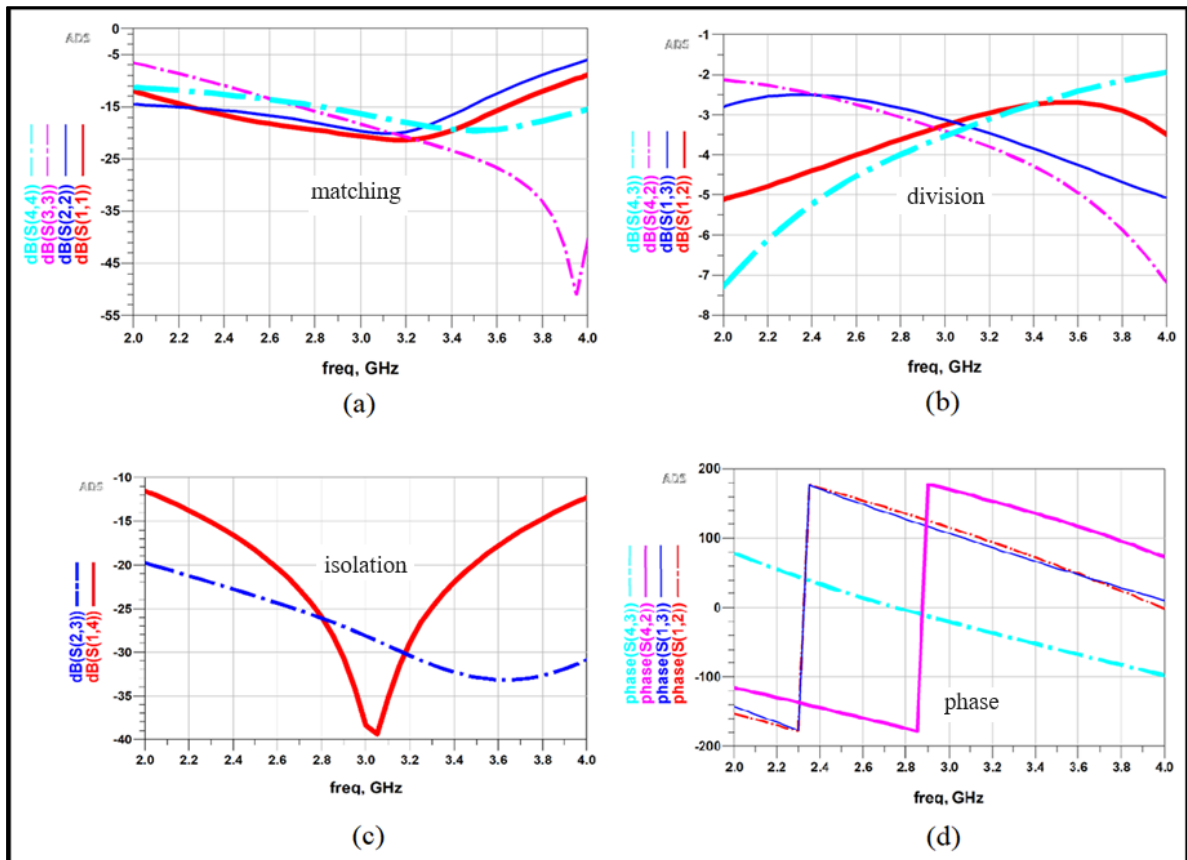The prototype used for Wilkson combiner verification is re-used to verify the performance of the cascaded combiner. The 100 Ω resistor is removed and replaced by the LC Balun simulated in section 2.4.1, as shown in Figure 2.17.
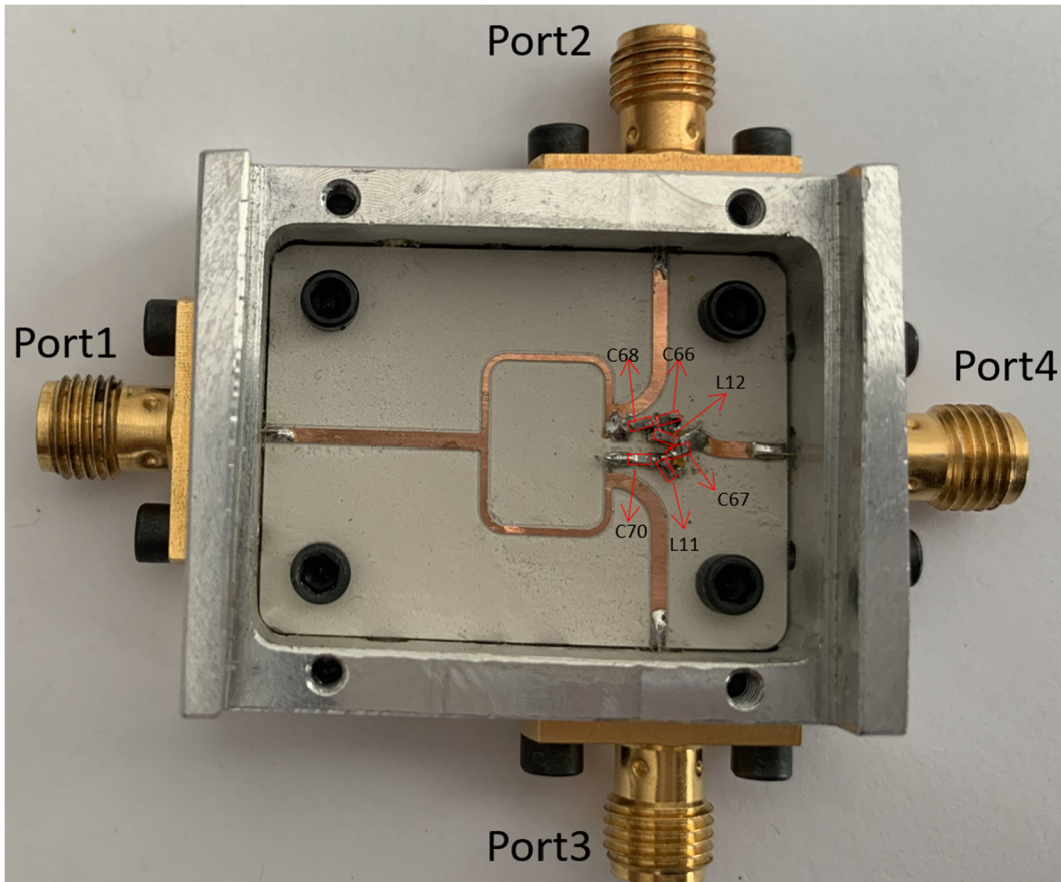
Figure 2.17   Fabricated prototype of the cascaded combiner/Balun

The S-parameters are measured with a network analyzer and demonstrated in Figure 2.18. It can be noticed that the best operating frequency shifts from 3GHz to 2.7GHz. It could be caused by the unideal model of ground via and the mutual coupling between the lines of a combiner and the lines of a Balun. Looking at 2.7GHz, the return losses for all four ports are less than -13 dB, and the insertion losses from two input ports to two output ports are all around 3.3 dB. From the phase response in Figure 2.18d, one can find that S12 and S13 have an identical phase delay, which indicates that the signal at port 1 is the vector sum of the signals at ports 2 and 3, while the phase difference between S42 and S43 is almost 180 degrees, which demonstrates that the signal at port 4 is the vector subtraction of the signal at ports 2 and 3.

Figure 2.18   Measured S-parameters of the modified Wilkinson power combiner
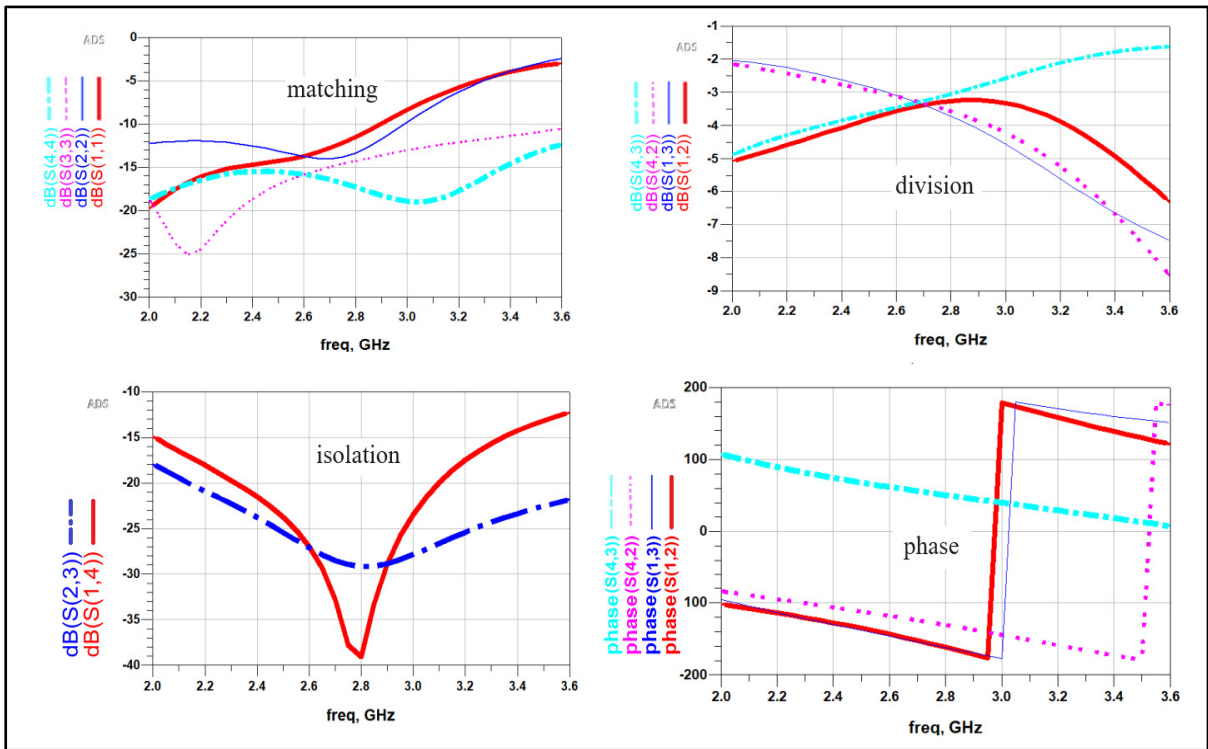
Based on the measured S-parameters, the efficiency for the modified Wilkinson power combiner's Sum and the Subtraction ports versus frequency can be calculated, as illustrated in Figure 2.19.
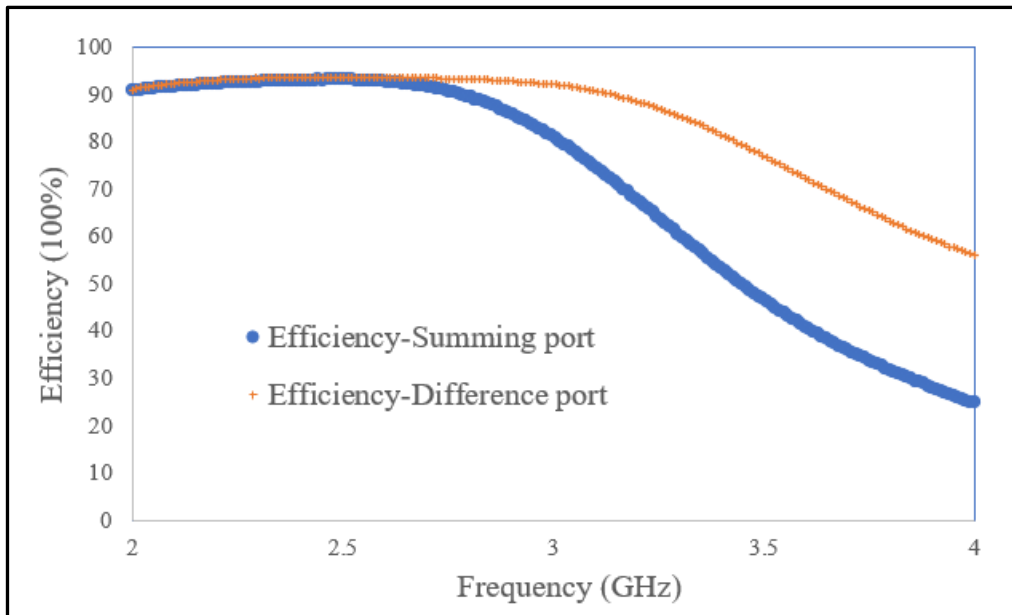
Figure 2.19 the efficiency for both the Sum port and the Subtraction port of the Wilkinson combiner

Figure 2.16(b) and Figure 2.18(b) show a frequency shift in the prototype. Even though the best efficiency of the Wilkinson combiner and LC Balun design is not at the center frequency of 3GHz, it can reach 93.293% for the sum port and 91.659% for the Balun output at 2.7GHz. In summary, the proposed design provides a good result even though the best efficiency is not at the design frequency. However, further optimization is needed to improve the efficiency at the center frequency. The higher efficiency at 2.7GHz may suggest that the proposed design is better suited for certain frequency ranges. Overall, this research demonstrates the potential of using LC Balun to replace the 100Ω resistor in the Wilkinson combiner for a good performance. This design can be used to connect to the rectifier circuit in the next stage to achieve power harvesting.

CHAPTER 3

DESIGN OF RECTIFIER

3.1   Introduction

In Chapter 2, one combiner with vector summing and vector difference outputs was designed, fabricated, and measured. In this chapter, a rectifier, which is used to convert RF energy to DC power, will be discussed. As shown in Figure 2.3 and Figure 2.14, the rectifier is connected to the Balun output port.

The typical half-wave double rectifier is illustrated in Figure 3.1. When the input AC signal, Vin, is in the negative half cycle, diode D1 is on, and the output DC voltage can be charged proportionally to the AC signal's amplitude. Similarly, during the input AC signal's positive half cycle, diode D2 is on, and the output DC voltage reaches approximately double the AC signal's amplitude.
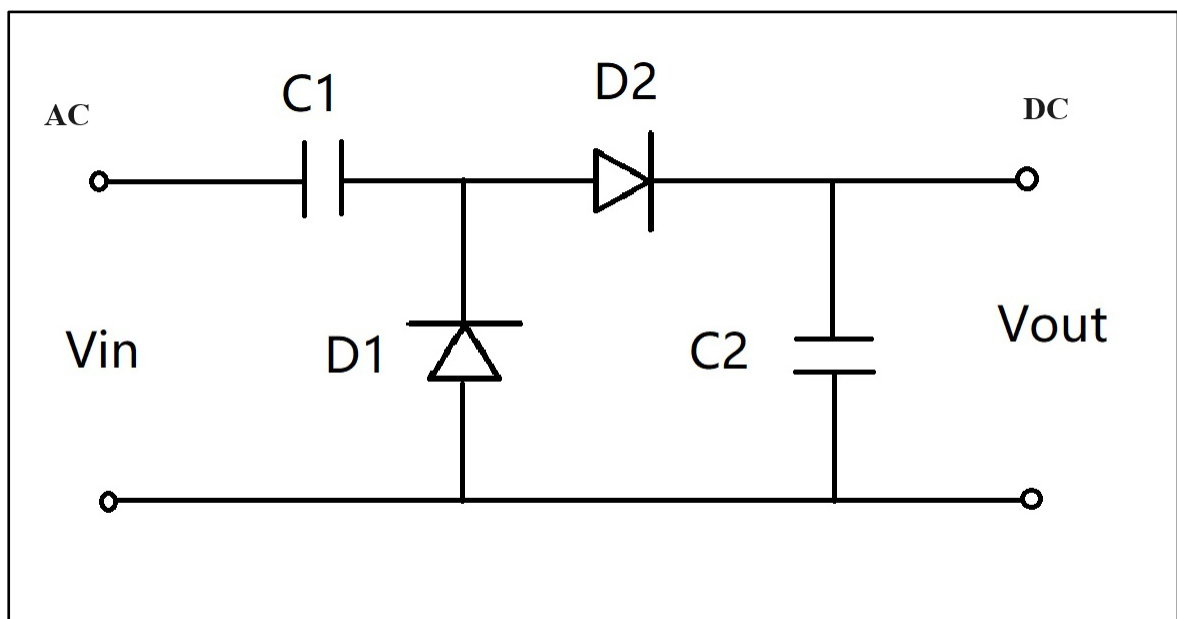

Figure 3.1   Circuit of half-wave voltage double rectifier

The power from the combiner's difference port varies over a large range, as equation (1.9) depicts. That poses a challenge for the rectifier design. The rectifier must maintain a stable impedance to keep the combiner's performance since the rectifier's input impedance is connected to the differential output of the combiner. Checking the voltage double rectifier, the nonlinear nature of the diode will cause the rectifier to present a variable load versus input power level for the preceded circuit. To reduce the variation range of the rectifier input impedance, several effective impedance compression technologies have been researched, including the Resistance Compression Network (RCN) mentioned in the works of (Philip A. Godoy. 2009) and (Yehui Han. 2007). A related evaluation version called Impedance Compression network (ICN) was also introduced in (Zhi-Xia Du.2018). This work uses the ICN method to achieve a stable input impedance. The block diagram is demonstrated in Figure 3.2. Two identical sub-rectifiers are used, which present an identical impedance, Z_L. One impedance compression network connected by two sub-rectifiers converts the extensive range of Z_L to a small impedance range, Z_{in1}. One impedance-matching network is inserted to match Z_{in1} to the combiner's differential port impedance. The structure of the ICN is demonstrated in Figure 3.3. The basic idea is to make the input impedance of the upper branch the conjugate of the input impedance of the lower branch. According to the deduction in (Zhi-Xia Du. 2018), the transmission line TL1's electric length and characteristic impedance can be determined by the equation below:

$$\tan(\theta_{ICN}) = \frac{2Z_{ICN}X_L}{|Z_L|^2 + Z_{ICN}^2} \tag{3.1}$$

In which $Z_L = R_L + jX_L$ is the impedance of the sub-rectifier.
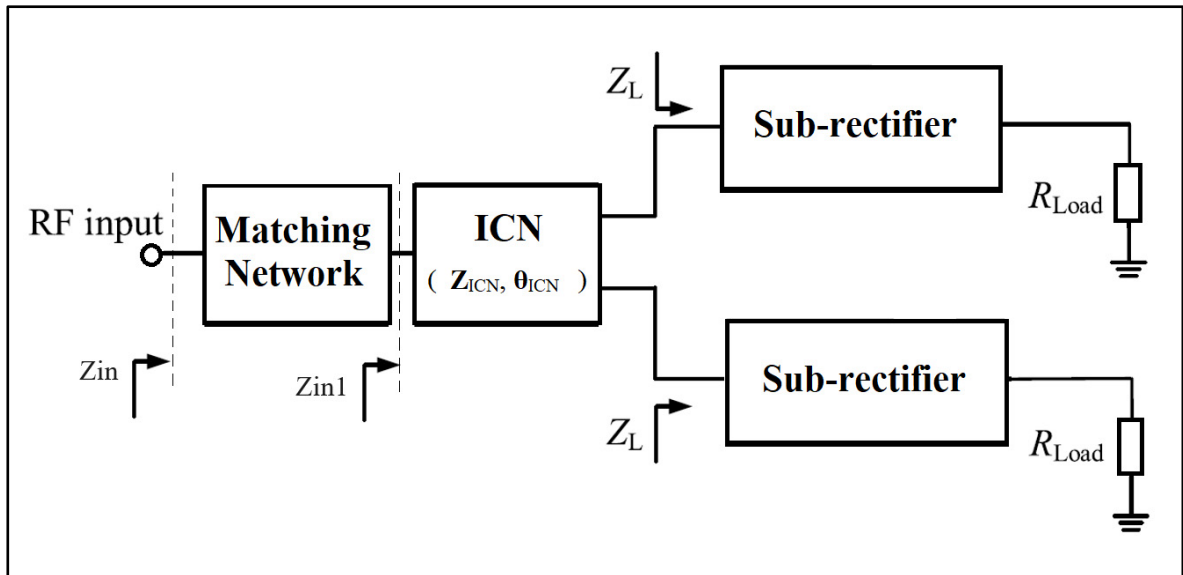
Figure 3.2   Block Diagram of rectifier with stable input impedance
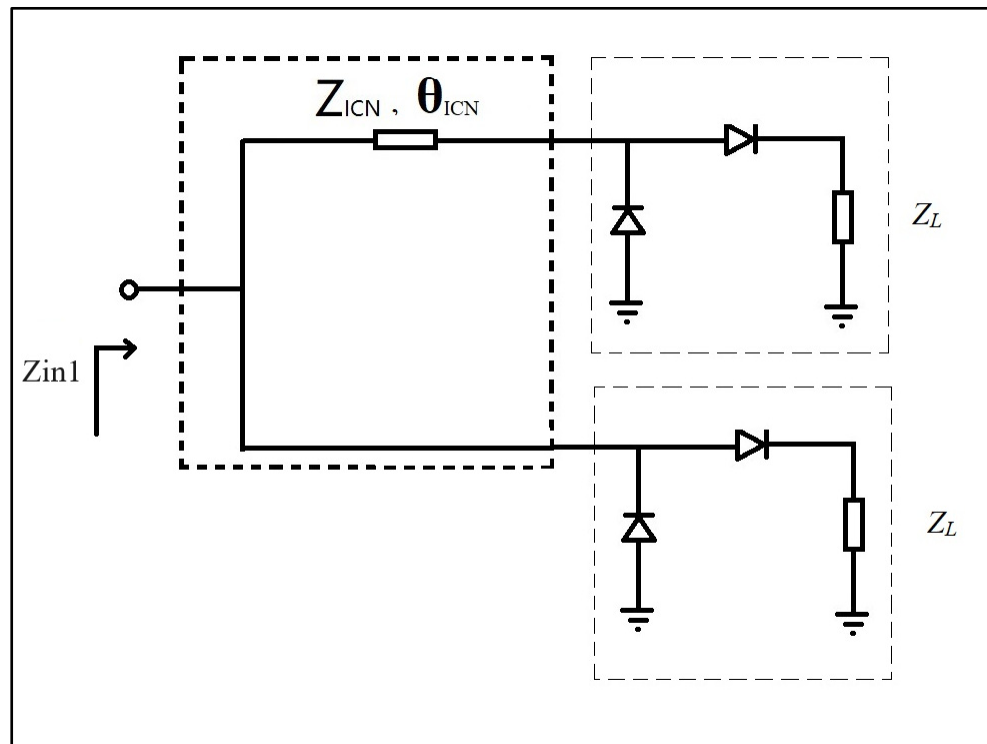

Figure 3.3   Structure of ICN

3.2   Simulation

First, to obtain the impedance of the sub-rectifier, a large-signal S-parameter simulation at 3.5GHz is conducted for the sub-rectifier. The DC output load, R_{Load}, is set to 220 Ω. A total input power of 23dBm is used for the simulation. The simulated data shows that the impedance is Z_L= (48.55 + j45.45) Ω, as shown in Figure 3.4.
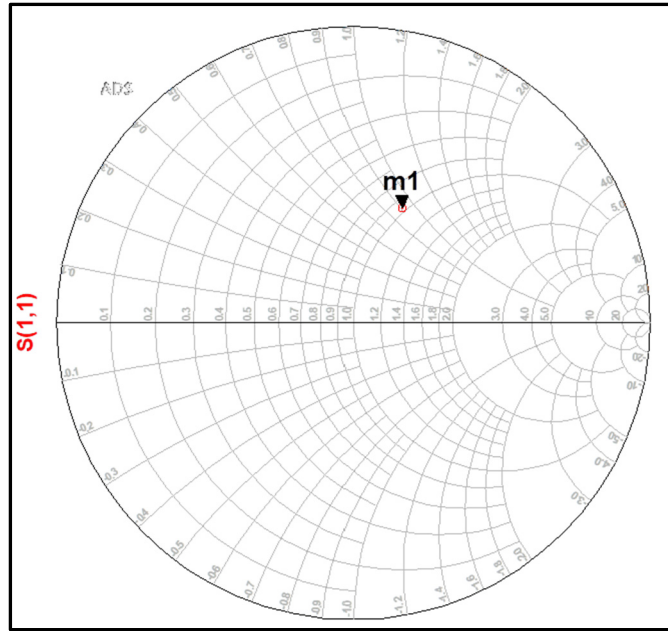
Figure 3.4   Simulated input impedance for
sub-rectifier with 23 dBm input power

Based on equation (3.1), The required transmission line characteristics for Z_L= (48.55 + j45.45) are $Z_{ICN} = 90$ Ω and $\theta_{ICN} =105.21°$. A microstrip line can be used to constitute the ICN. After adding the ICN, the input impedance should be $Z_L{}^*$= (48.55- j45.45) Ω. As shown in Figure 3.5(a), there is a little shift. The simulated impedance is $Z_L{}^*$= (49.25 − j45.45) Ω, which is almost the conjugation of Z_L. Therefore, the input impedance Z_{in1} is the parallel of two conjugated impedances and can be calculated with $Z_{in1} = Z_L//Z_L{}^* = (46.1 +j4.5)$ Ω, as marked in Figure 3.5b.
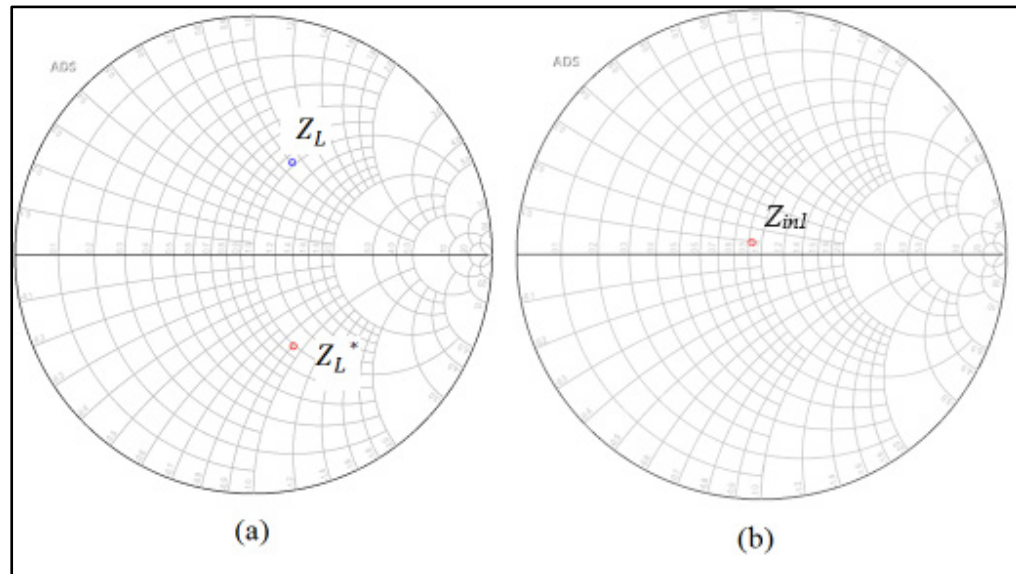
Figure 3.5   Simulated rectifier impedance

(a) two sub-rectifier branches; (b) total input impedance

A power sweep large-signal simulation from -1dBm and 31dBm is implemented to verify the impedance compression characteristic of the rectifier. In Figure 3.6, the dotted line is the original impedance Z_L, without the ICN circuit, and the solid line is the compressed impedance Z_{in1}. It can be observed that the impedance of the rectifier with ICN is closer to the center of the Smith chart, which illustrates that the input impedance is compressed with the aid of the ICN.
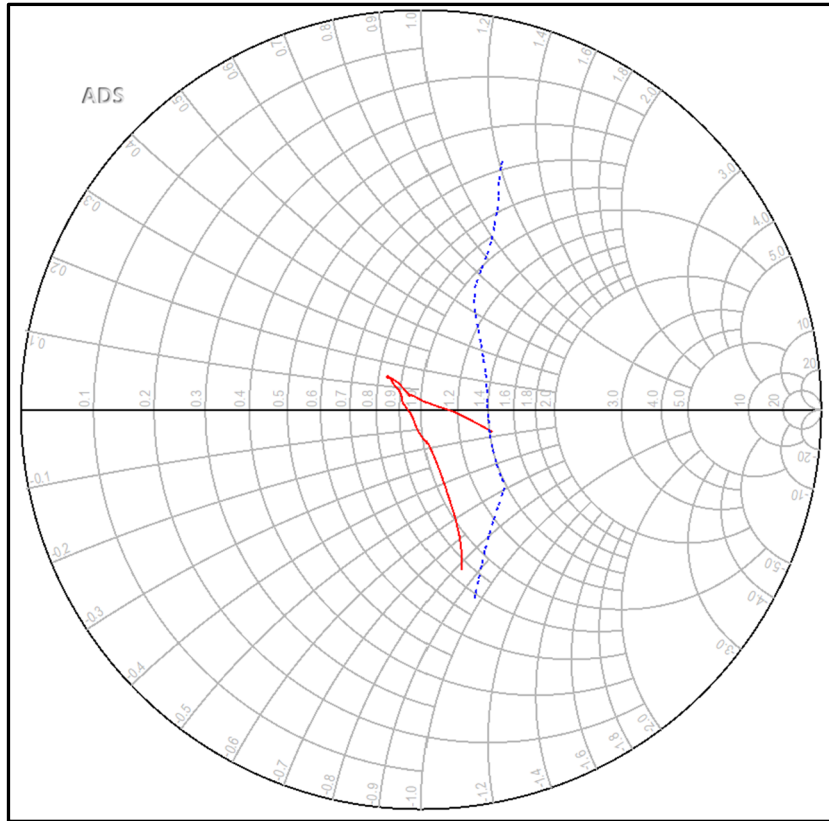
Figure 3.6   Impedance compression because of ICN

To match the input impedance to 50 Ω, one first chooses a point according to the desired frequency and previously used input power, which was employed to obtain the original impedance of the sub-rectifier as a reference input impedance. In this case, $Z_{in1} = (46.1 + j4.5)\,\Omega$ is the point. Subsequently, a single-branch matching network, including a serial stripe line and an open stub, is applied to the circuit. The total simulation circuit is shown in Figure 3.7. The same substrate as the fabricated combiner prototype is used for rectifier design. Every transmission line's width and length are calculated based on the required electrical length and characteristic impedance, which can be directly used for the prototype implementation.
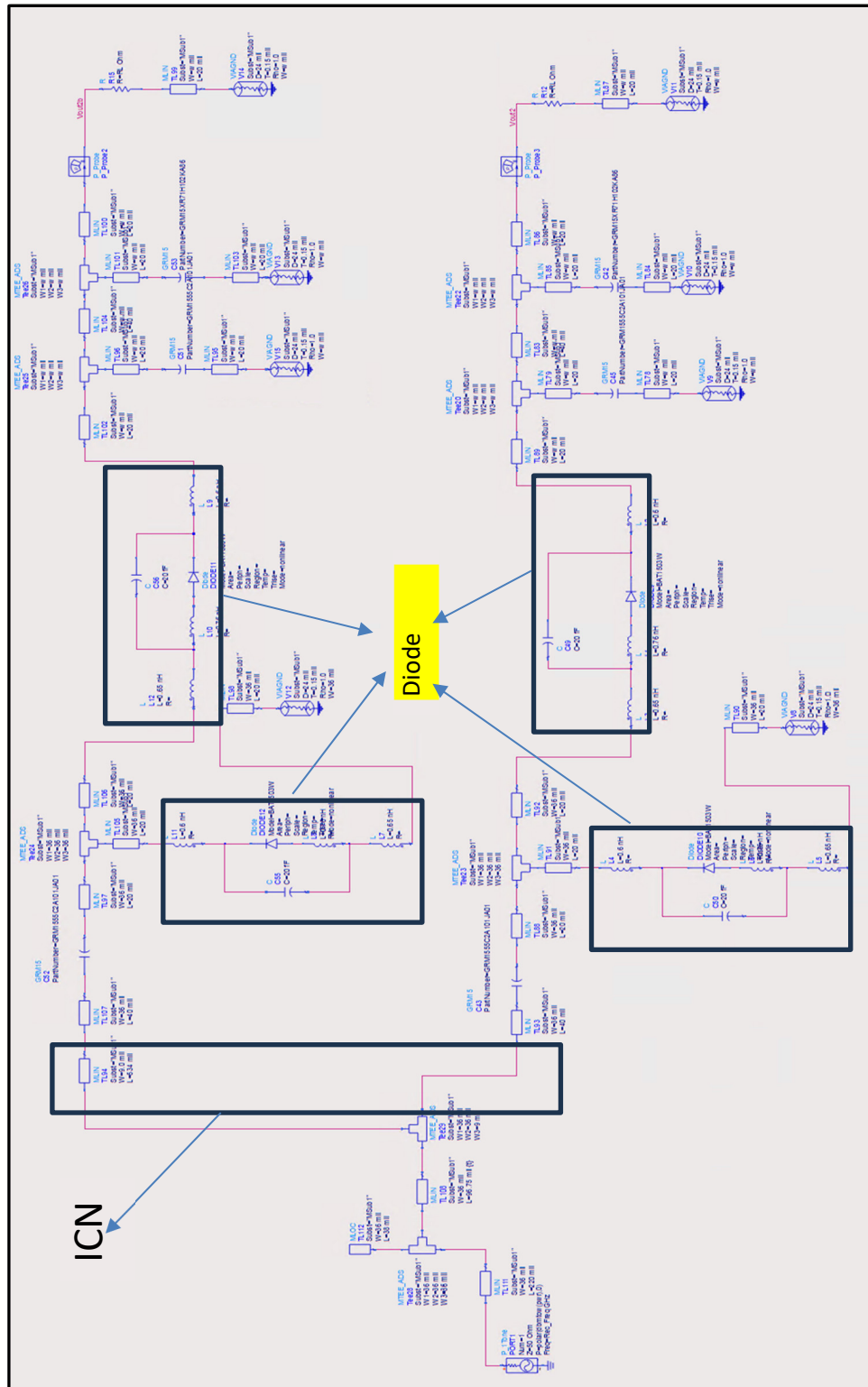
Figure 3.7   Schematic of rectifier used ICN

The ICN and matching circuits are designed based on 3.5GHz at 23 dBm of the input power. The first interesting aspect is the power range under which the designed rectifier still has a good input matching, say Return loss > 15dB. The input matching characteristics are obtained and illustrated in Figure 3.8 by sweeping the input power in a large-signal S-parameter simulation. One can find that the return losses with the input power from 15 dBm to 28 dBm is better than 15 dB.
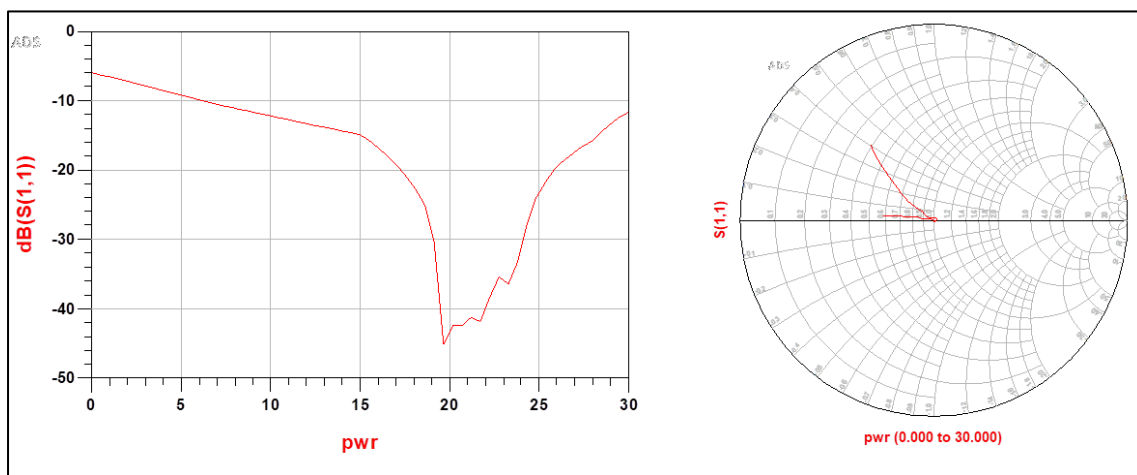
Figure 3.8   Input matching over power sweeping

Furthermore, input matching over frequency can be obtained by fixing the input power to 23 dBm and sweeping the RF frequency, as demonstrated in Figure 3.9. It can be observed that the designed rectifier presents a wide operating band from 2.5GHz to 5GHz regarding 15dB of Return loss.
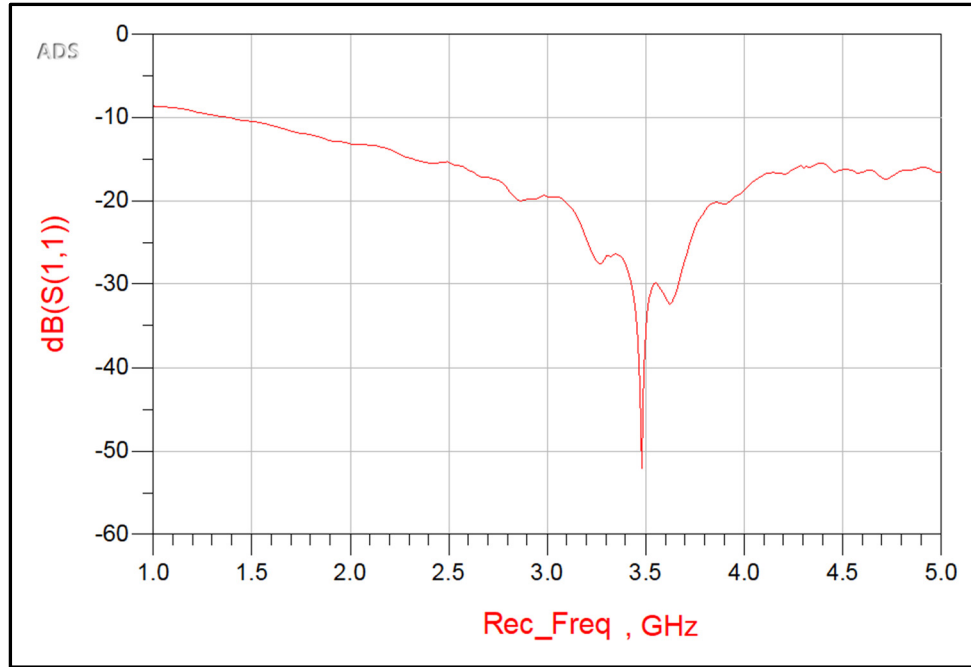
Figure 3.9   Input matching over frequency sweeping

Finally, the large-signal power-sweep simulations are conducted to obtain the relation between the rectifier input power P_{Rec_in} and its DC output power P_{Rec_out}. The efficiency of the designed rectifier can be calculated as Equation 3.2

$$\eta_{Rec} = \frac{P_{Rec\_out}}{P_{Rec\_in}} \cdot 100\% \qquad\qquad (3.2)$$

In which, $P_{Rec\_out} = \frac{V_{Rec\_out1}^2}{R_{Load1}} + \frac{V_{Rec\_out2}^2}{R_{Load2}}$. By reading the DC output voltages, V_{Rec_out1} and V_{Rec_out2}, of two sub-rectifier branches which with a $R_{load1} = R_{load2} = 220 \ \Omega$ respectively, the efficiency at the different input powers can be obtained.

The simulation is repeated at multiple frequency points from 1.2GHz up to 4.5GHz. The characteristic traces between the efficiency and the input power at four typical frequencies, 1.5GHz, 2.4 GHz, 3.5GHz, and 4.5GHz, are illustrated in Figure 3.10. It can be observed that:

a.) The efficiency increases almost linearly when the input power increases from 0 dBm to around 20 dBm. The diode exponential V-I characteristic may be the main dominant factor for this linear characteristic.

b.) When the input power is around 19 dBm ~ 23 dBm, the efficiency reaches the maximum value of around 69% ~ 74% at all four simulated frequencies.

c.) When the input power increases beyond 23dBm, the efficiency decreases dramatically. This phenomenon is related to the reverse breakdown characteristic of the diode.
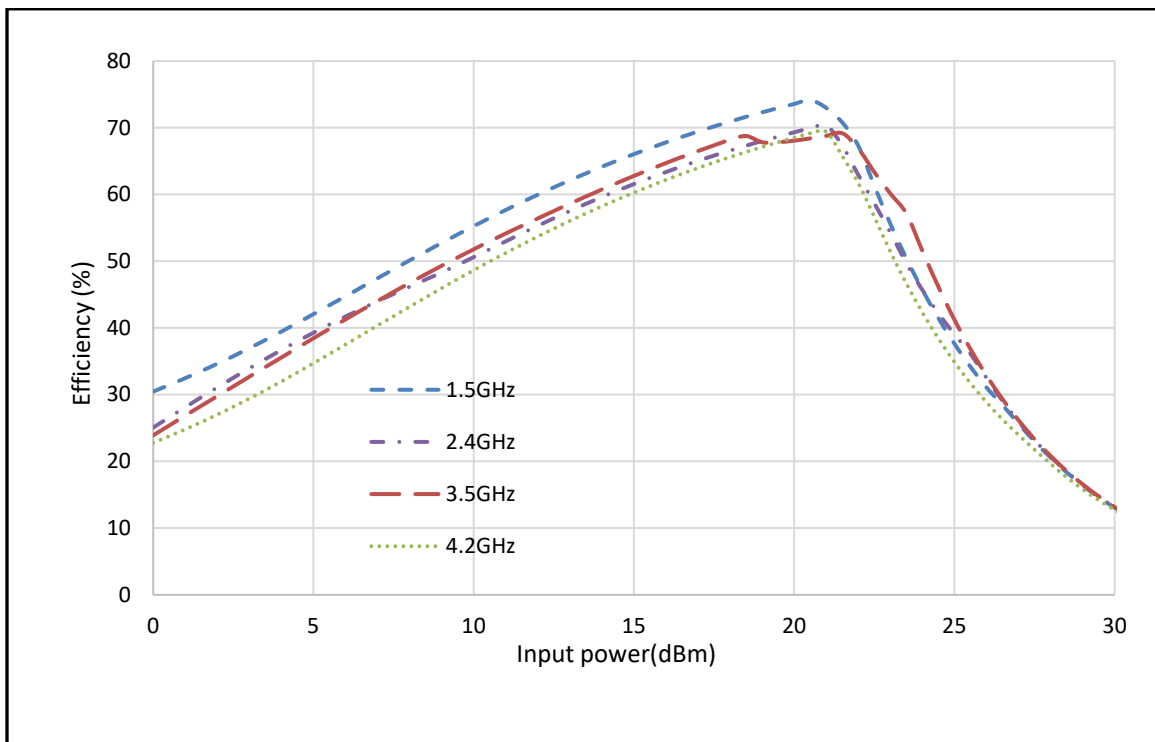
Figure 3.10   Rectifier Efficiency Vs. Input power under different frequencies

3.3　　　　Implementation and Measurement

Based on the simulation in Section 3.2, one rectifier prototype is fabricated, as shown in Figure 3.11. The physical dimension of the transmission lines for the matching component and ICN are directly taken from the simulation.
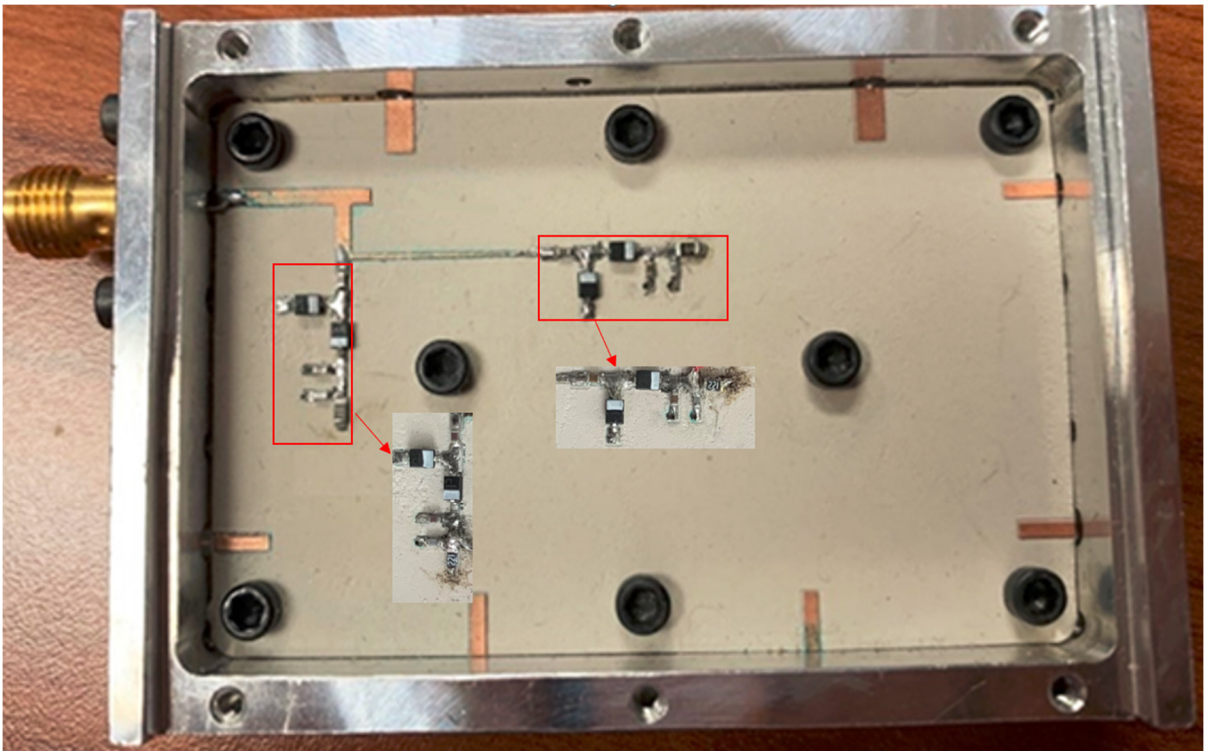
Figure 3.11　　Fabricated prototype of rectifier

The performance of the proposed rectifier is measured with the test bench setup shown in Figures 3.12 and 3.13. A Rohde & Schwarz SMW200A signal generator is used to generate the input signal. Then this signal is amplified by MINI-CIRCITS ZHL-42W, a 34 dB gain amplifier, to output a high-power signal ranging from 0 dBm ~ 24 dBm. This signal is the input of the rectifier under-test. The input signal is calibrated by a power meter (Keysight N1913A) to make sure the power reading is reading accurate. Two multimeters measure the output DC

voltages of the two branches. The efficiency of the designed rectifier can be calculated by using equation 3.2.
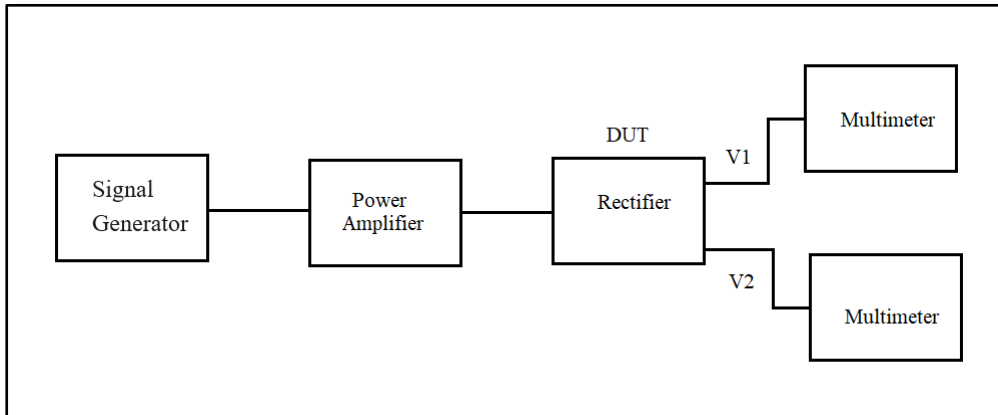
Figure 3.12   Block diagram of the setup of Rectifier measurement
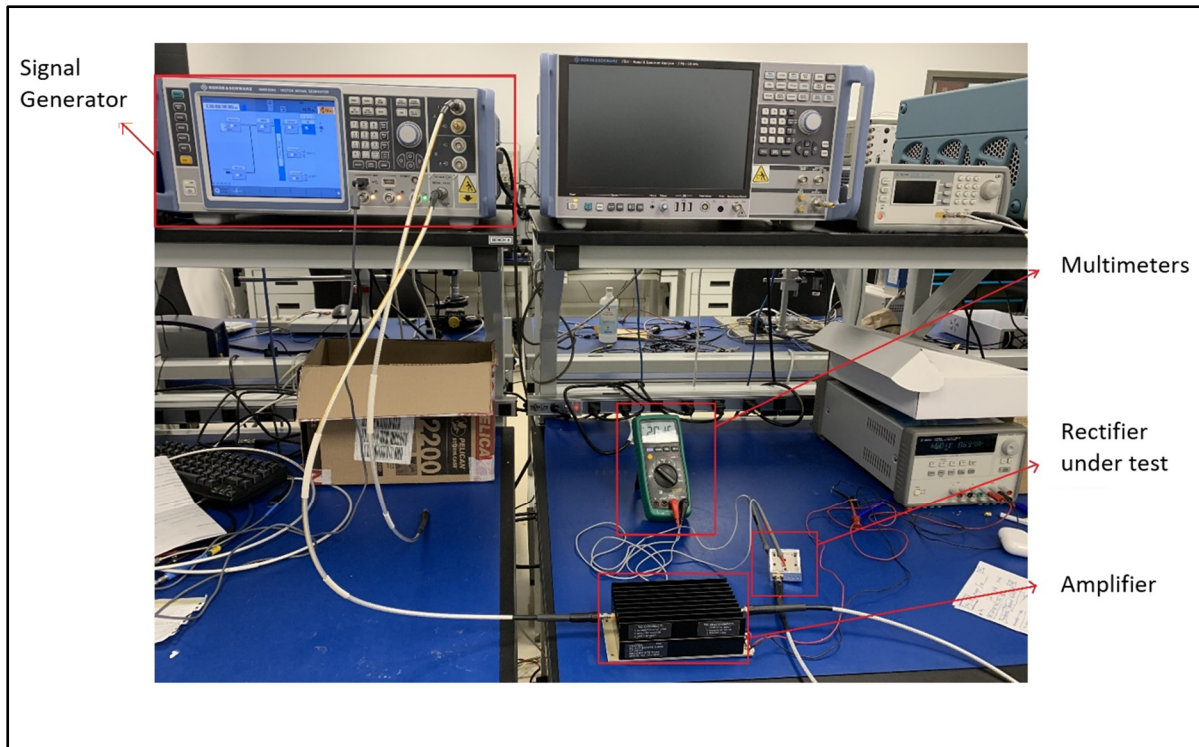
Figure 3.13   Photograph of the experimental rectifier measurement system

The rectifier's efficiency measurement is conducted at 3.5GHz (Figure 3.14) and 2.7GHz (Figure 3.15). In the forthcoming measurement for the combiner and rectifier cascade circuit, the measurement can only be conducted with a frequency less than 3GHz, because the signal generator can only generate a related signal pair up to 3GHz. Therefore, we also measure the rectifier's efficiency at 2.7GHz as a reference in this section. The comparisons between the measured and simulated results are shown in Figure 3.14 and Figure 3.15. From the curves, it can be seen that the measured efficiency presents a similar trend as the input power varies. The measured maximum efficiency at 3.5GHz reaches 66.2% at 20 dBm, slightly less than the simulated one. The measured maximum efficiency at 2.7GHz is 61.6% which also happens when the input power is 20dBm.
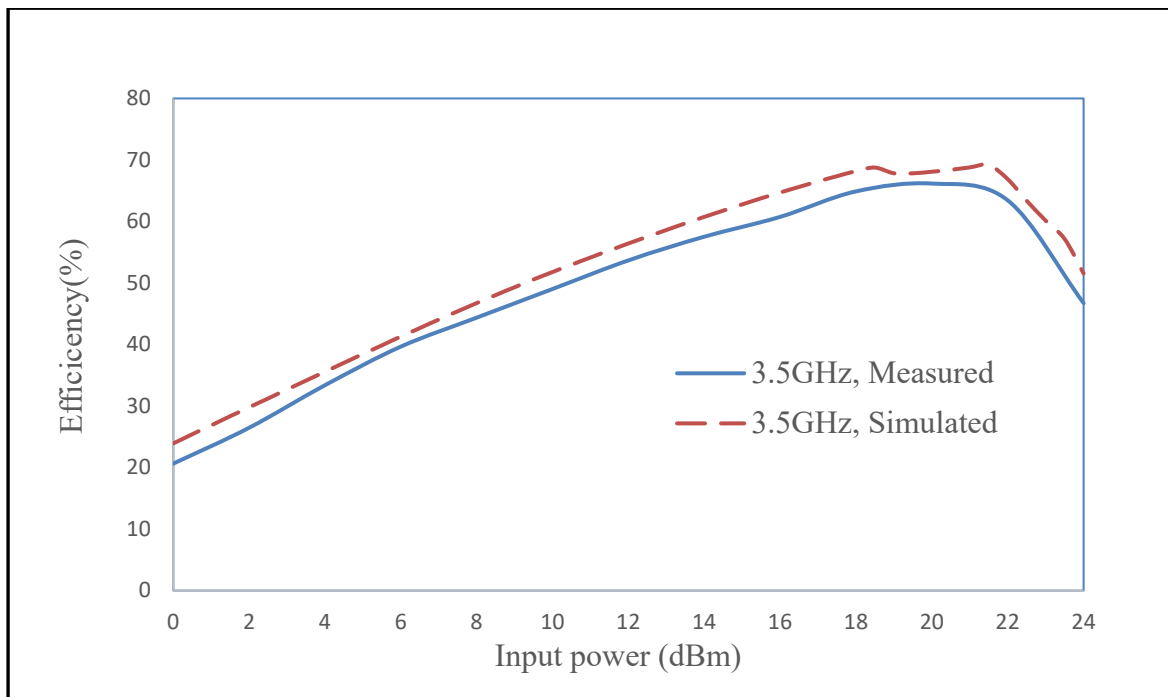
Figure 3.14 Comparison of Simulation and Measured
efficiency of rectifier at 3.5 GHz
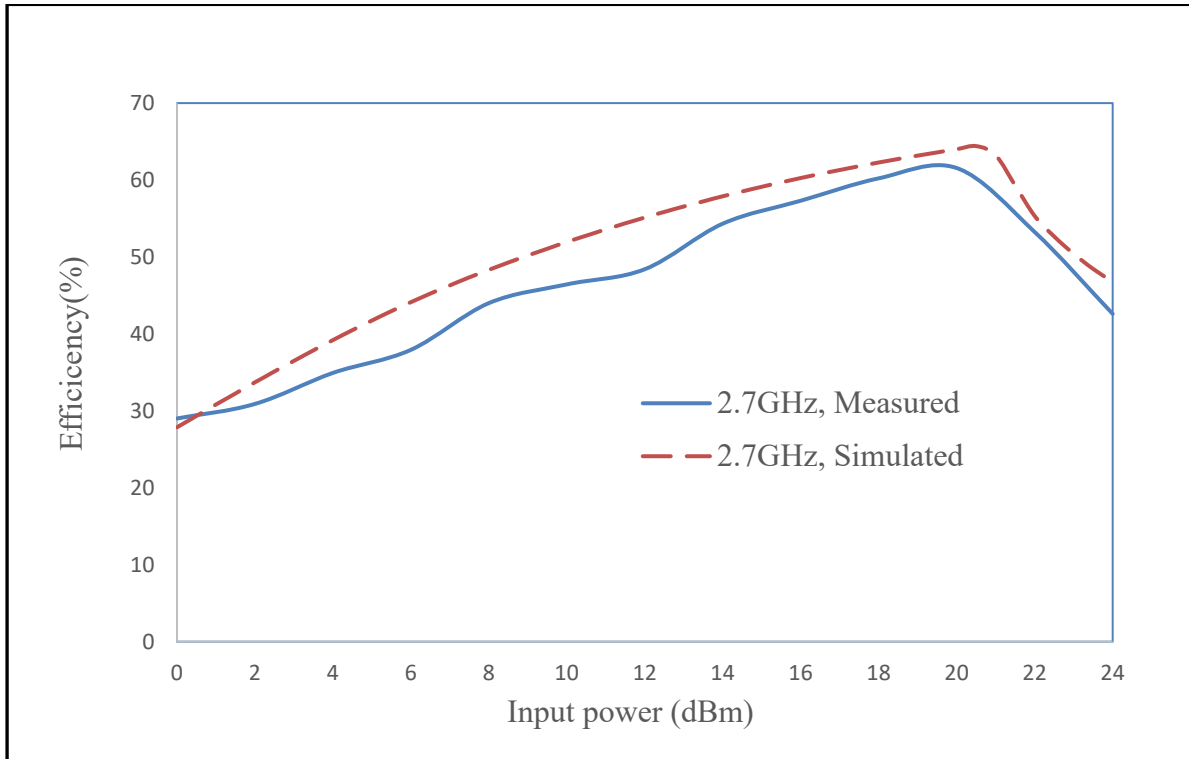
Figure 3.15 Comparison of Simulation and Measured
efficiency of rectifier at 2.7GHz

3.4   Results and Discussion

As depicted in the last section, the proposed rectifier can achieve a measured maximum rectifying efficiency of 66.2% by designing one ICN and matching the network with 20 dBm RF input signal power at 3.5GHz. It is also observed that from 6 dBm to 24 dBm, the designed circuit gives over 40% of the rectifying efficiency.

The proposed rectifier's performance is compared to other related works, as tabulated in Table 3.1. In [Tzu Han Wang. (2017)], one power recycling circuit working at 836MHz was presented with 52% of the maximum RF-DC conversion efficiency when the duty cycle is 50%. In [Rotenberg. (2020)], a power reuse circuit working at 1.96GHz provides a maximum

reuse efficiency of over 60%. However, because no impedance compression network is used in these two techniques, the efficiency of the rectifying circuit quickly deteriorates when the input power deviates from the maximum efficiency-optimized level. The work in [Rotenberg. (2020)] has a 9 dB power range with over 40% efficiency. The different impedance compression network techniques are applied in the work [Junfeng Xu. (2013)] and [Zhi-Xia Du (2018)]. The work in [Zhi-Xia Du (2018)] presents a 17 dB of power range for over 40% efficiency, and maximum efficiency reaches 79%. The operating power range is comparable to the proposed work, and the maximum efficiency is higher. But the high efficiency can only be observed in a minimal frequency range. Compared to the performance of these previous works, the proposed design provides a good compromise regarding the input power range and frequency range, which makes it an up-and-coming candidate for practical LINC applications.

Table 3. 1

Comparison of performance of rectifier

Ref.	Frequency	Maximum rectifying efficiency	Power range of over 40% Eff.
[Tzu Han Wang. (2017)]	836.5MHz	52%	N/A
[Rotenberg. (2020)]	1.96GHz	60% at 20dBm	14dBm ~ 25 dBm
[Junfeng Xu. (2013)]	4.6 GHz	56% at 31dBm	27dBm ~ 34.77 dBm
[Zhi-Xia Du (2018)]	2.45GHz	79% at 18.4dBm	3.2dBm ~ 20.4 dBm
This work	3.5GHz	66.2% at 20dBm	6dBm ~ 24 dBm

CHAPTER 4

OVERALL PERFORMANCE EVALUATION OF INTEGRATED COMBINER AND RECTIFIER

4.1   Introduction

In Chapter 2, one combiner was designed and verified. In Chapter 3, a rectifier with an impedance compression network was also designed and measured. These two circuits need to be cascaded to build a complete combiner for LINC PA power recycling and to collect the power in the out of phasing signals of the two saturation PAs and convert it to DC power. This chapter presents the integration and evaluation of the overall performance of the cascaded circuits.

As depicted in Figure 2.3 and Figure 3.1, the recycling efficiency is given by 4.1.

$$\eta_{Rec_{out}} = \frac{P_{Rec\_out}}{P_{in\_1} + P_{in\_2}} \cdot 100\% \tag{4.1}$$

The RF output efficiency at the summing port of the combiner, which is the combiner's efficiency of a LINC comply with LC Balun combiner, is given by 4.2.

$$\eta_{\Sigma\_out} = \frac{P_{\Sigma\_out}}{P_{in\_1} + P_{in\_2}} \cdot 100\% \tag{4.2}$$

Thus, the total system efficiency will be the sum of the recycling and combined output signal efficiency,

$$\eta_{total} = \frac{P_{Rec\_out} + P_{\Sigma\_out}}{P_{in\_1} + P_{in\_2}} \cdot 100\% \tag{4.3}$$

P_{in_1} and P_{in_2}, power of $S_a(t)$ and $S_b(t)$, are the two PAs' output powers and the inputs to the combiner. P_{Rec_out} is the power of rectifier output and P_{Σ_out} is the power of Wilkinson summing port output.
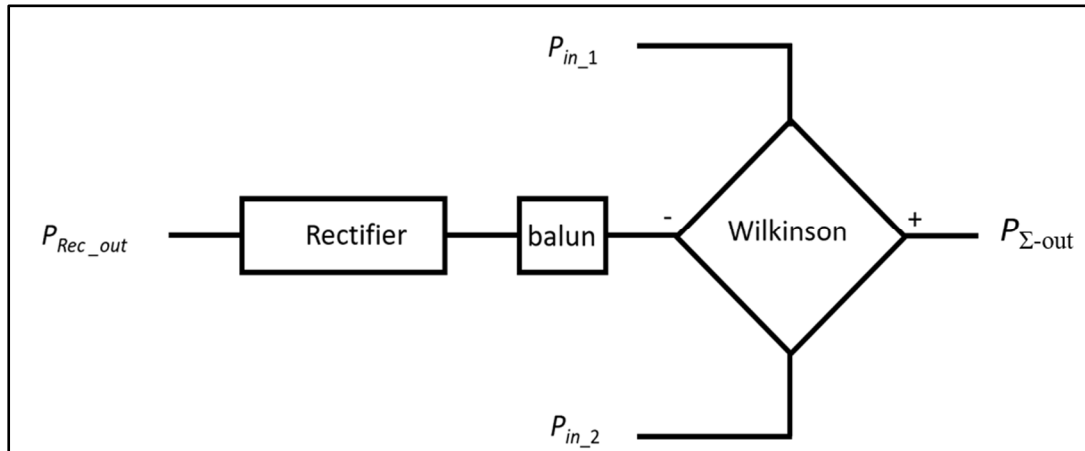
Figure 4.1   Power definition for cascaded circuits

4.2   Test setup

The experimental setup for the overall efficiency measurement is illustrated in Figure 4.2. A Rohde & Schwarz SMW200A Signal Generator with two RF output channels is used in place of two saturated PAs. The two output signals of the two channels are phase-related. Therefore, the phase difference between two signals can be adjusted in Signal Generator's user interface. Two isolators are added between the amplifier and combiner input to provide a good match for the combiner. After eliminated the loss of the cables and isolators, power at the Wilkinson combiner two input ports achieved an adequate power range from 0 to 20 dBm. Two multimeters are used to measure the DC voltages of the rectifier outputs. Meanwhile, one power meter measures the output RF power at the combiner's power-combining port.

Figure 4.2   Block diagram of the setup of Wilkinson measurement

Figure 4.3   Photograph of the experimental integrated circuit measurement system

4.3   Measured results

The measurements are conducted at 2.7GHz with two input signals setting to the power range from 0 dBm to 20 dBm with a 2 dB step. At each power level, the RF output power at the summing port and th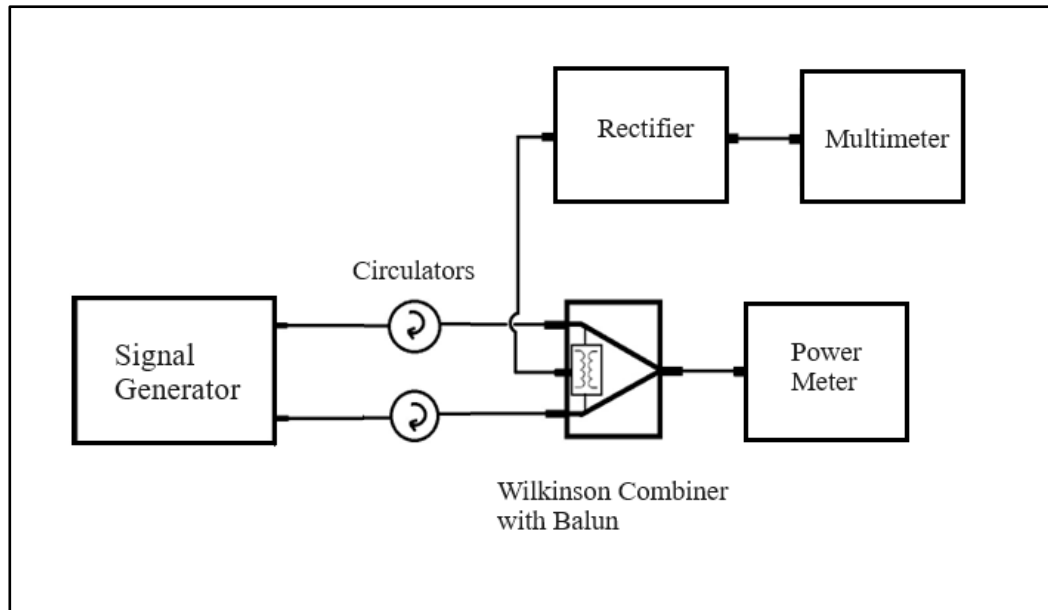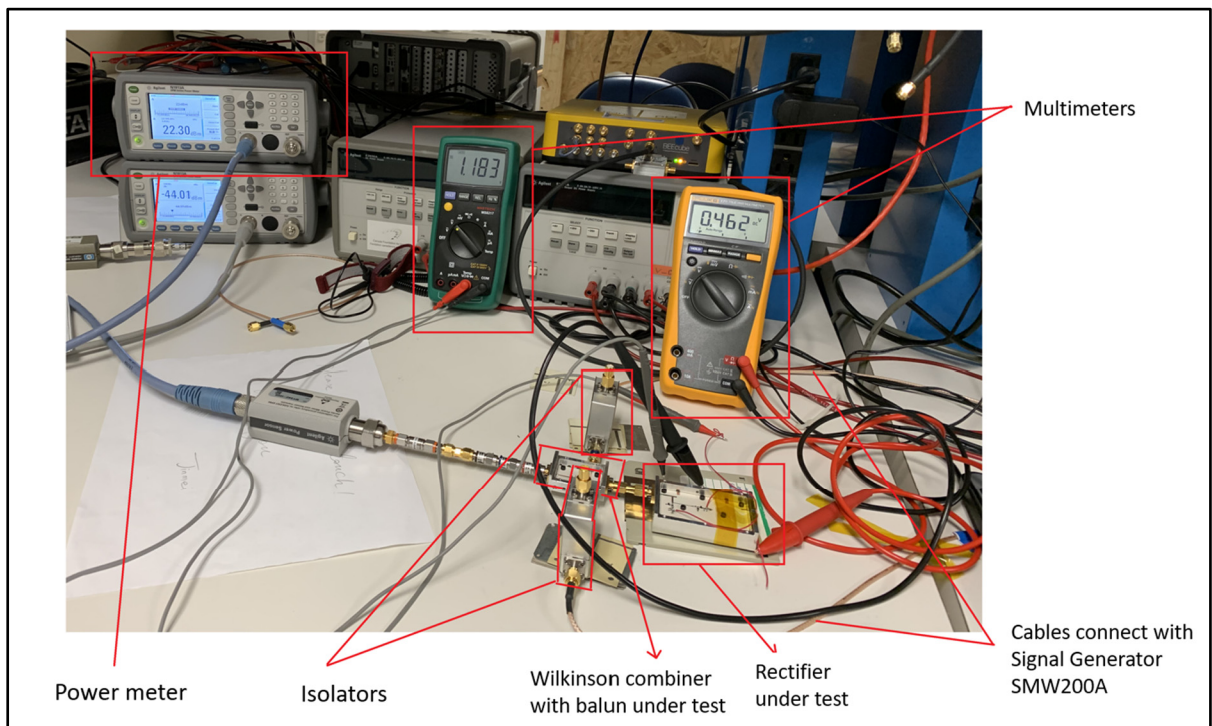e total rectified DC powers are recorded with the change of the two input signals' phase difference. The measured results are shown in Figures 4.4 (a)-(k). It can be observed that,

(a) For all the power levels measured, when the two input signals' phase difference is 0°, the RF summing port efficiency reaches the maximum of 92%. This is determined by the Wilkinson combiner's summing port efficiency and coincides with the results in Figure 2.19. The RF summing port efficiency reaches zero when the input signal phase difference is 180°.

(b) For all the power levels measured, when the input signal phase difference is 180°, the DC power collected through the rectifier reaches the maximum, and DC rectifying efficiency also reach the maximum. At the same time, the DC rectifying efficiency becomes zero when the input signals are in-phase.

(c) When the input power is 0 dBm, the maximum efficiency of the DC rectifying is only 17%, as shown in Figure 4.4(a). With the increase of the input power, it increased accordingly. With 20 dBm of the input power, the maximum efficiency of the DC rectifying can reach 53.5%.

(d) The total efficiency is the sum of the RF summing efficiency and DC rectifying efficiency. When the input signal phase difference is around 0°, the input power is delivered to the RF summing output port, and RF summing efficiency is the dominant contributor to total efficiency. When the input signal phase difference approaches 180°, the input power is delivered to the combiner's difference port, and DC rectifying efficiency is the dominant contributor to total efficiency. In this design, because the maximum DC rectifying efficiency is less than the RF summing efficiency, the total efficiency at $\theta_d = 0°$ is larger than the one at $\theta_d = 180°$.

(a) for input power set to 0dBm

(b) for input power set to 2dBm

(c) for input power set to 4dBm
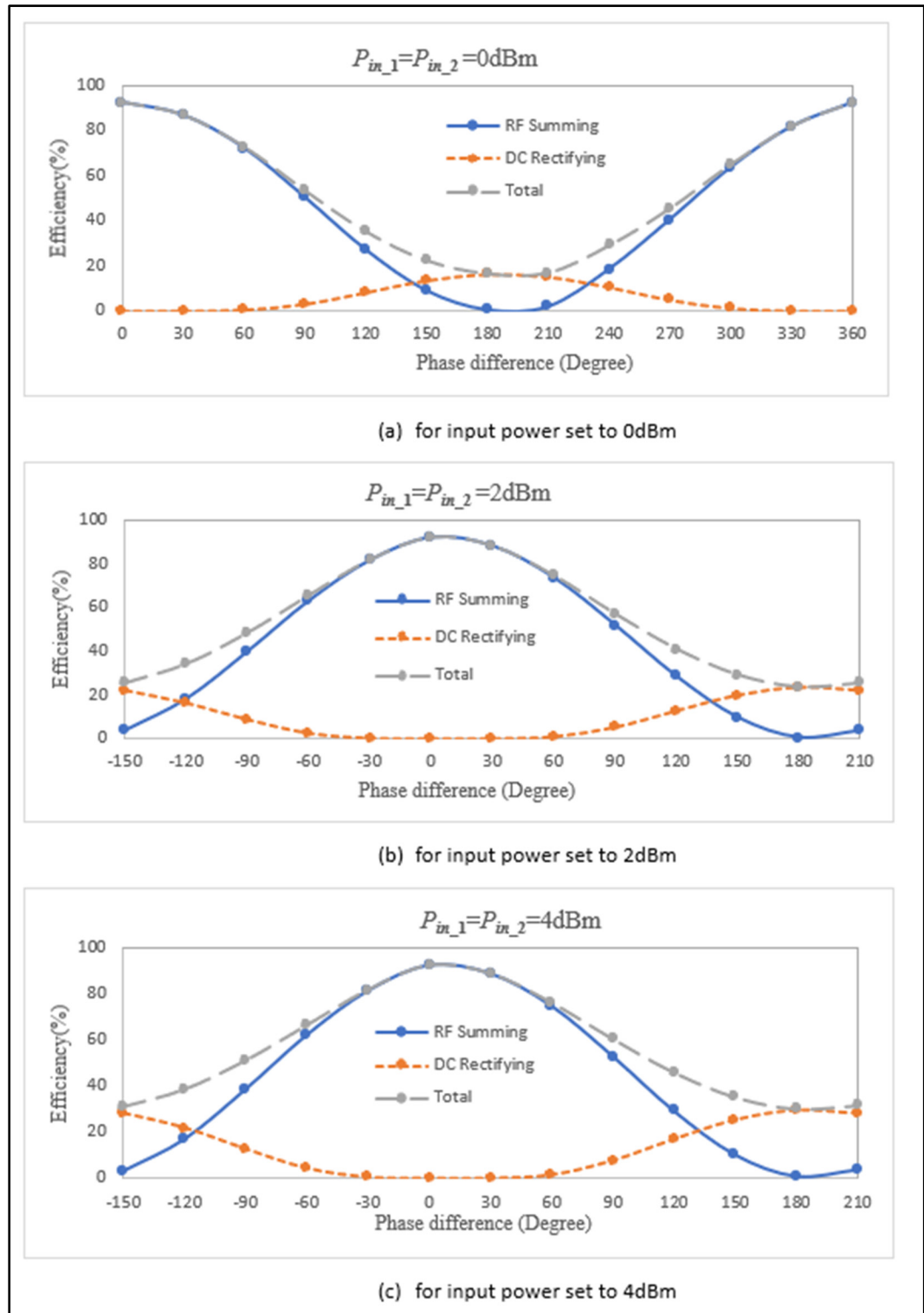
Figure 4.4   Efficiency of the integrated circuit

(d) for input power set to 6dBm

(e) for input power set to 8dBm

(f) for input power set to 10dBm
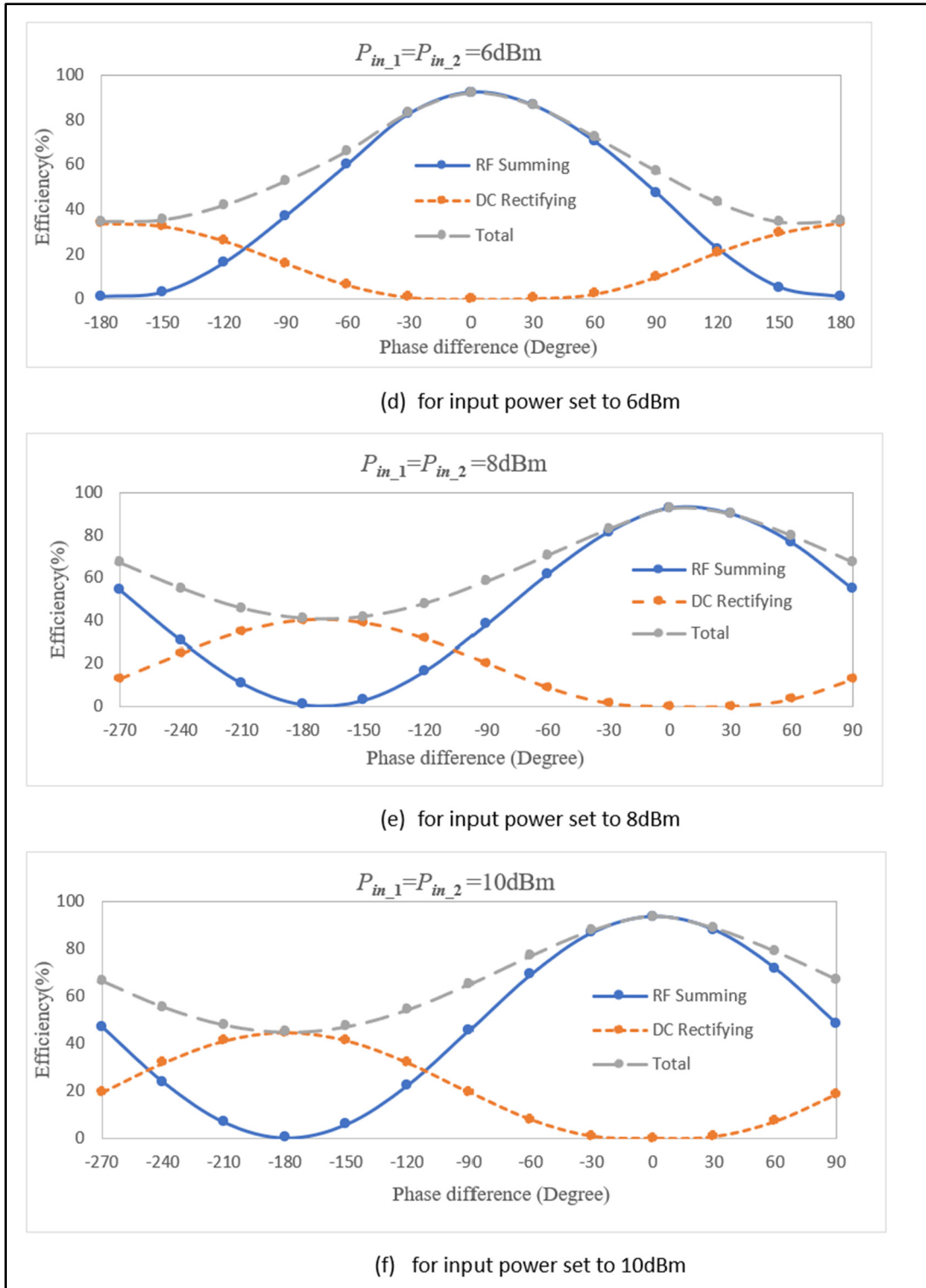
Figure 4.5   Efficiency of the integrated circuit (Continue)

(g) for input power set to 12dBm

(h) for input power set to 14dBm

(i) for input power set to 16dBm
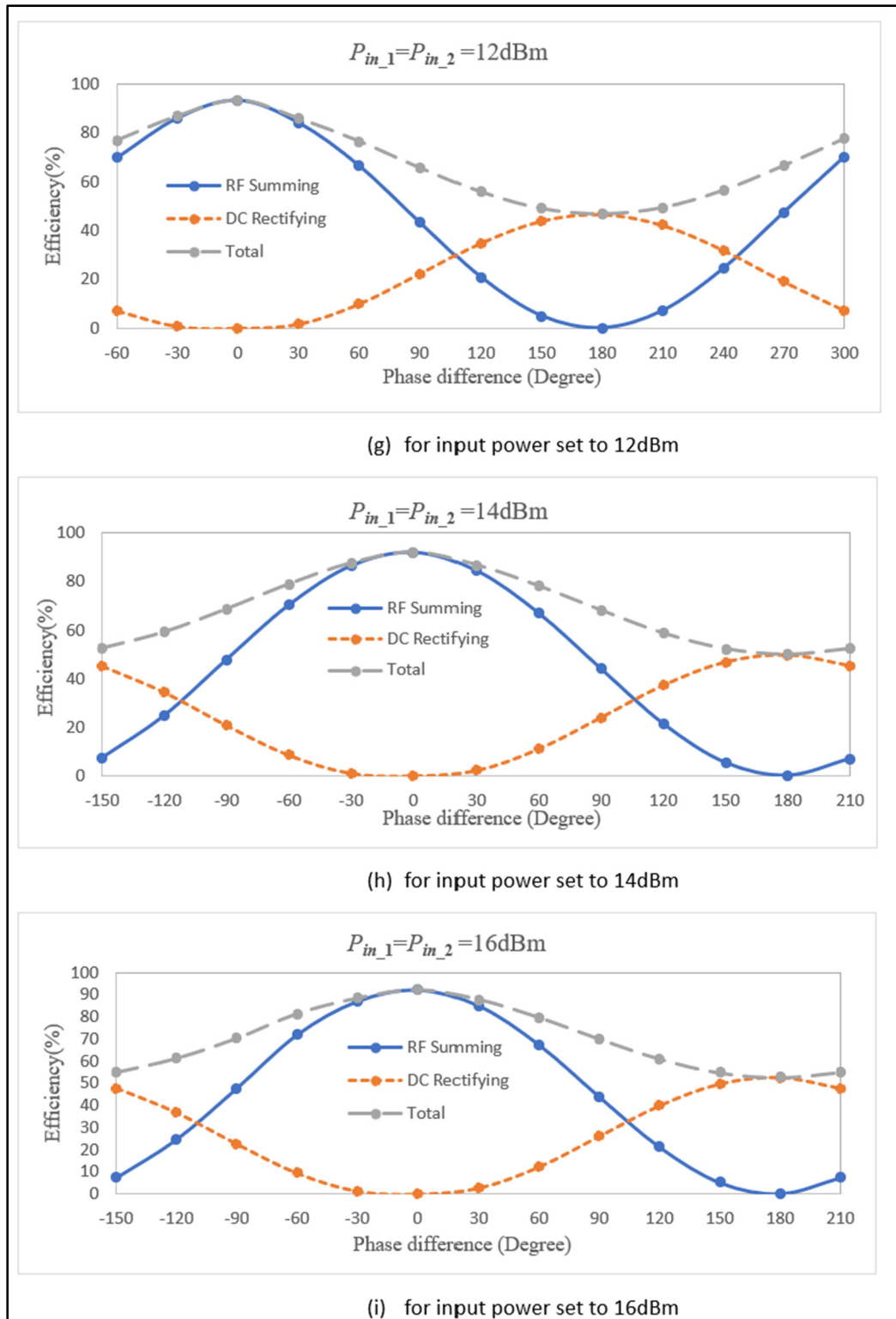
Figure 4.6   Efficiency of the integrated circuit (Continue)

(j) for input power set to 18dBm

(k) for input power set to 20dBm
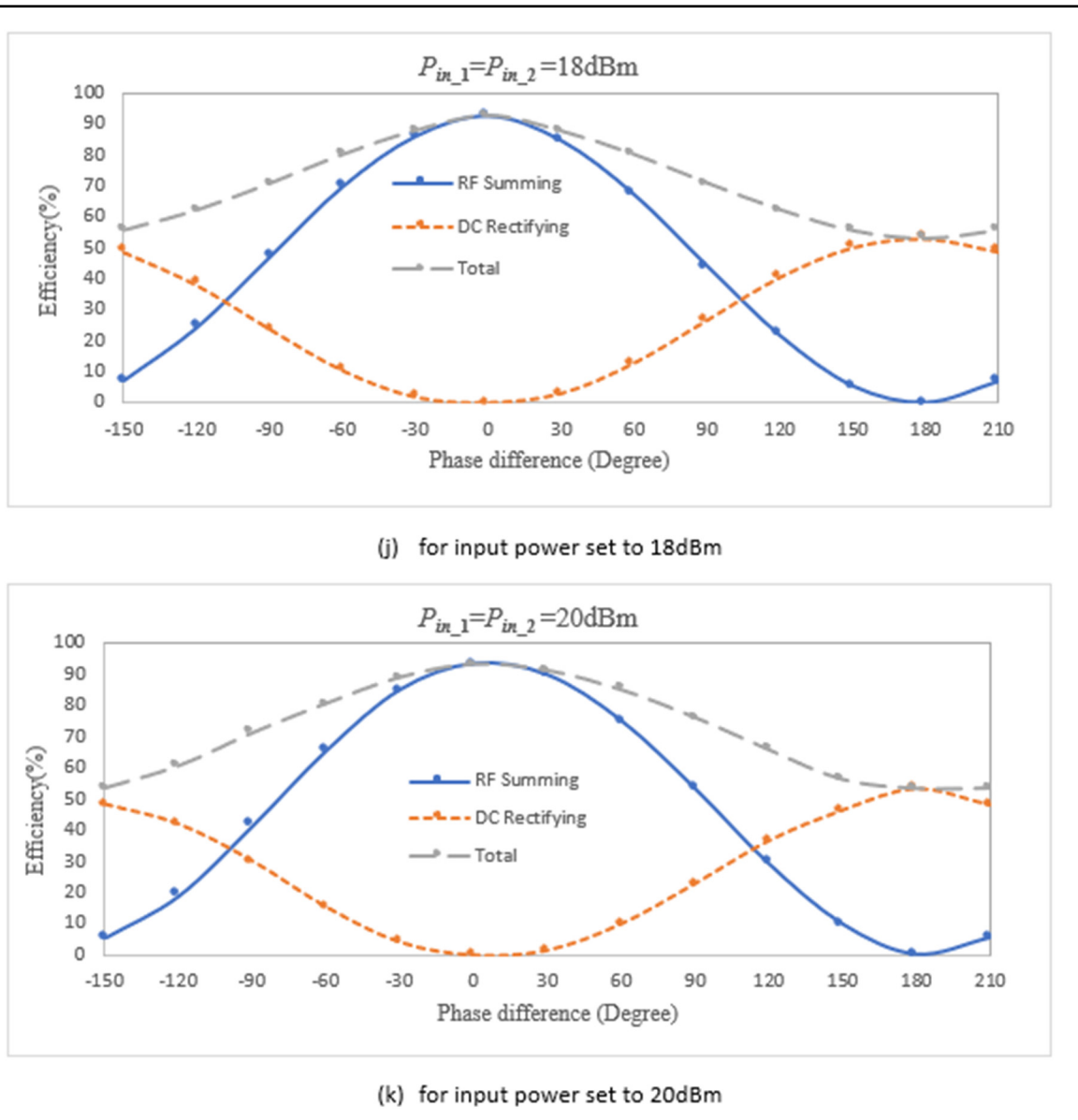
Figure 4.7 Efficiency of the integrated circuit (Continue)

4.4   **Discussion**

As discussed in Chapter 2, 92% of the RF power efficiency can be achieved at the combiner's difference port. Furthermore, the designed rectifier can achieve around 66.2% of the DC rectifying efficiency with one ICN and matching network. By cascading two circuits together, 53.5% of DC power recycling efficiency is observed with 20 dBm RF input signal power at 2.7GHz. It is also observed that from 8 dBm to 20 dBm, the designed circuit can present larger than 40% of efficiency, which makes it an up-and-coming candidate for practical LINC applications.

CONCLUSION & RECOMMENDATIONS

This project aimed to design a power combiner that could be used in the LINC power amplifier to rectify the power normally dissipated on the resistor as heat. By using this technique, we aimed to improve the efficiency of the LINC PA. To achieve this, we explored a different design approach, which involved combining the traditional Wilkinson combiner with the LC Balun and rectifier in one circuit to create a modified Wilkinson power combiner for the LINC PA.

The LINC PA uses a combiner like the Wilkinson combiner. It uses a 100Ω resistor to isolate the two input signals. When two input signals are in the differential phases, the RF power is dissipated as heat through the 100 Ω Resistor. This behavior affects the efficiency of the LINC power amplifier. However, when we use an LC Balun and rectifier circuit is used to replace the 100 Ω resistors, we convert the power that should have been lost as heat into DC, which can be used as a power source to supply other circuits. Therefore, we designed a modified Wilkinson power combiner by replacing the 100 Ω resistors of the traditional Wilkinson combiner with the LC Balun design and rectifier.

Through measurements of the total design, we found that the efficiency of the combiner is highly dependent on the phase relationship between the two input signals. That matches exactly the theory. The combiner can achieve maximum output power when the two input signals, $S_a(t)$ and $S_b(t)$, are in the same phase. On the other hand, when the two input signals, $S_a(t)$ and $S_b(t)$, are in the opposite phase, the combiner achieves a 92% efficiency, which is fed to the rectifier.

For the rectifier, we employed an impedance compression network to reduce the load sensitivity caused by the non-linear nature of diodes. The rectifier allowed us to efficiently convert the RF signal at a desired frequency into a DC voltage to power the other circuitry. The proposed rectifier can achieve 66.2% of the maximum rectifying efficiency with 20 dBm RF input signal power at 3.5GHz. It is also observed that from 6 dBm to 24 dBm, the designed circuit presents over 40% of the rectifying efficiency.

In conclusion, our power combiner and rectifier design allowed us to effectively collect RF energy and convert it into DC voltage, which can be used to power other circuitry. However, further optimization may be needed to achieve higher efficiency for the RF summing and power recycling section. Overall, the design work in the project provides a good candidate for practical LINC applications to achieve high power-recycling efficiency.

Based on the results obtained from the measurement of the total design in Chapter 3.3, it was observed that the maximum RF summing port efficiency achieved was not equal to the one achieved from the single Wilkinson combiner. This may be due to the accuracy of the simulation and the fabrication of the PCB. It also could be attributed to the accuracy of the components or the matching of the circuit needing to be further optimized.

Therefore, future work could involve improving the simulation and fabrication process of the PCB and optimizing the circuit matching to enhance the design. Additionally, exploring different types of Baluns and evaluating their performance in this design could be another avenue for improvement.

Furthermore, it would be beneficial to conduct further testing and analysis to examine the impact of varying the operating frequency and input power levels on the power combiner's performance. This could provide valuable insights into the design considerations for the LINC power amplifier.

Overall, the future work for this project involves improving the power combiner performance by optimizing the circuit design, exploring different Baluns, conducting further testing and analysis, and developing an improved system for maximizing power recycling while retaining the characteristic of a conventional Wilkinson power combiner.
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