A Reconfigurable Impedance Matching Network

by

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Réseau d'adaptation d'impédance auto-reconfigurable

Sajjad ATASH BAHAR

RÉSUMÉ

Les dispositifs mobiles et portables modernes dépendent de plus en plus de systèmes RF compacts et efficaces pour maintenir une communication fiable. Dans ces systèmes, les performances de l'étage d'entrée RF sont fortement influencées par les variations d'impédance de l'antenne, l'interaction avec l'utilisateur et les changements dans l'environnement immédiat. Ces facteurs peuvent provoquer des fluctuations importantes de l'impédance de charge, entraînant des désadaptations entre la charge et l'étage RF précédent notamment l'amplificateur, ce qui dégrade la qualité du signal et l'efficacité du transfert de puissance. Pour relever ce défi, un réseau d'adaptation reconfigurable, capable d'un réglage adaptatif, est essentiel.

Dans cette étude, nous présentons un réseau d'adaptation accordable à base de commutateurs, capable de s'ajuster dynamiquement aux variations d'impédance. Le système proposé se compose de trois sous-systèmes principaux : un bloc de mesure intégré, un bloc de contrôle et un bloc d'accord. Le système commence par mesurer le coefficient de réflexion d'entrée afin d'évaluer le niveau de désadaptation. Sur la base de cette mesure, l'unité de contrôle détermine la configuration optimale des commutateurs dans le bloc d'accord. Ces commutateurs sont ensuite activés en conséquence afin de reconfigurer le réseau et minimiser la désadaptation d'impédance.

Mots-clés: réseau d'autoréglage intégré

A Reconfigurable Impedance Matching Network

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ABSTRACT

Modern mobile and wearable devices increasingly rely on compact and efficient RF systems to maintain reliable communication. In these systems, the performance of the RF front-end is highly influenced by variations in antenna impedance, user interaction, and changes in surrounding materials. These factors can cause significant fluctuations in load impedance, leading to mismatch conditions between the load and the preceding RF stage—ultimately, notably the amplifier, degrading signal quality and power transfer efficiency. To address this challenge, a reconfigurable matching network is essential. Moreover, such a network must be compact and suitable for integration with embedded systems,in oder to minimize the increase in size and weight.

In this study, we present a SPDTs-based tunable matching network capable of adjusting to varying impedance conditions. The proposed system consists of three primary subsystems: an embedded measurement block, a control block, and a tuning block. The system begins by measuring the input reflection coefficient to evaluate the level of mismatch. Based on this measurement, the control unit determines the optimal configuration of the switches in the tuning block. These switches are then set accordingly to reconfigure the network and minimize the impedance mismatch.

Keywords: Impedance matching networks, Embedded tuning network

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LIST OF ABBREVIATIONS

ADC	Analog to Digital Converter
DAC	Digital to Analog Converter
RF	Radio frequency
CDMA	Code-division multiple access
SDR	Software-defined radio
TMN	Tunable Matching Networks
SPST	Single-Pole Single-Throw
SPDT	Single-Pole Double-Throw
AI	Artificial intelligence
CAD	Computer-Aided Design
IoT	long=Internet of Things
TL	Transmission lines
QFN	Quad flat No-Lead Package
PCB	Printed Circuit Board
SMD	Surface Mount Device
DUT	Device Under Test
VNA	Vector Network Analyzer

LIST OF SYMBOLS AND UNITS OF MEASUREMENTS

A	ampère
mA	mili-ampère
μA	micro-ampère
V	volt
mV	mili-volt
μV	micro-volt
W	watt
mW	mili-watt
μW	micro-watt
nW	nano-watt
s	second
ms	mili-second
μs	micro-second
ns	nano-second
Ω	ohm
F	Farad
Hz	Hertz

INTRODUCTION

In the rapidly advancing field of telecommunications, the demand for high-performance and efficient systems is continually on the rise. As telecommunication networks strive to meet the ever-increasing data transmission requirements, the design and optimization of critical components become paramount. Among these components, transmission lines, power amplifiers, and matching networks play pivotal roles in ensuring optimal signal transfer and power transmission.

Transmission lines serve as essential elements for signal propagation between different sections of a communication system. They are responsible for facilitating the transmission of electromagnetic waves from source to load while maintaining signal integrity. These transmission lines are crucial in various applications, including connecting antennas to transmitters or receivers, connecting different circuit blocks within a system, and linking subsystems in complex telecommunications networks.

Power amplifiers, on the other hand, are key components that significantly impact the overall performance of a telecommunication system. Their primary function is to amplify weak input signals to a level suitable for efficient transmission. Power amplifiers are employed in a wide range of applications, such as wireless communication systems, satellite communications, radar systems, and broadcasting. Achieving high power efficiency, linearity, and wide bandwidth are key objectives in power amplifier design to ensure reliable and robust signal amplification.

One critical aspect of telecommunications systems is the efficient transfer of power from the amplifier to the load. The load represents the impedance presented by the receiving device or the transmission line termination. Mismatch between the power amplifier output impedance and the load impedance can lead to signal reflections, power loss, and reduced overall system performance. Therefore, the use of matching networks becomes essential to ensure impedance matching between the power amplifier and the load, maximizing power transfer efficiency.

Matching networks are specialized circuits designed to overcome impedance mismatches and optimize power transfer between interconnected components in a telecommunication system. They play a crucial role in various RF and microwave circuits, including amplifiers, mixers, oscillators, antennas, and power dividers/combiners. By providing a proper impedance transformation, matching networks enable efficient power transfer, minimize signal loss, and improve system performance.

The reflection coefficient is a parameter used to quantify the amount of reflected wave at the interface between two transmission lines or components. The reflection coefficient between a transmission line and a load depends on the impedance of the load and the characteristic impedance of the transmission line. The reflection coefficient, denoted by Gamma (Γ), is a complex quantity that represents the magnitude and phase of the reflected wave at the interface between the transmission line and the load.

In telecommunication/electronic systems, the reflection coefficient at the interface of two components depends on the impedance characteristics of both components. Altering either impedance disrupts the proper matching between the two components. Such changes can occur due to various factors, such as frequency variations or modifications in load impedance (e.g., in antennas). Consequently, a variable matching system is necessary for these systems to accommodate these changes.

0.1 Motivation and context

The motivation behind this thesis is to explore, design, and build a integrated system positioned between two blocks within an electronic telecommunication system, as illustrated in Figure 0.1. Specifically, our focus lies in developing a reconfigurable matching network capable of adapting its impedance characteristics in response to changing conditions, frequencies, or requirements. Our aim is to achieve efficient power transfer and optimize system performance without the need for human intervention or decision-making. This reconfigurable matching network will serve as a pivotal component of the overall system, which is designed to detect and rectify the reflection coefficient.

Our investigation will involve a thorough analysis of the problem using a block diagram, identifying the function of each block, and addressing the design and construction challenges associated with creating such a system. Ultimately, this research strives to contribute to the advancement of integrated systems capable of managing the reflection coefficient and enhancing the overall performance of electronic telecommunication systems.

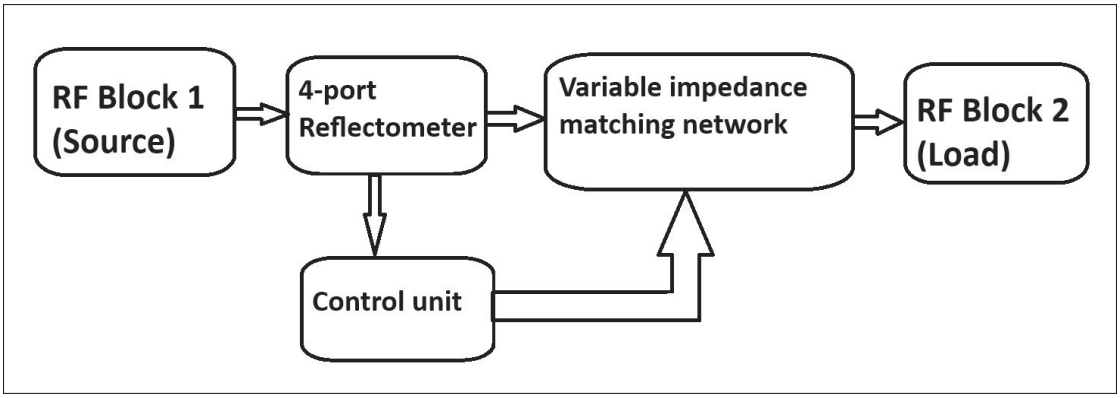


Figure 0.1 Variable matching network block diagram in an RF system

0.2 Research problem

Problem Statement:

The primary challenge addressed in this thesis revolves around the development of an integrated set of RF components capable of measuring the reflection coefficient and providing the necessary information required to manually determine the appropriate matching configuration. The system does not perform automatic or adaptive tuning. Instead, it focuses on accurately extracting the reflection characteristics so that the control unit can evaluate all predefined configurations and select the most suitable one based on measured data.

To achieve this objective, several specific technical challenges must be addressed within the individual system blocks:

Embedded Reflection Coefficient Measurement Problem:

The measurement challenge is centered on designing and implementing an embedded system capable of accurately assessing power levels on the transmission line. This requires integrating suitable measurement techniques into the RF front-end, ensuring high sensitivity and precision within the constraints of the embedded environment, and addressing challenges such as noise, and calibration drift. The embedded measurement system must provide reliable, information about impedance mismatch to the control unit, enabling adjustment of the variable impedance matching network.

Variable Impedance Matching Network Problem:

The problem associated with the variable impedance matching network is the development of a reconfigurable matching network capable of adjustment of its impedance characteristics. This entails exploring different circuit topologies, component selection, and control techniques to achieve efficient impedance matching. The challenge lies in creating a variable impedance matching network that can seamlessly adapt to varying load impedance, source impedance, or environmental factors while maintaining low loss, high efficiency, and robust performance.

In summary, the thesis addresses the complex problem of creating a integrated system that can detect and rectify the reflection coefficient within an electronic telecommunication system. This involves intelligent control, precise reflection coefficient measurement, and impedance matching, with the overarching goal of optimizing system performance without the need for human intervention.

0.3 Objective

The overall objective of this thesis is to develop an RF system for the efficient management and adjustment of reflection coefficients in an RF circuits. Achieving this entails three sub-objectives for each of the subsystem's main blocks.

Control Unit:

Objective: To provide control capabilities to the system.

Subject:The control unit collects and processes the information, and ultimately applies the necessary adjustments to the controllable part of the circuit

Embedded measurement:

Objective: To measure and monitor the reflection coefficient in the system.

Subject: Designing and implementing detectors capable of accurately measuring the reflection coefficient.

Focus: Selecting suitable detection techniques, ensuring high sensitivity and precision, addressing challenges like noise and signal integrity, and providing reliable information about impedance mismatch to the control unit for efficient decision-making and adjustment of the variable impedance matching network.

Variable Impedance Matching Network:

Objective: To adjust impedance for optimal matching between the source and load.

Subject: Designing a reconfigurable matching network capable of real-time impedance adjustment.

Focus: Exploring different circuit topologies, component selection, and control techniques to achieve efficient impedance matching.

Challenge: Developing a variable impedance matching network that adapts to varying load impedance, source impedance, or environmental factors while maintaining low loss, high efficiency, and robust performance.

Integration:

The integration and coordination of the control unit, detectors, and variable impedance matching network are essential to detect and rectify the reflection coefficient in the electronic telecommunication system.

In summary, the goal of the thesis centers on achieving reflection coefficient management within an electronic telecommunication system. This involves developing control strategies, precise reflection coefficient measurement, and impedance matching techniques, all working together to optimize system performance.

0.4 Thesis organization

The rest of the thesis is organized in three chapters. The first chapter investigates different types of matching networks and methods for measuring the reflection coefficient. The second chapter provides a detailed description and expansion of the employed methodology. Finally, the third part presents the measurement results and fabrication results.

CHAPTER 1

LITERATURE REVIEW AND BACKGROUND

1.1 Matching Networks

Matching networks, Figure 1.1, play a crucial role in electrical and communication systems by ensuring impedance matching between interconnected components. They facilitate efficient power transfer and minimize signal reflections, thereby optimizing system performance. Here are some commonly used types of matching networks:

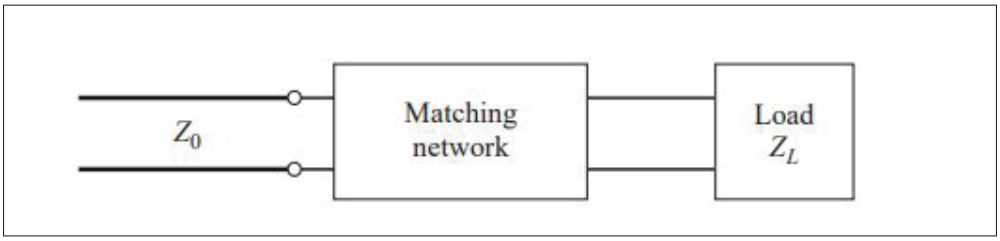


Figure 1.1 An ordinary matching network block diagram
Taken from Pozar (2000)

L-Matching network: The L-matching network Figure 1.2, consists of two reactive elements connected in an "L" configuration. It is widely used for impedance matching in RF circuits. The L-network can transform the impedance from a high value to a lower value or vice versa, depending on the component values.

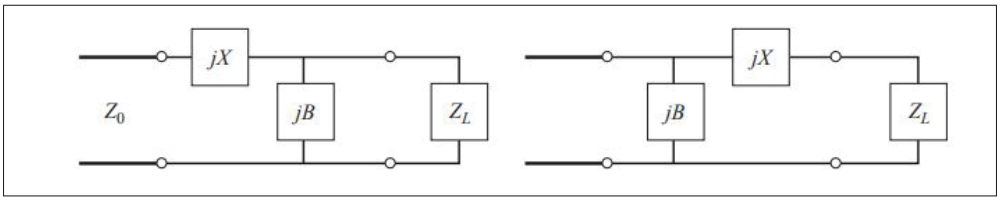


Figure 1.2 L-section matching networks
Taken from Pozar (2000)

π-Matching network: The π-matching network, Figure 1.3, utilizes three reactive elements connected in a π configuration. It is effective for achieving impedance matching and is commonly used in Radio frequency (RF) amplifiers. The π-network can provide impedance transformation between the source and load, improving power transfer efficiency.

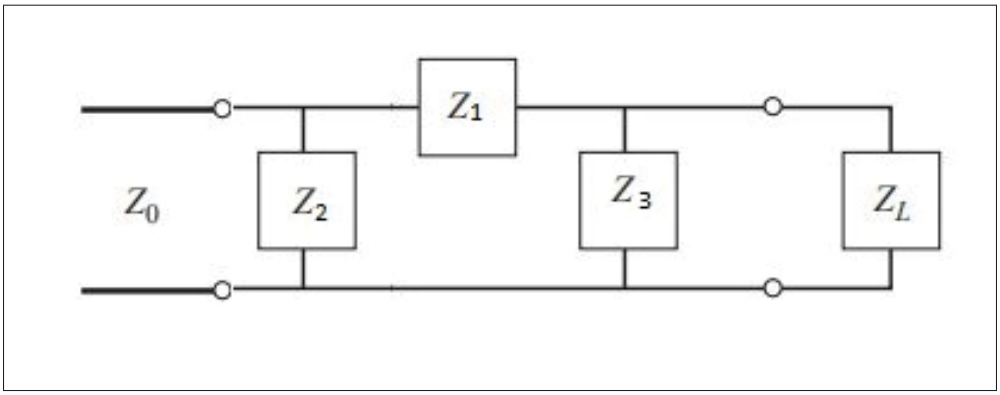


Figure 1.3 π-section matching networks
Taken from Pozar (2000)

T-Matching network: The T-matching network, Figure 1.4, involves three reactive elements connected in a "T" configuration. It is employed for impedance matching in RF and audio frequency applications. The T-network provides a wider range of impedance transformation options compared to L- and π-networks.

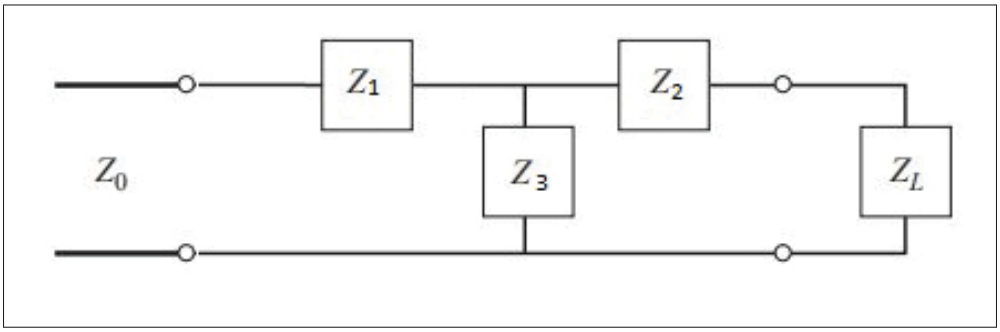


Figure 1.4 T-section matching networks
Taken from Pozar (2000)

The matching network involves placing impedance blocks in parallel or series, or a combination of both. If there are two elements, an L section is used. If there are three elements, a Pi or T

section is used. The network can be expanded and the number of series and parallel blocks increased to create a ladder structure.

Lumped element matching network: Various techniques, such as lumped element matching networks, can be used to create impedance components. Lumped element-matching networks utilize discrete components like resistors, capacitors, and inductors to achieve impedance matching. These networks are cost-effective and straightforward, making them suitable for various applications

Advantages of lumped element matching networks:

- Simplicity in design and implementation.
- Cost-effective using readily available discrete components.
- Versatility in matching a wide range of impedance values.

Disadvantages of Lumped Element Matching Networks:

- Limited high-frequency performance due to parasitic effects.
- Physical size constraints, less suitable for compact designs.
- Limited impedance transformation capability compared to other advanced techniques.

Transmission Line Matching Network: Transmission line matching networks, Figure 1.5 and Figure 1.6, utilize transmission lines such as microstrips or stripline to achieve impedance transformation. These networks are commonly used in high-frequency applications and can provide precise impedance matching over a wide frequency range.

Indeed, when utilizing a transmission line in the layout of a pi or L network, it will result in single stub matching and double stub matching, respectively, for the impedance blocks.

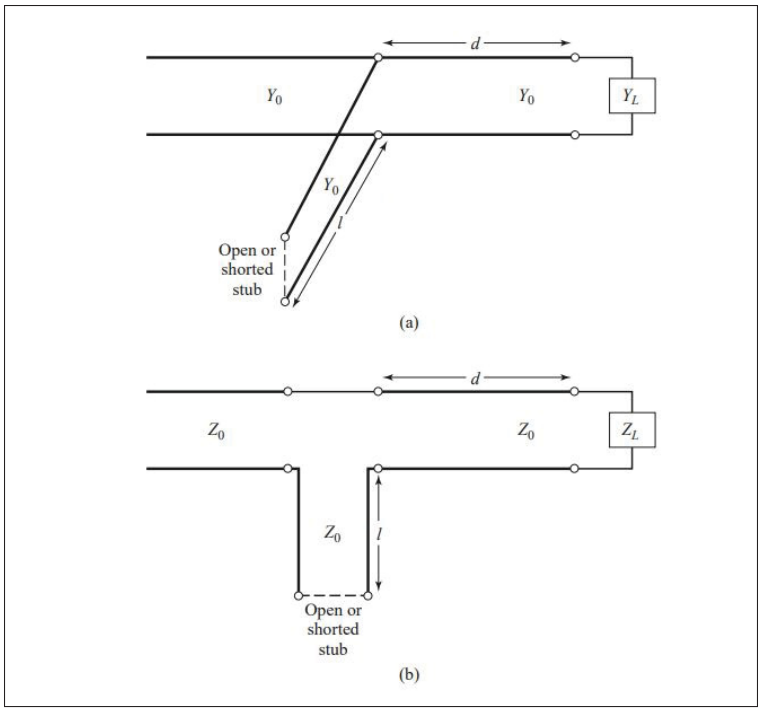


Figure 1.5 Single stub matching parallel(a) and Series(b)
Taken from Pozar (2000)

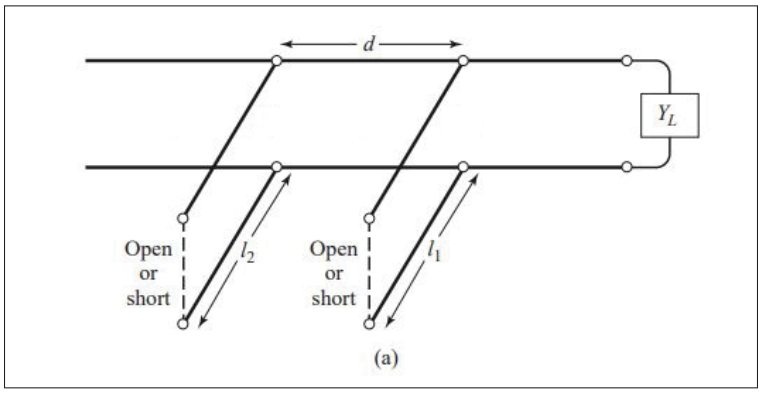


Figure 1.6 Double stub matching
Taken from Pozar (2000)

Variable matching network:

A matching network can be made variable by incorporating adjustable or tunable components into its design. These adjustable components allow for the modification of the network's

impedance transformation characteristics, making it adaptable to different operating conditions or changing impedance requirements.

Here are a few common ways in which a matching network can become variable:

Variable capacitors: Capacitors with adjustable capacitance values, such as varactors or variable capacitors, can be incorporated into the matching network. By changing the capacitance, the impedance presented by the capacitor can be varied, thereby modifying the overall impedance transformation of the network.Chen, Forse, Chase & York (2004)

Variable inductors: Inductors with adjustable inductance values, such as variable inductors or adjustable ferrite cores, can be used in the matching network. By altering the inductance, the impedance presented by the inductor can be modified, enabling variable impedance transformation.Saberkari, Ziabakhsh, Martinez & Alarcón (2016)

Switched parts: The matching network can include switches that allow the connection or disconnection of discrete components, such as resistors, capacitors, or inductors. By selectively activating or deactivating these components, the overall impedance characteristics of the network can be varied.Yazdani & Mansour (2017)

Digital tuning: In some advanced systems, digital tuning techniques can be employed to create a variable matching network. This involves using digitally controlled components, such as digitally tunable capacitors or digitally controlled impedance elements, that can be adjusted through digital signals or microcontroller-based control systems.Jeong, Lin & Tentzeris (2019a)

By incorporating these variable components into the matching network, the impedance transformation properties can be adjusted as needed. This flexibility allows for the optimization of the network's performance under varying conditions, such as changing frequency, load impedance, or other system parameters.

It is important to note that the design and implementation of a variable matching network require careful consideration of factors such as component selection, control mechanisms, calibration,

and stability. Proper tuning and calibration techniques are necessary to ensure optimal impedance matching and to maintain desired system performance.

1.2 Reflection coefficient measurement

Vector Network Analyzer: A Vector Network Analyzer (VNA), Figure 1.7, operates by transmitting a known test signal into the device or circuit under test and measuring the resulting signals at multiple frequencies. The key principle behind a VNA is the use of vector measurements, which means that both the amplitude and phase of the reflected and transmitted signals are measured.

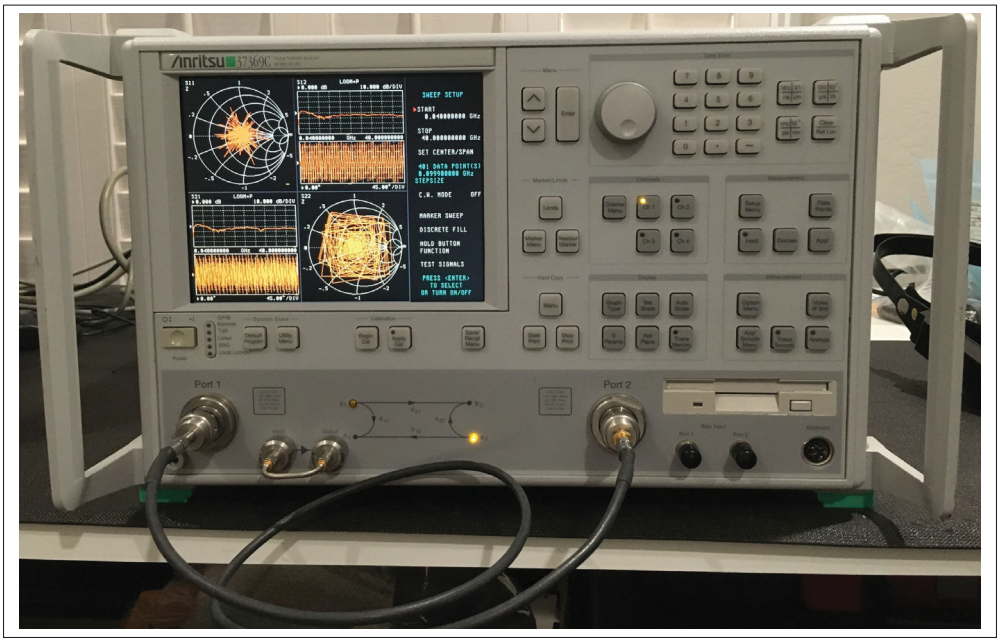


Figure 1.7 Vector network analyzer front panel view

Four-Port Reflectometer:

This device is a coupler used in a series of components through which waves travel, with the purpose of measuring the reflection coefficient, Figure 1.8. In an ideal scenario, it is designed to prevent any part of the incoming wave from port one from entering port four (ensuring isolation). Instead, a significant portion is directed to port two (output), while a very small portion is

directed to port three (measurement). A similar condition applies to the wave entering port two, between terminals 2, 3, and 4. By employing this technique, which has minimal impact on the wave passing through the transmission line, it becomes possible to sample both the incident and reflected waves and calculate the reflection coefficient.

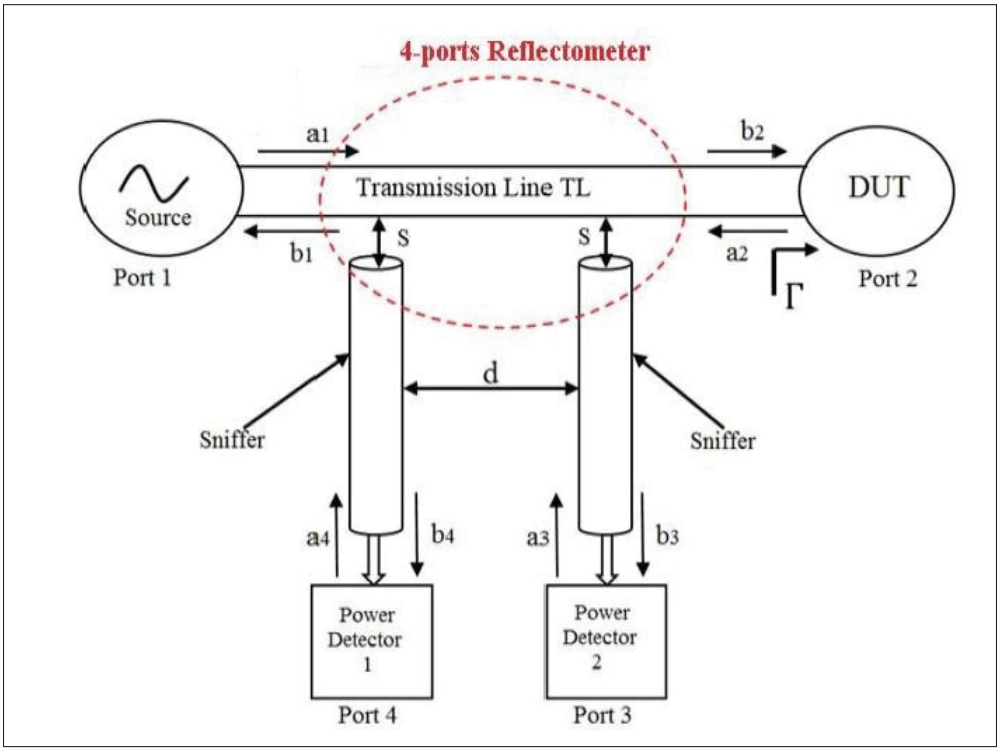


Figure 1.8 Four rort reflectometer block diagram
Taken from Mohamed & Kouki (2019)

Embedded RF Vector Measurement:

The depicted system can be observed in Figure 1.8. It is comprised of a transmission line, to which two additional transmission lines (referred to as sniffers) are vertically placed close, maintaining a specified distance denoted as "s". The separation distance between the two transmission lines indicated as "d", is also an essential parameter of the structure. In this approach, the power supply is connected to port number one, the load is connected to port number two, and ports three and four are connected to power measurement device. The S-parameter of the system can be simulated or measured after fabrication. In the subsequent equations, the 4x4 S-parameter of

the reflectometer is assumed to be known. A matrix can be constructed using the S-parameters as follows: taken from Kouki, Masri, Gagnon & Thibeault (2010)

$$\begin{bmatrix} A_1 & A_2 \\ B_1 & B_2 \\ C & D \end{bmatrix} = \begin{bmatrix} (S_{21}S_{32} - S_{31}S_{22}) & (S_{21}S_{41} - S_{41}S_{22}) \\ S_{31} & S_{41} \\ -S_{22} & 1 \end{bmatrix} \tag{1.1}$$

The reflection coefficient (Γ) is a parameter that describes how much of a wave is reflected by an impedance discontinuity in the transmission medium. It is equal to the ratio of the amplitude of the reflected wave(a_2) to the incident wave(b_2), with each expressed as phasors.The reflection coefficient is written for port two in 1.2.

$$\Gamma = \frac{a_2}{b_2} = x + jy \tag{1.2}$$

The power measured at ports 3 and 4 are:

$$P_3 = |b_3|^2 \tag{1.3}$$

$$P_4 = |b_4|^2 \tag{1.4}$$

To calculate the reflection coefficient Γ_L, the transmission coefficients between port 1 and ports 3 and 4, denoted as T_{31} and T_{41} respectively, are initially expressed in the following manner.

$$T_{31} = \frac{b_3}{a_1} = \frac{A_1\Gamma_L + B_1}{C\Gamma_L + D} \tag{1.5}$$

$$T_{41} = \frac{b_4}{a_1} = \frac{A_2\Gamma_L + B_2}{C\Gamma_L + D} \tag{1.6}$$

By putting equations 1.5 and 1.6 into 1.3 and 1.4 :

$$P_3 = P_1 \left| \frac{A_1\Gamma_L + B_1}{C\Gamma_L + D} \right|^2 \tag{1.7}$$

$$P_4 = P_1 \left| \frac{A_2\Gamma_L + B_2}{C\Gamma_L + D} \right|^2 \tag{1.8}$$

To compute Γ at port two, we express equations 1.7 and 1.8 explicitly in relation to both its real and imaginary components, as shown below

$$(x - \alpha_3)^2 + (y - \beta_3)^2 = r_3^2 \tag{1.9}$$

$$(x - \alpha_4)^2 + (y - \beta_4)^2 = r_4^2 \tag{1.10}$$

scattering matrix for the four-port reflectometer is known so the right side of equation 1.1 is known then A1, A2, B1, B2, C, and D can be calculated as some constant. P3 and P4 can be measured with the two sniffers as some scalar number. P_1 is the incident power so it is known.Here, α_3, β_3,α_4, β_4, r_3 and r_4 and r_4 represent six tangible parameters that can be included in the formulation of A1, B1, A2, B2, C, D, P1, while Q3 and Q4 denote the centers of the circles

In these two equations (1.9 and 1.10), the unknown components are the imaginary and real parts of Γ. By examining the structure of the equations, it becomes apparent that the relationships

governing these two unknowns resemble those observed in the construction of circles. By visualizing these relationships as circles, we obtain the following two intersections.

As it is shown in Figure 1.9 circle One is centered at Q3 with a radius of r_3 and Circle two is centered at Q4 with a radius of r_4. these two cicles have two intersections. Another requirement exists for linear and passive devices:

$$|\Gamma|^2 = x^2 + y^2 \leq 1 \tag{1.11}$$

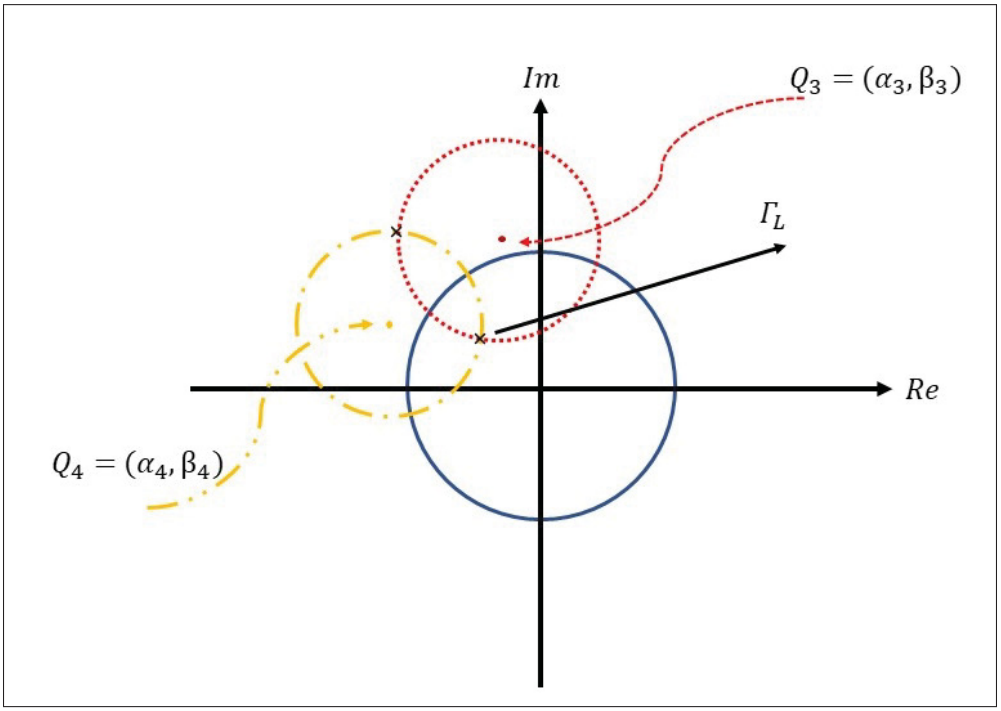


Figure 1.9 Circle Intersections, one in the unit circle and one out
Taken from Mohamed & Kouki (2019)

The presence and positions of the two solutions on the complex plane depend on the selected distance "d" that separates the two sniffers. If the distance "d" is below a certain minimum value d_{min}, both solutions will lie outside the unit circle. On the other hand, if the distance "d" exceeds a certain maximum value d_{max}, the two circles representing the solutions will not

intersect, indicating that no solution exists. However, between d_{min} and d_{max}, two solutions can be found, with one located inside the unit circle and the other outside of it.

1.3 Control block

The control Unit shown in figure 0.1 serves as the pivotal component of the system, responsible for receiving information from the data collector section (including the four-port reflectometer structure, sniffers, and ADC) and performing calculations to determine the required output data. Based on the results, it initiates the necessary adjustments to the system. The central core of the system can be implemented using a microcomputer, a mid-sized personal computer, or a network server, depending on the specific system's requirements and usage.

CHAPTER 2

METHODOLOGY

2.1 Introduction

This chapter focuses on the study of reconfigurable matching networks. It provides a comprehensive overview of the research approach and methodology employed in this study. It starts with a system overview then covers all hardware components and control techniques required for the operation a reconfigurable matching network.

2.2 System overview

An impedance-matching system is designed to adjust itself based on the signal power traveling through the transmission line, enabling it to achieve an acceptable level of impedance matching

This impedance-matching controlled system consists of the following parts:

- Measurement
- Desired Value
- Controller
- Control Element

Measurement: This component is responsible for sensing or measuring the relevant variables or parameters of the system. It may involve sensors, detectors, or instruments that gather data about the system's current state.

Desired Value: The reference or desired value represents the target or ideal value that the system aims to achieve or maintain. It serves as a benchmark for comparison with the system's actual state.

Controller: The controller is the central component that receives input from the sensing/measurement unit and compares it to the reference value. It determines the appropriate corrective

actions or control signals needed to achieve the desired outcome. The controller may operate based on predefined algorithms or rules.

Control Element: The actuation or control element is responsible for executing the corrective actions generated by the controller. It may be a physical device, such as a motor, valve, or switch, that adjusts the system's parameters to achieve the desired state. In this study, the element under investigation is a controllable capacitor with discretely adjustable values. Eight pairs of capacitors with different capacitance values are connected to the line through SPDT (Single-Pole Double-Throw) switches. By changing the state of the SPDT switches, this adaptable element influences the system.

Feedback Loop: The feedback loop provides information about the system's output or performance to the controller. It enables continuous monitoring and adjustment of control signals based on the feedback received. This mechanism helps maintain system stability and ensures that the actual output aligns with the desired value. In this study, the measurement of power on the line by the sensor, its conversion into processed data for the central processor, and the application of this information to correct the system output collectively constitute the feedback loop.

2.3 measurement

The sensing/measurement section of the system incorporates the LTC5582 power detector as a crucial component. The LTC5582 is a highly capable power detector integrated circuit that plays a significant role in accurately measuring the power levels of signals within the system (see Figure 2.1). With its advanced features and high-performance characteristics, the LTC5582 offers precise power measurement capabilities across a wide frequency range, spanning from 40MHz to 10 GHz. This power detector exhibits exceptional linearity, low insertion loss, and a broad dynamic range, with a linear dynamic range of up to 57 dB (see Appendix II), making it suitable for various applications in the system. Its integrated functionality and straightforward interface simplify the measurement process, allowing for efficient and reliable power detection.

Overall, the inclusion of the LTC5582 in the sensing/measurement section ensures accurate and dependable power measurements, contributing to the overall effectiveness and performance of the system.

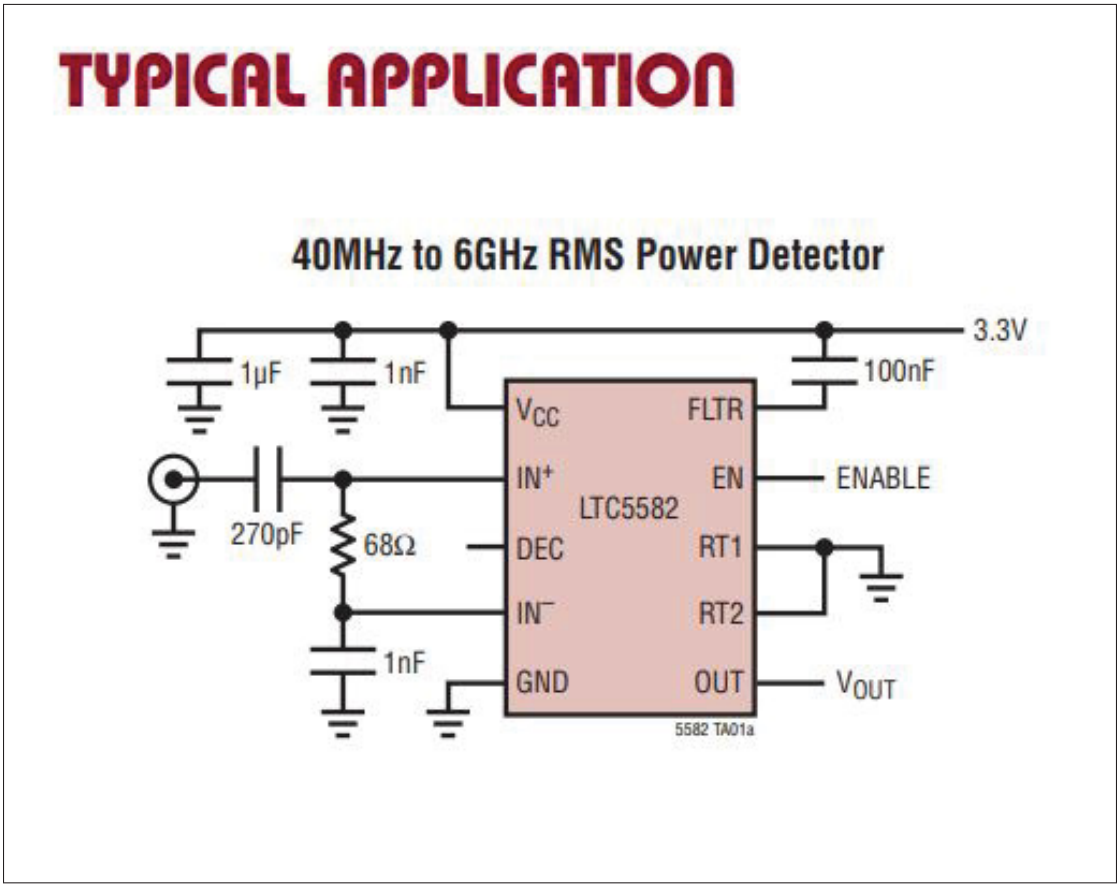


Figure 2.1 LTC5582 chip is RMS power detector 0.4 to 10GHz
Taken from Analogdevices (1965)5582 datasheet

2.4 Desired value

The reference or desired value corresponds to the designed matching level between two blocks in a 50-ohm system, which implies a reflection coefficient close to zero. The goal is to optimize impedance matching between the source block and the load block to ensure that the maximum amount of power is efficiently transmitted from one to the other. By minimizing the reflection coefficient, the system reduces the amount of power reflected back to the source, thereby maximizing power delivery to the load. This desired value sets the target for the system to achieve impedance matching that minimizes power losses and ensures optimal power transmission. Striving to minimize the reflection coefficient enables efficient energy transfer and improved overall system performance. The reference value serves as a benchmark against which the system's actual performance is compared, allowing the control algorithm to generate appropriate corrective actions to maintain the desired power transfer efficiency.

2.5 Controller

The ATMEGA16L-8AQ microcontroller as shown in Figure 2.2 was selected as the central controller of the system. It is a powerful and versatile component capable of managing various aspects of the reconfigurable impedance-matching system. Based on the ATmega16L architecture, this microcontroller features an advanced 8-bit RISC processing core, offering high performance and efficient execution of control algorithms.

With its ample input/output (I/O) pins, the ATMEGA16L-8AQ allows interfacing with sensors, detectors, actuators, and communication modules, facilitating effective integration within the system. In this application, the I/O pins are used as outputs to control the capacitor switches. The microcontroller's substantial memory resources, including Flash program memory and EEPROM data memory, provide sufficient capacity for storing both program code and operational data. The Flash memory is used to store the compiled code. In one section of the algorithm, 256 possible states are explored for network matching, and the corresponding reflection coefficient values are measured and stored. EEPROM is used to preserve this information.

Additionally, the microcontroller offers multiple communication interfaces, including UART, SPI, and I^2C, enabling seamless data exchange with external devices or systems. This enhances system flexibility and supports remote control functionality. The Serial Peripheral Interface (SPI) is used for both programming the microcontroller and for communication between the microcontroller and the ADC. Eight I/O pins are also configured as parallel outputs to drive a character display used for debugging purposes.

The selection of the ATMEGA16L-8AQ microcontroller in this thesis highlights its suitability for control tasks. Its processing power, memory capacity, I/O flexibility, and communication capabilities contribute to the efficient execution of control algorithms, enabling real-time decision-making and precise adjustment of system parameters. By employing the ATMEGA16L-8AQ, the system gains configurability, adaptability, and reliable operational control.

2.6 Control element

Within the controlled system, the actuation/control elements play a crucial role. One such component used in this system is the CG2179M2-C4 chip, which functions as a Single-Pole, Double-Throw (SPDT) switch. This chip is specifically designed for RF applications, enabling precise control over signal routing and impedance matching within the system.

The CG2179M2-C4 offers advanced features and performance characteristics that make it well-suited for this application. With its SPDT configuration, the chip provides two selectable states for signal path selection. This capability enables adjustment and reconfiguration of the impedance-matching network, accommodating varying operating conditions and optimizing power transfer efficiency. In this context, it is essential to minimize the impact on the signal within the line. This necessitates an SPDT switch with extremely low insertion loss—such as the 0.45 dB at 3 GHz provided by this chip. Furthermore, its single-bit control simplifies implementation, requiring fewer I/O pins on the main microcontroller. Its compact 6-Minimold package also helps reduce interference with high-frequency signals.

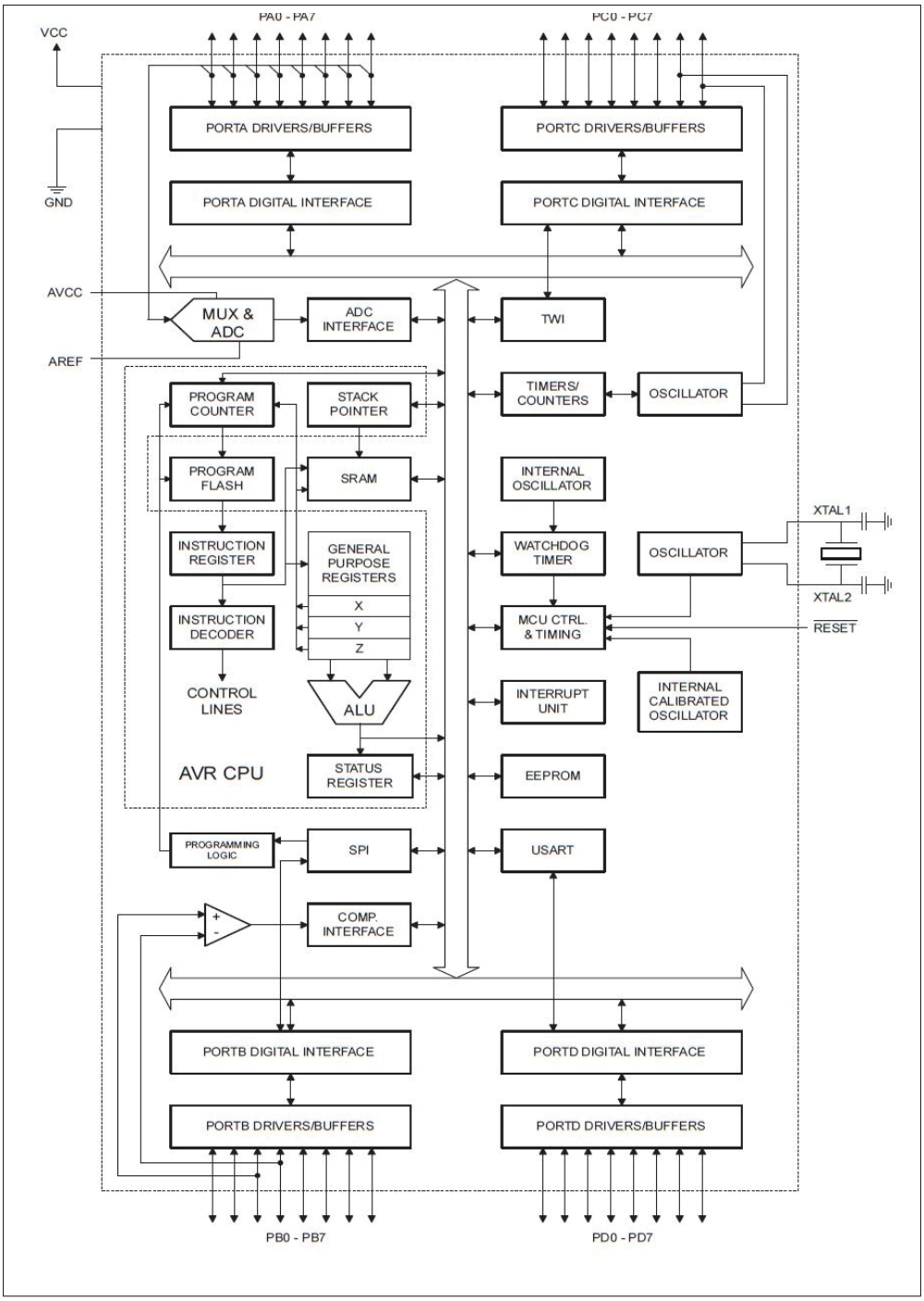


Figure 2.2 ATMEGA16 microcontroller inside block diagram
Taken from MicrochipTechnology (2006a)EGA16 datasheet

The chip's low insertion loss ensure minimal disruption to signal transmission and minimal power loss during the actuation process.

By employing the CG2179M2-C4 (see Figure 2.3) chip as the actuation/control element, the self-controlled system achieves precise control over the impedance-matching network. The chip's ability to efficiently switch RF signals within the transmission line allows the system to adapt its impedance characteristics in response to changing requirements or environmental conditions. This flexibility enhances the system's overall efficiency and ensures optimal power transfer between blocks.

In summary, the integration of the CG2179M2-C4 chip as the actuation/control element enables the system to reconfigure the impedance-matching network. The chip's advanced features—including fast switching speed, low insertion loss, and excellent linearity—contribute to improved signal integrity and efficient power transfer throughout the system.

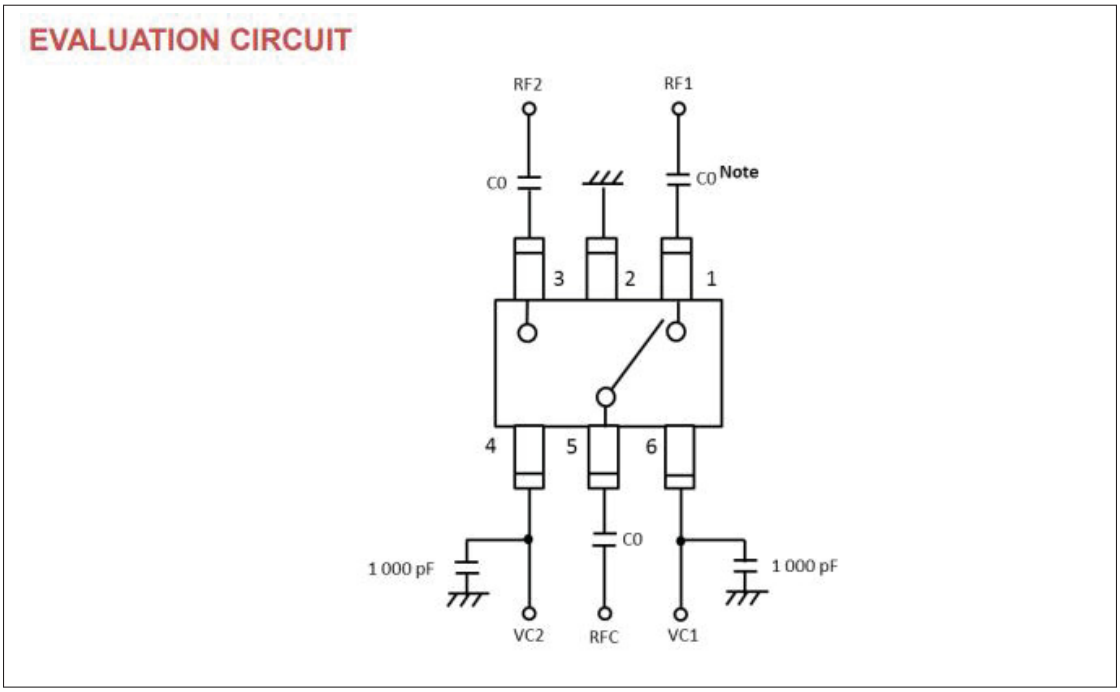


Figure 2.3 CG2179M2-C4 chip inside block diagram
Taken from Laboratories (2009) datasheet

2.7 ADC converter

The feedback loop in this system is designed to achieve the objective of power optimization. The reflection coefficient is measured to gather the necessary information for system control. In this context, the system utilizes the MCP3561-E chip, which functions as an analog-to-digital converter (ADC) (see Figure 2.4). The MCP3561-E converts the continuous analog signal—represented by voltage—into digital data that can be processed by the main processor.

The MCP3561-E is a low-power ADC specifically designed for accurate conversion of analog signals to digital format. It offers excellent resolution and sampling rates, ensuring precise measurement of the voltage that represents the reflection coefficient. The chip incorporates advanced features such as differential inputs, an on-chip voltage reference, and programmable gain amplifiers, which enhance its performance and flexibility.

By employing the MCP3561-E in the system, the analog voltage signal representing the reflection coefficient is efficiently and accurately digitized. This digital data is then transferred to the main processor. The high precision and reliability of the MCP3561-E contribute to the effectiveness of the feedback loop, enabling the system to continuously monitor and optimize power transfer based on the measured reflection coefficient.

In summary, the MCP3561-E chip plays a critical role in the system's feedback loop, serving as the ADC responsible for measuring the reflection coefficient. Its high precision, low power consumption, and advanced features make it an ideal choice for converting analog voltage signals to digital data, allowing the system to make informed control decisions and optimize power transfer efficiency.

2.8 Control algorithm

There are 10 SPDT switches(see Figure 2.3) in the system. Since each switch has two states, the matching network can achieve a total of 1024 possible configurations. The central processor(ATmega16; see Figure 2.2) sweeps through all these configurations and calculates

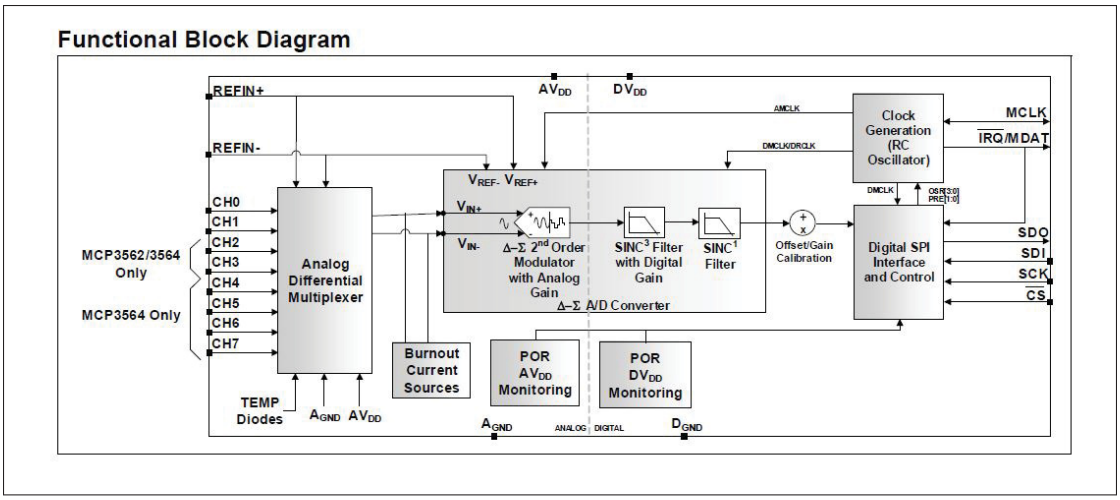


Figure 2.4 MCP3561-E functional block diagram
Taken from MicrochipTechnology (2006b)3561 datasheet

the reflection coefficient for each state. It then selects the most suitable option as the optimal configuration.

2.9 Matching network methodologe

To better explain this concept, let's visualize it using a Smith chart. When matching two adjacent blocks in a telecommunications system, it is necessary to determine an impedance transformation path on the Smith chart that connects one block to the other. Typically, such systems are normalized to a 50-ohm transmission line. Specific movements on the Smith chart can be used to achieve this matching, as discussed below.

Adding a series transmission line: In this case, movement occurs along a constant VSWR circle, which is centered at the origin of the Smith chart. The angular length of this arc corresponds to the electrical length of the added transmission line (see Figure 2.5 and Figure 2.6).

Adding a parallel capacitor: By placing a capacitive element between the transmission line and ground, movement is achieved along constant conductance circles on the Smith chart.

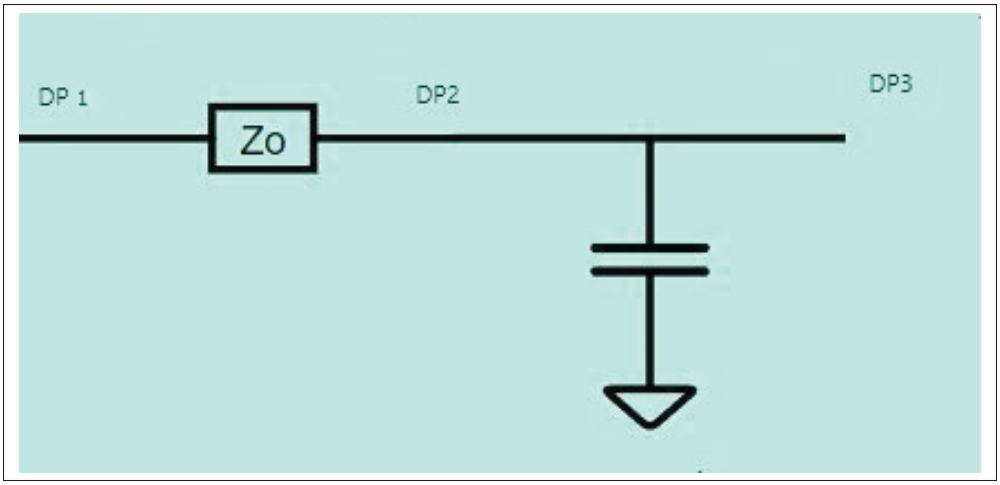


Figure 2.5 L section matching network consist
of transmission lines and parallel capacitor

By combining these types of movements—series line segments and shunt capacitive elements—the system can match a wide range of impedances to the center of the Smith chart, effectively achieving impedance matching.

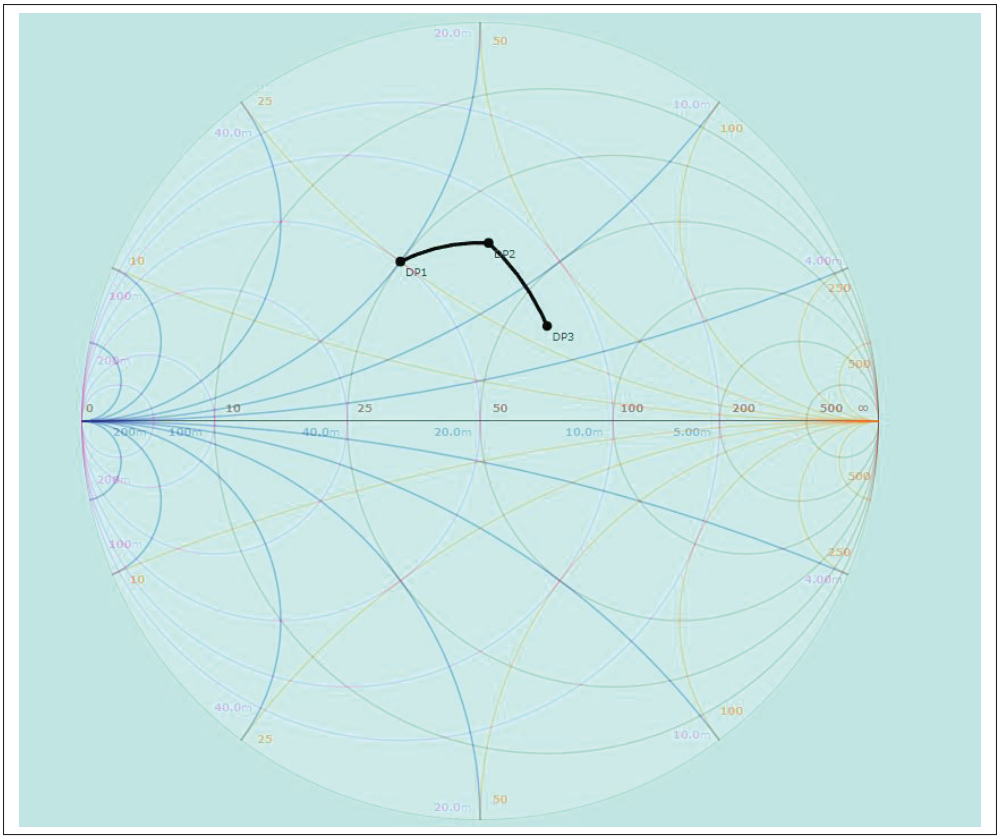


Figure 2.6 How series transmission lines and parallel capacitor moves on smith chart

CHAPTER 3

SYSTEM DESIGN DISCUSSION

3.1 Introduction

This chapter presents the system design, focusing on translating the theoretical concept into a practical and functional architecture. The main design aspects include component selection, topology configuration, and control integration. These elements are examined to ensure that the network can be adjust to achieve optimal power transfer.

The system shown in Figure 3.1 is composed of three main parts: the power-measurement block, the variable matching network, and the control unit. In the following sections, each block is examined in detail, along with its design requirements, constraints, and expected performance.

3.2 Power Measurement Block

The power measurement block consists of three essential sub blocks: the reflectometer, the power meter, and the analog to digital converter (ADC), as shown in Figure 3.1.

The primary function of this block is to sample the power of the signal propagating along the transmission line at two distinct points while ensuring that the sampling process introduces minimal disturbance to the signal path. The reflectometer provides directional power information, enabling the estimation of forward and reflected waves. Then, the power meter measures the absolute power level at a selected point.The ADC then converts the analog measurements into digital data with sufficient resolution and sampling accuracy to support the subsequent processing tasks in the control Unit.

In the following subsections, each of the three sub blocks is described in detail, including their operating principles, design considerations, and the rationale behind their selection for the implemented system.

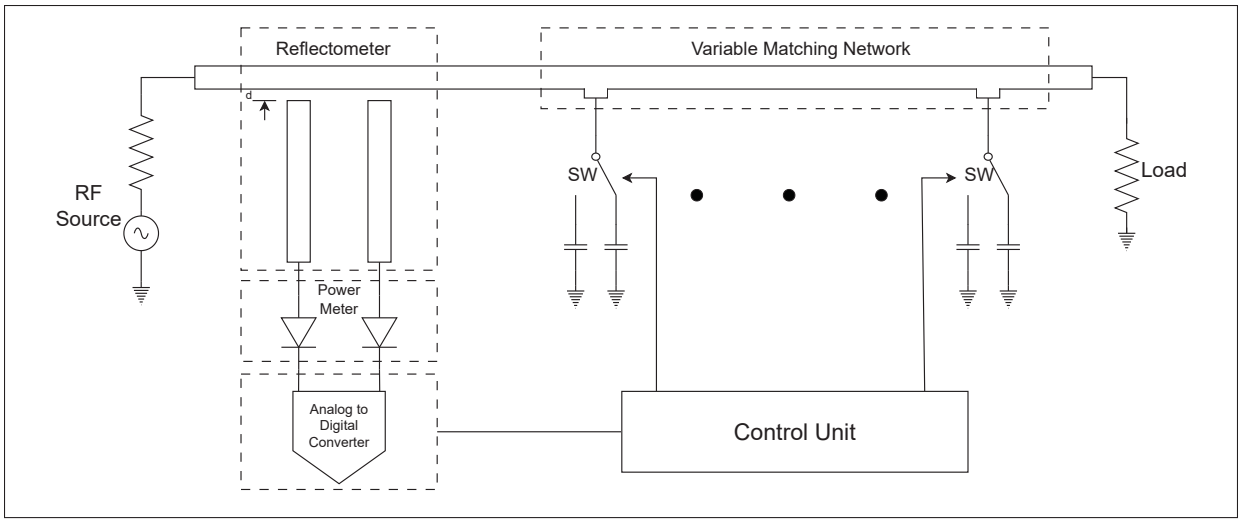


Figure 3.1 Overall block diagram of the system showing the power measurement block (Reflectometer, Power Meter, and Analog to Digital), the variable matching network, and the control unit

3.2.1 Reflectometer

The primary function of this block is to sample the power of the signal at two designated locations along the transmission line, separated by a predetermined distance. The output is a scalar power value, not a directional power signal, which is then passed to the analog-to-digital converter.

As shown in Figure 3.2, a four-port network, introduced in Section 1.2, is implemented. This structure consists of a transmission line and two sniffer branches, all designed with a characteristic impedance of 50 ohms. In this design, the spacing between the two sniffers (denoted as d in Figure 3.1) is a critical parameter, as it determines the operational frequency range of the structure based on the calculations presented in the previous chapter.

In addition, achieving a characteristic impedance as close as possible to 50 Ω—considering the dielectric material (ε_r = 4.5, height = 1.6 mm) and the required transmission line width—imposes further design constraints. After simulation and optimization, the transmission line was designed with a width of 2.98 mm, while the spacing between the two sniffers was set to 1.28 mm. Each

sniffers branch is 12.25 mm long, and the gap between each sniffer and the transmission line is 0.127 mm. These design parameters are illustrated in Figure 3.2.

The reflectometer structure is designed symmetrically. S-parameter simulation results obtained using ADS software are shown in Figures 3.2 through 3.7. As expected, the simulated value of S_{21} is less than -1 dB, and S_{11} is below -19 dB, indicating that the design closely approximates a 50-ohm impedance. The values of S_{31} and S_{41} range from -25 dB to -33 dB, which is acceptable in terms of minimizing the impact of the sniffers on the propagating signal. However, variations in attenuation across the frequency range require equalization, which will be addressed in the control unit section.

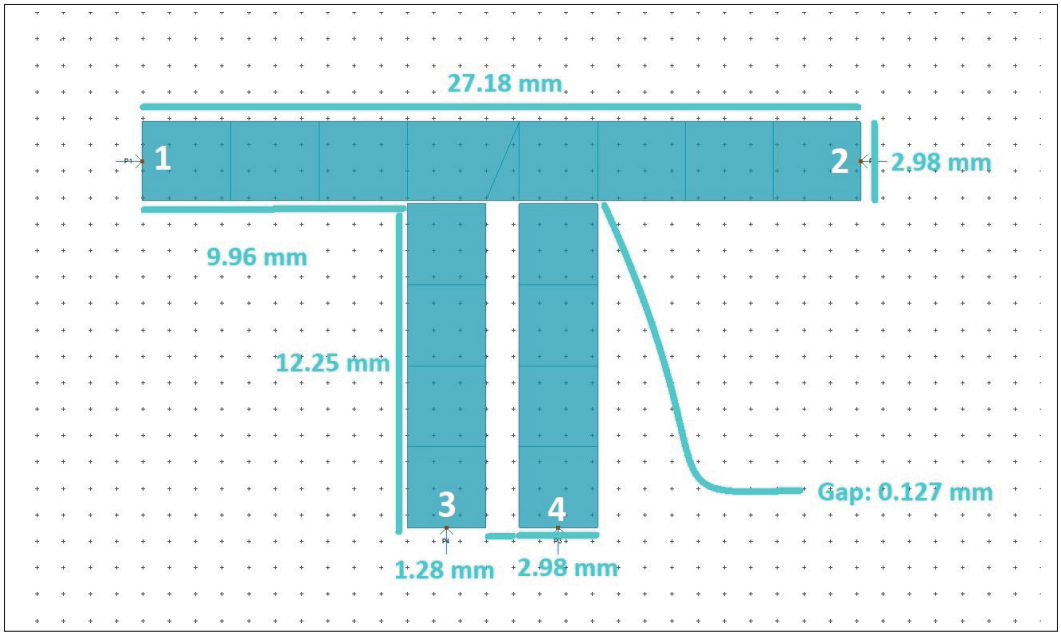


Figure 3.2 Sniffer PCB layout designed in ADS (EM simulation)

3.2.2 Power Measurement

At ports three and four of the sniffer, shown in Figure 3.2, the sum of the forward and reflected waves on the transmission line is observable. At these ports, a device is required to measure

Figure 3.3 S31 simulation results of the sniffer block

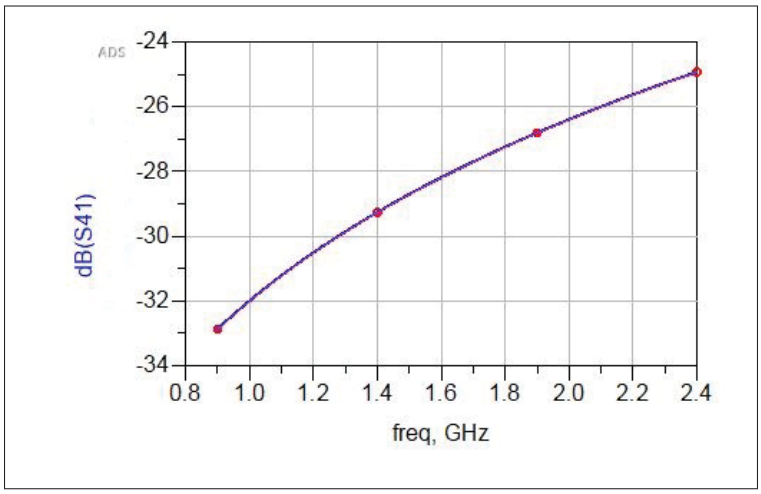


Figure 3.4 S41 simulation results of the sniffer block

this power and deliver it as processable data to the next stage, which is the analog-to-digital converter. For this purpose, the LTC5582 chip has been selected.

The LTC5582 is capable of measuring signal power over a frequency range of 40 MHz to 10 GHz. For accurate measurements, the input power must fall within the range of −60 dBm to 2 dBm. The chip features a 50-ohm input port, and its output provides a voltage signal ranging

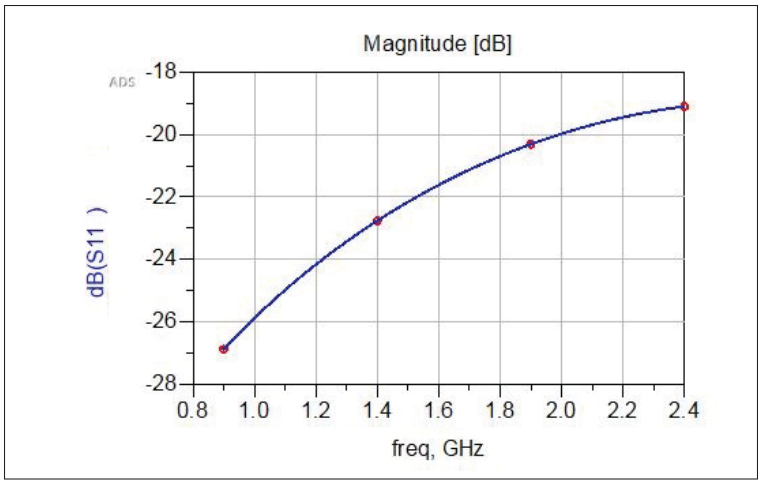


Figure 3.5 S11 simulation results of the sniffer block

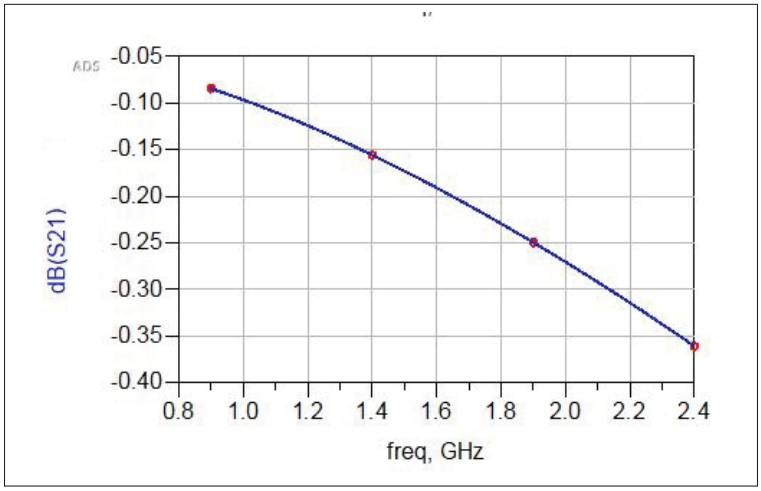


Figure 3.6 S21 simulation results of the sniffer block

from 0.8 V to 2.8 V. A visual representation of the power-to-voltage conversion characteristic is provided in Appendix II.

It should be noted that the effective measurable input power range of the LTC5582 is between −60 dBm and 2 dBm. Based on the S_{31} and S_{41} parameters shown in Figures 3.3 and 3.4, the input power level can be estimated along with the attenuation introduced by the sniffer network.

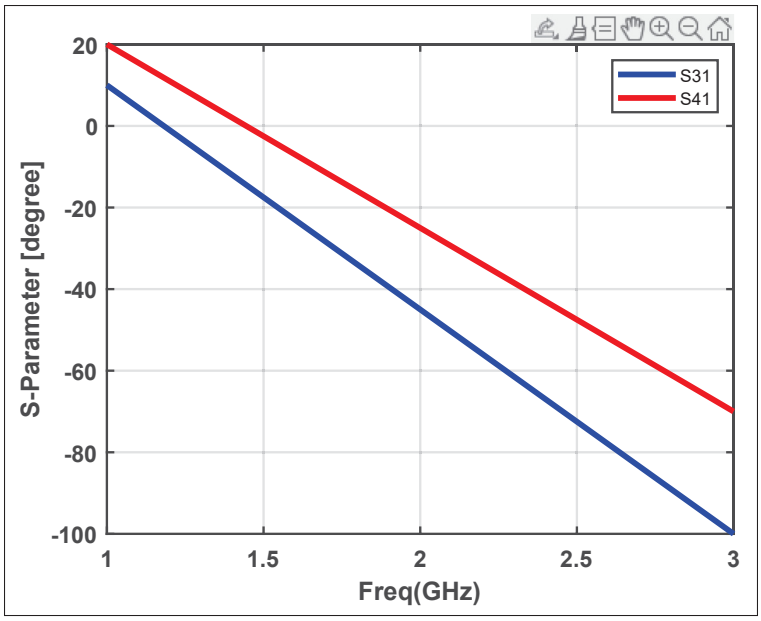


Figure 3.7 Simulation of the phase of the S31 and S41

Assuming an approximate attenuation of 30 dB (based on typical S_{31} and S_{41} values), the input power to the system should be between −30 dBm and +32 dBm in order to ensure that, after attenuation, the signal falls within the acceptable input range of the LTC5582. This simplification assumes a constant attenuation level, which will later be addressed more accurately in the central processing unit section.

3.2.3 Analog-to-Digital Converter (ADC)

In this section, a device is required to accurately convert an analog voltage ranging from 0.8 V to 2.8 V into a digital signal and transmit it to the central processor via a serial communication interface.

The MCP3562 chip has been employed as the core component for this task. It is a high-precision analog-to-digital converter (ADC) well-suited for measurement and data acquisition applications.

The MCP3562 utilizes a successive approximation register (SAR) architecture, allowing it to convert analog voltage signals into digital representations with high resolution and accuracy. It performs sampling and quantization by capturing the analog voltage at discrete time intervals and assigning corresponding digital codes.

A key feature of the MCP3562 is its 24-bit resolution, which enables it to detect extremely small changes in the input voltage. The resolution, defined by the number of bits in the digital output, determines the granularity and precision of the conversion process.

The chip supports flexible input voltage ranges, making it adaptable to signals of varying amplitudes and suitable for a wide range of measurement scenarios. It also integrates an internal voltage reference to provide a stable and accurate baseline for conversions.

The digital output from the MCP3562 can be easily interfaced with microcontrollers—such as the ATMEGA16 used in this system—digital signal processors, or other processing units for analysis, storage, or transmission. The chip supports standard serial interfaces, including SPI (Serial Peripheral Interface) and I^2C (Inter-Integrated Circuit); SPI is used in this implementation.

3.3 Matching Network

In this section, we focus on implementing a tunable matching network. The general concept was introduced in Section 2.9. This matching network consists of a number of series transmission lines and stubs, similar to the single-stub and double-stub structures shown in Figures 1.5 and 1.6, but with the addition of variable capacitors.

We begin by describing the physical structure of the network, which forms the fixed and unchangeable part of the system. The implementation of the variable capacitors will be discussed in the following section.

3.3.1 Structure

As shown in Figure 3.8, and based on the concept presented in Section 2.9 and Figures 2.5 and 2.6, a ten-port non-reconfigurable matching network has been designed in the ADS software.

Each block in the horizontal transmission line section is 8.5 mm long and 2.98 mm wide. Each block in the vertical stubs is 1.3 mm long and 2.96 mm wide.

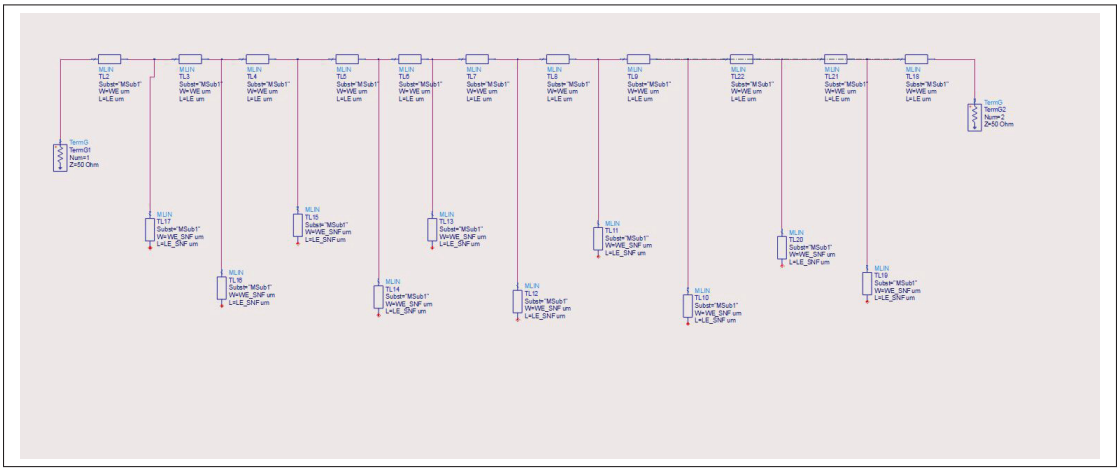


Figure 3.8 Matching network simulated in ADS

3.3.2 SPDTs

To enable reconfigurability in the system, an SPDT (Single-Pole Double-Throw) switch, the CG2179M2-C4 chip, is used. This chip connects one of two capacitors—each with a different capacitance value—to the transmission line. The selected capacitors have values of 2 pF and 0.3 pF and are specifically chosen for RF (Radio Frequency) applications.

3.3.3 Matching Network Integration

Before assembling the complete system, the matching network block was simulated independently, as described in Sections 3.4.1 and 3.4.2. A 50-ohm load was connected to one side of the network, and the network state was varied from 1 to 1024.

The results demonstrate that the matching network is capable of adapting a 50-ohm transmission line to various load impedances with different reflection coefficients. The simulation data was imported into MATLAB, and visualizations were generated to illustrate the network's matching capabilities.

These results are shown in Figures 3.9 to 3.12, which depict the regions covered on the Smith chart at different frequencies.

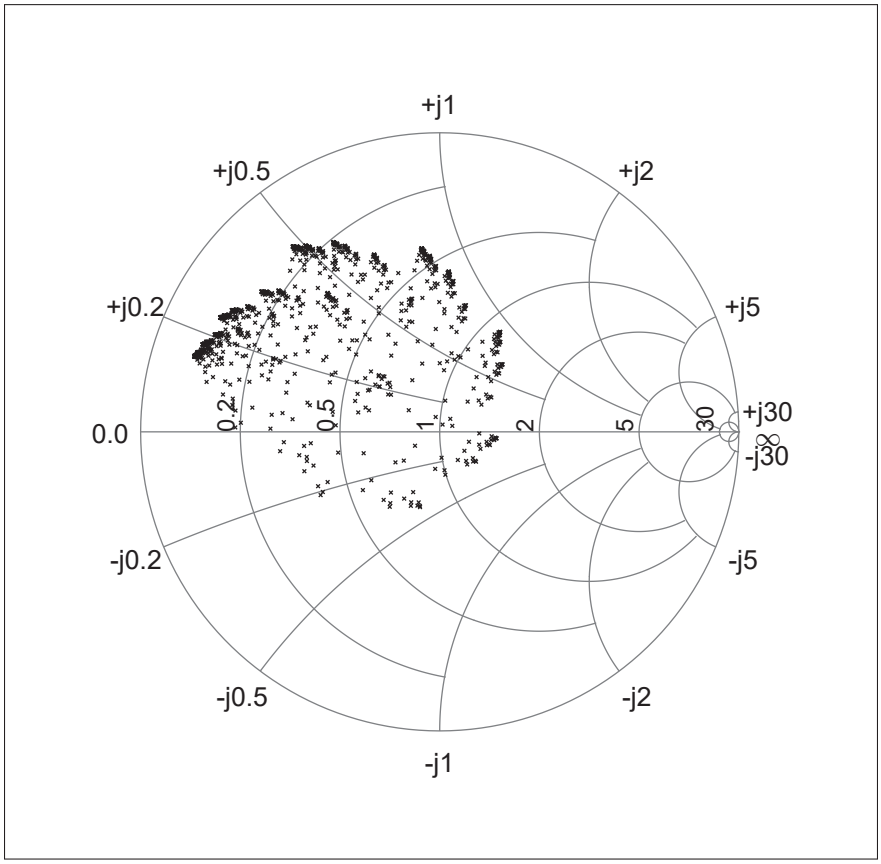


Figure 3.9 Simulation results, smith chart
Area covered at 1.2 GHz. (S11 in dB)

The Smith chart is a graphical tool commonly used in RF and microwave engineering to analyze and design impedance-matching networks. It provides a visual representation of the complex impedance plane, enabling engineers to assess the impedance-matching capability of their

circuits. By examining the coverage area on the Smith chart, one can determine the range of impedance values that the matching network can effectively match.

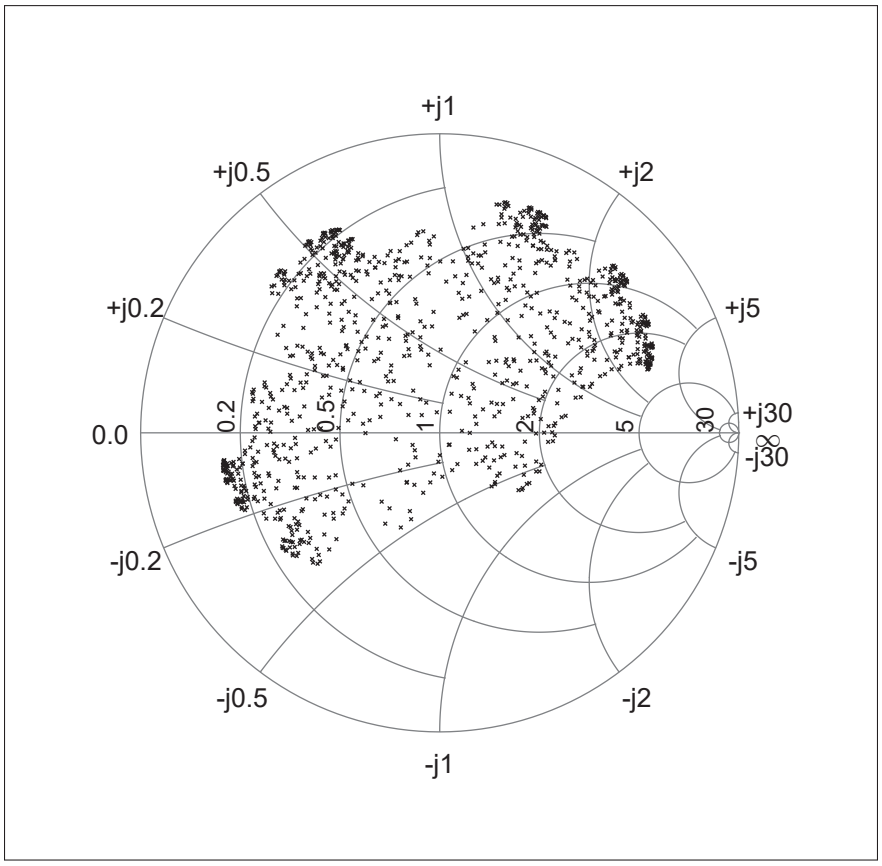


Figure 3.10 Simulation results, smith chart
Area covered at 1.4 GHz. (S11 in dB)

The simulation results illustrate the performance of the matching network across various frequencies within the 1.2–2.1 GHz range. Each figure corresponds to a specific frequency and shows the impedance values and the corresponding Smith chart coverage achieved by the matching network.

By analyzing the simulation results, the effectiveness of the designed matching network in covering the Smith chart across the specified frequency range can be evaluated.

This assessment helps determine the suitability and performance of the matching network for practical applications within the specified frequency band.

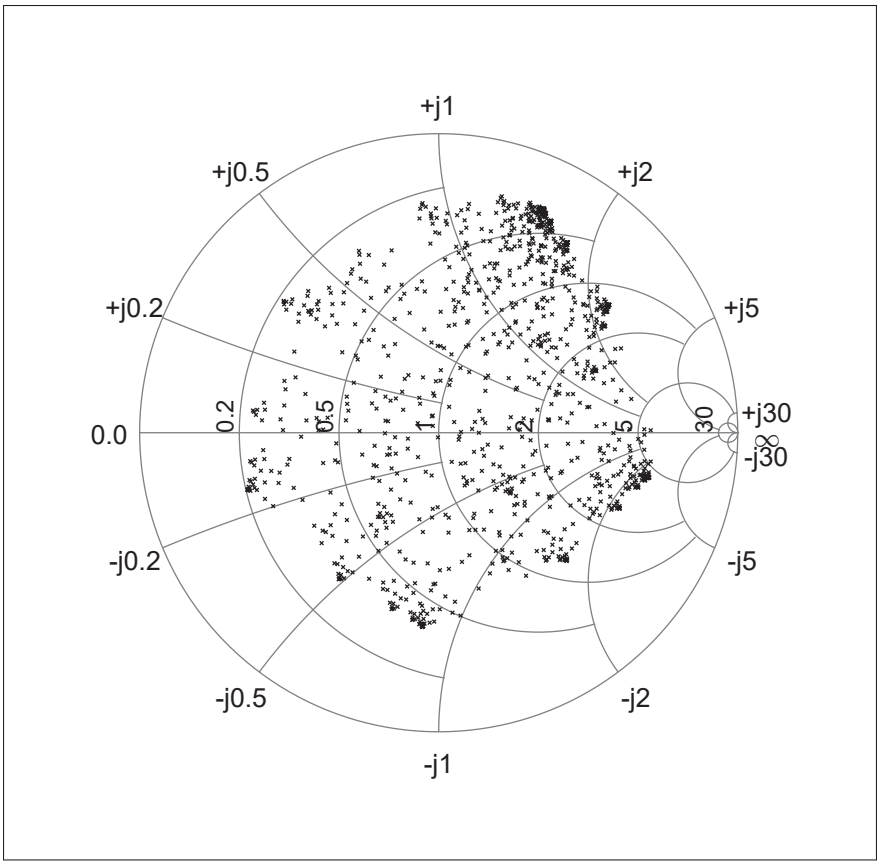


Figure 3.11 Simulation results, smith chart
Area covered at 1.8 GHz. (S11 in dB)

The simulation results (Figures 3.9 to 3.12) provide valuable insights into the behavior and capabilities of the designed matching network. They enable a thorough analysis of the network's impedance-matching performance, allowing for an evaluation of both its effectiveness and potential limitations.

Moreover, these results serve as evidence of the successful implementation and functionality of the matching network within the target frequency range.

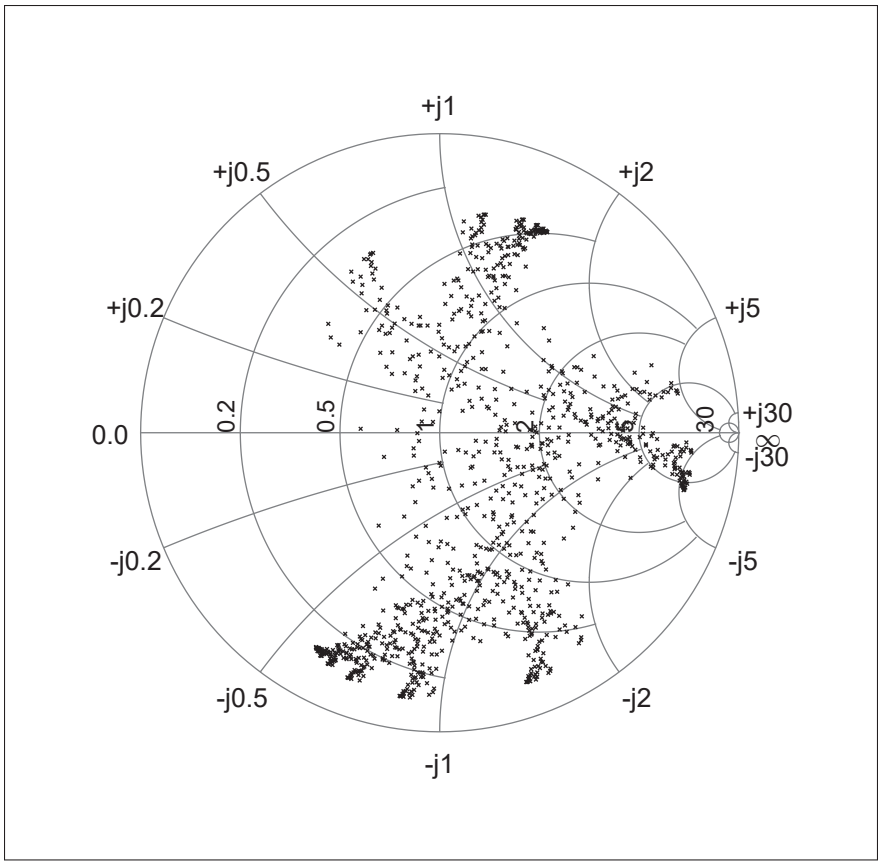


Figure 3.12 Simulation results, Smith Chart
Area Covered at 2.1 GHz. (S11 in dB)

3.4 Control unit

An ATmega16 microcontroller is used as the central controller of the system. The primary function of this block is to compute the reflection coefficient based on the signal power measured by the power measurement block.

Given that the matching network includes eight pairs of capacitors with different capacitance values—resulting in a total of 1024 distinct states—the system cycles through each state (from 1 to 1024), calculates the corresponding reflection coefficient, and stores the results. It then selects and reports the optimal state, i.e., the one that achieves the closest match between the line and the load.

As illustrated in Figures 3.4 and 3.5, the power attenuation coefficients S_{31} and S_{41} in the power measurement block vary across the 1.1–2.1 GHz frequency range. This variation necessitates compensation. In the power meter block, the signal power at ports three and four is detected by the reflectometer and converted to a voltage signal ranging from 0.8 V to 2.8 V. However, this conversion is not performed with a constant coefficient—it follows a frequency-dependent response curve, as shown in Appendix II.

The data required for these compensation processes is stored in libraries within the central processor's memory. During operation, the ATmega16 accesses this data to apply necessary corrections, thereby minimizing calculation errors and improving overall accuracy.

CHAPTER 4

SYTEM INTEGRATION AND EXPERIMENTAL VALIDATION

System Integration

The final configuration of all components within the system was designed using Altium software and subsequently fabricated. As illustrated in Figure 4.2, the system includes six ports for input and output, along with four primary functional blocks, which are described below:

- **Substrate** – The PCB base material that supports all electronic components and traces.
- **Port 1: UART Serial Communication** – Used for external data transmission and debugging.
- **Port 2: ISP Serial Programming** – Interface for in-system programming of the microcontroller.
- **Port 3: Power Input** – Provides power to the system.
- **Port 6: Character LCD** – Interface for a character-based display used during debugging or operation.
- **Block 1: Microcontroller** – The central processing unit, responsible for control logic and system coordination.
- **Block 2: ADC** – Converts analog voltage signals to digital values for processing.
- **Block 3: Power Measurement** – Measures signal power via the reflectometer and power meter.
- **Block 4: Matching Network** – Contains the tunable network used for impedance matching.

Substrate:

In this circuit, the entire system is implemented on a printed circuit board (PCB). Therefore, the substrate material and dielectric properties—such as thickness and permittivity—must be carefully selected to meet the electrical and mechanical requirements of all components.

For the PCB design, an FR4 substrate with a thickness of 1.6 mm is used. Figure 4.1 illustrates the layer configuration, which features copper conductors on both the top and bottom sides of the FR4 substrate. This structure is symmetrical, and the impact of ports three and four on the

signal propagating along the transmission line is less than −24 dB. The structure was simulated using ADS software to verify its performance.

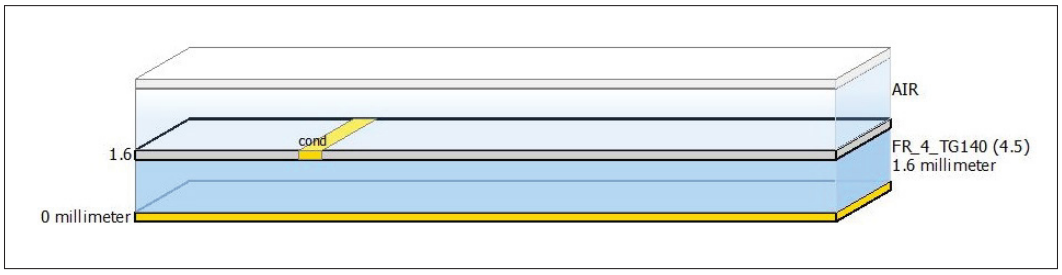


Figure 4.1 Substrate layer stackup

Ports:

As shown in Figure 4.2, the ATmega16L microcontroller in this system uses UART serial communication as its primary communication method. This interface allows real-time access to the microcontroller's internal information, including variables and registers. By utilizing UART, it is possible to establish instantaneous communication with the microcontroller and monitor system operation step-by-step.

The system also incorporates an In-System Programming (ISP) port for the ATmega16L microcontroller. This port enables direct firmware programming and updates within the target system, eliminating the need to remove or disassemble the microcontroller.

The ISP port offers significant advantages in terms of convenience and efficiency, streamlining the programming process and reducing development time.

The circuit is designed to operate with a 3.3 V power supply derived from an external power source.

Blocks:

As shown in Figure 4.2, Block 1 contains the central processing unit. Block 2 is an analog-to-digital converter (ADC) equipped with an external oscillator to enhance accuracy. Block 3

integrates both the reflectometer and the power meter. Finally, Block 4 consists of the variable matching network, which is controlled by the parallel outputs of the central controller.

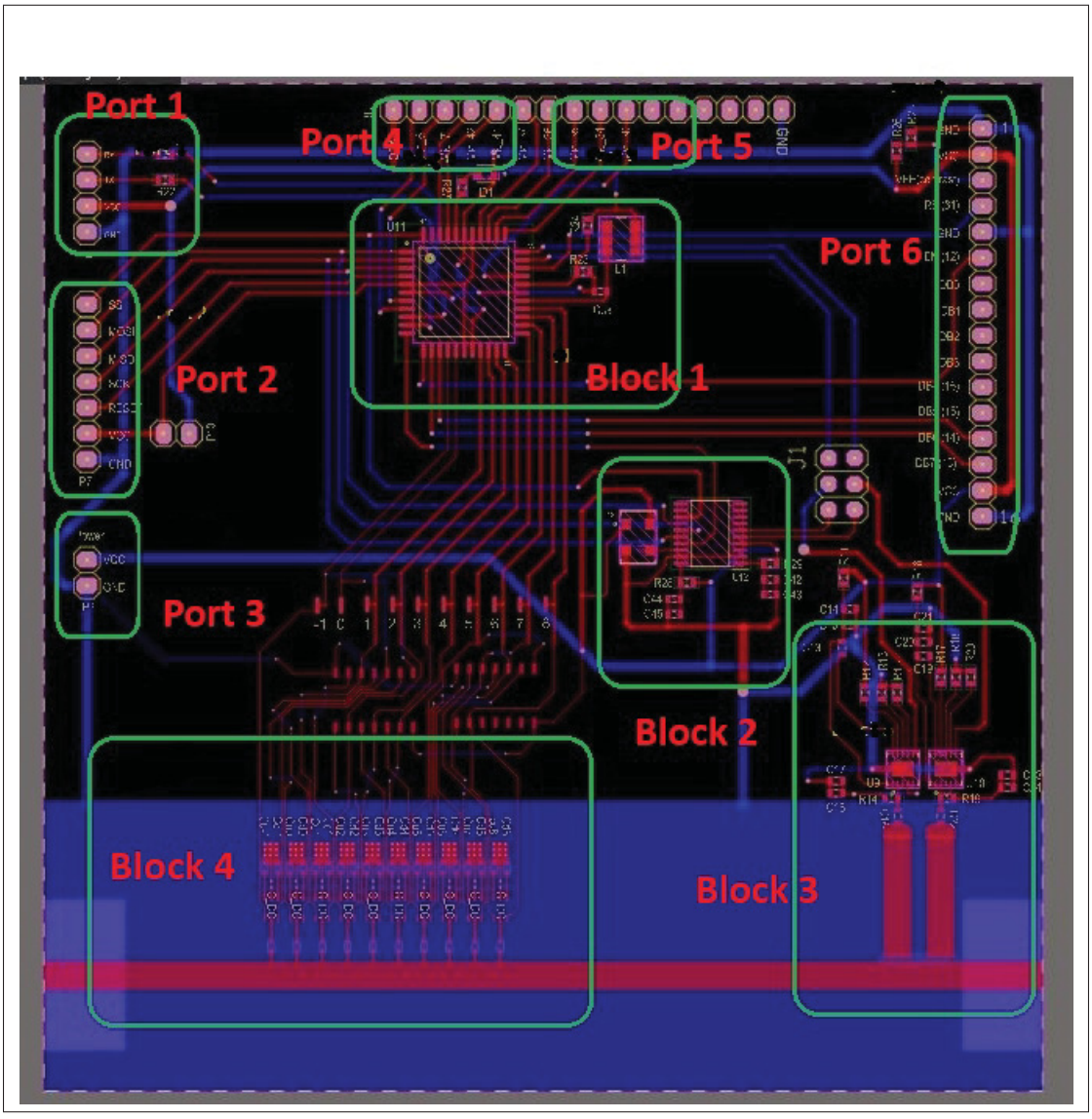


Figure 4.2 Final PCB design in Altium 2D view

4.1 Experimental Characterization of the Reconfigurable Impedance Matching System

The testing setup, as shown in Figure 4.3 and Figure 4.4 , consists of a vector network analyzer (VNA), a computer-controlled impedance tuner connected via LAN, and the device under test (DUT). These components will be described in further detail in the following section.

Initially, the calibration kit (Figure 4.5) is connected to one of the USB ports of the VNA, and the user waits for the red indicator light to turn green, signaling that the device is ready.

At this stage, the VNA is ready for accurate and reliable measurements.

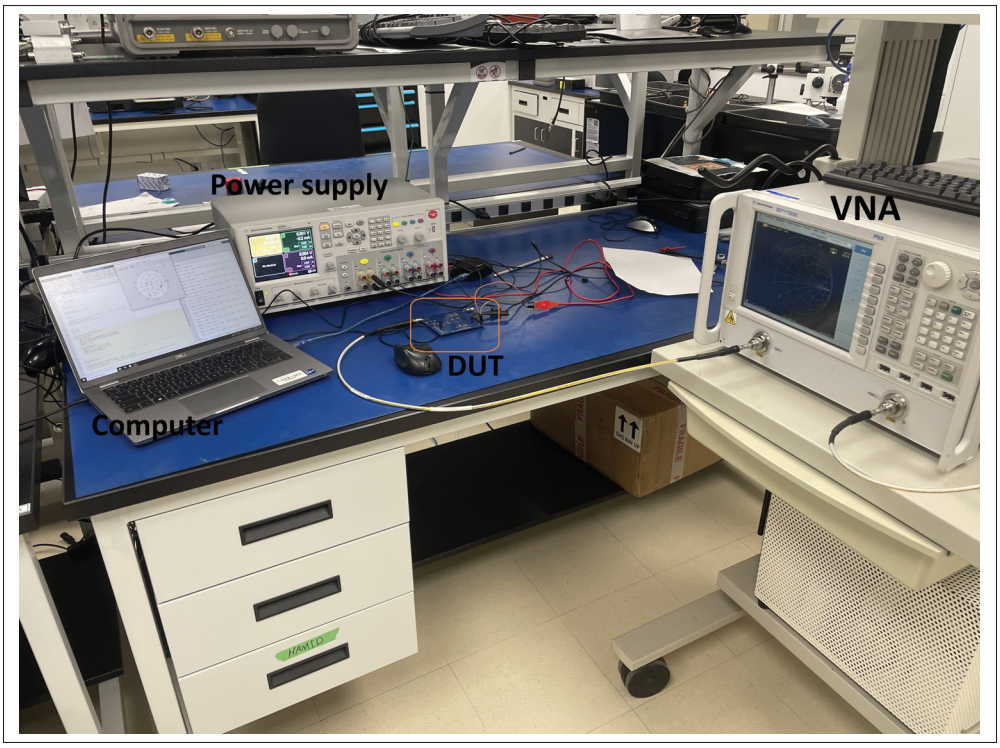


Figure 4.3 Test bench setup

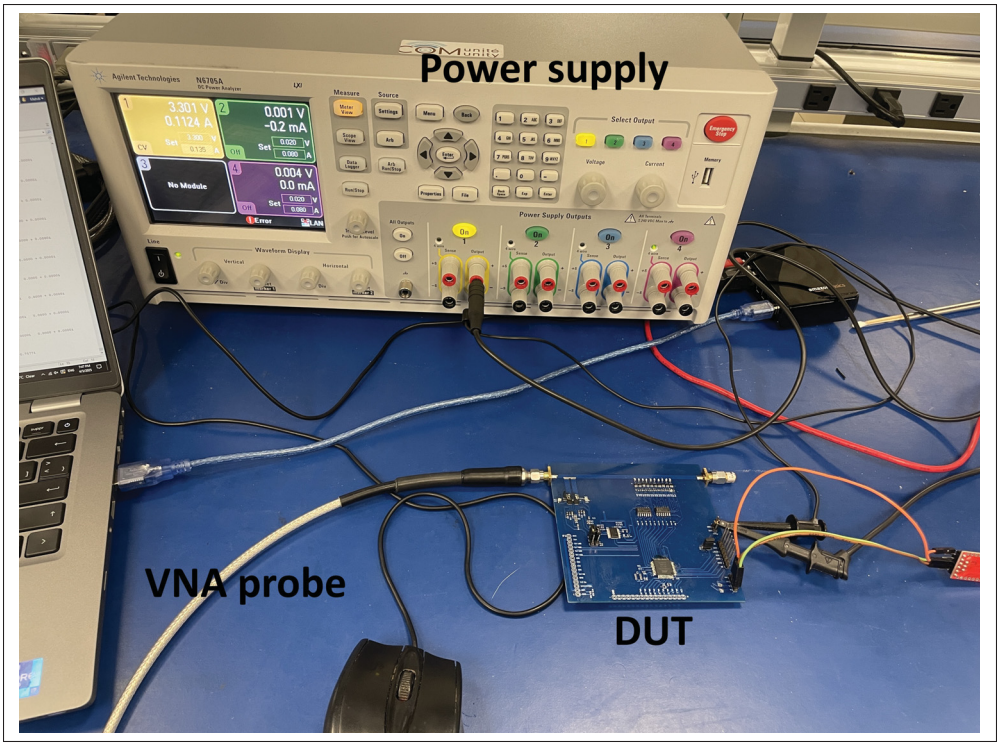


Figure 4.4 Test bench setup (DUT)

Figure 4.5 Electronic calibration module

Measurement results

As shown in Figure 4.6, the final circuit has been fabricated and assembled as designed in Altium , and is now ready for measurement. In Figure 4.7, the circuit is shown under test conditions, and the corresponding results will be analyzed in the following section.

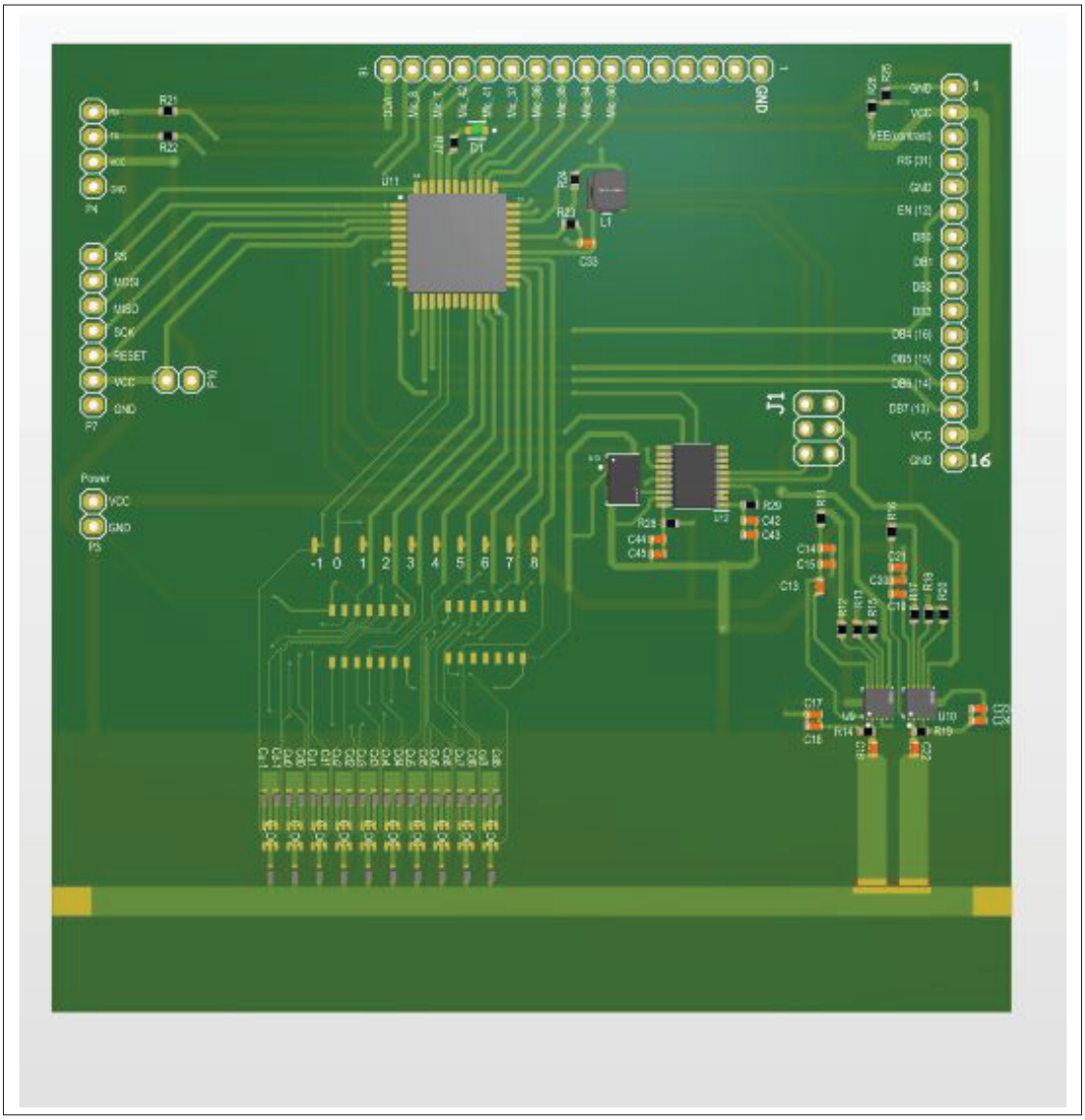


Figure 4.6 Final PCB design in Altium 3D view

As illustrated in Figure 4.7, the circuit was tested with a wideband 50-ohm load connected to its output port. The S_{11} parameter was measured from the input side of the circuit, as shown in Figures 4.8 to 4.11.

This measurement was performed using both a Vector Network Analyzer (VNA) and the embedded system integrated into the circuit. The results obtained from both methods were transferred to MATLAB for visualization and comparative analysis.

As shown in Figures 4.8 to 4.11, the blue points represent the measurement results obtained using the VNA, while the red points indicate the results measured by the embedded system. The magnitude and phase errors have been calculated for each pair of corresponding measurement points, and the error plots for both magnitude and phase are presented. Furthermore, to provide a better understanding, error scatter plots (histograms) have also been drawn, which are shown by frequency in Figures 4.12 to 4.15,.

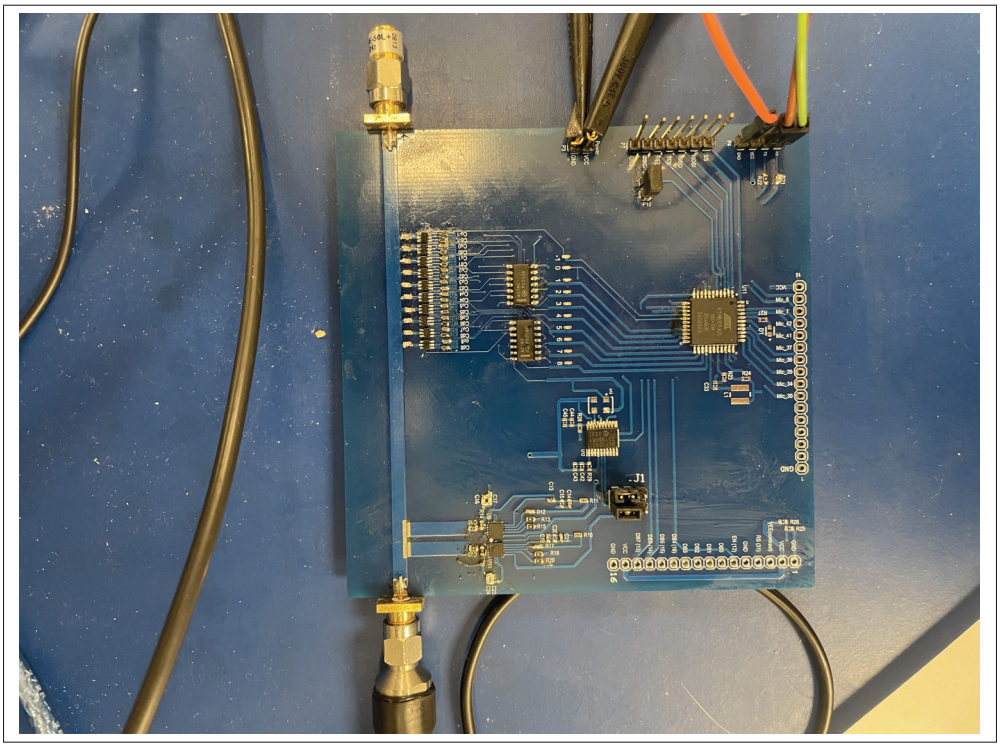


Figure 4.7 Fabricated circuit under the test

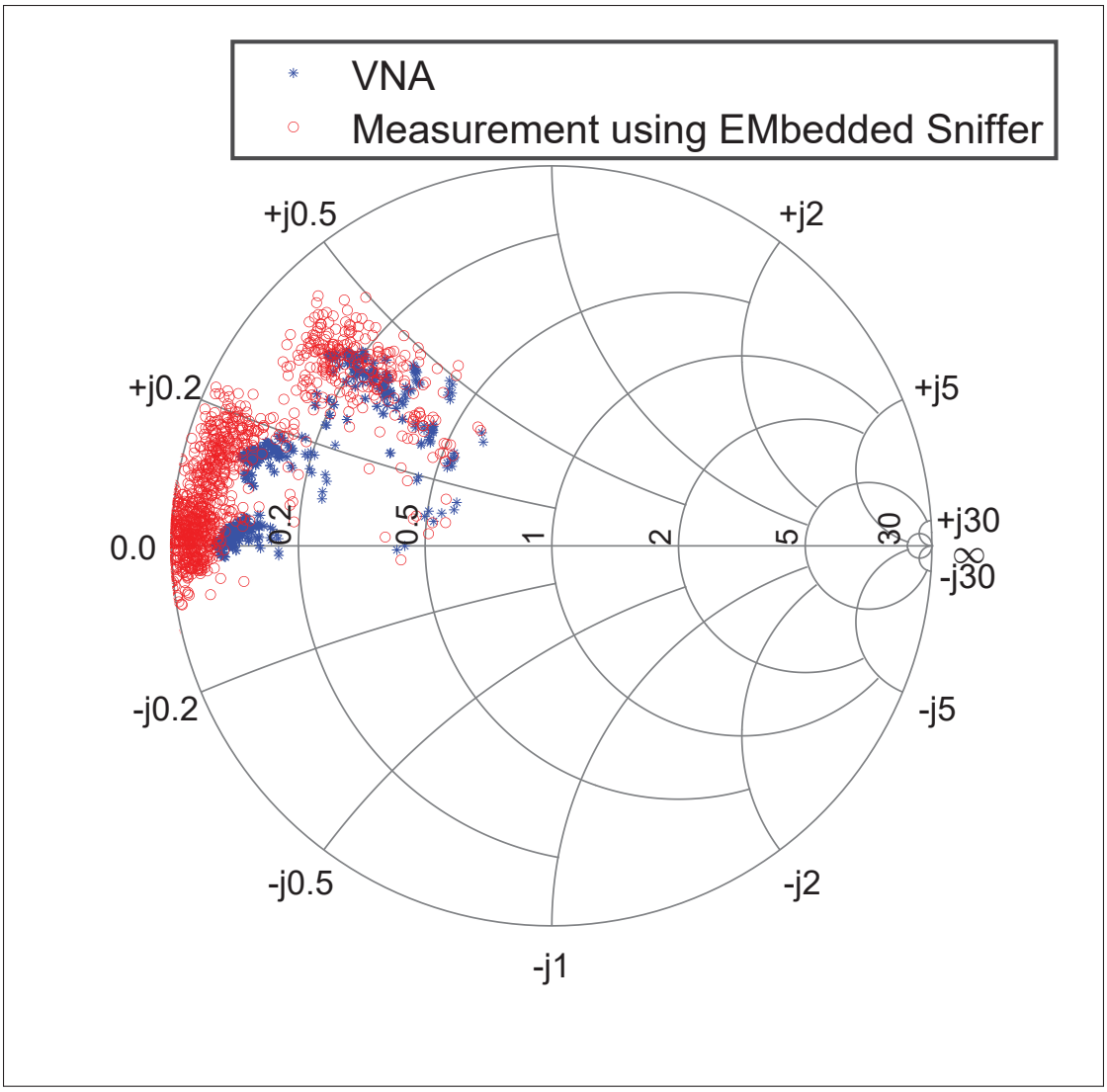


Figure 4.8 Measured S11, plotted on smith chart
Blue dots are VNA output,red dots are sniffer output
F= 1.2 GHz

Plotting S_{11} on the Smith chart enables the analysis of key characteristics such as impedance matching, reflection behavior related to the circuit or transmission line.

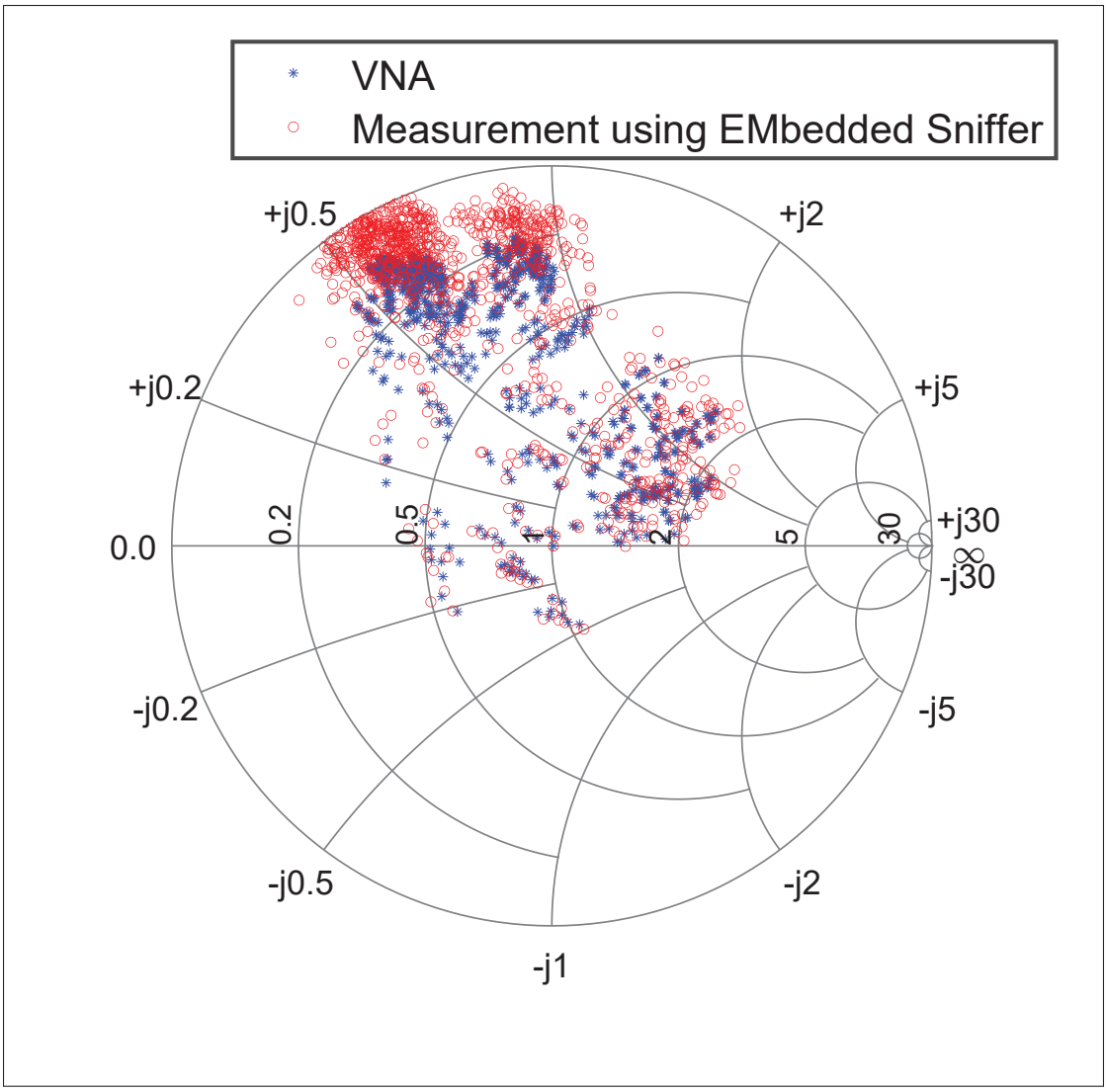


Figure 4.9 Measured S11, plotted on smith chart
Blue dots are VNA output,red dots are sniffer output
F= 1.4 GHz

4.2 Assessment of Board Performance in an Active System

In this research, a system has been developed for use in portable and compact applications. Importantly, this measurement system is not an external tool but an integral part of the system itself. Not only can it perform impedance measurements and matching while the system is operational, but the system's operation is also required for the measurement to occur.

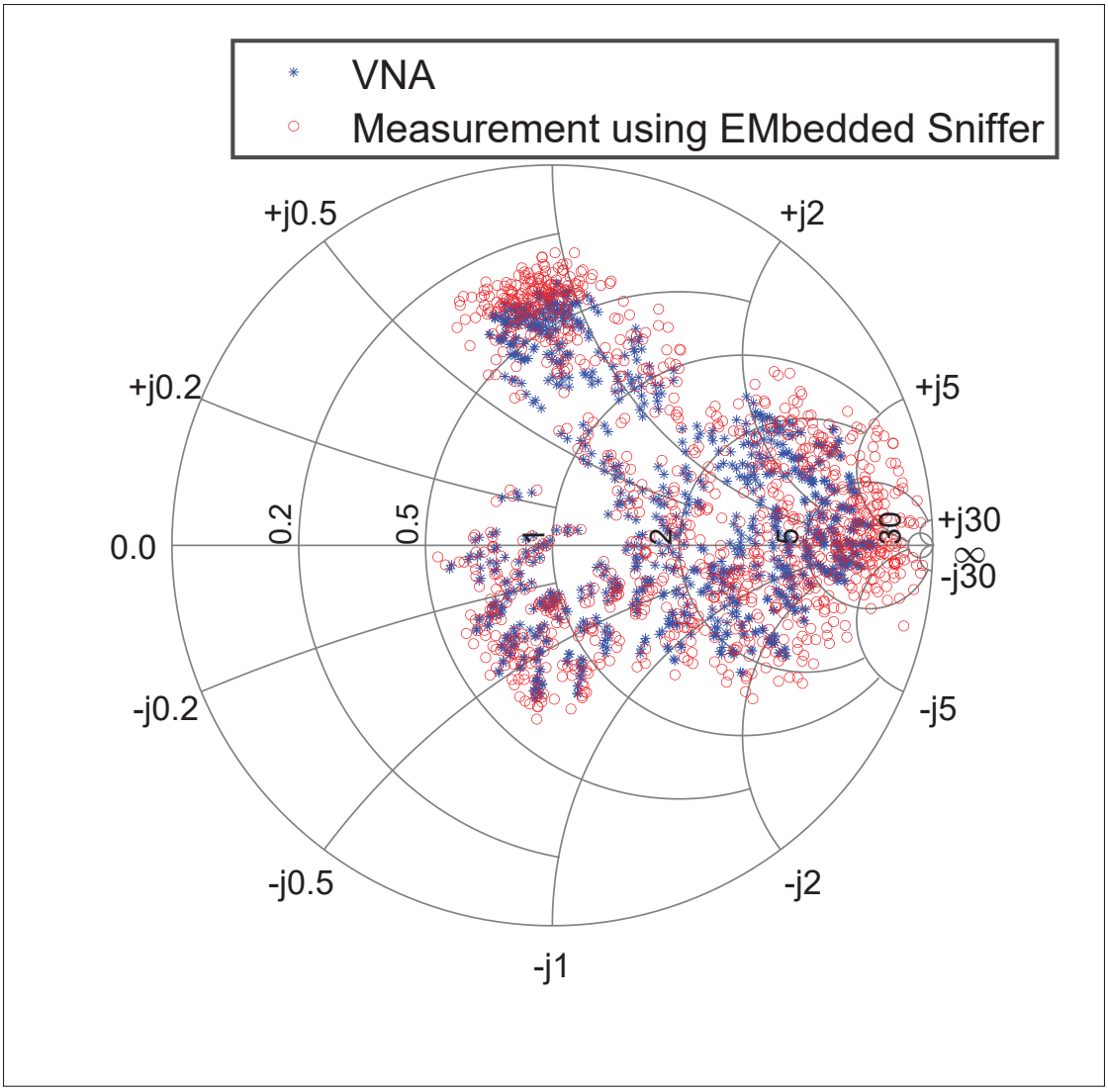


Figure 4.10 Measured S11, plotted on smith chart
Blue dots are VNA output,red dots are sniffer output
F= 1.8 GHz

4.3 Non 50 Ω load test

As illustrated in Figure 4.16 an arbitrary load was implemented. In this experiment, a non-50- Ω load was connected to the proposed matching network, and the search algorithm was executed. For each of the test runs, all 1024 possible switching states, the reflection coefficient was

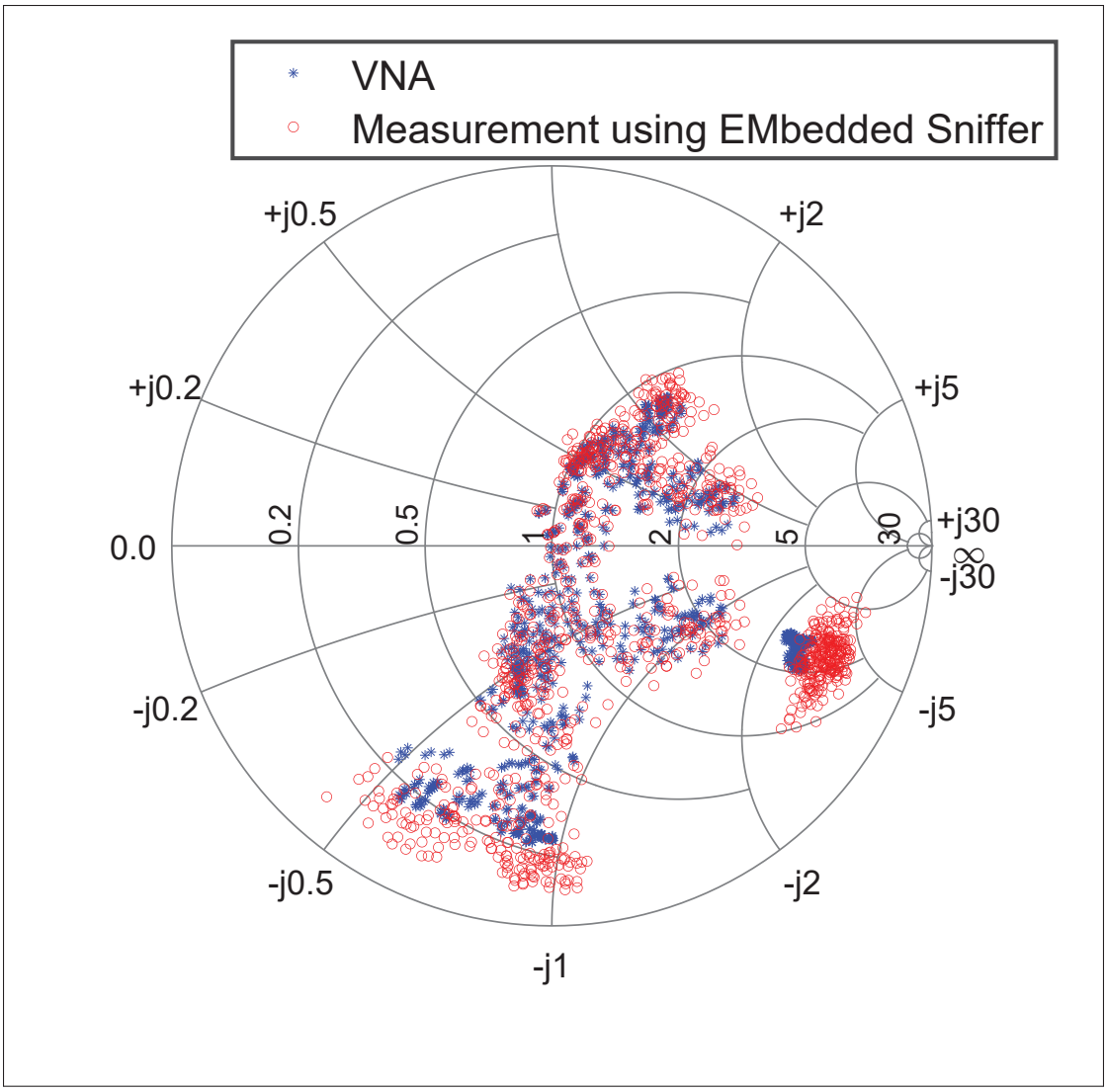
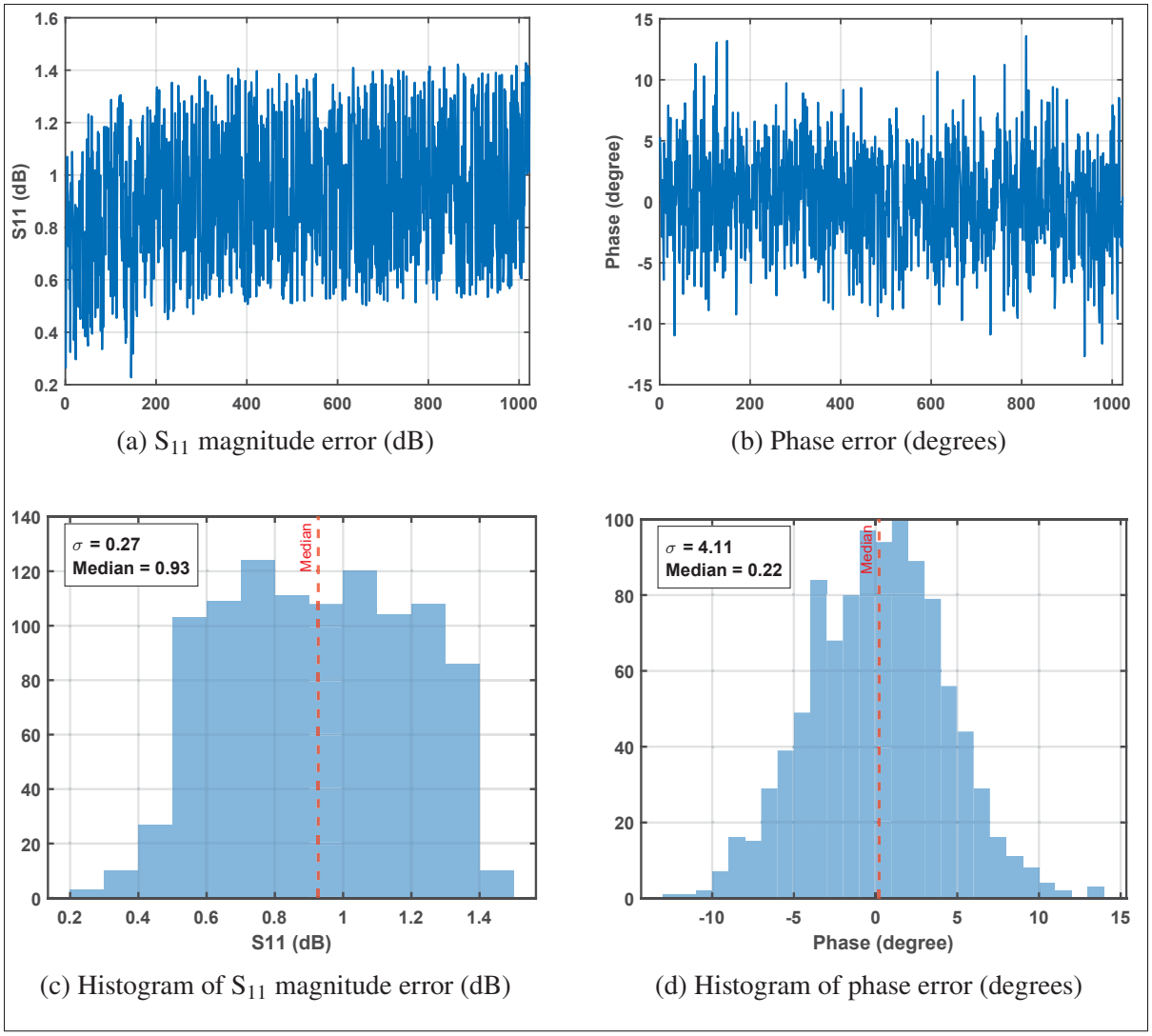


Figure 4.11 Measured S11,plotted on smith chart
Blue dots are VNA output,red dots are sniffer output
F= 2.1 GHz

measured using the VNA and stored for further analysis. The objective of the circuit in this stage was to match the non-50-Ω load to the standard 50-Ω system impedance.

Due to the inherently discrete nature of the proposed reconfigurable matching network, the achievable matching performance depends on the operating frequency and the position of the



(a) S_{11} magnitude error (dB)

(b) Phase error (degrees)

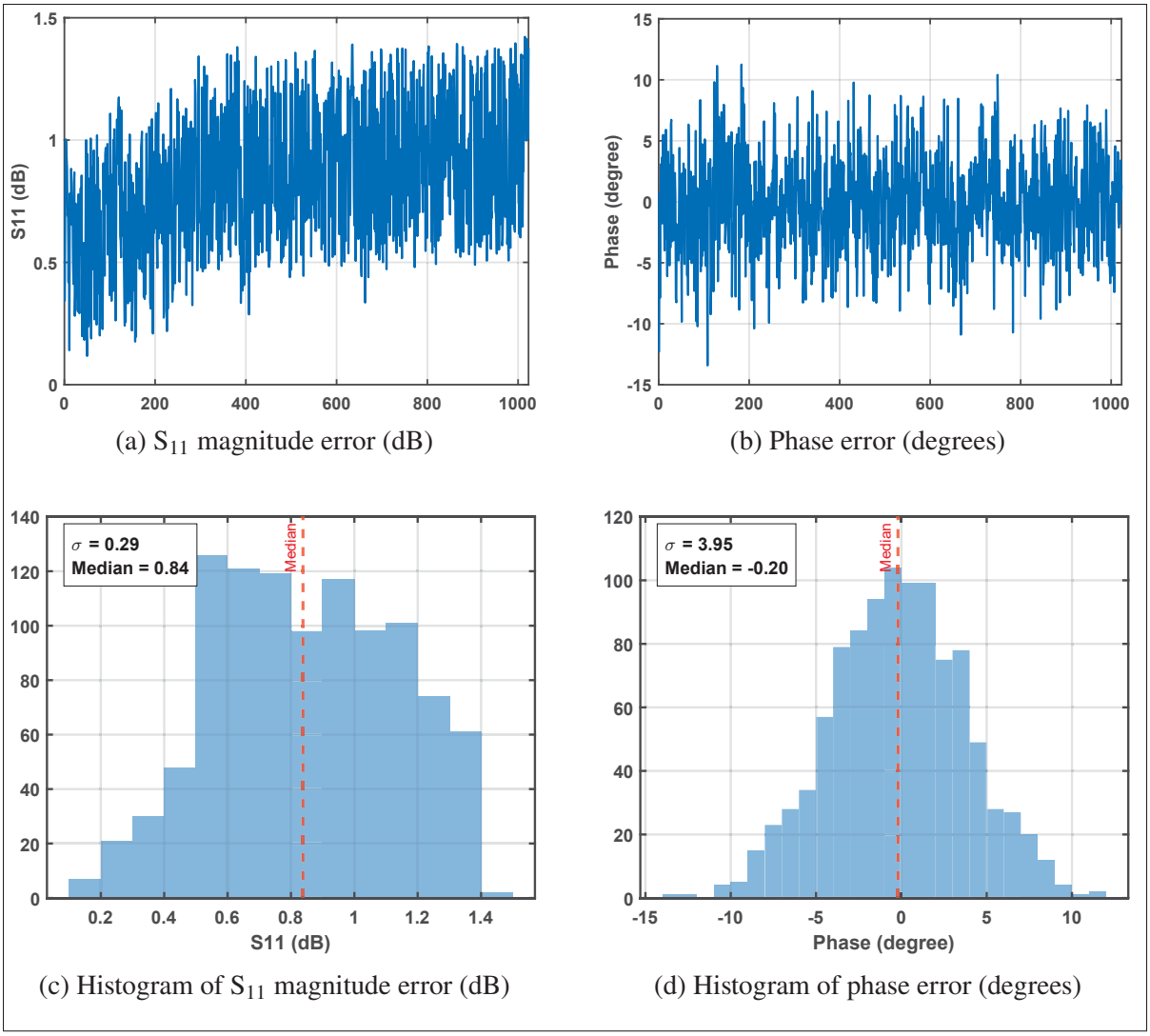
(c) Histogram of S_{11} magnitude error (dB)

(d) Histogram of phase error (degrees)

Figure 4.12 S_{11} magnitude and phase error analysis at 1.2 GHz.

load impedance on the Smith chart. Nevertheless, the results demonstrate that the circuit is capable of transforming a wide range of non-50 Ω loads toward a 50 Ω match.

As shown in Figure 4.17, the blue points indicate the region that the matching network is capable of matching at 1.2 GHz. The red marker represents the selected arbitrary load, with a magnitude of 0.49 and a phase of $-121°$. This load is then mapped to 1024 new impedance states, as illustrated in Figure 4.18 4.18. The figure shows that three out of the 1024 possible states achieve impedance matching.



(a) S_{11} magnitude error (dB)

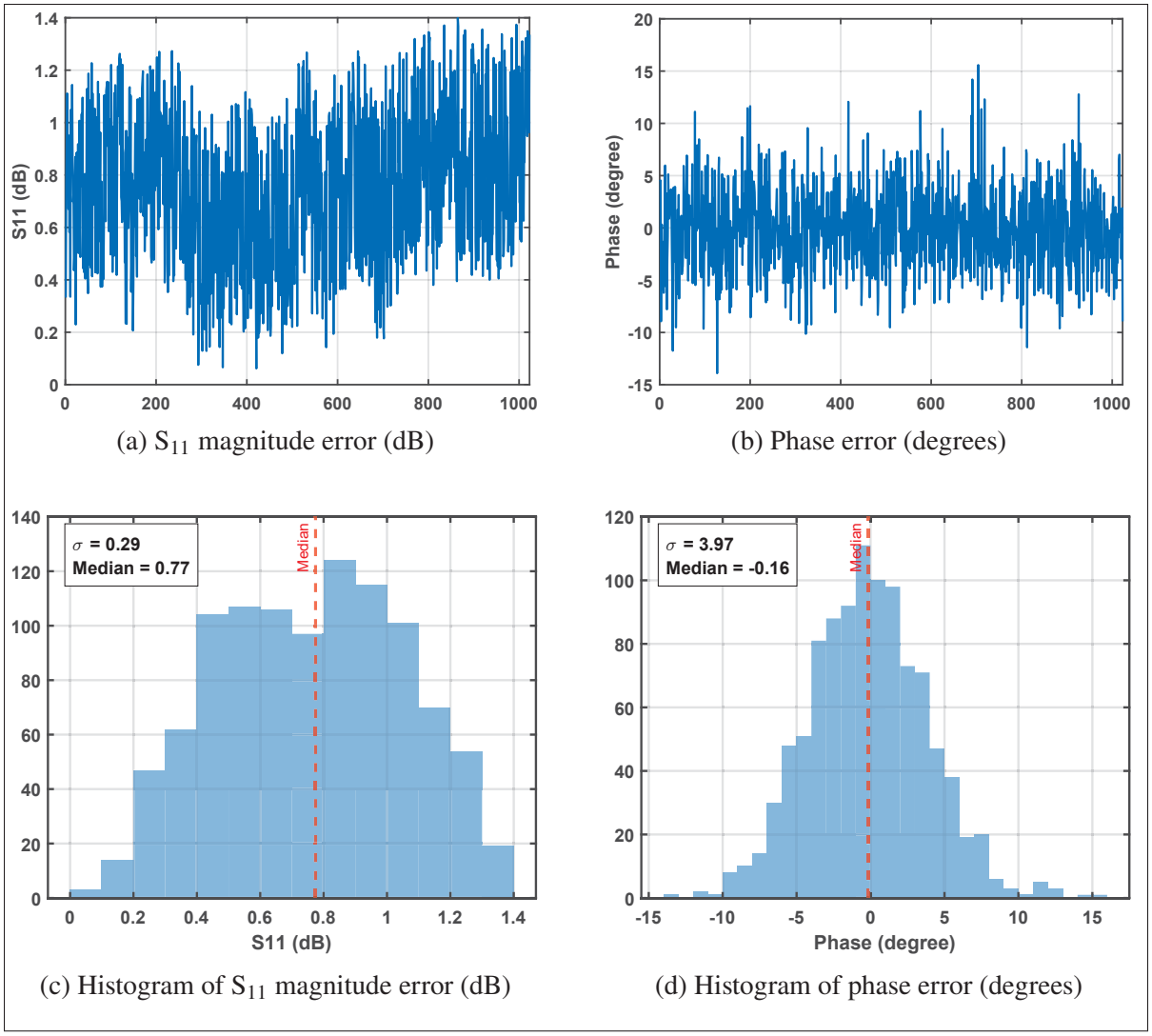
(b) Phase error (degrees)

(c) Histogram of S_{11} magnitude error (dB)

(d) Histogram of phase error (degrees)

Figure 4.13 S_{11} magnitude and phase error analysis at 1.4 GHz.

The same procedure is applied to another load with a magnitude of 0.25 and a phase of $-167°$ at a frequency of 1.8 GHz. The selected load and the corresponding coverage region are shown in Figure 4.19. Furthermore, Figure 4.20 demonstrates that impedance matching is achieved at a single state for this case.



(a) S_{11} magnitude error (dB)

(b) Phase error (degrees)

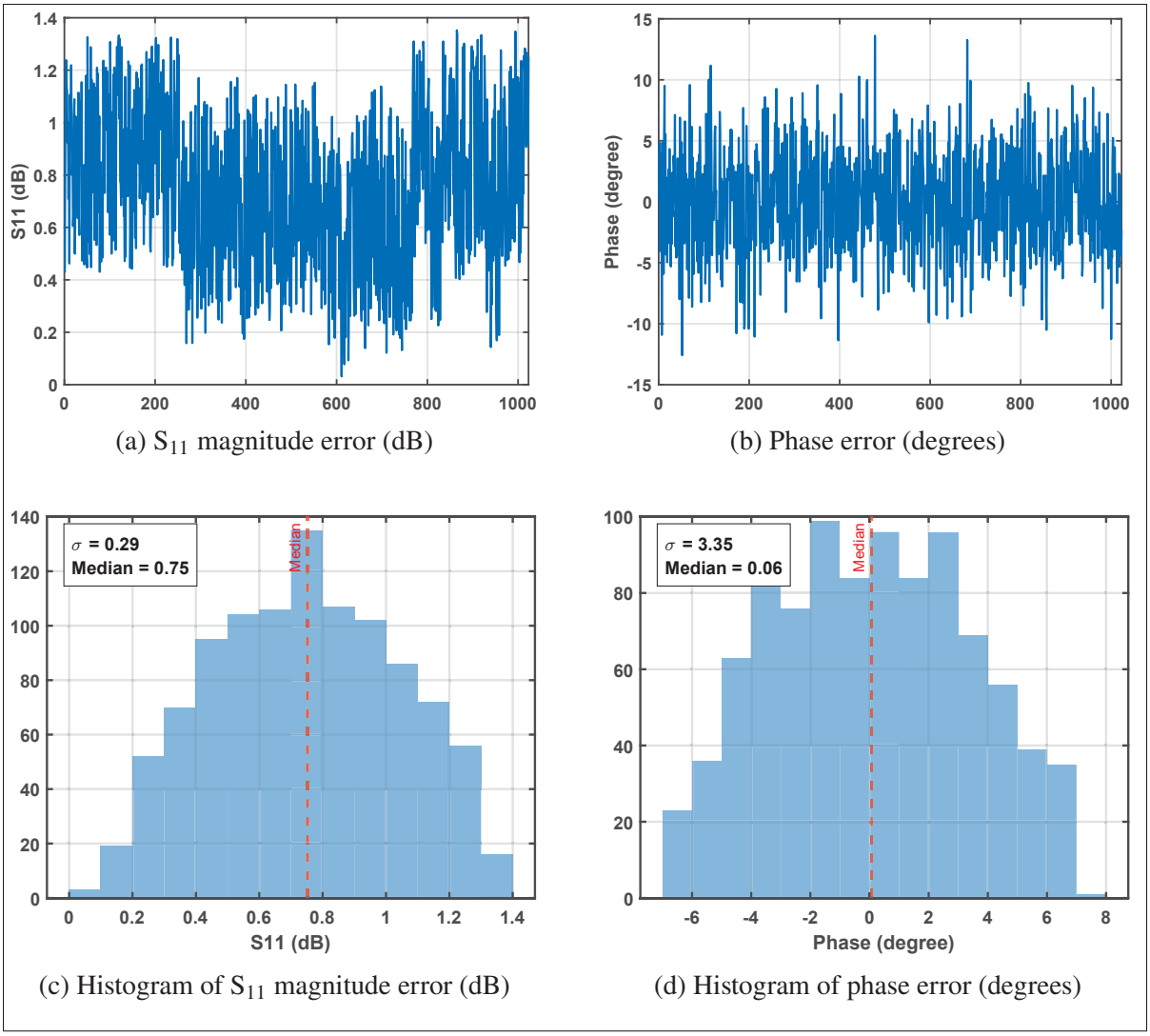
(c) Histogram of S_{11} magnitude error (dB)

(d) Histogram of phase error (degrees)

Figure 4.14 S_{11} magnitude and phase error analysis at 1.8 GHz.

4.4 Timing Analysis and Performance

This section presents a timing analysis and performance evaluation of the system, highlighting operational constraints and possible improvements. Most systems involve an initial configuration phase, which occurs only once at startup and is therefore excluded from the timing assessment. Instead, we focus on system behavior following any change in load or operating frequency, which triggers a sequence of operations required to reach a new steady state.



(a) S_{11} magnitude error (dB)

(b) Phase error (degrees)

(c) Histogram of S_{11} magnitude error (dB)

(d) Histogram of phase error (degrees)

Figure 4.15 S_{11} magnitude and phase error analysis at 2.1 GHz.

First, the signal power on the transmission line is converted into a voltage signal using the LTC5582 chip. This analog voltage is then passed to the analog-to-digital converter (MCP3561), where it is digitized. The resulting binary data is transmitted to the microcontroller. The algorithm implemented on the microcontroller computes the reflection coefficient and stores the result in memory.

The time required for this part of the process depends on several factors, including the microcontroller's operating frequency, its internal architecture, and the software compiler used.

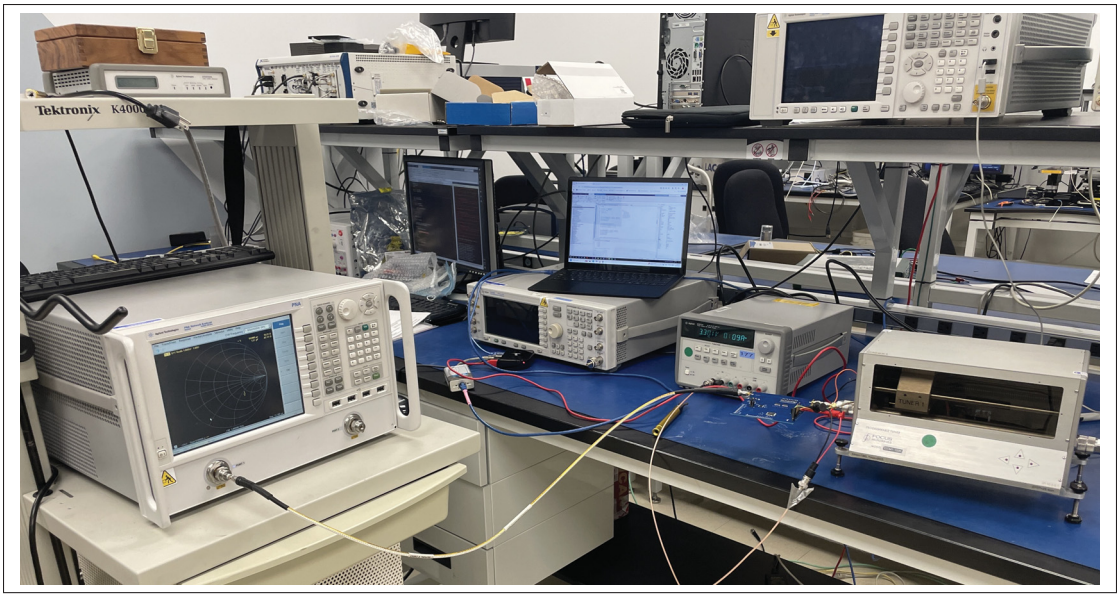


Figure 4.16 Non 50 Ω load test

In the current design, an ATmega16 microcontroller operating at a maximum frequency of 16 MHz is used.

Following this, the system iterates through 256 different switch configurations (an 8-bit binary sequence), recalculates the reflection coefficient for each configuration, and then selects the one that yields the optimal match.

It is important to note that the processing time of the microcontroller significantly exceeds that of other system components. The response time of the analog front-end components (e.g., LTC5582 and MCP3561) is in the nanosecond range and can therefore be considered negligible in comparison.

To improve system speed, one option is to replace the ATmega16 with a more powerful processor, such as one from the ARM family, which can operate at frequencies up to 1.4 GHz. Additionally, algorithmic optimization is possible. For instance, predictive methods can be employed to anticipate the optimal switch configuration, reducing the total number of iterations.

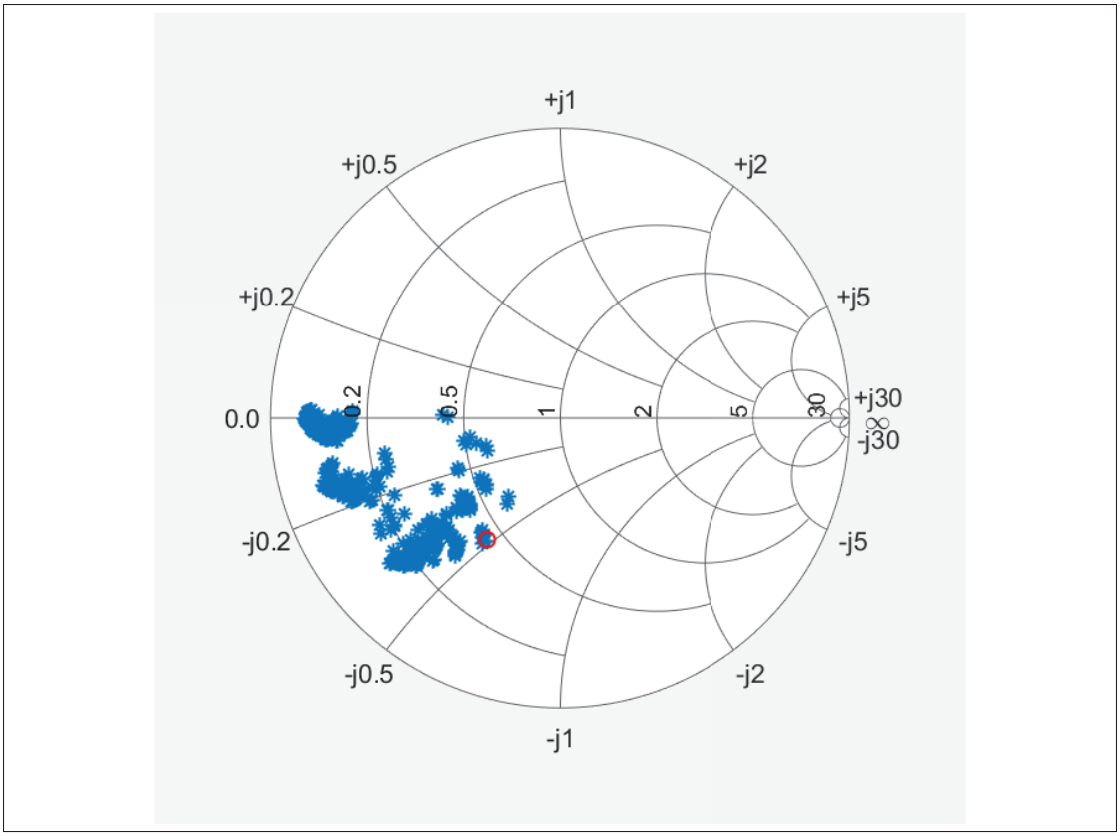


Figure 4.17 Covered area in blue, Chosen load in red at 1.2 GHz

Machine learning or artificial intelligence (AI) algorithms could also be applied to enhance decision-making efficiency.

However, these enhancements come at a cost. High-performance processors increase financial expense and power consumption, which is a critical concern in battery-powered portable systems. Furthermore, implementing AI-based solutions introduces additional complexities, including the need for data collection, model training (either offline or in real time), and increased hardware resources to support such computations.

To evaluate the accuracy of the embedded measurement system, S_{11} measurements were collected at four different frequencies:At 1.2 GHz, 1.4 GHz, 1.8 GHz, and 2.1 GHz. For each frequency,

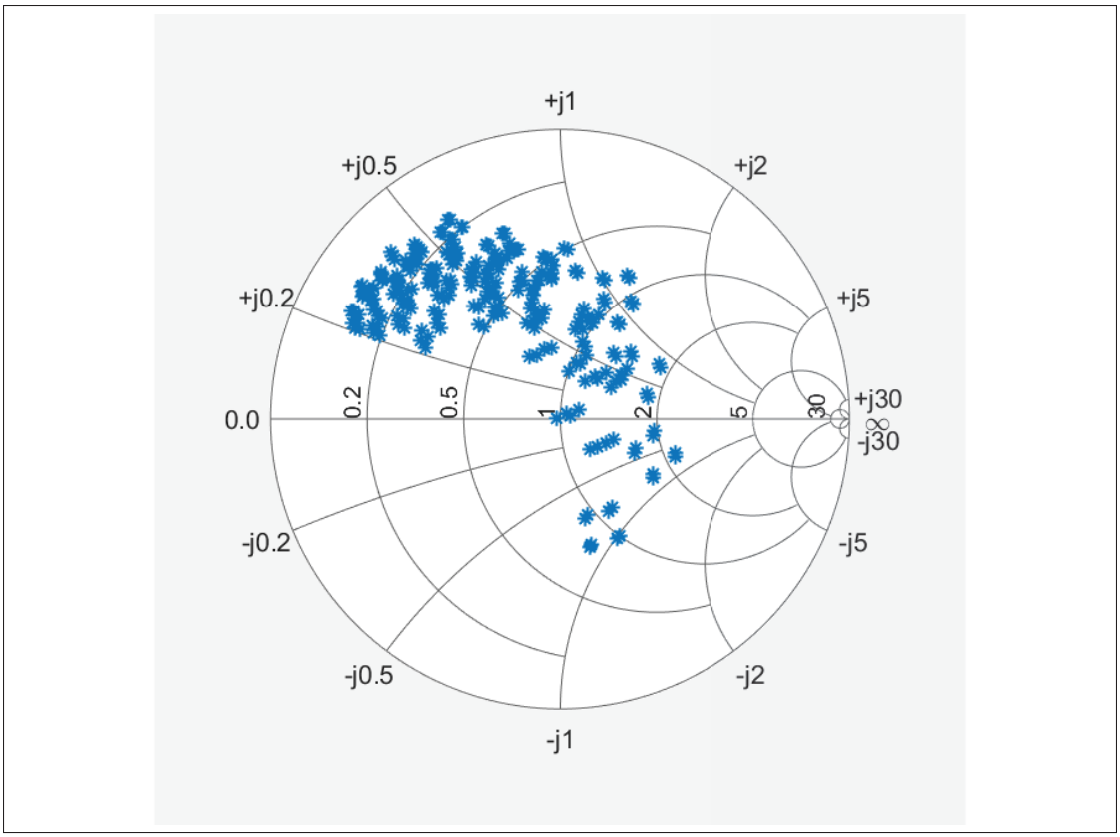


Figure 4.18 maped load to 1024 posible option at 1.2 GHz

both the magnitude and phase errors between the embedded system and the reference VNA measurements were computed.

The results are organized into four groups of figures, each corresponding to a specific frequency. Within each group, four of plots are presented:

- **a)** S_{11} magnitude error (dB)
- **b)** S_{11} phase error(degrees)
- **c)** histogram of S_{11} magnitude error (dB)
- **d)** phase error (degrees)

These plots provide insight into both the point-by-point deviation and the overall error distribution for each frequency.

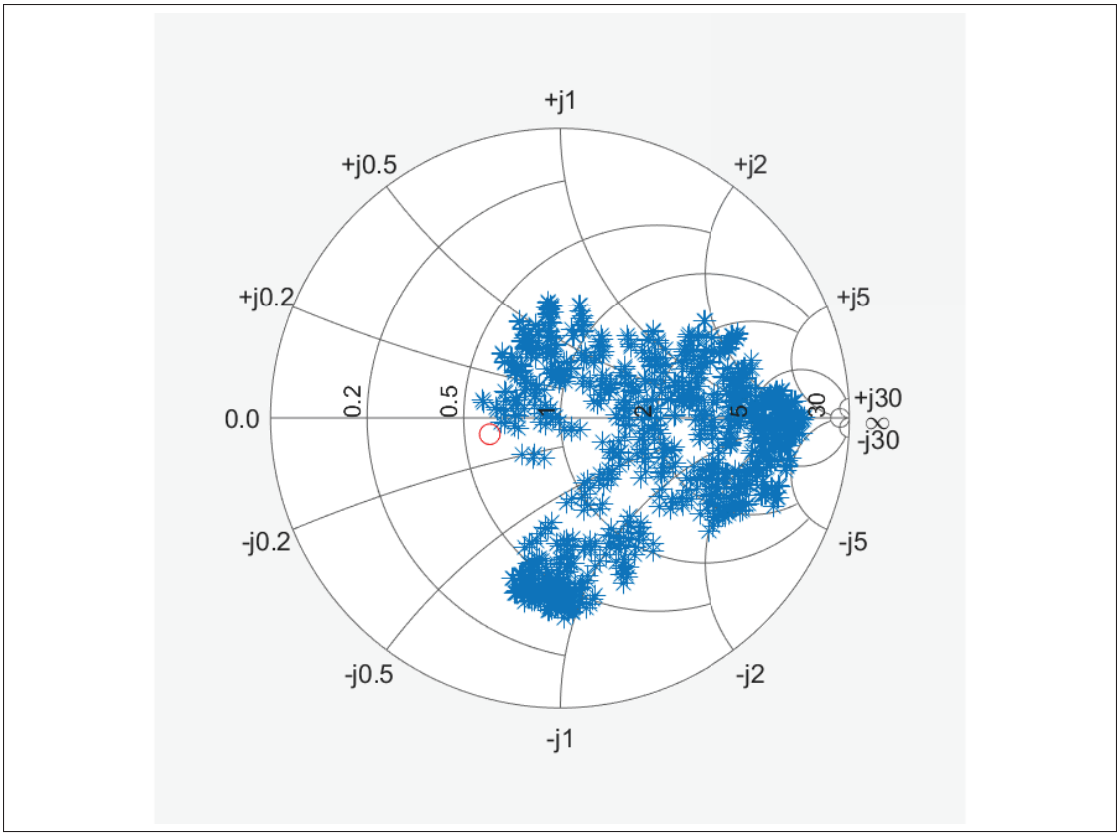


Figure 4.19 Covered area in blue, Chosen load in red at 1.8 GHz

At **1.2 GHz**, the S_{11} magnitude and phase errors remain low and relatively consistent across samples, with histogram plots showing a tight distribution centered near zero. The magnitude error has a median value of 0.93 dB, while the phase error is centered around a median of 0.22°. This indicates high agreement between the embedded system and the VNA at this frequency.

At **1.4 GHz**, a slight better resualts is observed in both error types. The magnitude error median decreases to 0.84 dB, and the phase error median shifts slightly to −0.20°. The histogram plots still show narrow distributions, suggesting good measurement stability with minor deviations.

At **1.8 GHz**, the error plots reveal larger fluctuations in both magnitude and phase compared to 1.4 GHz, though the overall error values continue to decrease. The magnitude error median drops to 0.77 dB, and the phase error median is −0.16°. The histograms show a broader

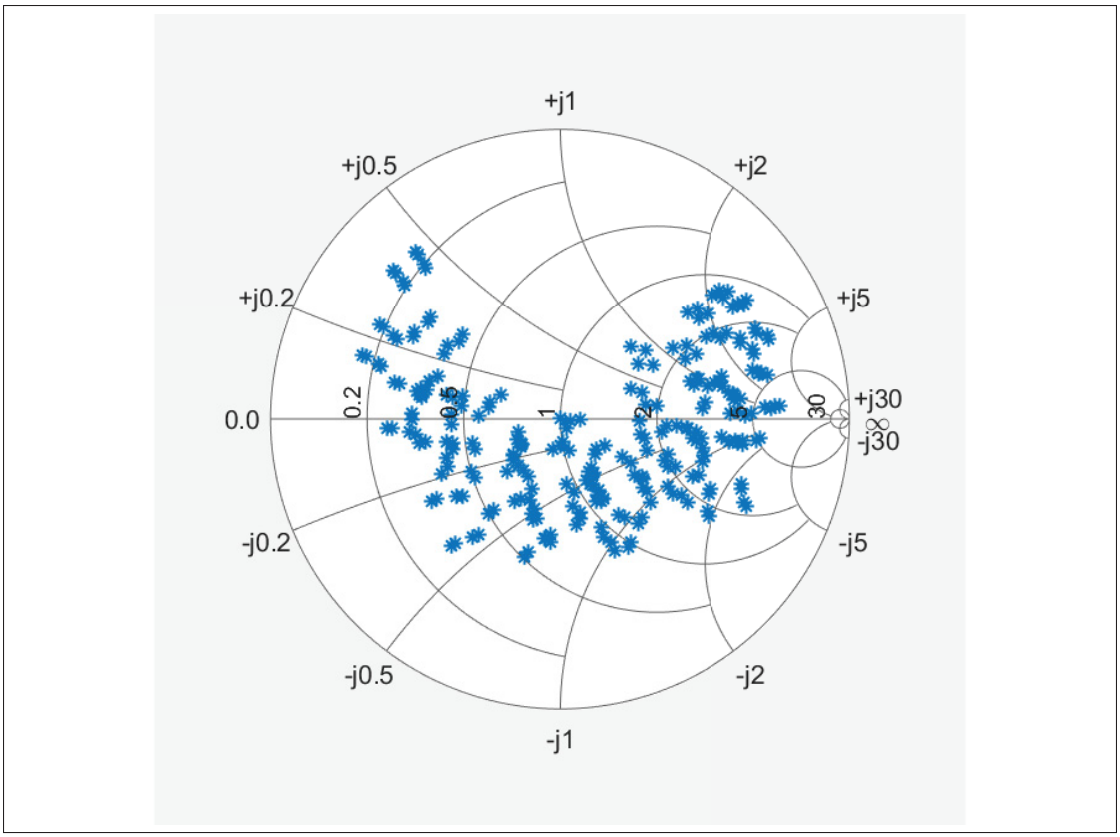


Figure 4.20 maped load to 1024 posible option at 1.8 GHz

spread, particularly for the phase error, suggesting reduced accuracy likely related to sensitivity variations in analog components.

At **2.1 GHz**, the magnitude error continues its downward trend with a median of 0.75 dB, while the phase error median increases slightly to 0.06°. Despite this slight rise in phase offset, the overall distribution remains symmetric and relatively narrow, indicating that the system maintains acceptable performance even at higher frequencies.

Overall, the plots and histograms demonstrate that the embedded measurement system maintains stable and acceptable accuracy across the evaluated frequency range. In contrast to typical expectations, the system does not degrade at higher frequencies; instead, both magnitude and phase errors slightly improve.

CONCLUSION AND RECOMMENDATIONS

To achieve optimal power transmission in telecommunication transmission lines, it is essential to match the impedance of the line with any connected devices, such as sources, loads, or adjacent circuit blocks. Impedance varies with multiple factors, including the frequency of the transmitted wave. As a result, in multi-frequency telecommunication systems, impedance matching is often lost when the operating frequency changes.

This thesis focused on the development of a regulating system that corrects the wave reflection coefficient along the transmission line. Chapter 1 reviewed related work and introduced the theoretical background, while Chapter 2 provided a more focused discussion of specific concepts. Chapter 3 presented the methodology and design approach used to implement the system.

In Chapter 4, the hardware components used in the system were introduced, including a detailed description of the matching circuit and its physical layout. Additionally, the system's operation was explained, and a comparison between simulated and experimental measurements was provided.

Based on the results, it is evident that the system is capable of correcting impedance mismatches across a wide range of values on the Smith chart, covering the frequency band from 1.2 GHz to 2.1 GHz. Using eight SPDT switches in the matching network, the system supports 1024 discrete matching states. Experimental results demonstrated that both S_{11} magnitude and phase error remained within acceptable bounds throughout the frequency range, with the best performance observed at higher frequencies (1.8–2.1 GHz). The median magnitude error decreased from 0.93 dB at 1.2 GHz to 0.75 dB at 2.1 GHz, while the phase error median remained centered around 0°. Contrary to common assumptions, system performance did not degrade at higher frequencies and instead showed improved consistency and accuracy.

Employing low-loss substrates, precision capacitors, or higher-performance RF switches could further improve matching accuracy and reduce signal attenuation. However, these improvements may also increase the system's complexity and cost. Balancing performance and practicality will be an important consideration for future designs.

APPENDIX I

SNIFFER PCB SUBSTRATE SPECIFICATIONS - CHAPTER 4

Figure I-1 shows the Sniffer PCB substrate specifications.

Material		Permittivity (Er)			Permeability (MUr)	
Material Name	Library	Real	Imaginary	TanD	Real	Imaginary
Alumina	**Des_lib**	9.6			1	
FR_4_Core	**Des_lib**	4.6		0.01	1	
FR_4_Prepreg	**Des_lib**	4.6		0.01	1	
FR_4_TG140	**Des_lib**	4.5		0.019	1	
FR_4_TG150	**Des_lib**	4.5		0.018	1	
SolderMask	**Des_lib**	3.3			1	

Figure-A I-1 Sniffer PCB substrate specificity

APPENDIX II

THE LTC5582 SPESIFICATIONS - CHAPTER 4

The figure II-1 illustrates the linearity error versus input power for the LTC5582, showcasing its performance in maintaining linearity across different input power levels. The figure II-2 demonstrates the relationship between output voltage and RF input power, providing insights into how the LTC5582 responds to varying RF input power. These figures collectively offer valuable information about the LTC5582's linearity and voltage output characteristics, aiding in its evaluation and optimization for specific applications.

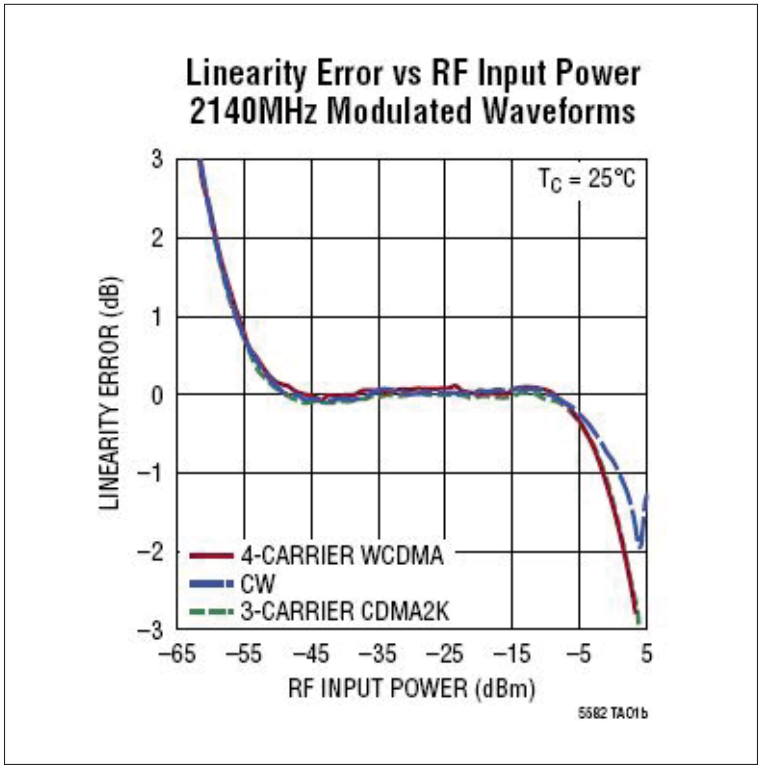


Figure-A II-1 LTC5582 Liniarity
Taken fromAnalogdevices (1965)

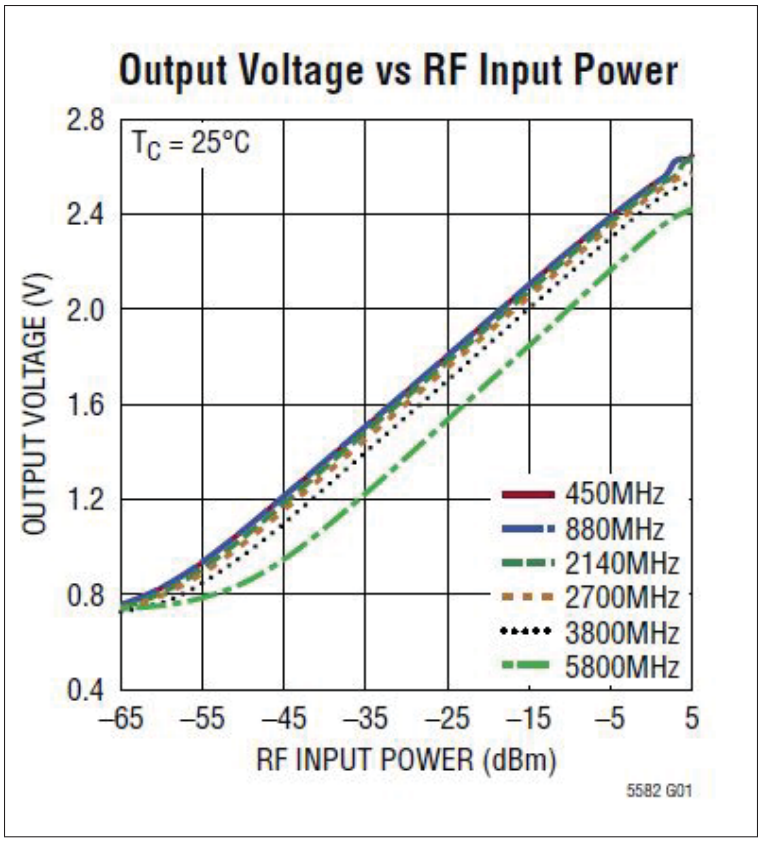


Figure-A II-2 LTC5582 Output Voltage vs RF Input Power.
Taken fromAnalogdevices (1965)

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