LTCC-Integrated MEMS Switches and Impedance Tuners for Field Programmable Amplifiers

by

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Commutateurs MEMS et accordeurs d'impédance intégrés LTCC pour amplificateurs programmables sur site

Ehsan FALLAH NIA

RÉSUMÉ

La conception d'un amplificateur micro-ondes programmable sur site (FPMA), objectif principal de cette thèse, répond au besoin des systèmes de communication sans fil de disposer de circuits reprogrammables matériellement sans circuits redondants. Ces circuits doivent pouvoir fonctionner dans des bandes de fréquences larges tout en conservant un encombrement minimal. Pour atteindre ces objectifs, un nouveau procédé de fabrication utilisant les technologies de céramique cocuite à basse température (LTCC) et de systèmes microélectromécaniques (RF-MEMS) a été développé. Ce procédé monolithique permet de fabriquer des dispositifs MEMS sur des substrats LTCC fonctionnels. L'exploitation des fonctionnalités des LTCC et la possibilité de fabriquer et d'aligner des circuits MEMS sur des circuits RF et DC intégrés dans les LTCC ont ouvert la voie à une nouvelle conception d'amplificateurs micro-ondes reconfigurables. À cette fin, et pour démontrer la faisabilité du procédé présenté, deux conceptions pour les bandes basses (3-5 GHz) et hautes (5-8 GHz) sont proposées. Grâce à de nouvelles conceptions monolithiques, des accordeurs d'impédance DMTL intégrés sont fabriqués simultanément avec des composants MEMS de surface et un renifleur intégré, afin de former un amplificateur micro-ondes reconfigurable. Le FPMA est fabriqué en cascade : des réflectomètres intégrés sont placés à l'entrée du DMTL pour détecter le gamma d'entrée approprié du transistor et lui envoyer les données afin de choisir la meilleure combinaison de commutation pour l'adaptation de fréquence sur toute la bande. Les modules fabriqués permettent l'adaptation d'impédance avec un gain d'entrée maximal tout en minimisant les pertes dues au diélectrique et aux conducteurs. Les conceptions proposées permettent une adaptation d'impédance continue grâce à l'interaction entre le DMTL et les renifleurs intégrés, tout en maintenant un encombrement total du module aussi réduit que possible par rapport aux travaux disponibles dans la littérature.

Mots clés : RF-MEMS, procédé monolithique, LTCC, réflectomètre renifleur, DMTL, amplificateur reconfigurable

LTCC-Integrated MEMS Switches and Impedance Tuners for Field Programmable Amplifiers

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ABSTRACT

Designing a Field Programmable Microwave amplifier (FPMA) as the main objective of the present thesis is derived from the need in wireless communication systems to have circuits which are able to be reprogrammed in hardware without redundant circuits. Such circuits should be able to operate in wide-band frequency ranges while their total footprints kept as small as possible. To realize these objectives, a novel fabrication process using Low Temperature Co-Fired Ceramic (LTCC) and RF-MEMS (Microelectromechanical systems) technologies is developed as a published paper which uses a monolithic process to fabricate MEMS devices on top of functional LTCC substrates. Leveraging the functionality of LTCC and being able to fabricate and align MEMS circuit on top of embedded RF and DC circuits inside the LTCC, opened a path to provide a new design for reconfigurable microwave amplifiers. To this end, and to demonstrate the capability of the presented process, two design for low (3-5 GHz) and high bands (5-8 GHz) are proposed. Using the novel monolithic designs, embedded DMTL impedance tuners are fabricated in a simultaneous process with surface MEMS devices and an embedded sniffer to have a reconfigurable microwave amplifier. Designed FPMA is fabricated in a cascade form where embedded reflectometers are placed at the input of DMTL to detect proper input gamma of the transistor and send the data to DMTL to choose the best switching combination for frequency matching over the entire band. Fabricated modules are able to do the impedance matching with maximum input gain considering minimum losses that are derived from dielectric and conductors. Proposed designs are able to continuously do the impedance matching using the interaction between DMTL and embedded sniffers while total footprint of the module is kept as small as possible compared to the available works in the literature.

Keywords: RF-MEMS, Monolithic process, LTCC, sniffer reflectometer, DMTL, reconfigurable amplifier

TABLE OF CONTENTS

LIST OF TABLES

Page

LIST OF FIGURES

Page

LIST OF ABBREVIATIONS AND ACRONYMS

3D	3 Dimensional
3DP	Three-Dimensional Printing
5G	Fifth Generation (wireless communication standard)
6G	Sixth Generation (wireless communication standard)
AAO	Anodic Aluminum Oxide
AFM	Atomic Force Microscopy
ALD	Atomic Layer Deposition
AM	Additive Manufacturing
BAW	Bulk Acoustic Wave
BJ	Binder Jetting
CMOS	Complementary Metal Oxide Semiconductor
CMP	Chemical Mechanical Polishing
CMUT	Capacitive Micromachined Ultrasonic Transducer
CPD	Critical Point Drying
CPW	Coplanar Waveguide
CTE	Coefficient of Thermal Expansion
CVD	Chemical Vapor Deposition
DI	Deionized (water)
DIW	Direct Ink Writing
DLP	Digital Light Processing
DMTL	Distributed MEMS Transmission Line
DXF	Drawing Exchange Format (AutoCAD file format)
FDM	Fused Deposition Modeling

FET	Field Effect Transistor
FPMA	Field Programmable Microwave Amplifier
GSG	Ground Signal Ground
HB	Higher Band
IPA	Isopropyl Alcohol
ISO	International Organization for Standardization
LB	Lower Band
LCD	Liquid Crystal Display
LED	Light Emitting Diode
LIS	Laser Induced Structuring
LNA	Low Noise Amplifier
LOM	Laminated Object Manufacturing
LTCC	Low Temperature Co Fired Ceramics
MEMS	MicroElectroMechanicalSystems
MIM	Metal Insulator Metal (capacitor structure)
MJ	Material Jetting
MMIC	Monolithic Microwave Integrated Circuit
MOEMS	Micro Opto-Electromechanical Systems
PA	Power Amplifier
PAS	Pulsed Argon Laser Sintering
PCB	Printed Circuit Board
PDMS	Polydimethylsiloxane
PECVD	Plasma Enhanced Chemical Vapor Deposition
PIN	Positive Intrinsic Negative (semiconductor diode structure)

PLAS	Pulsed Laser Assisted Sintering
PMUT	Piezoelectric Micromachined Ultrasonic Transducer
PNA	Performance Network Analyzer (Keysight's advanced VNA family)
PVD	Physical Vapor Deposition
PZT	Lead Zirconate Titanate
RF	Radio Frequency
RH	Relative Humidity
RIE	Reactive Ion Etching
RPM	Round Per Minute
SAW	Surface Acoustic Wave
SCPLAS	Single Crystal Pulsed Laser Assisted Sintering
SEM	Scanning Electron Microscope
SLA	Stereolithography
SLM	Selective Laser Melting
SLS	Selective Laser Sintering
SOI	Silicon on Insulator
SOLT	Short Open Load Thru (calibration method)
TRL	Thru Reflect Line (calibration method)
VNA	Vector Network Analyzer
VSWR	Voltage Standing Wave Ratio
YSZ	Yttria Stabilized Zirconia
ε_0	Vacuum permittivity
ε_r	Relative permittivity
ε_{eff}	Effective dielectric constant

Z_0	Characteristic impedance
E_L	Electrical length
Z_L	Load Impedance
Z_{in}	Input impedance
λ	Wavelength
β	Propagation constant
α	Attenuation constant
Γ	Reflection coefficient
Γ_L	Load Reflection coefficient
Tan δ	Dielectric tangent loss

INTRODUCTION

0.1 Background and motivation

The increasing demand for reconfigurable and adaptive microwave systems in communication, sensing, and defense applications has driven the development of tunable RF front-ends. Traditional fixed-design microwave amplifiers are limited in handling variations in load impedance, frequency spectrum, and environmental conditions. This limitation motivates the need for Field-Programmable Microwave Amplifiers (FPMA) that can dynamically adapt to operating conditions in real-time. There are several works on implementing FPMA using semiconductor switches, but limited bandwidth is achievable.

RF MEMS (Micro-Electro-Mechanical Systems) technology has emerged as a promising solution for implementing highly linear, low-loss, and reconfigurable microwave circuits. In particular, Distributed MEMS Transmission Line (DMTL) tuners offer wide tuning ranges with excellent power handling. Different substrates and packaging technologies with silicon-based, glass and quartz materials are reported for DMTL matching network designs to be implemented on FPMA. Meanwhile, Low Temperature Co-Fired Ceramic (LTCC) technology provides a compact, multilayer substrate platform that allows RF and DC lines to be buried, reducing parasitics, improving reliability, and enabling heterogeneous integration.

The combination of LTCC substrates with MEMS devices on top creates a powerful platform for realizing compact and functional microwave subsystems.

In this work, LTCC is used not only as a packaging medium but also as a functional substrate, embedding bias networks, RF distribution, and sensing elements directly into the multilayer ceramic.

0.2 Problem statement

Despite significant advances in implementing FPMAs, the integration of real-time adaptive matching within microwave amplifiers remains a challenge. Current solutions face several limitations:

- **RF semiconductor switches** suffer from high power consumption, more losses and larger footprints.
- **Conventional tuners** are bulky and difficult to embed in compact amplifier modules.
- **Adaptive matching techniques** often rely on external circuitry, increasing complexity and power consumption.

There is a clear need for a compact, embedded, and intelligent tuning solution that can dynamically adjust amplifier input matching without degrading RF performance.

This thesis addresses the problem by developing a field-programmable microwave amplifier architecture that leverages MEMS DMTL tuners fabricated on LTCC substrates. The LTCC not only hosts the RF and DC lines but also incorporates a buried sniffer circuit capable of measuring input impedance in real time. This feedback mechanism enables the tuner to automatically adjust and achieve optimal input matching for the amplifier.

0.3 Thesis objectives

The primary objective of this thesis is to design, fabricate, and demonstrate a field-programmable microwave amplifier using MEMS-based DMTL tuners integrated with LTCC technology. The specific goals are:

1. **Design of MEMS DMTL Tuners**
    - Develop MEMS-based distributed transmission line tuners with wide tuning range and low insertion loss.
2. **Integration with LTCC Substrate**
    - Utilize LTCC as a functional substrate to embed RF and DC bias lines, minimizing parasitics and improving reliability.
3. **Development of Buried Sniffer Circuits**
    - Design and implement a sniffer circuit in LTCC to measure input impedance and provide real-time feedback.
4. **Implementation of Adaptive Matching**
    - Demonstrate automatic reconfiguration of the amplifier’s input matching using MEMS DMTL tuning.

5. **Experimental Validation**
    - Fabricate and characterize the integrated system, verifying performance improvements in terms of gain, matching, and reconfigurability.

0.4 Thesis organization

The thesis format is organized as a paper-based thesis that includes four papers which address different aspects of MEMS and LTCC integration and the final goal of the thesis to implement the FPMA using monolithic LTCC-MEMS process. there are six chapters including the literature survey, four published/submitted papers following the conclusion of the thesis and are as follows:

- Chapter 1 introduces the background, and related works.
- Chapter 2 presents a paper published in IEEE JMEMS: “A Monolithic LTCC-MEMS Microfabrication Process”
- Chapter 3 presents a paper published in MDPI Micromachines: “Ceramics for Microelectromechanical Systems Applications: A Review”
- Chapter 4 presents a paper published in IEEE SENSORS conference: “Compact LTCC-Integrated Fully Decoupled Biasing for Wireless Sensors”.
- Chapter 5 presents a paper to be submitted to IEEE MTT journal: “Field Programmable Frequency Agile Microwave Amplifier Using LTCC-MEMS Process”.
- Chapter 6 concludes the thesis, summarizing the main contributions and outlining potential directions for future research.

CHAPTER 1

LITERATURE REVIEW

1.1 Introduction

The development of modern microwave systems has increasingly gained weight toward reconfigurability as a requirement for next-generation wireless communication, radar, and sensing systems. Conventional non-reconfigurable wireless systems, while adequate in narrowband applications, are limited when operating in wideband applications or under varying load conditions. To this end, comprehensive research on tunable and reconfigurable subsystems, specially in impedance matching networks and specifically for amplifiers, where performance is highly dependent on load and source conditions has been done.

To illustrate the present work, this chapter illustrates reviews of essential key units and their related context that enable field-programmable microwave amplifiers. Present chapter is organized as follow : (i) reconfigurable Radio Frequency (RF) and microwave system as the big picture to have an understanding as system level overview, (ii) then it is more focused on reconfigurable amplifiers and afterwards (iii) conventional matching techniques for different types of amplifiers are studied and then (iv) the need for a novel technology as Micro Electromechanical Systems (MEMS) and RF-MEMS switches and their role in reconfigurable tuners are explained. (v) RF-MEMS impedance tuners and their different architectures are explained with their advantage and disadvantages to narrow the path for the main goal of this work. (vi) integration between microwave amplifiers and RF-MEMS tuners are explained and based on the shortcomings that exists in the literature, (vii) a functional multi-layer layer substrate as LTCC is introduced to implement the reconfigurable microwave amplifier as a compact monolithically fabricated module.

1.2 Reconfigurable and adaptive microwave systems

In the past decades, reconfigurable microwave systems have gained weight, based on the growing demands for modern wireless communication, radar, and sensing applications. Unlike conventional circuits that are limited to a fixed hardware design, these systems can actively adjust their hardware functionality like: operating frequency range, bandwidth, gain, or linearity—in real time. This flexibility allows them to adapt a variety of applications or any system requirements (Sang et al., 2023). Such adaptability is indeed important for microwave systems that require multi-standard communication, dynamic spectrum access, and cognitive radio, where a single device often must handle several frequency bands efficiently. Among the reconfigurable microwave systems, antennas, filters, phase shifters and most importantly amplifiers are essential units in a front-end receiver or transmitter chain. In order to implement such systems, researchers have explored a variety of techniques and technologies to achieve this level of reconfigurability:

- **Semiconductor switches:** By using PIN diodes, varactors, or FET switches as common RF switches to switch quickly between different bands. Their main drawback is that they consume considerable power and can add unwanted losses and nonlinear effects (Nguyen et al., 2023).

- **Material-based tuning:** taking advantages of materials properties whose dielectric values can change under any voltage biasing, or their shape affect the path of an RF line. Examples include liquid metals, liquid crystals, or phase-change materials (Martin et al., 2002).

- **RF MEMS devices:** MEMS devices and sub-systems are growing in past decades for wireless communication and offer excellent linearity and very low signal loss, which makes them attractive for high-performance microwave systems. On the other hand, the disadvantages are that they still face challenges such as packaging issues and delicacy for harsh environments and are sensitive to mechanical and thermal stresses.

Although in recent years there are huge improvements to address these issues, and they illustrate promising performance (McFeetors & Okoniewski, 2004).

1.2.1 Front-ends amplifier architectures

As it is mentioned in the previous section, an essential part in a front-end receiver or transmitter is microwave amplifiers (Figure 1.1). Two of them that are critical units, are power amplifiers in transmitters and low noise amplifiers in receivers.

- **Power Amplifiers (PAs):** Reconfigurable power amplifiers offer the ability to adapt output power, efficiency, and linearity, all of which are key for supporting high data-rate communication while managing energy consumption. Solutions such as tunable matching networks, implemented with varactors or MEMS switches, have shown strong potential in sustaining optimal performance across wide frequency bands.
- **Low-Noise Amplifiers (LNAs):** LNAs enable multi-band operation, which plays a key role in improving receiver sensitivity within adaptive front-end architecture.

Designs that employ switched transistor arrays, adaptive biasing methods, or MEMS-based impedance tuning have demonstrated strong potential for achieving both frequency agility and flexible gain control. To elaborate more about tuning ability of these devices, first, impedance matching technique is introduced in the next section and then different technologies involved in impedance tuning is explored.

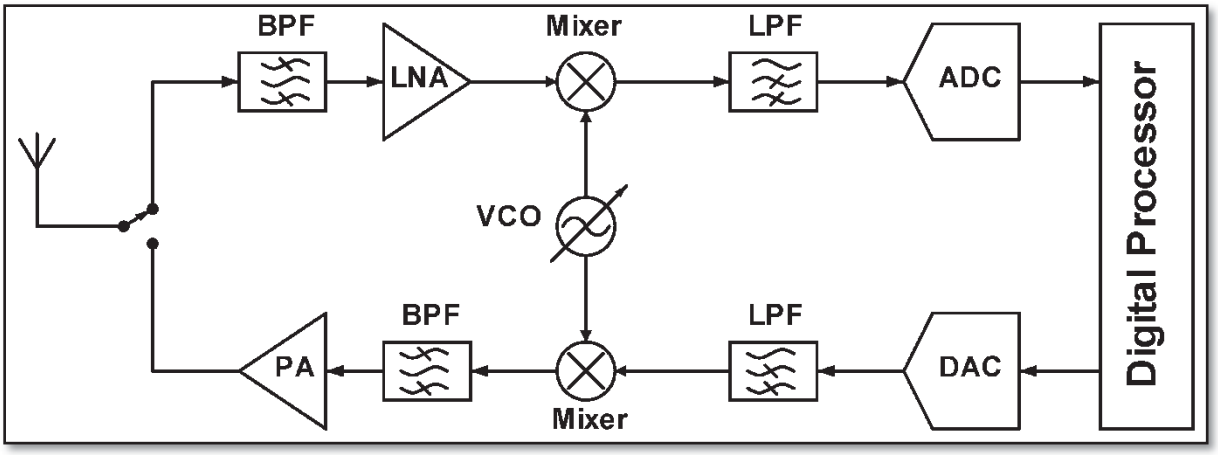

Figure 1.1 RF front-end receiver and transmitter chains
Taken from Michailidis et al. (2025)

1.3 Impedance matching techniques

Impedance matching is an essential technique to deliver maximum power transfer and mitigate losses across a microwave amplifier at a designated frequency. conventional matching techniques rely on lumped-element networks (L, π, or T configurations), which are properly developed for narrowband applications due to their simple structure and implementation (Mingo, Valdovinos, Crespo, Navarro, & Garcia, 2004). However, as operational frequencies increase into the microwave and mmWave domains, wide-band distributed matching circuits such as quarter-wave transformers and stub tuners are often preferred because of their higher power handling and wider matching abilities (Calabrese et al., 2020). To this end and to enable wideband impedance matching, variety of techniques have been proposed and studied in recent years. Multi-section quarter-wave transformers and tapered transmission lines can deliver broadband performance, though they come at the cost of increased physical length. In recent years, artificial intelligence techniques, including genetic algorithms and machine learning, have been introduced to help the design of refined and optimized wideband matching circuits, delivering higher flexibility for systems that must operate across multiple frequency bands. (Monika, Uchariya, Ranjan, & Kumar, 2025).

When both compactness and wideband operation is needed, reconfigurability of matching networks become critical. Utilizing conventional matching circuits like lumped and stub matching if required for wideband, require extensive space which is not suitable for miniaturizing purposes. On the other hand, efficient operation while saving energy for today's wireless systems are essential. To address these issues and prevent configurations that occupy large amounts of space while consuming more power, newly emerge technology like MEMS can play an important role to respond to the requirements. To fulfill this purpose, in the next section, RF-MEMS technology for implementing into the impedance matching circuits are elaborated

1.4 RF-MEMS technology

Most important RF-MEMS devices are MEMS phase shifters, MEMS capacitors and inductors, MEMS filers and especially MEMS switches. There are mainly two different types of RF-MEMS switches that are being used in microwave circuits: (i) Contact and (ii) Capacitive switches. The contact ones are usually acting like an open circuit when the switch is in the up-state, and no actuation voltage is applied. When the actuation voltage is applied, the switch will change position to down-state and acts like a short circuit when metal to metal contact is reached. Ideally, contact switches have very high isolation in the up-state position and have nearly zero insertion loss in the down-state condition. MEMS contact switches usually operate between 1 to 40-GHz applications. They have very high isolation, around -40 dB to -50 dB at lower frequencies and increasing to -30 to -40 dB at 20 GHz and higher. In the down-state position, they have very low insertion loss, around -0.1 to -0.2 dB at 0.1 to 40 GHz. Capacitive switches are usually mounted on a Coplanar Waveguide (CPW) where anchors are placed at ground planes and switch membrane is suspended on top of the signal line with a thin dielectric layer on top of it as capacitance area. When an actuation voltage is applied between the membrane and the ground, switch will drop to down-state and high isolation (more than -20 dB at 10–60 GHz) nearly to infinite will happen in an ideal condition at its resonance frequency and lower values on lower frequencies (Rebeiz & Tan, 2003).

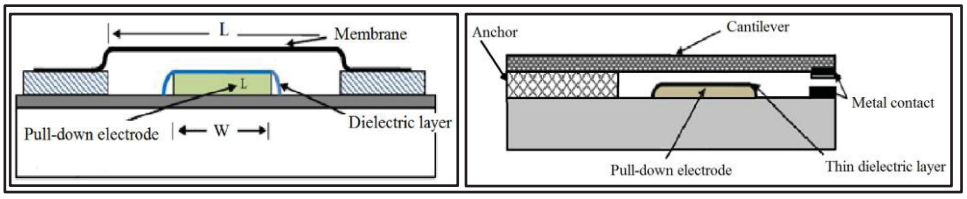

Figure 1.2 Capacitive and contact MEMS switches
Taken from Lysenko et al. (2018)

In up-state, shunt switches usually have very small insertion losses (-0.04 to -0.1 dB at 5–50 GHz). Capacitive switches performance is mostly greater for higher frequencies (5–100 GHz). Also, they may have higher power handling in high power applications like power amplifiers for matching purposes. In Figure 1.2, a MEMS shunt switch and a contact cantilever switch form front view can be seen.

1.5 RF-MEMS impedance tuners

Wide-band matching ability requires components that maintain compact footprints and operate efficiently. Impedance tuners using lumped elements and semiconductor switches usually operates at narrow band applications and as it is mentioned in previous sections, to cover wider bands, substantial space occupation is needed. RF-MEMS impedance tuners on the other hands have the feature to cover a wideband while less space is needed for the entire matching unit. Stub-matching using RF-MEMS contact switches is one of the configurations for such impedance tuners. Although it consumes nearly zero power, still it occupies considerable space. Regarding this issue, Distributed MEMS Transmission Line (DMTL) impedance tuners using capacitive mems switches along a CPW line is developed. Using this MEMS tuner and considering number of the MEMS switches to be N, by enabling $2^{N\ bit}$ combinations on the tuner, a wide range matching area can be achieved. each DMTL tuner dimension comparing to a stub matching tuner is substantial reduced while the coverage and the wideband matching ability is increased. There are several works reporting on DMTL design and their potential to be used for impedance matching in microwave amplifiers are detailed.

Some of the works are focused on increasing bandwidth while others are focused on power handling (Lu, Katehi, & Peroulis, 2005). In (Domingue, Kouki, & Mansour, 2009) a DMTL is connected to a transistor and matching ability is examined from 3.5 to 9 GHz and the tuner is able to reach maximum stable gain in different frequencies in a wide range. All these tuners are fabricated on top of a non-functional substrate like silicon and glass, and further assembly and integration is needed for cascading DMTL units into a microwave amplifier. Post processing fabrications is always complex and costly and may affect performance of the tuner. Consequently, a proper solution is required to respond the mentioned shortcoming. In the following section a solution using a 3D functional ceramic substrate called LTCC is introduced and elaborated.

1.6 LTCC technology and the novelties in integration of MEMS and microwave circuits

Low Temperature Co-Fired Ceramics (LTCC) are a promising platform for the integration of a wide range of MEMS devices, including sensors, microfluidic systems, and switches. Owing to their layer-by-layer fabrication process, LTCC structures can serve multiple roles: as a packaging medium, as a substrate with embedded passive components, or even as standalone miniaturized devices.

When used as a substrate, LTCC produced by conventional methods often requires surface planarization before MEMS processing. The Co-fired LTCC surface typically exhibits high roughness, which must be reduced to the nanometer scale to enable reliable microfabrication. Several studies have addressed this issue, reporting solutions based on chemical–mechanical polishing (CMP). In such approaches, CMP machines equipped with nanometer-sized abrasive slurry not only minimize surface roughness but also improve overall flatness. As a non-functional substrate, LTCC—similar to other ceramic materials, silicon, and glass—can be used directly for surface microfabrication. For instance, RF-MEMS switches have been fabricated on polished LTCC substrates (Buttiglione et al., 2008).

In addition to acting as a passive substrate, LTCC can be designed as a functional platform with embedded metallization for DC or RF routing, cavity formation, and vertical via interconnections. Numerous works report the hybrid integration of MEMS chips with functional LTCC, where chip contact pads are bonded to LTCC vias. A notable advance in this direction is the monolithic LTCC-MEMS process (E. Fallahnia & Kouki, 2023), where MEMS devices and LTCC structures are fabricated simultaneously. This eliminates the need for complex post-processing steps, such as alignment and bonding, which are required in processes like CMOS-MEMS integration. Challenges inherent to LTCC, such as surface roughness and dimensional shrinkage in all three axes, have been addressed through tailored polishing methods and design compensations, enabling misalignments of only a few microns. To validate the feasibility of this approach, a capacitive RF-MEMS switch was successfully fabricated on an LTCC substrate with embedded RF and DC lines. The device demonstrated competitive RF performance comparable to low-loss switches reported in the literature. By exploiting the mentioned monolithic process, it is possible to develop a reconfigurable microwave amplifier in a compact design with a wideband coverage while avowing complexity in the process of fabrication and maintain the performance of the impedance matching units.

1.7 Summary and structure of the thesis

In the literature review section, the importance of reconfigurable microwave units, specially for microwave amplifiers are extensively explored. Conventional technologies in developing reconfigurable amplifiers are explained and solutions using recent technologies to address current issues are reported. As the current thesis is a paper-based thesis structure, the following sections are divided into four papers which addresses different aspects of the technologies and approaches which are used to reach a solution for a full reconfigurable microwave amplifier. In chapter 2, a novel monolithic LTCC-MEMS process is introduced and is published in IEEE JMEMS. this work paves the way for developing a field programmable amplifier using the monolithic process. in chapter 3, is a comprehensive review paper which illustrates a full review on application of MEMS in ceramics and specially LTCC and its potential to develop

functional system and their integration with other active and passive devices be they transistors or sensors. This work is published in MDPI micromachines. In chapter 4, an embedded bias tee which is developed using LTCC as a functional substrate and it can serve as a compact bias tee for MEMS sensors for wireless applications and it is published in IEEE sensors and finally in chapter 5, a field programmable amplifier using monolithic LTCC process is completely implemented and is submitted to IEEE MTT journal.

CHAPTER 2

A MONOLITHIC LTCC-MEMS MICROFABRICATION PROCESS

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Abstract

A novel end-to-end monolithic process for the fabrication and integration of Micro Electromechanical Systems (MEMS) on functional Low Temperature Co-Fired Ceramics (LTCC) substrates is presented. The first phase is a conventional LTCC process that produces a functional multi-layer LTCC substrate that embeds all necessary passives in the inner layers and provides for surface to MEMS and other surface devices through built-in vias. The second phase consists of an adapted MEMS process carried out on top of the fabricated LTCC functional substrate. The adapted MEMS process addresses two main challenges that come with the sintered LTCC substrate: surface roughness and anisotropic shrinkage. A polishing step is introduced to achieve nm-level surface roughness taking into account the monolithic nature of the process where metallic via bumps and the LTCC surface must be polished together. To address the anisotropic shrinking problem, the MEMS lithography masks are adjusted to follow the post-sintered LTCC vias' positions, which are captured by an optical image, thereby achieving perfect alignment. The proposed monolithic process is applicable to arbitrary MEMS devices. It is demonstrated through the design, fabrication and testing of a capacitive RF-MEMS switch. The fabricated device is miniaturized by burying DC and RF lines in the LTCC substrate. Its measured performance is on par with that of similar non-monolithically fabricated switches.

Keywords: Monolithic LTCC-MEMS, functional substrate, integration, LTCC, MEMS, RF-MEMS, microfabrication.

2.1 Introduction

The MEMS technology has been the subject of ongoing research for more than three decades. Over this period, remarkable progress has been achieved covering a wide range of applications including sensors of various types, RF MEMS switches and bio-MEMS devices (Rebeiz & Tan, 2003; Asri, Hasan, Fuaad, Yunos, & Ali, 2021; Akshdeep et al., 2014; Pillai & Li, 2021) . However, in most applications, MEMS devices on their own are not sufficient and they need to be integrated with active and/or passive circuits in order to be usable. To accomplish this, two main approaches for fabricating MEMS circuits in different technologies are usually considered. In the first approach, which has been studied extensively over the past twenty years, fabrication of MEMS devices, be they switches or sensors, is typically carried out on non-functional substrates, i.e., silicon, glass, or quartz (Yan, Liao, Chen, & Li, 2018; Belkadi, Nadaud, Hallepee, Passerieux, & Blondy, 2020; Benoit, Rudy, Pulskamp, & Polcawich, 2020; Demirel, Yazgan, Ş, & Akın, 2016). Depending on the target application, these devices may need to be subsequently integrated or packaged onto a functional substrate. In the second approach, the MEMS devices can be post-fabricated and/or post-integrated on functional substrates that incorporate analog and/or digital functional circuitry (Laakso et al., 2018; Meng, Douglas, & Dasgupta, 2016). MEMS on CMOS is one of the more popular examples of such an approach where MEMS devices and CMOS ICs can be integrated together through different options, namely: (i) separate fabrication followed by post process integration like flip-chip, wire bonding, substrate transfer or other bonding technologies (Hayasaka et al., 2015; Q. X. Zhang et al., 2008), (ii) a monolithic simultaneous co-fabrication (Christoph et al., 2021; Valle, Fernández, Madrenas, & Barrachina, 2017; M. H. Li, Chen, Li, Chin, & Li, 2015) , or (iii) a monolithic sequential co-fabrication (Ghosh & Bayoumi, 2005). While the first option avoids any interference between the two processes, MEMS and CMOS, the final integration step can be complex, costly and technically challenging (Du et al., 2016) and may suffer from performance degradation in case of wire bonding (Hu et al., 2017; Carrasco, Barba, Reig, Dieppedale, & Encinar, 2012a). The second option offers advantages in terms of cost and noise reduction during the process, denser integration and less performance degradation of the whole system (H. Y. Chen, S. S. Li, & M. H. Li, 2021; Colon-Berrios, Edrees, Godoy, Kinget, &

Kymissis, 2017). However, it has some challenges given that the high temperature used during the CMOS process may lead to adverse effects, like thermal and mechanical stresses on some materials including metals like aluminum and gold. In this case, polysilicon material is substituted with some metals that are more compatible with high temperature (Pinto, Gund, Dias, Nagaraja, & Vinayakumar, 2022). In the third option, MEMS devices can be implemented after CMOS fabrication both with surface microfabrication or bulk fabrication by etching through the substrate to create MEMS devices. While this option is not sensitive to temperature like the previous one, it may face constraints with some material compatibilities between the CMOS materials and the MEMS process (Pinto et al., 2022). Irrespective of the process used, the fabricated MEMS device/circuit may still need to be packaged to meet the requirements imposed by the environment in which they are expected to operate. Plastic and silicon-based packages are widely used but are not suitable for operating under harsh mechanical and thermal conditions (P. Zhu et al., 2018; Ferrer et al., 2018). In such cases, the use of ceramics (Vaed et al., 2004) provides a good packaging option given that they offer more stability in harsh conditions (Choe, Tanaka, & Esashi, 2007). Low Temperature Co-Fired Ceramics (LTCC) is the main technology used in this area as it offers a 3D multilayer technology. Each LTCC layer starts a green sheet, made of a mix of glass, ceramic and chemical solvent, that can be processed individually with arbitrary metallized vias, cavities and printed lines. Multiple such sheets are then laminated together and co-fired at 850 ∼ 950 ◦C to ensure metals such as silver and gold do not melt. The Coefficient of Thermal Expansion (CTE) of typical LTCC materials is on the order of 2 to 5 W/m.K, depending on the sheet composition, and is relatively close to that of silicon and glass. This feature makes LTCC a good choice for bonding and assembly with other substrate materials like silicon chips and glass substrates (Vaed et al., 2004). LTCC technology has been successfully applied to the packaging of MOEMS and RF-MEMS as well as silicon photonics circuits and sensors (Z. Wang et al., 2019; Karioja et al., 2014; Mamoru Mohri, Masayoshi Esashi, & Shuji Tanaka, 2014; Yildiz, Matsunaga, & Haga, 2018). However, in all of these cases, the packaging was carried out by assembling the separately fabricated MEMS devices and LTCC package together in a heterogenous process. Direct fabrication of MEMS on LTCC (Lucibello et al., 2016; Cianci et al., 2007) can bypass this heterogeneous assembly step. However, the substrate

used in (Lucibello et al., 2016; Cianci et al., 2007) is non-functional and the MEMS fabrication process used therein is not monolithic. This being the case, issues related to anisotropic shrinkage and simultaneous polishing of surface metal and ceramic were not addressed. On the other hand, the embedding of 3-dimensional microstructures compatible with MEMS processes and suitable for high density integration has been demonstrated (Adibi, Isapour, Niayesh, & Kouki, 2018; Shafique, Steenson, & Robertson, 2015). Similarly, the embedding of a variety of passive elements, cavities, vertical interconnections and antennas is well established (Manzillo et al., 2016). Therefore, a MEMSLTCC co-fabrication process, i.e., monolithic process, can combine the advantages of both technologies to empower highly integrated smart and reconfigurable system-in-package (SiP) applications. In this paper, a novel end-to-end monolithic process for MEMS fabrication on functional LTCC is introduced and details of all its steps are given. In addition to being monolithic, the proposed process includes custom polishing and shrinkage compensation steps and is applicable to the design and fabrication of a variety of MEMS on LTCC devices. To validate the proposed process, the realization of a capacitive RF MEMS switch on a functional LTCC substrate is used as an example. The fabricated switch has RF performance that is on par with other fabrication approaches but with the advantages of being already integrated on a functional substrate that can serve as a package while offering significant size reduction through the integration of buried DC and RF lines. The rest of the paper is organized as follows: Section II presents the details of the proposed process and highlights its two main phases. In section III, the proposed process is applied to the design and fabrication of a RF MEMS capacitive switch while section IV presents the measurement results.

2.2 Proposed monolithic process

2.2.1 Process overview

The monolithic fabrication of MEMS on LTCC requires a holistic design approach whereby the integration of the MEMS devices within a fully functional component or subsystem is taken into account at the start of a two-phase process. In this regard, control circuitry for all MEMS

and active devices, passive interconnects, printed resistors, inductors, capacitors, filters, antennas, internal cavities, etc. are designed and fabricated in the first phase. All these features are limited to buried layers in the LTCC 3D stack. The result of this first phase is a functional 3D substrate without any surface metallization, except for that of vias which connects the top to the inner layers. In the second phase of the two-phase process, the functional LTCC substrate is used to monolithically fabricate MEMS devices and passive interconnects using an adapted lithography process, which must take into account the constraints of the LTCC process.

2.2.2 Phase I: Functional LTCC Substrate

Fabrication Figure 2.1a illustrates the concept of a multilayer functional LTCC substrate incorporating many components in the inner layers while Figure 2.1b shows how MEMS, and other surface mount components, can be integrated on top of it. Almost all LTCC fabrication processes follow the same steps starting with via-punching, conductor via-filling and screen printing of traces on individual layers followed by stacking, laminating, cutting and co-firing. For buried capacitors, high dielectric constant pastes are screen printed while for resistors, resistive pastes are used. In some processes, laser ablation can be used to introduce fine features such as small diameter vias, as small as 25 μm in diameter (Adibi et al., 2018), which is particularly useful for subsequent MEMS fabrication. Laser ablation in combination with carbon fugitive tapes can be used to make arbitrarily-shaped cavities. Additionally, mixed metallization, i.e., silver in the inner layers and gold on the outer ones, can be used to reduce conductor losses while ensuring chemical and environmental stability of exposed metals. By levering all these features, highly functional substrates can be designed using exclusively the inner layers of an LTCC stack, which connect to the top-most layer through metallized vias. Since LTCC stacks are typically fired at 850◦C, the resulting functional substrates are structurally robust and thermally stable. On the other hand, during the co-firing process, LTCC stacks will exhibit some level of shrinkage, which must be taken into account during the MEMS fabrication phase to ensure proper alignment. Additionally, the surface finish of fabricated

LTCC substrates is usually quite rough and can also be wavy. As such, it is not suitable in its raw state for MEMS fabrication and must first be properly treated.

2.2.3 Phase II: Adapted MEMS on LTCC Process

Unlike other MEMS processes where the surface finish is not an issue, including silicon wafer and glass substrates, the surface finish of functional LTCC substrates must first be improved before the MEMS fabrication process can be started. There are several works in the literature that address polishing of functional (Mamoru Mohri et al., 2014; Yildiz et al., 2018) and non-functional (Cianci et al., 2007) LTCC substrates. Both (Mamoru Mohri et al., 2014; Yildiz et al., 2018) perform polishing for anodic bonding of LTCC to SOI-based MEMS devices and neither provide details of the polishing process or materials used. Similarly, no usable polishing process and materials were detailed in (Cianci et al., 2007) nor was any mention given on how the polishing would have to be adjusted in the case of functional LTCC substrates.

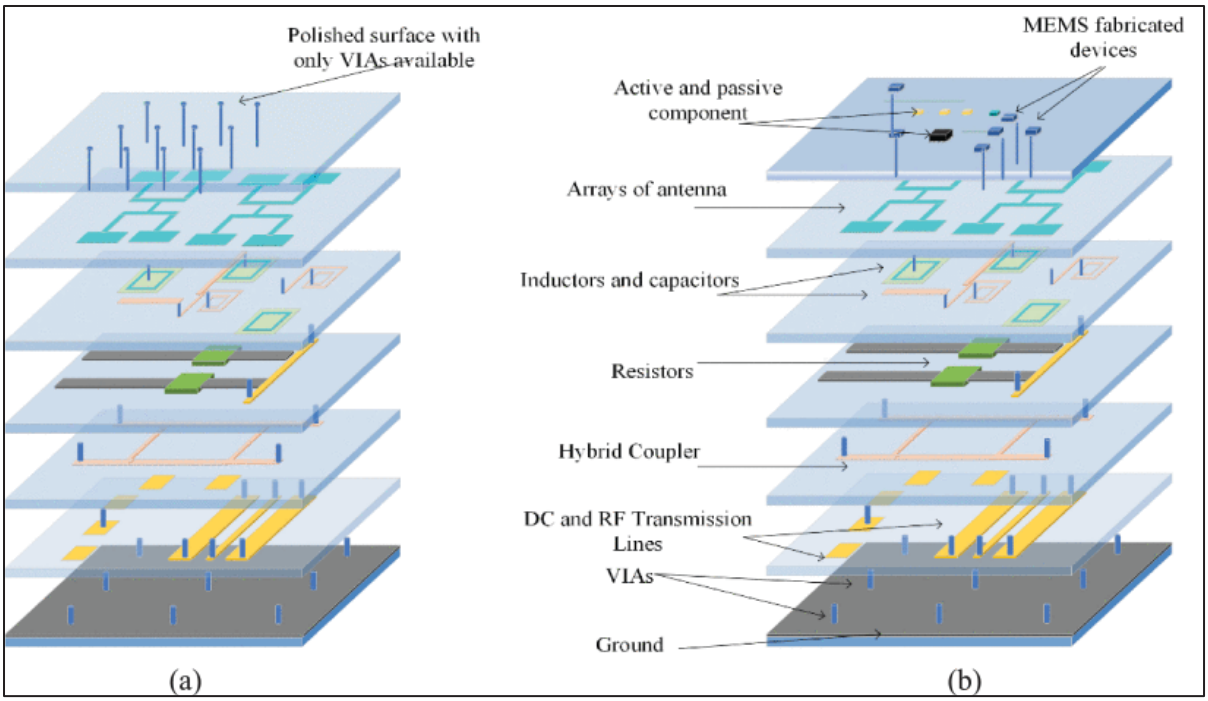

Figure 2.1 Functional LTCC substrates embedded with different components; (a) polished with only vias available for MEMS fabrication (b) anticipated final circuit with MEMS devices, active and passive components on the surface

In (Bartsch et al., 2019) Boron Carbide (B4C) and diamond is used to polish LTCC in a first step. Then, a layer of AlN is deposited. Afterwards, polishing is continued with colloidal silica to further reduce the roughness. Such a process yields good surface finish. However, the AlN layer blocks access from surface vias to inner layers in case of functional substrates, such as in the proposed monolithic process. In (Schmid & Grosser, 2009) , polishing is carried out with Al2O3 slurry and continued with diamond slurry to reduce the roughness to nm level. It is not clear, however, how the processes in(Bartsch et al., 2019) and (Schmid & Grosser, 2009) would apply to functional substrates where waviness due to buried metals and the presence of surface metallization due to surface vias must be considered. In order to achieve a nm-level surface finish of the sintered functional LTCC substrate suitable for MEMS fabrication in a repeatable and reproducible manner, we use a Chemical Mechanical Polishing (CMP) machine and a precise combination of polishing pad, slurries and speed settings. We start by carrying out a preliminary polishing step with a urethane rotating polishing pad, a 1-µm diamond slurry at a speed of 100 RPM for 3 hours. This removes the waviness of the sintered LTCC as well

as the metallic via bumps and reduces the overall surface roughness from few microns down to tens of nanometers. The sample is rinsed and inspected under a confocal microscope to confirm that the surface finish is consistent with the expected values of the preliminary polish. Next, a precision felt polishing pad with a 40-nm colloidal slurry are used for one hour at the same RPM to complete the polishing. Afterwards, the polished sample is carefully rinsed with DI water and then placed in an ultrasonic bath to completely remove all residual slurry from the surface. Then, the sample is heated on a hotplate. This produces the desired final surface finish, and the sample is ready for the MEMS process. It should be mentioned that the size of the wafer in this process is limited only by the size of wafer holder, up to 6 inches on our CMP machine. Furthermore, the polishing uniformity is the same throughout the polished area, allowing the fabrication of MEMS devices to be anywhere on the surface. Batch fabrication is possible as long as the sintering conditions are kept the same. It is worth mentioning that polishing of samples with buried cavities and empty vias for microfluidic applications may be feasible, depending on the size of the access vias' walls and cavity thickness, though we have not attempted this in our work. Further in-depth investigation of this aspect is warranted and must consider all aspects of the process like pressure on the polishing pad, type of slurry, speed of rotation, and other parameters, in addition to the aforementioned characteristics of the cavities/vias. Figure 2.2a shows the surface finish of the sintered entire LTCC sample before polishing while Figure 2.2b shows the same sample after polishing. Figure 2.2c and Figure 2.2d show zoomed views of parts of these same samples before and after polishing, respectively, at 20X and 50X magnifications. The LTCC tile used throughout this work is made of 7 layers of 10-mil Dupont 951 green tape. The roughness is measured with a 3D confocal microscope (Figure 2.2 c,d) and an atomic force microscopy (AFM) system (Figure 2.2 e,f). Having addressed the roughness issue, the next step that requires adapting in the MEMS process is related to the anisotropic shrinkage of the functional LTCC substrate that occurs during free sintering. Figure 2.3 shows the LTCC tile before and after sintering. The overall dimensions shrink from (x: 47 mm, y: 47mm, z: 1.7mm) to (x: 41 mm, y: 41mm, z: 1.48mm). The anisotropic nature of the shrinkage can be seen by zooming on vias. Fig. 4 shows a zoomed view on a section of the tile that contains multiple Vias. In Figure 2.4a, a 2.5 × 2.5 mm2 portion of the stacked tile before sintering is shown where via positions are based on the original

fabrication masks. Figure 2.4b, shows the same portion of the tile after sintering and polishing. Table 2.1 Shrinkage Ratio Before and After Sintering and Polishing summarizes various dimensions before and after sintering and gives the corresponding shrinkage ratio. Dimensions are based on the via-to-via center since the catch-pads before polishing may reduce the distances of vias.

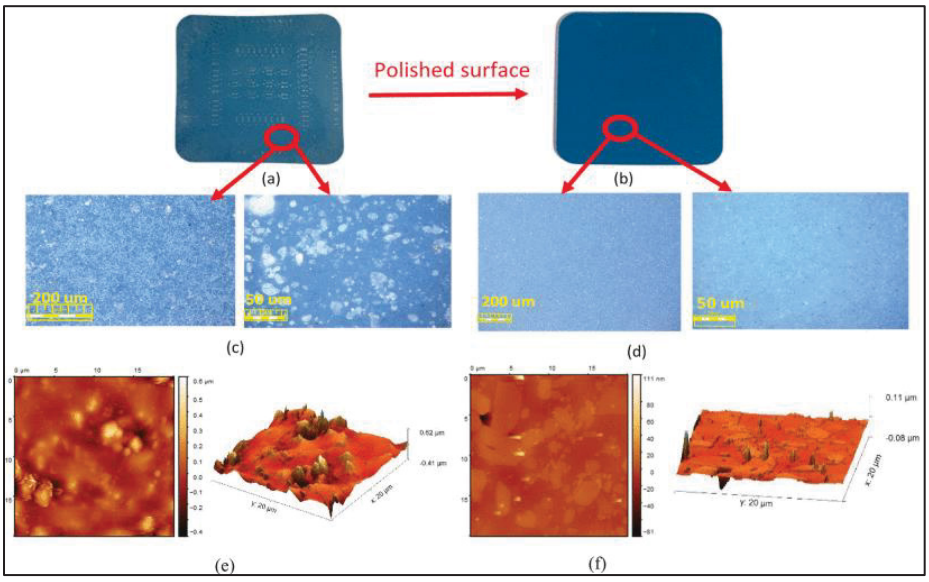

Figure 2.2 Sintered entire LTCC sample (a) before polishing (b) after polishing (c) with zoomed views at 20X and 50X before polishing and (d) with zoomed views at 20X and 50X after polishing. (e) AFM image before Polishing and (f) after polishing

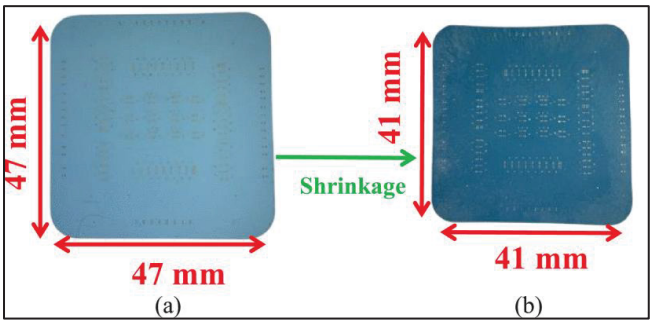

Figure 2.3 LTCC tile dimensions (a) after stacking (b) after sintering

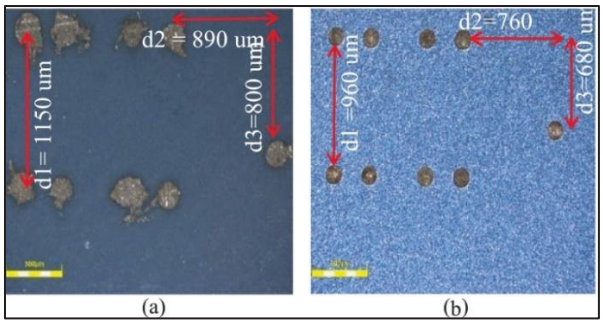

Figure 2.4 Evolution of vias and distances (a) before sintering to (b) sintered and polished substrate

Table 2.1 Shrinkage Ratio Before and After Sintering and Polishing

Dimensions (µm)	**Before sintering (µm)**	**After sintering and polishing (µm)**	**Shrinkage Ratio (%)**
d1	1150	960	16.5
d2	890	760	14.5
d3	800	680	15

Clearly, the anisotropic shrinkage is more pronounced when we consider a larger area. Indeed, as Figure 2.5 shows, the misalignment between the fabricated and initial layout via position is non-constant and shifts in both directions in a non-uniform fashion. Therefore, before proceeding with the MEMS process, this distortion effect must be taken into account and compensated. Two ways of addressing this issue can be found in the open literature. The first seeks to avoid the shrinkage by using a constrained sintering approach, such as pressure-assisted sintering (PAS), pressureless-assisted sintering (PLAS) and Self-Constrained PLAS (SCPLAS) (Needes et al., 2003; Mohanram, Lee, Messing, & Green, 2006; Ihle, Ziesche, Roscher, Capraro, & Partsch, 2013). In addition to requiring specialized equipment, this solution may still yield residual shrinkage above the minimum tolerance required to ensure proper alignment with MEMS masks, which can be as high as 25 µm (Ihle et al., 2013). To

circumvent these limitations while using free sintering, (Lenz, Kappert, Ziesche, Neubert, & Partsch, 2016) proposed a second option consisting of shrinkage prediction modeling through the use of phenomenological modeling and thermomechanical analysis methods for Dupont GT 951. This technique is complex and costly to implement and must be repeated each time the design changes significantly, i.e., layers and metal content. Furthermore, the prediction accuracy is limited and cannot account for any variability in the fabrication process.

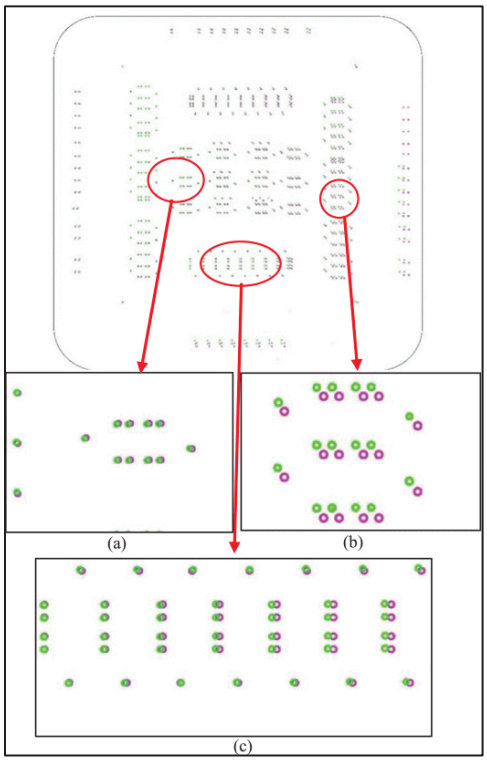

Figure 2.5 Anisotropic nature of the shrinkage in a tile of LTCC in different locations before remapping adjustments (Green Circles represents captured fabricated vias, Purple Circles are initial design layouts). (a) Less than 50 µm via to via Center shift (b) around 120 µm via to via center shift (c) Shrinkage distribution in a part of the sample

Unlike (Needes et al., 2003; Mohanram et al., 2006; Ihle et al., 2013), and (Lenz et al., 2016), here we propose to use a post-sintering shrinkage compensation technique that works with the actual outcome of the sintered functional LTCC substrate. As such, all process variabilities are automatically taken into account. To do this, we capture an image of the surface of the polished substrate with a confocal microscope. The captured image is then converted to a DXF format

file which is then used as a fixed base layer for the MEMS layout. The MEMS layout is then modified to ensure proper alignment with the vias in the base layer. At this point, a typical lithography process based on the new layout of the MEMS circuit can be performed. Figure 2.6 presents a complete block diagram of the proposed monolithic LTCC-MEMS process, clearly identifying the adapted process steps, while Table 2.2 Comparison between other related works with the monolithic process in this paper compares it to related works in literature. The full details of this process are illustrated in the next section where it is applied to an actual sample design.

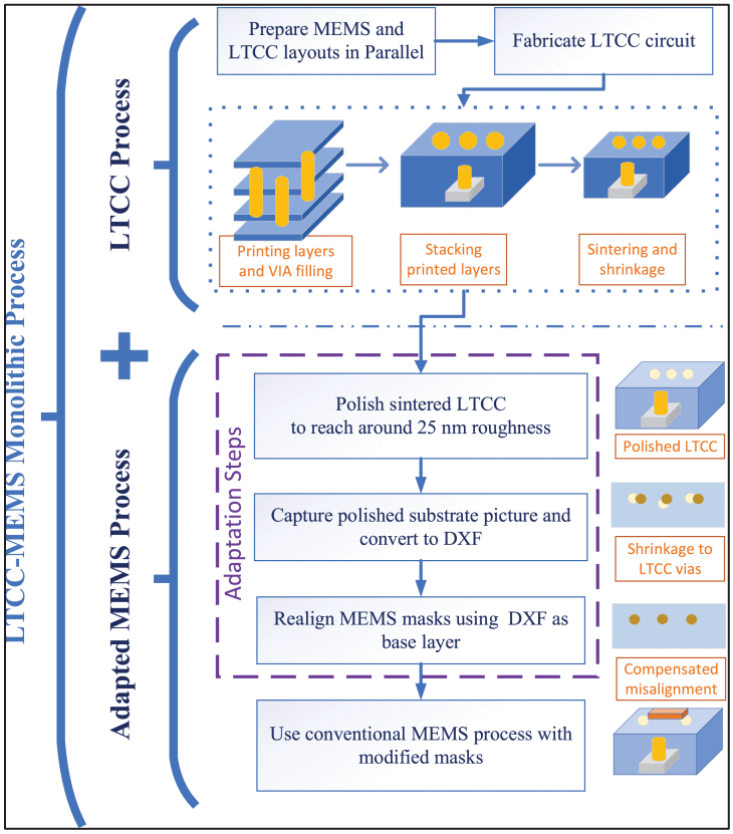

Figure 2.6 Monolithic LTCC-MEMS process block diagram

Table 2.2 Comparison between other related works with the monolithic process in this paper

Related Work	**Process type**	**Functional substrate**	**Monolithic**	**Reproducibility**	**Materials and process for polishing LTCC**	**Sintering shrinkage consideration**
(Lucibello et al., 2016)	MEMS on LTCC	No	No	No	Not mentioned	Not mentioned
(Cianci et al., 2007)	MEMS on LTCC	No	No	Yes (In MEMS process only)	Not mentioned	Not mentioned
(Adibi et al., 2018)	MEMS to LTCC bonding	Yes	No	Yes (For bonding)	Little details (mirror polished)	Not mentioned
(Shafique et al., 2015)	MEMS to LTCC bonding	Yes	No	Yes (For bonding)	No details	No details
(Needes et al., 2003)	LTCC only	Not applicable	Not applicable	Yes (For sintering purpose)	Not applicable	Yes (constrained sintering)
(Mohanram et al., 2006)	LTCC only	Not applicable	Not applicable	Yes (For sintering purpose)	Not applicable	Yes (predictive pre-sintering)
(Bartsch et al., 2019)	LTCC only	No	Not applicable	Yes (For Polishing purposes)	Boron Carbide (B4C) /Diamond Slurry	No
(Schmid & Grosser, 2009)	LTCC only	No	Not applicable	Yes (For polishing purposes)	Al2O3/Diamond Slurry	No
This Work	**MEMS on LTCC**	**Yes**	**Yes**	**Yes**	**Detailed**	**Yes (post-sintering)**

2.3 Application to the design and fabrication of MEMS capacitive switches

In this section, the proposed monolithic LTCC-MEMS process is illustrated through a simple design and fabrication of a capacitive RF-MEMS switch. We start by designing and fabricating the functional 7-layer LTCC substrate using 10-mil sheets of Dupont 951 green tape, which has a dielectric constant of 7.5. Figure 2.7 shows the proposed design whereby the MEMS switch and the surface conductors are to be fabricated monolithically on the polished LTCC surface (denoted as the first layer). The second layer from the top is used for RF ground while the third one is used for DC bias lines. An additional 4 layers are used to provide mechanical robustness and are placed below the others. This design offers two key advantages. First, by routing the DC lines without crossing any RF path we eliminate the need for an additional MEMS process step of surface passivation to isolate the RF and DC lines as commonly done (Rebeiz & Tan, 2003). In addition, the placement of the DC pads can be easily controlled to facilitate integration with other circuit components. Second, by placing the RF ground on the first layer, RF losses can be reduced.

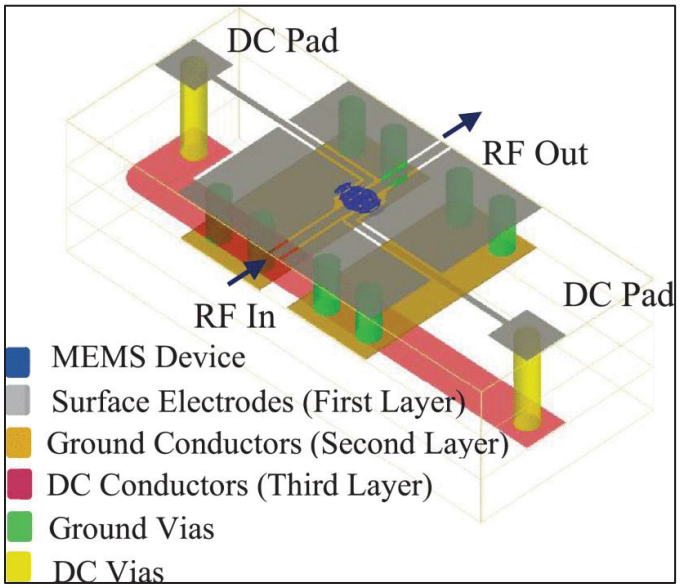

Figure 2.7 3D schematic of functional LTCC substrate with buried layers

The design for a single switch is repeated in layout three times in order to obtain multiple fabricated samples. The switches are fabricated using a standard LTCC process (Manzillo et al., 2016) where vias are first punched and filled with silver paste, then conductor traces are screen printed using silver paste followed by laser ablation to improve the metallization finish. The individual sheets are then stacked, laminated and diced using dedicated machines. The final step consists of sintering the laminated stacks. An X-Ray image of the fabricated substrate is shown in Figure 2.8 where vertical vias and connection to the DC and RF ground are visible. The fabricated LTCC substrate is then polished to a roughness level not exceeding 25 nm in accordance with the first MEMS process adaptation step. To illustrate the importance of the second MEMS process adaptation step, we proceed to fabricate the metallization on the top layer using the original layout, which assumes isotropic shrinkage. Figure 2.9 shows a photograph of one unit-cell where the misalignment of Coplanar Waveguide (CPW) and DC lines with fabricated vias is clearly visible. The figure also illustrates the original positions of the vias, in blue circles, and their positions after fabrication shown by the metallized circles. If the top layer circuit is fabricated using the original masks, i.e., without adjustments, the resulting circuit (CPW and DC lines) will not be functional as the CPW lines is shorted and the DC connection to the inner layer (red line in Figure 2.7) is lost. It should be mentioned that this misalignment is not identical for the other fabricated cells in line with what has been observed in Figure 2.5. For MEMS fabrication, few microns of misalignment are critical and must be considered before starting the process. Therefore, the second MEMS process adaptation step addresses the misalignment issue by adding a procedure for re-generating the MEMS process layers. This is done by (i) capturing an image of the surface of the fabricated LTCC substrate with actual via positions and converting it to a CAD layer, (ii) use the captured layer as a reference for the generation of the new MEMS process masks and apply the necessary rescaling and coordinate adjustment to ensure proper alignment. To this end, in addition to the circuit vias, four additional vias are placed at the substrate's corners to serve as alignment markers during mask regeneration steps. At the end of this procedure, the newly generated masks for the MEMS design are suitable for surface microfabrication on top of the LTCC substrate using the steps outlined in Fig. 10 and detailed in the following. The first step in fabricating the RF-MEMS switch consists of forming the electrodes layer to create the CPW

lines for RF and DC paths as well as the DC pads. To this end, 500 nm of Aluminum is sputtered on the polished LTCC surface, which is then spin-coated by an AZ 5214 positive photoresist. A top etching process is then preformed to pattern the metal layer using a type A aluminum etchant. It should be noted that there is no need to add a passivation layer or any resistive material to insulate the DC bias lines as they are already buried inside the LTCC, thereby eliminating few steps in the fabrication process. In the second step a 150 nm layer of Si3N4 dielectric is deposited using a PECVD process. A lithography process is then applied to pattern the dielectric areas using RIE followed by dipping the circuit in an 1165 remover solution at 80 ◦C for about one hour. Third, another lithography process is used to pattern the switch's anchors and gap between its dielectric and membrane using a 1.5 µm positive AZ photoresist. Steps 4, 5 and 6 in Figure 2.10 are used to create the suspended membrane of the switch. The membrane is made of 2.5 µm-thick aluminum layer sputtered at 3mtorr pressure. To release the membrane, the sample is placed in a 1165 remover solution at 80 ◦ for 40 minutes, to remove top and bottom photoresist layers, and then in a CPD process to complete the release with minimal residual stress. The purpose of this double step release is to prevent the switch stiction to the bottom electrodes. Since the liquid under the membrane in the wet etching process can cause stiction, another process like CPD (as used here) is necessary to guarantee a successful release with no stress. In (Akshdeep et al., 2014) a comparison of different release methods is carried out and the CPD is considered to be the most effective solution for such process. This process does not require any further assembly steps as the MEMS devices is already fabricated directly on the functional LTCC substrate.

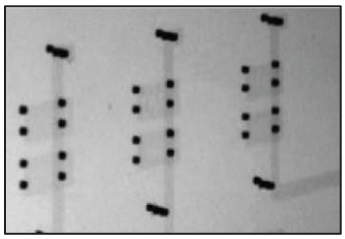

Figure 2.8 X-Ray Image of buried layers and Vias inside LTCC

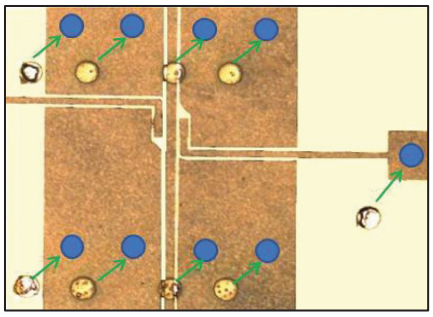

Figure 2.9 Misalignment between LTCC and MEMS fabrication

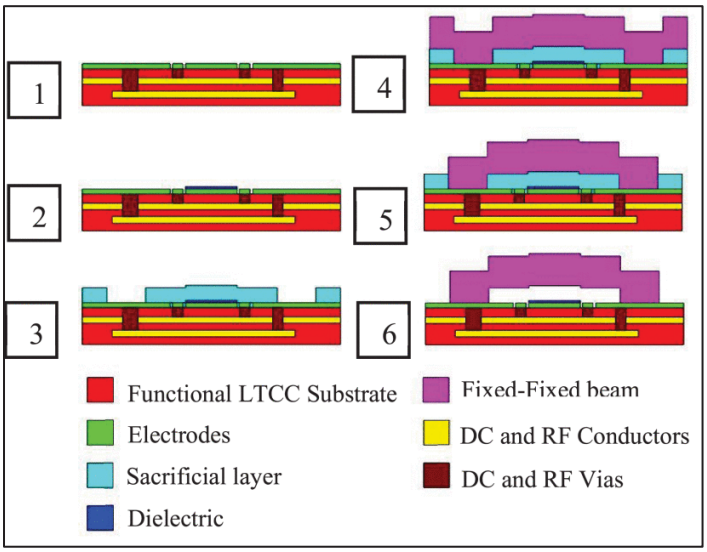

Figure 2.10 Microfabrication process of Capacitive MEMS switch on LTCC

2.4 Result and discussion

Figure 2.11 shows the fabricated switch with detailed views of its geometry. Its overall dimensions are 200 µm × 320 µm with a gap to the CPW line of 1.5 µm. The CPW line width is 100 µm and its gap is 30 µm. The switch's beam is composed of two springs, the quadrants, connecting the circular membrane to the anchors. The arc-shaped holes in the springs help to reduce their stiffness thereby easing the vertical actuation of the switch with lower voltages. The circular shape of the central part of the membrane helps to maximize the achievable capacitance values while the shape of the anchors has been optimized to reduce the actuation voltage and residual stress distribution. The RF performance of the fabricated switch under different bias conditions were measured using a network analyzer (PNA) over the frequency

range of 500 MHz to 20 GHz. The input and output ports were connected to two GSG probes while the DC control was supplied through micro needles connecting the power supply to the surface DC pads. The DC voltage was routed through the LTCC inner layers as shown in Figure 2.7 to eliminate discontinuities in the RF path. First, we measured the S-parameters under no-bias, i.e., the up-state. The results are given in Figure 2.13 and show that the insertion loss of the switch in up-state is better than 0.6 dB at 20 GHz despite all discontinuities and vertical transitions inside the LTCC substrate.

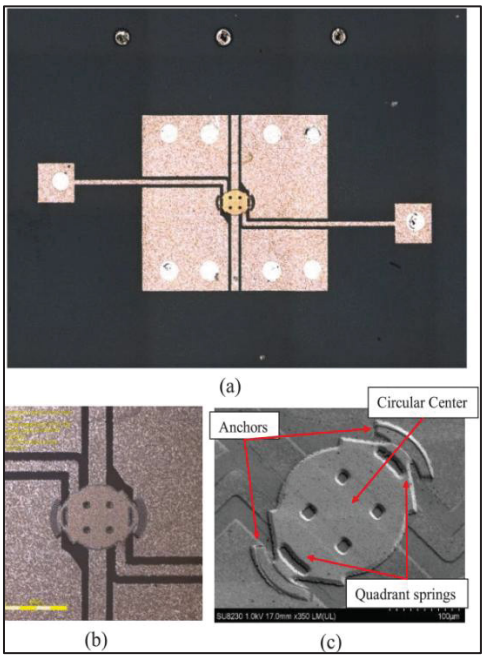

Figure 2.11 (a) Full View of the Fabricated MEMS device on top of LTCC substrate (b) Zoomed view of the capacitive switch (c) SEM image of the switch

Also, the return loss is better than 20 dB over the entire band. Next, we increased the bias voltage and noticed that the switch's response changed abruptly at 28 V, i.e., its pull-in voltage, and stabilized at 40 V, the actuation voltage. Under this condition, the switch is in the down-state, and the resulting S-parameters are also shown in Figure 2.13. To determine the capacitance of the switch in the up and down states, we remove one of the two GSG probes and carry out one-port measurements over the entire frequency band.

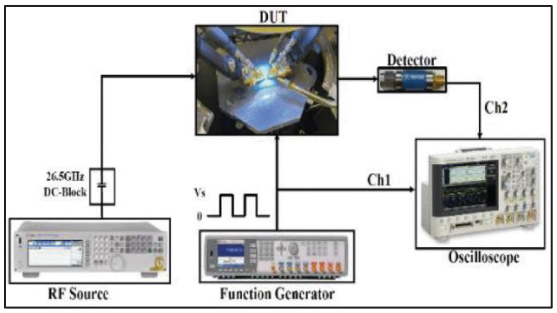

Figure 2.12 Switching time measurement setup

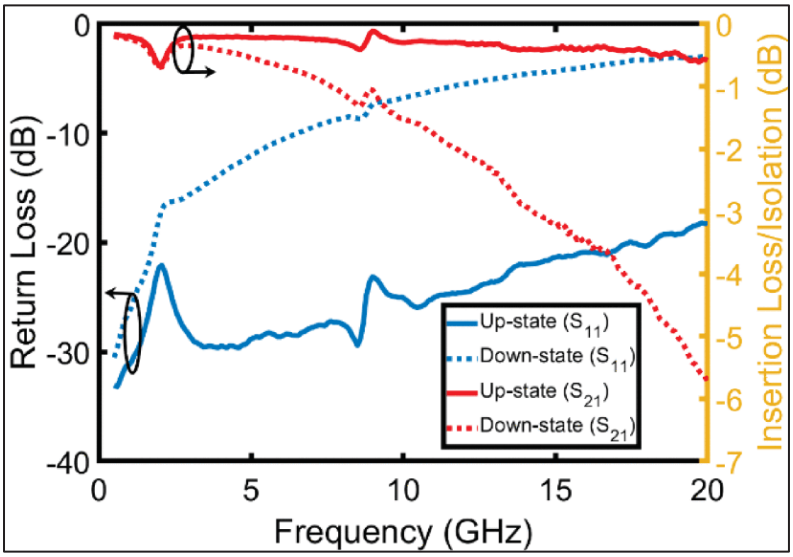

Figure 2.13 Measured S-parameters in the up and down states

. From the resulting S11 measurements, shown in Figure 2.14, select one frequency, 10 GHz, and read-off the corresponding capacitance value for the up and down states. Next, we repeat this operation while varying the bias voltage between 0 and 45 V. The resulting variation of the switch's capacitance versus voltage at 10 GHz is shown in Figure 2.15. This figure clearly illustrates that the pull-in voltage is 28 V, the actuation voltage is 40 V and the release voltage is 15 V while the capacitance increases from 250 fF in the up-state to 0.91 pF in the down state. To measure the switching time, we use the setup of Figure 2.12 where a generator providing 15 dBm at 10 GHz is connected to the switch's input while a power detector is connected to its output. A function generator is used to supply a 1 KHz squared pulse train with maximum amplitude of 40 V for biasing the switch. The output of the power detector and a sample of the

biasing signal are input into a two-channel oscilloscope and both channel voltages are normalized. The resulting measurements are shown in Figure 2.16 where it can be seen that the switching time from the up to down states is approximately 19 µs while it is around 63 µs when switching from the down to up states. Reliability of the switch in this design is enhanced in a way that prevents the stiction problem due to the trapped charging effect on the dielectric area of capacitive switches. This is done by separation of the actuation electrodes from the signal line where the dielectric layer is located as mentioned in literature [1]. In this way, a symmetric dual actuation pads are available at two sides of the membrane, consequently there is no direct bias voltage on the dielectric which prevent the charge trapping and consequently stiction. With such a design, it becomes possible to use materials that have high dielectric constants, for higher capacitance ratios, while tolerating high trap charge densities. All the above measured performance metrics are in line with similar RF MEMS switches in the literature (L. Y. Ma, Soin, Daut, & Hatta, 2019) that have been made using other non-LTCC-based processes.

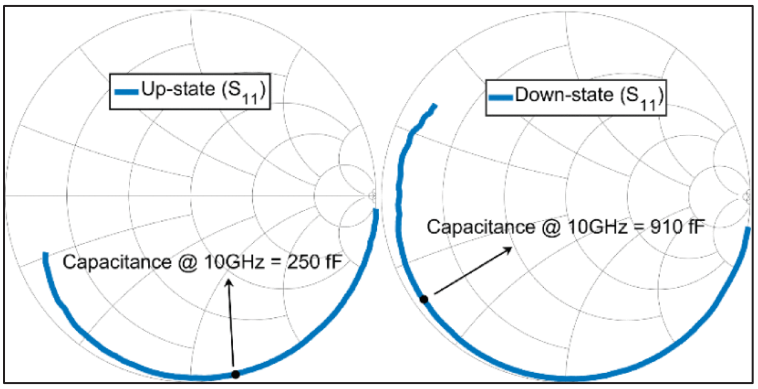

Figure 2.14 Measured Capacitance at 10 GHz in two states

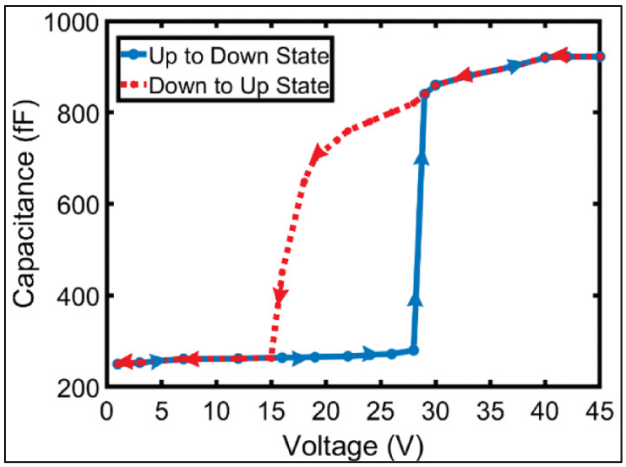

Figure 2.15 C-V curve with varying voltage

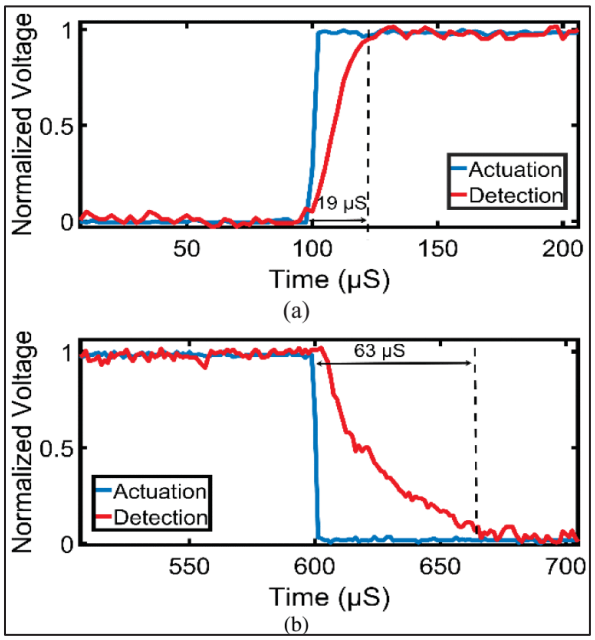

Figure 2.16 Switching Time, (a) Up to down (b) Down to up

2.5 Conclusion

A novel monolithic LTCC-MEMS process is presented in this work. The process leverages LTCC technology to produce highly functional LTCC stacks that are then used as a substrate to monolithically fabricate MEMS devices. In order to accomplish this, two major challenges

were addressed by adapting conventional MEMS process in two ways. First, a polishing step was introduced to ensure that the surface finish of the functional LTCC substrate is well-suited for MEMS fabrication by achieving nm-level surface roughness. Second, a custom mask generation and alignment procedure was introduced to compensate for the anisotropic shrinkage that is inherent to the LTCC fabrication process. The developed process was illustrated through successful design, fabrication and testing of an RF-MEMS capacitive switch. This process can be applied to a wide range of other MEMS devices, including sensors, optical devices, micro-fluidics, etc.

CHAPTER 3

CERAMICS FOR MICROELECTROMECHANICAL SYSTEMS APPLICATIONS: A REVIEW

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Abstract

A comprehensive review of the application of different ceramics for MEMS devices is presented. Main ceramics materials used for MEMS systems and devices including alumina, zirconia, aluminum Nitride, Silicon Nitride, and LTCC are introduced. Conventional and new methods of fabricating each material are explained based on the literature, along with the advantages of the new approaches, mainly additive manufacturing, i.e., 3D-printing technologies. Various manufacturing processes with relevant sub-techniques are detailed and the ones that are more suitable to have an application for MEMS devices are highlighted with their properties. In the main body of this paper, each material with its application for MEMS is categorized and explained. The majority of works are within three main classifications, including the following: (i) using ceramics as a substrate for MEMS devices to be mounted or fabricated on top of it; (ii) ceramics are a part of the materials used for an MEMS device or a monolithic fabrication of MEMS and ceramics; and finally, (iii) using ceramics as packaging solution for MEMS devices. We elaborate on how ceramics may be superior substitutes over other materials when delicate MEMS-based systems need to be assembled or packaged by a simpler fabrication process as well as their advantages when they need to operate in harsh environments.

Keywords: MEMS; ceramics; additive manufacturing; 3D printing; microfabrication

3.1 Introduction

Over the past three decades, tremendous research has been conducted on microelectromechanical systems (MEMS) technology and its potential. MEMS devices, be they sensors, switches, microfluidics, optics, and more, have been extensively studied and applied in different areas of application. Cellular and other wireless connections, medical devices, defense, and space are some prominent areas in which MEMS technology is utilized (Asri et al., 2021; Pillai & Li, 2021; L. Y. Ma et al., 2019; Y. M. Ma, Liu, Liu, Wang, & Zhang, 2024; Shao, Lu, Xiang, Li, & Song, 2024; Abbas, Mansoor, Habib, & Mehmood, 2023; Binali et al., 2024; Gill, Howard, Mazhar, & McKee, 2022; Z. Zhang, Zhang, Hao, & Chang, 2024; You, Wei, Zhang, Yang, & Wang, 2022; Ehsan Fallahnia & Nabavi, 2021). Fabrication of MEMS devices has always carried many challenges and considerations. MEMS devices are usually fabricated using surface microfabrication or bulk fabrication on a polished substrate with a surface roughness around tens of nanometers. These substrates are usually selected depending on the required application and can be categorized as silicon, glass, ceramic, and metals (Kuang et al., 2023; Madhankumar, Sujatha, Sundar, & Viswanadam, 2023; Y. F. Zhang, Cui, & Wu, 2023; Zhou, Wu, Pang, & Su, 2023). They may be used as a functional or non-functional substrate. Over the past two decades, extensive work has been conducted on the fabrication of MEMS devices on non-functional substrates. On the other hand, to benefit from all the potentials of the MEMS devices, they need to be integrated/mounted with other circuits and sub-systems. To realize this goal, functional substrates from different materials and fabrication technologies are developed. Depending on the required application, MEMS devices, after or during fabrication, may be integrated or packaged with a suitable process (L. T. Chen, Chang, Chien, Lee, & Shieh, 2023; Maggi et al., 2023; H. Xu et al., 2023; Y. Y. Xu et al., 2023). Most devices for integration or packaging go through the Complementary Metal-Oxide-Semiconductor (CMOS)-MEMS process. In this process, MEMS devices may be integrated with CMOS ICs as active or passive components. This process is mainly categorized in different approaches: (1) MEMS devices and CMOS circuits are fabricated in different processes and then are integrated or packaged together by different techniques like bond wiring, flip-chip, substrate transfer, etc. The main advantage of this type of integration is that

different processes related to MEMS and CMOS do not interfere with each other. However, the final integration as a post-process fabrication may face costly and challenging processes, subsequently affecting the final performance of the whole integrated circuit (Hayasaka et al., 2015; Q. X. Zhang et al., 2008). (2) Integration is conducted in a monolithic process and MEMS and CMOS are fabricated together (Valle et al., 2017; M. H. Li et al., 2015; Hohle et al., 2021; Bhattacharyya & Ghosh, 2008). While this process eliminates the drawbacks of the first approach in terms of degradation of the final devices and creates a more compact and miniaturized device, it still suffers from interference in the fabrication process with different materials. High temperatures during the CMOS process may introduce mechanical and thermal stress and deformation to materials used in the MEMS process (Pinto et al., 2022; Ku et al., 2021; Carrasco, Barba, Reig, Dieppedale, & Encinar, 2012b; H. Y. Chen, S. S. A. Li, & M. H. Li, 2021; Colon-Berrios, Edrees, De Godoy, Kinget, & Kymissis, 2017). Considering some disadvantages related to the mentioned process in MEMS and silicon-based integrations, other works have been reported with different materials and processes for packaging and integration. As it is essential for MEMS devices to be stable and reliable in harsh environments, special packaging and integration are necessary for them to tolerate mechanical, chemical, and thermal stresses and corrosion. There are different types of packaging and integration with materials including metal (M.-L. Wu & Lan, 2021; Barriere et al., 2010) , plastic (Goggin, Wong, Hecht, Fitzgerald, & Schirmer, 2011; Z. J. Wang, Yi, Qin, & Huang, 2021; Zimmerman, Felton, Lacsamana, & Navarro, 2005; Oouchi, 2014; Lou, Li, & Jin, 2006; G. Q. Wu et al., 2018) , glass, and ceramics (Seok, 2022; Schubring & Fujita, 2007; Heck, Arana, Read, & Dory, 2005; Liew et al., 2002) , which MEMS devices may be embedded, fabricated on the surface of, or fabricated monolithically within as 3D-dense structures. Among these materials, ceramics exhibit excellent performance when it comes to harsh environments. Because MEMS devices are so fragile and delicate at high temperatures, in dusty environments, and from corrosive chemicals, different types of ceramics microfabrication as a standalone microdevice or a host for another MEMS device are suitable options. Compared to other materials like metals and plastics, ceramics have some advantages that make them a better option. As reported in (M.-L. Wu & Lan, 2021), for metals, when it comes to hermetic packaging and the bonding process between MEMS and a metal lid or substrate, a mismatch in the Coefficient of Thermal

Expansion (CTE) between silicon-based MEMS devices and metal introduces challenges in bonding through vertical vias. While CTE for metals is in the order of 10 to 20 ppm/°C, different ceramics have lower ranges around 2 to 9 ppm/°C, which is closer to silicon that is 2.6 ppm/°C. There are several works in the literature that illustrate the integration performance of ceramic materials in different conditions (Gomez, Cardoso, Schianti, de Oliveira, & Gongora-Rubio, 2018; C. Li, Tan, Zhang, et al., 2014; Lucibello et al., 2018; M. Mohri, M. Esashi, & S. Tanaka, 2014). Depending on the availability of the fabrication process and requirements, a variety of ceramic substrates and packages are exploited for MEMS applications. Some of the more prominent materials like low-temperature co-fired ceramics (LTCCs), alumina, zirconia, aluminum nitride, and silicon nitride are reported in several works as ceramic substrates and packages. Ceramic substrates are usually compounds of ceramic, glass, and other chemical solvents with different manufacturing processes. In this review paper, five ceramic materials are chosen for review. The selection of these materials is based on their suitability and unique properties in handling high temperature, electrical and mechanical shocks, and easier integration with MEMS devices, and subsequently, other ceramic materials that are less applicable to MEMS are not included in this review paper. In the second section of this paper, these materials are introduced, and their properties are presented in a table. In the third section of this paper, additive manufacturing (AM) technologies and their sub-section techniques are presented, and among them, we focus more on those ceramics that have more applications for MEMS. Indeed, conventional and other deposition methods of fabricating ceramics are included in section three. In section four, each ceramic, based on its application for MEMS devices and circuits, is individually detailed. In most of the works, three different approaches are governed: (i) ceramics as a substrate for MEMS devices to be mounted or fabricated on top of it; (ii) ceramics are used as a part of MEMS devices or fabricated monolithically in a single process with the same process of MEMS fabrication; and (iii) ceramics as a packaging solution for an MEMS-based system or device. All these approaches are also categorized on a table at the end with their examples that are available in the literature.

3.2 Ceramic Materials and Their Properties

Ceramic materials are widely used in industry and are available in the literature. They are fabricated with different technologies and approaches. The main features of devices fabricated fully from ceramics or partly as an essential unit of a device, including electrical, thermal, and mechanical properties, are explained in detail in different works. Their integration with MEMS and other electronic devices may enhance their performance in different conditions. In terms of electrical properties, high breakdown voltages make the fabricated device more reliable with electrical shocks and possible short circuits in any embedded or integrated circuit. In thermal properties, the low CTE of many of the ceramics lets them integrate more easily with silicon-based MEMS devices like sensors and switches. Also, high thermal conductivity enables them to distribute temperature in the whole circuit uniformly with less energy waste and higher performance. In aspect of mechanical properties, ceramic materials exhibit high robustness when confronting mechanical shocks, cracks, and corrosion. Many MEMS devices including micro-heaters, high-temperature sensors, and RF MEMS devices, be they switches, filters, and phase shifters for arrays of antennas, are able to operate with higher performance and lower energy consumption in harsh environments (Cui, Huang, Li, & Meng, 2020; Stegner et al., 2016; H. Wang, Anand, & Liu, 2017; H. R. Wang et al., 2019; S. Wang, Yi, Qin, & Huang, 2019; Zehetner et al., 2016). There are a variety of ceramics that are manufactured in industry. Among them, Alumina, Zirconia, AlN, Si_3N_4, and LTCC, which are the focus of this review paper, are chosen (Table 3.1). These five materials are selected because they are more widely used in the literature, particularly in MEMS technology. Based on this body of literature, these materials showed more suitability for integration with MEMS devices due to their properties. In the following section, each material, in terms of manufacturing, its application and integration with MEMS, and related challenges for them, are explained.

Table 3.1 Frequently used ceramic materials for MEMS and their properties
Taken from Schubring et al, Stanimirovic et al, Kumta. (2007; 2014; 1996)

Properties / **Ceramic Materials**	**Thermal Conductivity ($W \cdot m^{-1} \cdot K^{-1}$)**	**CTE**	**Dielectric Constant**	**Breakdown Voltage (volts/mil)**	**Flexural Strength (MPa)**
Alumina	8–35	6.9–8	8.4–9.9	200–1090	120–400
Zirconia	3	10–11.4	28–33	100–150	710–1470
AlN	150	4.6–5.3	8.6	250–500	310
Si_3N_4	23–54	2.4–3.5	8.3–9.6	400–500	580–1020
LTCC	2–4.6	4.4–7	5.7–7.5	750–900	170–275

3.3 Ceramic Manufacturing Technologies

Ceramics are manufactured with different approaches, and each has its own benefits and challenges. Each fabrication method affects the properties of ceramics. Conventional methods of fabrication of ceramics are injection molding, dry pressing, sol-gel casting, tape casting, and iso-static press. In Figure 3.1 Conventional manufacturing of ceramics from beginning to final product, we can see the flowchart of ceramics formation from start to final product (Y. Lakhdar, C. Tuck, J. Binner, A. Terry, & R. Goodridge, 2021). In the first step, a specific powder, based on the final product, for instance, alumina, is selected, then the powder is mixed with a specific binder in dry form or with certain slurries. In the third step, the mixture is formed into a desired shape which is called green body. Following this step, a pre-consolidation step called brown body is performed. In the fifth step, a sintering process is conducted in a furnace at elevated temperatures (from 800 °C to more than 1000 °C depending on the ceramics type). Shrinkage happens to the ceramics in this step, which is important in the case of MEMS applications and should be controlled and compensated when alignment is needed with MEMS devices. Indeed, in the final step, machining is conducted for the required

dimension and surface finish. Cutting, laser ablation, and polishing are forms of machining. For MEMS applications, polishing is critical to reach a very smooth surface in the range of tens of nanometers. For more advanced technologies and approaches in ceramics manufacturing, AM, also known as 3D-printing technology, is widely reported in the literature. As reported in (Villa, Gianchandani, & Baino, 2024; Mousapour, 2020) , based on the ISO standard classification of AM technologies, there are seven main categories with sub-techniques in parentheses: (1) Vat photopolymerization (Stereolithography Apparatus (SLA), Digital Light Processing (DLP), Liquid Crystal Display (LCD)), (2) sheet lamination (laminated object manufacturing (LOM), ultrasonic additive manufacturing (UAM)), (3) Powder bed fusion (Selective laser sintering (SLS), Selective laser melting (SLM), electron beam melting (EBM), direct metal laser sintering (DMLS)), (4) directed energy deposition (laser-based metal deposition (LBMD), electron beam freeform fabrication (EBF3)), (5) material jetting (continuous stream mode (CS), drop on demand mode (DOD)), (6) binder jetting (BJ), and (7) material extrusion (fused filament fabrication (FFF), fused deposition modeling (FDM), Direct Ink Writing (DIW)). Each of these technologies has different techniques and methods which are suitable for certain applications (Figure 3.2). In recent years, the disadvantages of conventional methods like shrinkage, time-consuming sintering process, and demanding complex ceramic structures and rapid manufacturing, caused the emergence of AM technologies. complicated shapes like light-weighted structures in biomedical, aerospace, and automative applications are realizable through AM technologies (R. Su et al., 2024). On the other hand, it is widely reported that the very high melting point of ceramics is among the challenges when using AM technologies and layer-by-layer manufacturing of ceramics. Due to these challenges, some post-processing technologies are reported in (Dadkhah, Tulliani, Saboori, & Iuliano, 2023; R. Ma, Liu, & Lu, 2024; Abdelkader, Petrik, Nestler, & Fijalkowski, 2024; Ribeiro et al., 2020). In the following sections, the techniques that are most used in manufacturing the five mentioned ceramics and their suitability to be applied in MEMS technology are detailed. In Figure 3.3, all these methods are illustrated (Dong et al., 2022). Indeed, in Figure 3.4 Five different 3D-printing techniques: Digital Light Processing (DLP), material jetting (MJ), Stereolithography (SLA), Fused Deposition Modeling (FDM), Direct Ink Writing (DIW), it is shown that these processes may be manufactured to produce single-

material products or multi-material ones based on the utilization of a combination of materials in a hybrid manufacturing process (H. Chen, Guo, Zhu, & Li, 2022).

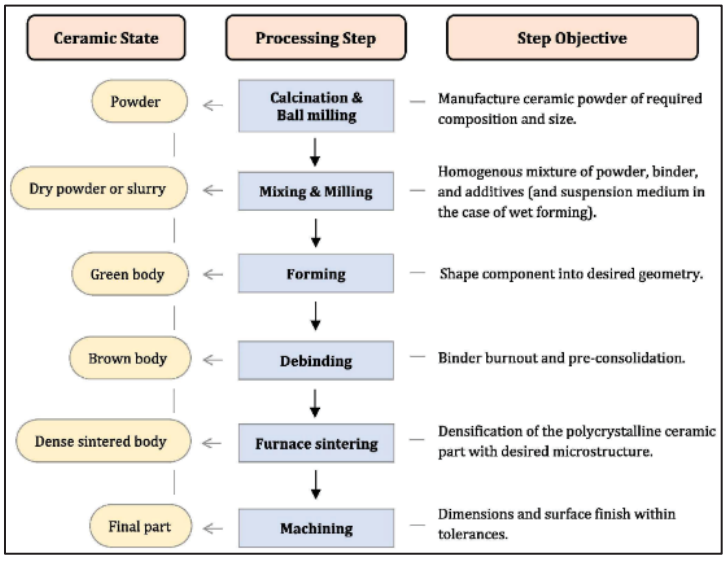

Figure 3.1 Conventional manufacturing of ceramics from beginning to final product
Taken from Lakhdar et al.(2021)

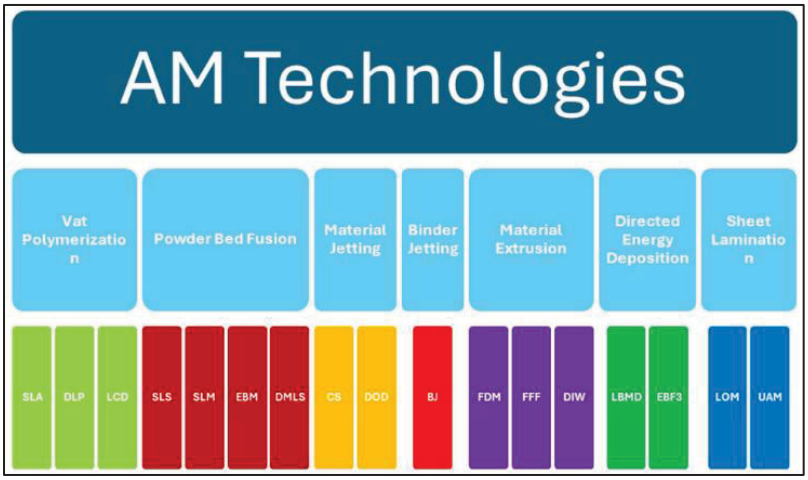

Figure 3.2 Different types of additive manufacturing and their techniques based on ISO classification

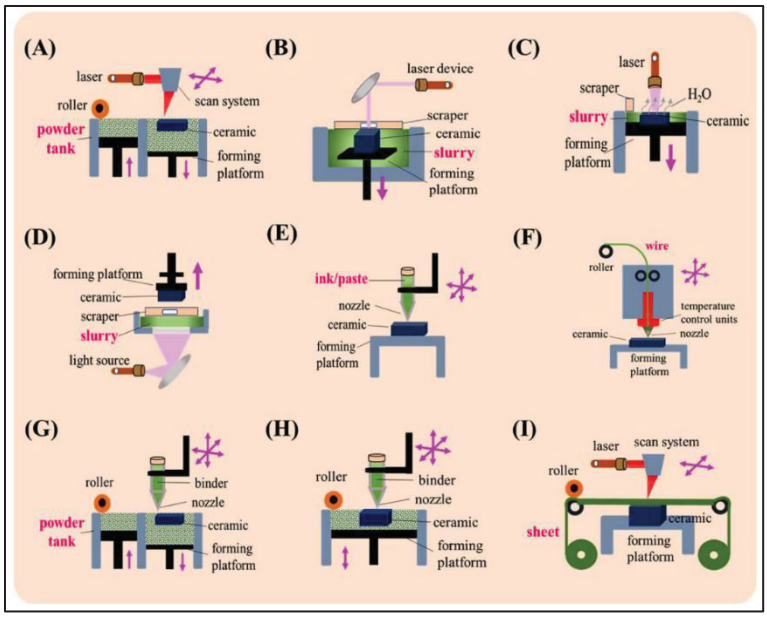

Figure 3.3 AM approaches for Si3N4 manufacturing: (A) SLS/SLM; (B) SLA; (C) LIS; (D) DLP, LCD; (E) DIW; (F) FDM; (G) BJ; (H) 3D printing (3DP); (I) LOM
Taken from Dong et al. (2022)

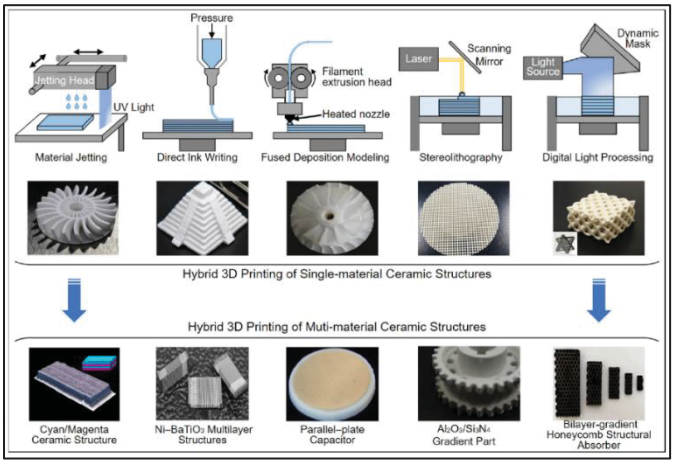

Figure 3.4 Five different 3D-printing techniques: Digital Light Processing (DLP), material jetting (MJ), Stereolithography (SLA), Fused Deposition Modeling (FDM), Direct Ink Writing (DIW)
Taken from H. Chen et al.(2022)

3.3.1 Additive Manufacturing Technologies

In the following section, AM technologies and their sub-techniques that are used most in the literature for five ceramics and their suitability for MEMS applications are presented.

3.3.1.1 Vat Polymerization

In this technique, which is based on a source of light, the light aims at a photopolymer material and makes changes to its properties, like hardening it. Two techniques, including SLA and DLP, are used to manufacture different types of ceramics. In some of the recent advancements in AM of alumina fabrication, for example in (Esteves et al., 2022), the author used Digital Light Processing (DLP) technology to fabricate alumina/calcium phosphate samples with microporous features to apply in lightweight and high-aspect-ratio structures. In this work, a high-quality and lightweight alumina ceramic is produced while the cost of fabrication is kept low. In another work (J. Schlacher et al., 2021), authors introduce a new way of using AM to produce alumina by using a layer-by-layer printing process. Compared to the reference in this paper illustrated to be 650 MPa, they achieved a very high biaxial strength of 1 GPa in fabricating alumina ceramic. In this process, a multi-material approach is used. Layers of alumina and zirconia ceramics are sandwiched together to form a stronger material compared to the fabricated monolithic alumina in another work. In Figure 3.5, two different fabricated ceramics are shown. Stereolithography by applying 3D-printing technology is used to fabricate alumina (H. Li, Elsayed, & Colombo, 2023). As the sintering process is difficult in alumina due to the high melting point, some aiding particles such as TiO_2, $CaCO_3$, and MgO are added to the sintered material. As a result, the flexural strength of fabricated ceramic is increased from 139.2 MPa to 216.7 MPa. Also, the anisotropic shrinkage of the final product is decreased, as shown in Figure 3.6. Like alumina preparation, SLA is used for zirconia in (Pchelintsev et al., 2023). For Zirconia, parameters like raw materials, slurry, debinding, and sintering in these processes all affect the final product. Aluminum Nitride plays an important role in many applications and is well-reported. Optoelectronics, MEMS, and packaging

electronic devices, especially for wireless communication (e.g., piezoelectric materials) are other important areas where AlN is used. As mentioned in earlier sections, AM technologies are applied to enhance the properties of AlN ceramics. For instance, in (Y. X. Tang, Z. H. Xue, G. H. Zhou, & S. Hu, 2024), Digital Light Processing is used to fabricate AlN with high thermal conductivity and density. In this process, the pressure of nitrogen gas and sintering temperature in the process are key factors to produce AlN with high quality. The optimum sintering temperature is determined to be 1720 °C while nitrogen gas pressure is kept below 1 MPa (around 0.6 MPa). The final AlN ceramic has a thermal conductivity of 168 $W \cdot m^{-1} \cdot K^{-1}$ and a density of 3.35 g/cm^3. A simple process is illustrated in Figure 3.7.

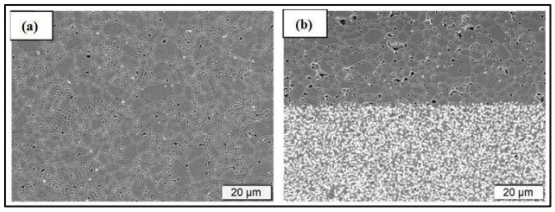

Figure 3.5 Microstructure of (a) monolithic (b) multi-structure of fabrication
Taken from Josef Schlacher et al. (2021)

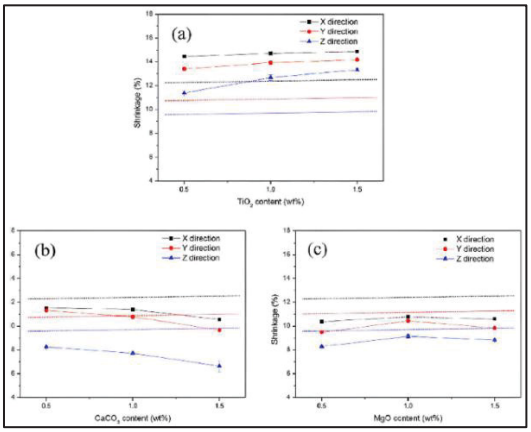

Figure 3.6 Shrinkage rate of the sintered ceramic with different sintering materials content, (a) (TiO2) on top, (b) (CaCO3) on left and (c) (MgO) on right in all direction (X direction in black, Y direction in red and Z direction in blue), direct lines indicate the shrinkage before adding materials
Taken from H. Li et al.(2023)

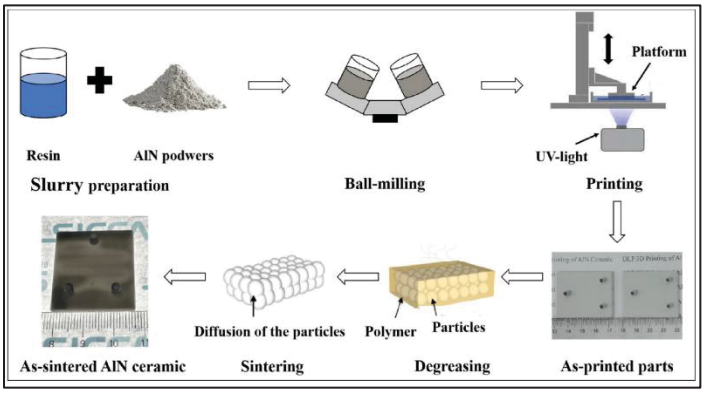

Figure 3.7 DLP technique for AlN 3D manufacturing
Taken from Y.Tang et al.(2024)

3.3.1.2 Powder Bed Fusion

In powder bed fusion, a source of laser melts ceramic powders and forms a solid material. In (S. Chen et al., 2022), the author applied laser powder bed fusion to fabricate alumina ceramics with a very low shrinkage rate with adequate strength, which may be suitable for MEMS that need precise alignment. More efforts are also reported in (Lomakin et al., 2020; Stoll, Kirstein, & Franke, 2018) , in which the laser-assisted selective and selective laser melting fabrication processes are shown. In these works, a laser is used to form deposited metallization on an alumina substrate to create transmission lines. The first process helps to fabricate the desired metallization on low-loss ceramic substrates like alumina, while the second process helps to fabricate 3D metallization with good adhesion of metal to alumina after heating during the fabrication. Like alumina in the previous section, there are plenty of AM technologies to fabricate zirconia ceramics (G. Y. Su et al., 2023; Yoo, Pang, Kim, & Jung, 2023; Willems et al., 2021). Two important challenges are considered in several works for the manufacturing of zirconia in SLS technology (X. P. Zhang, X. Wu, & J. Shi, 2020; Klocke, Derichs, Ader, & Demmer, 2007; Q. Liu et al., 2015). First, powder characteristics. The density of the powder is directly proportional to the size of the powder bed and the final structure of the zirconia

ceramic, and it could be increased by certain slurry deposition. Indeed, blending the powder with another low melting point solvent may enhance liquid phase sintering and subsequently result in a denser ceramic structure in laser processing. The second parameter is laser parameters. The velocity and power of the laser affect the final manufactured ceramic. As seen in Figure 3.8, laser power and velocity can clearly determine the surface of zirconia ceramic. For MEMS fabrication on a zirconia sample, a denser compound and fewer cracks and holes may help better surface microfabrication that has a direct influence on MEMS device performance. Another technology for zirconia ceramic fabrication is called laser melting and is almost identical to the previous technology, with one exception. This is a one-step process without any post-process like a low melting step. As reported in other works, the disadvantage of this process is the low density of the final ceramic product. To address this issue, a preheating process is supposed to be the most effective way (X. P. Zhang et al., 2020). Illustrations in Figure 3.9 show cracks that are more distributed and decreased when the preheated temperature increases in treating ceramic powder. Moreover, in (K. Zhang, Meng, Qu, & He, 2024), a comprehensive study on defects in ceramics is presented. Challenges and solutions to control defects are extensively studied. Pore, crack, delamination, and surface defects are addressed in this review work.

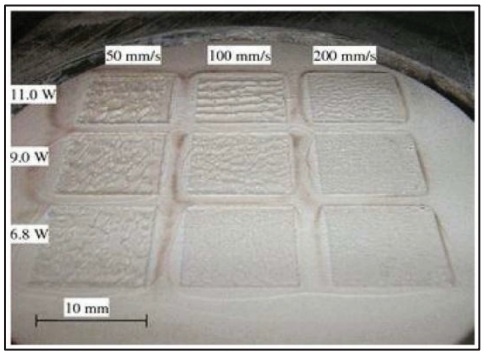

Figure 3.8 Laser power and velocity variation effect on surface morphology of zirconia sample
Taken from X.Zhang et al.(2020)

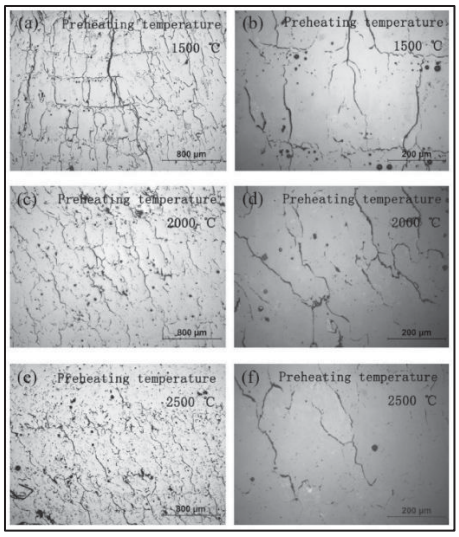

Figure 3.9 Preheat temperature effect on sample cracks
Taken from X.Zhang et al.(2020)

3.3.1.3 Binder and Material Jetting

In material jetting technology, the repeated processes of curing different materials with UV light are performed to create a 3D structure. The advantage of this process over Vat polymerization is that no further post-cure process is needed. Moreover, in binder jetting, layers of ceramic powder are attached to each other with a liquid. Inkjet printing is one of the techniques used in binder jetting that is applied in zirconia fabrication. This is a fast and economic process that makes it one of the most suitable approaches in AM of zirconia ceramics. The process starts with the drawing of the CAD file for 3D printing, then the preparation of the ink, printing, and sintering process. To improve LTCC ceramics properties and accelerate the fabrication process while avoiding complexity, AM, like other ceramic materials, is used in the manufacturing of LTCC. Comparing different methods, as reported in (C. Y. Liang et al., 2023), one of the best technologies to produce LTCC ceramic substrates is material jetting. In this work, LTCC ceramic ink materials and silver inks are jetted by a 3D printer equipped with a piezoelectric nuzzle print. Matching between LTCC material ink solid particles and silver ink is critical in this process and is selected in a way to have a similar

shrinkage rate between ceramic and silver after the sintering process. Indeed, the interaction between ceramic and silver is carefully examined to avoid any significant diffusion of silver into the ceramic (Figure 3.10 and Figure 3.11). Since LTCC ceramic is a suitable candidate to be a substrate or package for silicon-based devices, the ceramic material is chosen in a way to have a close value of CTE to silicon. In this work, this value is close to 4.1 ppm/°C. The final product, which is a metallized LTCC substrate is validated through different simple applications, a flat substrate with metallization and a curve substrate by a curved shape-printing process. A microstrip antenna is fabricated and S-parameters are measured between 9 and 11 GHz. Results are in good correlation with the simulation and gain of the antenna, showing good dielectric properties of the fabricated antenna (Figure 3.12). In the next application, an arc-shaped substrate with metallization is fabricated. The electrical properties and the shape of the LTCC ceramic substrate remained similar to a flat one, even after the sintering process exhibited a successful fabrication (Figure 3.13).

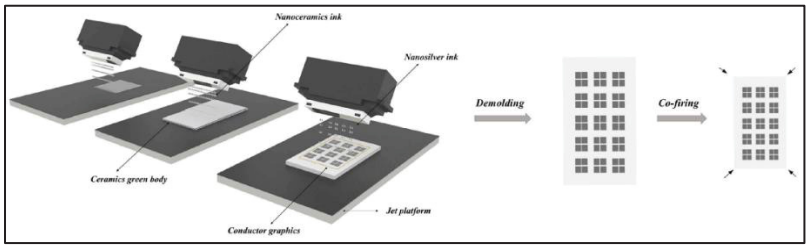

Figure 3.10 LTCC substrate and surface metallization by MJ technique
Taken from C.Liang et al(2023)

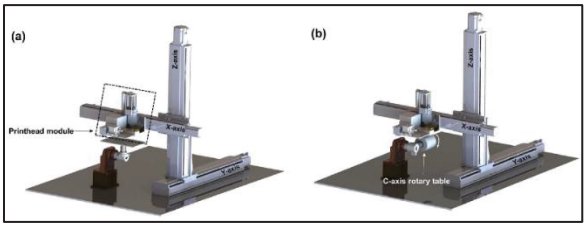

Figure 3.11 Machine for (a) flat and (b) curve printing of LTCC
Taken from C.Liang et al(2023)

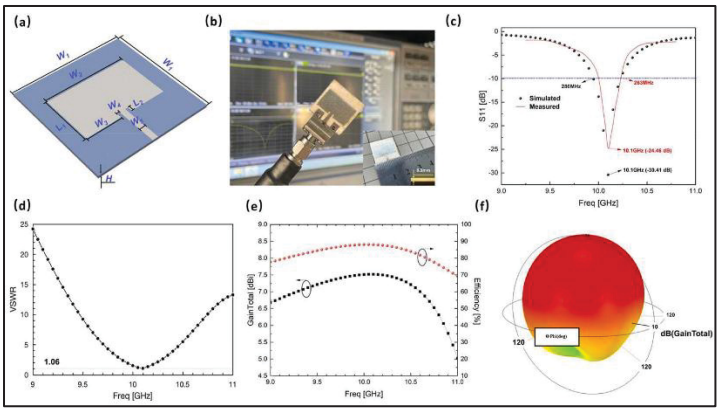

Figure 3.12 Microstrip patch antenna and RF measurements including S11, VSWR, and gain. (a) 3D perspective of the circuit (b) fabricated circuit (c) S11 simulation and measurement (d) VSWR simulation (e) gain and efficiency (f) 3D radiation
Taken from C.Liang et al(2023)

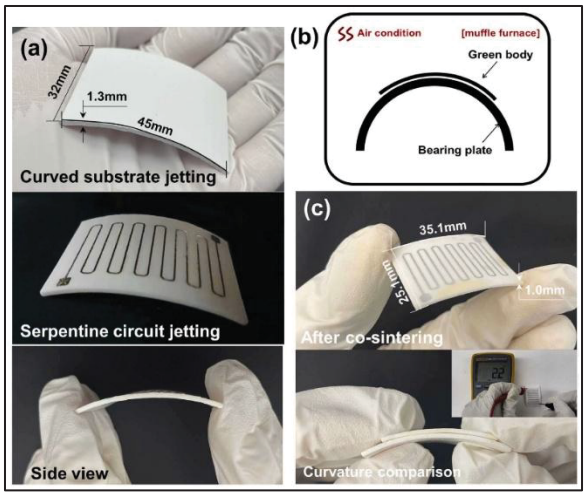

Figure 3.13 Fabricated curve LTCC with metallization on top by MJ technique. (a) fabricated curved LTCC (b) schematic diagram of the curved surface (c) shrinkage circuit after sintering with side views
Taken from C.Liang et al(2023)

3.3.2 Non-Additive Manufacturing Technologies

Apart from the ISO classification of ceramic-manufacturing techniques, there are other methods, including conventional and some specific deposition methods in the literature. In the next sections, these techniques are detailed.

3.3.2.1 Conventional Manufacturing

Conventional fabrication of ceramics commonly follows the same process (Figure 3.1). For instance, green sheets of LTCC that are used to fabricate substrates and packages for electronic and microwave circuits are widely produced through conventional methods. The combination of different types of ceramics and glass powders with certain slurries as solvents is used to prepare sheets. In (Aishwarya et al., 2022), depicted in Figure 3.14, a ceramic material that is used (Cordierite) is prepared by ball milling after calcination at 1350 °C. On the other hand, glass powder is prepared by melting process and then the quenching method. Ceramic and glass are then mixed in a ratio of 30:70 in an IPA solution and dried under an IR lamp. At the end of this step, LTCC powder is prepared. In the next step, to prepare LTCC slurry for tape casting, LTCC powder, as shown in Figure 3.15, is mixed with certain solvents, then, plasticizers and homogenizers with proper binders undergo ball milling for a full 24 h to prepare the final slurry. The prepared slurry is then processed in a tape-casting method, covers a suitable substrate as mylar, and is dried up to prepare the final LTCC green sheets.

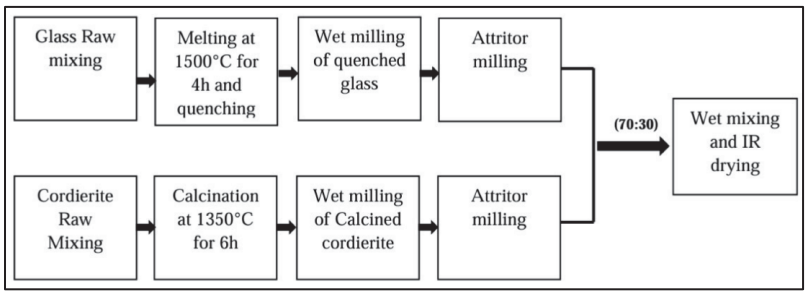

Figure 3.14 LTCC powder-preparation steps
Taken from Aishwarya et al(2022)

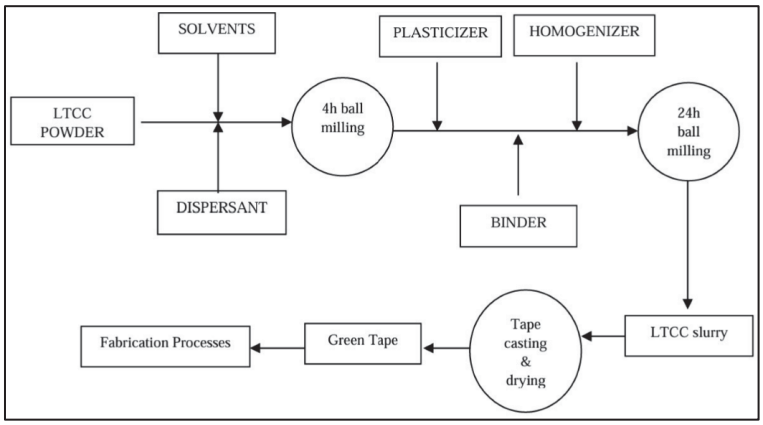

Figure 3.15 LTCC slurry and tape preparation
Taken from Aishwarya et al(2022)

In another work with tape-casting technology, AlN is produced (S. C. Liu, Ye, Liu, Liu, & Li, 2015). During the process, Aluminum dihydrogen phosphate is used to prevent AlN surface particles from hydrolysis. The final product is a well-dense structure with a homogeneous distribution of particles across the ceramic. Flexural strength is 283 MPa and thermal conductivity is around 116 $W \cdot m^{-1} \cdot K^{-1}$.

3.3.2.2 Manufacturing through Deposition Techniques

In addition to the conventional and AM fabrication of AlN, there are other deposition methods used in semiconductor and MEMS fabrication of AlN, Silicon Nitride, alumina, and zirconia. These processes usually take place in cleanrooms where MEMS devices are fabricated. Physical Vapor Deposition (PVD) is a way of creating tens and hundreds of nanometer-thick layers of AlN. DC-reactive sputtering is a kind of PVD that is used to create piezo AlN layers(Shariatdoust & Aghajani, 2018; La Spina, Schellevis, Nenadovic, & Nanver, 2006). Also, chemical vapor deposition is another method and atomic layer deposition is an example of this deposition technique (Alvarez, Spiegelman, Andachi, Kondusamy, & Kim, 2019). These processes also apply to Si_3N_4 ceramics. PVD deposition of Silicon Nitride is reported in(Cotell & Donovan, 1991) , as well as CVD in (Sota et al., 2024; Y. D. Zhang et al., 2021).

Alumina e-beam PVD is also reported in (Y. Zhang et al., 2021). Yttria-stabilized zirconia coatings by PVD are reported to create a dense layer in (L. Gao, Wei, Guo, Gong, & Xu, 2016). In the following section, where the application of ceramics in MEMS devices is studied, more details for final fabricated devices based on mentioned depositions are explained.

3.4 Use of Ceramics in MEMS-Based Systems

The use of ceramics in MEMS-based devices and systems can broadly be classified under three main areas: substrates, monolithic fabrication, and packaging. As non-functional substrates, ceramics, once properly polished, can be used as an alternative to other conventional substrates (silicon, glass, quartz) for MEMS surface microfabrication. In monolithic fabrication, ceramics can be part of an MEMS device (e.g., thin-sputtered layers) or as functional polished substrates on which MEMS devices can be fabricated in a single process. Ceramics can also be used for packaging purposes to cap and seal MEMS devices like sensors and switches. As highlighted before, the ceramics materials that are most frequently used for these applications are alumina, zirconia, AlN, silicon nitride, and LTCC. In the following, we review various applications of each of these materials in MEMS-based systems and provide a comparative summary table (as Table 3.2) between them at the end of this section.

3.4.1 Alumina-Based MEMS Devices and Systems

In the literature, several works are conducted in the MEMS area using alumina ceramics. As a smooth substrate for surface microfabrication, there are many works that use the potential of alumina, like in high-temperature sensors. In (J. Han et al., 2014), they use alumina as a substrate to fabricate a Pt sensor. A fabricated sensor is able to work at elevated temperatures (up to 900 °C) due to the very high melting temperature of alumina (Figure 3.16). In (Sharma, Kaneriya, Patel, Bindal, & Pargaien, 2013), the metallization of the alumina substrate by Cr, Cu, NiP (Nickel-plated), and Au is performed for the purpose of microwave-integrated circuits. Due to the very low dielectric loss of the alumina substrate, microwave circuits can operate

without significant insertion loss. In (Aslani-Amoli et al., 2021), authors demonstrated an ultra-miniaturized microwave circuit using 80 µm thick alumina ribbon as the substrate. Band Pass Filters and Low Pass Filters are fabricated and the top and bottom of the circuit are connected with internal vias through alumina ribbon. Circuit performance at 28 GHz is compared to the other conventional circuits available in the literature and results are promising. Ultra-miniaturized alumina ribbons help fabricate very small MEMS devices like microwave filters and sensors without losing performance. In (Aquino et al., 2022), a Ka-band cavity filter is fabricated with alumina as a dielectric. In this circuit, alumina is produced with AM technology as 3D printing. This design let the first fourth-order prototype with a high-quality factor (800). The return loss of the cavity filter is 13 dB and the insertion loss is 1.3 dB. Narrowing the size of the irises led to this loss. To avoid this problem, another fabrication of alumina with 3D-printing technology is performed, but this time with a higher resolution. Final devices have the potential to be used as a surface mounting unit due to the compact design (14 × 25 mm^2).

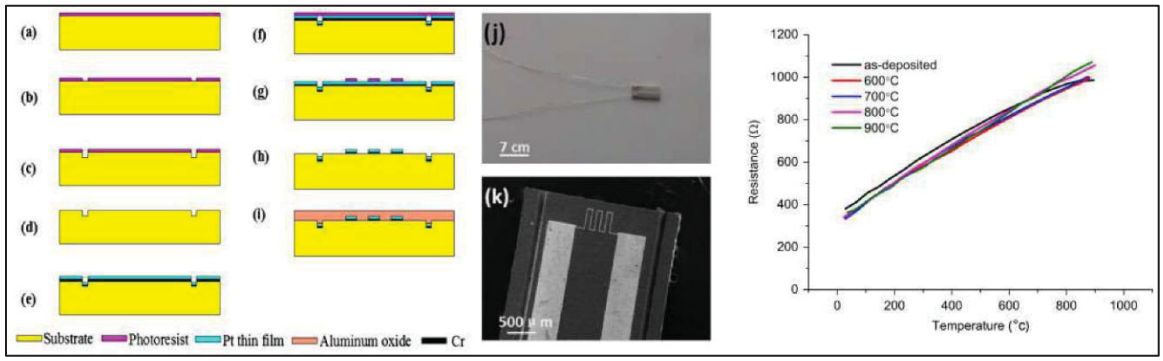

Figure 3.16 (a–i) Fabrication process of Pt film, (j) overall view of the sensor, (k) zoomed view of the sensitive area. Performance of the sensor on the right (resistance variation vs. temperature)
Taken from Jie Han et al.(2014)

In another type of application, alumina can be a part of MEMS device structures instead of being a substrate for another MEMS device. In (Y. S. Lee, J. J. Kim, & K. H. Jeong, 2011), an optical miniaturized device as an anti-reflective structure is fabricated using alumina ceramic. First, an aluminum substrate is machined to form a concave structure. After that, a two-step process of anodic oxidation of alumina is conducted on top of that to create nanopores and

arrays of nanonipples. The performance of the fabricated lens in terms of light transmission is illustrated compared to different sizes of pores and nipples and a normal lens which reflects the enhancement of the fabricated device (Figure 3.17). In another work (Suzuki, Horii, Kasagi, & Matsuda, 2004), a similar process for creating alumina is conducted. Anodic oxidation of aluminum created an alumina porous layer with an integrated ignition heater. The alumina layer is a support layer for the Pt catalyst. The measurement shows a heat release rate of around 830 MW/m^3.

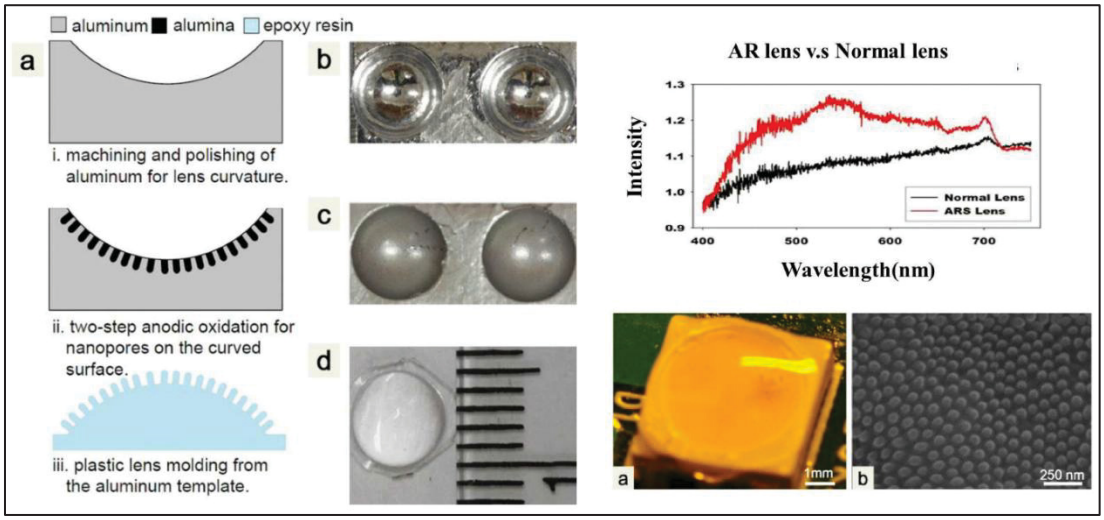

Figure 3.17 Fabrication process of AR lens (a) fabrication steps of AR lens, (b) polished surface of the curved aluminum (c) nanoporous alumina on curved aluminum (d) final optical image of the lens (left), AR lens vs. normal one comparison (top right), (a) AR lens on a yellow light, (b) nanopillars created by anodization of aluminum (bottom right) Taken from Y.S.Lee et al(2011)

In (László, András, Timár-Horváth, Desmulliez, & Dhariwal, 2008) as a sensing purpose, a Relative Humidity (RH) capacitive sensor is fabricated. The sensing layer is a porous alumina layer and the whole process is conducted by a monolithic CMOS-MEMS process. Based on this paper, sensing of the fabricated device is much higher than the average of the literature and is around 15 pF/RH% compared to 0.2–0.5 pF/RH% in other works. In another work for sensing purposes, high-temperature handling of alumina is the main feature of the fabricated sensor. A micro-hotplate is fabricated, which comprises gallium oxide as a sensing layer and an alumina-suspended membrane that is sandwiched between two platinum layers. The

alumina layer, compared to silicon nitride, can handle 650 °C for 110 h, while with silicon nitride, the micro-sensor is damaged within a few seconds. Carbone monoxide and nitrogen dioxide were sensed with the fabricated device under high temperature. The fabricated device under test and its performance are shown in Figure 3.18 (H. I. Jeong, G. Choi, & J. Kim, 2020).

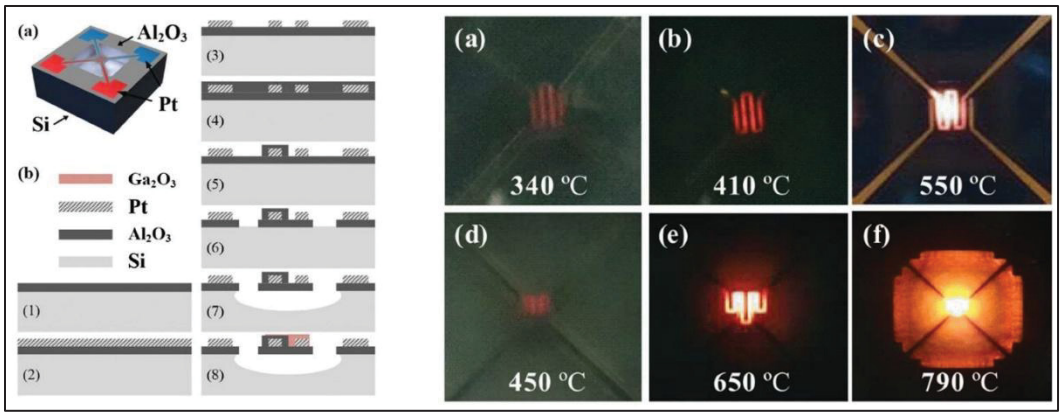

Figure 3.18 Alumina membrane gas sensor fabrication process (left), gas sensor under test in different temperatures (a–c) Si3N4 and (d–f) Al2O3 μHP (right)
Taken from H.I.Jeong(2020)

Finally, when it comes to the packaging of the MEMS devices, alumina can be a suitable candidate. There are several works demonstrating the application of alumina. In (J. Zekry et al., 2011), a wafer-level MEMS fabrication using an alumina nanopore layer is conducted. The alumina layer is around 2 to 3 μm and is sealed with silicon nitride to make the packaging stronger. Pores are 15–20 nm, and they are fabricated with the silicon oxide sacrificial layer and an HF release process. The fabricated RF device as a CPW transmission line is measured with s-parameters and the RF loss due to the package is very negligible up to 67 GHz (Figure 3.19). Another similar work also has been conducted to encapsulate the MEMS device with an anodic process of alumina. The pressure inside the package after the glow discharge due to the high voltage on the MEMS-suspended membrane is measured and is decreased from 50 μtorr to 2 μtorr (V. Maharshi, M. Kumar, A. Agarwal, & B. Mitra, 2023). In (D. Yildirim, G. P. Li, & M. Bachman, 2016), nanopillars of alumina with deep pores around 20–30 μm are

fabricated. the high aspect ratio fabricated alumina pillars can be a good housing for many MEMS devices for packaging purposes under high-temperature environments (Figure 3.20).

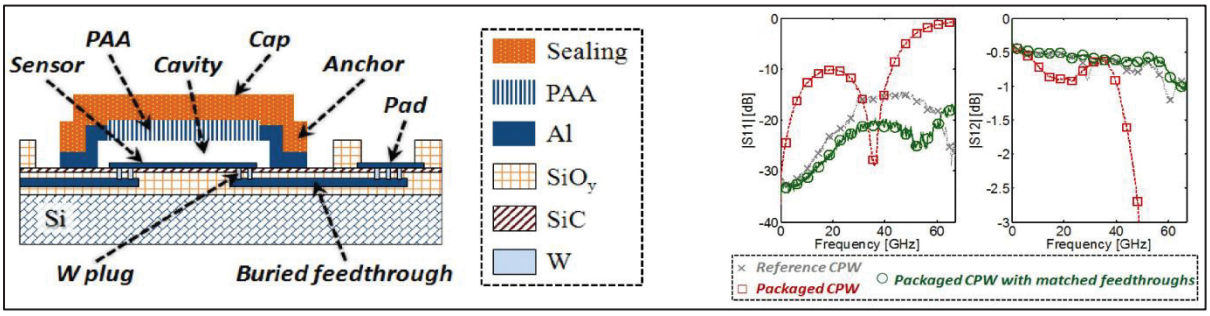

Figure 3.19 Fabricated bridge sealed with Alumina and silicon nitride (left). Measured S-parameters (right)
Taken from J.Zekry et al.(2011)

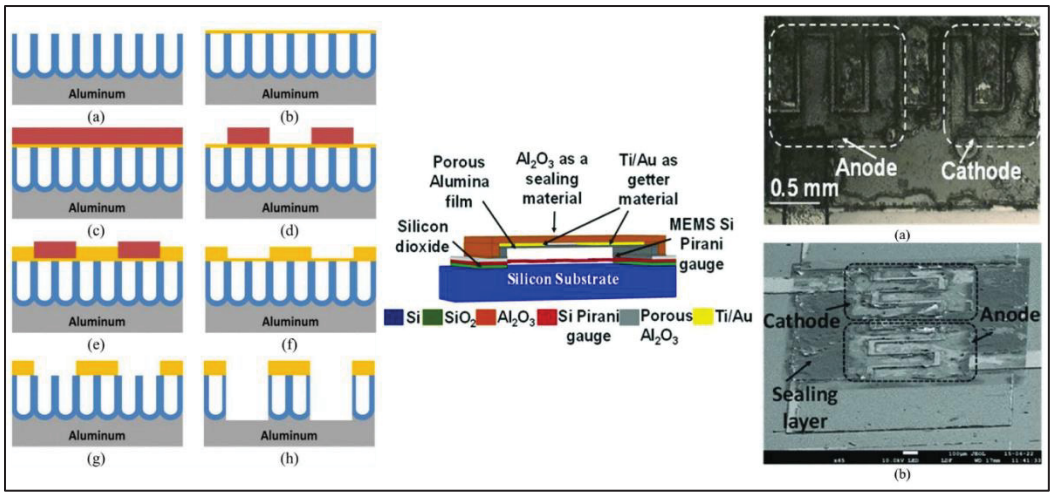

Figure 3.20 Fabricated alumina nanopores with high aspect ratio (a) Two-step anodization process. (b) Cu seed layer deposition process. (c) Photoresist spin coating process. (d) Photolithography and patterning processes. (e) Cu electroplating process. (f) Removal of photoresist. (g) Etching of cu seed layer. (h) Etching of AAO membrane (left). Thin film packaging using glow discharge (center) and fabricated view from top illustrating anode and cathode metals (a) top view (b) SEM image (right)
Taken from V.Maharshi et al, D.Yildirim et al.(2023; 2016)

3.4.2 Zirconia-Based MEMS Devices and Systems

Zirconia ceramic materials are used in several works involving MEMS structures, as a substrate, MEMS device, and packaging solutions. As a substrate, in (Oblov et al., 2015) a zirconium oxide membrane is fabricated for sensing purposes. The membrane is fabricated using slip casting under mechanical pressure and annealing process. Particle sizes of fabricated membranes are around 20 nm. The sintering process is also reported to be 1150 °C. The fabricated membrane is about 10 μm thick and the roughness is appropriate for the deposition of sensing the platinum layer. The application of zirconium oxide is due to its low CTE, which is about 2.5 $W \cdot m^{-1} \cdot K^{-1}$. This makes the sensor consume less power compared to an alumina membrane. The fabricated sensor is suitable for combustible gases and gas-fire detections. In another study (R. Zeiser et al., 2015), different substrates are used for an MEMS pressure sensor to analyze the effect of each substrate. Different ceramic substrates including AlN, Si_3N_4, Zirconia-silicate, and LTCC are used. Among them, LTCC and zirconia-silicate exhibit better performance in terms of mechanical and thermal stress reduction and cross-sensitivity enhancement, which totally increases the reliability of the MEMS device (Figure 3.21). As a flexible substrate, Yttria-Stabilized Zirconia (YSZ) is used to fabricate thin-film solar cells. The surface of the substrate is smooth, and the roughness (20 nm) does not need any modification like polishing. Copper indium gallium diselenide (CIGS) is deposited on top of the YSZ substrate. A 3000-angstrom molybdenum layer was deposited on the back of the substrate. Then, a 120-angstrom-thick layer of sodium fluoride is evaporated on top. Then on top of that, a 2 μm-thick CIGS layer is evaporated. The fabricated flexible device is illustrated in Figure 3.22. As reported in this paper, this device may open the door to fabricating many flexible MEMS devices, like high-temperature sensors that are able to work in high temperatures (D. Fobare et al., 2014).

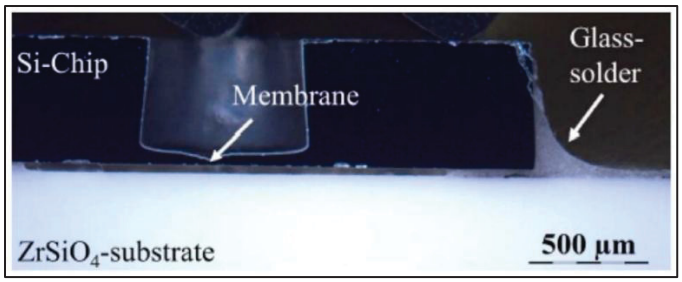

Figure 3.21 Flip-chip assembly on zirconia-silicate
Taken from R.Zeister et al.(2015)

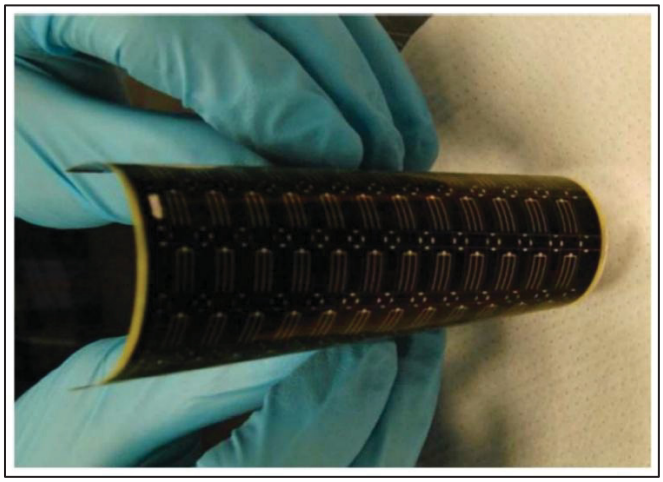

Figure 3.22 Fabricated flexible solar cell
Taken from D.Fobare et al.(2014)

In (K. H. Cheah, P. S. Khiew, & J. K. Chin, 2012) a zirconia MEMS-based micro-thruster is fabricated using a gel-casting method on polydimethylsiloxane (PDMS). In Figure 3.23, process fabrication is presented. After casting the zirconia ceramic suspension on PDMS and machining to form the structure, conductive pastes are printed, and after sealing, the device is sintered. Shrinkage after sintering is around 10–15%. Based on this paper, the formation of the structure can further be enhanced by using other techniques in MEMS fabrication like lithography. Current fabrication is a prototype that can be used for micro-propulsion systems that are able to work under harsh environments such as high-temperature, corrosive, and oxidative. In (G. M. Lin, C. L. Dai, & M. Z. Yang, 2013), an ammonia sensor is fabricated

using 0.18 μm CMOS technology integrated with a readout circuit. The sensor has interdigitated electrodes and a sensitive film, which is a zirconium oxide layer, and is deposited as a post-processing approach. Post-processing includes a sacrificial layer deposition and etching to create an opening by following the sol-gel method, which involves dropping zirconium oxide by micro-dropper and then calcinating it at 100 °C. The fabricated sensor and measurement results are available in Figure 3.24; the sensitivity of the sensor when ammonia gas is introduced at about 4.1 mV/ppm is also shown.

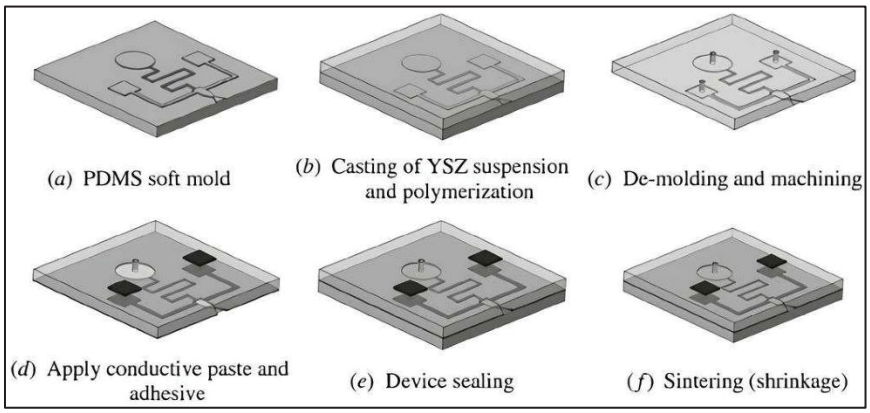

Figure 3.23 Fabrication process of micro-thruster
Taken from K.H. Cheah et al.(2012)

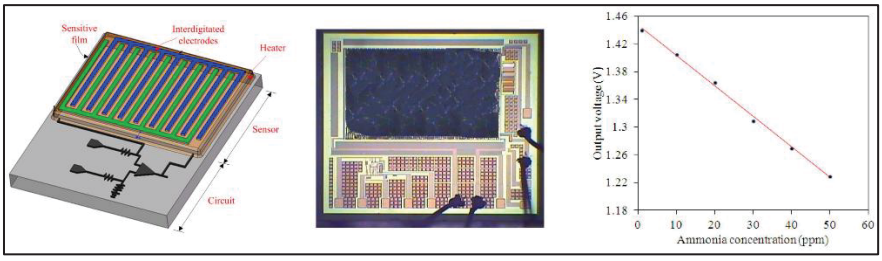

Figure 3.24 Ammonia sensor and readout circuit (left), fabricated circuit (center), measured results of the sensor (right)
Taken from G.M.Lin et al.(2013)

For the packaging aspect, titanium, zirconium, and Zr-Ti alloy are deposited under an ultra-high-vacuum condition. Grain sizes of layers are measured, and their values differ when the thickness of a deposition charges. It is found that the single metal layer has a lower grain boundary density. While it is stated in this paper that higher grain boundary density may lead to higher absorption of gases, the alloy has a better absorption, in conclusion. So, for the packaging purposes of an MEMS device, using a Zr-Ti alloy layer with a lower thickness may help to absorb more gases during the activation of an MEMS getter layer (Lemettre et al., 2023).

3.4.3 Aluminum Nitride-Based MEMS Devices and Systems

Due to the high thermal conductivity, the decent electrical properties of AlN, and its compatibility with other materials in the fabrication of MEMS devices, like silicon in the CMOS-MEMS process, it has been widely used and reported in the literature for the past decades. Since MEMS fabrication needs a very smooth surface, in (Z. Z. Zhou, J. L. Yuan, & B. H. Lv, 2009), AlN is reported as a substrate that needs to be polished before any MEMS fabrication. For this polishing and lapping process, SiO2 is used as a slurry, and other parameters like load on the sample and rotation speed are tuned in a way that the final roughness of the surface is around 6 nm, which is excellent for MEMS fabrication. Indeed, gaps found on the finishing surface of the substrate have an adverse effect on the fabricated MEMS device as well as AlN properties. For this reason, as advised in this paper, the AlN substrate should be as compact as possible before the final sintering of the ceramic (Figure 3.25). Following this issue in (Hassan et al., 2024), aluminum nitride-yttria ceramics are produced, aiming for a better substrate. Mechanical properties, including flexural, are enhanced through pressure-assisted two-step sintering at 1680 °C. After sintering, a post-process, which is microstructural freezing, is conducted. The result grain size of the ceramic is reduced from 2.21 μm to 1.08 μm.

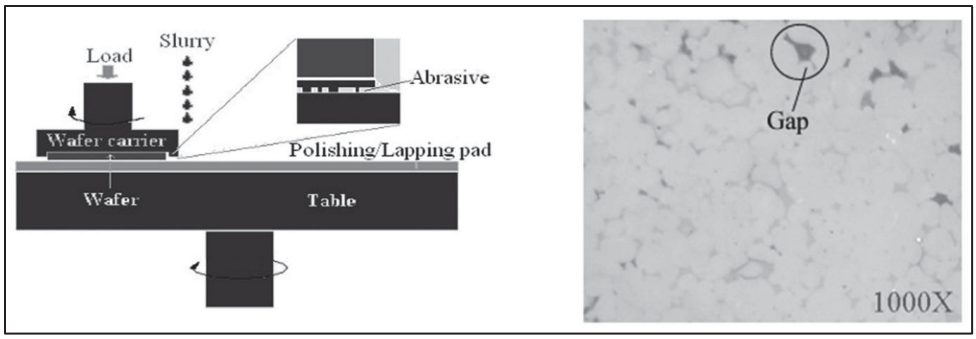

Figure 3.25 Polishing machine (left), gaps found on the surface of AlN after polishing (right) Taken from Z.Z.Zhou et al.(2009)

As a MEMS device, AlN has gained great attraction during the past years, especially as a piezoelectric device. Capacitive Micromachined Ultrasonic Transducers (CMUTs) and Piezoelectric Micromachined Ultrasonic Transducers (PMUTs) are among the most reported devices in the literature (Cai et al., 2022; Proto, Rufer, Basrour, & Penhaker, 2022; S. T. Haider, M. A. Shah, D. G. Lee, & S. Hur, 2023; Ledesma, Zamora, Uranga, Torres, & Barniol, 2021). Due to the need for high voltage in CMUTs and small voltage in PMUT devices, the latter attracted more people. MEMS microphones, speakers, and energy harvesters benefit from the piezoelectric feature of AlN. In Figure 3.26, some of the PMUT devices utilizing AlN and Si_3N_4 as ceramic materials are shown (Figure 3.27) (Ledesma et al., 2019; Horsley et al., 2016; W. J. Liu et al., 2019). In the telecommunication area, AlN MEMS-based devices are widely reported and investigated. In (Xie & Nguyen, 2020; Ding et al., 2022; A. M. Gao, Liu, Liang, & Wu, 2020; A. M. Gao et al., 2019) , AlN Bulk Acoustic Wave (BAW), Surface Acoustic Wave (SAW), and lamb-wave resonators and filters are among the most-reported devices. in Figure 3.28, some of the 3D and cross-section views of these devices are shown.

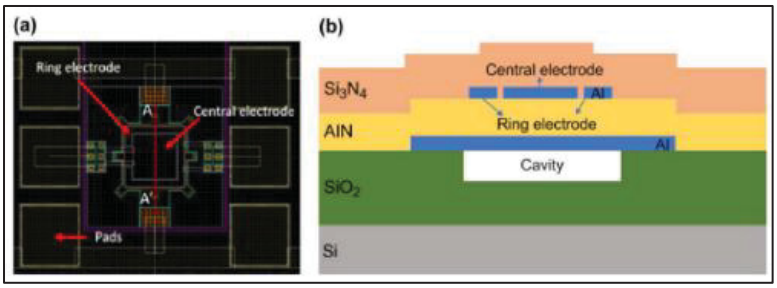

Figure 3.26 (a)A PMUT device top view (b) cross section with different layers including AlN piezo layer
Taken from S.T. Haider et al.(2023)

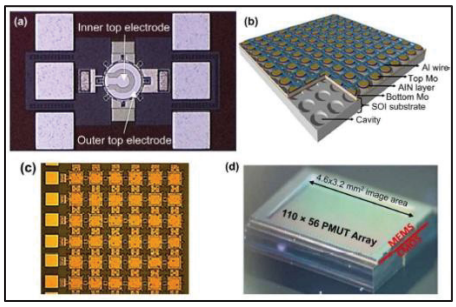

Figure 3.27 Different types of PMUT devices in arrays, (a) top view of a PMUT device, (b) arrays of PMUTs 3Ddesign, (c) top view of arrays of PMUTs, (d) dimensions of PMUT arrays as a MEMS chip on CMOS device
Taken from S.T. Haider et al.(2023)

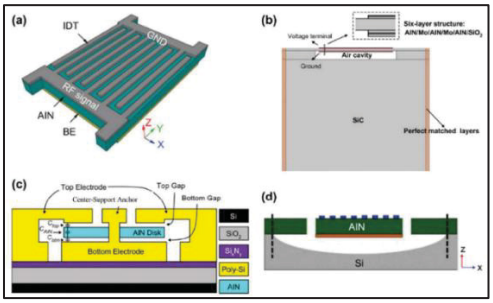

Figure 3.28 (a) A 3D view of AlN lamb wave resonator, (b) cross-section of AlN BAW resonator, (c) cross section of resonator with centered anchor, (d) cross section of a conventional lamb wave resonator
Taken from S.T. Haider et al.(2023)

For the packaging of MEMS devices, since AlN has excellent thermal and electrical properties like high thermal conductivity, low CTE, and high insulation, it is a good candidate for packaging MEMS high-power devices as heat sinks. In (Kanechika et al., 2018), a novel AlN filler approach was used to produce a high-thermal conductive resin for packaging MEMS devices. The thermal conductivity of epoxy resin filled with AlN filler in this work could reach 12 $W \cdot m^{-1} \cdot K^{-1}$.

3.4.4 Silicon Nitride-Based MEMS Devices and Systems

Intense research has been conducted for several years on silicon nitride ceramics when it comes to their application on MEMS. Apart from the preparation of Si_3N_4 with different approaches in the AM area, there are other techniques available in the MEMS area for producing Si_3N_4 thin films and substrates. Among them, we can mention CVD, PECVD, and ALD, which all lead to a thin film of Si_3N_4. As an application in the substrate of a MEMS device, Si_3N_4 is usually used to cover silicon wafers. High mechanical strength, gradual stress control, and corrosion prevention of silicon during the wet etching process are reasons for covering silicon wafers with Si_3N_4. Almost all MEMS devices can benefit from Si_3N_4 properties. In space and communications, biomedical, optics, and automobiles, we can mention RF-MEMS, sensors, and optical MEMS devices that use Si_3N_4 as a passivation layer when contact between RF and DC routes happens. On the other hand, it can be used as a dielectric layer to create a parallel plate capacitor. Due to its high dielectric constant and breakdown value, it is possible to fabricate very thin capacitors with high capacitance ratios that can handle high voltages (Koutsoureli, Siannas, & Papaioannou, 2017; Persano et al., 2023; Rahman, Johnson, Mccallum, Gauja, & Ramer, 2013; Shi et al., 2013). Advances in silicon photonics in the past three decades, thanks to the properties of Si_3N_4, and its compatibility with CMOS technology, opened new doors to enhance optical communications in silicon-based MEMS devices, whether in the passive or active domain. As a passive optical MEMS device, we can mention couplers and splitters reported in (X. T. Zhu et al., 2024; Zheng et al., 2023) , while as an active device, which is compatible with CMOS technology, we can mention the micro-ring modulator and PZT-covering Si_3N_4 waveguide (J. Wang, Liu, Harrington, Rudy, & Blumenthal, 2022).

For switching purposes in several works, Silicon Nitride optical switches are reported. In (S. Sharma, N. Kohli, J. Brière, F. Nabki, & M. Ménard, 2022), actuators with induced voltage move the optical waveguide and couple signals between the fixed and movable lines. Loss in this configuration is measured between 4.64 dB and 5.83 dB. As reported in this paper, this device promises improved tunable transceivers operating in C-band. Silicon nitride is also applied to the packaging of sensitive MEMS devices (Figure 3.29). As an example in (Seetharaman et al., 2010a), a capped BAW MEMS device is illustrated. The sealing of the MEMS device is implemented in a way that handles mechanical damage and loads due to external pressures from the dicing and wire-bonding wafer. As a result of this work, it is reported that this type of packaging can protect MEMS devices during mass production (Figure 3.30).

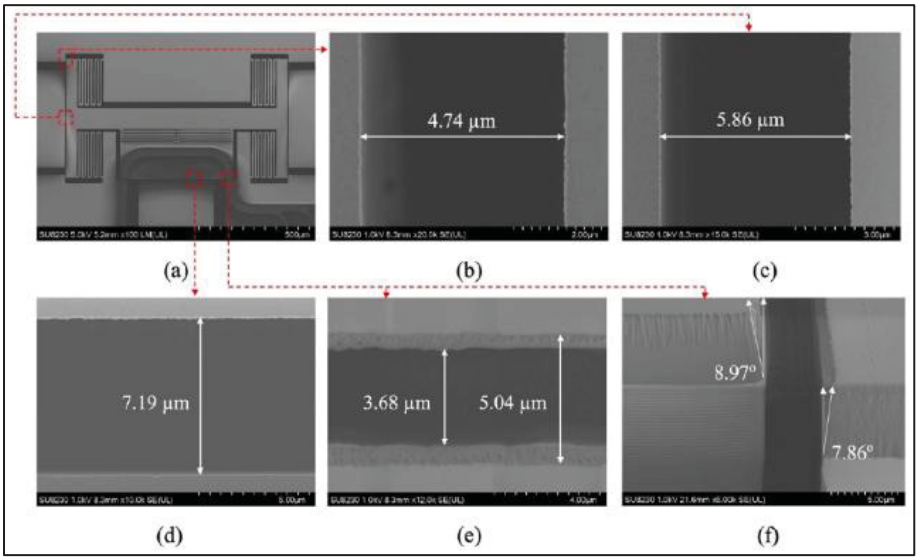

Figure 3.29 SEM image of the fabricated optical 3 × 1 switch with zoom views and dimensions, (a) fabricated device top view; (b) mechanical stopper gap; (c) switching actuator gap; (d) air gap of the gap closing actuator; (e) air gap closing interface; and (f) etch profile of the optical stack.
Taken from S.Sharma et al.(2022)

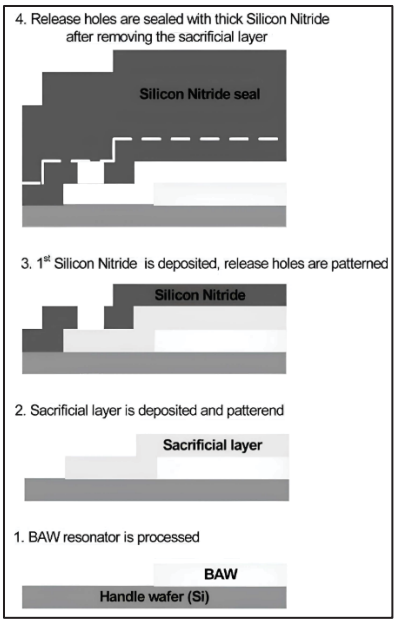

Figure 3.30 Silicon Nitride sealing fabrication process
Taken from Seetharaman et al.(2010b)

3.4.5 LTCC-Based MEMS Devices and Systems

LTCC ceramic materials can be a suitable option for integration with different MEMS devices, including sensors, microfluidics, and switches. Since LTCC ceramics are fabricated as the layer-by-layer process (conventional process) or as a whole 3D structure by printing (AM process), they could be used either as a package, a substrate with embedded passive components, or as a miniaturized device itself. As a substrate, if a conventional method is used to fabricate LTCC, the surface of the substrate before any MEMS process needs to be polished to reduce surface roughness to tens of nanometers. There are several works reporting this issue and solutions to overcome it. Usually, a chemical mechanical polishing machine with a proper slurry that includes nanometer-sized particles is used to reduce roughness as well as waviness of the substrate. As a non-functional substrate, LTCC, like other ceramics mentioned in previous sections, and other conventional substrates, like silicon and glass, are used for surface microfabrication. In (Cianci et al., 2007), RF-MEMS switches are fabricated on top of LTCC

substrates. In (Kolpe, Giramkar, Chaware, Joseph, & Phatak, 2015; Kumar, Suri, & Khanna, 2018) , micro-heaters are fabricated either by PVD sputtering after polishing or by metallization by the LTCC process. LTCC substrates, on the other hand, can be fabricated as functional substrates to embed metallization that either could be DC or RF lines, cavities formation, and vertical vias from the bottom to the top of the LTCC. There are several works that report the integration of the functional LTCC with previously fabricated MEMS devices. MEMS chips could be bonded to the LTCC by bonding from the chip contact pads to the LTCC vertical vias. In (E. Fallahnia & Kouki, 2023), a novel monolithic LTCC-MEMS process is reported, which is one process, LTCC and MEMS devices are fabricated together without the need for challenging post-processing, like alignment for bonding in other processes like the CMOS-MEMS process. Due to the nature of LTCC, which has a rough surface and shrinkage in X, Y, and Z directions, solutions are offered to facilitate the fabrication process as a monolithic one. The roughness of LTCC surface plus via bumps are controlled in a custom polishing process, and shrinkage is compensated with a straightforward solution to fabricate MEMS on top of LTCC vias with less than few micron misalignments. To prove that the process is practical, a capacitive RF-MEMS device is fabricated on top of the functional LTCC substrate while RF and DC control routes are buried inside LTCC layers. As shown in (E. Fallahnia & Kouki, 2023), RF performance is reported, and it is on par with what is available in the literature as a low-loss switch (Figure 3.31 and Figure 3.32). LTCC ceramics can be used as a miniaturized device itself. There are several works reporting LTCC devices as microfluidic devices. Like in (Gongora-Rubio, Espinoza-Vallejos, Sola-Laguna, & Santiago-Avilés, 2001), as a gas flow sensor, holes act as channels. In (C. Li, Tan, Xue, et al., 2014), pressure sensors are reported that are integrated with other electronic chips. Humidity sensors are also reported in (Smetana & Unger, 2008). Since LTCC could be fabricated layer-by-layer as a 3D structure, multifunction sensor fabrication is also feasible. Like in (Belavic et al., 2016), LTCC acts as a fluidic device hosting other heaters and optical sensors as a whole multifunction system. A movable capacitive force sensor as a cantilever with a one-side fixed anchor is reported (Fournier). A special sacrificial layer during the fabrication of an LTCC is used to create the gap between the cantilever bridge and the bottom electrode, which will be removed later for the structure.

Table 3.2 Application of different ceramics in three different categories for MEMS

Ceramic	Use in MEMS		
	Substrate	**Monolithic/Part of device**	**Package**
Alumina	Temperature Sensor (J. Han et al., 2014),Microwave Circuit(Sharma et al., 2013), (Aslani-Amoli et al., 2021), (Aquino et al., 2022)	Optical MEMS device (Y. S. Lee et al., 2011), (Suzuki et al., 2004),RH sensor (László et al., 2008), Gas sensor (H. I. Jeong et al., 2020)	Wafer level packaging(J. Zekry et al., 2011),(V. Maharshi et al., 2023),(D. Yildirim et al., 2016)
Zirconia	Gas sensor (Oblov et al., 2015), Pressure sensor (R. Zeiser et al., 2015), Flexible substrate (D. Fobare et al., 2014)	Micro thruster (K. H. Cheah et al., 2012), Ammonia sensor (G. M. Lin et al., 2013)	Alloy for gas absorbing in package (Lemettre et al., 2023)
AlN	Machining substrate for MEMS(Z. Z. Zhou et al., 2009),(Hassan et al., 2024)	CMUT,PMUT (Cai et al., 2022; Proto et al., 2022; S. T. Haider et al., 2023; Ledesma et al., 2021), SAW,BAW resonators (Ledesma et al., 2019; Horsley et al., 2016; W. J. Liu et al., 2019)	Heatsink package (Kanechika et al., 2018)
Si_3N_4	Passivation layer for Capacitors (Koutsoureli et al., 2017; Persano et al., 2023; Rahman et al., 2013; Shi et al., 2013)	Optical coupler, splitter (X. T. Zhu et al., 2024; Zheng et al., 2023), Micro ring modulator (J. Wang et al., 2022), Optical Switch (S. Sharma et al., 2022)	Capping and sealing BAW resonator (Seetharaman et al., 2010a)
LTCC	RF-MEMS switch (Cianci et al., 2007), Micro heater (Kolpe et al., 2015; Kumar et al., 2018)	Monolithic LTCC-MEMS process (E. Fallahnia & Kouki, 2023), Gas flow sensor(Gongora-Rubio et al., 2001), Pressure sensor (C. Li, Tan, Xue, et al., 2014), Humidity sensor (Smetana & Unger, 2008), Fluidic (Belavic et al., 2016), Cantilever (Fournier)	RF/Optical Switch, Sensors capping and embedding (Fournier)

LTCC is also used for packaging and its implementation is of it is well-reported for different RF-MEMS, MOEMS, sensors and optical circuits (Karioja et al., 2014). Some examples are shown in Figure 3.33.

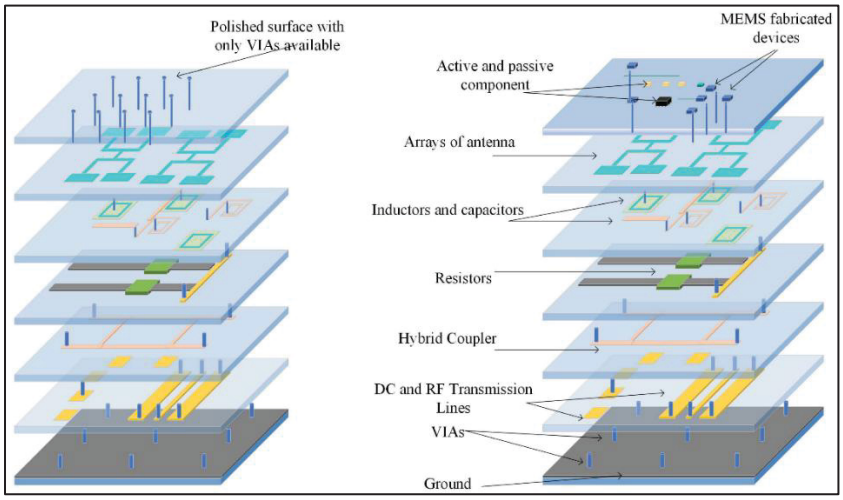

Figure 3.31 LTCC layers with embedded vias, cavities, and metallization as active substrate: (left) polished surface with vias on top, (right) active component and MEMS devices on top after final monolithic fabrication
Taken from E.Fallahnia et al.(2023)

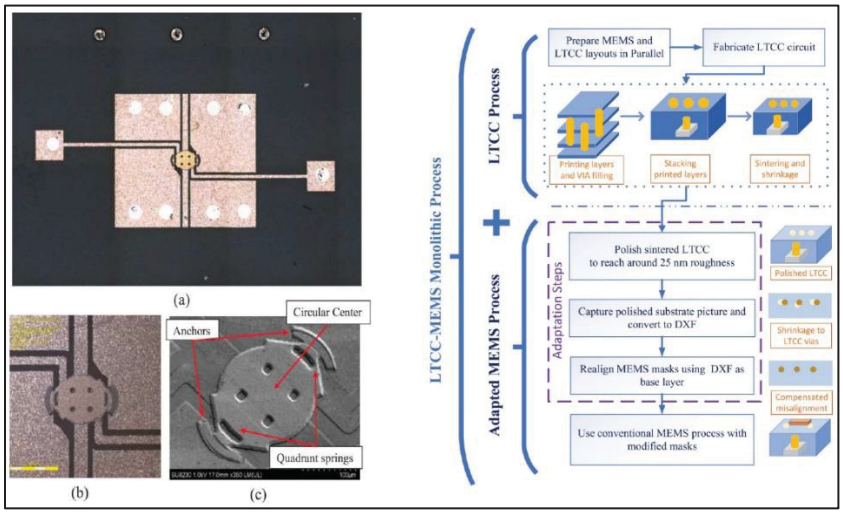

Figure 3.32 Fabricated capacitive MEMS switch with LTCC MEMS monolithic process, (a) Top image of the fabricated switch, (b) enlarged view (c) SEM image (left) LTCC-MEMS process flow (right)
Taken from E.Fallahnia et al.(2023)

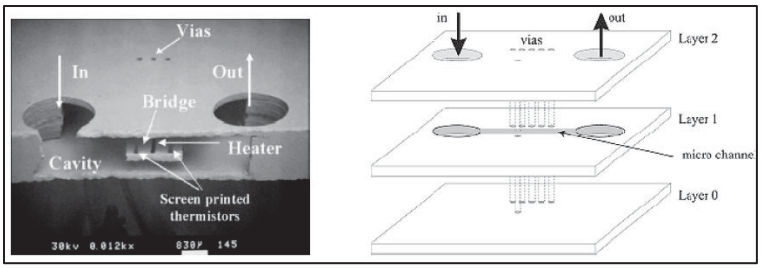

Figure 3.33 Cavities and via holes acting as a fluidic system for sensing application with embedded sensor
Taken from Fournier (2010)

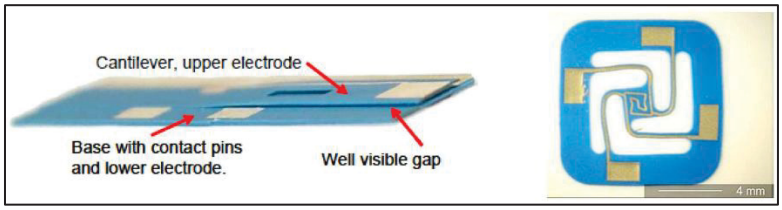

Figure 3.34 Fabricated cantilever with LTCC ceramic materials (left) LTCC hotplate (right)
Taken from Fournier (2010)

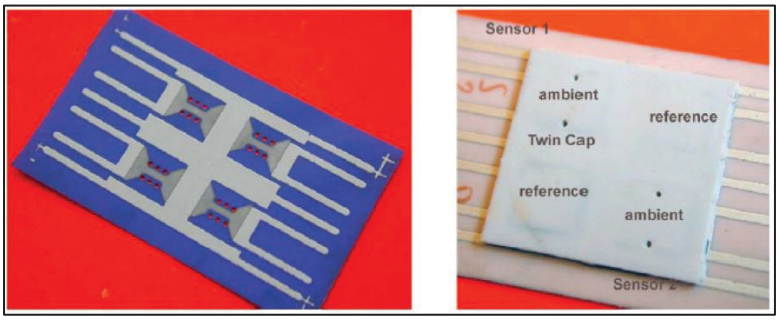

Figure 3.35 LTCC humidity sensors made of different LTCC ceramic materials
Taken from Fournier (2010)

3.5 Conclusion

In this review paper, the use of ceramics for MEMS devices and systems is discussed. Because MEMS devices are delicate and fragile, there is a need to mount, assemble, and pack them. Furthermore, MEMS devices may need to operate in harsh environments, where they are susceptible to high temperatures or chemical corrosion. For these and other considerations, ceramics can be the materials of choice for MEMS-based systems. The unique properties of ceramics, including close CTE values to silicon and high tolerance to elevated temperatures, mechanical and electrical shock, and their extensive use in other non-MEMS circuits and packaging applications make them suitable for MEMS-based systems. While there is a large variety of ceramic materials, the focus has been placed on the five most frequently used ones in this review, namely, alumina, zirconia, aluminum nitride, silicon nitride, and LTCC. Conventional manufacturing of ceramics has been a common process used for many years. However, due to the emergence of 3D-printing technology, additive manufacturing of ceramics paved the way for faster and easier fabrication of more complex ceramic structures, avoiding the lengthy and costly post-process steps associated with conventional methods. Consequently, more applications using ceramic-based MEMS devices are now available in simpler and more efficient ways. Looking ahead, it is expected that as ceramic-based MEMS devices and systems continue to develop and mature, they will be able to offer more reliability and cost-effectiveness in many systems such as automobiles, factory and plant safety systems, biomedical and communication equipment, and more.

CHAPTER 4

Compact LTCC-Integrated Fully Decoupled Biasing for Wireless Sensors

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Abstract

This paper presents the design, simulation, fabrication, and measurement of a compact bias-tee fully embedded in an LTCC substrate suitable for wireless sensor applications. The structure features two parallel-plate capacitors, one at each RF port, and a centrally placed inductor for DC injection, providing complete DC isolation while maintaining RF continuity. Unlike conventional bias-tees, this configuration isolates both RF ports from DC bias, making it ideal for sensitive RF front ends and embedded sensor systems. Simulated and measured S-parameters confirm excellent RF performance with low insertion loss and high isolation. The device was fabricated using DuPont 951 LTCC, and its internal structure was validated using X-ray imaging. This embedded bias-tee enables reliable, compact integration in multi-functional sensor systems, supporting co-packaged RF components and minimizing interference in high-density multi-layered devices and circuits.

Keywords: bias-tee, MEMS, LTCC, monolithic fabrication, wireless sensors

4.1 Introduction

Advanced wireless sensing systems utilized in defense, automotive, satellite communication, aerospace and other applications require the seamless integration of active sensor devices with radio communication circuitry. There are several works that demonstrate miniaturized devices with the possibility to be integrated in a wireless sensing system like radio-frequency microelectromechanical systems (RF-MEMS) power (Z. Zhang et al., 2025), temperature

(Huang et al., 2024), pressure (Tulaev et al., 2024), and humidity sensors (Chung, Liang, Cheng, Yip, & Fang, 2014). The incorporation of these types of miniaturized sensors, which may include MEMS switches, tunable capacitors, and varactors, necessitates the development of compact, highly reliable biasing circuits to ensure optimal performance and stability (Gu, Qiao, Wang, Cai, & Zhang, 2024; Hikmat & Ali, 2017; Z. Zhang, Gu, & Liu, 2023)while keeping cost and size to minimum. A bias-tee is a three-port device that enables the concurrent transmission of radio signals between two ports while supplying the necessary DC bias through a third port. Conventional bias tees, see Figure 4.1a, are typically discrete and bulky components that provide DC decoupling only on one side, i.e., one of the RF ports. If a single DC bias is required, e.g., a diode, an additional decoupling capacitor is usually required and added at the second RF port. When dual biasing is needed, e.g., a transistor, two bias tees are used as shown in Fig. 1a so that full DC decoupling is insured. However, in miniaturized wireless sensor modules where both RF ports interact with sensitive components, maintaining full DC decoupling at both ends is imperative to mitigate leakage currents, signal distortion, and potential component damage. In such cases, discrete bias tees are not adequate and having highly compact biasing structures that can be easily integrated with miniaturized sensors and provide full DC decoupling is a desired optimal solution. To this end, a novel bias tee architecture is introduced, see Fig. 1b and implemented using Low-Temperature Co-Fired Ceramic (LTCC) technology. This architecture incorporates capacitive DC isolation at both RF ports and one or two embedded RF chokes. By integrating key passive structures such as parallel-plate capacitors, inductors, and via transitions within the LTCC multilayer stack, the proposed design achieves a highly compact footprint optimized for high-density integration. This configuration is particularly advantageous for advanced sensing platforms, as it enhances electrical isolation, preserves RF signal integrity, and ensures mechanical robustness, making it well-suited for modern wireless sensor applications. The proposed design can be used in two distinct ways for sensor integration: (i) monolithically through a MEMS on LTCC process (E. Fallahnia & Kouki, 2023) where the MEMS sensor is fabricated on a functional LTCC substrate that incorporates the bias tee or (ii) discretely by mounting the sensor between the two ports of the bias-tee by techniques like wire-bonding, flip-chip or soldering.

The rest of this paper is organized as follows: section two, presents the proposed bias-tee module and its EM full-wave simulation results. In section three, the fabrication of the bias-tee based on the dense, 3D functional multi-layer LTCC technology is explained. Section four presents measurement results and compares them to simulations.

4.2 Design and Simulation of the proposed Bias-tee

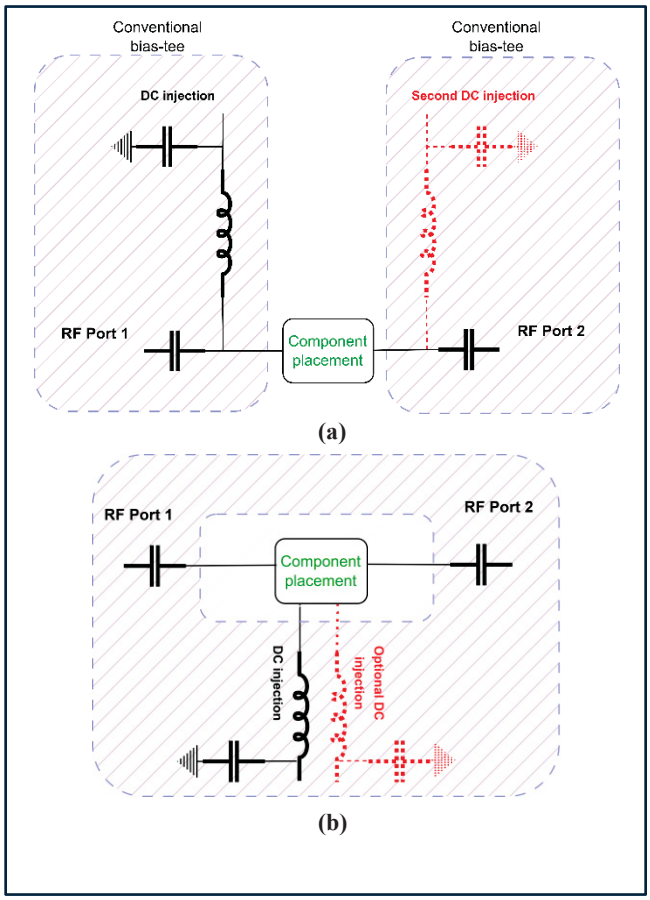

Figure 4.1 (a) Conventional bias-tee circuit (b) integrated bias-tee with sensor component

4.2.1 Design of the Bias-tee and its key embedded components

The proposed bias-tee is designed based on the functional Muli-layer LTCC technology. For this design, 13 sheets of 2 mil and two sheets of 10 mil layers from Dupont 951 material is chosen. While the first layer is dedicated to the surface Coplanar Waveguide (CPW) line (signal = 150 μm, gap = 50 μm) metallization, second and the third layers are used to form parallel plate capacitors for both input and output of the bias-tee. At the isolation port, a capacitor bank including six parallel plate capacitors are placed in parallel configuration to strengthen the isolation and grounding of the bias-tee. Between the isolation port and the input/output ports, a high impedance inductor is placed on the 10th layer of 2 mil sheet to connect the through path to the isolation port.

In Figure 4.2, we can observe a 3D view of the bias-tee. Two parallel plate capacitors at input/output ports are designed to have 1pF capacitance. Their dimensions are 800×700 μm^2, the dielectric thickness between plates are a 2-mil sheet and with Dupont 951 material, ε_r is around 7.5. The inductor length and width are 1250×40 μm^2. Designed value of the inductor is almost 3 nH. Finally, the capacitor bank, including six parallel plate capacitors that are in parallel configuration with the same dimensions of the coupling capacitors in port one and two, are placed at port three. The total module dimension is 3.5×3.5×1.1 mm^3. For this design, the area between the input and output port there is a CPW line where it is the potential spot for the sensor to be either fabricated monolithically with embedded bias-tee or mounted on the module.

4.2.2 EM simulation of the bias-tee module based on the designed parameters

For the proposed design, EM full-wave simulation using Ansys HFSS is performed from 3 to 8 GHz. Insertion loss better than 0.5 dB and return loss better than 20 dB for almost entire band between port one and two as well as isolations between port three and other ports are achieved. Results are illustrated on Figure 4.3.

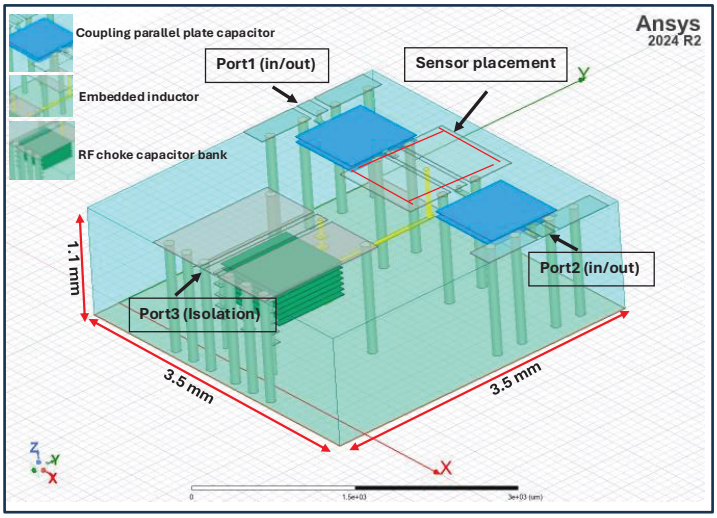

Figure 4.2 3D view of the bias-tee module

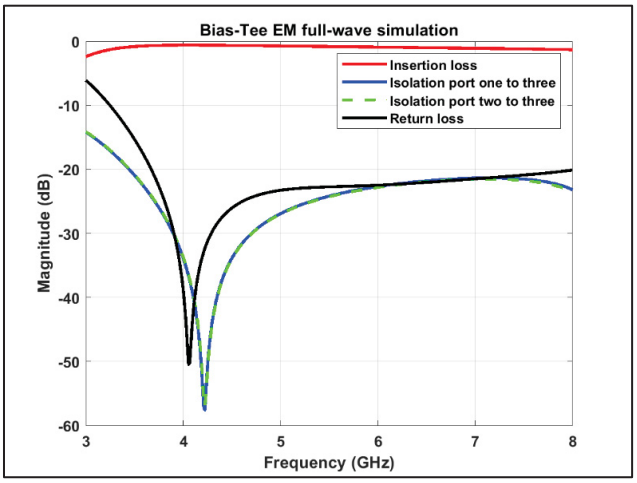

Figure 4.3 EM full-wave simulation of the bias-tee module

4.3 Fabrication process of the bias-tee module

Fabrication process of the bias-tee is done through the standard process of LTCC (Manzillo et al., 2016). Green tapes of LTCC are individually punched and then filled with silver paste to

form the vertical via connections. Conductor printings are performed using silver pastes to create parallel plate capacitors and the inductor as well as the CPW line at the surface layer. Vias from the top metallization to the capacitor plates and the inductor are formed with laser ablation and their diameters are 50 µm and the other vias for grounds of the circuit are punched with 150 µm diameter. Then all the layers are aligned and stacked together for lamination. In the next step, dicing is done in which, the whole stack is cut by laser ablation process into smaller pieces that on each of them, there are multiple fabricated bias-tees to validate the target design. At the final step, all the smaller tiles are placed into the oven and sintered to up to 900 °C to create a robust, dense 3D structure. In Figure 4.4 and Figure 4.5, we can see the fabricated bias-tee from top view and the X-Ray image, to see layers and vertical vias of the module inside the LTCC substrate. After the fabrication, an anisotropic shrinkage happens to the fabricated device. For Dupont 951, the shrinkage in X and Y is 12.7%, and in Z direction is around 15%. Also, it is worth mentioning that the thickness of printed conductor after the co-firing process is around 8 µm. Regarding the shrinkage factors, the initial design parameters are tuned based on the fabricated bias-tee after the sintering and applied shrinkages.

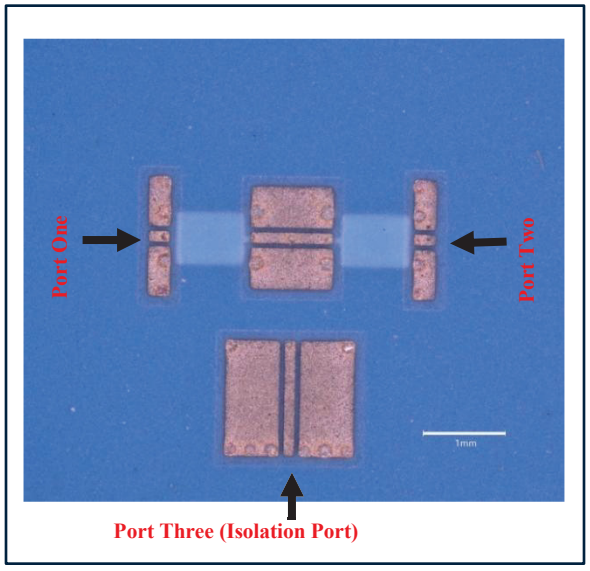

Figure 4.4 Fabricated bias-tee from Top view

Metallization on the surface of the module are printed to have access for the measurement. In case of integration of a sensor with the bias-tee in a monolithic fabrication process, the surface

is polished to nm roughness levels and only vias from internal layers are remaining at the surface. By proper alignment as detailed in (E. Fallahnia & Kouki, 2023) and surface microfabrication process, sensor and transmission lines can be fabricated at the surface where RF and DC vias are located.

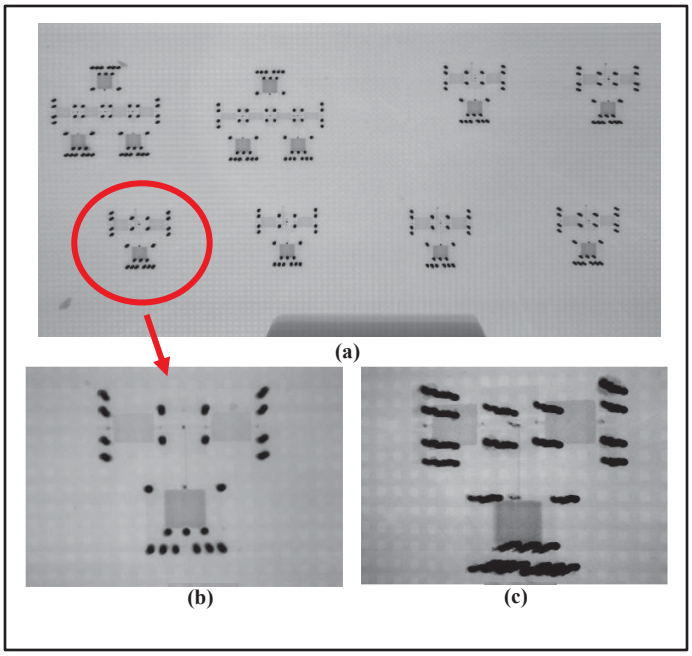

Figure 4.5 (a) X-ray top view of the whole tile with multiple bias-tee modules, (b) Zoomed view of a bias-tee from top, (c) Angle view of the bias-tee with vertical vias connections

4.4 Fabrication measurement results and discussion

Measurements of the bias-tee module is carried out using three GSG probes connected to a PNAx on a probe station (Figure 4.6). Calibration is done with Thru-Reflect-Line (TRL) method for three ports. Frequency range of measurements is set from 3 to 8 GHz and the S-parameters values are extracted from three ports to validate insertion loss and return loss between port one and two and the isolation between port three and the other two ports. Measurement results are shown on Figure 4.7. Differences between the isolation values from port three to one and two is because of the anisotropic shrinkage that happens to the LTCC and

in this case, minor differences in the capacitance dimensions at each port are causing the issue. Nevertheless, the results maintain perfect isolation at each port and variations are negligible. Based on the measurement results, we can see a strong correlation between the EM simulation and measured S-parameters. Regarding the wideband performance that covers C-band, some 5G and 6G bands as well as Wi-Fi 7 and 8, and also the compactness of the bias-tee module, it can be a suitable embedded component to be integrated with miniaturized RF sensors, including the RF-MEMS power sensors, thermopile sensors, pressure sensors and more in a wide variety of applications. Decent isolation between DC and RF at all ports, help to increase the performance of the sensor and the integrity of the whole wireless sensor system.

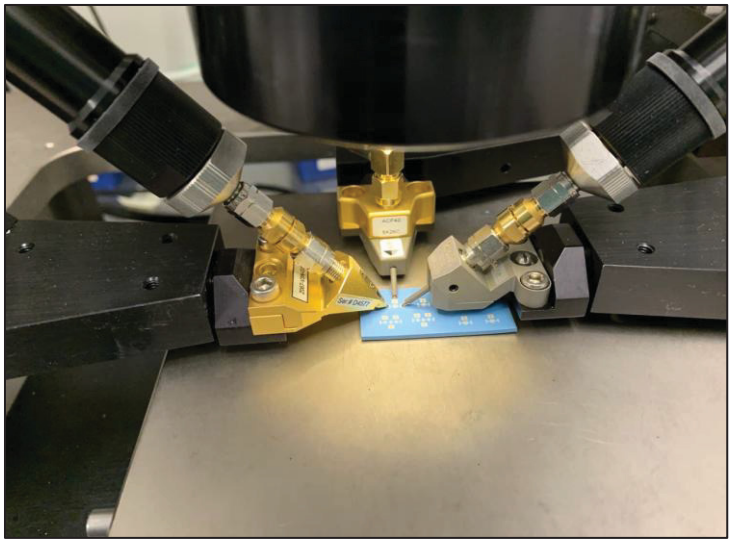

Figure 4.6 Measurement of the bias-tee module using three GSG probes

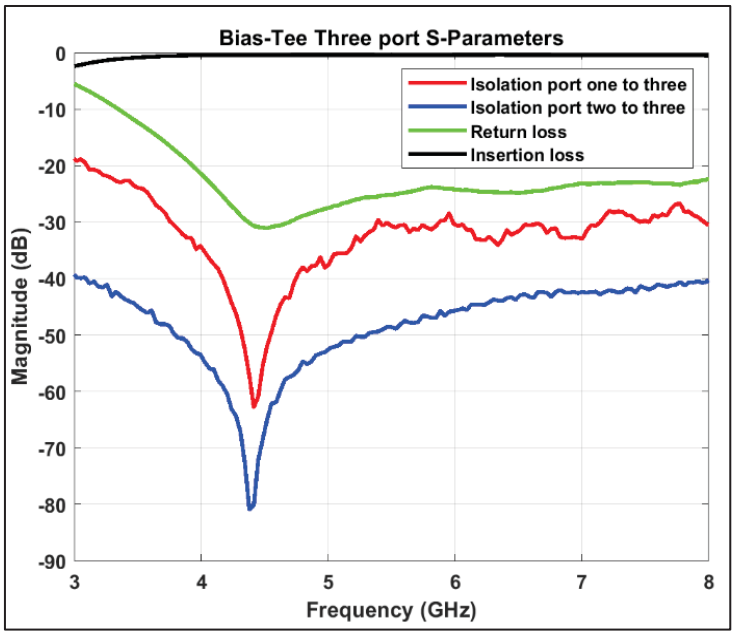

Figure 4.7 Measured S-parameters of the bias-tee module

4.5 Conclusion

A novel bias-tee design has been successfully demonstrated using LTCC technology, featuring dual capacitive DC isolation at each RF port and an embedded inductor for bias injection. The design was thoroughly validated through simulation, fabrication, and experimental measurements, showing excellent agreement with optimum RF characteristics. Its compact form factor, enabled by multilayer LTCC integration, makes it well-suited for embedding in sensor nodes, especially where signal integrity and DC isolation are critical. Furthermore, the use of LTCC allows for robust packaging in harsh environments and offers the potential for co-integration with additional passive or active devices with sensing elements. This work establishes a foundational component that can serve both as a reliable biasing interface and as an enabling technology for next-generation RF sensor modules. Future work includes incorporating active and passive sensor elements and evaluating performance in complete sensing platforms.

CHAPTER 5

Field Programmable Frequency Agile Microwave Amplifier based on Monolithic LTCC-MEMS Process

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Abstract

In this work, a Field Programmable Microwave Amplifier (FPMA) using LTCC-MEMS process is proposed and detailed in design, fabrication and measurement. With the advantage of RF-MEMS technology and LTCC 3D multi-layer substrates, miniaturized Distributed MEMS Transmission Line (DMTL) tuners embedded inside the LTCC layers are developed. Using monolithic LTCC-MEMS process, RF-MEMS capacitive switches are fabricated at top of functional LTCC substrates that embed vertical transitions of the DMTL to enable frequency tuning is different wide-bands. Lower band (LB) from 3 to 5 GHz and Higher Band (HB) from 5 to 8 GHz is determined for the operation. Reconfiguration is achieved using embedded reflectometer sniffers that are placed at the input of the DMTL tuners cascaded to GaN transistor device. Best MEMS switch combinations for impedance matching are detected with embedded sniffer and proper voltage controls are sent to the switches for actuation. The present designs are able to achieve stable gains for the amplifier close to maximum stable gains with minimum losses. Tuners' coverage in designated frequency band and their ability to cover areas for impedance matching are illustrated. Indeed, sniffer performance in detecting optimum gamma points for switch combinations is also investigated and decent performance for the entire band is obtained.

Keywords: **RF-MEMS, Monolithic process, LTCC, sniffer reflectometer, DMTL, reconfigurable amplifier**

5.1 Introduction

With advances in radio communication systems and technologies, like 5G, 6G, and IoT, and the increasing use of terrestrial and satellite frequency bands in a single terminal, the development of intelligent RF front-ends is becoming essential (Carlowitz & Dietz, 2023; Wane et al., 2020; Jain, Agrawal, Garg, & Natarajan, 2021). These front-ends can reduce hardware redundancy and cost by providing frequency agility and field programmability in single RF chains, unlike traditional approaches that implement multiple dedicated narrowband RF chains. A key to such front ends is having access to energy efficiency and cost-effective programmable microwave amplifiers with tunable matching network over a wide frequency range. Reconfigurable microwave amplifiers have been the subject of extensive research for applications in modern communication systems, radar, and adaptive sensing, where amplifiers must maintain optimal performance over wide frequency ranges or in dynamically changing environments (P. Li, Peng, & Li, 2019; Mikrut et al., 2024; Shaffer, Johnson, Jones, Semnani, & Peroulis, 2025). Numerous approaches have been reported to realize tunable matching networks, including CMOS-based lumped elements (Gilasgar, Barlabé, & Pradell, 2019), varactor-loaded lines (Moloudi & Eslamipour, 2021), PIN-diode and FET tuners (Kang, Kim, & Kim, 2015; Kim, Kang, Kim, & Kwon, 2014) and fluidic tuners (Bahloul & Kouki, 2020; Morishita, Dang, Gough, Ohta, & Shiroma, 2015). While these techniques can achieve impedance reconfiguration, they suffer from significant limitations. Most of them often exhibit high insertion loss, limited linearity, and restricted tuning range (Rebeiz, 2003); and many reported solutions are inherently narrowband (Ferris, Tant, Giry, Arnould, & Fournier, 2016). Thanks to progress in Microelectromechanical Systems (MEMS) technology, impedance tuners using RF-MEMS switches have become increasingly attractive due to their lower loss and near-zero power consumption. Various MEMS impedance tuners, including stub tuning and Distributed MEMS Transmission Line (DMTL) configurations, have been developed (Yazdani & Mansour, 2017; Vähä-Heikkilä & Rebeiz, 2004). Stub and lumped matching circuits usually can match a few points or narrow coverage by adjusting the length of the stubs or selecting lumped elements using contact MEMS switches; however, they require bulky circuits for wider matching bands (Vaha-Heikkila, Varis, Tuovinen, & Rebeiz, 2005; Okocha

& Rudolph, 2022). By contrast, DMTL units can achieve wide frequency range matching while occupying significantly less space. These units load a transmission line with multiple equally spaced MEMS switches which, when actuated, alter the impedance and effective dielectric constant locally. For a DMTL with N switches, 2^N impedance states scattered over the Smith chart can be achieved by actuating a subset of switches for each state. More recent research has explored DMTL as low-loss, high-linearity tunable matching networks (Fouladi, Domingue, Zahirovic, & Mansour, 2010). DMTLs provide controllable phase and impedance transformation, offering lower loss and higher linearity than semiconductor-based tuning elements. While MEMS DMTLs offer excellent RF characteristics, their integration and packaging present challenges. Most reported implementations, fabricate MEMS devices and RF circuits on non-functional substrates including silicon, glass, quartz, and alumina, which require different bonding methods for integration (Fall et al., 2013). This increases overall system size and introduces parasitics that degrade matching accuracy due to RF losses. Furthermore, in these designs, RF and DC bias lines often share the same layer, leading to layout compromises, larger footprints, and potential electromagnetic coupling between control and RF paths. On the other hand, these devices' performance in harsh environments degrades due to mechanical and thermal stresses and corrosive environments. Various integration technologies between MEMS devices and mentioned substrates which most of them uses silicon-based substrates, have been reported. They are commonly exploiting CMOS process in combination with MEMS fabrication in different approaches. They can be categorized in three different techniques: (i) MEMS and CMOS devices are fabricated in different processes and then the integration is done using different bonding methods like wire bonding and flip-chip or other post-process fabrication methods like substrate transfer that all of them introduces more costs and complexity to the integration (Q. X. Zhang et al., 2008), (ii) monolithic simultaneous fabrication of MEMS and CMOS devices which avoids problem of the previous method but suffers from temperature limitation during fabrication that stems from high temperature for CMOS process that can adversely affect fabricated MEMS devices (Valle et al., 2017) and (iii) Monolithic sequential fabrication which let the MEMS devices to be fabricated after the CMOS fabrication that eliminates limitation from previous technique but

suffers from incompatibility between materials and process used in MEMS fabrication like the need for bulk etching which may affect previously fabricated substrate (Pinto et al., 2022).
These limitations motivate the need for a substrate technology that supports: Compact three-dimensional routing of RF and DC lines, embedding of passive elements and sensing circuits with direct mounting of discrete and monolithic fabrication of MEMS units with minimal interconnect parasitics.
To address mentioned issues, ceramic substrate known as Low Temperature Cofired Ceramic (LTCC), meets these requirements by enabling multilayer integration of RF signal lines, DC bias networks, and embedded passive structures within a single compact substrate. LTCC substrates feature low dielectric loss, high thermal stability, and compatibility with hybrid metallization which can use different metals like gold and silver for vertical interconnections and conductor printings in a single process. By using LTCC in fabricating DMTL circuits, Internal layers can carry RF transmission lines to reduce the physical footprint of DMTLs, while DC bias lines can be routed independently to avoid interference with RF paths. Regarding the novel process introduced in (E. Fallahnia & Kouki, 2023), a monolithic LTCC-MEMS microfabrication process is illustrated and detailed which utilize a single fabrication to produce dense 3D LTCC substrate with MEMS devices on top of it. This process addresses limitations and shortcoming of mentioned techniques and provides novel integration techniques to fabricate a wide band Field Programmable Microwave Amplifier (FPMA) using MEMS DMTL circuits. The main idea is to implement a programmable RF amplifier using a single hardware without adding or removing redundant circuit units when frequency of operation changes. Main units of the FPMA are (i) DMTL MEMS circuits incorporated with MEMS tunable capacitors on top and embedded DMTL lines buried inside LTCC in different layers as spacing between MEMS switches, (ii) an embedded 4-port sniffer that detects optimum matching points for DMTL and (iii) stabilized GaN transistor which operates from 2 to 10 GHz.

The whole system is then controlled with an external circuit and based on the feedback from sniffer readings, target combination of the DMTL is selected for the maximum source gain in designated frequency bands. In Figure 5.1, a block diagram of the whole system is shown when a wideband operation with variable biasing of an amplifier for both input and output is required.

Two different FPMA are designed, fabricated and measured. One for Lower Band (LB) from 3 to 5 GHz and the other one which covers the Higher Band (HB) is from 5 to 8 GHz. Rest of the paper is organized as follows: Section II presents the design and simulation results for LB and HB DMTLs and their dedicated sniffers for each band. In section III, monolithic fabrication process and integration of the FPMAs and their feedback control system are presented and highlighted. In section IV, measurement results including tuner coverages, sniffer matching points detections and amplifier maximum gain within the desired frequency bands are discussed.

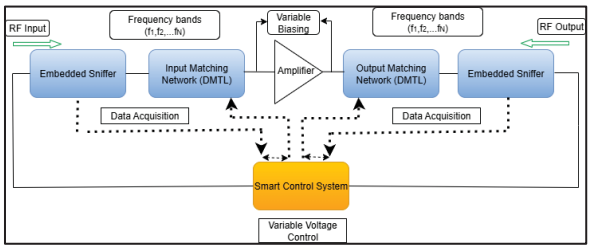

Figure 5.1 Block diagram of FPMA

5.2 Design and simulation of FPMA main units

The proposed FPMA designs are constructed from different key units that are essential for delivering maximum power from input to the output of the device by proper impedance matching in designated frequency bands. Capacitive MEMS switches provide for the capacitance ratio and are placed on top of embedded DMTLs. Each DMTL cell is buried in layers of the LTCC and determines spacing between MEMS switches. On the other hand, an embedded sniffer is placed at the input before DMTL to detect proper matching impedance and provide input data to enable the best combination for the 8-bit DMTL. The whole system is cascaded before a biased and stabilized GaN device. For the present design, only input matching and sniffer measurements are implemented since more input gain is available compared to output gain. All designs and fabrications are carried out using the same LTCC material, namely 4.5 mil and 10 mil-thick green tape of Dupont 951 (ε_r = 7.5 tan δ = 0.006) with silver metallization for the inner layers and gold for the top layer vias. Aluminum is used

for surface layer metallization and for MEMS switches. Each unit design and simulation results are detailed in the following sections.

5.2.1 MEMS capacitive switch design

The MEMS capacitive switch is the key building block for all impedance tuner designs. Its monolithic design consists of using a functional LTCC substrate, where DC and RF lines are already embedded, and switch is fabricated on a surface Coplanar Waveguide (CPW) line with anchors placed on the CPW grounds. DC biasing for actuation is routed inside the LTCC layer to avoid RF and DC interference and are connected to top actuation pads with vertical vias. The target Cr for this design is 7.8 with Cd = 890 fF and Cu = 115 fF Using 3D field simulation software. Cd and Cu are capacitances of the switch in down-state and up-state respectively. The overall dimensions of the switch are found to be 200×320 µm2 with a capacitive area of 200×80 µm2 with an actuation voltage of 30V and a release voltage of 10V.

5.2.2 DMTL designs and simulations for LB and HB

DMTLs are designed in a way to cover specific frequency bands be they LB and HB. Each DMTL can be divided into eight units. Each unit incorporates a central capacitive MEMS switch with two halves of the transmission lines on each side of the switch as spacings between MEMS switches. The spacing between MEMS switches (S) and their dedicated distances is one of the main factors that determines the coverage of the tuner. As the length between each switch increases, lower bands can be covered with a wider coverage on smith chart and vice versa. Another key factor that affects the coverage is Capacitance ratio (C_r) of the MEMS switches and each value of C_r varies characteristic impedance loading (Z_0) and the effective dielectric constant (ε_{reff}) of the line. As the C_r increases, wider coverage may be achieved on smith chart considering the distance between each switch. As it is reported in (Rebeiz, 2003), and the equations for calculating mentioned parameters, coverage of the smith chart is limited by the Bragg frequency. In Figure 5.2, an equivalent circuit model of the DMTL unit cell is shown. All parameters are validated by extracting them from 3D EM full-wave simulation and

equations in (Rebeiz, 2003). All parameters are shown in Table 5.1. To achieve wide coverage at lower frequencies and the advantages of dense 3D multi-layered LTCC substrates and the leverage to access inner layers of the substrate by using the proposed LTCC-MEMS monolithic process (E. Fallahnia & Kouki, 2023), the whole DMTLs footprints can be substantially smaller comparing to regular DMTLs which are fabricated at the surface of a substrate with a linear design(Vaha-Heikkila & Rebeiz, 2004).

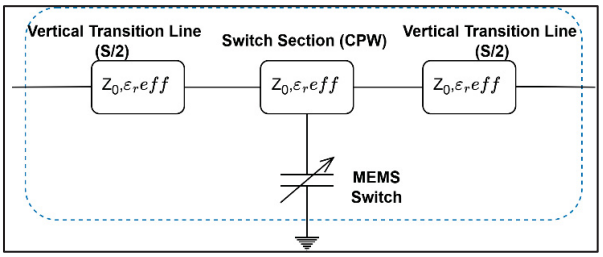

Figure 5.2 DMTL unit cell equivalent model

Table 5.1 DMTL parameters and their values in up and down states

C_{up}	115 fF	**Switch section $Z_{o\text{-}up}$**	44.3 Ω
C_{down}	890 fF	**Switch section $Z_{o\text{-}down}$**	27.4 Ω
Line $\varepsilon_{reff(CPW)}$	4.1	**Switch section $\varepsilon_{reff\text{-}up}$**	7.7
Line Z_o	58 Ω	**Switch section $\varepsilon_{reff\text{-}down}$**	20.5

For the LB and HB DMTL configuration, a three-layer design is proposed. These layers are 4.5 mil sheets of LTCC. The first layer is dedicated to aluminum CPW lines (Signal = 150 µm, Gap=50 µm) where the MEMS switches are fabricated. Second layer is intended for the RF vertical transition between each switch, and the third layer is where DC control routes are passing freely without any interference with RF lines. All internal conductors and vias with diameter of 130 µm are silver apart from top vias that are gold. Such design introduces advantages over surface fabricated DMTLs (Vaha-Heikkila & Rebeiz, 2004). MEMS process is more simplified by eliminating some steps that tries to isolate RF and DC lines and more

importantly, a compact design is achievable. In Figure 5.3, illustrations of several DC routes are avoided to make it simpler.

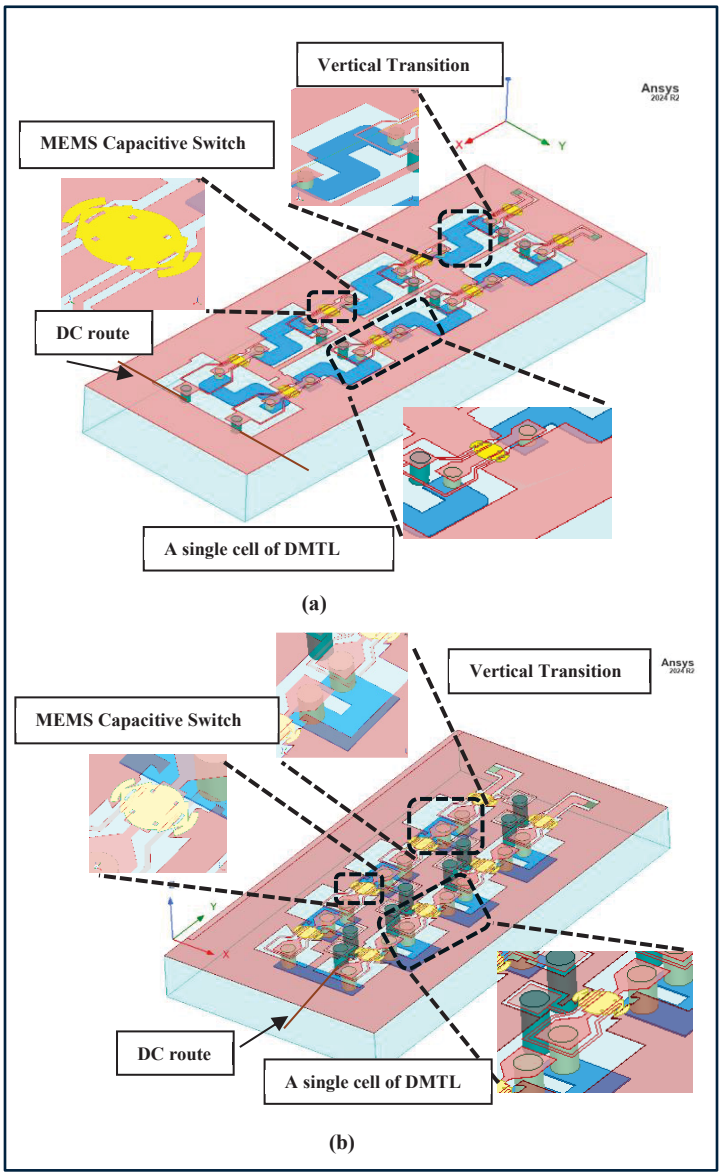

Figure 5.3 3D schematic of DMTLS, (a) LB, (b) HB designs

As is shown in Figure 5.3(a), for LB configuration, a meandered shape for the transition between MEMS switches is designed where it is connected to the top switches with a matched vertical connection through vias. The total length of the meandered line is 2 mm with 250 µm

width and the total dimension of the DMTL is 7.2×2 μm^2. Since the spacing is buried and meandered, a compact design comparing a linear DMTL is achieved, and the tuner is total dimension is reduced by 22.2 %. DC lines are also placed at the third layer for outer voltage control and vertical vias connect them to the surface pads for DC actuation.

For the HB design (Figure 5.3(b)), a more compact configuration is designed, and the vertical transition is a U-shape design between each switch and is buried inside the LTCC in the second layer with a length of 1 mm and width of it is 250 μm. Like the LB design, DC routes are placed at the third layer. The total dimension of this design is 4.1×2 μm^2 with a size reduction of 29% compared to a linear DMTL.

Since the transition between the switches in HB design is reduced and the total DMTL module dimension is reduced by 43.45 % compared to the LB, its bragg frequency is considered to be much higher. Designed tuners use one layer for RF transition and a total three-layer design, but they may be further miniaturized by leveraging inner layers of LTCC to design matched vertical transitions using more layers.

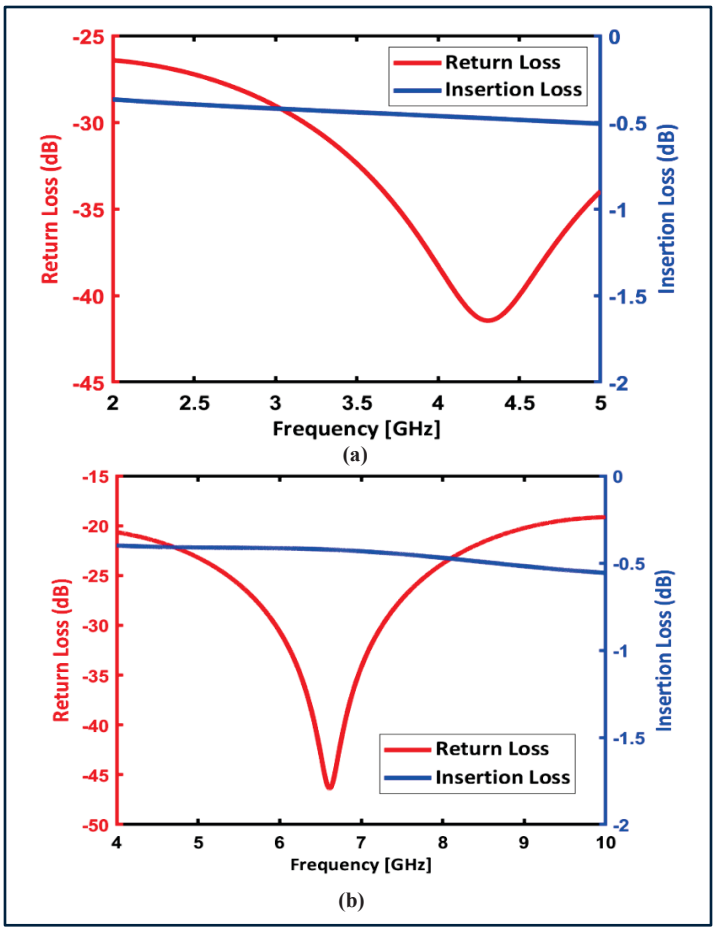

Figure 5.4 Full-Wave simulation S-parameter simulation of DMTLs, (a) LB, (b) HB when all switches are at up-state

3D full-wave electromagnetic performance of the DMTLs is analyzed and in Figure 5.4, return loss and insertion loss of each design when all switches are in up-state is illustrated. For the whole band, considering the dielectric and conductor loss, insertion loss is around 0.5 dB while the return loss is kept well below 20 dB for both designs. Indeed in

Figure 5.5, coverage of each tuner in different frequencies is shown. It can be observed that at 5 GHz the LB design is reaching its widest coverage and gradually proceeds to its Bragg frequency while for the HB design it is much smaller, and wider coverages happen until 8 GHz. Areas of the coverages on smith chart are calculated by tuning C_r and S and are based by the placement of the input impedances of the transistor. To this end, perfect matching is feasible, and more input gain can be achieved.

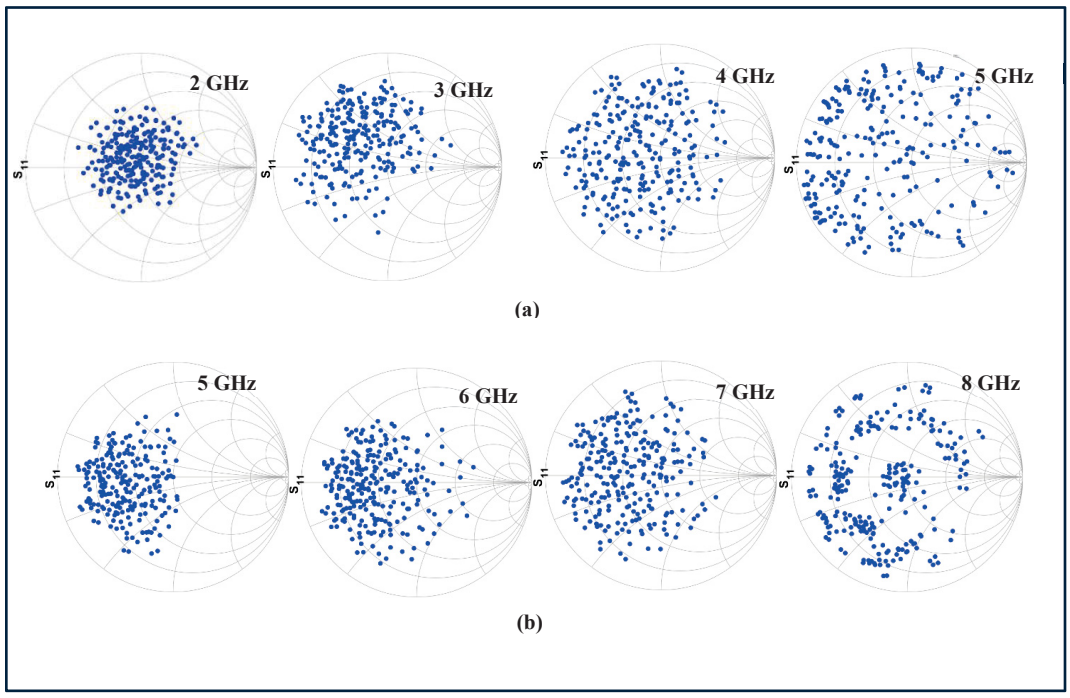

Figure 5.5 Full-Wave simulation Smith chart coverage of DMTLs, (a) LB, (b) HB designs

5.2.3 Embedded 4-port Sniffers design and simulation for LB and HB

Vector reflectometers are generally classified as coherent or non-coherent. Coherent designs (Nasr et al., 2014; Kissinger, Kaynak, & Mai, 2022), such as commercial VNAs, employ couplers, synthesizers, mixers, and LNAs, offering high accuracy and dynamic range but at the expense of size, complexity, and power, which limits their use in embedded applications. Non-coherent reflectometers instead use scalar detection of the reflection coefficient (Γ), most notably the six-port (Staszek, 2021; Wan, Huang, Liu, & Zhu, 2025) and sampled-line (Avci

& Ozev, 2023; Donahue, Falco, & Barton, 2020) structures. The latter is favored for embedded, wideband measurements due to its simplicity and compactness. A key challenge of sampled-line reflectometers is calibration. Conventional methods (Shihe & Bosisio, 1982) require external standards, impractical in embedded systems. An alternative approach [31] determines Γ using the reflectometer's S-parameters. In this work, leveraging the high accuracy of LTCC fabrication, we adopt this method to calibrate the in-situ reflectometers with acceptable accuracy. The detailed calibration procedure is described in Section IV-B. Multi-probe reflectometers with three (Chang, Li, & Sauter, 1990), four (Laemmle, Schmalz, Scheytt, Weigel, & Kissinger, 2013), and even hundreds (Philippe & Reynaert, 2019) of probes have been reported, but it has been shown (Mohamed & Kouki, 2019) that only two probes are sufficient if the incident power is known. To balance compactness and insertion loss, this work employs a four-port reflectometer.

Figure 5.6 shows the general configuration of the four-port reflectometer, where the output and the coupled ports are connected to an arbitrary unknown load and perfectly matched power detectors, respectively.

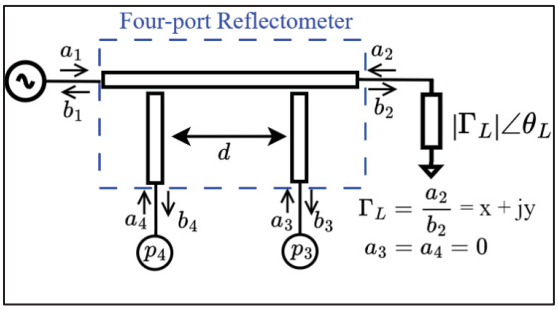

Figure 5.6 Four-port reflectometer configuration

The transmission coefficients between port 1 and ports 3 and 4, denoted as T_{31} and T_{41}, can be expressed using a signal flow graph as:

$$T_{31} = \frac{b_3}{a_1} = \frac{A_1\Gamma_L + B_1}{C\Gamma_L + D} \tag{5.1}$$

$$T_{41} = \frac{b_4}{a_1} = \frac{A_2\Gamma_L + B_2}{C\Gamma_L + D} \tag{5.2}$$

Where A_1, A_2, B_1, B_2, C and D are complex parameters that can be express as:

$$\begin{bmatrix} A_1 & A_2 \\ B_1 & B_2 \\ \mathrm{C} & D \end{bmatrix} = \begin{bmatrix} (S_{21}S_{32} - S_{31}S_{22}) & (S_{21}S_{42} - S_{41}S_{22}) \\ S_{31} & S_{41} \\ -S_{22} & 1 \end{bmatrix} \tag{5.3}$$

The detected powers at port 3 and 4 are related to the waves b_3 and b_4 as:

$$P_3 = \frac{|b_3|^2}{2} \tag{5.4}$$

$$P_4 = \frac{|b_4|^2}{2} \tag{5.5}$$

With using equations 1 to 5 we have:

$$P_3 = P_1 \left| \frac{A_1\Gamma_L + B_1}{C\Gamma_L + D} \right| \tag{5.6}$$

$$P_4 = P_1 \left| \frac{A_2\Gamma_L + B_2}{C\Gamma_L + D} \right| \tag{5.7}$$

Equations 6 and 7 can be expressed in terms of the real and imaginary parts of Γ_L, denoted by x and y, as follows:

$$(x - \alpha_3)^2 + (y - \beta_3)^2 = {r_3}^2 \tag{5.8}$$

$$(x - \alpha_4)^2 + (y - \beta_4)^2 = {r_4}^2 \tag{5.9}$$

The parameters α_3, β_3, α_4, β_4, r_3, and r_4 are derived from the values in equation 3. The intersection of the two circles defined in equations 8 and 9 yields the unknown Γ_L; however, two solutions may arise, one inside and one outside the Smith chart. If the probe spacing d is less than $\lambda/4$, only one valid solution lies inside the chart, avoiding ambiguity. While smaller spacing improves compactness, closely spaced probes are more sensitive to detector noise. To balance size and accuracy, a probe spacing of 45° ($\lambda/8$ at the highest frequency) was selected

for both reflectometers. For the LB design, a straight-line implementation is impractically large. To reduce size, the probe section is realized as a 3D embedded structure, similar to tuner implementations. Figure 5.7 and Figure 5.8 illustrates the 3D schematic of both LB and HB reflectometers, with EM full-wave simulations confirming electromagnetic performance. This approach reduces the LB reflectometer footprint by ~40%, yielding comparable dimensions for both designs. The measured insertion and return losses are better than 0.25 dB and 25 dB, respectively. Sampling is achieved using two buried strips beneath the main line (Orange traces), tuned to ~25 dB coupling, while a via-based quasi-coaxial transition minimizes reflections.

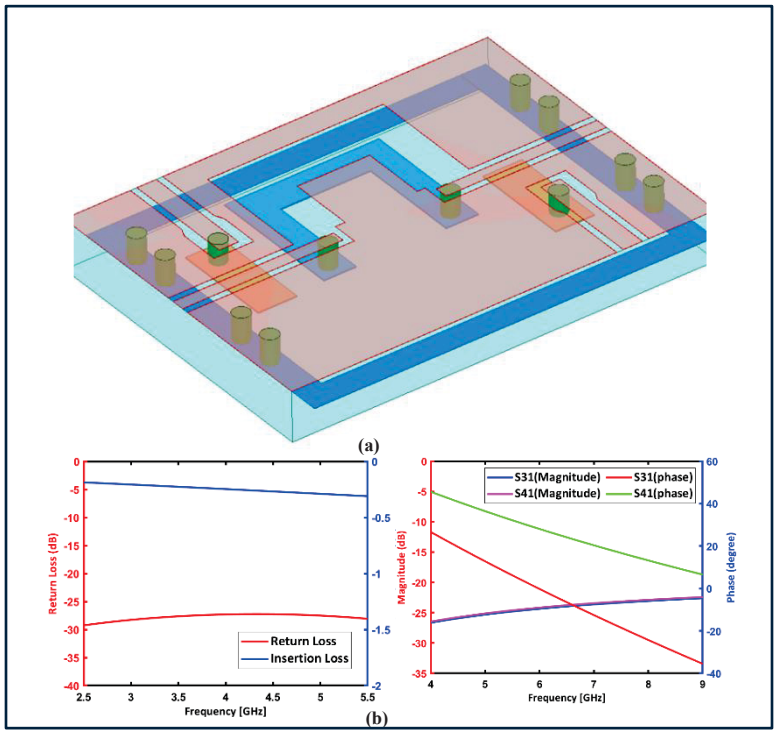

Figure 5.7 3D schematic of the LB sniffer, (b) Full wave simulations

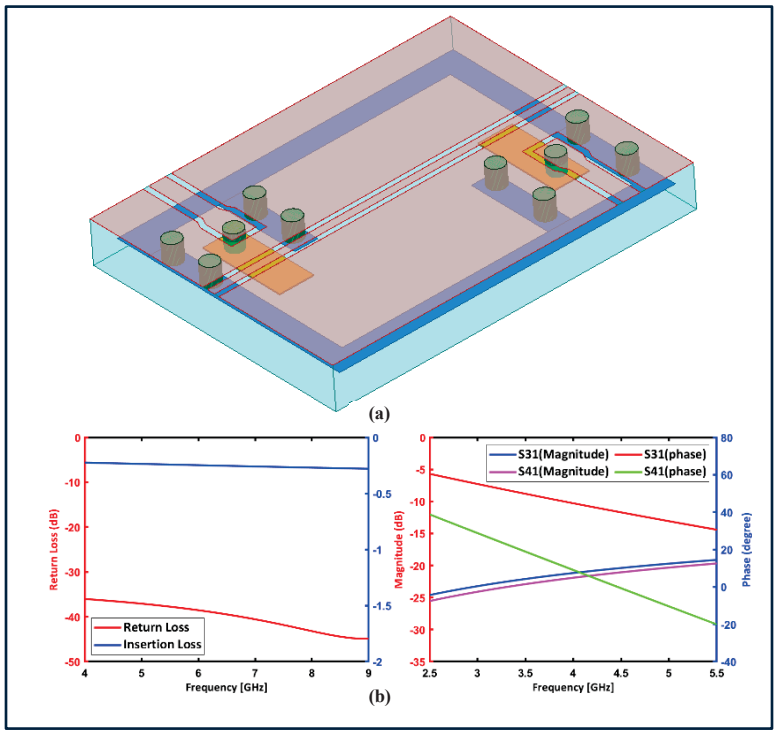

Figure 5.8 3D schematic of the HB sniffer, (b) Full wave simulations

5.3 Fabrication and integration process of FPMA

For FPMA fabrication using a monolithic LTCC-MEMS process, both MEMS and LTCC layout masks are produced together. The functional 3D-LTCC substrate is fabricated first using a standard LTCC process (E. Fallahnia & Kouki, 2023), with embedded DC/RF lines. Silver metallization is used for inner conductors and vias, except for the vias of the top layer which are filled with gold to avoid silver oxidation on the top layer. Next, the fabricated substrate is polished to a nanometer level surface finishing to be suitable for the MEMS fabrication phase. However, because the LTCC substrate goes through anisotropic shrinkage during the sintering step, the masks for the MEMS fabrication must be adjusted for perfect alignment with the final polished LTCC substrate. Once this step is completed, the MEMS process is carried out to fabricate the switches, CPW lines and DC pads. A 700 nm aluminum thin film is sputtered to

form the RF and DC lines and pads. This is followed by the deposition of a 200 nm AlN using reactive sputtering to form the dielectric layer of the capacitive switches. For the shunt MEMS membrane, a 1.4 µm thick sacrificial layer followed by a 1.5 µm of aluminum are sputtered. After lithography and etching of the aluminum the sample is dipped into a remover solution and subsequently transferred to Critical Point Dryer (CPD) machine for release. The final structure is a set of fixed-fixed capacitive switches suspended about 1.4 µm on top of the CPW line connected to the inner layers through vias. Figure 5.9 shows the fabricated 4×4 cm^2 LTCC tile where DMTL tuners, sniffers and complete FPMA circuits have been fabricated using 3 metallization layers on 4.5 mil sheets. Three 10 mil sheets were added for robustness.

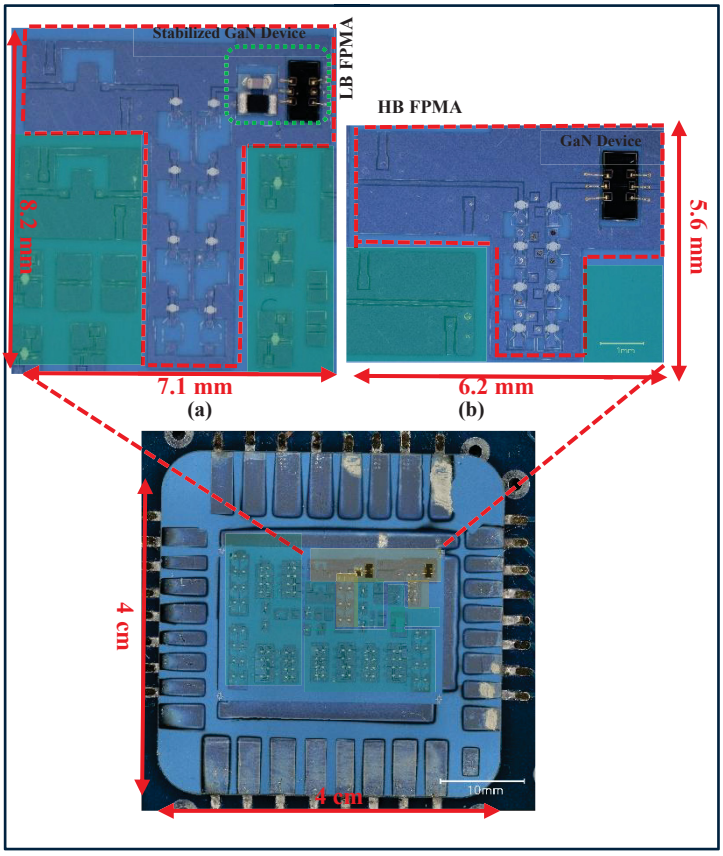

Figure 5.9 Fabricated FPMA for LB and HB, (a) LB and (b)HB design highlighted in yellow in the tile

In addition to the mentioned modules, the tile includes individual MEMS switches and single unit cells for validation (Figure 5.10).

After the monolithic process is carried out, GaN transistors (G28V4 MMIC) are mounted by wire bonding in the dedicated spots. Also, for the LB FPMA design, a parallel RC stabilizer network is added before the GaN device and is attached with silver epoxy to make the amplifier stable at low frequencies.

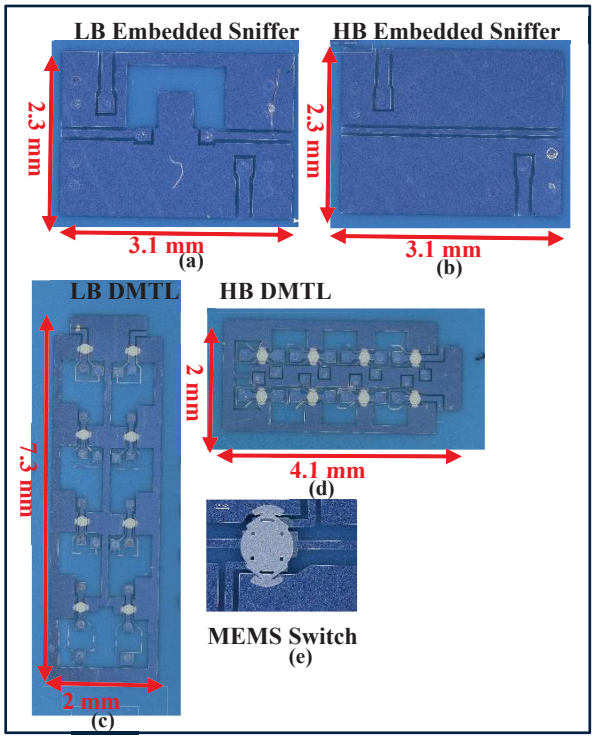

Figure 5.10 Single units for measurement validation highlighted in green area on the tile, (a) LB Sniffer, (b) HB Sniffer, (c) LB DMTL tuner, (d) HB DMTL tuner, (e) Capacitive MEMS switch

5.4 Measurement results of FPMA module and discussion

The fabricated LTCC tile is first mounted on a PCB board which is in turn connected to a driver circuit to control the actuation of each of the 8 switches independently in order to test all 256 tuner states as shown on Figure 5.11. RF measurements are then carried out using an on-wafer setup with PNA-X analyzer from 2 to 10 GHz after a standard SOLT calibration.

First for preliminary tests, individual switches were measured by stepping voltage from 0 to 30 V, for pull-in, and 30 to 10 and then to 0V, for lift-off. The measured capacitance for each switch is found to be around 125 to 836 fF at the up to down states, respectively, yielding a capacitance ratio of 6.7 which is lower than the simulation results and this is due to the roughness in capacitance area after MEMS process.

Measurement and results section for the whole FPMA is organized as follows: (i) two-port measurement of DMTL impedance tuners for LB and HB design, (ii) four-port measurements of sniffers and (iii) four-port measurements of the whole FPMA for s-parameters on matching locations and achieved gains in desired frequencies for both designs.

Figure 5.11 Fabricated LTCC tile mounted on control system PCB

5.4.1 Two-port measurements and results of DMTL impedance tuners

S-parameters and coverages for LB and HB tuners are obtained from DMTLs discrete units on the LTCC tile. Figure 5.12shows the measured insertion loss and return loss of the tuners when all switches are at up-state, and they are in good correlation with simulation results.

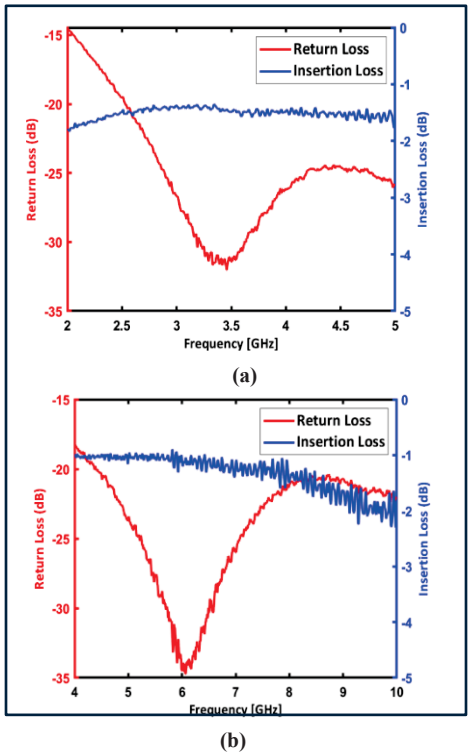

Figure 5.12. Measured S-parameters for (a) LB and (b) HB DMTL tuners

Degradation in insertion and return losses in the measurement results are due to several factors including: (i) surface oxidation of aluminum thin film, (ii) surface roughness of the sputtered metals and (iii) LTCC fabrication defects like minor misalignments, laser ablation and anisotropic shrinkages after co-firing process. Besides S-parameters results, obtained coverage areas for both LB and HB tuners from 3 to 5 GHz for LB and 5 to 8 GHz for HB tuners are shown. To assess the tuner's matching capability at a given frequency the return loss can be computed and plot in the Γ plane for each tuner setting with varying source impedance (Z_S) using (Domingue, Fouladi, Kouki, & Mansour, 2009):

$$Return\ Loss = MAX_i(-20log_{10}|\ \Gamma_{in}^{i}\ |) \tag{5.10}$$

where Γ_{in}^{i} is the input reflection coefficient of the tuner in its ith state corresponding to an input impedance of Z_{in}^{i}:

$$\Gamma_{in}^{i} = \frac{Z_{in}^{i} - Z_s}{Z_{in}^{i} + Z_s} \tag{5.11}$$

Figure 5.13 shows the achievable matching level over the entire Smith chart for the fabricated LB and HB tuners at different frequencies. LB tuner results are reported from 3GHz because of the stability of the transistor that is unconditionally stable from 3 GHz and higher frequencies. In addition, GaN device input impedance points are marked for each frequency on smith chart. While the coverage degrades as expected to be at lower frequency for each tuner (3 GHz for LB, 5 GHz for HB), tuners can still provide better than 20dB matching for the GaN device for all input impedances at designated frequencies and it is realized through tuning of the DMTL tuner's parameters.

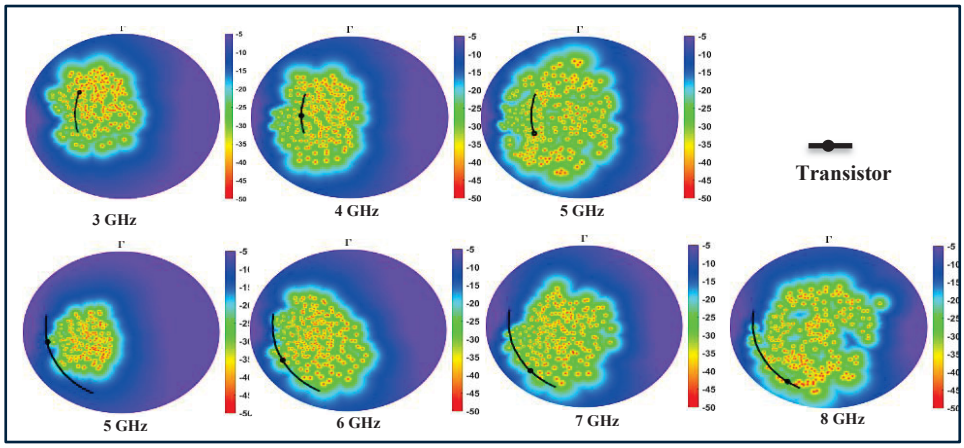

Figure 5.13 Measured smith chart coverages of LB and HB DMTLs

5.4.2 Four-port measurements and results of Sniffers

To measure Γ provided by tuners, the four-port reflectometers or sniffers are placed at input of the tuners. The third and fourth probes are connected to average power detectors, which are capable of measuring RF signals down to -35 dBm. Prior to measurement, the power detectors are calibrated to remove the effects of cables and adapters, ensuring accurate absolute power readings. Using the PNAx as both the RF source and for measuring Γ. The input power is set to 5 dBm so that the transistor operates at linear region. With the designed 25 dB coupling of the reflectometers, the detected power levels remain within the operating range of the detectors.

To evaluate the performance of the designed four-port reflectometers, we fabricated stand-alone versions for both the LB and HB bands, ensuring they were isolated from any other devices on the same substrate. Figure 5.14 shows the measured S-parameters of these stand-alone reflectometers. Compared with the simulated results in Figure 5.7 and Figure 5.8, the phases of S31 and S41 exhibit good agreement, while small discrepancies are observed in the coupling values. These differences are likely caused by non-idealities in the LTCC fabrication process, such as slight misalignments between the coupling strips and the main transmission line, which affect coupling strength. Although these deviations are minor, the measured S-parameters of the stand-alone reflectometers are used to characterize the in-situ reflectometers to enhance the measurement accuracy.

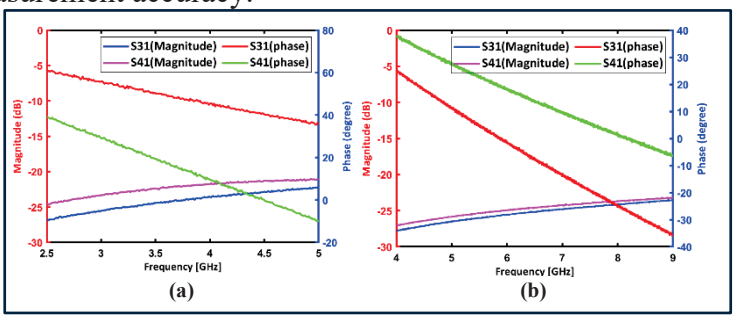

Figure 5.14 Measured S-parameter of (a) HB reflectometer (b) LB reflectometer

5.4.3 Four-port measurements and results of FPMA

To measure the performance of FPMA module, Embedded sniffer, LB/HB DMTL and stabilized transistor device are cascaded together with buried RF and DC control in 3D functional LTCC substrate. the GaN device is first biased with V_{ds} = 28V and I_{ds} = 20 mA. Device is unconditionally stabilized with a parallel RC circuit (R=50 Ω, C=1 pF) from 3 GHz to 5GHz for LB and no stabilization network is needed for HB as the device is stable from 5 GHz. Regarding these conditions, and using PNAx, a four-port calibration is performed from 3 to 8 GHz using four GSG probes for input of the sniffer, output of the transistor and two other ports for couplings of the sniffer. Seven frequency points are selected and maximum stable gain (G_{MAX}) with its related return loss to illustrate matching performance is reported.

Since load gain (G_L) values are much lower than source gain (G_S), for this measurement, impedance tuning using DMTL is only performed at input of the device and total maximum stable gain is reported based on the sum of transistor S21 and G_S. In order to maximize the gain which corresponds to maximum input matching, G_S, sweeping for all 256 combinations of MEMS switches are performed. The reflection coefficient (Γ) at the input of the tuners is measured using both the VNA and the embedded four-port reflectometer, as shown in Figure 5.15. For each DMTL design, a representative frequency is selected: 4 GHz for LB and 7 GHz for HB. Since the VNA and the embedded reflectometer do not share the same reference plane, the VNA-measured Γ is de-embedded using the reflectometer's S-parameters. Based on Figure 5.15, three VSWR zones are defined to show accuracy of the sniffer's detection. for LB design, a 1.74 VSWR value for up to 5% Γ detection error, up to 15% within 1.74 and 3.55 and more than 25% for 3.55 and more VSWR values and for HB design, a 1.95 VSWR value for up to 5% Γ detection error, up to 15% within 1.95 and 4.3 and more than 25% for 4.3 and more VSWR values are achieved.

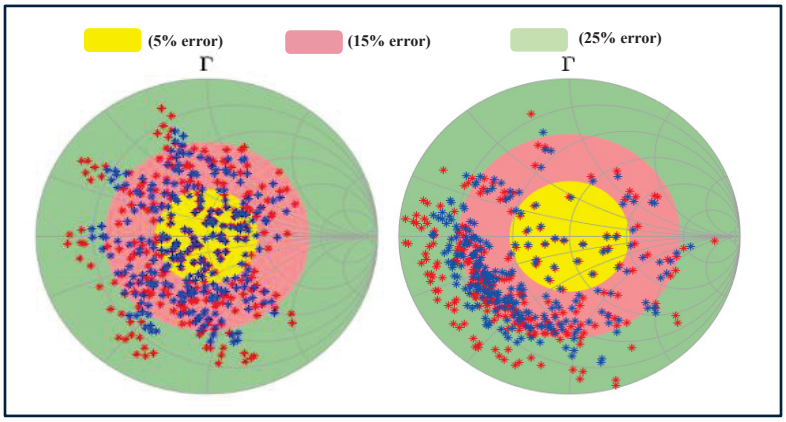

Figure 5.15 Measured Gamma seen from tuner: VNA (blue) vs sniffer (red), 4GHz for LB (left) and 7GHz for HB (right)

Results demonstrate good agreement between the two methods for the loads in yellow and pink areas, while noticeable deviations appear in green area. These deviations are attributed to differences between the in-situ and stand-alone reflectometers performance caused by LTCC fabrication defectives. Since in this work we only focus on smallest VSWR values (yellow area) representing matched load, the employed calibration technique is quite acceptable. The

same procedure is applied to the rest of the desired frequencies and for all of them, yellow VSWR area Γ points are in correlation with reported values with less than 5% error detection. Therefore, by employing sniffers we could find the best switches combinations. For both designs and based on the matching areas on Figure 5.13, measured S11 and G_{MAX} of the device is shown in Figure 5.16. As is shown on Figure 5.16(a), for LB design, three different combinations of MEMS switch yield to perfect matching and maximum stable gains while for HB design (Figure 5.16(b)), four combinations are available. Combinations include switches that are actuated. Although perfect matching well below 20 dB is available for all matching points it was not possible for all points to reach the maximum stable gain. The reason lies behind the fact that the whole system is not lossless, and the sum of dielectric and conductor loss of the structure leads to 1 to 2 dB loss for the entire band.

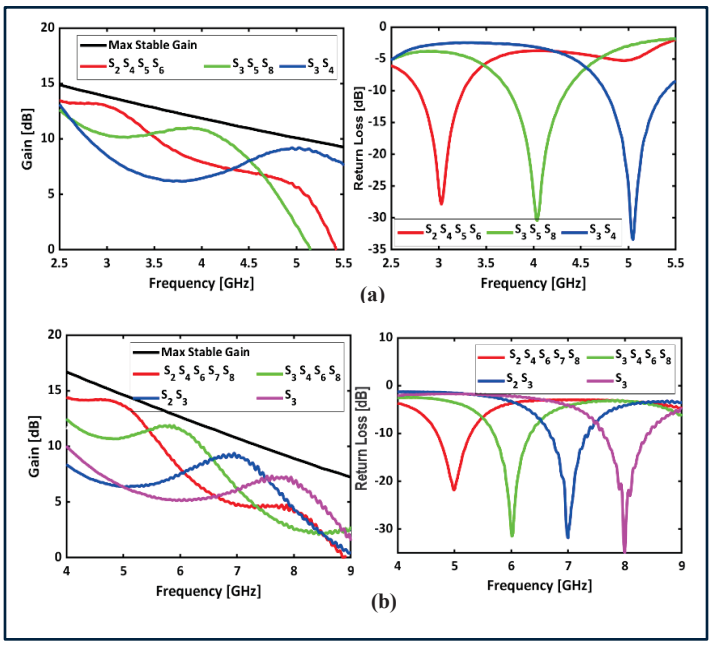

Figure 5.16 Maximum stable gains and return loss of (a)LB and (b)HB designs

As shown on Table 5.2, current work is compared to other reconfigurable amplifiers using either RF-MEMS tuners, fluidic tuners or semiconductor ones with different configurations. In (Domingue, Kouki, et al., 2009), a discrete reconfigurable amplifier using DMTL tuner is introduced. While it covers a wideband and keeps the footprint small because of smaller

transistor device and the lack of sniffers, the cascading of amplifier and DMTL is done through simulation and combinations of switches to achieve maximum stable gains are done manually. In (Bahloul & Kouki, 2020), a reconfigurable tuner using water filled cavities are using inside the LTCC. While a wide coverage is achieved in lower frequencies, the dimension of the whole distributed tuner is considerably high and tuning using fluidic cells are performed manually. In (Morishita et al., 2015) , a stub tuning impedance matching using MEMS switches are reported. Tuning is achieved through liquid metal capabilities by resizing stubs to achieve required matching for each frequency. While the wide band is achieved, still the dimension of the whole module is quite high, and the circuit is fabricated on a PCB by creating etched holes for liquid metal to enter and is actuated with the required voltage to form a stub for tuning. In (Gilasgar, Barlabé, & Pradell, 2020) , a tunable Power Amplifier (PA) using RF-MEMS switches are introduced. The proposed design covers narrow band (900/1800 MHz) and the whole module is large compared to DMTL designs. Impedance tuning is also performed manually to achieve required gain. In (Fontana, Cheng, & Psychogiou, 2025) a narrow band design using varactor-loaded capacitors on a PCB for a reconfigurable Low Noise Amplifier (LNA) is introduced. The design covers a limited band using tunable filters, requires mounting and assembly of switches on a PCB and occupies considerable space. Compared to the mentioned works, proposed designs in this work are fabricated through a monolithic LTCC-MEMS process to avoid further assembly. The reconfigurability is performed using embedded reflectometer sniffers and the whole module dimension is kept small compared to similar works. Designs in this work can be further reconfigured in more frequency bands with enhanced miniaturization using inner LTCC layers with matched vertical transitions.

Table 5.2. Comparison of other works reported in literature with current work

Works	Process of integration	Tuner design	Mode of tuning	module Size (mm^3)	Frequency(coverage)
(Domingue, Kouki, et al., 2009)	Surface microfabrication on alumina	DMTL	Manual	5.75×1×0.5	3.5 – 7 GHz (Wide)
(Bahloul & Kouki, 2020)	Fluid cells on LTCC	Distributed cavity cells	Manual	26×10×1.5	0.9 – 2.4 GHz (Wide)
(Morishita et al., 2015)	Liquid Metal on PCB	Stub	Manual	135×35×0.7	3.3 – 6 GHz (Wide)
(Gilasgar et al., 2020)	Mounting RF-MEMS on PCB	Stub	Manual	71.6×112×1.5	900/1800 MHz (Narrow)
(Fontana et al., 2025)	Mounted varactors on PCB	Varactor-loaded filters	Manual	53.9×45.15×1.57	2.65-3.25 GHz (Narrow)
This Work (LB)	**Monolithic LTCC-MEMS**	**DMTL**	**Automated through Sniffer detection**	**7.1×8.2×1**	**3 – 5 GHz (Wide)**
This Work (HB)	**Monolithic LTCC-MEMS**	**DMTL**	**Automated through Sniffer detection**	**5.6×6.2×1**	**5 – 8 GHz (Wide)**

5.5 Conclusion

With the advantages of a novel monolithic LTCC-MEMS process, a field programmable microwave amplifier is designed, fabricated and measured for its impedance matching performance over a wide band in two different lower and higher bands. Using inner layers of LTCC as a 3D functional substrate, and fabricating RF-MEMS DMTL tuners at the surface, a variety of miniaturized impedance tuners are developed. By embedding a reflectometer sniffer at the input of the DMTL which is cascaded to a transistor, optimum Γ points are detected and sent to MEMS switch control units to determine the best actuation combinations for impedance matching. Excellent matching capability using programmable DMTL tuners are achieved to reach maximum stable gain for the entire bands of operation. Compared to other works,

proposed designs benefit from an automated impedance tuning while whole module dimension is kept small. Level of reconfigurability and module dimensions, simply could be changed based on the leverage of the inner layers of the LTCC as a reproducible design based on its application.

CONCLUSIONS AND RECOMMENDATIONS

In this Thesis, which is divided into different published papers, different aspects of LTCC technology, its integration with RF-MEMS technology through a novel monolithic process, and the final goal of the thesis, which is designing a FPMA, is thoroughly detailed. In the first section a comprehensive literature review is done to familiarize the idea of reconfigurable microwave devices and specially amplifiers and the demand for them for wireless communications is explained. Shortcoming of the several reported works as a problem statement, made new objectives for the current thesis to design a novel FPMA using RF-MEMS and LTCC technology. In the second section, a novel monolithic process is introduced which enables the fabrication of MEMS devices on functional 3D dense LTCC substrates and pave the way for the ultimate design of the thesis. In the third section, in a review paper, a complete review of MEMS application in ceramics technology from different aspects are studied to give a clearer idea of how MEMS and ceramics can be integrated for novel sub-circuits and systems which are able to be reconfigured and reprogrammed as hardware. In section four, a simple application of functional LTCC substrate is demonstrated. An embedded miniaturized novel dual sided bias-tee is introduced. The device can be fabricated monolithically with MEMS sensors or as a package which a MEMS device can be mounted on it. this design is perfectly appropriate for MEMS wireless sensors which need bias-tees as embedded units to avoid using commercial bulky bias-tees. After all these works, in the last section, which is the main objective of the thesis, a FPMA using monolithic LTCC-MEMS process is introduced and detailed. Two different designs in different frequency bands are proposed and frequency tuning ability using embedded DMTLs, embedded sniffer reflectometers and a GaN device is reported. Comparing to the other works reported in the literature, the FPMA designs, are able to be continuously reprogrammed using the detection of embedded sniffers and different combinations of 8-bit DMTLs.

From this design and final results, a reproducible process flow is disclosed, and it can be applied to a variety of microwave reconfigurable systems with miniaturized footprints and wide-band operation with a single hardware without the need to a redundant circuit.

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